



 <div> <div>QUANTA</div> <div>COMPUTER</div> </div>			
Title			
BLOCK DIAGRAM			
Size	Document Number	Rev	
	Calpella	3A	
Date:	Thursday, August 20, 2009	Sheet	1 of 61

Table of Contents

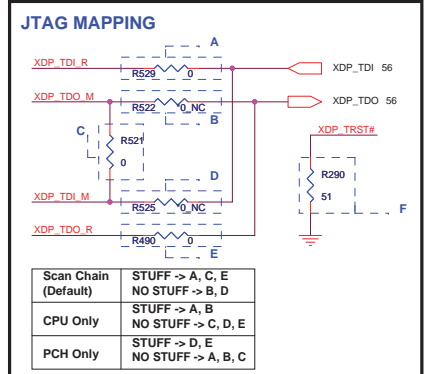
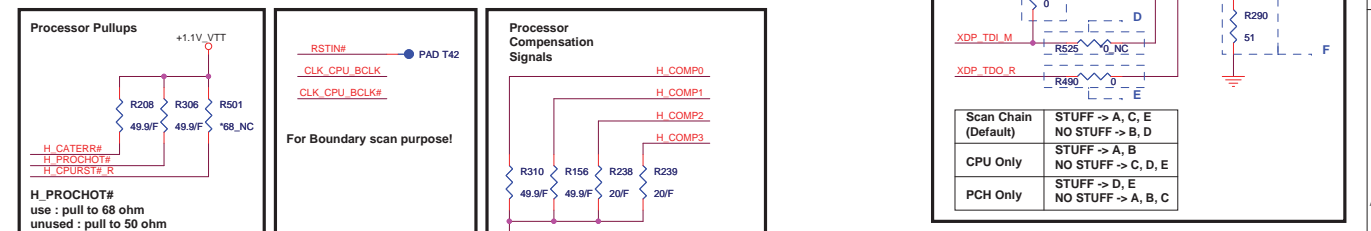
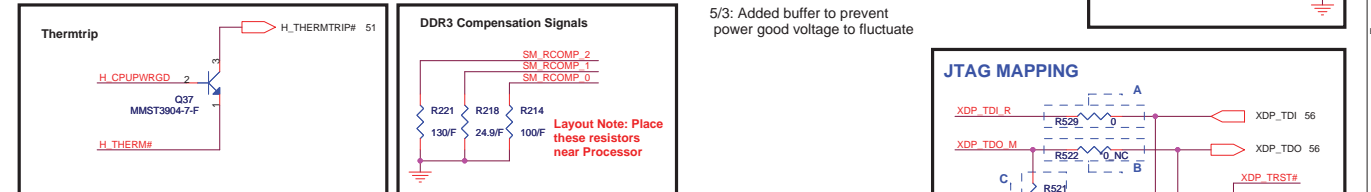
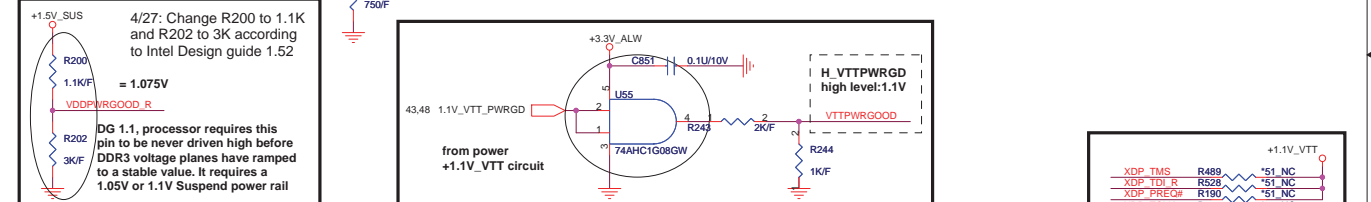
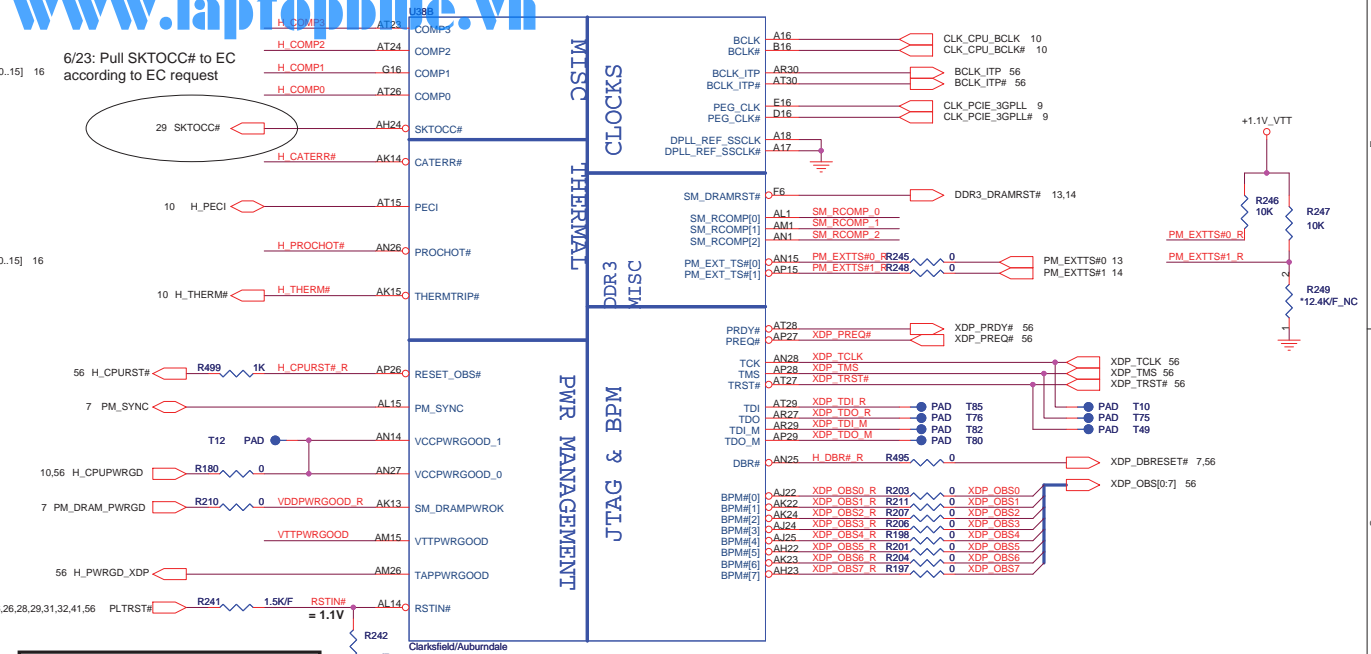
PAGE	DESCRIPTION
1	Block Diagram
2	Front Page
3-6	CPU (Clarksfield)
7-12	PCH (IBex Peak-M)
13-14	DDR3 SO-DIMM(204P)
15	Clock Generator
16-22	GPU (M96XT)
23	HDMI & DP
24	LCD connector
25	CRT
26	Card reader PCIe interface
27	Card reader & 1394 CONN
28	Express card
29	SIO (IT8512)
30	Flash/RTC/CIR
31	WLAN
32	WWAN/WPAN
33	USB & eSATA & TV
34	SATA HDD & ODD
35	KB/CCD/UI
36	LED
37	FAN/Thermal
38-40	Audio/CONN/Subwoofer (92HD73C).
41-42	LAN/RJ45 (BCM5784M)
43	System Reset Circuit
44	PAD & SCREW & SPRING
45	CHARGER (MAX8731A)
46	1.8V_RUN (TPS51218)
47	1.5_SUS/0.75(TPS51116)
48	1.1V_VTT(TPS51218)
49	1.05V_PCH (TPS51218)
50	VCC_CORE(MAX17036GTL+)
51	3.3V/5V/15V (MAX17020)
52	VGA_M97(MAX8792)
53	VDDCI_M97(TPS51218)
54	Run Power Switch
55	DCIN & Batt
56	XDP Connector
57	Power Block Diagram
58	SMBUS BLOCK
59	Power status

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51,52,53	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	8,11,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	3,29,30,34,35,36,43,45,51,54,55	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	24,33,34,35,47,51,52,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	24,34,51,54	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	41,42	LAN POWER	AUX_ON	
+5V_SUS	+5V	11,46,48,49,52,53,54	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,8,9,10,11,20,24,28,29,42,43,46,47,48,49,52,53,54	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.5V_SUS	+1.5V	3,5,13,14,47,52,54	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,54	SODIMM POWER	SUS_ON	
+5V_RUN	+5V	11,18,23,25,33,35,36,37,38,50,54	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	7,8,9,10,11,13,14,15,18,23,24,26,28,29,30,31,32,33,34,35,36,37,38,39,40,41,50,52,54,56	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	5,11,17,18,19,46,54	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	28,31,32,54	PCH POWER	1.5V_RUN_ON	
+1.1V_VTT	+1.1V	3,5,10,11,48,50,56	CPU POWER	RUN_ON	
+1.05V_PCH	+1.05V	8,9,11,15,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.5V	5,50	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	34	Module Power	MODC_EN#	
+5V_HDD	+5V	34	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	35,36,51,54,55	LED power source	LDO output	

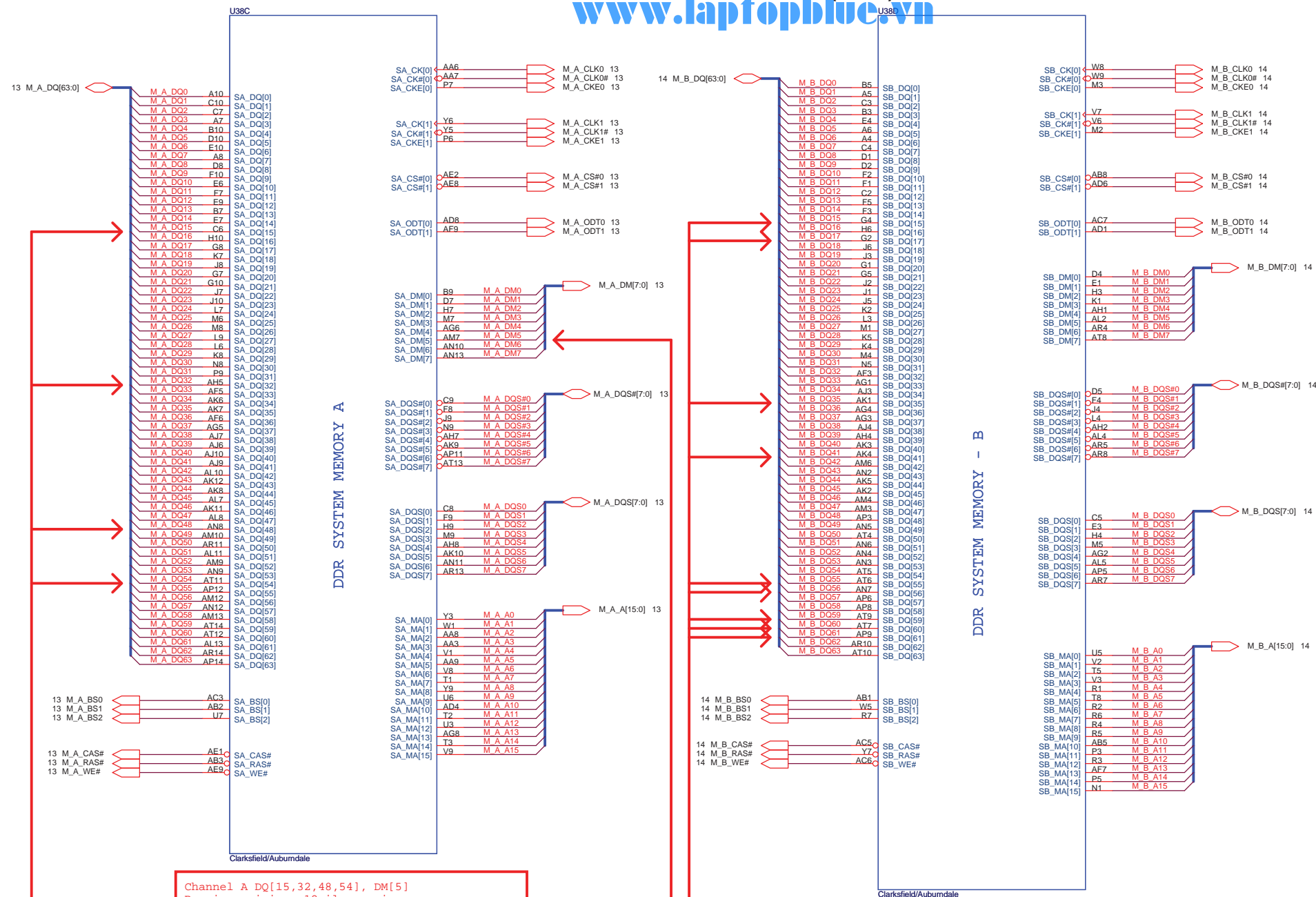
GND PLANE	PAGE	DESCRIPTION
 AGND	38,39,40	
 AGND_DC/DC	51	
 AGND_VCORE	50	
 GND	ALL	

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



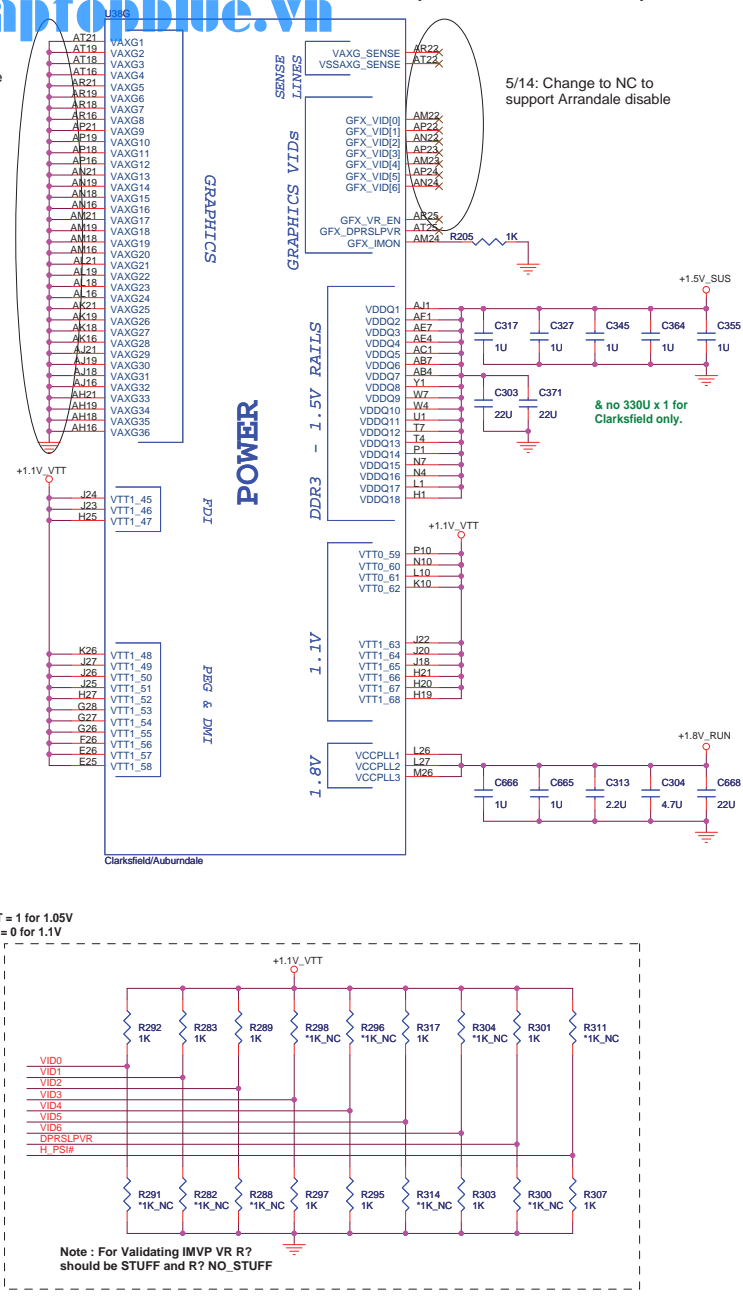
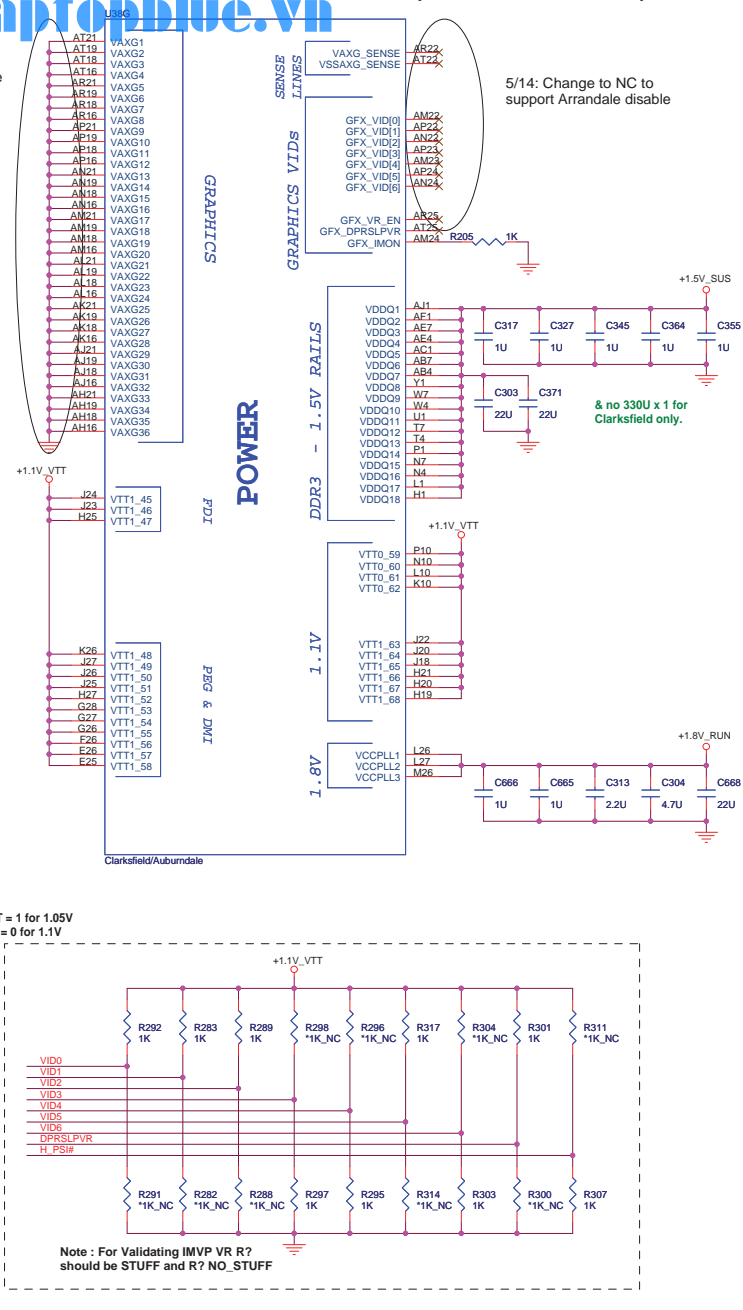
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)


www.lapfopblue.vn

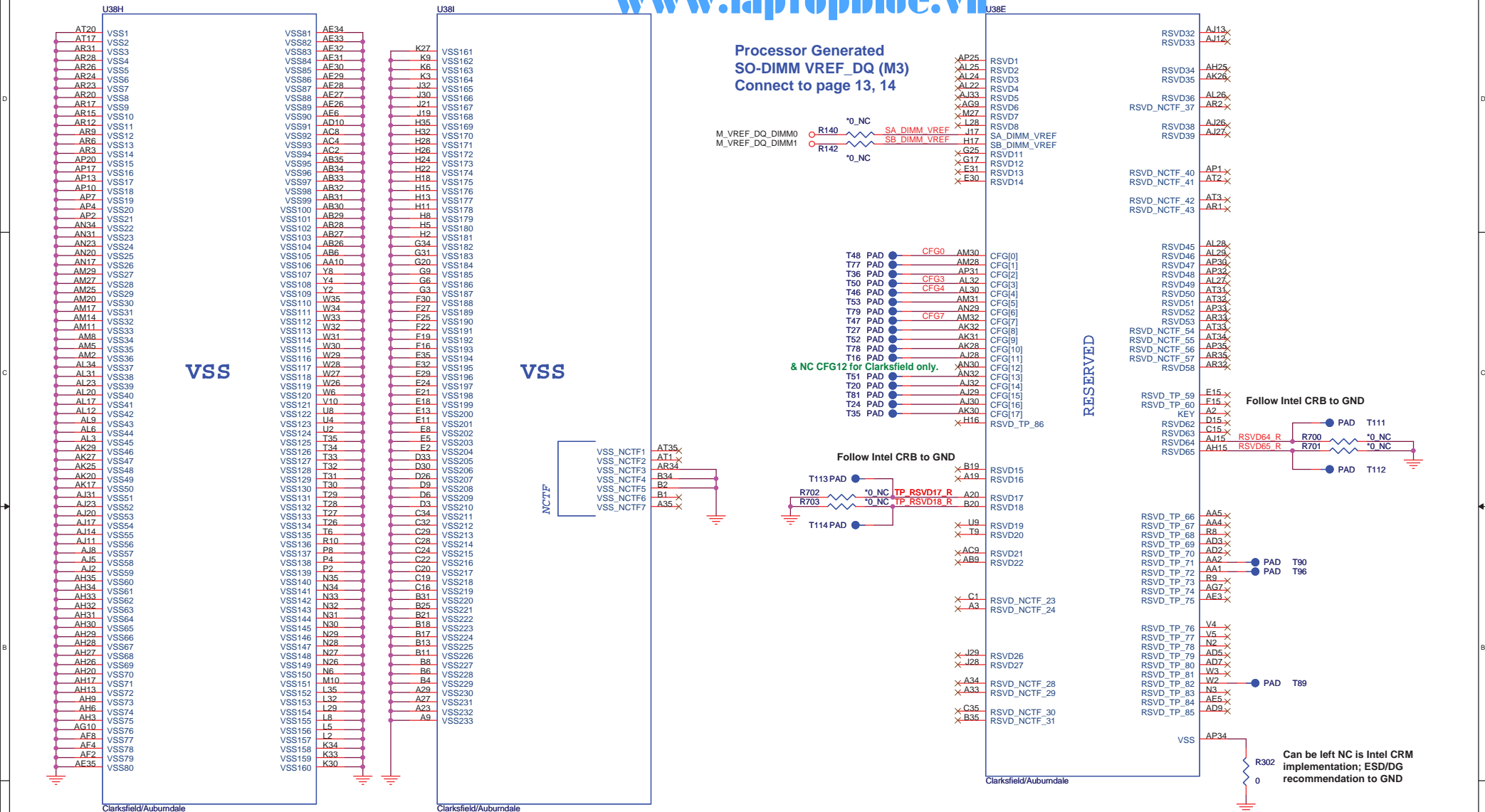


Title			CPU 2/4(DDR)
Size	Document Number	Rev	
	RM5	3A	
Date:	Thursday, August 20, 2009	Sheet	4 of 61

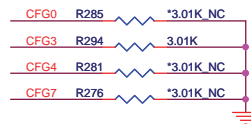
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



 <div> <div>QUANTA</div> <div>COMPUTER</div> </div>			
Title			
CPU 3/4(POWER)			
Size	Document Number		Rev
	RMS		3A
Date:	Thursday, August 20, 2009	Sheet 5 of 61	



Scott_0630:Change R294 footprint from RC0402-C to RC0402



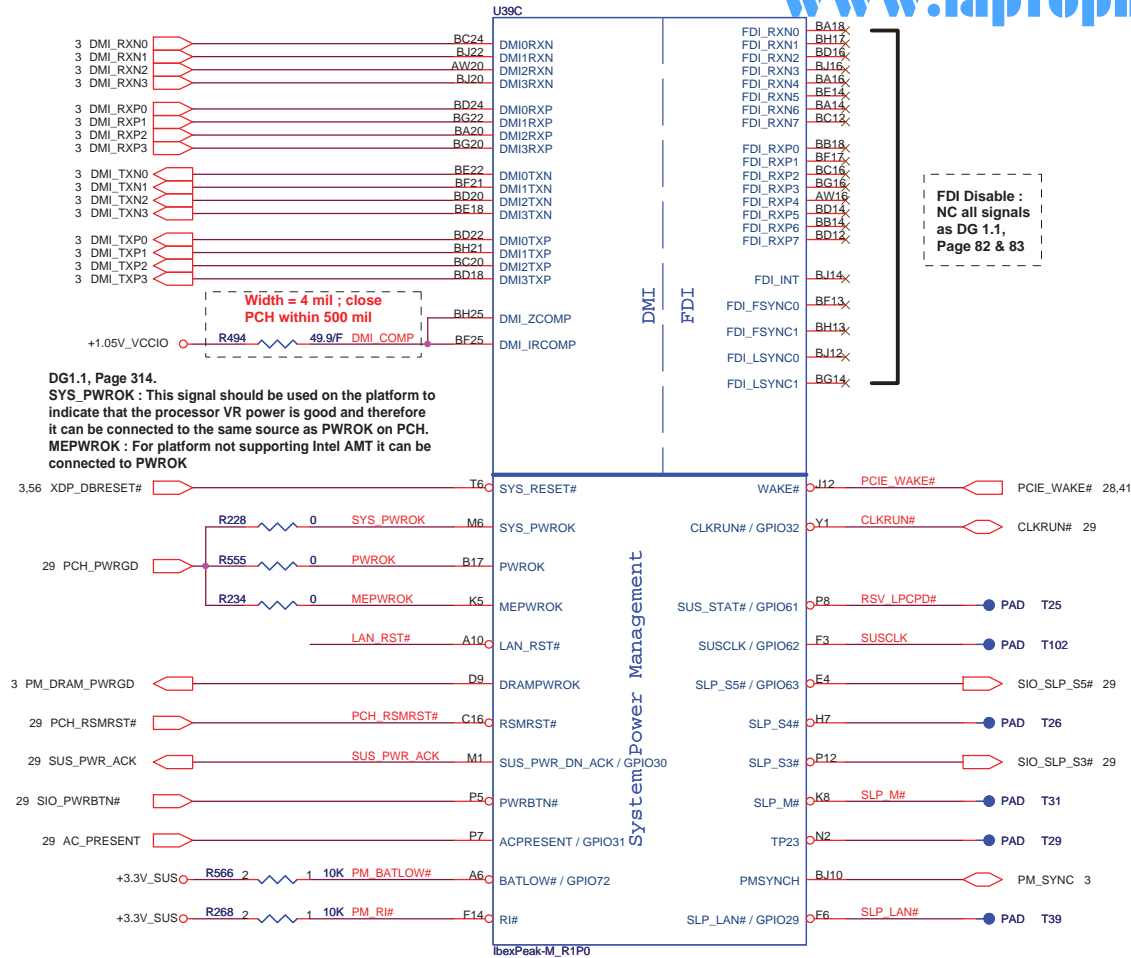
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG0 (PCI-Epress Configuration Select)	Single PEG (Default)	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation (Default)	Lane Numbers Reversed
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port (Default)	Enabled; An external Display port device is connected to the Embedded Display port
CFG7 Clarkfield (only for early samples pre-ES1)	Common motherboard design	For early samples pre-ES1 CFD (Default)



IBEX PEAK-M (DMI,FDI,GPIO)

www.laptopblue.vn

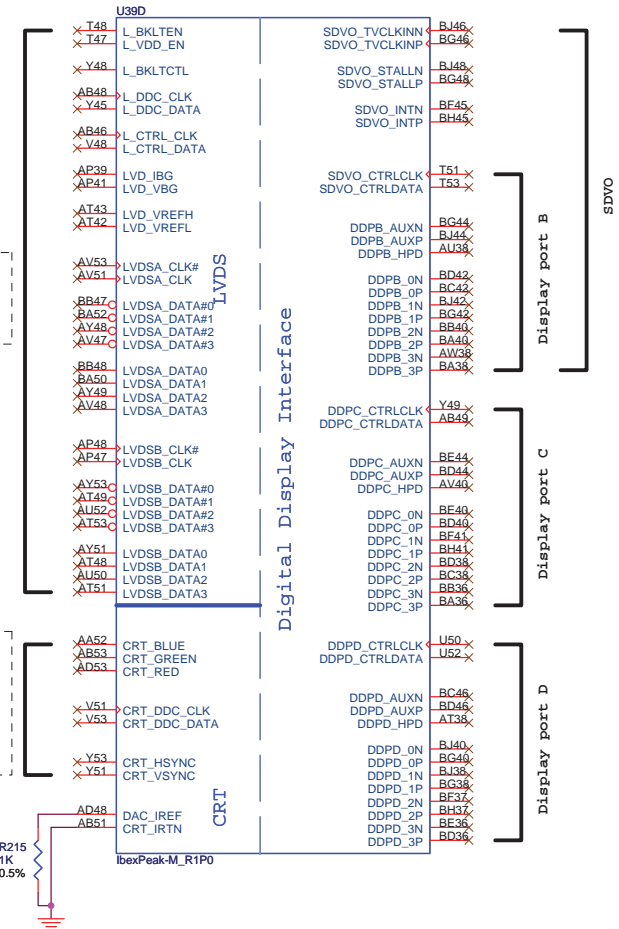


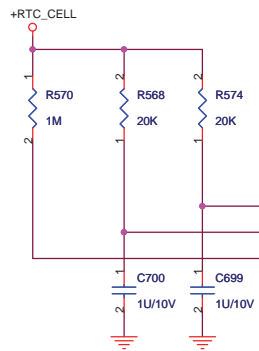
FDI Disable :
NC all signals
as DG 1.1,
Page 82 & 83

LVDS Disable :
All signals associated
with the interface can
be left as No connects.

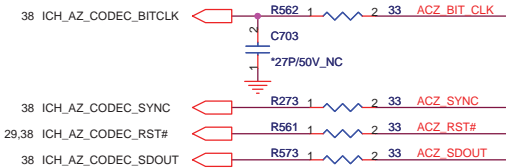
CRT Disable :
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_HSYCN
CRT_VSYNC
Leave as NC (floating).

IBEX PEAK-M (LVDS,DDI)





INTVRMEN (Internal Voltage Regulator Enable) :
This signal enables the internal 1.05 V regulators.
This signal must be always pulled-up to VccRTC.

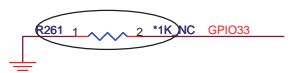
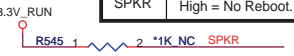


Place all series terms close to PCH (within 500 mil) except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

No Reboot strap.

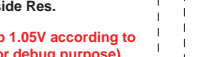
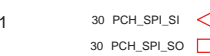
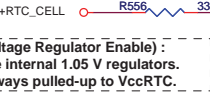
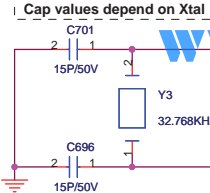
SPKR Low = Default.
High = No Reboot.

Scott_0630: Change R545 footprint from RC0402-C to RC0402.



Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.

6/2: Change R261 from 10K_NC to 1K_NC according to Intel design guide 1.51



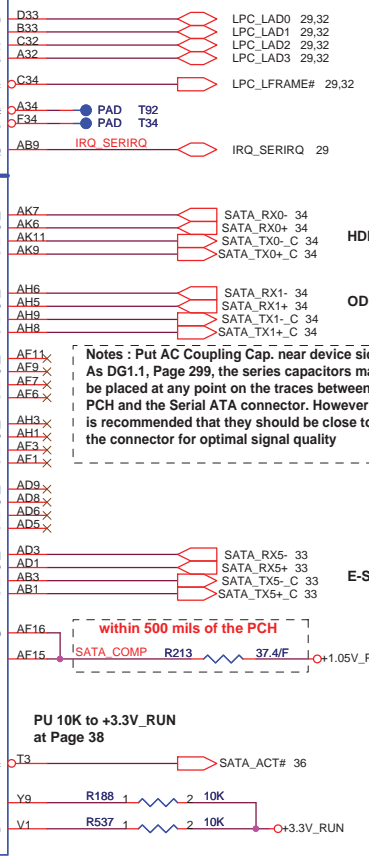
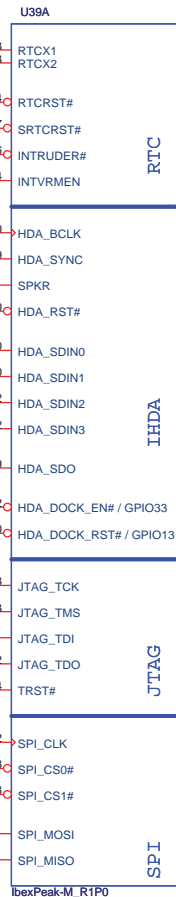
Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

Scott_0703 : Note : Delete pull up 1.05V according to Intel change notice! (Reserved for debug purpose)

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

Scott_0707: Reserver PCH_JTAG_RST# circuit as review.

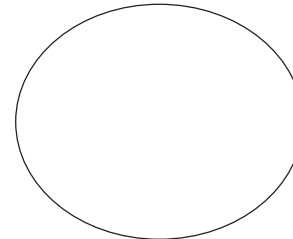


Notes : Put AC Coupling Cap. near device side. As DG1.1, Page 299, the series capacitors may be placed at any point on the traces between PCH and the Serial ATA connector. However, it is recommended that they should be close to the connector for optimal signal quality

Notes : FIS-based Port Multiplier support on SATA Ports 4 and 5 in AHCI/RAID mode.

within 500 mils of the PCH
SATA_COMP R213 37.4/F +1.05V_PCH

PU 10K to +3.3V_RUN at Page 38



QUANTA COMPUTER

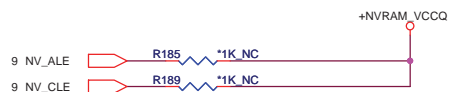
Title PCH 2/6(SATA_SPI)		
Size RM5	Document Number	Rev 3A
Date: Thursday, August 20, 2009	Sheet 8	of 61

IBEX PEAK-M (GPIO, VSS, NCTF, RSVD)

www.laptopblue.vn



Note : TP3 is not part of the JTAG interface, but is required to select the Boundary Scan test mode.



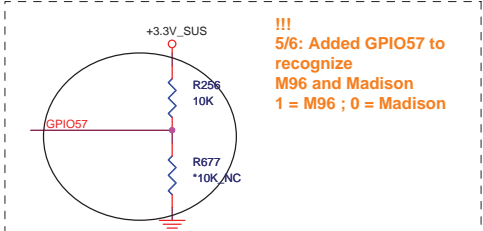
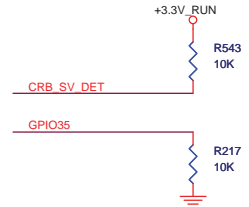
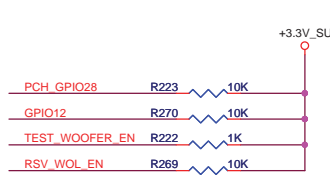
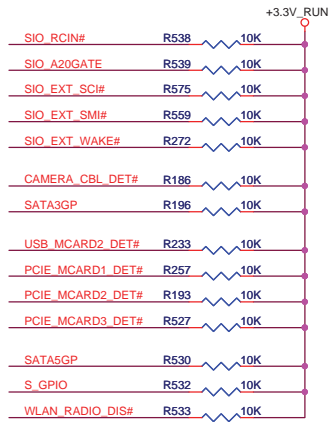
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Anti-Theft Enabled	
NV_ALE	High = Enable (Default) Low = Disable

2/12: Peter: According to checklist, default is set to low for disabling anti-theif!

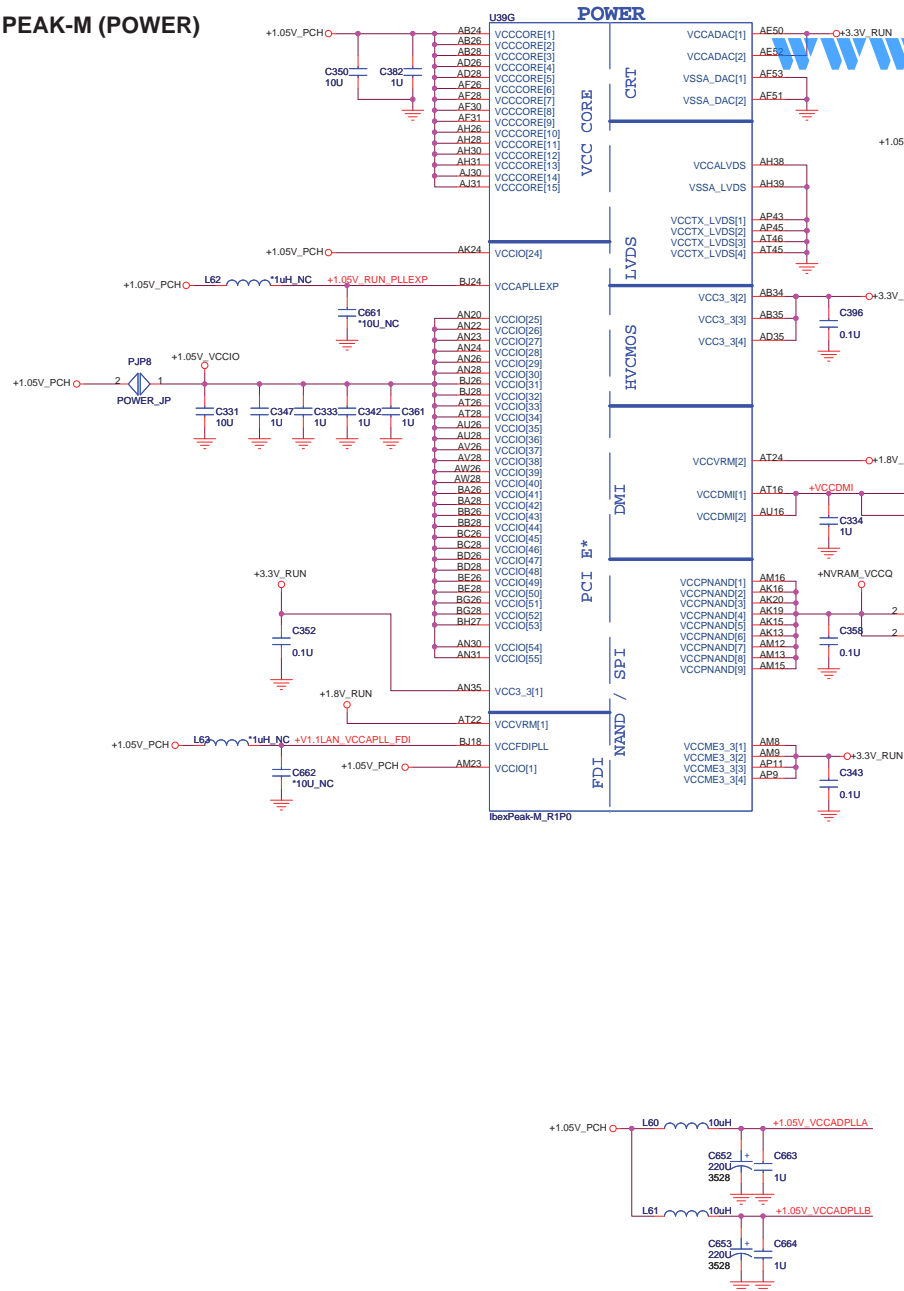


SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

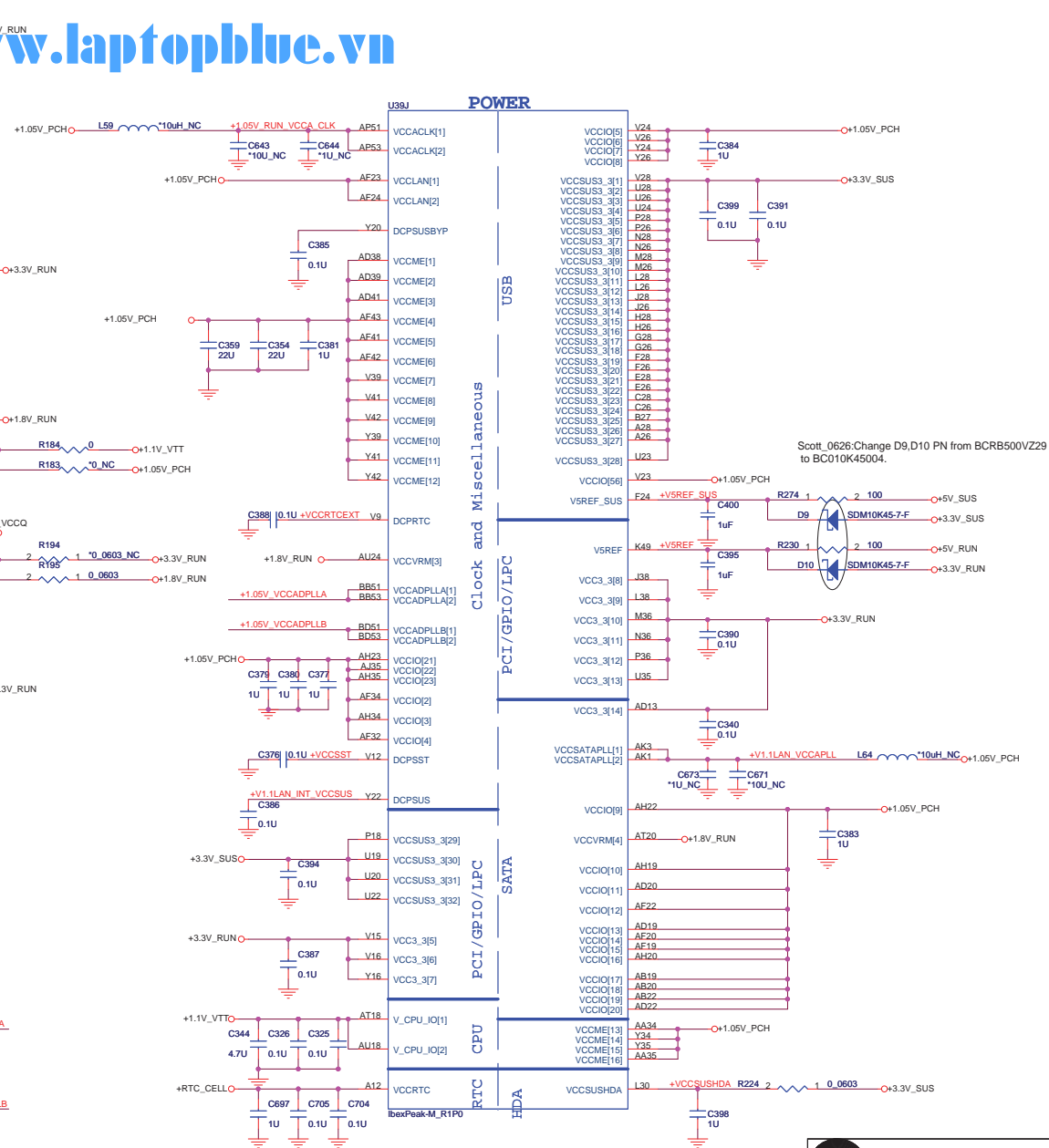


!!!
5/6: Added GPIO57 to recognize M96 and Madison
1 = M96 ; 0 = Madison

IBEX PEAK-M (POWER)



Use External Graphics. Can connect power directly without Inductor & Cap ? As Ibex peak-M EDS 1.0, need +1.05V. Can use +1.1V_VTT as CPU ?



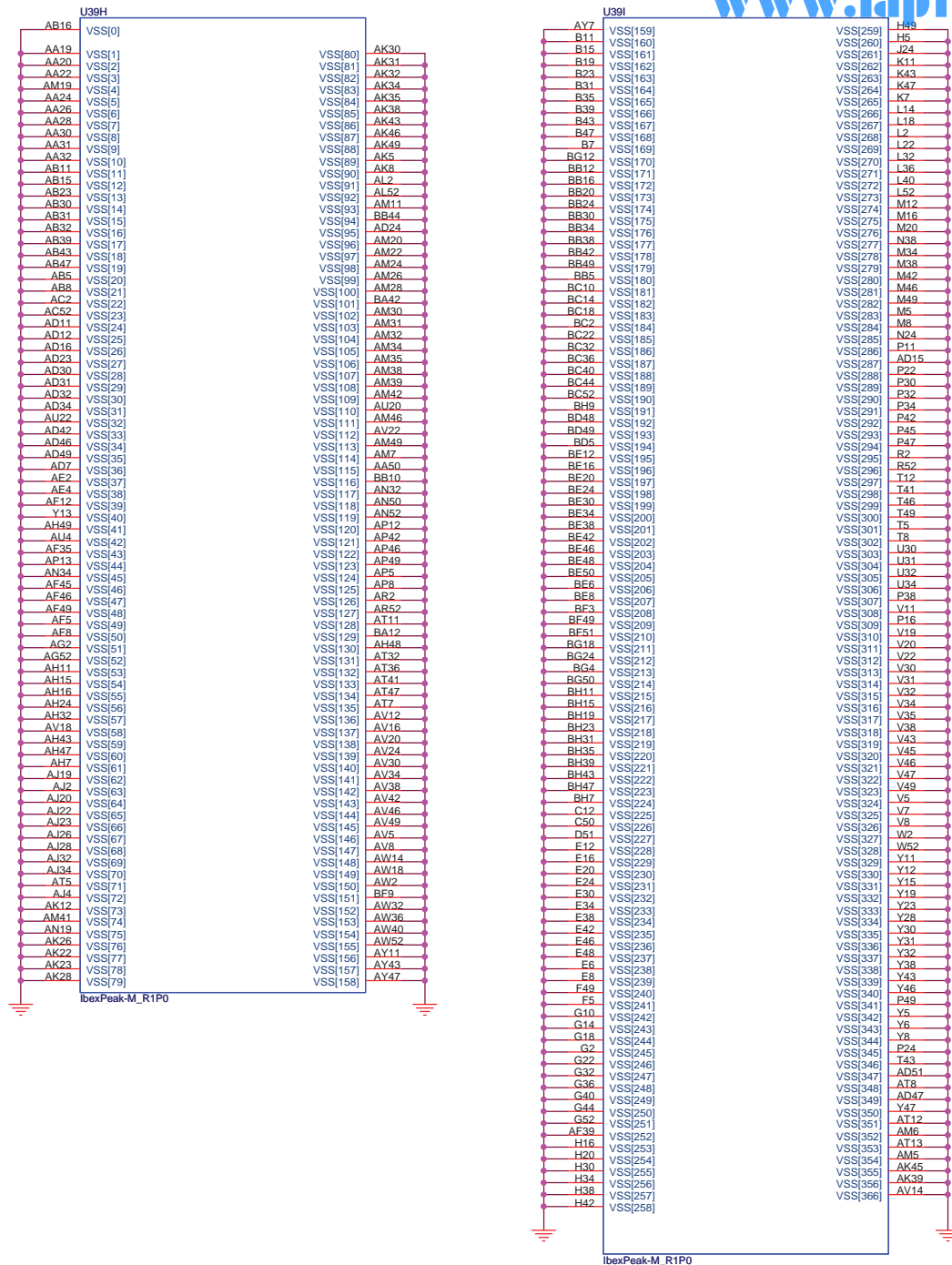
Title PCH 5/6(POWER)

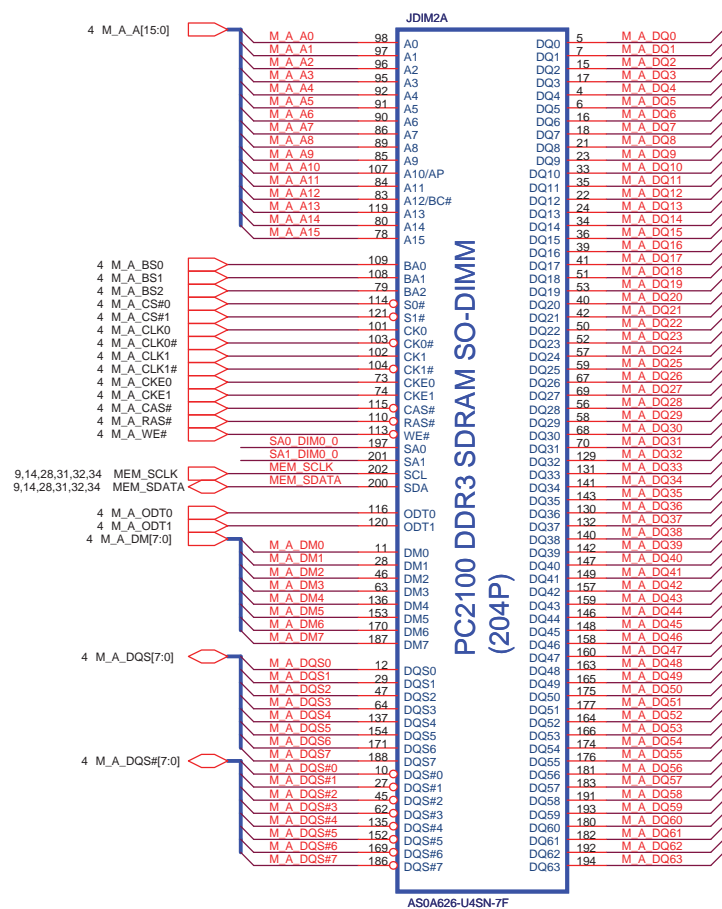
Size	Document Number RM5
------	------------------------

Date: Thursday, August 20, 2009 Sheet 11 of 61

IBEX PEAK-M (GND)

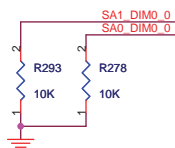
www.laptopblue.vn





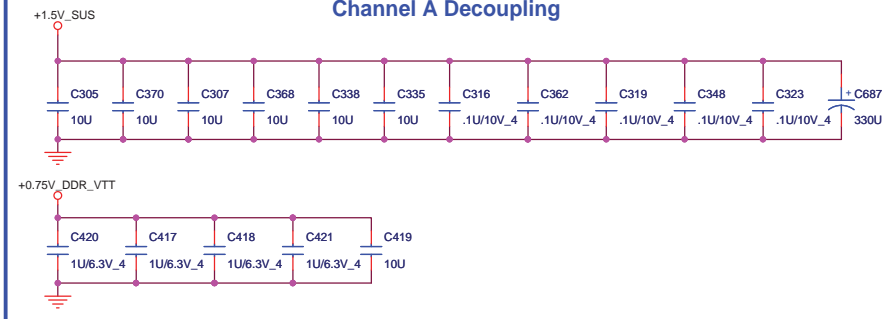
PC2100 DDR3 SDRAM SO-DIMM
(204P)

AS0A626-U4SN-7F



Note:
If SA1_DIM0 = 0, SA0_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA1_DIM0 = 0, SA0_DIM0 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Channel A Decoupling



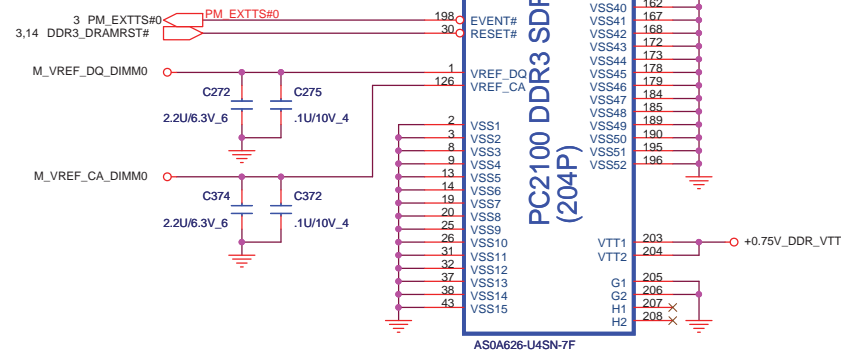
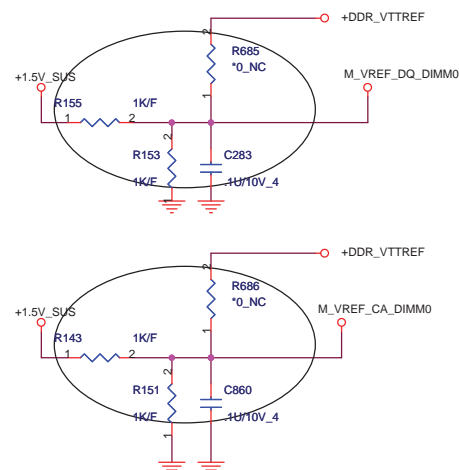
For CH A SO-DIMM VREF_DQ for M2

Delete according to Intel Design Change

M1 VREF

5/18: Separate voltage divider for M_VREF_DQ_DIMM0 and M_VREF_CA_DIMM0 to follow Intel CRB design

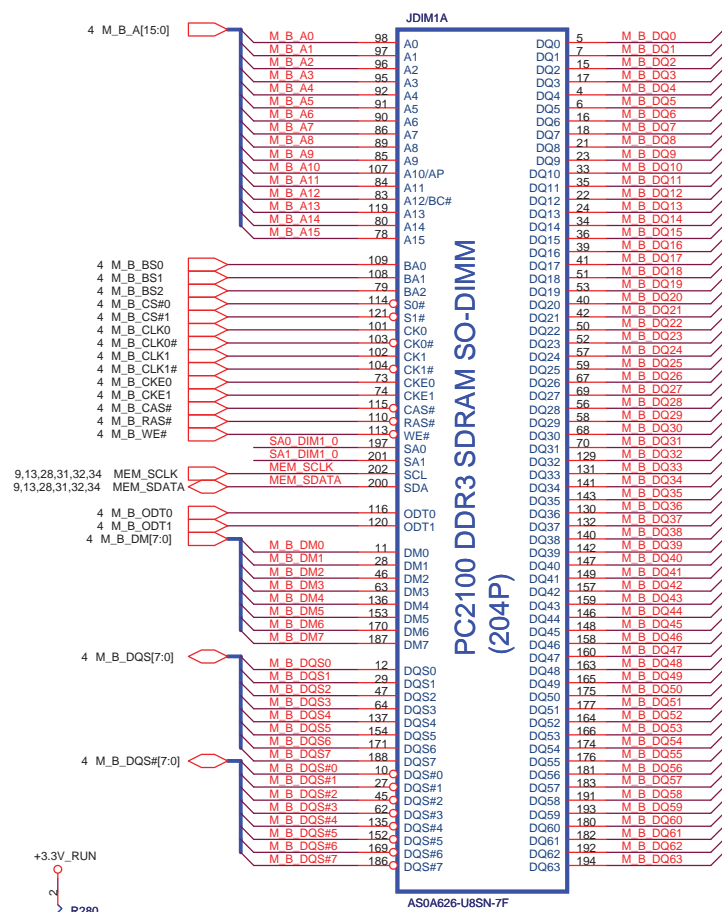
6/02: Change M1 from voltage regulator to voltage divider



5/13: Change connector from Tyco to Foxconn to avoid shortage

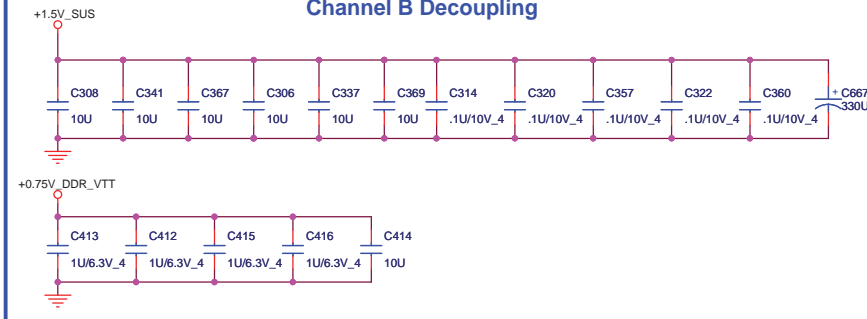
Channel B

www.laptopblue.vn



Note:
If SA1_DIM1 = 1, SA0_DIM1 = 0
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34
If SA1_DIM1 = 1, SA0_DIM1 = 1
SO-DIMMA SPD Address is 0xA6
SO-DIMMA TS Address is 0x36

Channel B Decoupling



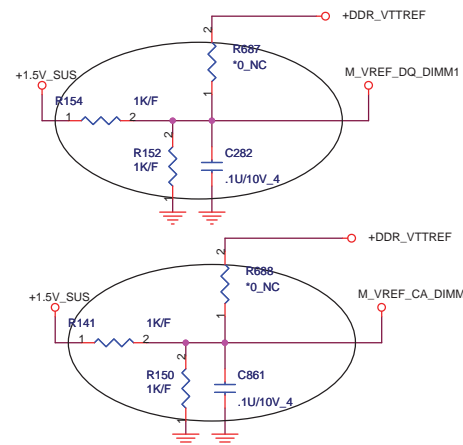
For CH B SO-DIMM VREF_DQ for M2

Delete according to Intel Design Change

M1 VREF

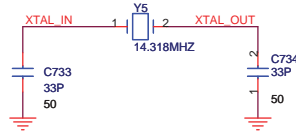
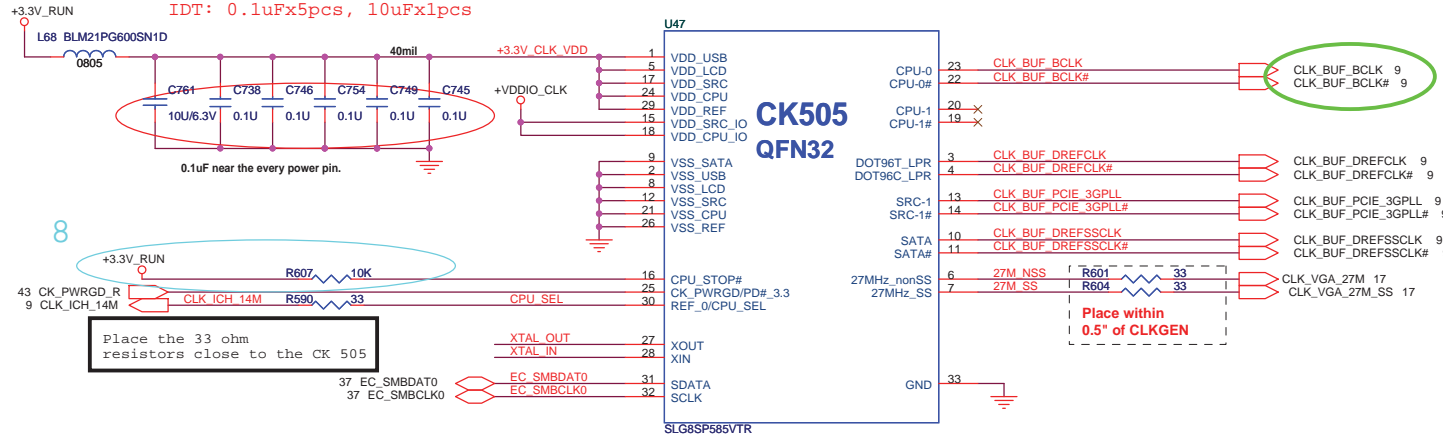
5/18: Separate voltage divider for M_VREF_DQ_DIMM1 and M_VREF_CA_DIMM1 to follow Intel CRB design

6/02: Change M1 from voltage regulator to voltage divider

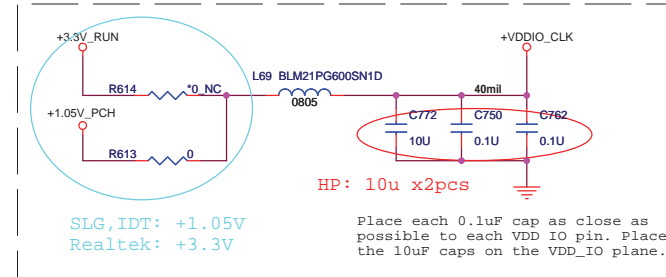


Title DDR3 DIMM-B		
Size RM5	Document Number	Rev 3A
Date: Thursday, August 20, 2009	Sheet 14	of 61

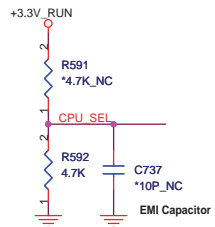
Realtek: 0.1uFx6pcs, 22uFx1pcs
IDT: 0.1uFx5pcs, 10uFx1pcs



Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs



+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V,
Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V,
IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.

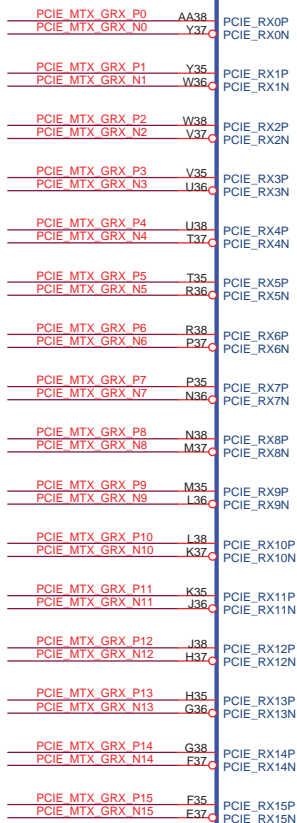


PIN	30	CPU_0	CPU_1
0 (default)		133MHz	133MHz
1 (0.7V~1.5V)		100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V,
Realtek date sheet (V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V,
IDT date sheet (V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V



3 PCIE_MTX_GRX_P[0..15]
3 PCIE_MTX_GRX_N[0..15]



U29A

PCI EXPRESS INTERFACE

ASIC

PN

100-CK

QC/P/N

M96-M2 XT A13 216-0729051 100-CK3186 AJ072900T08
M97-M2 LP A11 216-0731001 100-CG1806 AJ073100T01

PCIE_MRX_GTX_P[0..15] 3
PCIE_MRX_GTX_N[0..15] 3



9 CLK_PCIE_VGA
9 CLK_PCIE_VGA#

!!! Park, Madison : Pop 0 Ohm
M96: depop 0 ohm

R426 *0 NC

CLOCK
PCIE_REFCLKP
PCIE_REFCLKN

CALIBRATION

PCIE_CALRP

PCIE_CALRN

NC#1
NC#2
PWRGOOD

PERSTB

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

PERST#

216-0729051(M96-M2 XT)



Title		
M96XT_PCIE		
Size	Document Number	Rev
RM5		3A
Date:	Thursday, August 20, 2009	Sheet 16 of 61

Note : Required Frequency = 800 MHz

+3.3V_DELAY



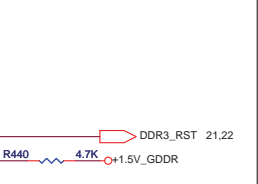
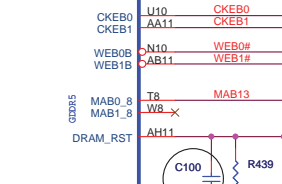
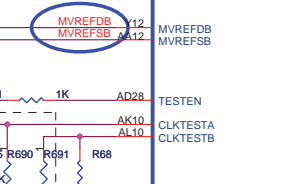
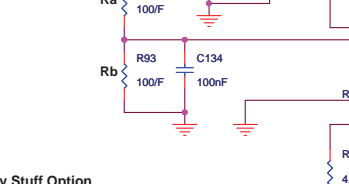
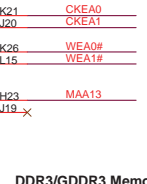
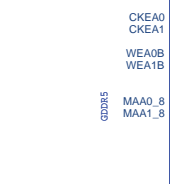
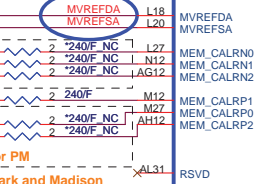
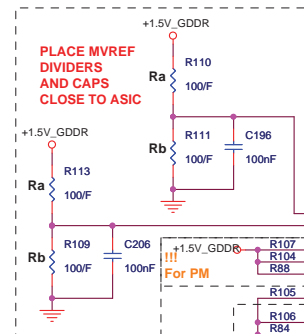
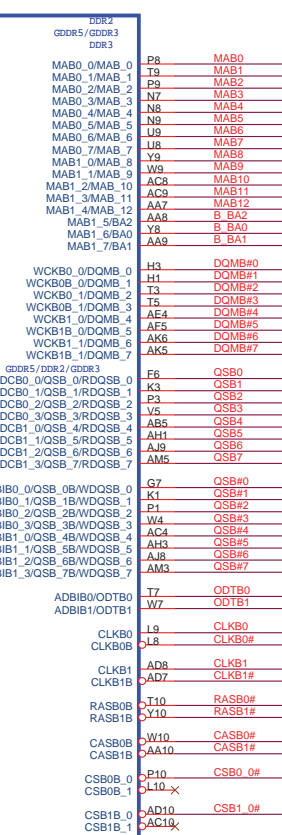
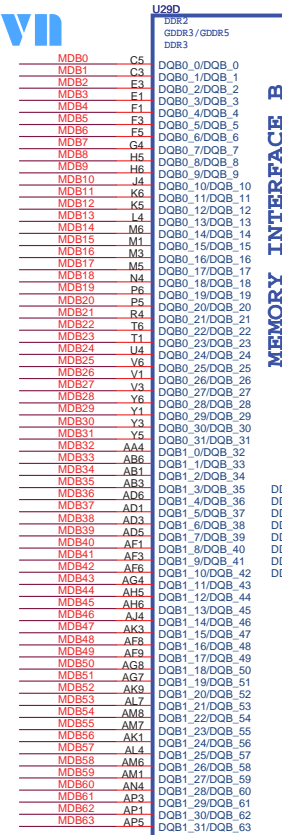
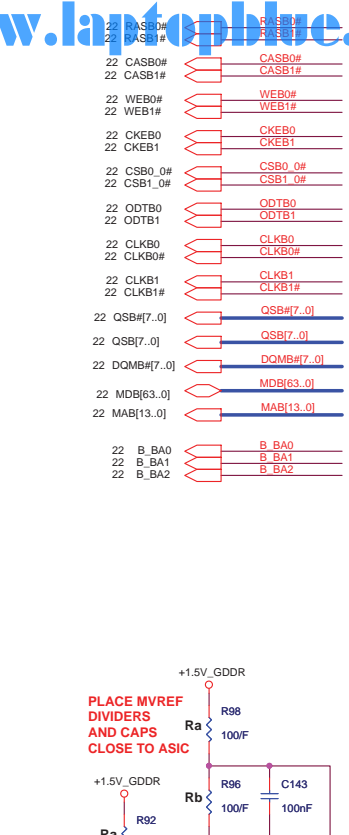
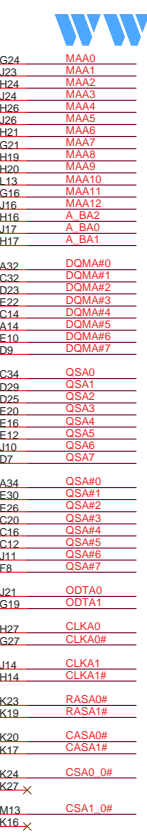
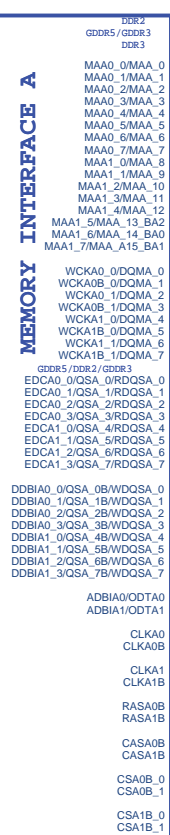
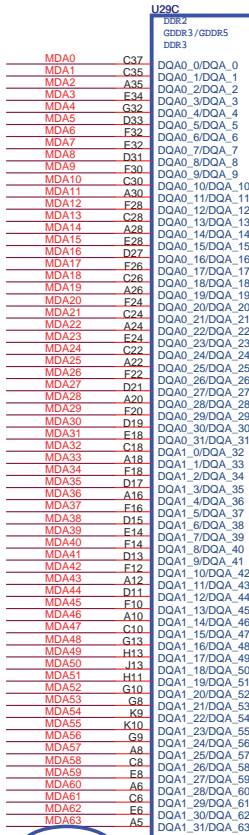
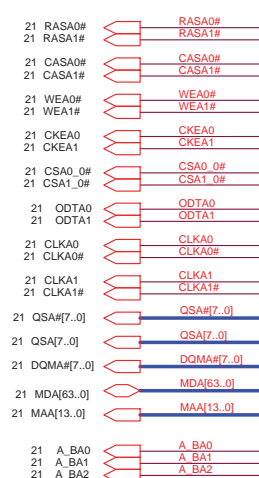
AR8	DVPCTRL_MVR
AR9	DVPCTRL_MVR
AR10	DVPCTRL_0
AR11	DVPCTRL_1
AR12	DVPCTRL_2
AR13	DVPCTRL_3
AR14	DVPCTRL_4
AR15	DVPCTRL_5
AR16	DVPCTRL_6
AR17	DVPCTRL_7
AR18	DVPCTRL_8
AR19	DVPCTRL_9
AR20	DVPCTRL_10
AR21	DVPCTRL_11
AR22	DVPCTRL_12
AR23	DVPCTRL_13
AR24	DVPCTRL_14
AR25	DVPCTRL_15
AR26	DVPCTRL_16
AR27	DVPCTRL_17
AR28	DVPCTRL_18
AR29	DVPCTRL_19
AR30	DVPCTRL_20
AR31	DVPCTRL_21
AR32	DVPCTRL_22
AR33	DVPCTRL_23
AR34	DVPCTRL_24
AR35	DVPCTRL_25
AR36	DVPCTRL_26
AR37	DVPCTRL_27
AR38	DVPCTRL_28
AR39	DVPCTRL_29
AR40	DVPCTRL_30
AR41	DVPCTRL_31
AR42	DVPCTRL_32
AR43	DVPCTRL_33
AR44	DVPCTRL_34
AR45	DVPCTRL_35
AR46	DVPCTRL_36
AR47	DVPCTRL_37
AR48	DVPCTRL_38
AR49	DVPCTRL_39
AR50	DVPCTRL_40
AR51	DVPCTRL_41
AR52	DVPCTRL_42
AR53	DVPCTRL_43
AR54	DVPCTRL_44
AR55	DVPCTRL_45
AR56	DVPCTRL_46
AR57	DVPCTRL_47
AR58	DVPCTRL_48
AR59	DVPCTRL_49
AR60	DVPCTRL_50
AR61	DVPCTRL_51
AR62	DVPCTRL_52
AR63	DVPCTRL_53
AR64	DVPCTRL_54
AR65	DVPCTRL_55
AR66	DVPCTRL_56
AR67	DVPCTRL_57
AR68	DVPCTRL_58
AR69	DVPCTRL_59
AR70	DVPCTRL_60
AR71	DVPCTRL_61
AR72	DVPCTRL_62
AR73	DVPCTRL_63
AR74	DVPCTRL_64
AR75	DVPCTRL_65
AR76	DVPCTRL_66
AR77	DVPCTRL_67
AR78	DVPCTRL_68
AR79	DVPCTRL_69
AR80	DVPCTRL_70
AR81	DVPCTRL_71
AR82	DVPCTRL_72
AR83	DVPCTRL_73
AR84	DVPCTRL_74
AR85	DVPCTRL_75
AR86	DVPCTRL_76
AR87	DVPCTRL_77
AR88	DVPCTRL_78
AR89	DVPCTRL_79
AR90	DVPCTRL_80
AR91	DVPCTRL_81
AR92	DVPCTRL_82
AR93	DVPCTRL_83
AR94	DVPCTRL_84
AR95	DVPCTRL_85
AR96	DVPCTRL_86
AR97	DVPCTRL_87
AR98	DVPCTRL_88
AR99	DVPCTRL_89
AR100	DVPCTRL_90
AR101	DVPCTRL_91
AR102	DVPCTRL_92
AR103	DVPCTRL_93
AR104	DVPCTRL_94
AR105	DVPCTRL_95
AR106	DVPCTRL_96
AR107	DVPCTRL_97
AR108	DVPCTRL_98
AR109	DVPCTRL_99
AR110	DVPCTRL_100
AR111	DVPCTRL_101
AR112	DVPCTRL_102
AR113	DVPCTRL_103
AR114	DVPCTRL_104
AR115	DVPCTRL_105
AR116	DVPCTRL_106
AR117	DVPCTRL_107
AR118	DVPCTRL_108
AR119	DVPCTRL_109
AR120	DVPCTRL_110
AR121	DVPCTRL_111
AR122	DVPCTRL_112
AR123	DVPCTRL_113
AR124	DVPCTRL_114
AR125	DVPCTRL_115
AR126	DVPCTRL_116
AR127	DVPCTRL_117
AR128	DVPCTRL_118
AR129	DVPCTRL_119
AR130	DVPCTRL_120
AR131	DVPCTRL_121
AR132	DVPCTRL_122
AR133	DVPCTRL_123
AR134	DVPCTRL_124
AR135	DVPCTRL_125
AR136	DVPCTRL_126
AR137	DVPCTRL_127
AR138	DVPCTRL_128
AR139	DVPCTRL_129
AR140	DVPCTRL_130
AR141	DVPCTRL_131
AR142	DVPCTRL_132
AR143	DVPCTRL_133
AR144	DVPCTRL_134
AR145	DVPCTRL_135
AR146	DVPCTRL_136
AR147	DVPCTRL_137
AR148	DVPCTRL_138
AR149	DVPCTRL_139
AR150	DVPCTRL_140
AR151	DVPCTRL_141
AR152	DVPCTRL_142
AR153	DVPCTRL_143
AR154	DVPCTRL_144
AR155	DVPCTRL_145
AR156	DVPCTRL_146
AR157	DVPCTRL_147
AR158	DVPCTRL_148
AR159	DVPCTRL_149
AR160	DVPCTRL_150
AR161	DVPCTRL_151
AR162	DVPCTRL_152
AR163	DVPCTRL_153
AR164	DVPCTRL_154
AR165	DVPCTRL_155
AR166	DVPCTRL_156
AR167	DVPCTRL_157
AR168	DVPCTRL_158
AR169	DVPCTRL_159
AR170	DVPCTRL_160
AR171	DVPCTRL_161
AR172	DVPCTRL_162
AR173	DVPCTRL_163
AR174	DVPCTRL_164
AR175	DVPCTRL_165
AR176	DVPCTRL_166
AR177	DVPCTRL_167
AR178	DVPCTRL_168
AR179	DVPCTRL_169
AR180	DVPCTRL_170
AR181	DVPCTRL_171
AR182	DVPCTRL_172
AR183	DVPCTRL_173
AR184	DVPCTRL_174
AR185	DVPCTRL_175
AR186	DVPCTRL_176
AR187	DVPCTRL_177
AR188	DVPCTRL_178
AR189	DVPCTRL_179
AR190	DVPCTRL_180
AR191	DVPCTRL_181
AR192	DVPCTRL_182
AR193	DVPCTRL_183
AR194	DVPCTRL_184
AR195	DVPCTRL_185
AR196	DVPCTRL_186
AR197	DVPCTRL_187
AR198	DVPCTRL_188
AR199	DVPCTRL_189
AR200	DVPCTRL_190
AR201	DVPCTRL_191
AR202	DVPCTRL_192
AR203	DVPCTRL_193
AR204	DVPCTRL_194
AR205	DVPCTRL_195
AR206	DVPCTRL_196
AR207	DVPCTRL_197
AR208	DVPCTRL_198
AR209	DVPCTRL_199
AR210	DVPCTRL_200
AR211	DVPCTRL_201
AR212	DVPCTRL_202
AR213	DVPCTRL_203
AR214	DVPCTRL_204
AR215	DVPCTRL_205
AR216	DVPCTRL_206
AR217	DVPCTRL_207
AR218	DVPCTRL_208
AR219	DVPCTRL_209
AR220	DVPCTRL_210
AR221	DVPCTRL_211
AR222	DVPCTRL_212
AR223	DVPCTRL_213
AR224	DVPCTRL_214
AR225	DVPCTRL_215
AR226	DVPCTRL_216
AR227	DVPCTRL_217
AR228	DVPCTRL_218
AR229	DVPCTRL_219
AR230	DVPCTRL_220
AR231	DVPCTRL_221
AR232	DVPCTRL_222
AR233	DVPCTRL_223
AR234	DVPCTRL_224
AR235	DVPCTRL_225
AR236	DVPCTRL_226
AR237	DVPCTRL_227
AR238	DVPCTRL_228
AR239	DVPCTRL_229
AR240	DVPCTRL_230
AR241	DVPCTRL_231
AR242	DVPCTRL_232
AR243	DVPCTRL_233
AR244	DVPCTRL_234
AR245	DVPCTRL_235
AR246	DVPCTRL_236
AR247	DVPCTRL_237
AR248	DVPCTRL_238
AR249	DVPCTRL_239
AR250	DVPCTRL_240
AR251	DVPCTRL_241
AR252	DVPCTRL_242
AR253	DVPCTRL_243
AR254	DVPCTRL_244
AR255	DVPCTRL_245
AR256	DVPCTRL_246
AR257	DVPCTRL_247
AR258	DVPCTRL_248
AR259	DVPCTRL_249
AR260	DVPCTRL_250
AR261	DVPCTRL_251
AR262	DVPCTRL_252
AR263	DVPCTRL_253
AR264	DVPCTRL_254
AR265	DVPCTRL_255
AR266	DVPCTRL_256
AR267	DVPCTRL_257
AR268	DVPCTRL_258
AR269	DVPCTRL_259
AR270	DVPCTRL_260
AR271	DVPCTRL_261
AR272	DVPCTRL_262
AR273	DVPCTRL_263
AR274	DVPCTRL_264
AR275	DVPCTRL_265
AR276	DVPCTRL_266
AR277	DVPCTRL_267
AR278	DVPCTRL_268
AR279	DVPCTRL_269
AR280	DVPCTRL_270
AR281	DVPCTRL_271
AR282	DVPCTRL_272
AR283	DVPCTRL_273
AR284	DVPCTRL_274
AR285	DVPCTRL_275
AR286	DVPCTRL_276
AR287	DVPCTRL_277
AR288	DVPCTRL_278
AR289	DVPCTRL_279
AR290	DVPCTRL_280
AR291	DVPCTRL_281
AR292	DVPCTRL_282
AR293	DVPCTRL_283
AR294	DVPCTRL_284
AR295	DVPCTRL_285
AR296	DVPCTRL_286
AR297	DVPCTRL_287
AR298	DVPCTRL_288
AR299	DVPCTRL_289
AR300	DVPCTRL_290
AR301	DVPCTRL_291
AR302	DVPCTRL_292
AR303	DVPCTRL_293
AR304	DVPCTRL_294
AR305	DVPCTRL_295
AR306	DVPCTRL_296
AR307	DVPCTRL_297
AR308	DVPCTRL_298
AR309	DVPCTRL_299
AR310	DVPCTRL_300
AR311	DVPCTRL_301
AR312	DVPCTRL_302
AR313	DVPCTRL_303
AR314	DVPCTRL_304
AR315	DVPCTRL_305
AR316	DVPCTRL_306
AR317	DVPCTRL_307
AR318	DVPCTRL_308
AR319	DVPCTRL_309
AR320	DVPCTRL_310
AR321	DVPCTRL_311
AR322	DVPCTRL_312
AR323	DVPCTRL_313
AR324	DVPCTRL_314
AR325	DVPCTRL_315
AR326	DVPCTRL_316
AR327	DVPCTRL_317
AR328	DVPCTRL_318
AR329	DVPCTRL_319
AR330	DVPCTRL_320
AR331	DVPCTRL_321
AR332	DVPCTRL_322
AR333	DVPCTRL_323
AR334	DVPCTRL_324
AR335	DVPCTRL_325
AR336	DVPCTRL_326
AR337	DVPCTRL_327
AR338	DVPCTRL_328
AR339	DVPCTRL_329
AR340	DVPCTRL_330
AR341	DVPCTRL_331
AR342	DVPCTRL_332
AR343	DVPCTRL_333
AR344	DVPCTRL_334
AR345	DVPCTRL_335
AR346	DVPCTRL_336
AR347	DVPCTRL_337
AR348	DVPCTRL_338
AR349	DVPCTRL_339
AR350	DVPCTRL_340
AR351	DVPCTRL_341
AR352	DVPCTRL_342
AR353	DVPCTRL_343
AR354	DVPCTRL_344
AR355	DVPCTRL_345
AR356	DVPCTRL_346
AR357	DVPCTRL_347
AR358	DVPCTRL_348
AR359	DVPCTRL_349
AR360	DVPCTRL_350
AR361	DVPCTRL_351
AR362	DVPCTRL_352
AR363	DVPCTRL_353
AR364	DVPCTRL_354
AR365	DVPCTRL_355
AR366	DVPCTRL_356
AR367	DVPCTRL_357
AR368	DVPCTRL_358
AR369	DVPCTRL_359
AR370	DVPCTRL_360
AR371	DVPCTRL_361
AR372	DVPCTRL_362
AR373	DVPCTRL_363
AR374	DVPCTRL_364
AR375	DVPCTRL_365
AR376	DVPCTRL_366
AR377	DVPCTRL_367
AR378	DVPCTRL_368
AR379	DVPCTRL_369
AR380	DVPCTRL_370
AR381	DVPCTRL_371
AR382	DVPCTRL_372
AR383	DVPCTRL_373
AR384	DVPCTRL_374
AR385	DVPCTRL_375
AR386	DVPCTRL_376
AR387	DVPCTRL_377
AR388	DVPCTRL_378
AR389	DVPCTRL_379
AR390	DVPCTRL_380
AR391	DVPCTRL_381
AR392	DVPCTRL_382
AR393	DVPCTRL_383
AR394	DVPCTRL_384
AR395	DVPCTRL_385
AR396	DVPCTRL_386
AR397	DVPCTRL_387
AR398	DVPCTRL_388
AR399	DVPCTRL_389
AR400	DVPCTRL_390
AR401	DVPCTRL_391
AR402	DVPCTRL_392
AR403	DVPCTRL_393
AR404	DVPCTRL_394
AR405	DVPCTRL_395
AR406	DVPCTRL_396
AR407	DVPCTRL_397
AR408	DVPCTRL_398
AR409	DVPCTRL_399
AR410	DVPCTRL_400
AR411	DVPCTRL_401
AR412	DVPCTRL_402
AR413	DVPCTRL_403
AR414	DVPCTRL_404
AR415	DVPCTRL_405
AR416	DVPCTRL_406
AR417	DVPCTRL_407
AR418	DVPCTRL_408
AR419	DVPCTRL_409
AR420	DVPCTRL_410
AR421	DVPCTRL_411
AR422	DVPCTRL_412
AR423	DVPCTRL_413
AR424	DVPCTRL_414
AR425	DVPCTRL_415
AR426	DVPCTRL_416
AR427	DVPCTRL_417
AR428	DVPCTRL_418
AR429	DVPCTRL_419
AR430	DVPCTRL_420
AR431	DVPCTRL_421
AR432	DVPCTRL_422
AR433	DVPCTRL_423
AR434	DVPCTRL_424
AR435	DVPCTRL_425
AR436	DVPCTRL_426
AR437	DVPCTRL_427
AR438	DVPCTRL_428
AR439	DVPCTRL_429
AR440	DVPCTRL_430
AR441	DVPCTRL_431
AR442	DVPCTRL_432
AR443	DVPCTRL_433
AR444	DVPCTRL_434
AR445	DVPCTRL_435
AR446	DVPCTRL_436
AR447	DVPCTRL_437
AR448	DVPCTRL_438
AR449	DVPCTRL_439
AR450	DVPCTRL_440
AR451	DVPCTRL_441
AR452	DVPCTRL_442
AR453	DVPCTRL_443
AR454	DVPCTRL_444
AR455	DVPCTRL_445
AR456	DVPCTRL_446
AR457	DVP



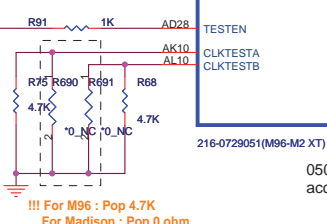
M96XT_JO & STRAP		
Size	Document Number RM5	Rev 3A
Date:	Thursday, August 20, 2009	Sheet 17 of 61



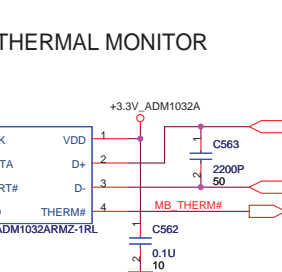
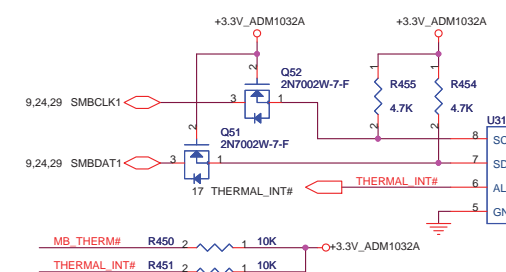
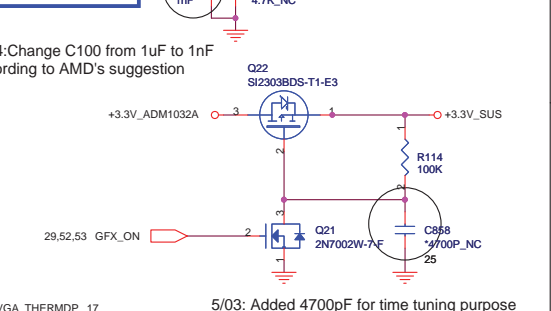




	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	100R
Rb	100R	100R

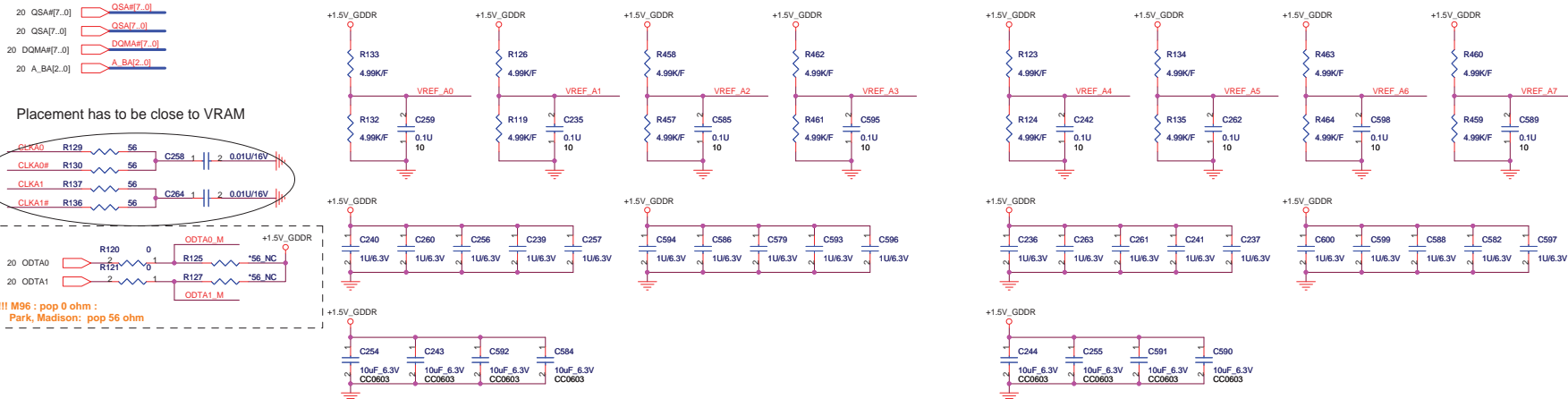
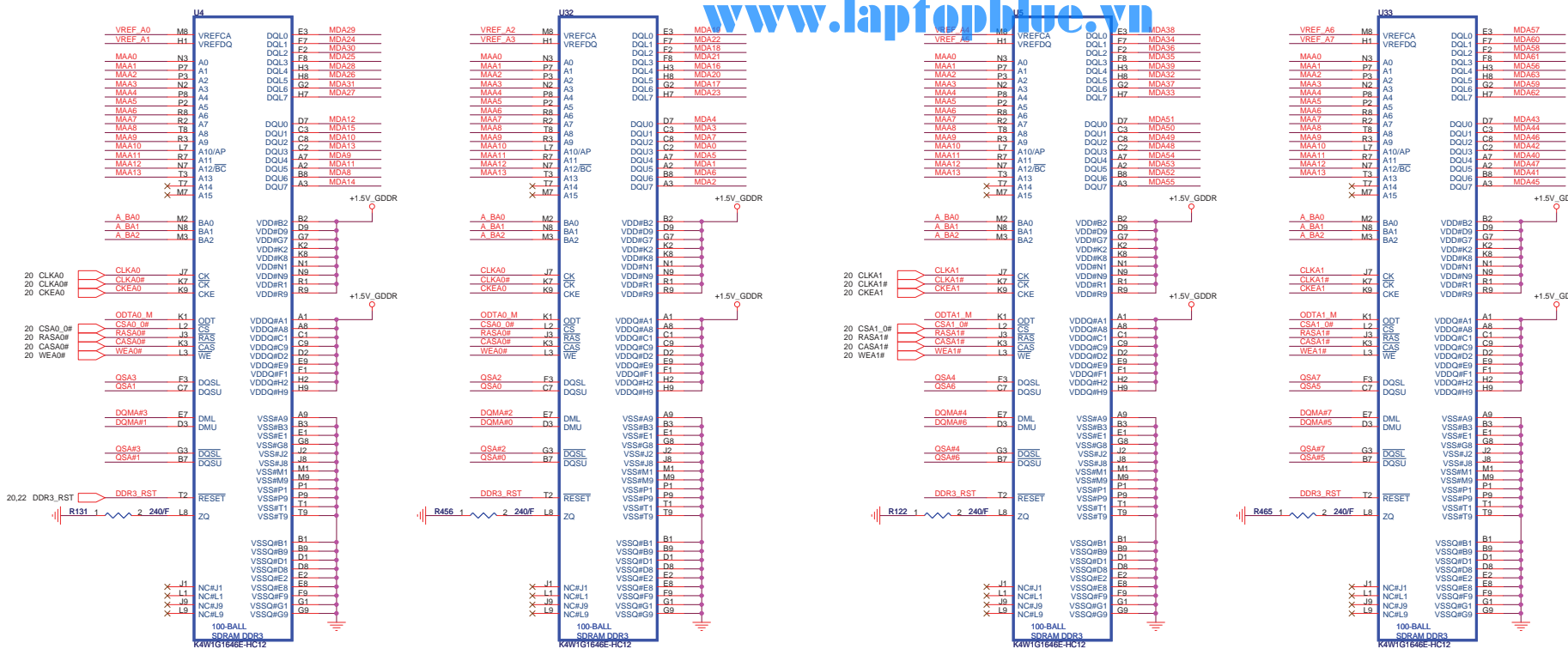


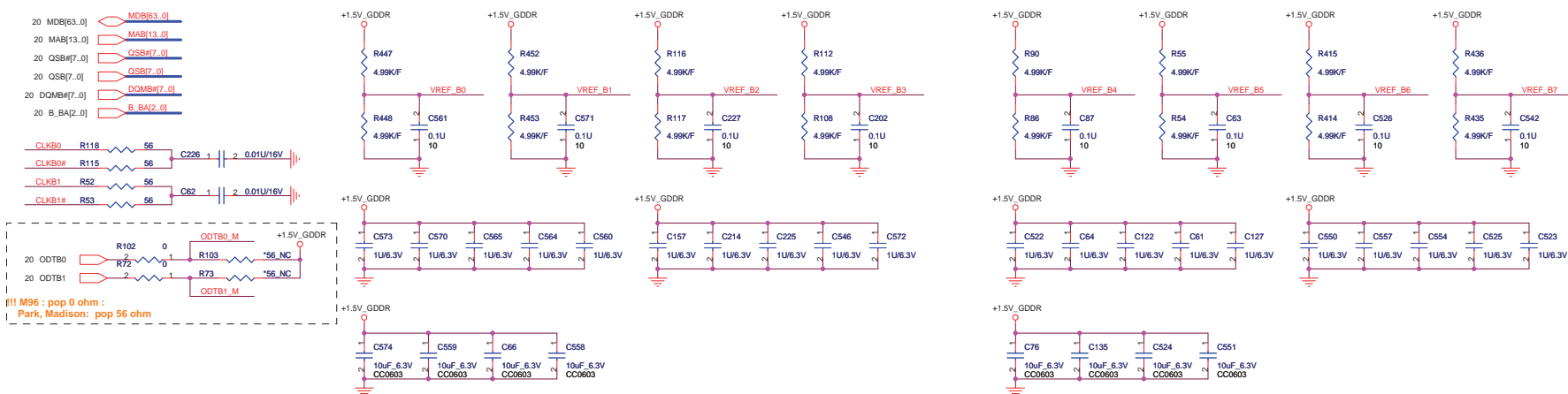
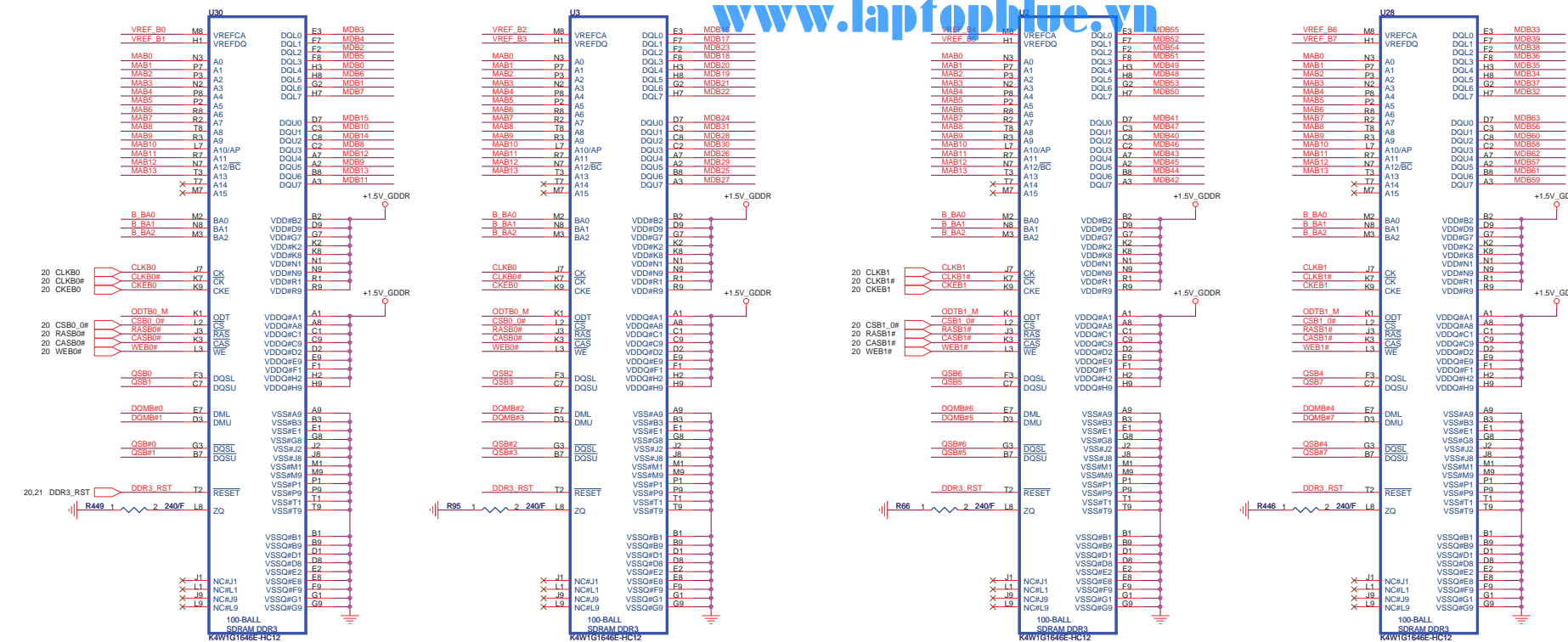
0504:Change C100 from 1uF to 10uF according to AMD's suggestion

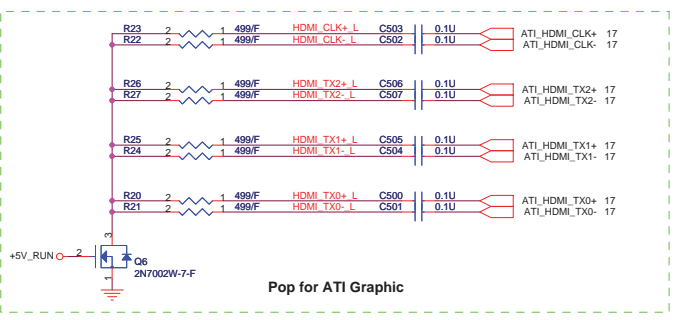


THERMAL MONITOR

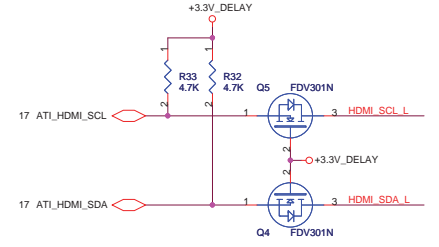
5/03: Added 4700pF for time tuning purpose



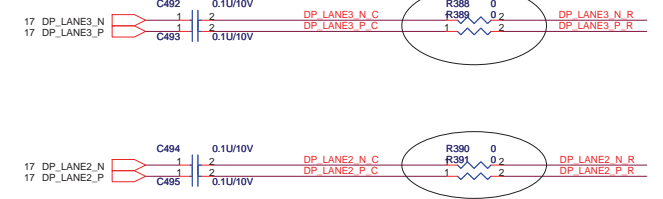




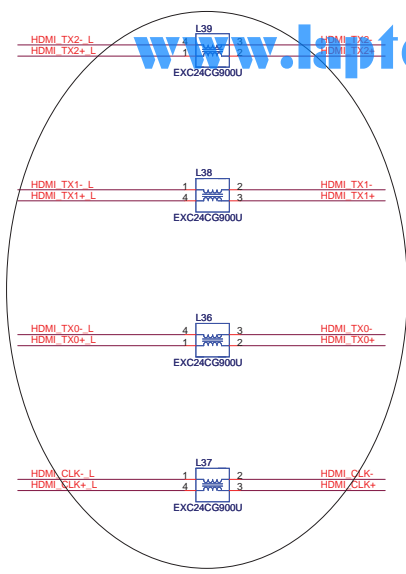
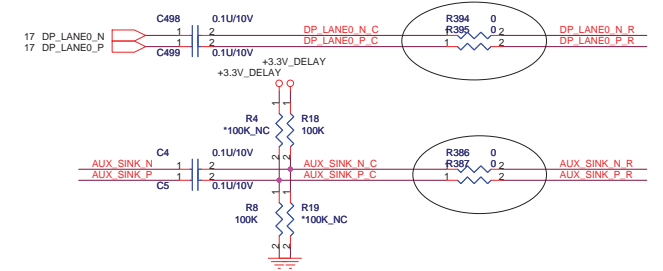
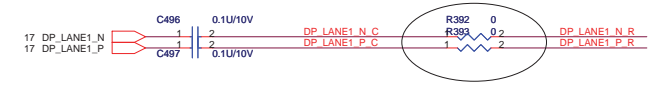
Pop for ATI Graphic



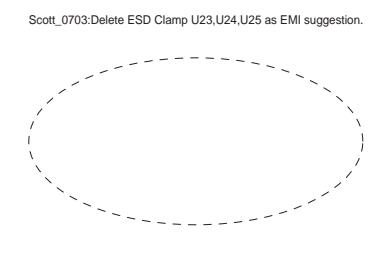
Reserve For EMI



Scott_0814:Delete reserve choke as confirm with EMI.

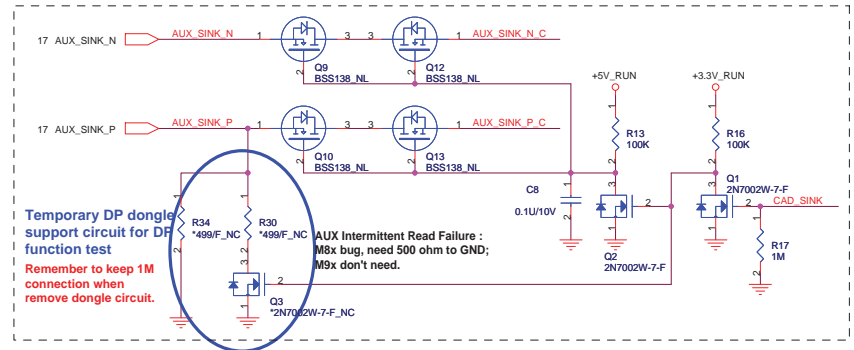
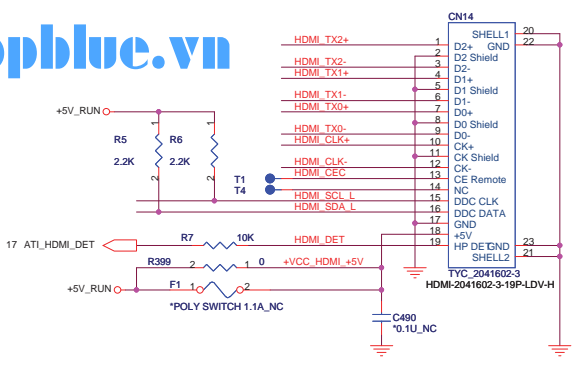


Scott_0814:Delete 0ohm reserve resistors as confirm with EMI.
Delete EMI ESD IC for EMI asked HDMI signals link to CONN directly.



Scott_0703:Delete ESD Clamp U23,U24,U25 as EMI suggestion.

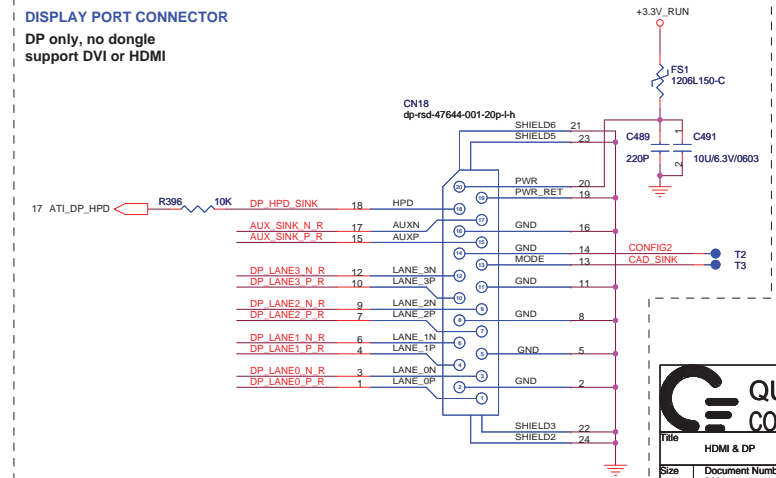
www.laptopblue.vn



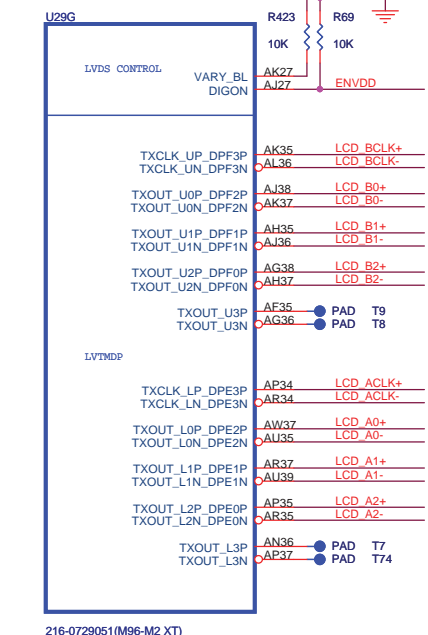
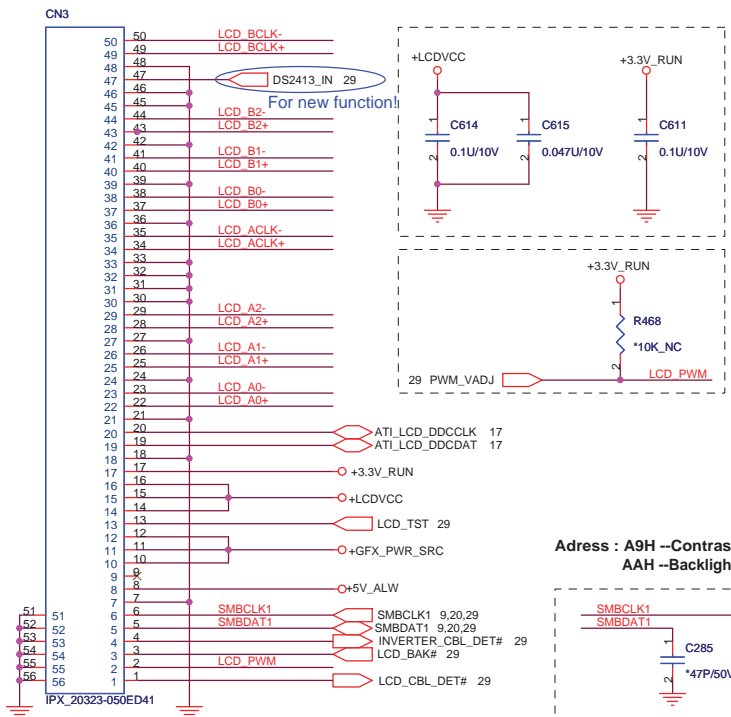
Temporary DP dongle support circuit for DP function test
Remember to keep 1M connection when remove dongle circuit.
AUX Intermittent Read Failure : M8x bug, need 500 ohm to GND; M9x don't need.

DISPLAY PORT CONNECTOR

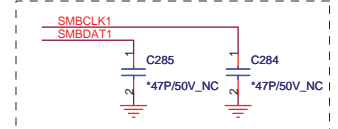
DP only, no dongle support DVI or HDMI



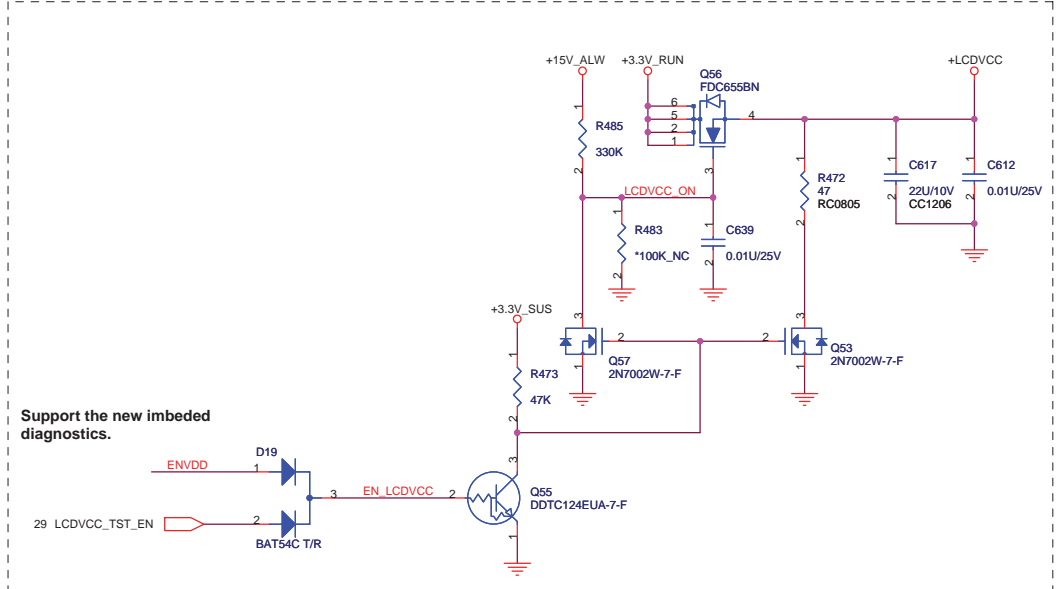
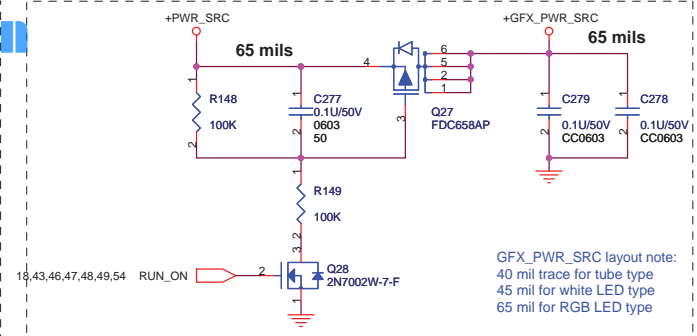
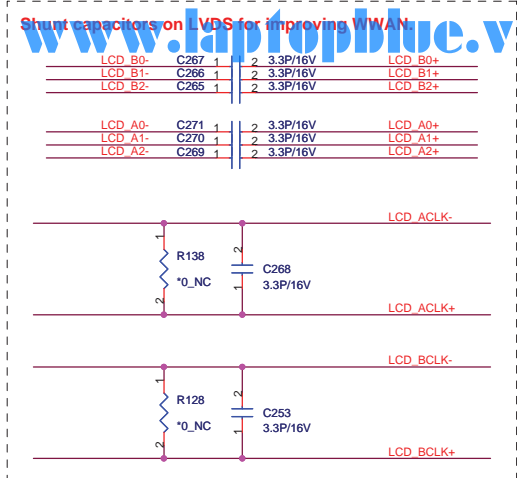
File	HDMI & DP	Rev	3A
Size	Document Number RM5		
Date:	Thursday, August 20, 2009	Sheet	23 of 61

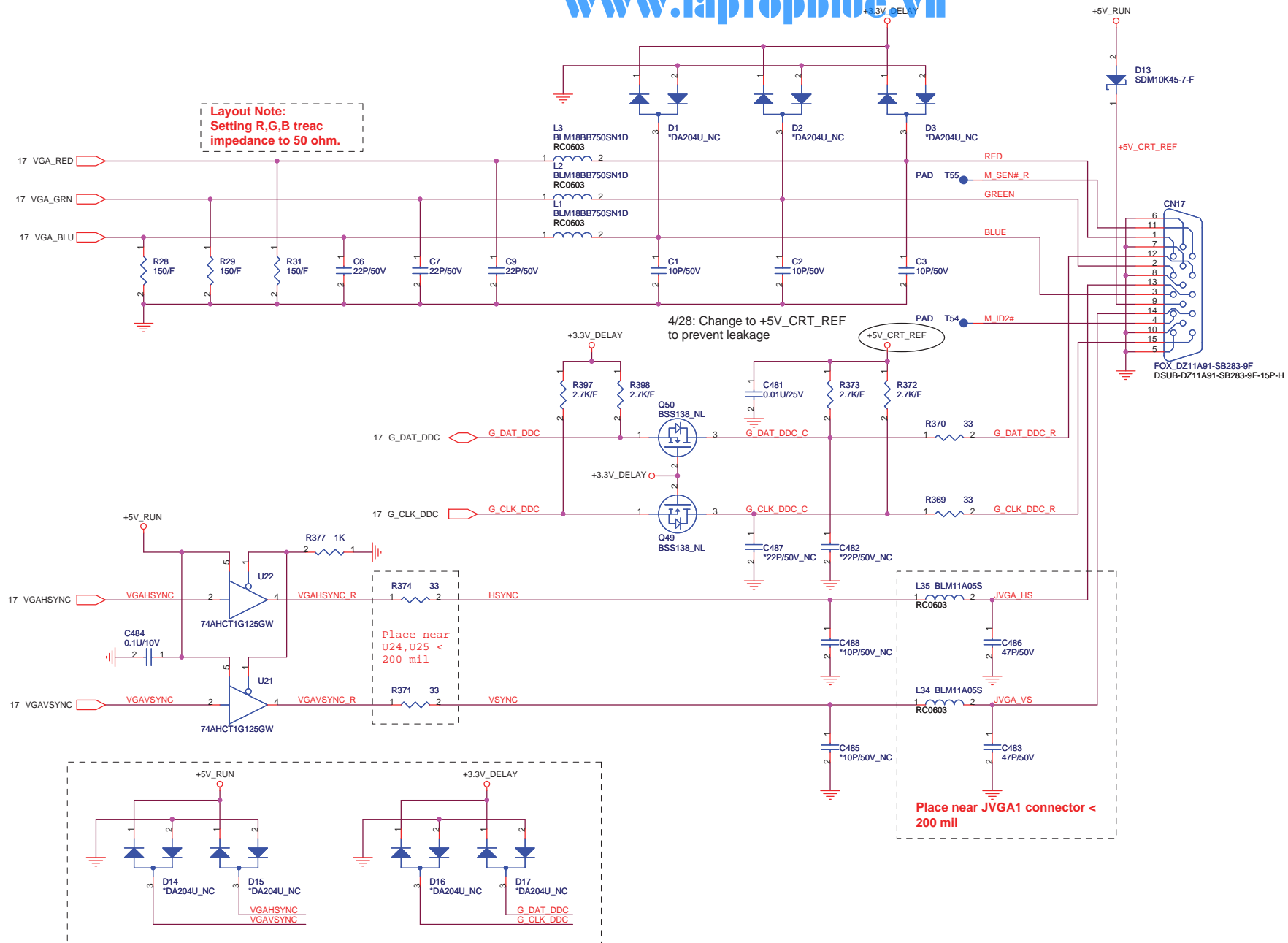


Address : A9H --Contrast
AAH --Backlight

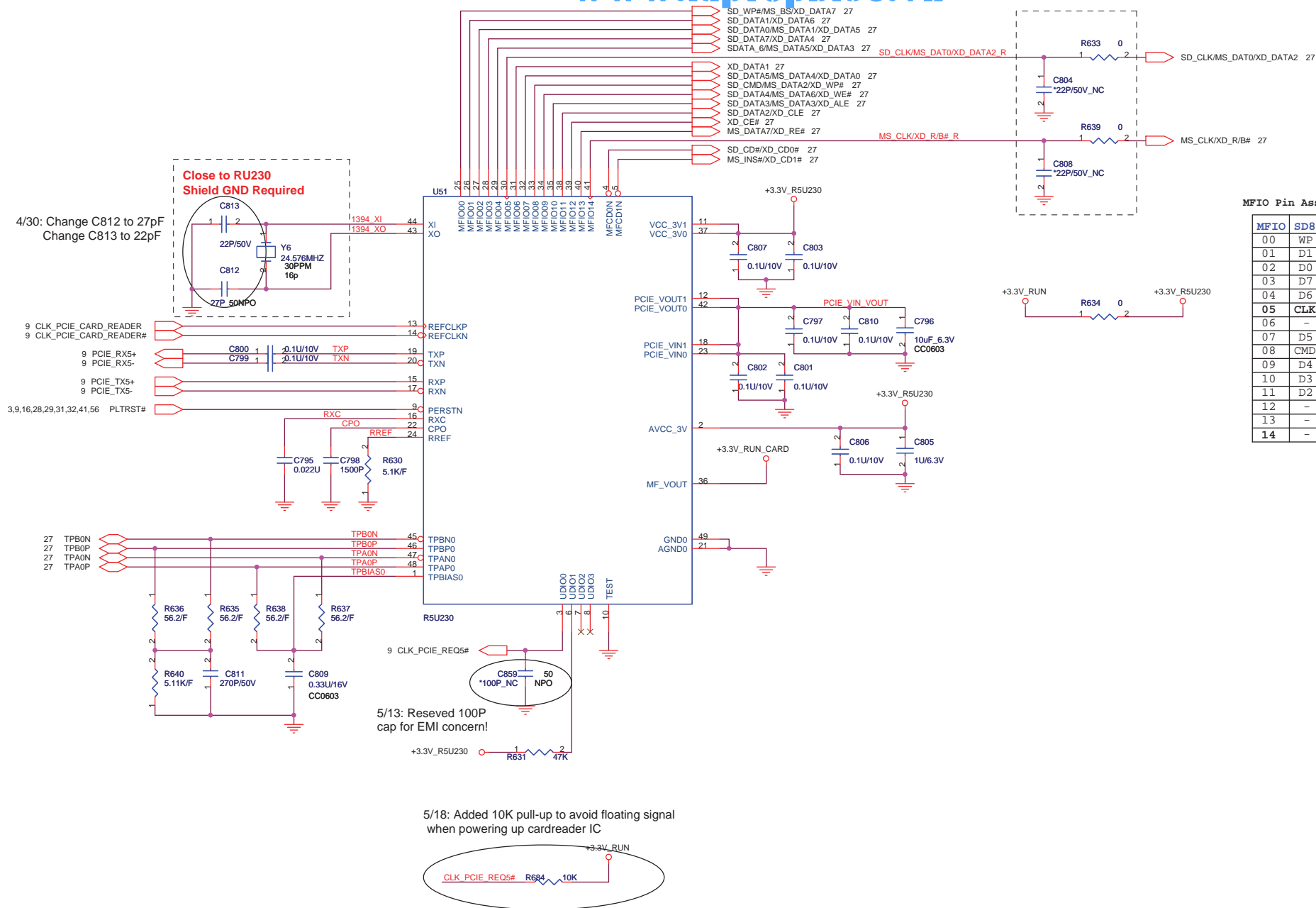


Scott_0812: Delete DPST function as non-used.





Place close U23



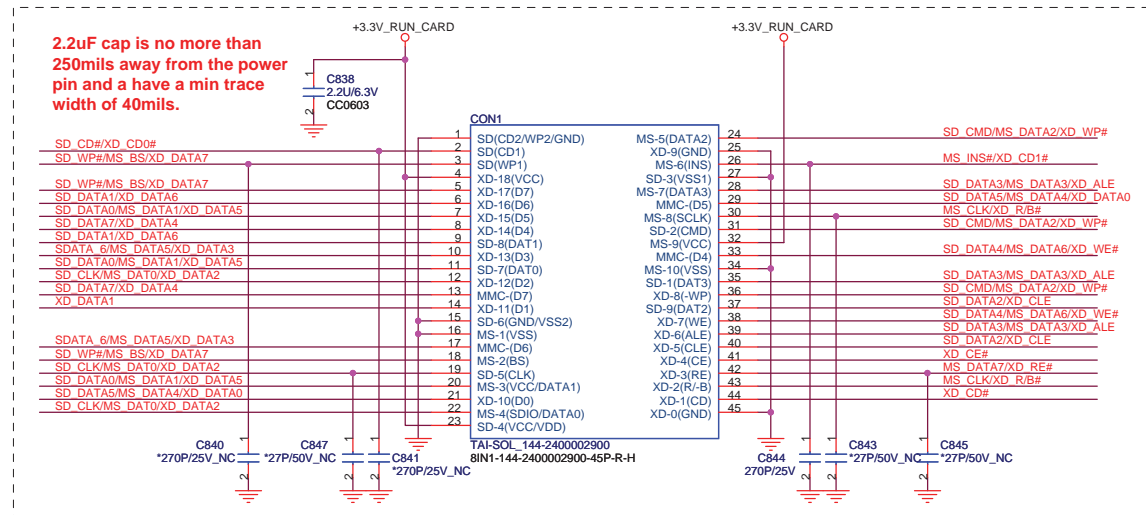
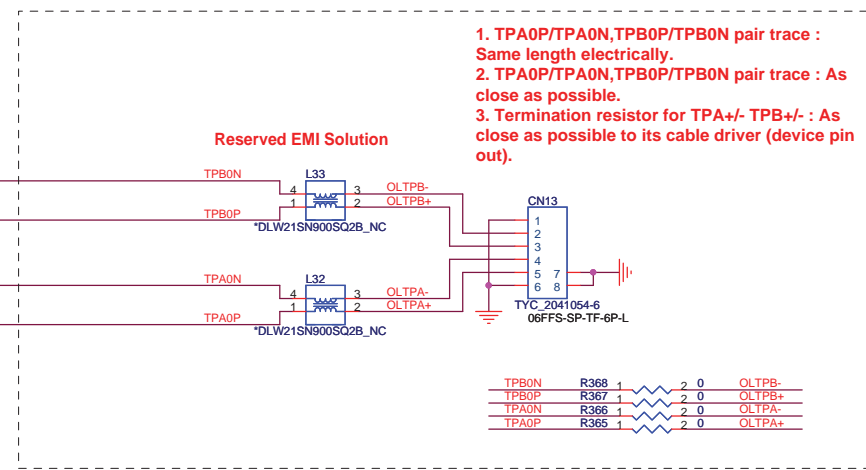
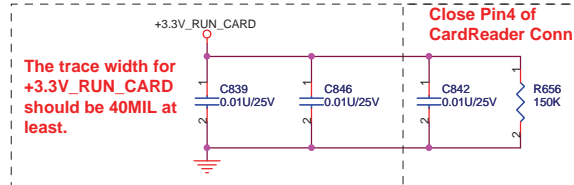
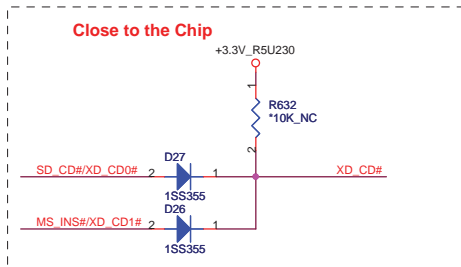
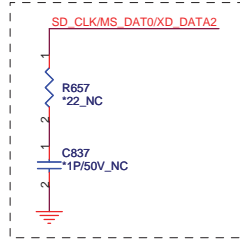
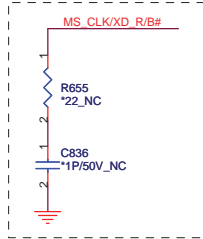
MFIO Pin Assignment Table

MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	CLK	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	CLK	R/B#

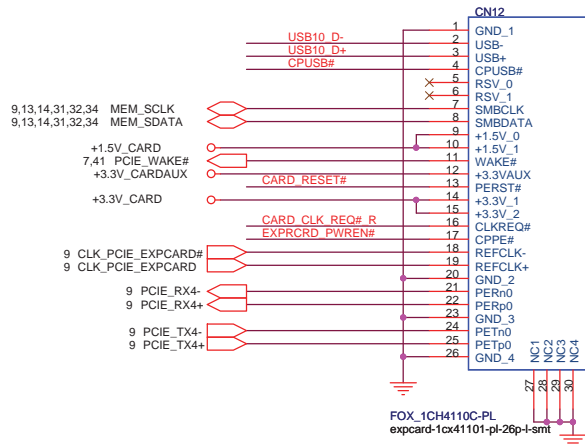


26 SD_WP#/MS_BS/XD_DATA7
26 SD_DATA1/XD_DATA6
26 SD_DATA0/MS_DATA1/XD_DATA5
26 SD_DATA7/XD_DATA4
26 SDATA_6/MS_DATA5/XD_DATA3
26 SD_CLK/MS_DATA0/XD_DATA2
26 XD_DATA1
26 SD_DATA5/MS_DATA4/XD_DATA0
26 SD_CMD/MS_DATA2/XD_WP#
26 SD_DATA4/MS_DATA6/XD_WE#
26 SD_DATA3/MS_DATA3/XD_ALE
26 SD_DATA2/XD_CLE
26 XD_CE#
26 MS_DATA7/XD_RE#
26 MS_CLK/XD_R/B#
26 SD_CD#/XD_CD0#
26 MS_INS#/XD_CD1#

SD_WP#/MS_BS/XD_DATA7
SD_DATA1/XD_DATA6
SD_DATA0/MS_DATA1/XD_DATA5
SD_DATA7/XD_DATA4
SDATA_6/MS_DATA5/XD_DATA3
SD_CLK/MS_DATA0/XD_DATA2
XD_DATA1
SD_DATA5/MS_DATA4/XD_DATA0
SD_CMD/MS_DATA2/XD_WP#
SD_DATA4/MS_DATA6/XD_WE#
SD_DATA3/MS_DATA3/XD_ALE
SD_DATA2/XD_CLE
XD_CE#
MS_DATA7/XD_RE#
MS_CLK/XD_R/B#
SD_CD#/XD_CD0#
MS_INS#/XD_CD1#

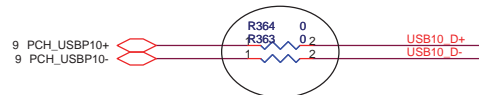


Express Card

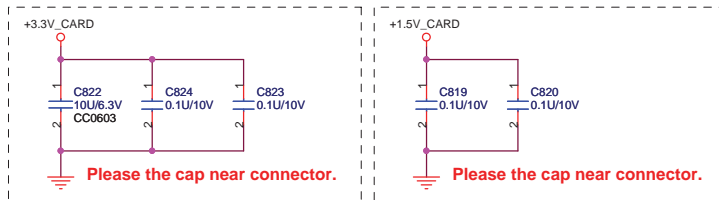


Scott_0813:Change CN12 F/P to expcard-1cx41101-pl-26p-l-smt as ME modify.

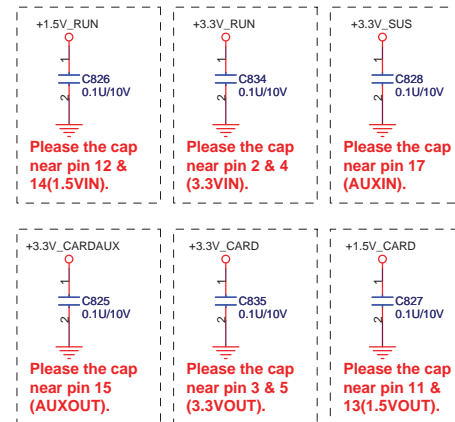
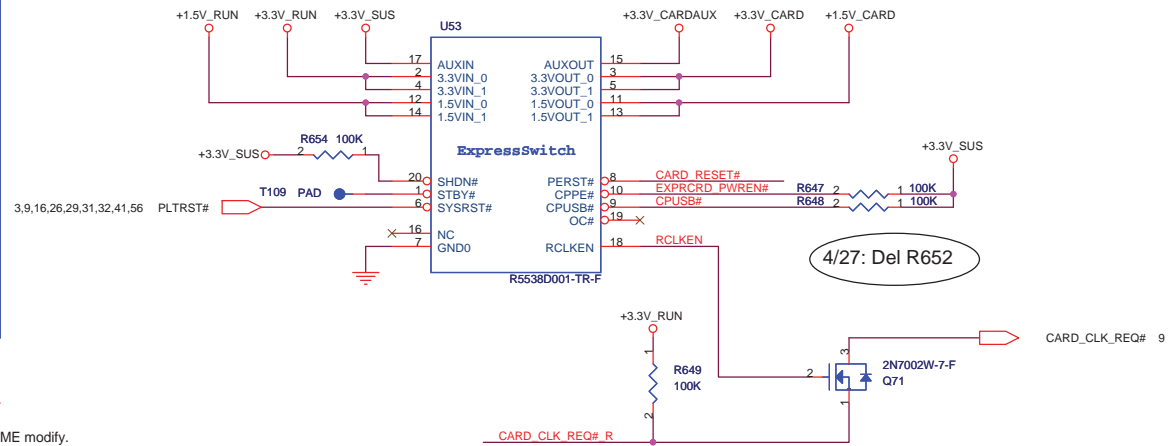
PCI-Express TX and RX direct to connector.

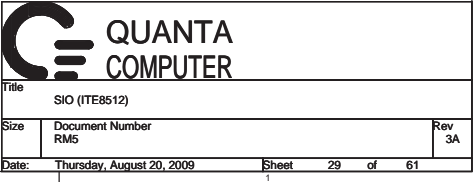


Scott_0814:Delete L31 as confirm with EMI.

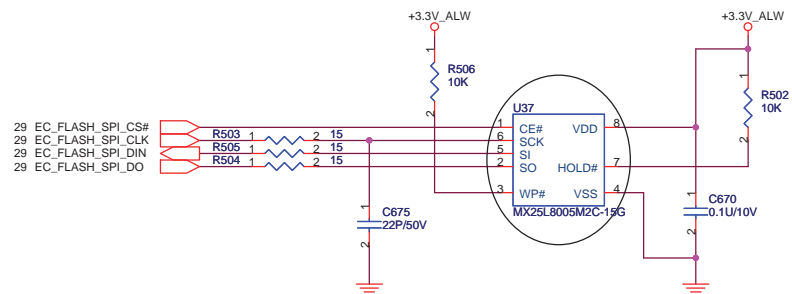


+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

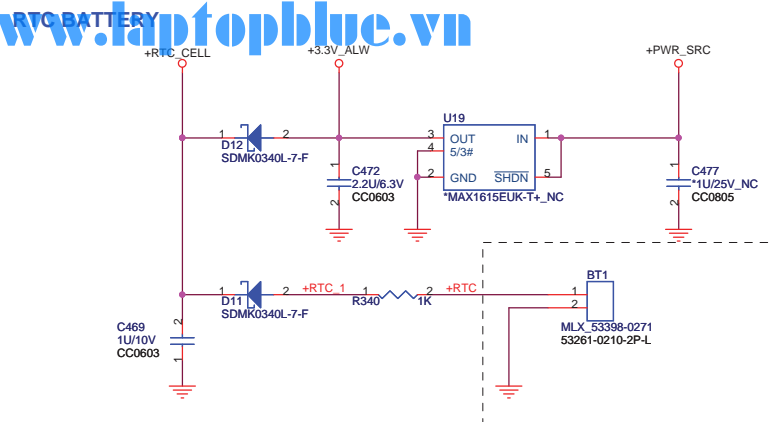




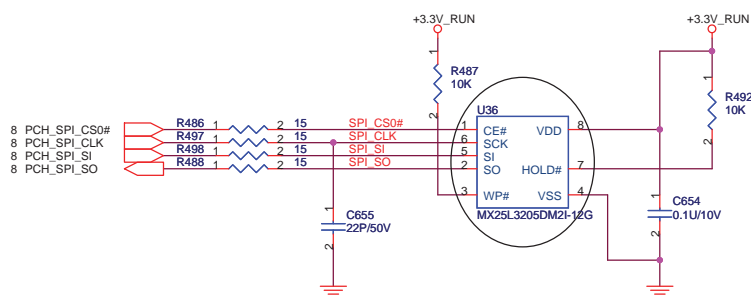
EC SPI ROM, 8Mbit (1M Byte) 5/12: Change U37 from 2MB to 1MB according to BIOS request!



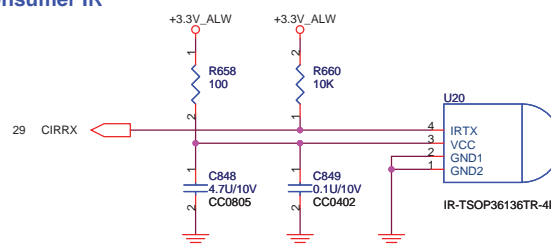
www.laptopblue.vn



PCH SPI ROM, (4M Byte) 5/12: Change U36 from 2MB to 4MB according to BIOS request!



Consumer IR

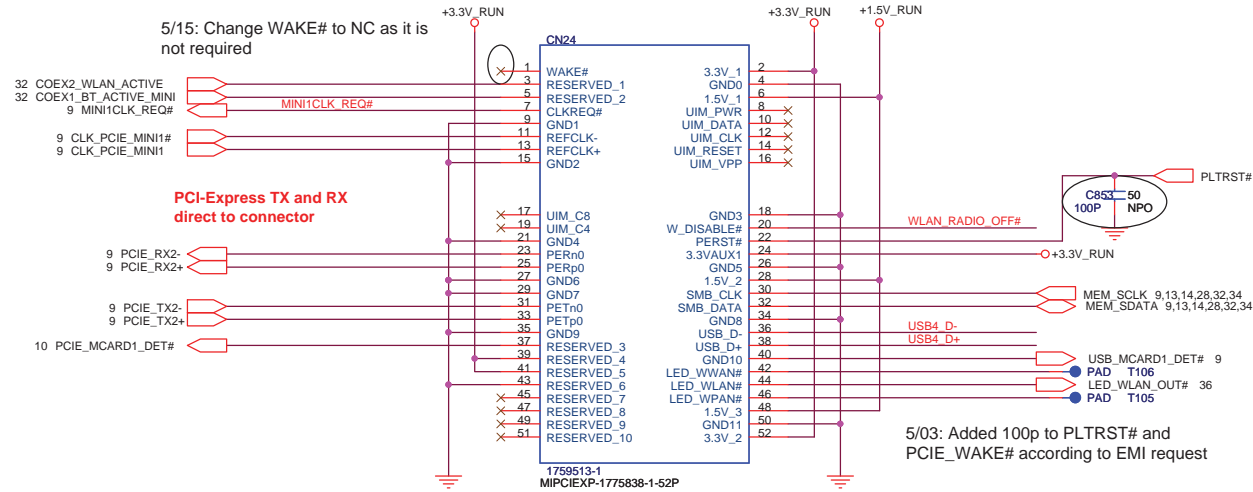


Title		
FLASH/ RTC/ CIR		
Size	Document Number	Rev
	RM5	3A
Date:	Thursday, August 20, 2009	Sheet 30 of 61

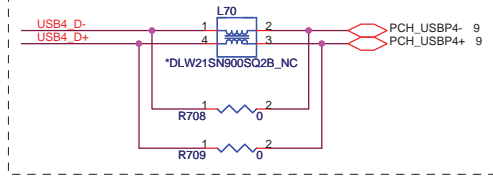
Mini Card Nut
H21
Mini Card Align (h6.6)

MiniCard WLAN Connector

5/15: Change WAKE# to NC as it is not required

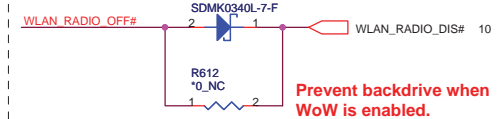


Reserved PAD for EMI

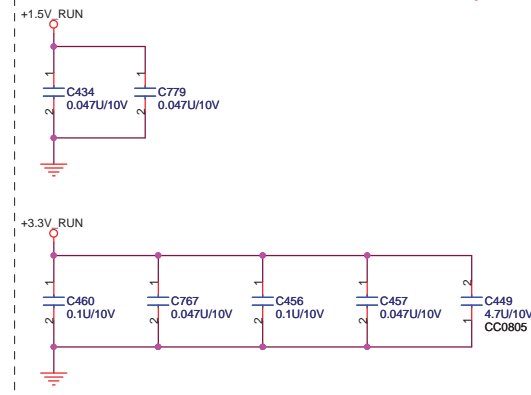


5/03: Added 100p to PLTRST# and PCIE_WAKE# according to EMI request

Support for WoW



Place caps close to connector.



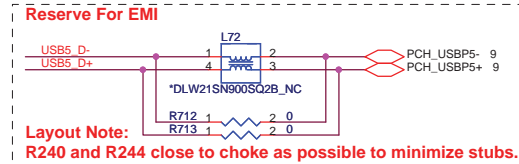
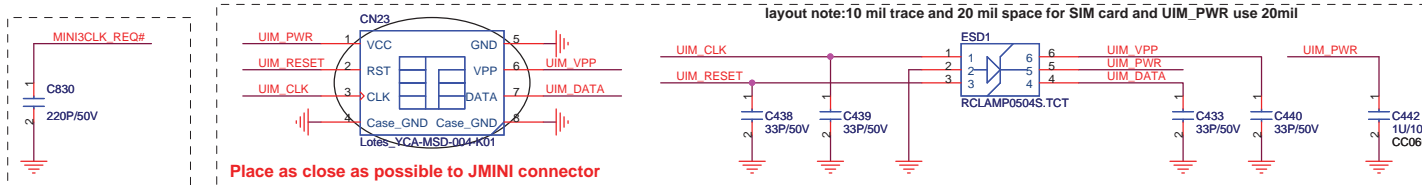
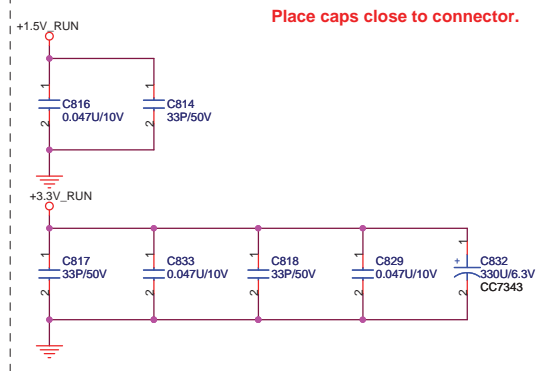
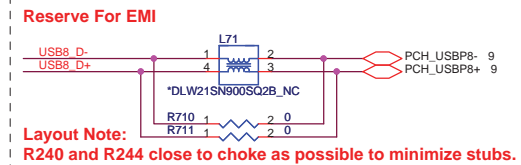
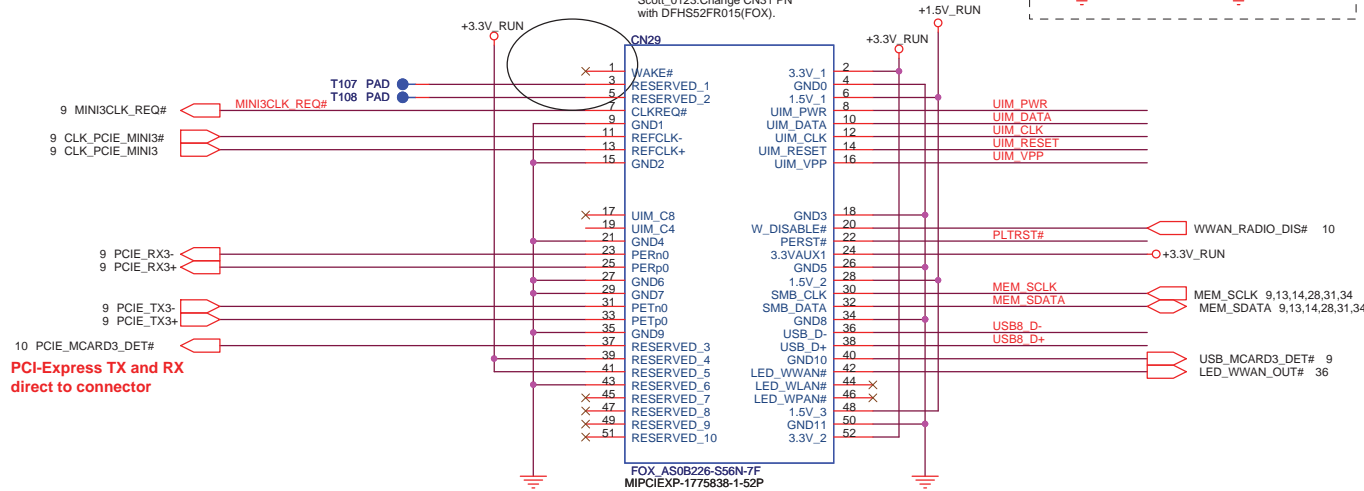
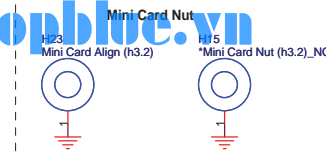
5/13: Pull up WAKE# to 3.3V_RUN
so as to avoid leakage

5/15: Change WAKE# to NC as it is
not required

5/08: Swap WWAN and WLAN according
to antenna team's suggestion

MiniCard WWAN Connector

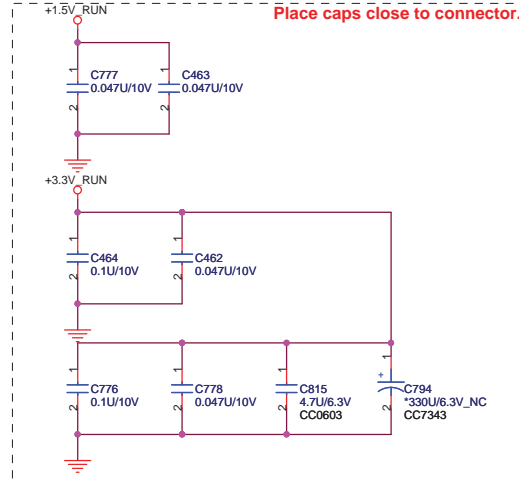
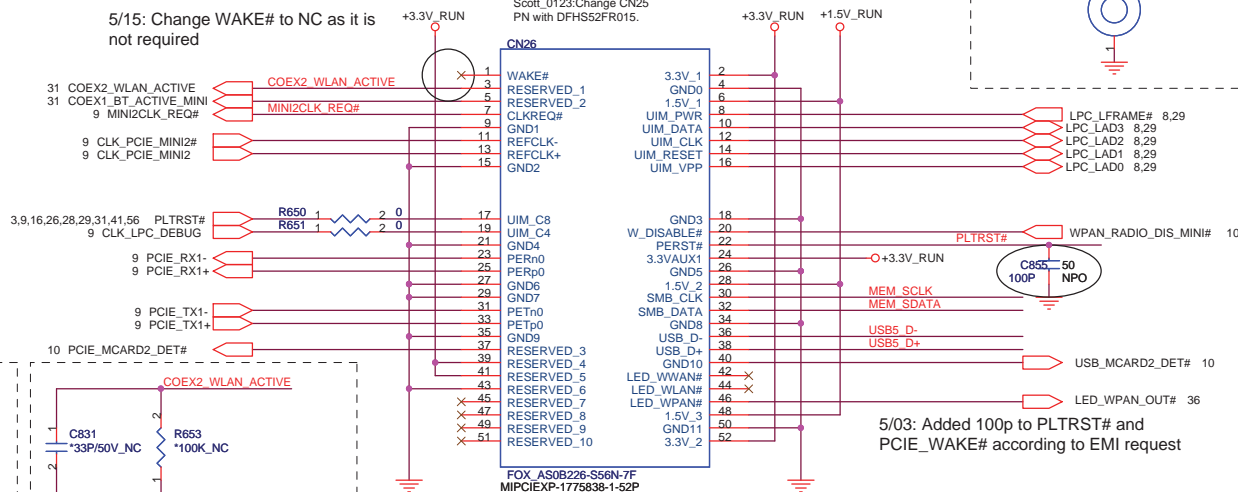
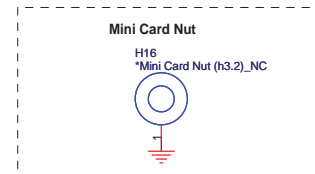
Scott_0123:Change CN31 PN
with DFHS52FR015(FOX).



MiniCard Robson, BT. UWB Connector

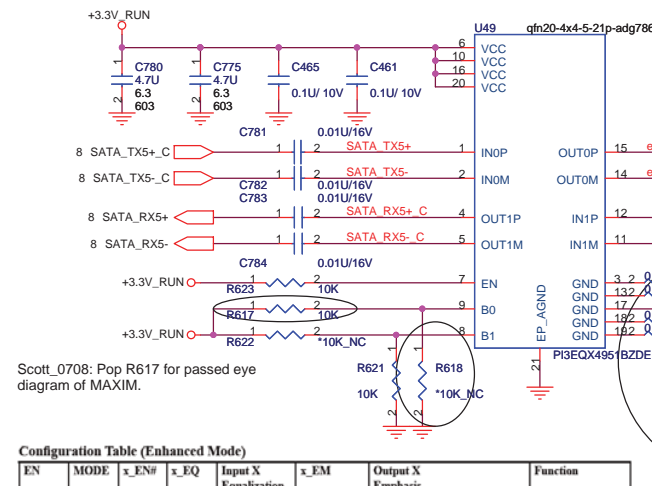
5/15: Change WAKE# to NC as it is
not required

Scott_0123:Change CN25
PN with DFHS52FR015.



Title MINI-CARD (WPAN,WWAN)		
Size RM5	Document Number	Rev 3A
Date: Thursday, August 20, 2009	Sheet 32	of 61

eSATA Re-driver IC

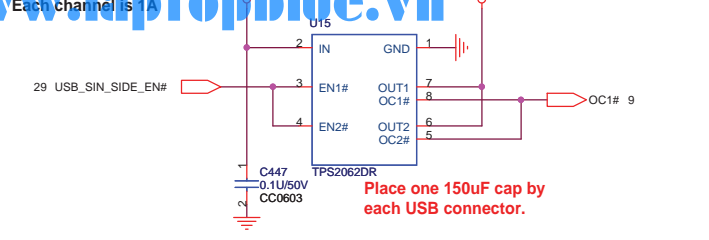


Configuration Table (Enhanced Mode)

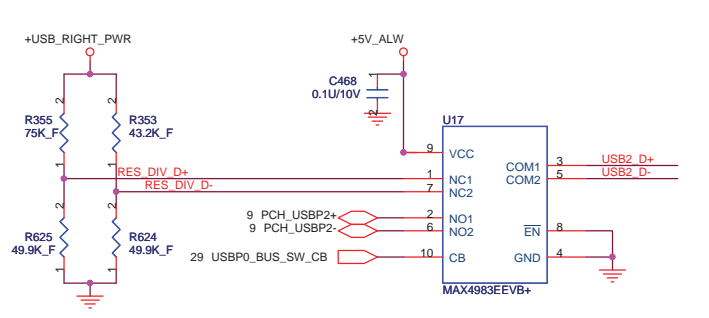
EN	MODE	x_EN#	x_EQ	Input X Equalization	x_EM	Output X Emphasis	Function
0	X	X	X	n/a	X	n/a	Chip Power Down
1	1	1	X	n/a	X	n/a	Chip enabled, Channel x disabled
1	1	0	0	2.5dB	1.1K to 15K resistor	Resistor Controlled, 6dB to 0dB (0)	Chip and channel enabled, low input equalization
1	1	0	1	6.5dB	1.1K to 15K resistor	Resistor Controlled, 6dB to 0dB (0)	Chip and channel enabled, high input equalization

5/11: Reserved 0 ohms for Pericom enhanced mode select
5/12: Change IC to Pericom as Maxim failed EA test
6/23: NC according to Pericom recommendation!

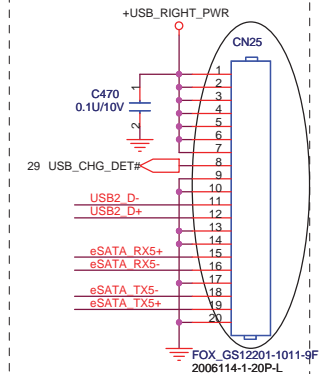
USB POWER SW



USB Power Share



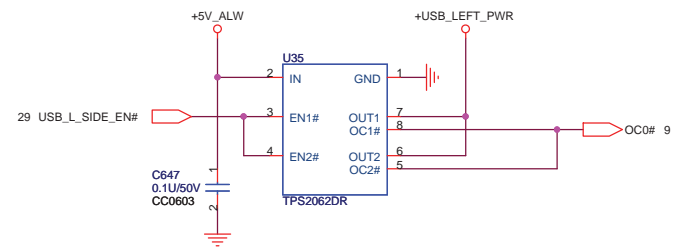
eSATA CONN



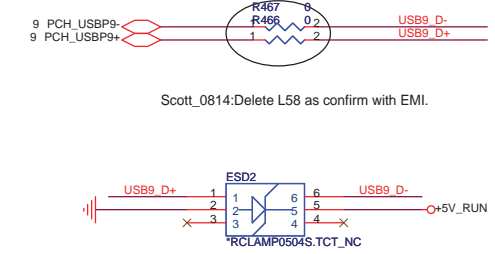
5/13: Change Connector to Foxconn to avoid material shortage for Tyco

USB POWER SW

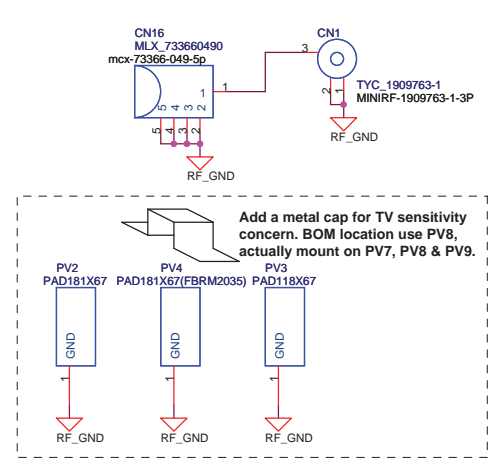
Each channel is 1A



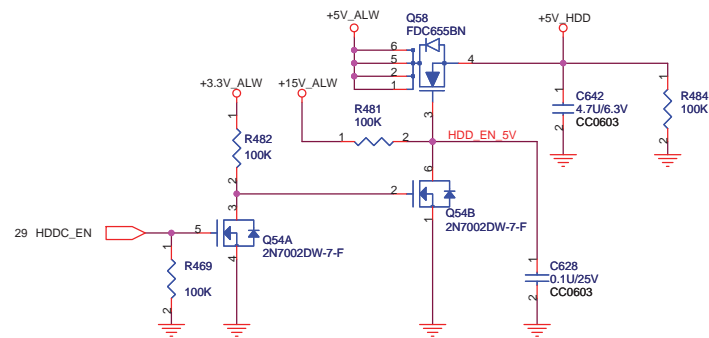
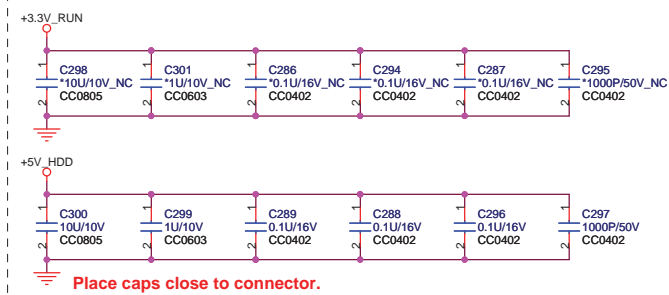
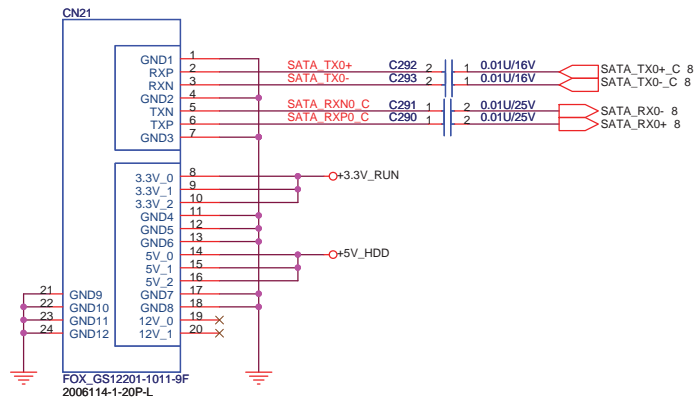
TV module



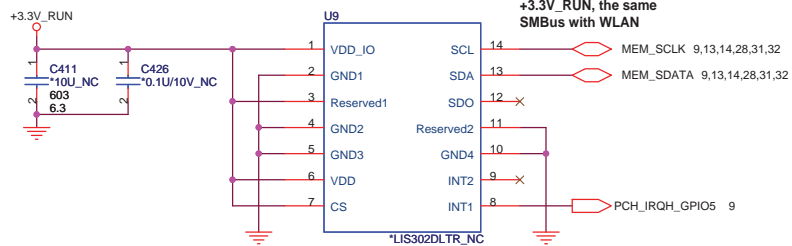
TV RF Jack & Microwave connector



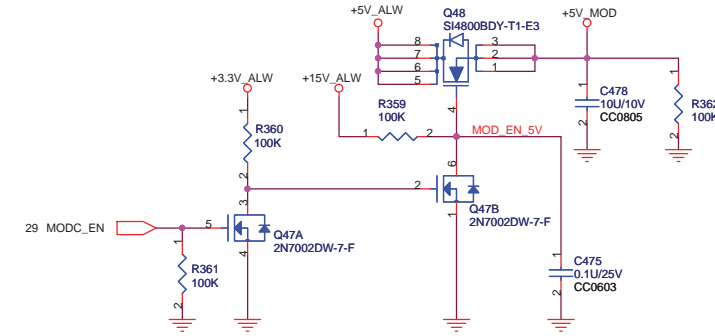
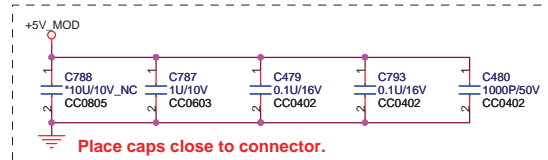
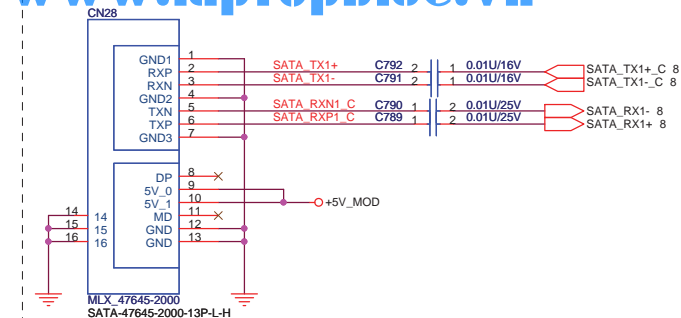
SATA Connector



3-axis Fall Sensor (HDD data protector)



www.laptopblue.vn



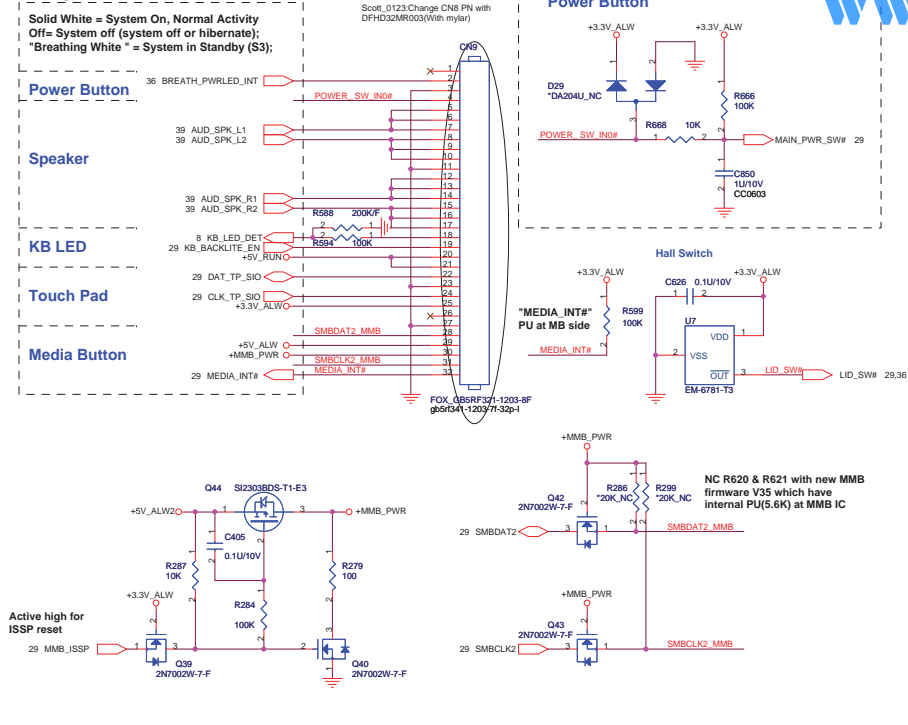
Solid White = System On, Normal Activity
Off= System off (system off or hibernate);
"Breathing White" = System in Standby (S3);

Speaker

KB LED

Touch Pad

Media Button

[illegible][illegible]

5/03: Populate according to EMI request!

5/12: Change from CA110084N04 to
CA110084N39 due to material shortage!

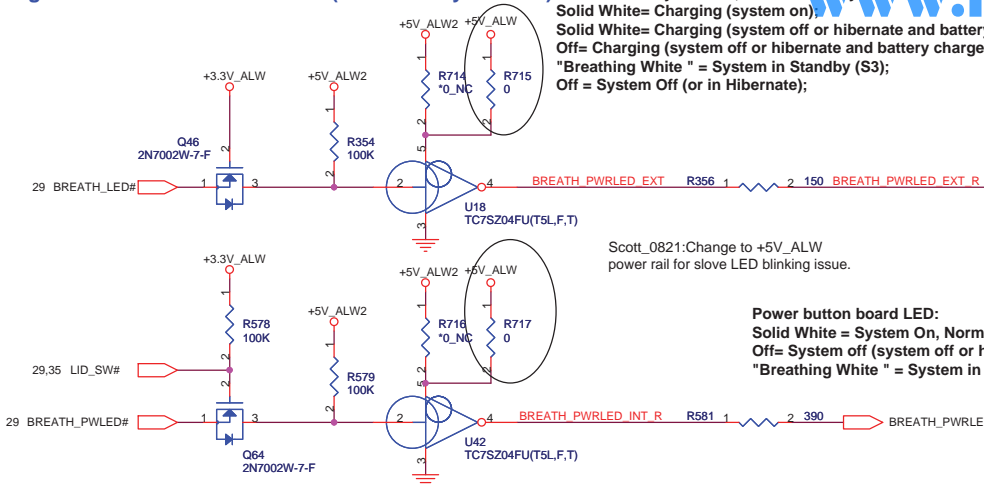


Title			
KB/ CCD/ UI			
Size	Document Number		Rev
	RM5		3
Date:	Thursday, August 20, 2009	Sheet	35 of 61

Hinge & Power Button board LED (PWR/Battery indicator)

Hinge LED

Solid White= System On, Normal Activity
Solid White= Charging (system on);
Solid White= Charging (system off or hibernate and battery charge <90%);
Off= Charging (system off or hibernate and battery charge > 90%);
"Breathing White " = System in Standby (S3);
Off = System Off (or in Hibernate);

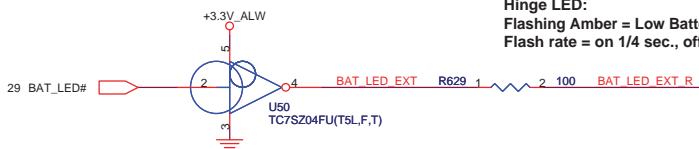


Scott_0821:Change to +5V_ALW power rail for solve LED blinking issue.

Power button board LED:
Solid White = System On, Normal Activity
Off= System off (system off or hibernate);
"Breathing White " = System in Standby (S3)

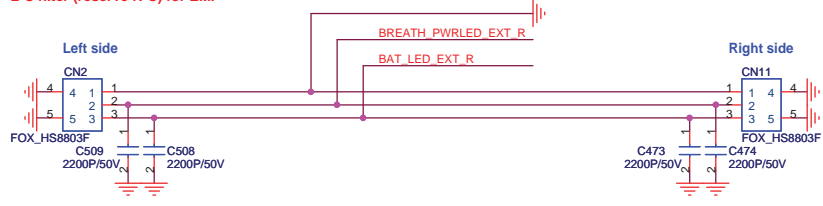
Hinge LED:

Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%
Flash rate = on 1/4 sec., off 3/4 sec.



Hinge LED (PWR/Battery indicator)

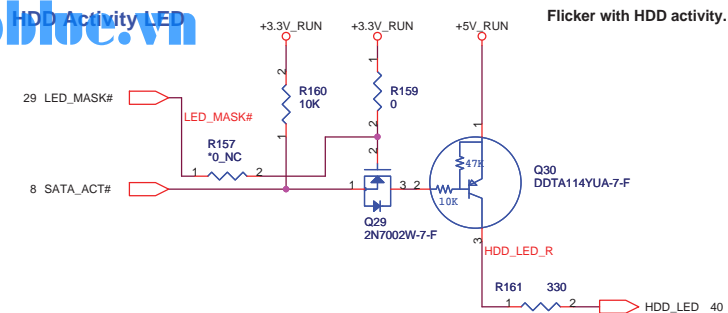
L-C filter (reserve R-C) for EMI



Solid White= System On, Normal Activity
Solid White= Charging (system on);
Solid White= Charging (system off or hibernate and battery charge <90%);
Off= Charging (system off or hibernate and battery charge > 90%);
"Breathing White " = System in Standby (S3);
Off = System Off (or in Hibernate);

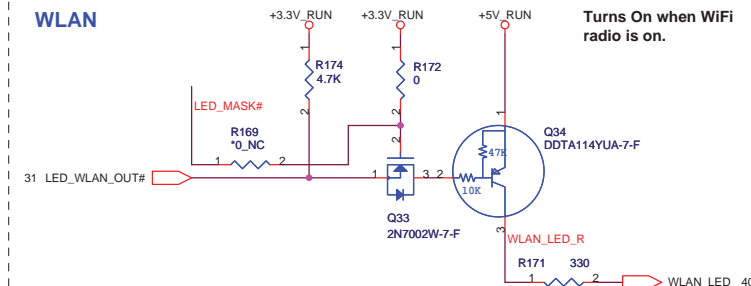
Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%
Flash rate = on 1/4 sec., off 3/4 sec.

HDD Activity LED



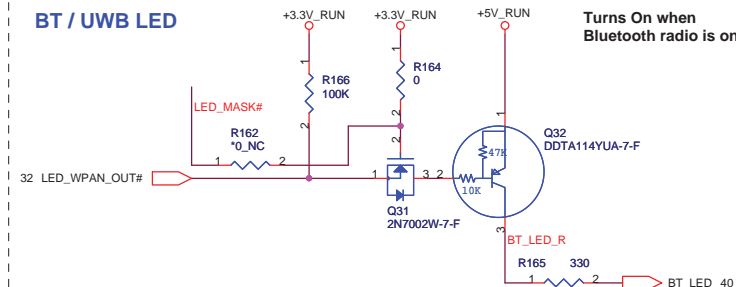
Flicker with HDD activity.

WLAN



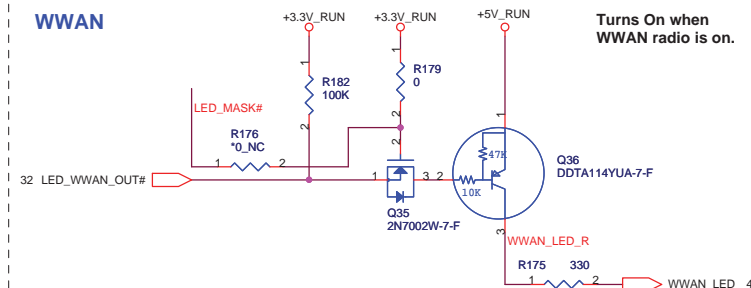
Turns On when WiFi radio is on.

BT / UWB LED



Turns On when Bluetooth radio is on.

WWAN

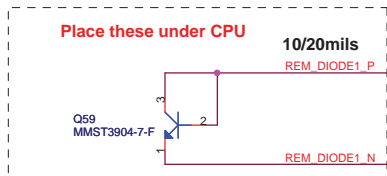
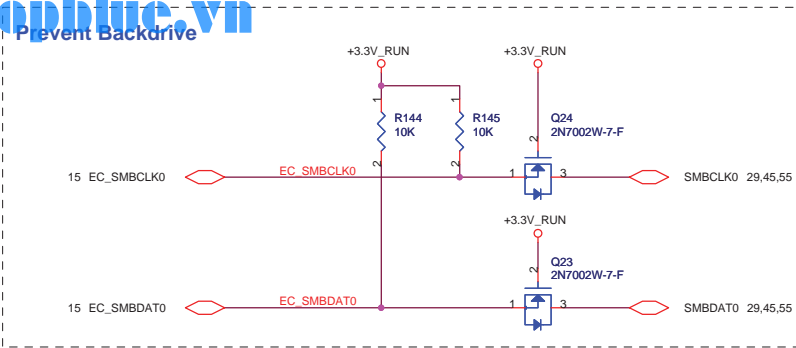
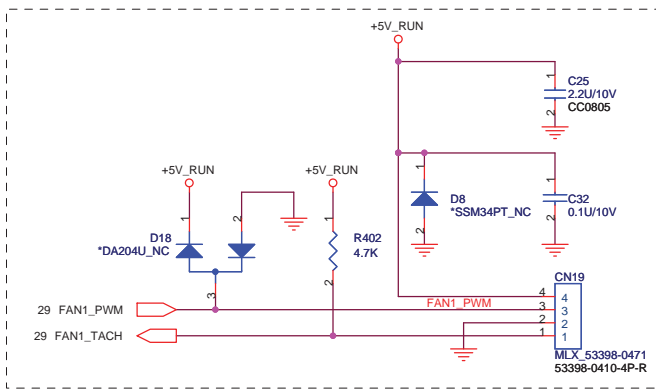


Turns On when WWAN radio is on.

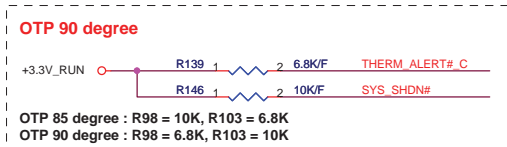
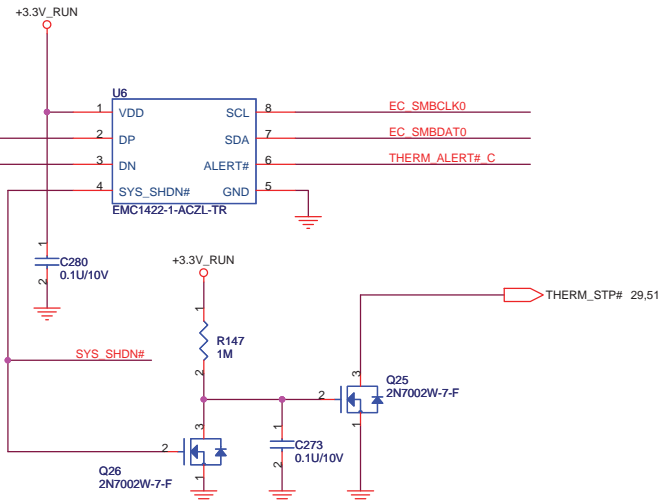


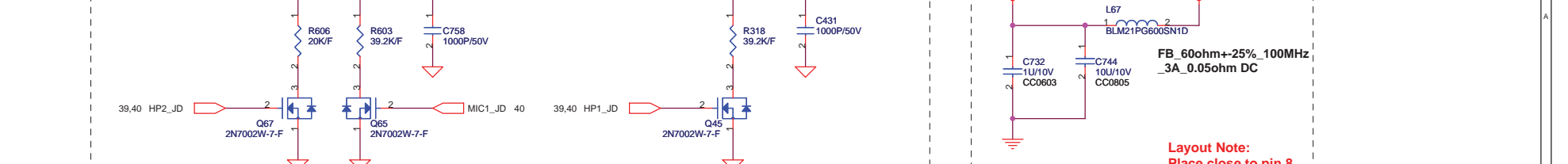
Title		
LED		
Size	Document Number	Rev
	RM5	3A
Date:	Friday, August 21, 2009	Sheet 36 of 61

Prevent Backdrive

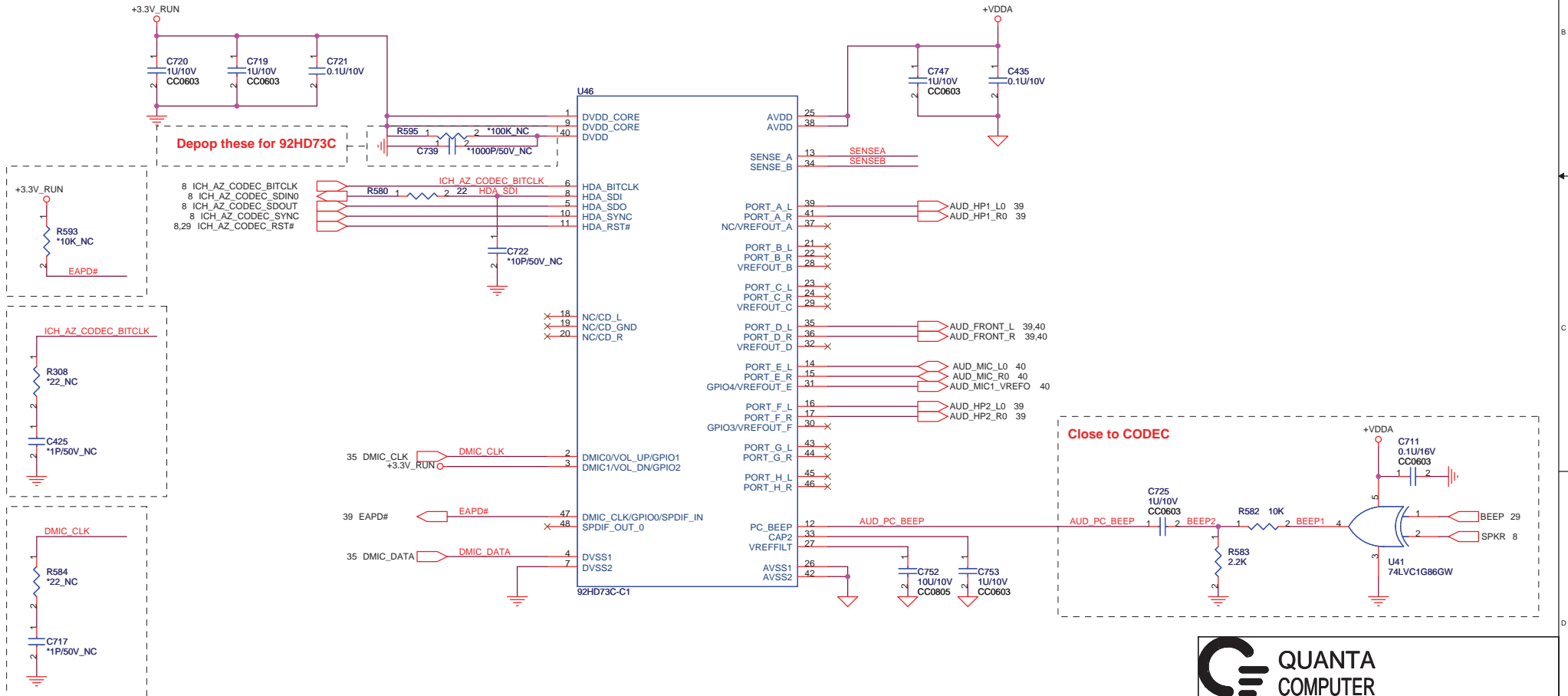


1.Place C579 close to EMC1422
Total capacitance between D+/D- is 2200pF(max)



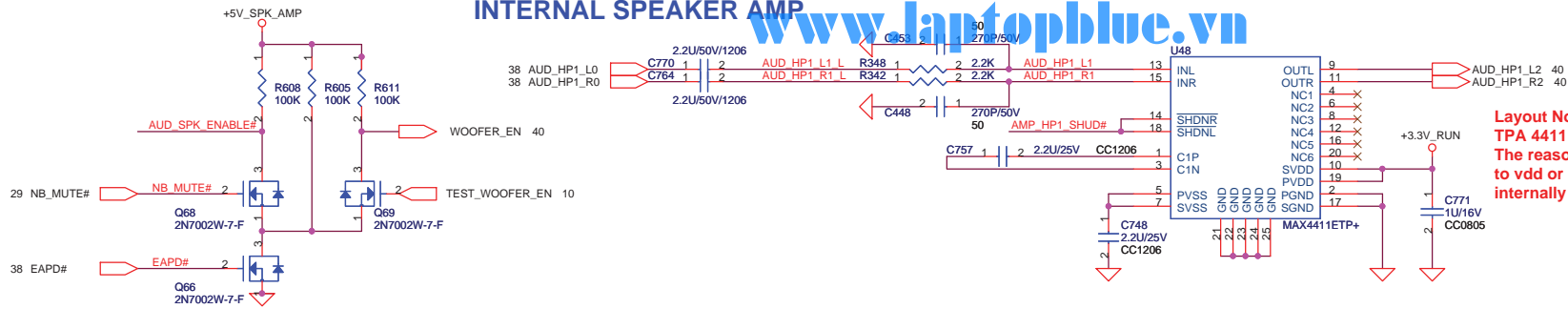


AZALIA (HD) CODEC

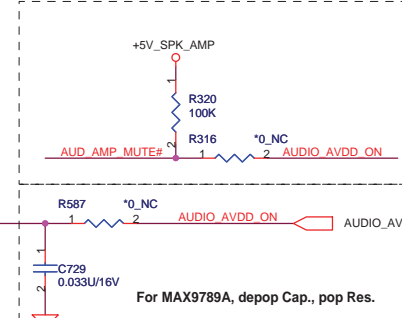
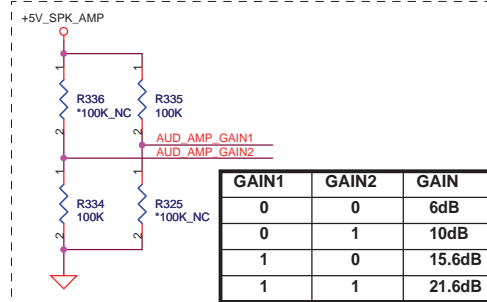
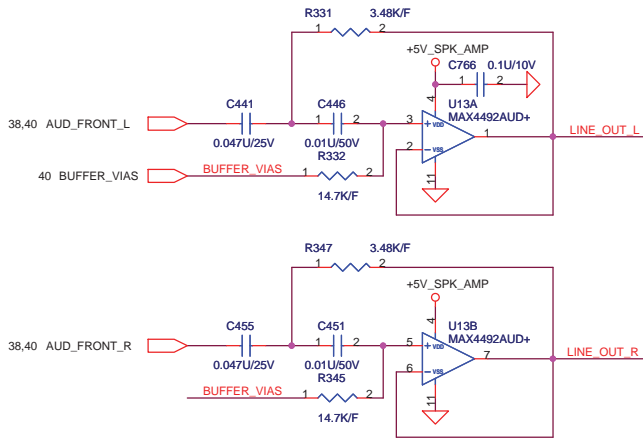
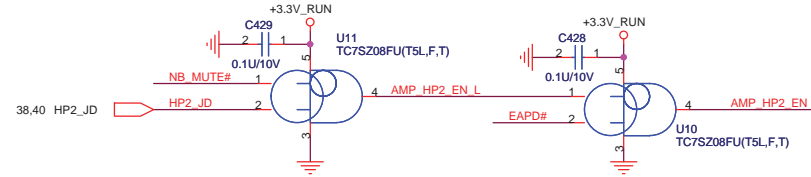
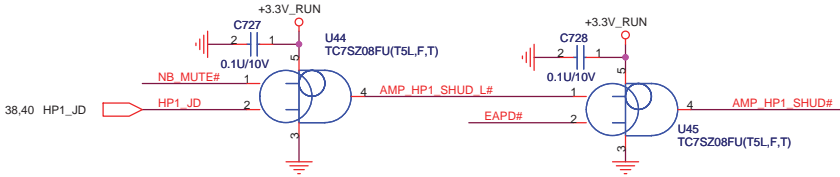


INTERNAL SPEAKER AMP

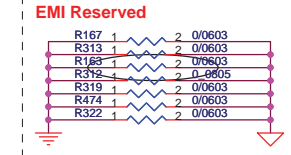
www.laptopblue.vn



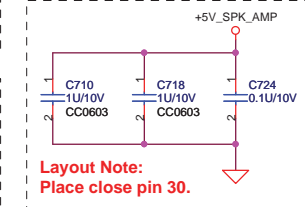
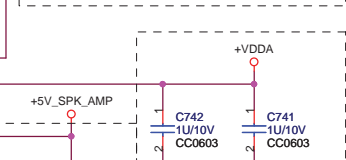
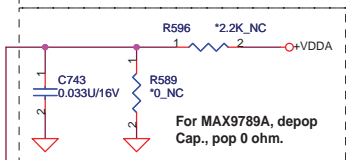
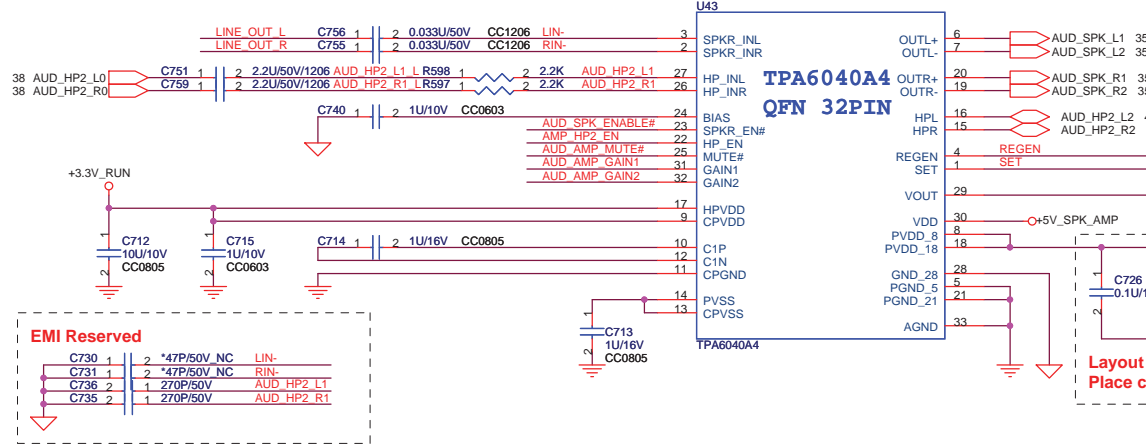
Layout Note:
TPA 4411 : cannot connect EP to GND.
The reason that we can't solder the pad to vdd or ground is because it is internally connected to VSS.



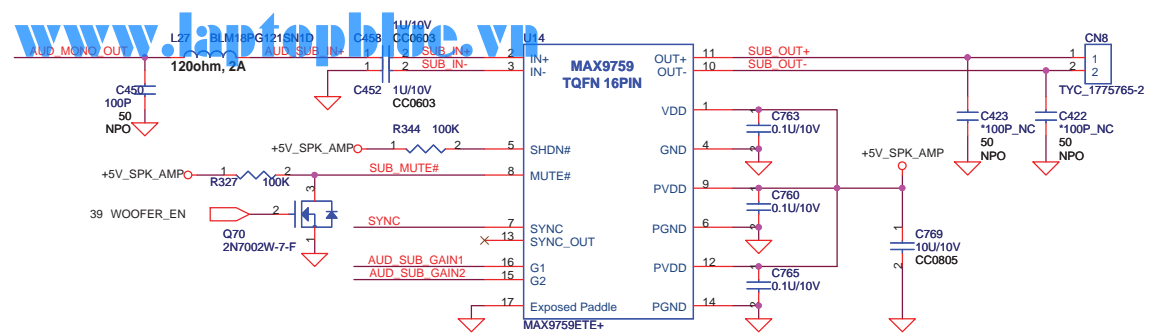
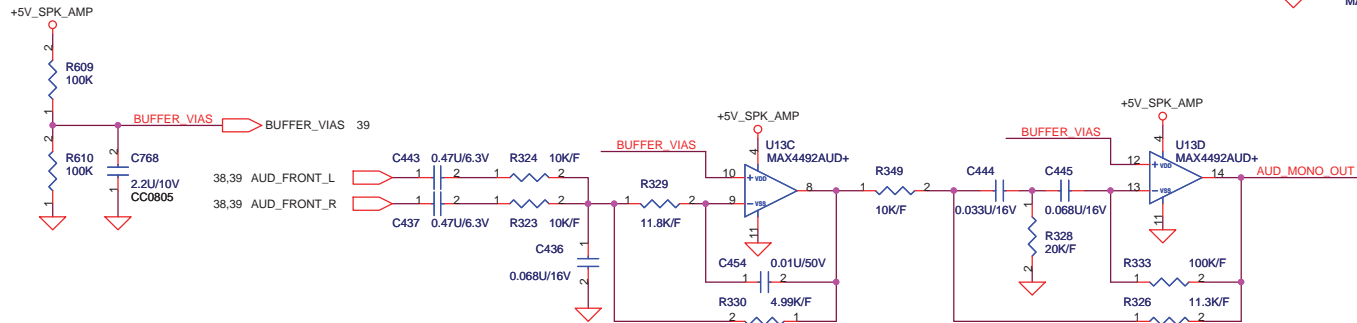
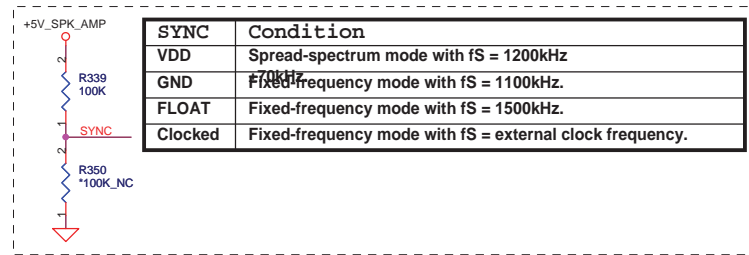
Layout Note:
MAX9789A/TPA6040A : need to connect EP (exposed paddle) to GND.
TPA 4411 : cannot connect EP to GND.
MAX 4411: can connect EP to GND.



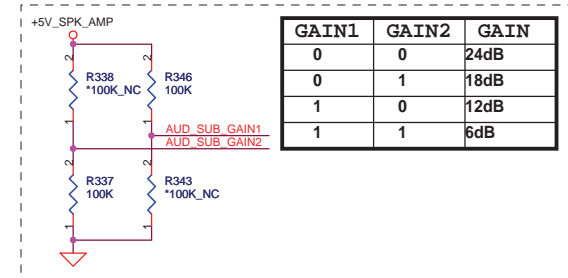
7/01: Populate according to EMI request!



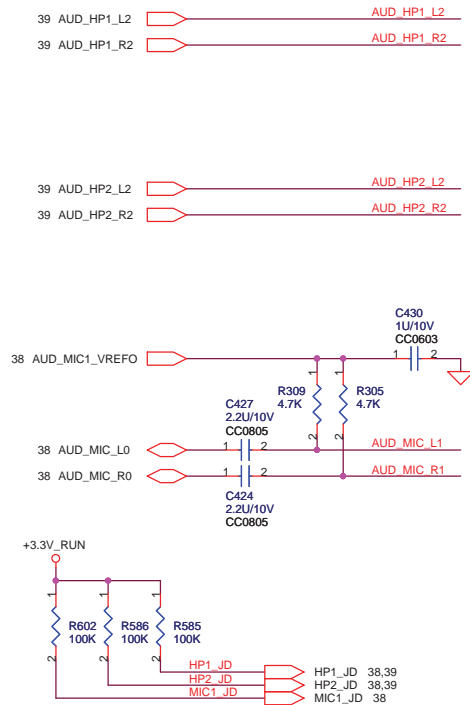
INTERNAL SUBWOOFER AMP



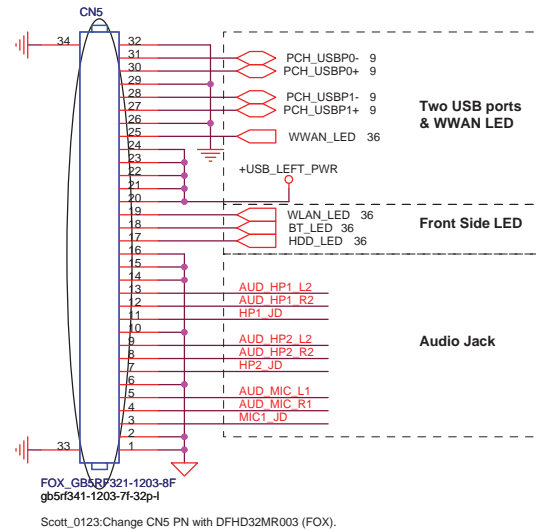
GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB



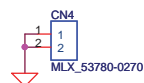
Ambient Parts of Headphone & MIC Jack



To IB(IO Board) connector



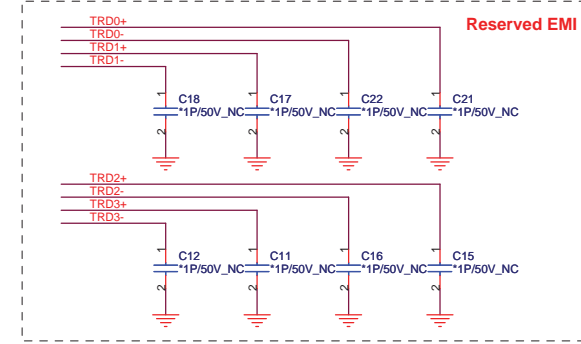
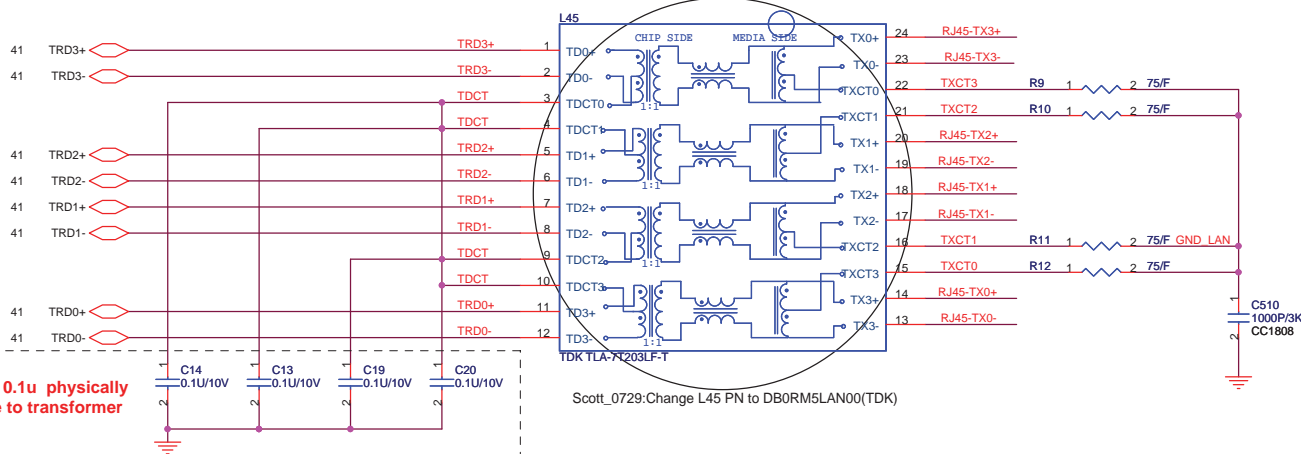
Adding additional AGND



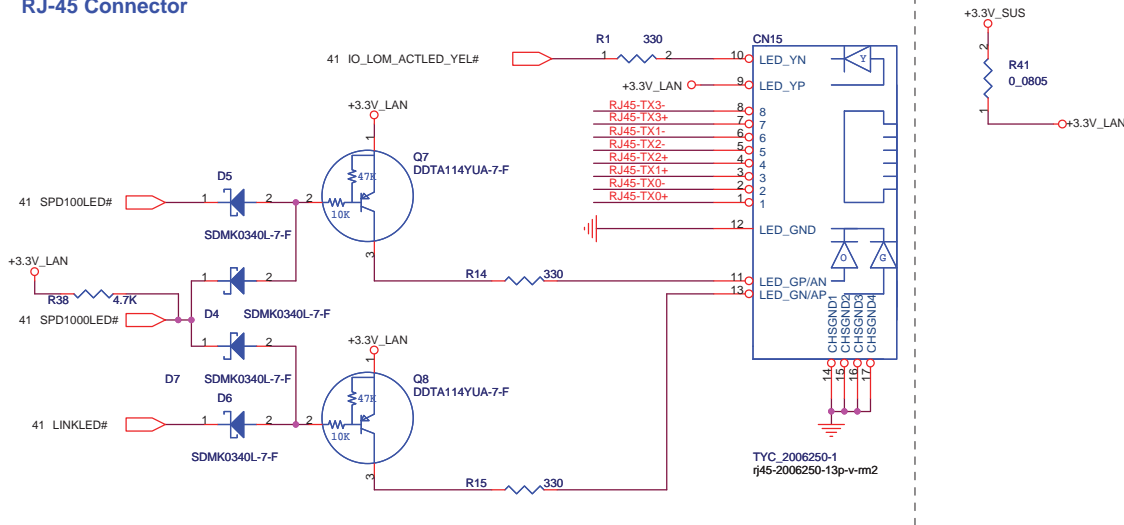
TRANSFORMER

www.laptopblue.vn

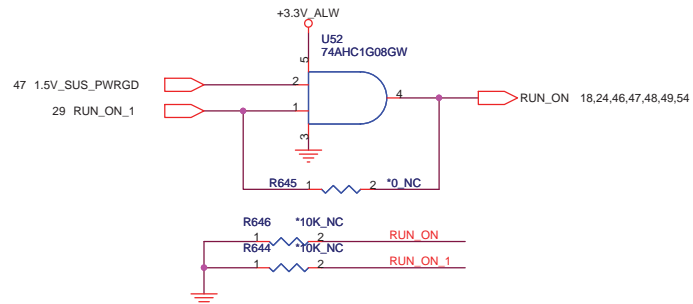
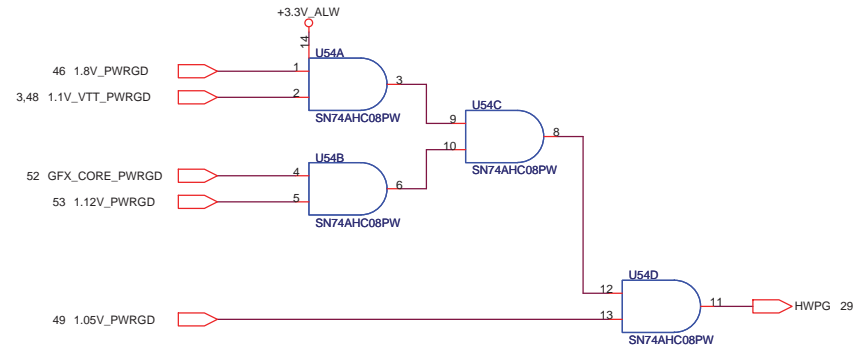
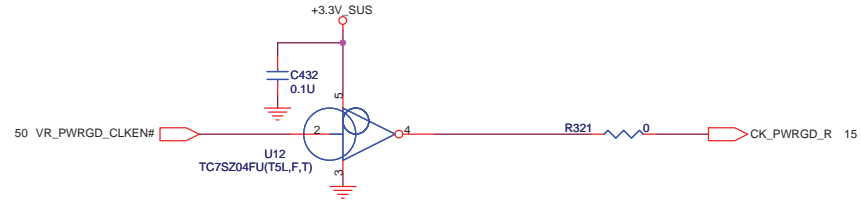
Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.



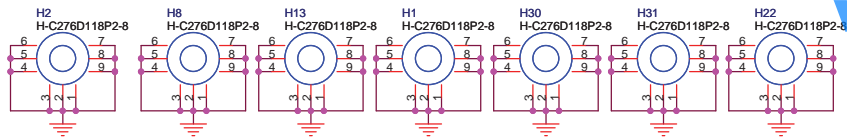
RJ-45 Connector



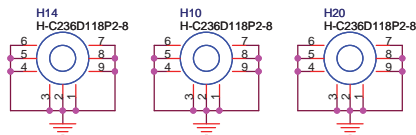
Title			LAN SWITCH
Size	Document Number	Rev	
	RM5	3A	
Date:	Thursday, August 20, 2009	Sheet	42 of 61



H-C276D118P2-8 * 7



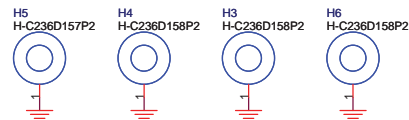
H-C236D118P2-8 * 3



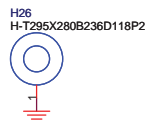
h-c236d197p2 * 1



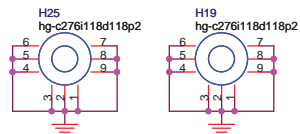
H-C236D158P2 * 4



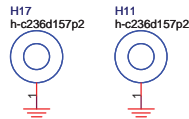
H-T295X280B236D118P2 * 1



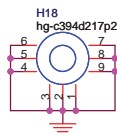
hg-c276i118d118p2 * 2



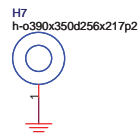
h-c236d157p2 * 2



h-c394d260p2 * 1



H-C394D260P2-8 * 1



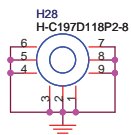
Scott_0731: change H7 & H18 footprint as ME change

Scott_0812:Delete H7 Pin2~Pin9 for layout requite.

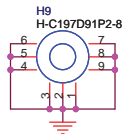
h-c236d236n * 2



H-C197D118P2-8 * 1



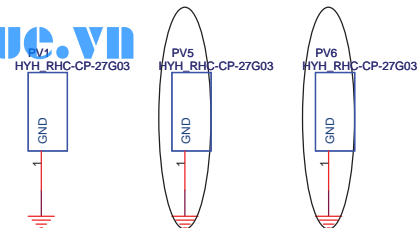
H-C197D91P2-8 * 1



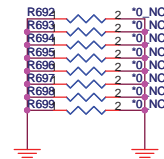
h-o205x157d138x91p2 * 1



www.laptopblue.vn



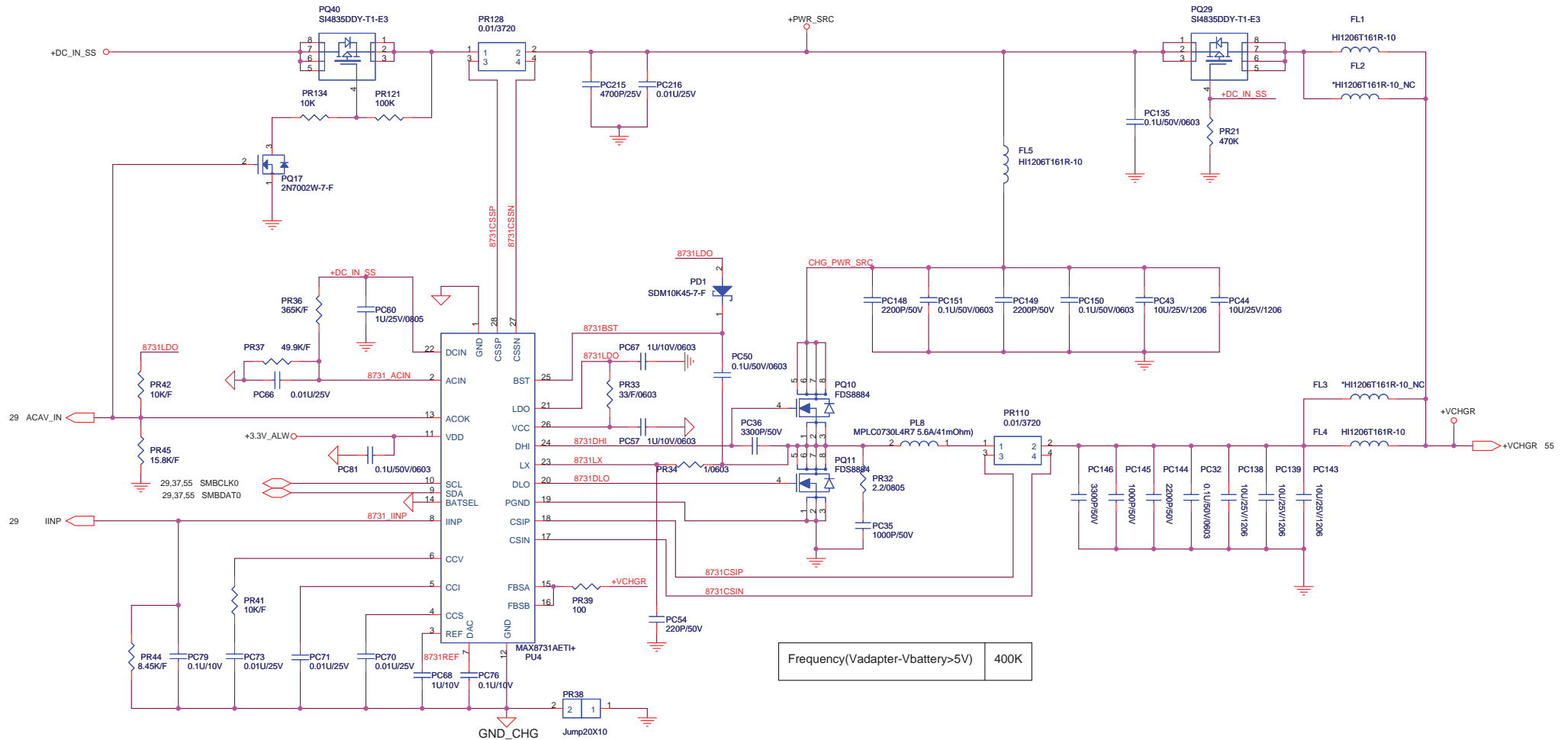
Scott_0701:: Added PV6 according to EMI's suggestion

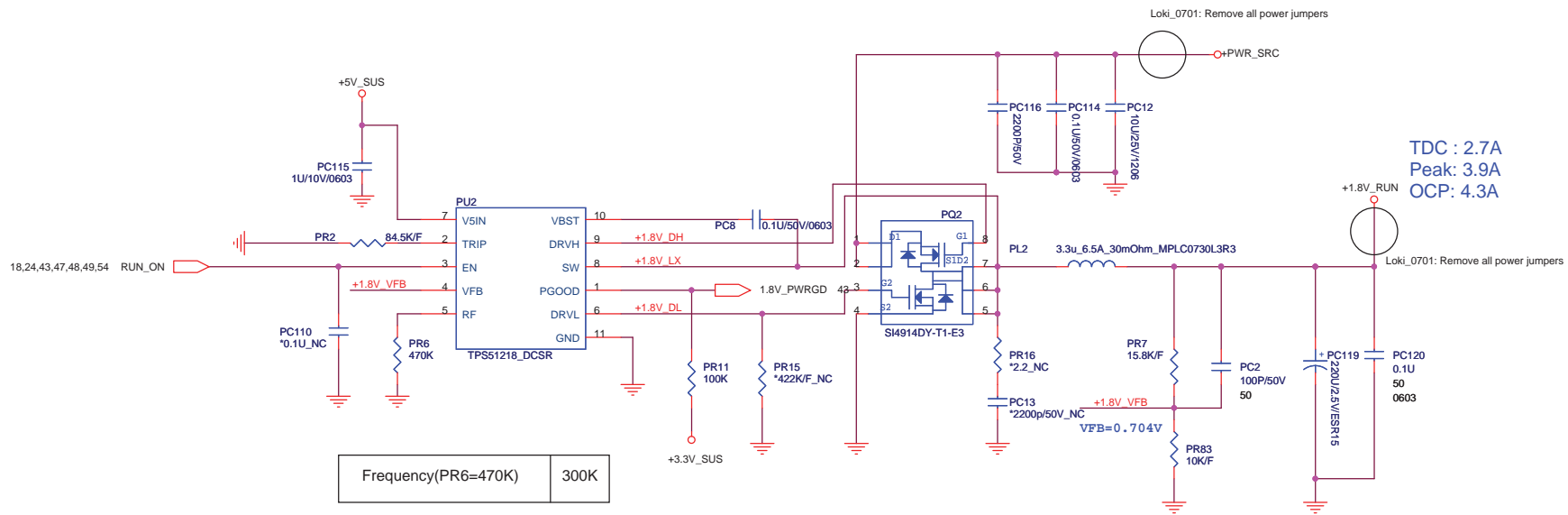


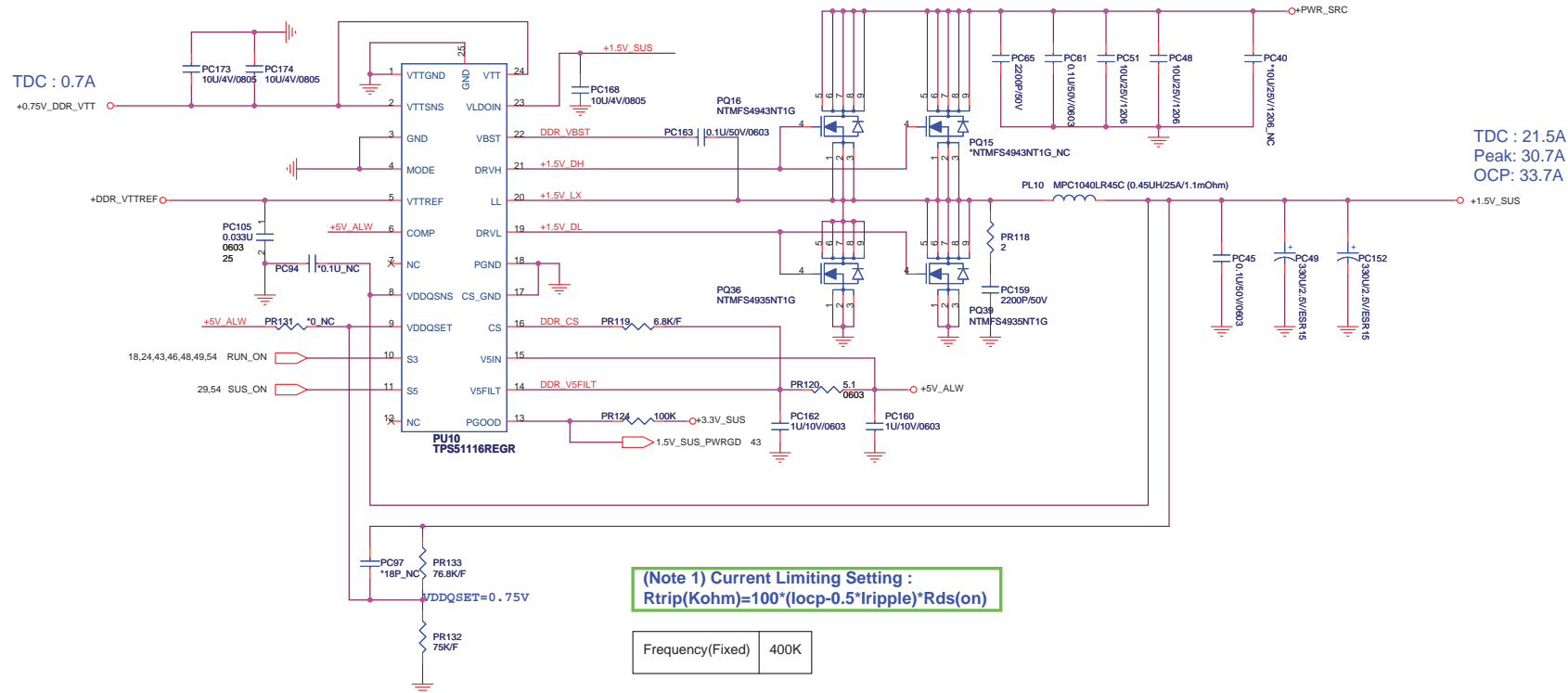
Scott_0703:Add 8pcs 0ohm resistors R692~R699 for thermal issue as EMI concern.

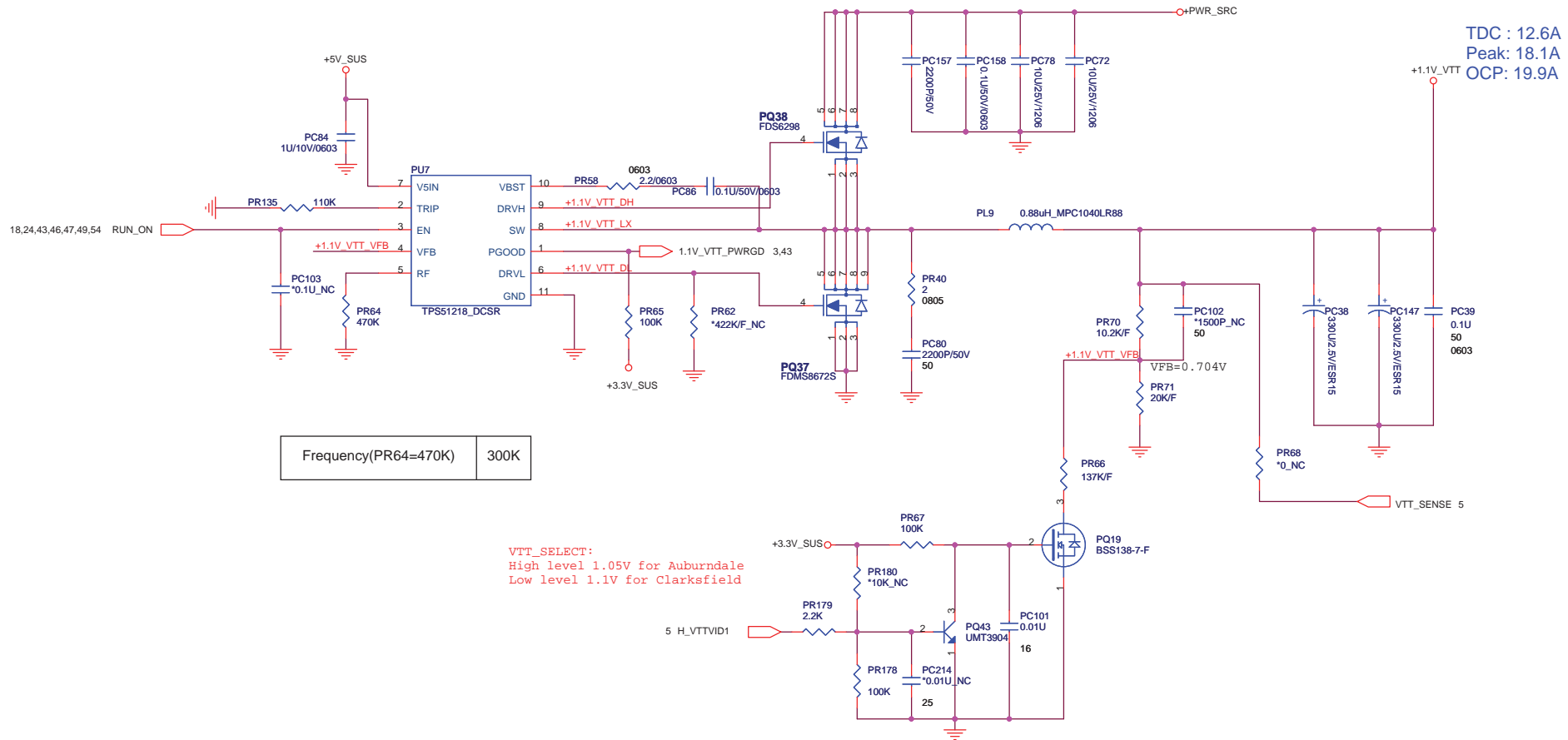
Scott_0707: Reserver R692~R699.

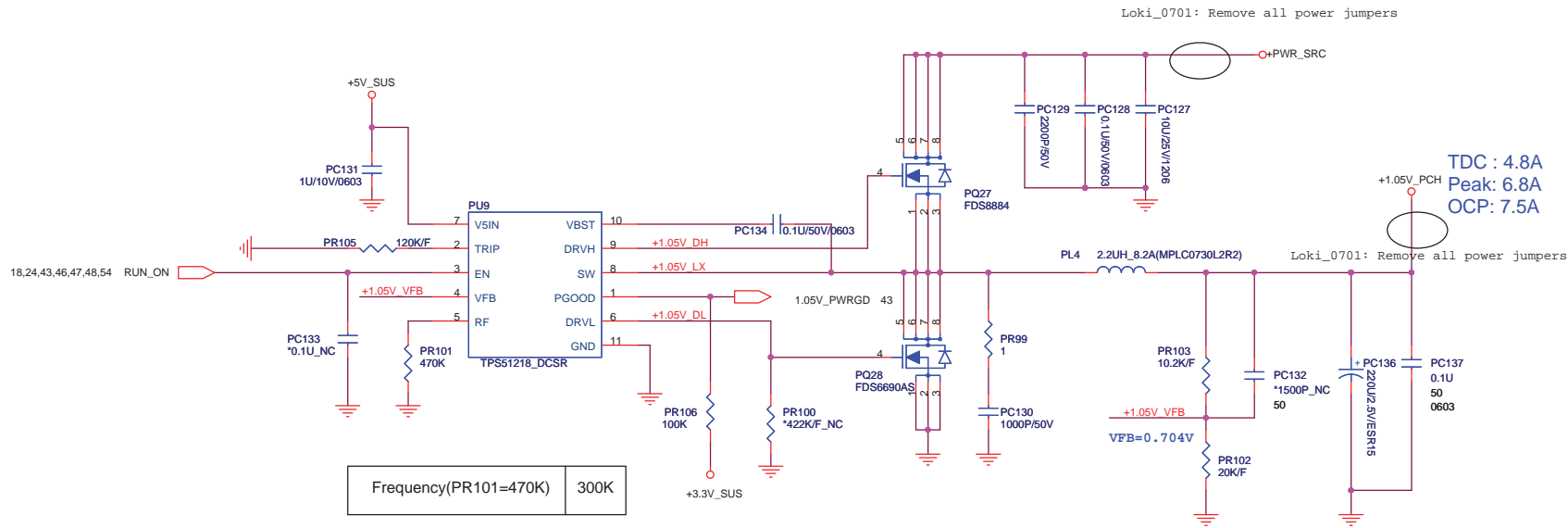








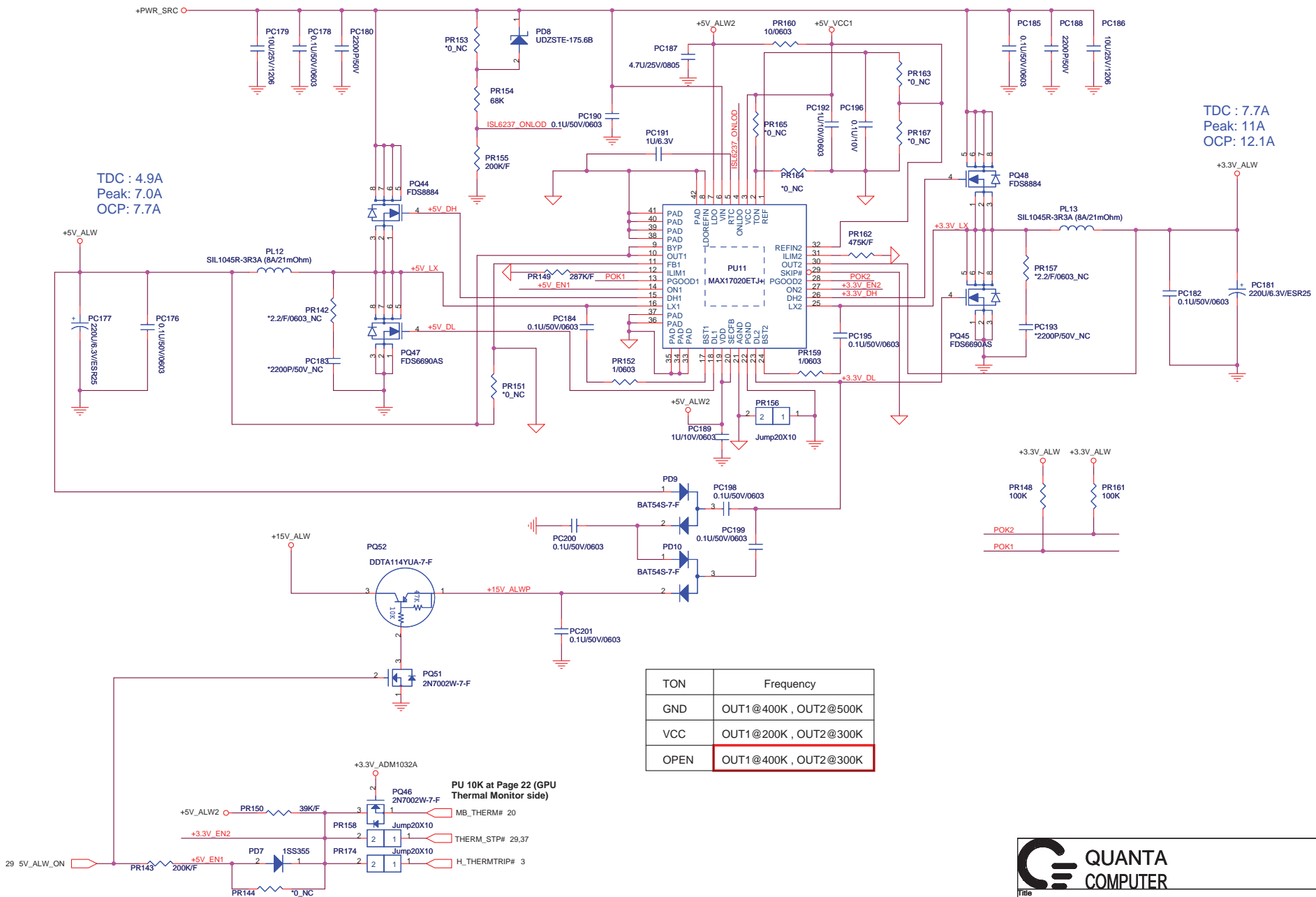




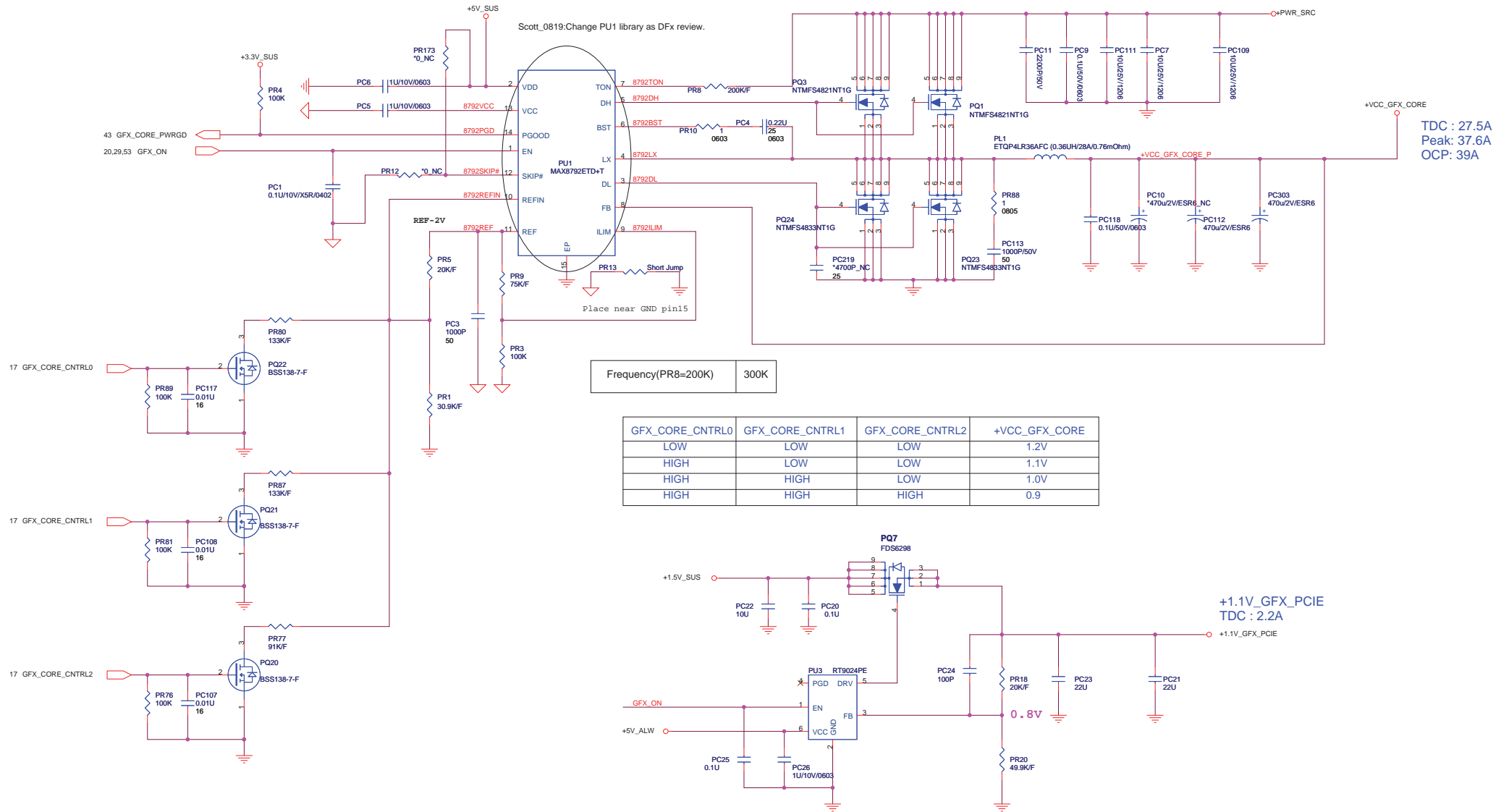
• **+PWR_SRC**
Loki_0813: De-pop PC171, PC169 and PC156 because acoustic noise is passed

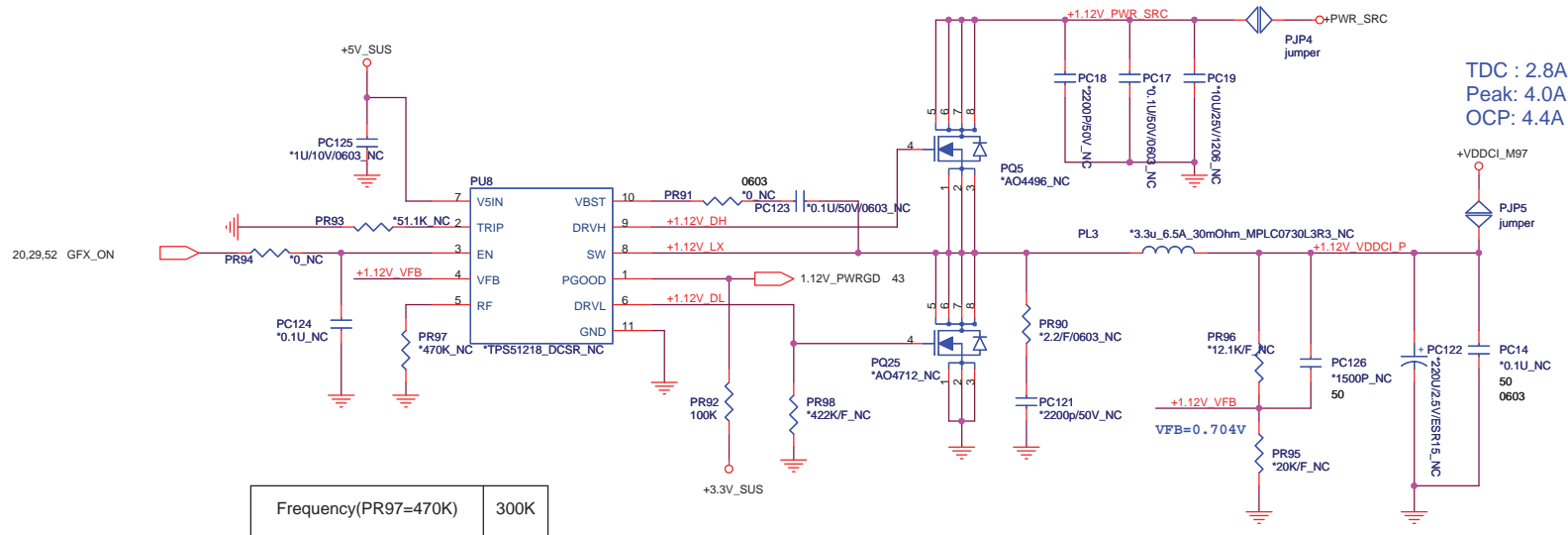


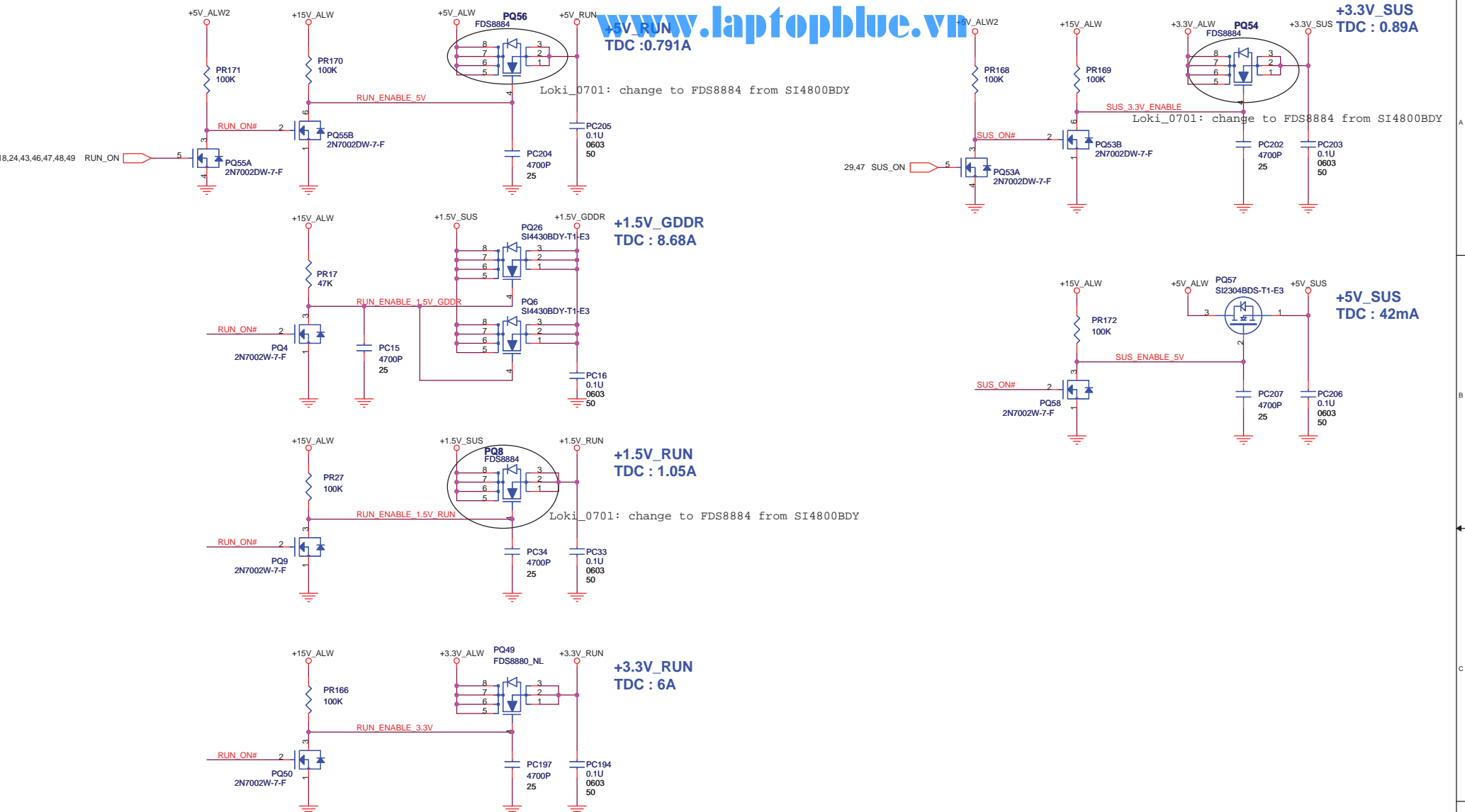
Title +VCC_CORE (MAX17030)			
Size	Document Number RM15		Rev 3A
Date:	Thursday, August 20, 2009	Sheet 50 of 61	



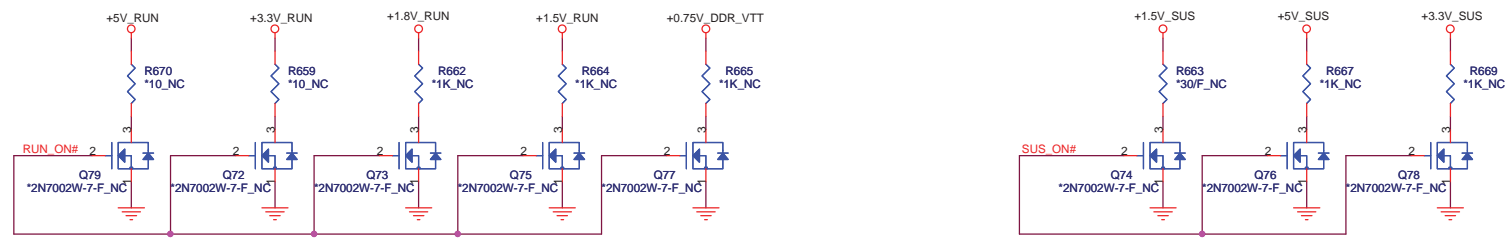
TON	Frequency
GND	OUT1@400K , OUT2@500K
VCC	OUT1@200K , OUT2@300K
OPEN	OUT1@400K , OUT2@300K





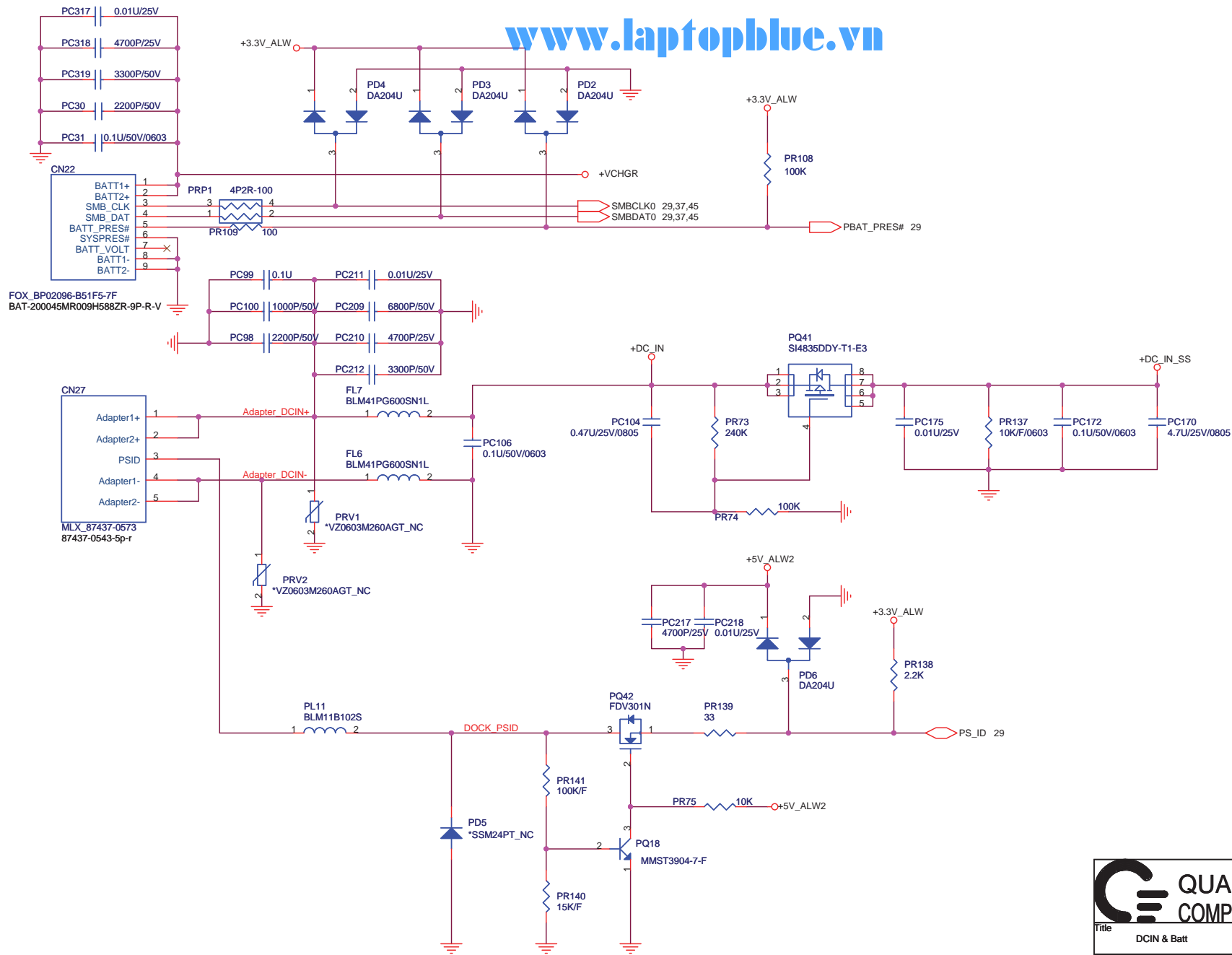


Reserve discharge path



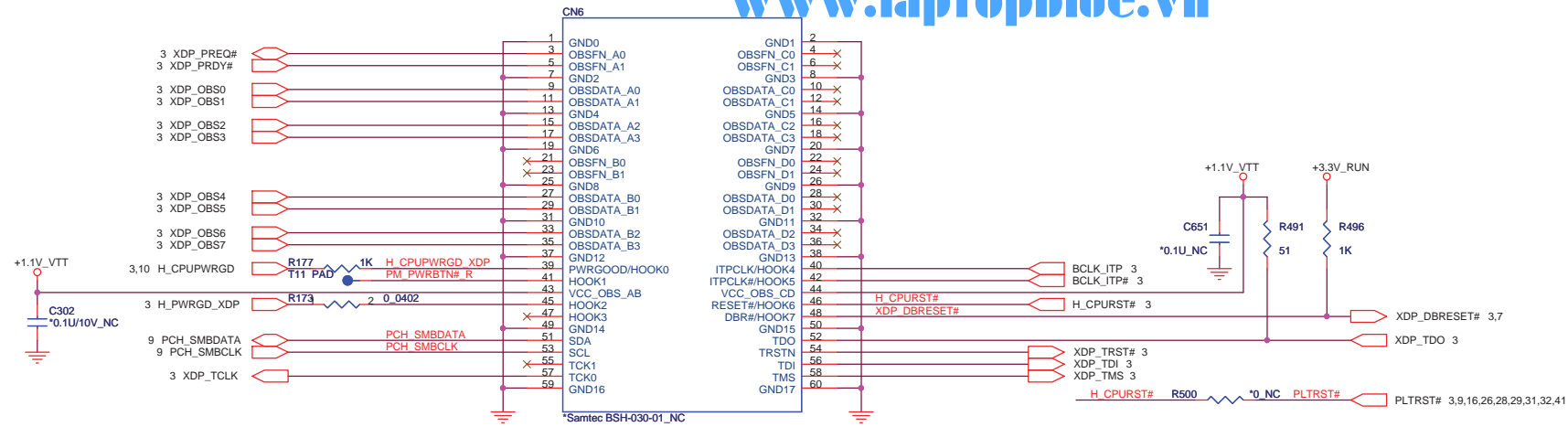
**QUANTA
COMPUTER**

Title RUN POWER SW		
Size RM5	Document Number	Rev 3A
Date: Thursday, August 20, 2009	Sheet 54	of 61



Title			DCIN & Batt
Size	Document Number	Rev	3A
	RMS		
Date:	Thursday, August 20, 2009	Sheet	55 of 61

CPU XDP

www.laptopblue.vn

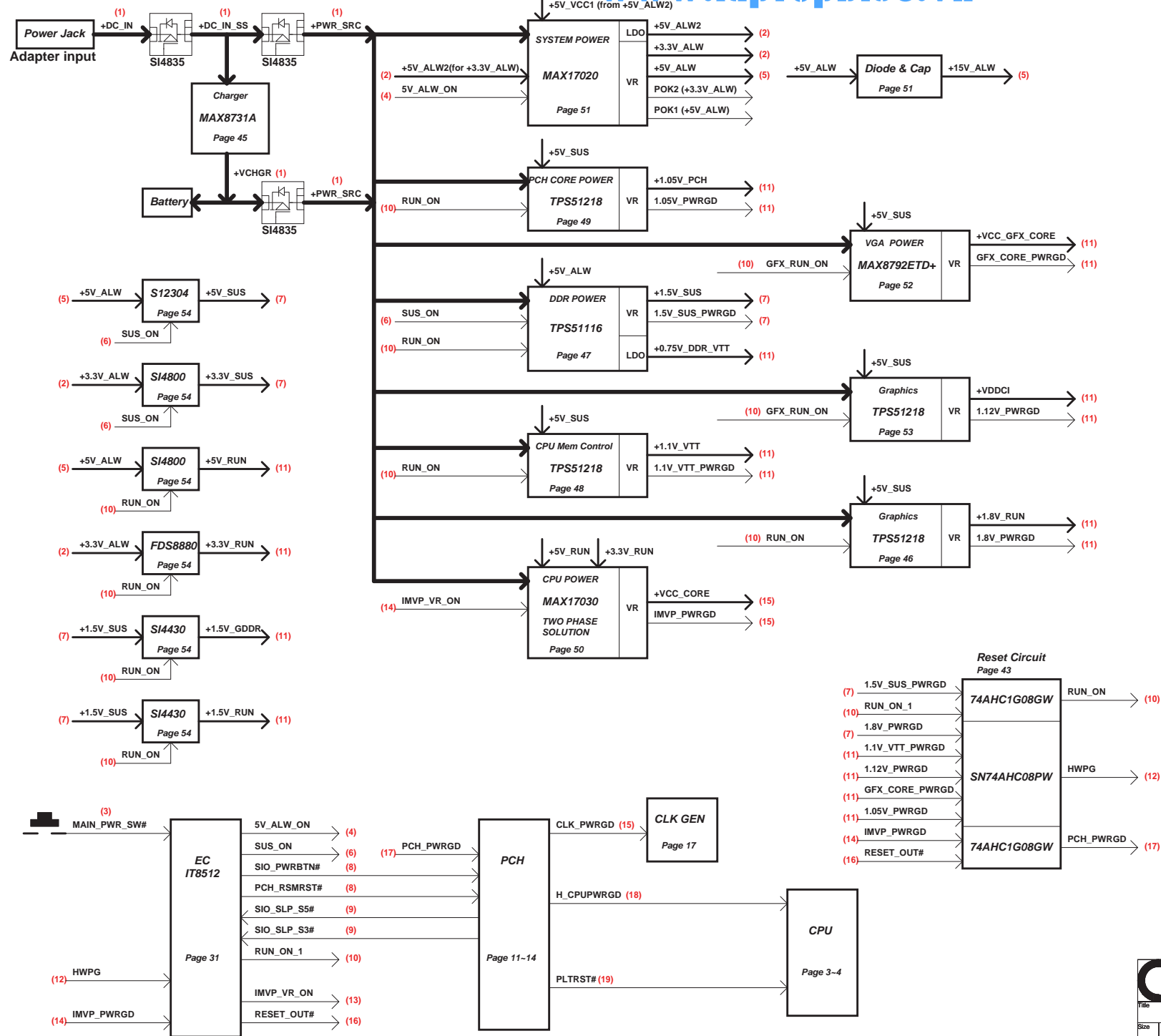
PCH XDP

DEL PCH XDP as FM9 confirmed with Intel that its not necessary!



RM5 Power Design Block Diagram 2009/02/25

www.laptopblue.vn



- (1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
- Bat : +VCHGR -> +PWR_SRC
- (2) +5V_ALW2, +3.3V_ALW
- (3) MAIN_PWR_SW#
- (4) 5V_ALW_ON
- (5) +5V_ALW -> +15V_ALW
- (6) SUS_ON
- (7) All SUS power & PWRGD
- (8) SIO_PWRBTN#, PCH_RSMRST#
- (9) SIO_SLP_S5#, SIO_SLP_S3#
- (10) RUN_ON_1, RUN_ON, GFX_RUN_ON
- (11) All RUN power & PWRGD
- (12) HWPG
- (13) IMVP_VR_ON
- (14) IMVP_PWRGD
- (15) CLK_PWRGD
- (16) RESET_OUT#
- (17) PCH_PWRGD
- (18) H_CPUPWRGD
- (19) PLTRST#



POWER STATES

State \ Signal	SLP_S3#	SLP_S4#	SLP_S5#	S4_STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	N/A	HIGH	N/A	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	N/A	HIGH	N/A	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	N/A	HIGH	N/A	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	N/A	LOW	N/A	ON	OFF	OFF	OFF

PM TABLE

power plane \ State	+RTC_CELL	+DC_IN +DC_IN_SS +PWR_SRC +CPU_PWR_SRC +5V_ALW2 +MMB_PWR +3.3V_ALW	+5V_ALW +15V_ALW +5V_SUS +3.3V_SUS +3.3V_LAN +3.3V_CARDAUX +1.8V_SUS +1.5V_SUS	+VCC_CORE +0.75V_DDR_VTT +1.05V_PCH +1.1V_GFX_PCIE +1.2V_LOM +1.5V_RUN +1.5V_CARD +1.8V_RUN +3.3V_RUN +3.3V_DELAY +3.3V_R5C833	+3.3V_RUN_CARD +3.3V_CARD +5V_RUN +LCDVCC +5V_HDD +5V_MOD +5V_SPK_AMP +VDDA +GFX_PWR_SRC
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	OFF	OFF
S5 & S4 with AC or BAT	ON	ON	OFF	OFF	OFF
no AC/Battery	ON	OFF	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
NONE			

PCH IBEX PEAK-M	USB PORT#	DESTINATION
	0	Side pair Top / left
	1	Side pair Bottom / left
	2	USB W/ E-SATA port
	3	Reserved
	4	Mini Card (WLAN)
	5	Mini Card (WWAN)
	6	Reserved
	7	Reserved
	8	Mini Card (WPAN)
	9	TV
	10	Express Card
	11	Camera

PCH IBEX PEAK-M	PCI EXPRESS	DESTINATION
	Lane 1	Mini Card-1 WWAN
	Lane 2	Mini Card-2 WLAN
	Lane 3	Mini Card-3 WPAN
	Lane 4	Express Card
	Lane 5	Cardreader
	Lane 6	LOM

www.s-manuals.com