

Compal Confidential

NCWGO/H0 Schematics Document

AMD S1g1 / RS780MN/ SB710

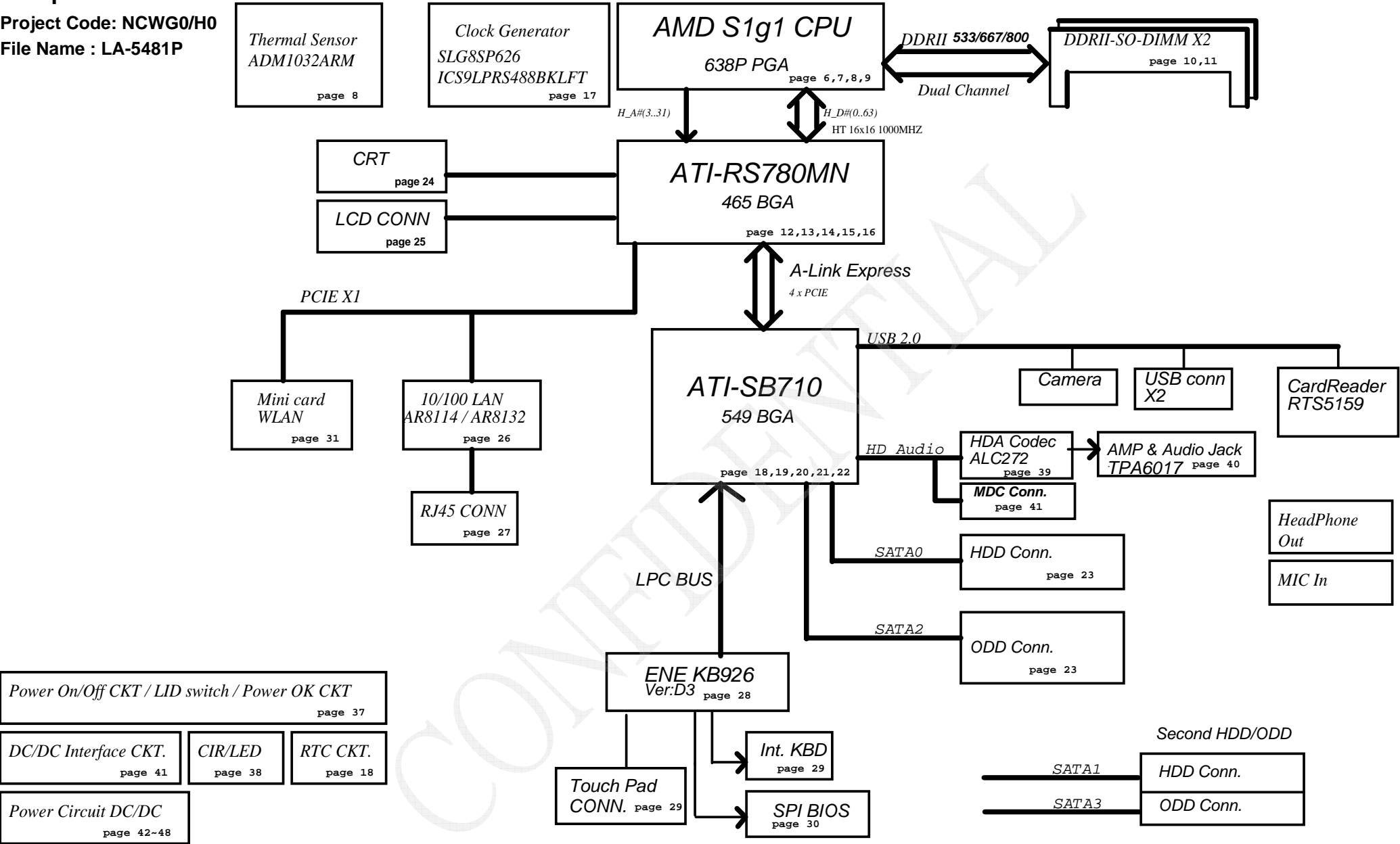
2009 / 06 / 24

LA-5481

Rev:1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2005/03/08	Deciphered Date		2010/03/12
Title		SCHEMATIC, MB A5481			
Size		Document Number		401743	
Custom		Date		Wednesday, June 24, 2009	Sheet 1 of 47
Rev		C			

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VIN	Adapter power supply (19V)			
B+	AC or battery power rail for power circuit.			
+CPU_CORE	Core voltage for CPU			
+0.9V	0.9V switched power rail for DDR terminator	ON	OFF	
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON		ON*
+1.8V	1.8V power rail for DDR	ON		
+1.8VS	1.8V switched power rail		OFF	
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address		EC SM Bus2 address	
Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

SB600 SM Bus 2 address

Device	Address	Device	Address
Clock Generator	1101 001Xb	New Card	
DDR DIMM0	1001 000Xb		
DDR DIMM2	1001 010Xb		
Wireless Lan			

SIGNAL STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

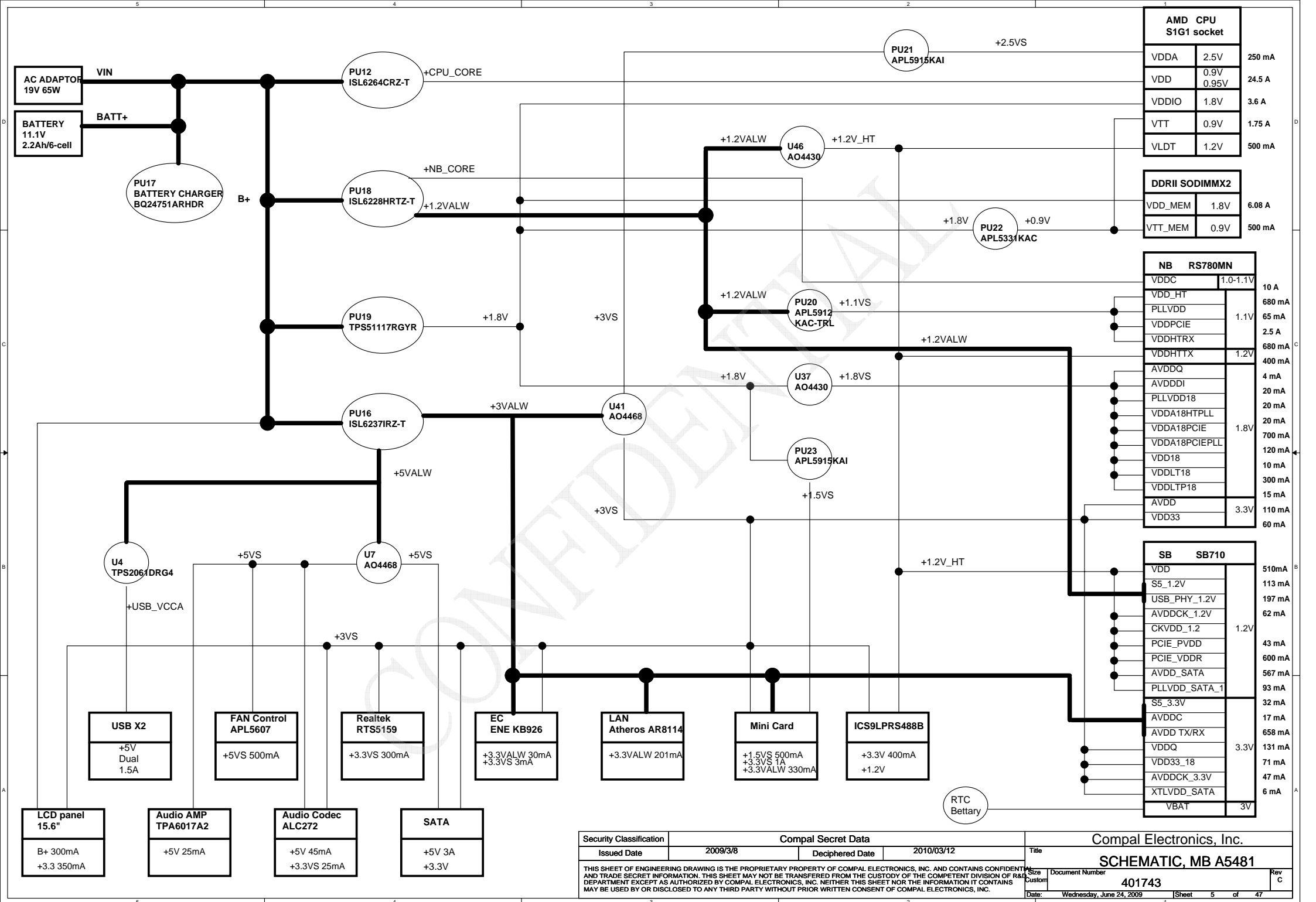
Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

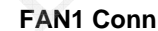
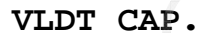
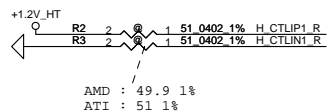
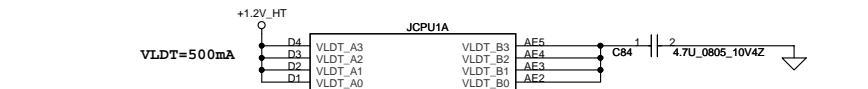
Board ID	PCB Revision
0	No Support VaryBright
1	
2	
3	Support VaryBright
4	
5	
6	
7	

[illegible]

SKU ID	SKU
0	NCWG0
1	
2	
3	NAL00
4	
5	
6	
7	NCWH0

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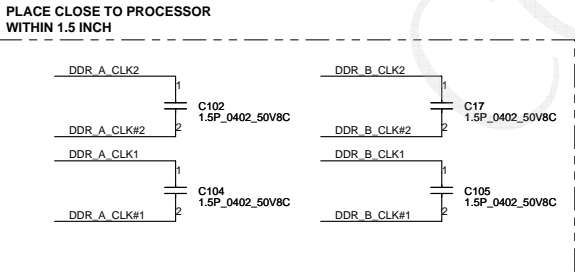
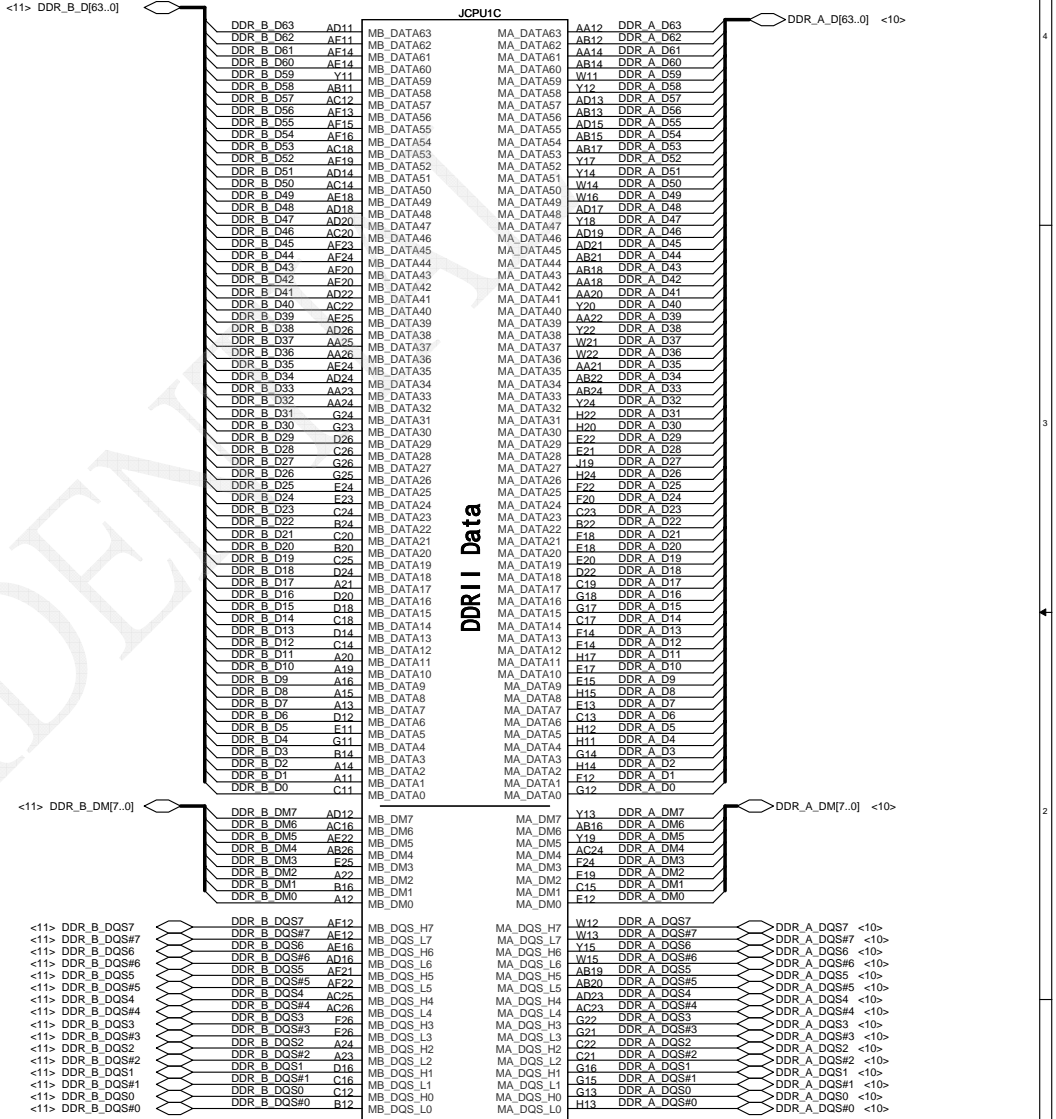
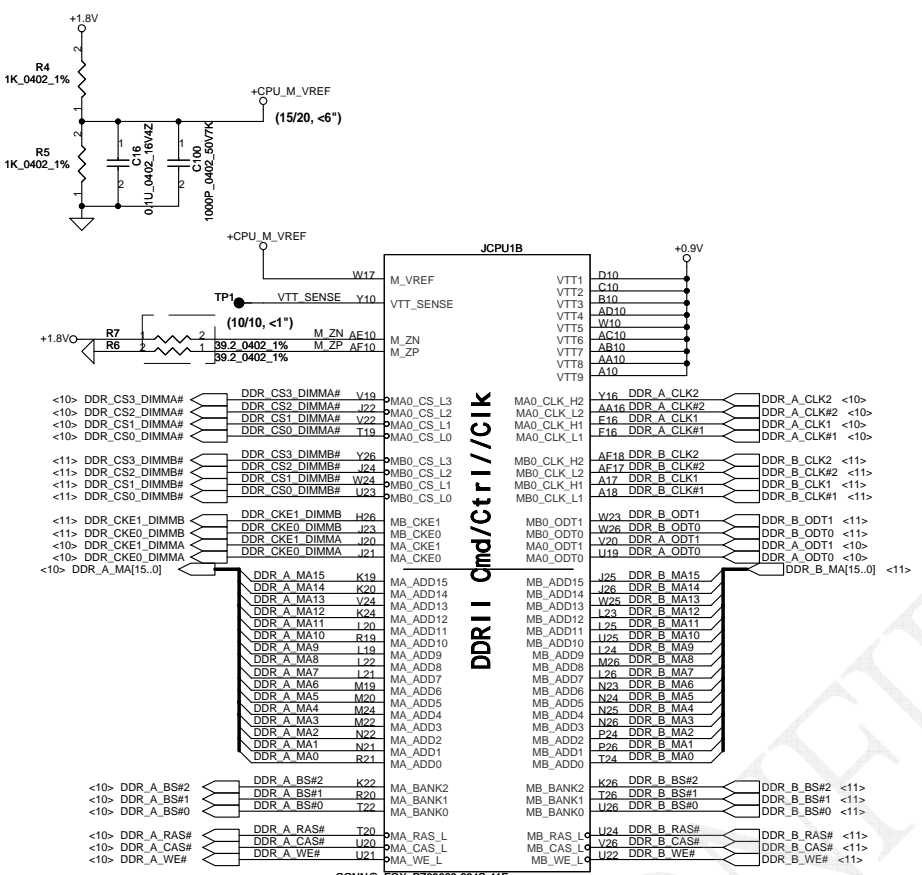
Compal Electronics, Inc.

SCHEMATIC, MB A5481

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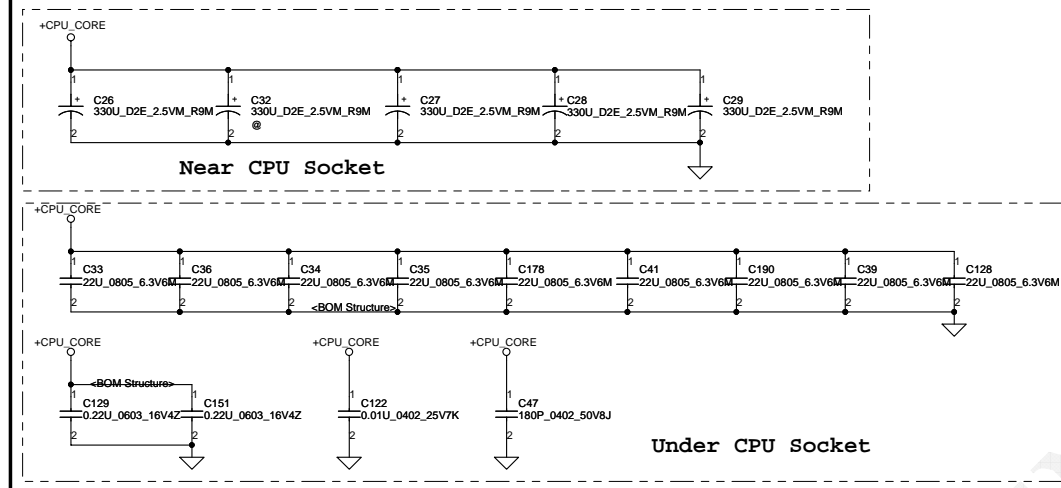
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Processor DDR2 Memory Interface

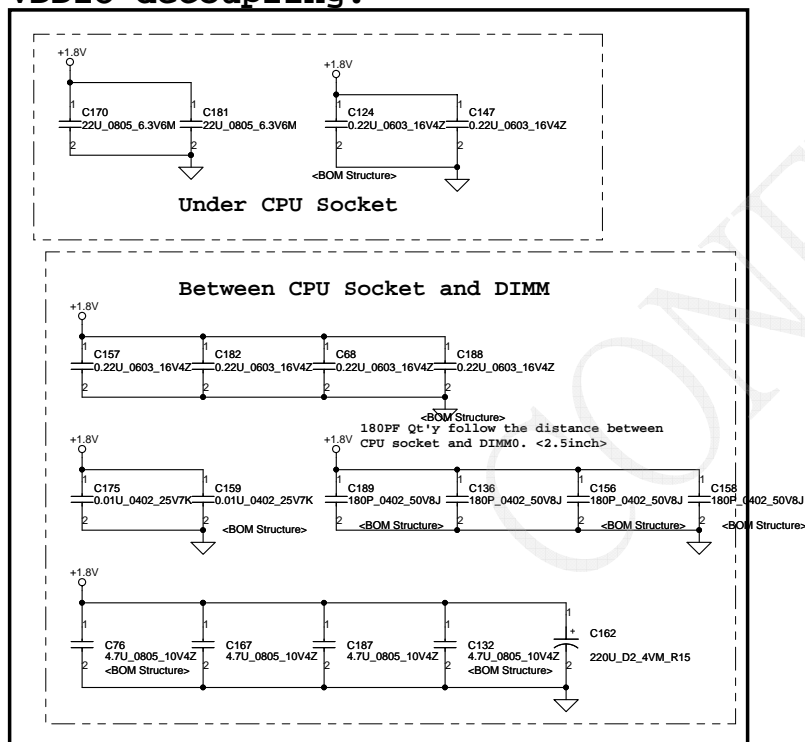


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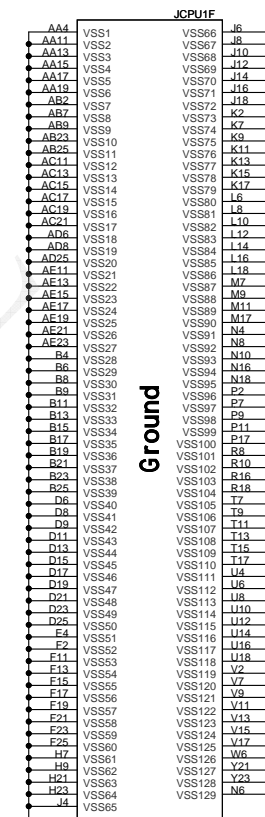
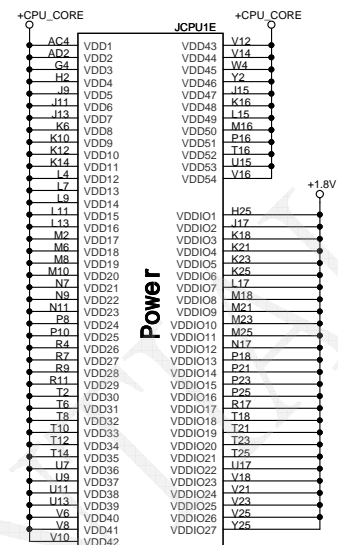
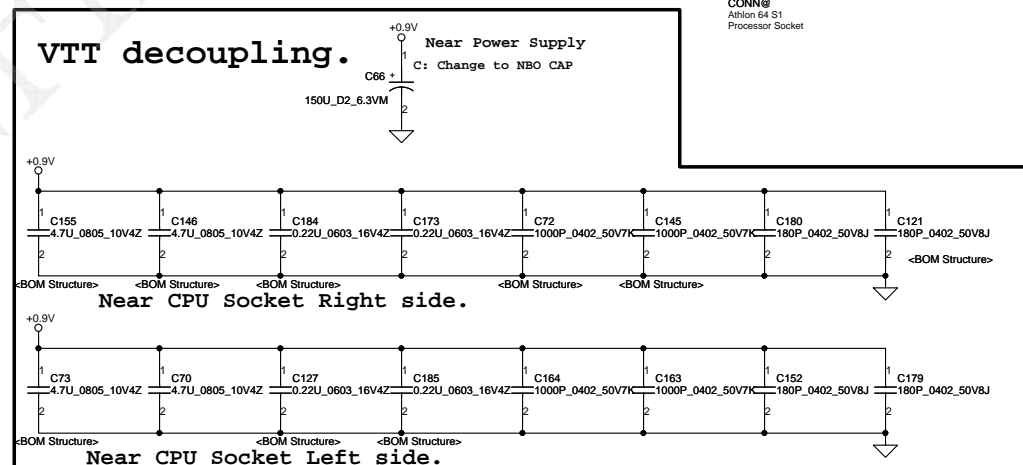
VDD(+CPU_CORE) decoupling.



VDDIO decoupling.



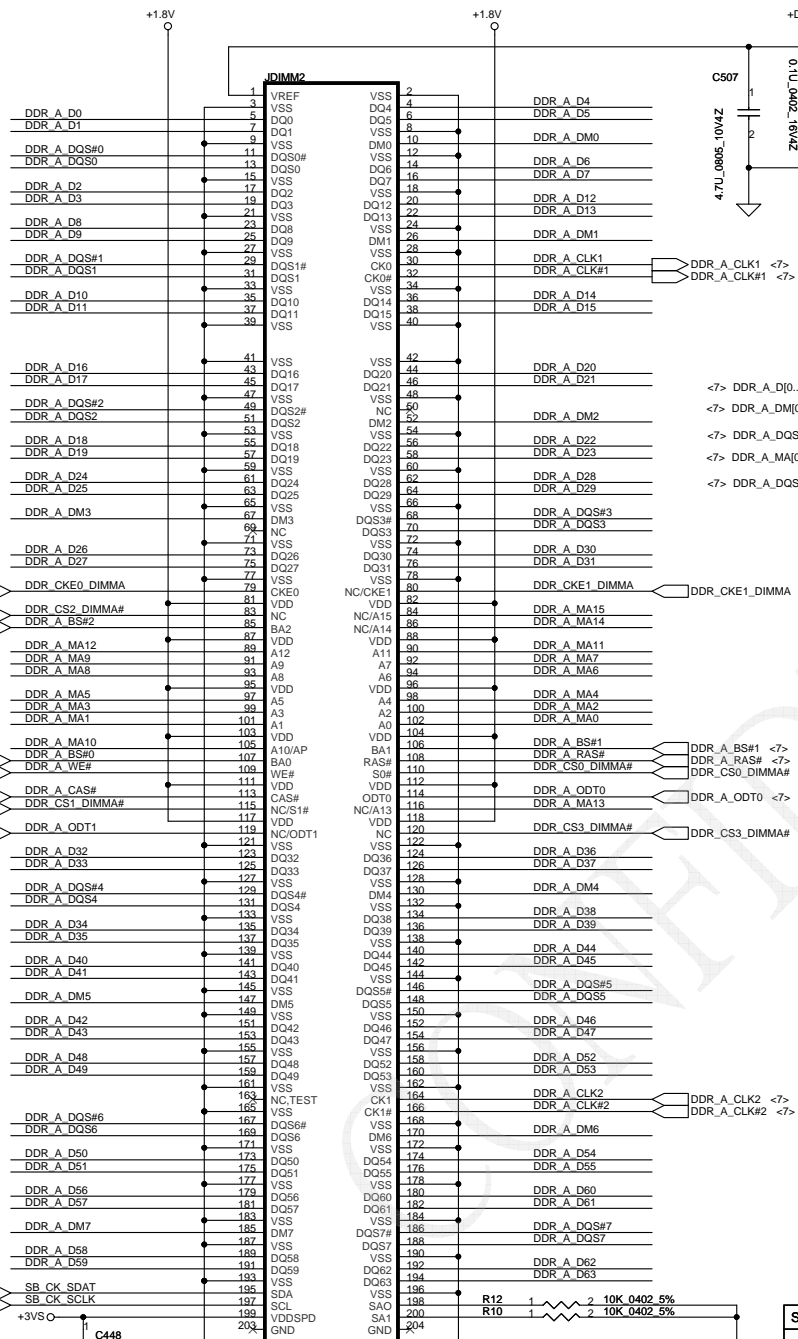
VTT decoupling.

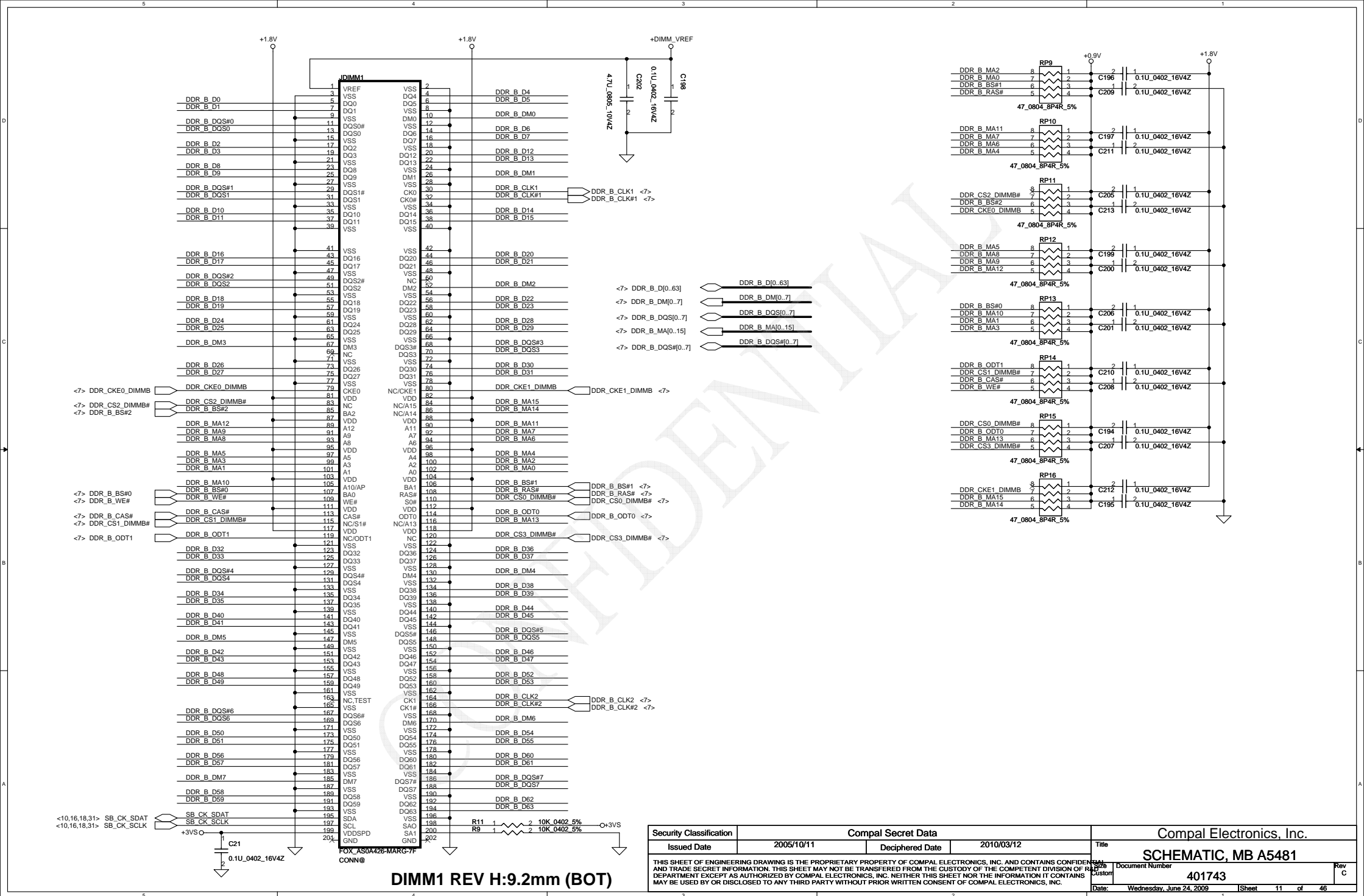


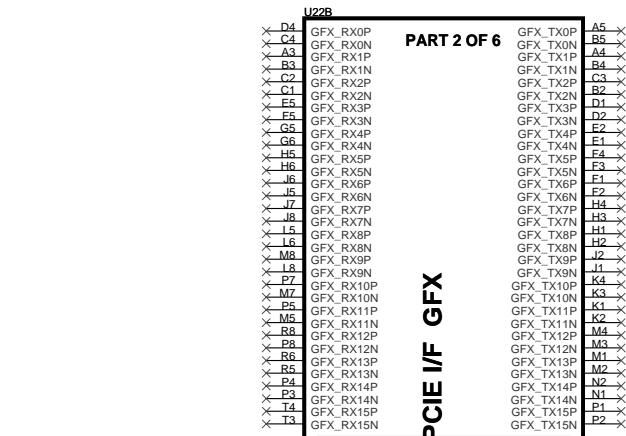
FOX_P263823-284S-41F
CONN@
Athlon 64 S1
Processor Socket

FOX_P263823-284S-41F
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Athlon 64 S1
Processor Socket

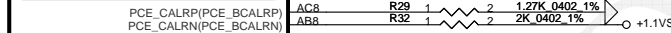
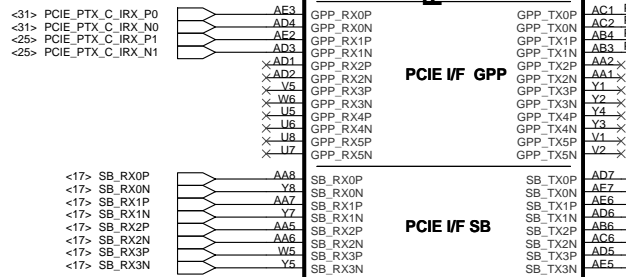
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Check SW Routing
AN_RS780MN1. Only suggest pair0-3 can
usage for power save.



RS780M_FCBGA528

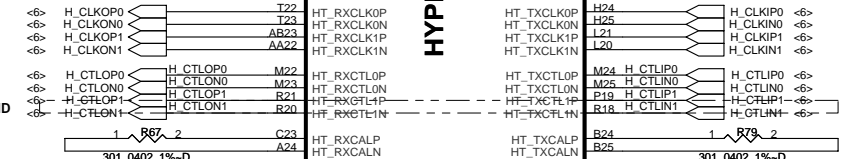
RS780MN-SA00002DR30 Ver:A13

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

HT Link
When tune trace length, must
keep 1:4 on self-trace

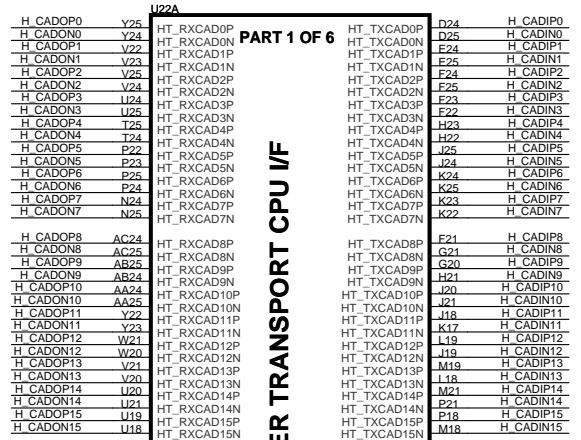
Check AMD



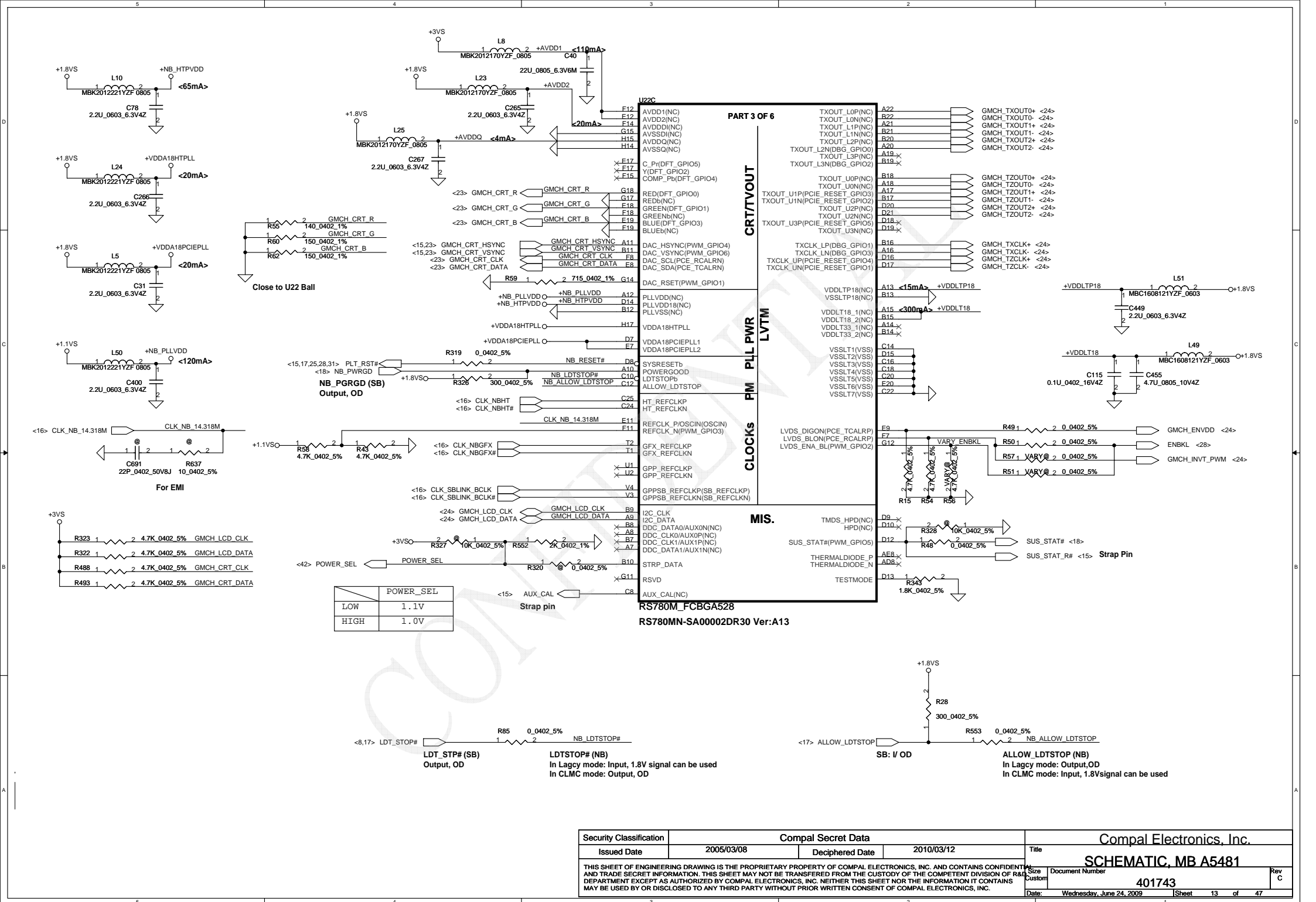
Place within 1"
layout 4/8

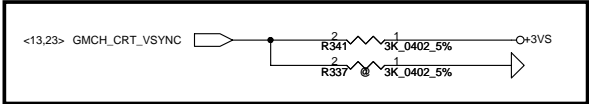
RS780M_FCBGA528
RS780MN-SA00002DR30 Ver:A13

Place within 1"
layout 4/8



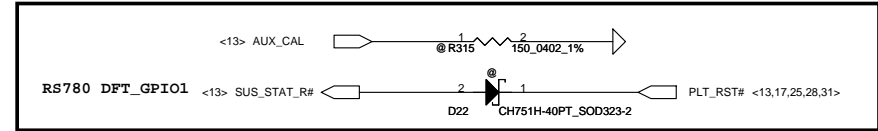
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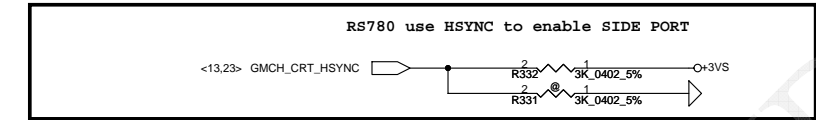
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)



DFT_GPIO1: LOAD_EEPROM_STRAPS

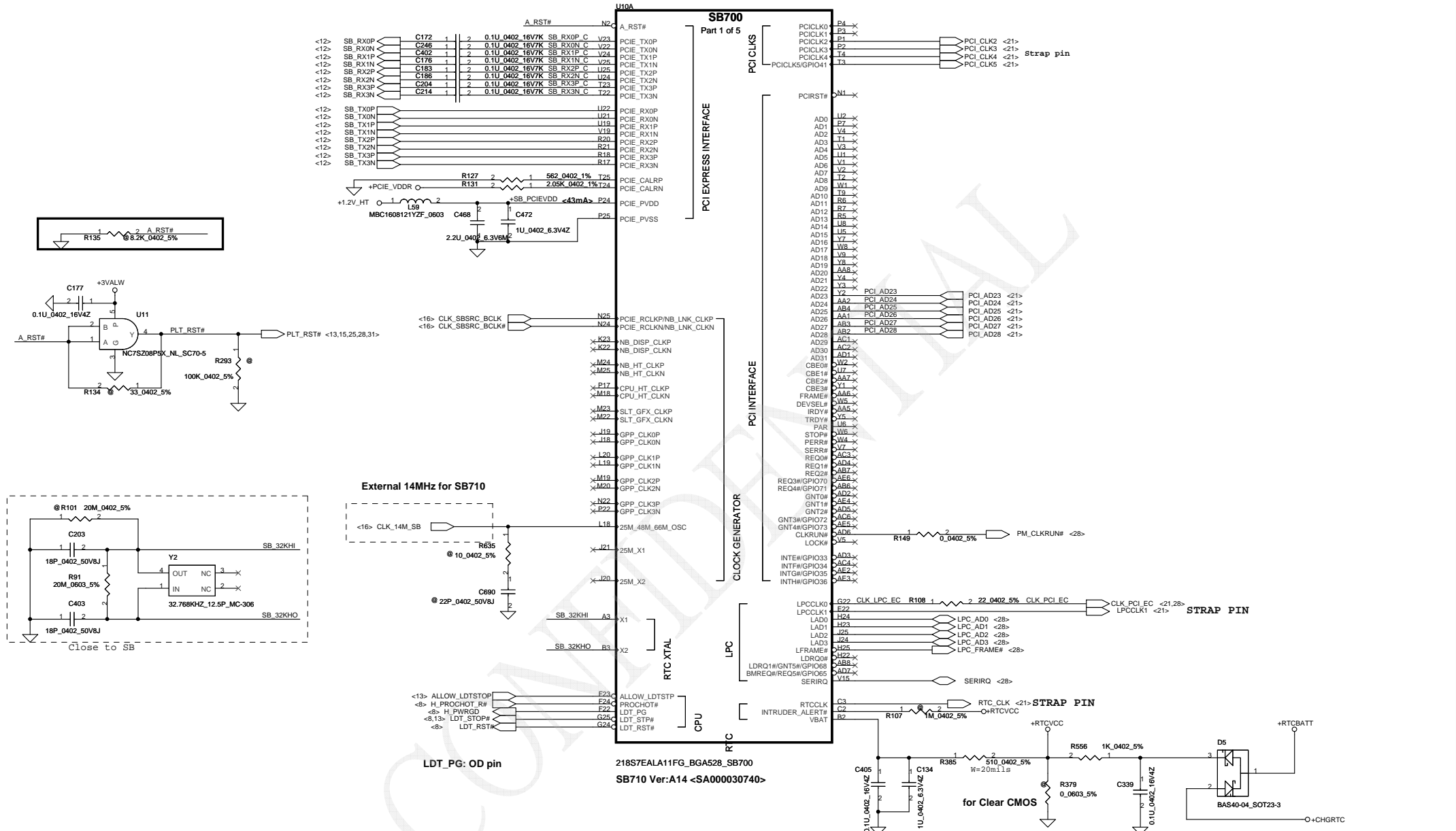
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



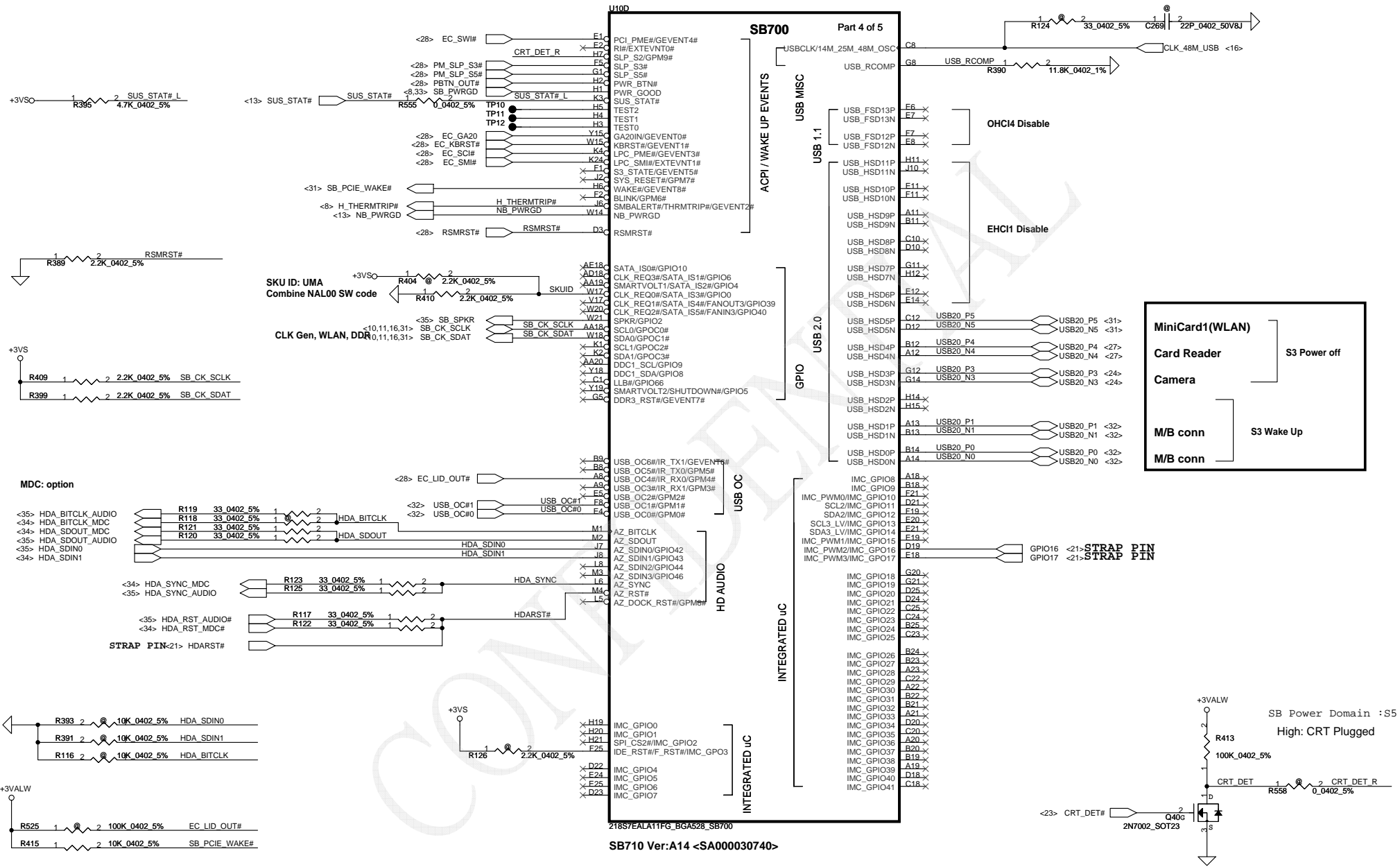
RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
0. Enable (RS780)
1 : Disable(RS780)

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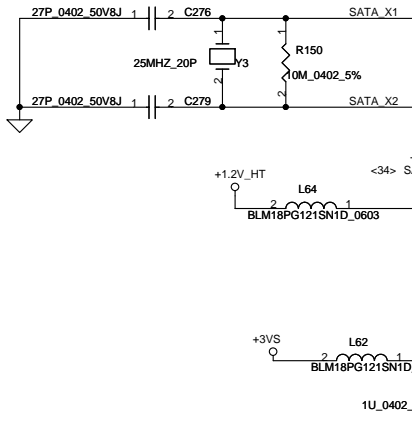
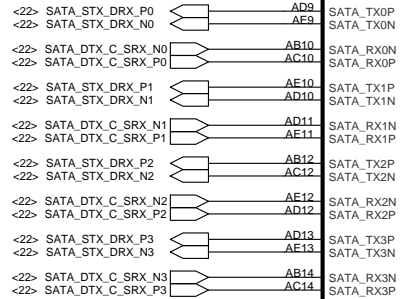


Main
HDD

2nd
HDD

Main
ODD

2nd
ODD



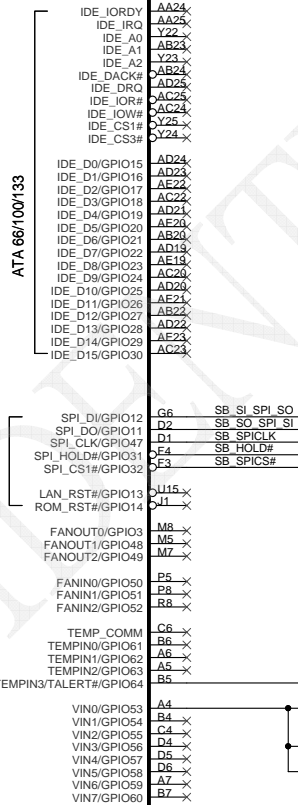
U10B

SB700
Part 2 of 5

SERIAL ATA

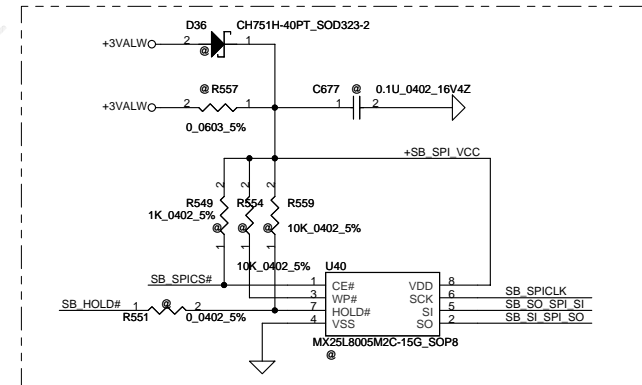
SPI ROM

HW MONITOR



218S7EALA11FG_BGA528_SB700
SA00001S570 Ver:A12

Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller



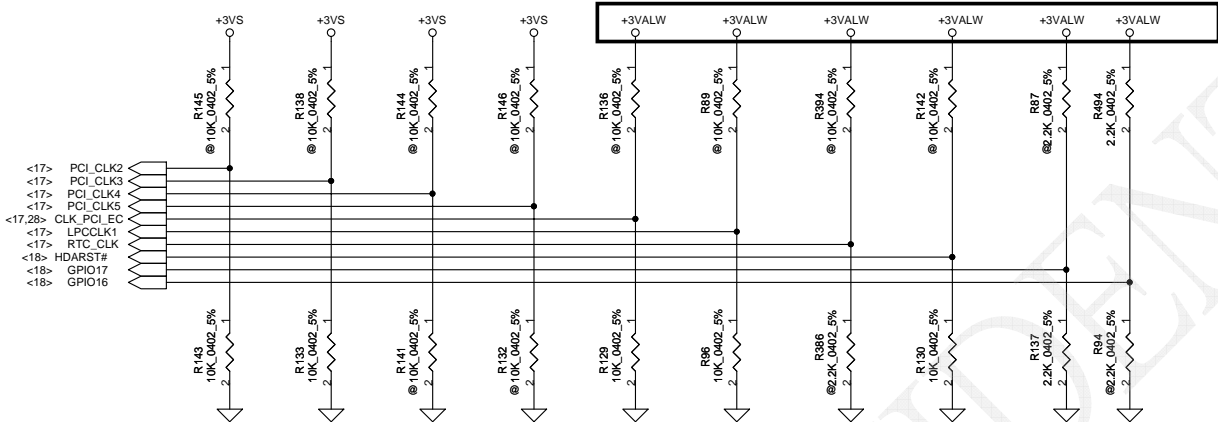
for ACIN level issue

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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default L,NC) L,L = FWH ROM

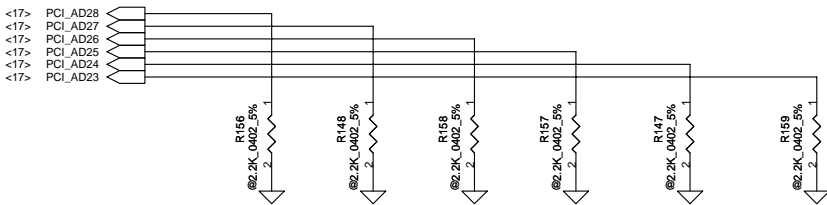


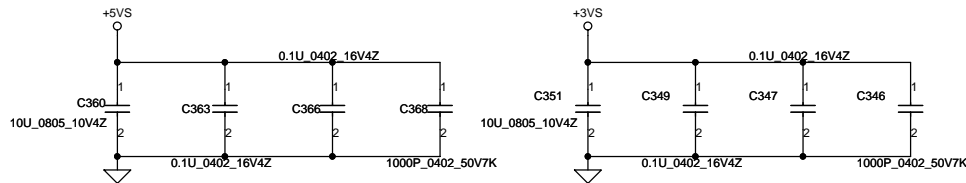
DEBUG STRAPS

DEBUG STRAPS

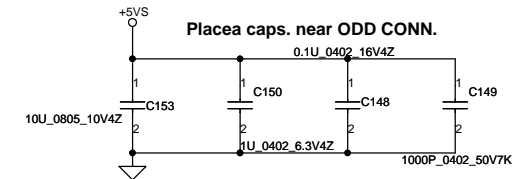
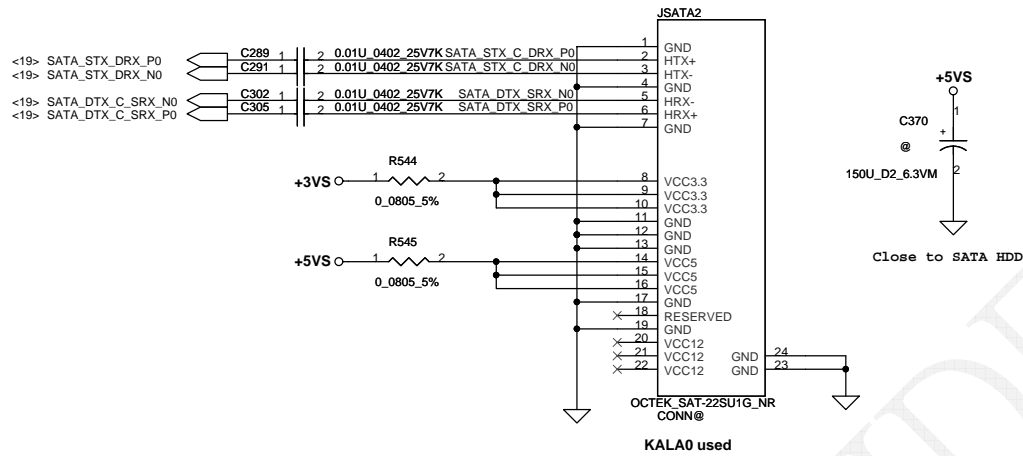
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

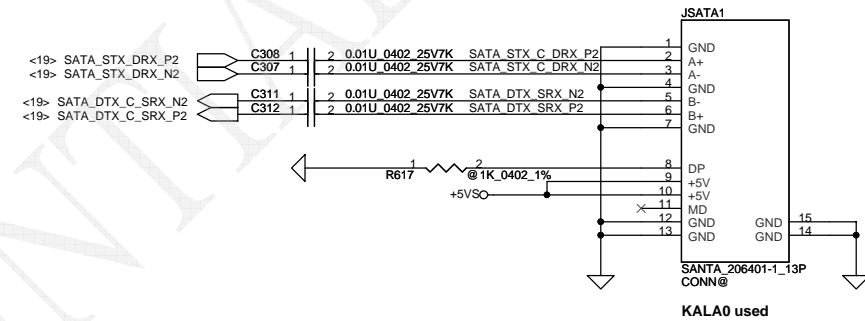




SATA HDD CONN

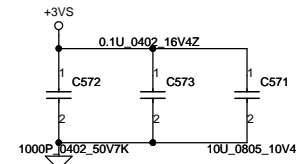
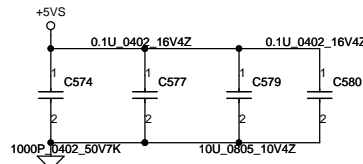
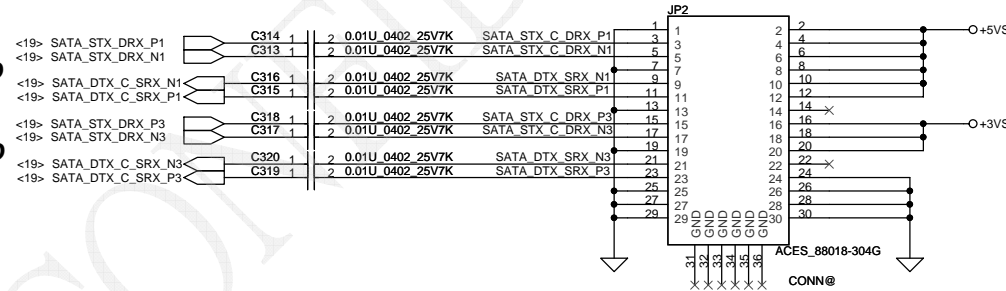


SATA ODD CONN



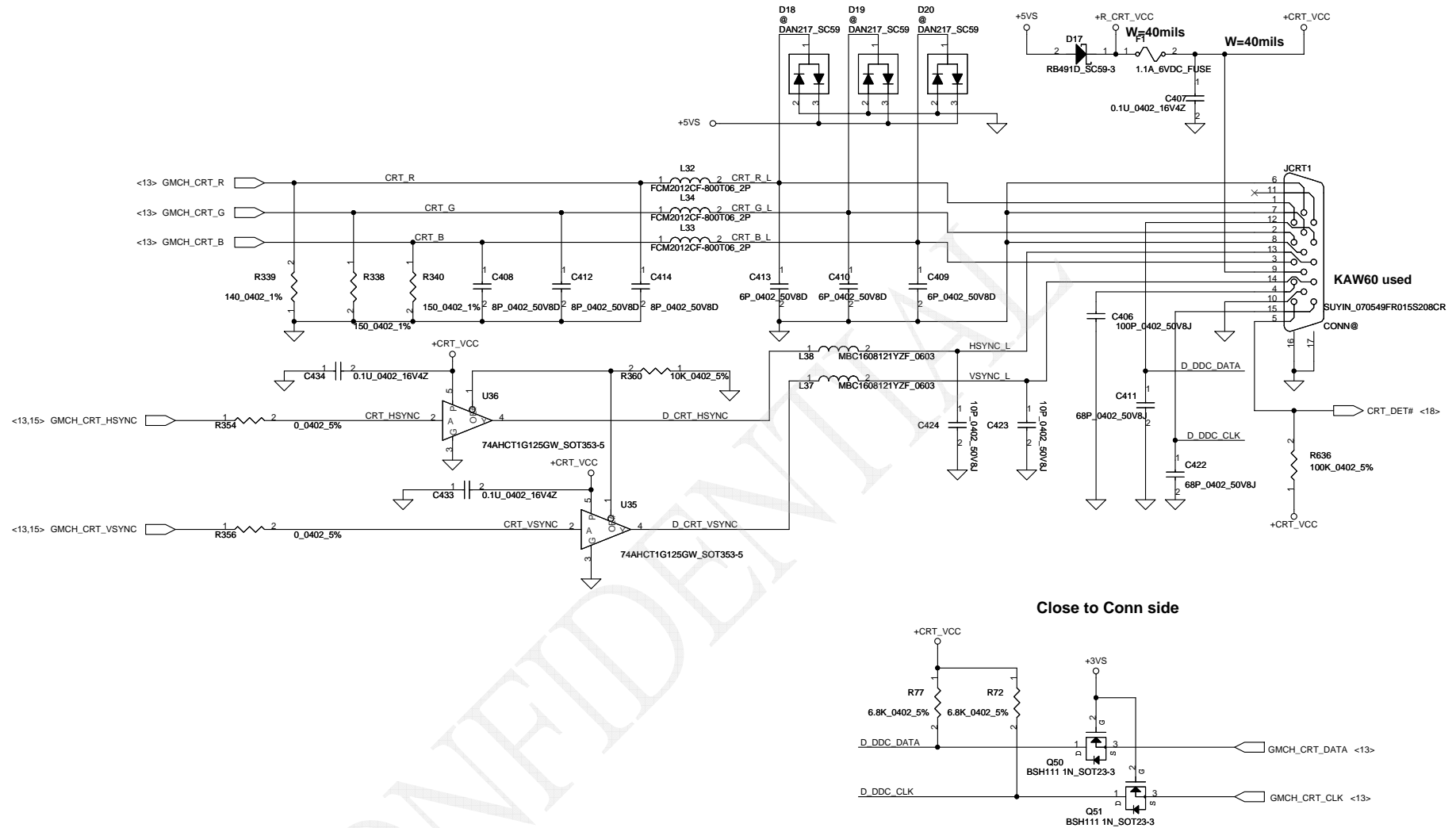
Second HDD

Second ODD



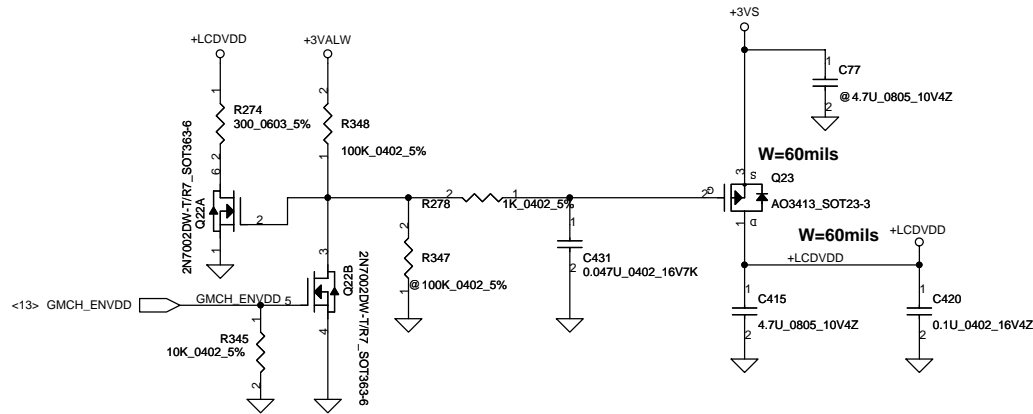
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CRT Connector

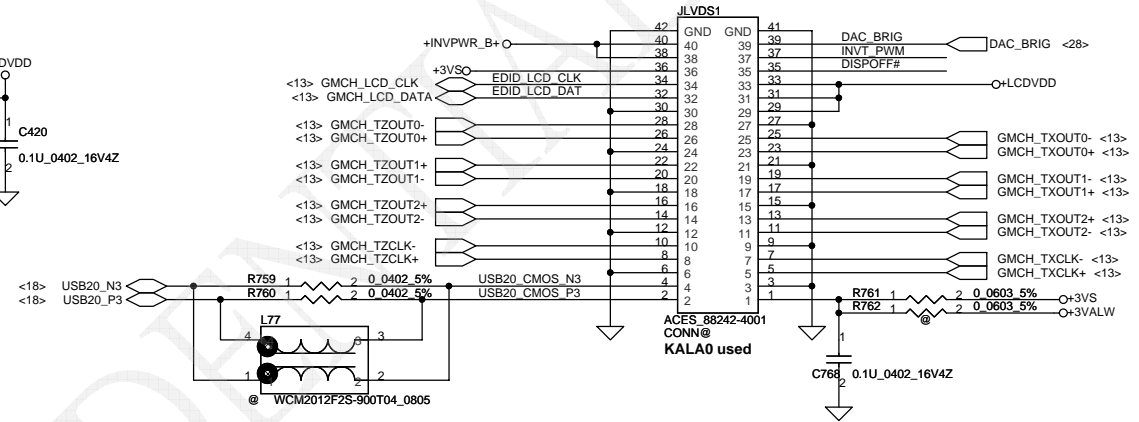


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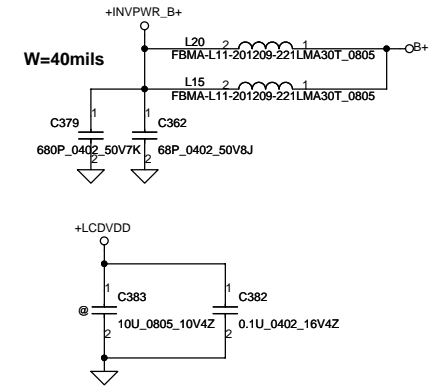
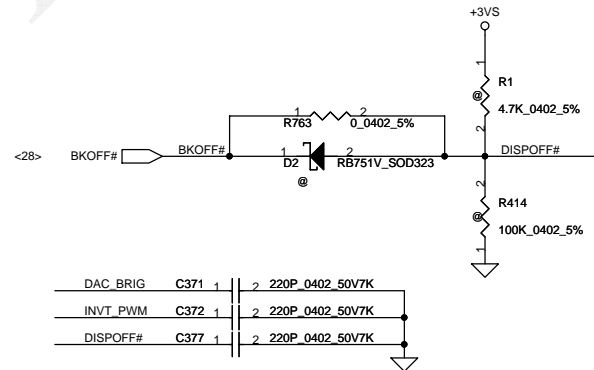
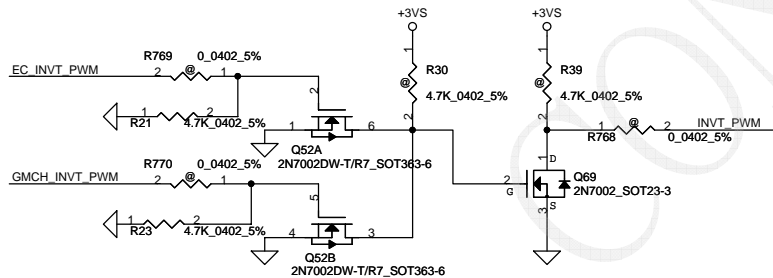
LCD POWER CIRCUIT



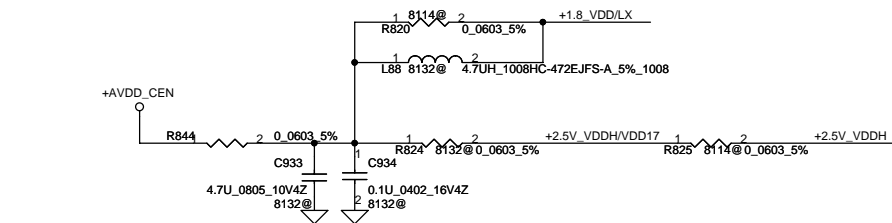
LCD/PANEL CONN.



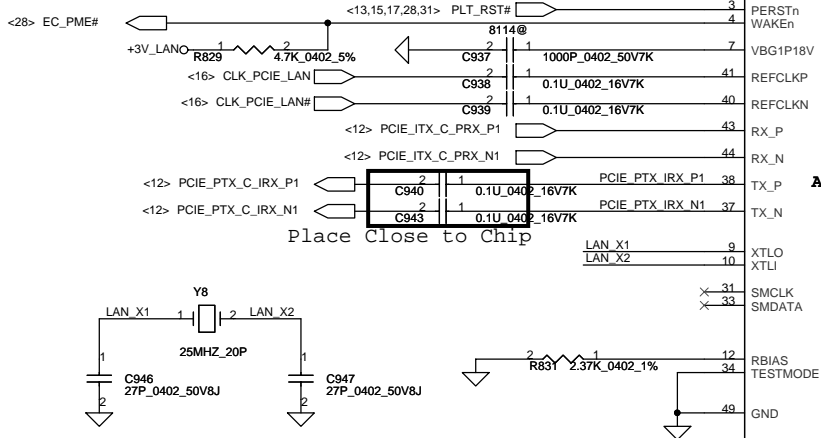
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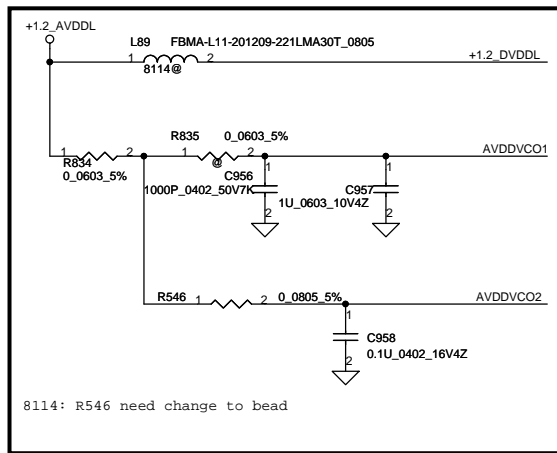
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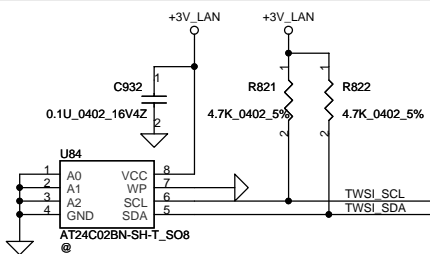
WAKEn
8114: Internal PU
8132: OD



Place Close to Chip



8114: R546 need change to bead

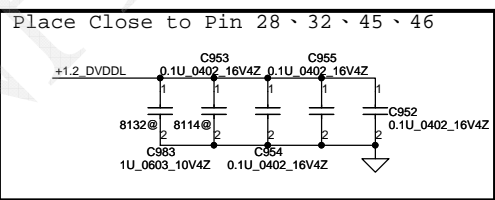


U85

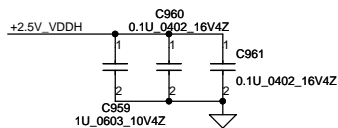
Atheros
AR8114A 10/100 LAN

AR8114-AL1E_QFN48_6X6

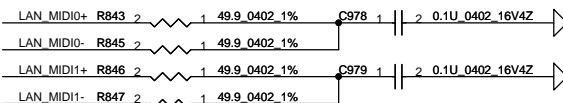
change to AR8132L-AL1E



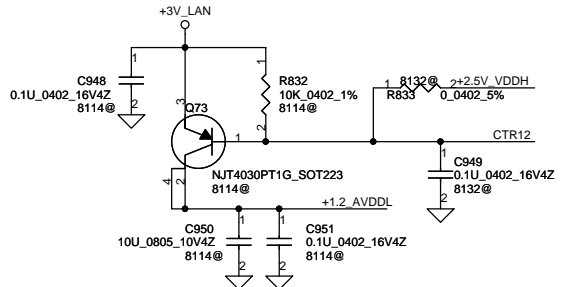
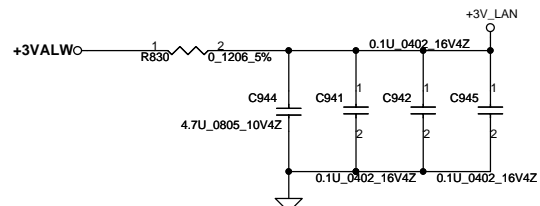
Place Close to Pin15、19、25



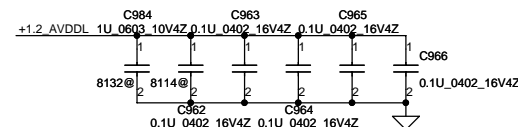
Place Close to Chip



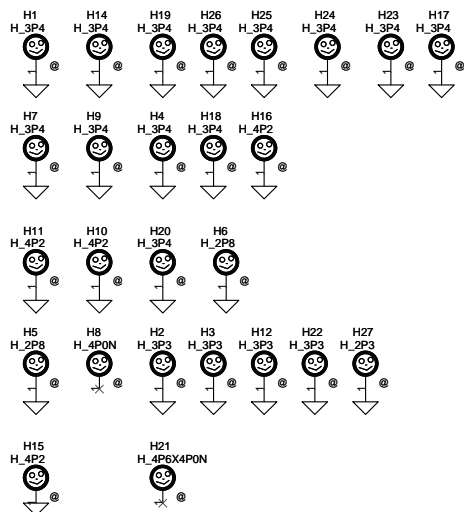
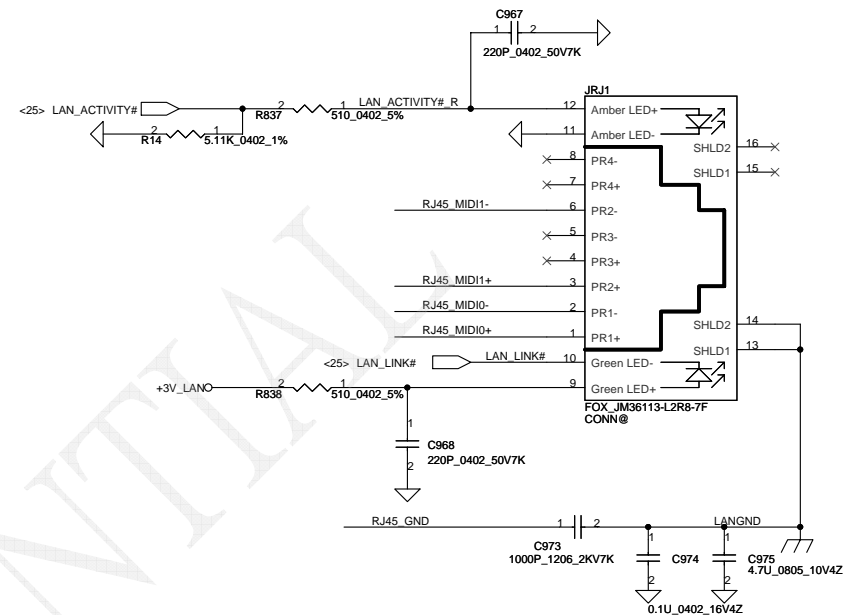
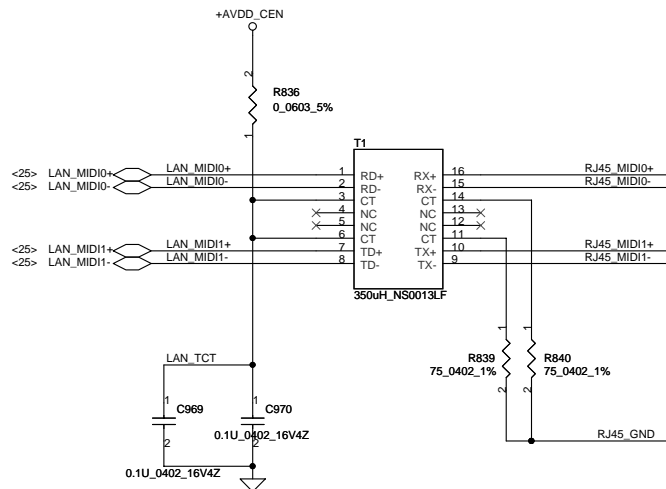
Layout Notice : Close to chip



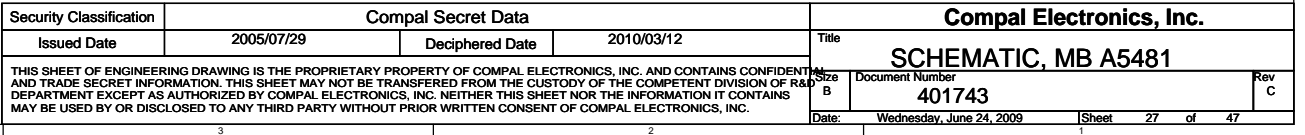
Place Close to Pin8、16、22、36、39

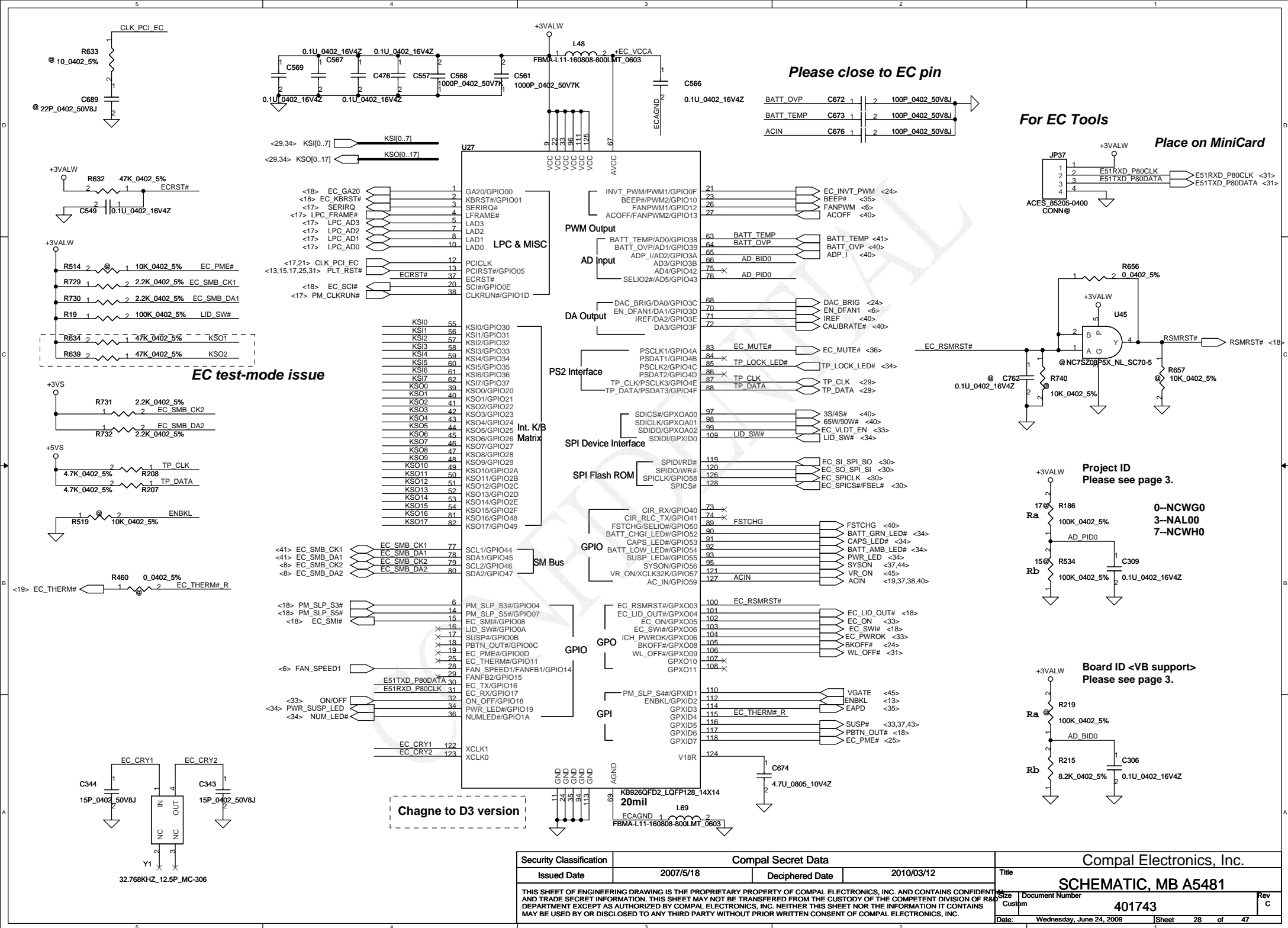


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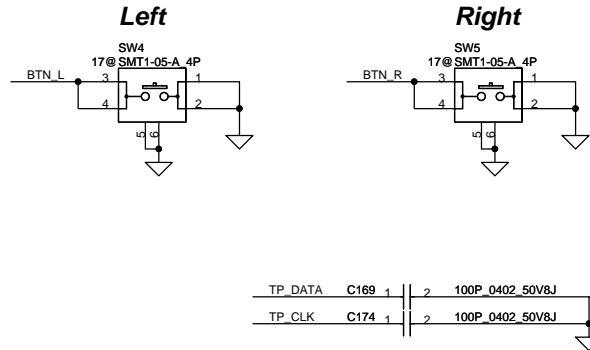


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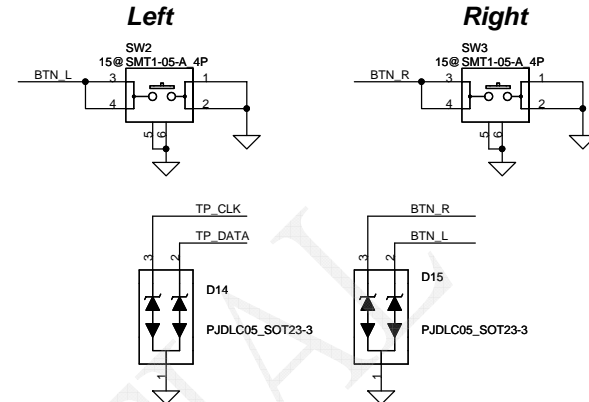




For 17"

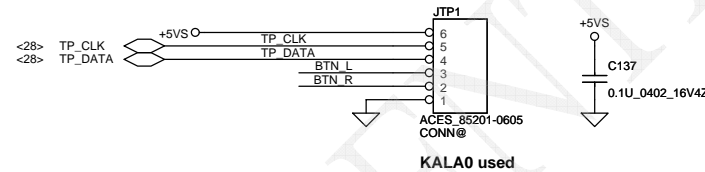


For 15"

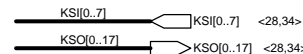


To TP/B Conn.

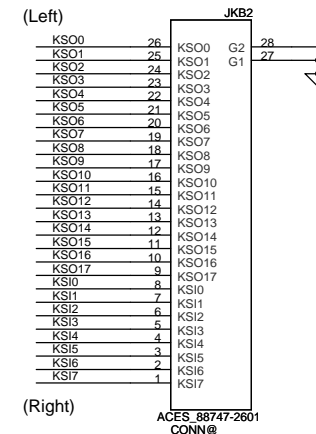
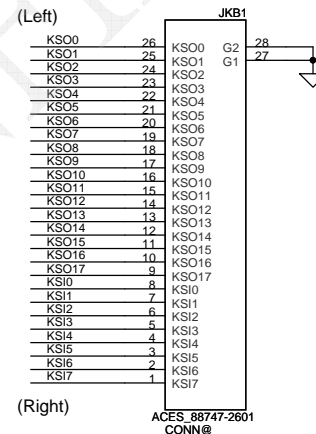
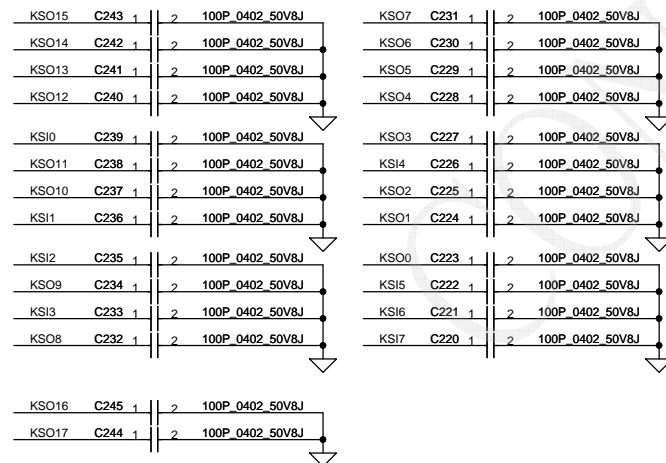
Change to SCA00000200



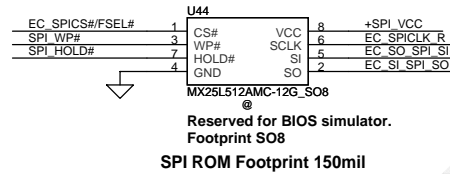
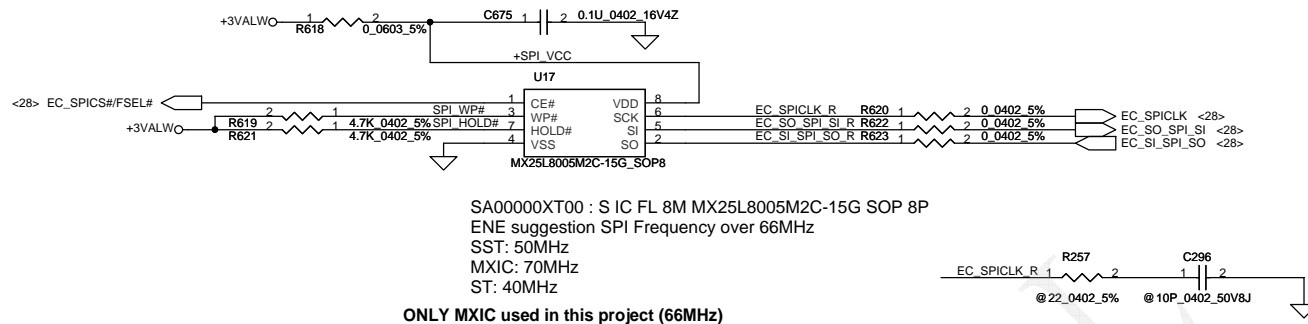
INT_KBD Conn.



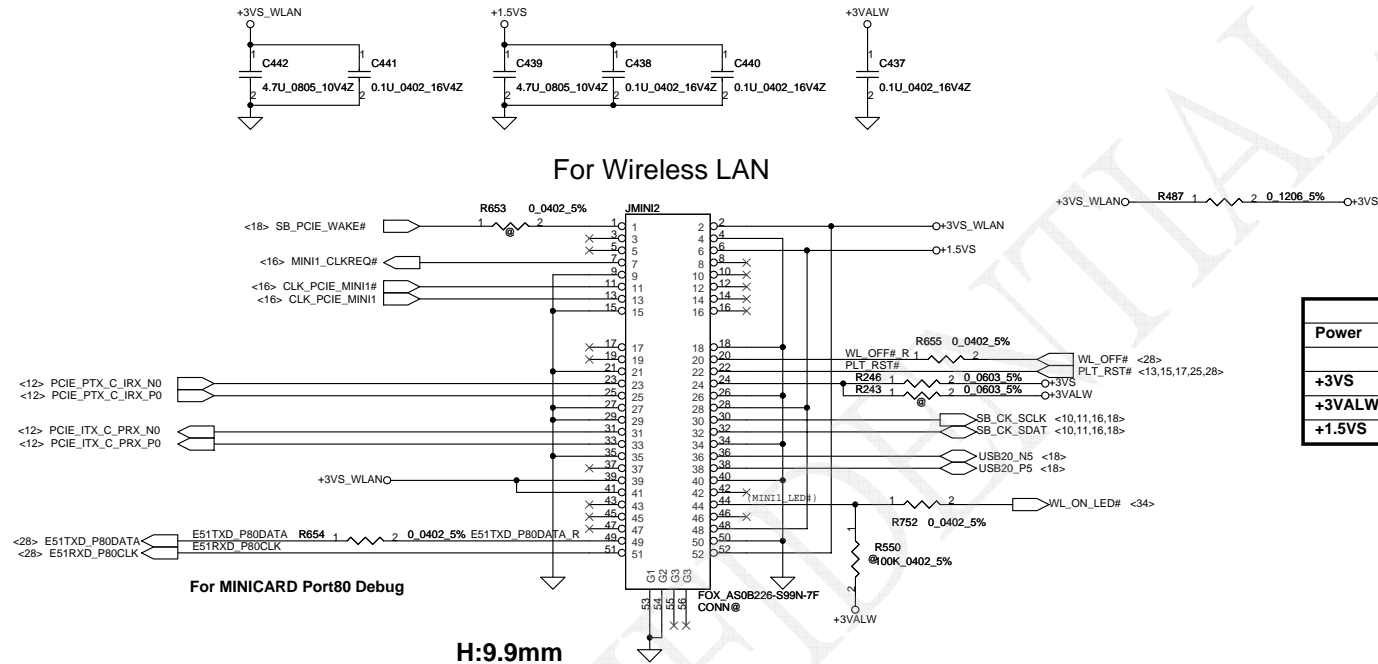
KB1 for 15"
KB2 for 17"

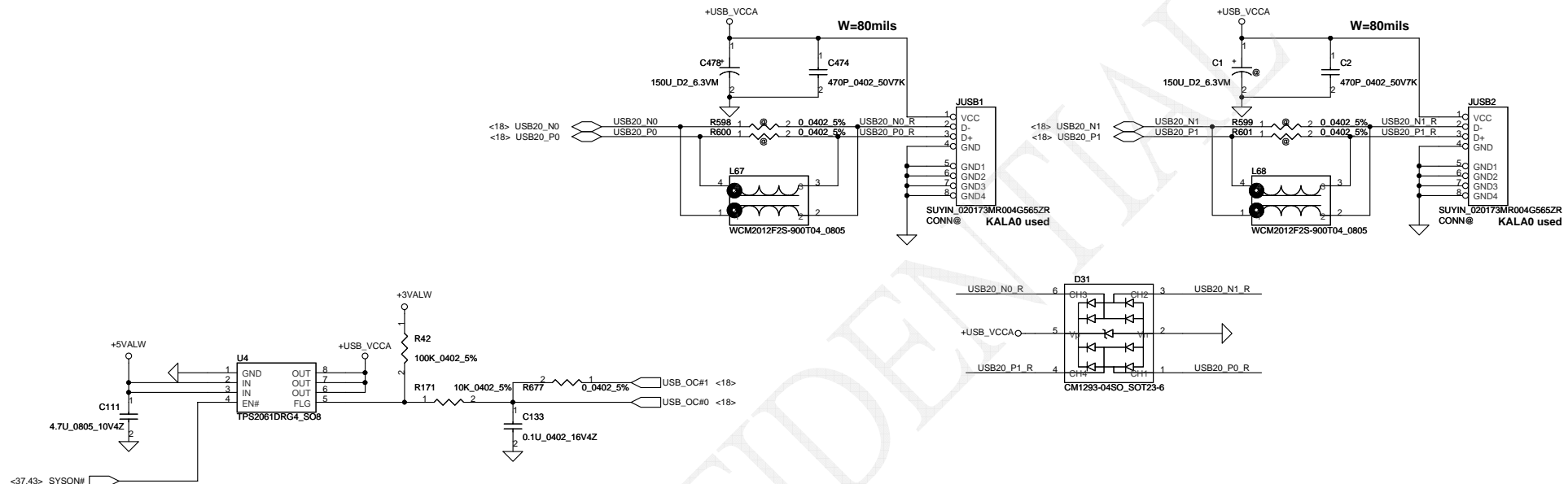


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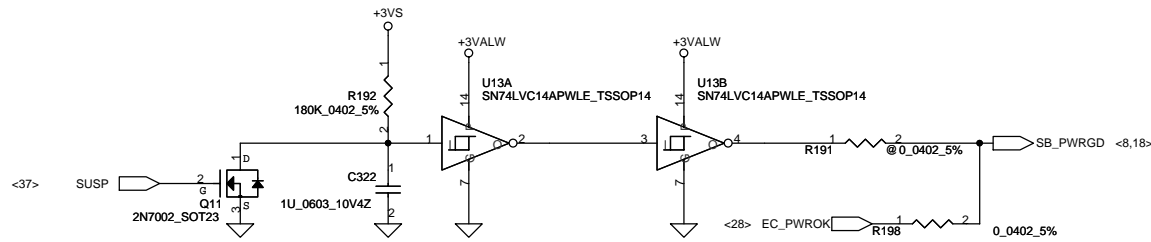


USB CONN. 1 & 2

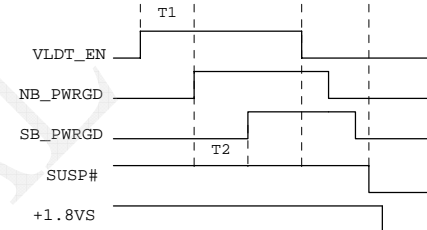
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Power ON Circuit

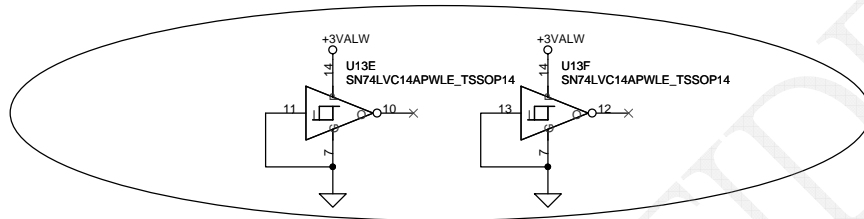
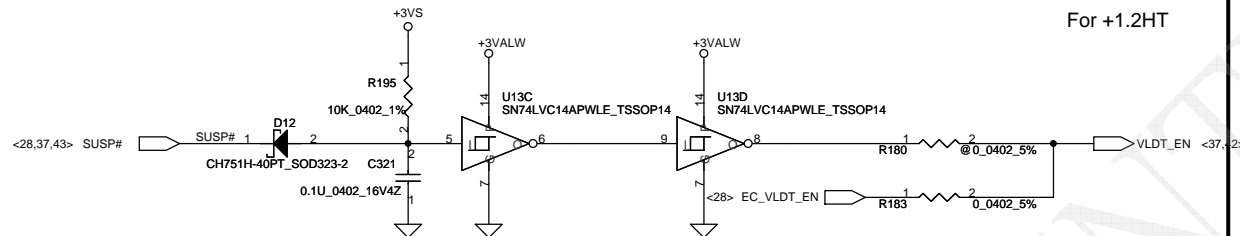
For South Bridge



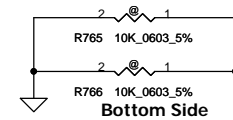
note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



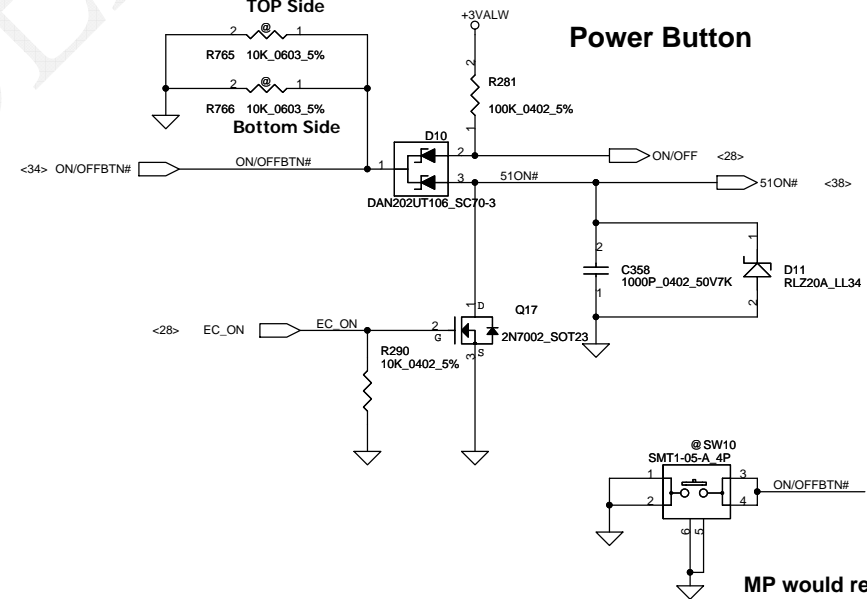
For +1.2HT



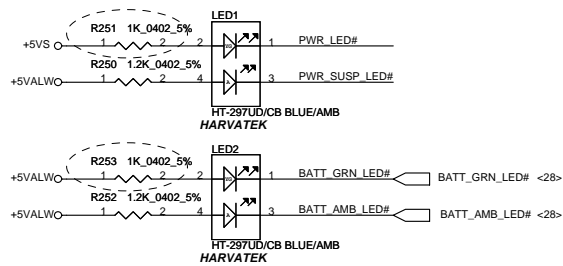
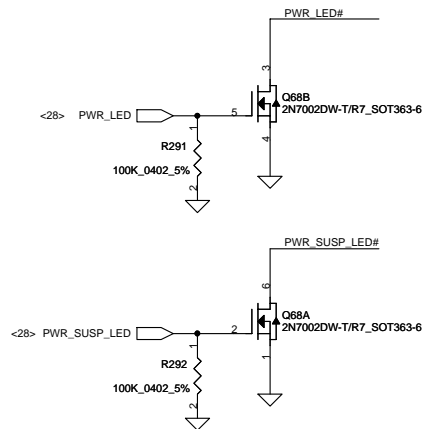
TOP Side



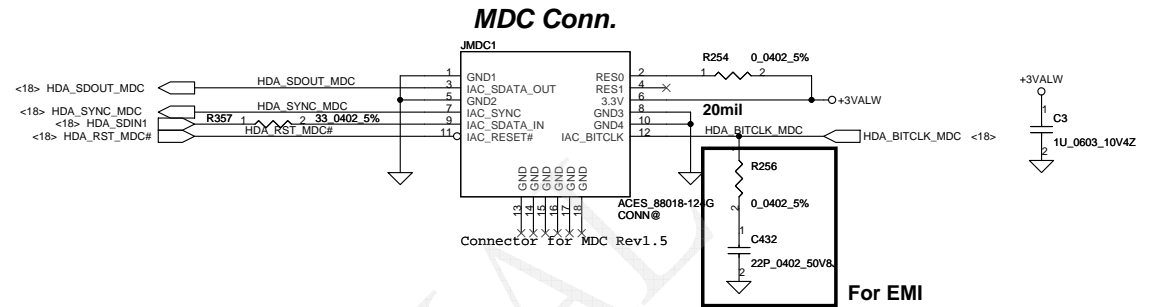
Bottom Side



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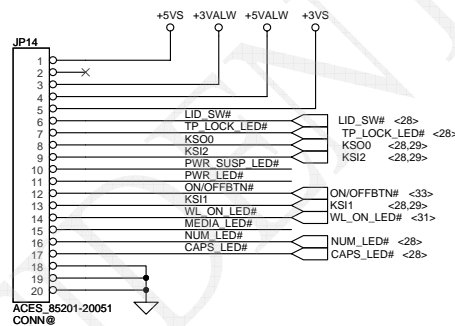


BLUE/AMB LED

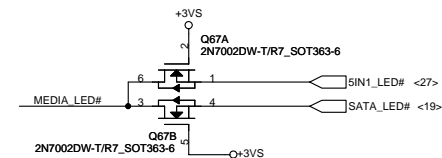
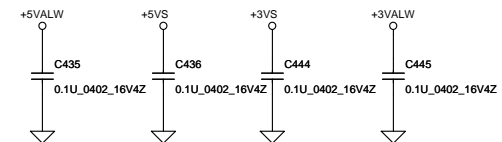


For EMI

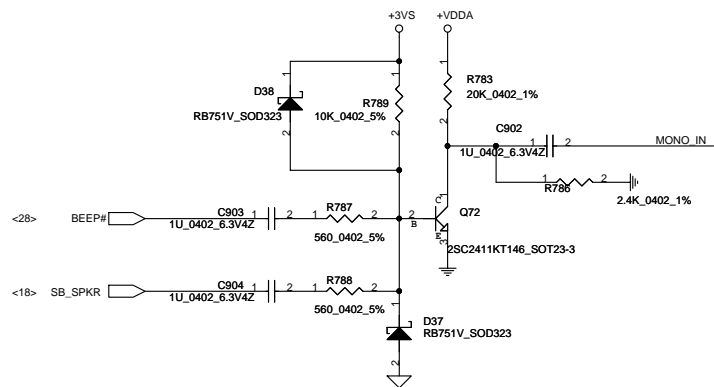
To PWR LED/B



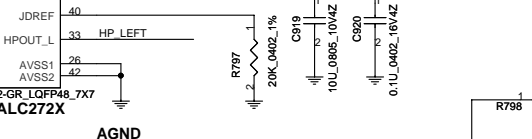
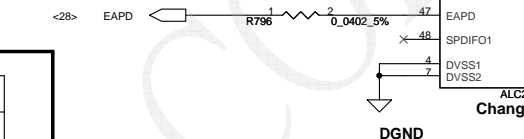
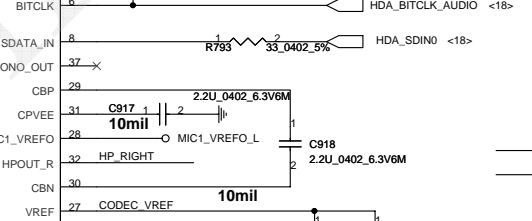
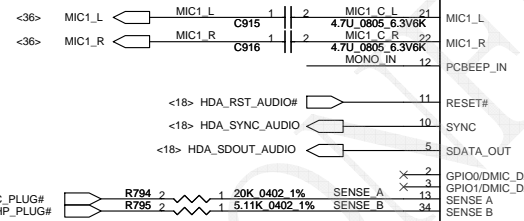
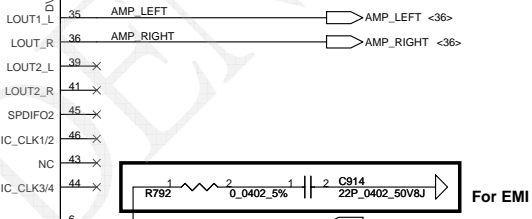
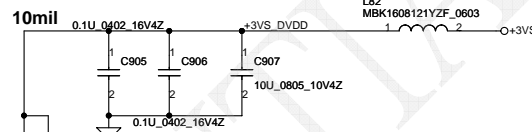
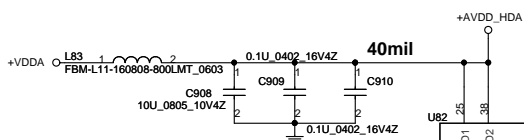
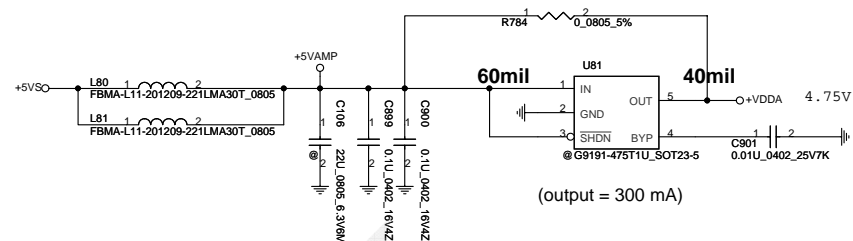
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KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



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HD Audio Codec



update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

DGND

AGND

ALC272-VA2-GR_LQFP48_7X7
Change to ALC272X

For EMI

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HDA_RST_AUDIO# <18>

HDA_SYNC_AUDIO <18>

HDA_SDOUT_AUDIO <18>

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MIC1_R <36>

MIC2_L <36>

MIC2_R <36>

LINE1_L <36>

LINE1_R <36>

LINE2_L <36>

LINE2_R <36>

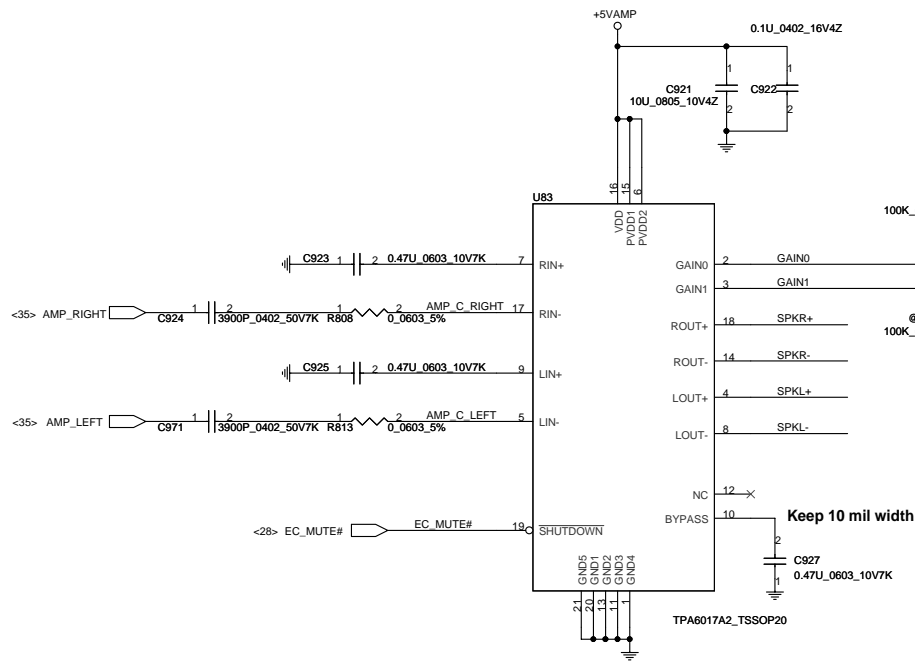
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AMP_RIGHT <36>

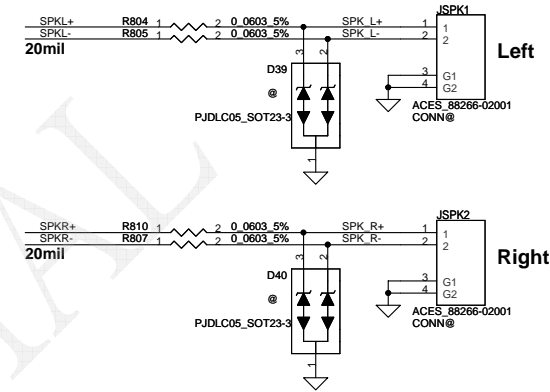
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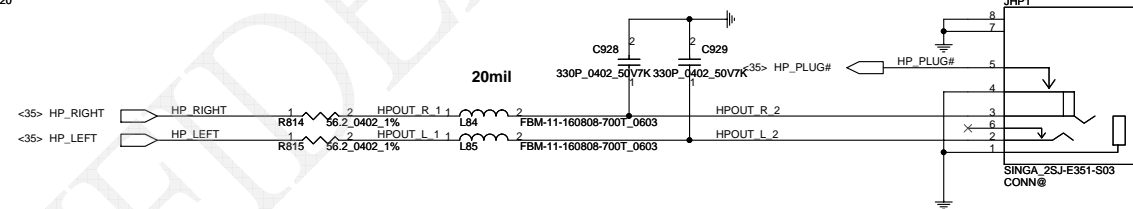
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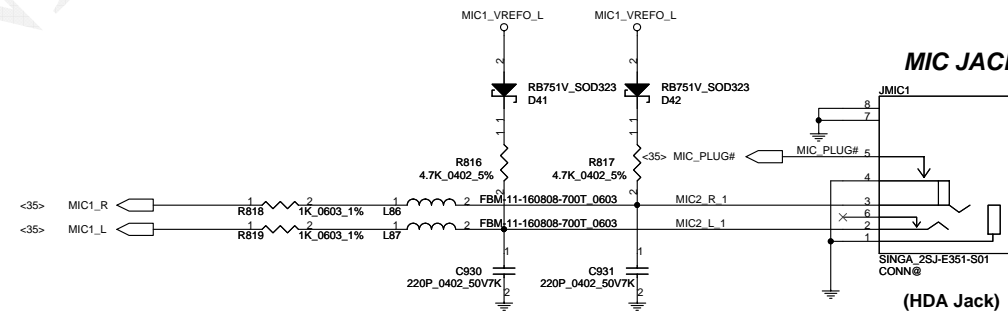
Int. Speaker Conn.



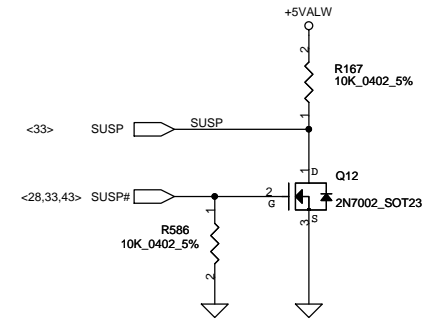
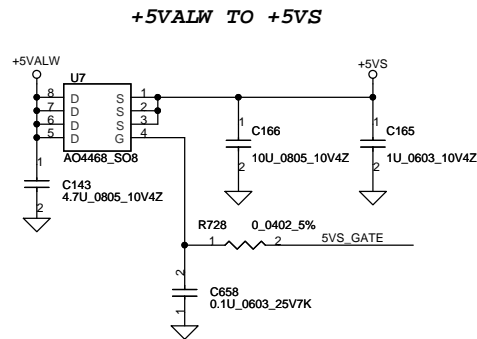
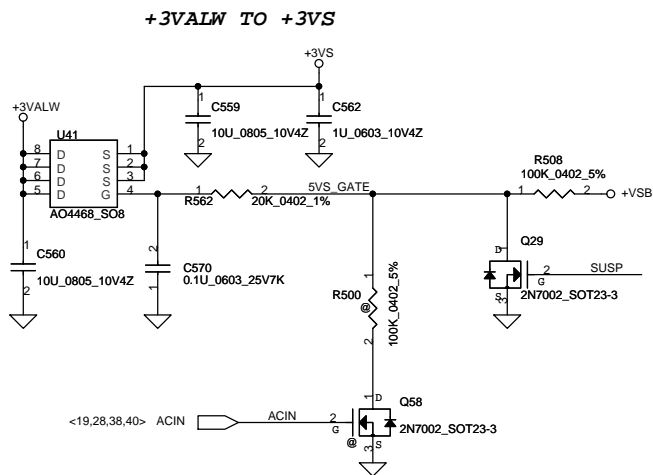
LINE Out/Headphone Out



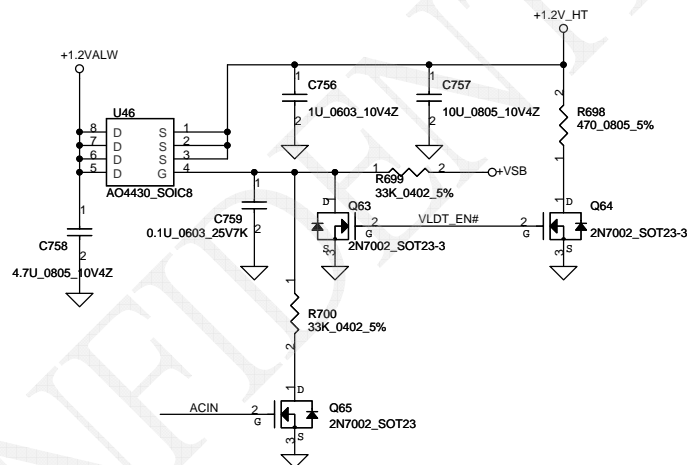
MIC JACK



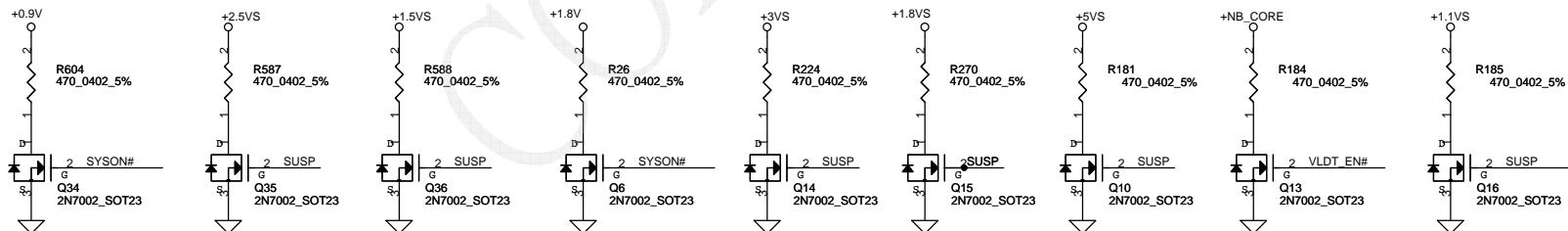
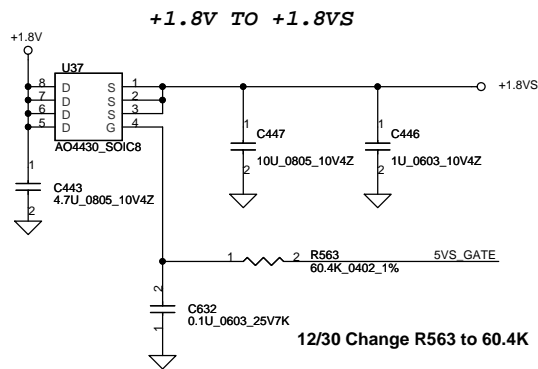
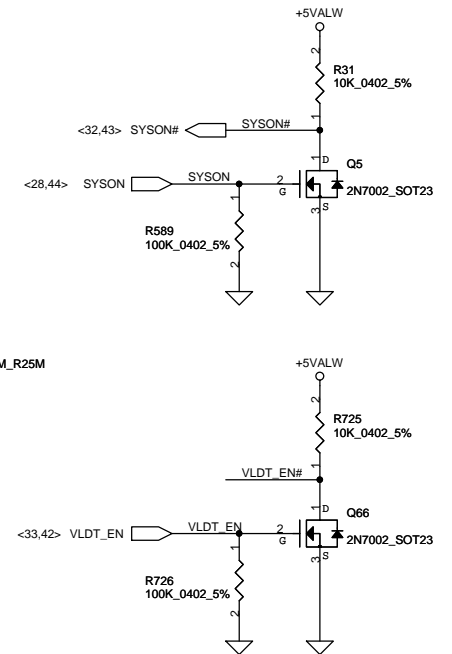
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+1.2VALW TO +1.2V_HT

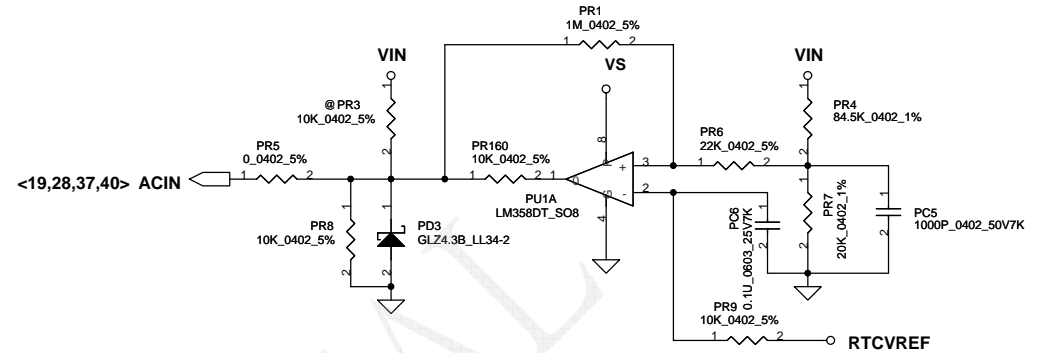
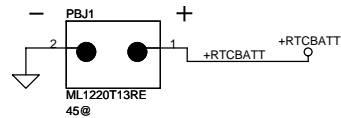
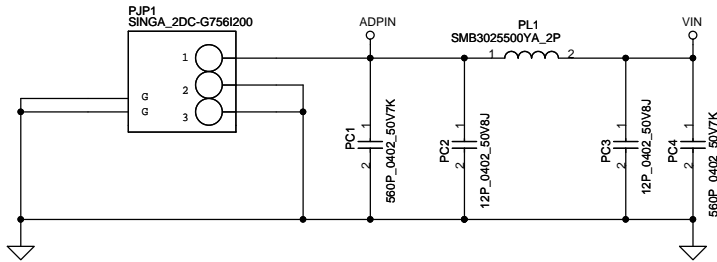


For PWR request

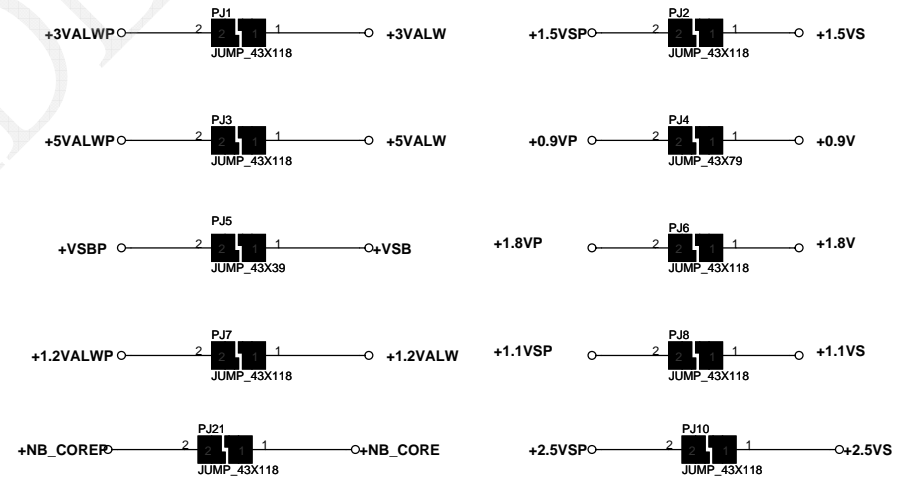
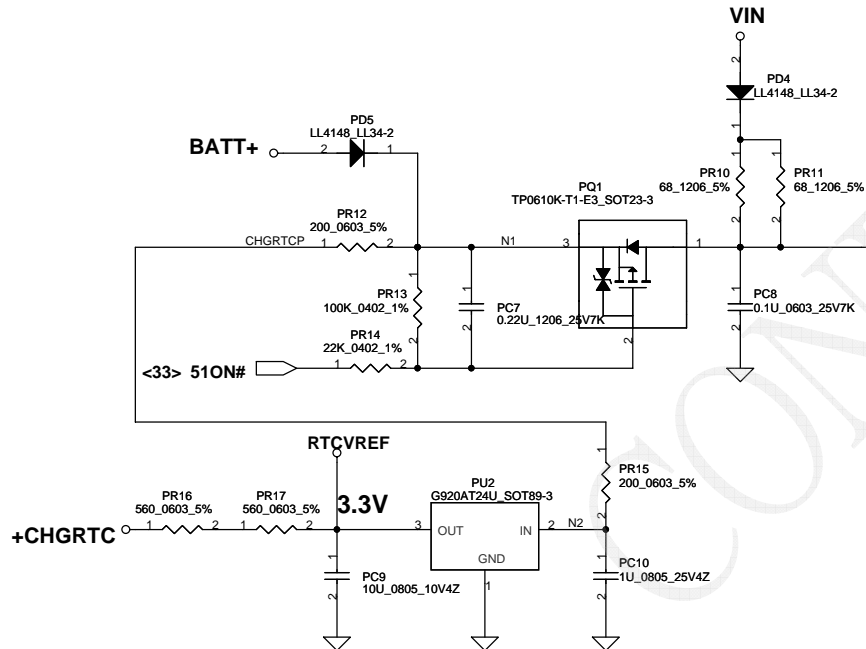


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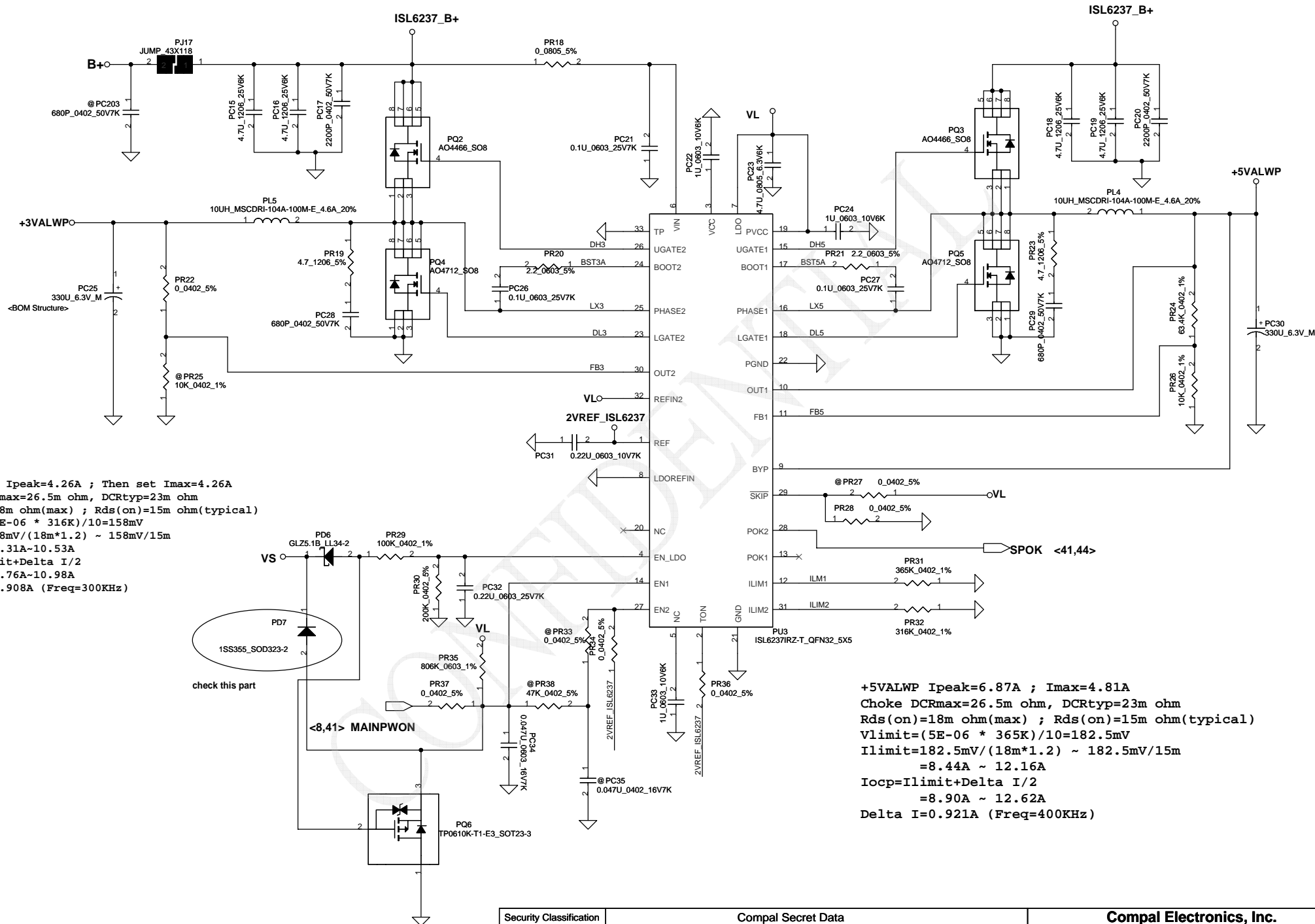
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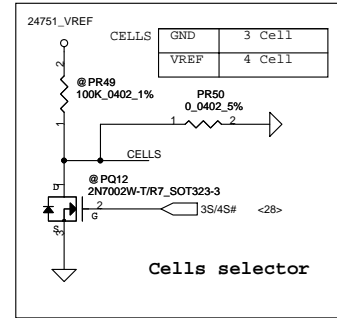
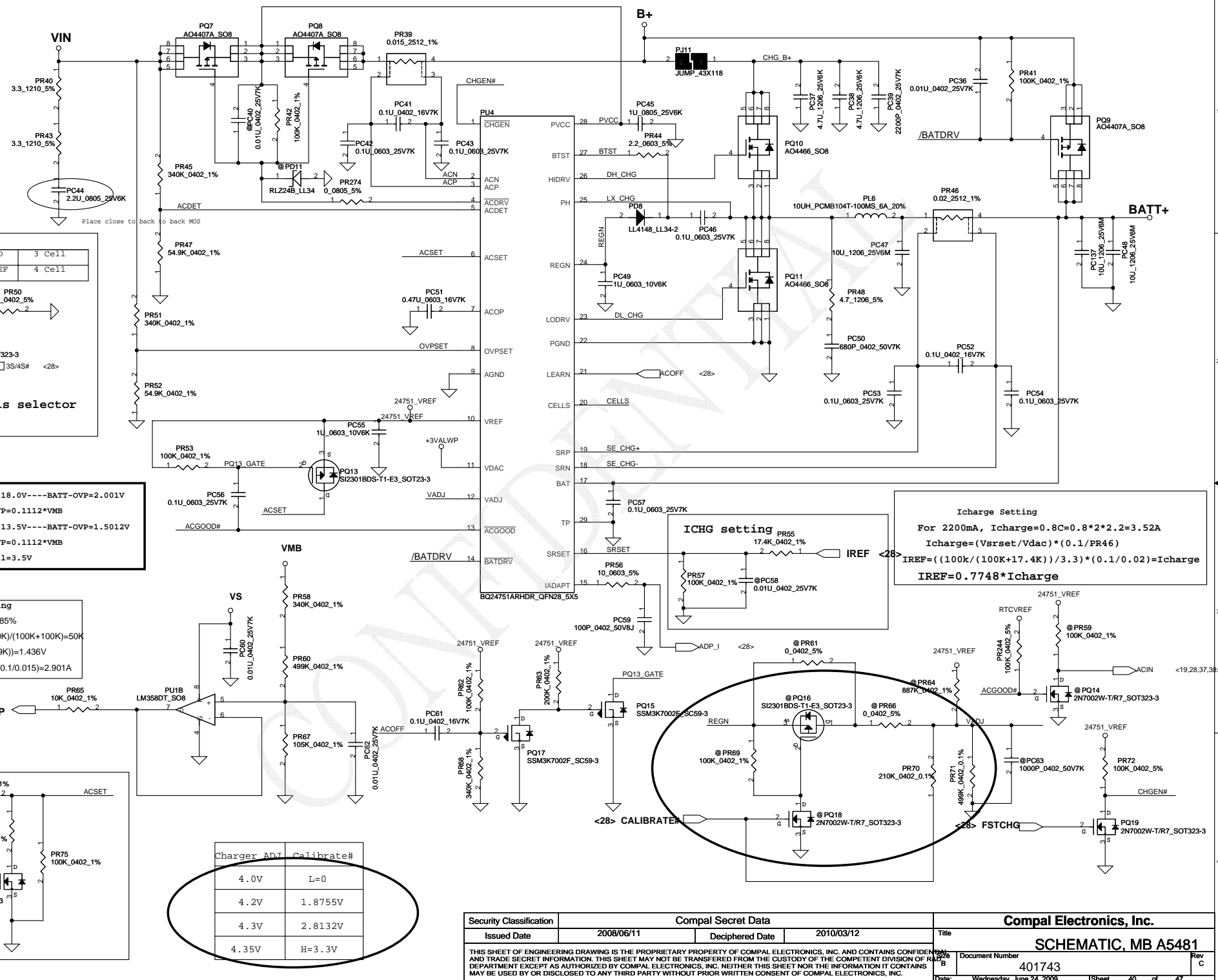
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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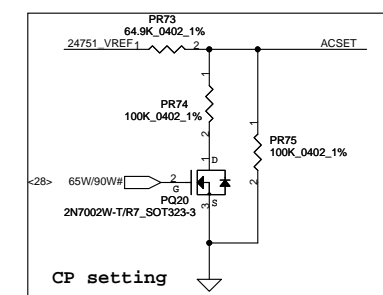
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Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

LI-4S : 18.0V----BATT-OVP=2.001V
BATT-OVP=0.1112*VMB
LI-3S : 13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

CP Point Setting
CP point=ladapter*85%
65W adapter R=(100K*100K)/(100K+100K)=50K
Vacset=3.3*(50K/(50K+64.9K))=1.436V
CP POINT=(1.436V/3.3V)*(0.1/0.015)=2.901A



Charger ADI Calibrate#

4.0V	L=0
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V

ICHG setting

PR55 17.4K_0402_1%

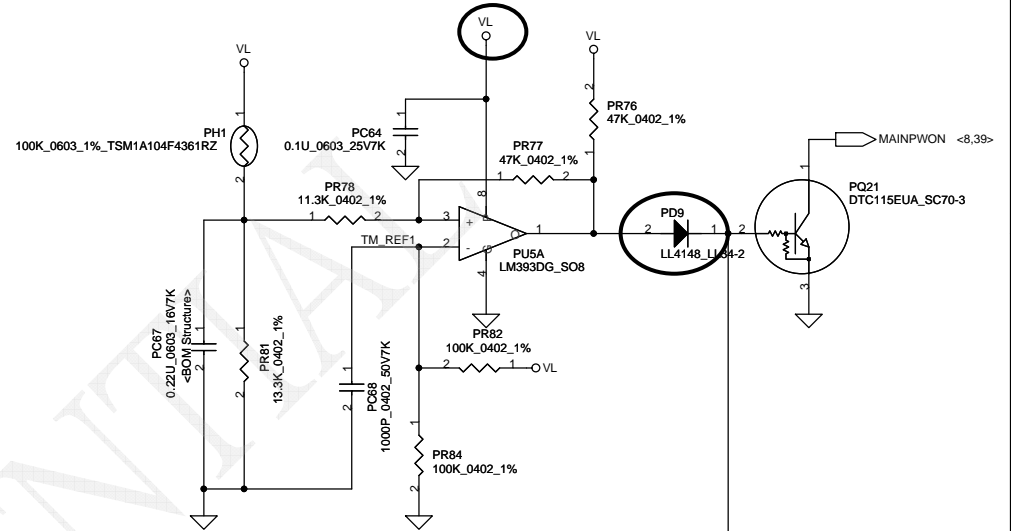
PR57 100K_0402_1%

PC58 0.01U_0402_25V7K

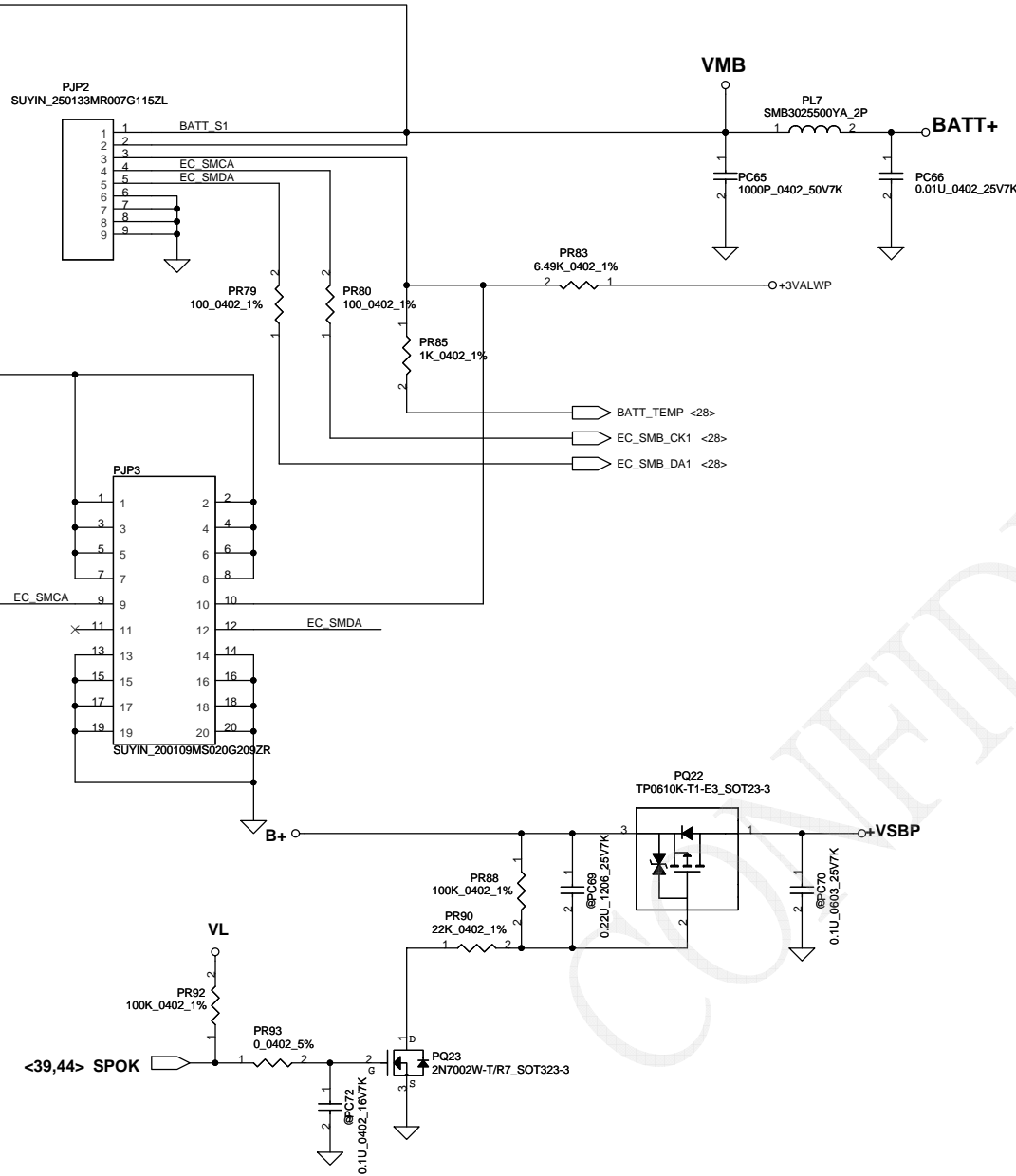
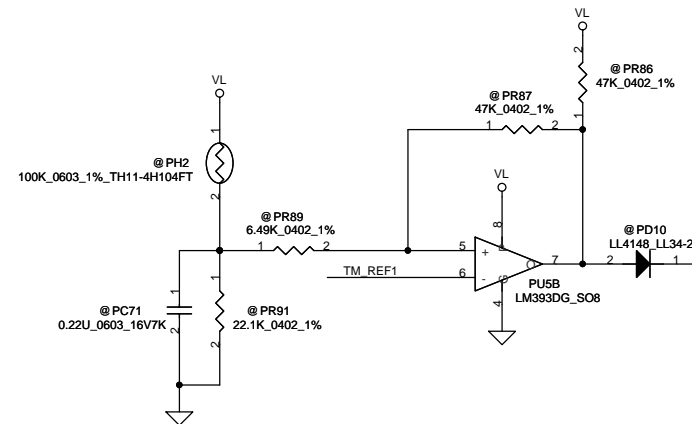
IREF <28>

Icharge Setting
For 2200mA, Icharge=0.8C=0.8*2*2.2=3.52A
Icharge=(Vsrset/Vdac)*(0.1/PR46)
IREF=((100k/(100K+17.4K))/3.3)*(0.1/0.02)=Icharge
IREF=0.7748*Icharge

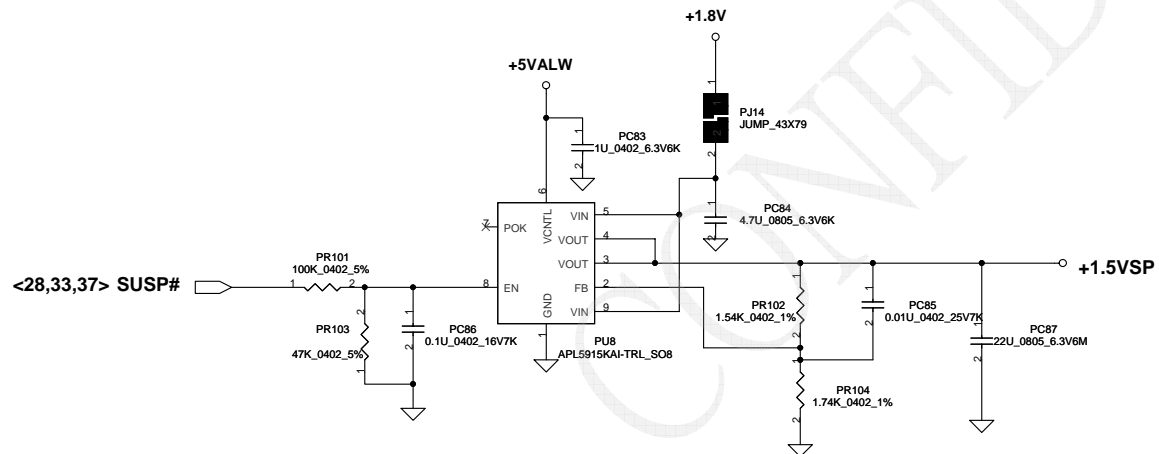
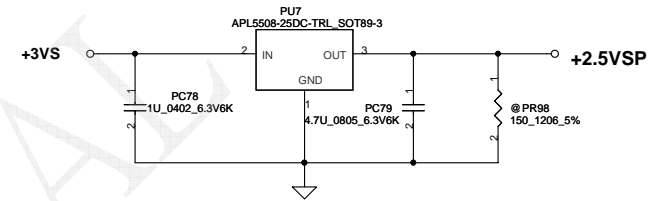
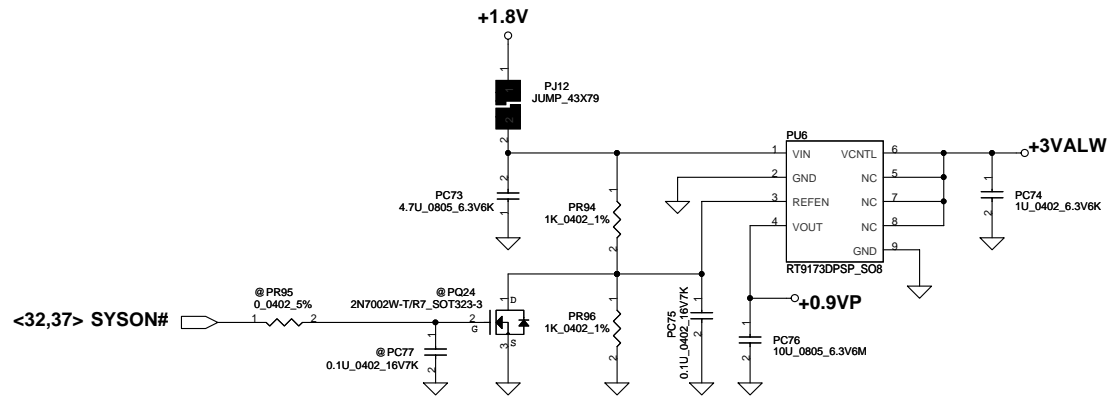
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



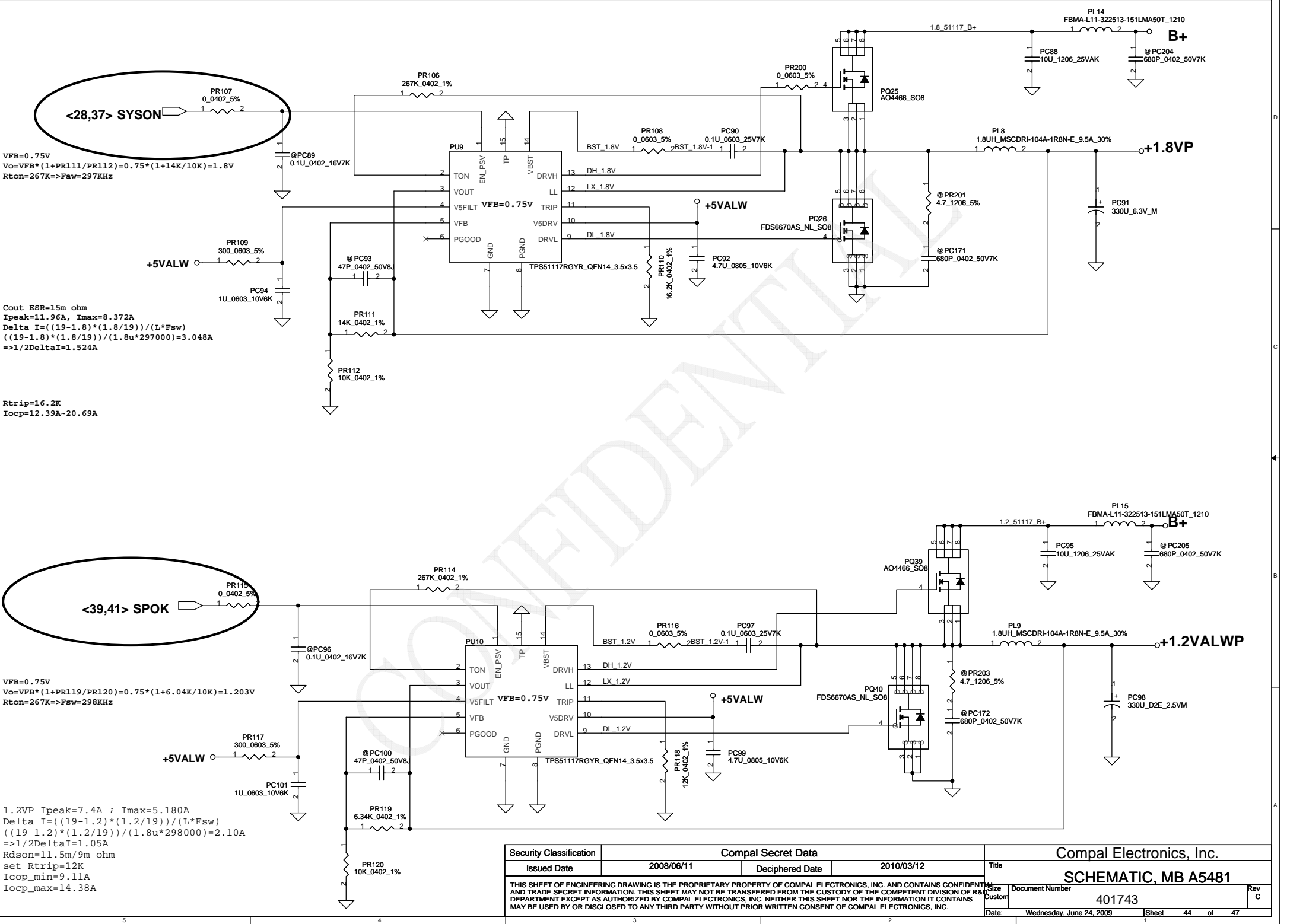
PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C



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VFB=0.75V
Vo=VFB*(1+PR111/PR112)=0.75*(1+14K/10K)=1.8V
Rton=267K=>Faw=297KHz

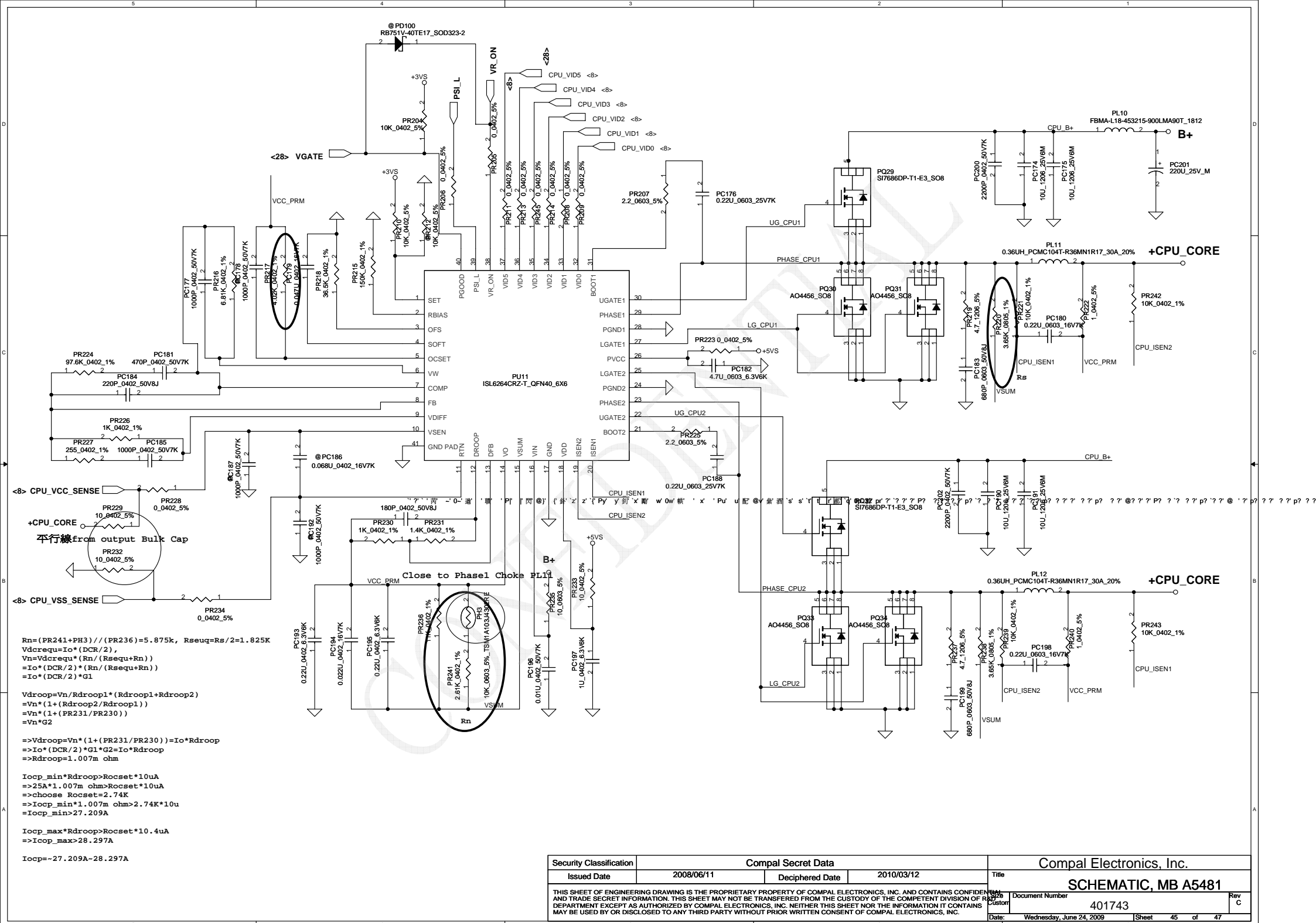
Cout ESR=15m ohm
Ipeak=11.96A, Imax=8.372A
Delta I=((19-1.8)*(1.8/19))/(L*Fsw)
((19-1.8)*(1.8/19))/(1.8u*297000)=3.048A
=>1/2Delta I=1.524A

Rtrip=16.2K
Iocp=12.39A-20.69A

VFB=0.75V
Vo=VFB*(1+PR119/PR120)=0.75*(1+6.04K/10K)=1.203V
Rton=267K=>Fsw=298KHz

1.2VP Ipeak=7.4A ; Imax=5.180A
Delta I=((19-1.2)*(1.2/19))/(L*Fsw)
((19-1.2)*(1.2/19))/(1.8u*298000)=2.10A
=>1/2Delta I=1.05A
Rdson=11.5m/9m ohm
set Rtrip=12K
Icop_min=9.11A
Iocp_max=14.38A

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW required to adjust from 1.14V to 1.12V	HW required to adjust from 1.14V to 1.12V	0.1	42	Change PR271 from SD034300180 (S RES 1/16W 3K +-1% 0402) to SD034324180 (S RES 1/16W 3.24K 0402 1%)	09, 05/07	to PVT
2	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Add PC208 SE076104K80 (S CER CAP .1U 16V K X7R 0402)	09, 05/07	to PVT
3	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Change PR247 from SD028000080 (S RES 1/16W 0 +-5% 0402) to SD028130180 (S RES 1/16W 1.3K 0402 5%)	09, 05/07	to PVT
4	NB_COREP working frequency has issue.	Because NB_COREP working frequency will be gitter while system at heavy loading. Change to larger ESR Cap will be solve.	0.1	42	Change PC210 from SGAI9331D00 (S POLY C 330U 2.5V M D2 TPE LESR15M H1.8) to SGA00002B00 (S POLY C 330U 6.3V M D2E ESR25M TPE H1.8)	09, 05/07	to PVT
5	BOM error	BOM error	0.1	42	Add PR270 SD28100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
6	BOM error	BOM error	0.1	42	Change PR103 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
7							
8							
9							
10							
11							
12							
13							
14							
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Version change list (P.I.R. List) for HW									
Item	Reason for change	Modify List	PG#	Date	Item	Reason for change	Modify List	Rev.	PG#
1	PWR update circuit			4/9	26				
2	BOM change	R118 reserve	P.18	4/9	27				
3	BOM change	Change R178, R179 to 90.9/158 ohm	P.16	4/9	28				
4	BOM change	R30, R39 reserve	P.24	4/9	29				
5	BOM change	Add C30	P.38	4/9	30				
6	BOM change	Add R634, R639	P.28	4/9	31				
7	BOM change	C383 Reserve	P.24	4/9	32				
8		Pop R419	P.20	4/10	33				
9	PWR update circuit			5/15					
10	For Panel flash issue	R1.D2 Reserve, pop R763	P.24	5/18					
11	For Panel flash issue	Add R414 and non-pop	P.24	5/18					
12	Lid_SW intial issue	Add R19	P.28	5/18					
13	HPET timer issue	Change C288,C290 to 33P	P.16	5/18					
14	BOM change	change C276,C279 10P to 27P	P.19	5/19					
15									
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Version change list (P.I.R. List) for HW									
Item	Reason for change	Modify List	PG#	Date	Item	Reason for change	Modify List	Rev.	PG#
1	PWR update circuit			4/9	26				
2	BOM change	R118 reserve	P.18	4/9	27				
3	BOM change	Change R178, R179 to 90.9/158 ohm	P.16	4/9	28				
4	BOM change	R30, R39 reserve	P.24	4/9	29				
5	BOM change	Add C30	P.38	4/9	30				
6	BOM change	Add R634, R639	P.28	4/9	31				
7	BOM change	C383 Reserve	P.24	4/9	32				
8		Pop R419	P.20	4/10	33				
9	PWR update circuit			5/15					
10	For Panel flash issue	R1.D2 Reserve, pop R763	P.24	5/18					
11	For Panel flash issue	Add R414 and non-pop	P.24	5/18					
12	Lid_SW intial issue	Add R19	P.28	5/18					
13	HPET timer issue	Change C288,C290 to 33P	P.16	5/18					
14	BOM change	change C276,C279 10P to 27P	P.19	5/19					
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Item	Reason for change	Modify List	PG#	Date	Item	Reason for change	Modify List	Rev.	PG#
1	PWR update circuit			4/9	26				
2	BOM change	R118 reserve	P.18	4/9	27				
3	BOM change	Change R178, R179 to 90.9/158 ohm	P.16	4/9	28				
4	BOM change	R30, R39 reserve	P.24	4/9	29				
5	BOM change	Add C30	P.38	4/9	30				
6	BOM change	Add R634, R639	P.28	4/9	31				
7	BOM change	C383 Reserve	P.24	4/9	32				
8		Pop R419	P.20	4/10	33				
9	PWR update circuit			5/15					
10	For Panel flash issue	R1.D2 Reserve, pop R763	P.24	5/18					
11	For Panel flash issue	Add R414 and non-pop	P.24	5/18					
12	Lid_SW intial issue	Add R19	P.28	5/18					
13	HPET timer issue	Change C288,C290 to 33P	P.16	5/18					
14	BOM change	change C276,C279 10P to 27P	P.19	5/19					
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