

Compal Confidential

QML70 Schematics Document

AMD Comal

APU Trinity / Hudson M3 / Thames XT M2
UMA Only / PX Muxless with BACO

2011-10-17

LA-8371P REV: 0.2

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Model Name : QML70



VRAM 2G/1G
128M x16 x 8 /
64M x 16 x 8

page 24, 25

DDR3

Thermal Sensor
ADM1032
page 19

ATI Thames XT M2
uFCBGA-962

+1.0VSG, +1.5VSG, +1.8VSG,
+3VSG, +VGA_CORE, +VDDCI

Page 18~25

GFX x 16 Gen2

DP x4 (DP0 TXP/N0 ~ 3)

APU HDMI
(UMA / Muxless)

DP x2 (DP2 TXP/N0 ~ 1)

HDMI Conn.
page 29

LVDS Conn.
page 28

LVDS

LVDS Translator
RTD2136S-VE-CG
page 27

CRT Conn.
page 28

FCH CRT (VGA DAC)

GPP1

GPP2

LAN(GbE)
RTL8111F-CGT
page 30

RJ45
page 30

MINI Card 1
WLAN w/ BT
page 33

LED
page 39

RTC CKT.
page 13

DC/DC
Interface CKT.
page 39

VGA DC/DC
Interface CKT.
page 26

Power Circuit
page 40~50

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AMD FS1r2 APU
Trinity
uPGA-722 Package

+APU_CORE, +APU_CORE_NB,
+1.5V, +1.2VS, +2.5VS

Page 6~10

P_GPP x 2
GEN1

DP x4 (DP1 TXP/N0 ~ 3)

UMI

FCH
Hudson-M3
uFCBGA-656

+3V_PCH, +1.1VALW, +1.1VS

Page 13~17

LPC BUS

ENE KB9012
page 37

SPI ROM
128KB
(Reserve)
page 37

Touch Pad
page 38

Int.KBD
page 38

Memory BUS(DDR3)

Dual Channel

1.5V DDRIII 800~1333MHz

204pin DDRIII-SO-DIMM X2

BANK 0, 1, 2, 3

Page 11, 12

USB 2.0 + 3.0
page 35

USB 2.0 + 3.0
page 35

USB2.0
page 30

USB2.0
page 30

CMOS
Camera
page 28

Mini Card
(with BT)
page 33

USB
3.3V 48MHz

USB3.0 Port 0
USB2.0 Port 10

USB3.0 Port 1
USB2.0 Port 11

USB2.0 Port 0

USB2.0 Port 1

USB2.0 Port 2

USB2.0 Port 3

HD Audio 3.3V 24.576MHz/48MHz

USB2.0 Port 4

SATA Gen2

port 0

port 1

port 2

SATA HDD1
Conn.
page 34

SATA HDD2
Conn.
page 34

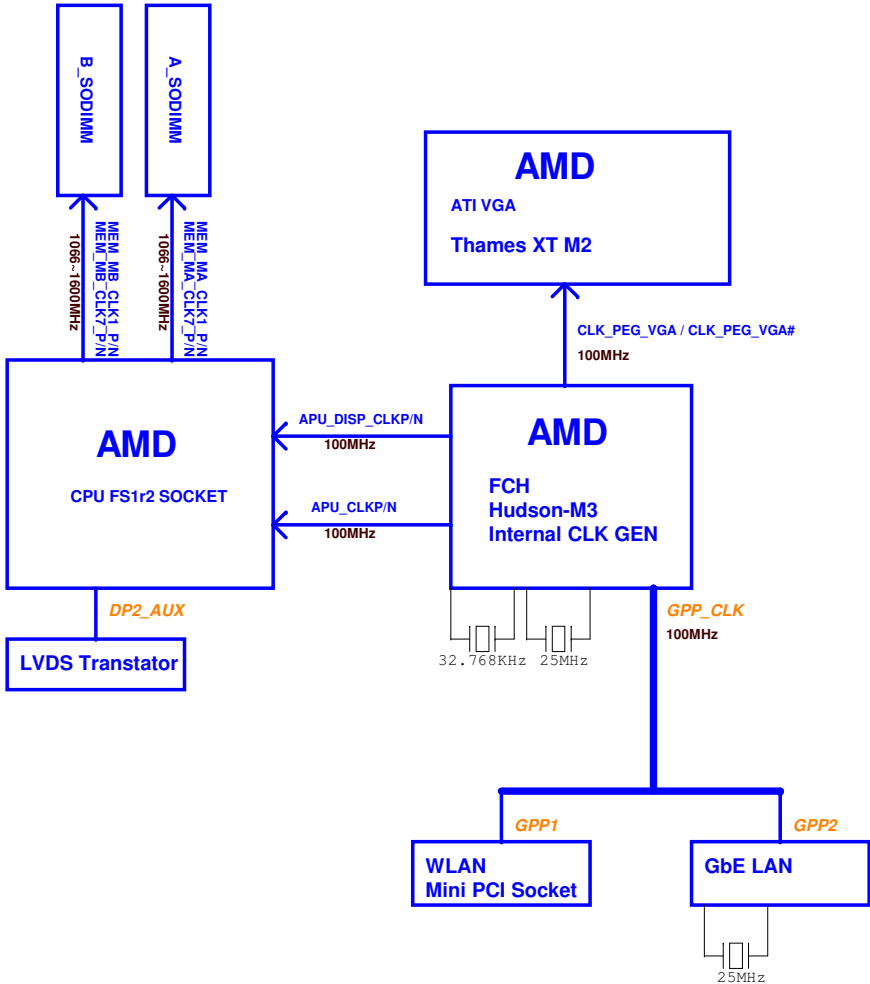
ODD
Conn.
page 34

HDA Codec
ALC269Q-VB5-GR
page 31

Card Reader
RTS5137-GR
page 32

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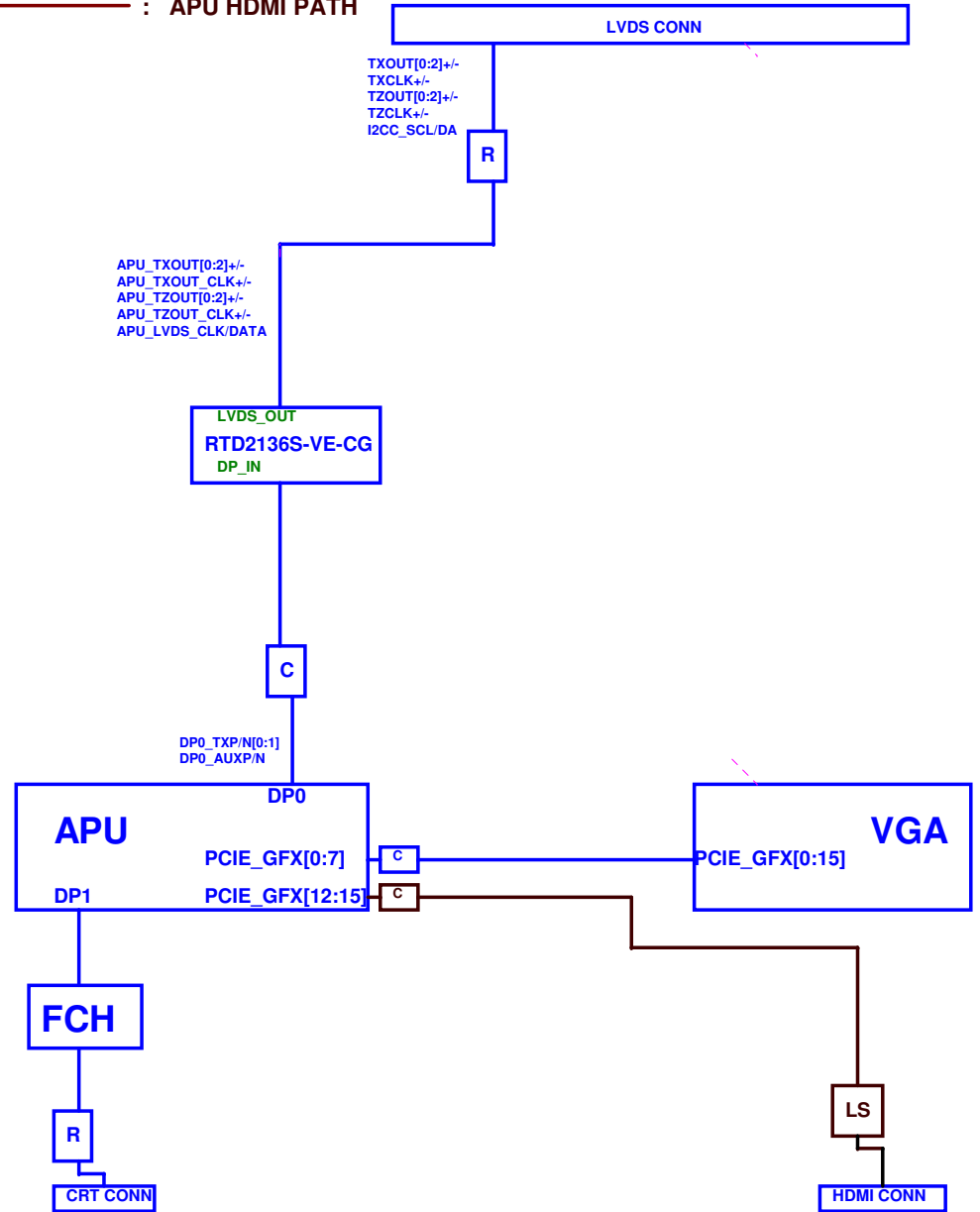
CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION

: LVDS PATH

: APU HDMI PATH



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Voltage Rails

Power Plane	Description	S1	S3	S4/S5	Deep S3
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF	ON
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*	OFF
+3V_PCH	3.3V switched power rail for FCH	ON	ON	ON*	OFF
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF	OFF
+3VSG	1.8V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF	ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*	ON
+LAN_IO	3.3V power rail for LAN	ON	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*	ON
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*	ON
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032	1001 101X b	9AH
			AMD Thames XT M2	1000 001X b	82H
			AMD FS1r2 (APU)	1001 1000 b	98H
			RTD2132S (TL)	1010 1000 b	A8H

FCH
SM Bus 0 address

FCH
SM Bus 1 address

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	D0			
DDR DIMM2	1101 001X b	D2			

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BOM Structure	BTO Item
PX@	Use VGA (Mux)
X76@	VRAM ID Table
AI	Use AI Charger
nonAI@	Do not use AI Charger
CARD@	Use Card Reader IC
nonCARD@	do not use Card Reader IC
X76L01@	Use Hynix GDDR3 1GB VRAM
X76L02@	Use Hynix GDDR3 2GB VRAM
X76L03@	Use Samsung GDDR3 1GB VRAM
X76L04@	Use Samsung GDDR3 2GB VRAM
930@	Use EC KB930
9012@	Use EC KB9012

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0 +/- 5%	0 V	0 V	0.155 V
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V

RTC BAT	VDDBT_RTC_G
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VRAM 1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VSG	2.4 A

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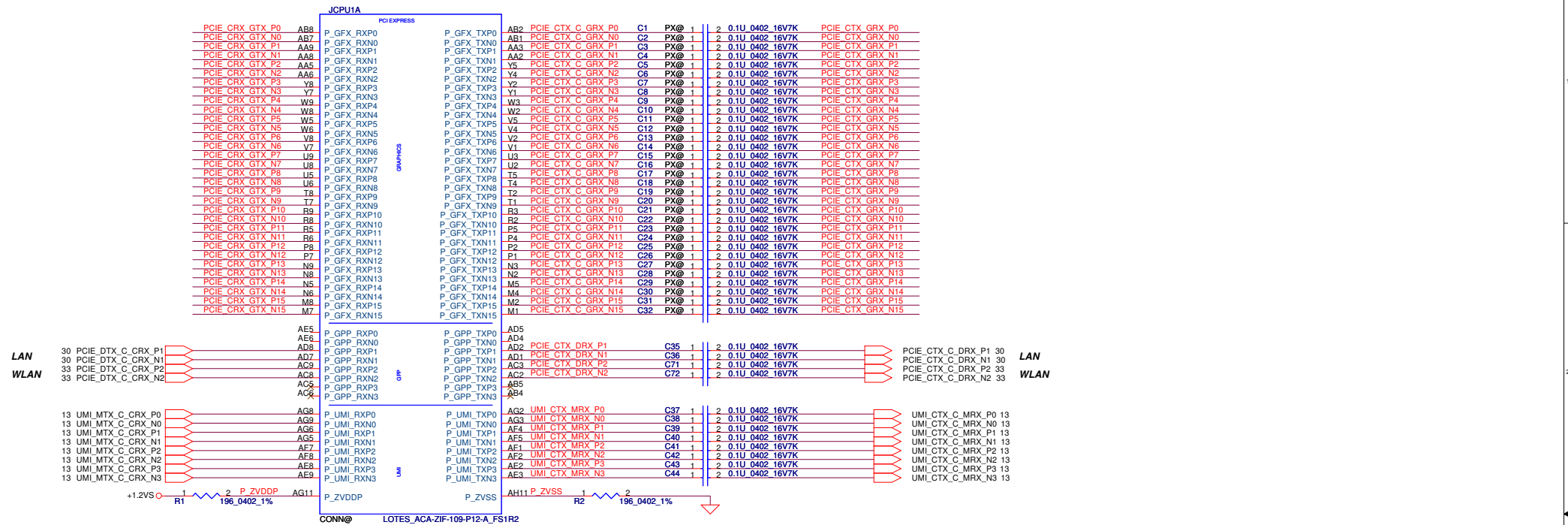
18 PCIE_CRX_GTX_P[0..15]

18 PCIE_CRX_GTX_N[0..15]

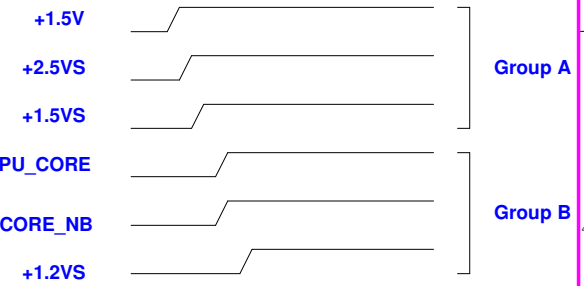
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PCIE_CTX_GRX_P[0..15] 18

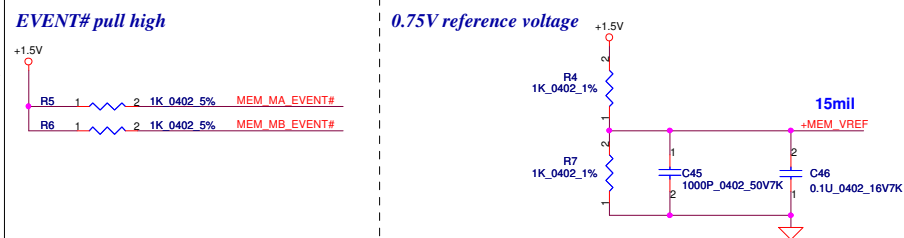
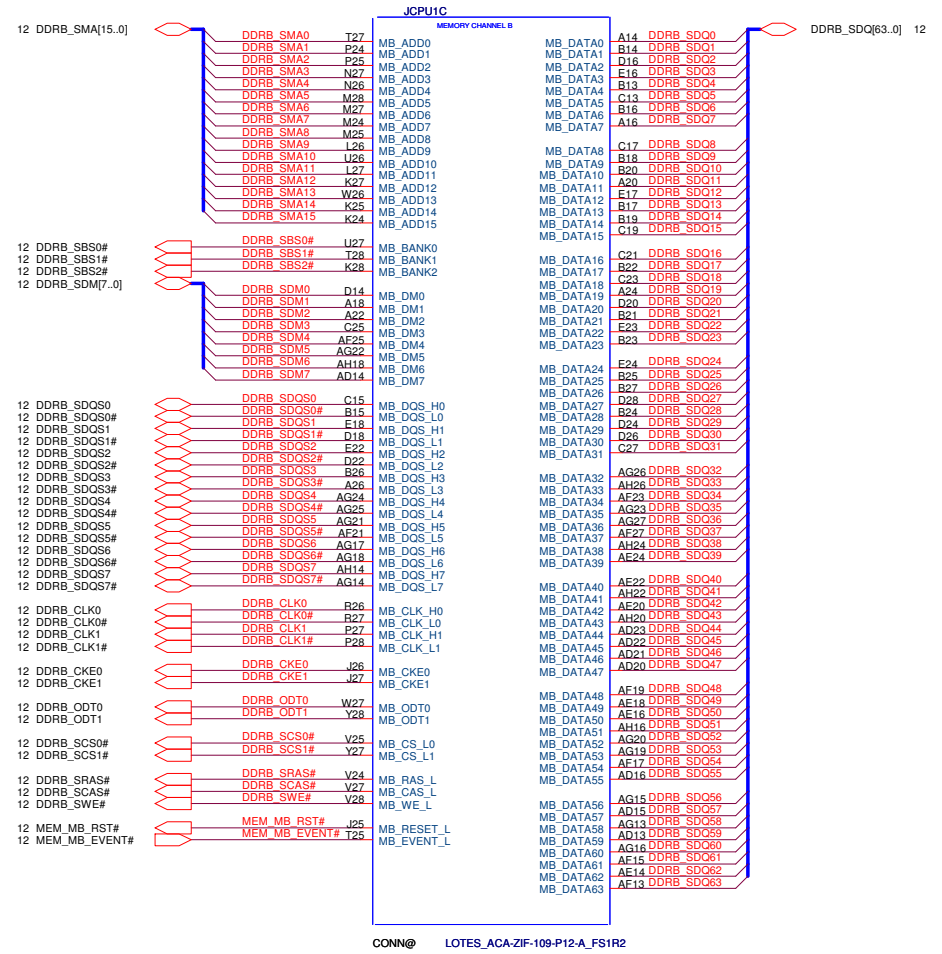
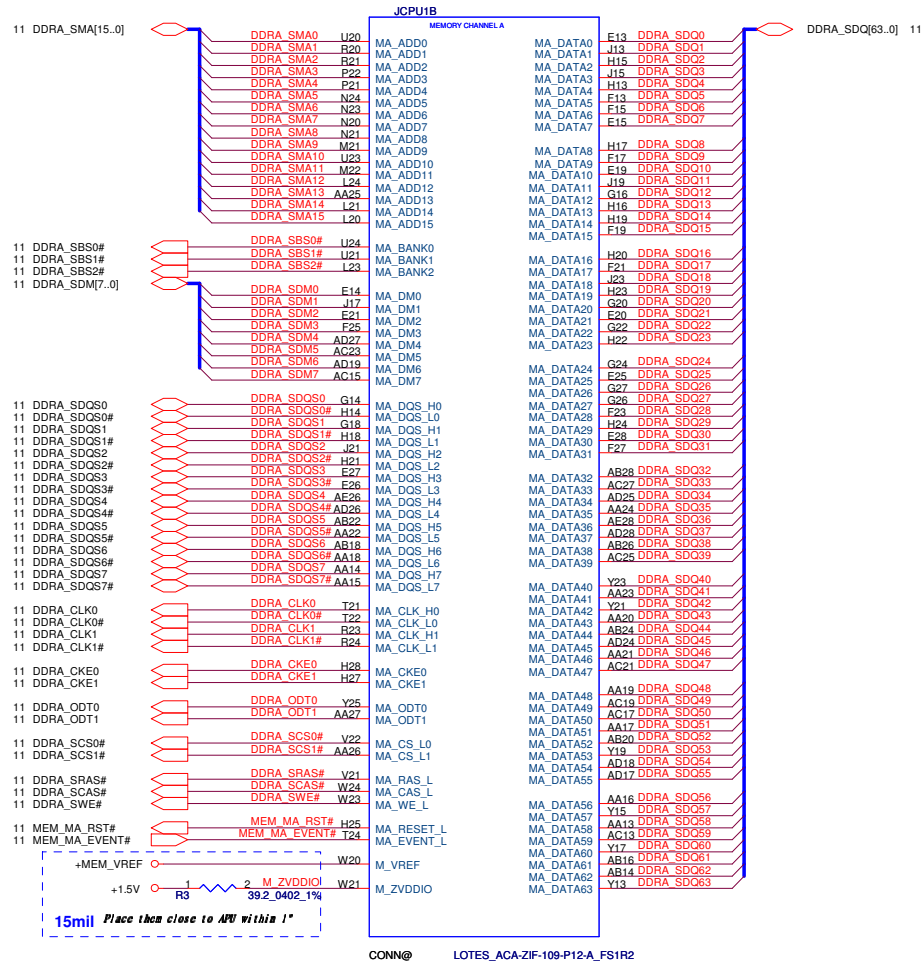
PCIE_CTX_GRX_N[0..15] 18



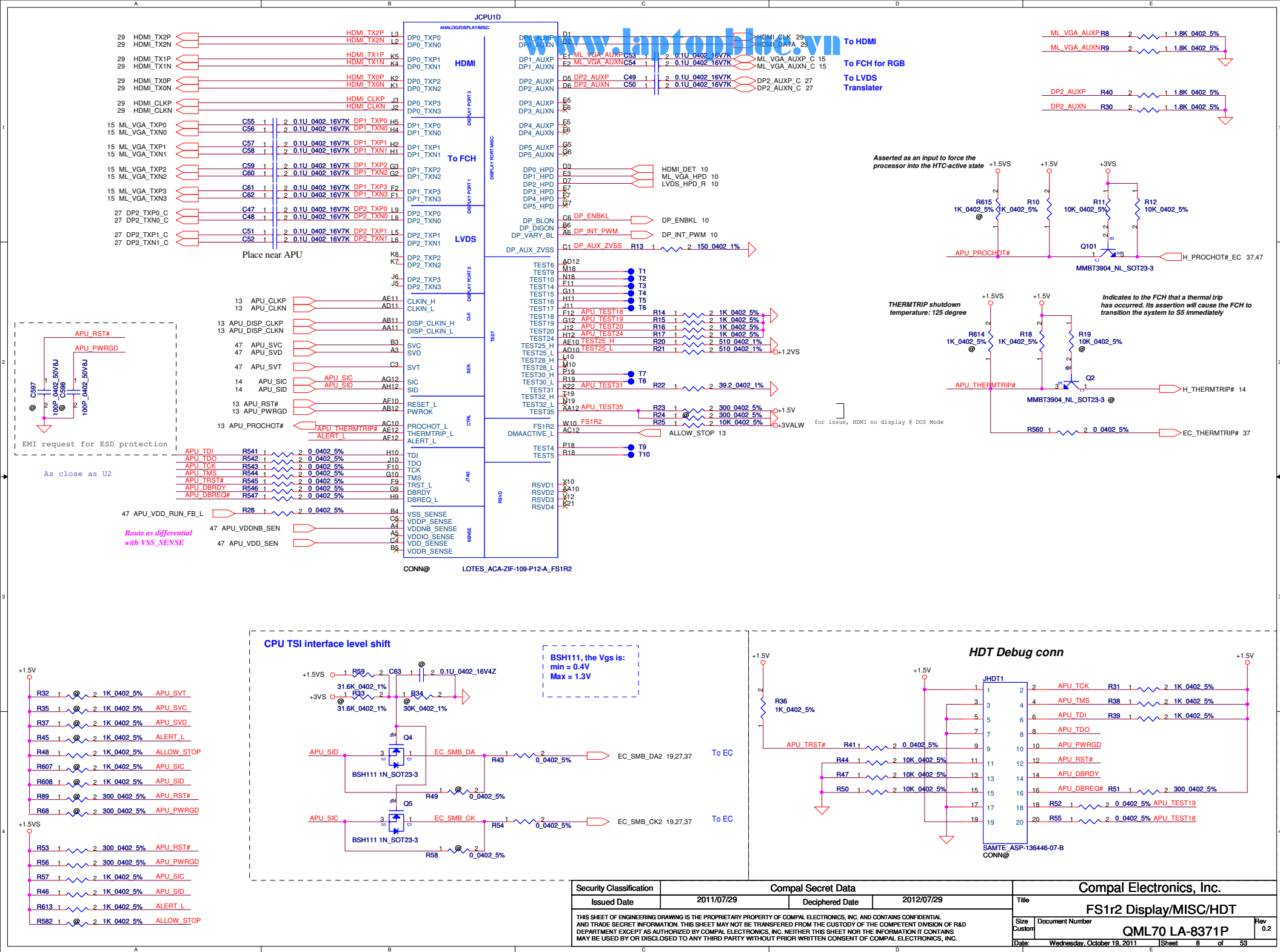
Power Sequence of APU



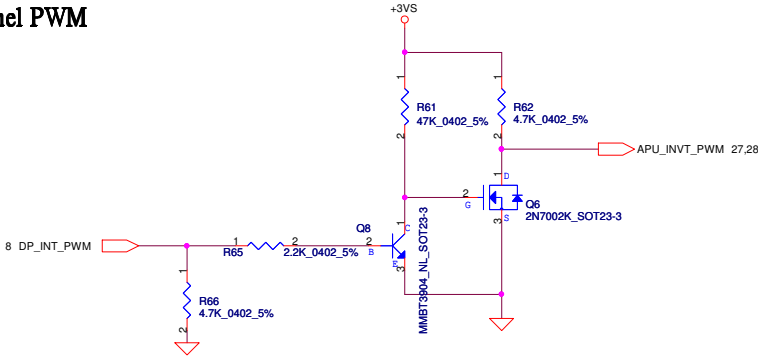
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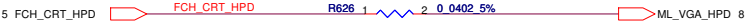
Panel PWM



HPD

CRT HPD

From FCH



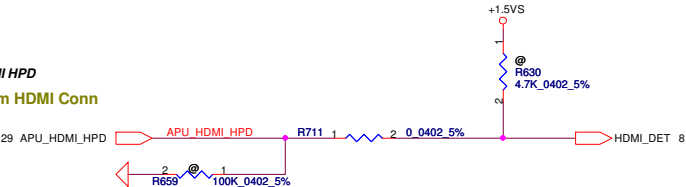
Translator HPD

From Translator

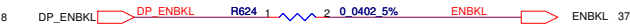


HDMI HPD

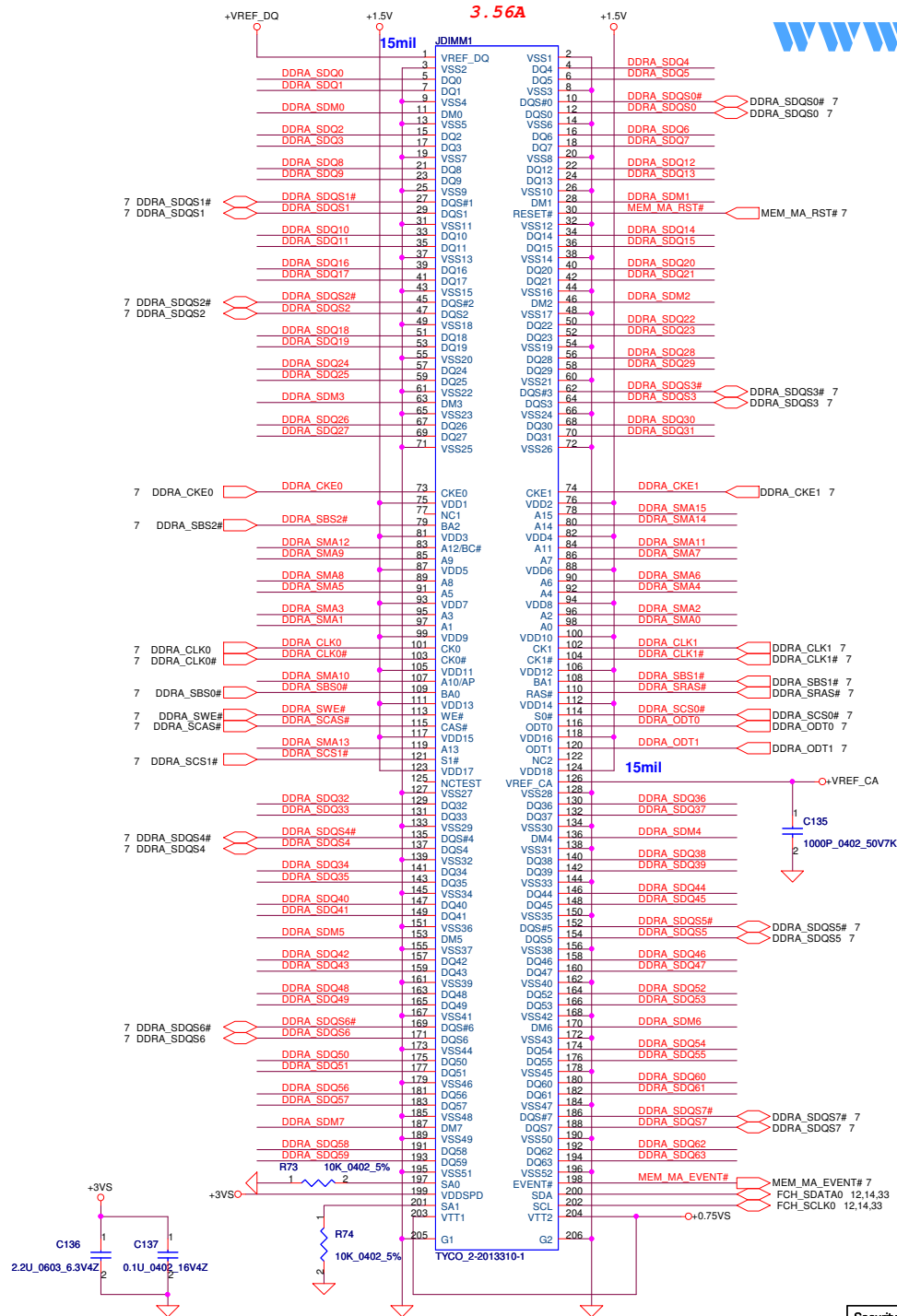
From HDMI Conn



Panel ENBKL



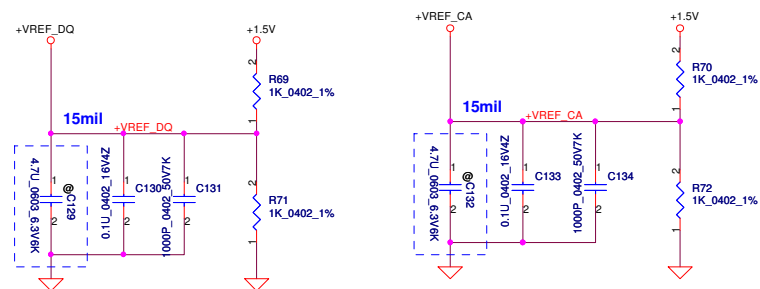
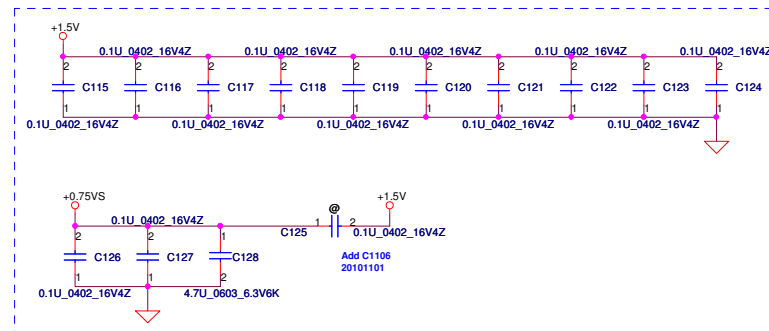
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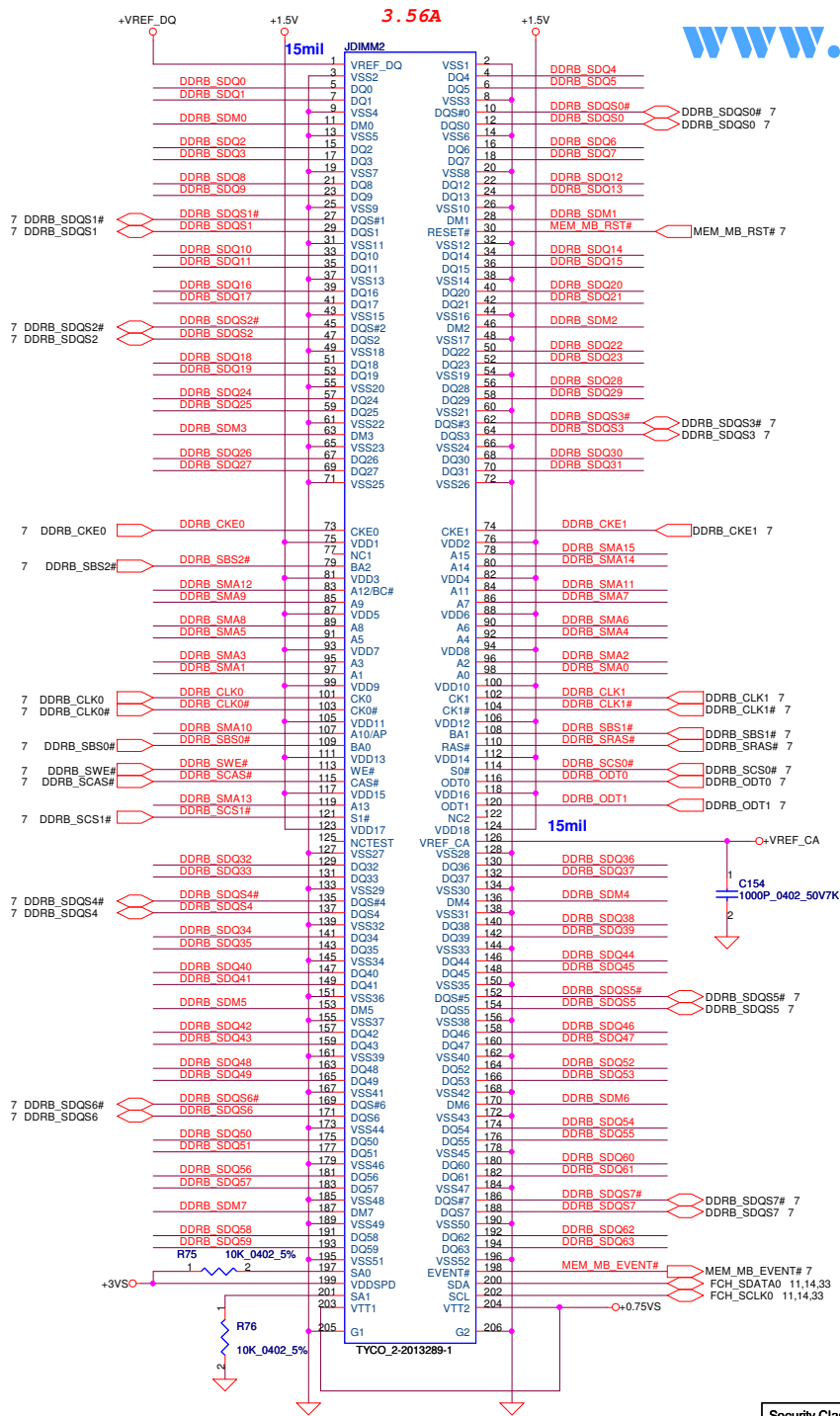
DIMM_A STD H:9.2mm
 <Address: 00>



Place near DIMM1



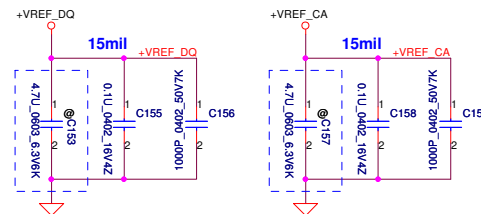
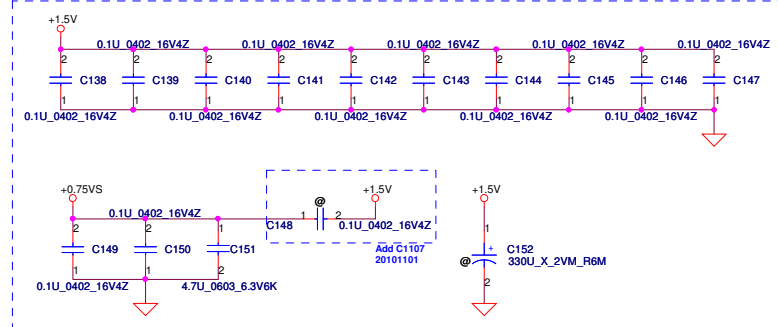
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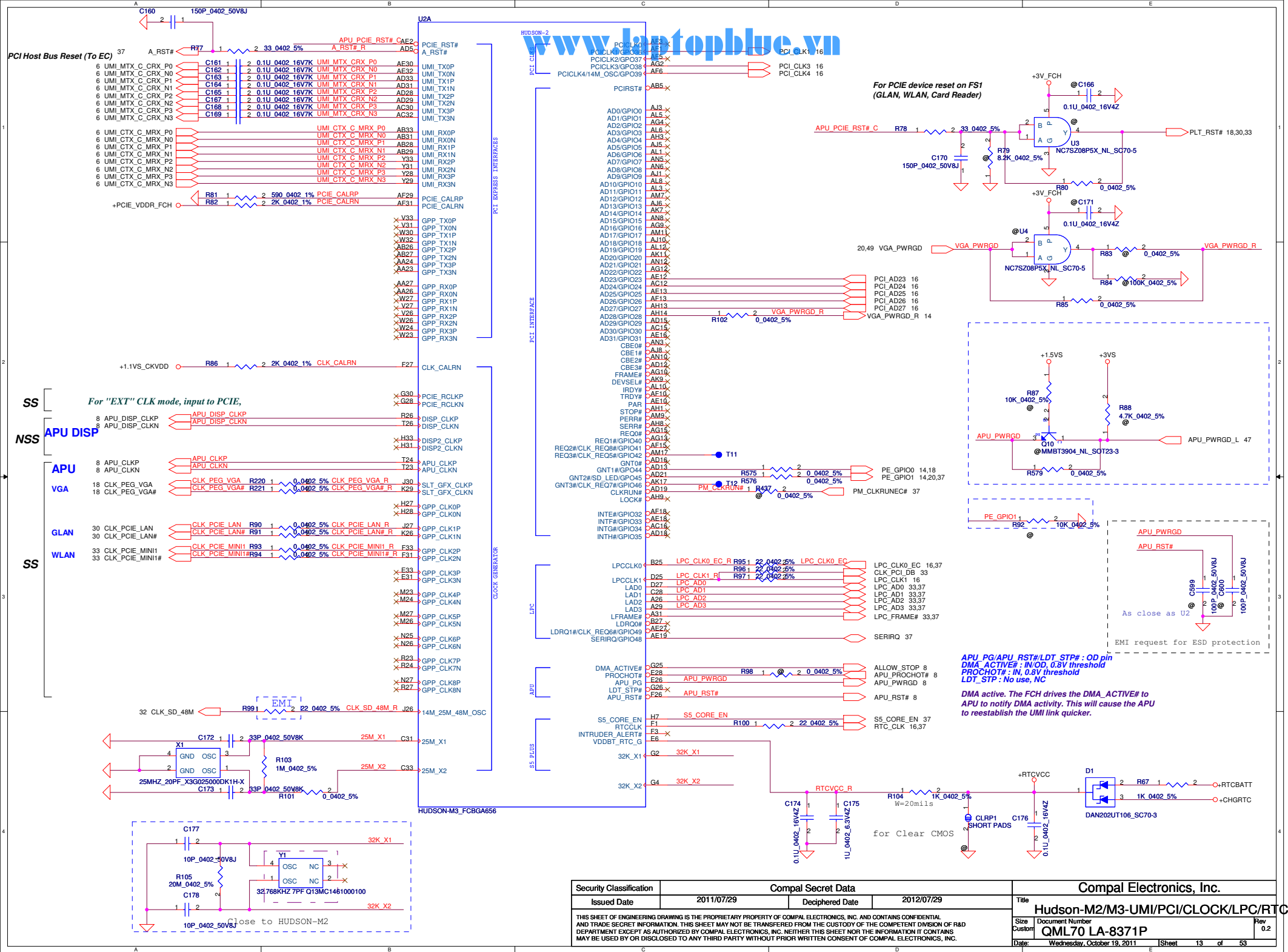
DIMM_B STD H:5.2mm
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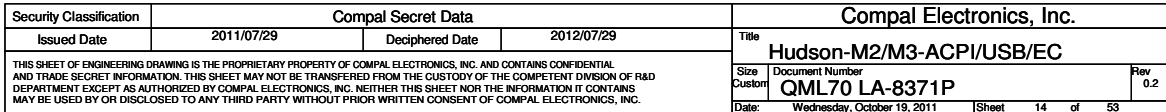


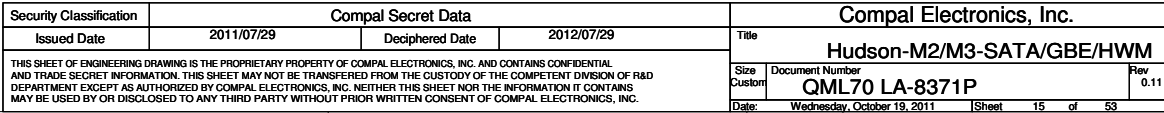
Place near DIMM2



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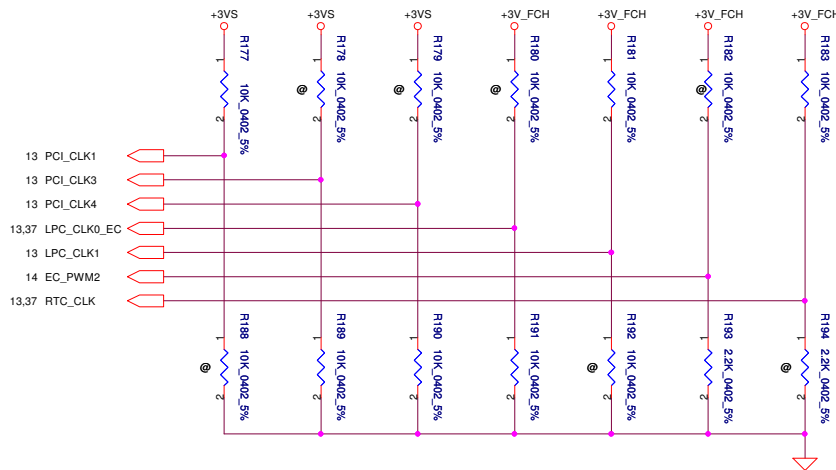






STRAP PINS

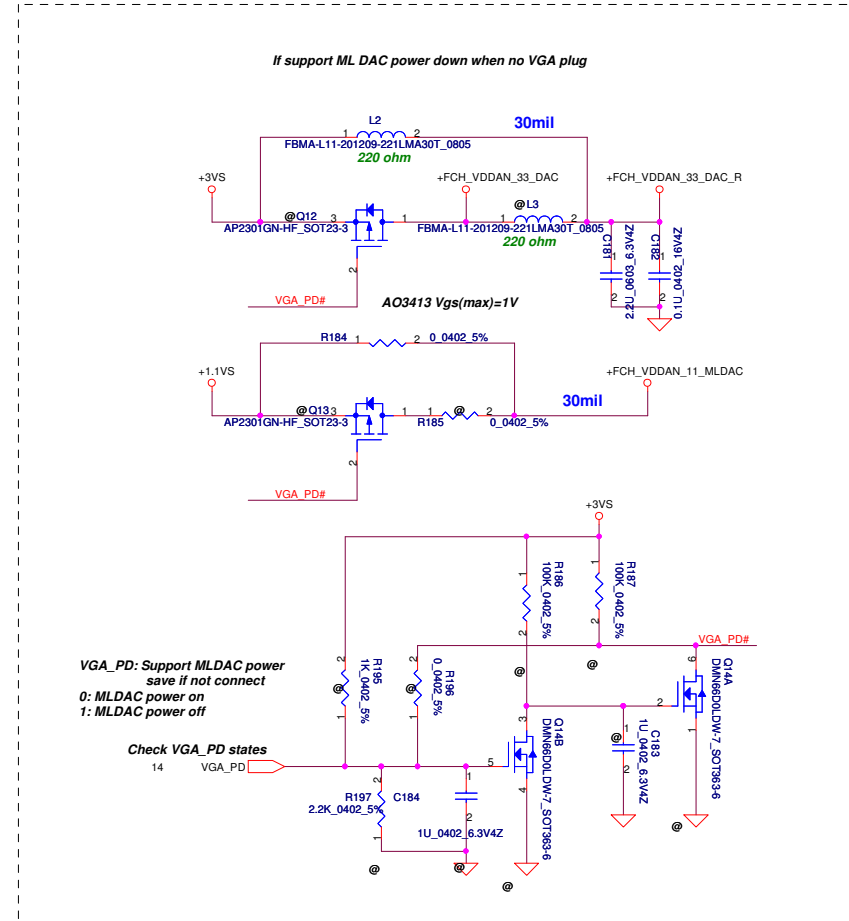
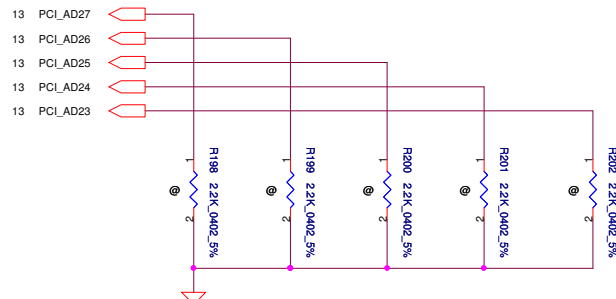
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED



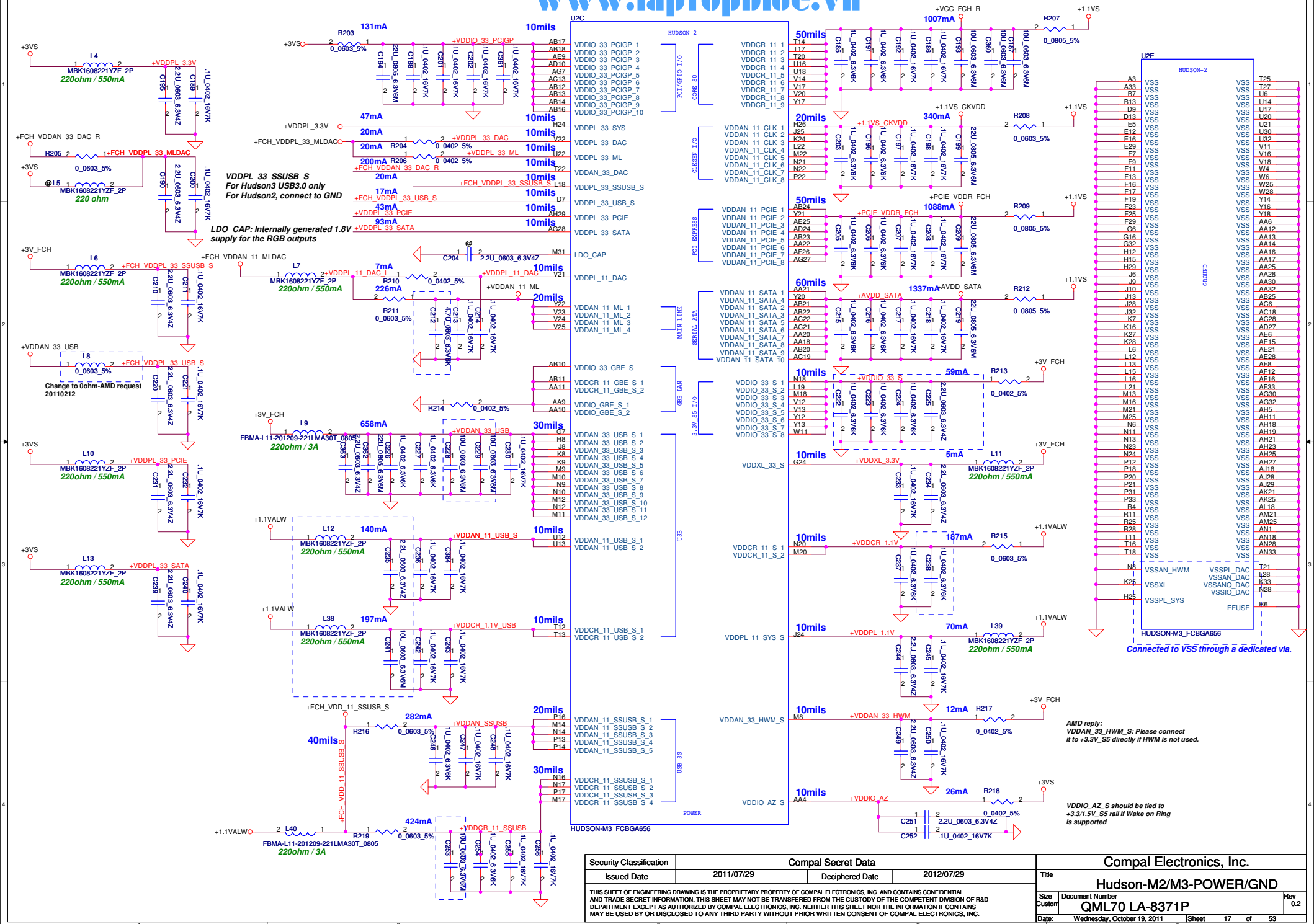
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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								Hudson-M2/M3-STRAP			
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6 PCIE_CTX_GRX_P[15..0]
6 PCIE_CTX_GRX_N[15..0]

PCIE_CTX_GRX_P[15..0]
PCIE_CTX_GRX_N[15..0]

U7A

PCIE_CTX_GRX_P0 AA38 PCIE_RX0P
PCIE_CTX_GRX_N0 Y37 PCIE_RX0N

PCIE_CTX_GRX_P1 Y35 PCIE_RX1P
PCIE_CTX_GRX_N1 W36 PCIE_RX1N

PCIE_CTX_GRX_P2 W38 PCIE_RX2P
PCIE_CTX_GRX_N2 V37 PCIE_RX2N

PCIE_CTX_GRX_P3 Y35 PCIE_RX3P
PCIE_CTX_GRX_N3 U36 PCIE_RX3N

PCIE_CTX_GRX_P4 U38 PCIE_RX4P
PCIE_CTX_GRX_N4 T37 PCIE_RX4N

PCIE_CTX_GRX_P5 T35 PCIE_RX5P
PCIE_CTX_GRX_N5 R36 PCIE_RX5N

PCIE_CTX_GRX_P6 R38 PCIE_RX6P
PCIE_CTX_GRX_N6 P37 PCIE_RX6N

PCIE_CTX_GRX_P7 P35 PCIE_RX7P
PCIE_CTX_GRX_N7 N36 PCIE_RX7N

PCIE_CTX_GRX_P8 N38 PCIE_RX8P
PCIE_CTX_GRX_N8 M37 PCIE_RX8N

PCIE_CTX_GRX_P9 M35 PCIE_RX9P
PCIE_CTX_GRX_N9 L36 PCIE_RX9N

PCIE_CTX_GRX_P10 L38 PCIE_RX10P
PCIE_CTX_GRX_N10 K37 PCIE_RX10N

PCIE_CTX_GRX_P11 K35 PCIE_RX11P
PCIE_CTX_GRX_N11 J36 PCIE_RX11N

PCIE_CTX_GRX_P12 J38 PCIE_RX12P
PCIE_CTX_GRX_N12 H37 PCIE_RX12N

PCIE_CTX_GRX_P13 H35 PCIE_RX13P
PCIE_CTX_GRX_N13 G36 PCIE_RX13N

PCIE_CTX_GRX_P14 G38 PCIE_RX14P
PCIE_CTX_GRX_N14 F37 PCIE_RX14N

PCIE_CTX_GRX_P15 F35 PCIE_RX15P
PCIE_CTX_GRX_N15 E37 PCIE_RX15N

PCI EXPRESS INTERFACE

PCIE_CRX_GTX_P[15..0]
PCIE_CRX_GTX_N[15..0]

PCIE_CRX_GTX_P[15..0]
PCIE_CRX_GTX_N[15..0]

PCIE_TX0P Y33 PCIE_CRX_C_GTX_P0 0.1U_0402 16V7K 2 1 C257 PX@ PCIE_CRX_GTX_P0
PCIE_TX0N Y32 PCIE_CRX_C_GTX_N0 0.1U_0402 16V7K 2 1 C258 PX@ PCIE_CRX_GTX_N0

PCIE_TX1P W33 PCIE_CRX_C_GTX_P1 0.1U_0402 16V7K 2 1 C264 PX@ PCIE_CRX_GTX_P1
PCIE_TX1N W32 PCIE_CRX_C_GTX_N1 0.1U_0402 16V7K 2 1 C259 PX@ PCIE_CRX_GTX_N1

PCIE_TX2P U33 PCIE_CRX_C_GTX_P2 0.1U_0402 16V7K 2 1 C260 PX@ PCIE_CRX_GTX_P2
PCIE_TX2N U32 PCIE_CRX_C_GTX_N2 0.1U_0402 16V7K 2 1 C261 PX@ PCIE_CRX_GTX_N2

PCIE_TX3P U30 PCIE_CRX_C_GTX_P3 0.1U_0402 16V7K 2 1 C262 PX@ PCIE_CRX_GTX_P3
PCIE_TX3N U29 PCIE_CRX_C_GTX_N3 0.1U_0402 16V7K 2 1 C263 PX@ PCIE_CRX_GTX_N3

PCIE_TX4P T33 PCIE_CRX_C_GTX_P4 0.1U_0402 16V7K 2 1 C265 PX@ PCIE_CRX_GTX_P4
PCIE_TX4N T32 PCIE_CRX_C_GTX_N4 0.1U_0402 16V7K 2 1 C266 PX@ PCIE_CRX_GTX_N4

PCIE_TX5P T30 PCIE_CRX_C_GTX_P5 0.1U_0402 16V7K 2 1 C267 PX@ PCIE_CRX_GTX_P5
PCIE_TX5N T29 PCIE_CRX_C_GTX_N5 0.1U_0402 16V7K 2 1 C268 PX@ PCIE_CRX_GTX_N5

PCIE_TX6P P33 PCIE_CRX_C_GTX_P6 0.1U_0402 16V7K 2 1 C269 PX@ PCIE_CRX_GTX_P6
PCIE_TX6N P32 PCIE_CRX_C_GTX_N6 0.1U_0402 16V7K 2 1 C270 PX@ PCIE_CRX_GTX_N6

PCIE_TX7P P30 PCIE_CRX_C_GTX_P7 0.1U_0402 16V7K 2 1 C271 PX@ PCIE_CRX_GTX_P7
PCIE_TX7N P29 PCIE_CRX_C_GTX_N7 0.1U_0402 16V7K 2 1 C272 PX@ PCIE_CRX_GTX_N7

PCIE_TX8P N33 PCIE_CRX_C_GTX_P8 0.1U_0402 16V7K 2 1 C273 PX@ PCIE_CRX_GTX_P8
PCIE_TX8N N32 PCIE_CRX_C_GTX_N8 0.1U_0402 16V7K 2 1 C274 PX@ PCIE_CRX_GTX_N8

PCIE_TX9P N30 PCIE_CRX_C_GTX_P9 0.1U_0402 16V7K 2 1 C275 PX@ PCIE_CRX_GTX_P9
PCIE_TX9N N29 PCIE_CRX_C_GTX_N9 0.1U_0402 16V7K 2 1 C276 PX@ PCIE_CRX_GTX_N9

PCIE_TX10P L33 PCIE_CRX_C_GTX_P10 0.1U_0402 16V7K 2 1 C277 PX@ PCIE_CRX_GTX_P10
PCIE_TX10N L32 PCIE_CRX_C_GTX_N10 0.1U_0402 16V7K 2 1 C278 PX@ PCIE_CRX_GTX_N10

PCIE_TX11P L30 PCIE_CRX_C_GTX_P11 0.1U_0402 16V7K 2 1 C279 PX@ PCIE_CRX_GTX_P11
PCIE_TX11N L29 PCIE_CRX_C_GTX_N11 0.1U_0402 16V7K 2 1 C280 PX@ PCIE_CRX_GTX_N11

PCIE_TX12P K33 PCIE_CRX_C_GTX_P12 0.1U_0402 16V7K 2 1 C281 PX@ PCIE_CRX_GTX_P12
PCIE_TX12N K32 PCIE_CRX_C_GTX_N12 0.1U_0402 16V7K 2 1 C282 PX@ PCIE_CRX_GTX_N12

PCIE_TX13P J33 PCIE_CRX_C_GTX_P13 0.1U_0402 16V7K 2 1 C283 PX@ PCIE_CRX_GTX_P13
PCIE_TX13N J32 PCIE_CRX_C_GTX_N13 0.1U_0402 16V7K 2 1 C284 PX@ PCIE_CRX_GTX_N13

PCIE_TX14P K30 PCIE_CRX_C_GTX_P14 0.1U_0402 16V7K 2 1 C285 PX@ PCIE_CRX_GTX_P14
PCIE_TX14N K29 PCIE_CRX_C_GTX_N14 0.1U_0402 16V7K 2 1 C286 PX@ PCIE_CRX_GTX_N14

PCIE_TX15P H33 PCIE_CRX_C_GTX_P15 0.1U_0402 16V7K 2 1 C287 PX@ PCIE_CRX_GTX_P15
PCIE_TX15N H32 PCIE_CRX_C_GTX_N15 0.1U_0402 16V7K 2 1 C288 PX@ PCIE_CRX_GTX_N15

13 CLK_PEG_VGA
13 CLK_PEG_VGA#

CLK_PEG_VGA AB35
CLK_PEG_VGA# AA36

CLOCK

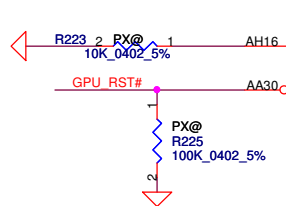
PCIE_REFCLKP
PCIE_REFCLKN

CALIBRATION

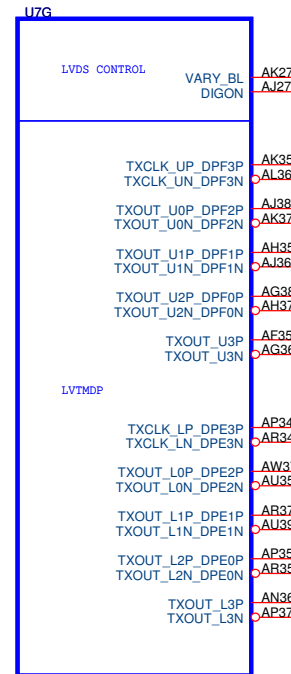
PCIE_CALRP
PCIE_CALRN

THAMES XT M2 FCBGA 962P

PX@

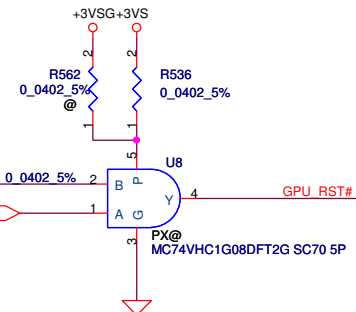


LVDS Interface



THAMES XT M2 FCBGA 962P

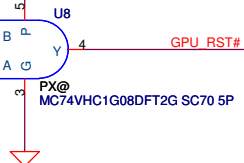
PX@



13,14 PE_GPIO0

R556 2 PX@ 1 0.0402 5% 2

13,30,33 PLT_RST#



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								Size B	Document Number						Rev 0.2
								QML70 LA-8371P							
								Date:		Wednesday, October 19, 2011		Sheet 18 of 53			

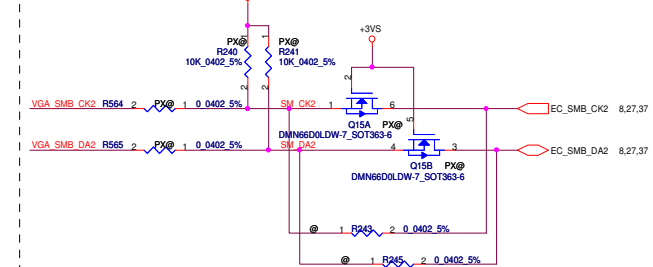
CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESETRECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 10K RESISTOR
X= DESIGN DEPENDANT
NA= NOT APPLICABLE

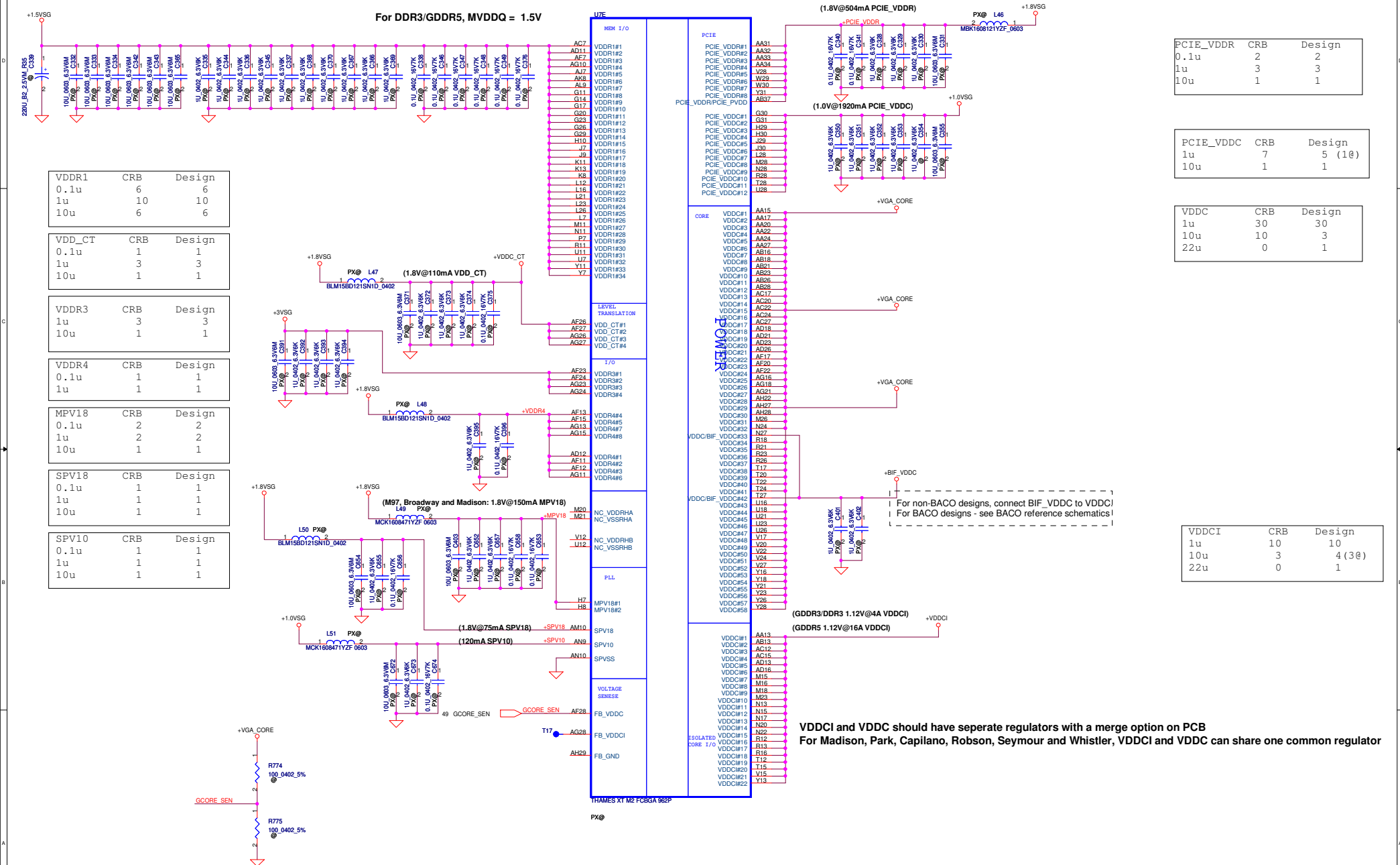
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIe speed when compliance test 0: 2.5Gt/s 1: 5Gt/s	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort only 1 0 Audio for DisplayPort and HDMI, if dongle is detected. 1 1 Audio for both DisplayPort and HDMI	11
AUD[0]	VSYN		

AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21 H2SYNC GENERICC GPIO2 GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)

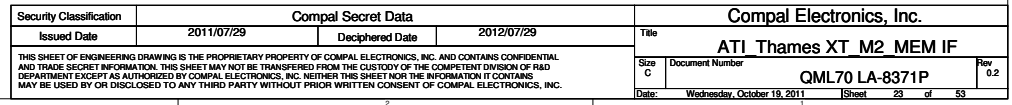
Internal VGA Thermal Sensor

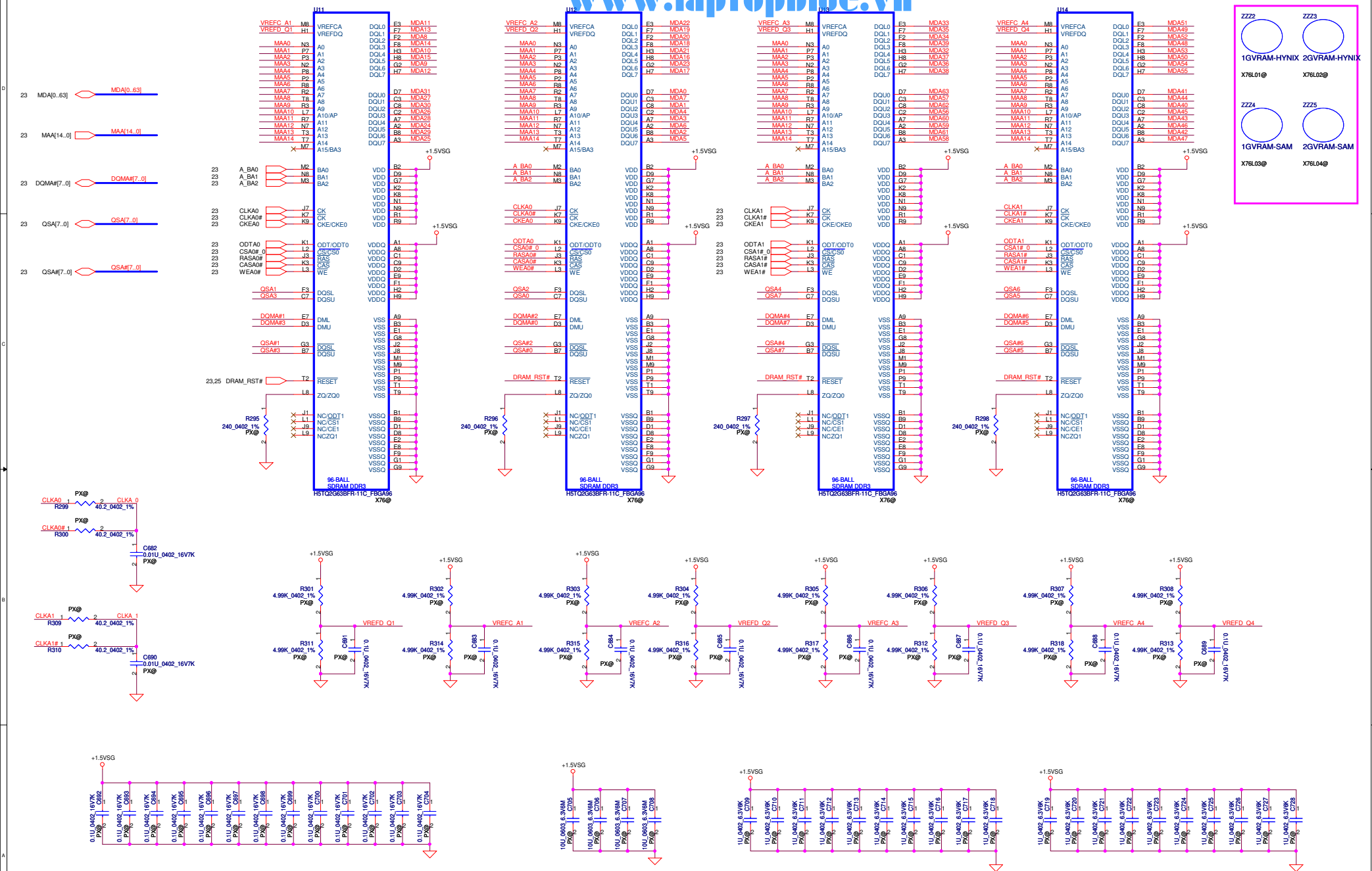


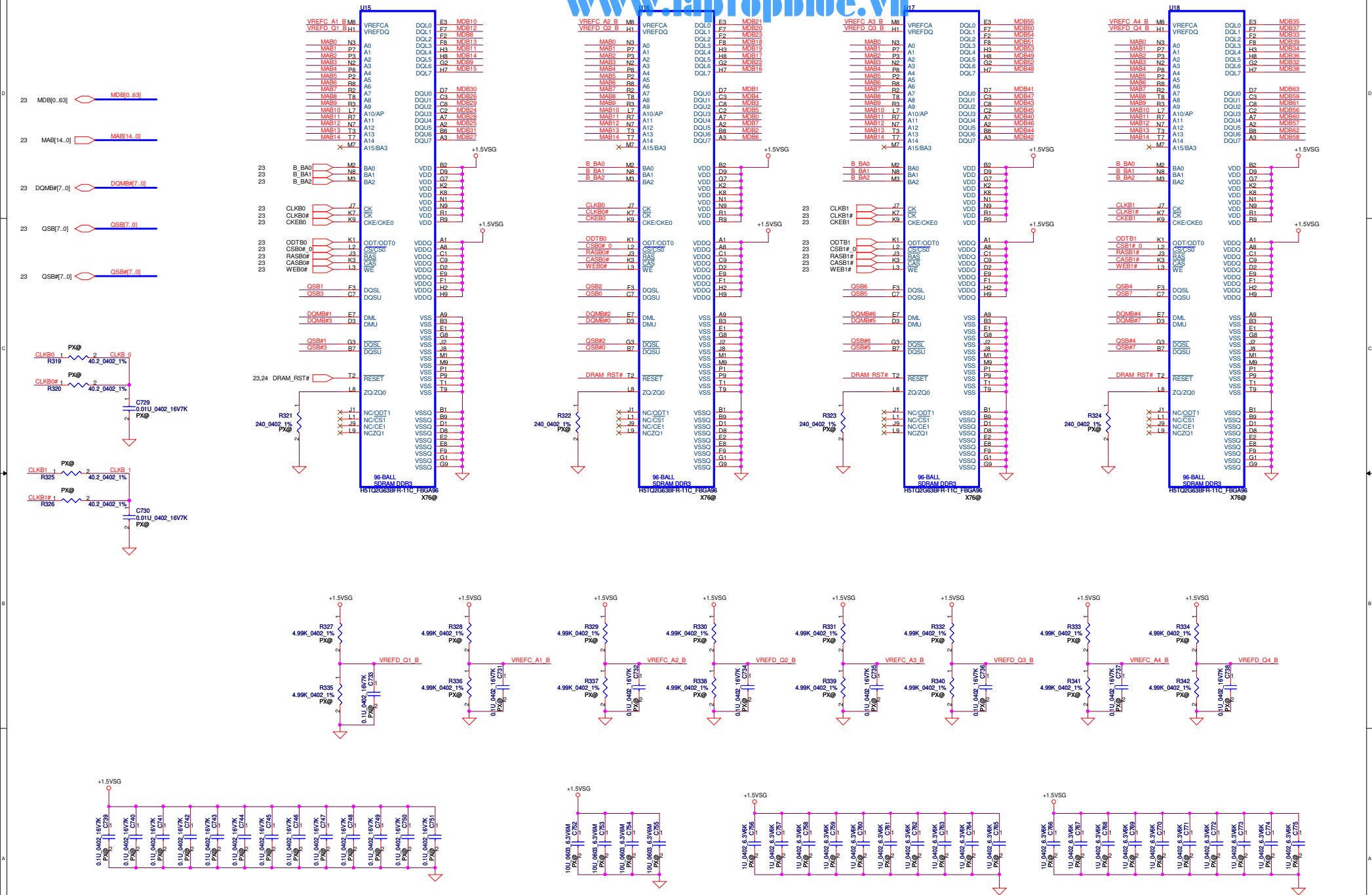
VDDC	CRB	Design
1u	30	30
10u	10	3
22u	0	1

VDDCI	CRB	Design
1u	10	10
10u	3	4 (3)
22u	0	1

VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

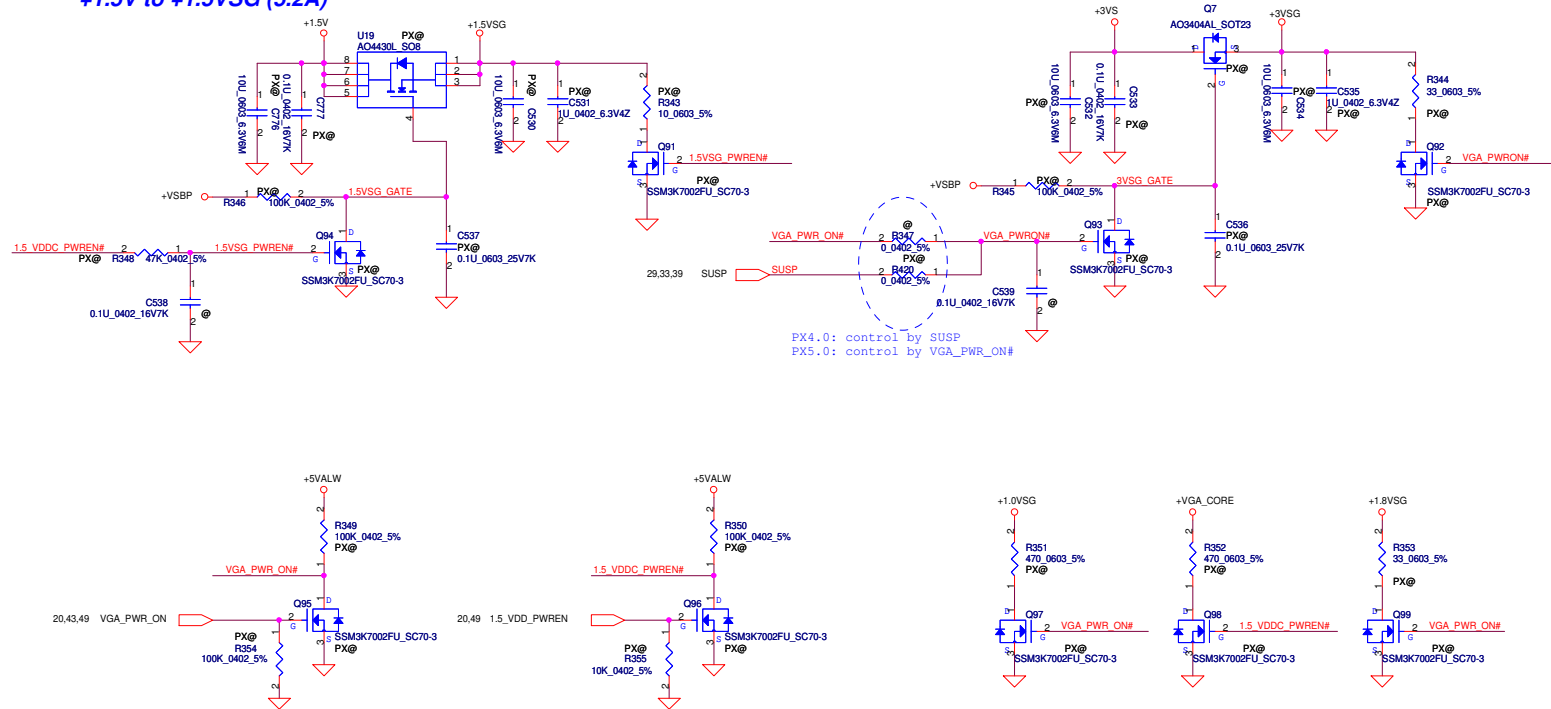




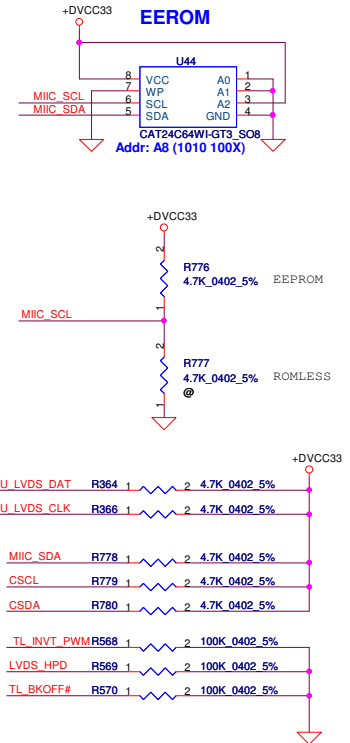


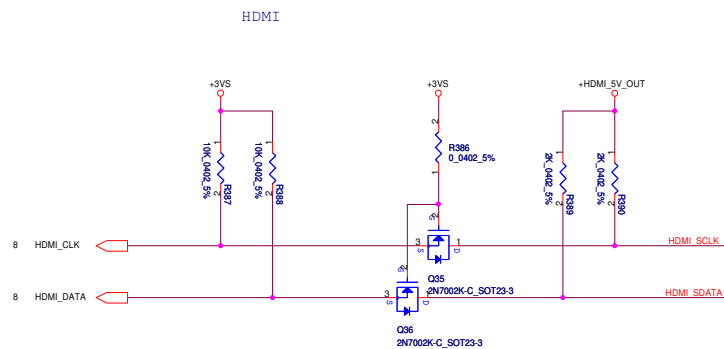
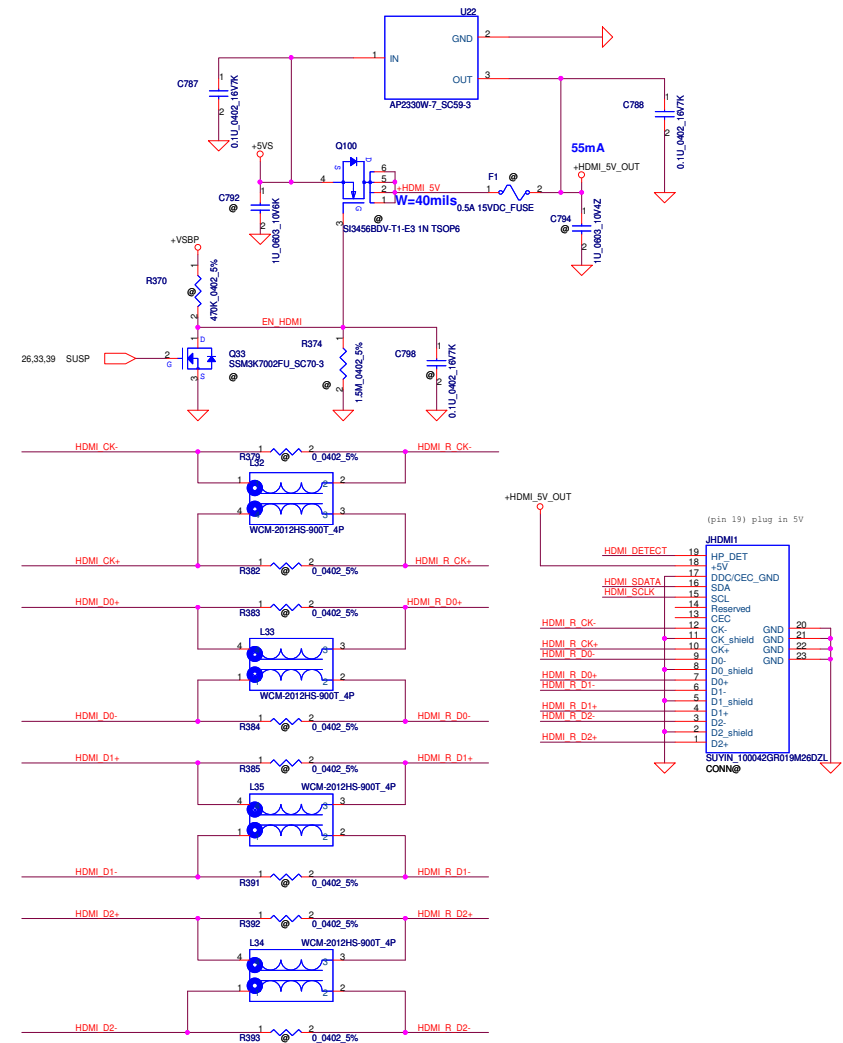
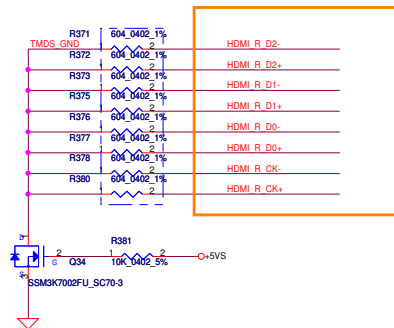
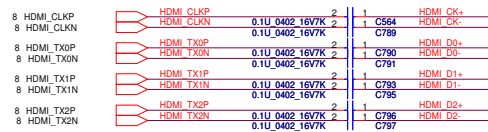
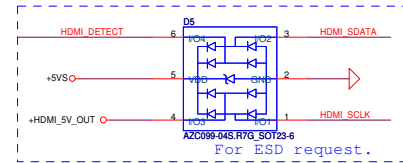
+1.5V to +1.5VSG (5.2A)

www.laptopblue.vn
+3VS to +3VSG (60mA)

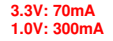
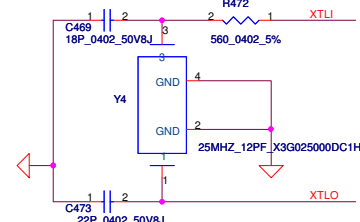
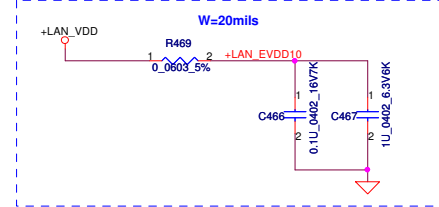
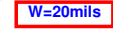


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				Custom	Document Number QML70 LA-8371P
				Date:	Wednesday, 09/11/2011 Sheet 26 of 53

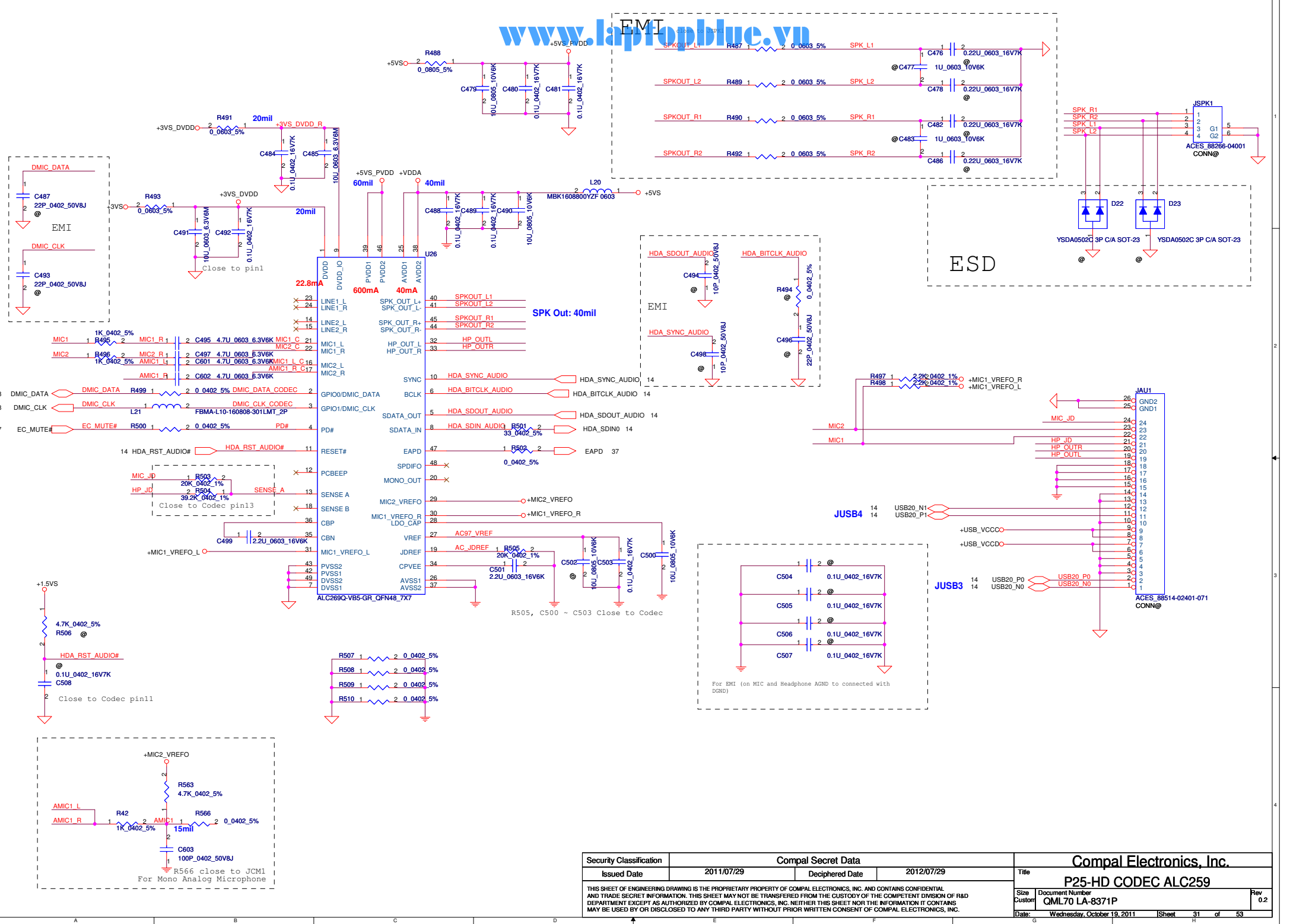




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				Date:	Wednesday, October 19, 2011
				Sheet	29 of 53

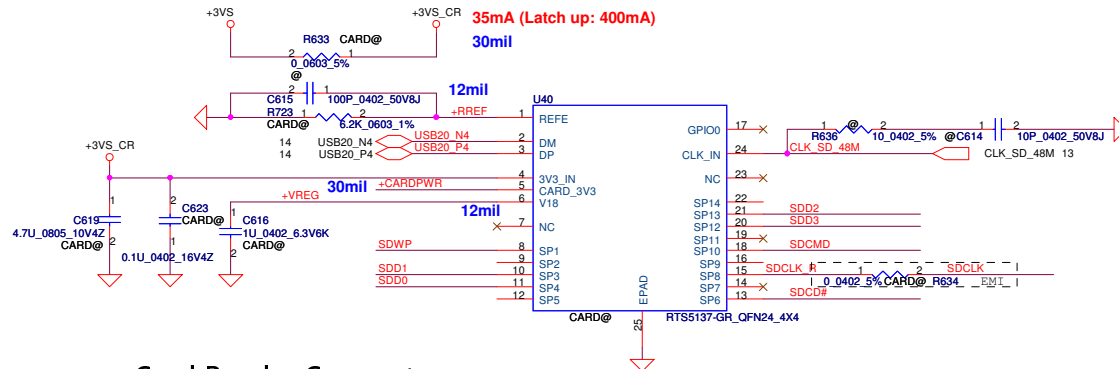


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				Date:	Wednesday, October 19, 2011	Sheet 30 of 53

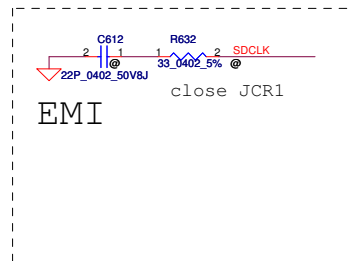
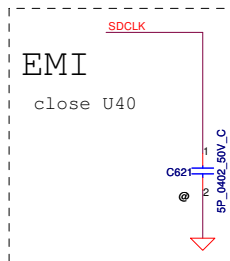
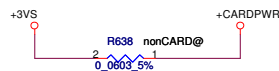
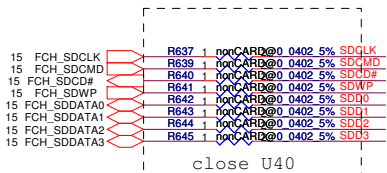
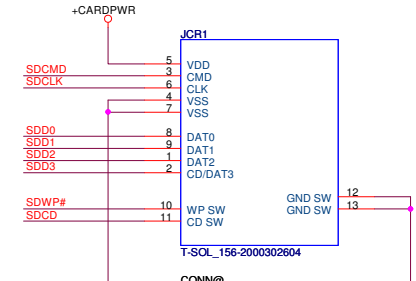
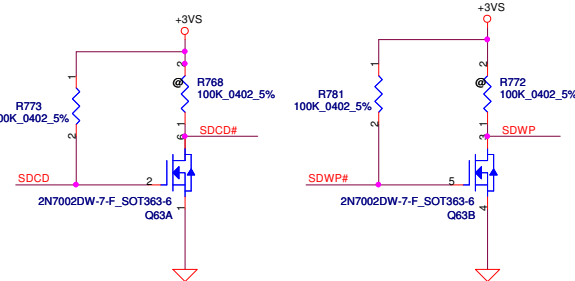
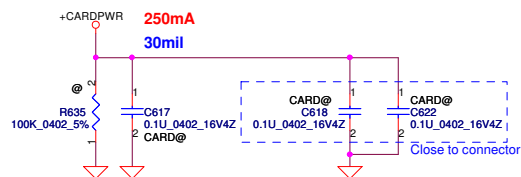


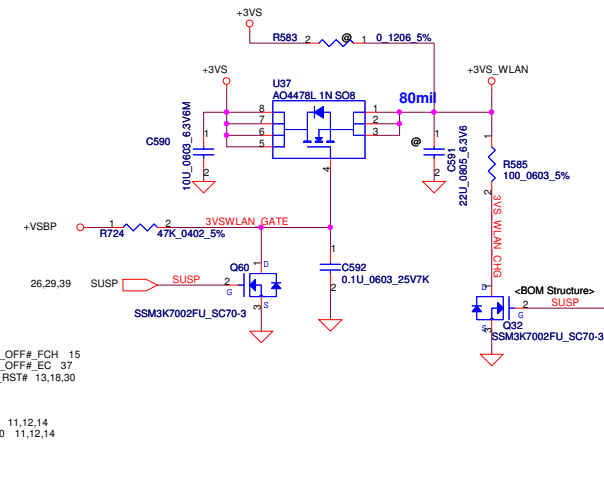
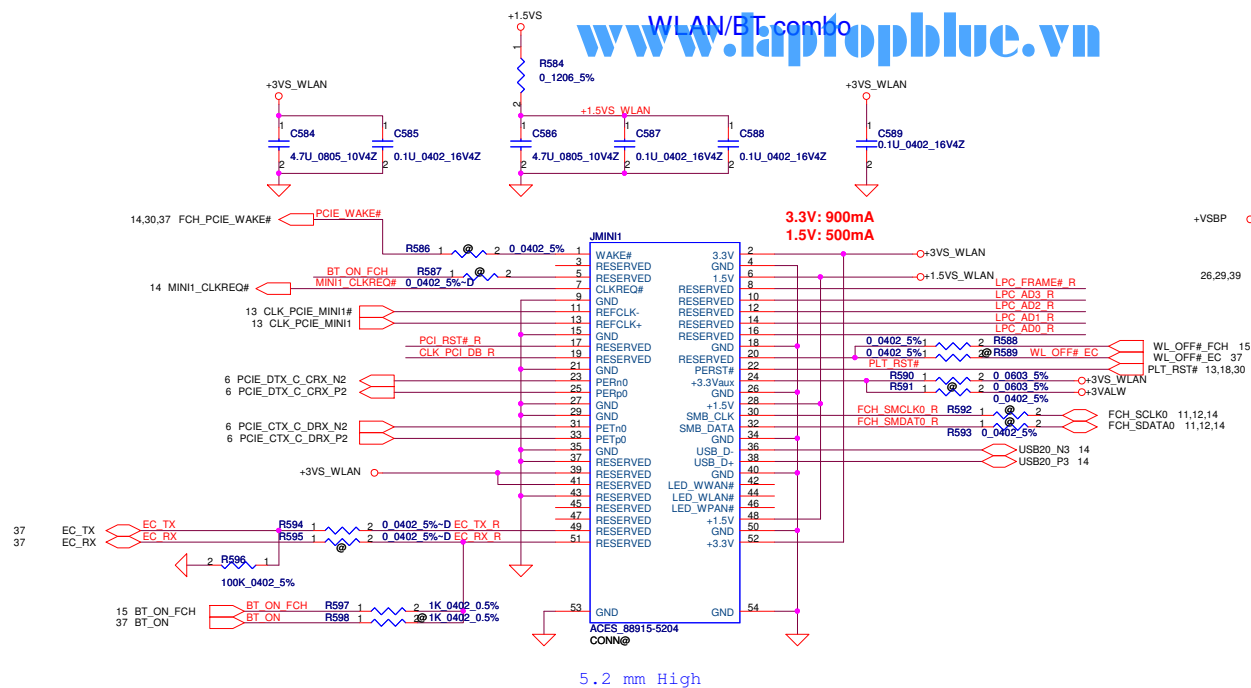
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Card Reader RTS5137 (only SD/MMC/MS function)

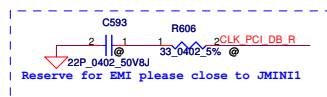
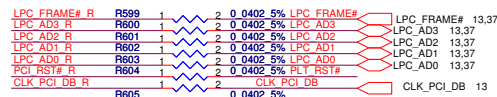


Card Reader Connector



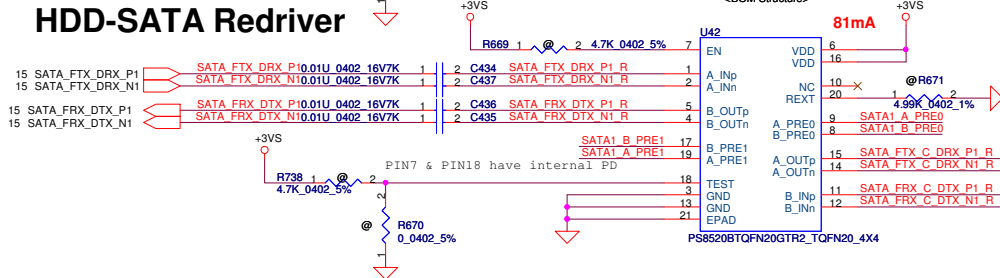
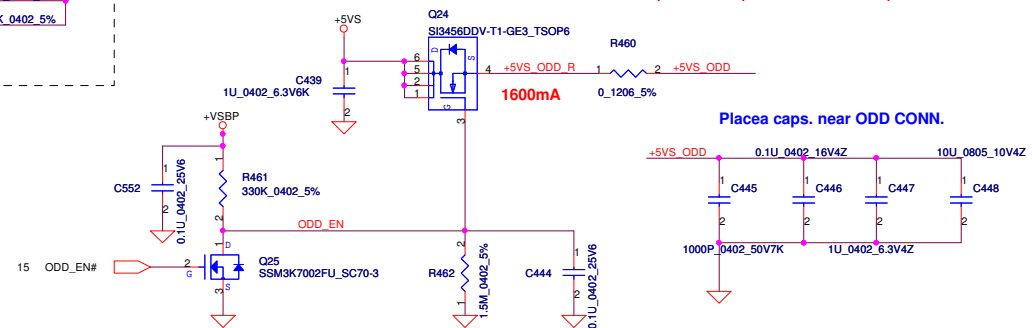
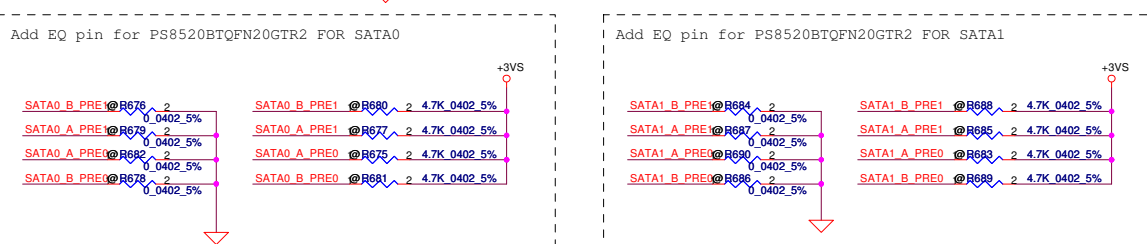
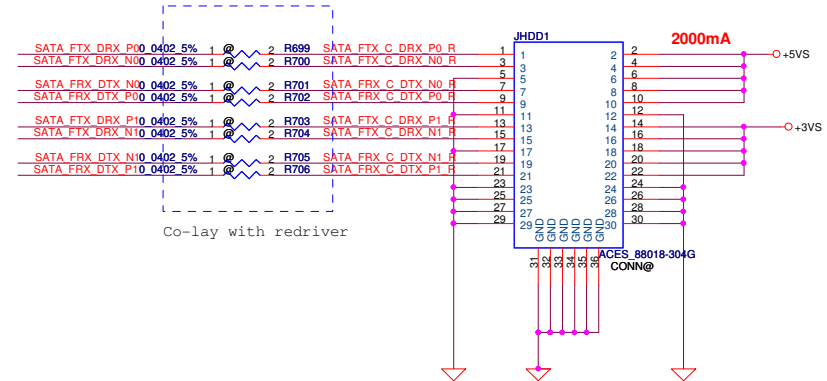


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

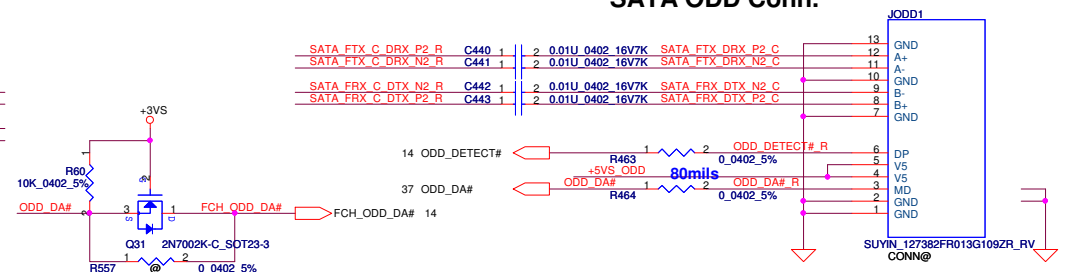
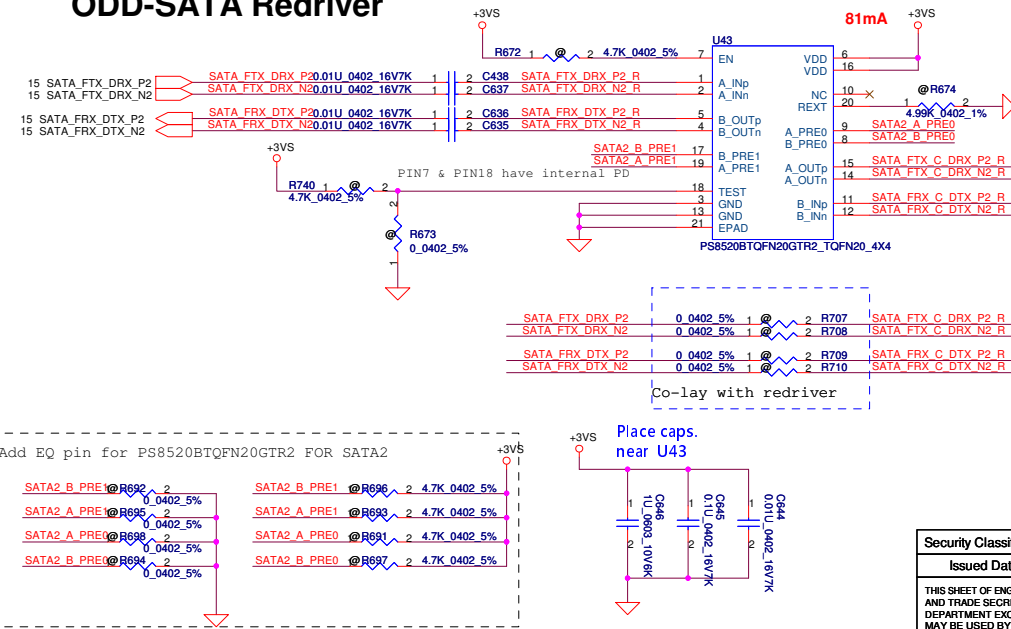


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				QML70 LA-8371P		0.2
				Date:	Wednesday, October 19, 2011	Sheet 33 of 53

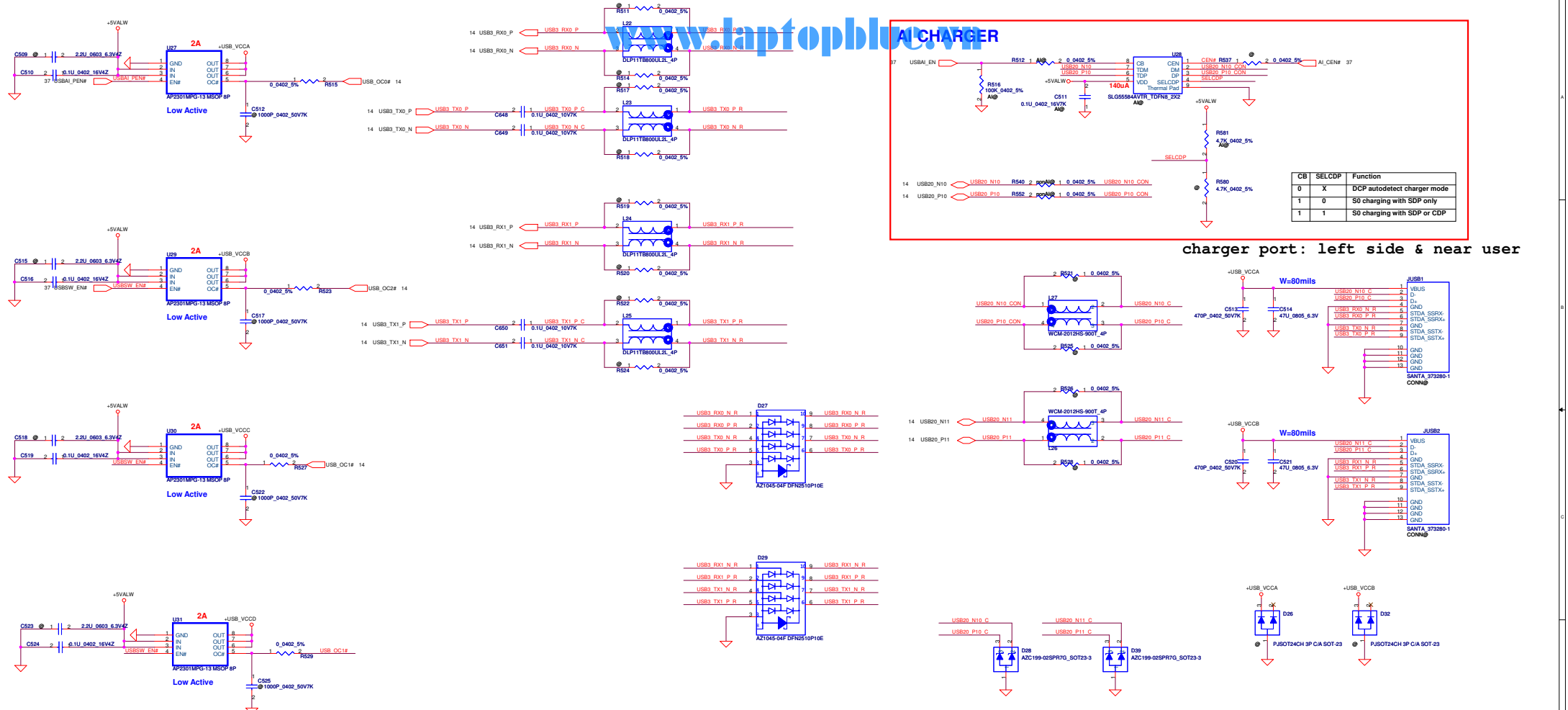
HDD-SATA Redriver

[illegible]

SATA ODD Conn.



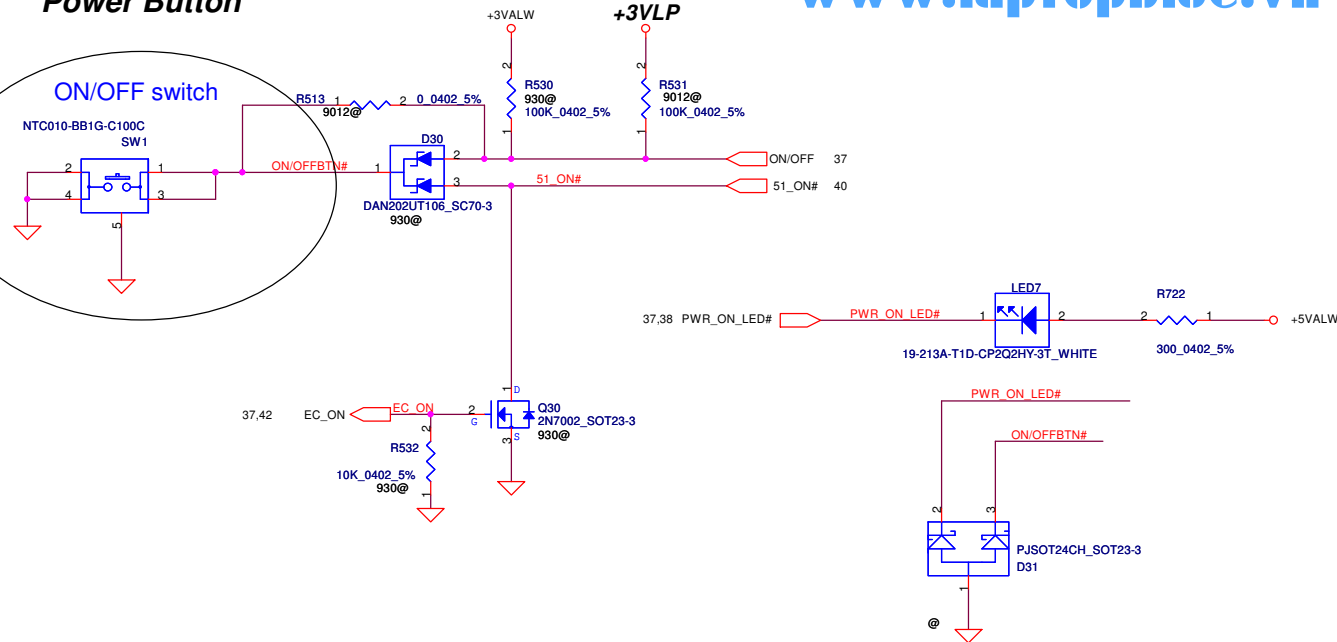
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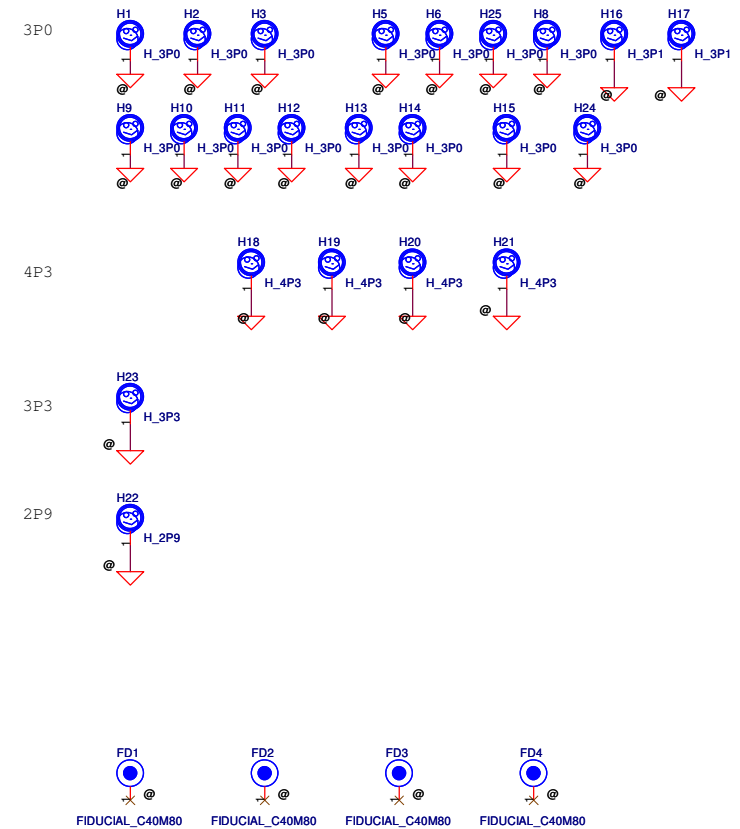
CB	SELCDP	Function
0	X	DCP autotdetect charger mode
1	0	S0 charging with SDP only
1	1	S0 charging with SDP or CDP

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				0.11

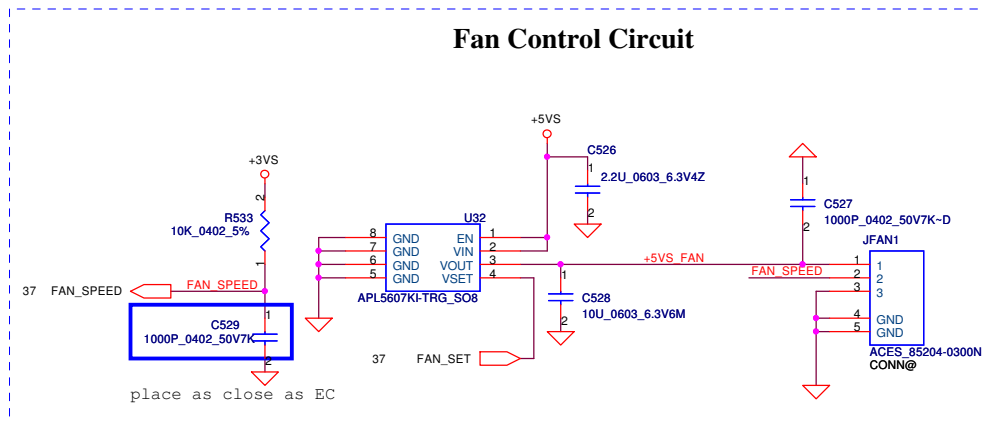
Power Button



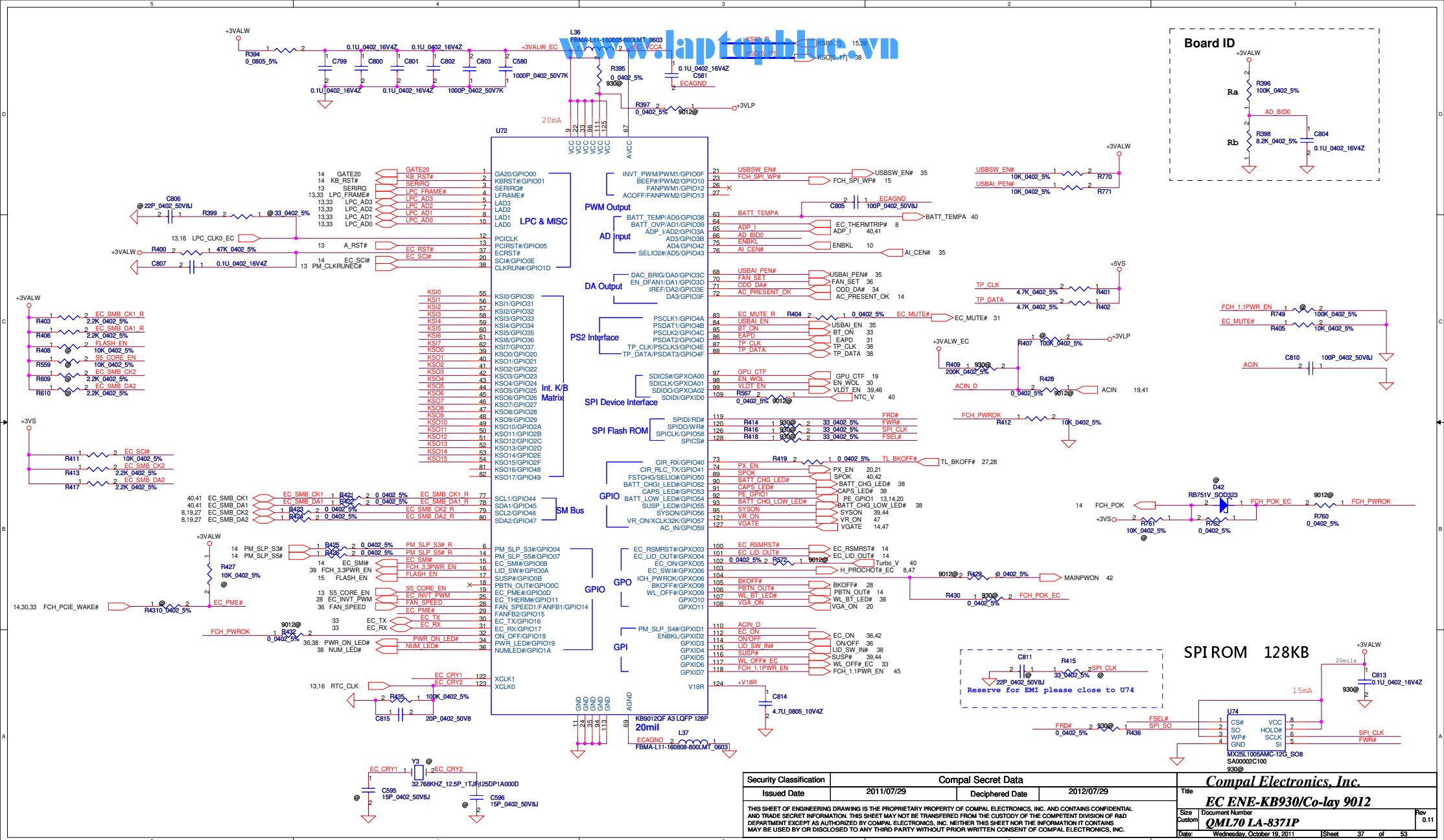
Screw Hole



Fan Control Circuit

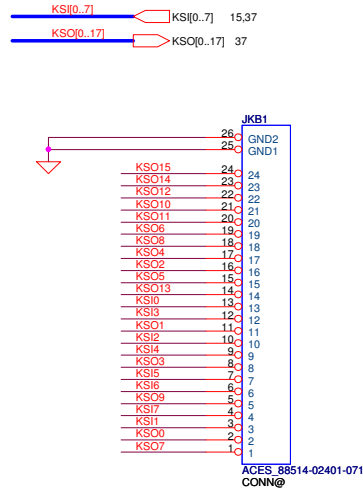


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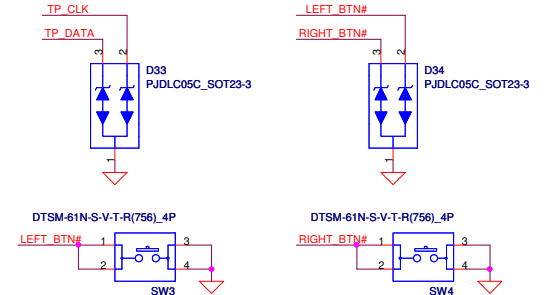
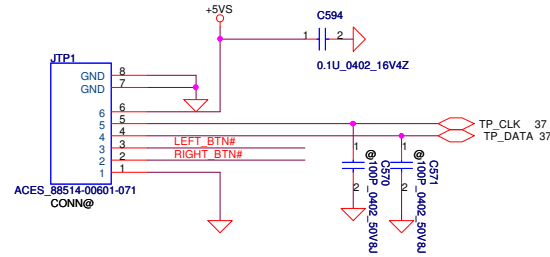


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				Date	Wednesday, October 19, 2011 Sheet 37 of 53

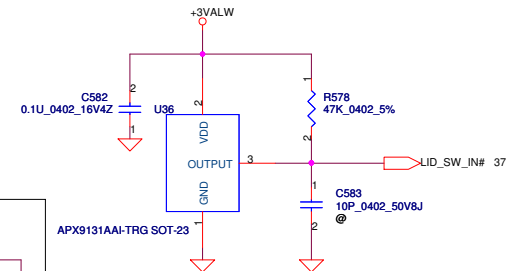
INT_KBD Conn.



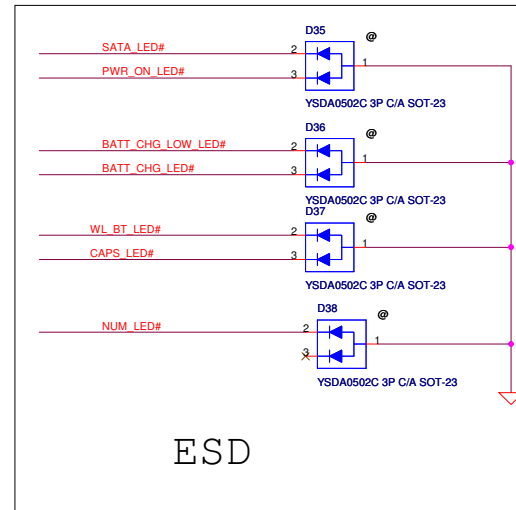
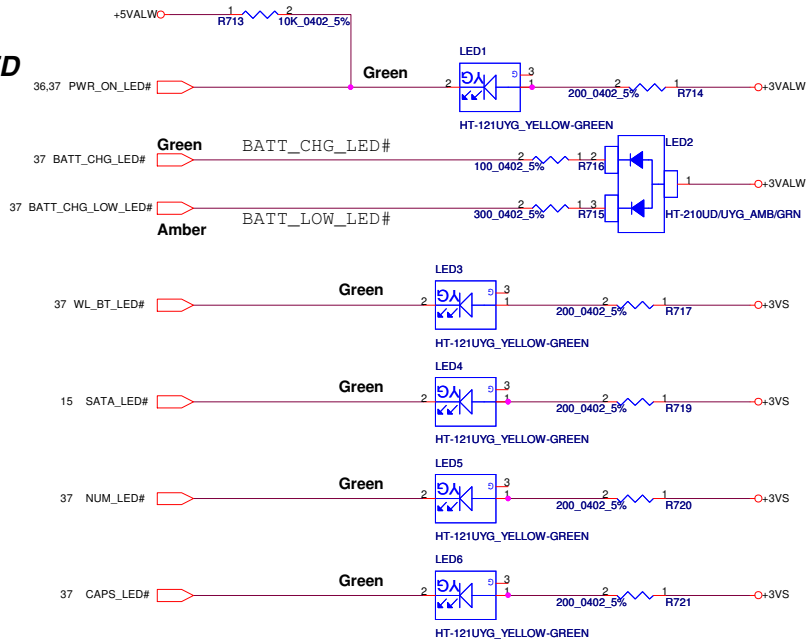
Touch/B Connector



Lid Switch (Hall Effect Switch)



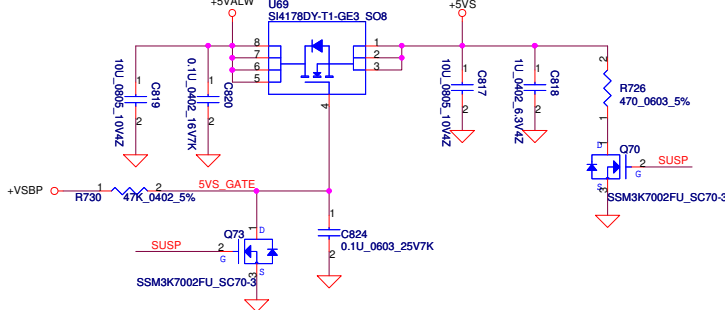
LED



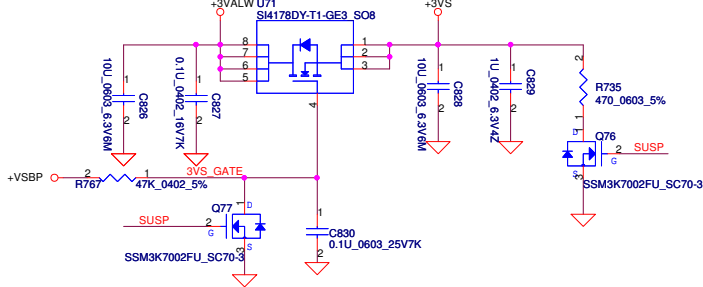
ESD

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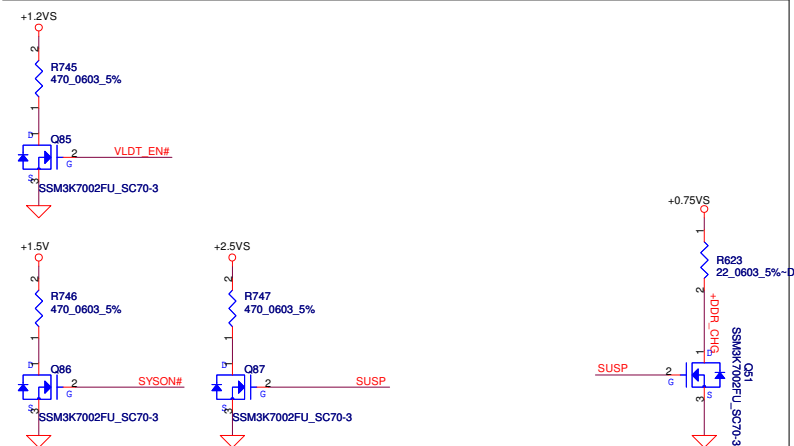
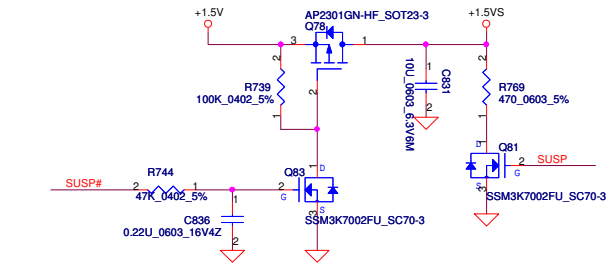
+5VALW TO +5VS (5.35A)



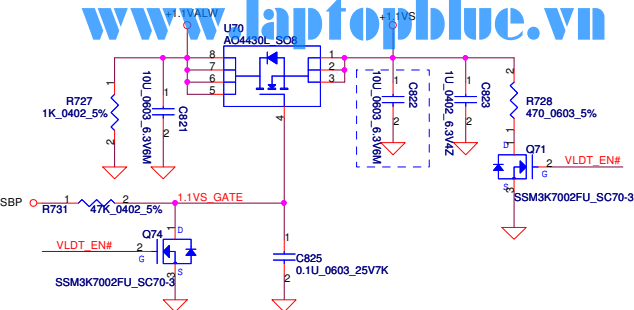
+3VALW TO +3VS (3A)



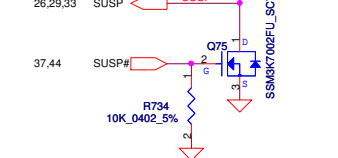
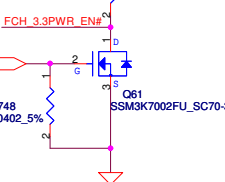
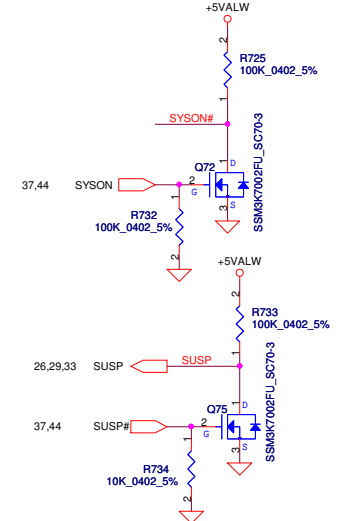
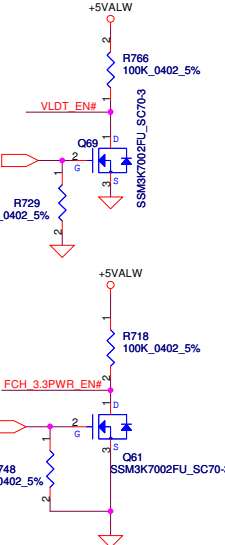
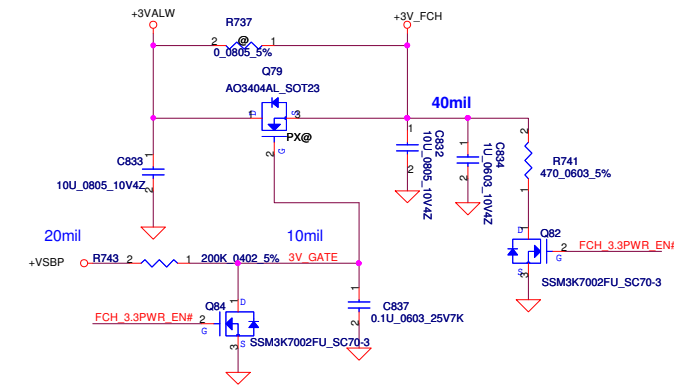
+1.5V TO +1.5VS (0.5A)



+1.1VALW TO +1.1VS (4A)



Instant On +3VALW TO +3V_FCH (1A)

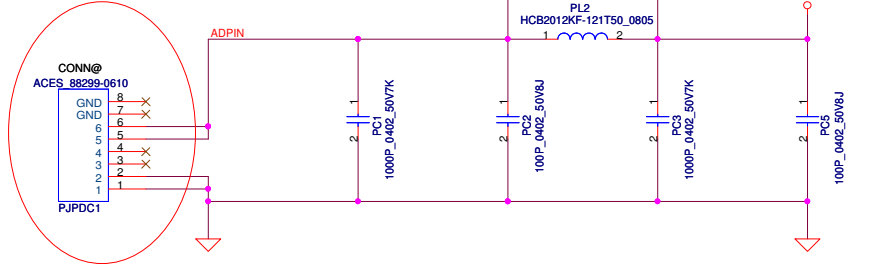


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Deciphered Date				2012/07/29				DC Interface			
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								Sheet 39 of 53			
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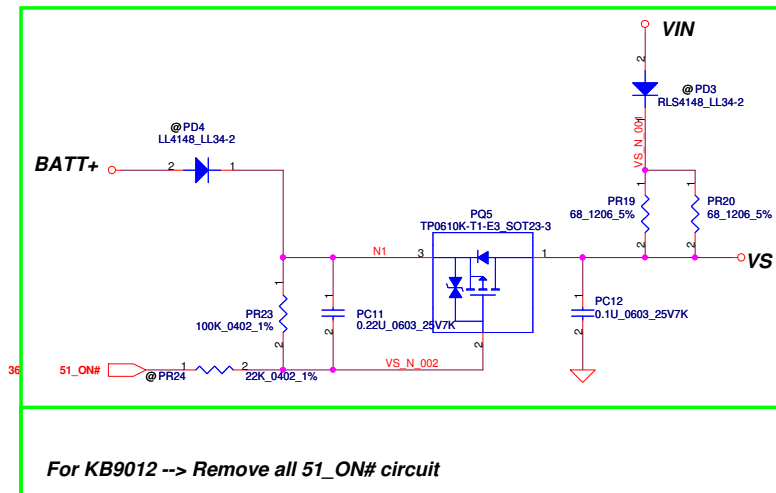
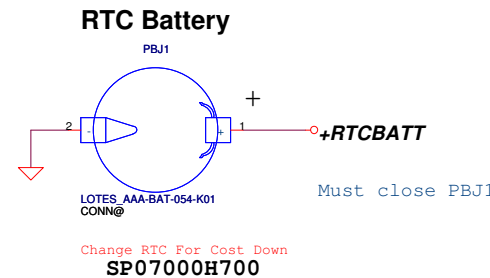
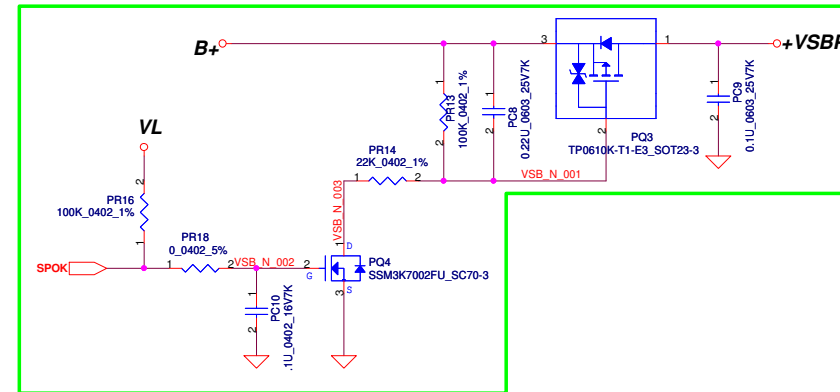
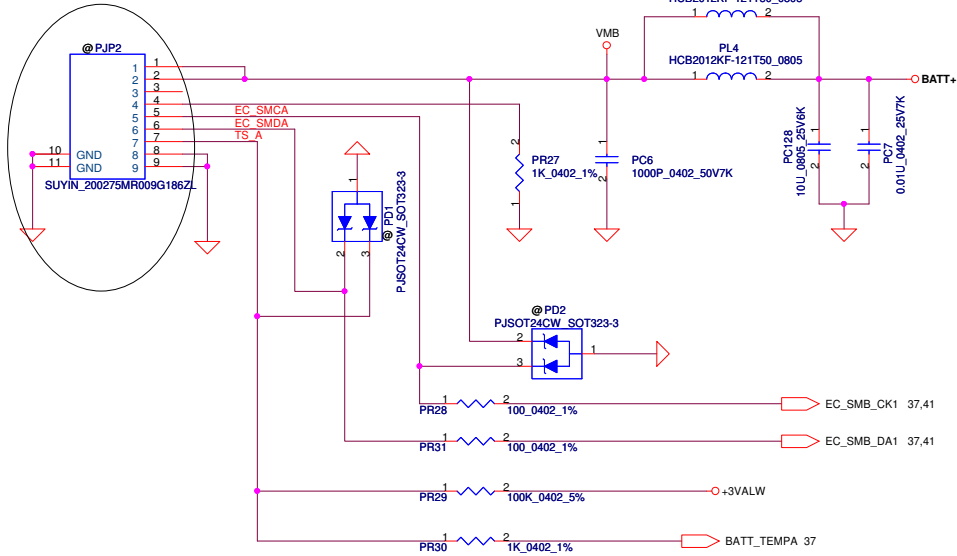
DCIN jack P/N:SP02000N000,
need doble confirm P/N with ME

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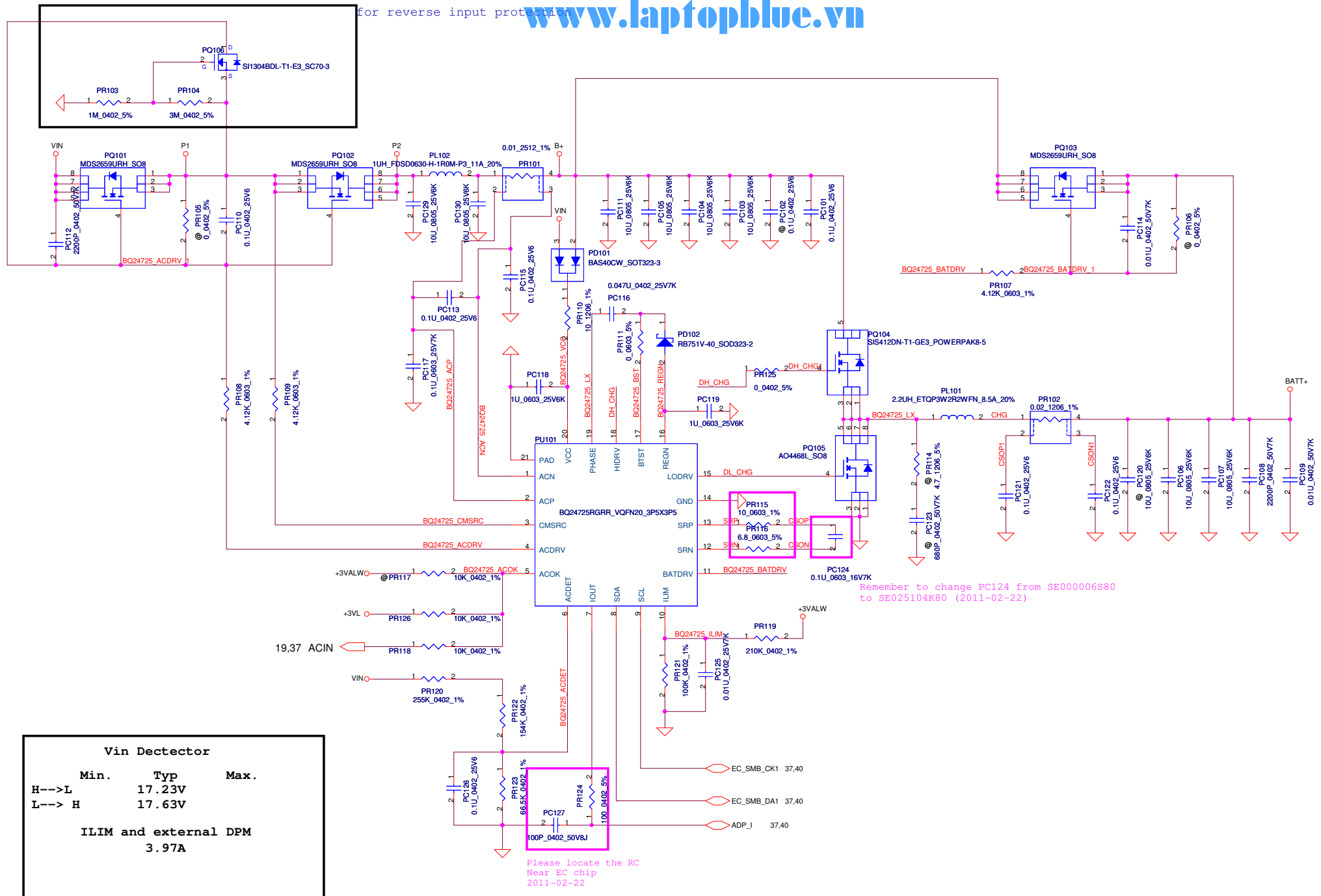
PH901 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C

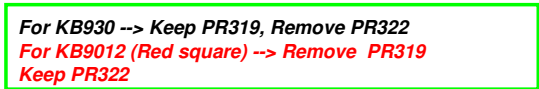


Change DC040007T01 to DC040004L00
(Use DC040001V00 symbol)



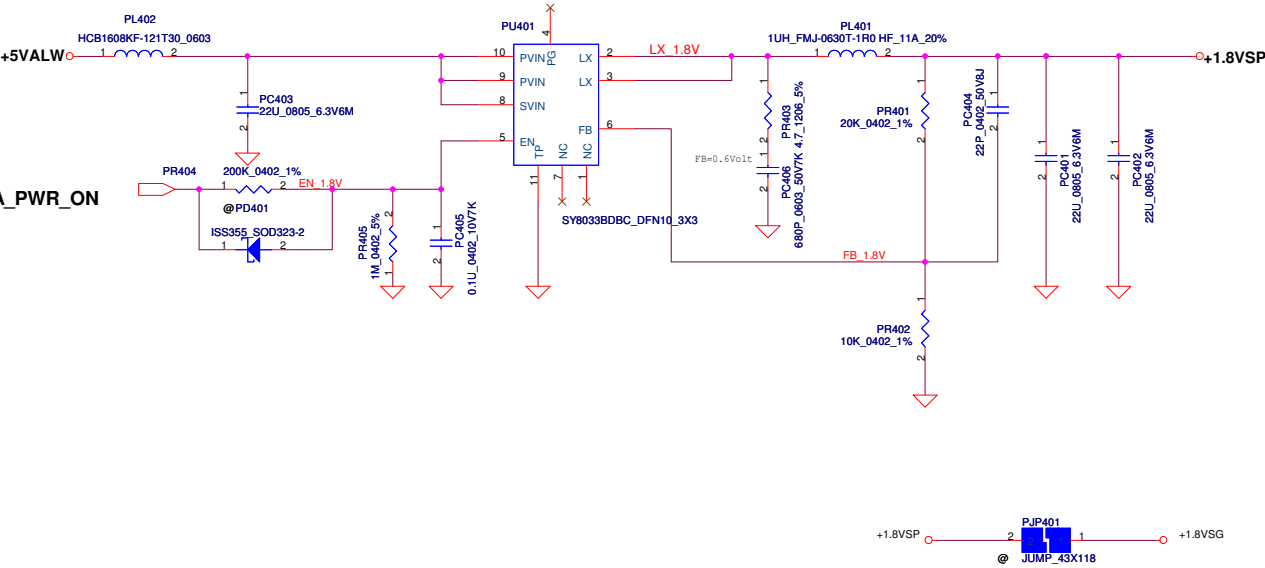
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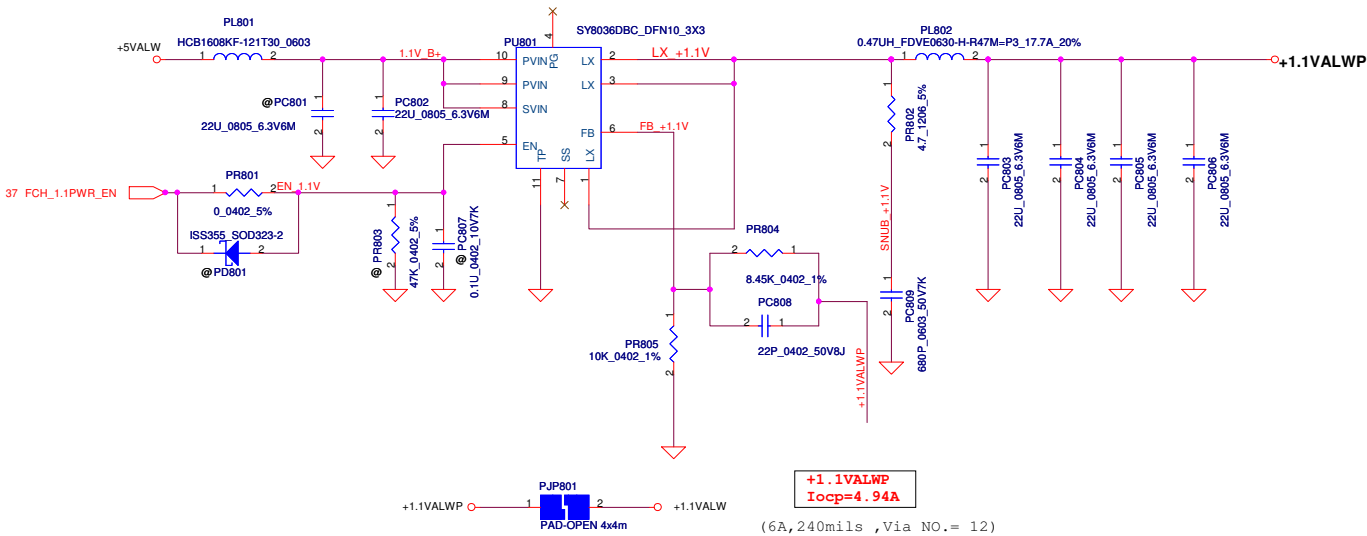


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20,26,49 VGA_PWR_ON



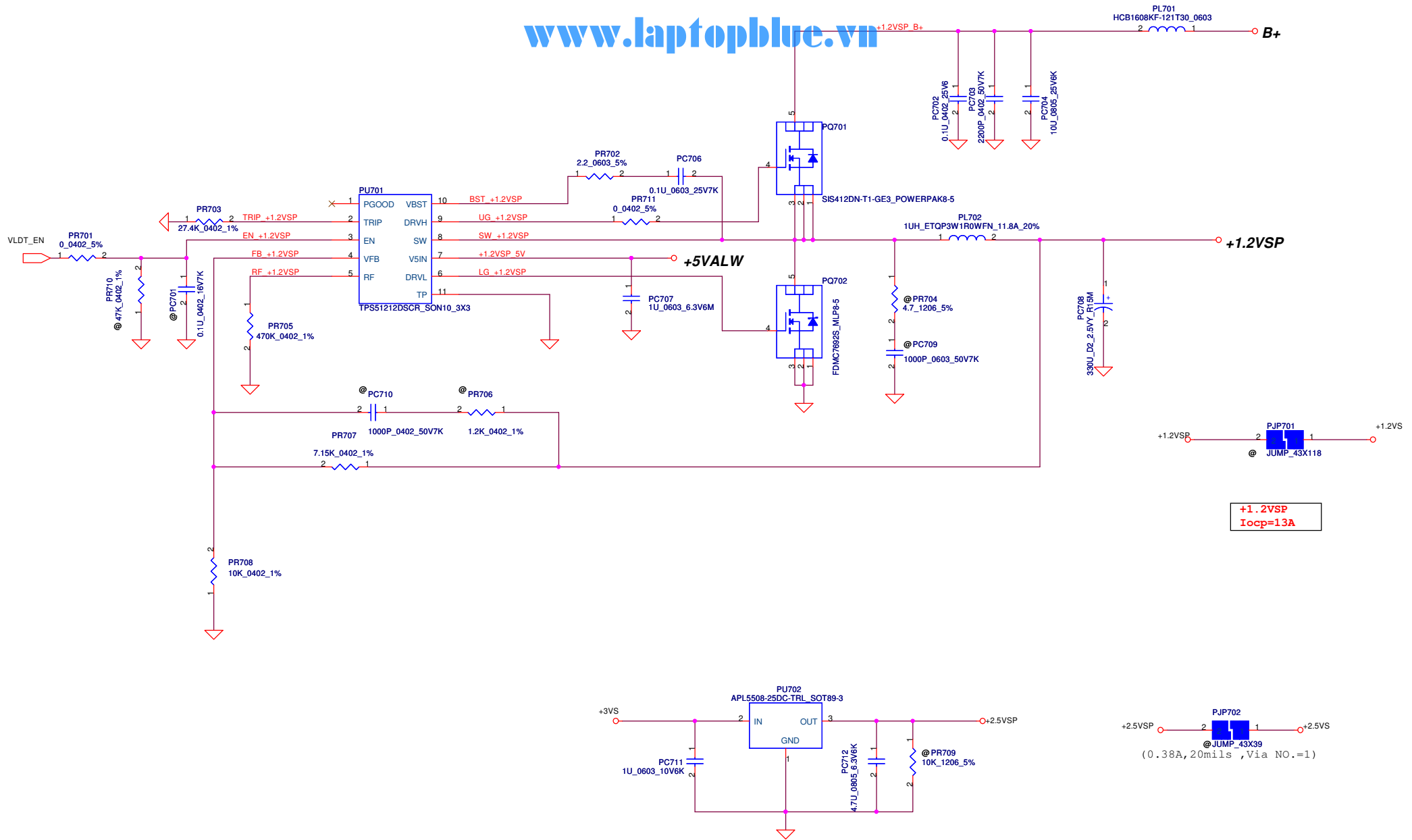
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Issued Date	2011/07/29	Deciphered Date		+1.8VP	
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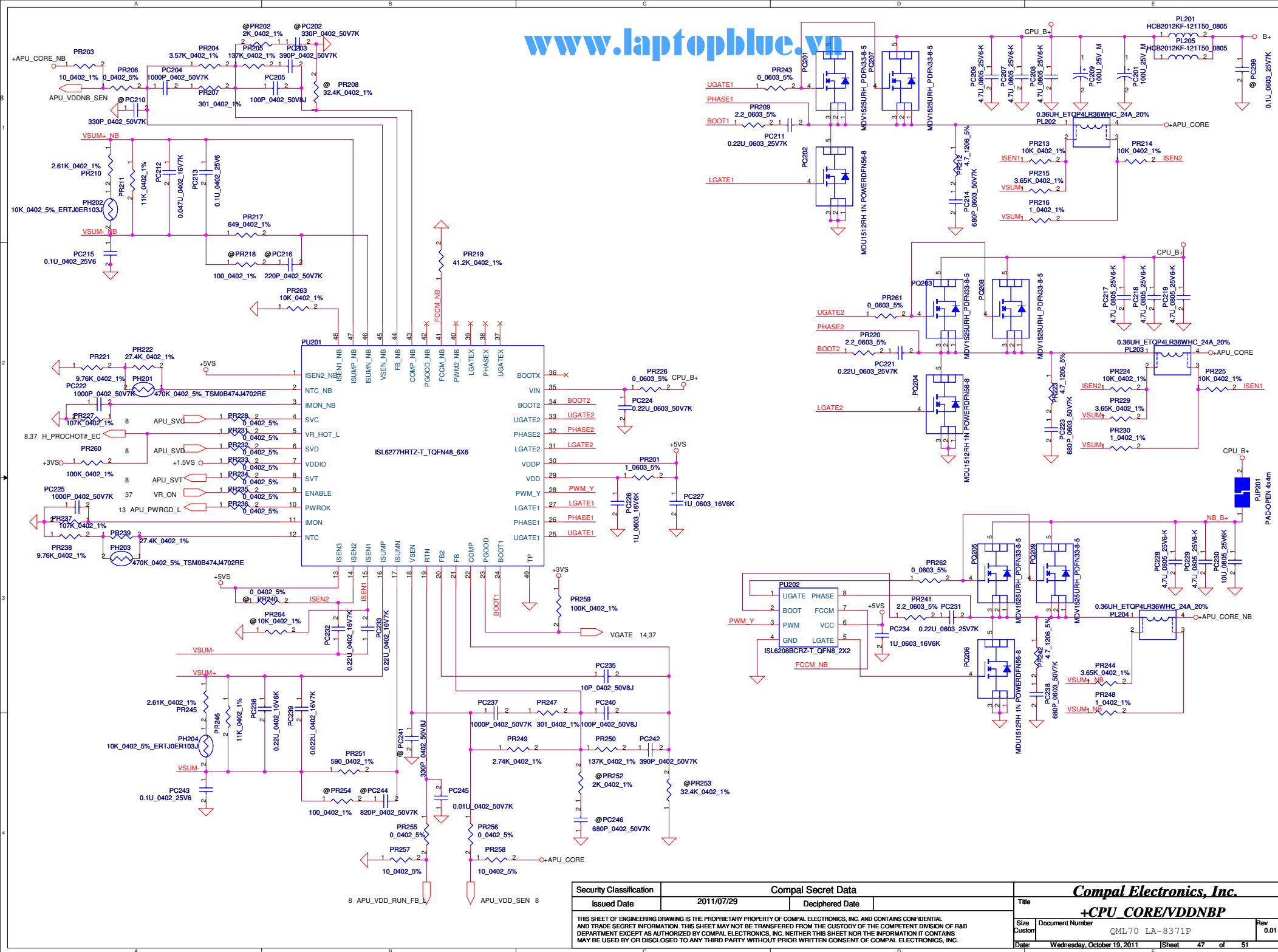
+1.1VALWP
Iocp=4.94A

(6A, 240mils, Via NO.= 12)

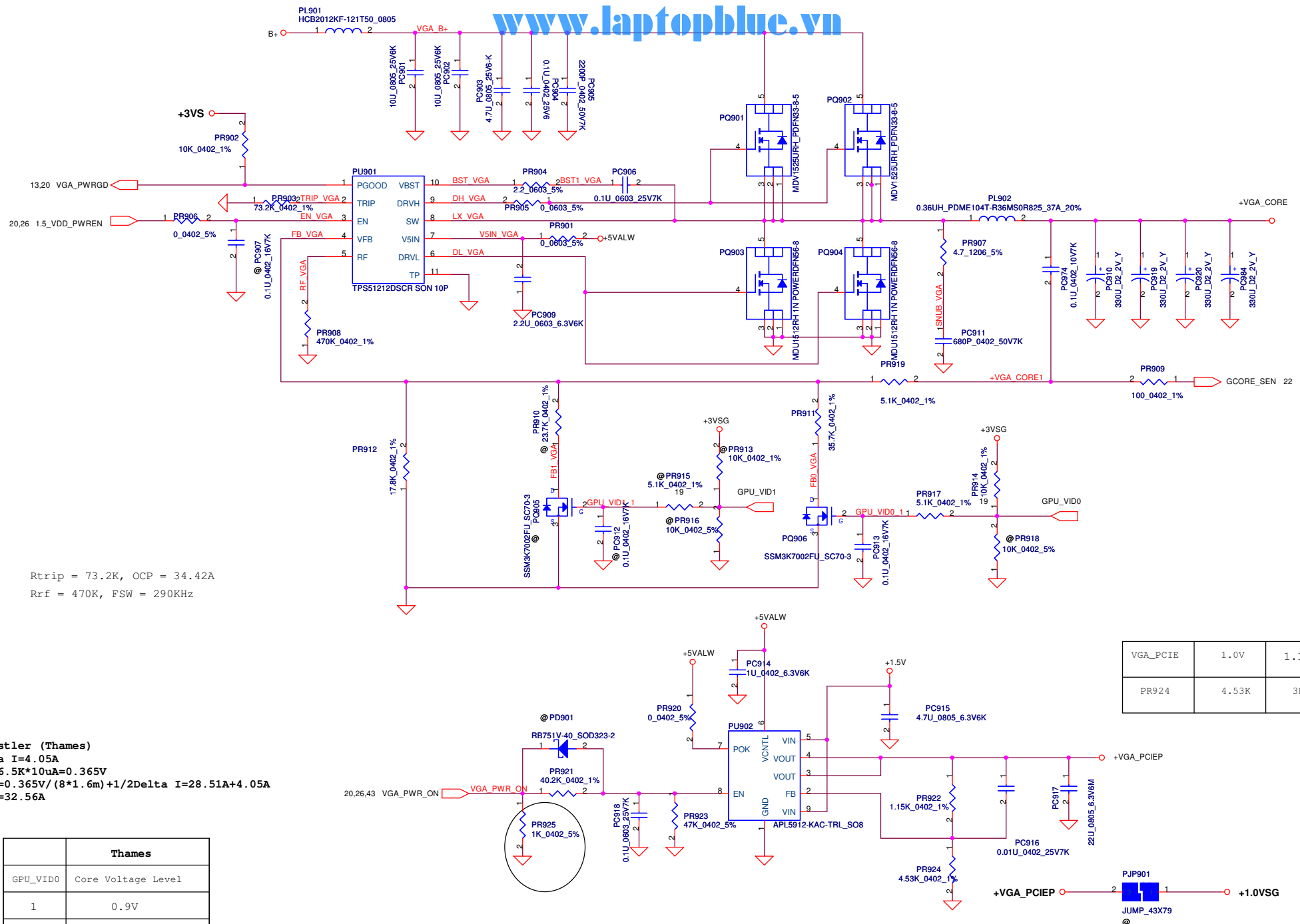
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Base on GPU Reference schematic	0.02	22	Reserve pull-up / pull-down resistor 100ohm on GCORE_SEN	08/30	SR
2			0.02	15	Modify Netname of SPI signal of U5	08/30	SR
3			0.02	26	Change Q91.2 from 1.5_VDDC_PWREN# to 1.5VSG_PWREN#	08/30	SR
4		These components are for VGA	0.02	26	Change BOM Structure of R349, R350, R354, R355, Q95, Q96 to PX0	08/30	SR
5		Base on AMD Comal CRB	0.02	8	Change pull-up voltage of APU_RST#, APU_PWRGD, APU_SVT, APU_SVC, APU_SVD, ALERT_L, ALLOW_STOP from +1.5V to +1.5VS	08/30	SR
6		For EMI request	0.02	15	Reserve R559, R561, C624, C625 @ FCH_SDCLK / FCH_SDWP	08/30	SR
7			0.02	36	Remove USB3.0 Host contorller circuit	09/01	SR
8			0.02	17	Remove componets of HUDSON_M2	09/01	SR
9		Set PCIE FULL TX OUTPUT SWING to High (Full Swing)	0.02	19	Modify GPU Straps: GPU_GPIO0 pull-high	09/01	SR
10			0.02	23	Reserve pull-high and pull-down resistor of MAA14/MBB14	09/01	SR
11		Base on Thames M2 datasheet	0.02	21	Modify U7.U13, U7.14 to NC	09/01	SR
12			0.02	19	Add THM_ALERT# to from U7.AG30 (GPU_THERMAL INT) to U34.6 (ADM1032) Add GPU_CTF from U7.AM17 (GPU_CTF) to U72.97 (EC)	09/02	SR
13			0.02	31	Reserve Analog microphone circuit	09/02	SR
14			0.02	9, 39, 45	Change contorl singal of 1.1VALWP from SPOK to FCH_1.1PWR_EN Change +1.1V_FCH to +1.1VALW	09/02	SR
15			0.02	15, 37	Connect U72.92 (EC) to U2.V1 (FCH)for SYS ROM Write Protect	09/02	SR
16			0.02	35	Co-lay AI Charger	09/02	SR
17			0.03	31	Modify Analog Microhpone circut base on Vendor suggestion	09/05	SR
18			0.03	22	Add decoupling cap. base on GPU check list	09/06	SR
19			0.03	17	Change decoupling cap. base on FCH check list	09/06	SR
20			0.03	27	Change LVDS translator to RTD2136	09/06	SR
21			0.03	28	Add pull-up resistor R129, R132 (2.2K) of FCH_CRT_DDC_SDA / SCL	09/06	SR
22			0.03	13	Change R99 to 22ohm (CLK_SD_48M)	09/07	SR
23			0.03	14	Pull-down PEG_CLKREQ#	09/08	SR
24			0.03	37	Change Board ID, R398: 0ohm	09/08	SR
25			0.03	34	Change Power source of ODD from +5VS to +5VALW	09/09	SR
26			0.03	33	Change Power source of WLAN from +3VALW to +3VS	09/09	SR
27			0.03	32	Add power source for none Card Reader IC solution	09/09	SR

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Blue Screen after install VGA Driver		0.2	15	Change U5 power from +3V_PCH to +3V_FCH	10/11	SR2
2			0.2	15	Change GBE_MDIO pull-up voltage from +3VALW to +3V_FCH	10/11	SR2
3			0.2	25	SWAP QSB7 and QSB#7	10/11	SR2
4			0.2	32	Delete Net SDCD, SDWP# that connect to EC Add MOSFET inverter of SDWP#	10/11	SR2
5			0.2	8	Un-mount pull-high resistor of APU_SVT, APU_SVC, APU_SVD	10/11	SR2
6			0.2	28	Follow QCL70 pin define	10/11	SR2
7			0.2	38	Modify Touch Pad pin define	10/11	SR2
8		For voltage leakage	0.2	8	Change pull-high voltage of APU_PROCHOT#, APU_THERMTRIP#, APU_SVT, APU_SVC, APU_SVD, ALERT_L, ALLOW_STOP, APU_RST#, APU_PWRGD, APU_SIC, APU_SID	10/11	SR2
9		Base on AMD recommend	0.2	24, 25	Change R299, R300, R309, R310, R319, R320, R325, R326 from 56ohm to 40.2ohm	10/11	SR2
10			0.2	37	Change Board ID to "1" for SR2	10/13	SR2
11			0.2	22	Seperate VDDC and VDDCI of VGA	10/14	SR2
12			0.2	23	Reserve R611, R612 for MAA14, MAB14	10/14	SR2
13							
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				Document Number	
				QML70 LA-8371P	
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