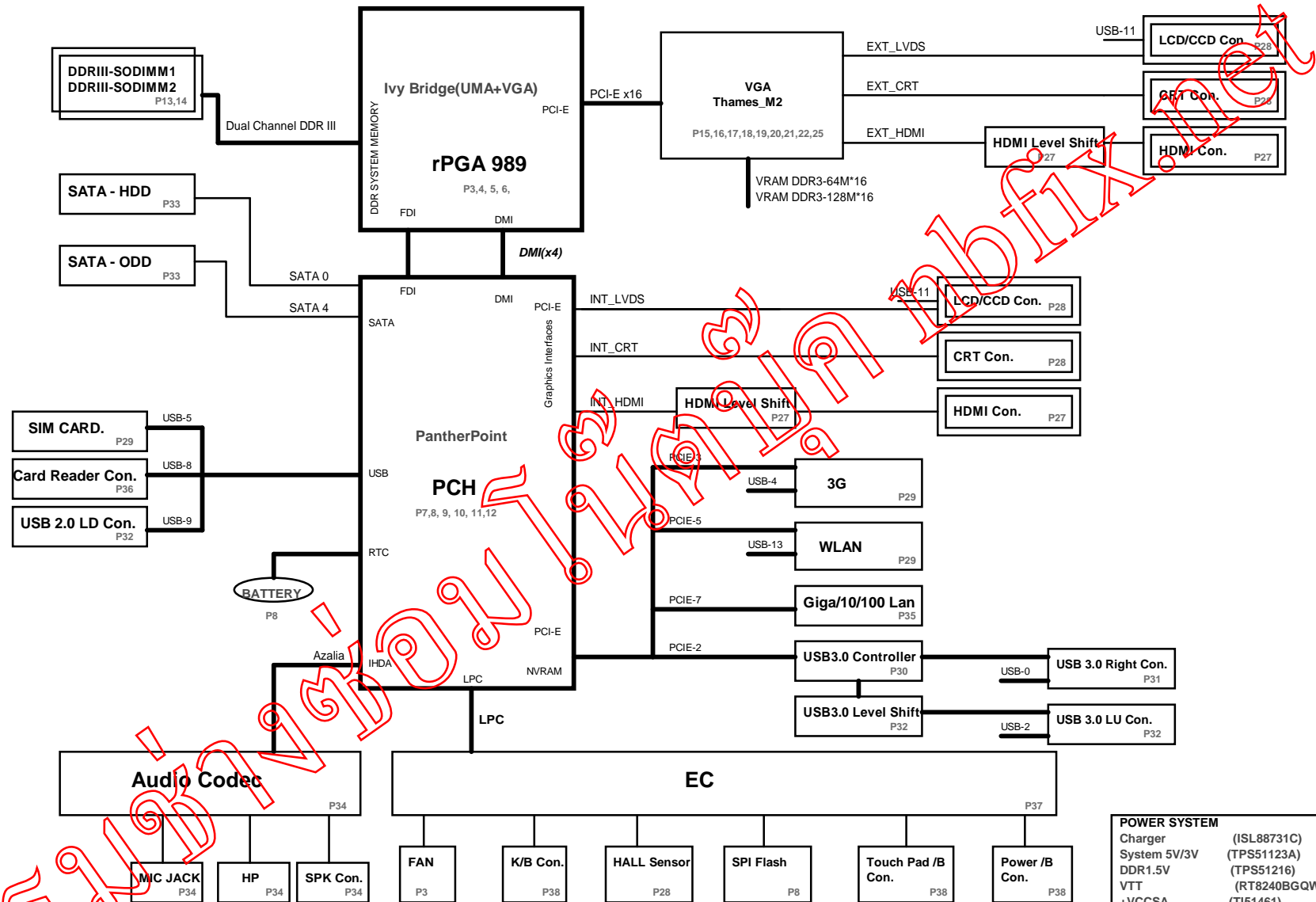
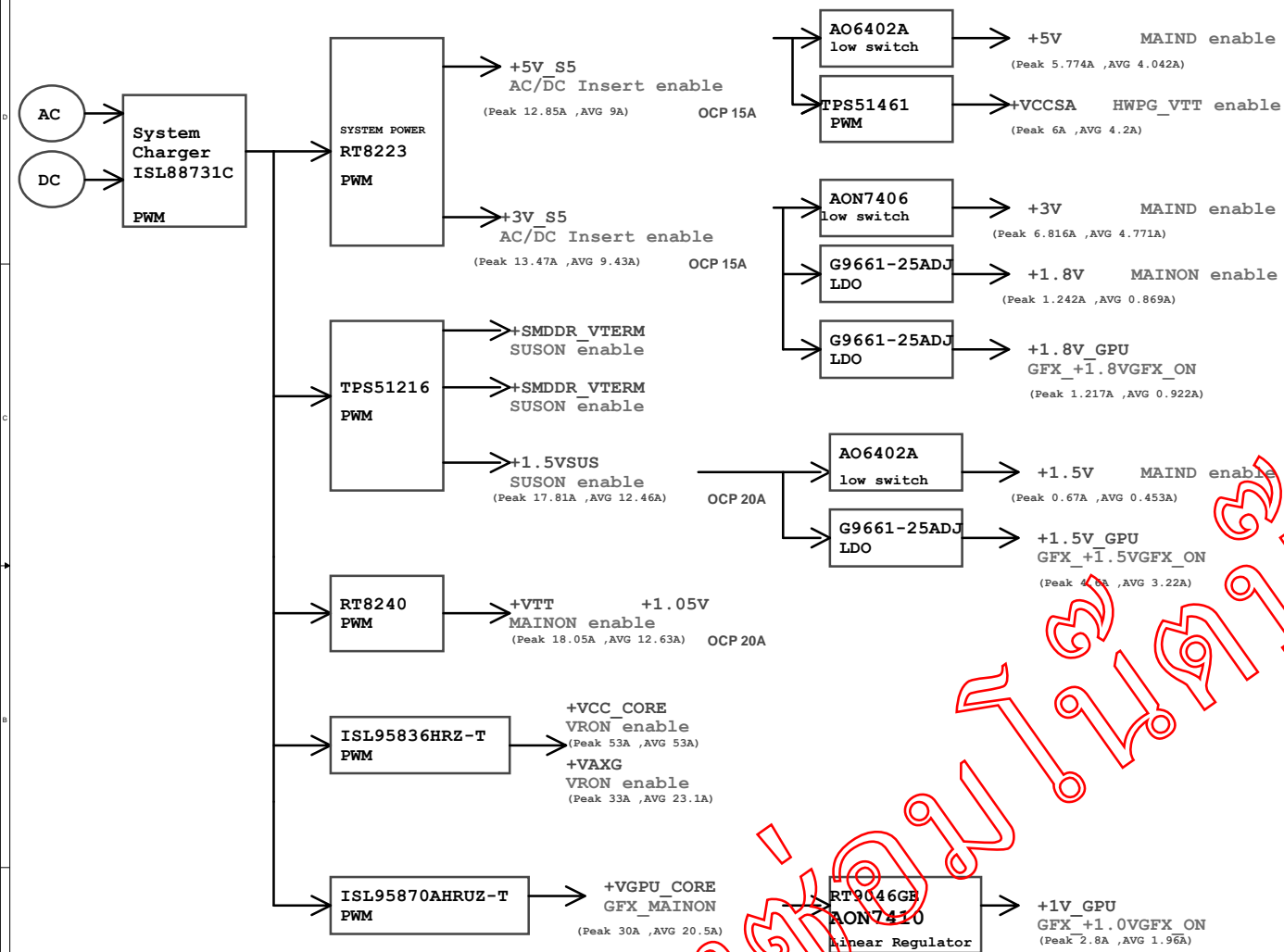


Chief River Block Diagram

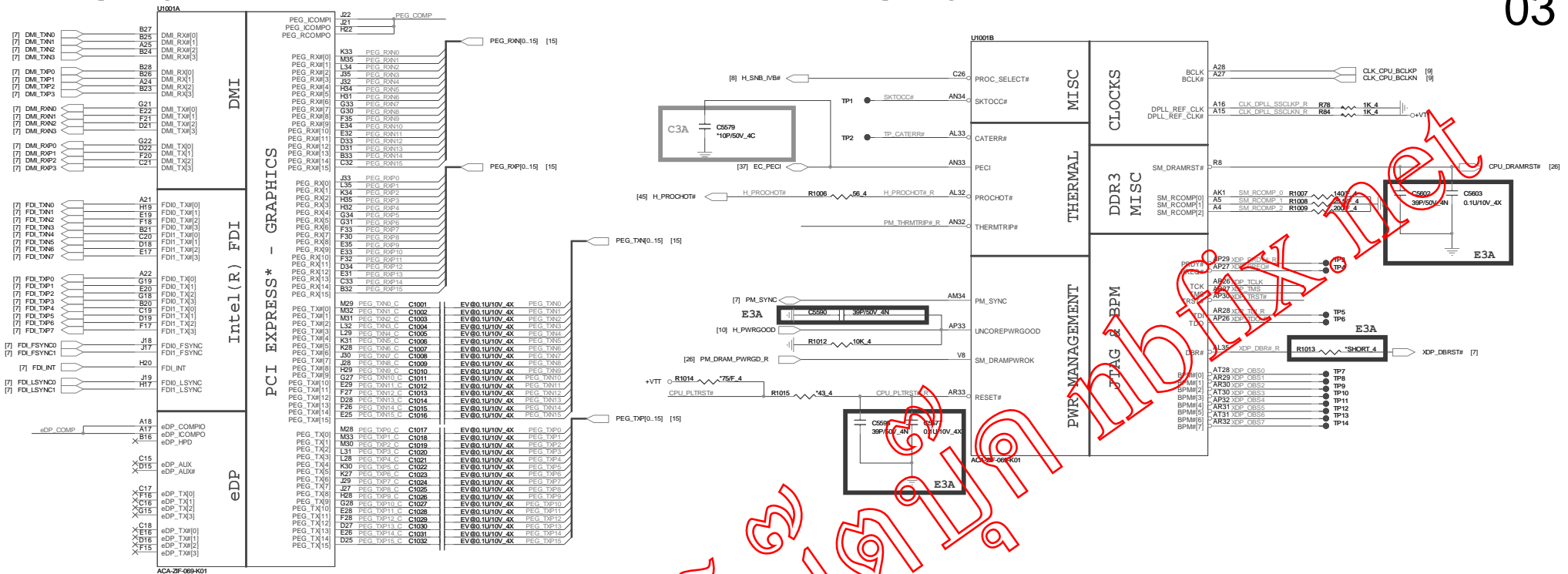
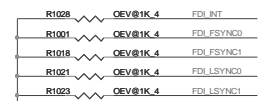
01



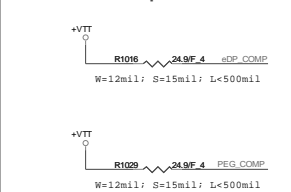
| POWER SYSTEM | | |
|--------------|--------------|-----|
| Charger | (ISL88731C) | P40 |
| System 5V/3V | (TPS51123A) | P41 |
| DDR1.5V | (TPS51216) | P42 |
| VTT | (RT8240BGQW) | P43 |
| +VCCSA | (TI51461) | P44 |
| +VCORE+VGFX | (ISL95836) | P45 |
| +1.8V | (G966A) | P46 |
| AMD_GPU | (ISL95870A) | P47 |



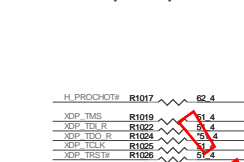
| POWER PLANE | VOLTAGE | CONTROL SIGNAL | Power States ACTIVE IN |
|-------------|-------------|---------------------|------------------------|
| VIN | 10V~+19V | | S0-S5 |
| +VCCRTC | +3.0V~+3.3V | | S0-S5 |
| +3V | +3.3V | MAIN_ON | S0 |
| +3V_S5 | +3.3V | S5_ON | S0-S5 |
| +3V_HDP | +3.3V | MAIN_ON | S0 |
| +3VPCU | +3.3V | AC/DC Insert enable | S0 |
| +5V | +5V | MAIN_ON | S0 |
| +5V_S5 | +5V | S5_ON | S0-S5 |
| +5VPCU | +5V | AC/DC Insert enable | S0-S5 |
| WIMAX_P | +3.3V | WMAX_P for WLAN | |
| +1.8V | +1.8V | MAIN_ON | S0 |
| +1.5V | +1.5V | MAIN_ON | S0 |
| +1.5V_SUS | +1.5V | SUSON | S0-S3 |
| +VCC_CORE | | VRON | S0 |
| +VTT | +1.05V | MAIN_ON | S0 |
| +1.05V | +1.05V | MAIN_ON | S0 |
| +VAXG | | MPWROK | S0 |

FDI Disabling (Discrete Only)
OE

DP & PEG Compensation CPU



Processor pull-up CPU



Level Shift



CPU Thermal sensor / MB Local



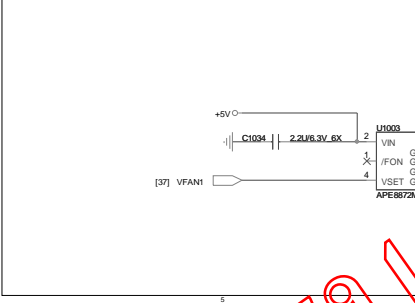
Thermal Trip & Process HOT CPU



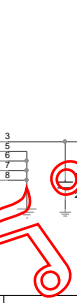
Intel Turbo mode only CPU



FAN Control-->For one FAN solution



THC



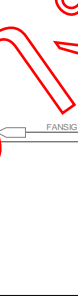
CPU Thermal sensor / MB Local



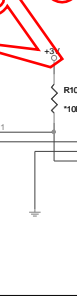
THP/UGA/VGA



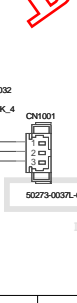
CPU Thermal sensor / MB Local



THP/UGA/VGA



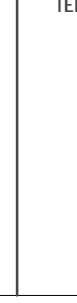
CPU Thermal sensor / MB Local



THP/UGA/VGA



CPU Thermal sensor / MB Local



THP/UGA/VGA



CPU Thermal sensor / MB Local



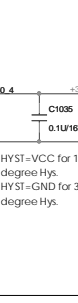
THP/UGA/VGA



CPU Thermal sensor / MB Local



THP/UGA/VGA



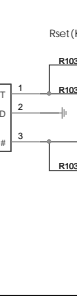
CPU Thermal sensor / MB Local



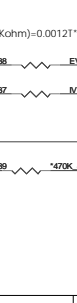
THP/UGA/VGA



CPU Thermal sensor / MB Local



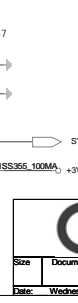
THP/UGA/VGA



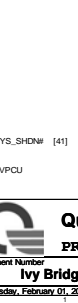
CPU Thermal sensor / MB Local



THP/UGA/VGA



CPU Thermal sensor / MB Local



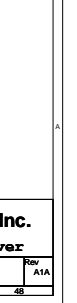
THP/UGA/VGA

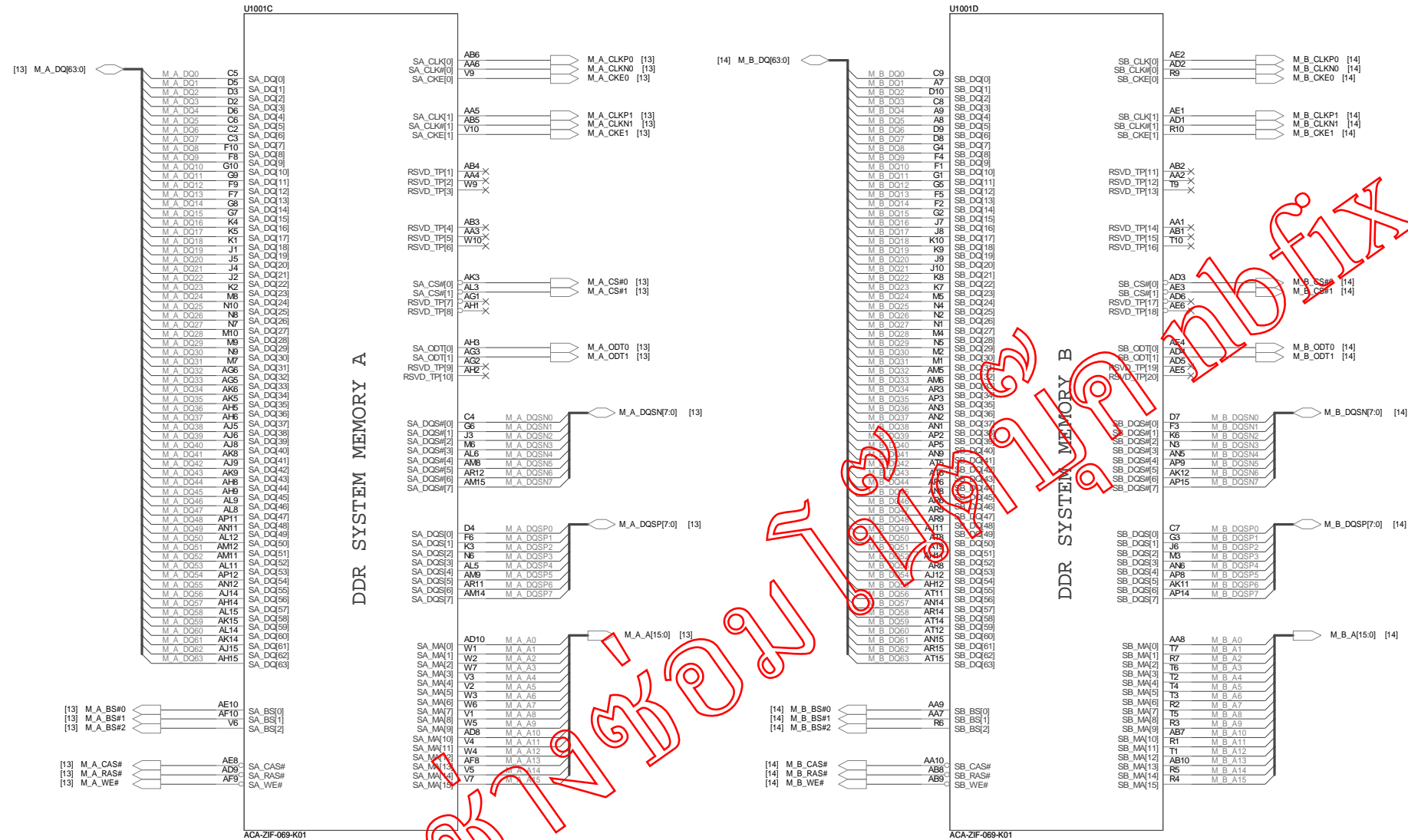


CPU Thermal sensor / MB Local



THP/UGA/VGA

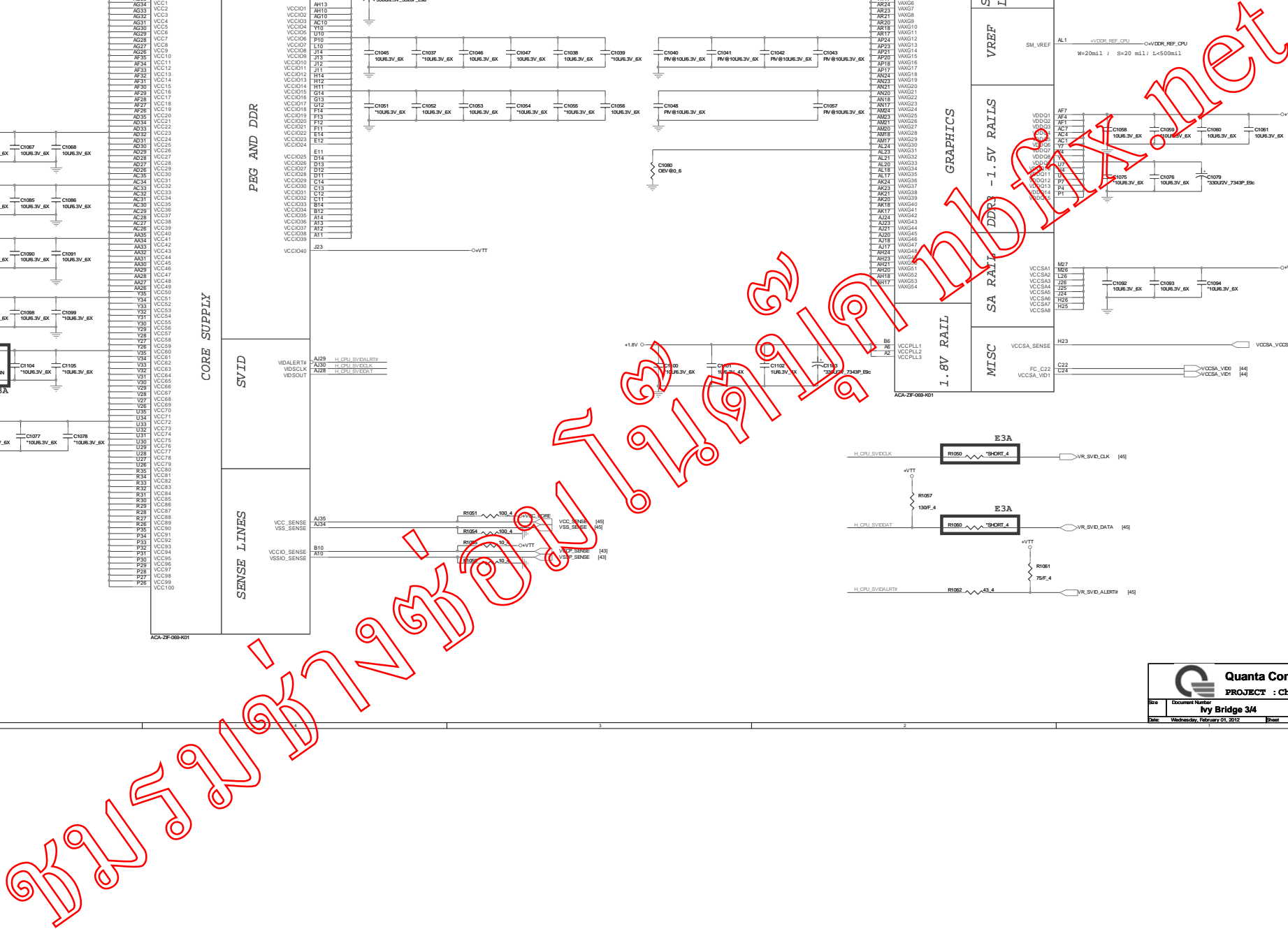


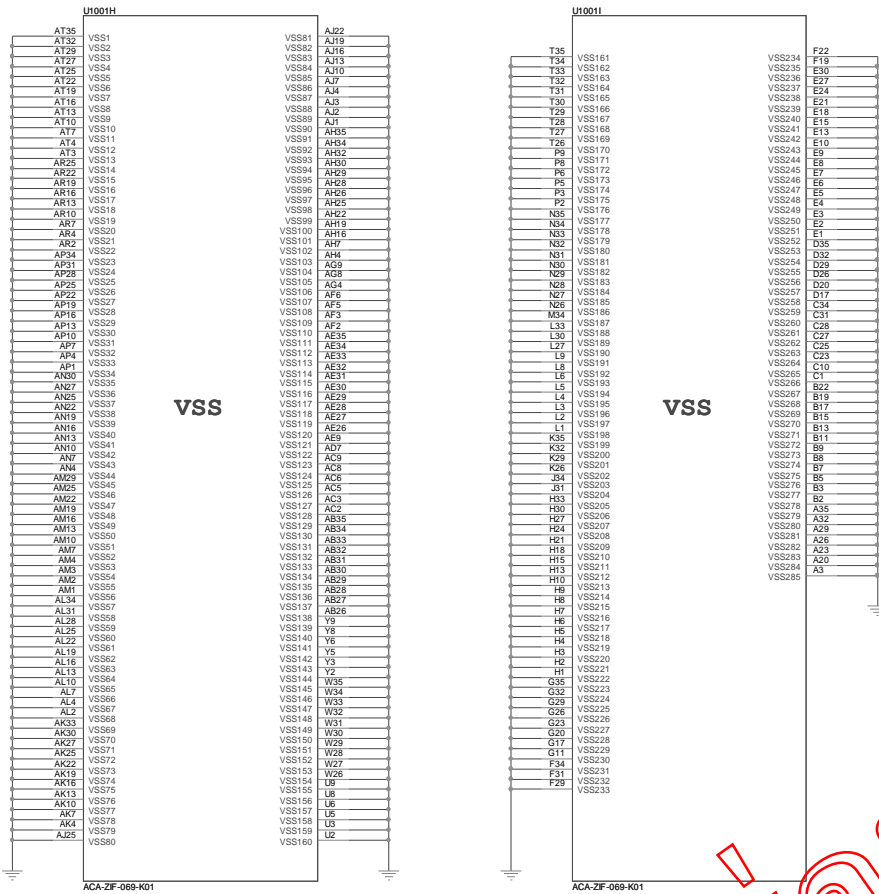


Quanta Computer Inc.

PROJECT : Chief River

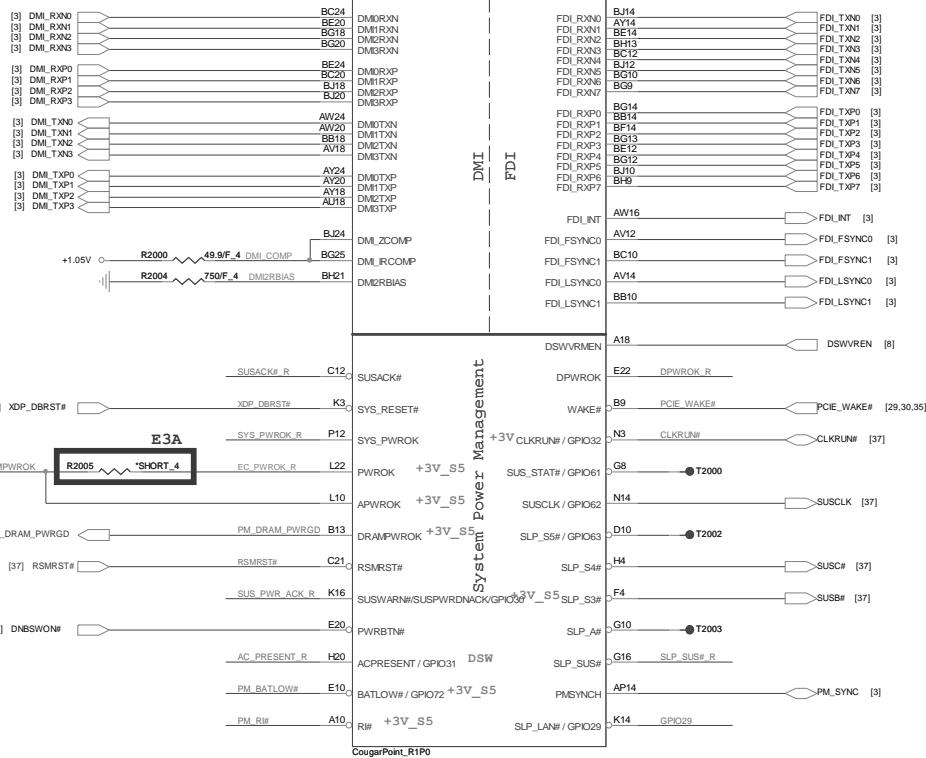
| | | |
|-------|------------------------------|---------------|
| Size | Document Number | Rev |
| | Ivy Bridge 2/4 | A1A |
| Date: | Wednesday, February 01, 2012 | Sheet 4 of 48 |





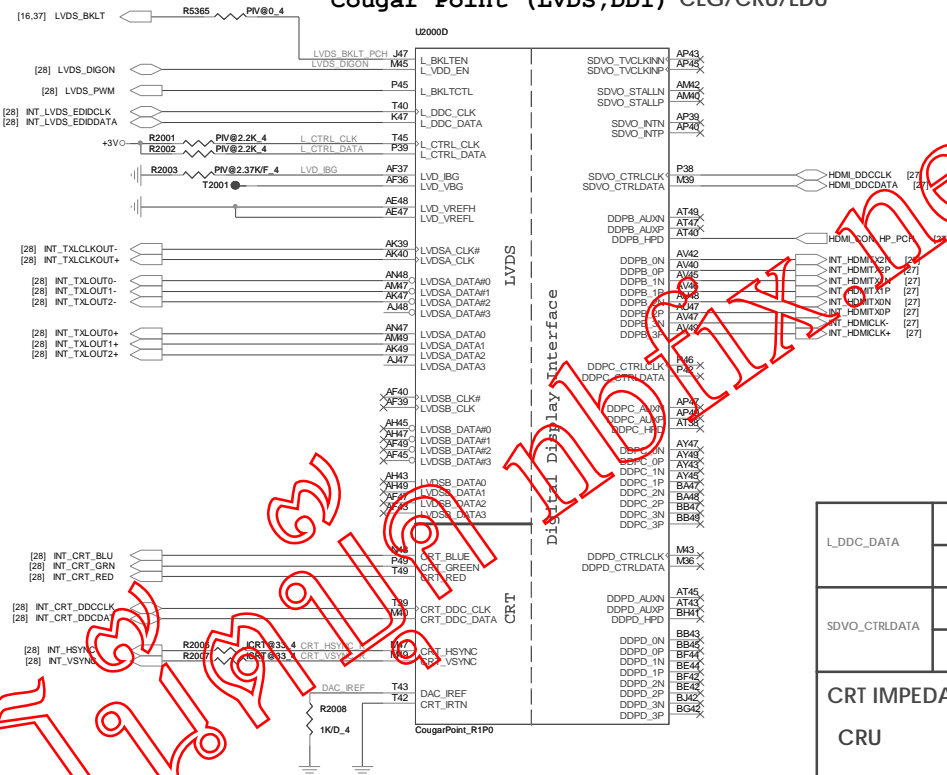
Cougar Point (DMI, FDI, PM) CLG

U2000C



Cougar Point (LVDS, DDI) CLG/CRU/LDU

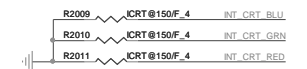
U2000D



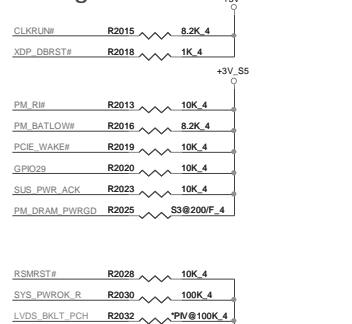
| | |
|--------------|----------------------|
| L_DDC_DATA | 1 -- LVDS ENABLE |
| | 0 -- LVDS DISABLE |
| SDVO_CTRLCLK | 1 -- PORT B Detected |
| | 0 -- PORT B Disable |

CRT IMPEDANCE MATCHING

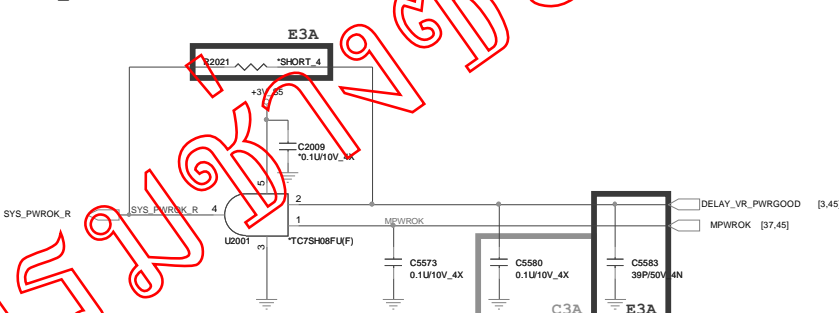
CRU



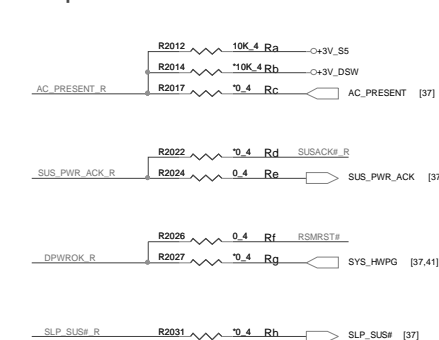
PCH Pull-high/low



System PWR_OK

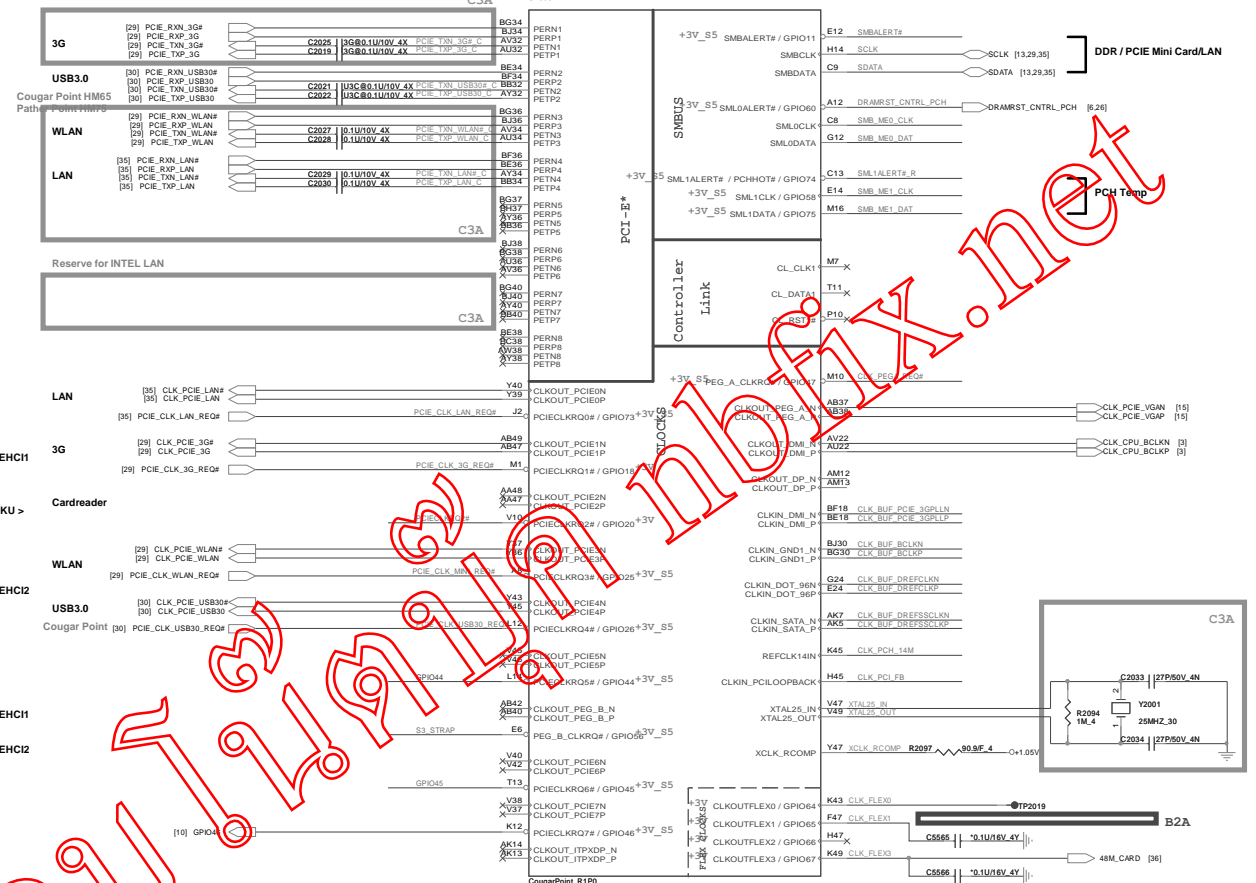


Deep Sx CLG



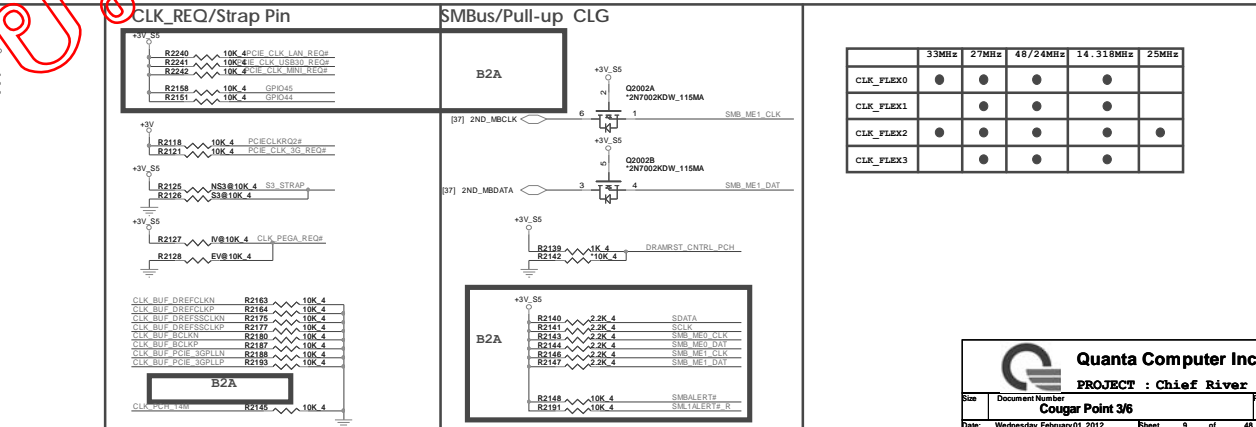
| Net Name | Deep Sx Support | Deep Sx No Support |
|-------------|-----------------|--------------------|
| AC_PRESENT | Rb,Rc stuff | Ra stuff |
| SUS_PWR_ACK | Rd stuff | Re stuff |
| DPWROK | Rg stuff | Rf stuff |
| SLP_SUS | Rh stuff | Rh No stuff |

114

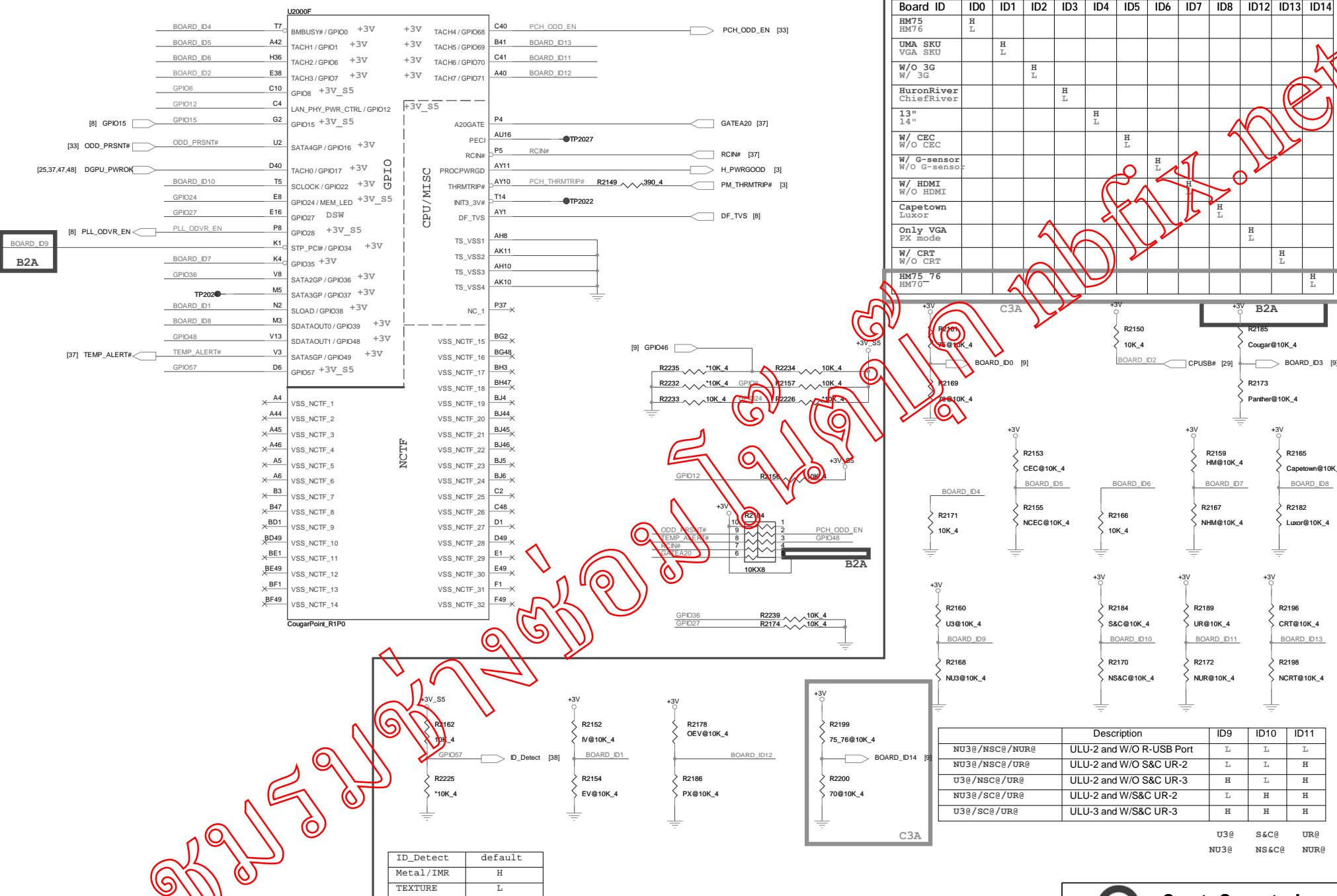


CLG/S3P/NS3P/VGA/UGA

| | |
|---------------|-----|
| SMBus/Pull-up | CLG |
|---------------|-----|



Cougar Point (GPIO,VSS_NCTF,RSVD) CLG



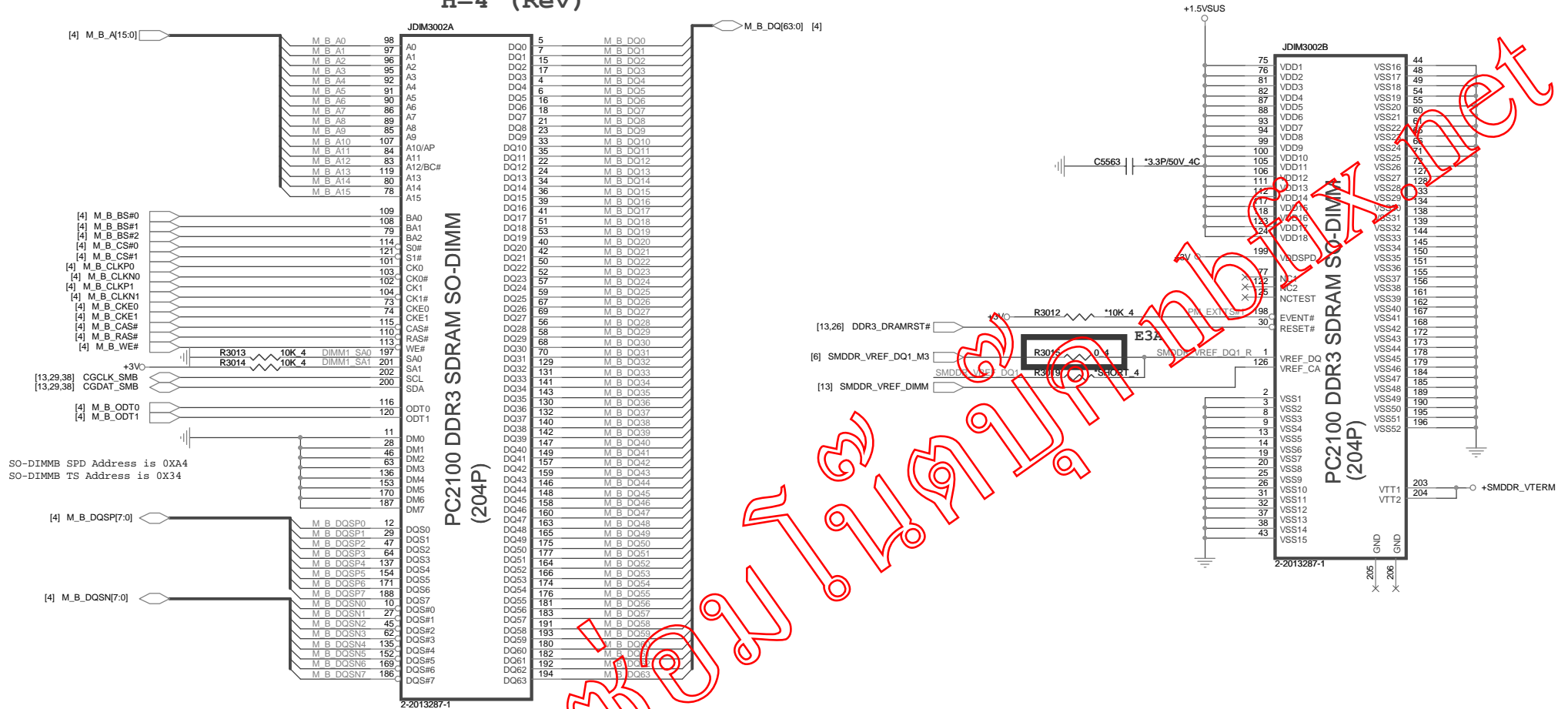


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PROJECT : Chief River

| | | |
|------|------------------------------|----------------|
| Size | Document Number | Rev |
| | Cougar Point 6/6 | A1A |
| Date | Wednesday, February 01, 2012 | Sheet 12 of 46 |

H=4 (Rev)

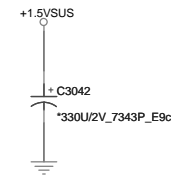
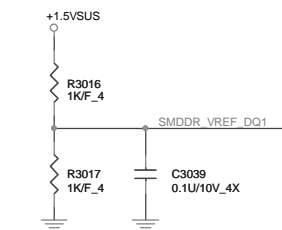
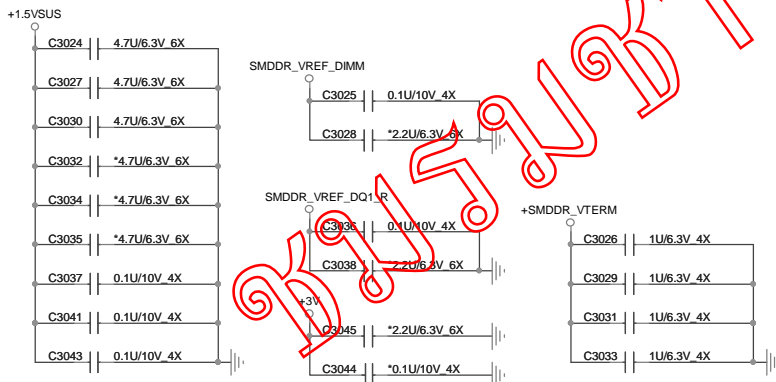


2-2013287-1

2-2013287-1

DDR Power Decoupling DDR

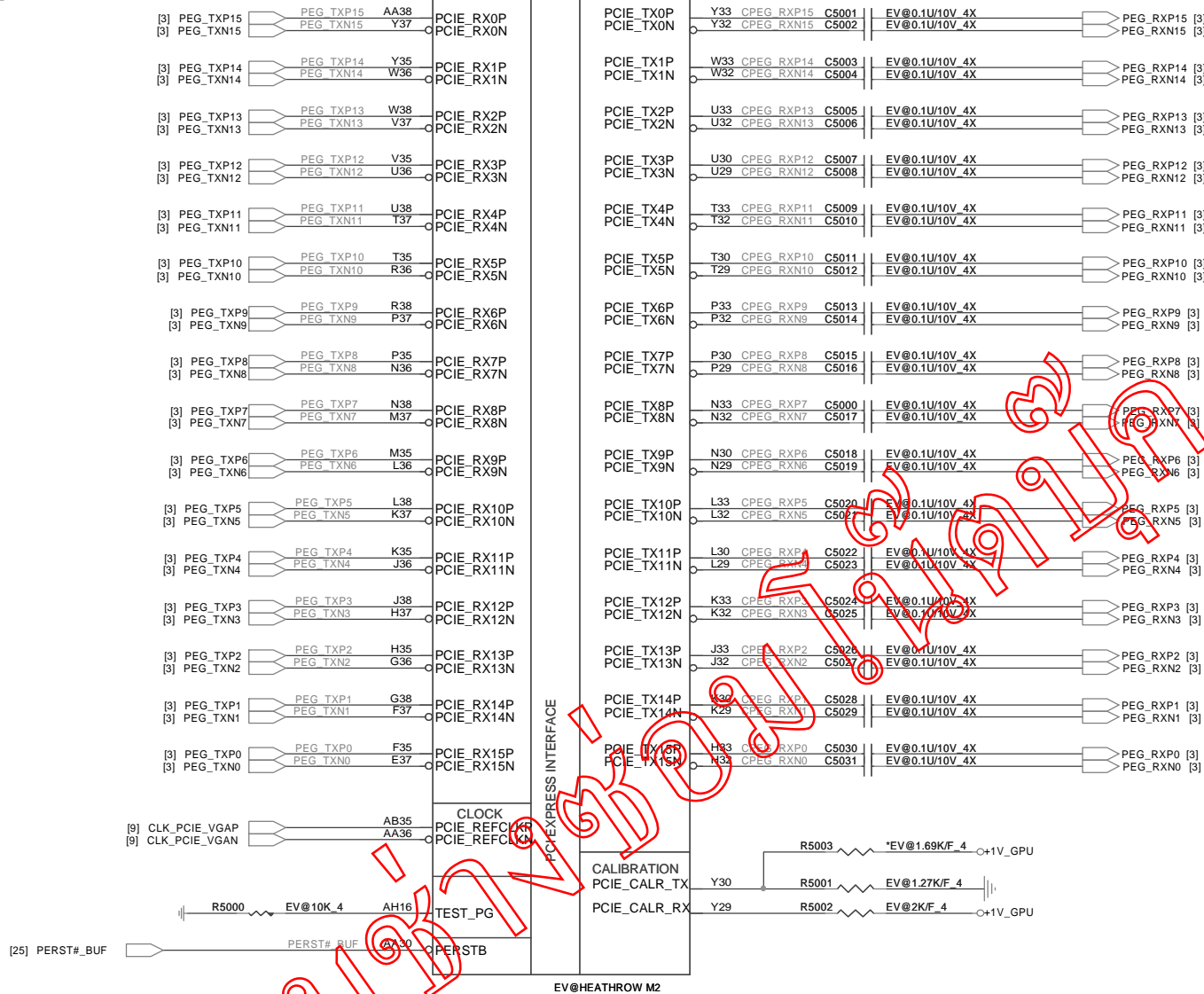
DDR3 VREF DQ (M1) DDR



VGA

[3] PEG_TXP[0..15] → PEG_TXP[0..15]
 [3] PEG_TXN[0..15] → PEG_TXN[0..15]
 [3] PEG_RXP[0..15] → PEG_RXP[0..15]
 [3] PEG_RXN[0..15] → PEG_RXN[0..15]

U5000A
 PART 1 OF 9



Thames and Seymour Power-on sequence

1 => +1V_GPU

2 => +3V_D

3 => +VGPU_CORE,+1.5V_GPU

4 => +1.8V_GPU

PEG

Intel platform: Lane0 ~ Lane15

Brazos platform: Lane12 ~ Lane15

Comal and Sabine platform: Lane8 ~Lane15



Quanta Computer Inc.

PROJECT : Chief River

| | | |
|-------|------------------------------|----------------|
| Size | Document Number | Rev |
| | Thames_M2/ PEG*16 | A1A |
| Date: | Wednesday, February 01, 2012 | Sheet 15 of 48 |



The diagram illustrates the signal paths for the GPU MBCLK and GPU SMBDA signals. The MBCLK path involves a 3V_D supply connected to pin 6 of Q5047A, which is also connected to pin 1 of EVB@2N7002KD_W_115MA through a 10K resistor R5005. The SMBDA path involves a 3V_D supply connected to pin 3 of Q5047B, which is also connected to pin 4 of EVB@2N7002KD_W_115MA through a 10K resistor R5004. Both paths include a 3N0_MBCLK and 3N0_MBDATA input signal.

DAC1 Analog Power
1.8V @ 18mA

AVDD

C5032
EV@0.1U10V_4X

C5033
EV@1U6.3V_4X

C5034
EV@4.7U6.3V_6X

L5000

EV@BLM15BD121SN1D_300MA

1.8V_GP

DAC1 Digital Power
1.8V @ 117mA

VDD1DI

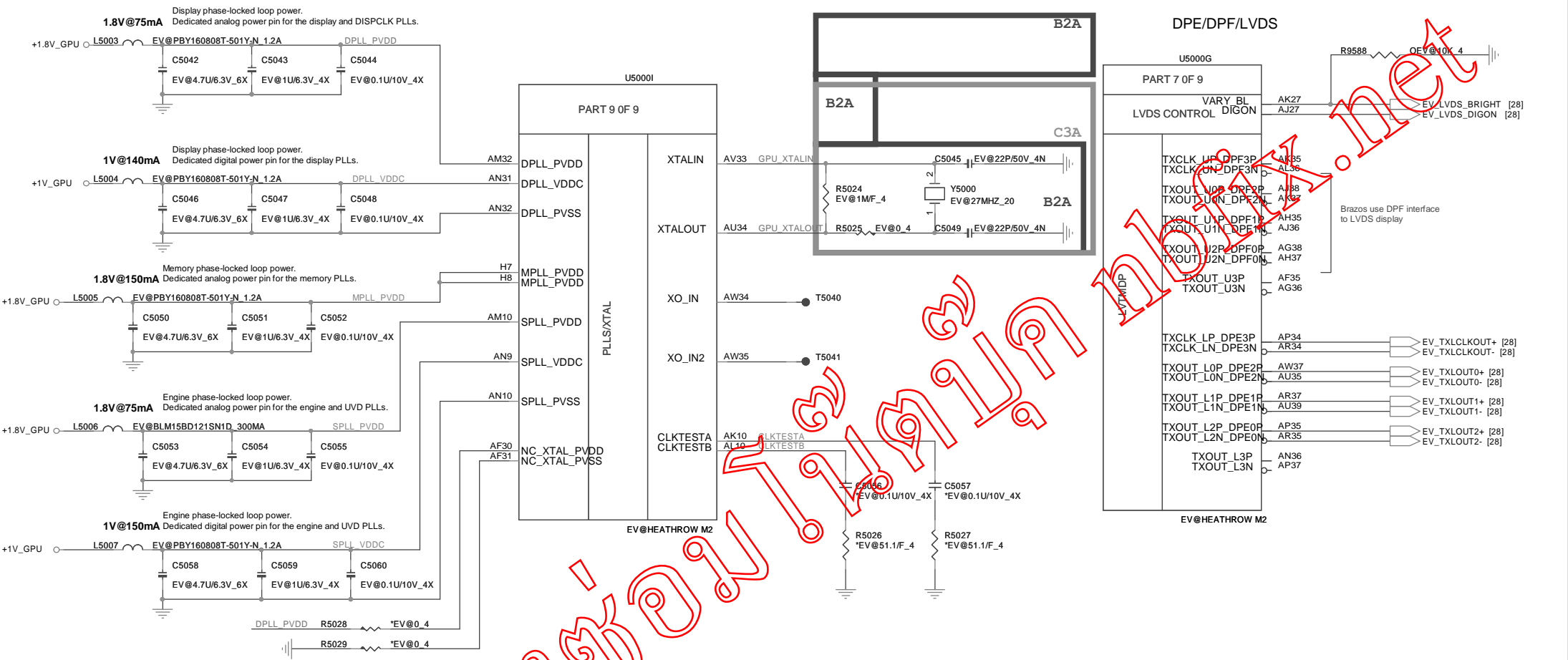
C5035
EV@0.1U10V_4X

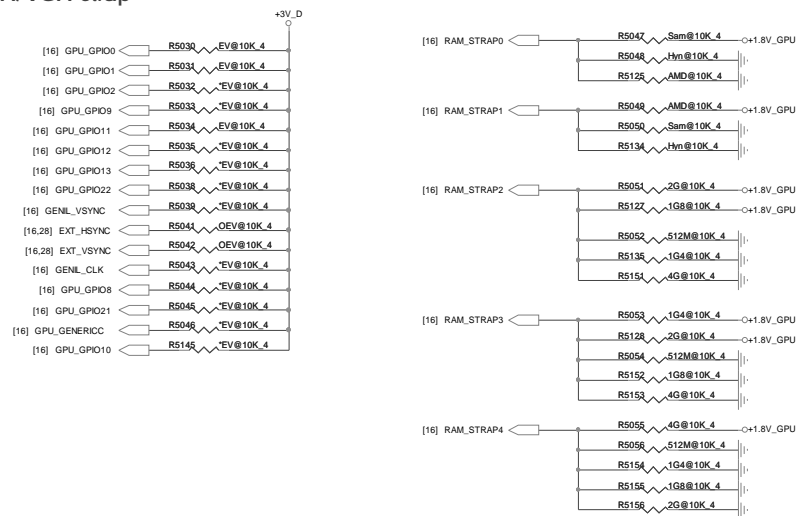
C5036
EV@1U6.3V_4X

C5037
EV@4.7U6.3V_6X

L5001

EV@BLM15BD121SN1D_300MA





| DDR3 Memory TYPE | | | | Size | | Vendor | | |
|------------------|------------------------------|------------------|-------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| Vendor | Vendor P/N | STN B/S P/N | Size | RAM_STRAP4 DVPDATA_4 | RAM_STRAP3 DVPDATA_3 | RAM_STRAP2 DVPDATA_2 | RAM_STRAP1 DVPDATA_1 | RAM_STRAP0 DVPDATA_0 |
| Hynix | H5TQ1G63DFR-11C (64M*16) | AKD5LZWTW02 * 4 | 512MB | 0 | 0 | 0 | 0 | 0 |
| | | AKDSLZWTW02 * 8 | 1GB | 0 | 0 | 1 | 0 | 0 |
| | H5TQ2G63BFR-11C (128M*16) | AKD5MGWWTW00 * 4 | 1GB | 0 | 1 | 0 | 0 | 0 |
| | | AKD5MGWWTW00 * 8 | 2GB | 0 | 1 | 1 | 0 | 0 |
| | H5TQ4G***** (256M*16) | AK***** * 8 | 4GB | 1 | 0 | 0 | 0 | 0 |
| Samsung | K4W1G1646G-BC11 (64M*16) | AKD5EGGT500 * 4 | 512MB | 0 | 0 | 0 | 0 | 0 |
| | | AKD5EGGT500 * 8 | 1GB | 0 | 0 | 1 | 0 | 1 |
| | K4W2G1646G-HC11 (128M*16) | AKD5MGWT500 * 4 | 1GB | 0 | 1 | 0 | 0 | 1 |
| | | AKD5MGWT500 * 8 | 2GB | 0 | 1 | 1 | 0 | 1 |
| | K4W4G***** (256M*16) | AK***** * 8 | 4GB | 1 | 0 | 0 | 0 | 1 |
| AMD | 23EY2387MC11 (64M*16) | AKD5EZWT700 * 4 | 512MB | 0 | 0 | 0 | 1 | 0 |
| | | AKD5EZWT700 * 8 | 1GB | 0 | 0 | 1 | 1 | 0 |
| | 23EY4187MC11 (128M*16) | AKD5DZWT700 * 4 | 1GB | 0 | 1 | 0 | 1 | 0 |
| | | AKD5DZWT700 * 8 | 2GB | 0 | 1 | 1 | 1 | 0 |
| | 23EY***** (256M*16) | AK***** * 8 | 4GB | 1 | 0 | 0 | 1 | 0 |

512@ & Hyn@

1GB@ & Hyn@

1GB@ & Hyn@

2GB@ & Hyn@

4GB@ & Hyn@

512@ & Sam@

1GB@ & Sam@

1GB@ & Sam@

2GB@ & Sam@

4GB@ & Sam@

512@ & AMD@

1GB@ & AMD@

1GB@ & AMD@

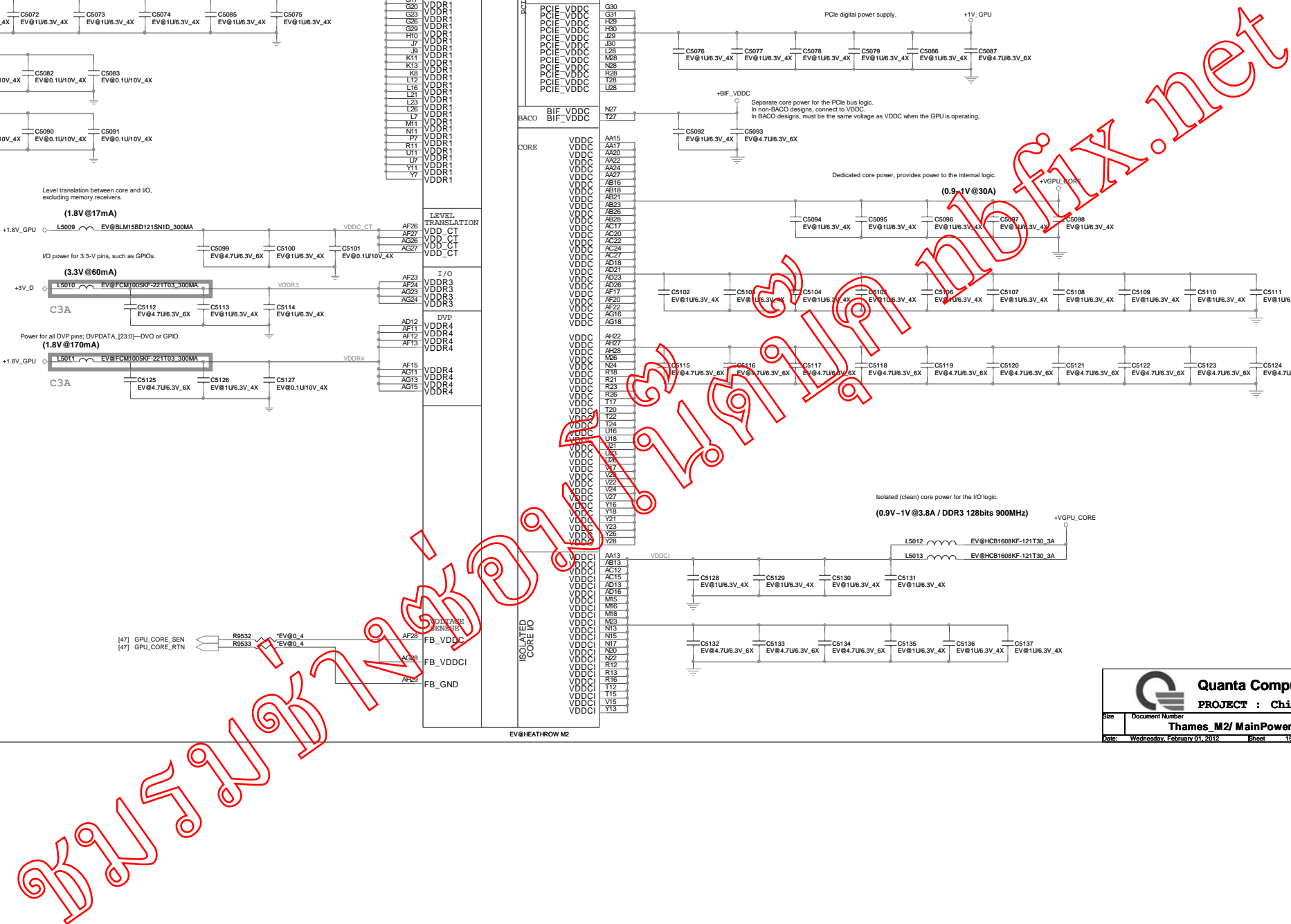
2GB@ & AMD@

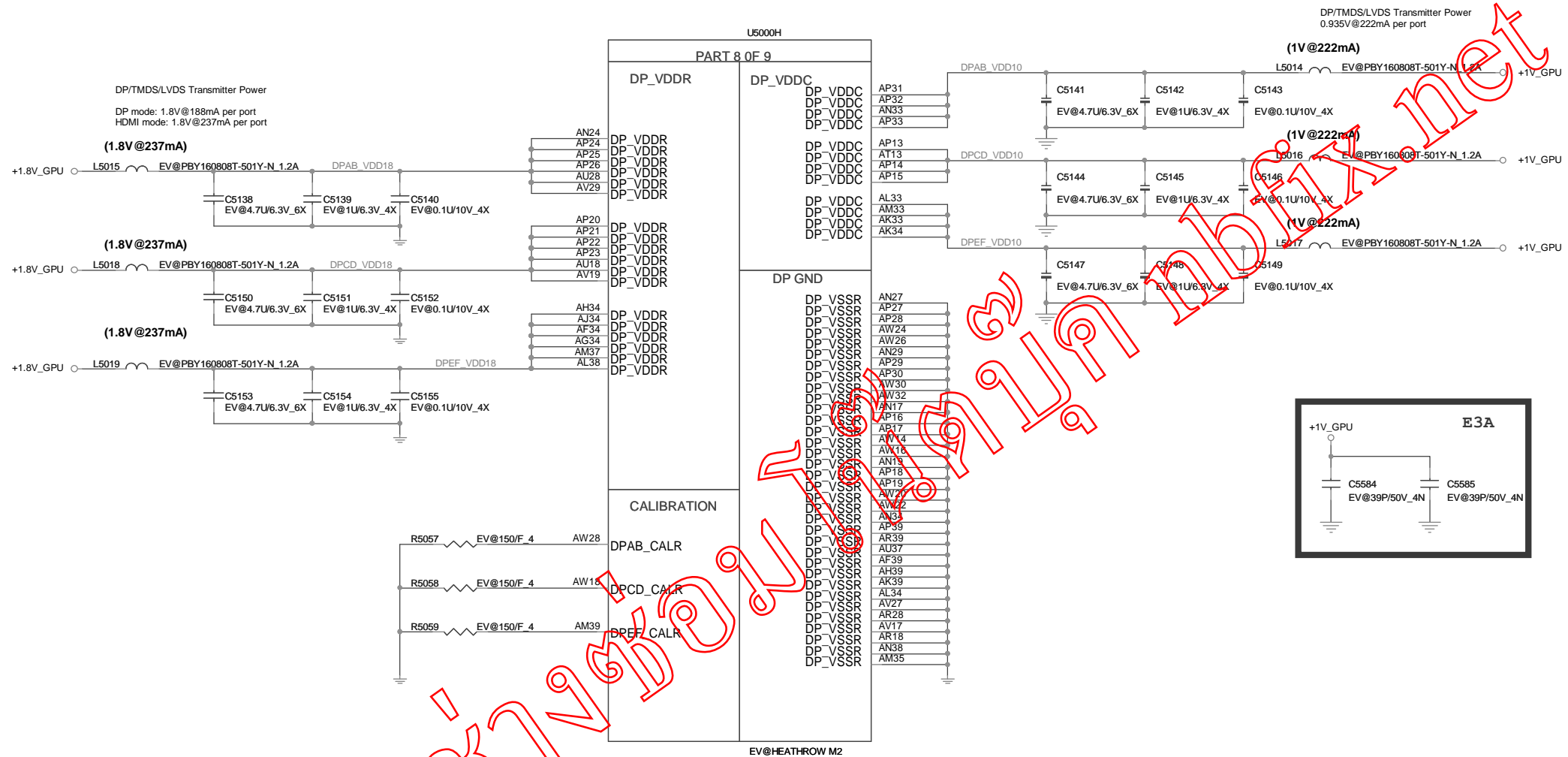
4GB@ & AMD@

| CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET | | | | MB Default Setting(IC internal PD) | |
|---|-------------------------------|-------------------------------------|---|------------------------------------|--|
| STRAPS | MLPS | GPIO PIN | DESCRIPTION OF DEFAULT SETTINGS | | |
| MLPS_DISABLE | NA | GPIO_28_FDO | Enable MLPS. NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP | 1 | |
| TX_PWRS_ENB | PS_1[4] | GPIO0 | Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing | 1 | |
| TX_DEEMPH_EN | PS_1[5] | GPIO1 | PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled | 1 | |
| BIF_GENB_EN_A | PS_1[1] | GPIO2 | PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on | 0 | |
| BIF_VGA_DIS | PS_2[4] | GPIO9 | VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU) | 0 | |
| ROMIDCFG[2:0] | PS_0[3..1] | GPIO[13:11] | Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05 (ST) 101 - 1Mbit M25P06 (ST) 101 - 2Mbit M25P02 (ST) 101 - 8Mbit M25P09 (ST) 100 - 512Kbit Pm25LV01 (Winbond) 101 - 1Mbit Pm25LV010 (Winbond) | xxx | |
| BIOS_ROM_EN | PS_2[3] | GPIO22 | Enable external BIOS ROM device 0: Disabled 1: Enabled | 0 | |
| AUD[1] AUD[0] | NA NA | HSYNC VSYNC | 00 - No audio function 01 - Audio for Display 10 - Audio for Display and HDMI 11 - Audio for both Display and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature. | XX | |
| CEC_DIS | PS_0[4] | GENL_CLK | Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled | 0 | |
| RESERVED RESERVED RESERVED | PS_1[3] PS_1[2] NA | GPIO2 GPIO3 GPIO22 GENERIC | Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only) | 0 0 0 0 | |
| AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0] | PS_3[5] PS_3[4] PS_0[5] | NA NA NA | STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable | xxx | |

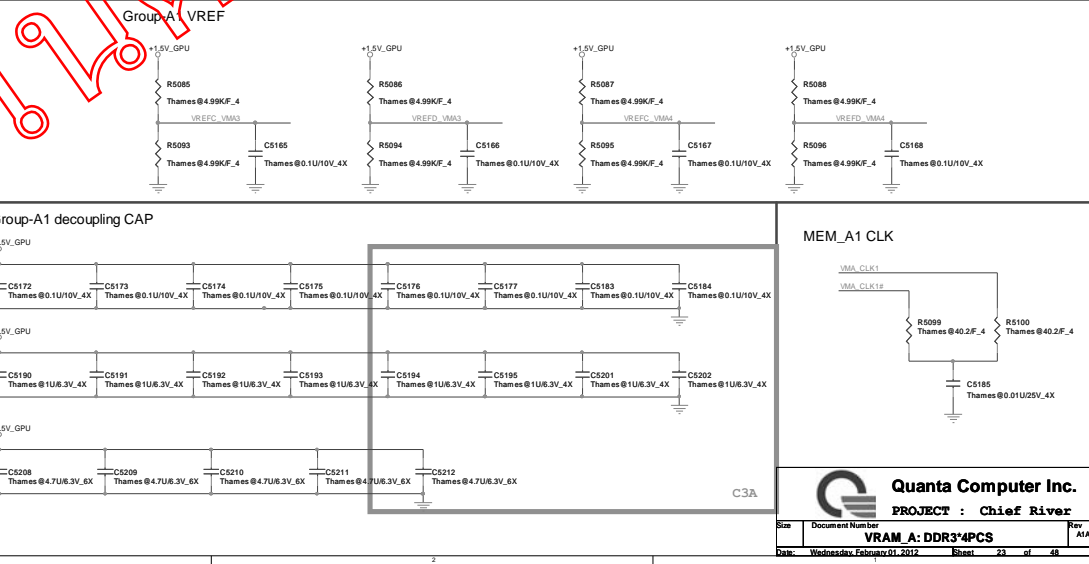
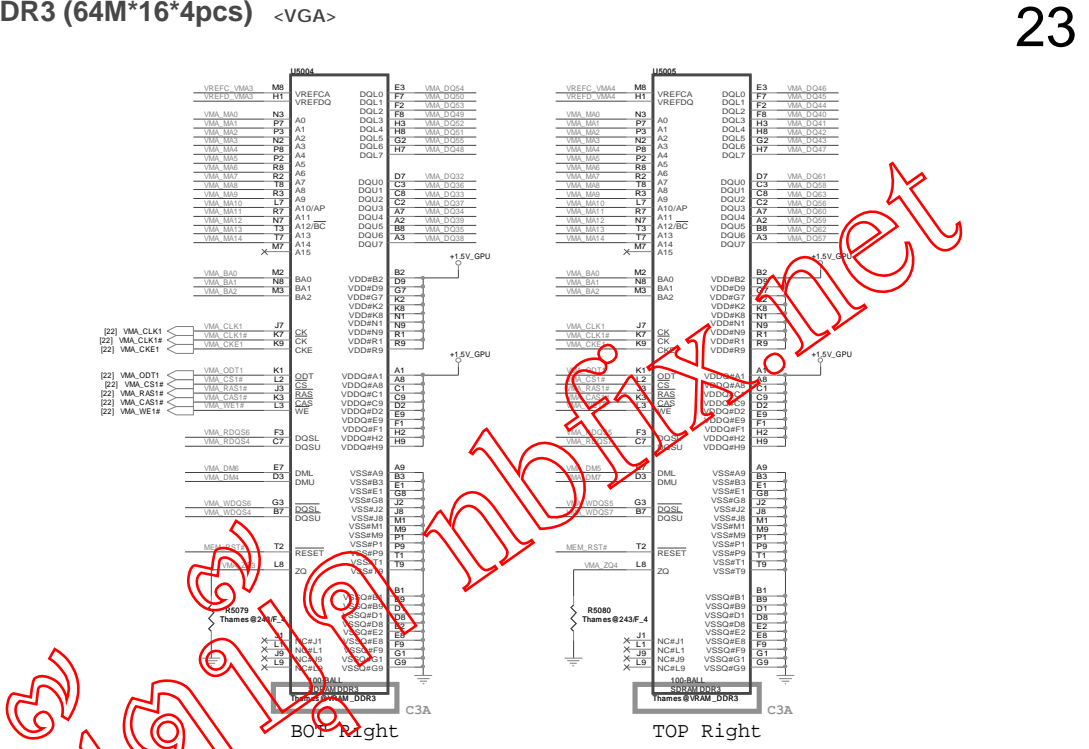
System Memory Aperture size

| GPIO22 BIOSROM | | GPIO13 ROMIDCFG2 | GPIO12 ROMIDCFG1 | GPIO11 ROMIDCFG0 |
|-------------------|------|---------------------|---------------------|---------------------|
| 0 | 128M | 0 | 0 | 0 |
| 0 | 256M | 0 | 0 | 1 |
| 0 | 64M | 0 | 1 | 0 |
| 0 | 32M | 0 | 1 | 1 |

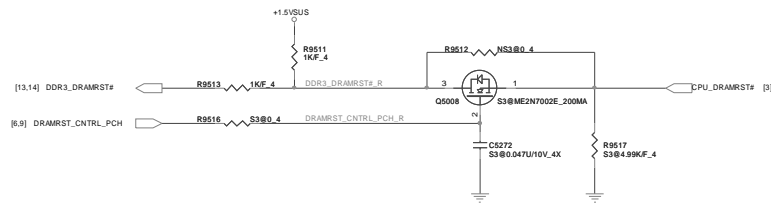




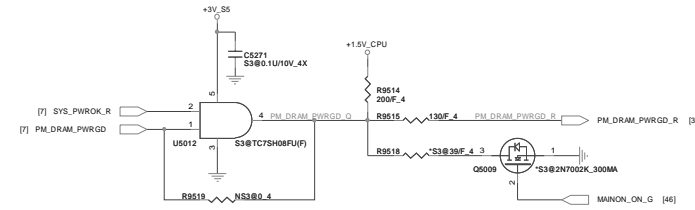
EV@HEATHROW M2



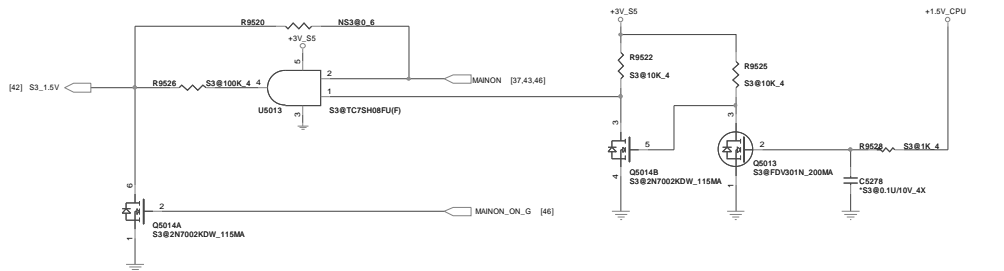
S3 power Reduction (SM_DRAMRST#) S3P/NS3P/CPU



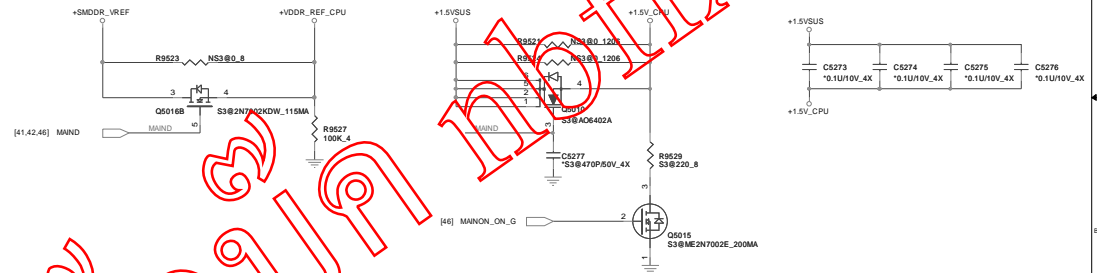
S3 power Reduction (SM_DRAMPWROK) S3P/NS3P/CPU



For S3 power Reduction Sequence S3P/NS3P/CPU



S3 power Reduction (CPU Power) S3P/NS3P/CPU



For S3 power Reduction VTT discharge S3P/NS3P/CPU

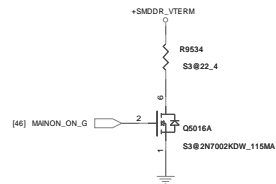
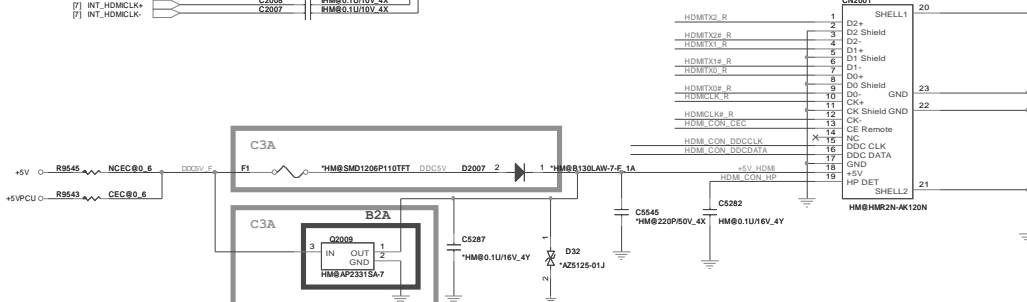
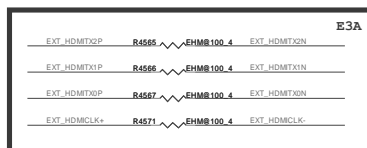
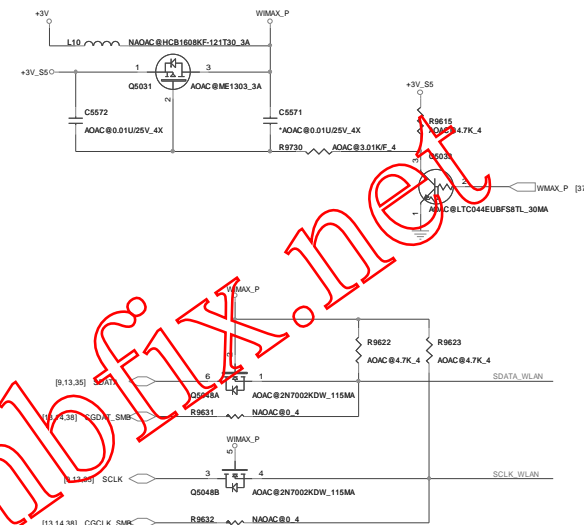
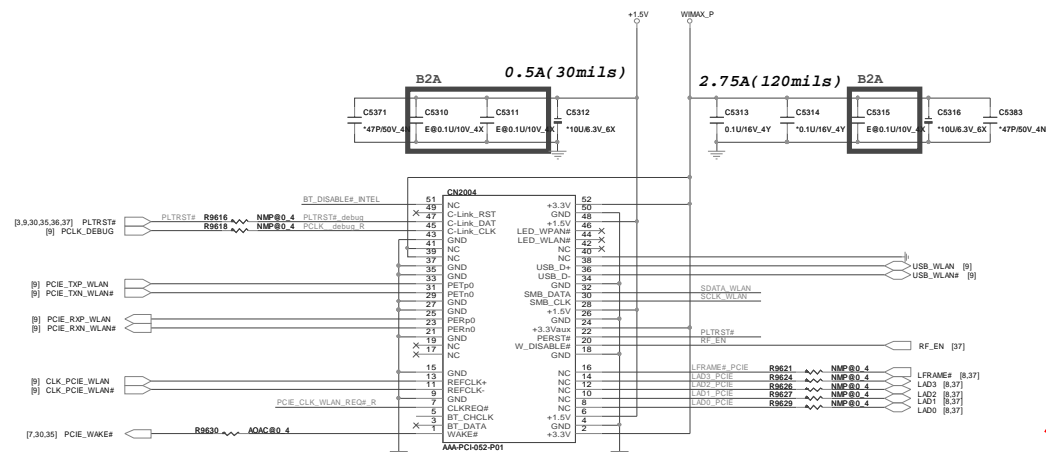
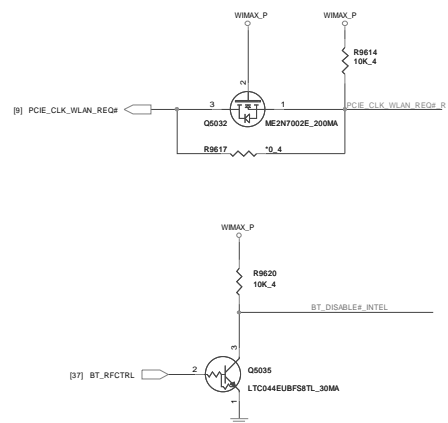
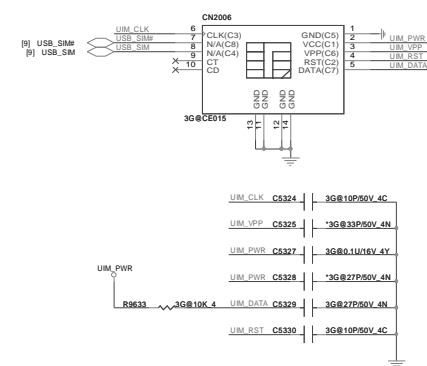
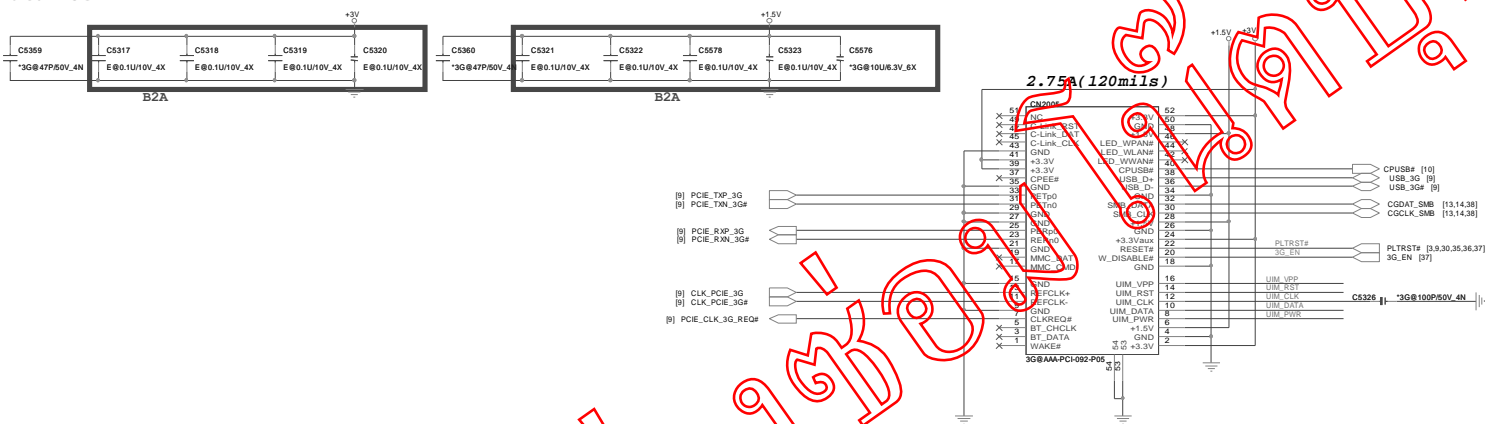


Figure 1: Schematic representation of the HMDT-XN and HMDT-XN-KLK circuit. The diagram shows two main sections: HMDT-XN (top) and HMDT-XN-KLK (bottom). Each section has an input stage with two inputs (EXT and INT) and an output stage with two outputs (R and KLK). The input stage uses a 2-to-1 multiplexer (MUX) to select between the EXT and INT inputs based on a control signal (XN or XN-KLK). The output stage uses a 2-to-1 MUX to select between the outputs of the two input stages based on a control signal (R or KLK). The HMDT-XN section uses a 2-to-1 MUX to select between the outputs of the two input stages based on a control signal (R or KLK). The HMDT-XN-KLK section uses a 2-to-1 MUX to select between the outputs of the two input stages based on a control signal (R or KLK).

[illegible][illegible]



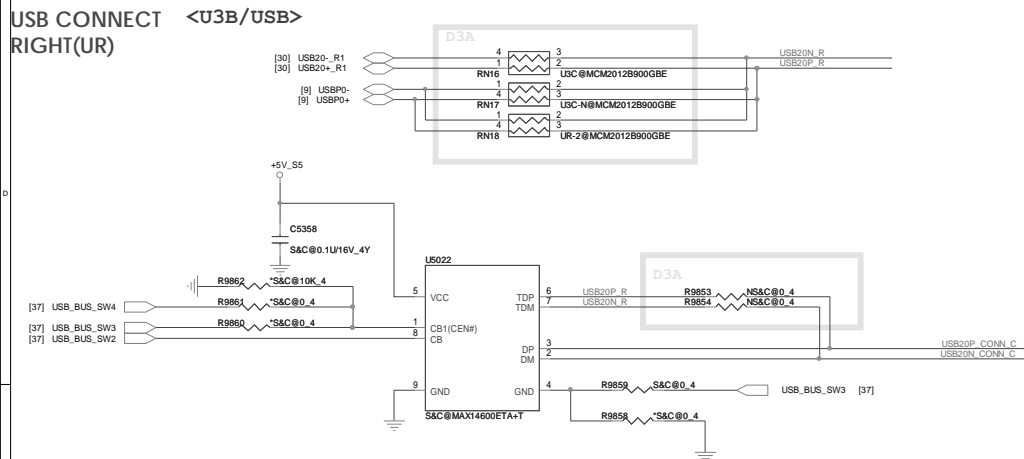
| | |
|-----------|-----|
| MINI | MNG |
| Card | |
| Slot#2-3G | |



| DVCC10 | | |
|----------------|-------|-------|
| Min | Typ | Max |
| 1.00V | 1.05V | 1.10V |
| Current = 71mA | | |

| | |
|---------|---------------------------------------|
| PPWRCTL | VBus controllable, internal pull down |
| 0 | VBus is not controlled by FL1009 |
| 1 | VBus is controlled by FL1009 |

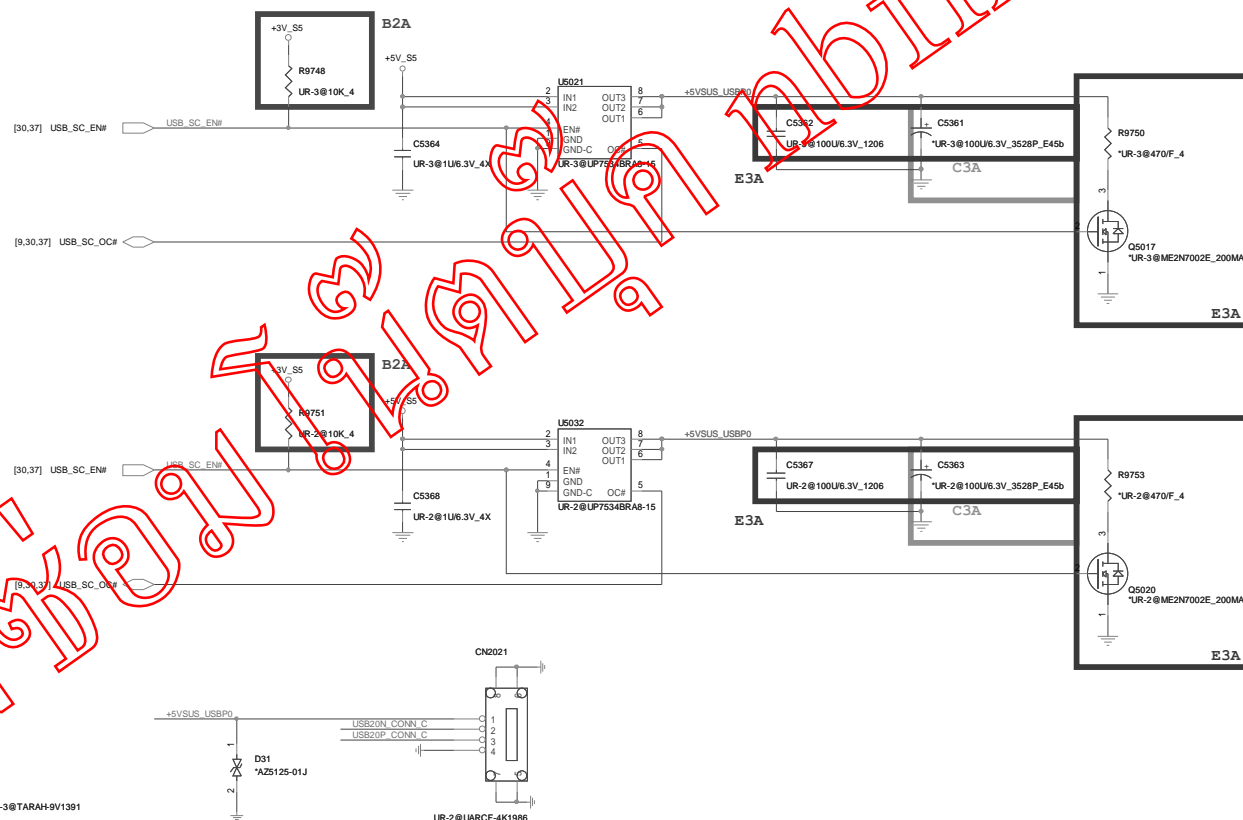
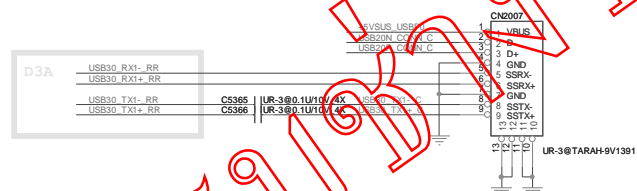




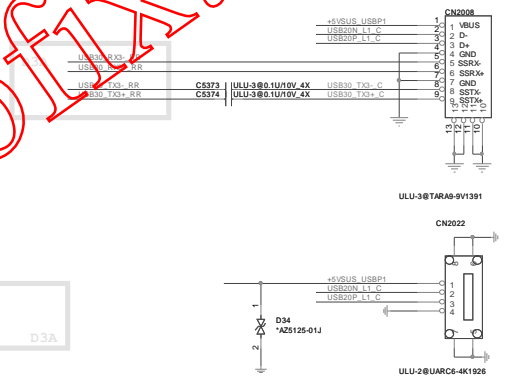
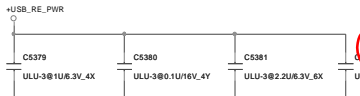
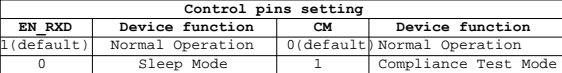
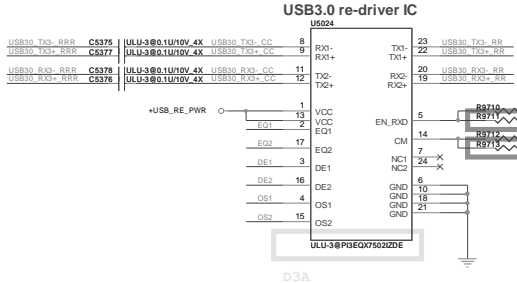
| | R9861 | R9860 | R9859 | R9858 | R9862 |
|-----------------|-------|-------|-------|-------|-------|
| 14566 | | V | | V | |
| 14600 | | | V | | |
| 14617(with CB2) | V | | V | | |
| 14617(no CB2) | | | V | | V |

| | | |
|-----|-----|---|
| | | 14566/14600 |
| CB0 | CB1 | Status |
| 0 | 0 | Auto mode |
| 0 | 1 | Force dedicated charger mode |
| 1 | X | Pass-Through(USB) mode: Connect DP/DM to TDP/TDM for 14566 |
| 1 | 0 | Pass-Through(USB) mode for 14600 |
| 1 | 1 | pass-through(USB) with CDP Emulation for 14600 |

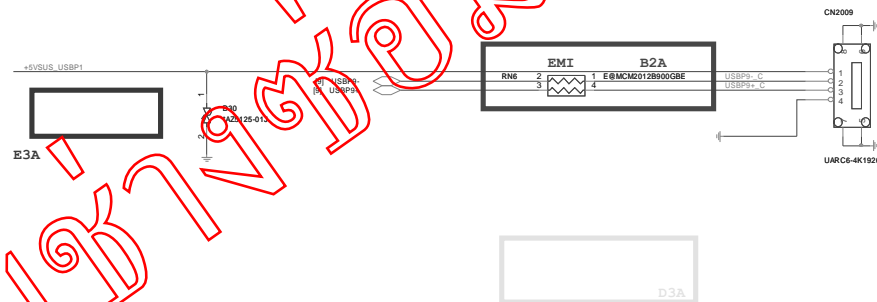
| 14617 | | | |
|-------|-----|-----|---|
| CB0 | CB1 | CB2 | Status |
| X | X | 1 | Force Apple 2A Charger Mode |
| 0 | 0 | 0 | Autodetection charger mode |
| 0 | 1 | 0 | Force-Dedicated Charger Mode |
| 1 | 0 | 0 | USB Pass-Through Mode(USB) Connect DP/DM to TDP/TDM |
| 1 | 1 | 0 | USB Pass-Through Mode with CDP Emulation. Auto connect DP/DM to TDP/TDM depending on CDP status |



<U3B>

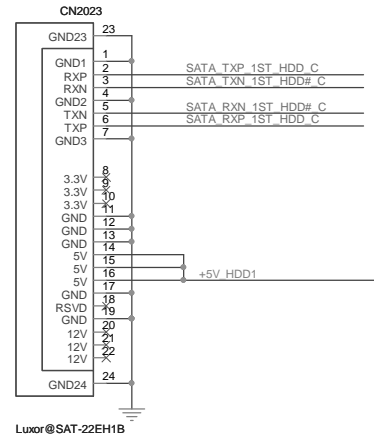
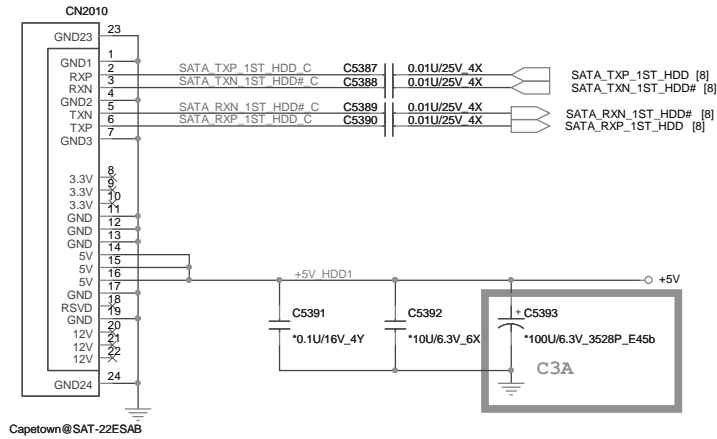


ULD



SATA
HDD

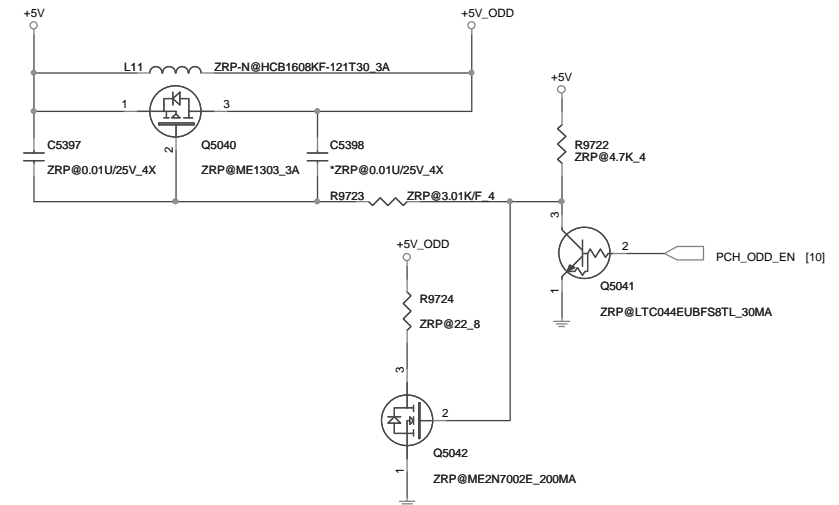
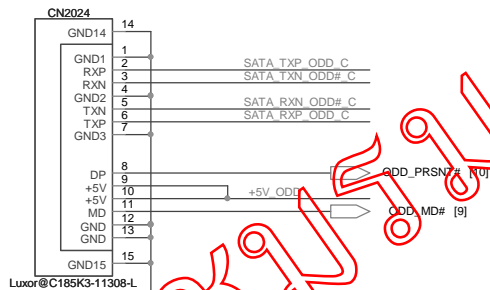
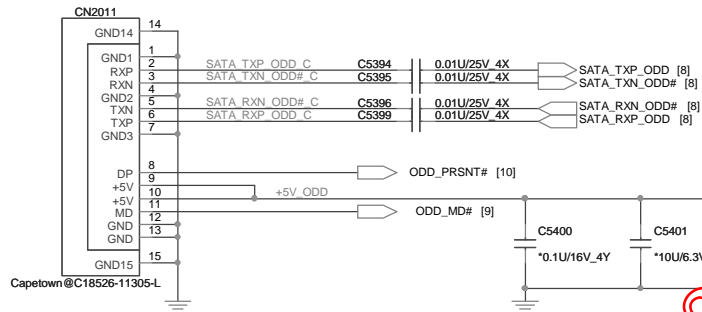
HDD



SATA ODD <ODD>

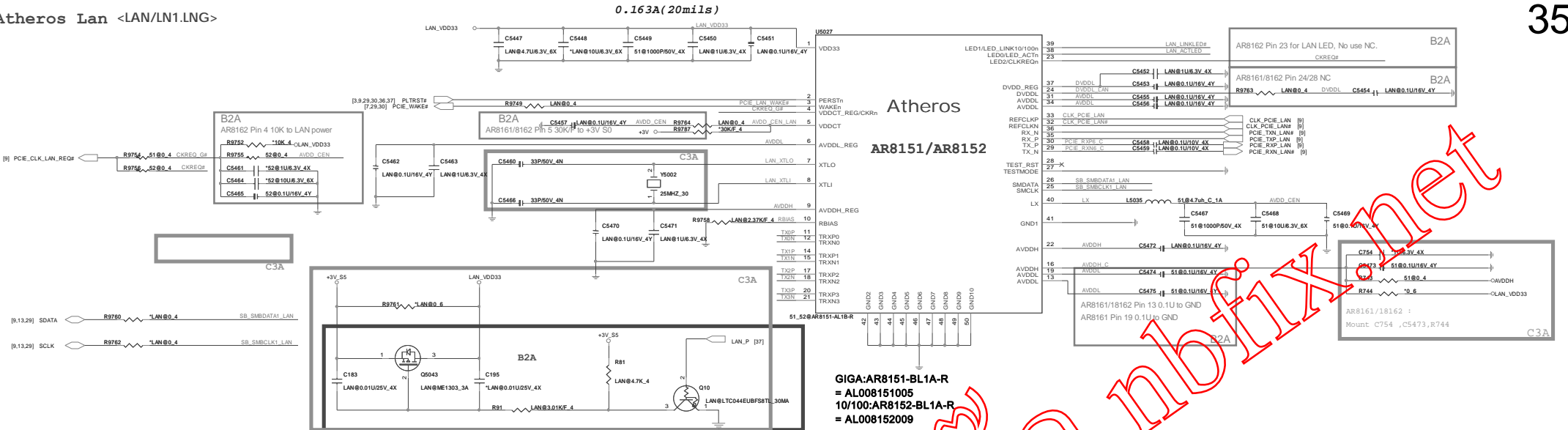
ODD zero power .
(Only for Intel)

<OZP>

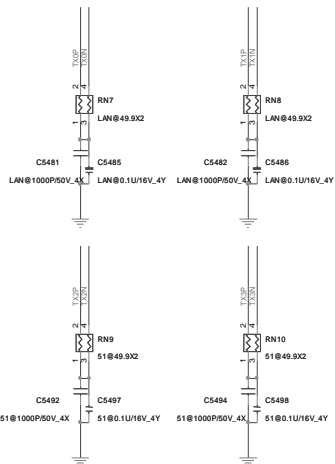


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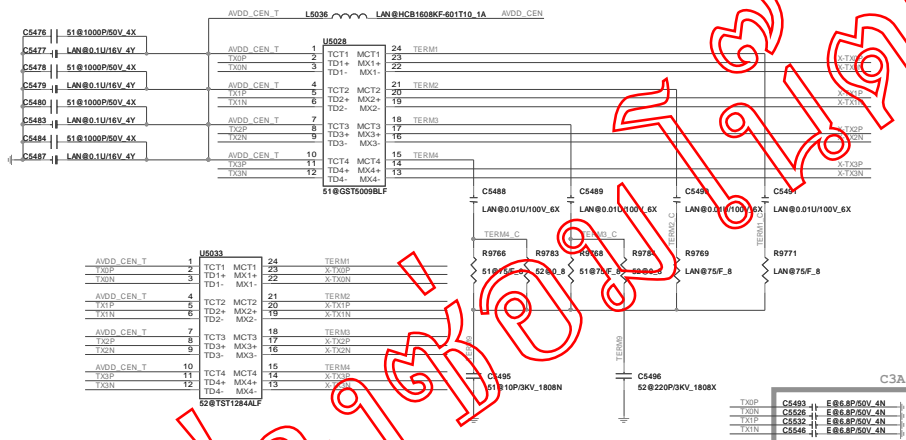
PROJECT : Chief River



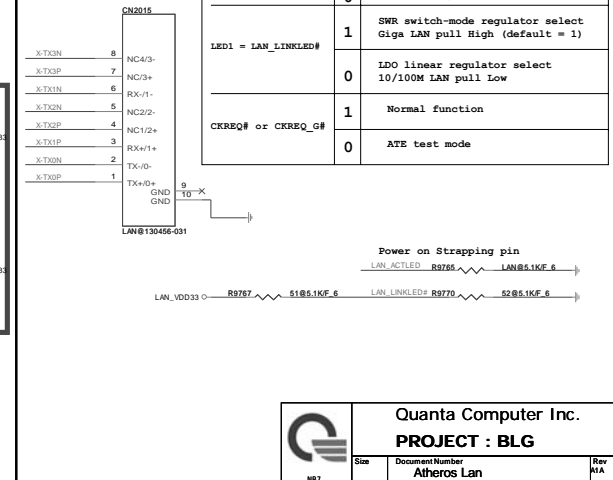
PLACE NEAR LAN IC SIDE <LAN/LN1.LNG>

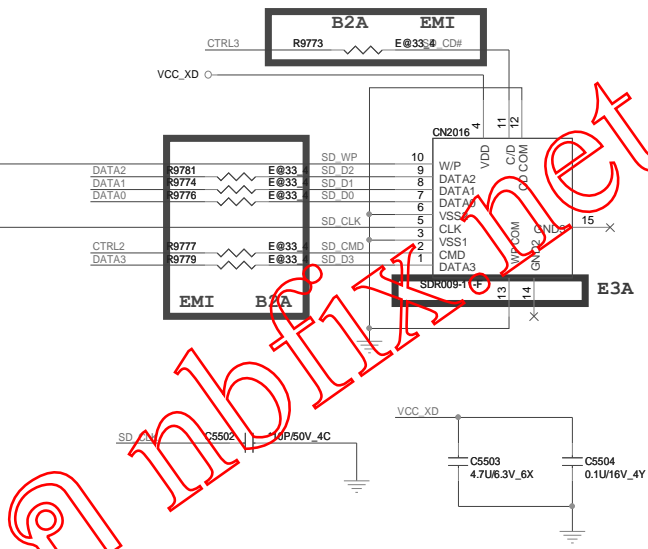
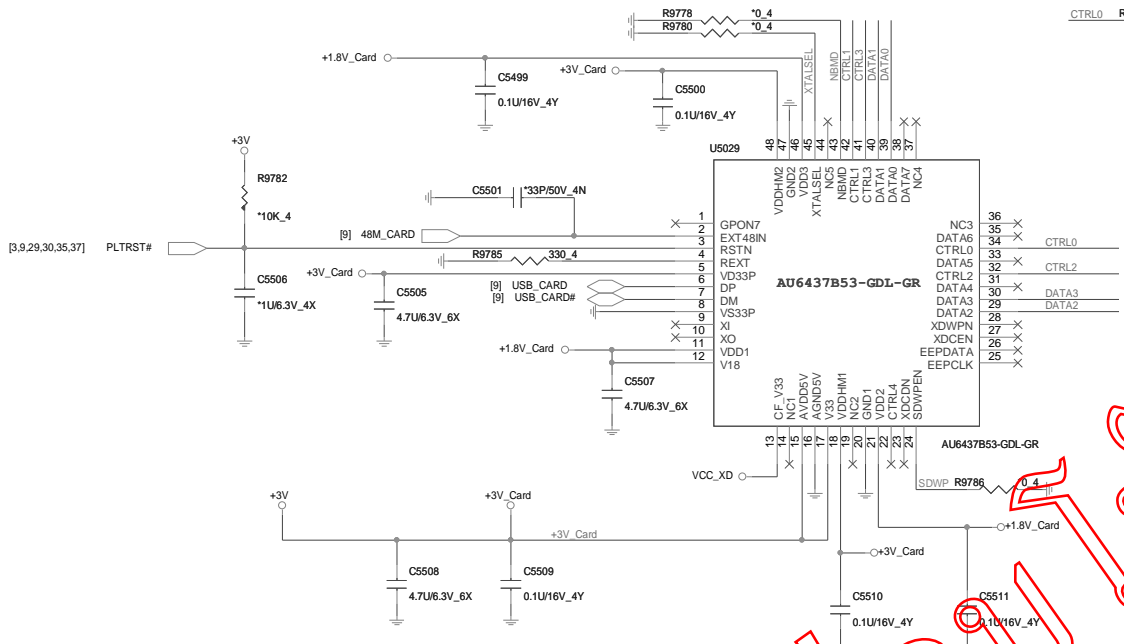


TRANSFORMER <LAN/LN1.LNG>



RJ45 <LAN>

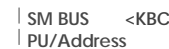




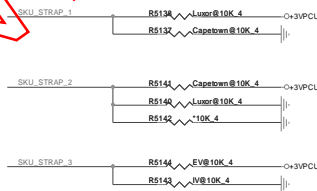
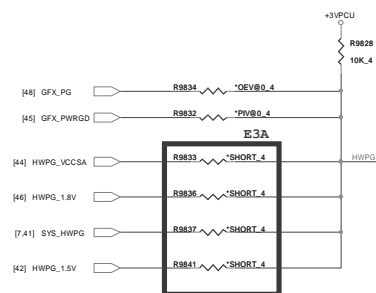
SDWPEN (SD write protect enable)
1 : decided by SDWP(default)
0 : SD always write-able

NBMD (Power saving mode enable)
1 : enable (default)
0 : disable

XTALSEL (Clock input selection)
1 : 48MHz input (default)
0 : 12MHz input



| | SMBUS | Devices | Address |
|-----|-------|----------------------|---------|
| U | 1 | Battery(A) | |
| | 2 | PCH(S5) | |
| | | G-sensor(S0) | |
| | | CPU Thermal(A) | 98H |
| | | IDROM(A) | |
| PCU | 3 | VGA Thermal(A or S0) | 98H |
| | | CEC(A) | |
| | | MMIO(A) | |
| | | | |

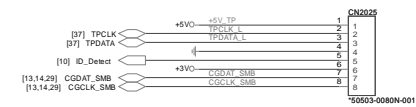


| | Capetown@Luxor@ | | EV@ / I@ |
|------------------|-----------------|-------------|-------------|
| MS Strap | SKU_STRAP_1 | SKU_STRAP_2 | SKU_STRAP_3 |
| 13" UMA | 0 | 0 | 0 |
| 13" DIS | 0 | 0 | 1 |
| 14" Capetown UMA | 0 | 1 | 0 |
| 14" Capetown DIS | 0 | 1 | 1 |
| 14" Luxor UMA | 1 | 0 | 0 |
| 14" Luxor DIS | 1 | 0 | 1 |

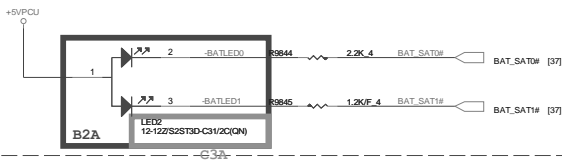
| | |
|-------------------|-------|
| Power board w LED | <PSW> |
|-------------------|-------|



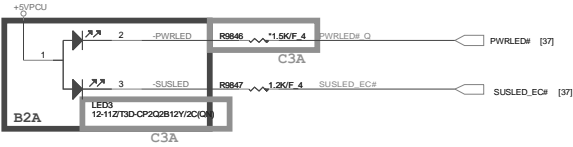
TP board <TPD>



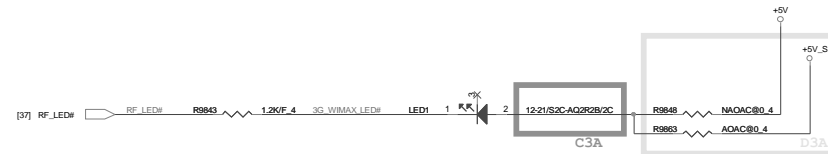
LED LED
BATTERY



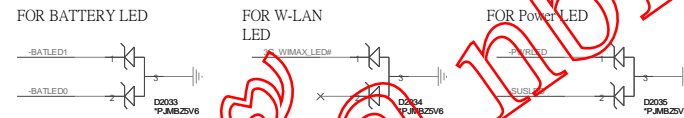
POWER LED



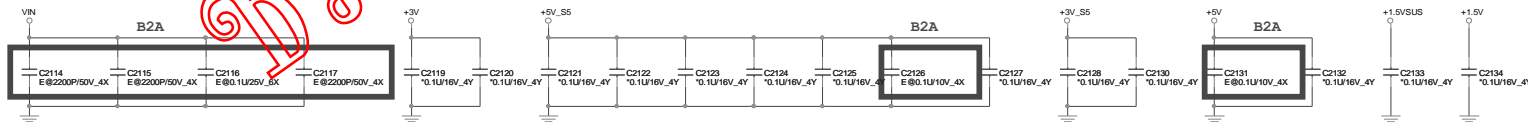
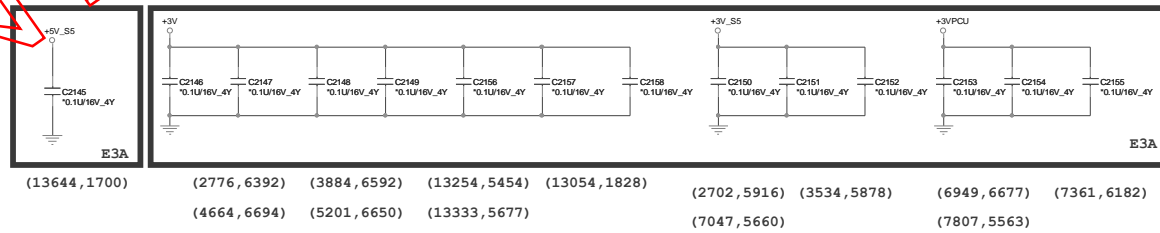
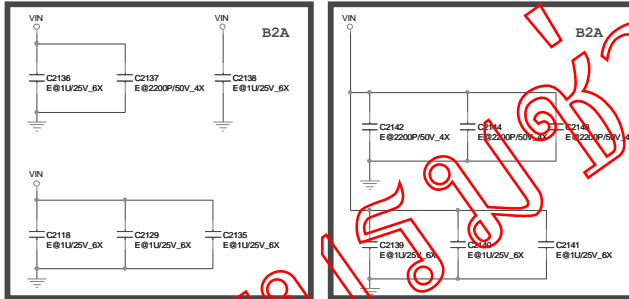
RF LED LED

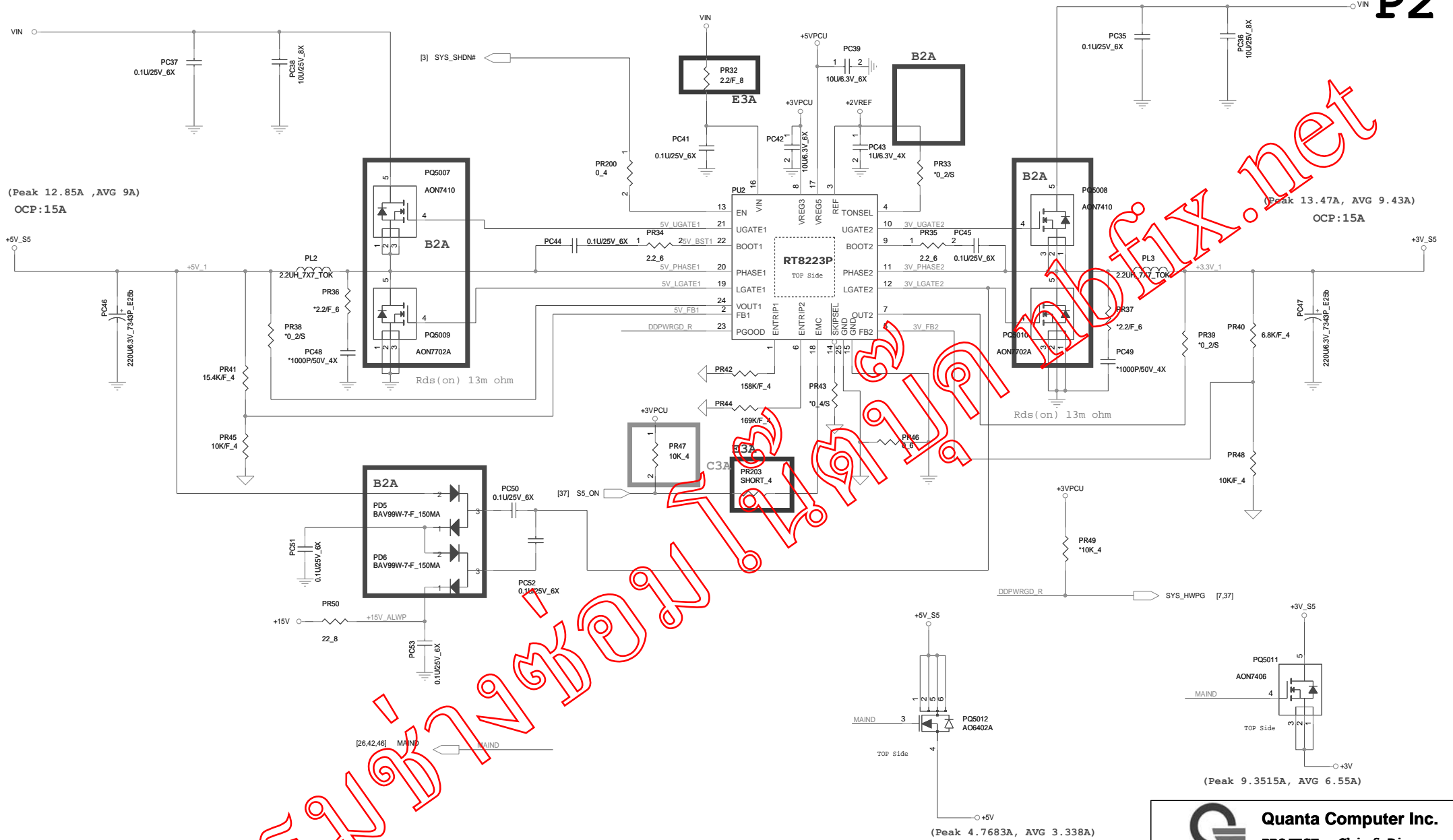


ESD Protect LED



EMI EMI



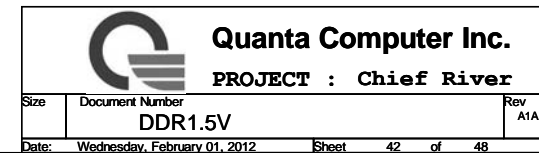


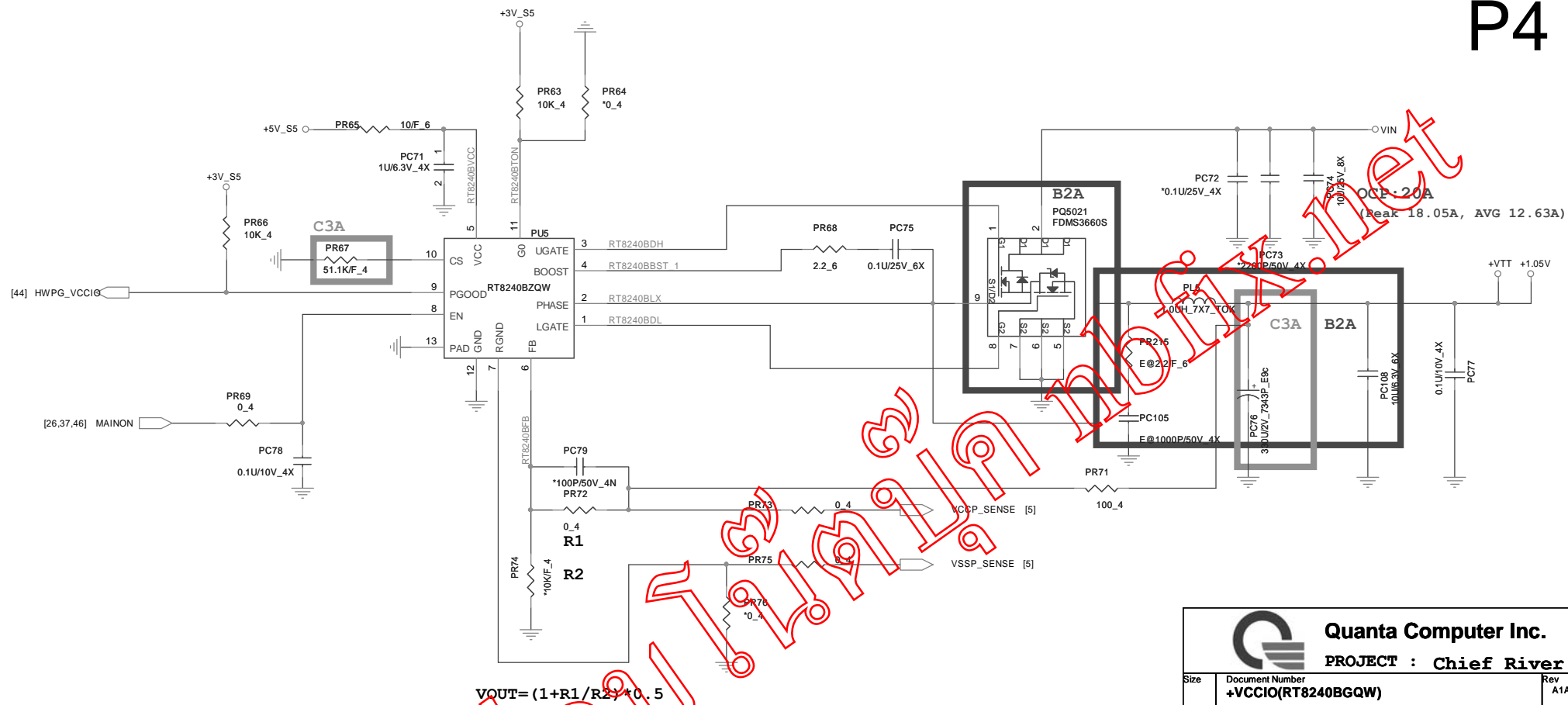
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PROJECT : Chief River

| Size | Document Number | Rev |
|------|-------------------------|-----|
| | System 3V/5V(TPS51123A) | A1A |

Date: Wednesday, February 01, 2012 Sheet 41 of 48



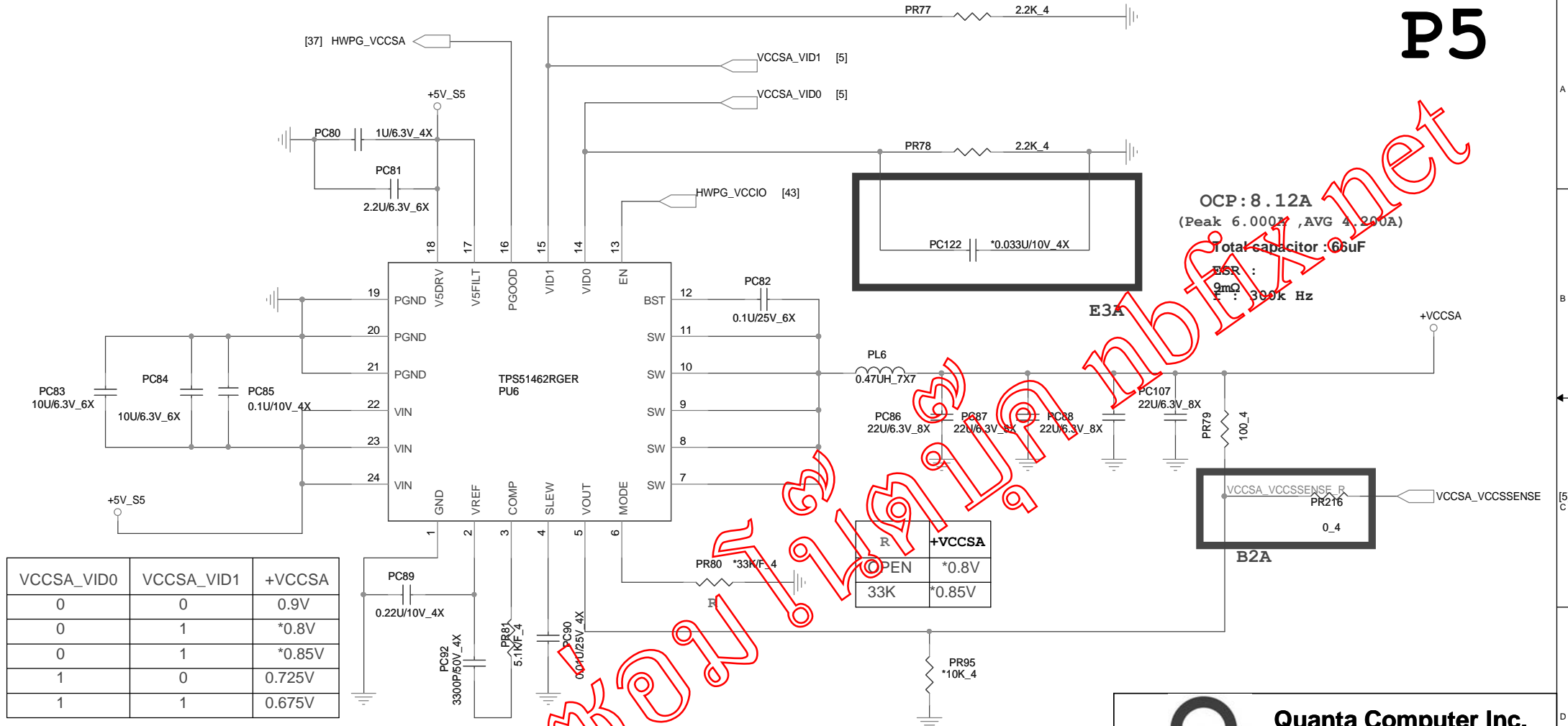


Quanta Computer Inc.

PROJECT : Chief River

| Size | Document Number | Rev |
|-------|------------------------------|----------------|
| | +VCCIO(RT8240BGQW) | A1A |
| Date: | Wednesday, February 01, 2012 | Sheet 43 of 48 |

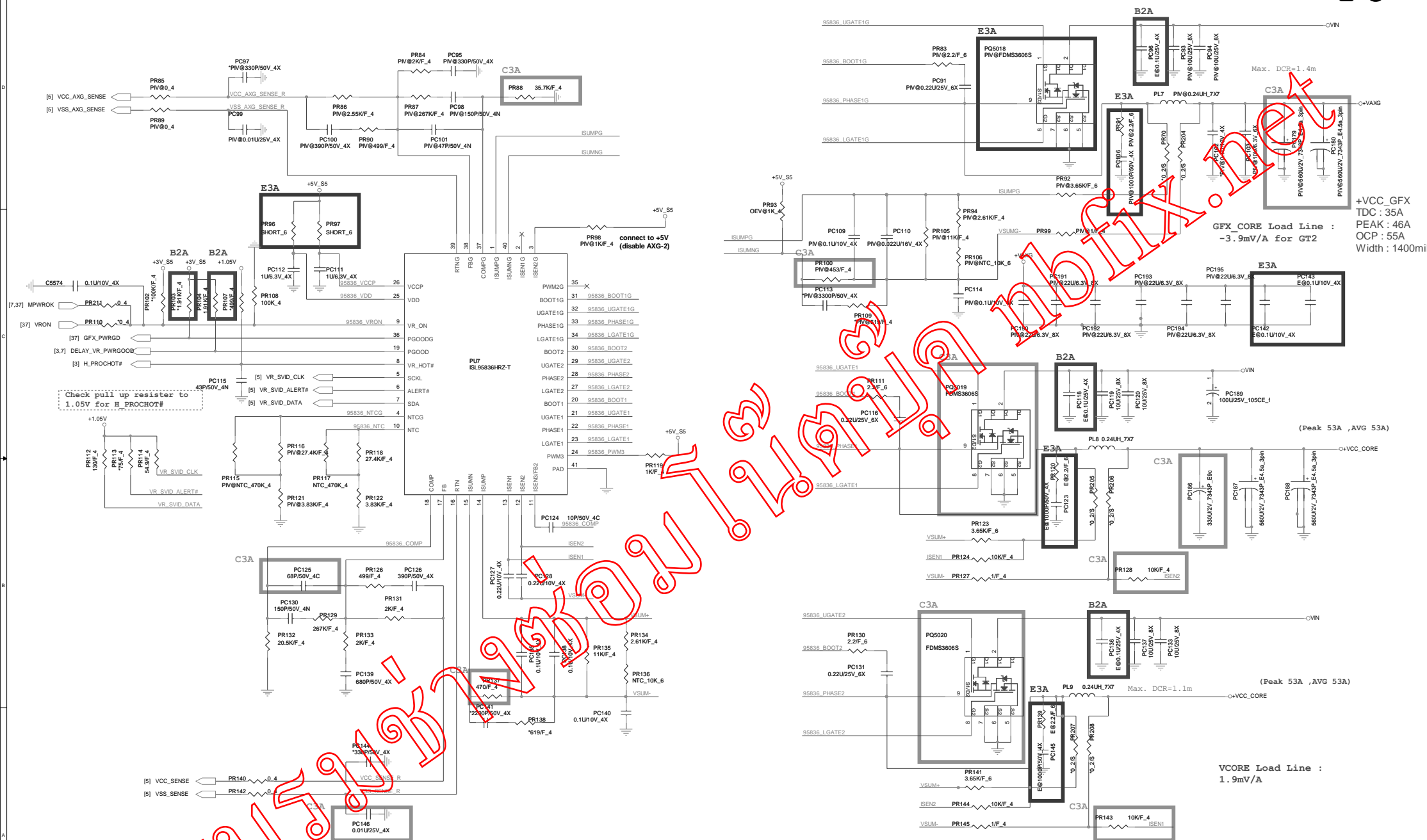
P5



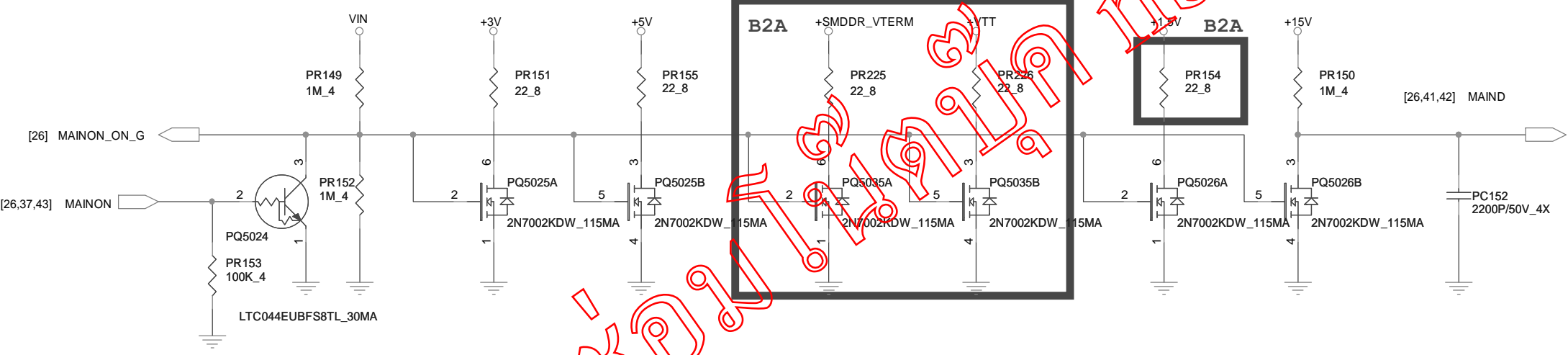
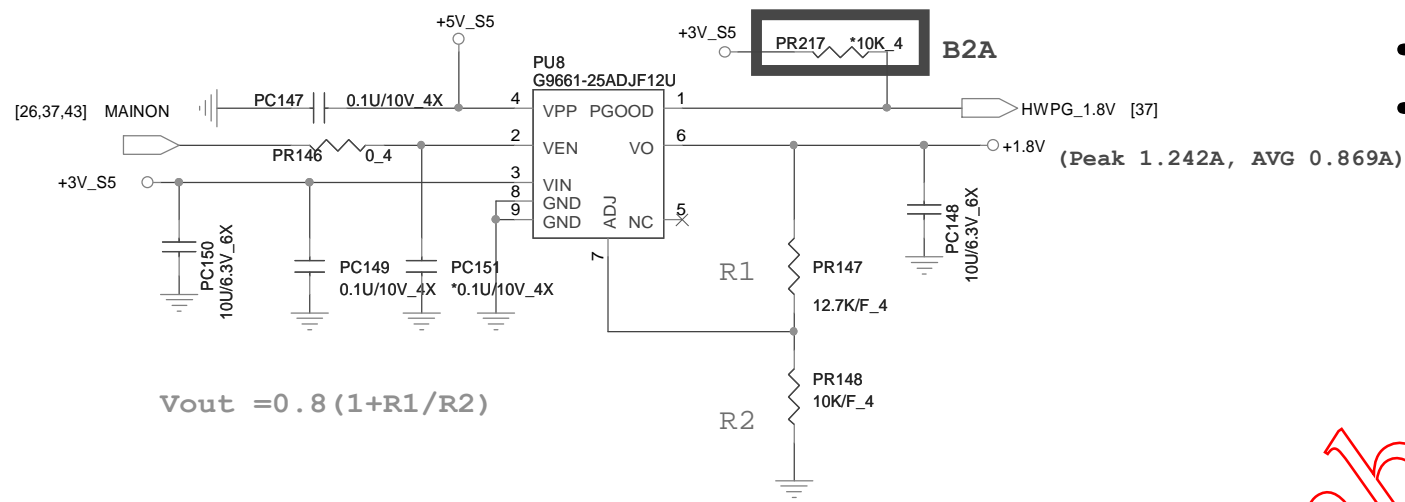
*0.8V FOR SV TYPE
*0.85V FOR LV/ULV TYPE

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PROJECT : Chief River

| | | |
|-------|------------------------------|----------------|
| Size | Document Number | Rev |
| | +VCCSA(TI51461) | A1A |
| Date: | Wednesday, February 01, 2012 | Sheet 44 of 48 |



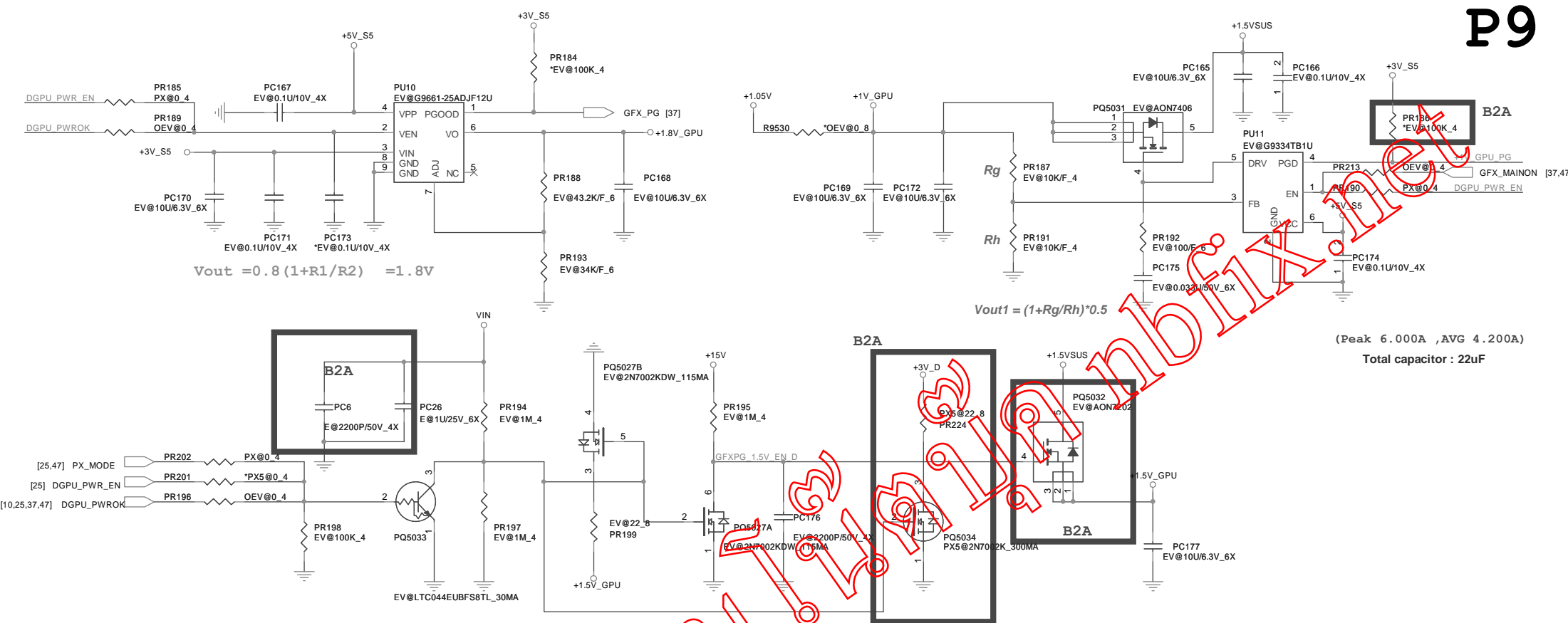
P7



Quanta Computer Inc.


PROJECT :Chief River

| | | |
|--|---|------------|
| Size | Document Number +1.8V/Discharge | Rev A1A |
| Date: Wednesday, February 01, 2012 Sheet 46 of 48 | | |



Power On Sequence

1. +3V_GPU connect +3V
2. PX_PWRGOOD Enable +VGPU_CORE
3. DGPU_PWROK Enable(Delay) +1.8V_GFX
4. DGPU_PWR_EN Enable(Delay) +1.5V_GFX
5. DGPU_PWR_EN Enable(Delay) +1V_GFX

| Model | REV | CHANGE LIST | MODEL | | | TE5 |
|-------------|-----|---|---------|--------------|-----------|--|
| | | | PAGE | FROM | To | |
| BY3/BY4 | 1A | <p>PAGE 8: Dual SPI ROM circuit modify for Win8.</p> <p>PAGE 8: C2010 change value to 15P/C2013 change value to 12P.</p> <p>PAGE 9: SMBUS/CLK REQ pin PU/PD resister pallerel resister to single resister.</p> <p>PAGE 10: R2185 change power to +3V.</p> <p>PAGE 10: R2160 MB_ID9 change to GPIO34.</p> <p>PAGE 16/28: d-GPU CRT Port change from Port6 to Port3.</p> <p>PAGE 17: C5045/C5049 change to 22P.</p> <p>PAGE 25: Del PX Mode PERST# BUF double drawing.</p> <p>PAGE 30: C5345/C5348 change value to 22P.</p> <p>PAGE 31: Add RN12/RN13 CHOCK for EMI test..</p> <p>PAGE 32: Add RN11/RN6 CHOCK for EMI test..</p> <p>PAGE 34: Stuff C5438/C5439/C5440/C5441 for EMI test.</p> <p>PAGE 35: Reserve LAN power circuit.</p> <p>PAGE 36: r9781/r9774/r9776/r9777/r9779/r9733 to 33ohm for EMI test.</p> <p>PAGE 37: Reserve GPIO for USB3.0 Power enable/LAN power/Inform VGA power status.</p> <p>PAGE 39: LED3 change to single white color for PRD1.0</p> <p>PAGE 39: Add C2136/C2137/C2138/C2118/C2129/C2135/C2142/C2144/C2143/C2139/C2140/C2141 for EMI test.</p> | 1 | 1A | | |
| | | | 2 | 1A | | |
| | | | 3 | 1A | | |
| | | | 4 | 1A | | |
| | | | 5 | 1A | | |
| | | | 6 | 1A | | |
| | | | 7 | 1A | | |
| | | | 8 | 1A | | |
| | | | 9 | 1A | | |
| | | | 10 | 1A | | |
| | | | 11 | 1A | | |
| | | | 12 | 1A | | |
| | | | 13 | 1A | | |
| | | | 14 | 1A | | |
| | | | 15 | 1A | | |
| | | | 16 | 1A | | |
| | | | 17 | 1A | | |
| | | | 18 | 1A | | |
| | | | 19 | 1A | | |
| | | | 20 | 1A | | |
| | | | 21 | 1A | | |
| | | | 22 | 1A | | |
| | | | 23 | 1A | | |
| | | | 24 | 1A | | |
| | | | 25 | 1A | | |
| | | | 26 | 1A | | |
| | | | 27 | 1A | | |
| | | | 28 | 1A | | |
| | | | 29 | 1A | | |
| | | | 30 | 1A | | |
| DOC NO. 204 | | PROJECT MODEL : | BY3,BY4 | APPROVED BY: | DATE: |  Quanta Computer Inc. PROJECT : BY3,BY4 Change list Date: Wednesday, February 01, 2012 Sheet 43 of 43 |
| | | PART NUMBER: | | DRAWING BY: | REVISION: | |