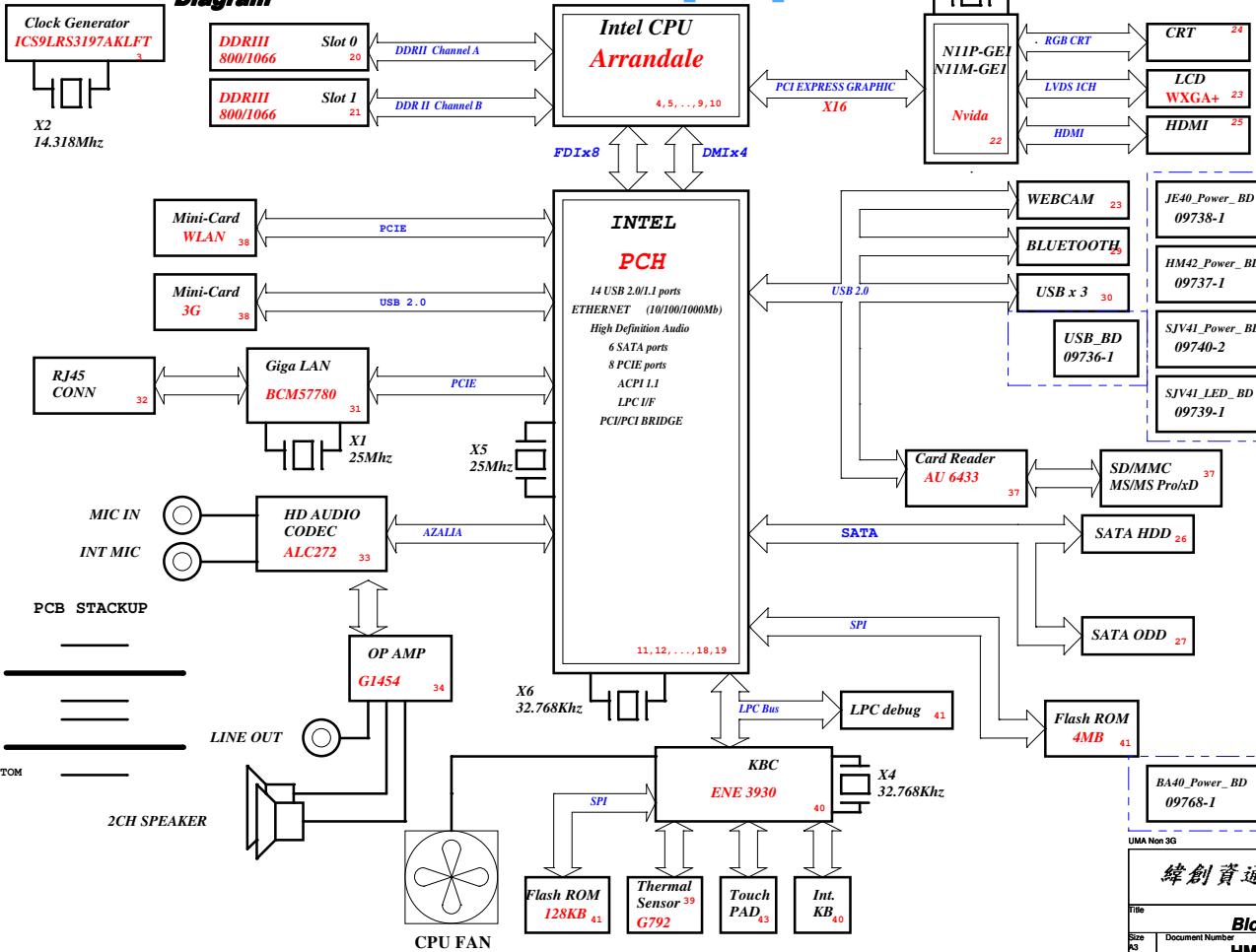


**JE40-CP/SJV41-CP/
HM42-CP /BA40-CP Block
Diagram**

PCB P/N : 48.4GW01-021
REVISION : -2 09320

Project code: 91.4GW01.001 (HM42-CP)
91.4GY01.001 (JE40-CP)
91.4GZ01.001 (SVJ41-CP)
91.4JD01.001 (BA40-CP)



SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
49	
SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3
50	
SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTF 1D05V_S0
51	
SYSTEM DC/DC RT9025	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0
52	
SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
55	
SYSTEM DC/DC TPS5161	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
47, 48	
CPU DC/DC ISL62882C	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
47, 48	
CHARGER ISL88731C	
INPUTS	OUTPUTS
DCBATOUT	BT+
53	

UMA Non 3G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 301, Taiwan, R.O.C.

Block Diagram

HM42-CP

File: _____
Size: _____
Date: Monday, March 01, 2010 Sheet 1 of 72

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
WC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in affect.
RDA_SDO	Weak internal pull-down. Do not pull high.
RDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[5]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[6]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ESI) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCIE Routing

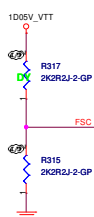
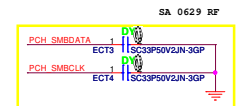
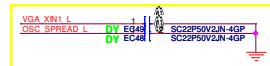
LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1 (HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Table of Content
Size A3	Document Number HM42-CP Rev -2
Date: Monday, March 01, 2010	Sheet 2 of 72



1130 -SC

320V 50

RN32
SRN10KJ-5-GP

CPU_STOP#

PCH_SMBDATA
EC9

PCH_SMBCLK
EC14

CLK_EN

1016 -SA

Q18

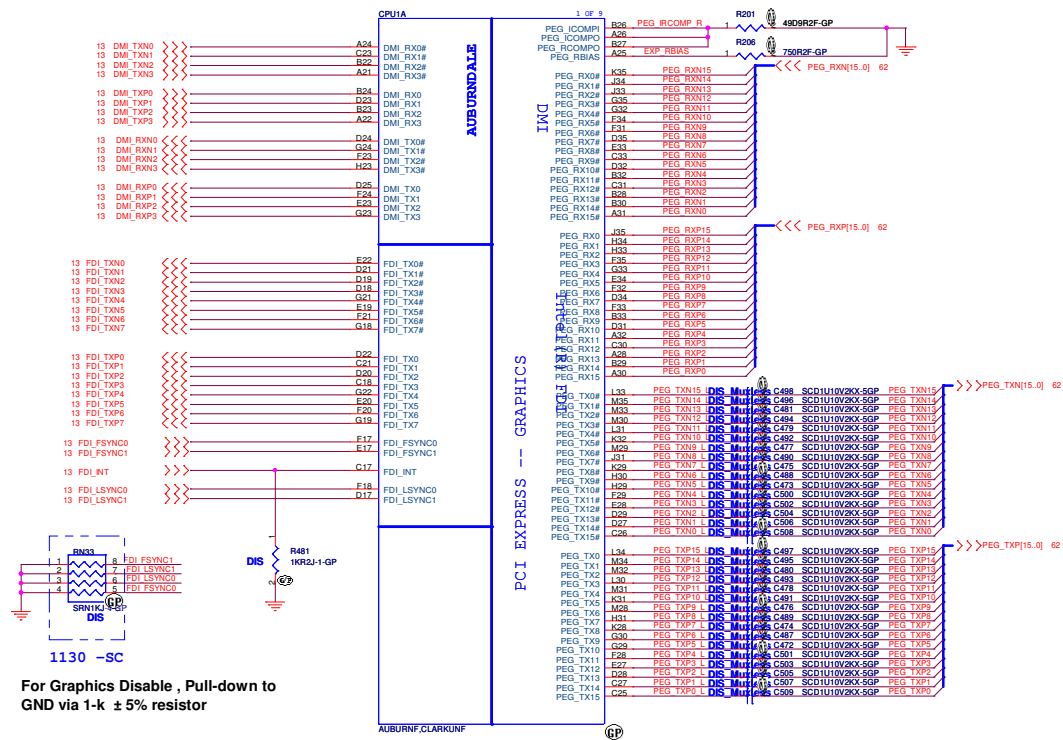
2N7002E-1-GP

84.2N702.E31

2ND = 84.2N702.E31

<<< VP_CLKEN# 47

UMA			
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Clock Generator			
Size K3	Document Number	Rev	
HM42-CP		-2	
Date:	Monday, March 01, 2010	Sheet	3 of 72



For Graphics Disable , Pull-down to GND via 1-k \pm 5% resistor

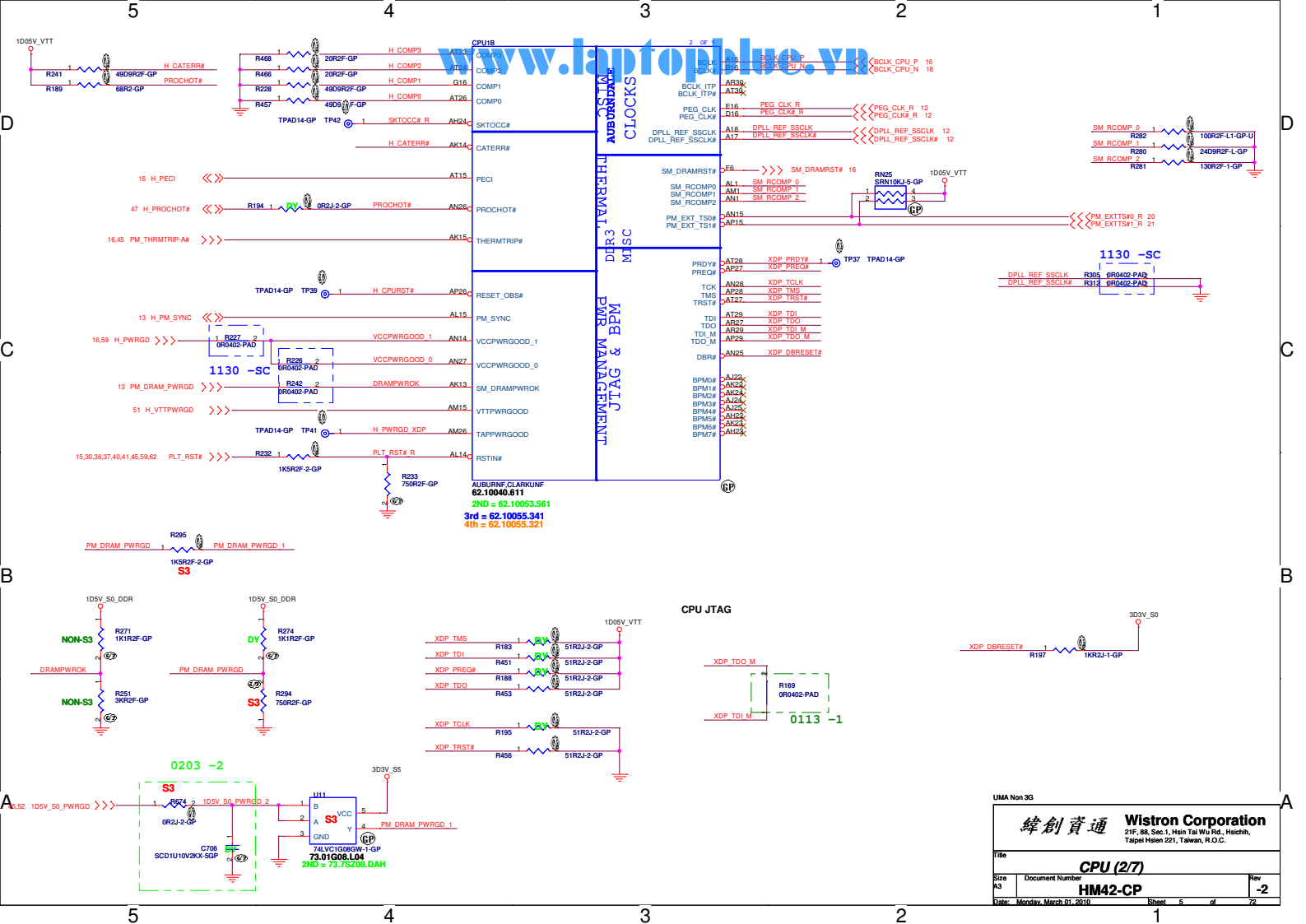
62.10040 611
2ND = 62.10053.561
3RD = 62.10055.341
4th = 62.10055.321

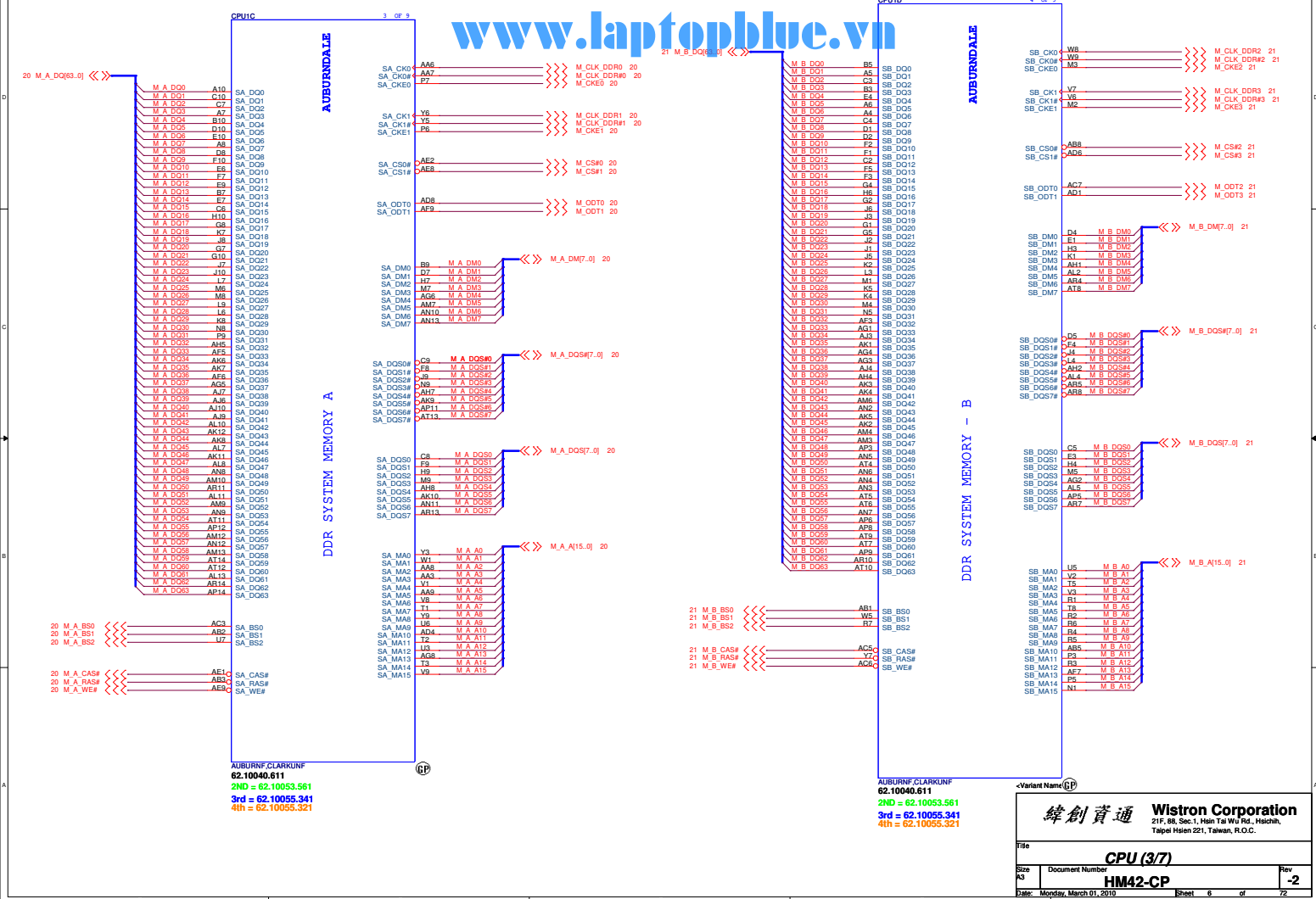
lab stuff 2nd,3rd and 4 th in BOM
Eng add 1st source(62.10040.611)
Eng do not stuff 4 th in BOM
because 4 th have been purge ,so stuff 1st in BOM
but CE said, 4th need stuff in PD if not any comp

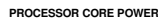
0113 -1

Del 3rd 62.10055.341 and 4th 62.10055.321
3rd and 4th have been purged
CE will confirm SQM if it can add BOM
CE will release EC to add to BOM

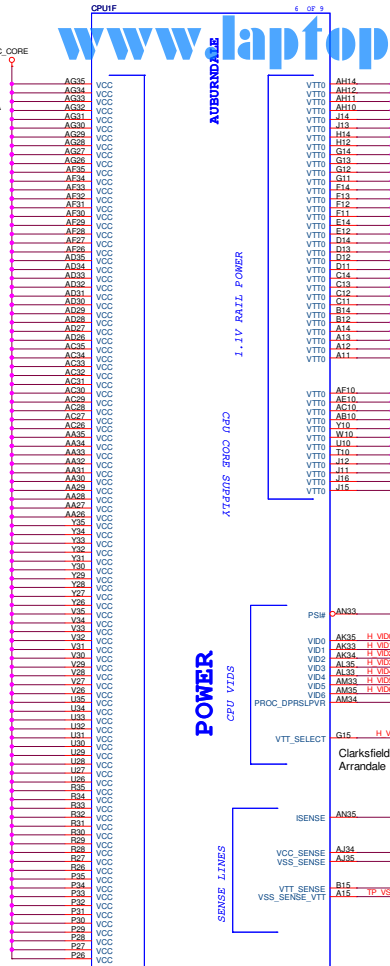
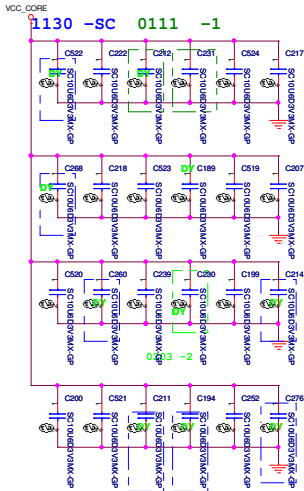
 緯創資通		Wistron Corporation 21F, B8, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (1/7)			
Size A3	Document Number		Rev
	HM42-CP		-2
Date: Monday, March 01, 2010		Sheet 4 of	72







48A



1130 -SC

1130 -SC

1130 -SC

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



PE

1

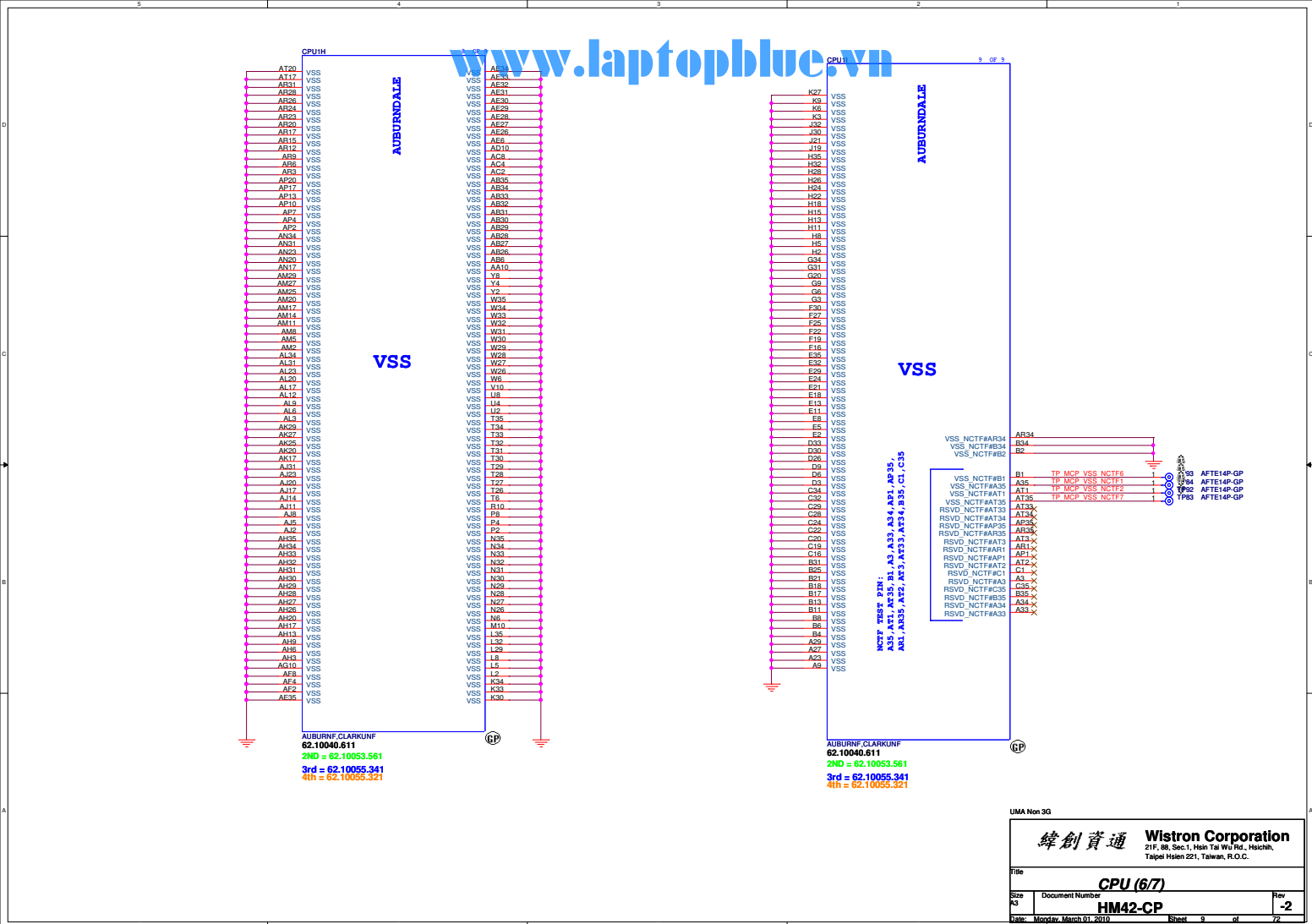
5.34

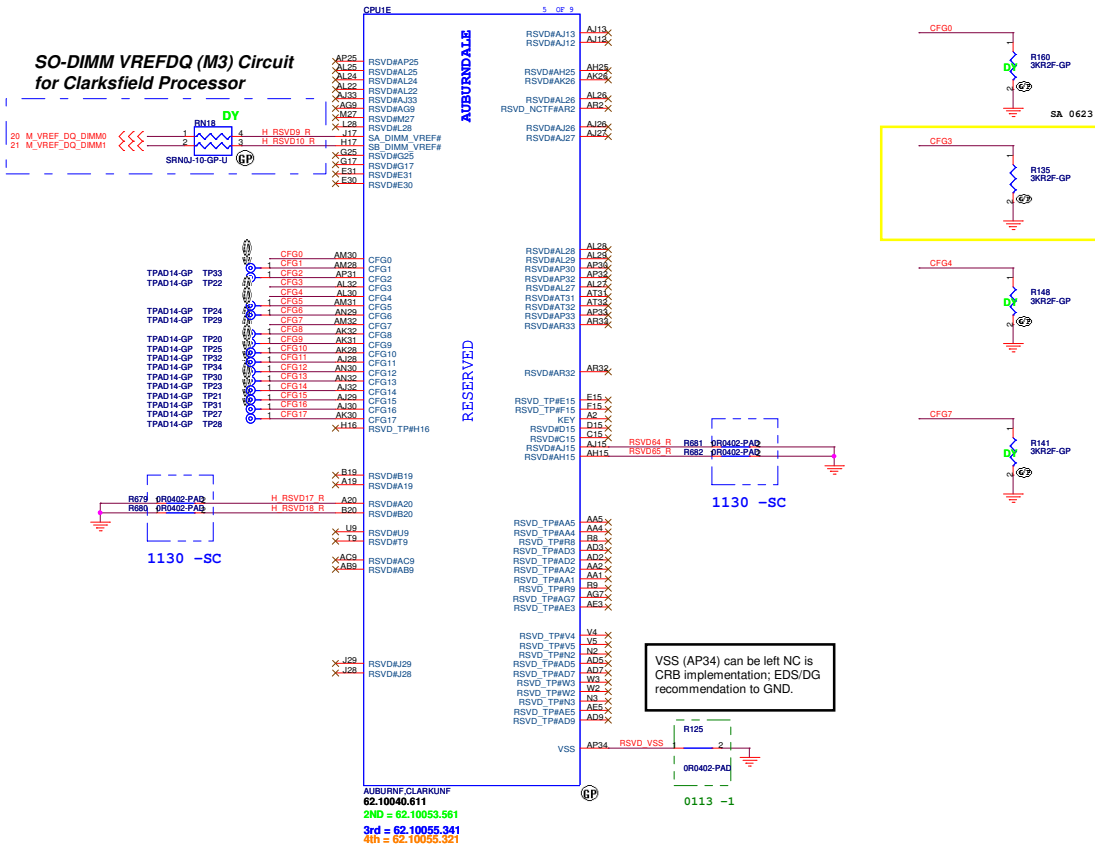
<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU (4/7)			
Size	Document Number	Rev	
Custom	HM42-CP	-2	
Date:	Monday, March 01, 2010	Sheet	7 of 72



SO-DIMM VREFDQ (M3) Circuit
for Clarkfield Processor

Processor Strapping

PCI-Express Configuration Select	
CFG0	1: Single PEG (Default) 0: Bifurcation enabled

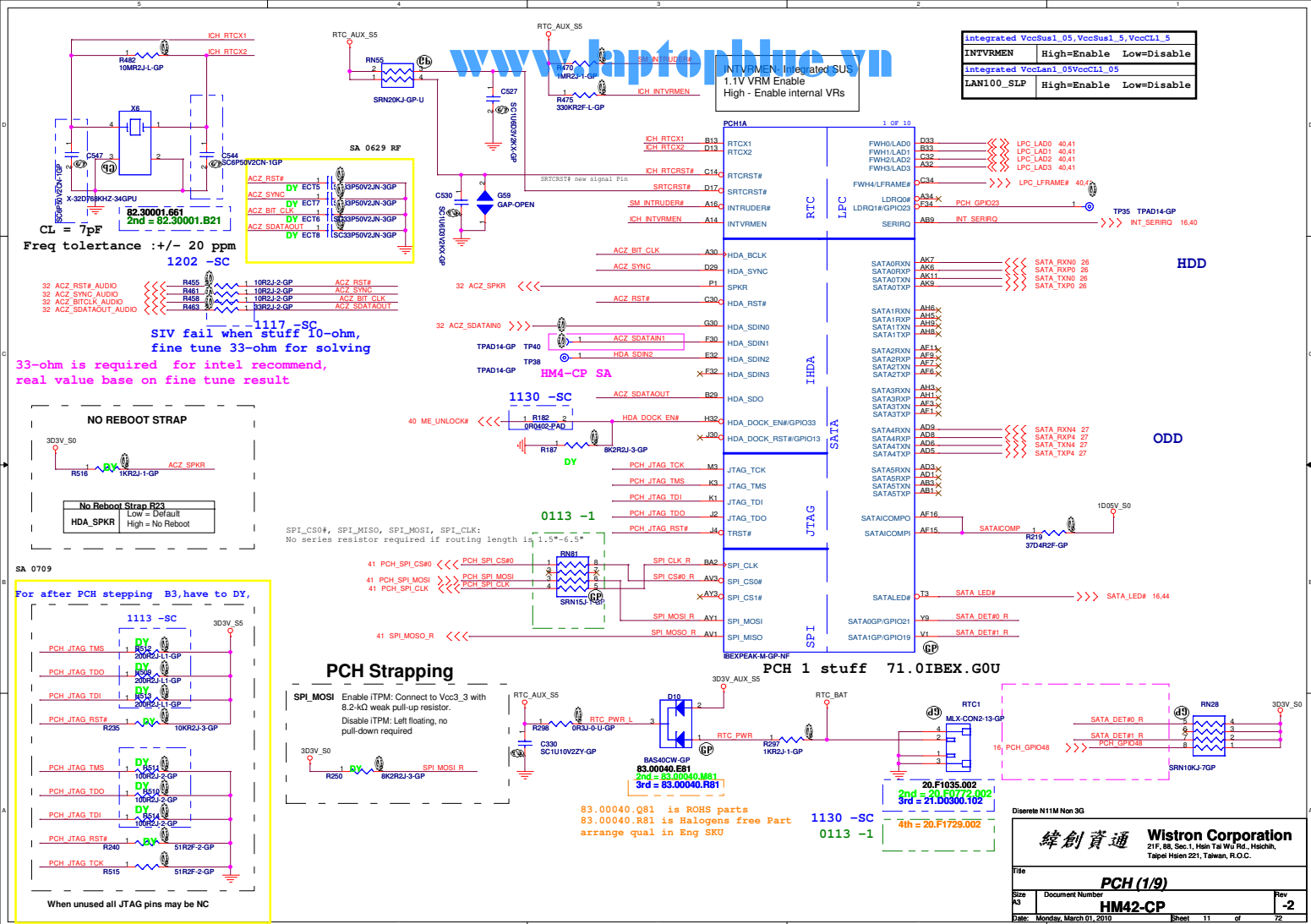
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1: Normal Operation (Default) 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

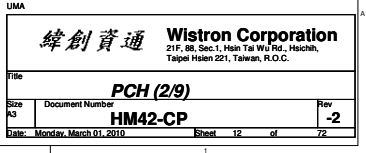
CFG4 - Display Port Presence	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0: Enabled; An external Display Port device is connected to the Embedded Display Port

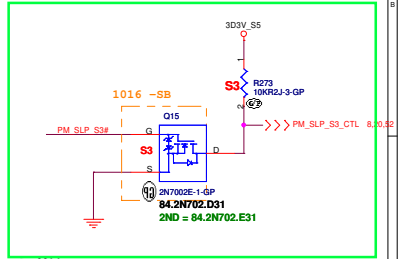
CFG7 (Reserved) - Temporarily used for early Clarkfield samples.	
CFG7	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common MB design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

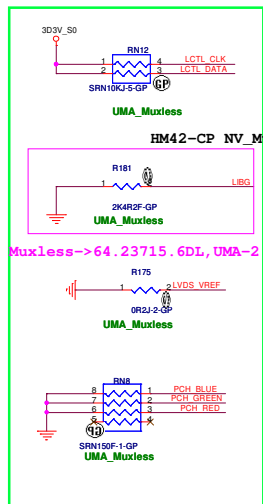
VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

0113 -1

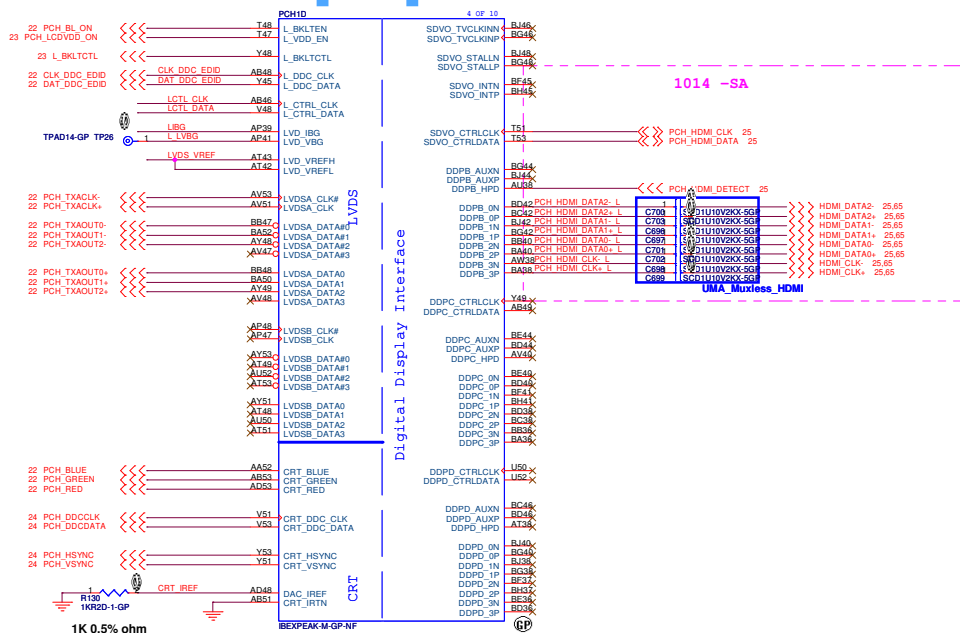








SB 0811

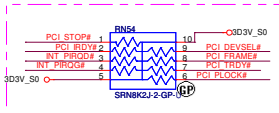


UMA Non 3G

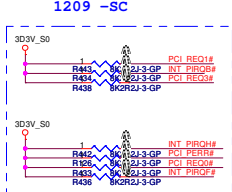
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

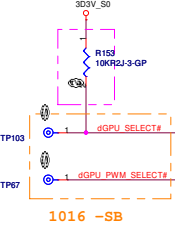
Title			PCH (4/9)
Size	Document Number	Rev	-2
Date: Monday, March 01, 2010			Sheet 14 of 72



HM42 NV Muxless SA 0925



HM42 NV Muxless SA 0924

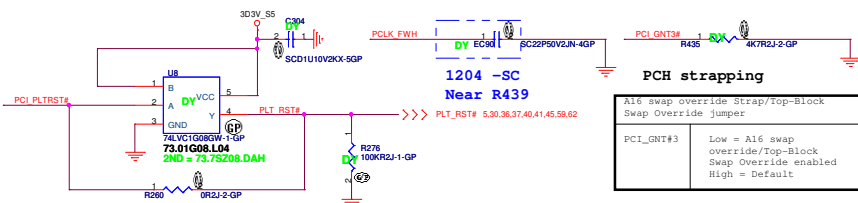


PCH strapping

BOOT BIOS Strap		
GNT#0	GNT#1	BOOT BIOS Location
0	0	LPC
1	0	Reserved
Floating	0	PCI
Floating	Floating	SPI(Default)

PCI_GNT#1	Default
1	Default
0	Configures DMI for ESI compatible operation (Not for Mobile platform)

41 CLK_FWH
12 CLK_PCI_FB
40 CLK_PCI_KBC



PCH strapping

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

PCH strapping

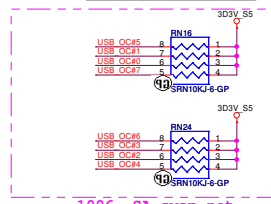
NV_CLE	DMI termination voltage
floating	internal pull-up

NV_ALE	Enable Anti-Theft Tech
floating	Disable (internal pull-down)

NV_CLE	Set to Vss when low. Set to Vcc when high.
--------	---

USB

Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1 (WLAN)
4	WECAM
5	NC
6	NC
7	NC
8	3G SIM Card
9	USB1 (HS)
10	NC
11	Blue Tooth
12	MINIC2 (3G)
13	Cardreader

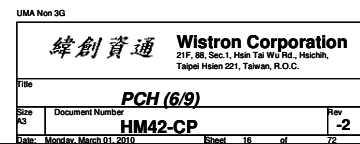


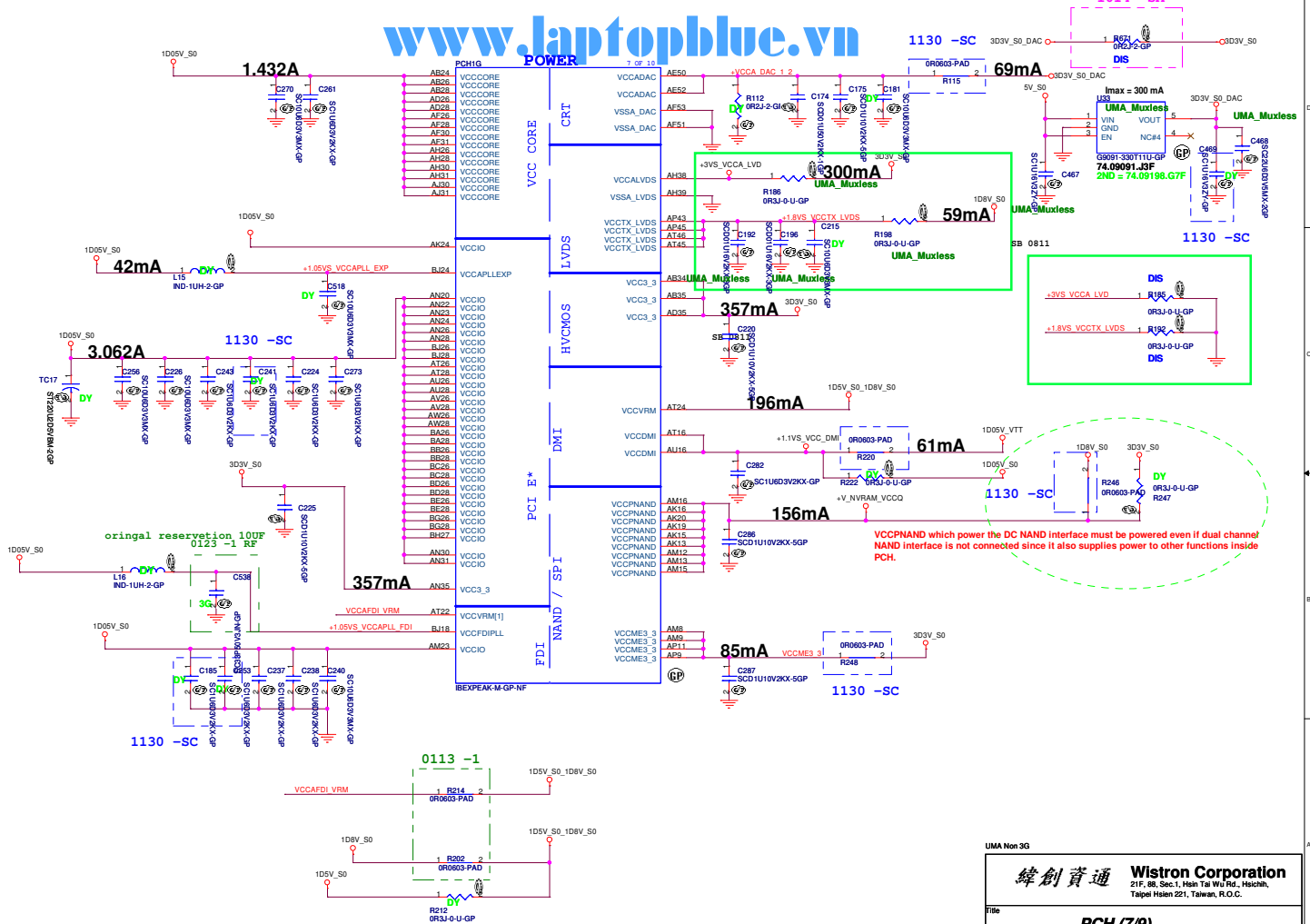
UMA Non 3G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 301, Taiwan, R.O.C.

PCH (5/9)		
HM42-CP		
Date: Monday, March 01, 2010	Sheet 15 of 72	Rev -2

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

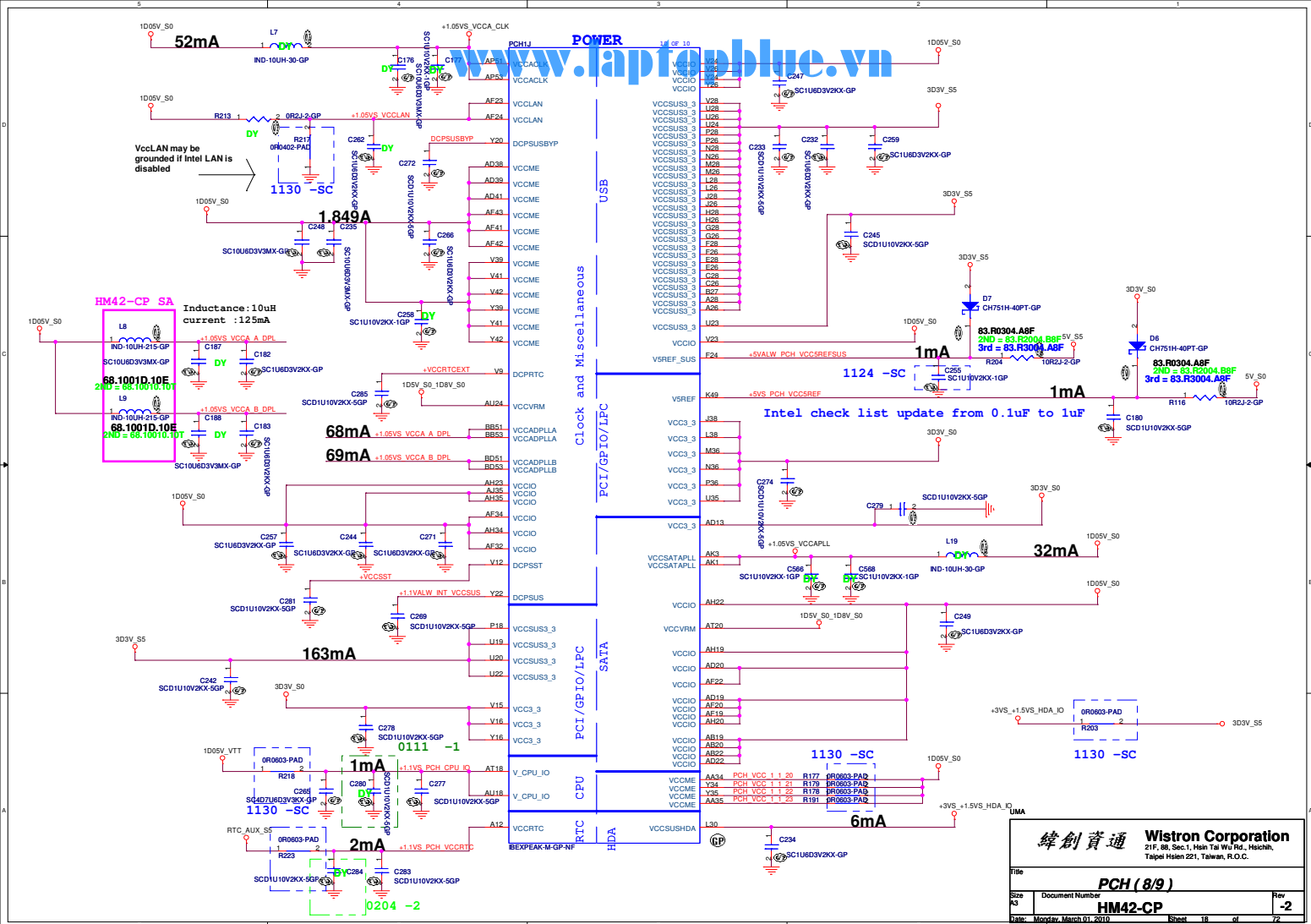




UMA Non 3G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

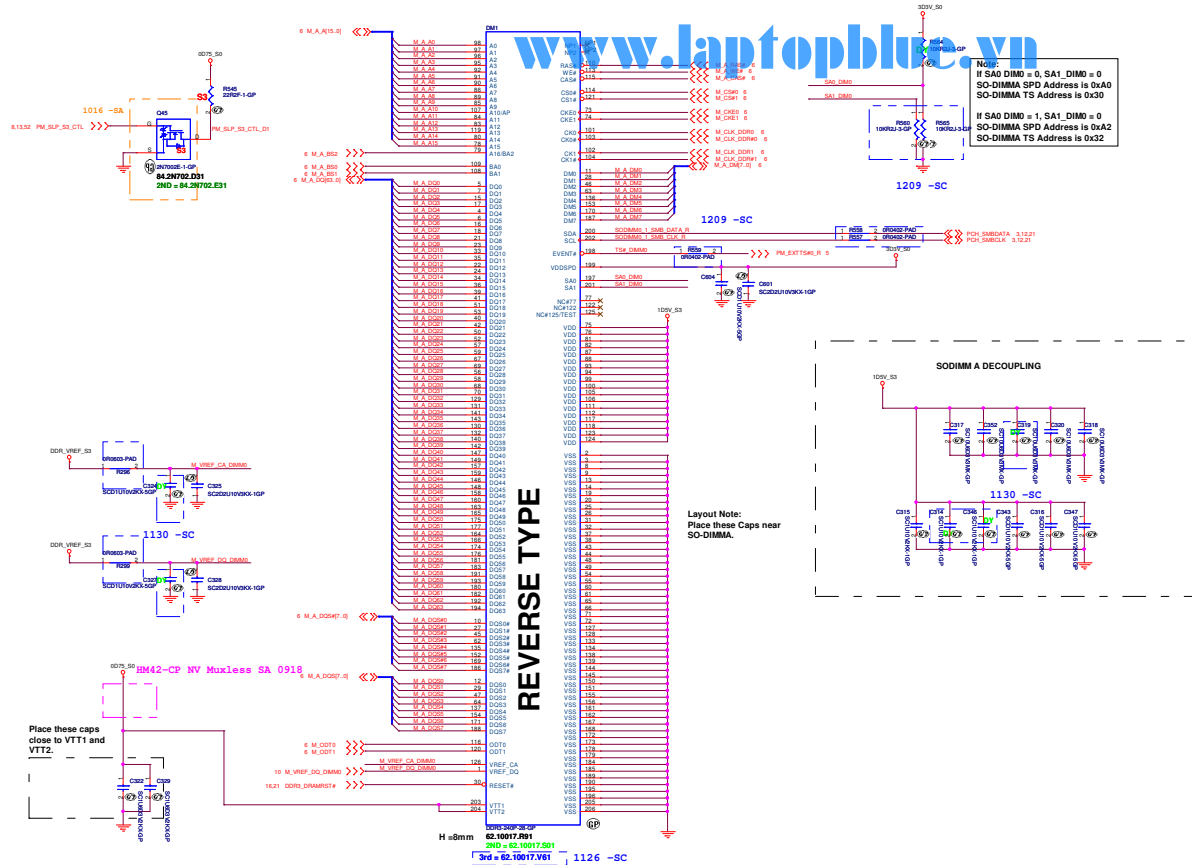
Title			
PCH (7/9)			
Size A3	Document Number		Rev
	HM42-CP		-2
Date:	Monday, March 01, 2010	Sheet	17 of 72





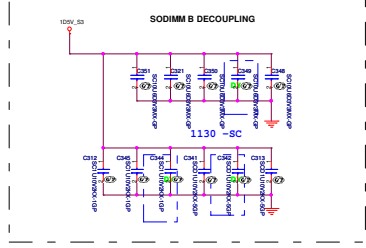
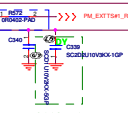
-Variant Name-

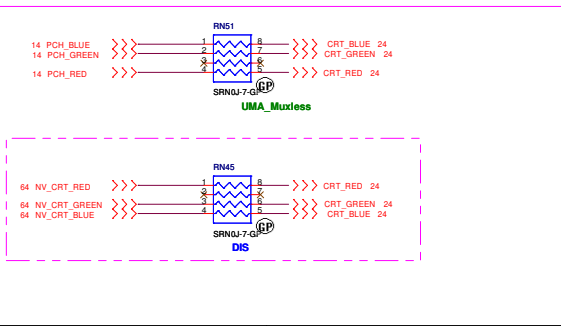
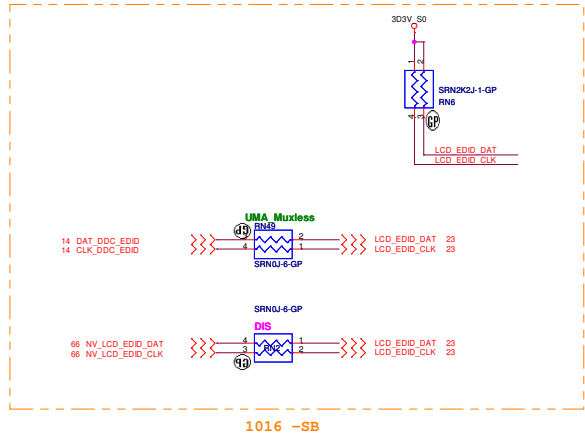
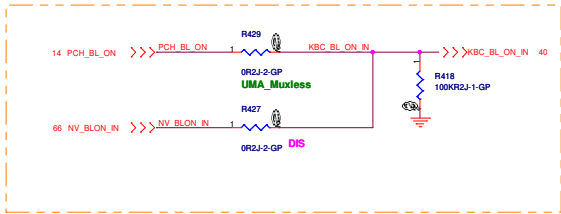
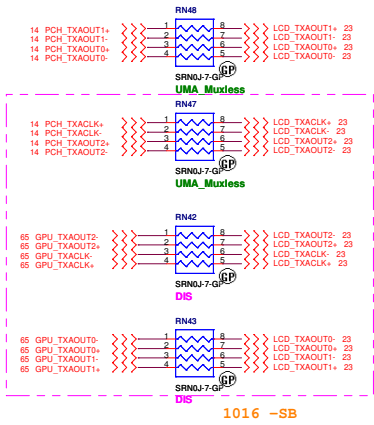
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
PCH (9/9)	
Size	Document Number
R3	HM42-CP
Date: Monday, March 01, 2010	Sheet 19 of 72





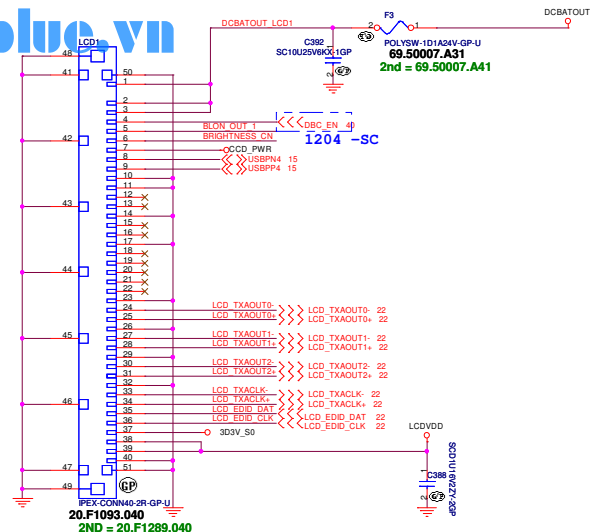
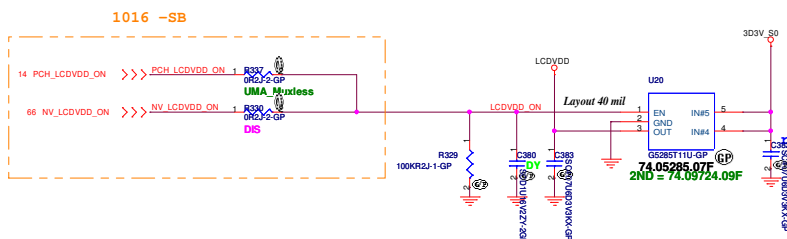
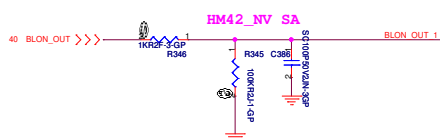
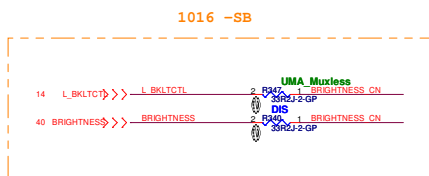
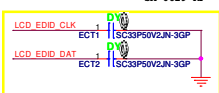
Note:
SO-DIMM SPD Address is 0xA4
SO-DIMM TS Address is 0x34
SO-DIMM is placed farther from the Processor than SO-DIMMA





UMA		Wistron Corporation	
緯創資通		21F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.	
File		Function	
Size	Document Number	Rev	
A3	HM42-GP	-2	
Date	Monday, March 01, 2010	Sheet	22 of 72

www.laptopblue.vn



```
1005 -SA
define same as SJM50-PU,can use SJM50 Cable
```

0128 -1

32 INT_MNC1 <<<

69.80007.021

D1
MLV50402M04-GP

20.1561002

2ND = 20.15612.002

3rd = 20.15686.002

AMC11

10k

100p

100k


100p

1130 -SC

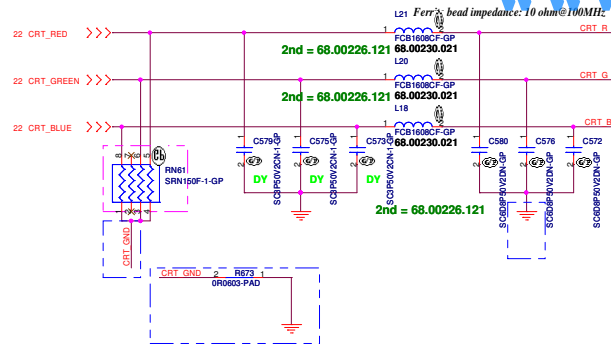
Pin 1- >right side
20.1561002 Pin1->left side
same as JV70-CP

09 -SC
t by EMI Aaron

Discrete N11M Non-3G

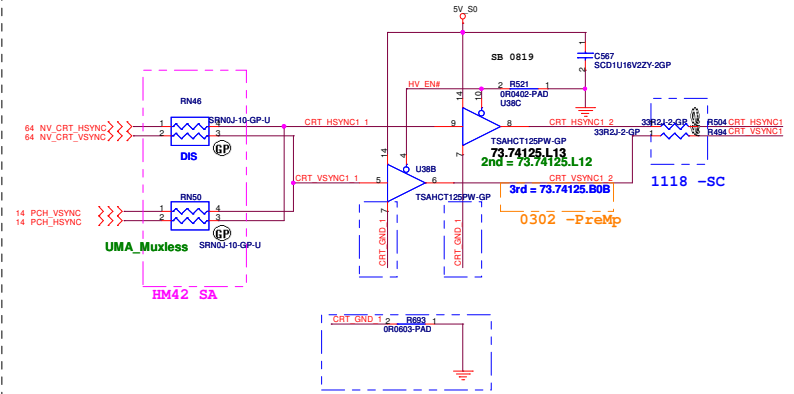
 緯創資通		Wistron Corporation 21F, 88, Sec. 1, Hsin Ya Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LCD CONN			
Size	Document Number	Rev	
		HM42-CP	
Date:	Tuesday, March 02, 2010	Sheet	23 of 72

Layout Note:
Place these resistors
close to the CRT-out
connector

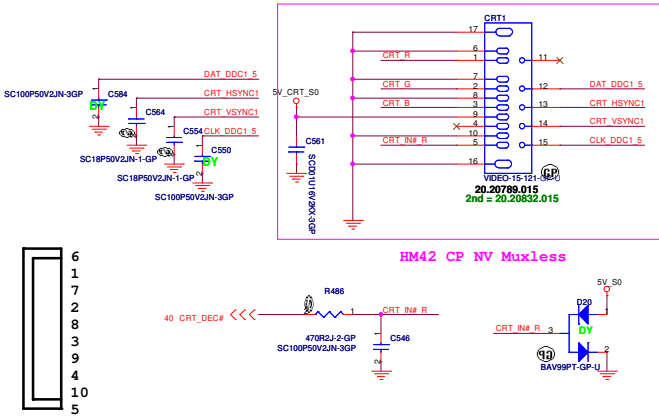


Layout Note:

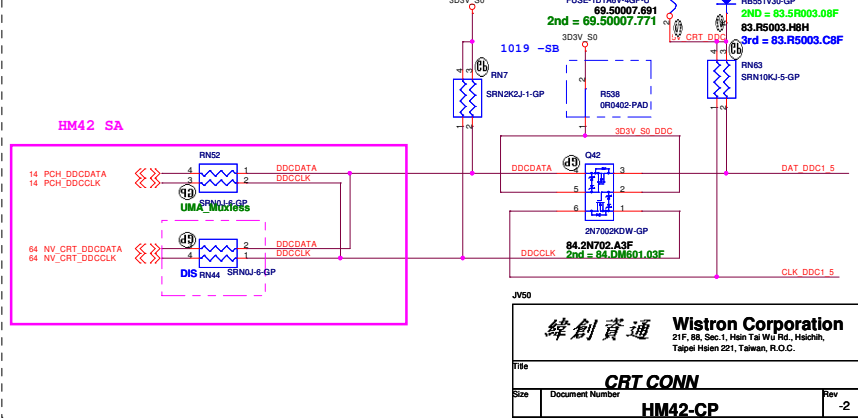
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift





IA Collector
www.laptopblue.vn



Sheet 26 of 72



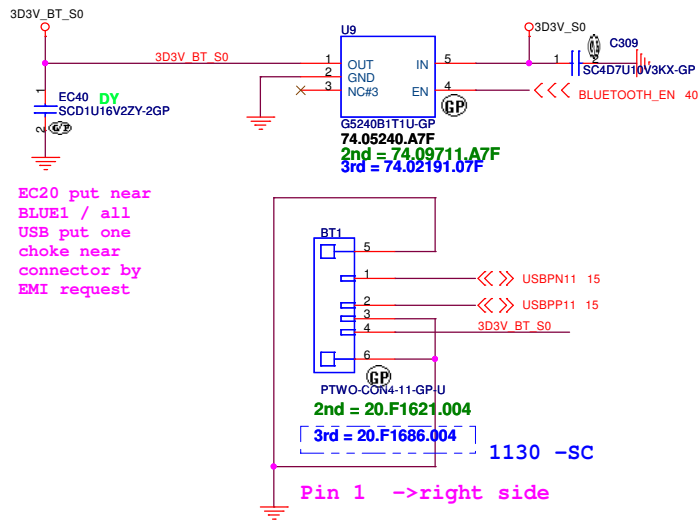
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ODD

Size	Document Number	Rev
	HM42-CP	-2
Date: Monday, March 01, 2010	Sheet 27 of 72	

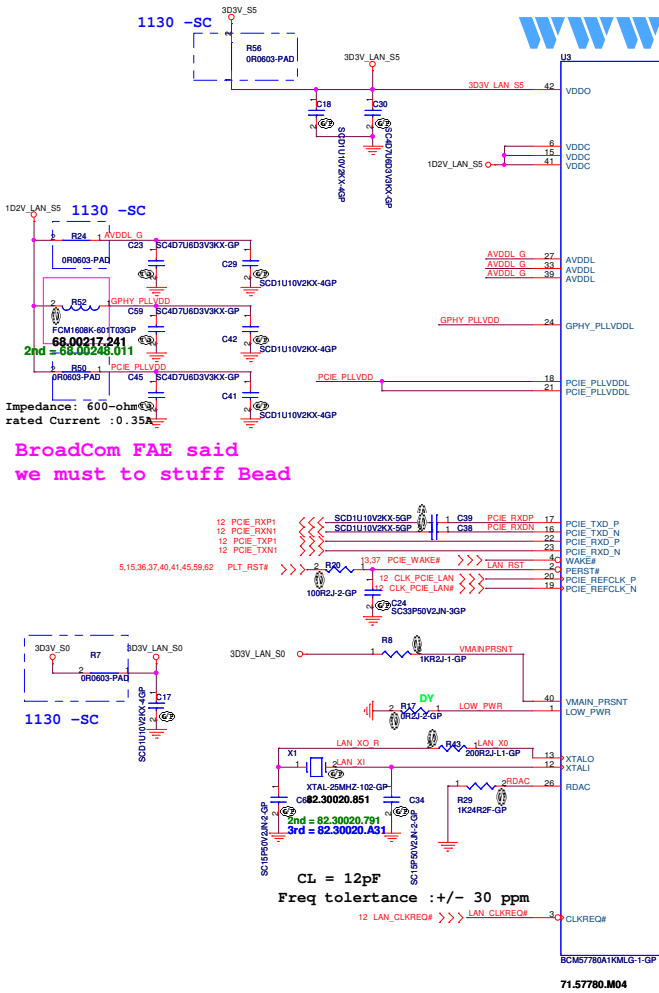
BLUETOOTH MODULE



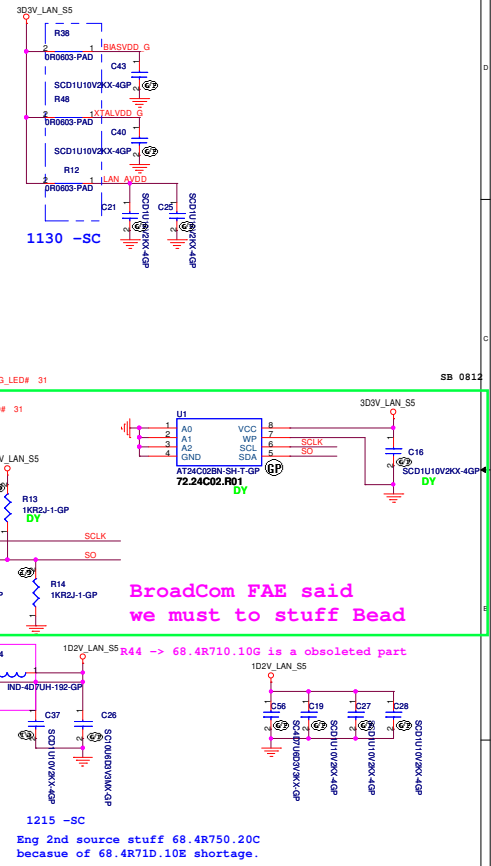
JV50

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BLUETOOTH			
Size	Document Number		Rev
	HM42-CP		-2
Date:	Monday, March 01, 2010	Sheet 28 of 72	

1130 -SC



3.3V LAN_SS



緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
File	BCM57780
Size	Document Number
A3	HM42-CP
Date: Monday, March 01, 2010	Sheet 30 of 72

- LAN Connector
www.laptopblue.vn

30 10M100M10Q_LED# >>> CONN_PWR#

30 LAN_ACT_LED# <<<

RM45

14 8 10 11 1 2 3 4 5 6 7 8 12 13 14

22.10177.C01
2ND=22.10177.BS1
3rd=22.10177.C21
4th=22.10177.BS3
5th=22.10177.H31

30V_S5

CONN_PWR#

SB 1208

EC50 EC53

SC10P50V2A3GP

SC10P50V2A3GP

30V

HM42 CP NV Muxless SA

MCT1 MCT2 MCT3 MCT4

1N39 SRN75J-1 GP

SC10P20V80GP

30V

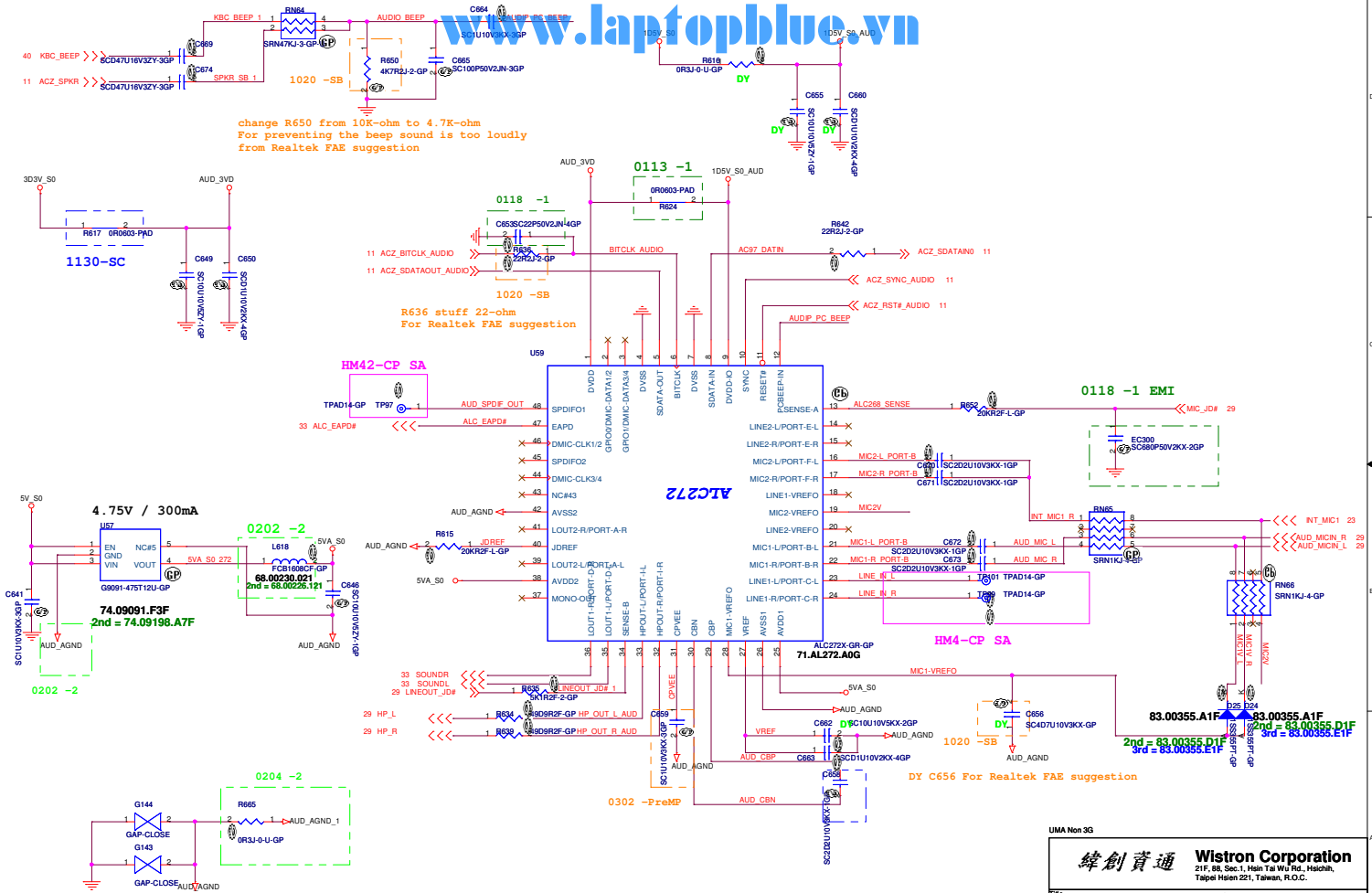
Discrete N11M Non 3G

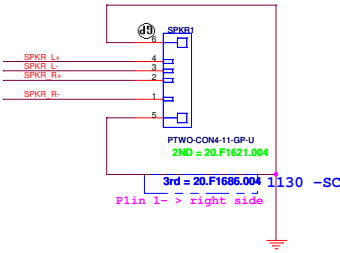
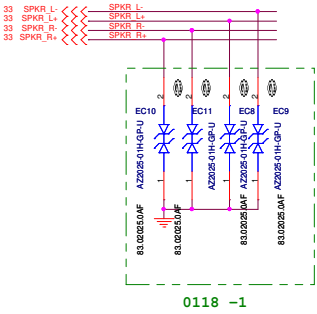
2 LED LAYOUT

NODE	COLOR	
12(+)	13(-)	YELLOW

3 LED LAYOUT

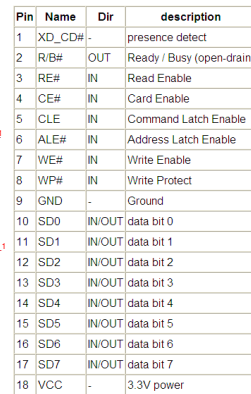
NODE	COLOR	
9(-)	10(+)	GREEN
11(-)	10(+)	ORANGE






JV50

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
Resrve MDC		
Size	Document Number	Rev
	HM42-CP	-2
Date: Monday, March 01, 2010		
Sheet 35 of 72		



Pin	Pin Name	Description
1	VSS	Vss
2	BS	Bus state signal
3	DATA1	Data1 Parallel / NC Serial
4	SDIO/DATA0	Data0 Parallel / Data Serial
5	DATA2	Data2 Parallel / NC Serial
6	INS	Stick detect (connected to VSS)
7	DATA3	Data3 Parallel / NC Serial
8	SCLK	Clock signal
9	VCC	Vcc (2.7V - 3.6V)
10	VSS	Vss

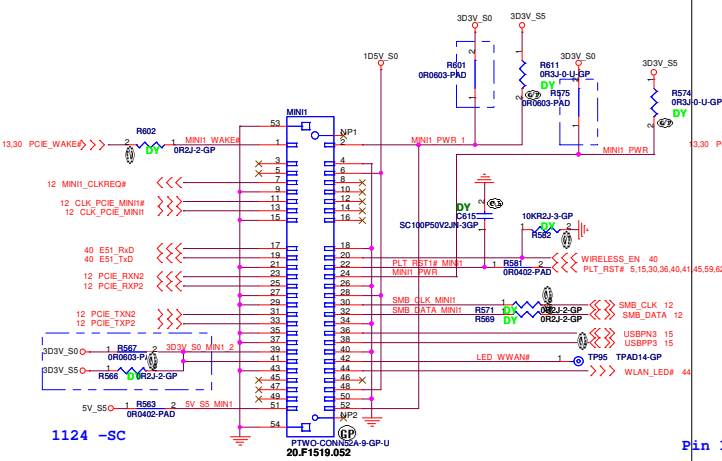
Discrete N11M Non 30

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Cardreader		
Size	Document Number	Rev
	HM42-CP	-2
Date:	Monday, March 01, 2010	Sheet 36 of 72

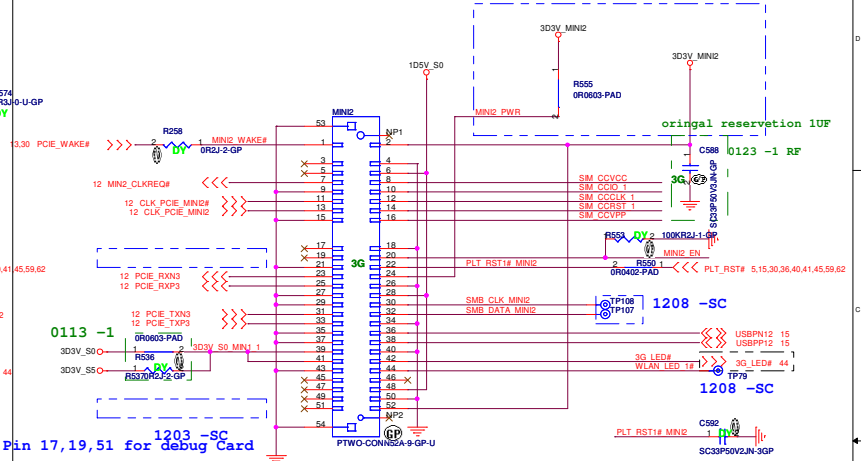
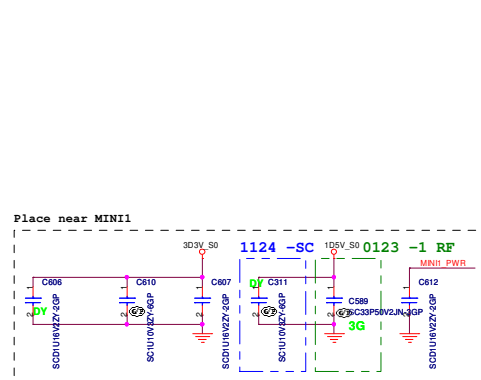
Mini Card Connector(WLAN) Support debug-card

www.laptopblue.vn

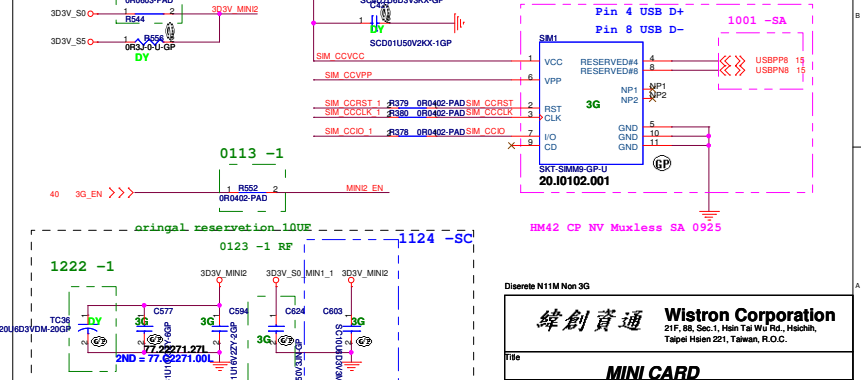
Mini Card Connector(Robson2 and 3G)

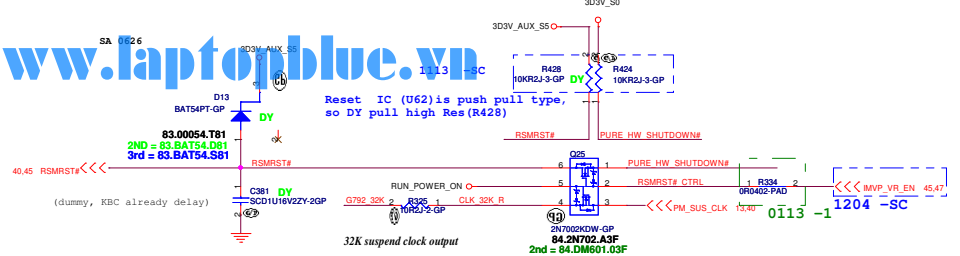


Place near MINI1



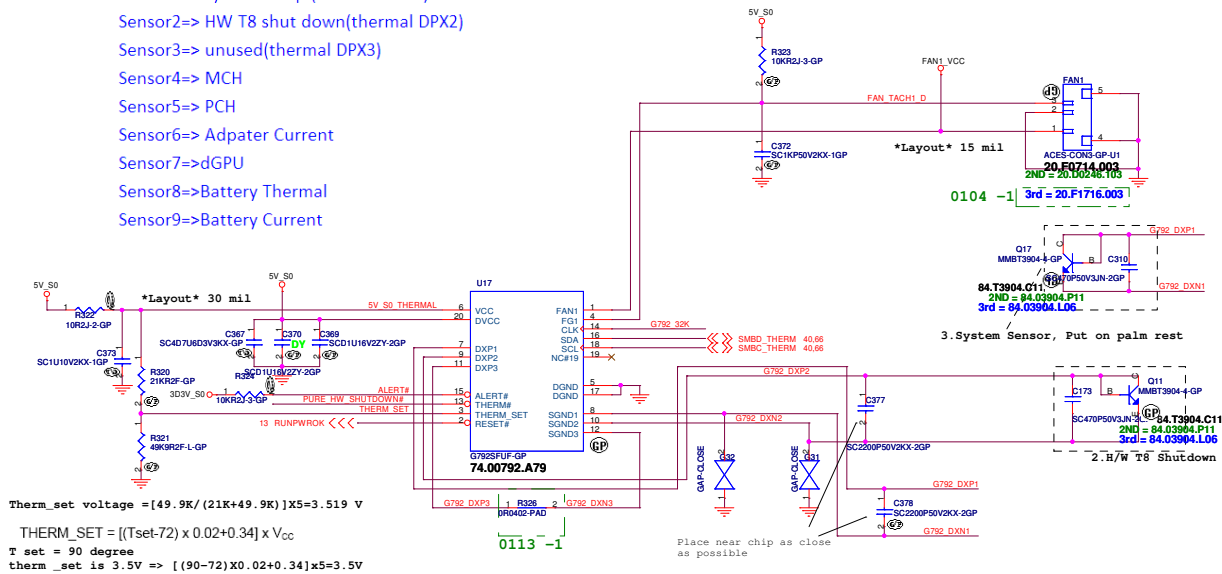
Pin 17,19,51 for debug Card





Thermal Get define

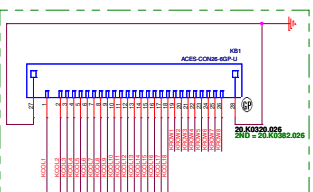
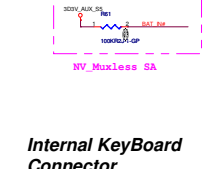
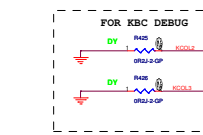
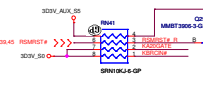
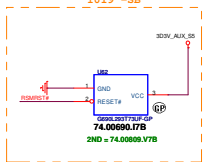
- Sensor0 => CPU
- Sensor1=> system temp (thermal DPX1)
- Sensor2=> HW T8 shut down(thermal DPX2)
- Sensor3=> unused(thermal DPX3)
- Sensor4=> MCH
- Sensor5=> PCH
- Sensor6=> Adpater Current
- Sensor7=>dGPU
- Sensor8=>Battery Thermal
- Sensor9=>Battery Current


$$\text{Therm_set voltage} = [49.9\text{K} / (21\text{K} + 49.9\text{K})] \times 5 = 3.519 \text{ V}$$
$$\text{THERM_SET} = [(T_{\text{set}} - 72) \times 0.02 + 0.34] \times V_{\text{CC}}$$

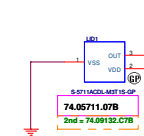
```
T set = 90 degree
therm_set is 3.5V => [(90-72)X0.02+0.34]x5=3.5V
```

```
DXP1: System Sensor
DXP2: H/W Setting(T8)
DXP3: do not use
```

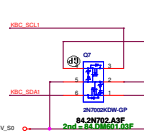
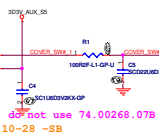
Prevent BIOS data loss solution
1019 -SB



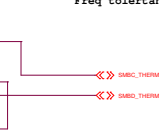
change connect to FPC (Same as Lab)
20.K0251.026 Pin 1 -> left side
20.K0320.026 Pin 1 -> right side(use in lab stage)
so swap net



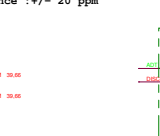
Cover Up Switch



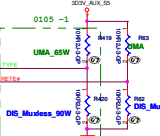
2nd = 82.3001.661
82.3001.661
CL = 7pF
Freq tolerance : +/- 20 ppm



2nd = 82.3001.661
82.3001.661
CL = 7pF
Freq tolerance : +/- 20 ppm



2nd = 82.3001.661
82.3001.661
CL = 7pF
Freq tolerance : +/- 20 ppm



2nd = 82.3001.661
82.3001.661
CL = 7pF
Freq tolerance : +/- 20 ppm

PCB Version AD (Pin)	Pull-Up Resistor	Pull-Down Resistor	Value	Pin
5A	10K	10K	33V	
5B	10K	10K	23V	
5C	10K	10K	23V	
5D	10K	10K	23V	
5E	10K	10K	23V	
5F	10K	10K	23V	
5G	10K	10K	23V	
5H	10K	10K	23V	
5I	10K	10K	23V	
5J	10K	10K	23V	
5K	10K	10K	23V	
5L	10K	10K	23V	
5M	10K	10K	23V	
5N	10K	10K	23V	
5O	10K	10K	23V	
5P	10K	10K	23V	
5Q	10K	10K	23V	
5R	10K	10K	23V	
5S	10K	10K	23V	
5T	10K	10K	23V	
5U	10K	10K	23V	
5V	10K	10K	23V	
5W	10K	10K	23V	
5X	10K	10K	23V	
5Y	10K	10K	23V	
5Z	10K	10K	23V	

Character 10 1M 10m 100m
Wistron Corporation
2/F, 88, Sec. 1, Hsin-Tai Rd., Hsinchu, Taiwan 30001, Taiwan, R.O.C.
KBC KB930
Rev. 1
Date: 10/10/2010, March 10, 2010
Page 1 of 2

for ENE FAE suggest, SPICS# is push-pull pin,
don't need to pull high

-SA 0930

base on FAE Kevin discuss with KBC

0203 -2

128KB

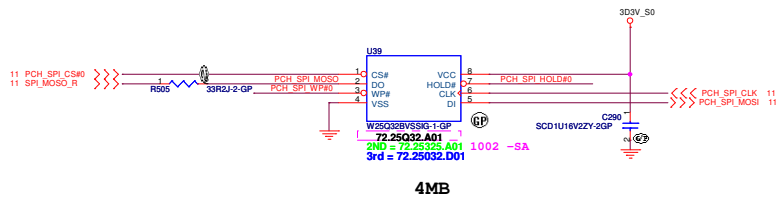
For TM jack suggestion
arrange to qual in PreMP
and do not use 72.25010.I01
I01 is 25nm N01 is 18nm
I01 is obsoleted parts

72.25105.A01
2nd = 72.25010.K01
3rd = 72.25010.N01
4th = 72.25010.J01

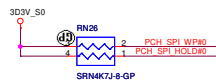
0304 -PreMP

close to SPI ROM

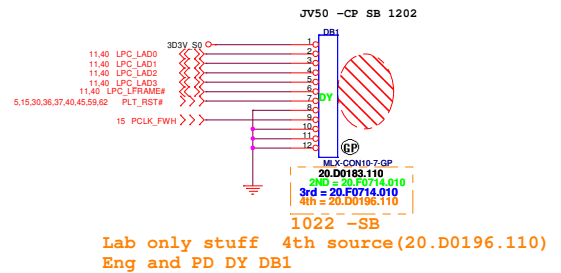
System BIOS Flash ROM



4MB



GOLDEN FINGER FOR DEBUG BOARD

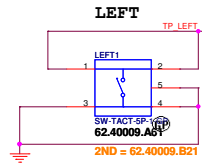
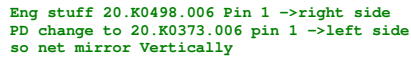


Lab only stuff 4th source (20.D0196.110)
Eng and PD DY DB1

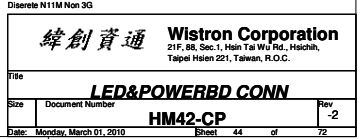
Discrete N11M

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

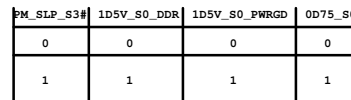
Title: BIOS
Size: Document Number: HM42-CP
Date: Wednesday, March 03, 2010 Sheet: 41 of 72 Rev: -2



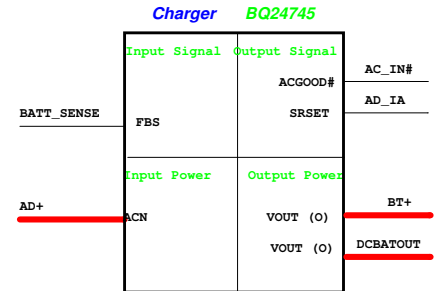
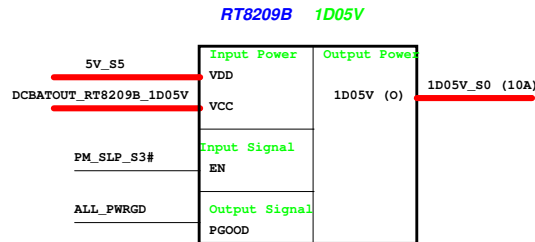
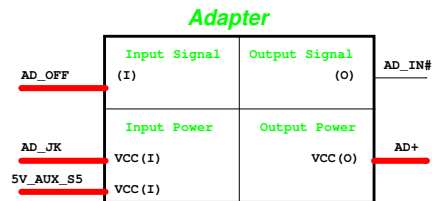
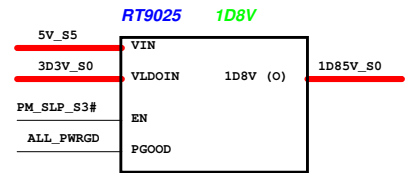
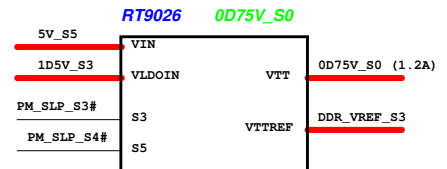
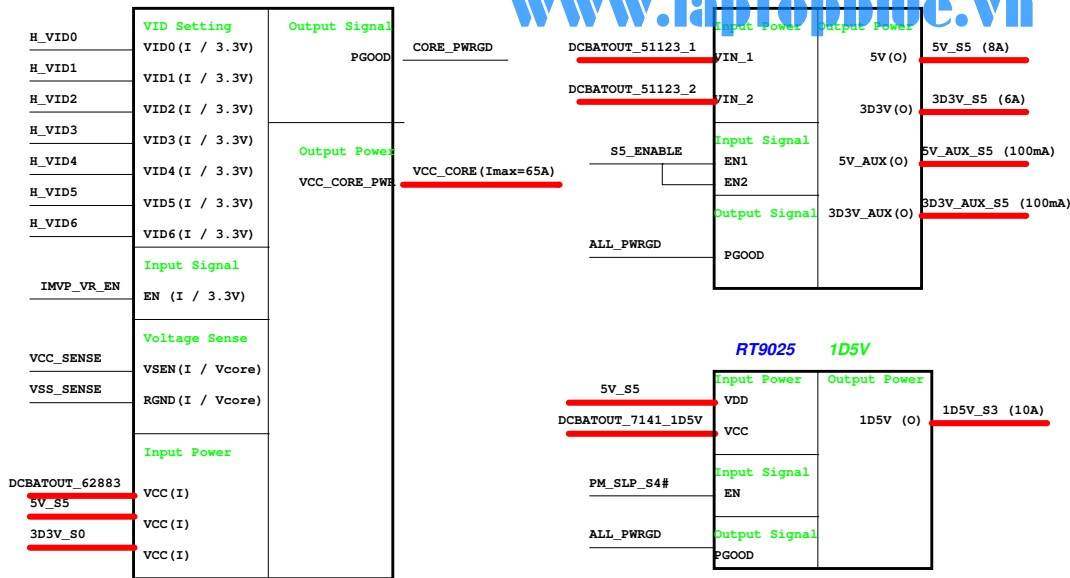
Power LED (Blue)

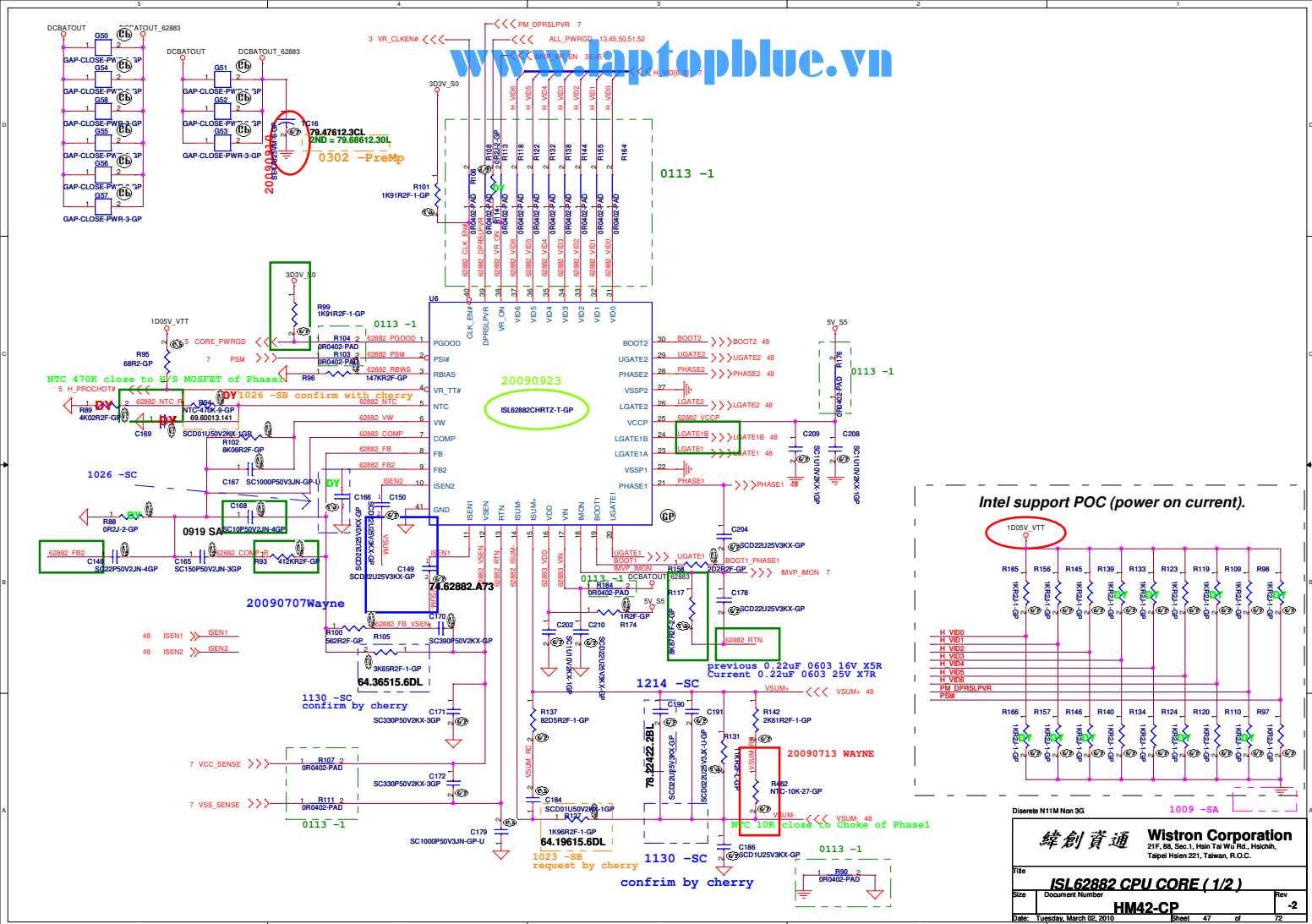


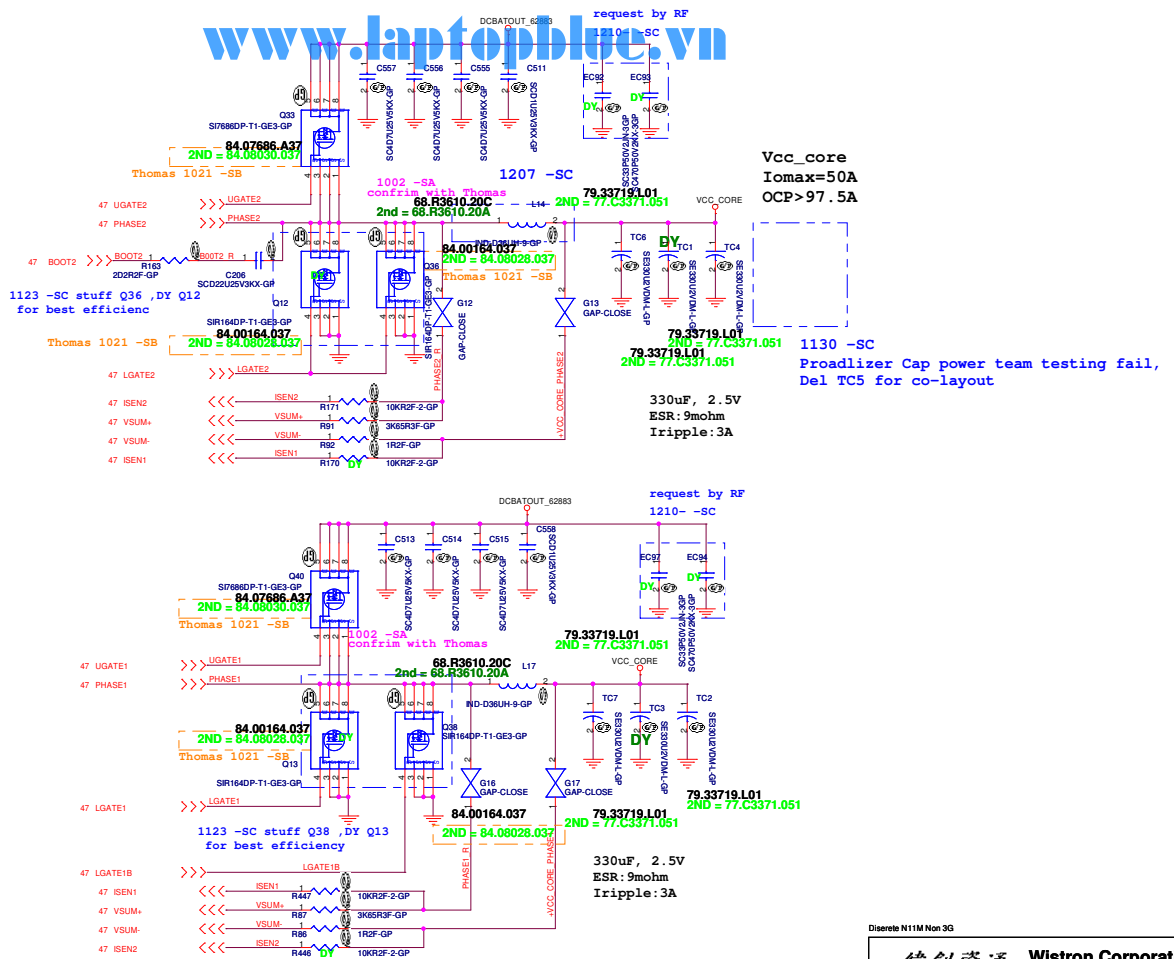
1008 -SA



Title			
<i>RUN POWER and 3D3V AUX S5</i>			
Size	Document Number	Rev	
	HM42-CP	-2	
Date: Monday, March 01, 2010	Sheet 45	of 72	



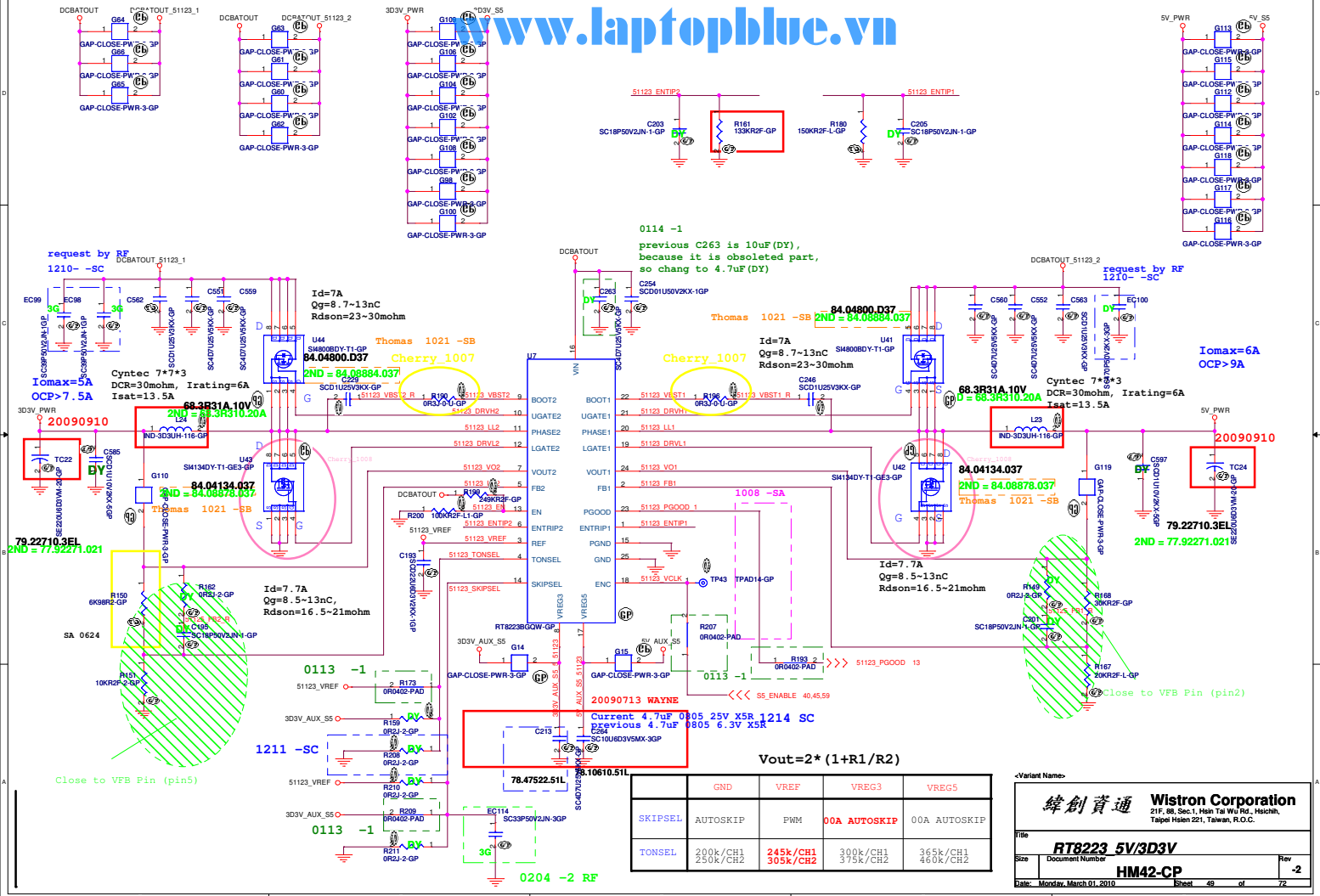




Discrete N11M Non 3G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File	ISL62882 CPU CORE (1/2)
Size	Document Number
Date	Monday, March 01, 2010
Sheet	48 of 72
Rev	-2



Vout=2* (1+R1/R2)

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

Variant Name:

緯創資通 Wistron Corporation
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

File: **RT8223 5V/3D3V**

Size: Document Number

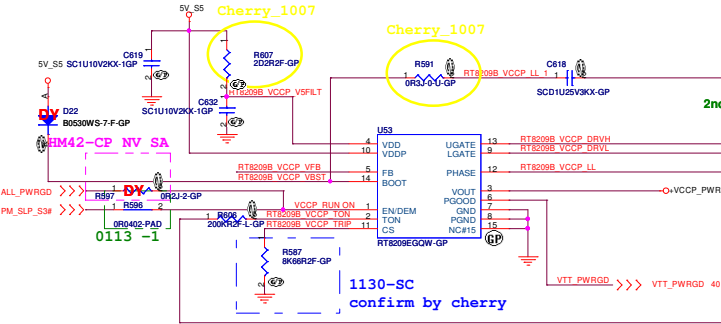
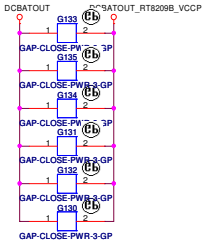
Rev: **HM42-CP**

Date: Monday, March 01, 2010

Sheet 49 of 72

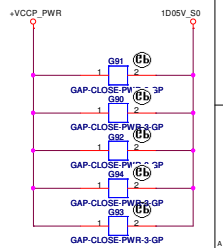
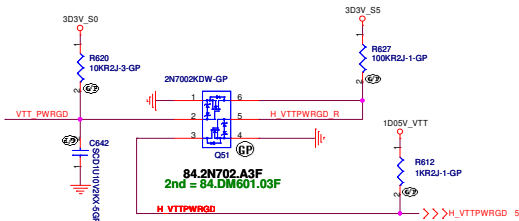


RT8209E for VCCP



Freq=360KHz

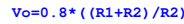
because of 1.05V_S0 and 1.05V_VTT combin together
use PM_SLP_S# Enable 1.05V power



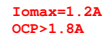
Discrete N11M Non 3G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsien 221, Taiwan, R.O.C.

Title		RT8209B +VCCP	
Size	Document Number	HM42-CP	Rev
Date	Monday, March 01, 2010	Sheet	1 of 2

$$I_{\text{omax}} = 0.8 \text{ A}$$


RT9026 for 0D75V_S0



HM42-CP NV Muxless 0917

UMA Non 3G

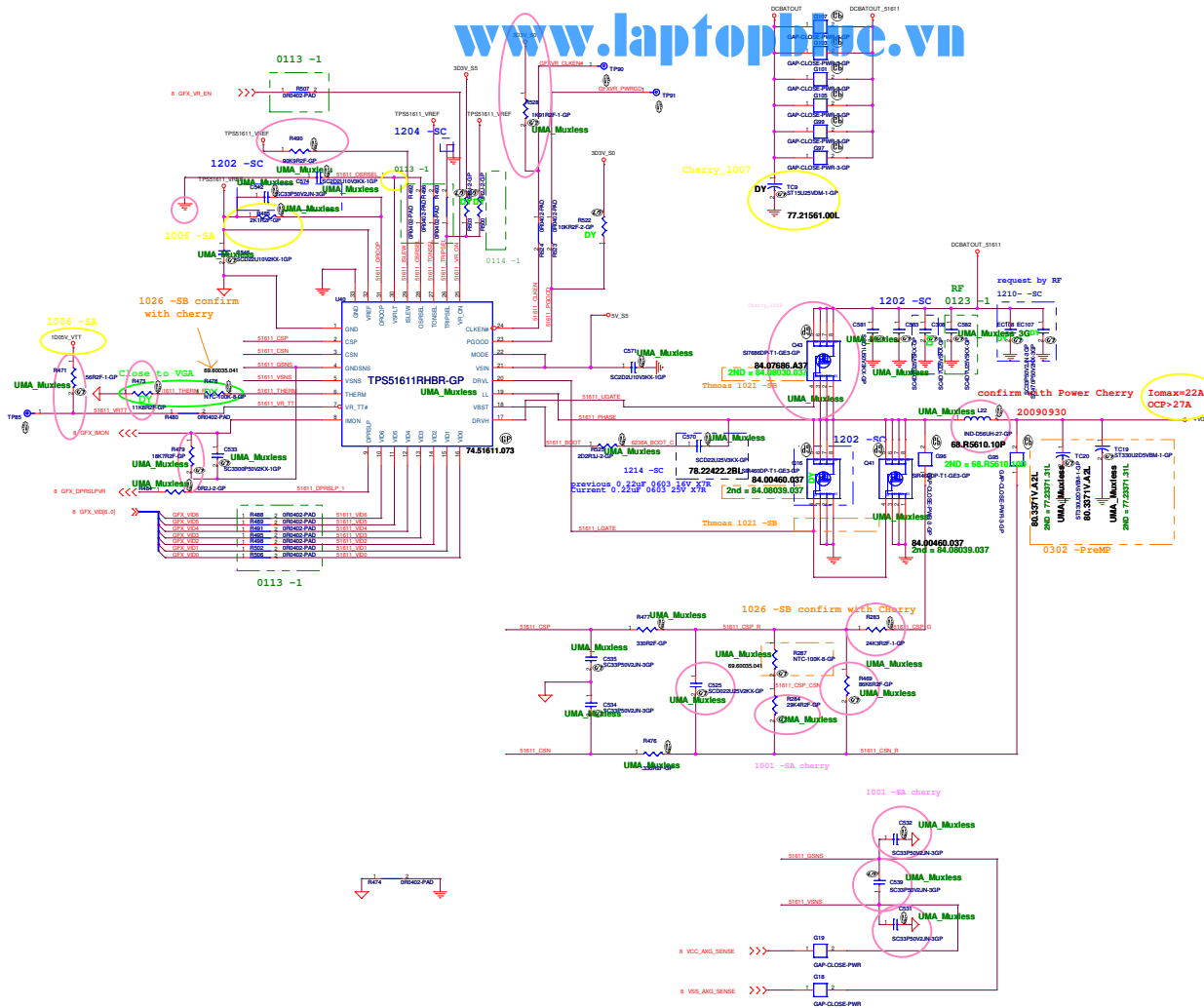
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT9025 1D8V/RT9026 0D75
-------	--------------------------------

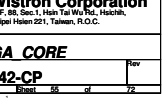
Size	Document Number
	HM42-CP
Date: Monday, March 01, 2010	Sheet 52 of 52

Date: Monday, March 01, 2010 Sheet 52 of 72





0.75V* (R1+R2) /R2



Mode	Product (s)	NVCLK (MHz)	MCLK (MHz)	NVDD
Performance (P0)	N11P-GE1	575	790	0.95 V
Performance (P0)	N11P-P1	475	700	0.85 V
Balanced (P8)	N11P-GE1 N11P-P1	405	324	0.85 V
Battery (P12)	N11P-GE1 N11P-P1	135	135	0.80 V

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11M-GE1	625	790	1.03 V
Performance (P0)	N11M-LP1	525	700	0.86 V
Balanced (P8)	N11M-GE1 N11M-LP1	405	405	0.85 V
Battery (P12)	N11M-GE1 N11M-LP1	135	135	0.85 V

Mode	Product (±)	NVCLK (MHz)	MCLK (MHz) DDR3	NVDD
<u>Performance (P0)</u>	N11M-OP1	625	790	<u>1.03 V</u>
Performance (P0)	N11M-OP2	525	700	0.86 V
<u>Balanced (P8)</u>	<u>N11M-OP1</u> N11M-OP2	405	405	<u>0.85 V</u>

0	0	0.8
0	1	0.85
1	0	0.95

GPIO6/NVDD_ALTV1	GPIO5/NVDD_ALTV0	NVDD_ALTV0
0	1	0.1
1	0	1.1

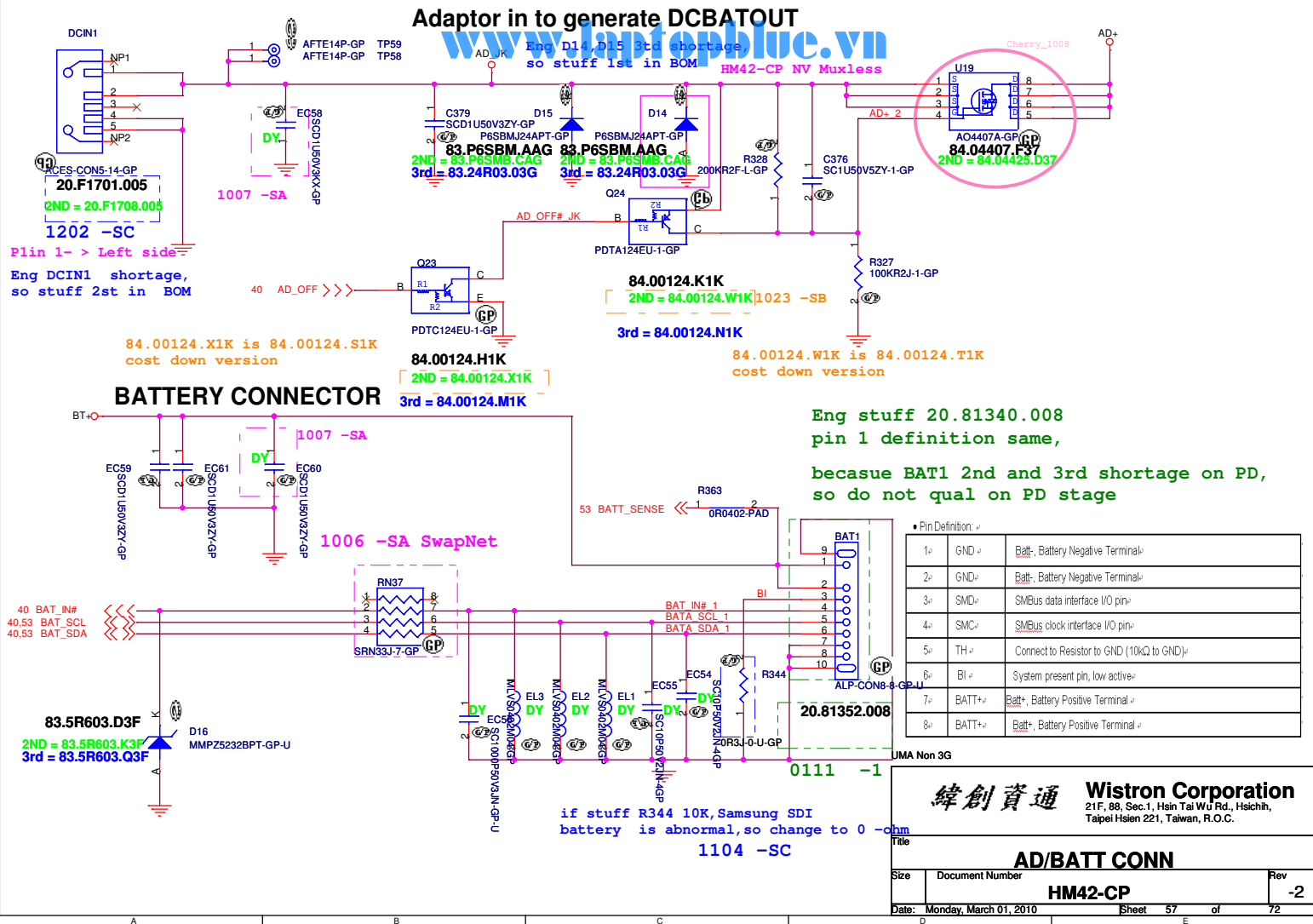
UM

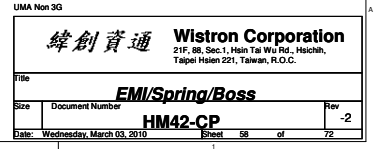
RT8209A VGA CORE

Document Number	Rev
HM42-CP	
Date: Tuesday, March 02, 2010	Sheet 55 of 72

Adaptor in to generate DCBATOUT

www.hapblue.vn





Check test point

delete 3D3V_S0 test point



Test Point放在Dimm Door打開可量測處

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

AFTE_TP

Size

Document Number

HM42-CP

Rev

-2

Date: Monday, March 01, 2010

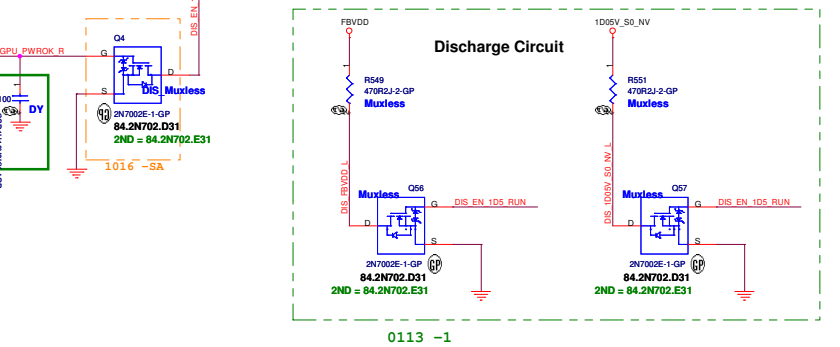
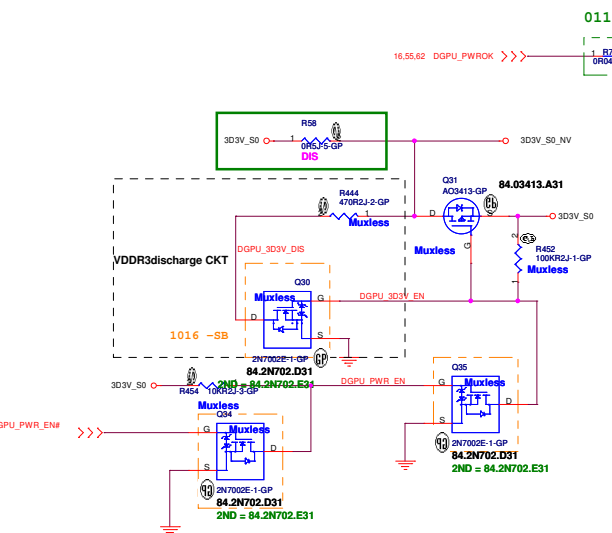
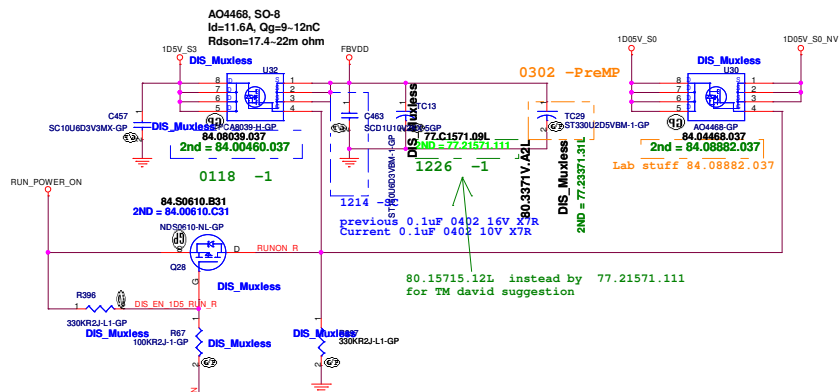
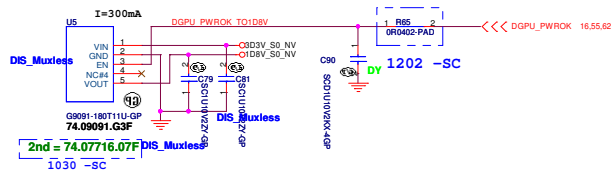
Sheet 59 of 72

+3VS to 1.8V Transfer

www.laptopblue.vn

+1.5V to FBVDD Transfer

+1.05V to +1.05V_NV Transfer



UMA Non 3G

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipai Hsien 221, Taiwan, R.O.C.

File

NV power

Size

Document Number

Rev

Date

Tuesday, March 02, 2010

Sheet

61

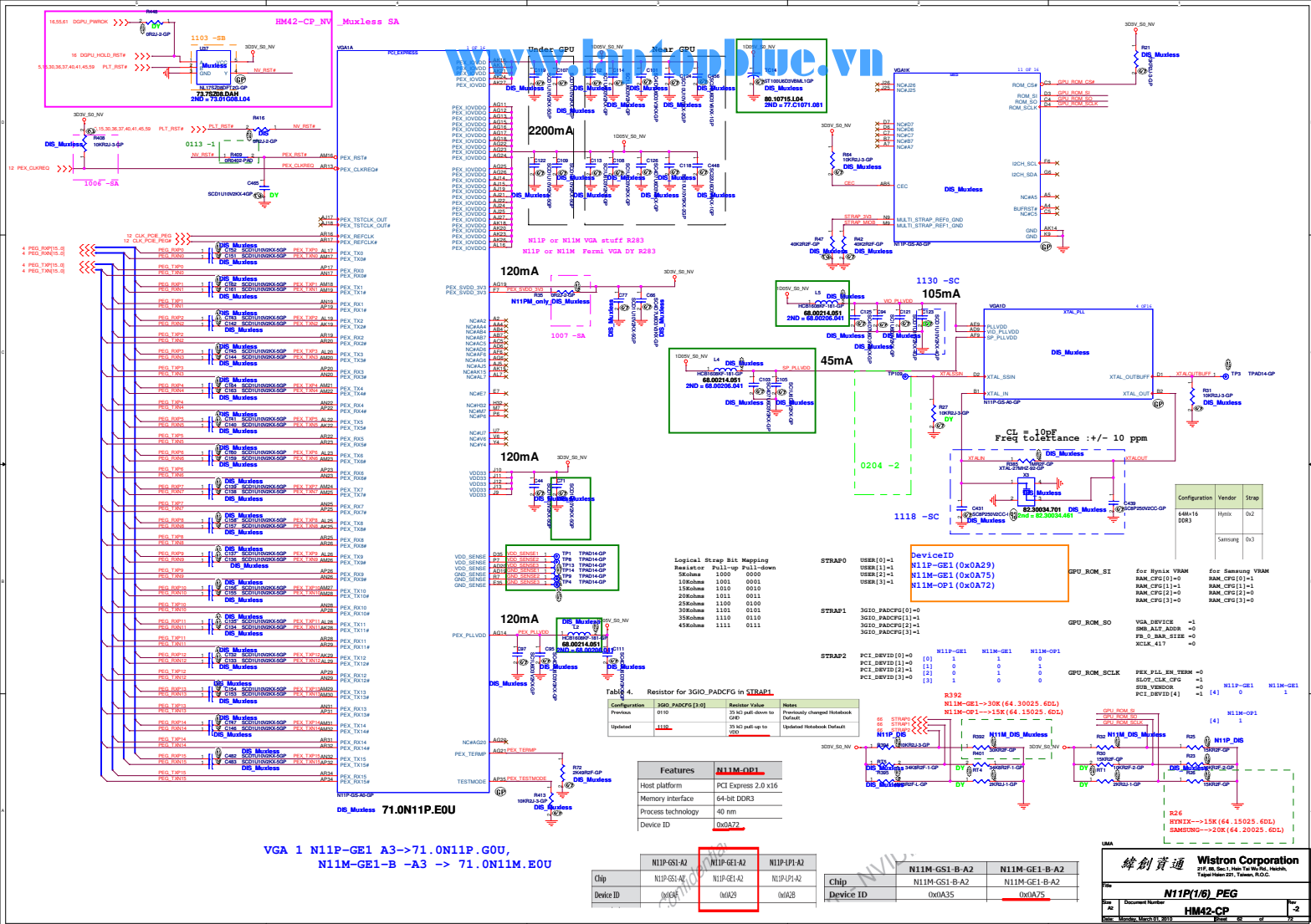
of

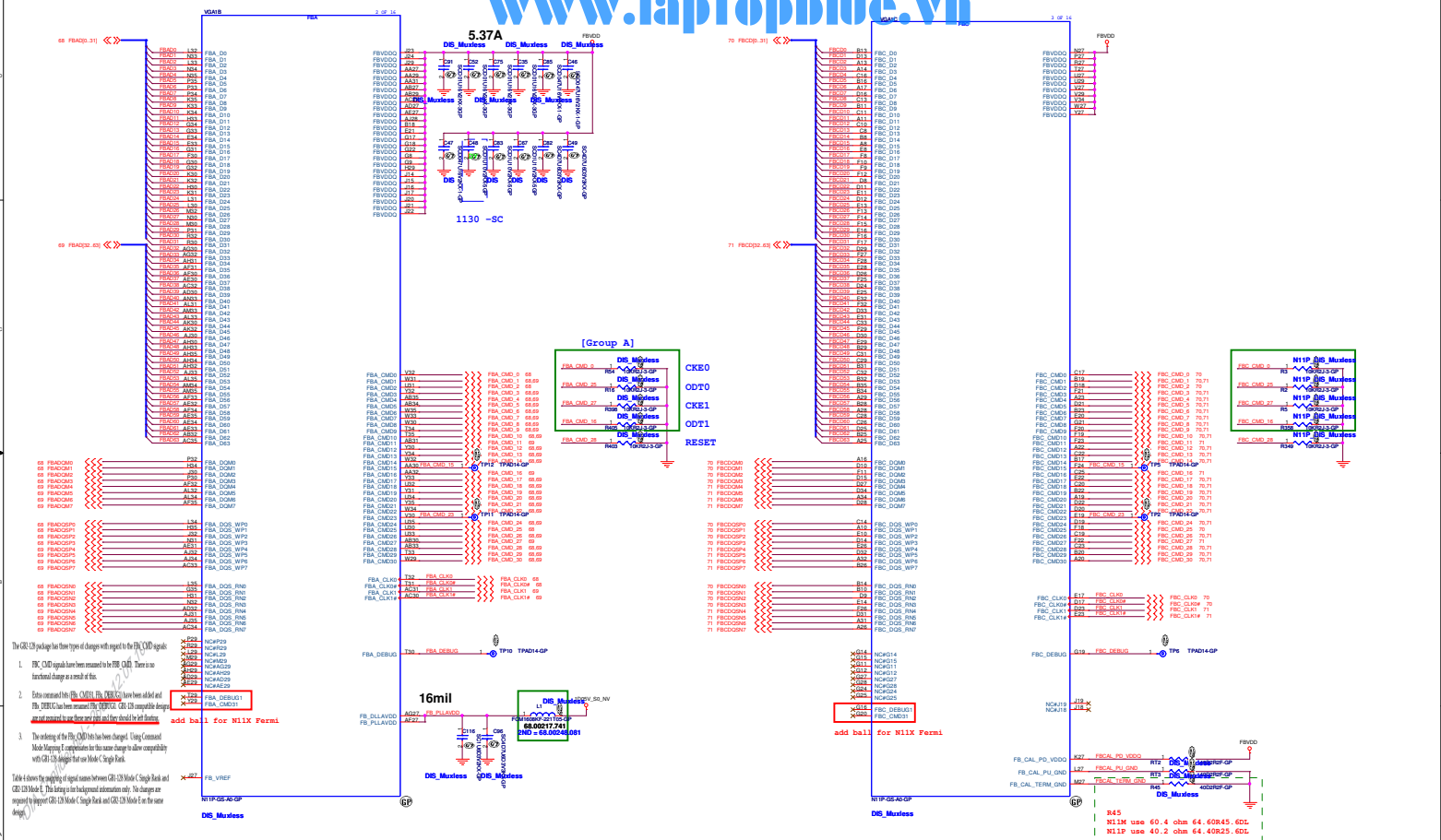
72

HM42-CP

Rev

-2



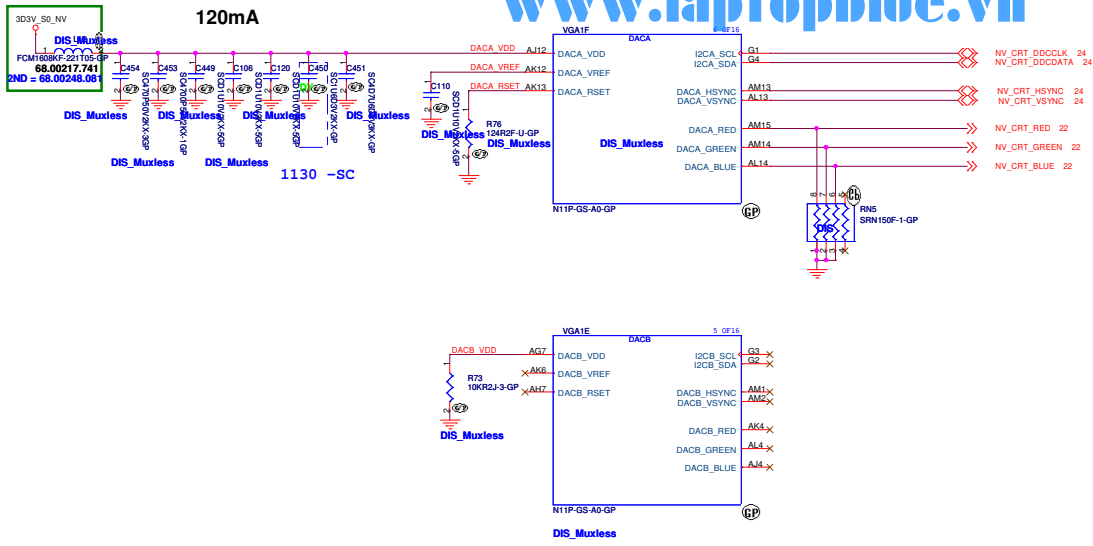


Observe 101 Mm Rom 25

Wistron Corporation
217, 2nd Floor, No. 1, Ta Hsin Rd., Taichung, R.O.C.

Document Number: **N11P(2/5) MEMORY**
Revision: **HM42-CP**
Date: March 21, 2010

2



Discrete N11M

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

N11P(3/6)_DAC

Size
A3

Document Number

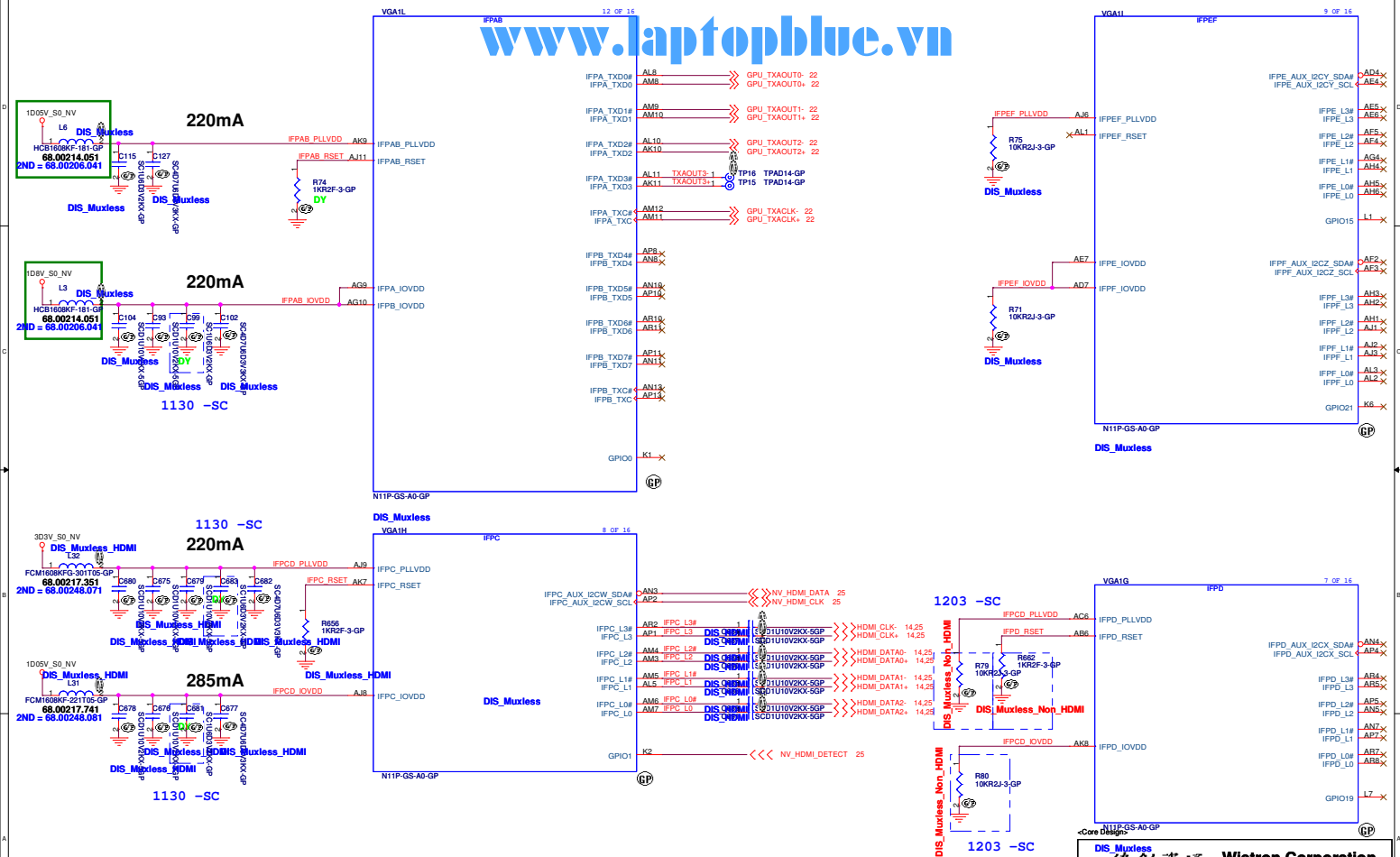
	A
--	---

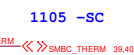
HM42-CP

Date:

Monday, March 01, 2010

--	--





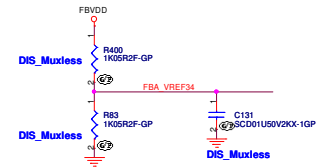


1123 -SC

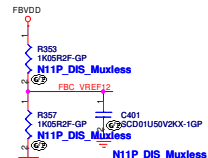
1130 -SC

[illegible]

緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
VRAM(1/4)	
Document Number	Rev
HM42-CP	
Monday, March 01, 2010	Sheet 68 of 72



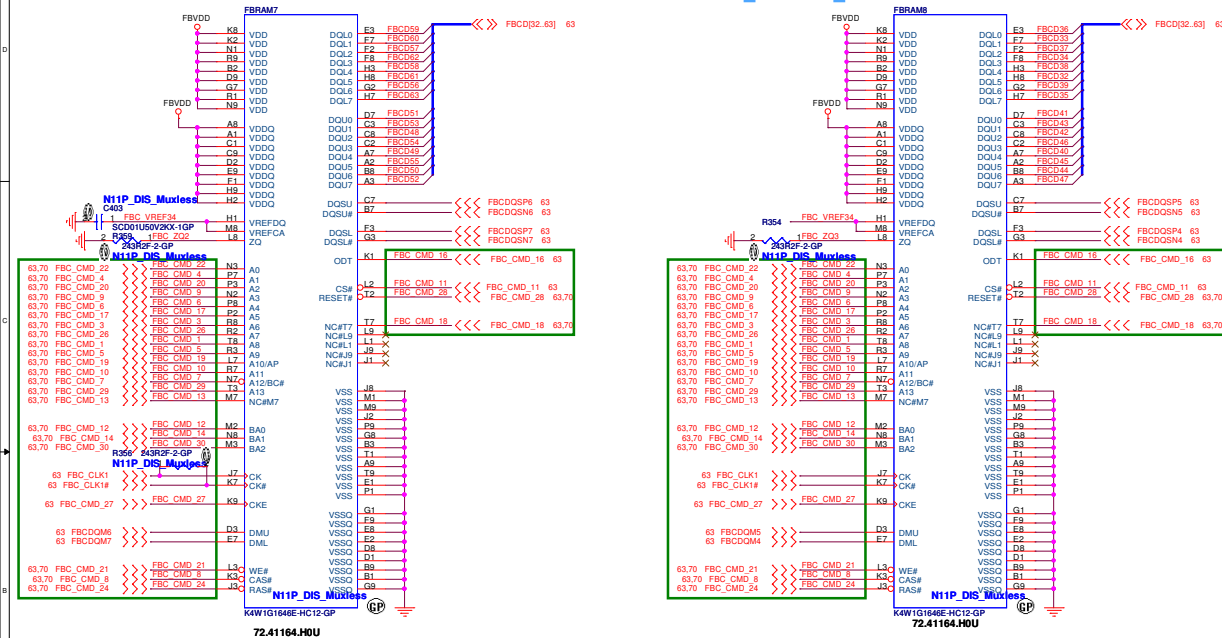
HM42-CP			
緯創資通		Wistron Corporation 21F, 88, Sec. 1, Hsain Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
VRAM(2/4)			
Size A3	Document Number	Rev -2	
HM42-CP			
Date: Monday, March 01, 2010		Sheet 69 of 72	



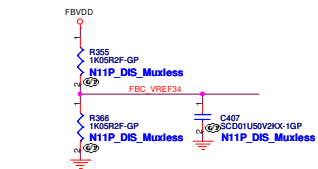
HM42-CF

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
VRAM(3/4)			
Size A3	Document Number		Rev
	HM42-CP		-2
Date: Monday, March 01, 2010		Sheet 70 of 72	



```
SAMSUNG: 72.41164.H0U
HYNIX:   72.51G63.C0U
```



UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Year	Journal	Volume	Page
...

Title	VRAM(4/4)
-------	------------------

Size
A3

Size A3	Document Number
------------	-----------------

Date:

Date: Monday, March 01, 2010

PLATE 1

DATE: Monday, March 01, 20

