

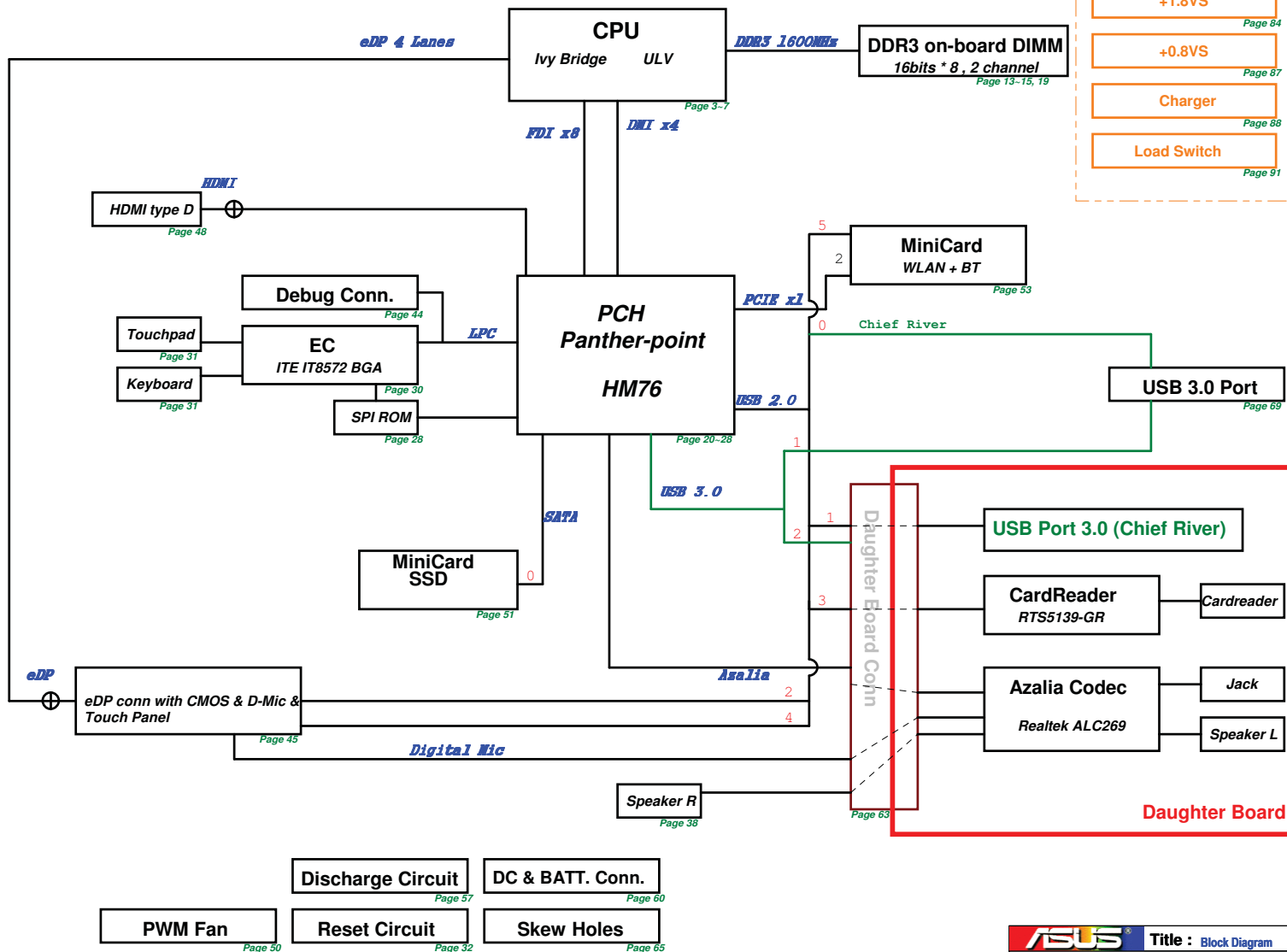
SYSTEM PAGE REF.

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80. PW_VCORE(RT8168B)
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 83. PW_I/O_DDR(RT8207M)
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 87. PW_+0.8VS(RT8015B)
 88. PW_CHARGER(BQ24725)
 91. PWR_LOAD SWITCH

UX31A2 SCHEMATIC Revision R2.0

BLOCK DIAGRAM



Power

VCORE+GFX CORE

System

+1.05VS

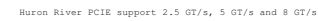
+1.5V & +0.75V

+1.8VS

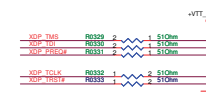
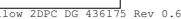
+0.8VS

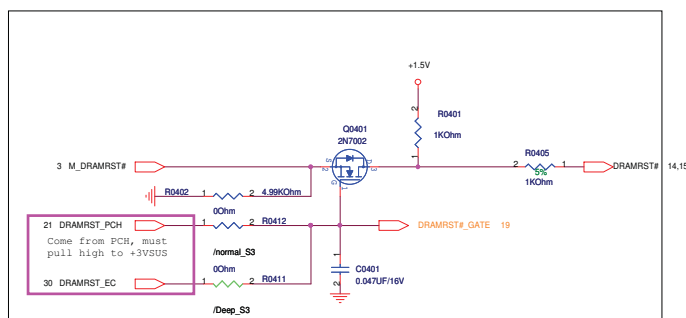
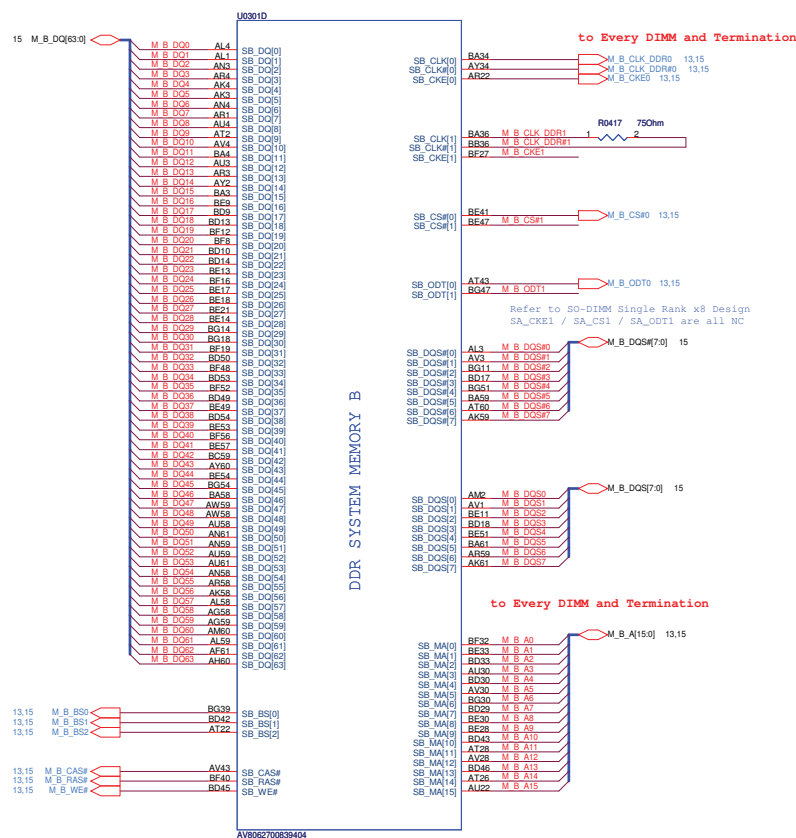
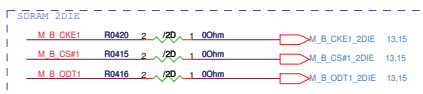
Charger

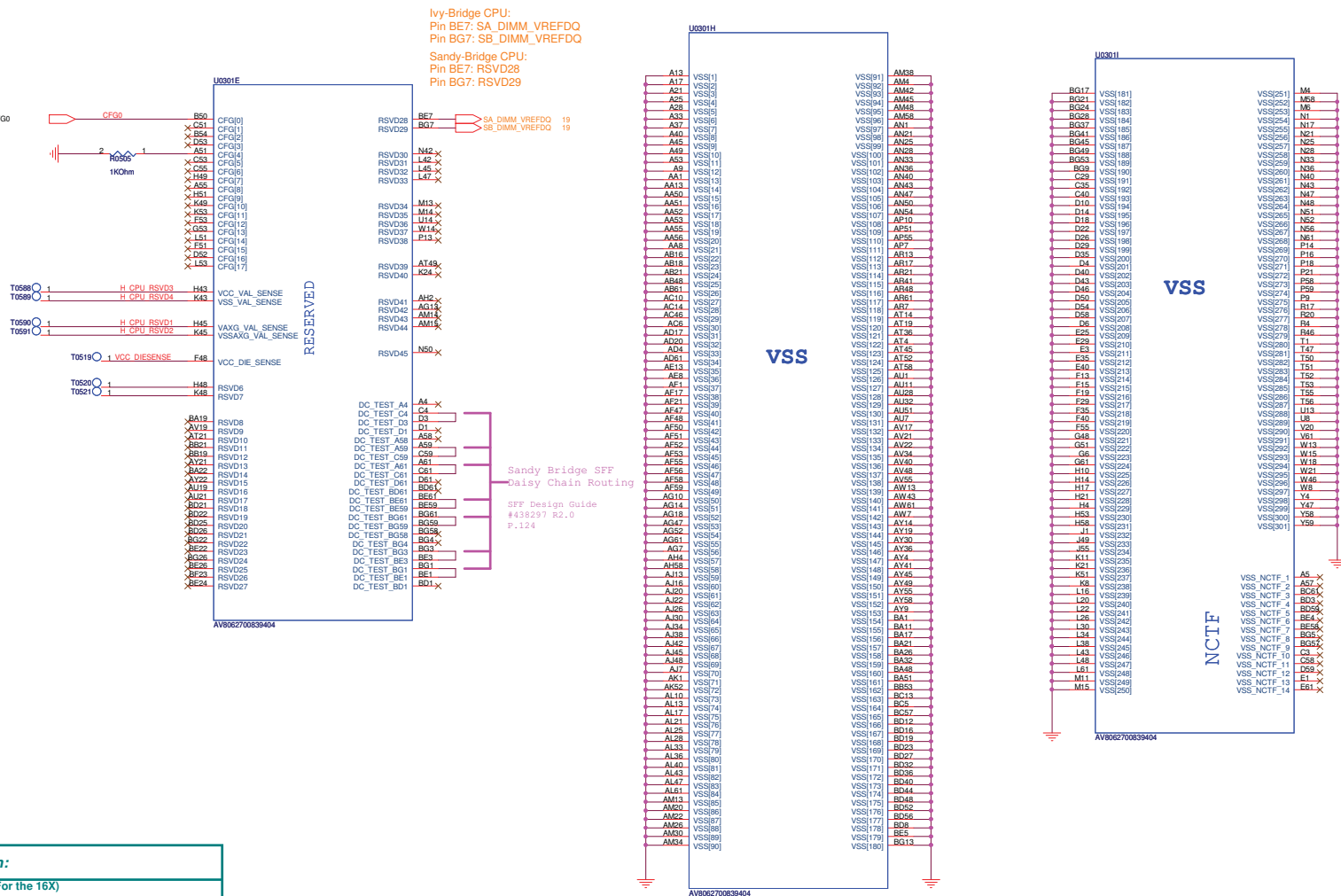
Load Switch



3. 436735 PDG Page 41, 180nF-265nF







CFG strapping information:

CFG[2]: PEG Static Lane Reversal (For the 16X)

- 1: (Default) Normal Operation; Lane # definition matches socket pin map definition
- 0: Lane Reversed

CFG[4]: Display Port Presence Strap

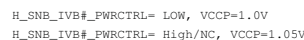
- 1: (Default) Disable; No Physical Display Port attached to Embedded Display Port
- 0: Enable; An external Display Port device is connected to the Embedded Display port

CFG[6:5]: PCIe Port Bifurcation Straps

- 11: (Default) X16 - Device 1 functions 1 and 2 disable
- 10: X8, X8 - Device 1 function 1 enabled; Function 2 disable
- 01: Reserved - (Device 1 Function 1 disable; Function 2 enable
- 00: X8, X4 X4 - Device 1 function 1 and 2 enabled

CFG[7]: Defer Training

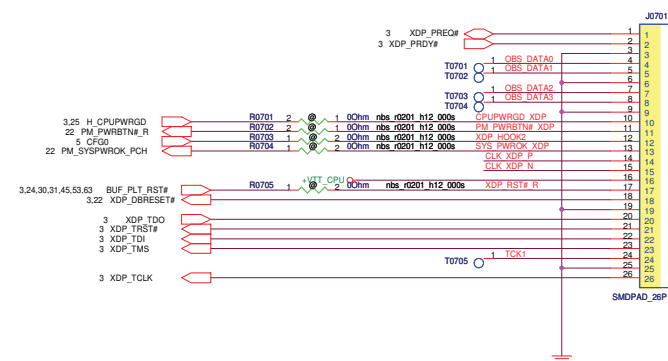
- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS for training



VCCSA_SEL0	VCCSA_SEL1	VCCSA_SEL
L	L	0.9V
L	H	0.85V
H	L	0.75V
H	H	0.65V

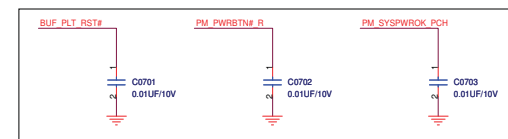
The schematic diagram illustrates the XDP module's connections to various system components:

- WTT_CPU:** Connected to the XDP module via a 510 Ohm resistor (R0707).
- XDP_TDO:** Connected to the XDP module via a 60 Ohm resistor (R0708).
- PCH_JTAG_TDO:** Connected to the XDP module via a 60 Ohm resistor (R0708).
- +3VS:** Connected to the XDP module via a 1K Ohm resistor (R0709).
- XDP_DBRESET#:** Connected to the XDP module via a 60 Ohm resistor (R0709).
- +3VA:** Connected to the XDP module via a 1K Ohm resistor (R0711).
- SYS_PWROCK_XDP:** Connected to the XDP module via a 60 Ohm resistor (R0711).
- XDP_TDI:** Connected to the XDP module via a 60 Ohm resistor (R0712).
- PCH_JTAG_TDI:** Connected to the XDP module via a 60 Ohm resistor (R0712).
- XDP_TMS:** Connected to the XDP module via a 60 Ohm resistor (R0710).
- PCH_JTAG_TMS:** Connected to the XDP module via a 60 Ohm resistor (R0710).
- CLK_XDP_P:** Connected to the XDP module via a 60 Ohm resistor (R0710).
- CLK_XDP_N:** Connected to the XDP module via a 60 Ohm resistor (R0710).
- CLK_XDP_P:** Connected to the XDP module via a 60 Ohm resistor (R0710).
- CLK_XDP_N:** Connected to the XDP module via a 60 Ohm resistor (R0710).
- CLK_XDP_P:** Connected to the XDP module via a 60 Ohm resistor (R0710).
- CLK_XDP_N:** Connected to the XDP module via a 60 Ohm resistor (R0710).

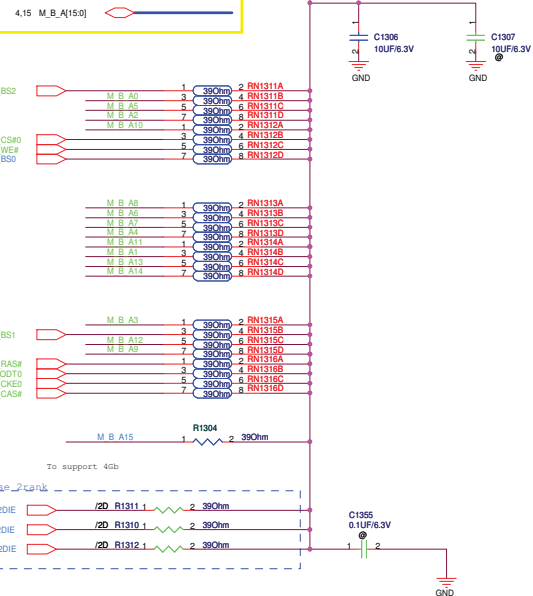
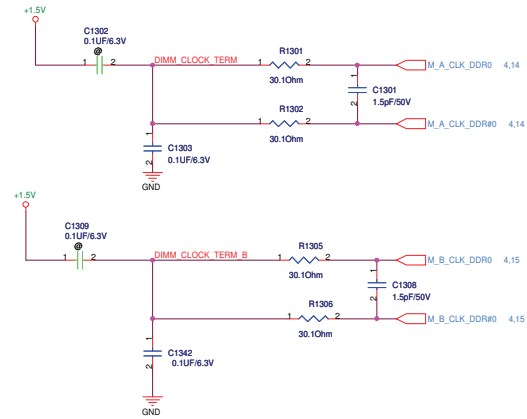
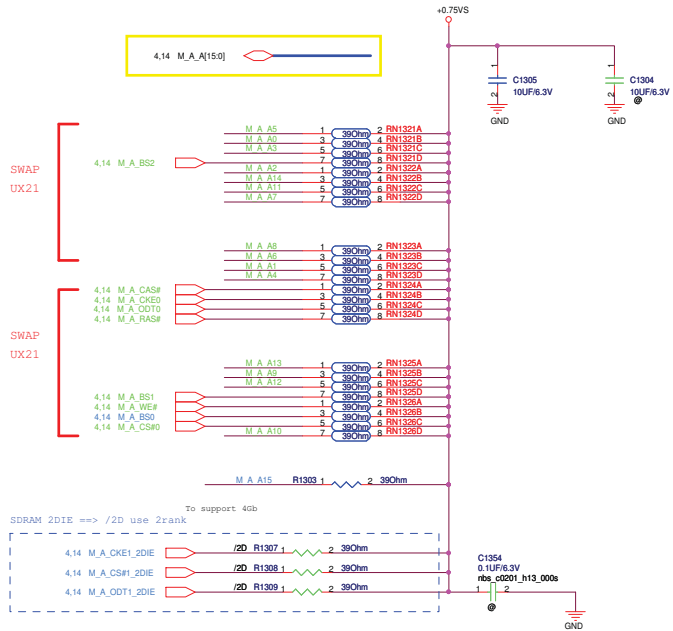


Please mount J0701,
R0701~R0705 and RNX0702
for debug on SR and ER

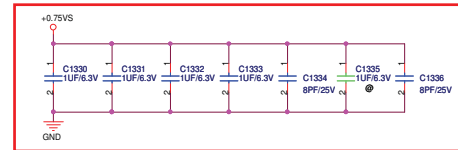
Place near J0701



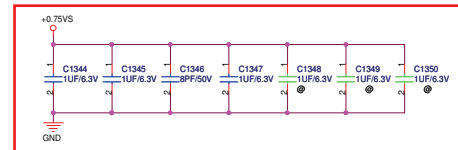
5					4					3					2					1																								



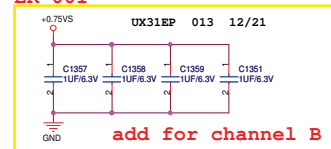
Refer to Intel CSB



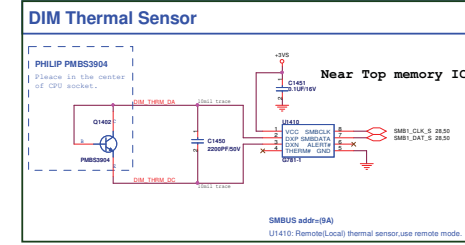
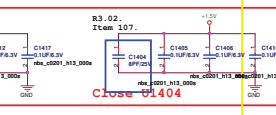
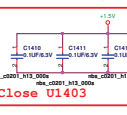
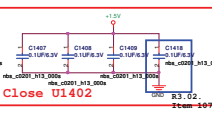
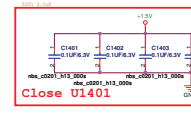
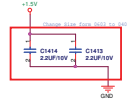
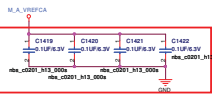
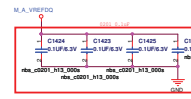
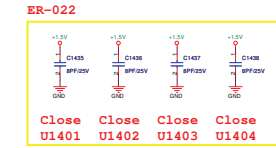
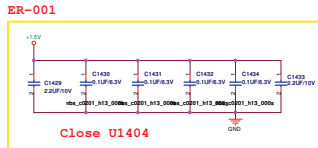
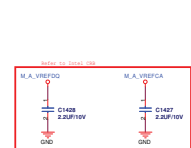
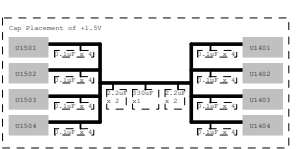
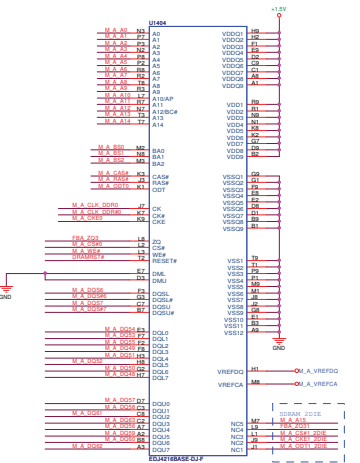
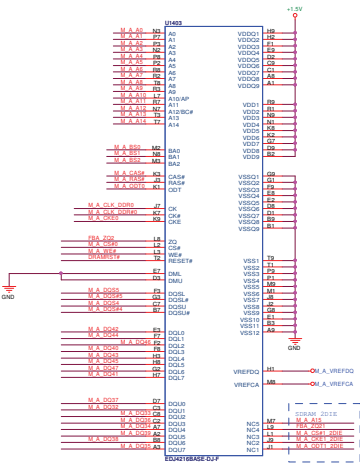
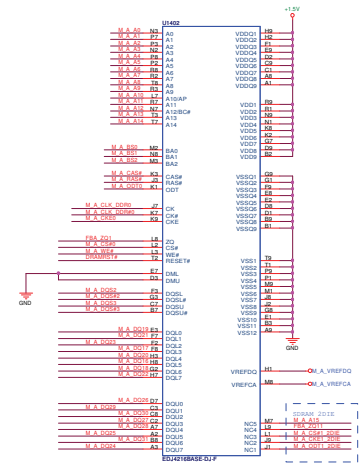
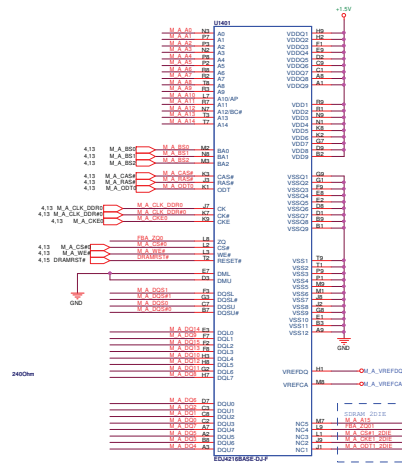
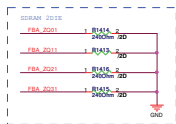
Refer to Intel CSB

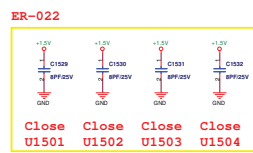
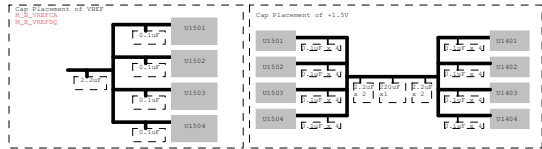
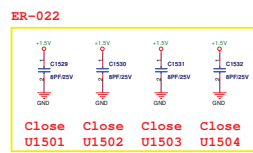


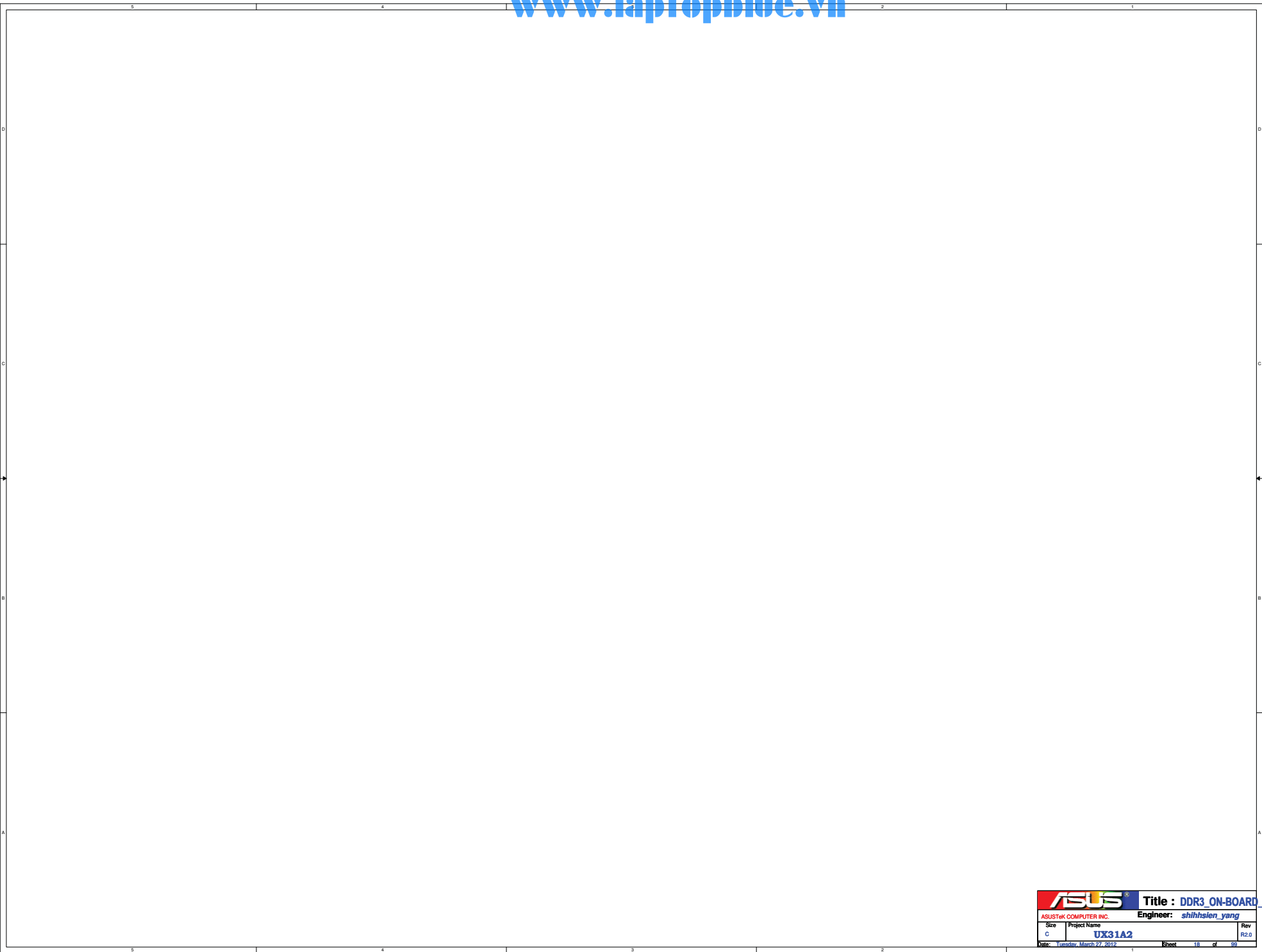
ER-001



ER-022



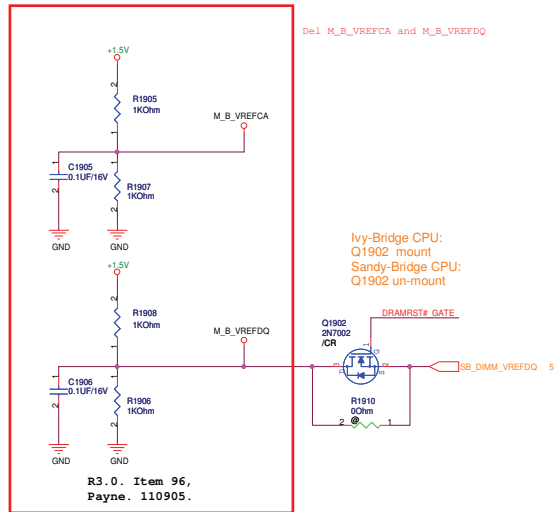
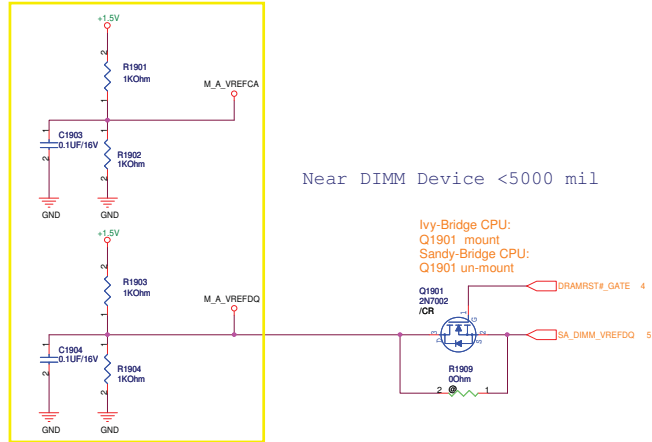




Calpella Clarksfield DDR3 SO-DIMM VREFDQ
Platform Design Guide Change Details

DDR3 Vref

Intel Document Number: 400755



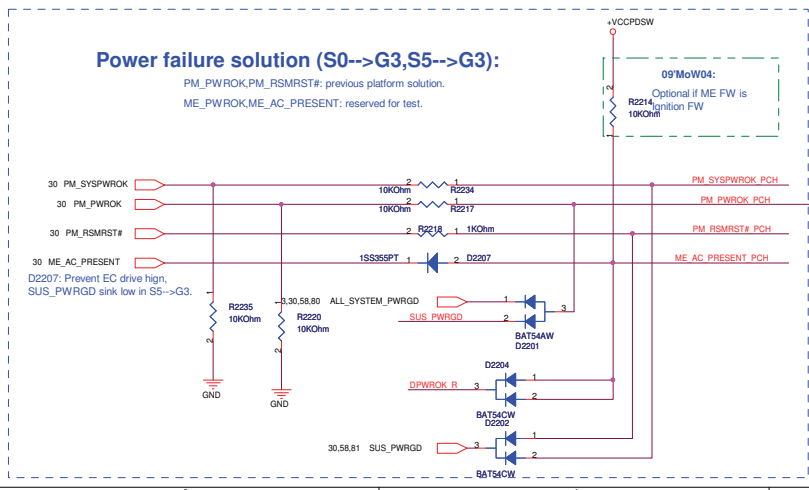
SUSACK#:
SUSACK# and SUSWRN# can be tied together
if EC does not want to involve in handshake
mechanism for the Deep Sleep state entry and exit.

APWROK:
For platform not supporting IAMT
it can be connected to PWROK.

SUSPWRDNACK (PCH to EC):
This pin requires a pull-up to +3VSUS.
Platforms are not expected to use this
signal when the PCH's Deep S4/S5 feature is used.

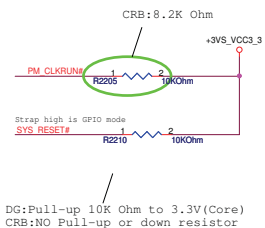
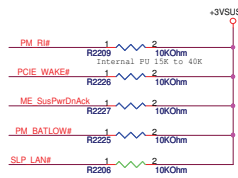
SUSWRN# (PCH to EC):
This pin asserts low when PCH is planning
to enter the DeepSx power state and remove
Suspend power (using SLP_SUS#)

Entry Into Deep S4/S5
A combination of condition is required for entry into Deep S4/S5
All of the following must be met:
-Intel ME in Mof.
-AND either "a" or "b"(EDS R0.7v1 p.186).

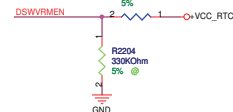


CHECK PULL-UP OR DOWN

For PU/PD



DSWVRMEN:
High -> DSW On-Die VR Enable
Low -> DSW On-Die VR disable



DPWROK:
This input is tied
together with RSMRST#
in platforms that do not
support DeepSx

VCCDSW stable to DPWROK
assertion is 10ms (min)

4/23 Delete R2222, R2228,
U2201, R2230, R2233, C2201
and D2203, Deeper
sleeper要那掉

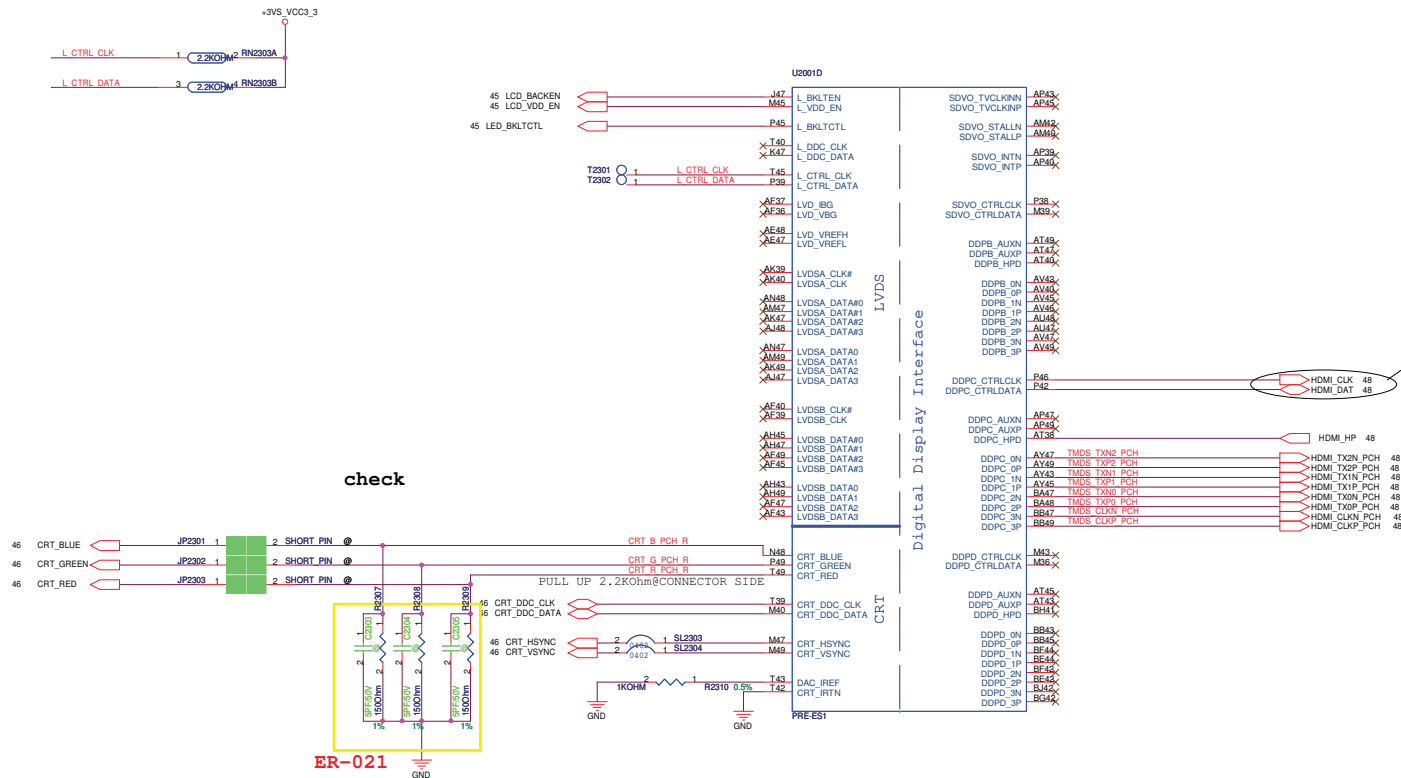
PMSYNCH is Low in C6/C7 states only

Boundary Scan TP (PCH)

PM_RSMRST# PCH 1 T2217
PM_PWROK PCH 1 T2211
APWROK_R 1 T2215
PM_SYSPWROK PCH 1 T2216

PORT	STRAP	ENABLE PORT	DISABLE PORT
LVDS	L_DDC_DATA	Pull up to 3.3 (V) with 2.2k Ohm	NC
PORT B	SDVO_CTRLDATA		
PORT C	DDPC_CTRLDATA		
PORT D	DDPD_CTRLDATA		

DG P.105,168



Tacoma Pass (NVRAM) Disabling and termination guidelines (DG R0.7 p.322)
If the Tacoma Pass interface is not used,
the interface signals, including NV_RCOMP,
can be left as No connects with few exceptions.
VccpM0, NV_ALE, NV_CLE

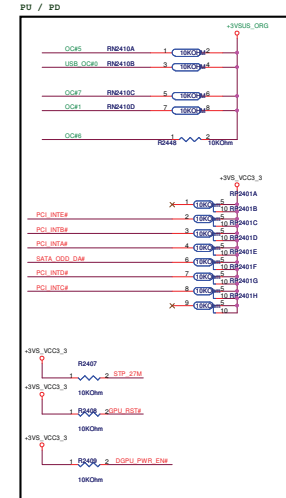
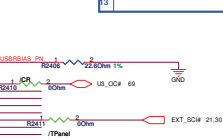
DMI & FDI Termination Voltage	
NV_CLE	LOW : Set to Vss
CSB	HIGH : Set to Vcc

ER-018



USB2.0		USB 3.0	
0	USB 3.0 Port	1	USB 3.0 Port
1	USB 2.0 Port (Debug)	2	USB 3.0 Port
2		3	
3		4	
4	Camera		
5	WiFi/ WiMax/ Blue Tooth		
6			
7			
8	Touch Panel		
9	Card Reader		
10			
11			
12			
13			

ER-031



DIMM_SEL

Schematic diagram showing the DIMM selection logic. The circuit consists of four resistors (R342, R343, R344, R345) connected in series to a 5VDDUS_GND supply. The nodes between the resistors are labeled DIMM_SEL0, DIMM_SEL1, DIMM_SEL2, and DIMM_SEL3. The resistors are connected to a GND symbol.

PCBID:10 2GB (DDR3_1333)

DDR3_1333	Samsung	Hynix	ELPIDA	Micron
DIMM_SEL0	L	H	L	H
DIMM_SEL1	L	L	H	H
DIMM_SEL2	L	L	L	L

PCBID:10 4GB (DDR3_1333)

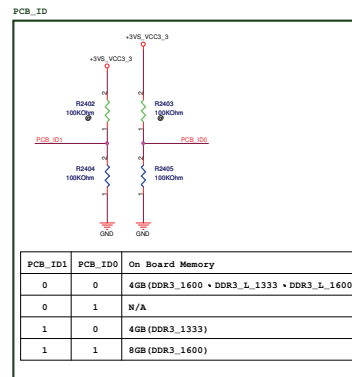
DDR3_1333	Samsung	ASIN	ELPIDA	Micron
DIMM_SEL0	L	H	L	H
DIMM_SEL1	L	L	H	H
DIMM_SEL2	H	H	H	H

PCBID:00 4GB (DDR3_L_1333 + DDR3L_1600 + DDR3_1600)

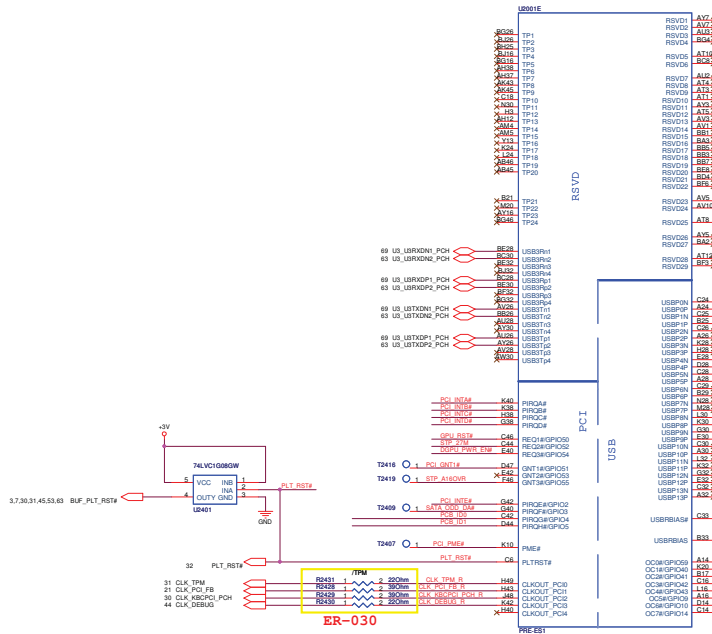
DDR3_L_1333		Hynix	ELPIDA	
DIMM_SEL0		H	L	
DIMM_SEL1		L	H	
DIMM_SEL2		L	L	
DDR3L_1600	Micron		ELPIDA	
DIMM_SEL0	L			H
DIMM_SEL1	L			H
DIMM_SEL2	H			H
DDR3_1600		Hynix	ELPIDA	
DIMM_SEL0		H	L	
DIMM_SEL1		L	H	
DIMM_SEL2		H	H	

PCBID:11 8GB (DDR3_1600)

DDR3_1600		Hynix	ELPIDA	
DIMM_SEL0		H	L	
DIMM_SEL1		L	H	
DIMM_SEL2		H	H	



PCB_ID1	PCB_ID0	On Board Memory
0	0	4GB (DDR3_1600 + DDR3_L_1333 + DDR3_L_1600)
0	1	N/A
1	0	4GB (DDR3_1333)
1	1	8GB (DDR3_1600)



ER-030

Boot BIOS Strap : GNT1#, SATA1GP

Boot BIOS Strap		
GNT1#(BBS1)	SATA1GP(BBS2)	Boot BIOS Location
0	1	Reserved
1	0	PCI
1	1	SPT (PCH)
0	0	LPC

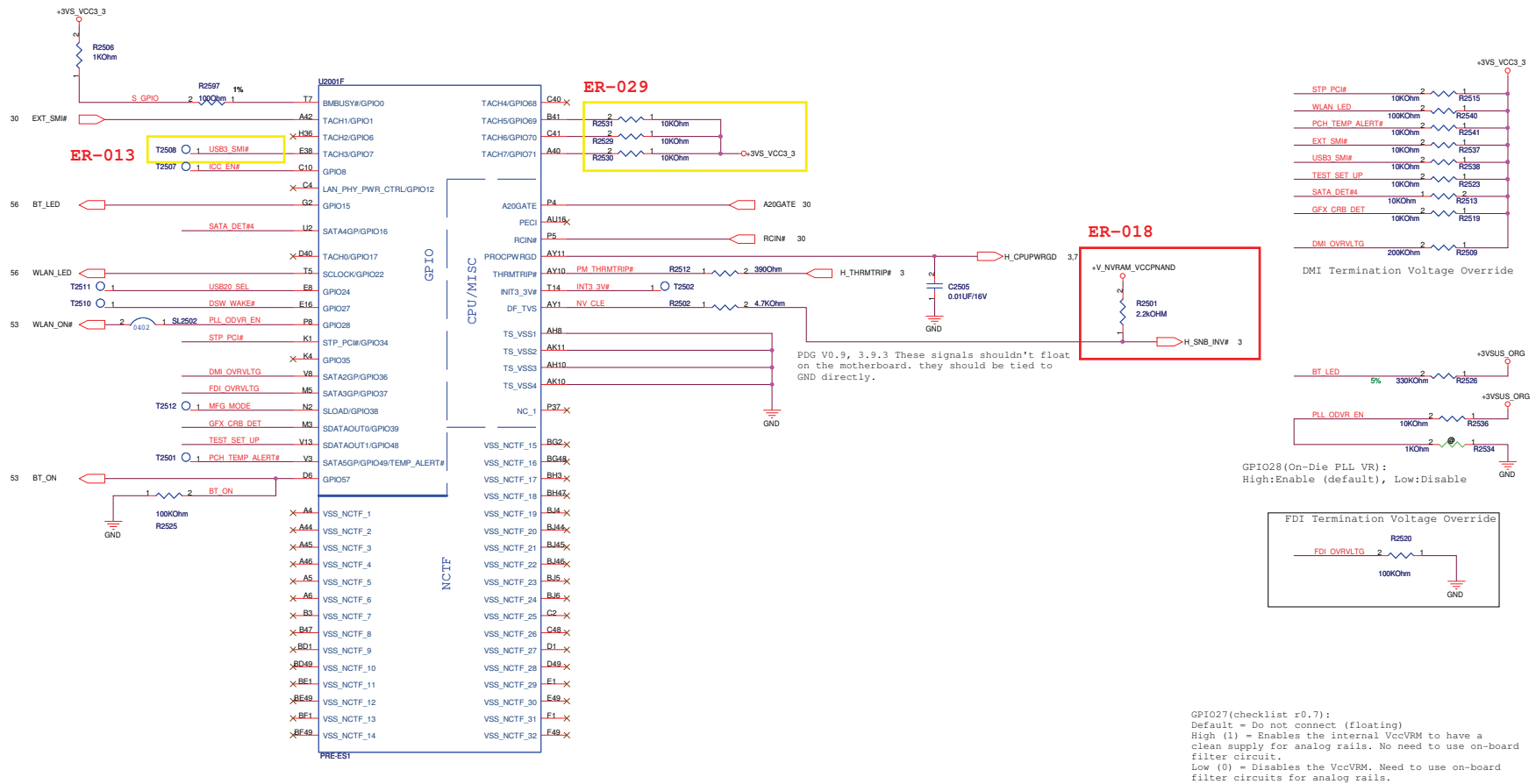
Sampled on rising edge of PWRCK.

Default
PU 20K
OHM

GNT3#: A16 swap override Strap/
Top-Block swap override jumper

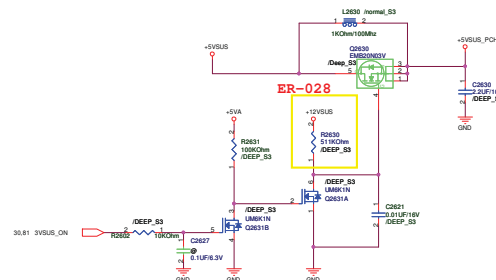
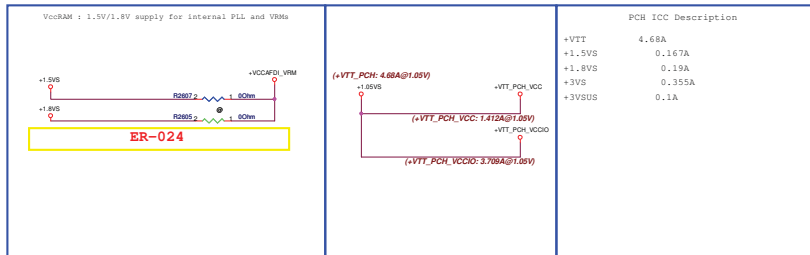
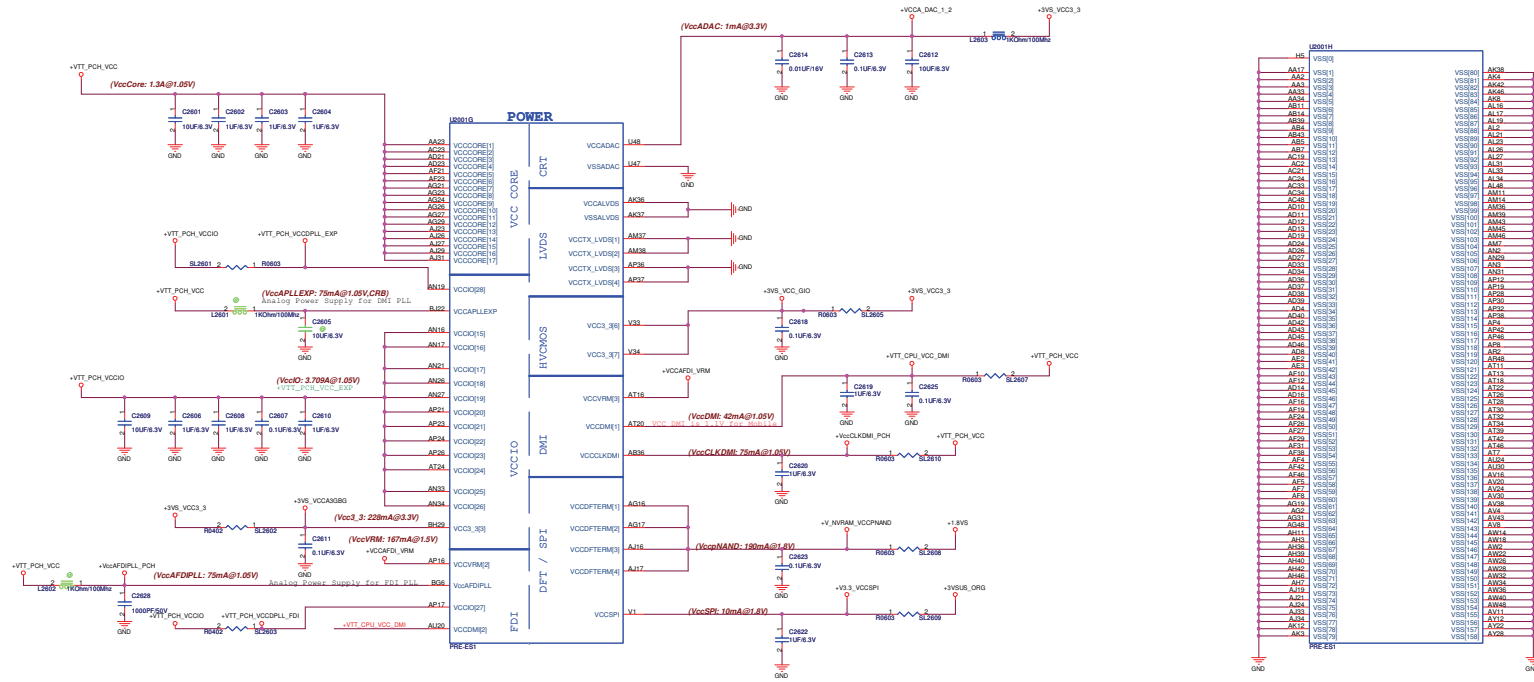
Low=Enabled A16 swap override/
Top-Block swap override

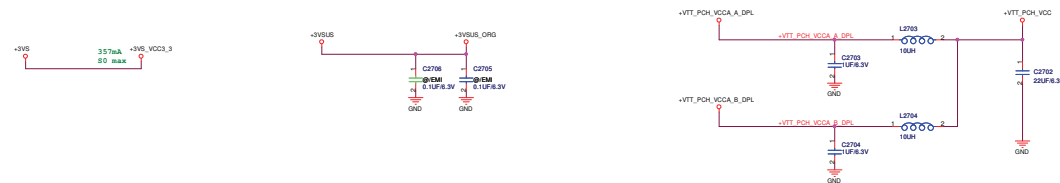
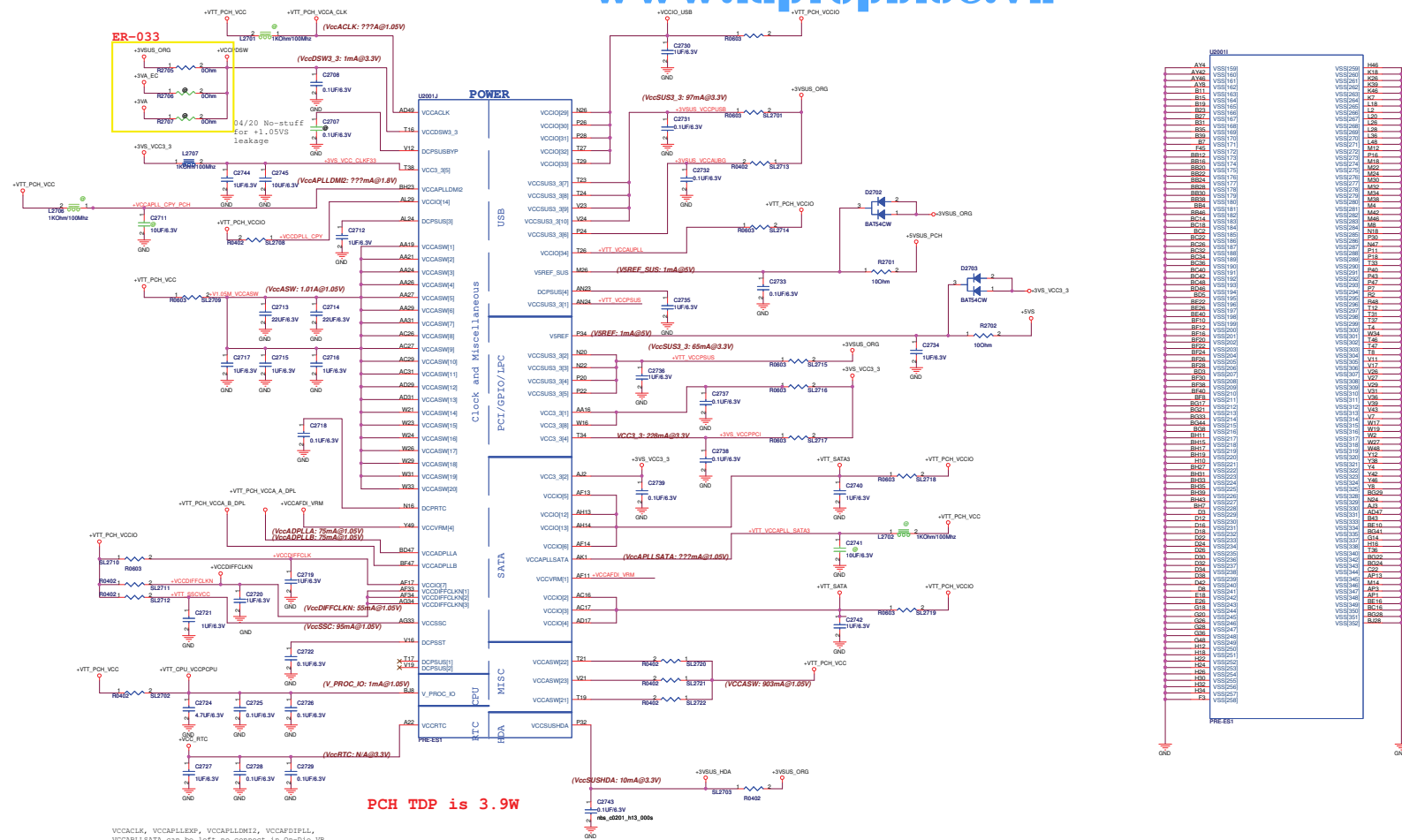
High=Default



U37 3/11 015

All Beads : 0603 !!



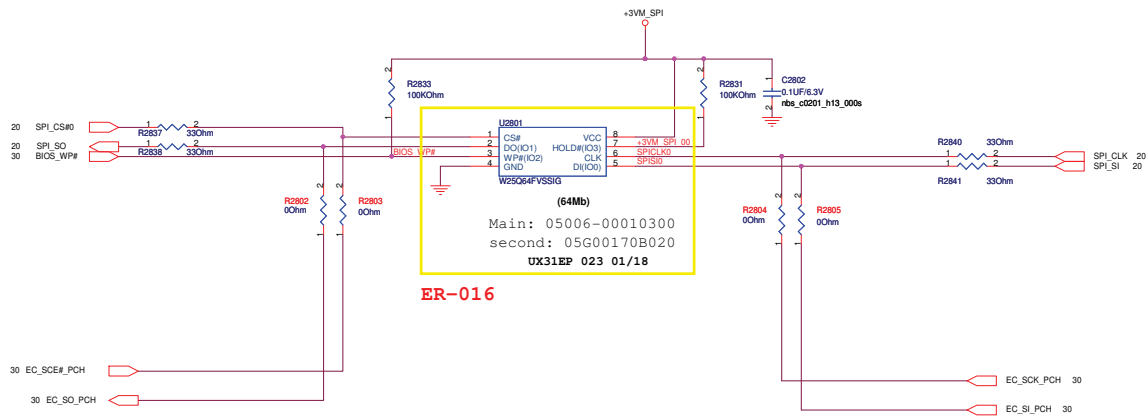


05/12 delete +3VA

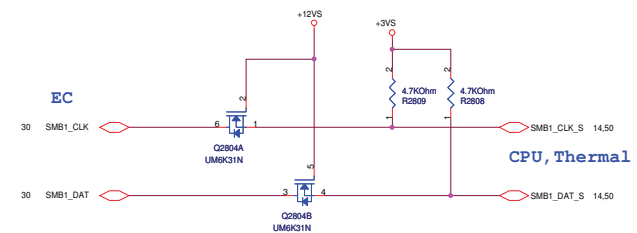
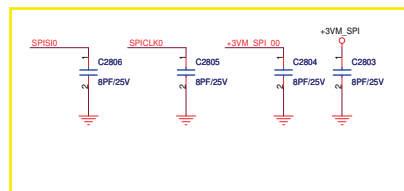
+3VSUS_ORG

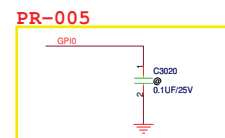
+3VM_SPI

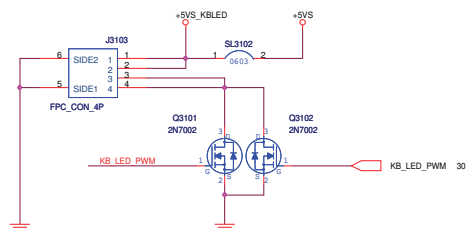
Remove SPI FLASH TOOL CON



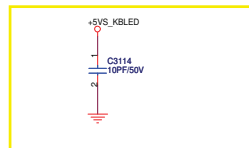
ER-025





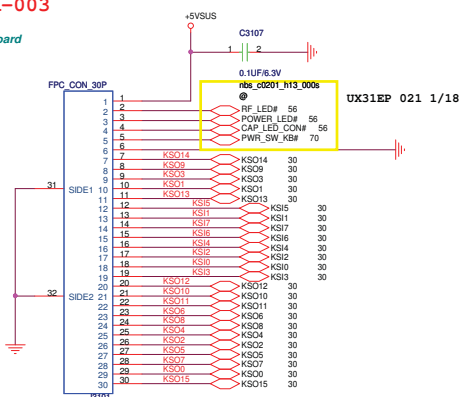
BL_CON

PR-009



ER-003

Keyboard



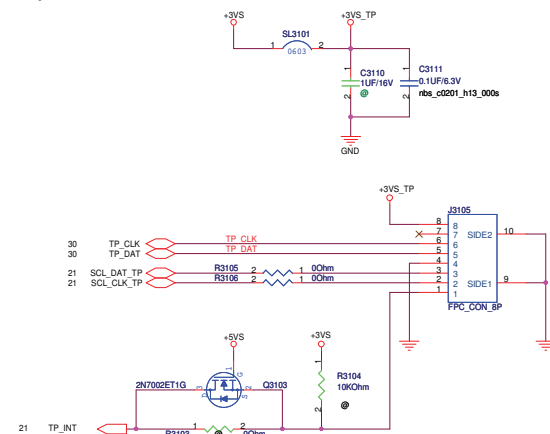
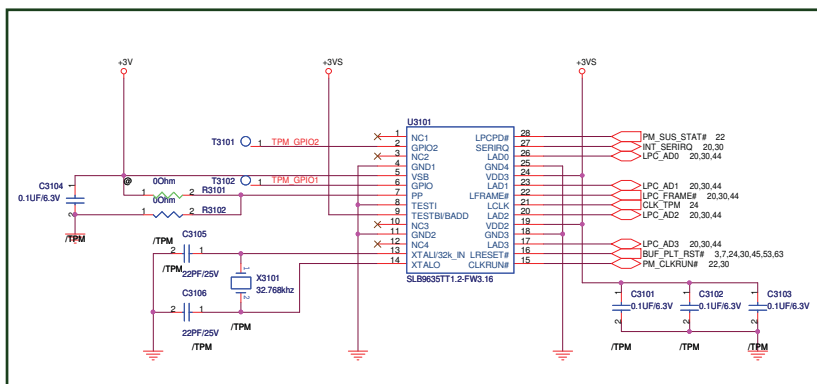
BOM_Note

Synaptics SMBUS TP option

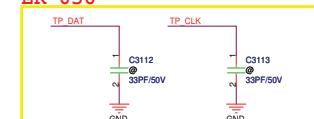
click pad option is for win8 requirement Function

PR-005

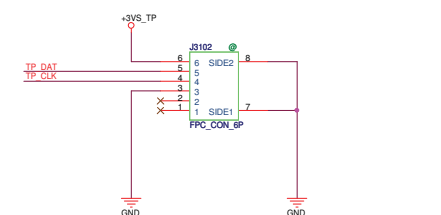
T/P

***TPM***

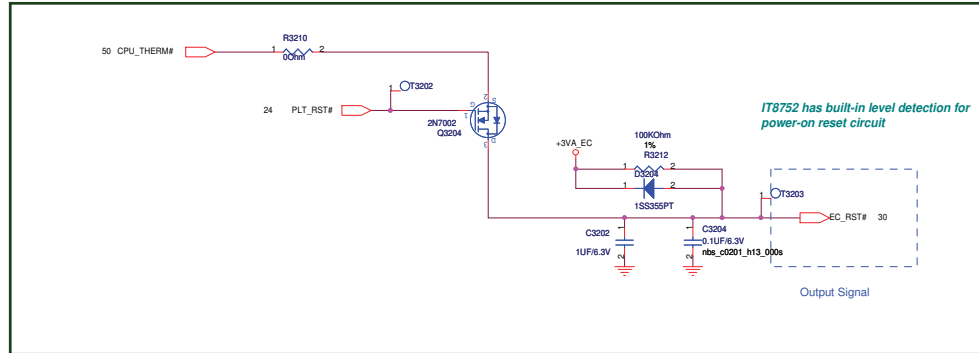
ER-036



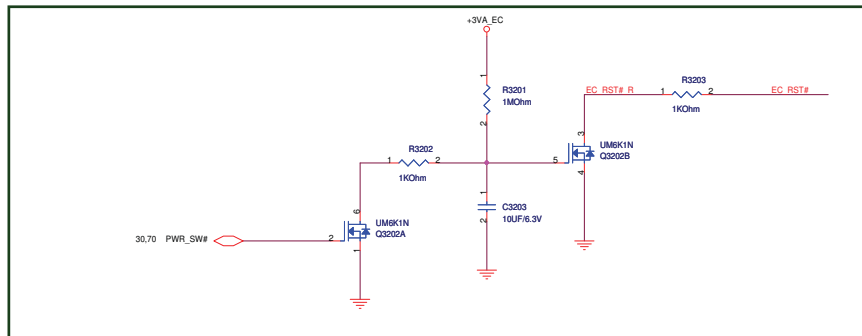
PR-010

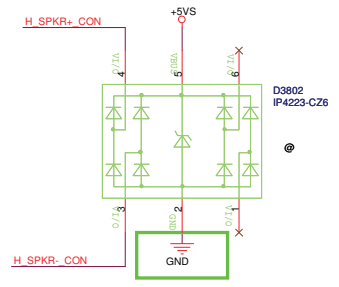
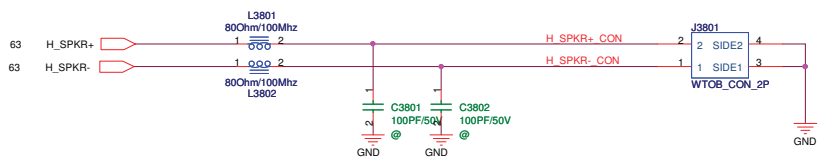


Thermal Policy



battery embedded (press pwr_sw 10sec, then reset ec)



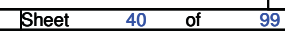


5

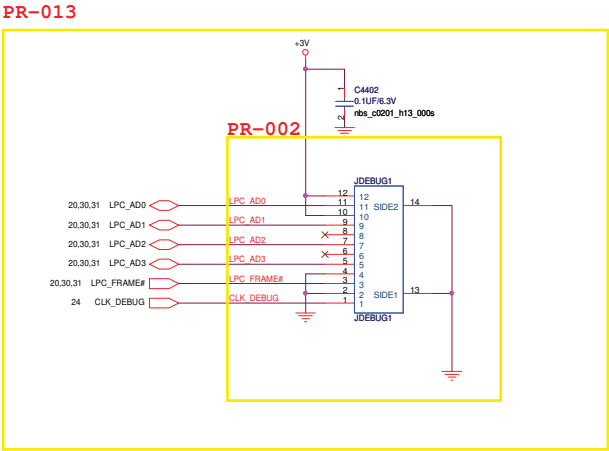
C

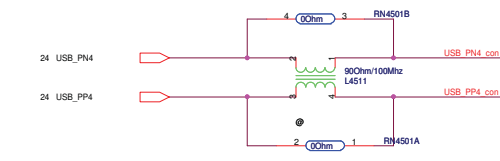
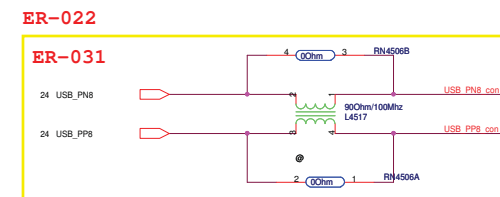
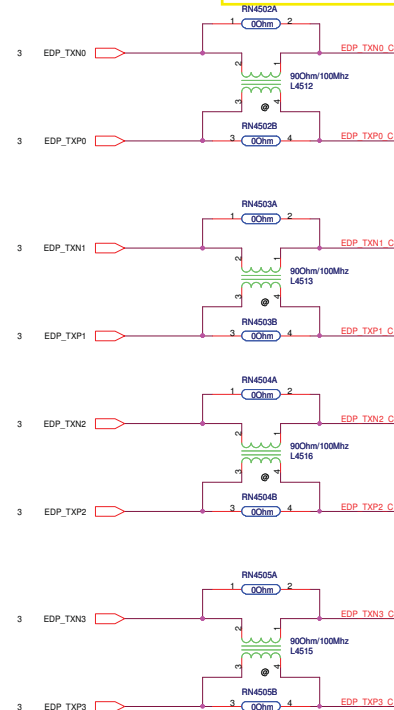
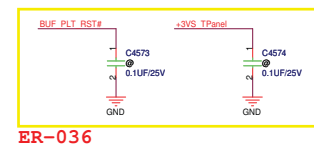
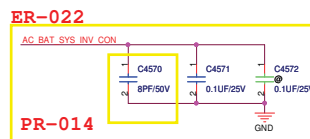
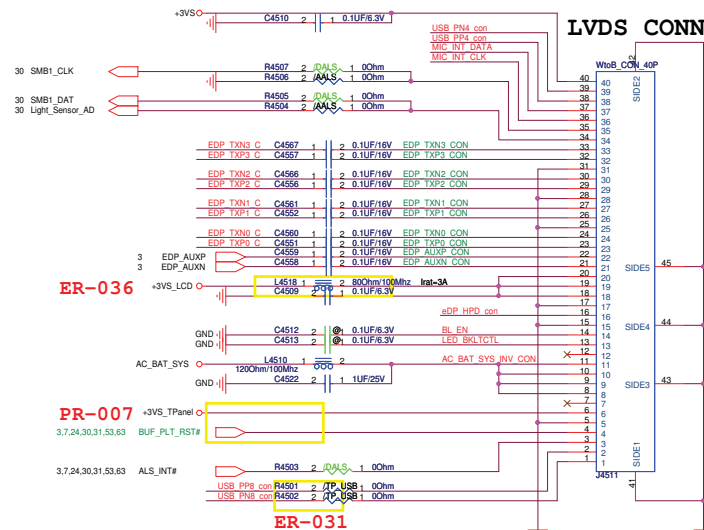
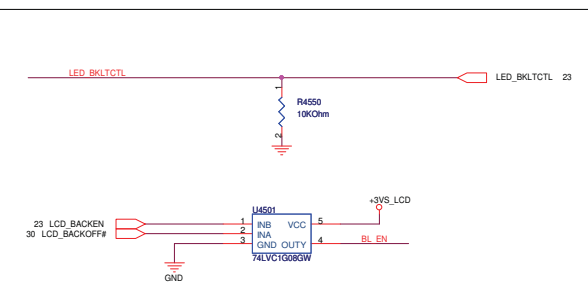
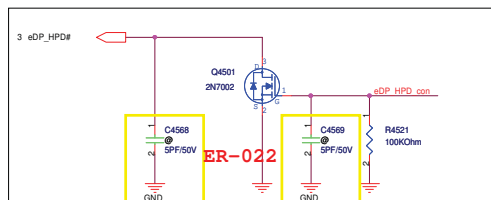
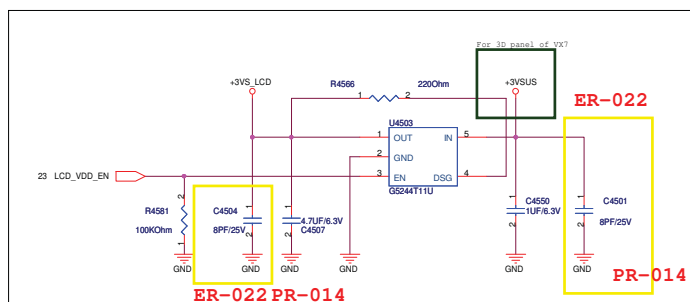
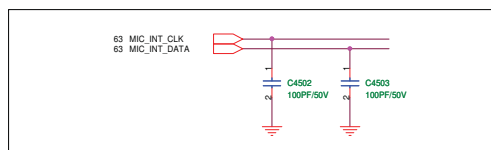
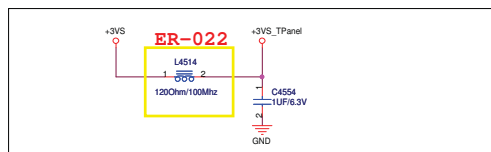
E

A

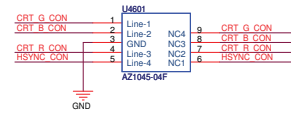
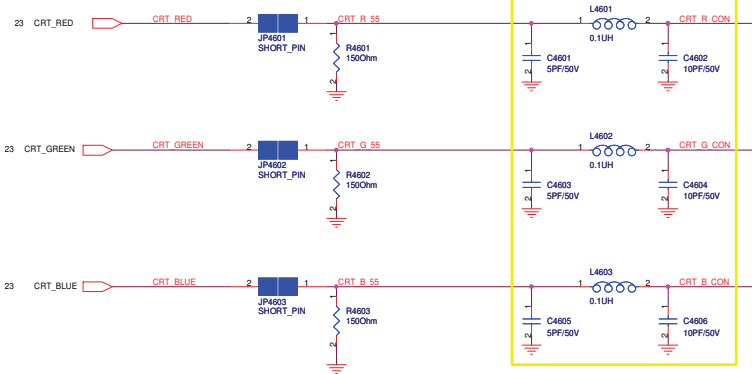


LPC Debug Port



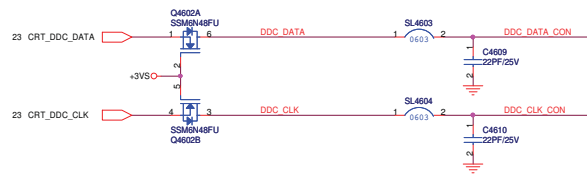
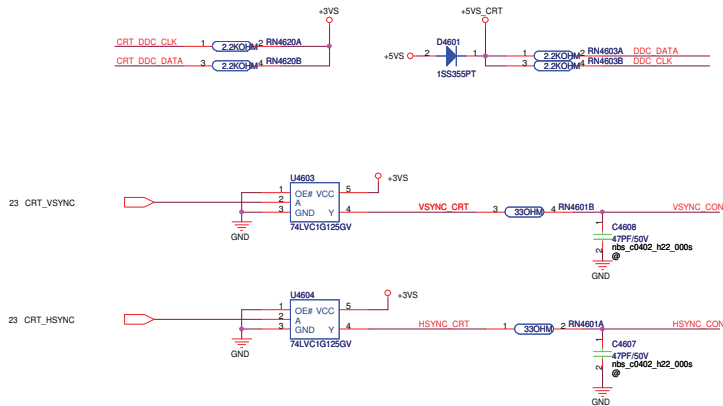
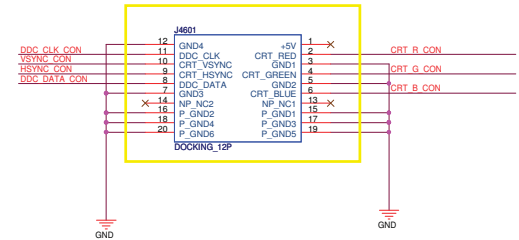


ER-030



ER-004

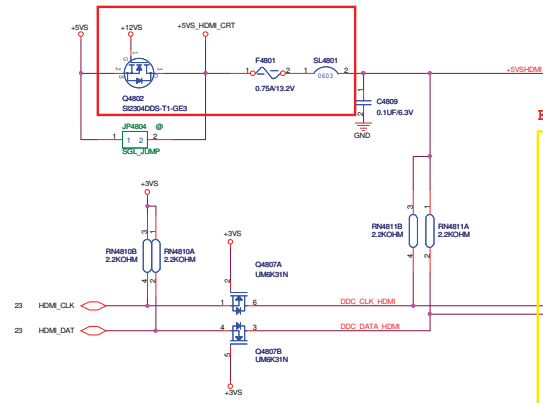
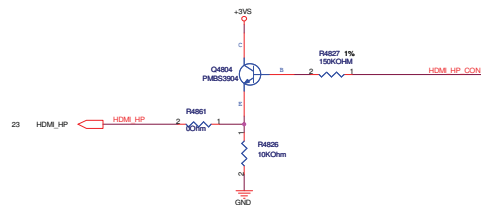
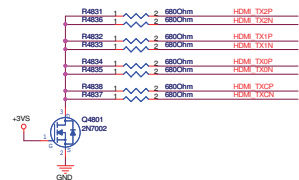
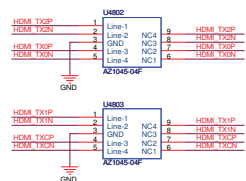
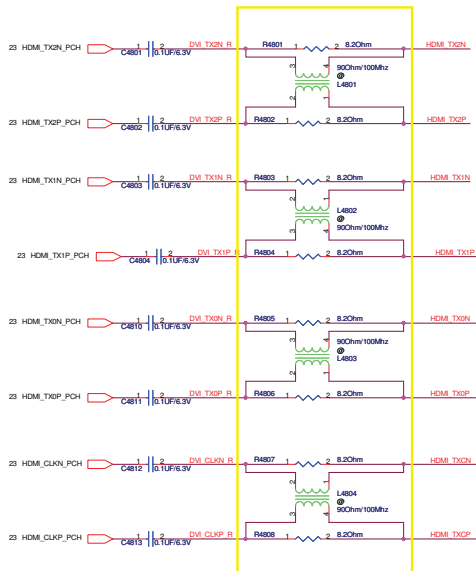
UX31EP 004 12/21



Close to CONNECTOR

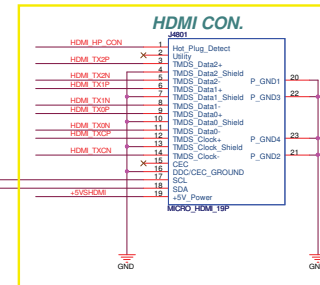
Near CON J4801

ER-022

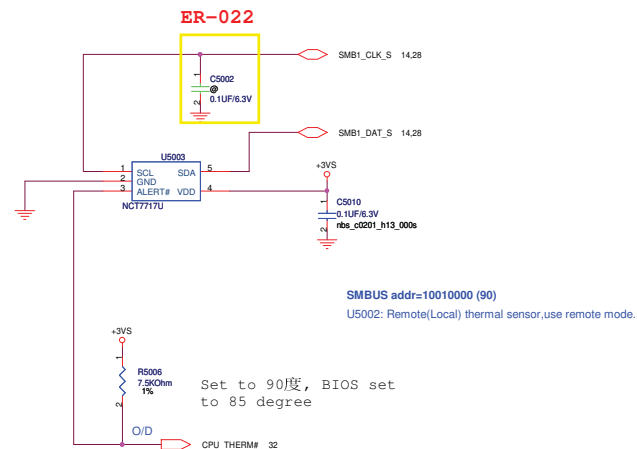


ER-005

UX31EP 005 12/21



CPU Thermal Sensor

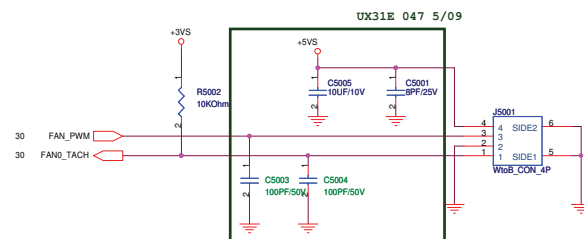


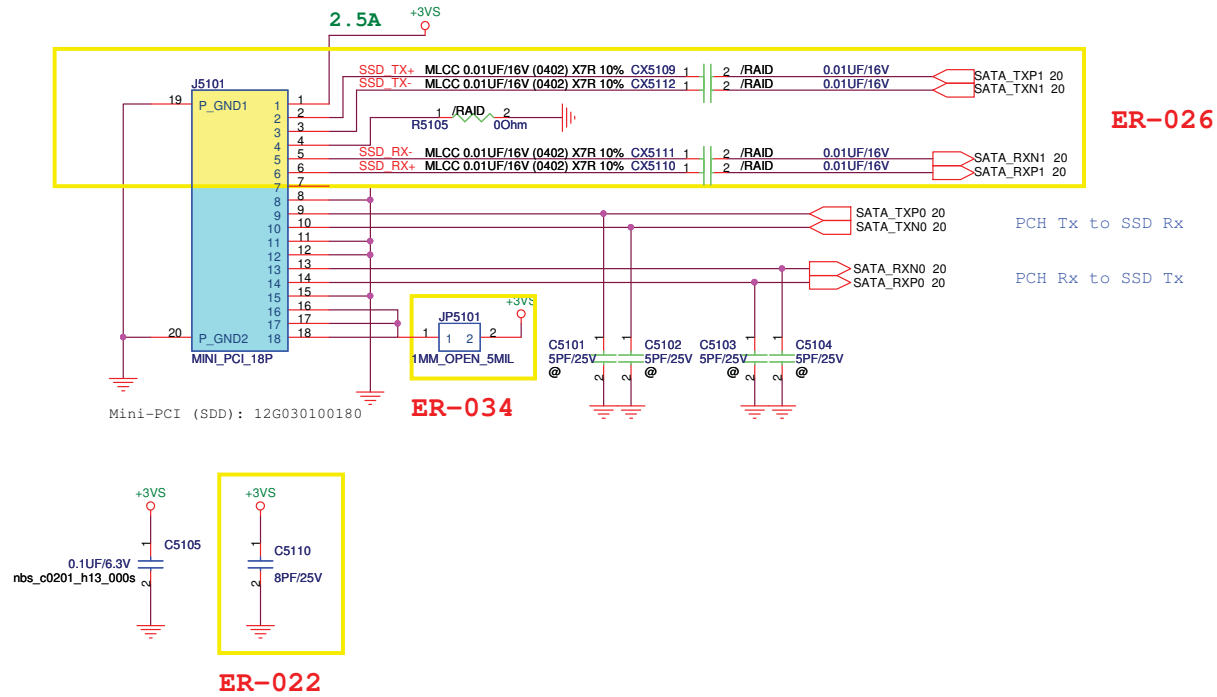
Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

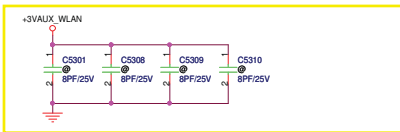
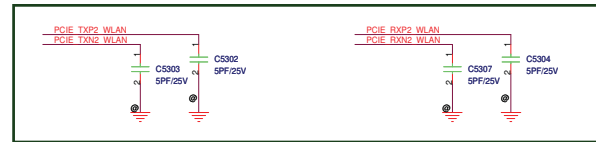
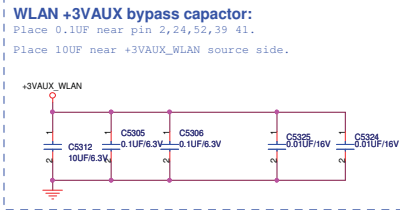
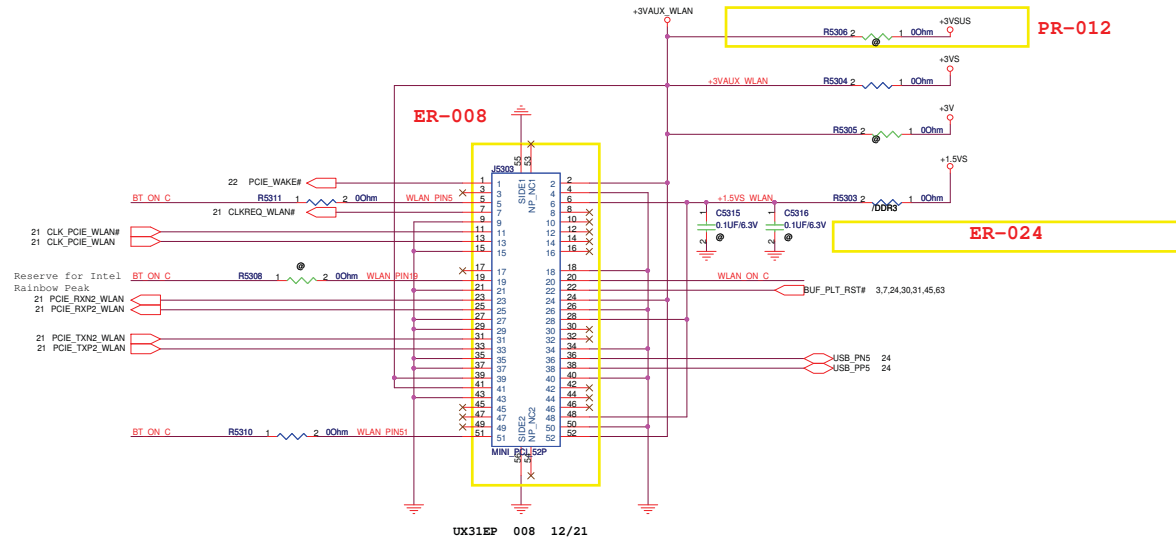
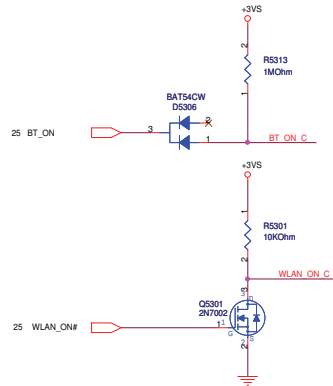
-----OTHER SIGNALS
10 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
10 mils
-----OTHER SIGNALS

Avoid FSB,Power

DC FAN Control

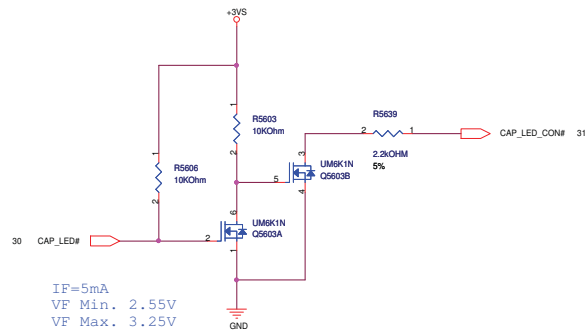




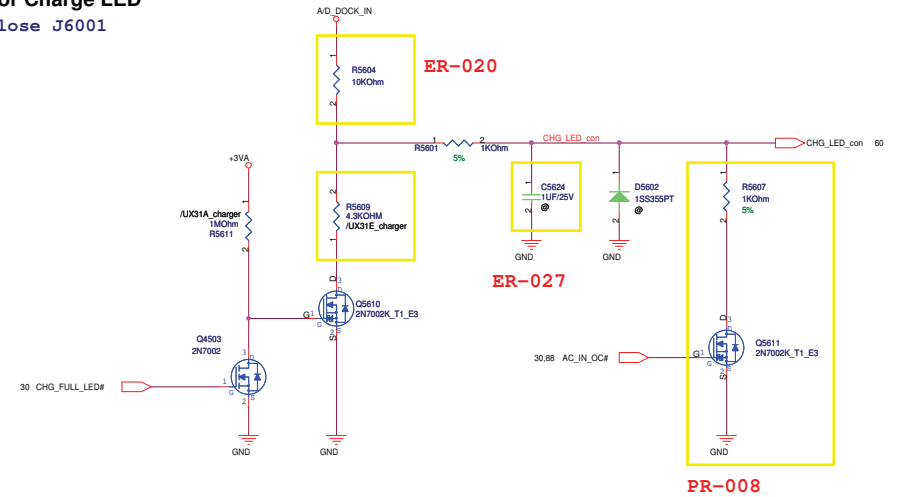


ER-022

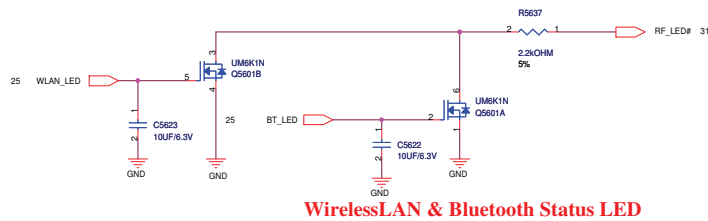
CAPS_LOCK LED



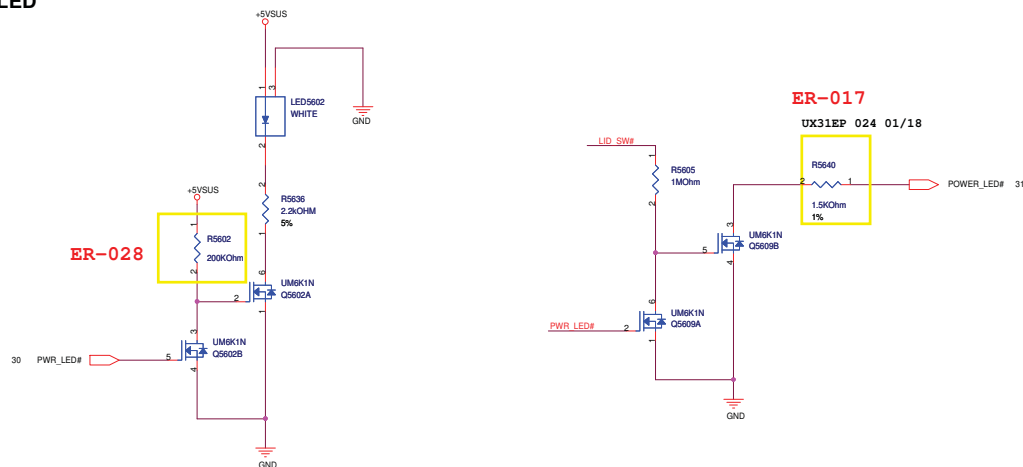
For Charge LED Close J6001



WireLess/BT LED

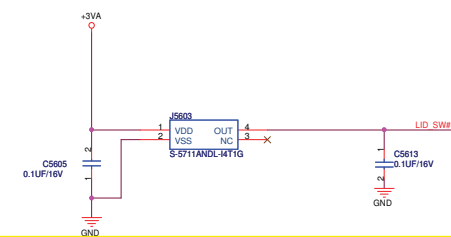


PWR LED

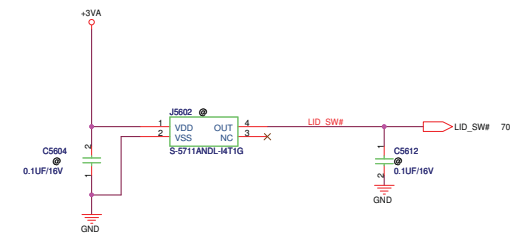


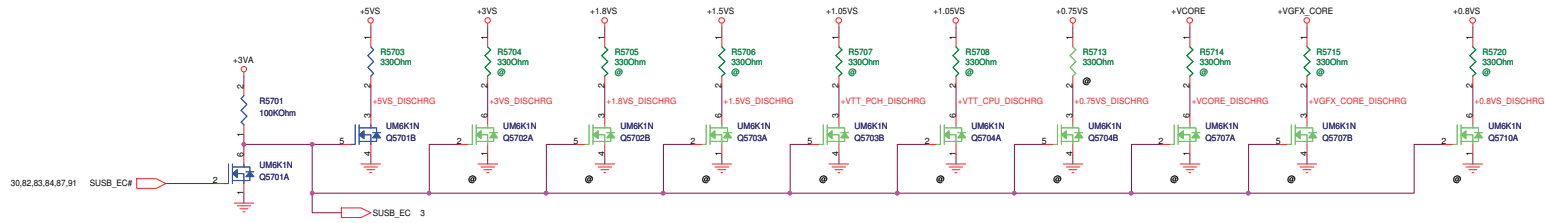
PR-003

LID SW (no TouchPanel)

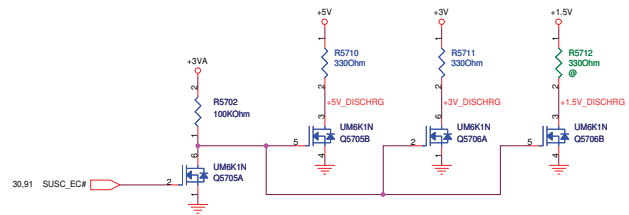


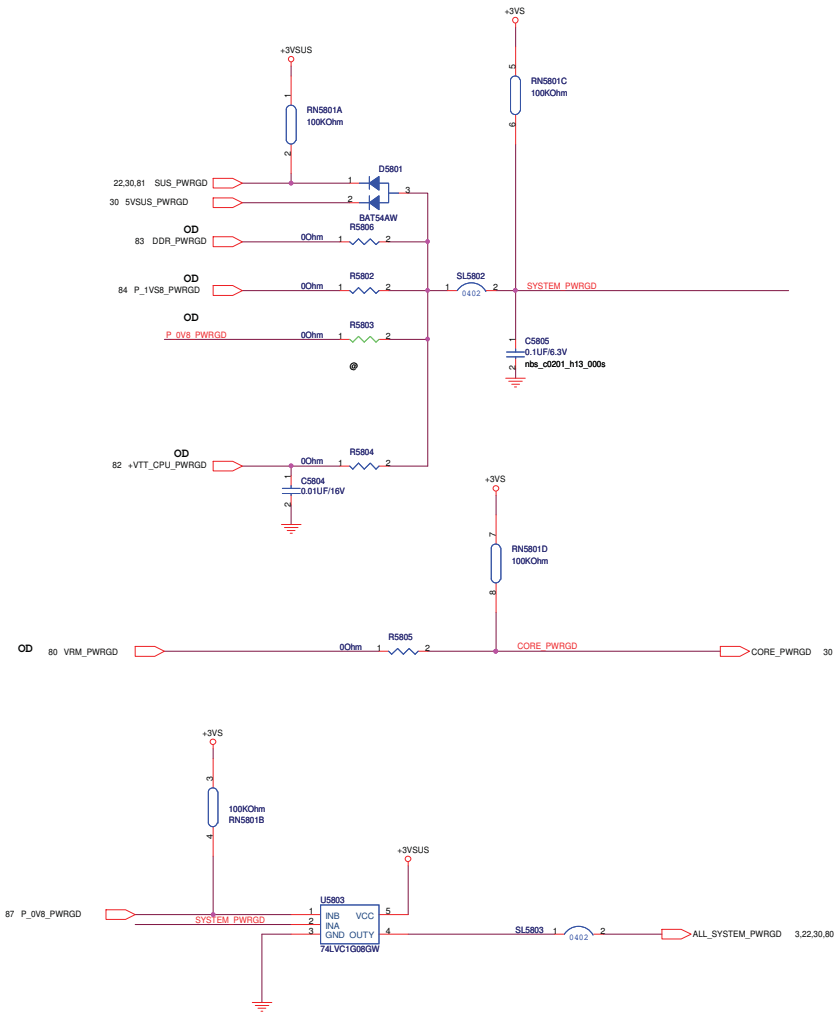
LID SW (for TouchPanel)



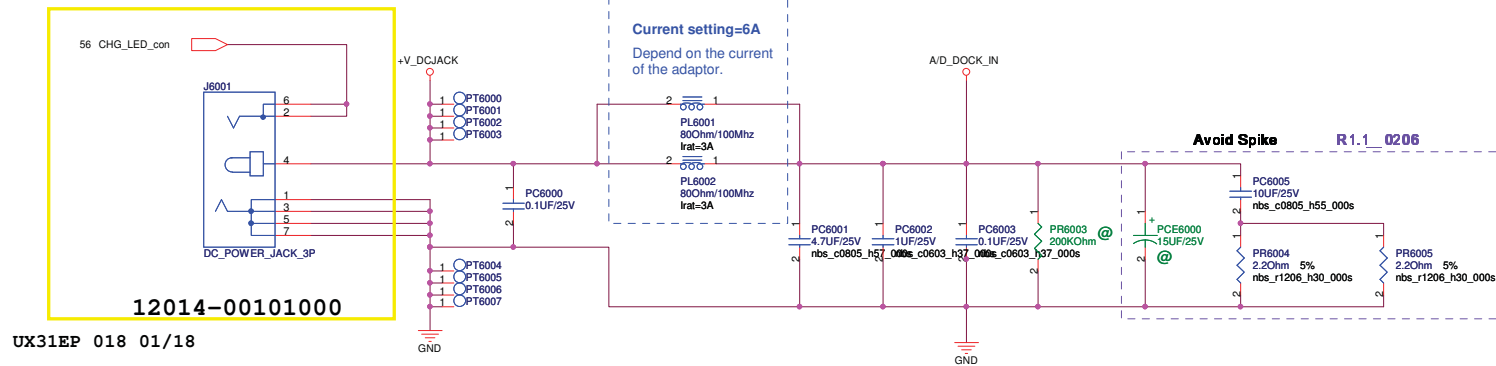


4/20 Stuff R5710 and R5711

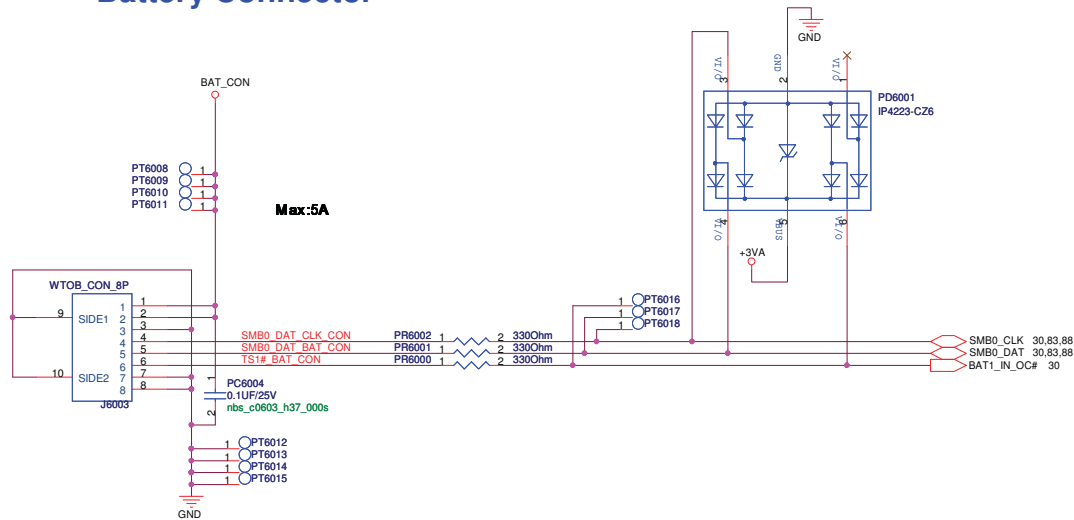




ER-015



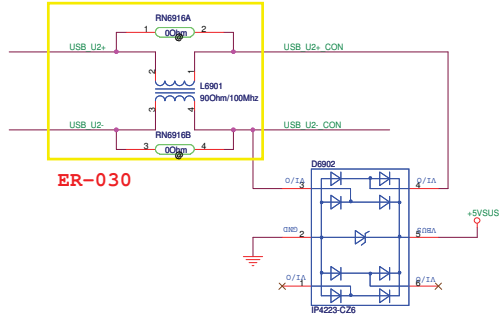
Battery Connector



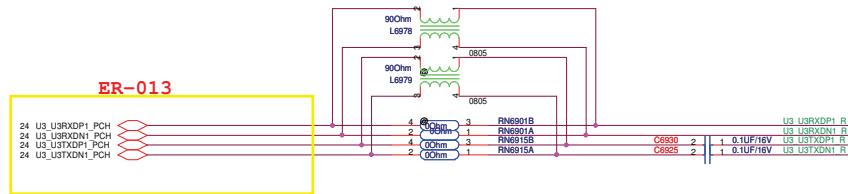
ER-013



USB2.0 EMI-Protection & ESD-Protection

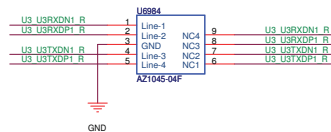


USB3.0 EMI-Protection



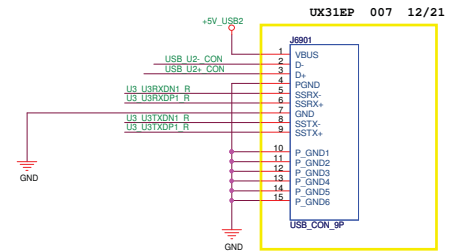
USB3.0 ESD-Protection

1st : 07G028076030
ESD PROTECTION AZ1045-04F
2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

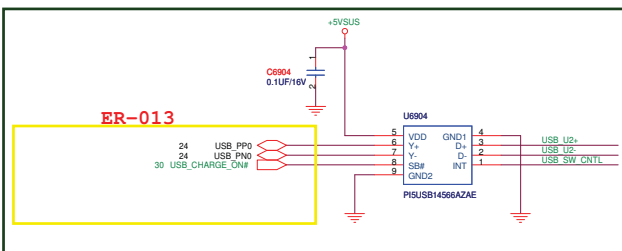


USB30 CONN

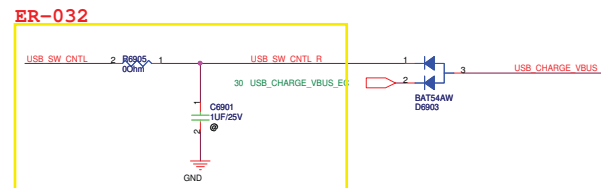
USB30 CONN
UX21 CON 12013-00011600



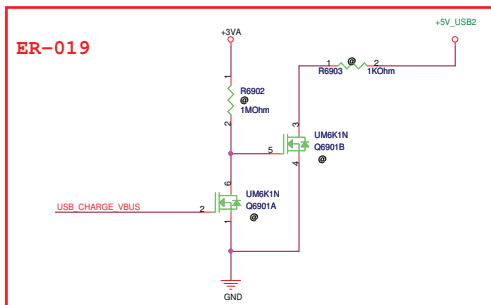
USB Charger



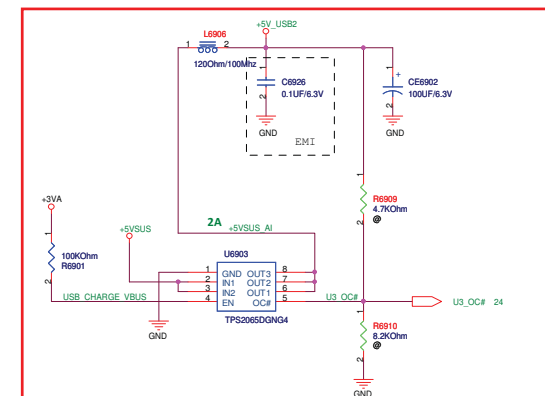
Charger_pwr_control & DC mode low voltage control



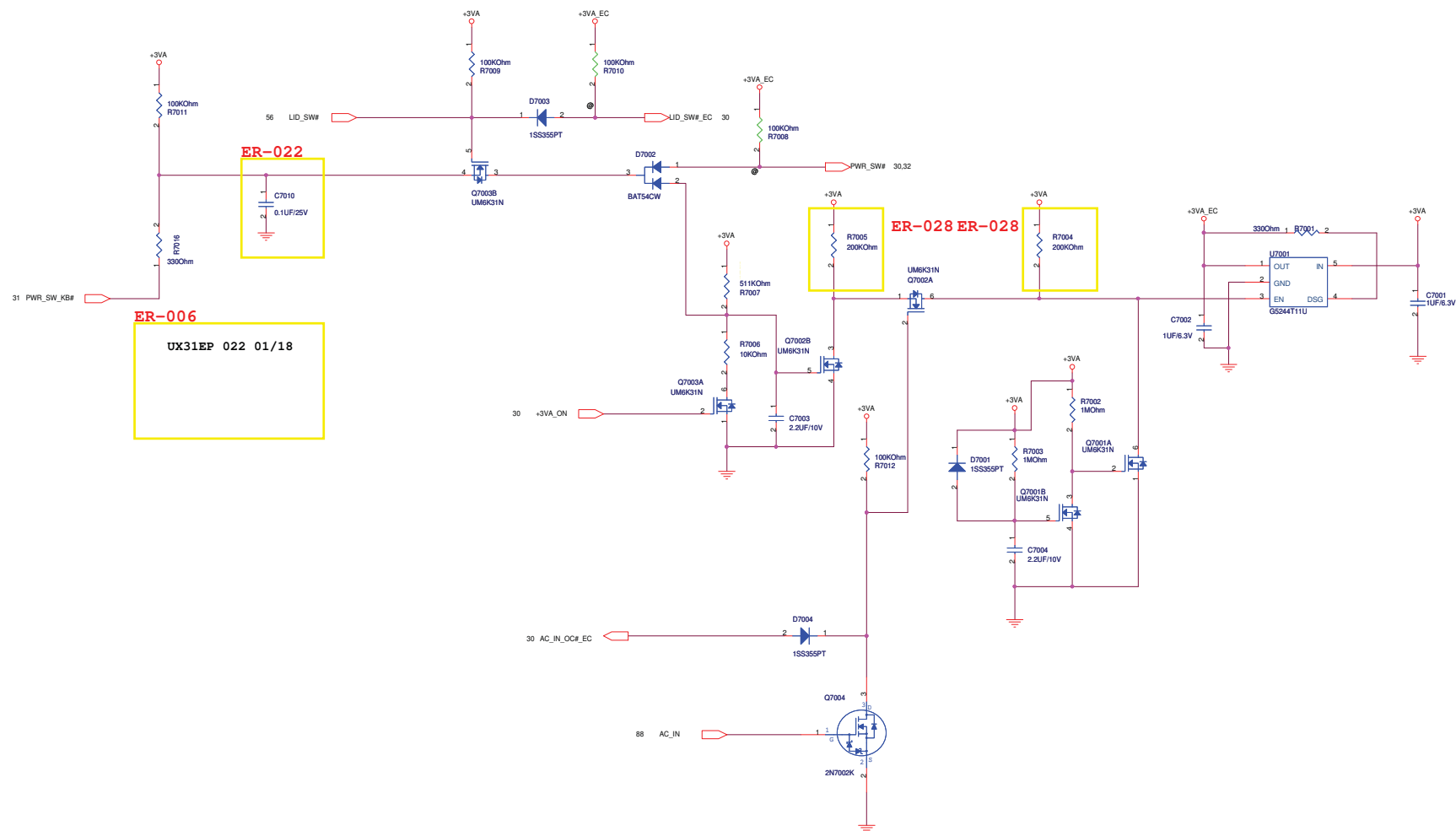
VBUS_discharger

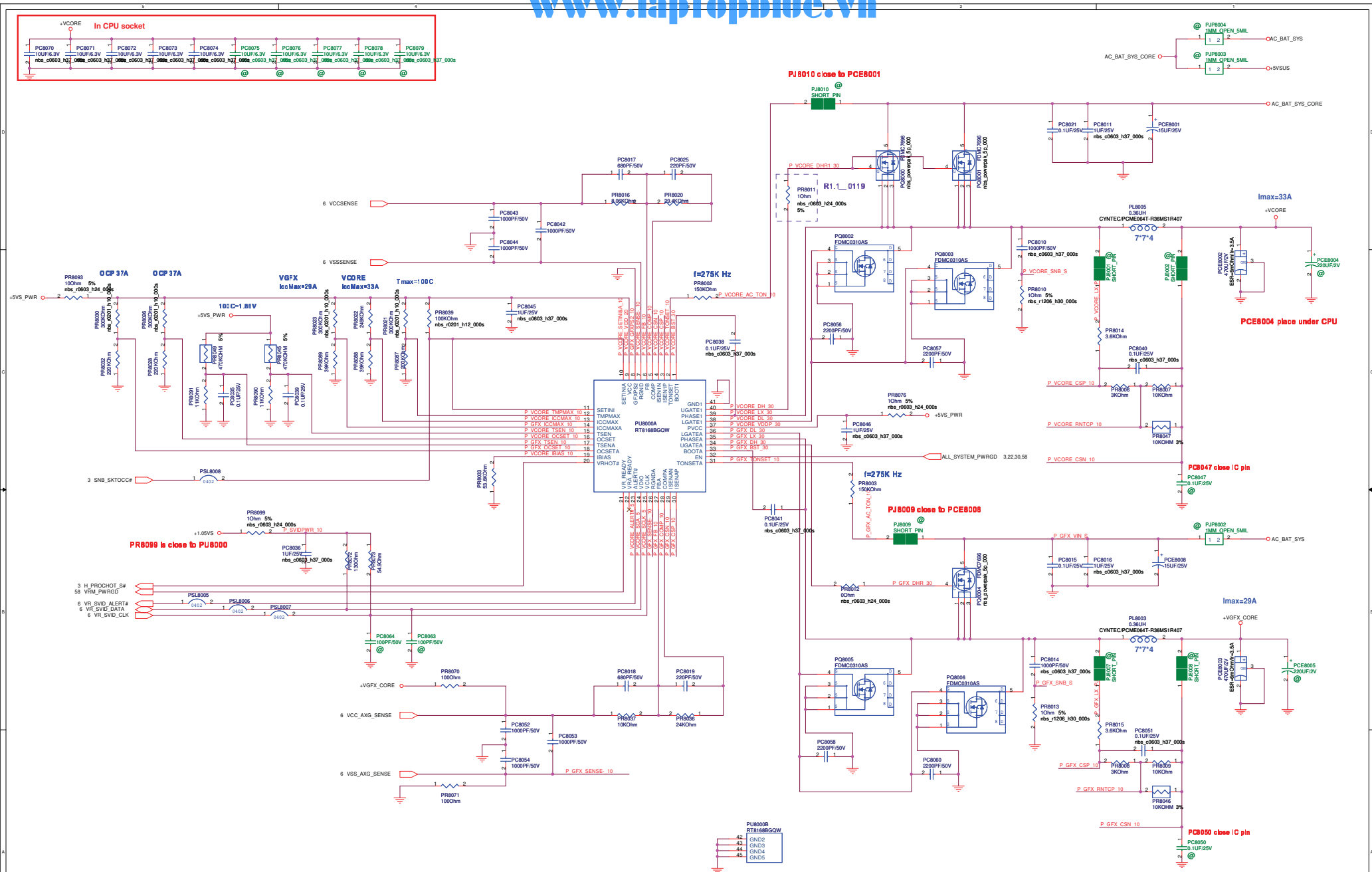


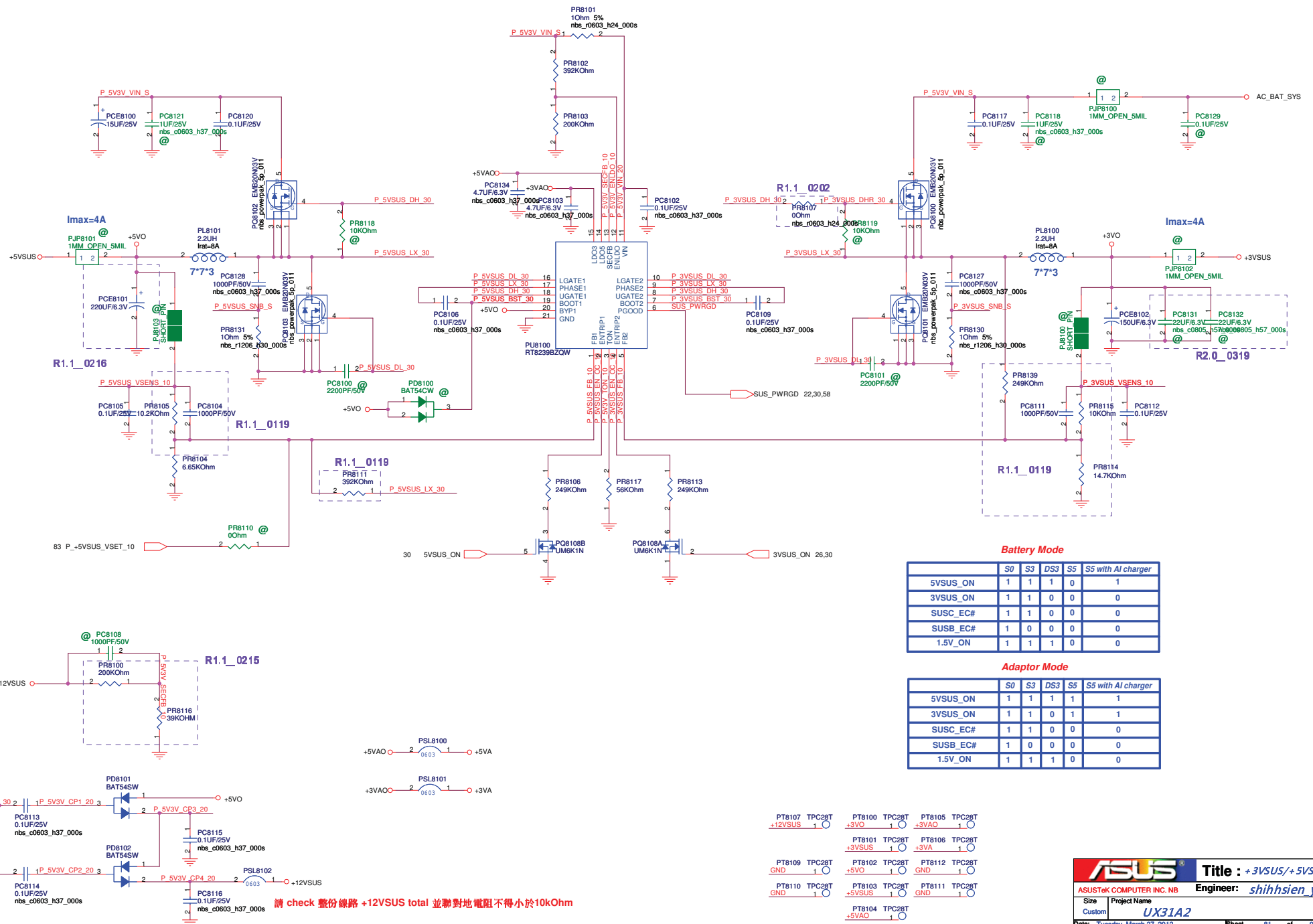
USB_SW VBUS Contorl Circuit



Using TI IC, then the
iphone4S can't charger
in S4&S3 mode.



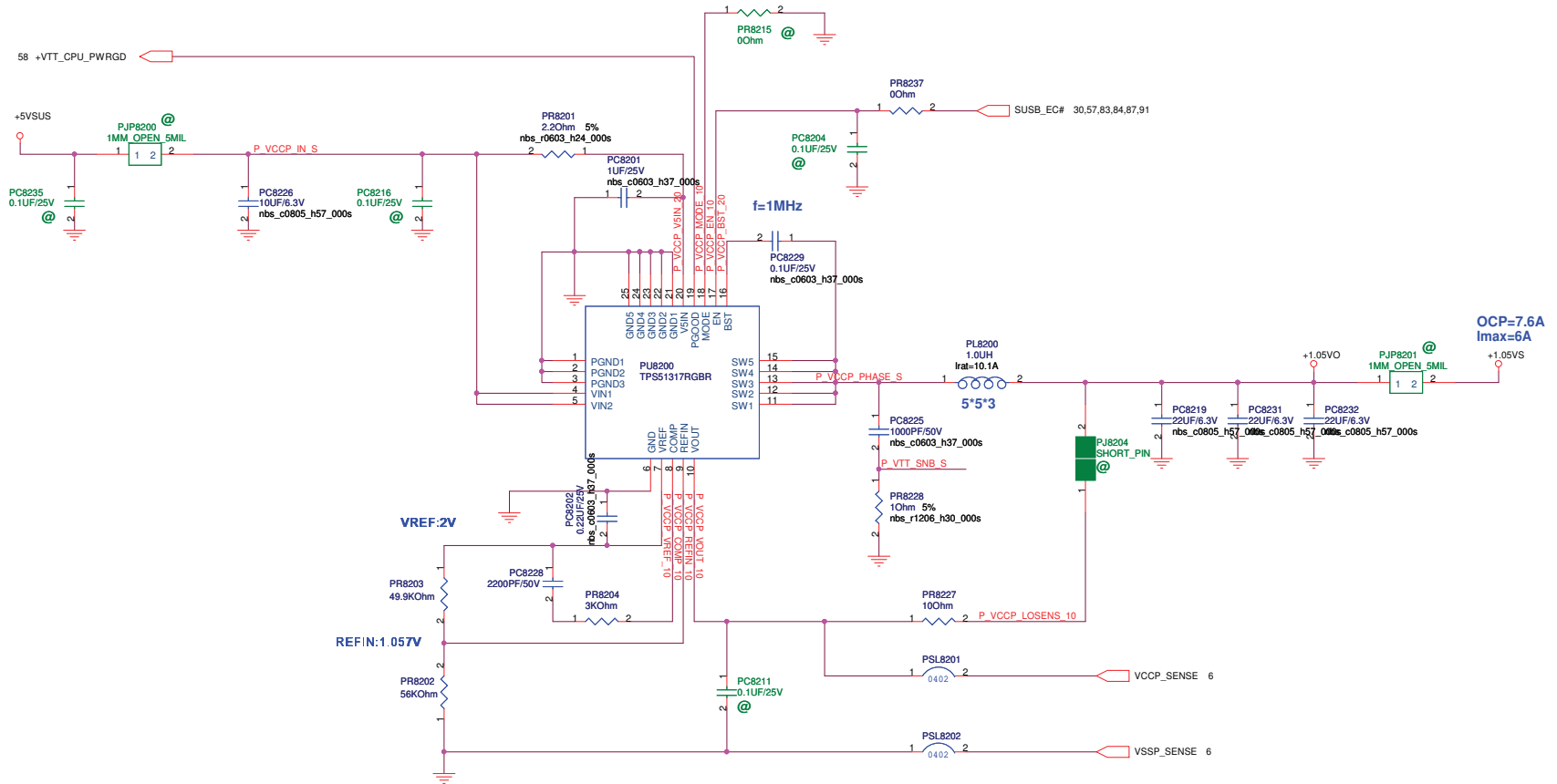




	S0	S3	DS3	S5	S5 with AI charger
5VSUS_ON	1	1	1	0	1
3VSUS_ON	1	1	0	0	0
SUSC_EC#	1	1	0	0	0
SUSB_EC#	1	0	0	0	0
1.5V_ON	1	1	1	0	0

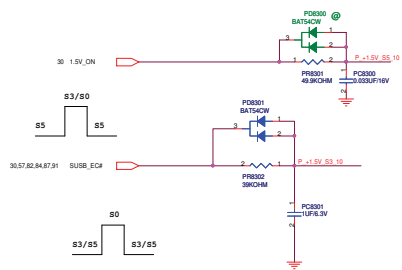
	S0	S3	DS3	S5	S5 with AI charger
5VSUS_ON	1	1	1	1	1
3VSUS_ON	1	1	0	1	1
SUSC_EC#	1	1	0	0	0
SUSB_EC#	1	0	0	0	0
1.5V_ON	1	1	1	0	0

+VTT_CPU & +VTT_PCH & +1.05VS POWER SUPPLY



<Variant Name>

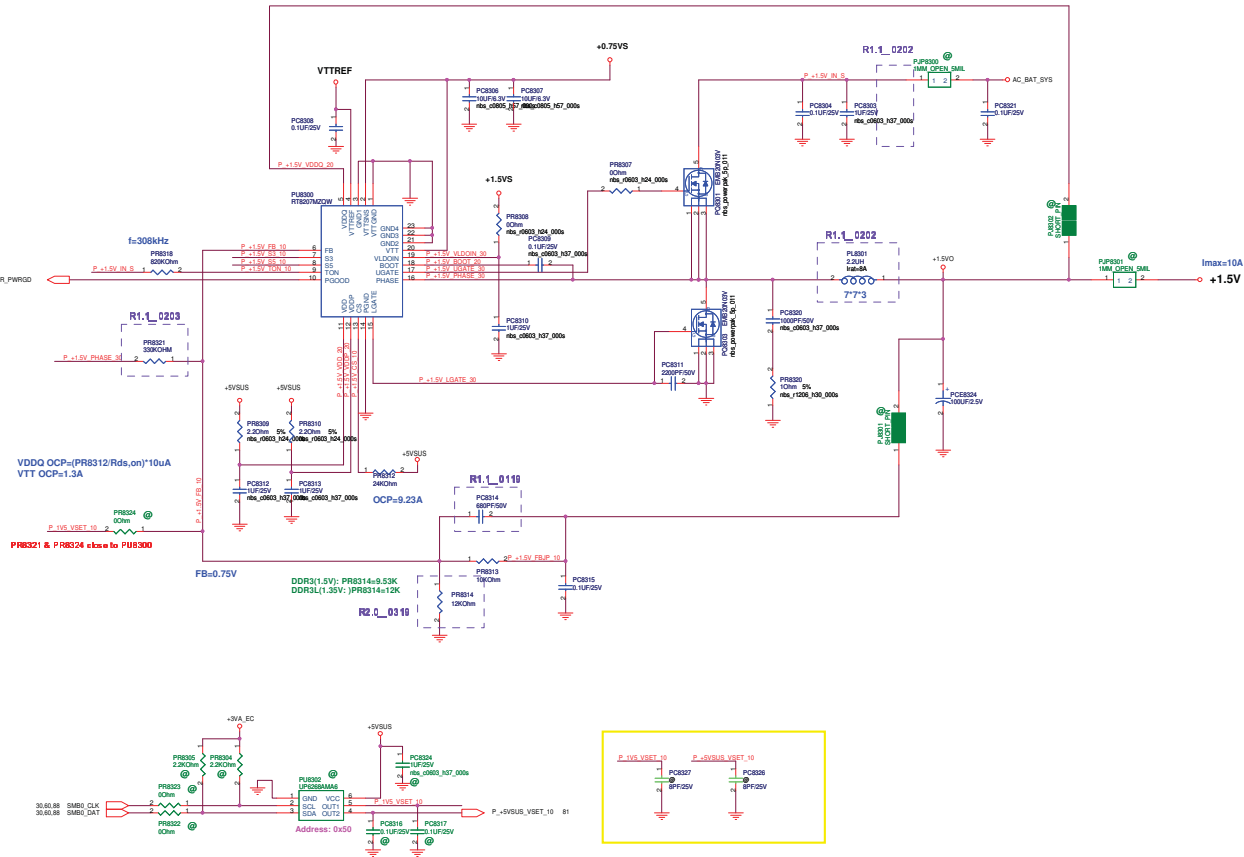
ASUS		Title : +1.05VS	
ASUSTek COMPUTER INC. NB		Engineer: shihhsien yang	
Size	Project Name	Rev	
Custom	UX31A2	R2.0	
Date: Tuesday, March 27, 2012		Sheet 82 of 99	

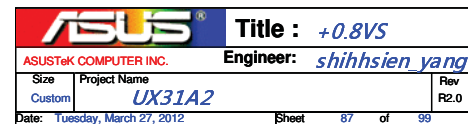


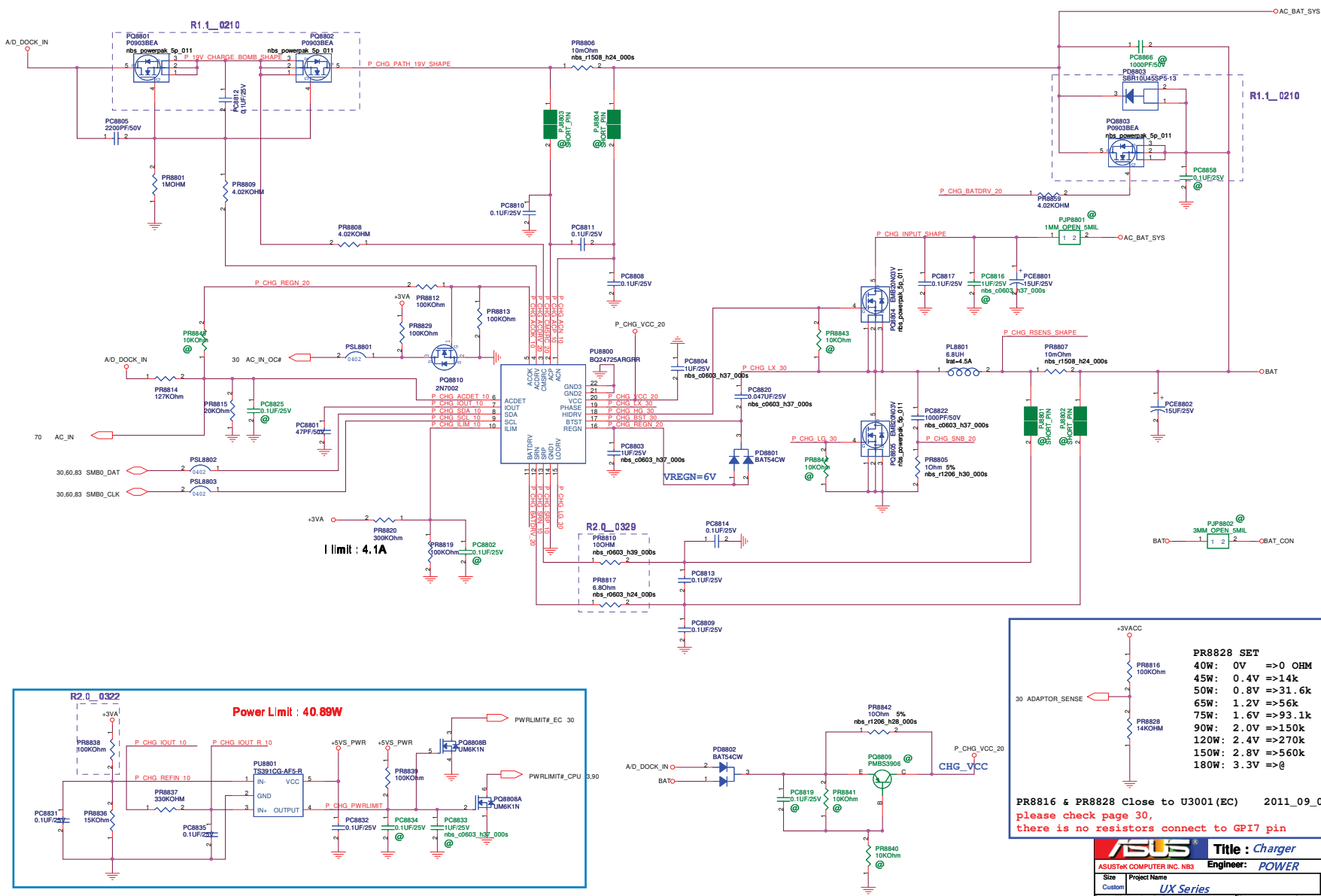
S3 And S5 Truth Table

State	S3	S5	VDDQ
S0	1	1	On
S3	0	1	On
S4/S5	0	0	On

State	VTTREF	VTT
S0	On	On
S3	On	Off (H-Z)
S4/S5	Off (Discharge)	Off (Discharge)

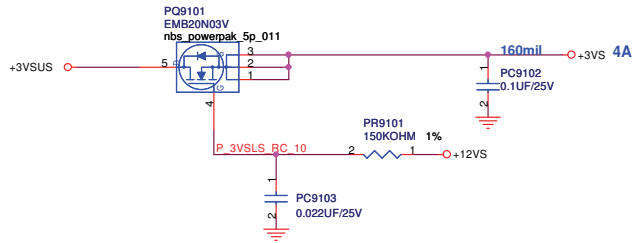
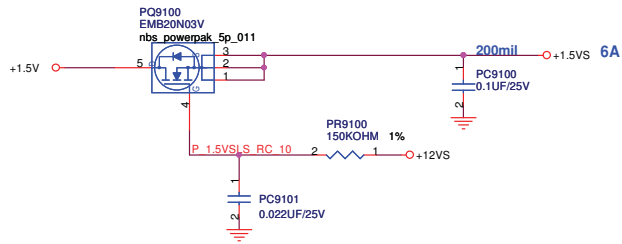




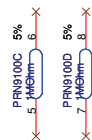
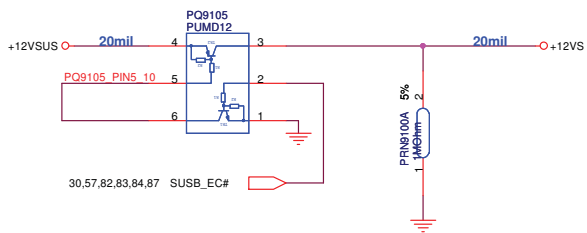
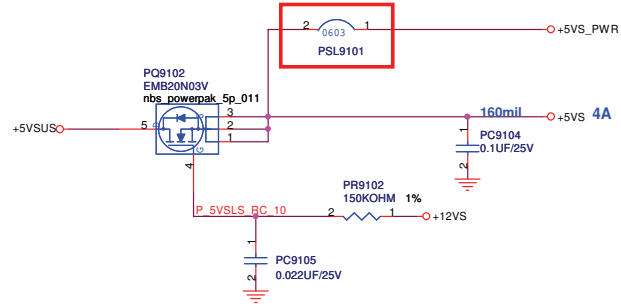


		Title : <i>Charger</i>	
ASUSTeK COMPUTER INC. NB3		Engineer: <i>POWER</i>	
Size Custom	Project Name <i>UX Series</i>		Rev 1.0
Date: <i>Wednesday, April 11, 2012</i>		Sheet <i>88</i> of <i>97</i>	

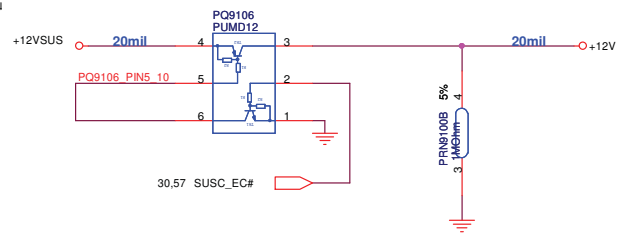
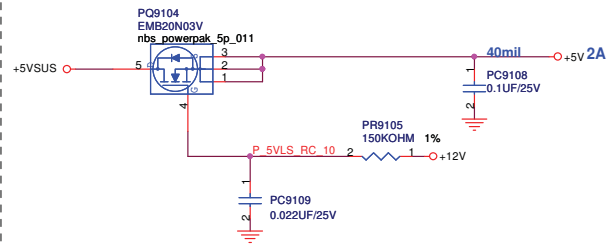
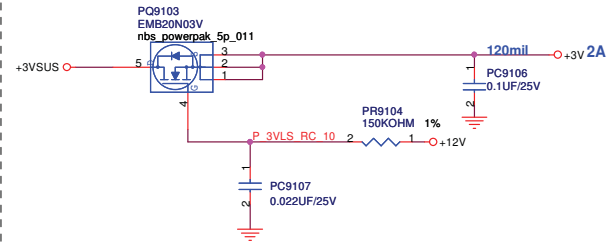
SUSB#_PWR POWER



PSL9101 請擺在 PQ9102 旁邊



SUSC#_PWR POWER



<Variant Name>

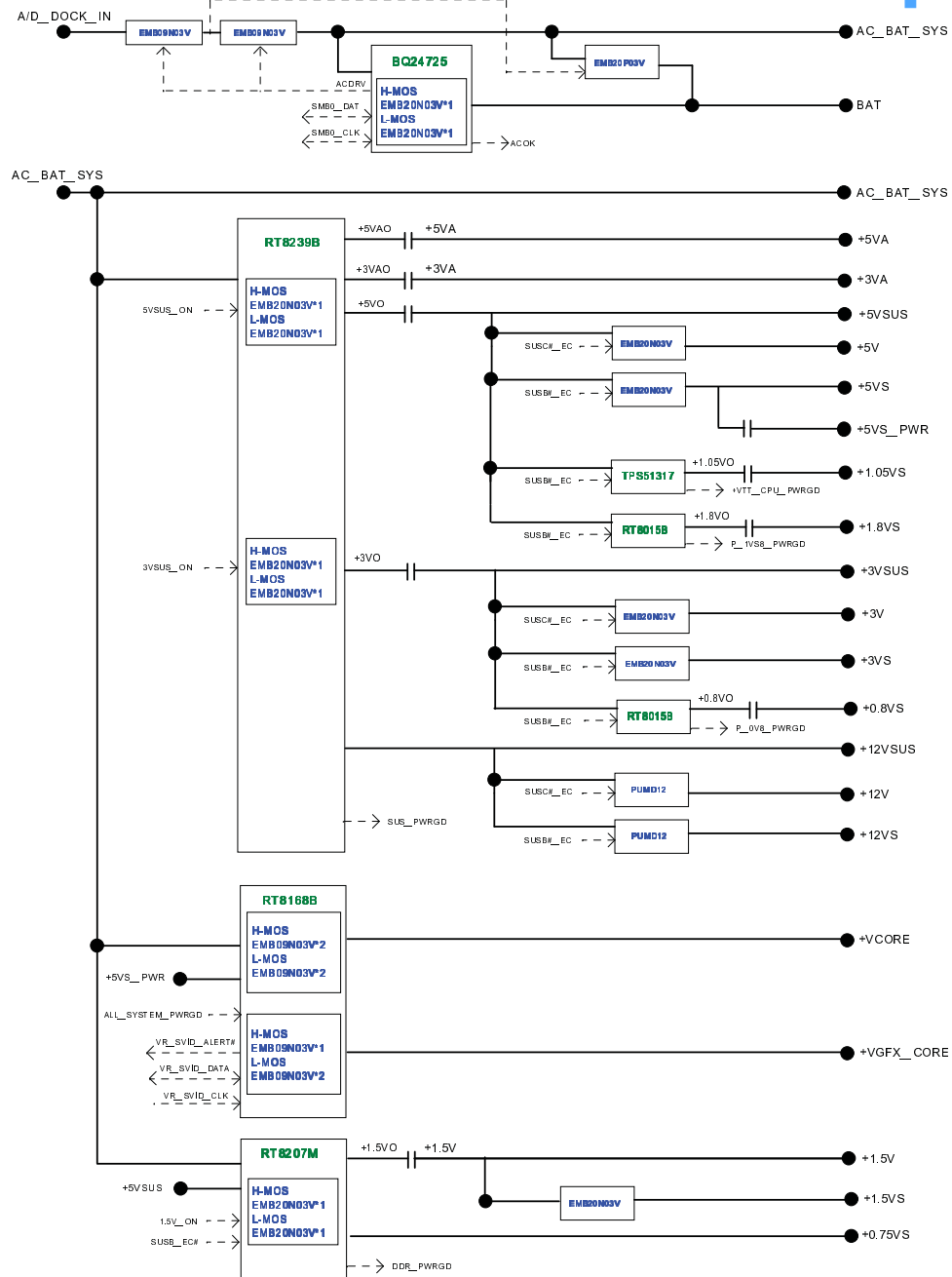


Title : *Load Switch*

ASUSTeK COMPUTER INC. NB Engineer: *shihhsien_yang*

Size Custom	Project Name <i>UX31A2</i>	Rev R2.0
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Date: Tuesday, March 27, 2012 Sheet 91 of 98






[U36SD] R1.1

- 1. Change source of PQ9102 and PQ9104 from +5VSUS to +5VSYS p91
- 2. transform pin1,4,7,10 trace to +1.7v_lan p34
- 3. WLAN clk_req1 follow u36jc pull low p21
- 4. ALC269 pin9 trace to +3vsus for leakage current p36
- 5. EC PIN3 is NC p30
- 6. Add ESD protect part for HDMI p48
- 7. Add capacitance for EMI request on H_CPUPWRGD p25
- 8. Change C3404 trace from GND_LAN to GND p34
- 9. Follow U36JC CRT solution p46

[M61JA] R1.0 => R1.1

1. Follow E.E RC delay
+5v R9107 100K change to 68K
+3v R9106 200K change to 121K
+1.5v R8306 49.9K change to 68K
+5VS R9104 200K change to 68K
+3VS R9103 200K change to 121K
+1.8VS R8401 33.2K change to 121K
+1.5VS R9102 470K change to 390K
+1.05VS R8252 39K change to 200K
+0.75VS R8312 0 change to 2.49K C8310 0.1U change to 2.2U
- 2.VR_VID0~2 pull high 1K VR_VID6 pull low 1K.
- 3.U8401 RT8015A change to RT8015B
- 4.Reserve GVR_VID0~VID6 pull high and low resistor R8627~R8633
- 5.Reserve R8517~R5720 pull high & pull low resistor for MCP_CORE_VID
- 6.page86 component option change to ARD (CFD no stuff)
- 7.R8004 option change to CFD & R8049 change to ARD(For IMON)
- 8.Change RN8801A RN8801B(layout request)
- 9.R8517 R8519 change to stuff
- 10.R8406 13K change to 12K
- 11.CE8005 no stuff , CE8007 stuff
- 12.C8403 C8406 size 0603 change to 0805
- 13.R8213 R8305 ohm change to 2.2 ohm
- 14.R8621~R8633 stuff 1K ohm
- 15.R8512 change form 200K to 33K ohm
- 16.VTT_PCH component option change to CFD
- 17.Delete U8502 & GPU_PWRON signal change to GPU_PWRON_1.8VSG_&_3.3VSG
- 18.L8601 1uH => 0.56uH , C8608 0.01uF/50 => 0.01uF/16V , R8621 43K => 36K , C8617 =>0.1uF/16V 1uF/10V ,
C8607 68pF/50V => 33pF/50V , R8625 10K => 18.7K , R8613 3.6K => 4.02K
- 19.R8057 change form 10K to 2.05K
- 20.Add Q8007 & Q8008 form thermal issue

		Title : System History	
ASUSTeK COMPUTER INC. NB		Engineer:	
Size Custom	Project Name UX31A2		Rev
Date: Tuesday, March 27, 2012		Sheet	96 of 99

ER

001 Page 13 & 14 : add +0.75VS de-coupling capacitors for channel B by samsung simulation recommend , and add +1.5V de-coupling capacitors around U1404 by samsung simulation recommend

002 Page 65 : remove U6511~14, U6516

003 Page 31: change J3101 to 12G183000403 and add PWR_SW ~ PWR_LED function on Keyboard

004 Page 46 : change J4601 to 12019-00020000

005 Page 48 : change J4801 to 12022-00013700

006 Page 70 : remove SW7001

007 Page 69 : change J6901 to 12013-00011600

008 Page 53 : change J5303 to 12003-00020700

009 Page 30 : swap EC GP20 and GPH4 for EC request

010 Page 30 : +3VA ON pull low

011 Page 30 : add R3002 for without Light sensor system

012 Page 30 : unmount R3084, mount R3083 for S4/S5 EC power down

013 Page 21,68,69 : remove about FL1009 circuit

014 Page 06 : modify R0617, R0618 to 1K follow intel DG

015 Page 60 : change J6001 to 12014-00101000 for MP

016 Page 28 : change U2801 to 05006-00010300 (64M)

017 Page 56 : add R5640 for PWR_LED current limit

018 Page 24,25 : change (H_SMB_INV#) AV10 to AV1 for following VC circuit.

019 Page 69 : add +5V USB2 discharge for AI-charger function fail on iPhone 4S

020 Page 56 : Change R5604 size from 0201 to 0402.

021 Page 23 : Reserve 5pF cap. of RGB signals for EMI suggestion.

022 Page 45 : Reserved 8pF cap. to +3VS_LCD & +3VSUS for RF suggestion.

Page 45 : Reserved 5pF cap. to G & D sides of Q4501 for RF suggestion.

Page 45 : Reserved 5pF cap. to G & D sides of Q4501 for RF suggestion.

Page 45 : Reserved 0.1pF cap. to AC_BAT_SYS_INV_CON for RF suggestion.

Page 45 : Changed R4503 to L4514 for RF suggestion.

Page 45 : Colay USB_PP2 0 ohm & choke for RF suggestion.

Page 13 : Add cap. to +1.5V for RF suggestion.

Page 14 : Add cap. to +1.5V for RF suggestion.

Page 15 : Add cap. to +1.5V for RF suggestion.

Page 48 : Colay HDMI ohm & choke for RF suggestion.

Page 50 : Reserved cap. to SMB1_CLK_3 for RF suggestion.

Page 51 : Reserved cap. to +3VS for RF suggestion.

Page 53 : Reserved cap. to +3VAUX_WLAN for RF suggestion.

Page 70 : Reserved cap. to pin 4 of Q7003 for RF suggestion.

Page 70 : Reserved cap. to pin 4 of Q7003 for RF suggestion.

Page 63 : Reserved cap. to +3V for RF suggestion.

Page 63 : Reserved cap. to net of for RF suggestion.

Page 20 : Reserved R2009 for RTC battery change type.

024 Page 26 : Deleting R2606 for DDR3L power change path.

Page 53 : Deleting R5302 for DDR3L power change path.

025 Page 28 : Add cap. to pin 5-8 of SPT ROM for RF suggestion.

026 Page 20 & 51 : Add SATA_TX1 net to SSD for SSD support RAID

027 Page 56 : Change R5609 and reserve C5624 for DC jack change size.

028 Page 26 : Change resistor value of R2630 to 511K ohm and change size from 0201 to 0402 for reducing power consumption.

Page 70 : Change resistor value of R7004 ~ R7005 to 200K ohm for reducing power consumption.

Page 56 : Change resistor value of R5602 to 200K ohm for reducing power consumption.

029 Page 25 : Change R2529 ~ R2530 ~ R2531 for following sedding schematic design.

030 Page 46 : Change C4602 ~ C4604 ~ C4606 cap. value to 10PF and L4601 ~ L4602 ~ L4603 for EMI suggestion & EA measure pass.

Page 24 : Change R2428 resistor value to 39 ohm for EA measure pass.

Page 69 : Delete RN6916 and add L6901 for EMI suggestion.

031 Page 24 & 45 & 63 : Change USB port2 & port3 to port 8 & port 9 for BIOS suggestion.

032 Page 69 : Add R6905 & C6901 for USB problem.

033 Page 27 : Change power plane of VCCDSW3_3 for supporting hybrid sleep mode.

034 Page 51 : Add JP5101 for measurement.

035 Page 63 : Add 0.1uF cap. to +3VS & +5V for RF suggestion.

036 Page 45 : Reserve 0.1uF cap. to BUF_PL1_RST# & TPANEL_INT#_C for EMI suggestion.

Page 31 : Reserve 0.1uF cap. to TP_DAT & TP_CLK for EMI suggestion.

Page 45 : Add L4518 to +3VS_LCD for EMI suggestion.

037 Page 14 & 15 : Change C1416 & C1501 cap. value from 8PF to 0.1uF for RF suggestion.

PWR modify

Page 88 : Updating CHG IC to BQ24725A

Page 88 : Add shut down sche.

Page 90 : Add HW throttle sche.

Page 90 : Add PR8107 for WLAN noise.

Page 83 : Delete PCE8301 for WLAN noise.

Page 83 : Change PL8300 to 2.2uH for WLAN noise.

Page 83 : Add PC8326 ~ PC8327 for RF suggestion.

Page 83 : Add PR8321 to 330K

Page 83 : Change PR8314 to 9.53k

Page 60 & 90 : Change BOM

Page 81 & 90 : Change BOM & sche. for power design ip sche change.

Page 81 & 90 : Change BOM PCE8101 to 220uF, and FR9005 to 49.9k ohm

PR

001 Page 03 : Change U0303 to 06G004753010 for CR sche.

002 Page 44 : Change JDBUG1 to 12G18340120R

003 Page 56 : Add a new lid sw for touchpanel using. (Panel PCB length change)

004 Page 30 : Reserved 0.1uF to light_sensor.

005 Page 31 : Change 6 pin to 8 pin for TP changing.

006 Page 21 : Change SMBus and INT for TP using.

007 Page 45 : Change Touch Panel pin define.

008 Page 56 : Change control method of charger led.

009 Page 31 : Add C3114 for RF suggestion.

010 Page 31 : Add and reserve the old 6 pins con and delete +5VS_TP.

011 Page 63 : Add 8PF cap. to +5VS for RF suggestion.

012 Page 53 : Add R5306 and Pull high to +3VSUS for intel smart card function using.

013 Page 44 : Change pin define for footprint vs datasheet aren't the same.

014 Page 45 : Add C4570 ~ C4501 ~ C4504 Cap. for RF suggestion.

PWR modify

Page 81 : Add PC8131, PC8132

Page 83 : Add PC8317 / P8316 / PR8305 / PC8305

Page 83 : Change PR8314=>12k

Page 88 : Update Adaptor voltage table

Page 84 : Change PL8400 BOM

Page 87 : Change PL8700 BOM

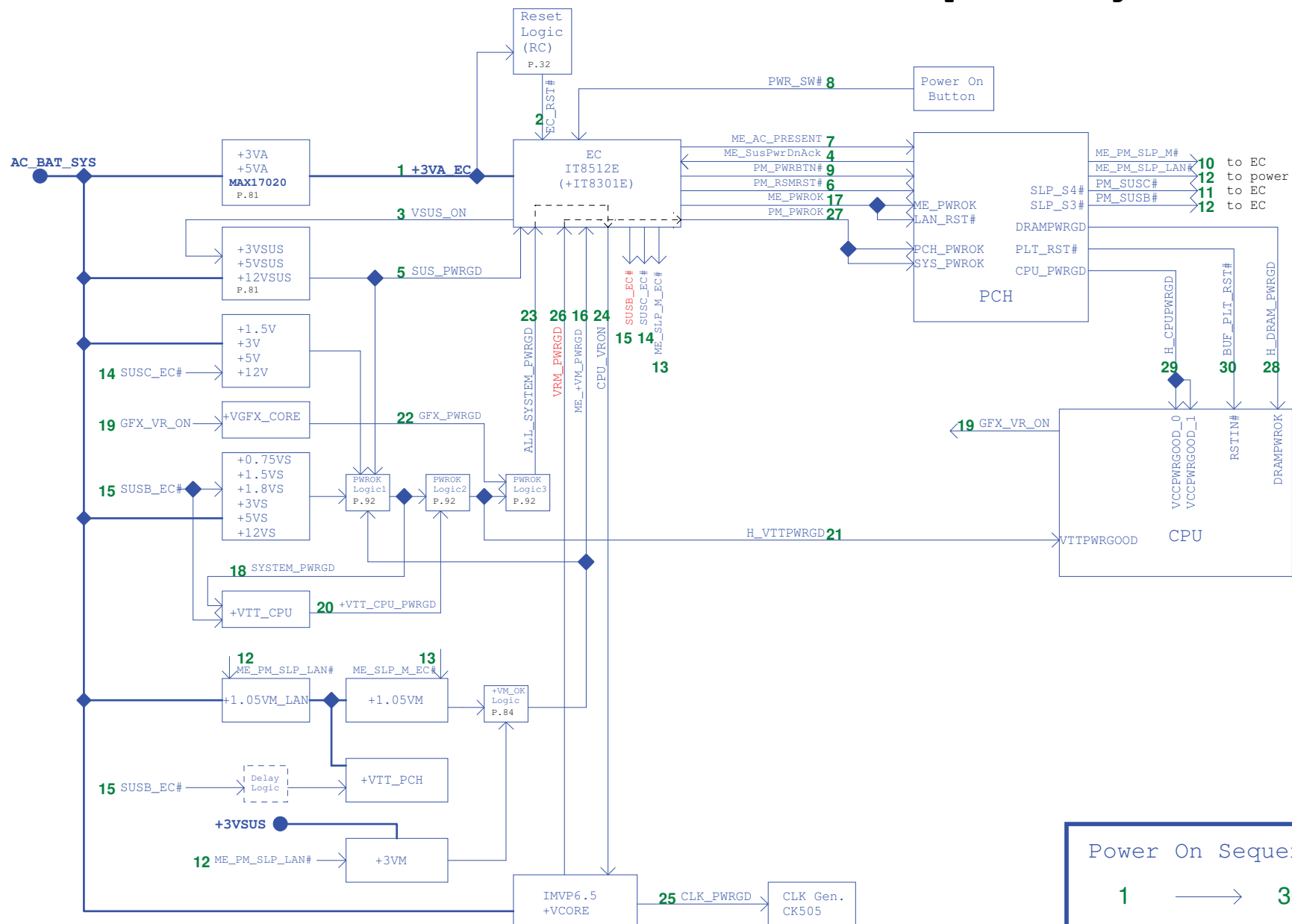
Page 83 : PR8304 & PR8305 pull high to +3VA_EC

Page 88 : PR8810 & PR8817 change 10ohm/0603 to 0ohm/0603.

Page 88 : PR8838 change 95.3kohm/0402 to 100kohm/0402.

AC-IN Mode

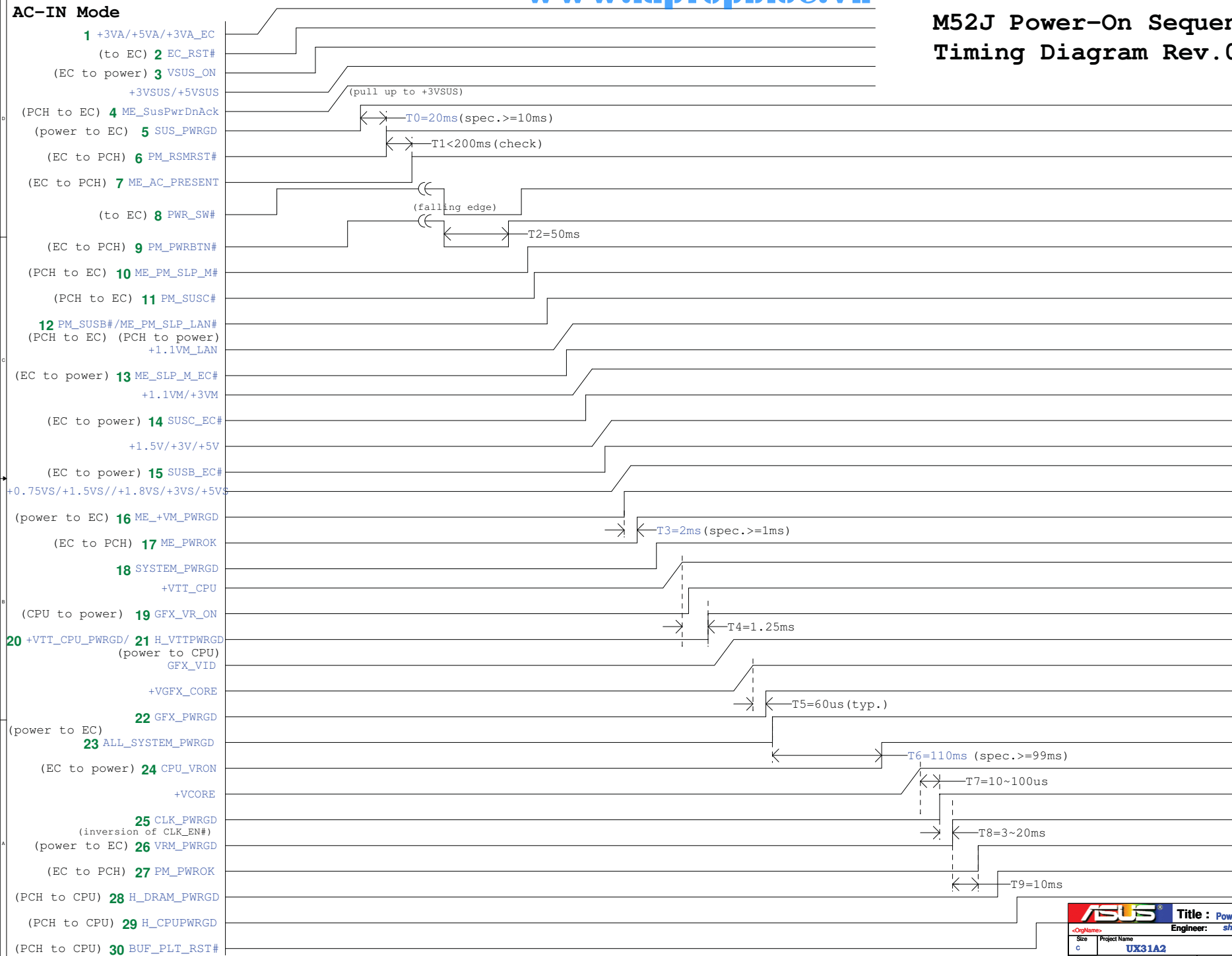
M52J Power On Sequence Diagram Rev. 0.31



Power On Sequence

1 → 30

M52J Power-On Sequence Timing Diagram Rev.0.31



UX31A R2.0 SKU table

BCM	CPU	Memory	TPM	SSD	PANEL
Option	/CPU	/MEM	/TPM		
60-NIOMBI60*-B0*	I7-3517U	Elpida 4G DDR3LRS-1600	/TPM	A-DATA/XM11-256GB-V2	CMD/N133HSE-EA1
60-NIOMBI60*-A0*	I7-3517U	Elpida 4G DDR3LRS-1600	N/A		
60-NIOMBI60*-B0*	I5-3317U	Elpida 4G DDR3LRS-1600	/TPM		
60-NIOMBI60*-B0*	I5-3317U	Elpida 4G DDR3LRS-1600	N/A	A-DATA/XM11-128GB-V2	CMD/N133HSE-EA1
60-NIOMBI60*-A0*	I7-3667U	Micron 4G DDR3LRS-1600	/TPM		
60-NIOMBI60*-A0*	I7-3517U	Elpida 4G DDR3-1600	N/A	SANDISK/SDSA5JK-128G	CPT/CLAA133UA03 CW

1. CPU:
- INT I7-3667U 2G/4M : 01001-00173400 (MP)
- INT I7-3517U 1.9G/4M : 01001-00172300 (MP)
- INT I5-3317U 1.7G/3M : 01001-00172400 (MP)
2. PCH:
- INT PANTHERPOINT HM76 : 02001-00051100 (MP)
3. MEM: Differential memory DIMM & Vendor have the differential DIMM_SEL[2:0] defined on board memory.
- Elpida 4G DDR3LRS 1600 256M*16 : 03006-00051300
- Elpida 4G DDR3 1600 256M*16 : 03006-00050800
- Micron 4G DDR3LRS 1600 256M*16 : 03006-00051100

DDR3L_1600	Micron			ELPIDA
DIMM_SEL0	L			H
DIMM_SEL1	L			H
DIMM_SEL2	H			H
DDR3_1700	Hyundai	ELPIDA		
DIMM_SEL0	H		H	
DIMM_SEL1	L		H	
DIMM_SEL2	H	H	H	