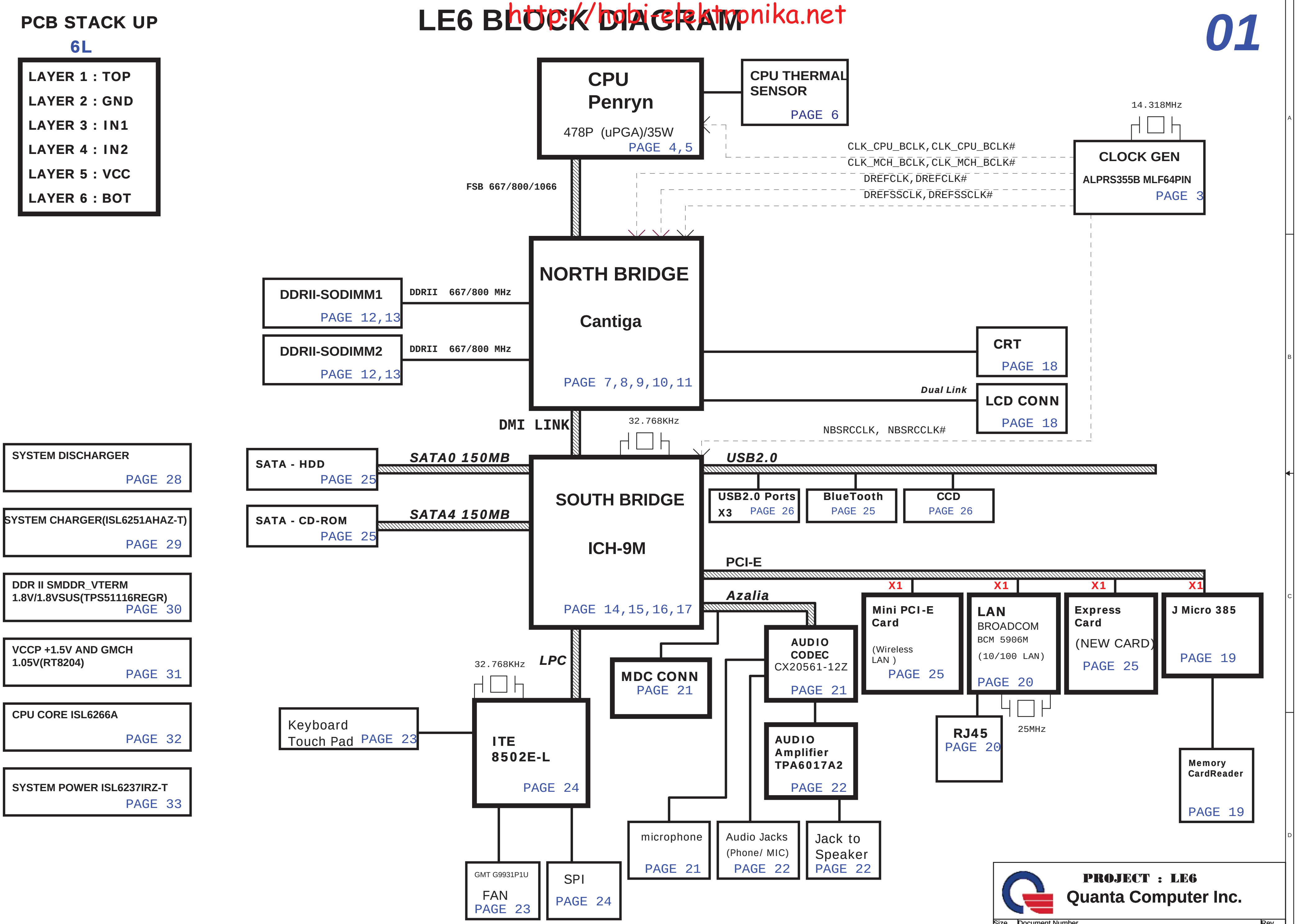
LE6 BLOCK DIAGRAM



PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGERAM	1A

Date: Wednesday, April 23, 2008 Sheet 1 of 34

Board Stack up Description

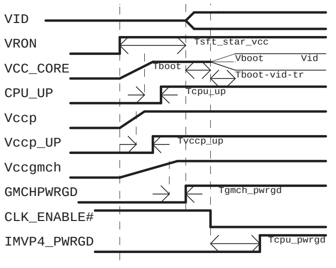
PCB Layers

Layer 1	TOP
Layer 2	GND
Layer 3	IN1
Layer 4	IN2
Layer 5	SVCC
Layer 6	BOTTOM

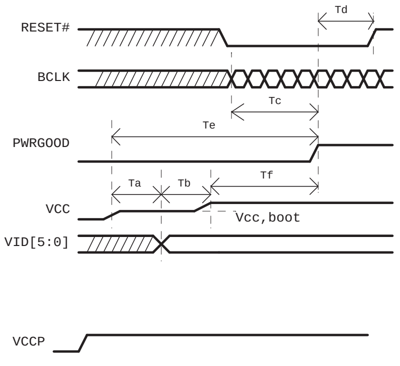
Voltage Rails

Voltage Rails	ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5/1.5V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.8VSUS	X	X			SUSON
SMDDR_VTERM/+2.5V/+3V/+5V/+12V	X				MAINON
+VCC_GFX_CORE/+1.2V_GFX_PCIE	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL

Power On Sequencing Timing Diagram

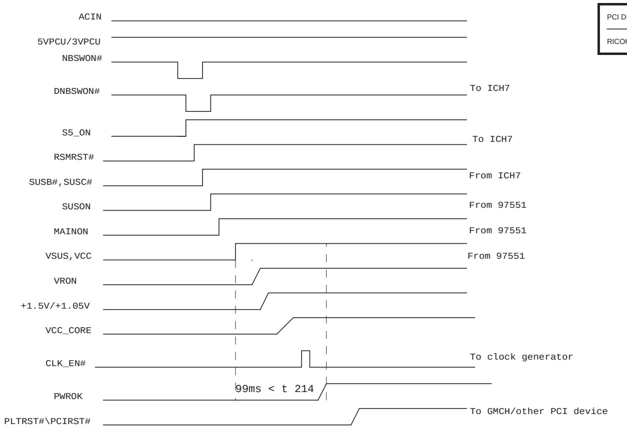


YONAH Power-up Timing Specifications



Ta=VCC and VCCP asseration to VID[5:0] vaild
Tb=VID[5:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

ACIN POWER ON TIMING



PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
RICOH832	AD25	REQ0# / GNT0#	INT E#/F#

PROJECT : LE6
Quanta Computer Inc.

Size: Custom	Document Number: SYSTEM INFORMATION	Rev: 1A
Date: Friday, May 02, 2008	Sheet 2 of 34	

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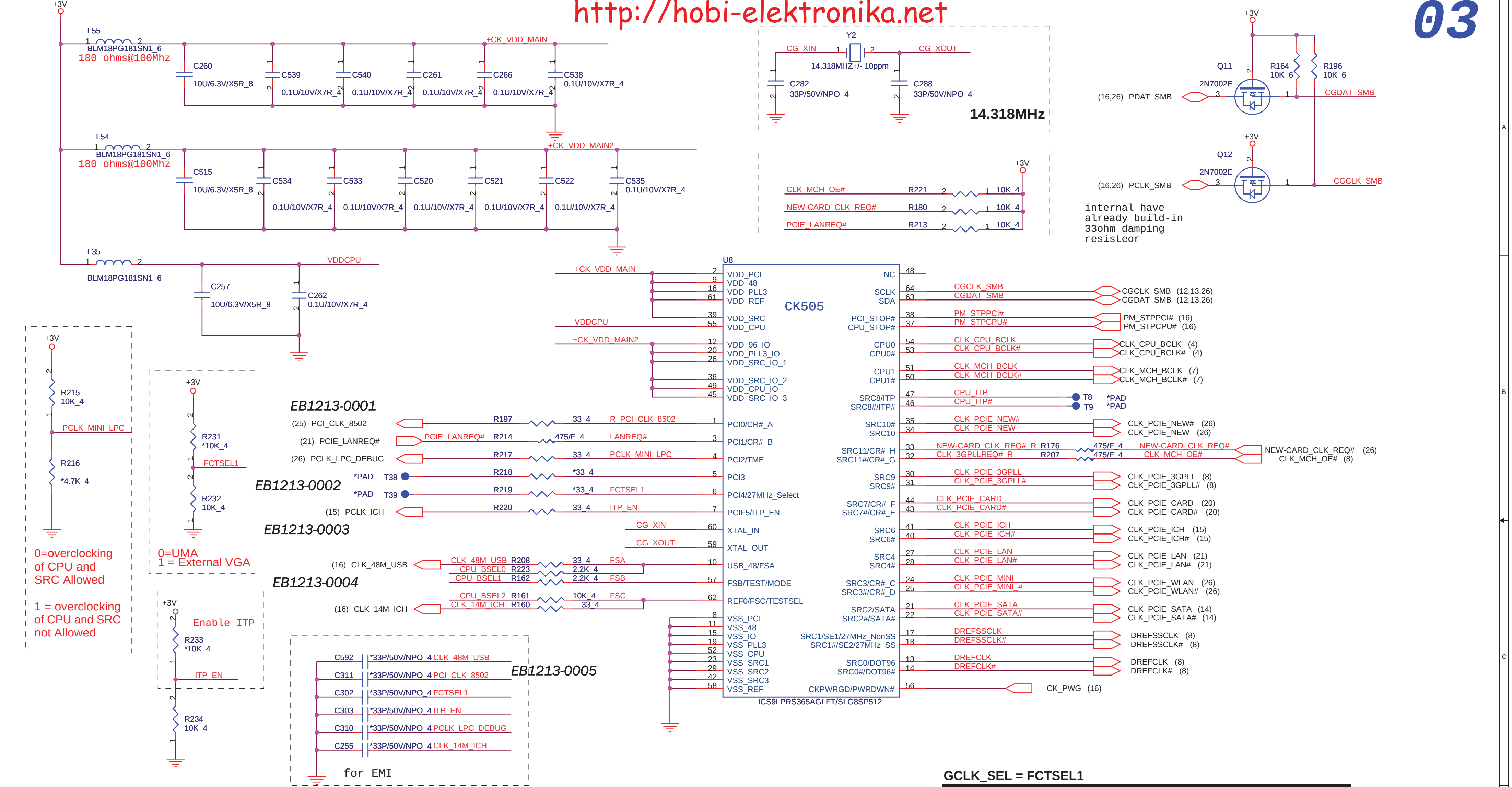
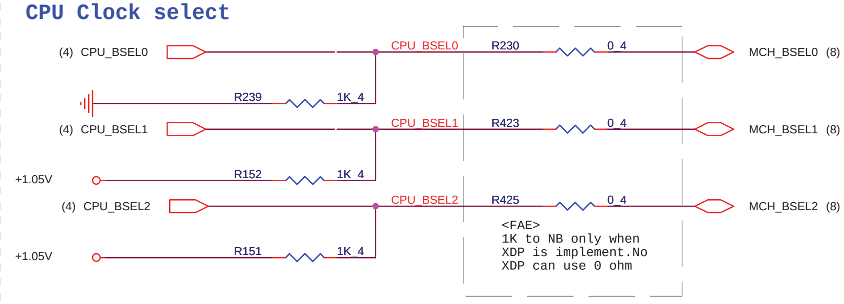
03



GCLK_SEL = FCTSEL1

FCTSEL1 (PIN6)	PIN13	PIN14	PIN24	PIN25
0=UMA	DREFCLK	DREFCLK#	SRCT1/LCDT_100	SRCT1/LCDT_100

CPU Clock select



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PROJECT : LE6

Quanta Computer Inc.

Size: Custom | Document Number: CLOCK GENERATOR | Rev: 1A

Date: Friday, May 02, 2008 | Sheet 3 of 34

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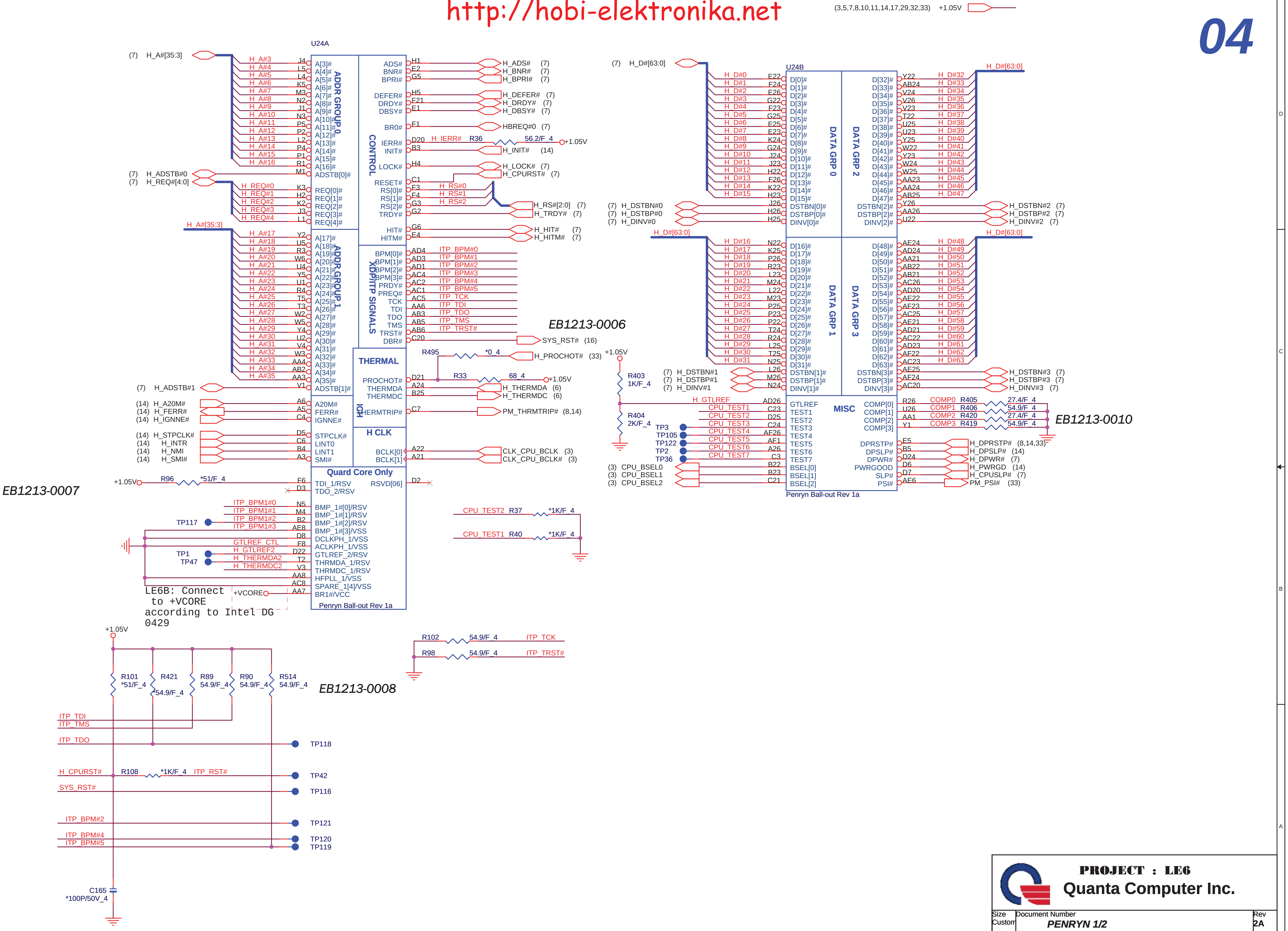
04

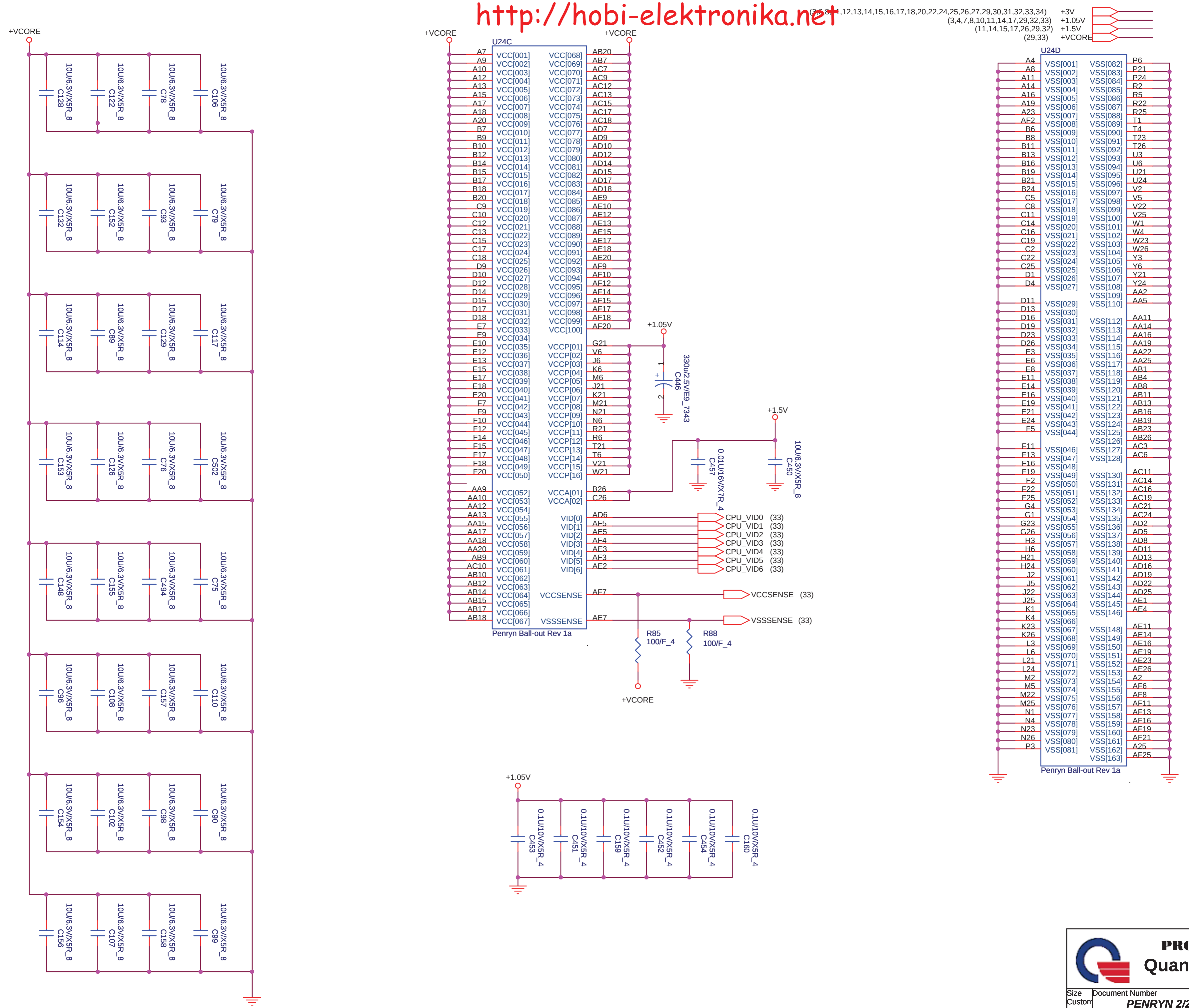


PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PENRYN 1/2	2A

Date: Friday, May 02, 2008 Sheet 4 of 34

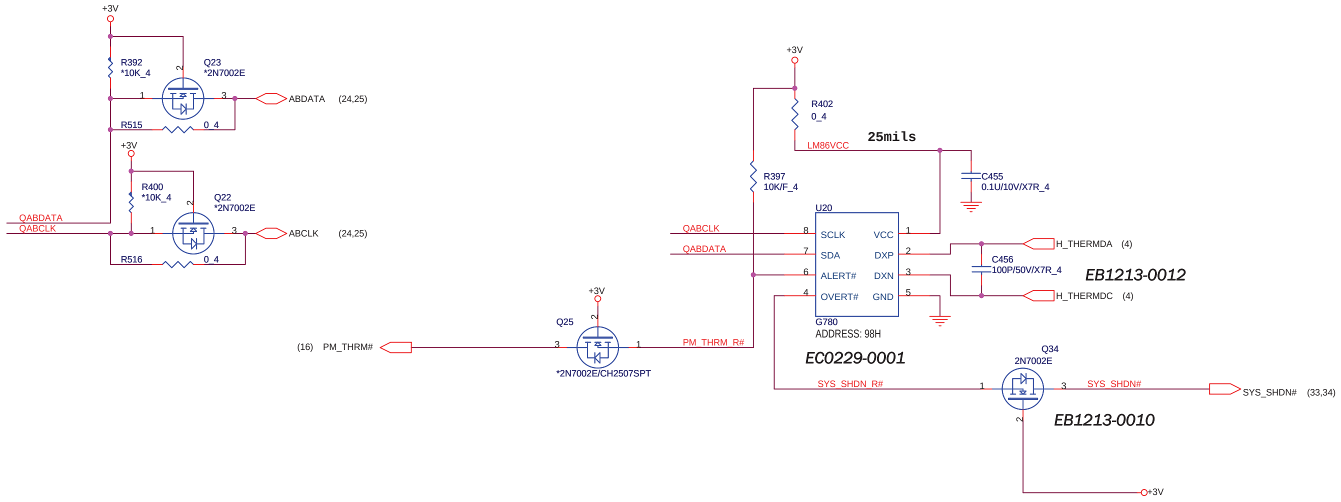


PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PENRYN 2/2	1A
Date: Tuesday, April 29, 2008	Sheet 5 of 34	

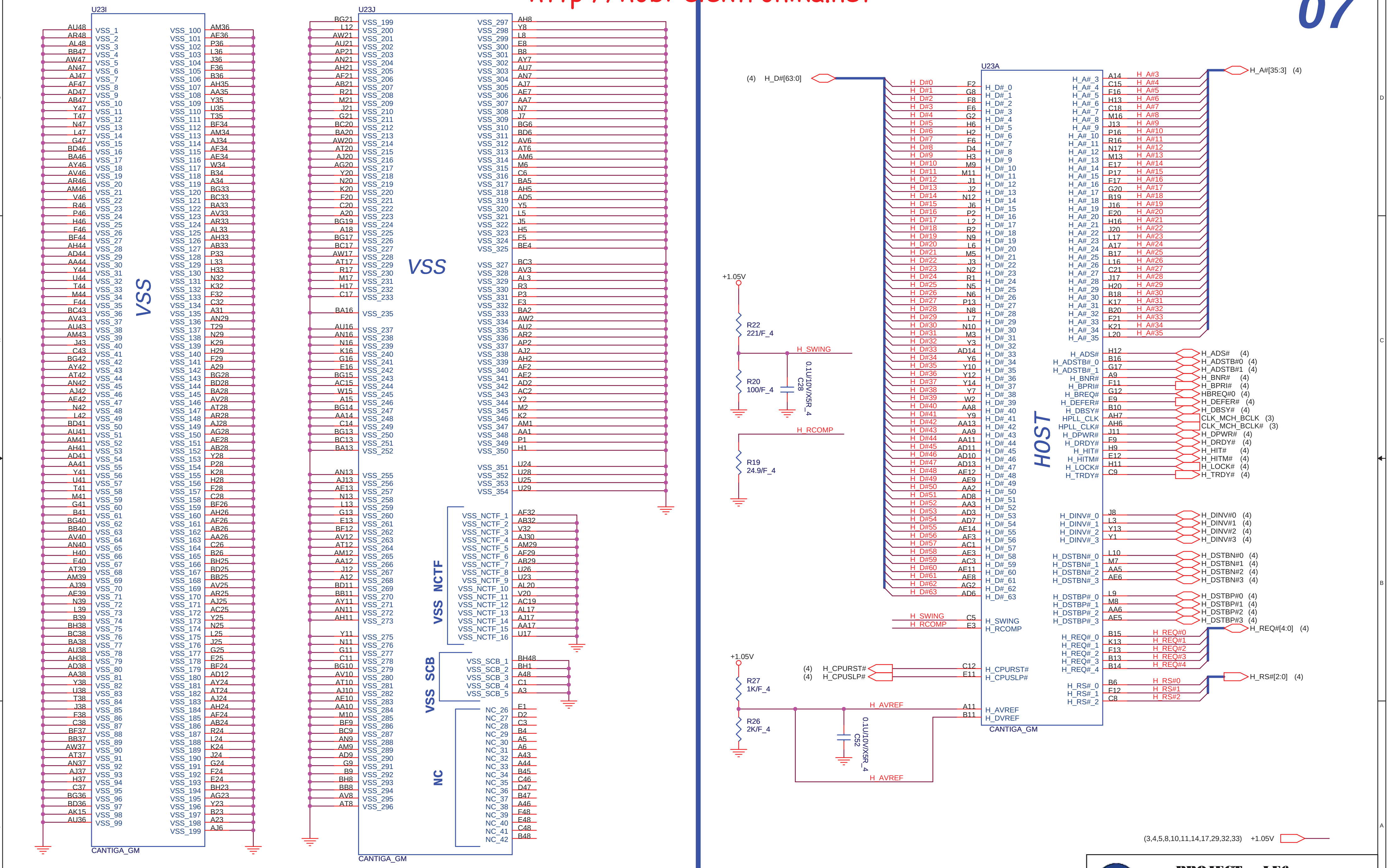
CPU H/W MONITOR



EB1213-0011

http://hobi-elektronika.net

07



(3,4,5,8,10,11,14,17,29,32,33) +1.05V

PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga Host & VSS 1/5	1A

Date: Tuesday, April 29, 2008 Sheet 7 of 34

MCH_CFG_5 DMIx2 selection

Low: DMIx2
High: DMIx4 (Default)

MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)

MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reserved

MCH_CFG_6 iTPM Host Interface

Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)

MCH_CFG_7 Intel (R) Management Engine Crypto

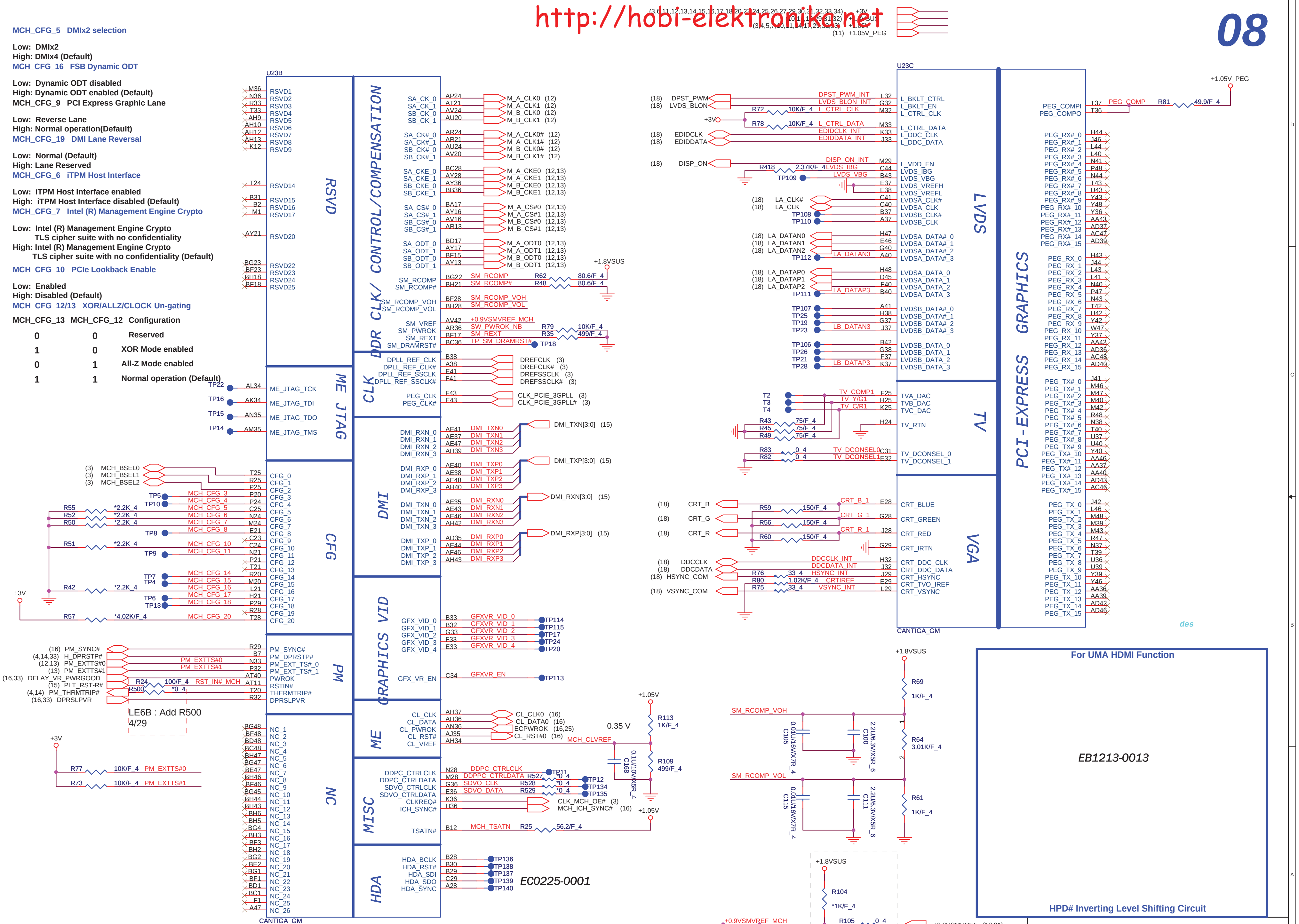
Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

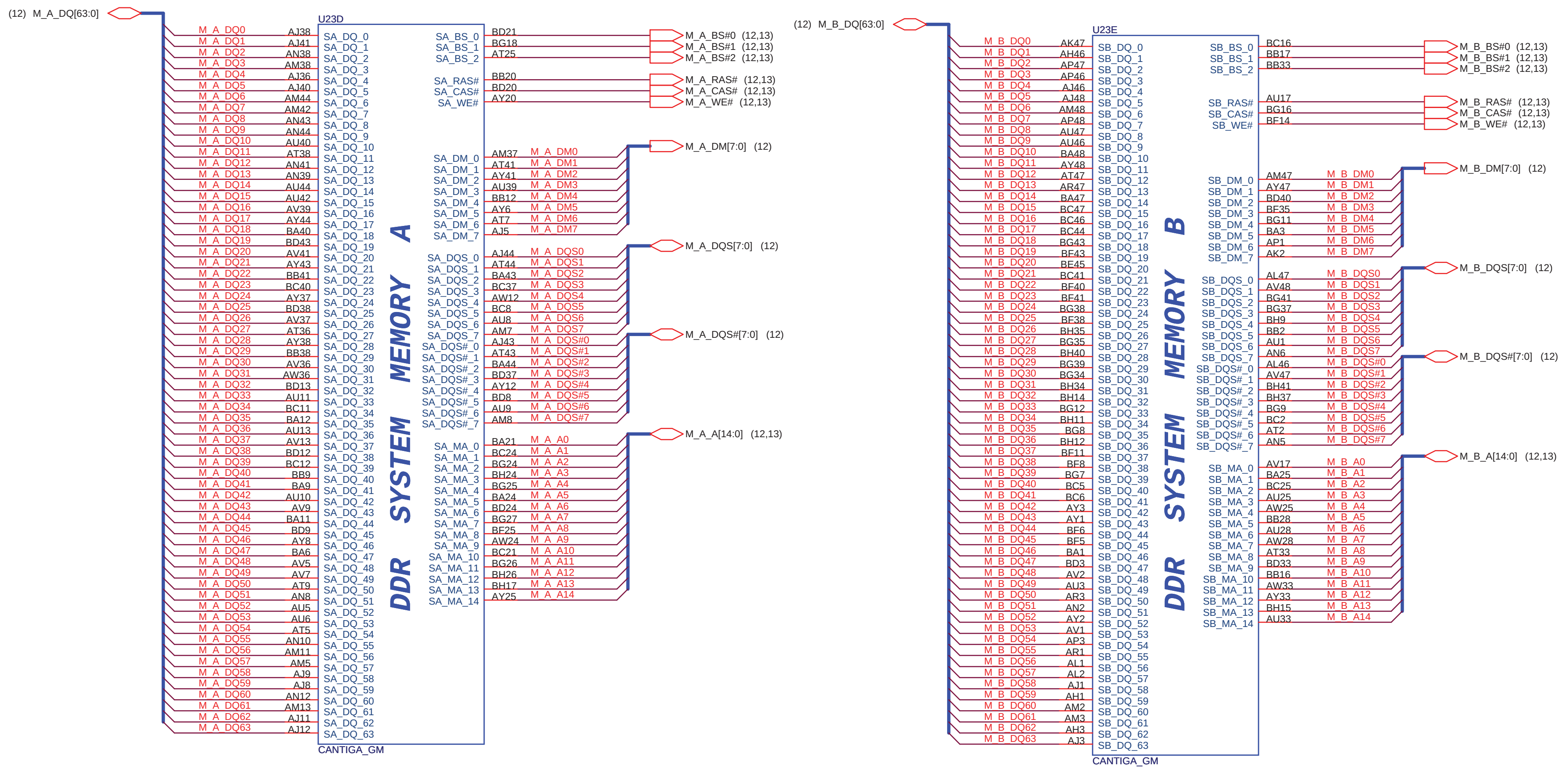
MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)



PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Canting DMIDISP 2/5	1A

Date: Friday, May 02, 2008 Sheet 8 of 34

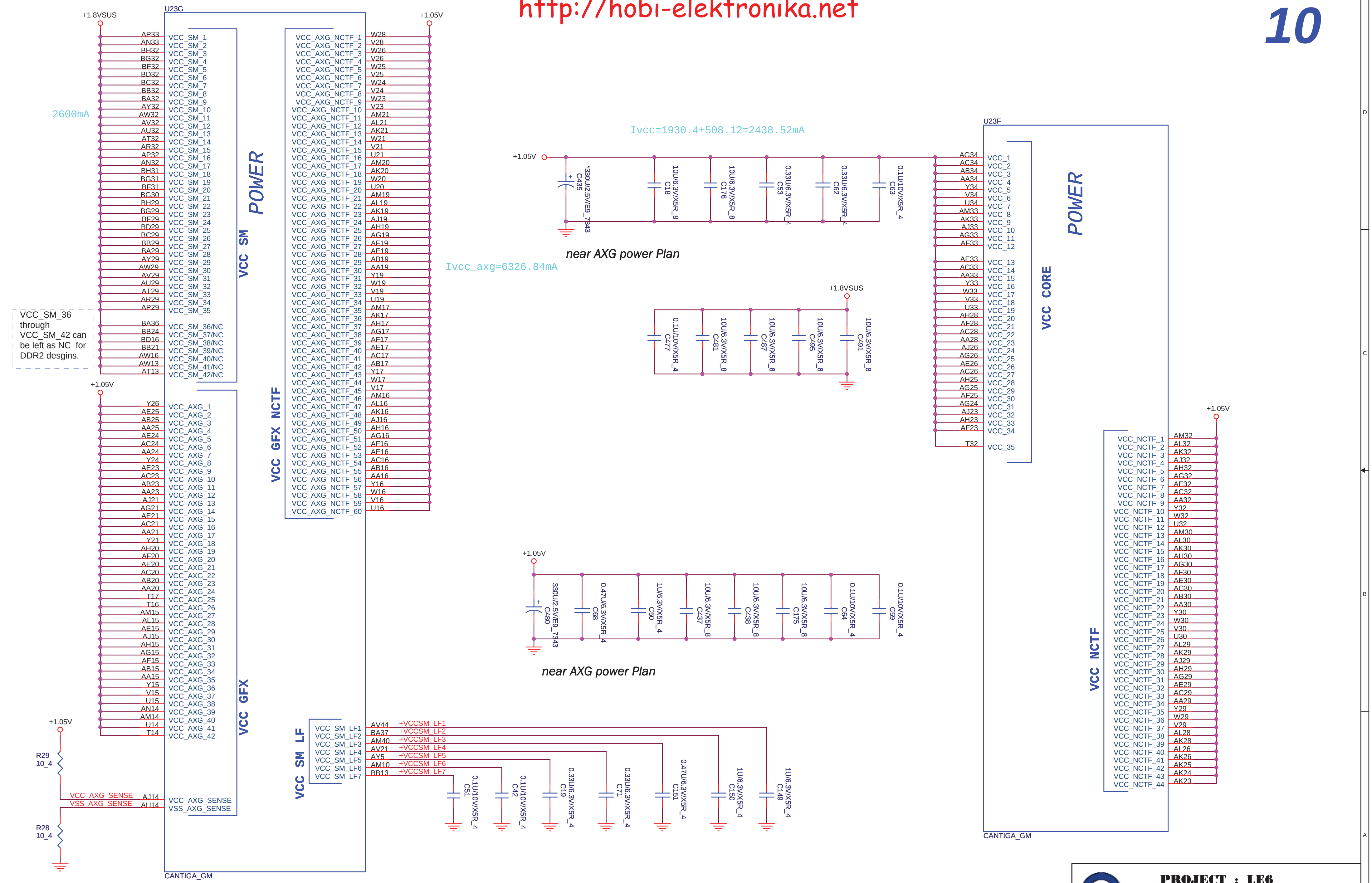


PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Canting DDR2 3/5	1A

Date: Tuesday, April 29, 2008 Sheet 9 of 34

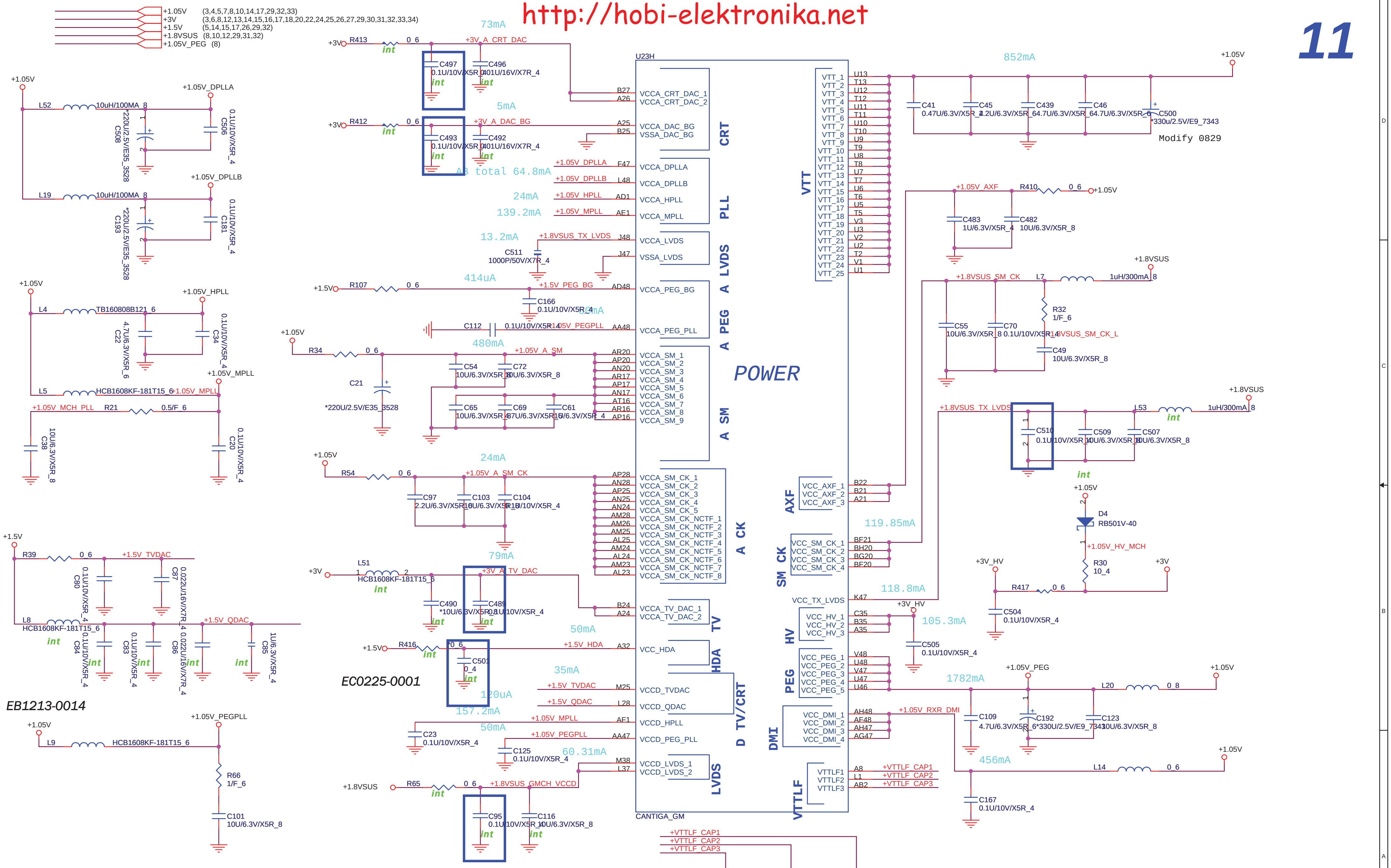


(8,11,12,29,31,32) +1.8VSUS
(3,4,5,7,8,11,14,17,29,32,33) +1.05V

PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Canting Vcc 4/5	1A

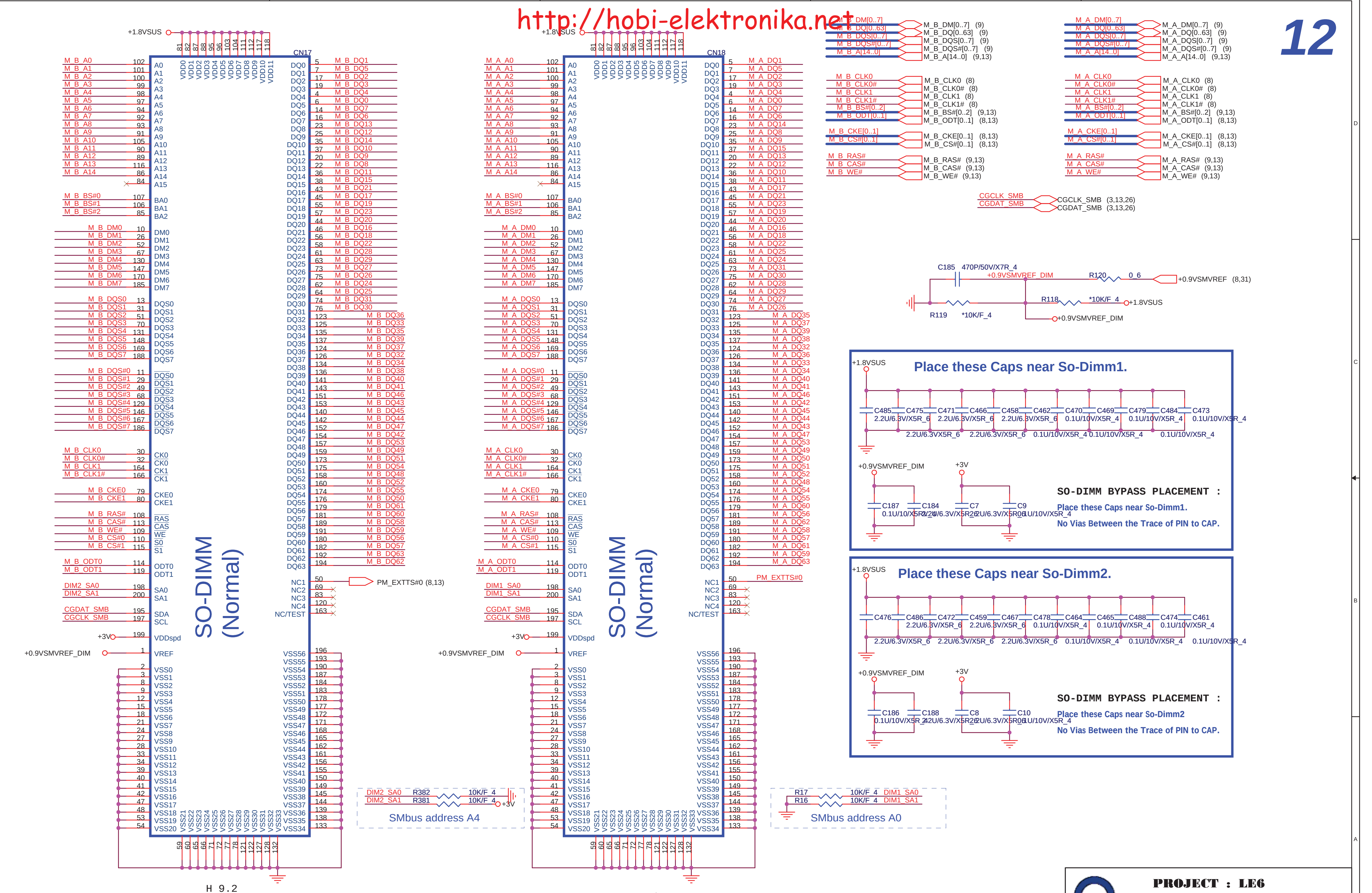


PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Canting Power 5/5	1A

Date: Tuesday, April 29, 2008 Sheet 11 of 34



PROJECT : LE6

Quanta Computer Inc.

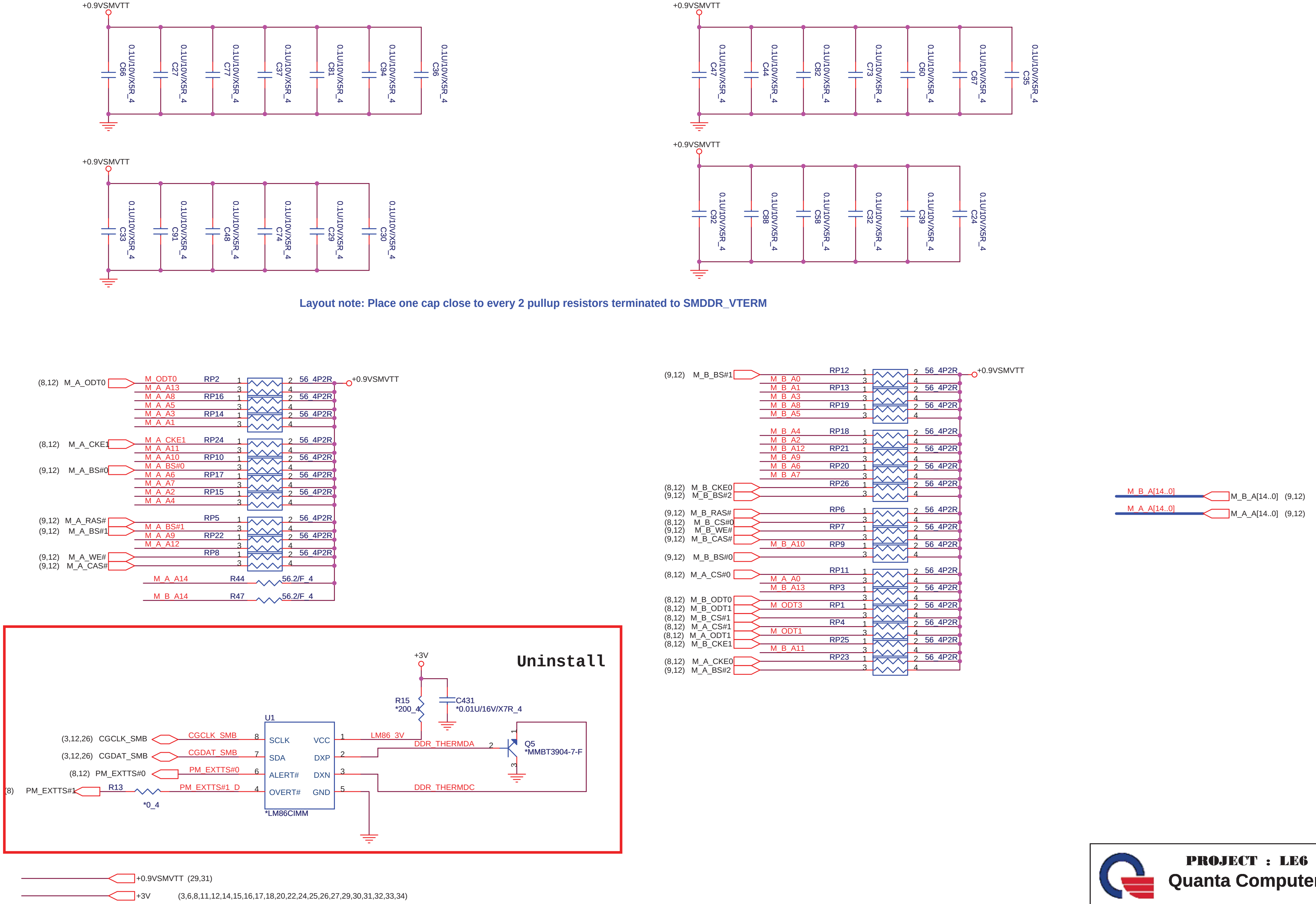
Size	Document Number	Rev
Custom	DDR2 DIMM	1A

Date: Tuesday, April 29, 2008 Sheet 12 of 34

DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

DDRII B CHANNEL

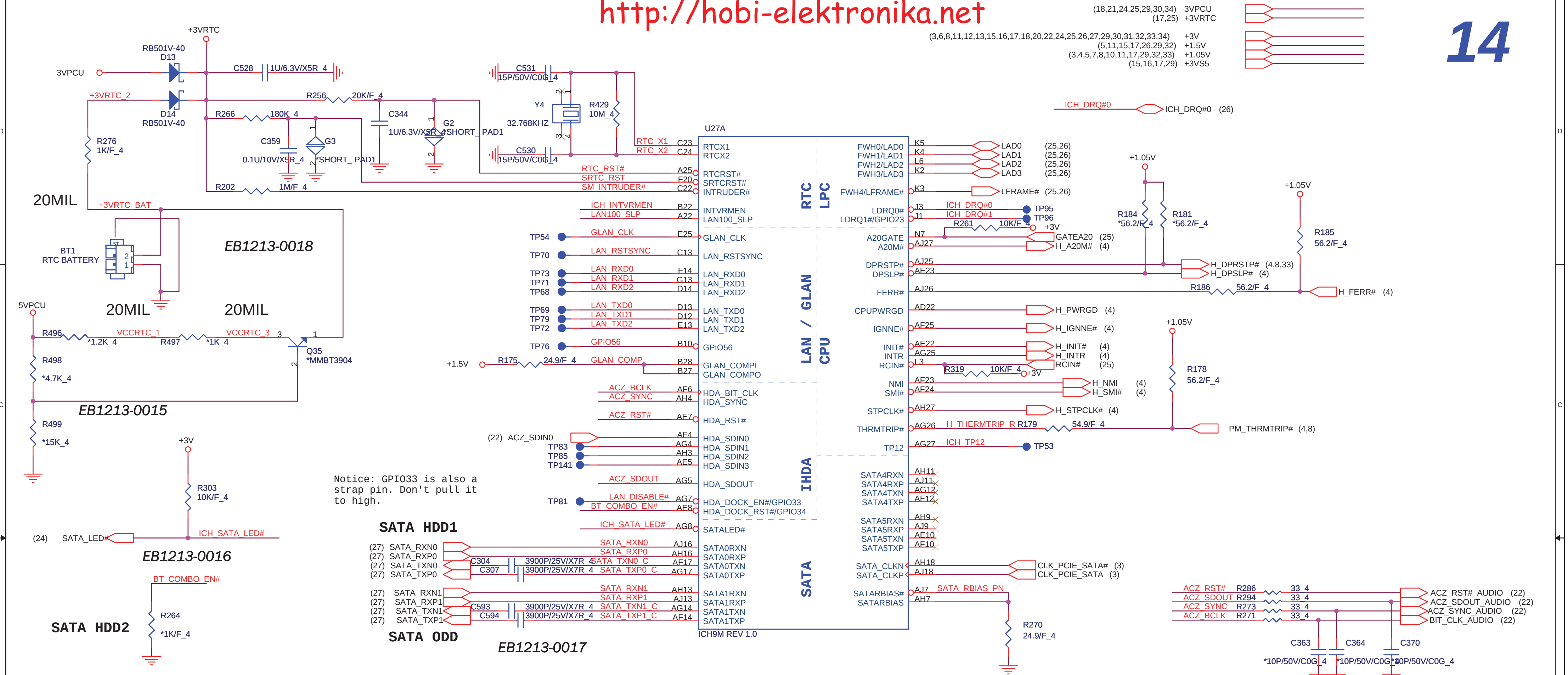


PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 termination	1A

Date: Tuesday, April 29, 2008 Sheet 13 of 34



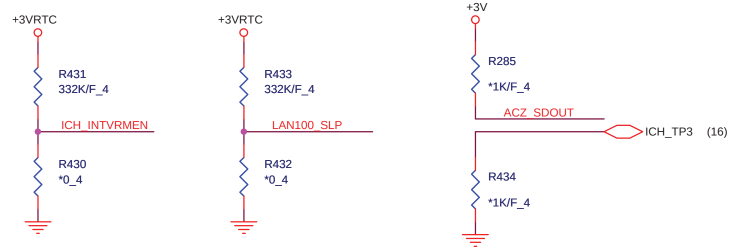
SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



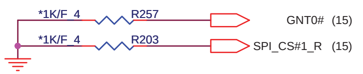
XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

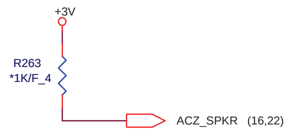
STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

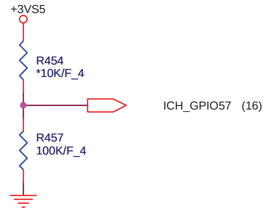


A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot



TPM physical presence	
ICH_GPIO57	Low: Default



EC0225-0002

PROJECT : LE6

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Size	Document Number	Rev
Custom	ICH9-M Host 1/4	1A

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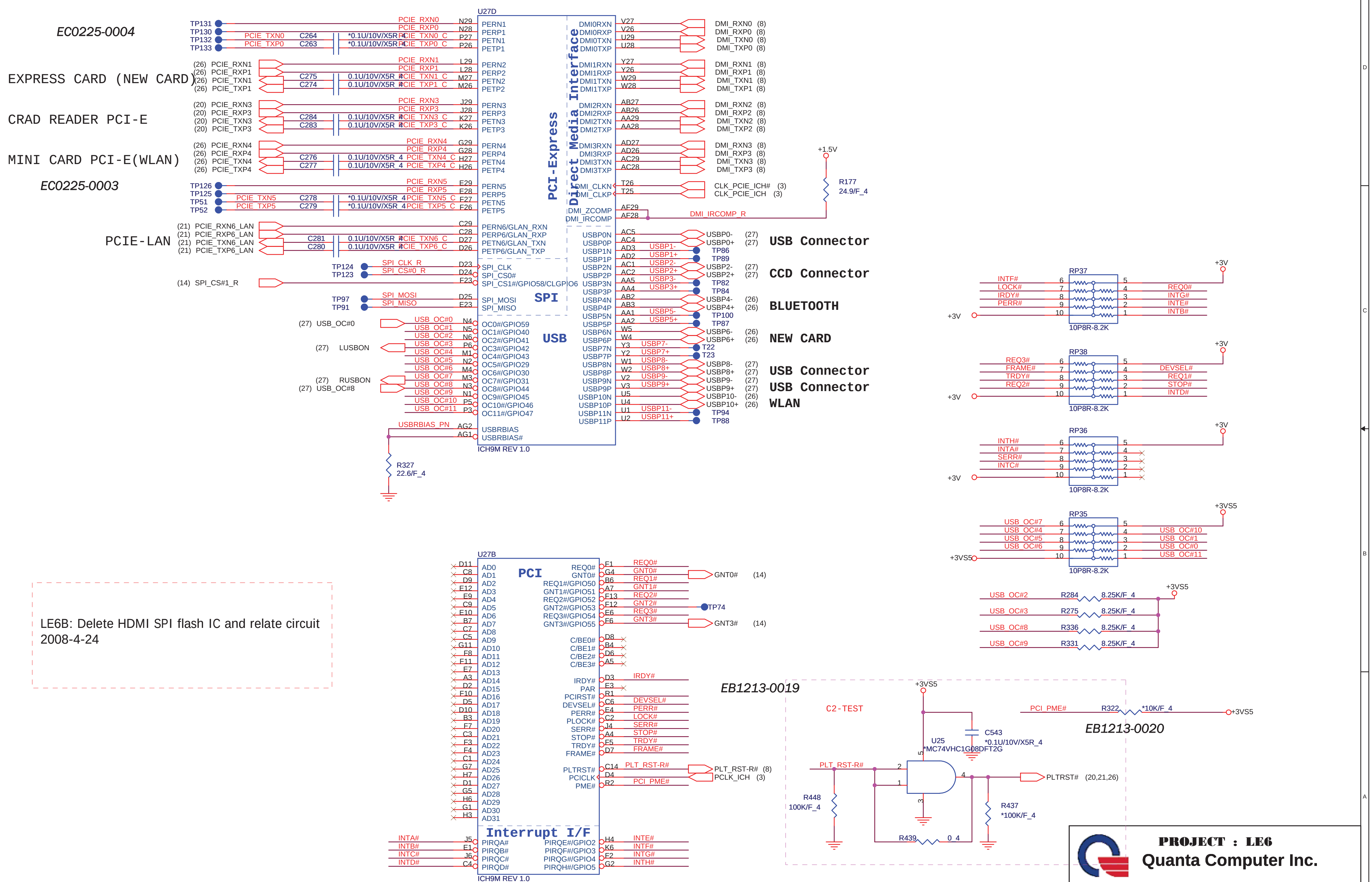


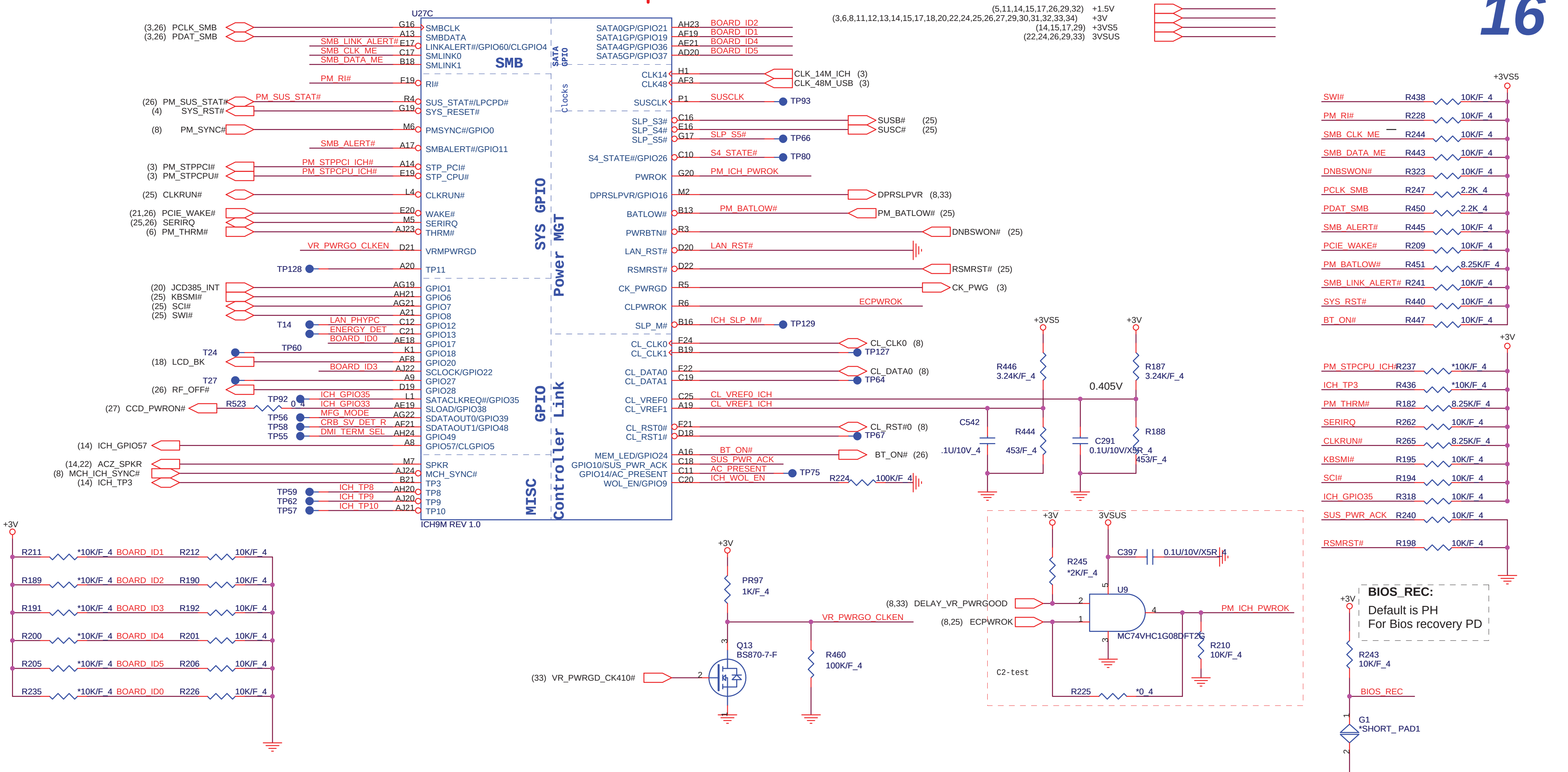
LE6B: Delete HDMI SPI flash IC and relate circuit
2008-4-24

PROJECT : LE6

Quanta Computer Inc.

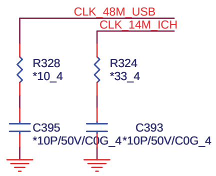
Size	Document Number	Rev
Custom	ICH9-M PCIE 2/4	1A

Date: Friday, May 02, 2008 Sheet 15 of 34



BOARD_ID0 GPIO17	BOARD_ID1 GPIO19	BOARD_ID2 GPIO21	BOARD_ID3 GPIO22	BOARD_ID4 GPIO36	BOARD_ID5 GPIO37	
L	L	L	L	L	L	LE6 (GPIO36/GPIO37)
L	L	L	L	H	L	LE7 (GPIO36/GPIO37)

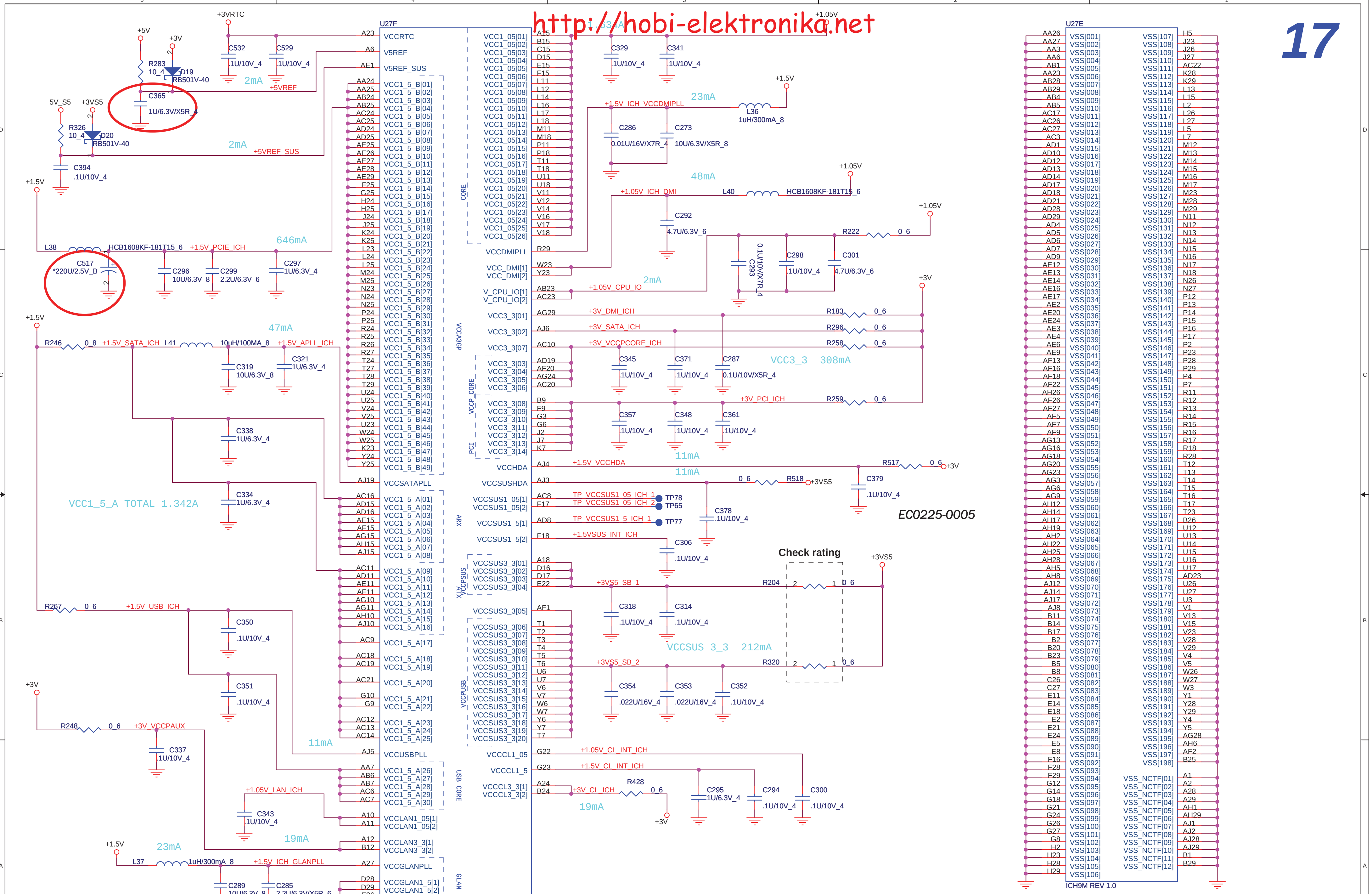
EB1213-0004



PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M GPIO 3/4	1A

Date: Friday, May 02, 2008 Sheet 16 of 34



PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M Power 4/4	1A

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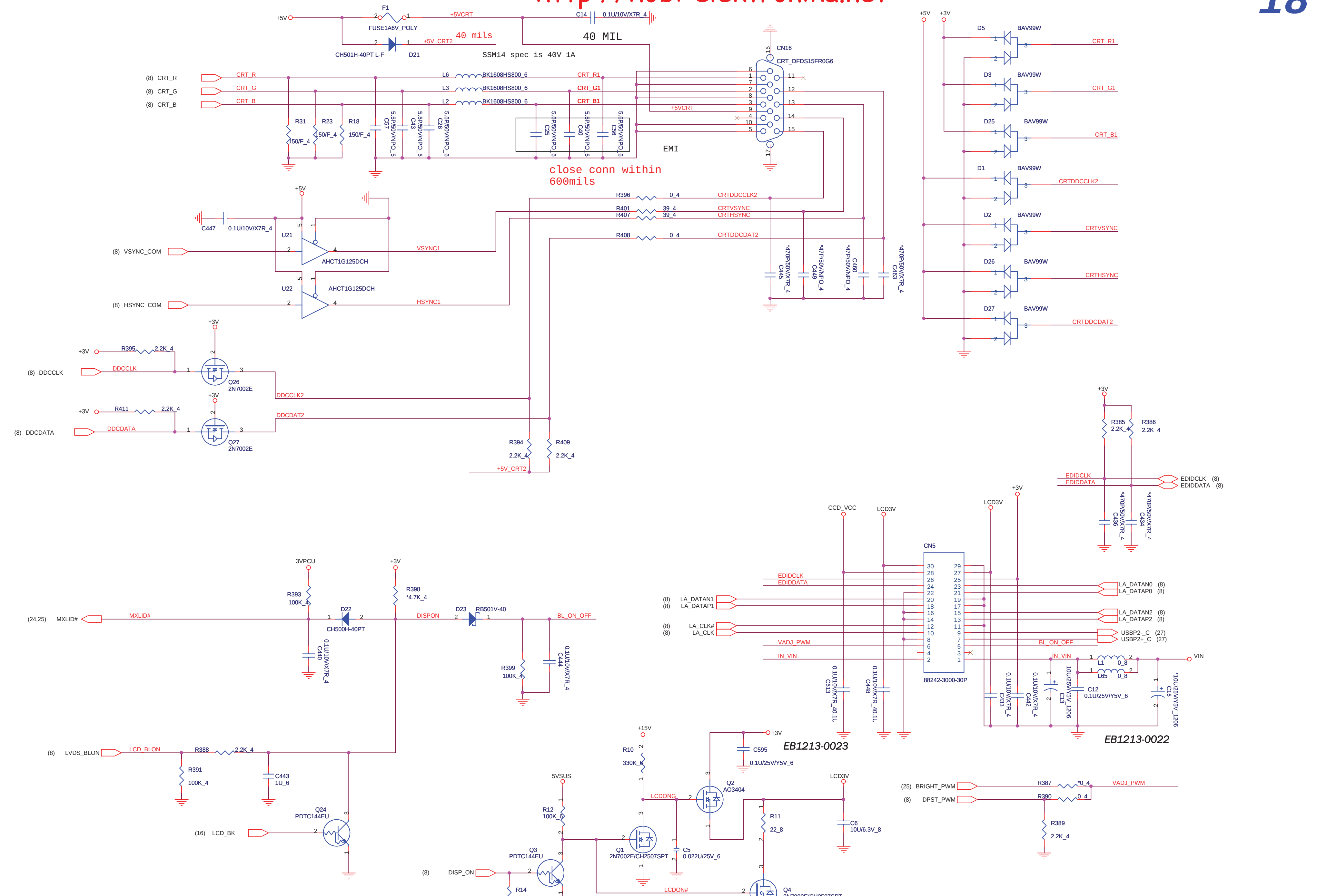
CRT PORT



PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
C	CRT/LCD/LID SWITCH	1A

Date: Friday, May 02, 2008 Sheet 18 of 34

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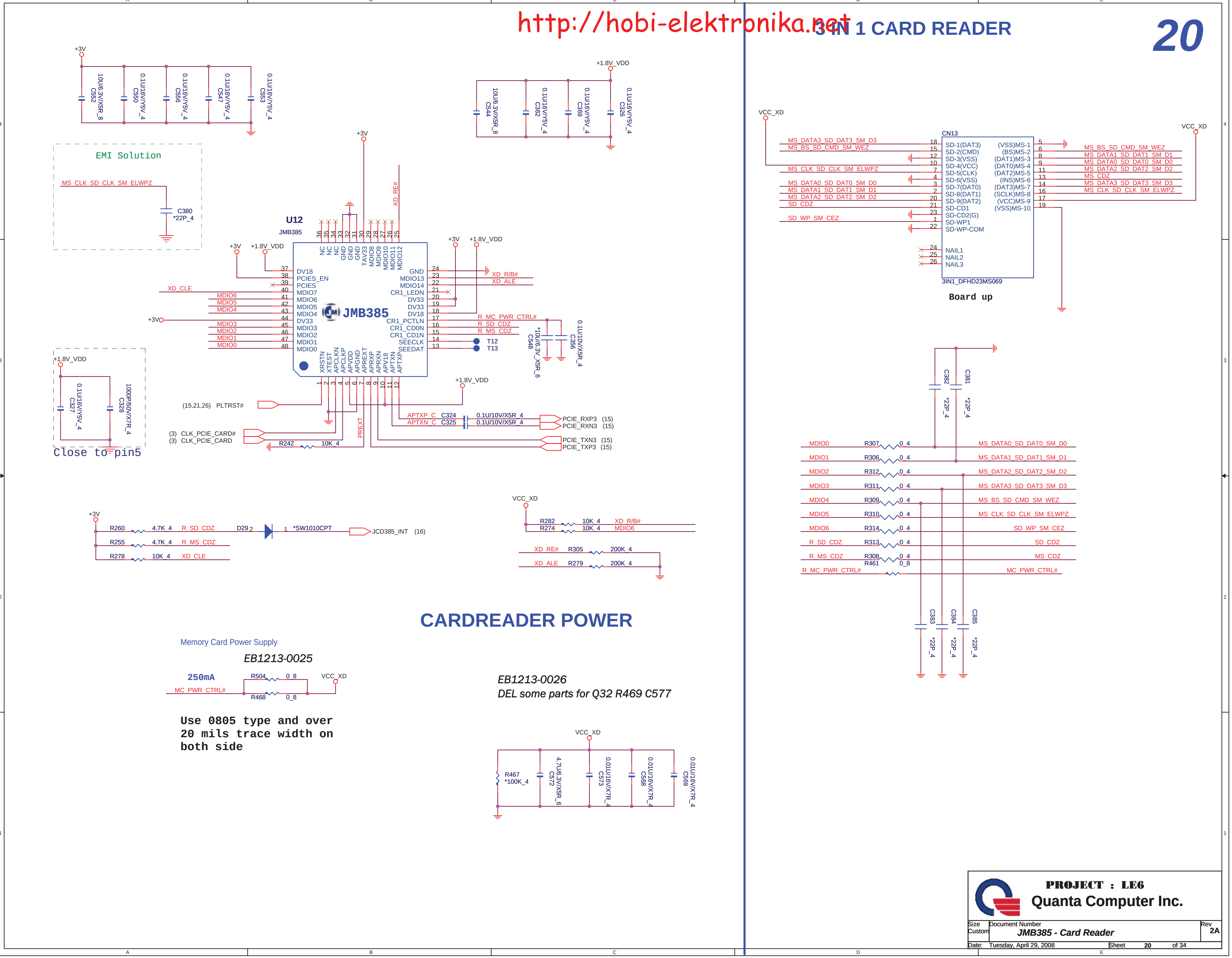
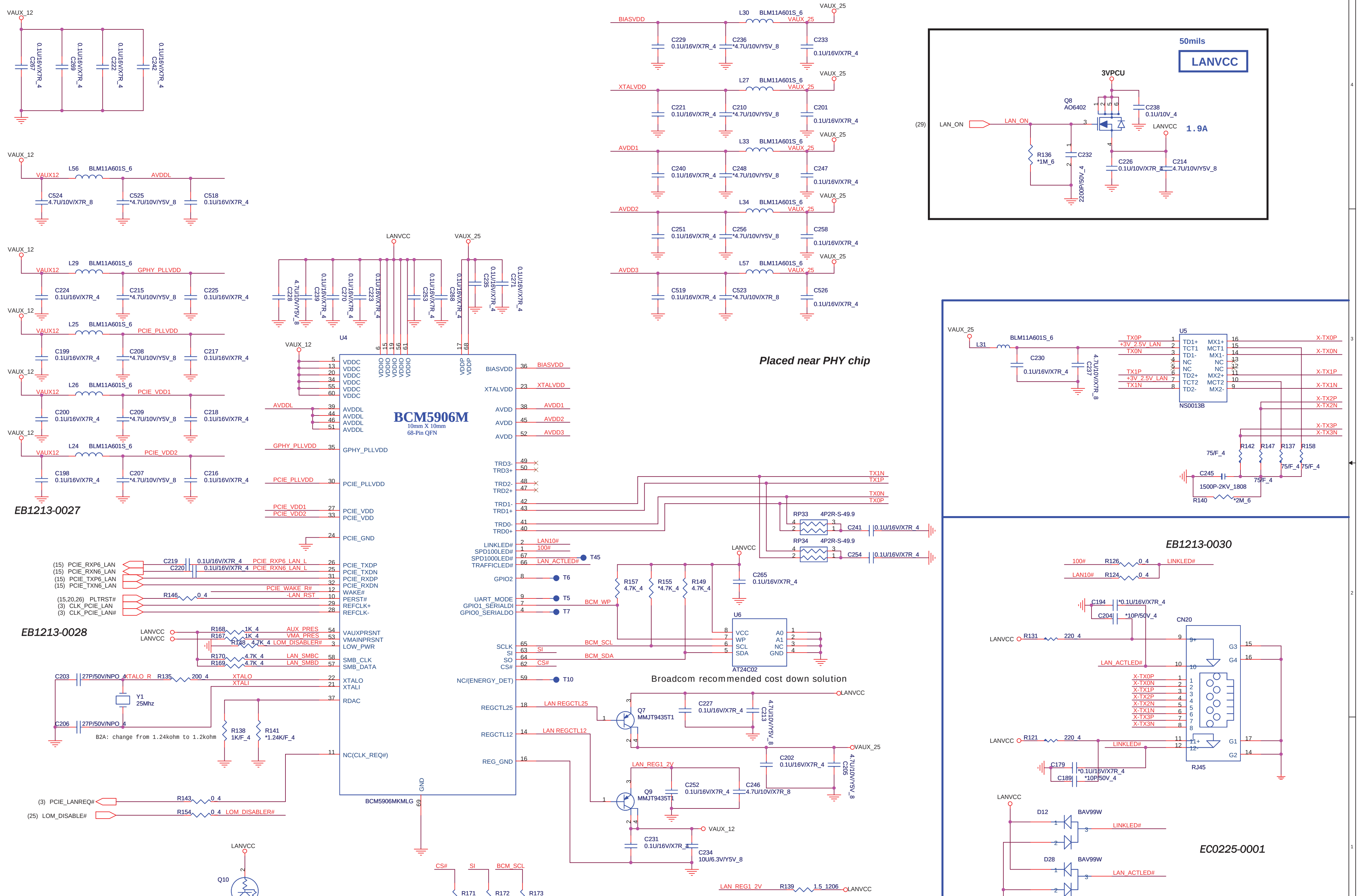


http://hobi-elektronika.net
3 IN 1 CARD READER
20
EMI Solution
Close to pin5
U12
JMB385
Board up
CN13
3IN1_DFHD23MS069
CARDREADER POWER
Memory Card Power Supply
EB1213-0025
250mA
EB1213-0026
DEL some parts for Q32 R469 C577
Use 0805 type and over
20 mils trace width on
both side
PROJECT : LE6
Quanta Computer Inc.
Size
Custom
Document Number
JMB385 - Card Reader
Rev
2A
Date: Tuesday, April 29, 2008
Sheet 20 of 34



PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
C	LAN	1A

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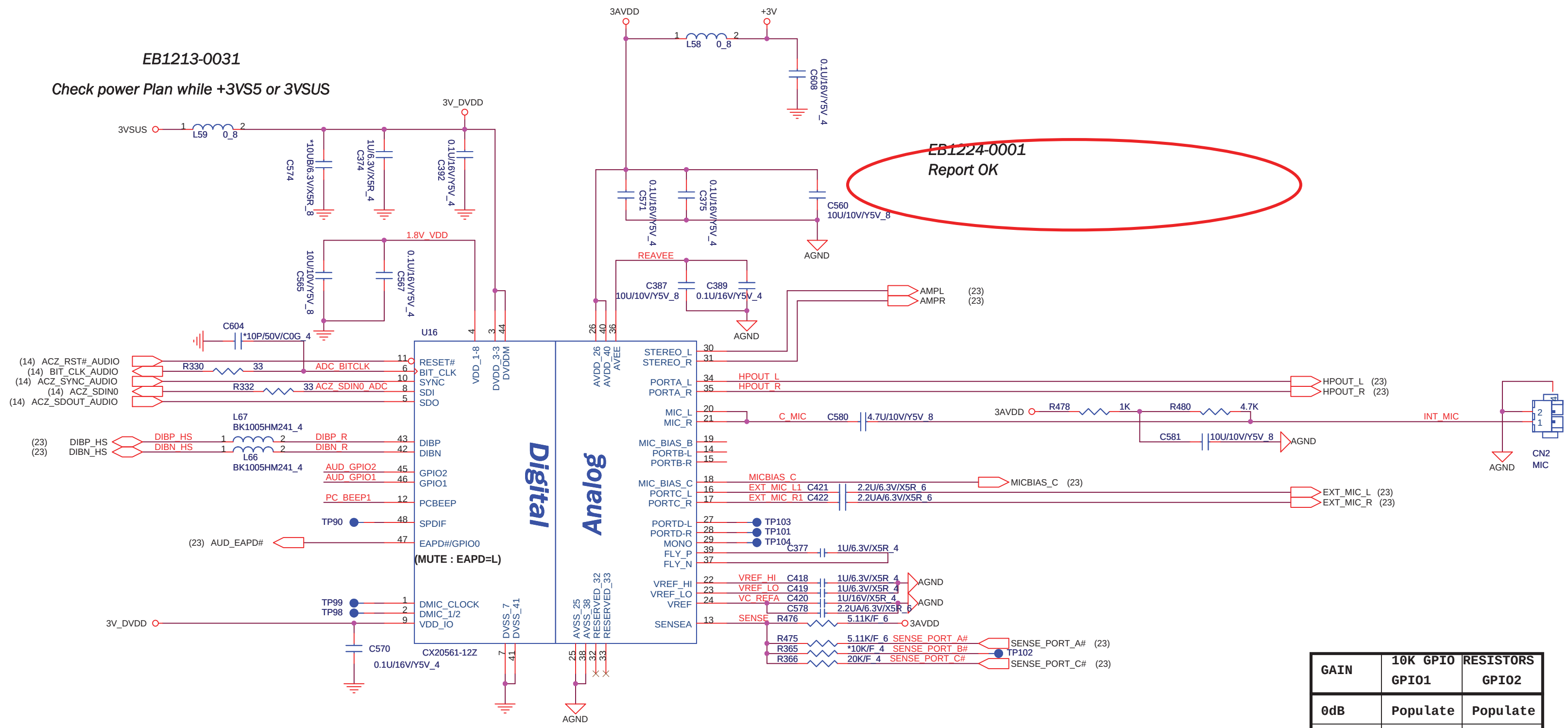
EB1213-0031

Check power Plan while +3VS5 or 3VSUS

EB1224-0001
Report OK



GAIN	10K GPIO RESISTORS	
	GPIO1	GPIO2
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-16dB	Omit	Populate

EB1213-0032

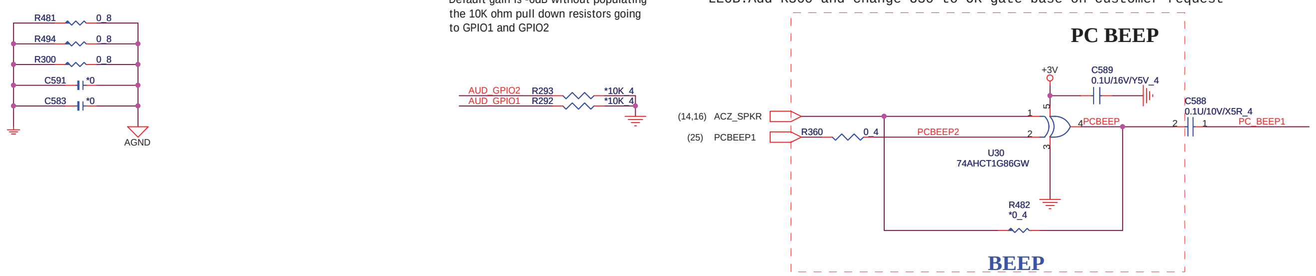
Check power Plan while +1.5VS5 or 1.5VSUS

STEREO	INTERNAL SPEAKERS
PORT-A	EXTERNAL HEAD-PHONE
MIC	INTERNAL MIC
PORT-B	EXTERNAL MIC

FOR EMI SOLUTION

Default gain is -6dB without populating the 10K ohm pull down resistors going to GPIO1 and GPIO2

LE6B:Add R360 and change U30 to OR gate base on customer request



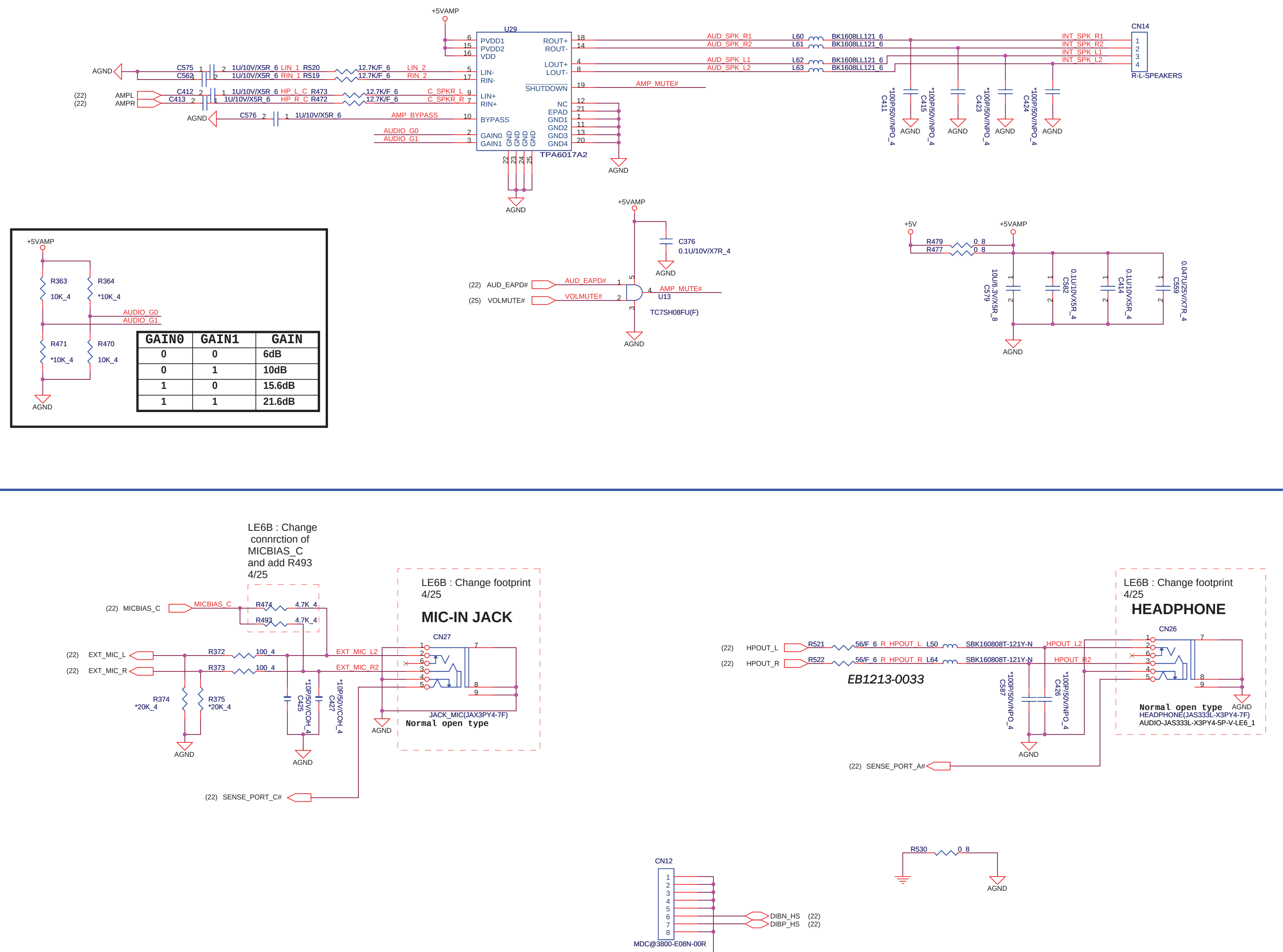
PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
C	AUDIO CODEC(CX20561-12Z)	1A

Date: Friday, May 02, 2008 Sheet 22 of 34

INTERNAL SPEAKER AMPLIFIER



GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Modem connector

PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
C	TPA6017 & JACKS & MDC	1A

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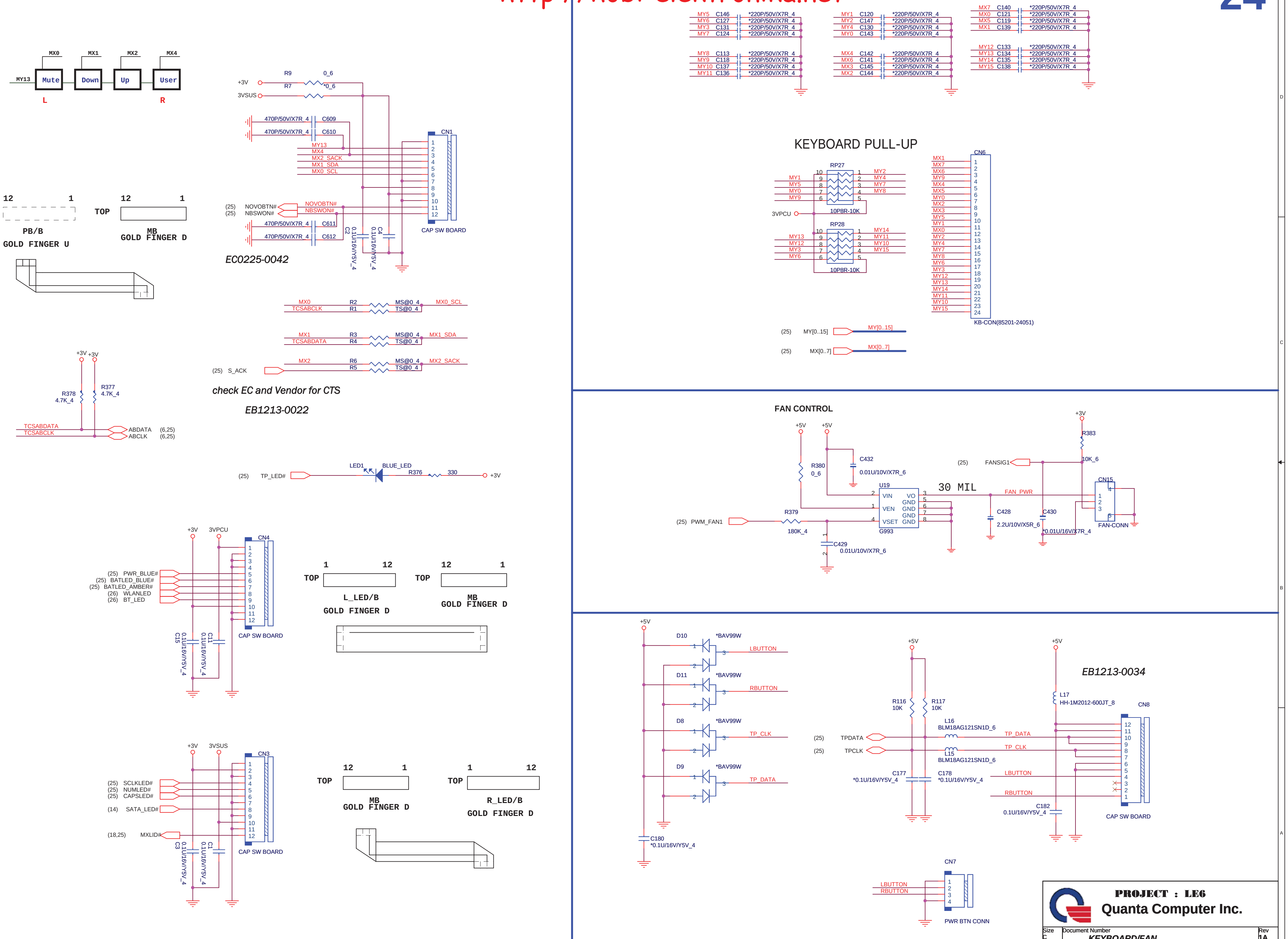
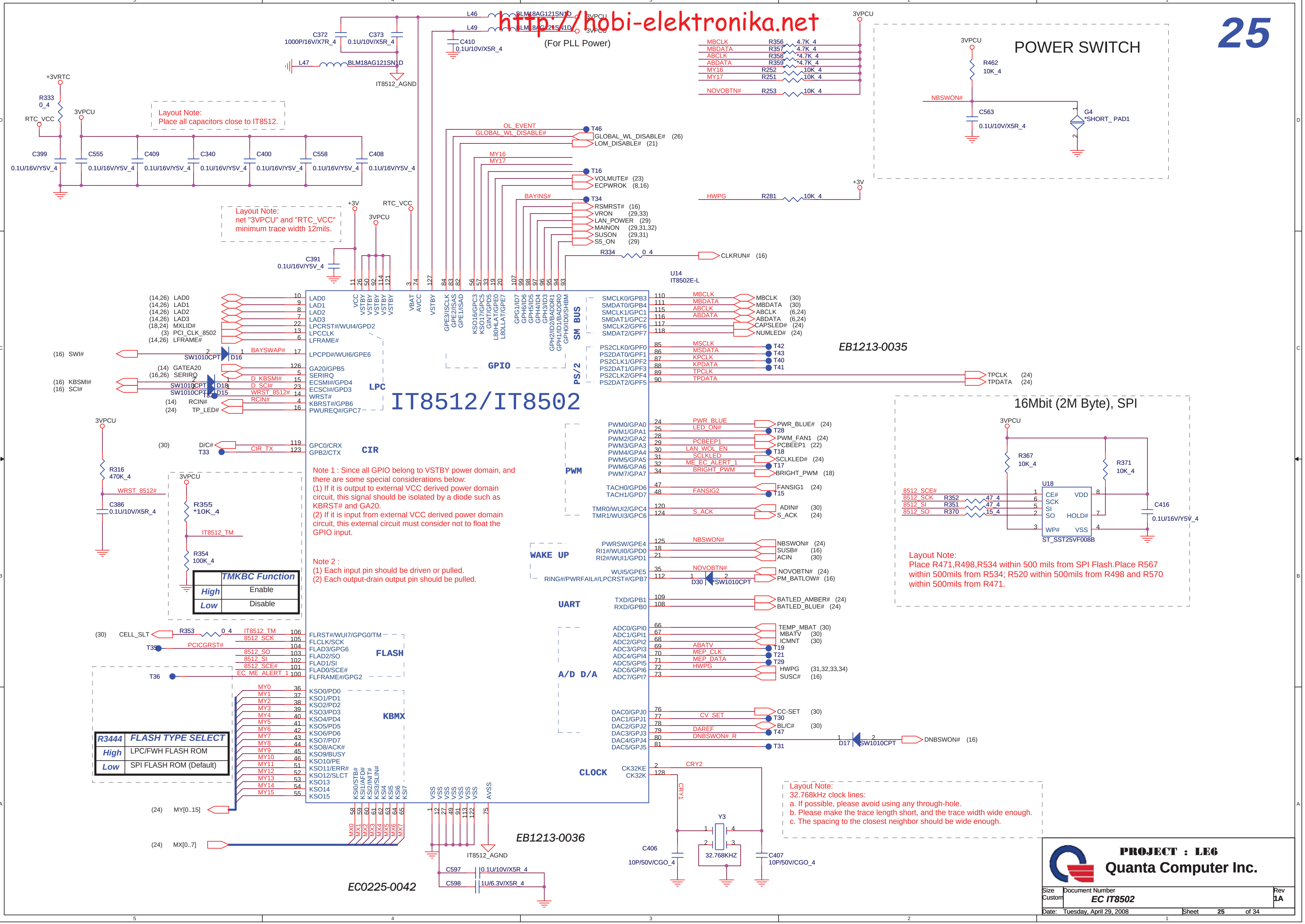


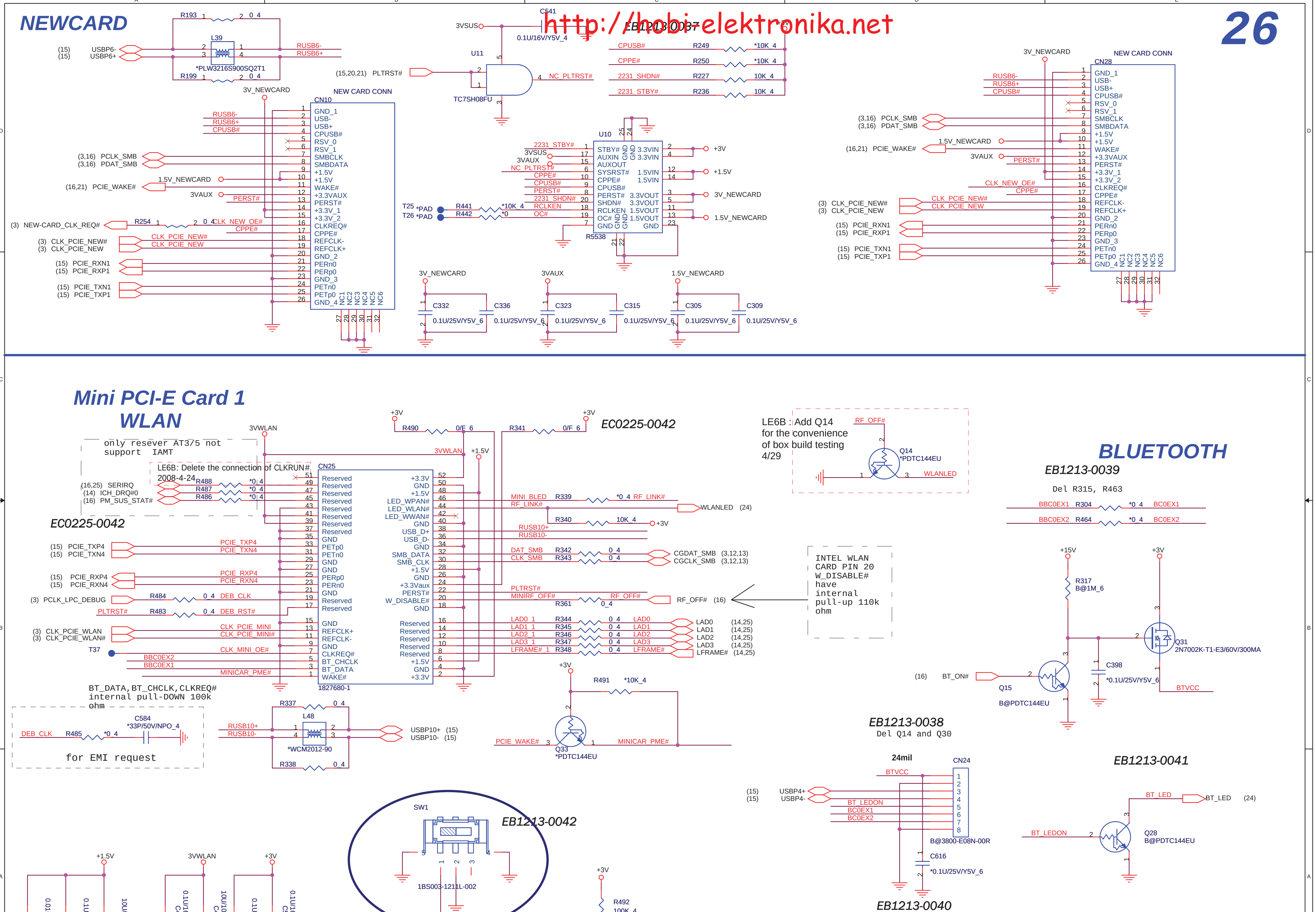
PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
C	KEYBOARD/FAN	1A

Date: Tuesday, April 29, 2008 Sheet 24 of 34


http://hobi-elektronika.net
(For PLL Power)
POWER SWITCH
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
U14
IT8502E-L
IT8512/IT8502
LPC
GPIO
SM BUS
PS/2
CIR
PWM
WAKE UP
UART
FLASH
A/D D/A
KBMX
CLOCK
EB1213-0035
EB1213-0036
EC0225-0042
16Mbit (2M Byte), SPI
U18
ST_SST25VF008B
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.
TMKBC Function
High Enable
Low Disable
R3444 FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
Layout Note:
32.768KHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.
Y3
32.768KHZ
PROJECT : LE6
Quanta Computer Inc.
Size Custom
Document Number EC IT8502
Rev 1A
Date: Tuesday, April 29, 2008
Sheet 25 of 34

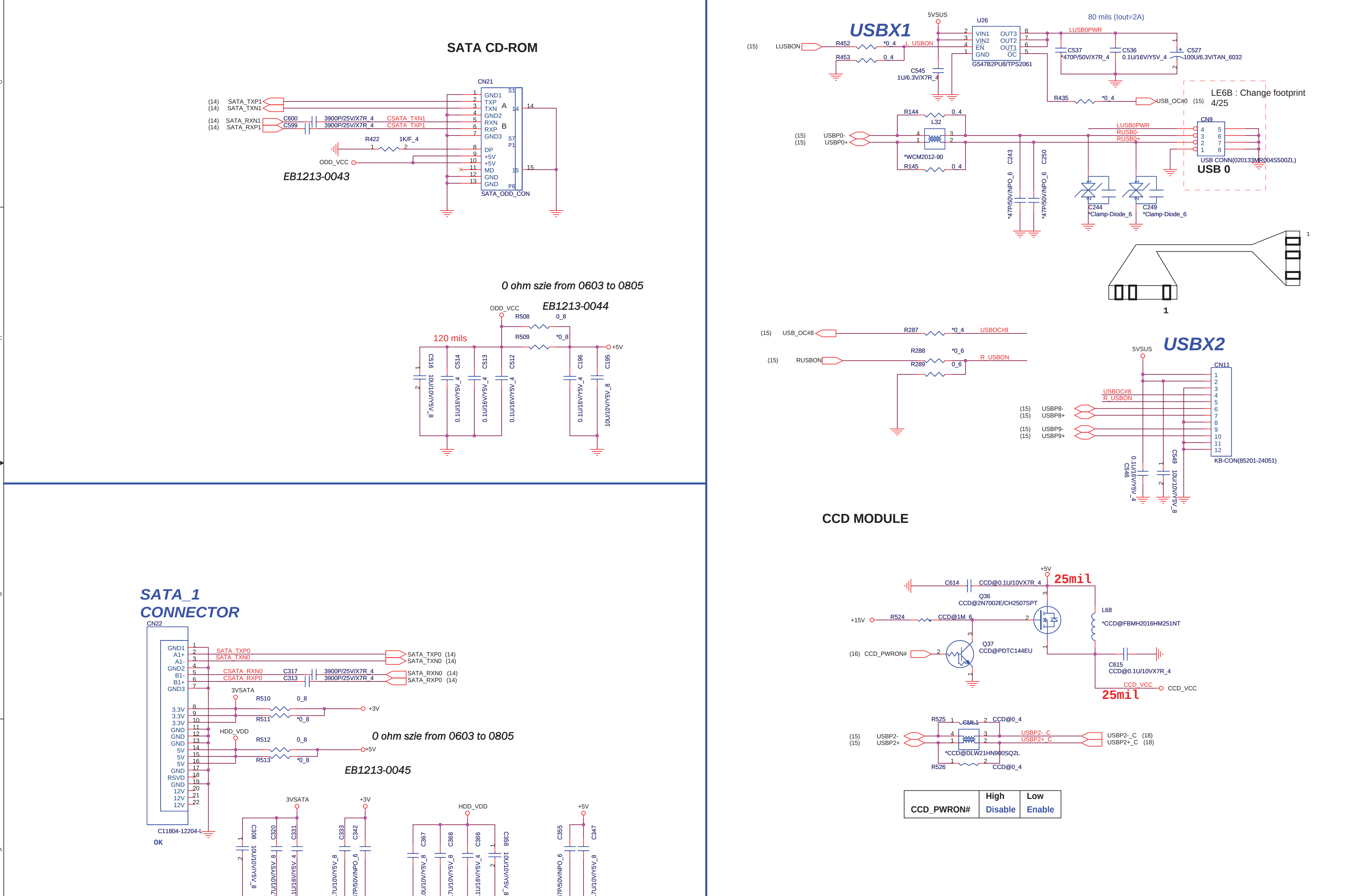


PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	New Card/BlueTooth/Mini Card	1A

Date: Friday, May 02, 2008 Sheet 26 of 34



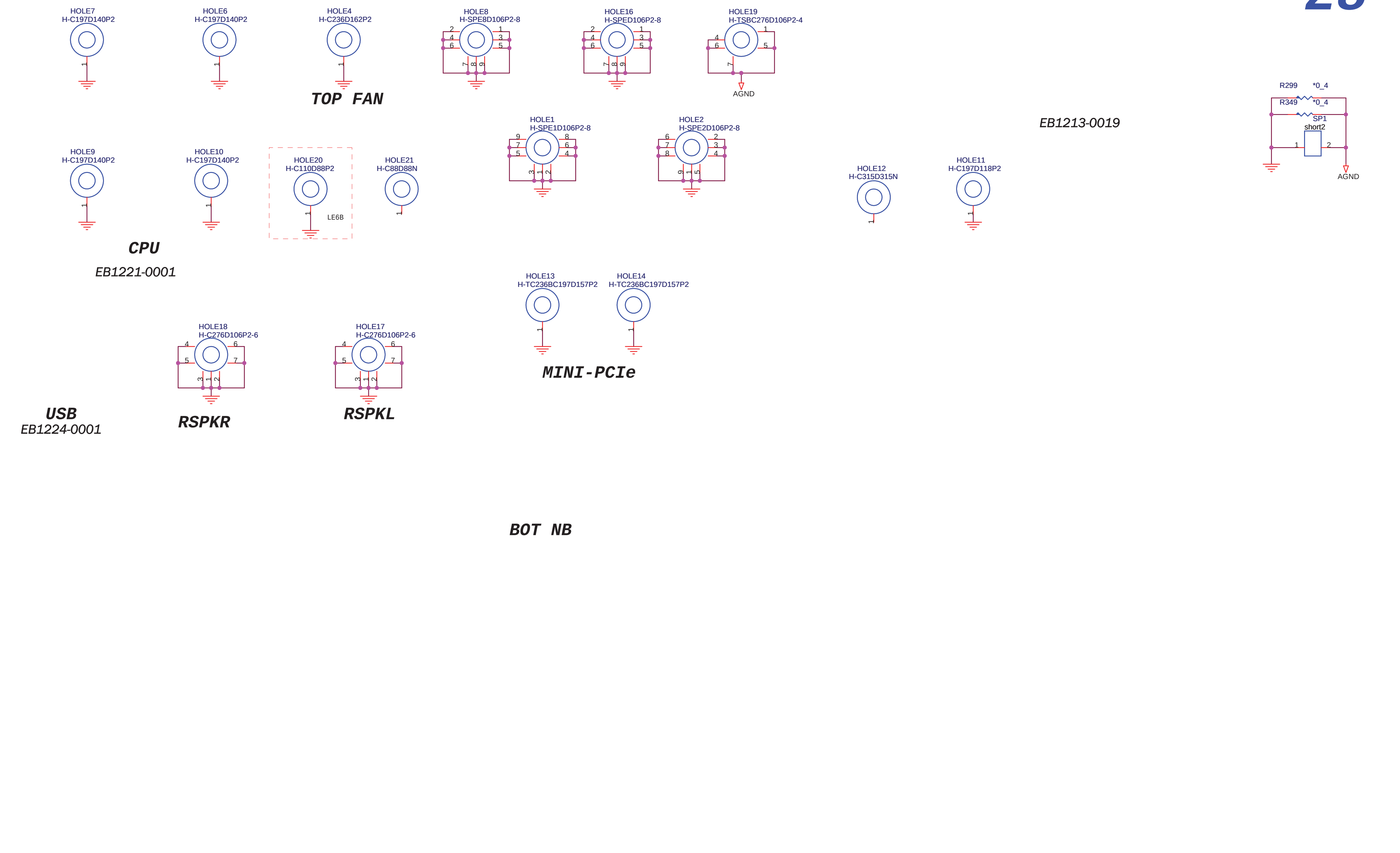
CCD_PWRON#	High	Low
	Disable	Enable

PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
C	SATA HDD/ODD USB*1	1A

Date: Friday, May 02, 2008 Sheet 27 of 34



PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	EMI PAD/SCREW/DEBUG PORT	1A

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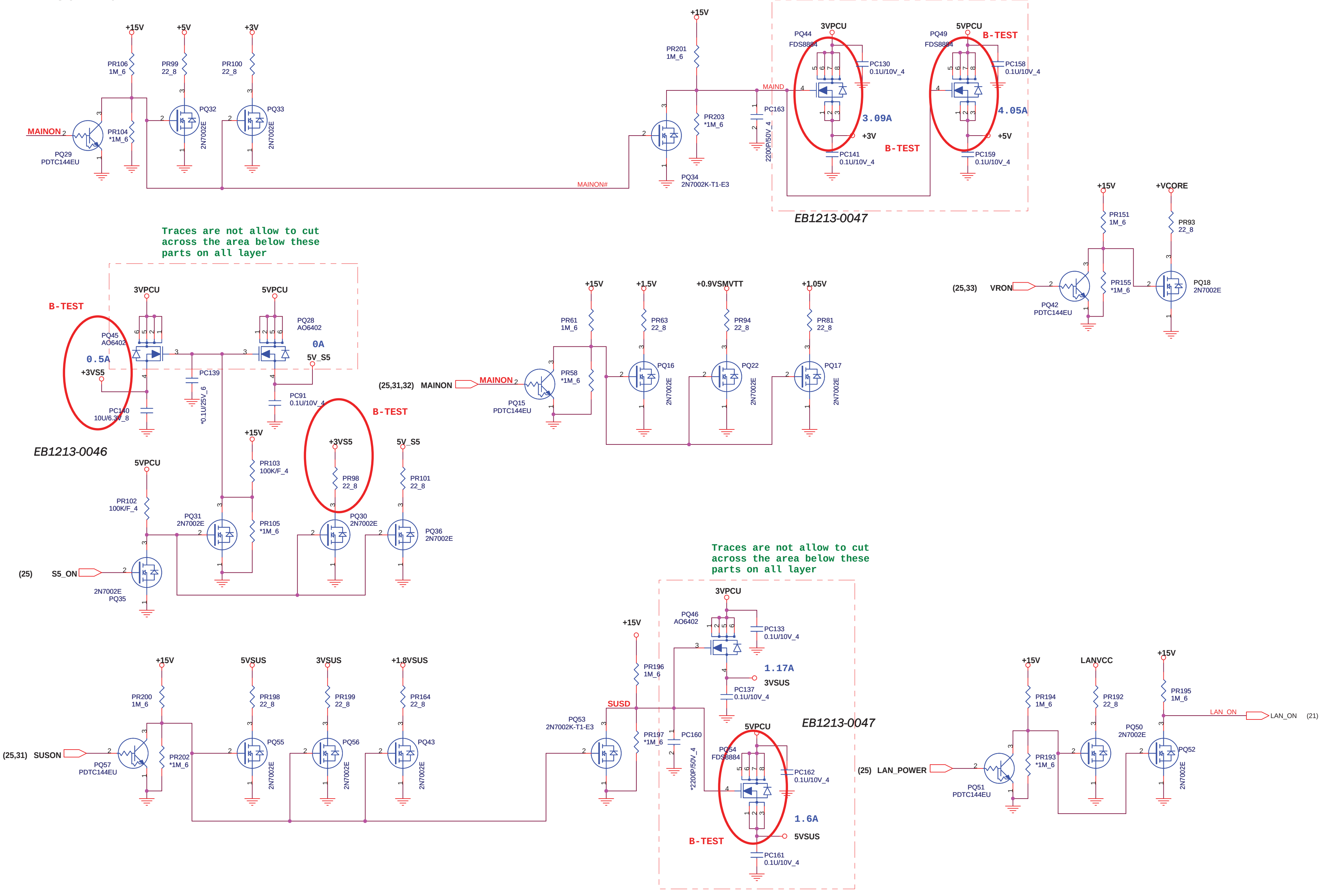
DISCHARGE

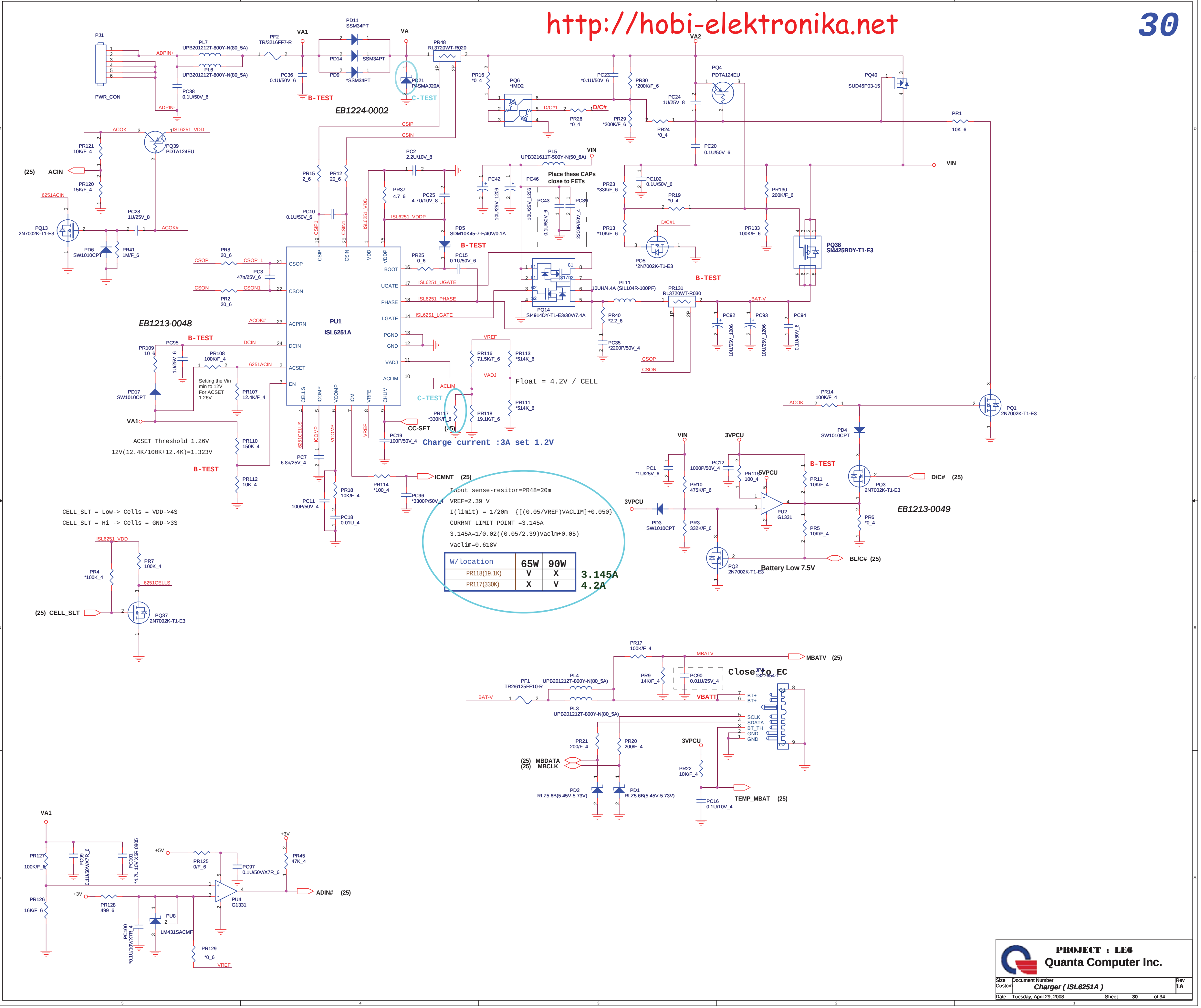


PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	1A

Date: Friday, May 02, 2008 Sheet 29 of 34



EB1224-0002
EB1213-0048
EB1213-0049
Place these CAPs close to FETs
Float = 4.2V / CELL
Charge current :3A set 1.2V
Setting the Vin min to 12V For ACSET 1.26V
ACSET Threshold 1.26V
12V(12.4K/100K+12.4K)=1.323V
CELL_SLT = Low-> Cells = VDD->4S
CELL_SLT = Hi -> Cells = GND->3S
Input sense-resitor=PR48=20m
VREF=2.39 V
I(limit) = 1/20m {[(0.05/VREF)VACLIM]+0.050}
CURRNT LIMIT POINT =3.145A
3.145A=1/0.02((0.05/2.39)Vaclm+0.05)
Vaclm=0.618V
W/location 65W 90W
PR118(19.1K) V X
PR117(330K) X V
3.145A
4.2A
Battery Low 7.5V
Close to EC
PU1 ISL6251A
B-TEST
C-TEST
PROJECT : LE6
Quanta Computer Inc.
Charger (ISL6251A)
Rev 1A
Date: Tuesday, April 29, 2008
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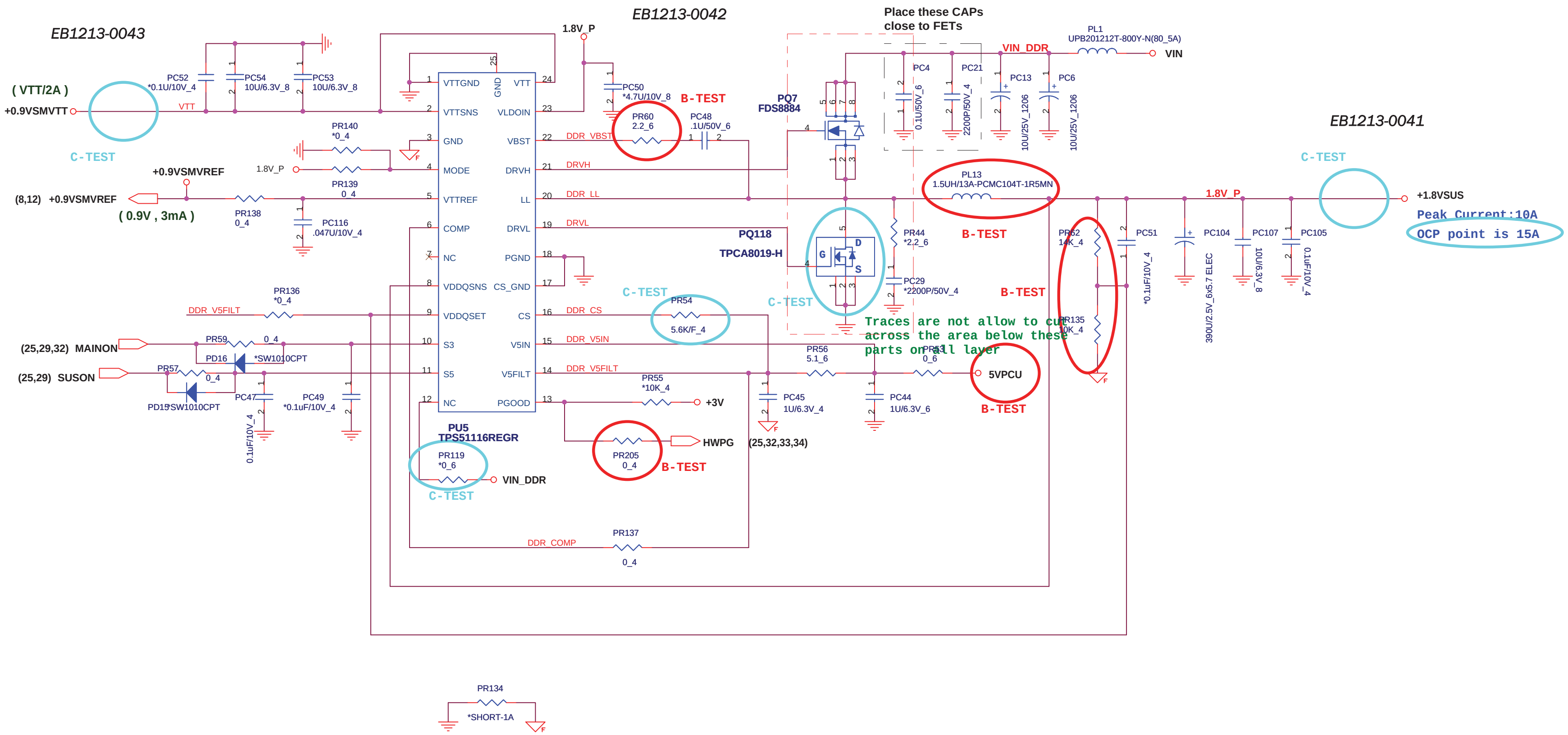

PROJECT : LE6

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Size	Document Number	Rev
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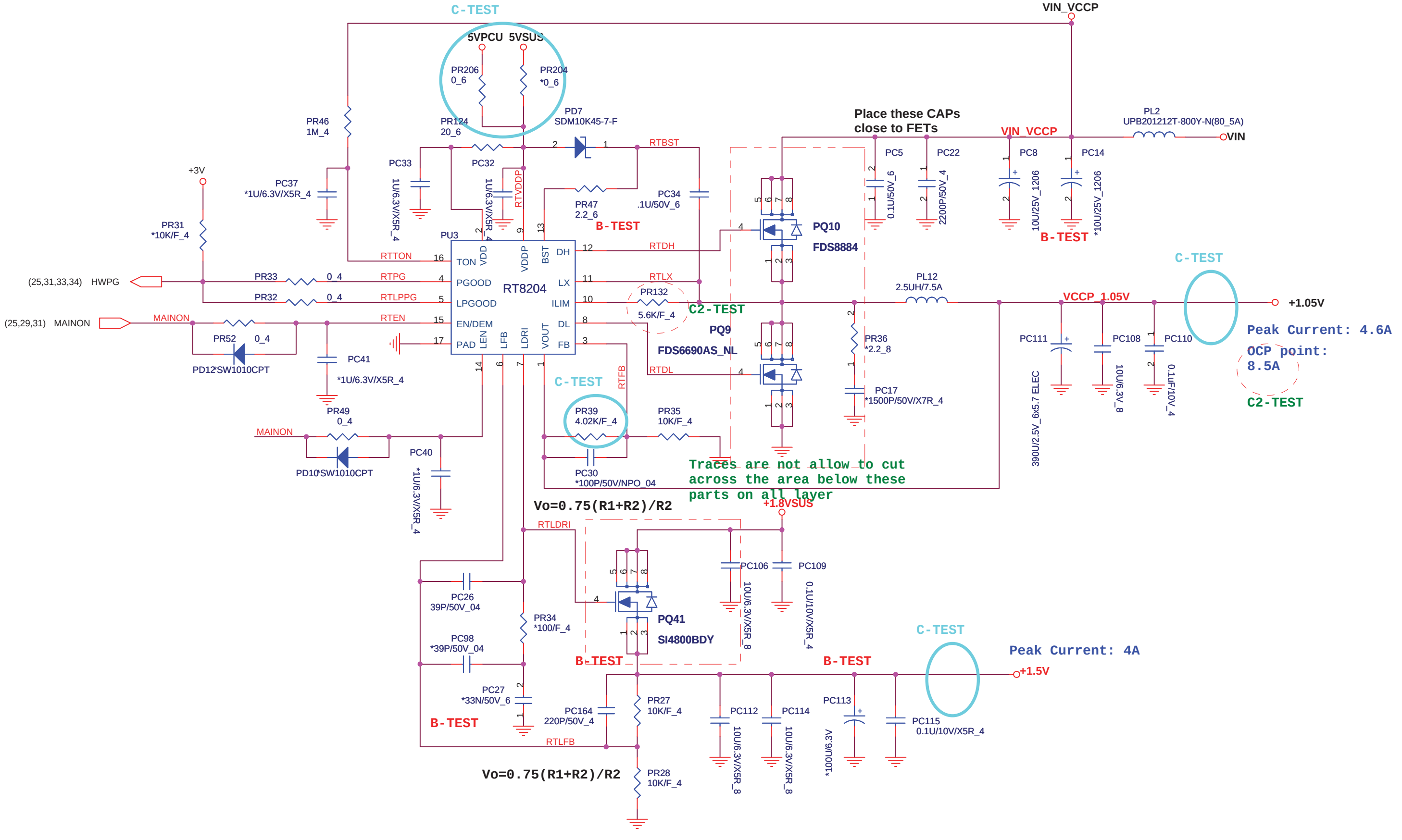

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Size	Document Number	Rev
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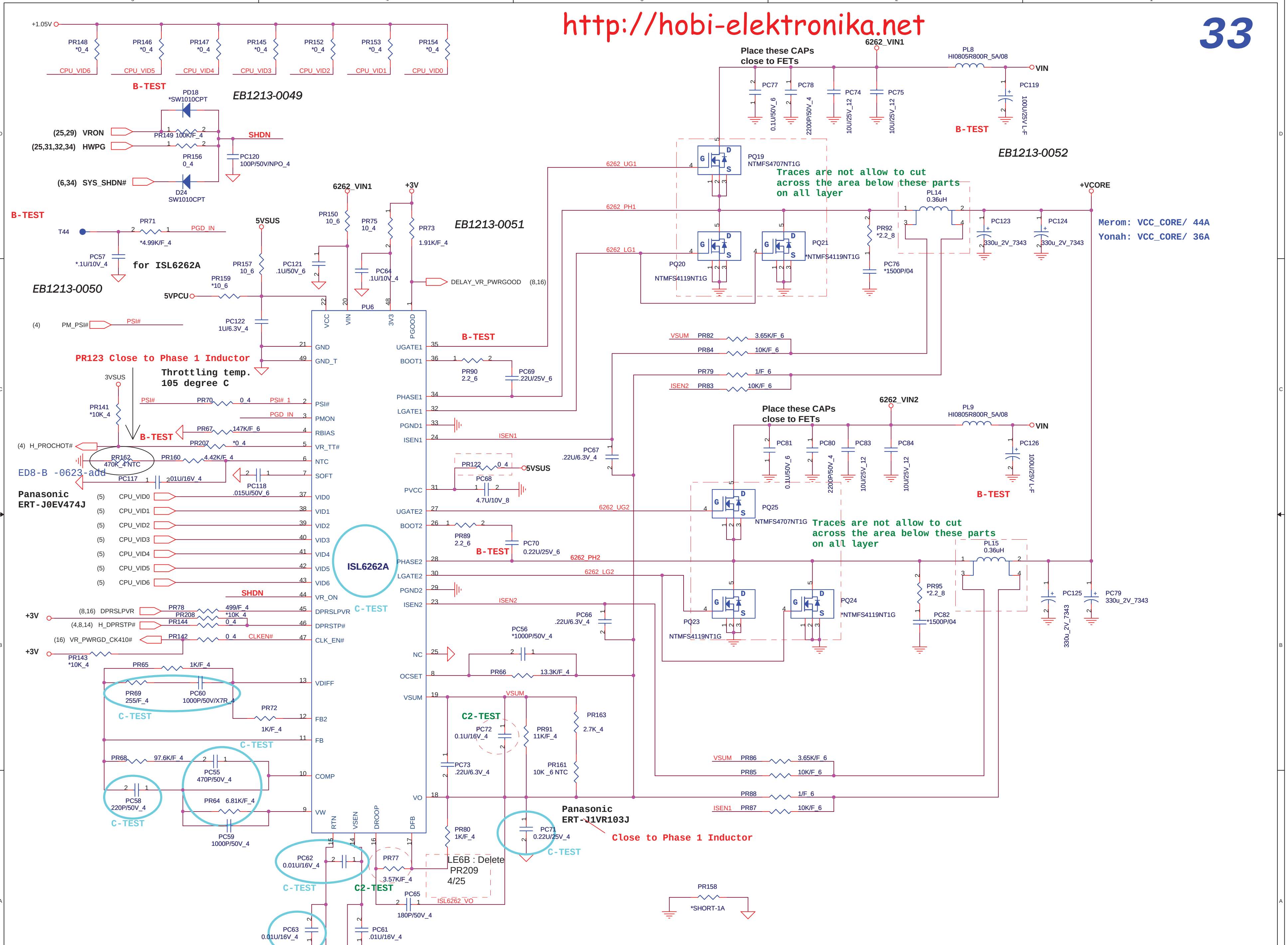

PROJECT : LE6

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Size	Document Number	Rev
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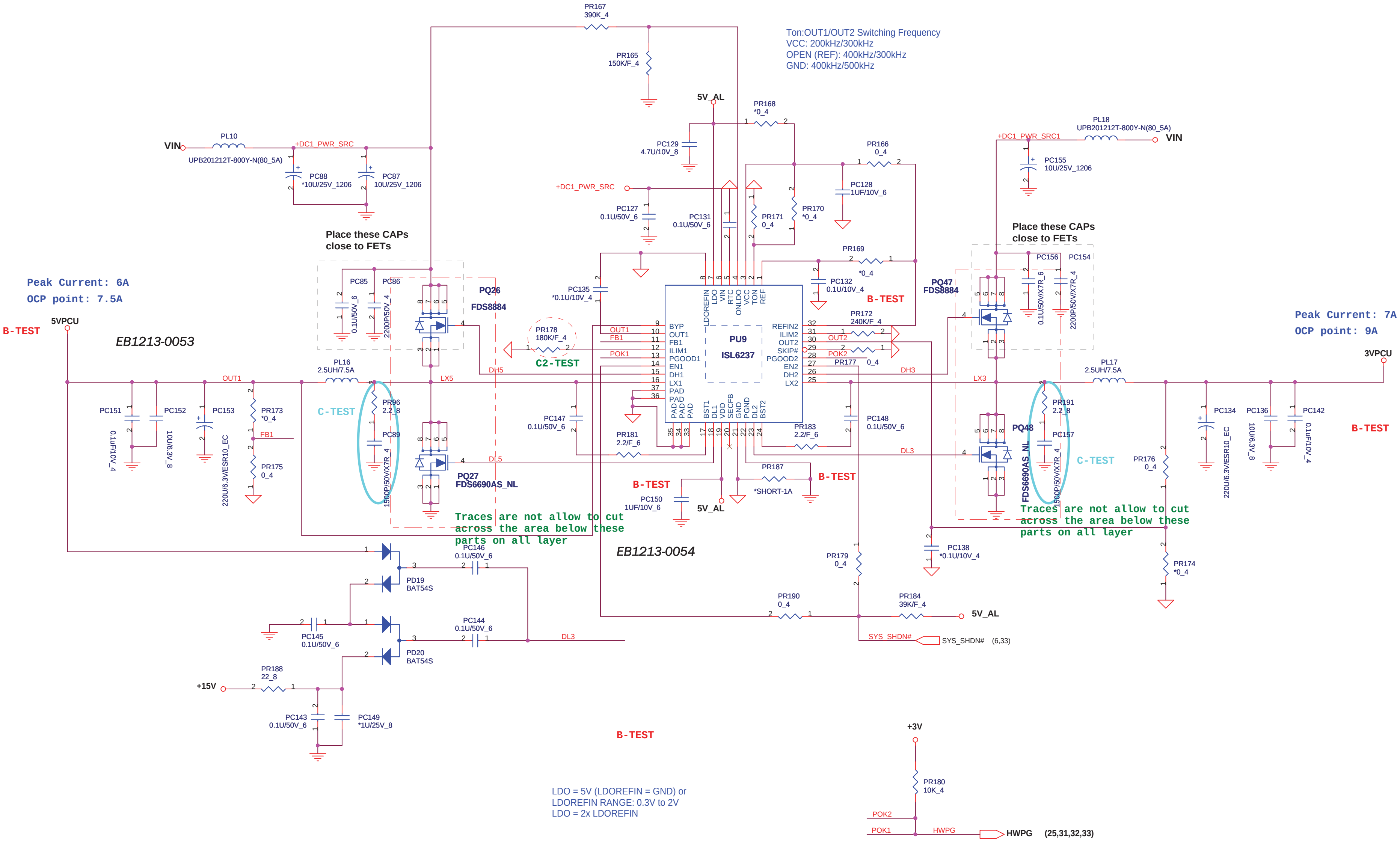
DC/DC 3VPCU/5VPCU/+15V



PROJECT : LE6

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Size	Document Number	Rev
Custom	3V/5V (ISL6237)	3A

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