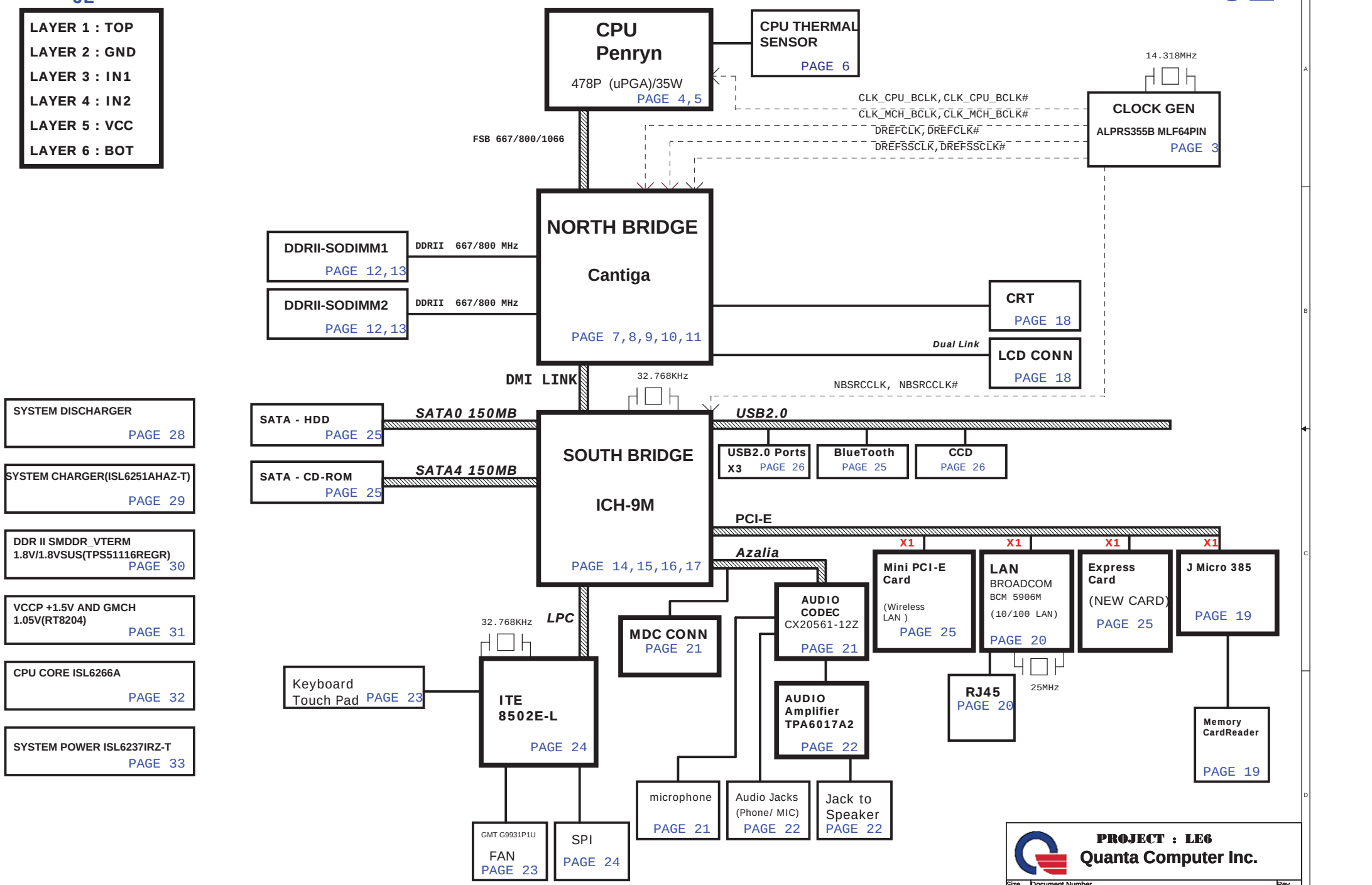
LE6 BLOCK DIAGRAM

01

PCB STACK UP

6L

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT



PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGERAM	1A

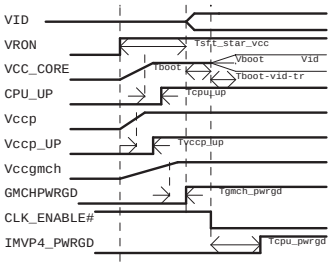
Date: Wednesday, April 23, 2008 Sheet 1 of 34

Board Stack up Description

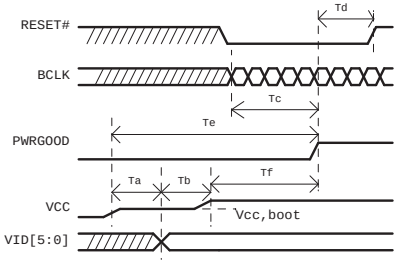
PCB Layers

Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		BOTTOM

Power On Sequencing Timing Diagram



YONAH Power-up Timing Specifications

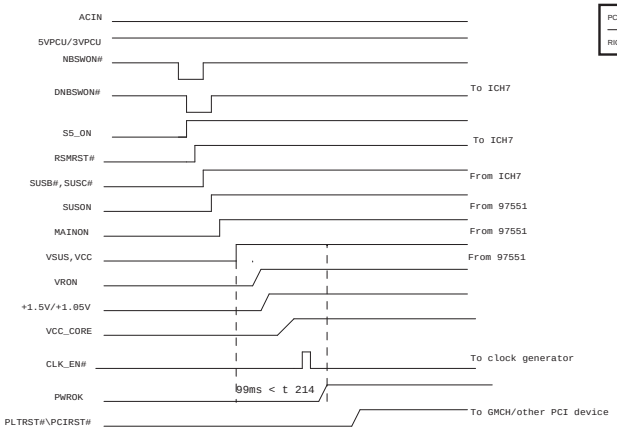


Ta=VCC and VCCP asseration to VID[5:0] vaild
Tb=VID[5:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

Voltage Rails

Voltage Rails	ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5/1.5V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.8VSUS	X	X			SUSON
SMDDR_VTERM/+2.5V/+3V/+5V/+12V	X				MAINON
+VCC_GFX_CORE/+1.2V_GFX_PCIE	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL

ACIN POWER ON TIMING

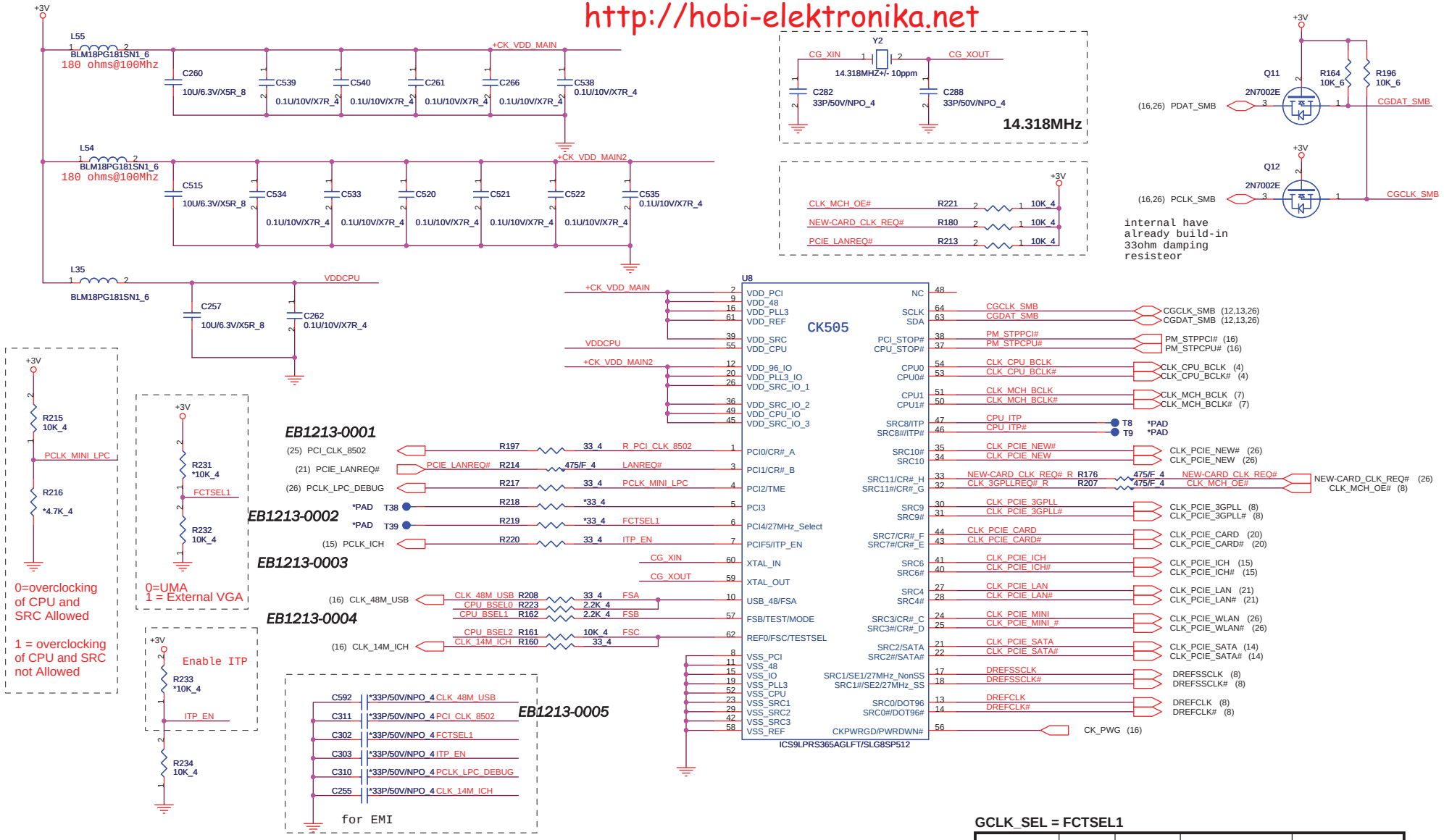


PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
RICOH832	AD25	REQ0# / GNT0#	INT E#/F#

PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM INFORMATION	1A

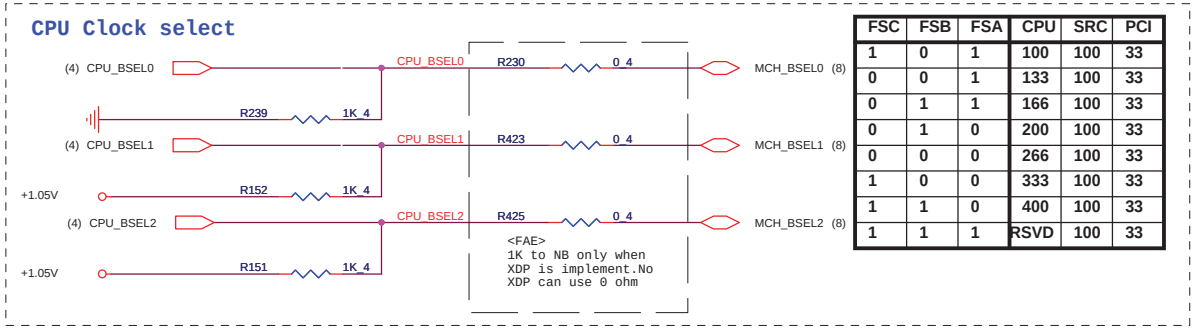
Date: Friday, May 02, 2008 Sheet 2 of 34



GCLK_SEL = FCTSEL1

FCTSEL1 (PIN6)	PIN13	PIN14	PIN24	PIN25
0=UMA	DREFCLK	DREFCLK#	SRCT1/LCDT_100	SRCT1/LCDT_100

CPU Clock select



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

Date: Friday, May 02, 2008 Sheet 3 of 34

(3,5,7,8,10,11,14,17,29,32,33) +1.05V

U24A

(7) H_A#[35:3]

ADDR GROUP 0

H_A#3 J4
H_A#4 L5
H_A#5 L4
H_A#6 K5
H_A#7 M3
H_A#8 N2
H_A#9 J1
H_A#10 N3
H_A#11 P5
H_A#12 P2
H_A#13 L2
H_A#14 P4
H_A#15 P1
H_A#16 R1

(7) H_ADSTB#0
(7) H_REQ#[4:0]

H_REQ#0 K3
H_REQ#1 H2
H_REQ#2 K2
H_REQ#3 J3
H_REQ#4 L1

H_A#[35:3]

ADDR GROUP 1

H_A#17 Y2
H_A#18 U5
H_A#19 R3
H_A#20 W6
H_A#21 U4
H_A#22 Y5
H_A#23 U1
H_A#24 R4
H_A#25 T5
H_A#26 T3
H_A#27 W2
H_A#28 W5
H_A#29 Y4
H_A#30 U2
H_A#31 V4
H_A#32 W3
H_A#33 AA4
H_A#34 AB2
H_A#35 AA3

(7) H_ADSTB#1

(14) H_A20M#
(14) H_FERR#
(14) H_IGNNE#

(14) H_STPCLK#
(14) H_INTR
(14) H_NMI
(14) H_SMI#

ADDR GROUP 0: A[3]# A[4]# A[5]# A[6]# A[7]# A[8]# A[9]# A[10]# A[11]# A[12]# A[13]# A[14]# A[15]# A[16]# ADSTB[0]#

ADDR GROUP 1: A[17]# A[18]# A[19]# A[20]# A[21]# A[22]# A[23]# A[24]# A[25]# A[26]# A[27]# A[28]# A[29]# A[30]# A[31]# A[32]# A[33]# A[34]# A[35]# ADSTB[1]#

ICH: A20M# FERR# IGNNE#

STPCLK# LINT0 LINT1 SMI#

CONTROL

ADS# H1
BNR# E2
BPRI# G5

DEFER# H5
DRDY# F21
DBSY# E1

BR0# F1

IERR# D20
INIT# B3

LOCK# H4

RESET# C1
RS[0]# F3
RS[1]# F4
RS[2]# G3
TRDY# G2

HIT# G6
HITM# E4

H_ADS# (7)
H_BNR# (7)
H_BPRI# (7)

H_DEFER# (7)
H_DRDY# (7)
H_DBSY# (7)

HBREQ#0 (7)

H_IERR# R36 56.2/F_4 +1.05V
H_INIT# (14)

H_LOCK# (7)
H_CPURST# (7)

H_RS#0
H_RS#1
H_RS#2

H_RS#[2:0] (7)
H_TRDY# (7)

H_HIT# (7)
H_HITM# (7)

XDP/ITP SIGNALS

BPM[0]# AD4
BPM[1]# AD3
BPM[2]# AD1
BPM[3]# AC4
PRDY# AC2
PREQ# AC1
TCK AC5
TDI AA6
TDO AB3
TMS AB5
TRST# AB6
DBR# C20

ITP_BPM#0
ITP_BPM#1
ITP_BPM#2
ITP_BPM#3
ITP_BPM#4
ITP_BPM#5
ITP_TCK
ITP_TDI
ITP_TDO
ITP_TMS
ITP_TRST#

SYS_RST# (16)

EB1213-0006

THERMAL

PROCHOT# D21
THERMDA A24
THERMDC B25

THERMTRIP# C7

R495 *0_4 H_PROCHOT# (33) +1.05V
R33 68_4 +1.05V
H_THERMDA (6)
H_THERMDC (6)
PM_THRMTRIP# (8,14)

H CLK

BCLK[0] A22
BCLK[1] A21

CLK_CPU_BCLK (3)
CLK_CPU_BCLK# (3)

Quard Core Only

TDI_1/RSV F6
TDO_2/RSV D3

RSVD[06] D2

BMP_1#[0]/RSV N5
BMP_1#[1]/RSV M4
BMP_1#[2]/RSV B2
BMP_1#[3]/VSS AE8
DCLKPH_1/VSS D8
ACLKPH_1/VSS F8
GTLREF_2/RSV D22
THRMDA_1/RSV T2
THRMDC_1/RSV V3
HFPLL_1/VSS AA8
SPARE_1[4]/VSS AC8
BR1#/VCC AA7

ITP_BPM1#0
ITP_BPM1#1
ITP_BPM1#2
ITP_BPM1#3

GTLREF_CTL
H_GTLREF2
H_THERMDA2
H_THERMDC2

TP117
TP1
TP47

+VCORE

Penryn Ball-out Rev 1a

+1.05V R96 *51/F_4

CPU_TEST2 R37 *1K/F_4
CPU_TEST1 R40 *1K/F_4

LE6B: Connect to +VCORE according to Intel DG 0429

EB1213-0007

U24B

(7) H_D#[63:0]

DATA GRP 0

H_D#0 E22
H_D#1 F24
H_D#2 E26
H_D#3 G22
H_D#4 F23
H_D#5 G25
H_D#6 E25
H_D#7 E23
H_D#8 K24
H_D#9 G24
H_D#10 J24
H_D#11 J23
H_D#12 H22
H_D#13 F26
H_D#14 K22
H_D#15 H23

(7) H_DSTBN#0
(7) H_DSTBP#0
(7) H_DINV#0

DATA GRP 1

H_D#16 N22
H_D#17 K25
H_D#18 P26
H_D#19 R23
H_D#20 L23
H_D#21 M24
H_D#22 L22
H_D#23 M23
H_D#24 P25
H_D#25 P23
H_D#26 P22
H_D#27 T24
H_D#28 R24
H_D#29 L25
H_D#30 T25
H_D#31 N25

(7) H_DSTBN#1
(7) H_DSTBP#1
(7) H_DINV#1

DATA GRP 2

H_D#32 Y22
H_D#33 AB24
H_D#34 V24
H_D#35 V26
H_D#36 V23
H_D#37 T22
H_D#38 U25
H_D#39 U23
H_D#40 Y25
H_D#41 W22
H_D#42 Y23
H_D#43 W24
H_D#44 W25
H_D#45 AA23
H_D#46 AA24
H_D#47 AB25

H_DSTBN#2 (7)
H_DSTBP#2 (7)
H_DINV#2 (7)

DATA GRP 3

H_D#48 AF24
H_D#49 AD24
H_D#50 AA21
H_D#51 AB22
H_D#52 AB21
H_D#53 AC26
H_D#54 AD20
H_D#55 AE22
H_D#56 AF23
H_D#57 AC25
H_D#58 AF21
H_D#59 AD21
H_D#60 AC22
H_D#61 AD23
H_D#62 AF22
H_D#63 AC23

H_DSTBN#3 (7)
H_DSTBP#3 (7)
H_DINV#3 (7)

MISC

GTLREF AD26
TEST1 C23
TEST2 D25
TEST3 C24
TEST4 AF26
TEST5 AE1
TEST6 A26
TEST7 C3

BSEL[0] B22
BSEL[1] B23
BSEL[2] C21

(3) CPU_BSEL0
(3) CPU_BSEL1
(3) CPU_BSEL2

CPU_TEST1
CPU_TEST2
CPU_TEST3
CPU_TEST4
CPU_TEST5
CPU_TEST6
CPU_TEST7

H_GTLREF

R403 1K/F_4
R404 2K/F_4

TP3
TP105
TP122
TP2
TP36

COMP[0] R26
COMP[1] U26
COMP[2] AA1
COMP[3] Y1

COMP0 R405 27.4/F_4
COMP1 R406 54.9/F_4
COMP2 R420 27.4/F_4
COMP3 R419 54.9/F_4

EB1213-0010

DPRSTP# E5
DPSLP# B5
DPWR# D24
PWRGOOD D6
SLP# D7
PSI# AF6

H_DPRSTP# (8,14,33)
H_DPSLP# (14)
H_DPWR# (7)
H_PWRGD (14)
H_CPUSLP# (7)
PM_PSI# (33)

Penryn Ball-out Rev 1a

+1.05V

R101 *51/F_4
R421 *54.9/F_4
R89 54.9/F_4
R90 54.9/F_4
R514 54.9/F_4

ITP_TDI
ITP_TMS
ITP_TDO

TP118

H_CPURST# R108 *1K/F_4 ITP_RST#

TP42

SYS_RST#

TP116

ITP_BPM#2

TP121

ITP_BPM#4
ITP_BPM#5

TP120
TP119

C165 *100P/50V_4

EB1213-0008

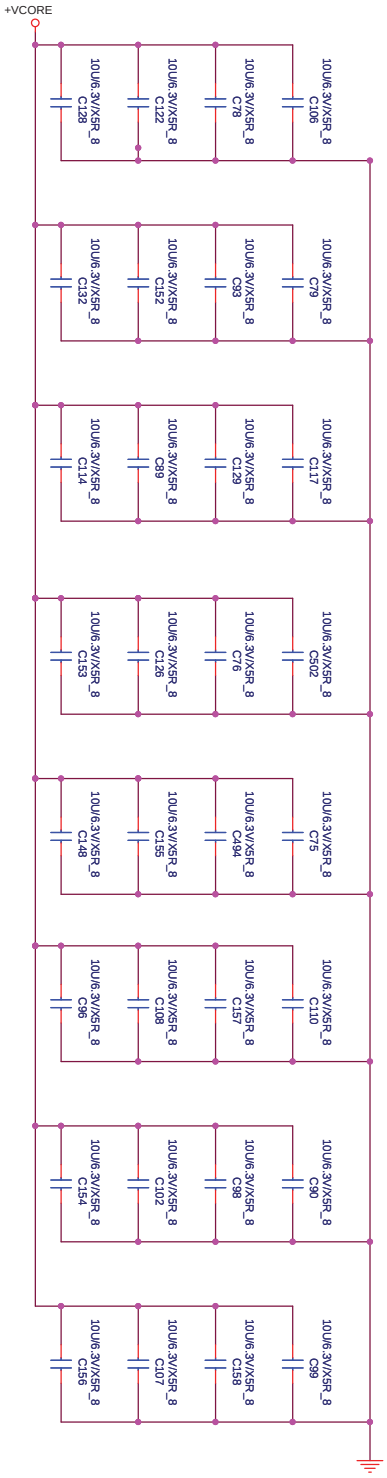
R102 54.9/F_4 ITP_TCK
R98 54.9/F_4 ITP_TRST#

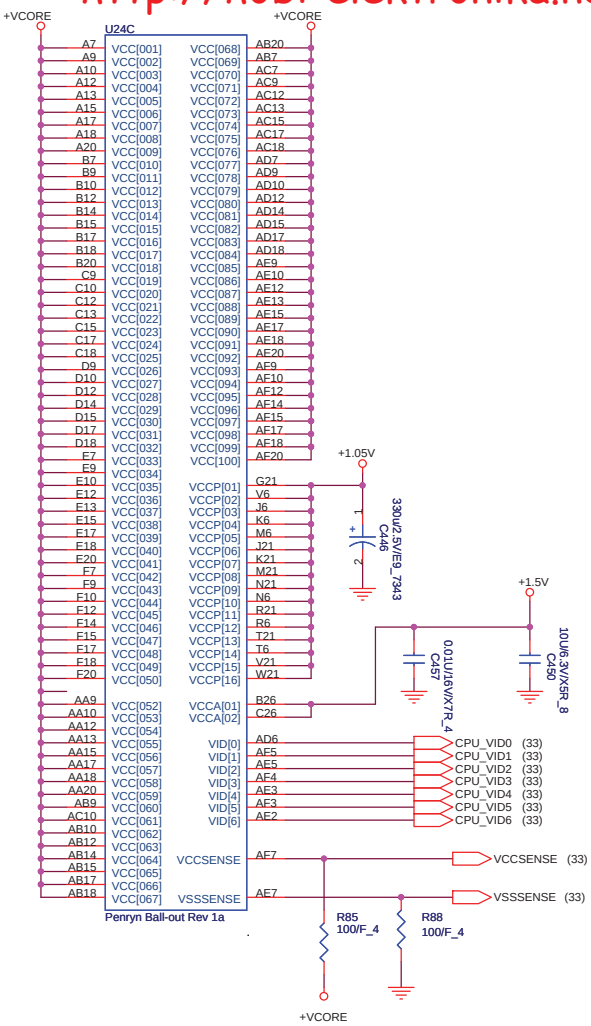
PROJECT : LE6

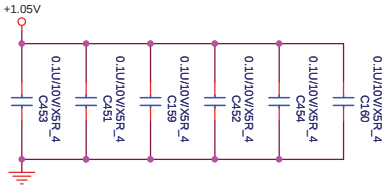
Quanta Computer Inc.

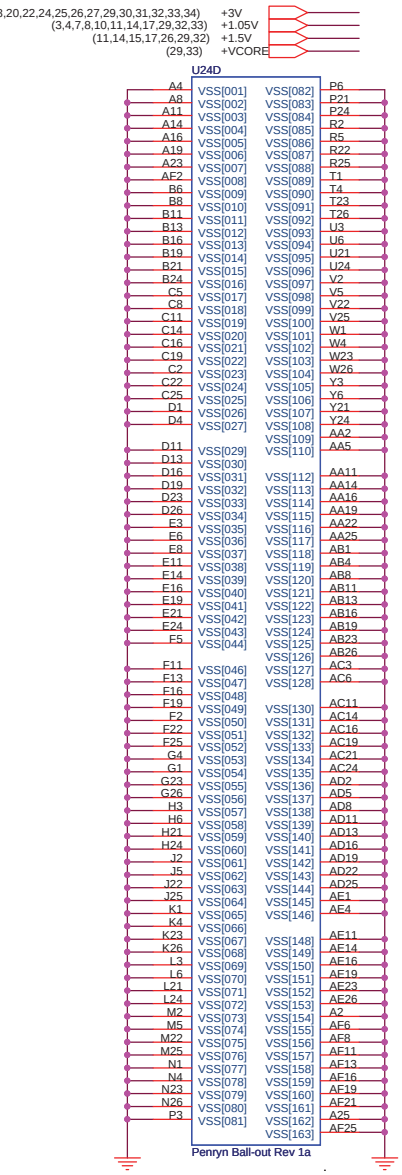
Size	Document Number	Rev
Custom	PENRYN 1/2	2A

Date: Friday, May 02, 2008 Sheet 4 of 34







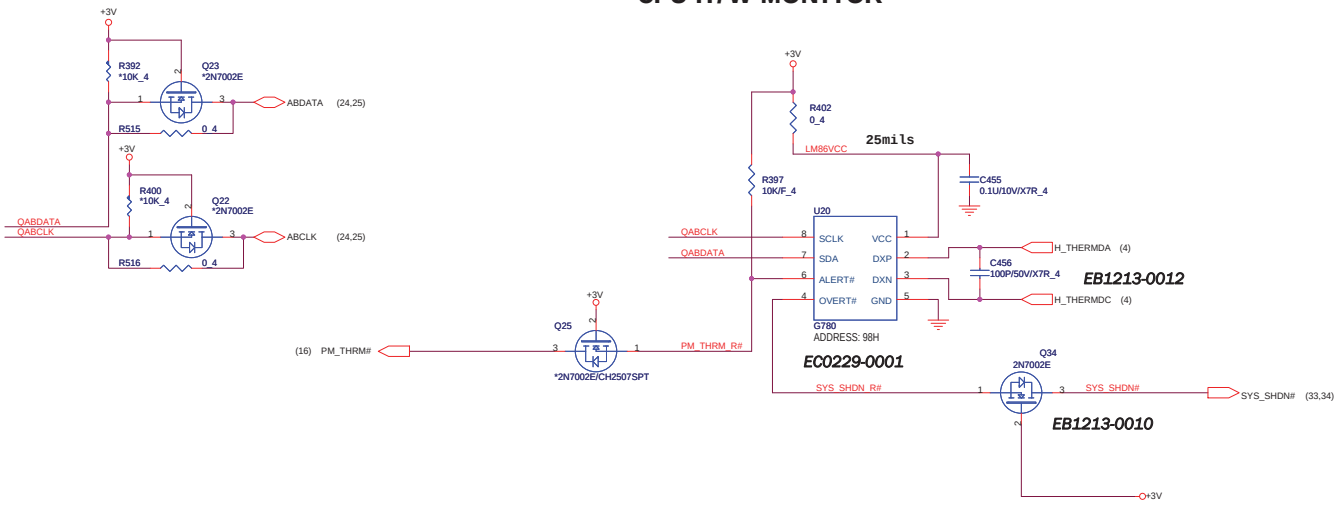


PROJECT : LE6

Quanta Computer Inc.

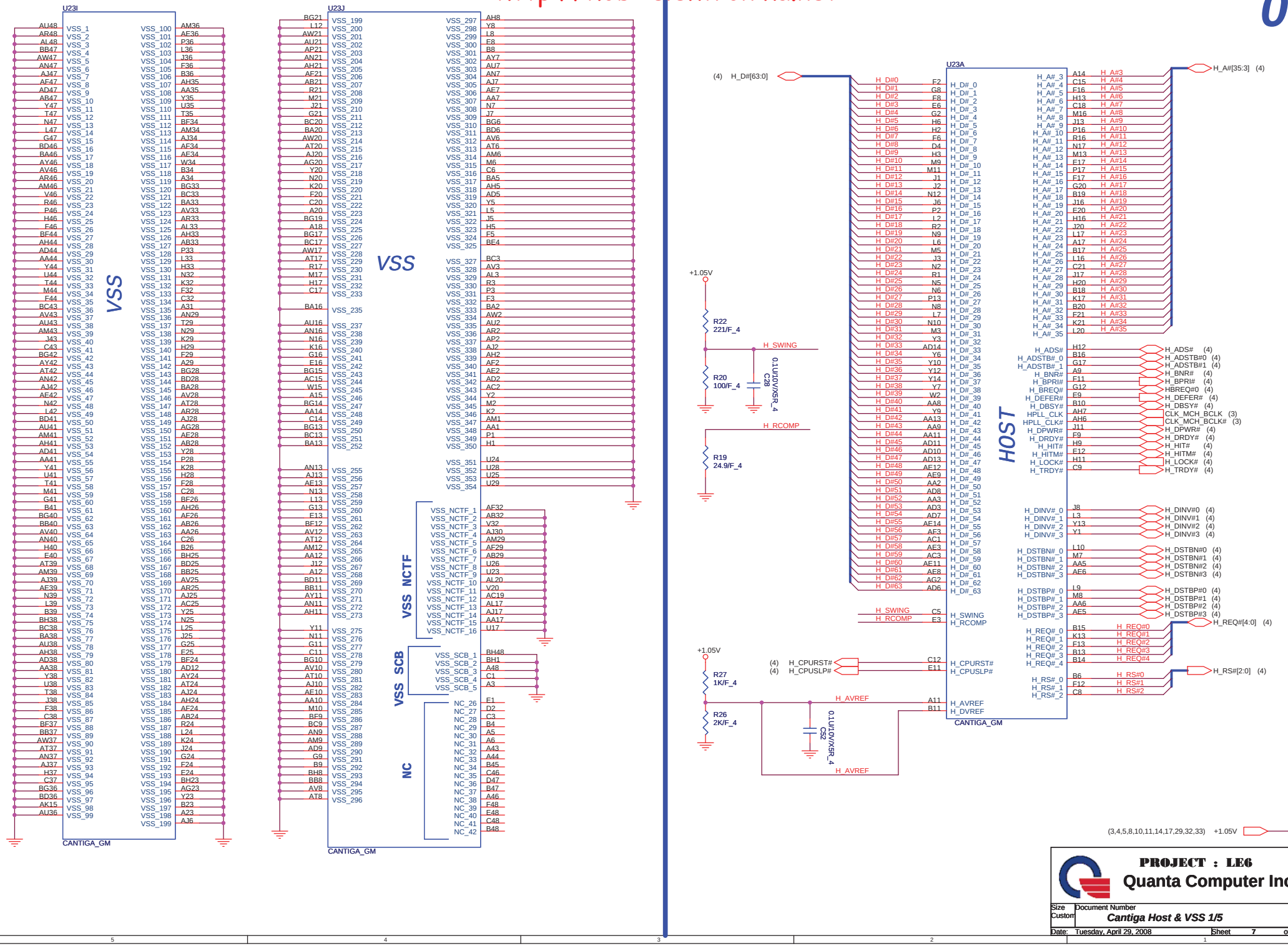
Size	Document Number	Rev
Custom	PENRYN 2/2	1A
Date: Tuesday, April 29, 2008	Sheet 5 of 34	

CPU H/W MONITOR



EB1213-0011

PROJECT : LE6		
Quanta Computer Inc.		
Size: C	Document Number: CPU THERMAL/HW PRODCT	Rev: 1A
Date: Tuesday, April 29, 2008	Sheet 6 of 34	



PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga Host & VSS 1/5	1A
Date: Tuesday, April 29, 2008	Sheet 7 of 34	

MCH_CFG_5 DMIx2 selection

Low: DMIx2
High: DMIx4 (Default)

MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)

MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reserved

MCH_CFG_6 iTPM Host Interface

Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)

MCH_CFG_7 Intel (R) Management Engine Crypto

Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

U23B

RSVD
RSVD1 M36
RSVD2 N36
RSVD3 R33
RSVD4 T33
RSVD5 AH9
RSVD6 AH10
RSVD7 AH12
RSVD8 AH13
RSVD9 K12
RSVD14 T24
RSVD15 B31
RSVD16 B2
RSVD17 M1
RSVD20 AY21
RSVD22 BG23
RSVD23 BF23
RSVD24 BH18
RSVD25 BF18

DDR CLK/ CONTROL/COMPENSATION
SA_CK_0 AP24 → M_A_CLK0 (12)
SA_CK_1 AT21 → M_A_CLK1 (12)
SB_CK_0 AV24 → M_B_CLK0 (12)
SB_CK_1 AU20 → M_B_CLK1 (12)
SA_CK#_0 AR24 → M_A_CLK0# (12)
SA_CK#_1 AR21 → M_A_CLK1# (12)
SB_CK#_0 AU24 → M_B_CLK0# (12)
SB_CK#_1 AV20 → M_B_CLK1# (12)
SA_CKE_0 BC28 → M_A_CKE0 (12,13)
SA_CKE_1 AY28 → M_A_CKE1 (12,13)
SB_CKE_0 AY36 → M_B_CKE0 (12,13)
SB_CKE_1 BB36 → M_B_CKE1 (12,13)
SA_CS#_0 BA17 → M_A_CS#0 (12,13)
SA_CS#_1 AY16 → M_A_CS#1 (12,13)
SB_CS#_0 AV16 → M_B_CS#0 (12,13)
SB_CS#_1 AR13 → M_B_CS#1 (12,13)
SA_ODT_0 BD17 → M_A_ODT0 (12,13)
SA_ODT_1 AY17 → M_A_ODT1 (12,13)
SB_ODT_0 BF15 → M_B_ODT0 (12,13)
SB_ODT_1 AY13 → M_B_ODT1 (12,13)
SM_RCOMP BG22 SM_RCOMP R62 80.6/F_4
SM_RCOMP# BH21 SM_RCOMP# R48 80.6/F_4
SM_RCOMP_VOH BF28 SM_RCOMP_VOH
SM_RCOMP_VOL BH28 SM_RCOMP_VOL
SM_VREF AV42 +0.9VSMVREF_MCH
SM_PWROK AR36 SW_PWROK_NB R79 10K/F_4
SM_REXT BF17 SM_REXT R35 499/F_4
SM_DRAMRST# BC36 TP_SM_DRAMRST# TP18
+1.8VSUS

CLK
DPLL_REF_CLK B38 → DREFCLK (3)
DPLL_REF_CLK# A38 → DREFCLK# (3)
DPLL_REF_SSCLK F41 → DREFSSCLK (3)
DPLL_REF_SSCLK# F41 → DREFSSCLK# (3)
PEG_CLK F43 → CLK_PCIE_3GPLL (3)
PEG_CLK# E43 → CLK_PCIE_3GPLL# (3)

ME JTAG
TP22 AL34 ME_JTAG_TCK
TP16 AK34 ME_JTAG_TDI
TP15 AN35 ME_JTAG_TDO
TP14 AM35 ME_JTAG_TMS

DMI
DMI_RXN_0 AE41 DMI_TXN0
DMI_RXN_1 AE37 DMI_TXN1
DMI_RXN_2 AE47 DMI_TXN2
DMI_RXN_3 AH39 DMI_TXN3 → DMI_TXN[3:0] (15)
DMI_RXP_0 AE40 DMI_TXP0
DMI_RXP_1 AE38 DMI_TXP1
DMI_RXP_2 AE48 DMI_TXP2
DMI_RXP_3 AH40 DMI_TXP3 → DMI_TXP[3:0] (15)
DMI_TXN_0 AE35 DMI_RXN0
DMI_TXN_1 AE43 DMI_RXN1
DMI_TXN_2 AE46 DMI_RXN2
DMI_TXN_3 AH42 DMI_RXN3 → DMI_RXN[3:0] (15)
DMI_TXP_0 AD35 DMI_RXP0
DMI_TXP_1 AE44 DMI_RXP1
DMI_TXP_2 AE46 DMI_RXP2
DMI_TXP_3 AH43 DMI_RXP3 → DMI_RXP[3:0] (15)

CFG
(3) MCH_BSEL0 → T25
(3) MCH_BSEL1 → R25
(3) MCH_BSEL2 → P25
TP5 MCH_CFG_3 P20
TP10 MCH_CFG_4 P24
R55 *2.2K_4 MCH_CFG_5 C26
R52 *2.2K_4 MCH_CFG_6 N24
R50 *2.2K_4 MCH_CFG_7 M24
TP8 MCH_CFG_8 F21
R51 *2.2K_4 MCH_CFG_10 C23
TP9 MCH_CFG_11 C24
TP7 MCH_CFG_14 N21
TP4 MCH_CFG_15 R20
R42 *2.2K_4 MCH_CFG_16 M20
TP6 MCH_CFG_17 L21
TP13 MCH_CFG_18 H21
R57 *4.02K/F_4 MCH_CFG_20 P29
CFG_0 … CFG_20 T28

GRAPHICS VID
GFX_VID_0 B33 GFXVR_VID_0 TP114
GFX_VID_1 B32 GFXVR_VID_1 TP115
GFX_VID_2 G33 GFXVR_VID_2 TP17
GFX_VID_3 F33 GFXVR_VID_3 TP24
GFX_VID_4 E33 GFXVR_VID_4 TP20
GFX_VR_EN C34 GFXVR_EN TP113

PM
(16) PM_SYNC# → R29
(4,14,33) H_DPRSTP# → B7
(12,13) PM_EXTTS#0 → N33
(13) PM_EXTTS#1 → P32
(16,33) DELAY_VR_PWRGOOD → AT40
(15) PLT_RST-R# → R24 100/F_4 RST_IN# MCH → AT11
(4,14) PM_THRMTRIP# → R500 *0_4 → T20
(16,33) DPRSLPVR → R32
PM_SYNC# … DPRSLPVR

LE6B : Add R500
4/29

NC
BG48 … BG1 NC_1 … NC_26

ME
CL_CLK AH37 CL_CLK0 (16)
CL_DATA AH36 CL_DATA0 (16)
CL_PWROK AN36 ECPWROK (16,25)
CL_RST# AJ35 CL_RST#0 (16)
CL_VREF AH34 MCH_CLVREF
0.35 V
+1.05V
R113 1K/F_4
R109 499/F_4
0.1U/10V/X5R_4 C108

MISC
DDPC_CTRLCLK N28 DDPC_CTRLCLK TP11
DDPC_CTRLDATA M28 DDPC_CTRLDATA R527 *0_4 TP12
SDVO_CTRLCLK G36 SDVO_CLK R528 *0_4 TP134
SDVO_CTRLDATA E36 SDVO_DATA R529 *0_4 TP135
CLKREQ# K36 → CLK_MCH_OE# (3)
ICH_SYNC# H36 → MCH_ICH_SYNC# (16)
TSATN# B12 MCH_TSATN R25 56.2/F_4
+1.05V

HDA
HDA_BCLK B28 TP136
HDA_RST# B30 TP138
HDA_SDI B29 TP137
HDA_SDO C29 TP139
HDA_SYNC A28 TP140

EC0225-0001

U23C

LVDS
(18) DPST_PWM → DPST_PWM_INT L32
(18) LVDS_BLON → LVDS_BLON_INT G32
L_BKLT_CTRL
L_BKLT_EN
L_CTRL_CLK
+3V R72 10K/F_4 L_CTRL_CLK M32
R78 10K/F_4 L_CTRL_DATA M33
L_CTRL_DATA
(18) EDIDCLK → EDIDCLK_INT K33
(18) EDIDDATA → EDIDDATA_INT J33
L_DDC_CLK
L_DDC_DATA
(18) DISP_ON → DISP_ON_INT M29
L_VDD_EN
R418 2.37K/F_4 LVDS_IBG C44
LVDS_IBG
TP109 LVDS_VBG B43
LVDS_VBG
E37
E38
LVDS_VREFH
LVDS_VREFL
(18) LA_CLK# → LVDSA_CLK# C41
(18) LA_CLK → LVDSA_CLK C40
TP108 LVDSB_CLK# B37
TP110 LVDSB_CLK A37
(18) LA_DATAN0 → LVDSA_DATA#_0 H47
(18) LA_DATAN1 → LVDSA_DATA#_1 F46
(18) LA_DATAN2 → LVDSA_DATA#_2 G40
TP112 LA_DATAN3 LVDSA_DATA#_3 A40
(18) LA_DATAP0 → LVDSA_DATA_0 H48
(18) LA_DATAP1 → LVDSA_DATA_1 D45
(18) LA_DATAP2 → LVDSA_DATA_2 F40
TP111 LA_DATAP3 LVDSA_DATA_3 B40
TP107 LVDSB_DATA#_0 A41
TP25 LVDSB_DATA#_1 H38
TP19 LVDSB_DATA#_2 G37
TP23 LB_DATAN3 LVDSB_DATA#_3 J37
TP106 LVDSB_DATA_0 B42
TP26 LVDSB_DATA_1 G38
TP21 LVDSB_DATA_2 F37
TP28 LB_DATAP3 LVDSB_DATA_3 K37

TV
T2 TV_COMP1 F25
T3 TV_Y/G1 H25
T4 TV_C/R1 K25
TVA_DAC
TVB_DAC
TVC_DAC
H24 TV_RTN
R43 75/F_4
R45 75/F_4
R49 75/F_4
R83 0_4 TV_DCONSEL0 C31
R82 0_4 TV_DCONSEL1 E32
TV_DCONSEL_0
TV_DCONSEL_1

VGA
(18) CRT_B → R59 150/F_4 → CRT_B_1 E28
(18) CRT_G → R56 150/F_4 → CRT_G_1 G28
(18) CRT_R → R60 150/F_4 → CRT_R_1 J28
G29
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_IRTN
(18) DDCCLK → DDCCLK_INT H32
(18) DDCDATA → DDCDATA_INT J32
CRT_DDC_CLK
CRT_DDC_DATA
(18) HSYNC_COM → R76 33_4 → HSYNC_INT J29
R80 1.02K/F_4 CRTIREF E29
CRT_TVO_IREF
(18) VSYNC_COM → R75 33_4 → VSYNC_INT L29
CRT_HSYNC
CRT_VSYNC

PCI-EXPRESS GRAPHICS
PEG_COMPI T37
PEG_COMPO T36
PEG_COMP R81 49.9/F_4
+1.05V_PEG
PEG_RX#_0 … PEG_RX#_15 H44 … AD39
PEG_RX_0 … PEG_RX_15 H43 … AD40
PEG_TX#_0 … PEG_TX#_15 J41 … AD46
PEG_TX_0 … PEG_TX_15 J42 … AD45

CANTIGA_GM

+1.8VSUS
R69 1K/F_4
SM_RCOMP_VOH
C105 0.01U/16V/X7R_4
C100 2.2U/6.3V/X5R_6
R64 3.01K/F_4
SM_RCOMP_VOL
C115 0.01U/16V/X7R_4
C111 2.2U/6.3V/X5R_6
R61 1K/F_4

+1.8VSUS
R104 *1K/F_4
+0.9VSMVREF_MCH
R105 0_4 → +0.9VSMVREF (12,31)
C162 0.1U/10V/X5R_4
C161 470PF/50V/X7R_4
*1K/F_4
R97
HP SVTP TEST

For UMA HDMI Function

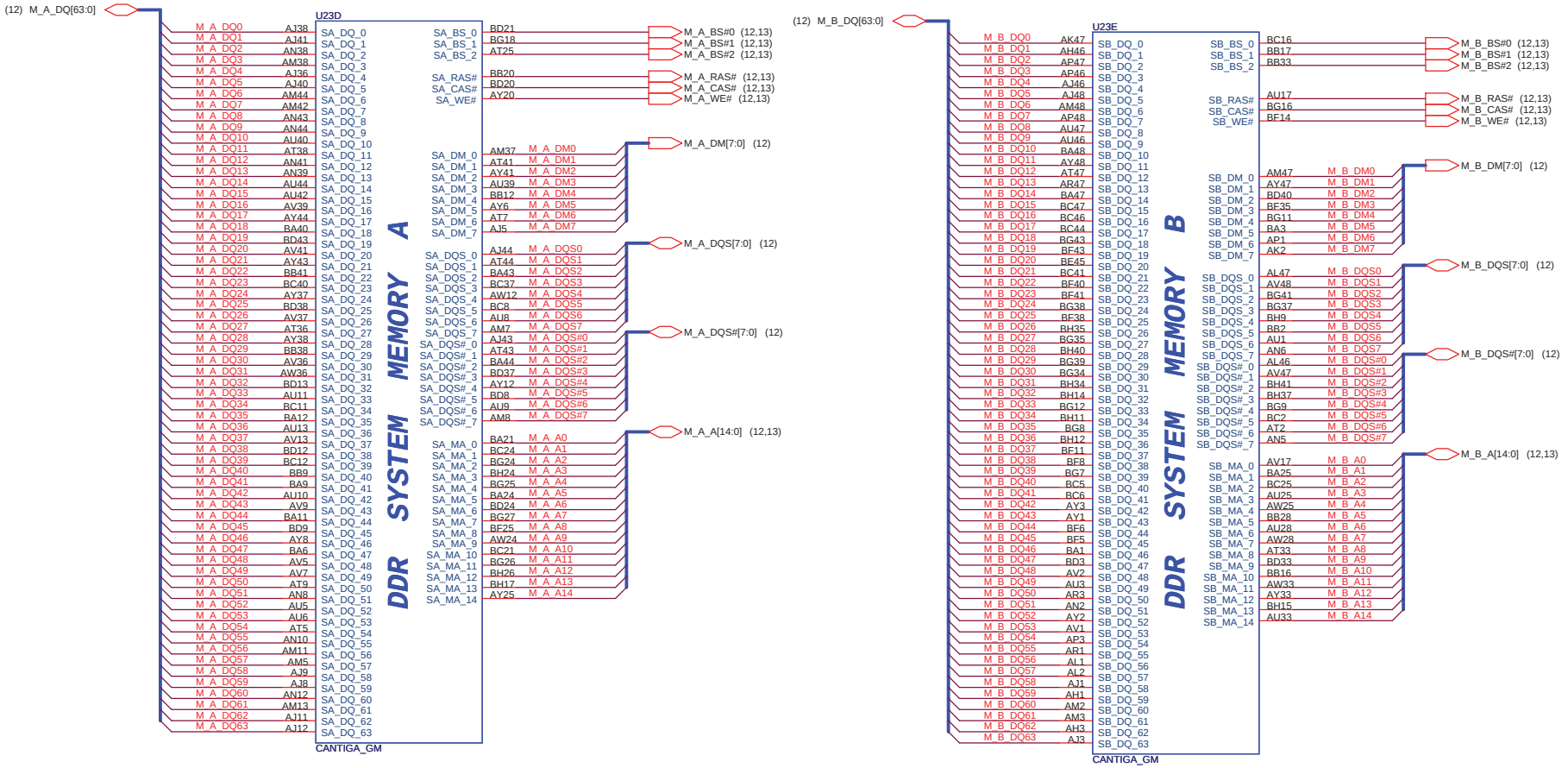
EB1213-0013

HPD# Inverting Level Shifting Circuit

PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Canting DMIDISP 2/5	1A

Date: Friday, May 02, 2008 Sheet 8 of 34

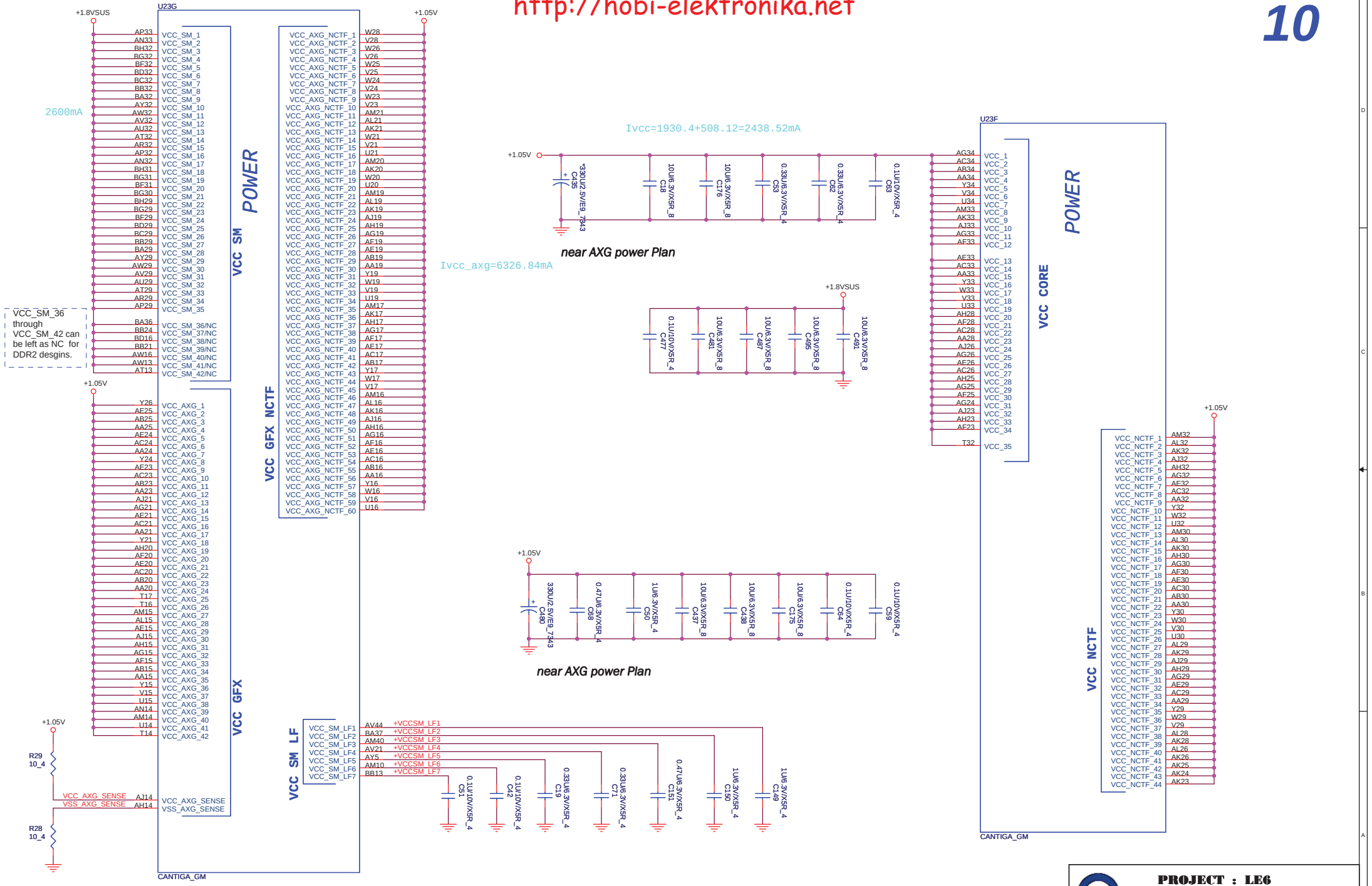


PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Canting DDR2 3/5	1A

Date: Tuesday, April 29, 2008 Sheet 9 of 34



PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Canting Vcc 4/5	1A
Date: Friday, May 02, 2008	Sheet 10 of 34	

+1.05V (3,4,5,7,8,10,14,17,29,32,33)
+3V (3,6,8,12,13,14,15,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34)
+1.5V (5,14,15,17,26,29,32)
+1.8VSUS (8,10,12,29,31,32)
+1.05V_PEG (8)

EB1213-0014

EC0225-0001

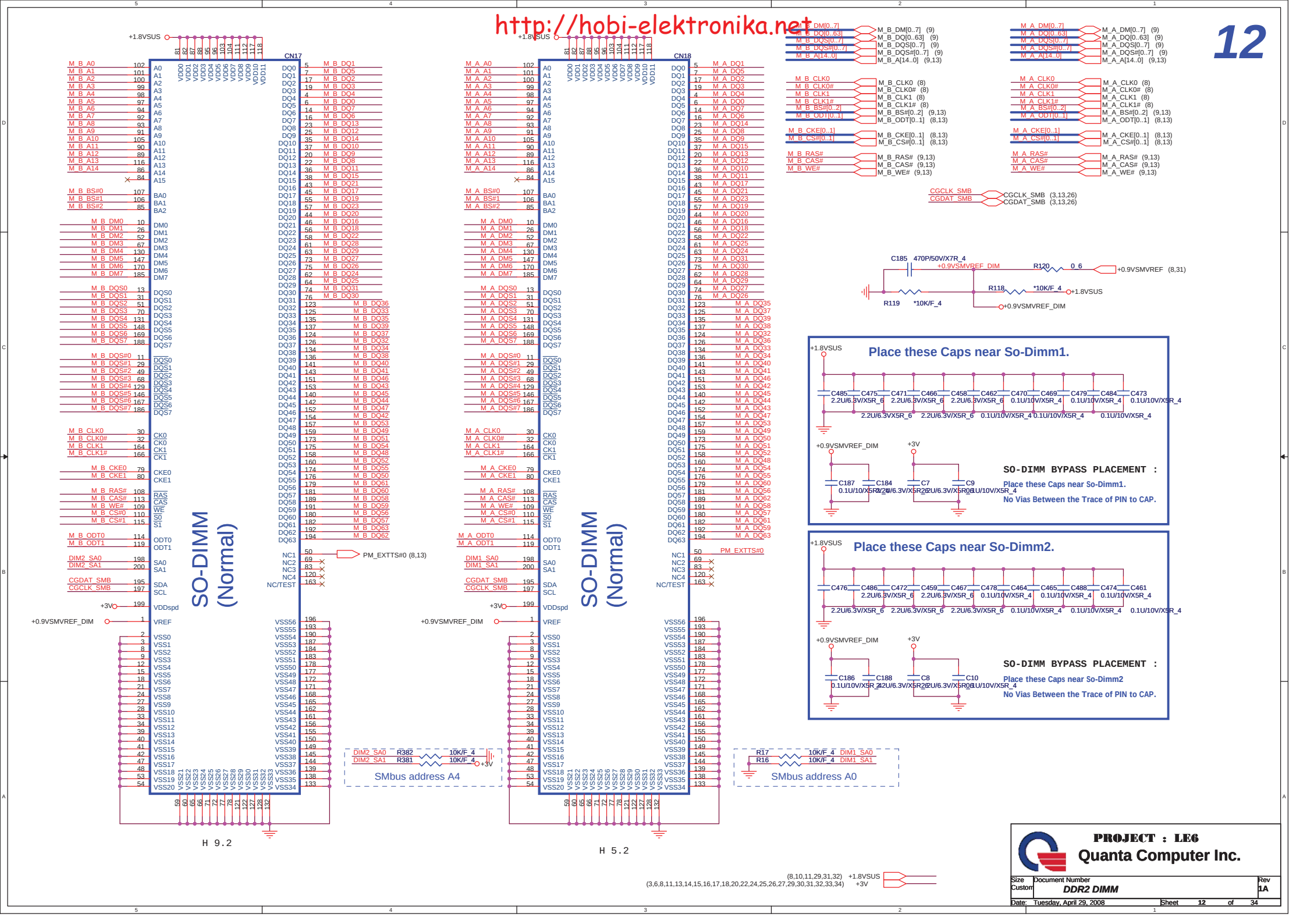
POWER

CANTIGA_GM

Modify 0829

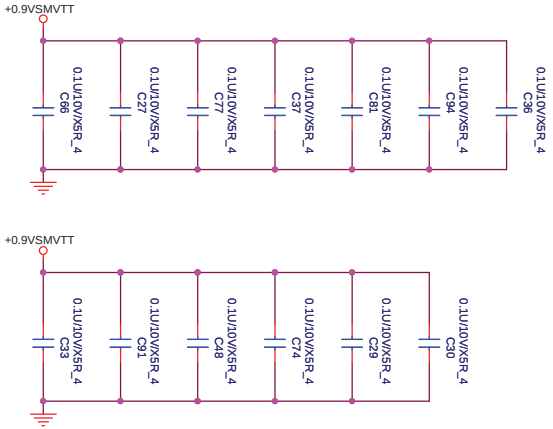
PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Canting Power 5/5	1A
Date: Tuesday, April 29, 2008	Sheet 11 of 34	

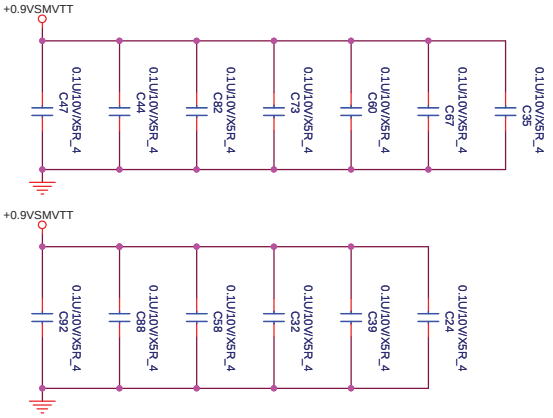


DDRII DUAL CHANNEL A,B.

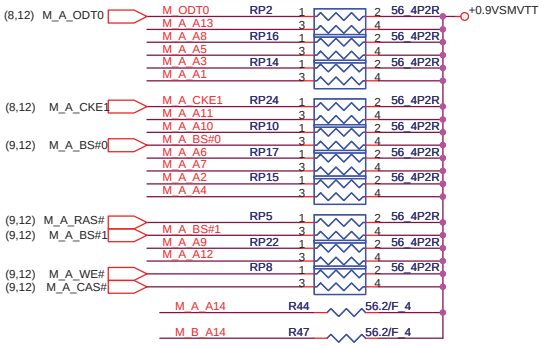
DDRII A CHANNEL

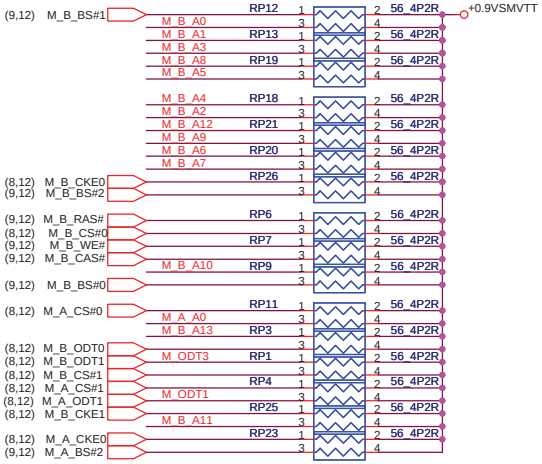


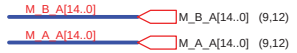
DDRII B CHANNEL

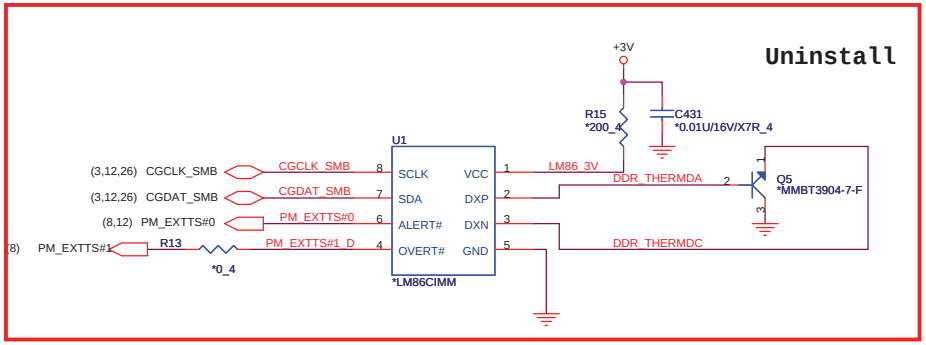


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM









+0.9VSMVTT (29,31)

+3V (3,6,8,11,12,14,15,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34)

PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	*DDR2 termination*	1A
Date: Tuesday, April 29, 2008	Sheet 13 of 34	

(18,21,24,25,29,30,34) 3VPCU
(17,25) +3VRTC
(3,6,8,11,12,13,15,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34) +3V
(5,11,15,17,26,29,32) +1.5V
(3,4,5,7,8,10,11,17,29,32,33) +1.05V
(15,16,17,29) +3VS5

20MIL

EB1213-0018

EB1213-0015

EB1213-0016

EB1213-0017

EC0225-0002

Notice: GPIO33 is also a strap pin. Don't pull it to high.

SATA HDD1

SATA HDD2

SATA ODD

U27A

ICH9M REV 1.0

SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1	
SPI	0	1	
PCI	1	0	
LPC	1	1	(default)

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

TPM physical presence	
ICH_GPIO57	Low: Default

PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M Host 1/4	1A

Date: Friday, May 02, 2008 Sheet 14 of 34

(5,11,14,17,26,29,32) +1.5V
(3,6,8,11,12,13,14,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34) +3V
(16,22,24,26,29,33) 3VSUS

EC0225-0004

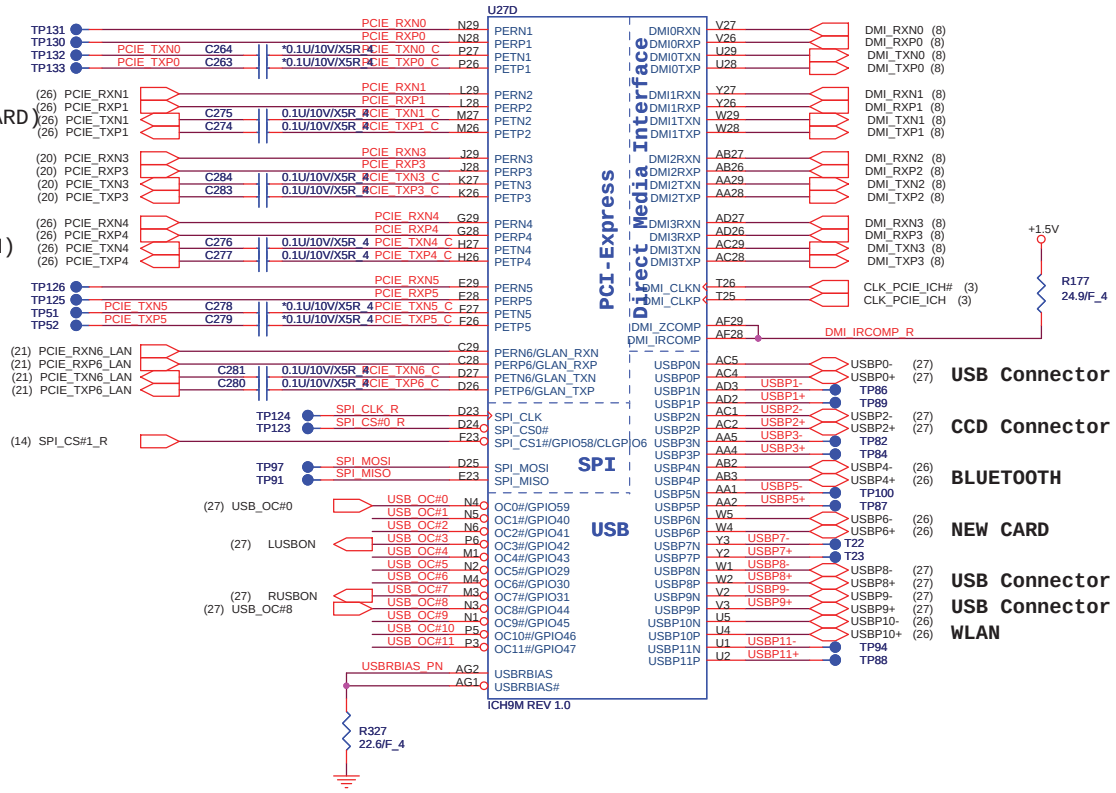
EXPRESS CARD (NEW CARD)

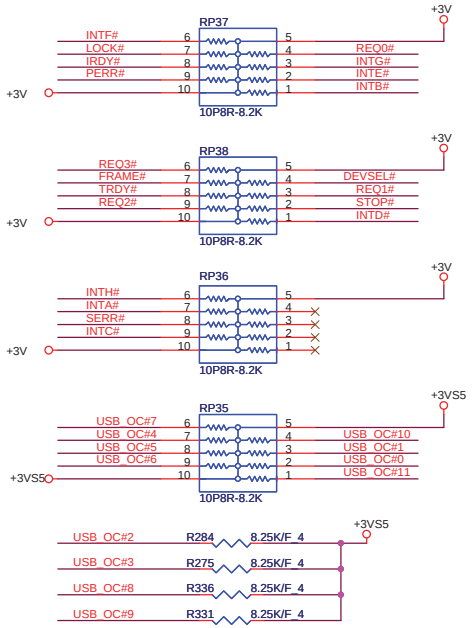
CRAD READER PCI-E

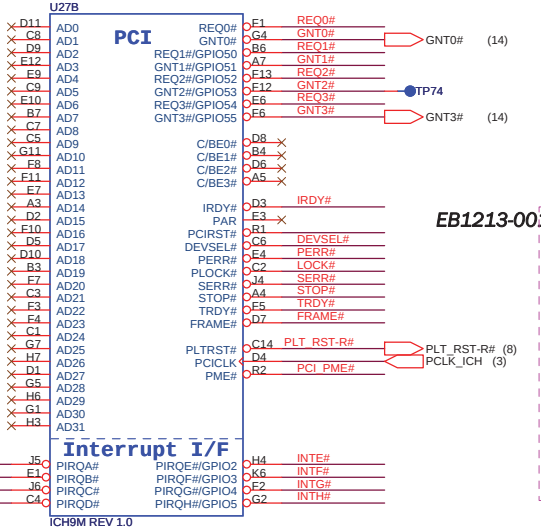
MINI CARD PCI-E(WLAN)

EC0225-0003

PCIE-LAN

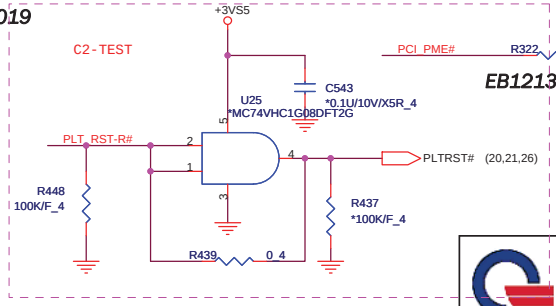




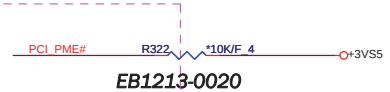


LE6B: Delete HDMI SPI flash IC and relate circuit
2008-4-24

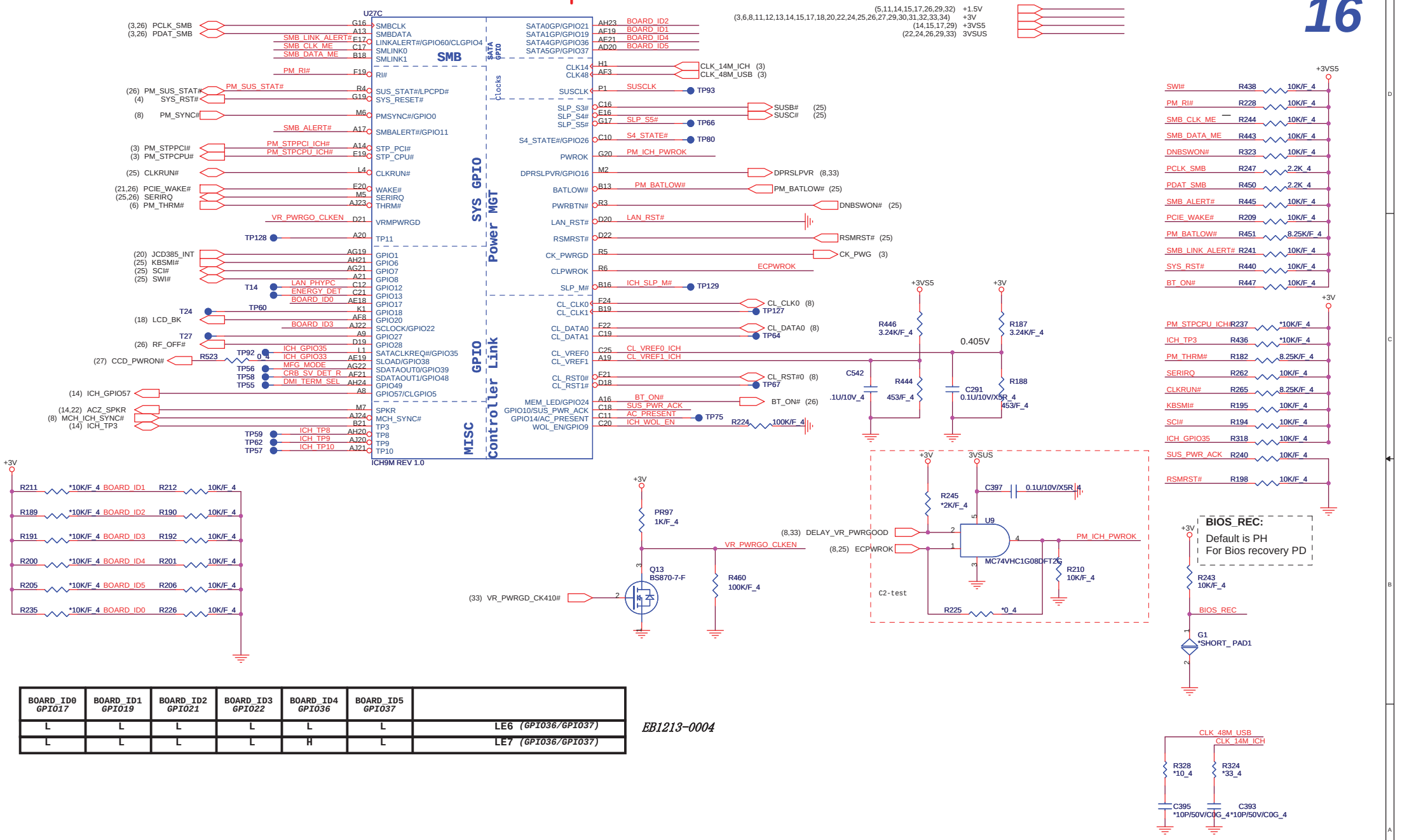
EB1213-0019



EB1213-0020



PROJECT : LE6			
Quanta Computer Inc.			
Size: Custom	Document Number: ICH9-M PCIE 2/4		Rev: 1A
Date: Friday, May 02, 2008		Sheet 15 of 34	



BOARD_ID0 GPIO17	BOARD_ID1 GPIO19	BOARD_ID2 GPIO21	BOARD_ID3 GPIO22	BOARD_ID4 GPIO36	BOARD_ID5 GPIO37	
L	L	L	L	L	L	LE6 (GPIO36/GPIO37)
L	L	L	L	H	L	LE7 (GPIO36/GPIO37)

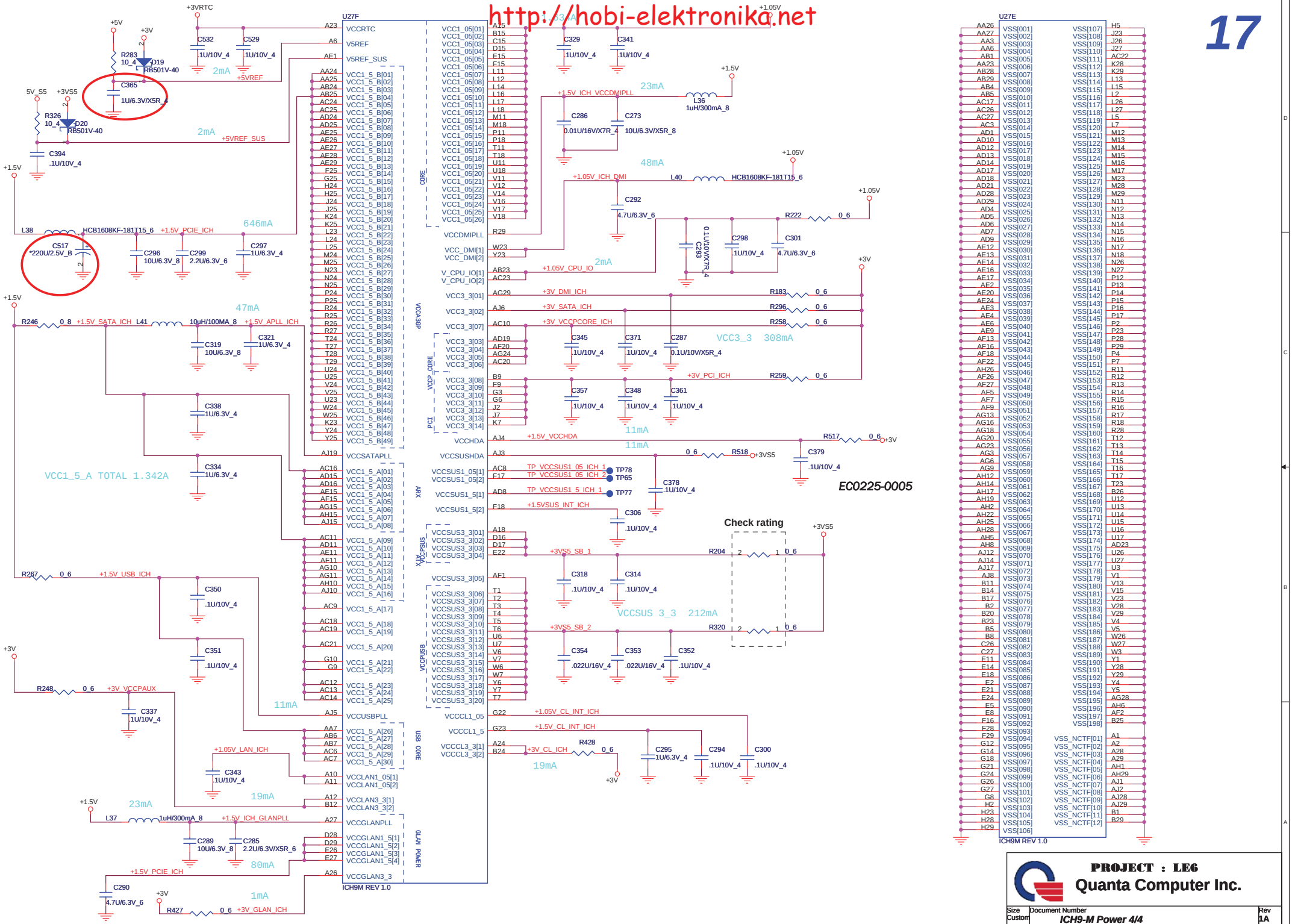
EB1213-0004

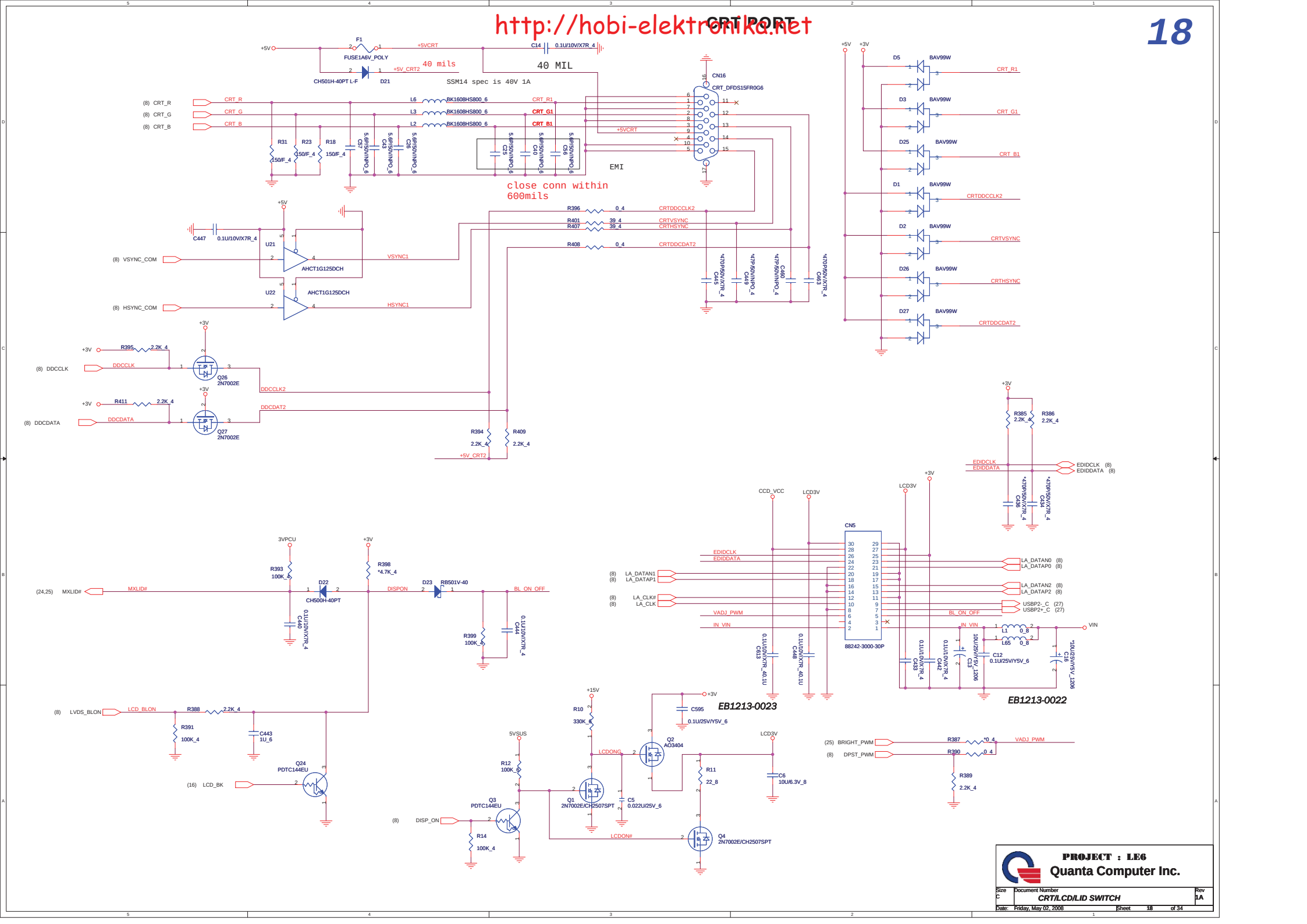
PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M GPIO 3/4	1A

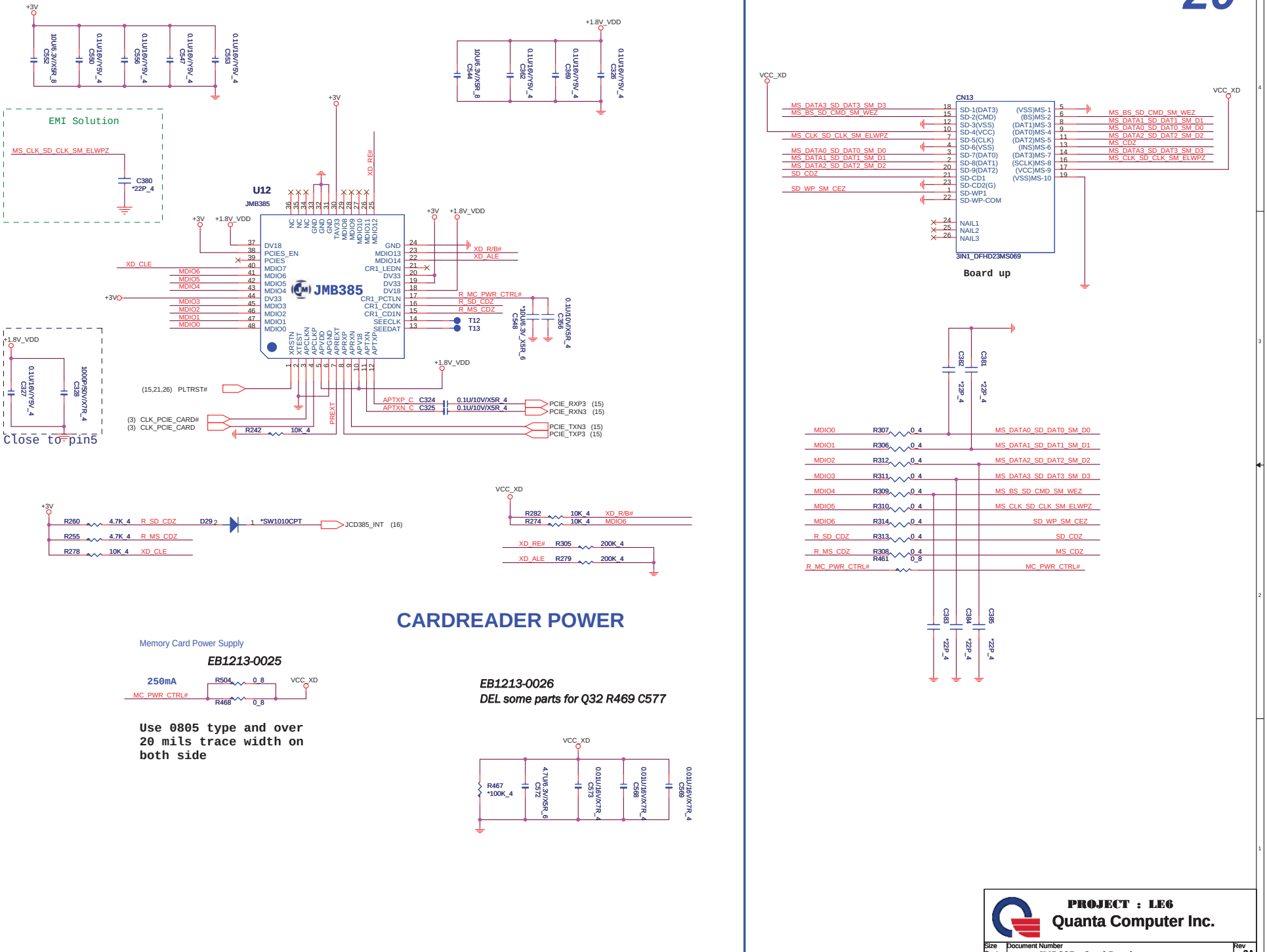
Date: Friday, May 02, 2008 Sheet 16 of 34





PROJECT : LE6			
Quanta Computer Inc.			
Size: C	Document Number: CRT/LCD/LID SWITCH		Rev: 1A
Date: Friday, May 02, 2008	Sheet 18 of 34		

BLANK PAGE FOR PAGE NUMBER SAME AS DISCRETE



CARDREADER POWER

Memory Card Power Supply

EB1213-0025

250mA

R504 0_8 VCC_XD

MC_PWR_CTRL#

R468 0_8

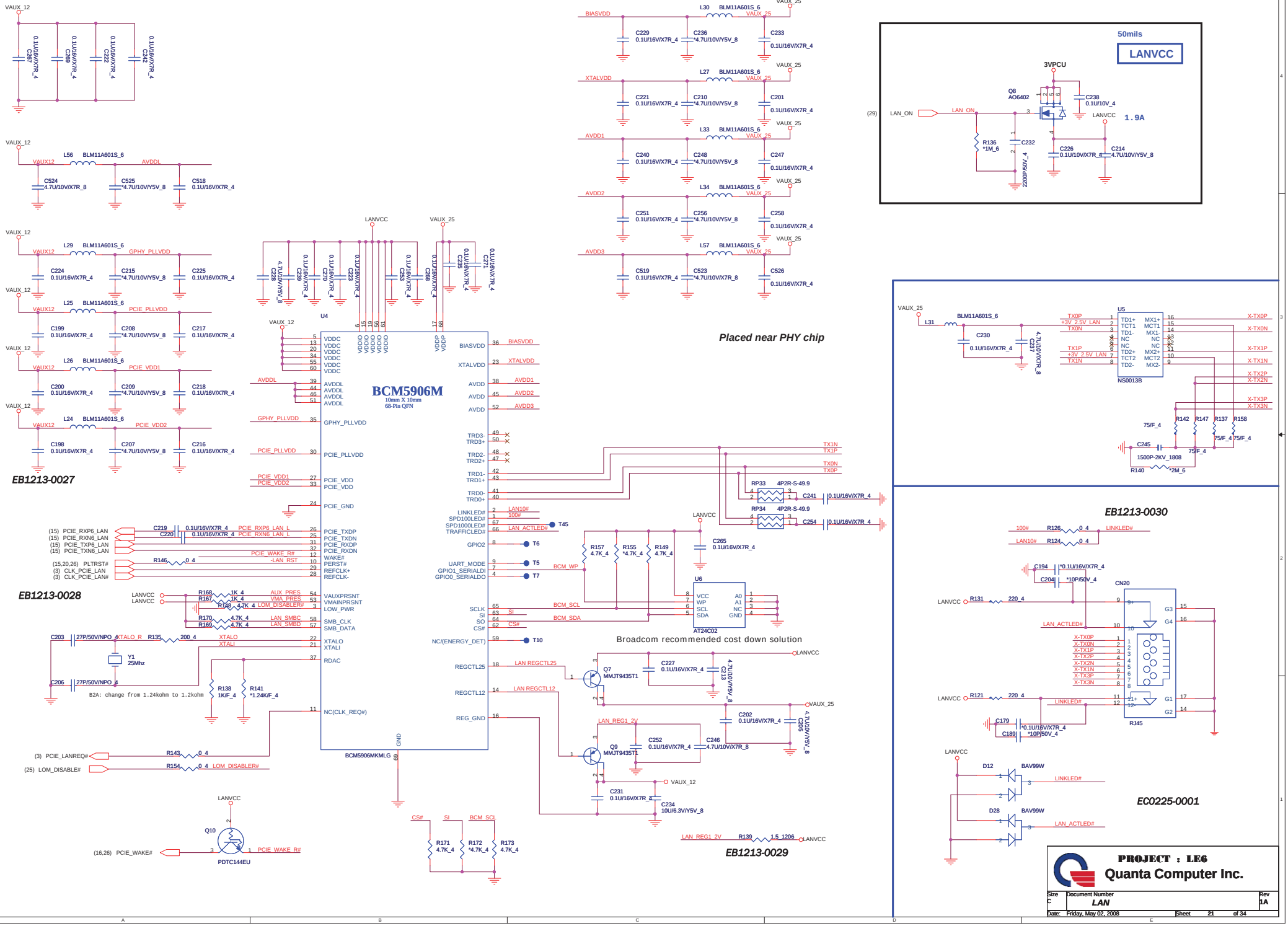
Use 0805 type and over 20 mils trace width on both side

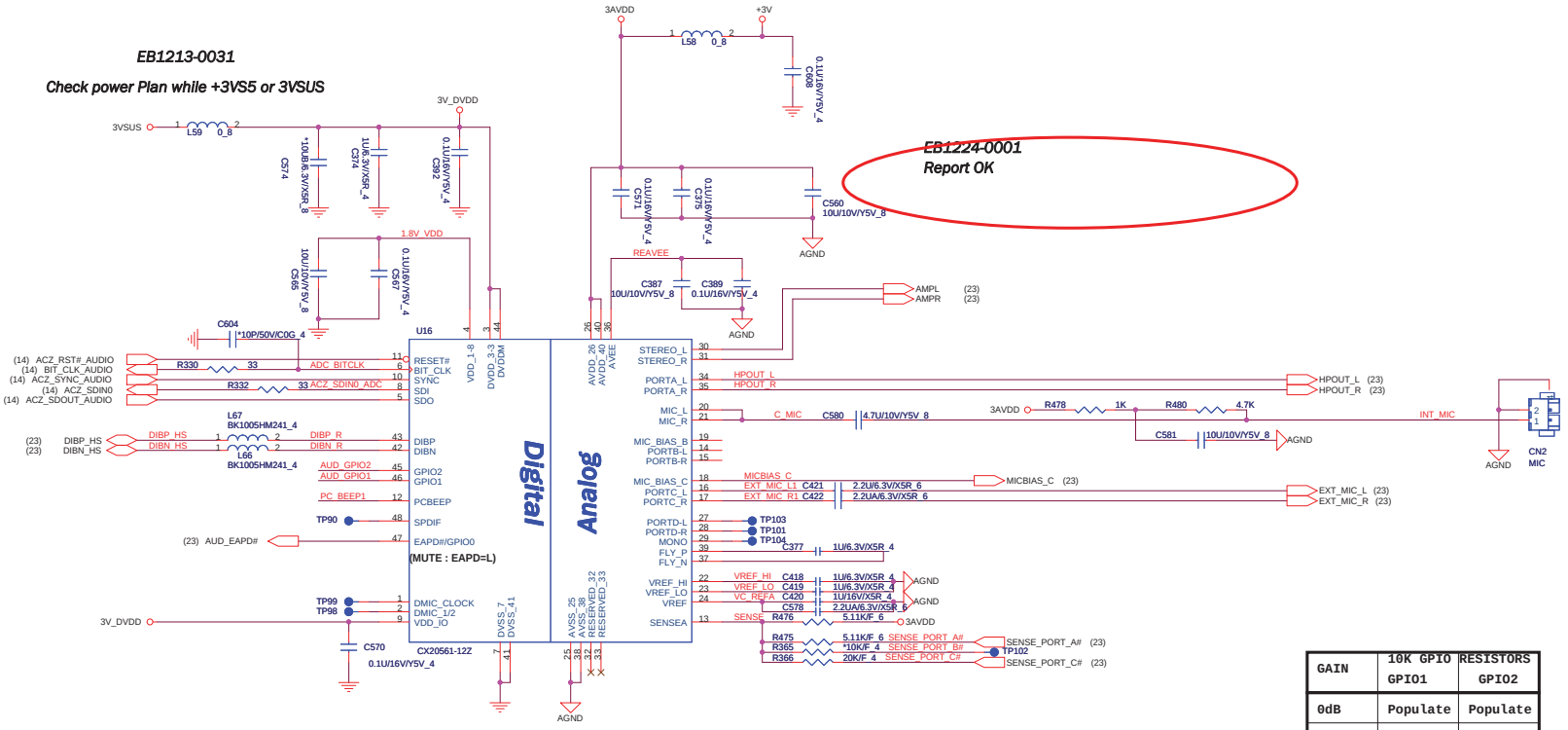
EB1213-0026

DEL some parts for Q32 R469 C577

R467 *100K_4

PROJECT :	LE6
Quanta Computer Inc.	
Size: Custom	Document Number: JMB385 - Card Reader
Rev: 2A	
Date: Tuesday, April 29, 2008	Sheet 20 of 34

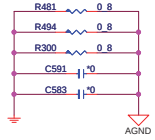




GAIN	10K GPIO GPIO1	RESISTORS GPIO2
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-16dB	Omit	Populate

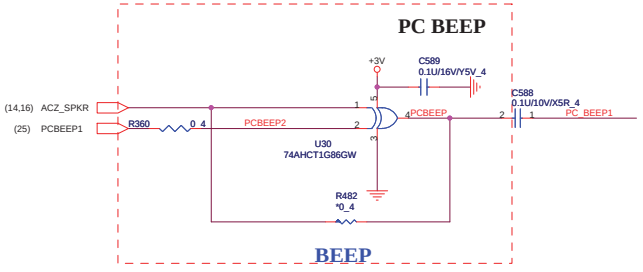
STEREO	INTERNAL SPEAKERS
PORT-A	EXTERNAL HEAD-PHONE
MIC	INTERNAL MIC
PORT-B	EXTERNAL MIC

FOR EMI SOLUTION



Default gain is -6dB without populating the 10K ohm pull down resistors going to GPIO1 and GPIO2

LE6B:Add R360 and change U30 to OR gate base on customer request

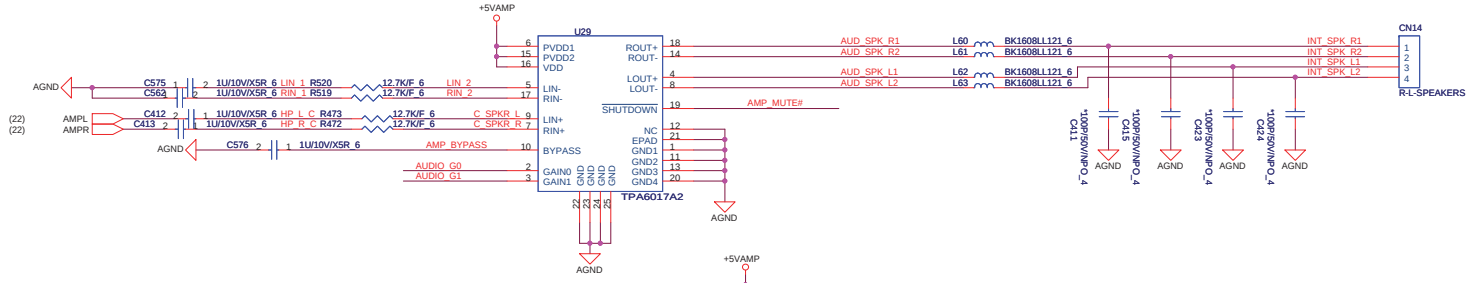


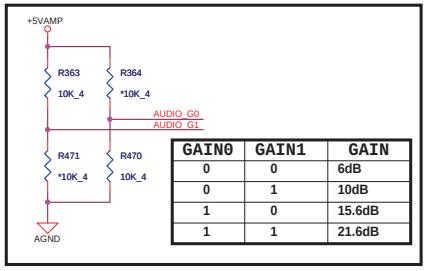
PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
C	AUDIO CODEC(CX20561-12Z)	1A

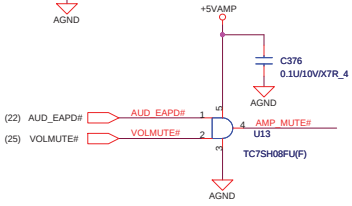
Date: Friday, May 02, 2008 Sheet 22 of 34

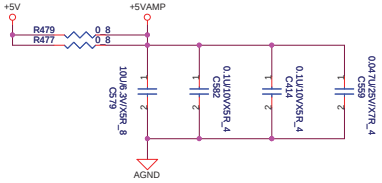
INTERNAL SPEAKER AMPLIFIER



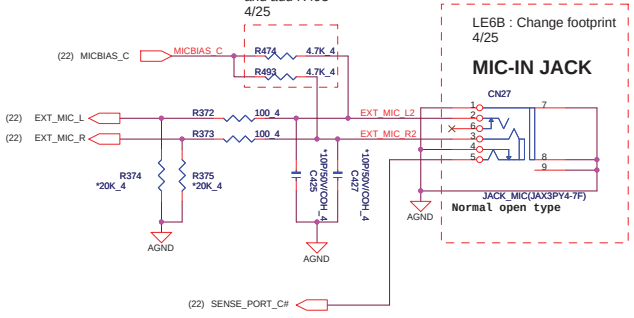


GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB





LE6B : Change connrction of MICBIAS_C and add R493 4/25

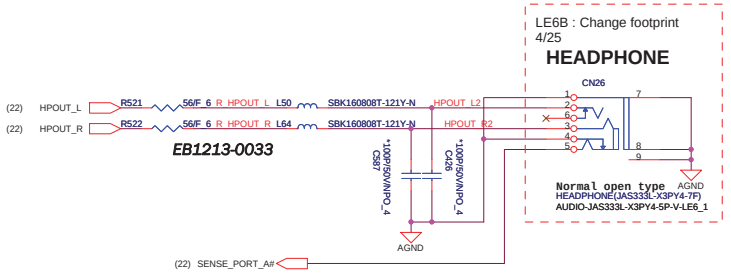


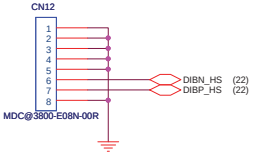
LE6B : Change footprint 4/25

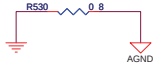
MIC-IN JACK

LE6B : Change footprint 4/25

HEADPHONE





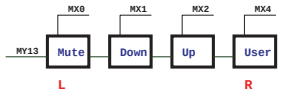


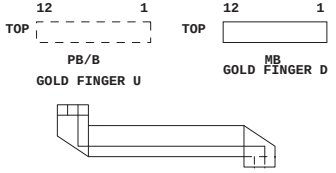
Modem connector

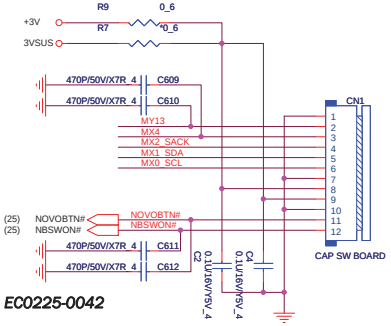
PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
C	TPA6017 & JACKS & MDC	1A

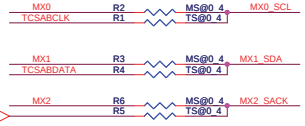
Date: Friday, May 02, 2008 Sheet 23 of 34





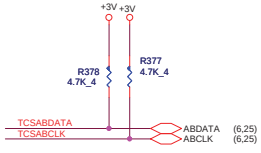


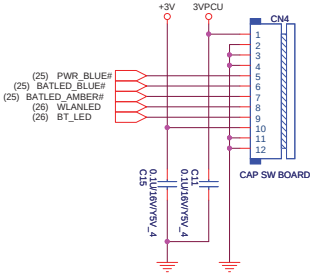
EC0225-0042

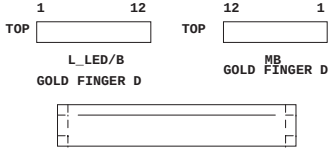


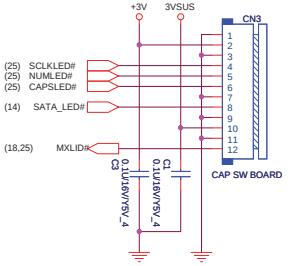
check EC and Vendor for CTS

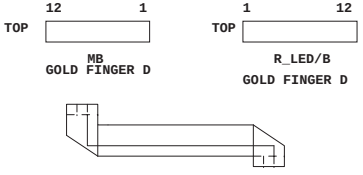
EB1213-0022



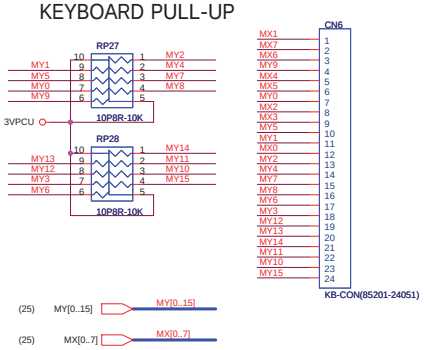




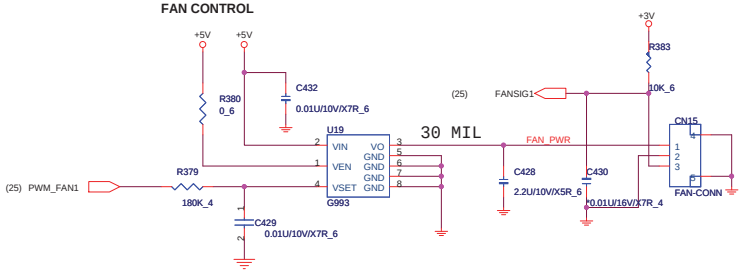


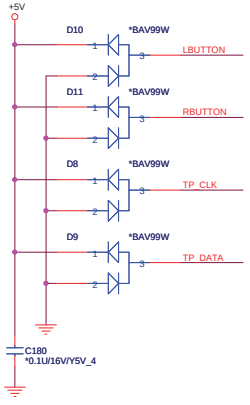


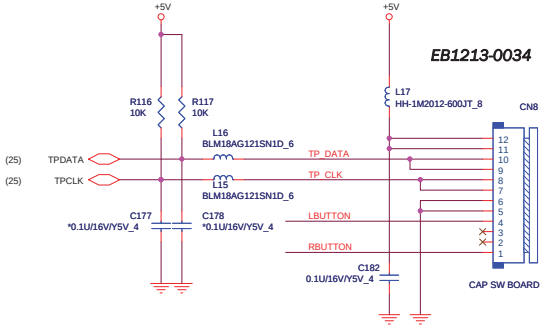
KEYBOARD PULL-UP

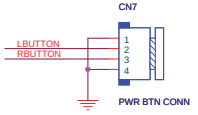


FAN CONTROL









PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
C	KEYBOARD/FAN	1A
Date: Tuesday, April 29, 2008	Sheet 24 of 34	

IT8512/IT8502

(For PLL Power)

POWER SWITCH

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

R3444	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

16Mbit (2M Byte), SPI

ST_SST25VF008B

Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

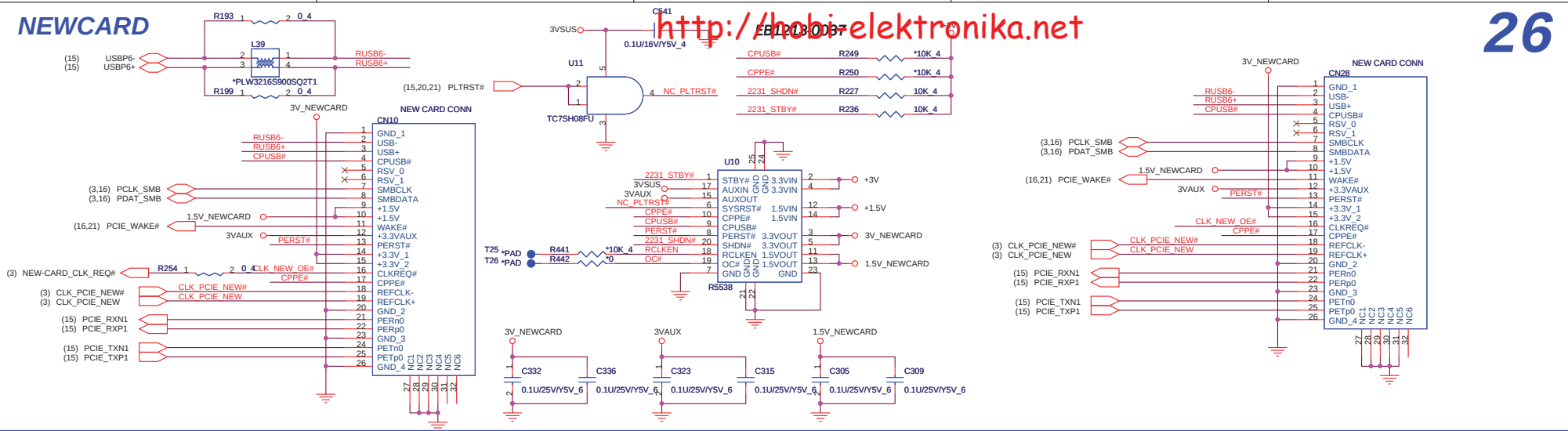
EB1213-0035

EB1213-0036

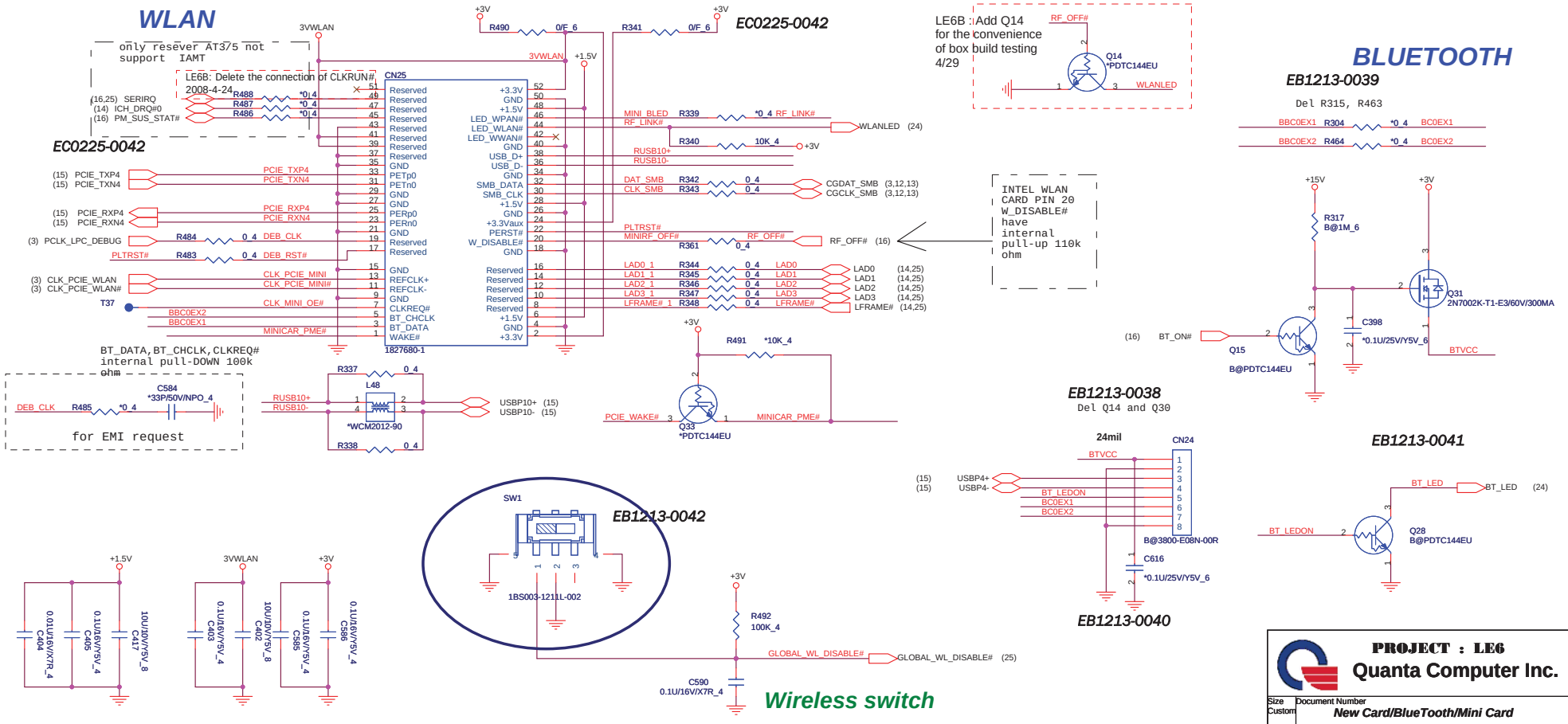
EC0225-0042

PROJECT :	LE6
Quanta Computer Inc.	
Size: Custom	Document Number: EC IT8502
Rev: 1A	
Date: Tuesday, April 29, 2008	Sheet 25 of 34

NEWCARD



Mini PCI-E Card 1 WLAN



BLUETOOTH

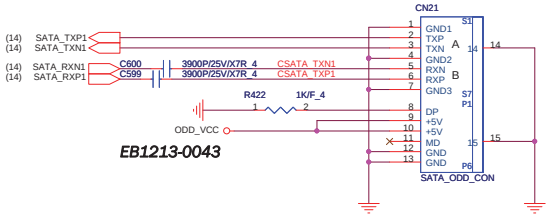
Wireless switch

PROJECT : LE6

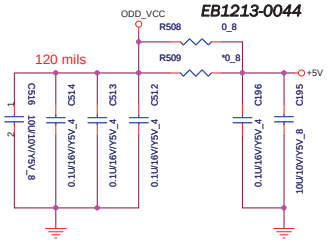
Quanta Computer Inc.

Size	Document Number	Rev
Custom	New Card/BlueTooth/Mini Card	1A
Date: Friday, May 02, 2008	Sheet 26 of 34	

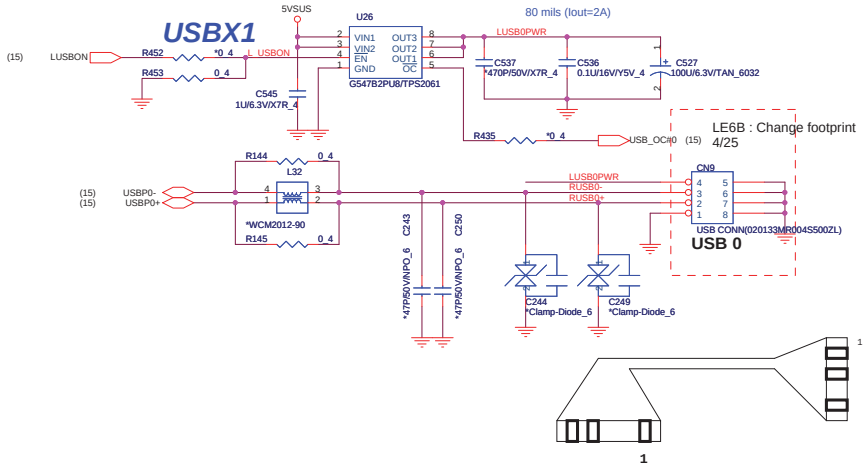
SATA CD-ROM



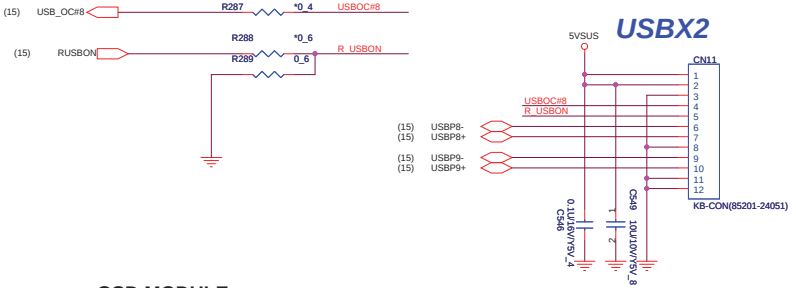
0 ohm szie from 0603 to 0805



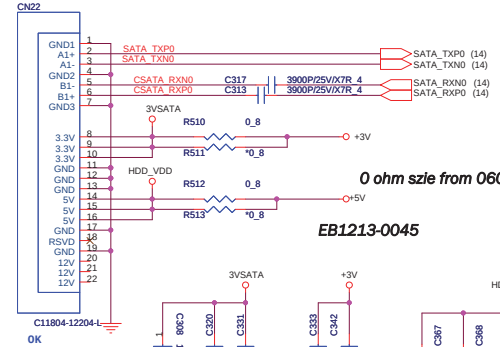
USBX1



USBX2

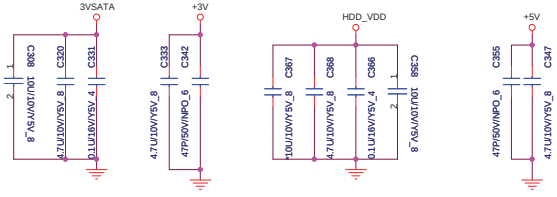


SATA_1 CONNECTOR

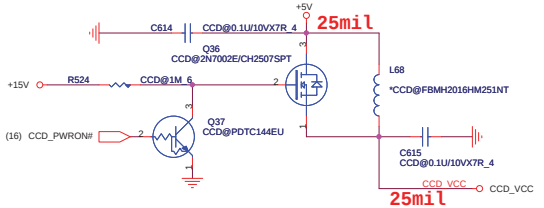


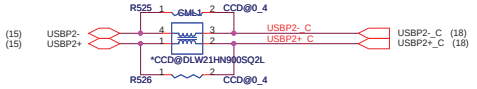
0 ohm szie from 0603 to 0805

EB1213-0045



CCD MODULE





CCD_PWRON#	High	Low
	Disable	Enable

PROJECT : LE6		
Quanta Computer Inc.		
Size: C	Document Number: SATA HDD/ODD USB*1	Rev: 1A
Date: Friday, May 02, 2008	Sheet 27 of 34	

HOLE7
H-C197D140P2

HOLE6
H-C197D140P2

HOLE4
H-C236D162P2

HOLE8
H-SPE8D106P2-8

HOLE16
H-SPED106P2-8

HOLE19
H-TSBC276D106P2-4

AGND

TOP FAN

HOLE9
H-C197D140P2

HOLE10
H-C197D140P2

HOLE20
H-C110D88P2

LE6B

HOLE21
H-C88D88N

CPU

EB1221-0001

HOLE1
H-SPE1D106P2-8

HOLE2
H-SPE2D106P2-8

HOLE12
H-C315D315N

HOLE11
H-C197D118P2

EB1213-0019

R299 *0_4

R349 *0_4

SP1

short2

AGND

HOLE13
H-TC236BC197D157P2

HOLE14
H-TC236BC197D157P2

MINI-PCIe

HOLE18
H-C276D106P2-6

HOLE17
H-C276D106P2-6

USB

EB1224-0001

RSPKR

RSPKL

BOT NB

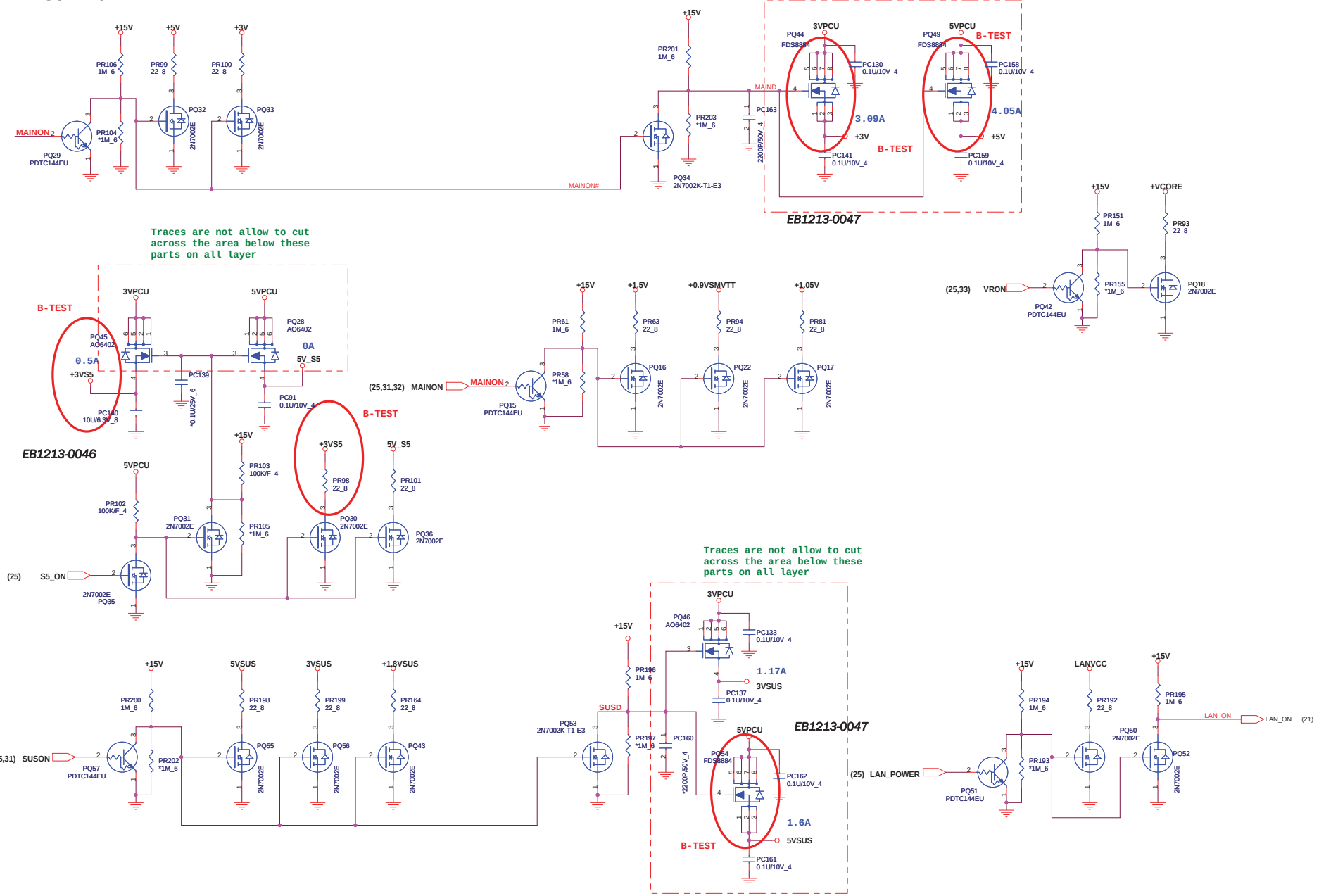
PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	*EMI PAD/SCREW/DEBUG PORT*	1A

Date: Friday, May 02, 2008 Sheet 28 of 34

DISCHARGE

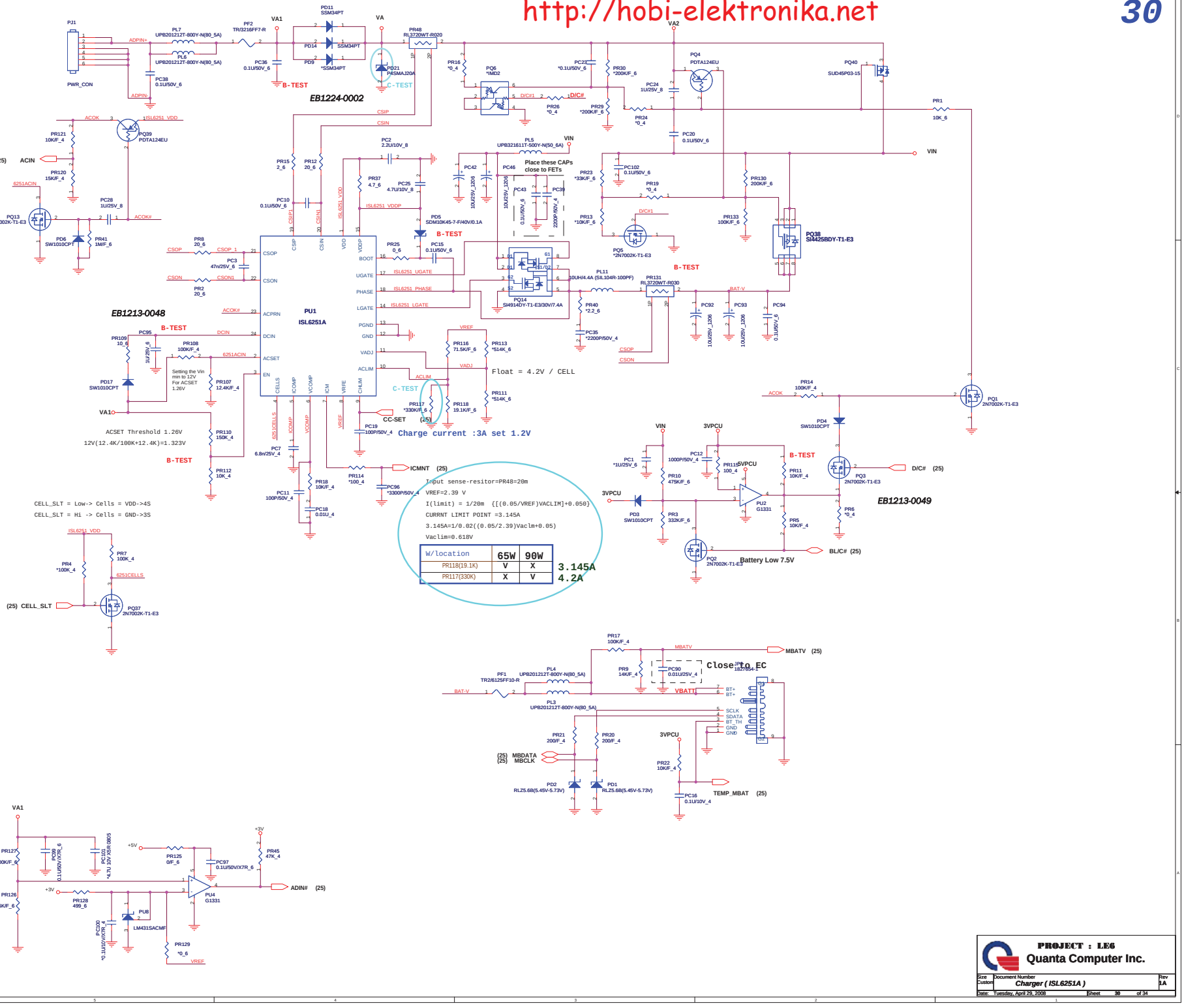


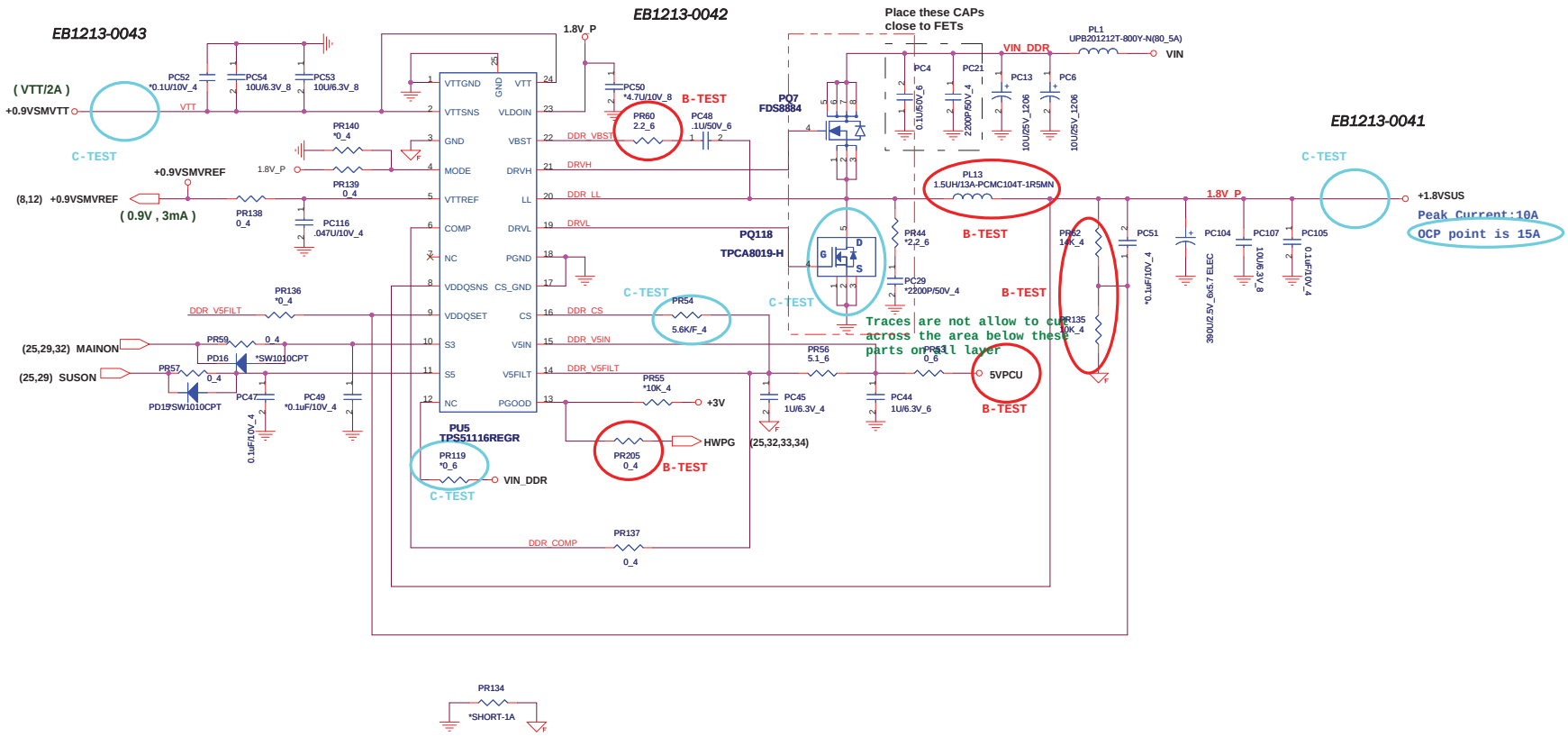
PROJECT : LE6

Quanta Computer Inc.

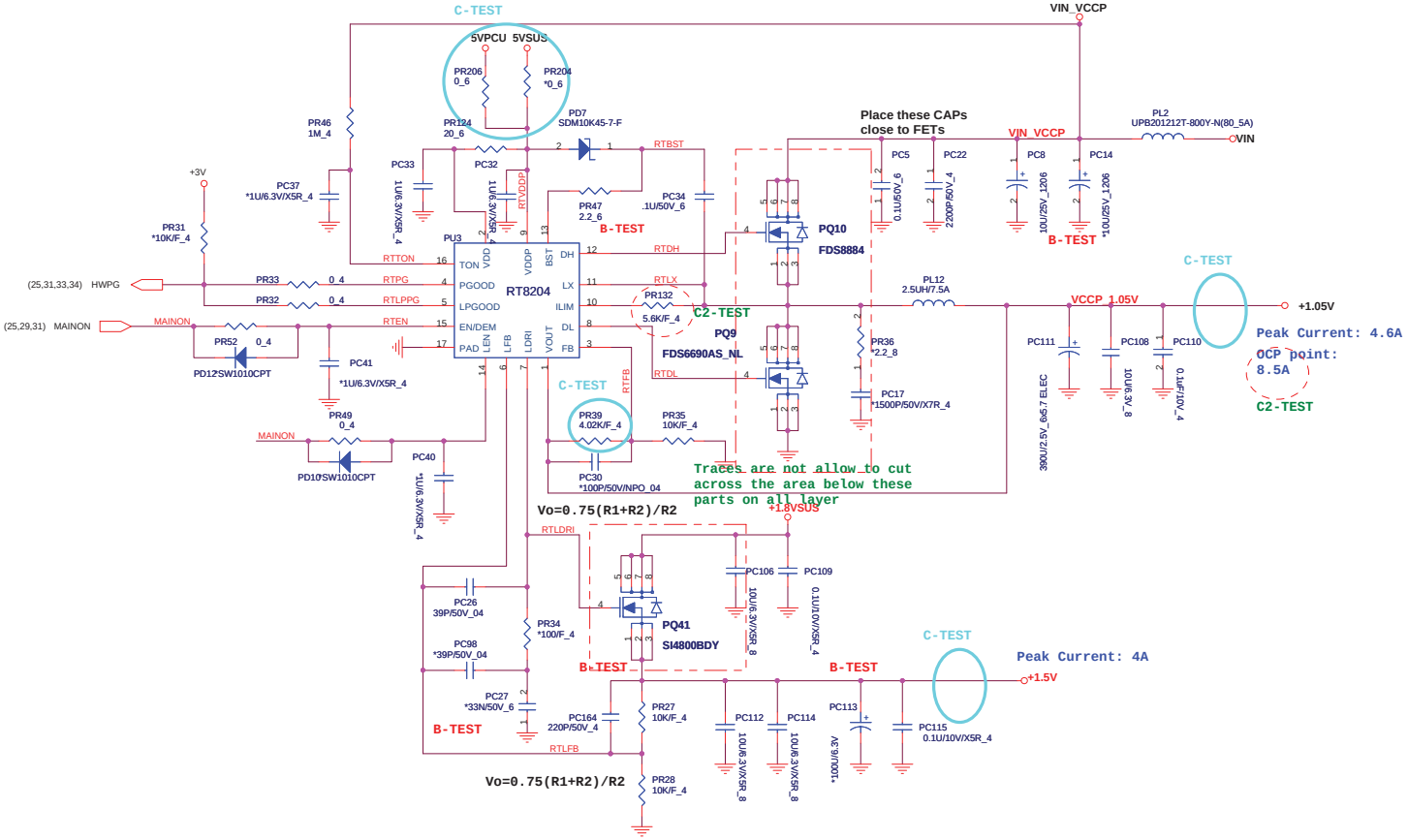
Size	Document Number	Rev
Custom	Discharge	1A

Date: Friday, May 02, 2008 Sheet 29 of 34





PROJECT : LE6			
Quanta Computer Inc.			
Size: Custom	Document Number: DDR (TPS51116PEGR)		Rev: 1A
Date: Friday, May 02, 2008	Sheet 31 of 34		

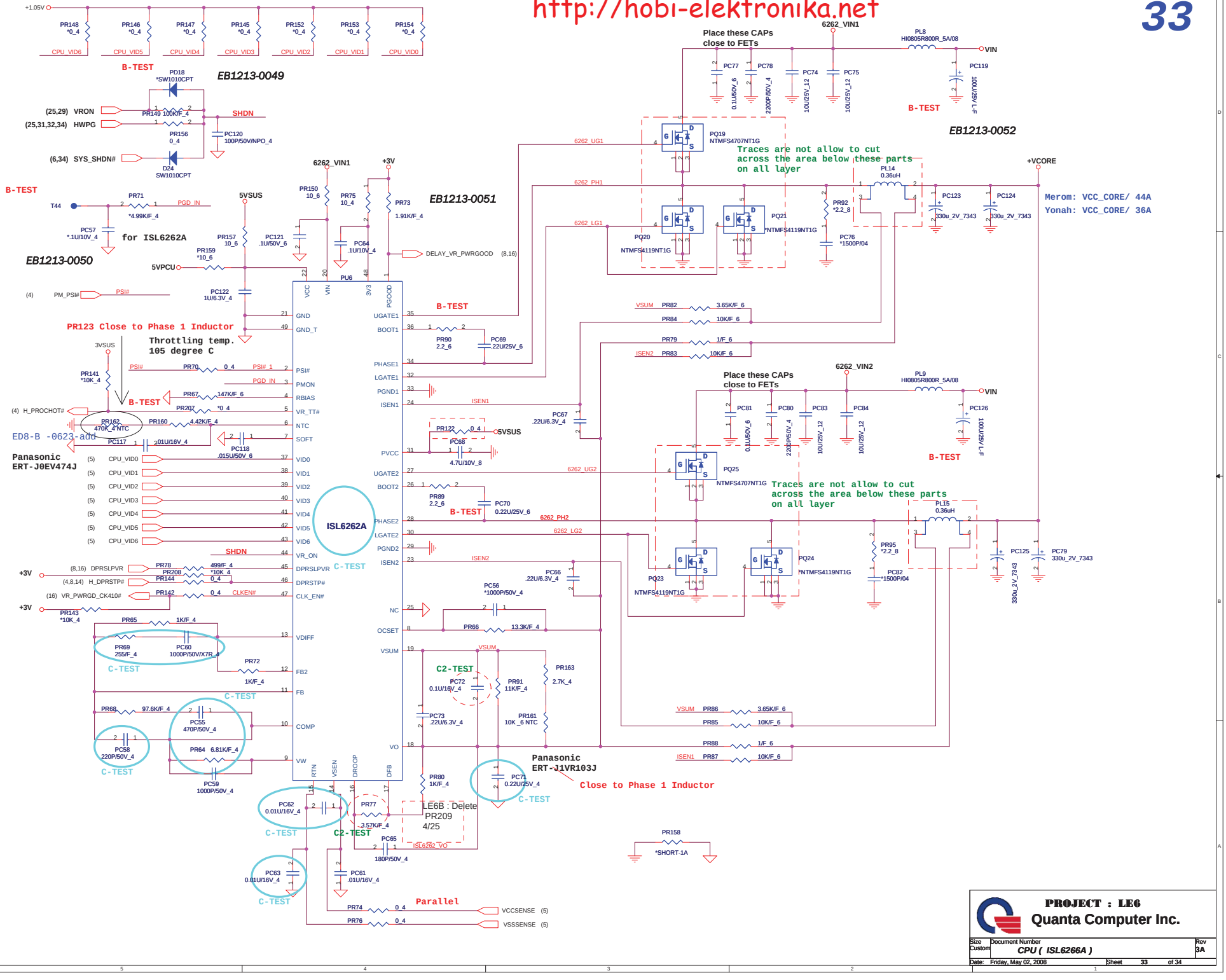


PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.05V/1.5V/1.25V (ISL6228)	3A

Date: Friday, May 02, 2008 Sheet 32 of 34



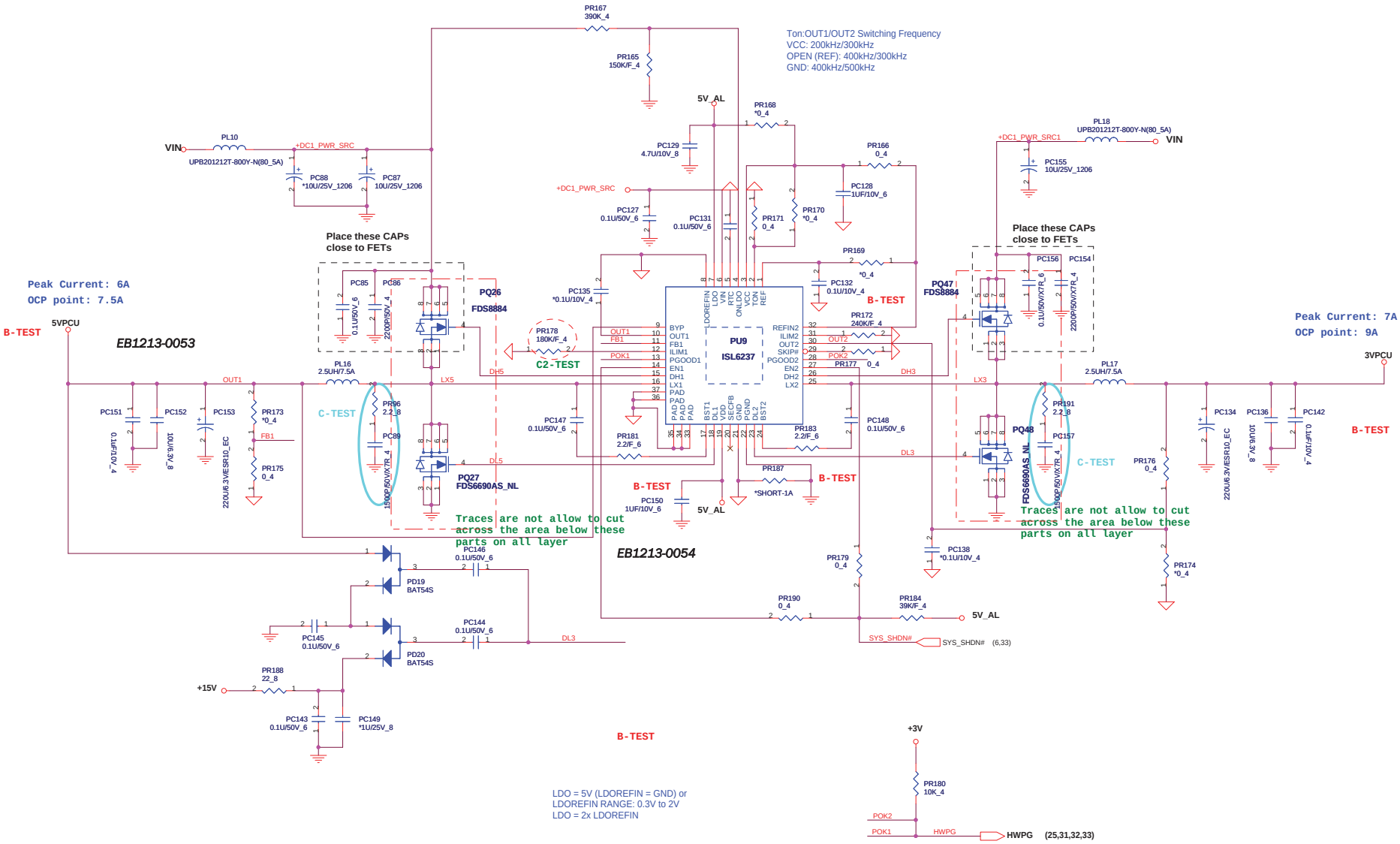
PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU (ISL6266A)	3A

Date: Friday, May 02, 2008 Sheet 33 of 34

DC/DC 3VPCU/5VPCU/+15V



PROJECT : LE6			
Quanta Computer Inc.			
Size: Custom	Document Number: 3V/5V (ISL6237)		Rev: 3A
Date: Friday, May 02, 2008	Sheet 34 of 34		