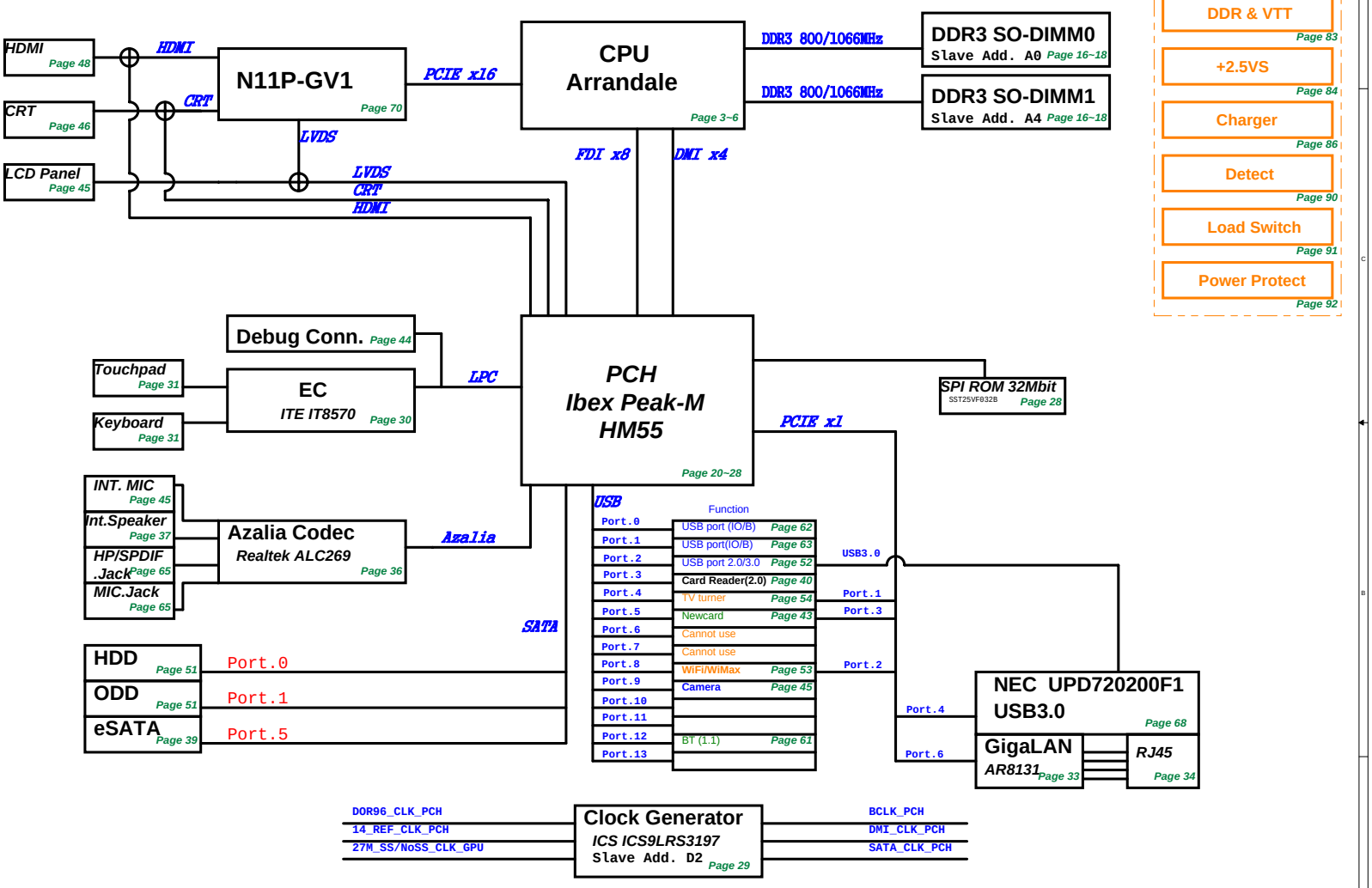
N61Jv SCHEMATIC Revision 2.0

SYSTEM PAGE REF.

N61Jv BLOCK DIAGRAM



Power

- VCORE — Page 80
- System — Page 81
- 1.5VS & 1.05VS — Page 82
- DDR & VTT — Page 83
- +2.5VS — Page 84
- Charger — Page 86
- Detect — Page 90
- Load Switch — Page 91
- Power Protect — Page 92

PWM Fan	Reset Circuit	Discharge Circuit	DC & BATT. Conn.	Skew Holes
Page 50	Page 32	Page 57	Page 60	Page 65

ASUSTeK COMPUTER INC. NB4

Title : Block Diagram

Engineer: yun-feng_yan

Size	Project Name	Rev
C	N61Jv	1.0

Date: Thursday, December 17, 2009 Sheet 1 of 95

PCH_IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	NC_TP	-	+3VS
GPIO 01	GPO	NC_TP	INT TBD	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	EXT PU	+5VS
GPIO 06	GPO	NC_TP	INT TBD	+3VS
GPIO 07	GPO	NC_TP	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	NC_PU	EXT PU	+3VSUS
GPIO 10	Native	NC_PU	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	NC_TP	-	+3VSUS
GPIO 13	GPO	NC_TP	-	+3VSUS
GPIO 14	GPO	NC_PU	EXT PU	+3VSUS
GPIO 15	GPO	BT_LED	INT PD	+3VSUS
GPIO 16	GPI	DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 17	GPI	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	GPI	CLKREQ1#_TV	EXT PD	+3VS
GPIO 19	GPI	SATA1GP	EXT PU	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PD	+3VS
GPIO 21	GPI	SATA0GP	EXT PU	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	Native	NC_TP	INT PU	+3VS
GPIO 24	GPO	NC_TP	-	+3VSUS
GPIO 25	GPI	CLKREQ3#_NEWCARD	EXT PD	+3VSUS
GPIO 26	GPI	CLK_REQ4#_CB	EXT PD	+3VSUS
GPIO 27	GPO	NC_TP	INT WEAK PU	+3VSUS
GPIO 28	GPO	WLAN_ON#	EXT PD	+3VSUS
GPIO 29	Native	NC_TP	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	GPO	ME_SusPwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	GPIO	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPI	HDA_DOCK_EN#	-	+3VS
GPIO 34	Native	NC_TP	-	+3VS
GPIO 35	GPO	SATA_CLK_REQ#	EXT PD	+3VS
GPIO 36	GPI	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSNT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	NC_PU	EXT PU	+3VSUS
GPIO 41	Native	NC_PU	EXT PU	+3VSUS
GPIO 42	Native	NC_PU	EXT PU	+3VSUS
GPIO 43	Native	NC_PU	EXT PU	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU	+3VSUS
GPIO 45	Native	NC_TP	EXT PU	+3VSUS
GPIO 46	Native	NC_TP	EXT PU	+3VSUS
GPIO 47	GPI	CLKREQ_PEG#	EXT PU	+3VSUS
GPIO 48	GPO	NC_TP	-	+3VS
GPIO 49	GPIO	PCH_TEMP_ALERT#	EXT PU	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	Native	DGPU_SELECT#_R	EXT PU	+5VS
GPIO 53	GPO	DGPU_PWM_SELECT#	INT PU	+3VS
GPIO 54	Native	PCI_REQ3#	EXT PU	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	GPI	CLKREQ_GLAN#	EXT PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	GPIO	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	NC_PU	EXT PU	+3VSUS
GPIO 60	Native	SML0ALERT#	EXT PU	+3VSUS
GPIO 61	Native	NC_TP	-	+3VSUS
GPIO 62	Native	NC_TP	-	+3VSUS
GPIO 63	Native	NC_TP	-	+3VSUS
GPIO 64	Native	NC_TP	INT TBD	+3VS
GPIO 65	Native	NC_TP	INT TBD	+3VS
GPIO 66	Native	NC_TP	INT TBD	+3VS
GPIO 67	Native	EDID_SELECT#	INT TBD	+3VS
GPIO 72	Native	PM_BATLOW#	EXT PU	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU	+3VSUS
GPIO 74	Native	SML1ALERT#	EXT PU	+3VSUS
GPIO 75	GPIO	SML1_DATA	EXT PU	+3VSUS

EC IT8541

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2		-
GPA3		-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN0_PWM
GPA6		-
GPA7		-
GPB0	O	BATSEL_0
GPB1	O	BATSEL_1
GPB2		ME_AC_PRESENT_EC
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RCIN#
GPB7	O	PM_RSMRST#
GPC0		-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7		-
GPE0	O	VSUS_ON
GPE1	O	EGAD (IT8301 Address/Data connect)
GPE2	O	EGCS (IT8301 Cycle Start connect)
GPE3	O	EGCLK (IT8301 Clock connect)
GPE4	I	PWR_SW#
GPE5		-
GPE6	I	LID_SW#
GPE7		-
GPF0	O	-
GPF1		-
GPF2	I	EXP_GATE#
GPF3		-
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7	O	PCH_SPI_OV
GPG0	I	ME_SUSPWRDNACK_EC
GPG1	I	PM_SUSB#
GPG2		-
GPG6		-
GPH0	IO	PM_CLKRUN#
GPH1	O	GFX_VR_ON
GPH2	O	CHG_EN
GPH3	O	SUSC_EC#
GPH4	O	SUSB_EC#
GPH5	O	NUM_LED#
GPH6	O	CAP_LED#
GPI0		-
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ALERT#
GPI5	I	ALS_AD
GPI6	I	CAP_ACK_A#
GPI7	I	CAP_ACK_B#
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISET_EC
GPJ4	O	TP_LED
GPJ5		-

EC IT8301 R1.3 removed

EC GPIO	Use As	Signal Name
GPIO00	I	ME_PM_SLP_M#
GPIO01	I	ME_SusPwrDnAck
GPIO2		-
GPIO3		-
GPIO4	I	ME_+VM_PWRGD
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	O	ME_AC_PRESENT
GPIO7		-
GPIO8		-
GPIO9		-
GPIO10		-
GPIO11		-
GPIO12	O	ME_PWROK
GPIO13		-
GPIO14	O	ME_SLP_M_EC#
GPIO15		-
GPIO16		-
GPIO17		-
GPIO18		-
GPIO19		-
GPIO20		-
GPIO21		-
GPIO22		-
GPIO23		-
GPIO24		-
GPIO25		-
GPIO26		-
GPIO27		-
GPIO28		-
GPIO29		-
GPIO30		-
GPIO31		-
GPIO32		-
GPIO33		-
GPIO34		-
GPIO35		-
GPIO36		-
GPIO37		-

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
Clock Generator(ICS9LRS3197)	1101001x (D2)	
SO-DIMM 0	1010000x (A0)	
SO-DIMM 1	1010001x (A2)	
VID Controller(ASM8272)	0011011x (36)	
WiFi/WiMax	N/A	
EC Master (SMB1)		
SM-Bus Device	**SM-Bus Address**	
CPU Thermal Sensor(G781)	1001100x (9A)	
VGA Thermal IC(G781-1)	1001101x (9E)	

Device Identification

	CPU Thermal Sensor P/N:	component name
1st	06G023048011	G781F
S		
S		
S		

	Clock Gen P/N:	component name
1st	06G011604010	ICS9LRS3197
S		
S		

	VGA Thermal Sensor	component name
1st	06G023048020	G781-1
S		
S		

PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	Card reader
PCIE 6	GLAN
PCIE 7	
PCIE 8	

SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	ESATA

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	Minicard TV Tuner
USB 5	NewCard
USB 6	
USB 7	
USB 8	WLAN
USB 9	CMOS Camera
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	Finger Printer

ASUSTeK COMPUTER INC. NB4

Title : System Setting

Engineer: yun-feng_yan

Size	Project Name	Rev
C	N61Jv	1.0

Date: Wednesday, November 11, 2009 Sheet 2 of 95

Main Board

JTAG MAPPING

XDP_TDI_R — SL0328 0402 — XDP_TDO_M — R0350 0Ohm — XDP_TDI 7 / XDP_TDO 7

R0351 0Ohm

XDP_TDI_M — R0352 0Ohm — XDP_TDO_R — SL0327 0402

FDI disable: (For discrete graphic)

1. NC:
   FDI_TX#[0:7],FDI_TX[0:7],FDI_RX#[0:7],FDI_RX[0:7]
   VCC_AXGSENSE,VSS_AXGSENSE
2. Pull-down to GND via 1K ± 5% resistor:
   FDI_FSYNC[0:1],FDI_LSYNC[0:1],FDI_INT,GFX_IMON
   ~15mW power saving.(DG R0.8 P.70)
3. Connected to GND:
   VCCAXG,
4. Can be connected to GND directly:
   DPLL_REF_CLK,DPLL_REF_CLK#
5. Connect to +V1.05S rail:
   VCCFDIPLL

FDI_FSYNC0 — 1KOhm — R0364
FDI_FSYNC1 — 1KOhm — R0361
FDI_LSYNC0 — 1KOhm — R0365
FDI_LSYNC1 — 1KOhm — R0362
FDI_INT — 1KOhm — R0363

DG R1.1 P.83:

•FDI_FSYNC[0],FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1] can be ganged together with one resistor.
•On the other hand,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on PCH side can be left as no connect without any power or functional impact.

U0301A

DMI_TXN[3:0] — DMI_RX#[3:0]
DMI_TXP[3:0] — DMI_RX[3:0]
DMI_RXN[3:0] — DMI_TX#[3:0]
DMI_RXP[3:0] — DMI_TX[3:0]

FDI_TXN[7:0] — FDI_TX#[0:7]
FDI_TXP[7:0] — FDI_TX[0:7]
FDI_FSYNC0 / FDI_FSYNC1 — FDI_FSYNC[0:1]
FDI_INT
FDI_LSYNC0 / FDI_LSYNC1 — FDI_LSYNC[0:1]

For Intel GFX display

DMI / FDI / PCI EXPRESS - GRAPHICS

PEG_ICOMPI — R0301 1% 49.9Ohm
PEG_ICOMPO — R0302 1% 750hm
PEG_RCOMP

PEG_RX#[15:0] — PCIENB_RXN[15:0] 70
PEG_RX[15:0] — PCIENB_RXP[15:0] 70

PEG_TX#[15:0] — C0301–C0316 0.1UF/16V — PCIEG_RXN[15:0] 70
PEG_TX[15:0] — C0317–C0332 0.1UF/16V — PCIEG_RXP[15:0] 70

SOCKET989

12G011909890

R0370,R0371,R0372 near U0301

SKTOCC#:pulled to ground on processor.
may use to determine if CPU is present

U0301B

MISC CLOCKS

COMP3 — R0303 20Ohm 1% — H_COMP3
COMP2 — R0304 20Ohm 1% — H_COMP2
COMP1 — R0305 49.9Ohm 1% — H_COMP1
COMP0 — R0306 49.9Ohm 1% — H_COMP0
SKTOCC# — T0301 TP_SKTOCC#
CATERR# — H_CATERR#
PECI — H_PECI
PROCHOT# — H_PROCHOT_S# — R0310 0Ohm — H_PROCHOT_S#_R
THERMTRIP# — H_THRMTRIP# — R0311 0Ohm — H_THRMTRIP#_R
RESET_OBS# — H_CPURST#
PM_SYNC — PM_SYNC# — SL0329 — PM_SYNC#_R
VCCPWRGOOD_1 — SL0330 — T305 — VCCPWRGOOD_1_R
VCCPWRGOOD_0 — SL0331 — T304 — VCCPWRGOOD_0_R
SM_DRAMPWROK — SL0332 — VDDPWRGOOD_R
VTTPWRGOOD — T303
TAPPWRGOOD — H_PWRGD_XDP
RSTIN# — T306 — PLT_RST#_R

THERMAL

+VTT_CPU — R0317 0Ohm — THRO_CPU
+VTT_CPD — 25 — H_PECI
R0322 68OHM
R0310 don't remove
30,90 PWRLIMIT# — D0301 — RB751V-40 — H_PROCHOT_S#
Q0301 2N7002 — 30 THRO_CPU

For EC request, to read PECI via EC.
Connection: R0317.2-->Q0301.1-->U3001.118

DDR3 MISC

SM_DRAMRST# — F6 — M_DRAMRST# 16,17
SM_RCOMP[0] — AL1 SM_RCOMP0 — R0331 24.9Ohm 1%
SM_RCOMP[1] — AM1 SM_RCOMP1 — R0332 24.9Ohm 1%
SM_RCOMP[2] — AN1 SM_RCOMP2 — R0333 130Ohm 1%
PM_EXT_TS#[0] — AN15 — PM_EXTTS#1 — PM_EXTTS#0 16,17
PM_EXT_TS#[1] — AP15
+VTT_CPU — RN0301A 10KOHM — RN0301B 10KOHM

JTAG & BPM

PRDY# — AT28 — XDP_PRDY# 7
PREQ# — AP27 — XDP_PREQ# 7
TCK — AN28 — XDP_TCK 7
TMS — AP28 — XDP_TMS 7
TRST# — AT27 — XDP_TRST# 7
TDI — AT29 — XDP_TDI_R — T310
TDO — AR27 — XDP_TDO_R — T311
TDI_M — AR29 — XDP_TDI_M — T312
TDO_M — AP29 — XDP_TDO_M — T313
DBR# — AN25 — H_DBR#_R — R0336 0Ohm — XDP_DBRESET# 7,22
BPM#[7:0] — AJ22–AH23 — XDP_OBS0–XDP_OBS7 — XDP_OBS[7:0] 7

PWR MANAGEMENT

7,24,30,32,33,40,43,53,54,68,70 BUF_PLT_RST# — R0318 1.5KOhm 1% — R0319 750Ohm 1%

R1.0

BCLK — CLK_CPU_BCLK — SL0323 — BCLK_CPU_P_PCH 25
BCLK# — CLK_CPU_BCLK# — SL0324 — BCLK_CPU_N_PCH 25
BCLK_ITP — CLK_ITP_BCLK_R — SL0333 — CLK_ITP_BCLK 7
BCLK_ITP# — CLK_ITP_BCLK#_R — SL0334 — CLK_ITP_BCLK# 7
PEG_CLK — CLK_EXP_P — SL0325 — CLK_DMI_PCH 21
PEG_CLK# — CLK_EXP_N — SL0326 — CLK_DMI#_PCH 21
DPLL_REF_SSCLK — CLKDREF — R0329 0Ohm — CLK_DREF 21
DPLL_REF_SSCLK# — CLKDREF# — R0330 0Ohm — CLK_DREF# 21

120MHz from PCH.

DRAMPWROK: (DGU R1.52)

+1.5V — R0320 1.1KOhm 1% — VDDPWRGOOD_R — R0321 3.01KOHM 1% — GND

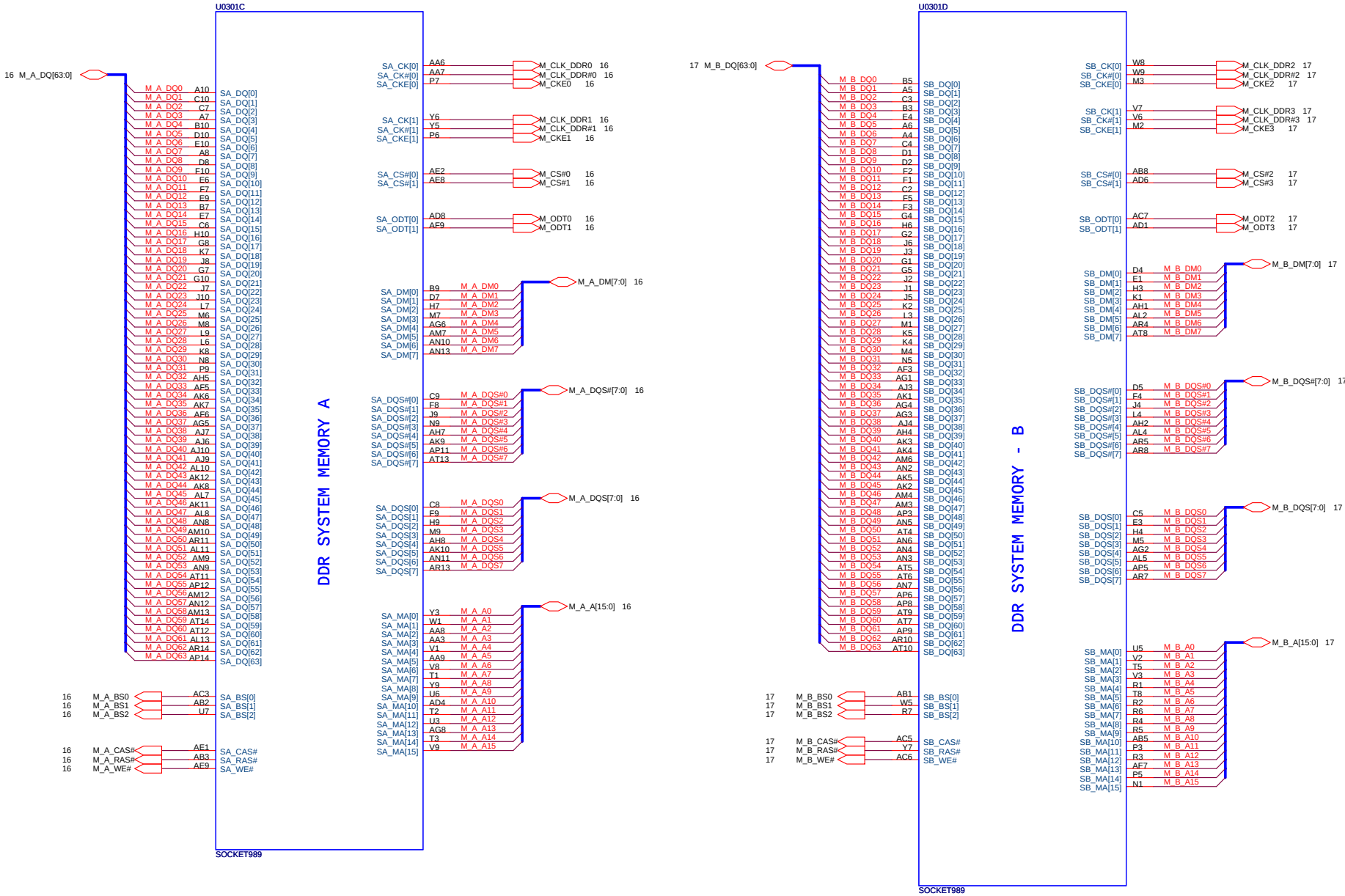
R1.3,item 1

+VTT_CPU
H_CPURST# — R0313 68OHM
XDP_TMS — R0345 51Ohm
XDP_TDI_R — R0346 51Ohm
XDP_PREQ# — R0347 51Ohm
XDP_TCLK — R0348 51Ohm
XDP_TRST# — R0354 51Ohm

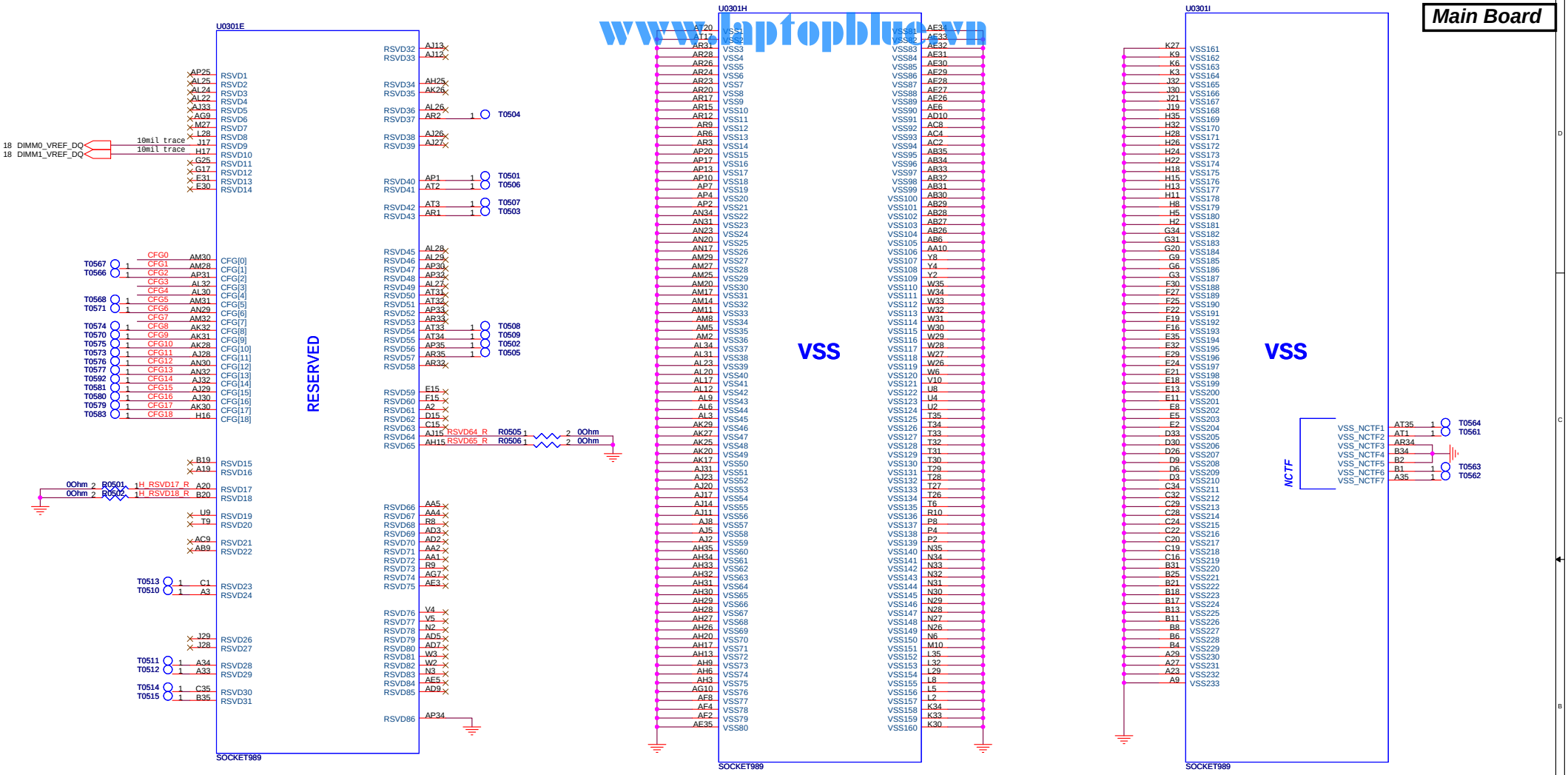
CLKDREF — R330 0Ohm
CLKDREF# — R331 0Ohm

Title :	DMI,PEG,FDI,CLK
ASUSTeK COMPUTER INC. NB1	Engineer: yun-feng_yan
Size: C	Project Name: N61Jv
Rev: 1.0	
Date: Friday, December 11, 2009	Sheet 3 of 95

Main Board



ASUSTeK COMPUTER INC. NB1	Title : CPU(2)_DDR3	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 4 of 95	



CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation (Clarksfield Only)

- 11 : 1 x 16 PEG (Default)
- 10 : 2 x 8 PEG

CFG[3]: PCIE Static Numbering Lane Reversal (Auburndale Only)

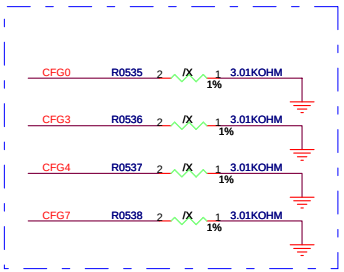
- 1 : Normal Operation (Default)
- 0 : Lane Numbers Reversed

CFG[4]: Embedded DisplayPort Detection (Auburndale Only)

- 1 : Disabled - No Physical Display Port attached to eDP
- 0 : Enabled - An external Display Port device is connected to eDP

CFG[7]: Fixed for PCI Express 2.0 jitter specifications (Clarksfield)

- only for early samples pre-ES1 : Connect to GND with 3.01K Ohm 5% resistor



* Note:
Auburndale Hardware Straps are sampled on asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.
Clarksfield Hardware Straps are sampled after RSTIN# de-assertion.

ASUSTeK COMPUTER INC. NB1

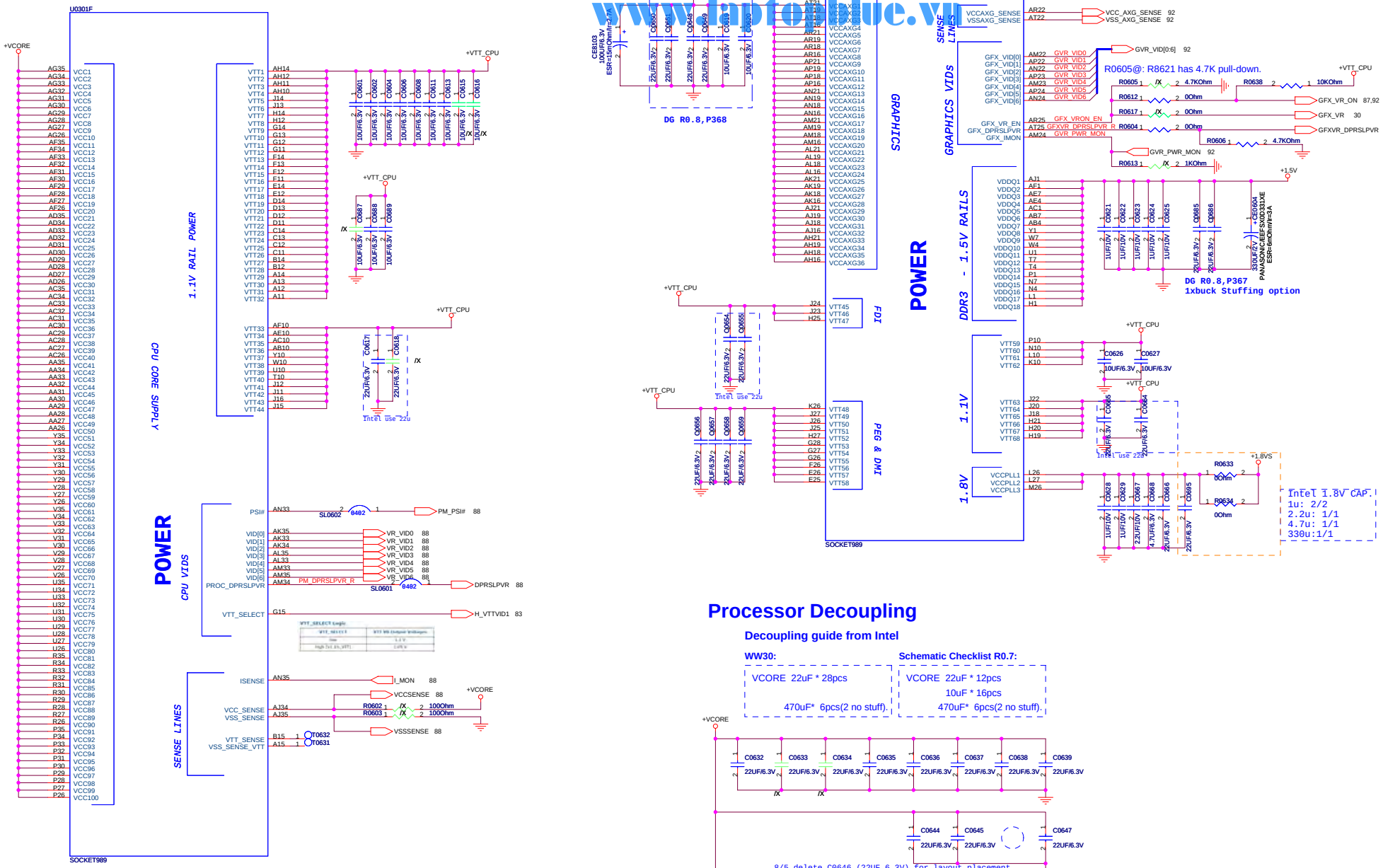
Title : CFG,RSVD,GND

Engineer: yun-feng_yan

Size	Project Name	Rev
Custom	N61Jv	1.0

Date: Friday, December 11, 2009 Sheet 5 of 95

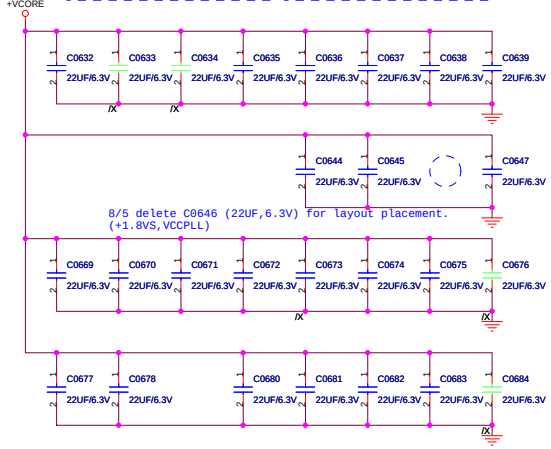
Add Jumper to measure power?



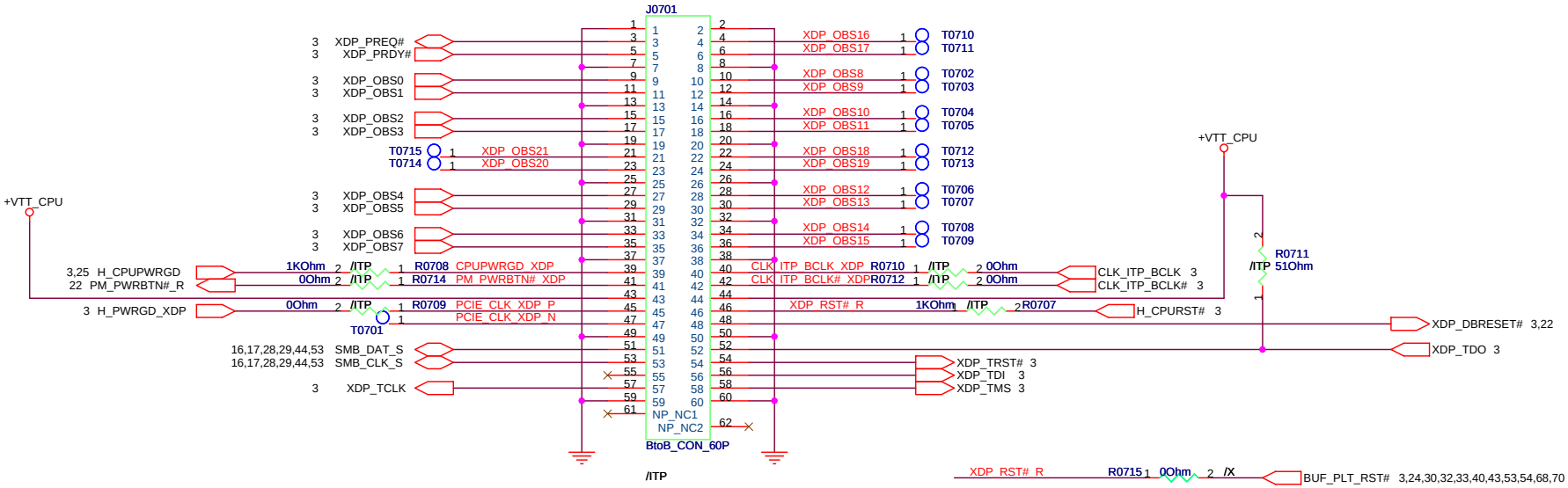
Processor Decoupling

Decoupling guide from Intel

WW30:	Schematic Checklist R0.7:
VCORE 22uF * 28pcs	VCORE 22uF * 12pcs
	10uF * 16pcs
470uF* 6pcs(2 no stuff).	470uF* 6pcs(2 no stuff).



ASUSTeK COMPUTER INC. NB1	Title : CPU(4)_PWR		
	Engineer: yun-feng_yan		
Size: C	Project Name: N61Jv		Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 6 of 95		



CPU XDP connector

ASUSTeK COMPUTER INC. NB1	Title : CPU(5)_XDP		
	Engineer: Yun-feng_yan		
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Friday, December 11, 2009	Sheet 7 of 95		

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: CH_Lin		
Size: Custom	Project Name: N61JA		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 8 of 95		

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB ****	
	Engineer: CH_Lin	
Size: Custom	Project Name: N61JA	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 9 of 95	

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: CH_Lin		
Size: Custom	Project Name: N61JA		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 10 of 95		

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: CH_Lin		
Size: Custom	Project Name: N61JA		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 11 of 95		

Main Board

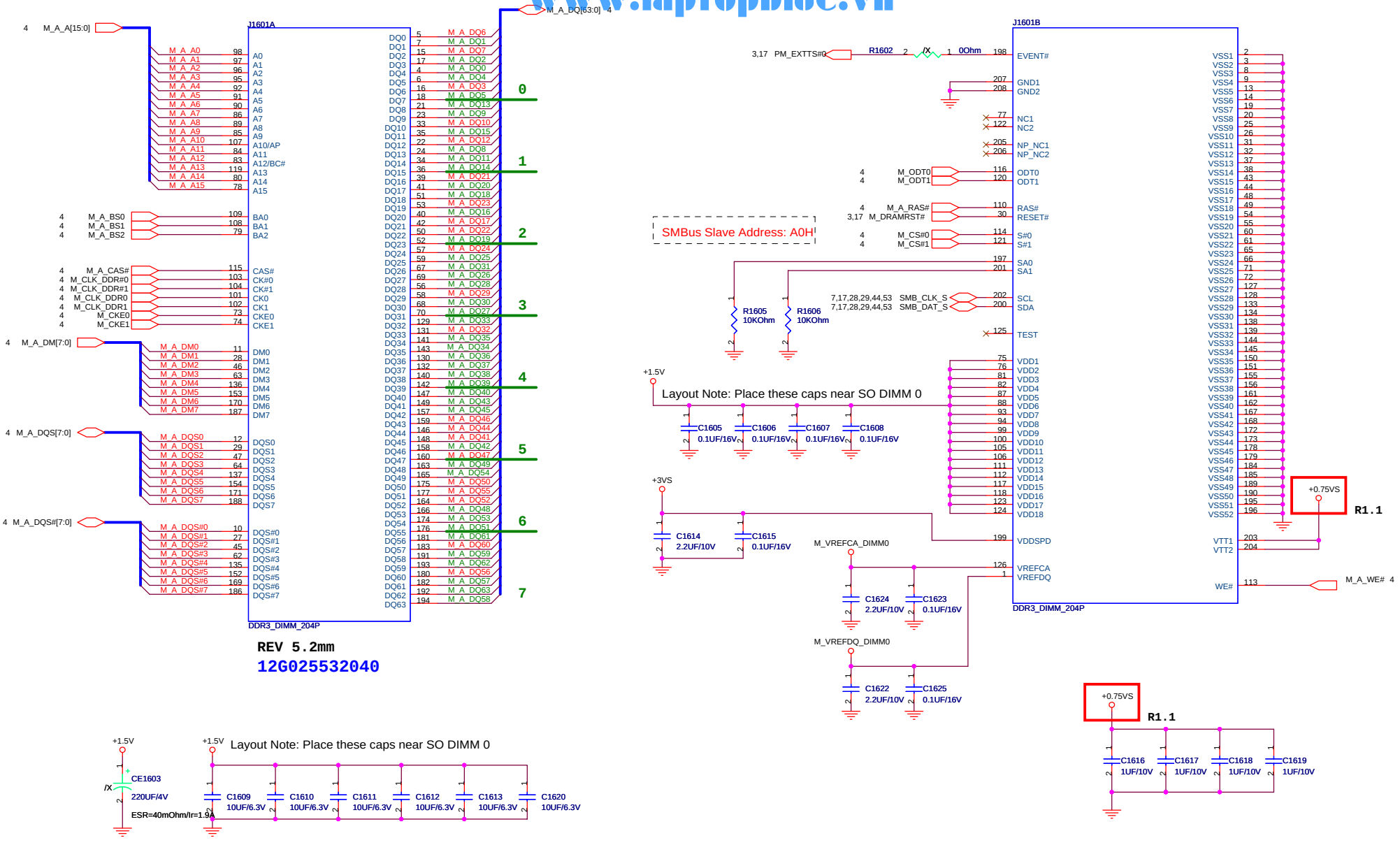
ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: CH_Lin		
Size: Custom	Project Name: N61JA		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 12 of 95		

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: CH_Lin		
Size: Custom	Project Name: N61JA		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 13 of 95		

ASUSTeK COMPUTER INC. NB6	Title :	Engineer: CH_Lin
Size: A	Project Name: N61JA	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 14 of 95	

ASUSTeK COMPUTER INC. NB6	Title :	Engineer: CH_Lin
Size: A	Project Name: N61JA	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 15 of 95	



Title	DDR3 SO-DIMM_0	
ASUSTeK COMPUTER INC. NB6	Engineer:	yun-feng_yan
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 16 of 95	

SWAP

M_B_DQ[63:0] 4

4 M_B_A[15:0]

J1701A

M_B_A0 98 A0
M_B_A1 97 A1
M_B_A2 96 A2
M_B_A3 95 A3
M_B_A4 92 A4
M_B_A5 91 A5
M_B_A6 90 A6
M_B_A7 86 A7
M_B_A8 89 A8
M_B_A9 85 A9
M_B_A10 107 A10/AP
M_B_A11 84 A11
M_B_A12 83 A12/BC#
M_B_A13 119 A13
M_B_A14 80 A14
M_B_A15 78 A15

4 M_B_BS0 109 BA0
4 M_B_BS1 108 BA1
4 M_B_BS2 79 BA2

4 M_B_CAS# 115 CAS#
4 M_CLK_DDR#2 103 CK#0
4 M_CLK_DDR#3 104 CK#1
4 M_CLK_DDR2 101 CK0
4 M_CLK_DDR3 102 CK1
4 M_CKE2 73 CKE0
4 M_CKE3 74 CKE1

4 M_B_DM[7:0]
M_B_DM0 11 DM0
M_B_DM1 28 DM1
M_B_DM2 46 DM2
M_B_DM3 63 DM3
M_B_DM4 136 DM4
M_B_DM5 153 DM5
M_B_DM6 170 DM6
M_B_DM7 187 DM7

4 M_B_DQS[7:0]
M_B_DQS0 12 DQS0
M_B_DQS1 29 DQS1
M_B_DQS2 47 DQS2
M_B_DQS3 64 DQS3
M_B_DQS4 137 DQS4
M_B_DQS5 154 DQS5
M_B_DQS6 171 DQS6
M_B_DQS7 188 DQS7

4 M_B_DQS#[7:0]
M_B_DQS#0 10 DQS#0
M_B_DQS#1 27 DQS#1
M_B_DQS#2 45 DQS#2
M_B_DQS#3 62 DQS#3
M_B_DQS#4 135 DQS#4
M_B_DQS#5 152 DQS#5
M_B_DQS#6 169 DQS#6
M_B_DQS#7 186 DQS#7

DQ0 5 M_B_DQ5
DQ1 7 M_B_DQ4
DQ2 15 M_B_DQ7
DQ3 17 M_B_DQ6
DQ4 4 M_B_DQ0
DQ5 6 M_B_DQ1
DQ6 16 M_B_DQ2
DQ7 18 M_B_DQ3
DQ8 21 M_B_DQ10
DQ9 23 M_B_DQ8
DQ10 33 M_B_DQ11
DQ11 35 M_B_DQ14
DQ12 22 M_B_DQ9
DQ13 24 M_B_DQ12
DQ14 34 M_B_DQ15
DQ15 36 M_B_DQ13
DQ16 39 M_B_DQ17
DQ17 41 M_B_DQ20
DQ18 51 M_B_DQ23
DQ19 53 M_B_DQ18
DQ20 40 M_B_DQ16
DQ21 42 M_B_DQ21
DQ22 50 M_B_DQ22
DQ23 52 M_B_DQ19
DQ24 57 M_B_DQ28
DQ25 59 M_B_DQ25
DQ26 67 M_B_DQ26
DQ27 69 M_B_DQ31
DQ28 56 M_B_DQ24
DQ29 58 M_B_DQ29
DQ30 68 M_B_DQ27
DQ31 70 M_B_DQ30
DQ32 129 M_B_DQ33
DQ33 131 M_B_DQ37
DQ34 141 M_B_DQ35
DQ35 143 M_B_DQ38
DQ36 130 M_B_DQ36
DQ37 132 M_B_DQ32
DQ38 140 M_B_DQ34
DQ39 142 M_B_DQ39
DQ40 147 M_B_DQ41
DQ41 149 M_B_DQ44
DQ42 157 M_B_DQ42
DQ43 159 M_B_DQ43
DQ44 146 M_B_DQ45
DQ45 148 M_B_DQ40
DQ46 158 M_B_DQ46
DQ47 160 M_B_DQ47
DQ48 163 M_B_DQ48
DQ49 165 M_B_DQ50
DQ50 175 M_B_DQ54
DQ51 177 M_B_DQ55
DQ52 164 M_B_DQ52
DQ53 166 M_B_DQ53
DQ54 174 M_B_DQ51
DQ55 176 M_B_DQ49
DQ56 181 M_B_DQ60
DQ57 183 M_B_DQ57
DQ58 191 M_B_DQ61
DQ59 193 M_B_DQ63
DQ60 180 M_B_DQ56
DQ61 182 M_B_DQ58
DQ62 192 M_B_DQ59
DQ63 194 M_B_DQ62

DDR3_DIMM_204P

STD 9.2mm

12G02553204D

+1.5V
/X CE1703 220UF/4V
ESR=40mOhm/Ir=1.9A

+1.5V Layout Note: Place these caps near SO DIMM 1
C1709 10UF/6.3V
C1710 10UF/6.3V
C1711 10UF/6.3V
C1712 10UF/6.3V
C1713 10UF/6.3V
C1726 10UF/6.3V

J1701B

3,16 PM_EXTTS#0 — RX1704 0Ohm /X — 198 EVENT#

207 GND1
208 GND2

77 NC1
122 NC2
205 NP_NC1
206 NP_NC2

4 M_ODT2 — 116 ODT0
4 M_ODT3 — 120 ODT1

4 M_B_RAS# — 110 RAS#
3,16 M_DRAMRST# — 30 RESET#

4 M_CS#2 — 114 S#0
4 M_CS#3 — 121 S#1

SMBus Slave Address: A4H

+3VS — R1706 10KOhm — 197 SA0, 201 SA1

R1705 10KOhm
7,16,28,29,44,53 SMB_CLK_S — 202 SCL
7,16,28,29,44,53 SMB_DAT_S — 200 SDA

125 TEST

+1.5V Layout Note: Place these caps near SO DIMM 1
C1705 0.1UF/16V
C1706 0.1UF/16V
C1707 0.1UF/16V
C1708 0.1UF/16V

75 VDD1
76 VDD2
81 VDD3
82 VDD4
87 VDD5
88 VDD6
93 VDD7
94 VDD8
99 VDD9
100 VDD10
105 VDD11
106 VDD12
111 VDD13
112 VDD14
117 VDD15
118 VDD16
123 VDD17
124 VDD18

+3VS
C1714 2.2UF/10V
C1715 0.1UF/16V

199 VDDSPD

M_VREFCA_DIMM1
C1724 2.2UF/10V
C1723 0.1UF/16V

126 VREFCA
1 VREFDQ

M_VREFDQ_DIMM1
C1722 2.2UF/10V
C1725 0.1UF/16V

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43
VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

+0.75VS R1.1

VTT1 203
VTT2 204

WE# 113 — M_B_WE# 4

DDR3_DIMM_204P

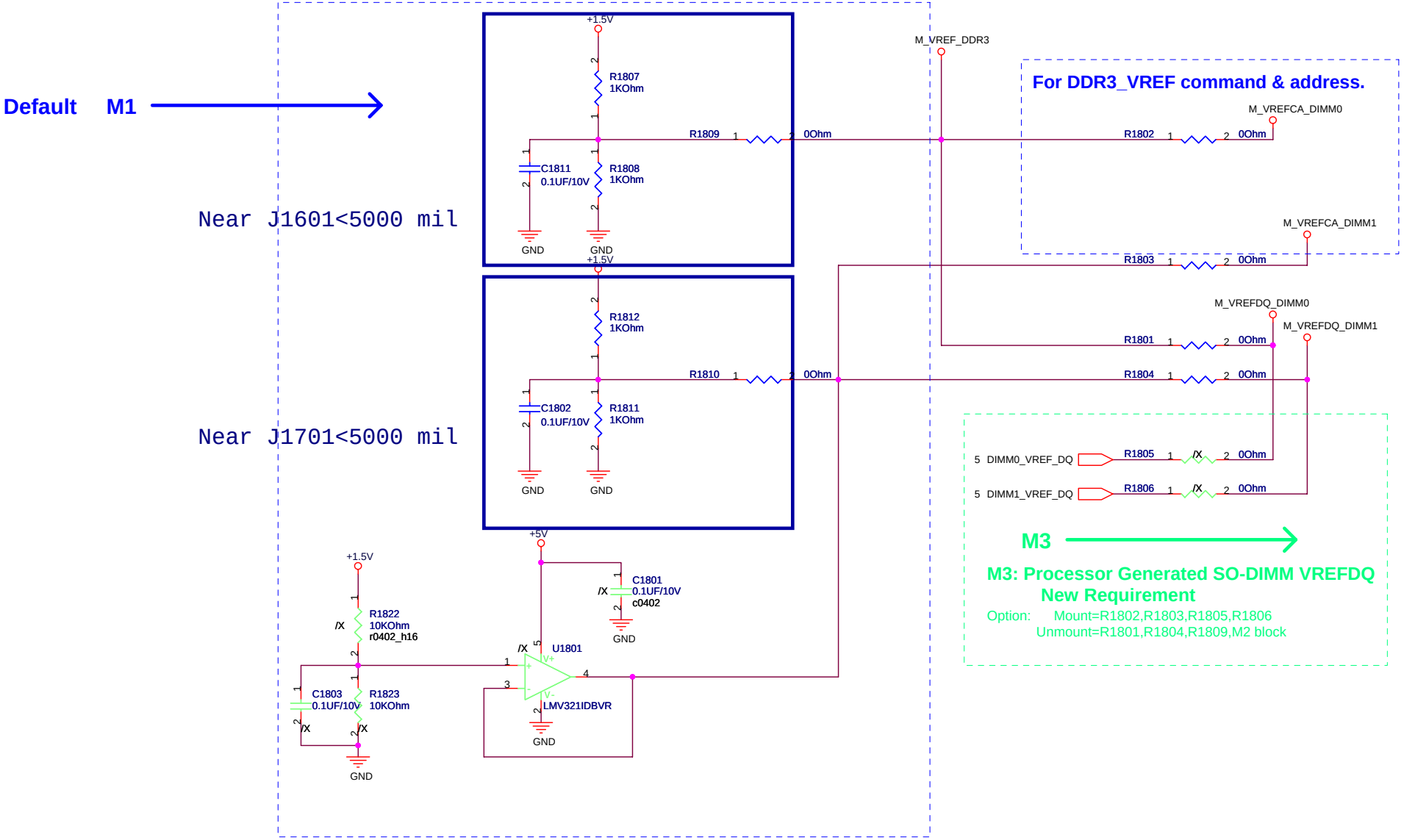
+0.75VS R1.1
C1716 1UF/10V
C1717 1UF/10V
C1718 1UF/10V
C1719 1UF/10V

ASUSTeK COMPUTER INC. NB6	Title: DDR3 SO-DIMM_1	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 17 of 95	

Calpella Clarksfield DDR3 SO-DIMM VREFDQ
Platform Design Guide Change Details

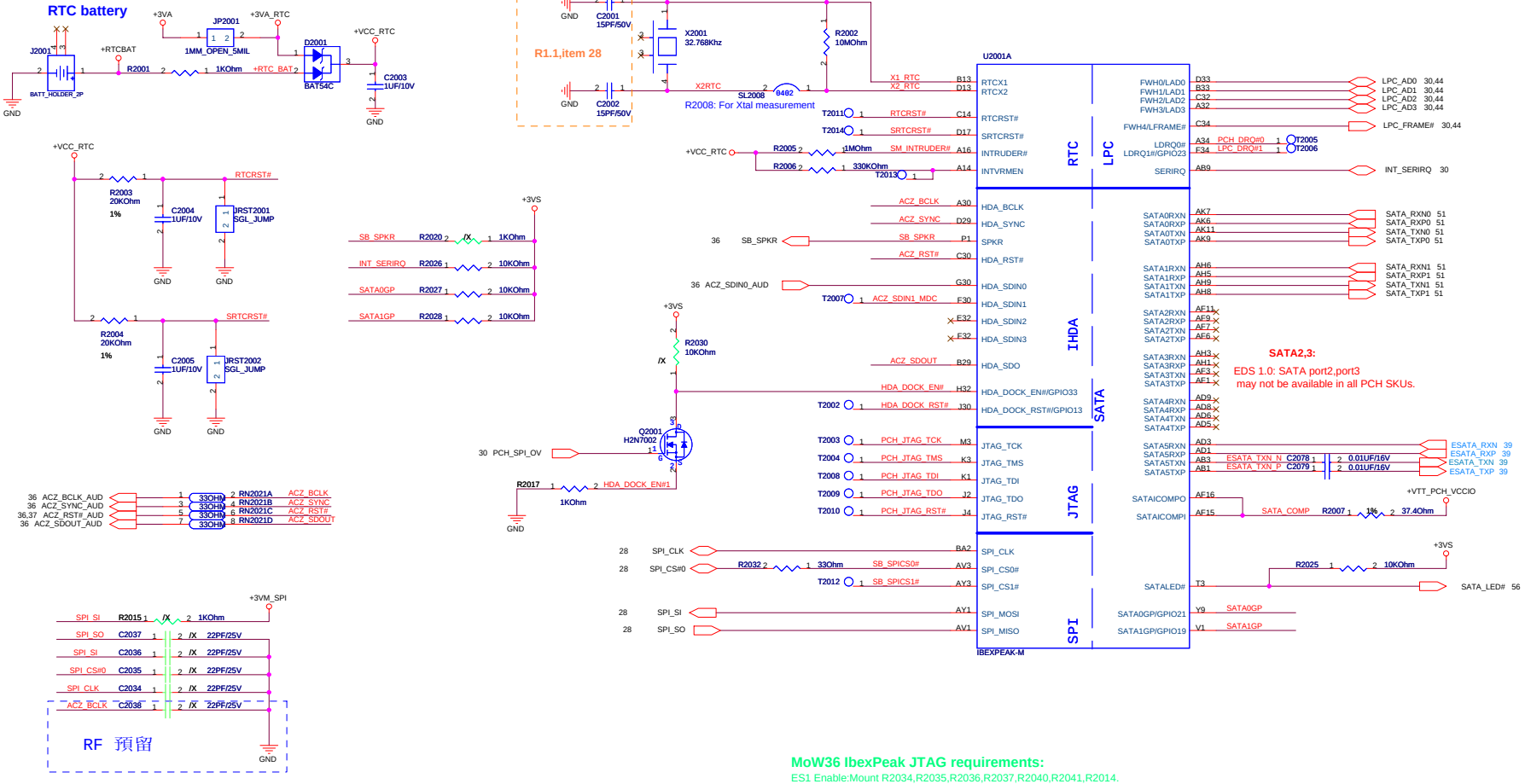
DDR3 Vref

Intel Document Number: 400755



ASUSTeK COMPUTER INC. NB6	Title : CA_DQ VOLTAGE	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 18 of 95	

<Engineer Name>	Title : VID		
ASUSTeK COMPUTER INC. NB1	Engineer:		
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 19 of 95		



414044 Design Guide R1.11 Update: page9

GPIO33:
This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.

Without connecting GPIO33,
customers may not be able to override SPI flash contents.

Strap information:

HDA_SPKR: No reboot strap
- **Low: Disable.**
- **High:Enable**

HDA_DOCK_EN#:
1. **Flash descriptor security:**
   - **Sampled low: override**
   - **Sampled high: in effect.**
2. **GPIO33 low on the rising edge of PWROK,**
   Will also disable Intel ME.

SPI_MOSI: iTPM strap.
- **Mount R2015: Enable**
- **Unmount R2015: Disable(default)**

MoW36 IbexPeak JTAG requirements:

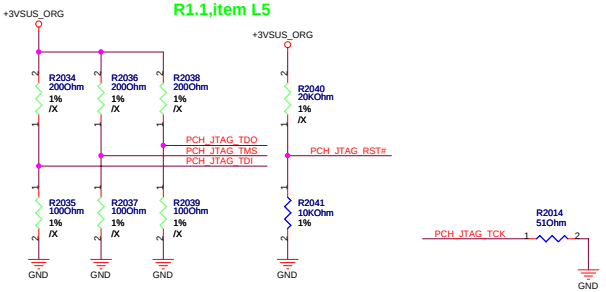
ES1 Enable:Mount R2034,R2035,R2036,R2037,R2040,R2041,R2014.
DNI R2038,R2039. (TDO)
ES1 Disable:Mount R2040,R2041,R2014.
DNI: others.

R1.2,item L5

MoW50 IbexPeak JTAG requirements:

Stuff for pre-production

R1.1,item L5



ES2 Mount :R2034,R2035,R2036,R2037,R2038,R2039,R2040,R2041,R2014.

ASUSTeK COMPUTER INC. NB6	Title : SATA,IHDA,RTC,LPC	
	Engineer: yun-feng_yan	
Size: C	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 20 of 95	

PCIE 1	TV Tuner
PCIE 2	WLAN
PCIE 3	NewCard
PCIE 4	USB 3.0
PCIE 5	
PCIE 6	LAN
PCIE 7	
PCIE 8	

U2001B

PCI-E* / SMBus / Controller Link / PEG / From CLK BUFFER / Clock Flex

PCIE7,8:

EDS 1.0: port7,port8 may not be available in all PCH SKUs.

Note: Place these resisters near to PCIe Slots

iBEXPEAK-M

R2120: For Xtal measurement

PCH CLKREQ Setting:

Not connected to device.

Connected to device.

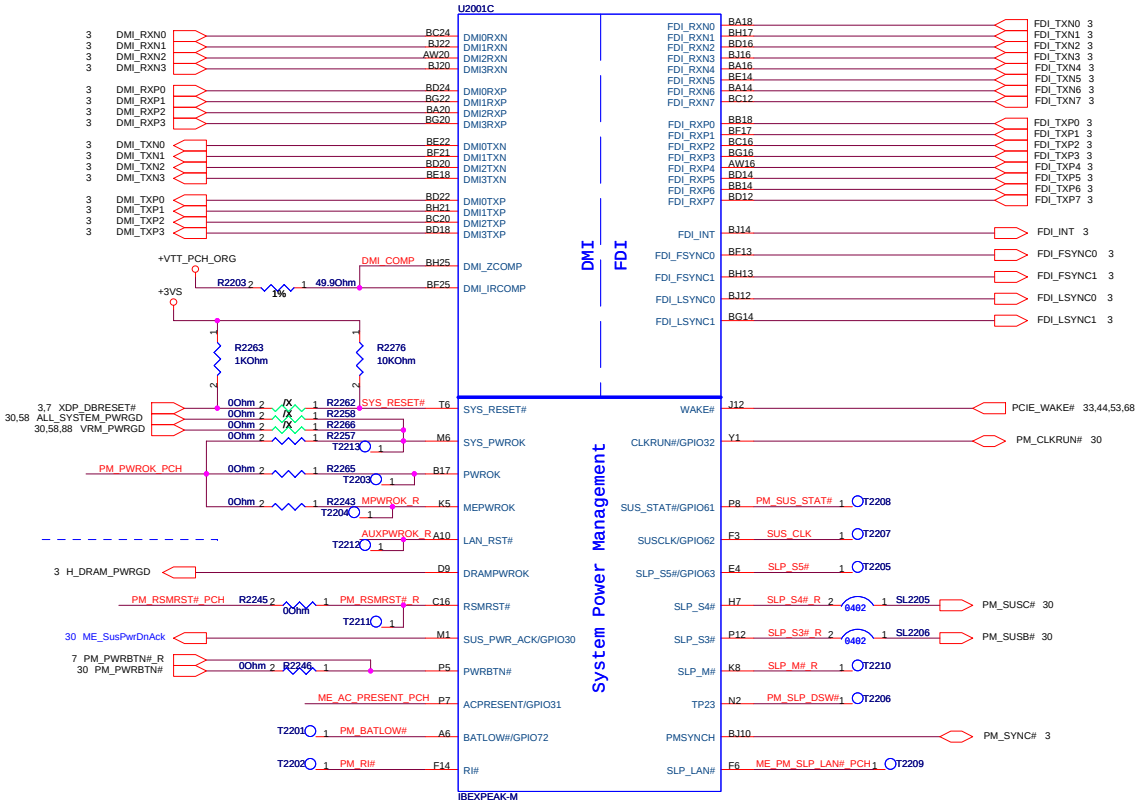
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.

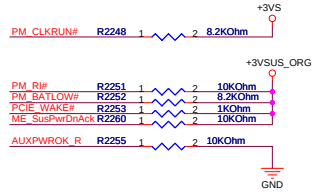
R1.2,item L1

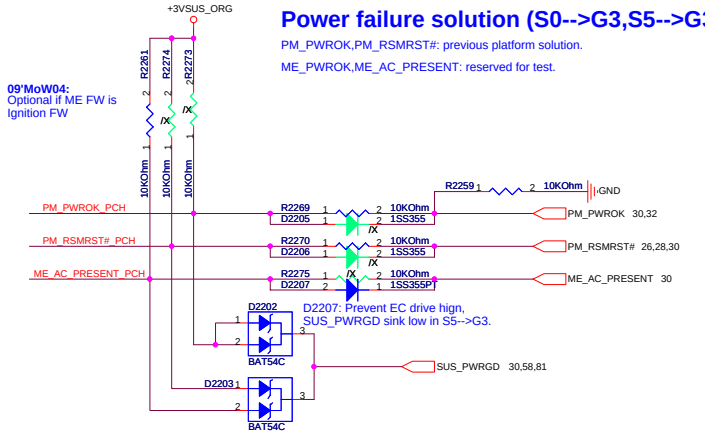
R1.1,item 25

Title :	PCIE,CLK,SMB,PEG
ASUSTeK COMPUTER INC. NB6	Engineer: yun-feng_yan
Size: Custom	Project Name: N61Jv
Rev: 1.0	
Date: Friday, December 11, 2009	Sheet 21 of 95

pre-ES1 not support
Reversal Feature







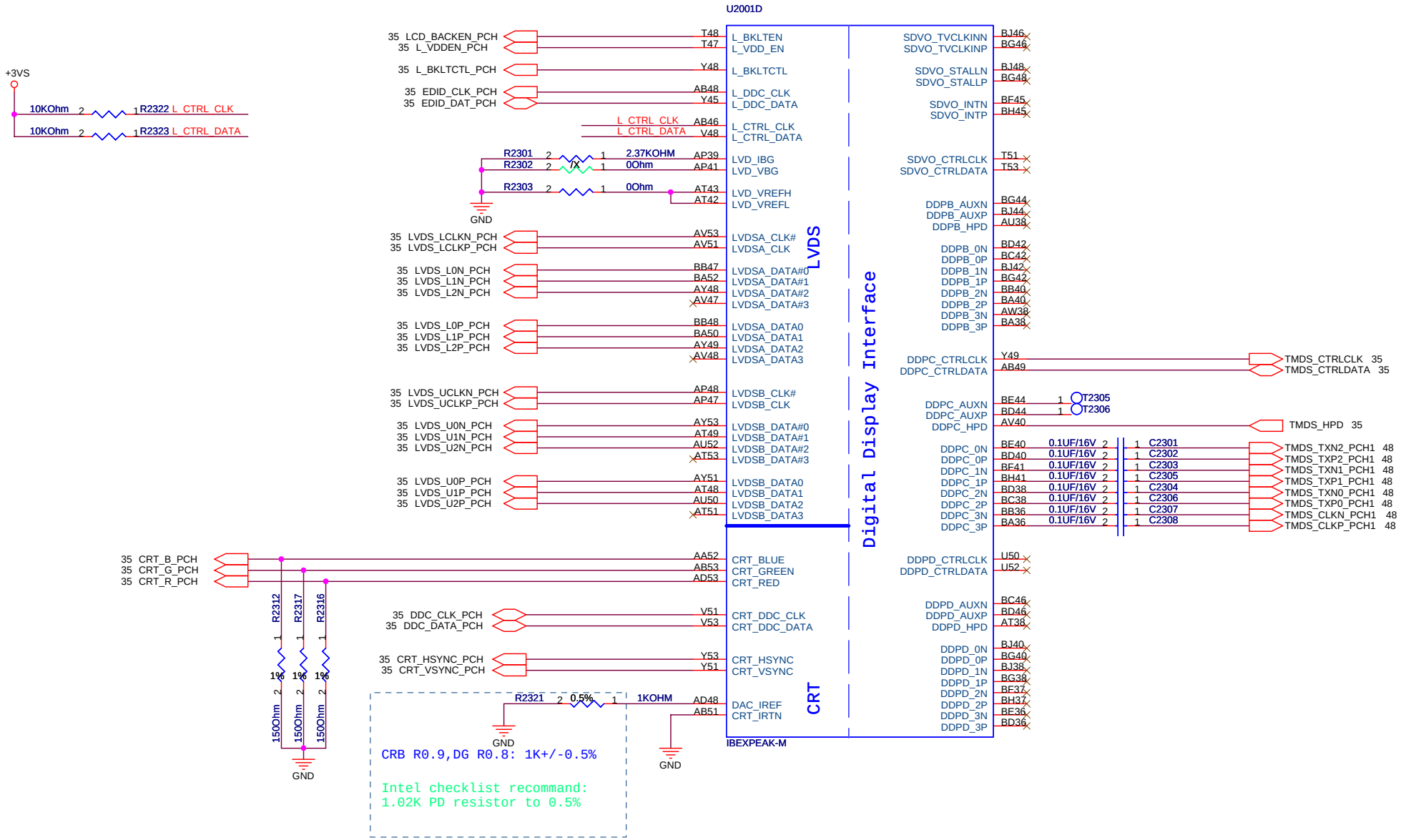
Power failure solution (S0-->G3,S5-->G3):

PM_PWROK,PM_RSMRST#: previous platform solution.

ME_PWROK,ME_AC_PRESENT: reserved for test.

D2207: Prevent EC drive high,
SUS_PWRGD sink low in S5-->G3.

ASUSTeK COMPUTER INC. NB6	Title : FDI,DMI,SYS PWR		
	Engineer: yun-feng_yan		
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 22 of 95		



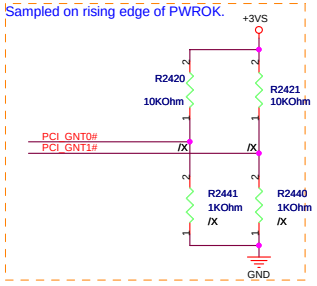
ASUSTeK COMPUTER INC. NB6	Title : DP,LVDS,CRT	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 23 of 95	

GNT0#,GNT1#: Boot BIOS Strap.

Boot BIOS Strap

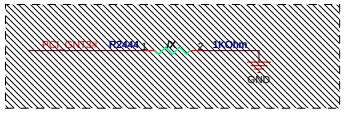
PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI **(PCH)**

Sampled on rising edge of PWROK.



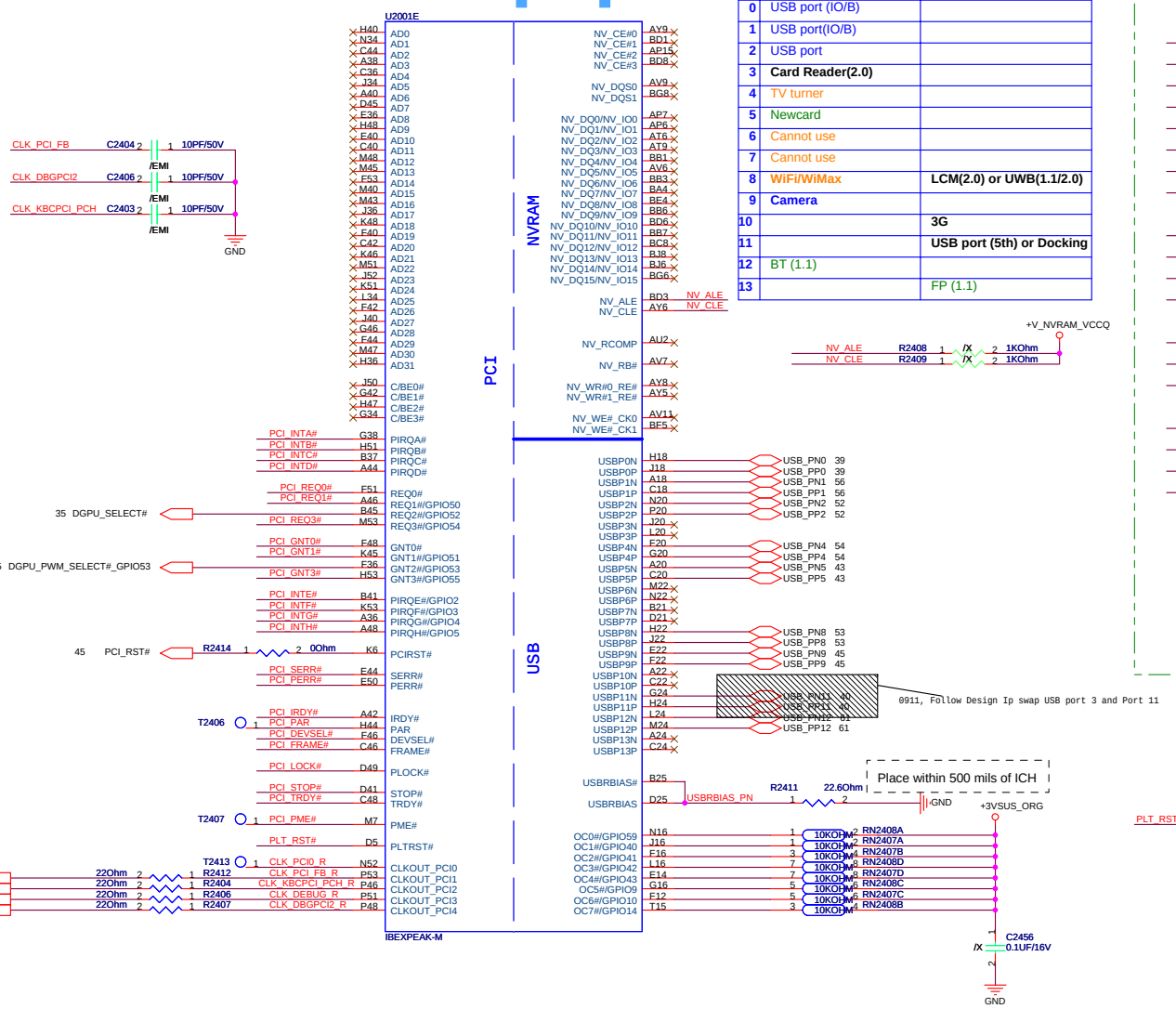
GNT3#: A16 swap override Strap/ Top-Block swap override jumper

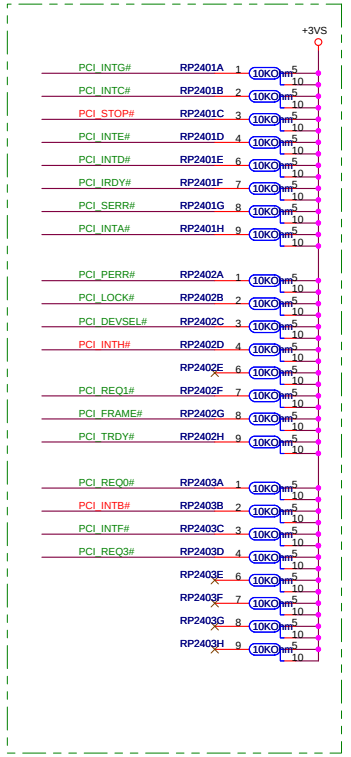
Low=Enabled A16 swap override/ Top-Block swap override
High=Default



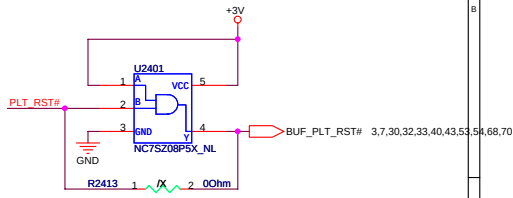
DGPU_SELECT#:
0=dGPU, 1=iGPU

N61Jv	Recommand settings
0 USB port (IO/B)	
1 USB port(IO/B)	
2 USB port	
3 **Card Reader(2.0)**	
4 TV turner	
5 Newcard	
6 Cannot use	
7 Cannot use	
8 **WiFi/WiMax**	**LCM(2.0) or UWB(1.1/2.0)**
9 **Camera**	
10	**3G**
11	**USB port (5th) or Docking**
12 BT (1.1)	
13	FP (1.1)

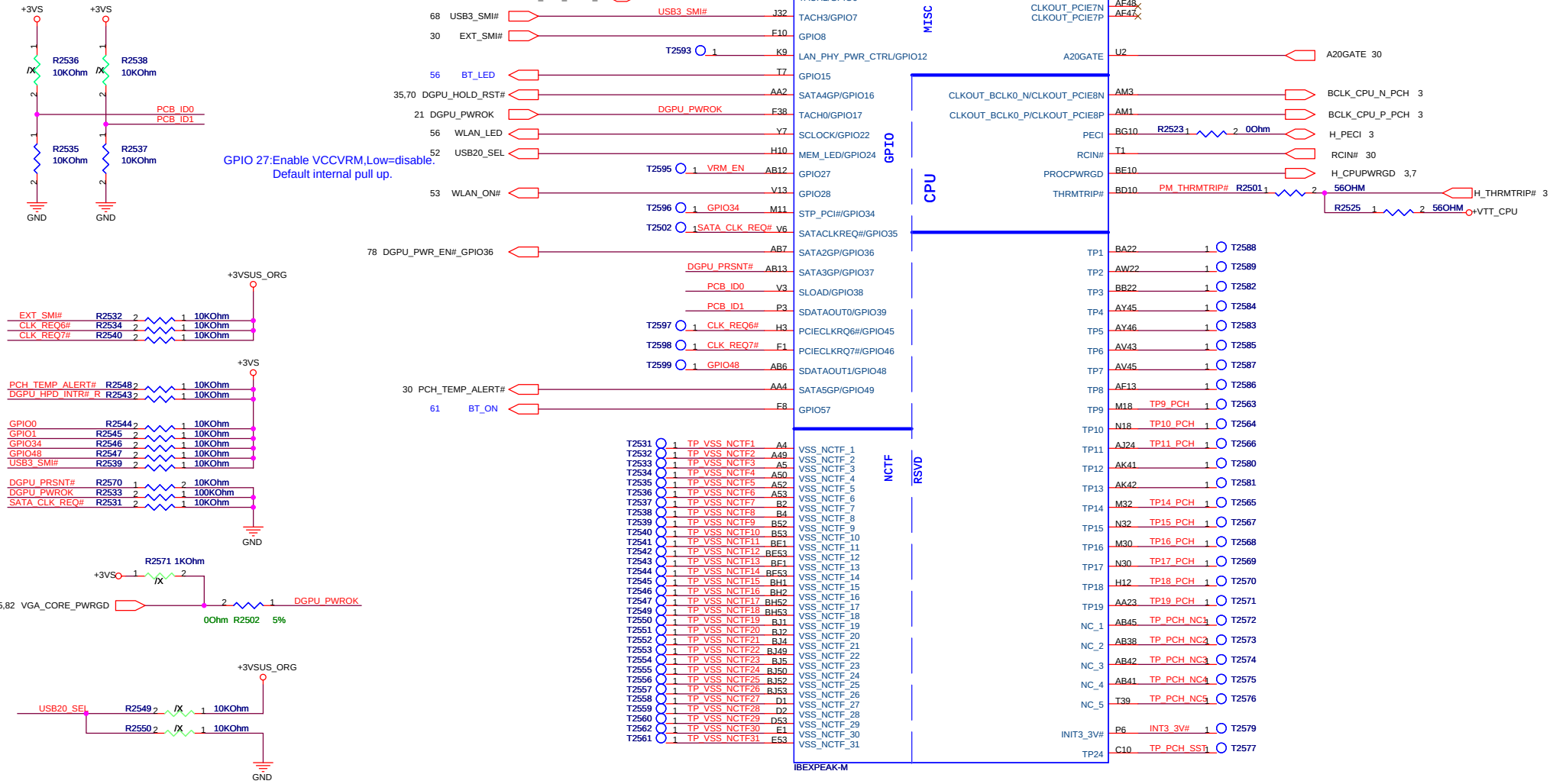




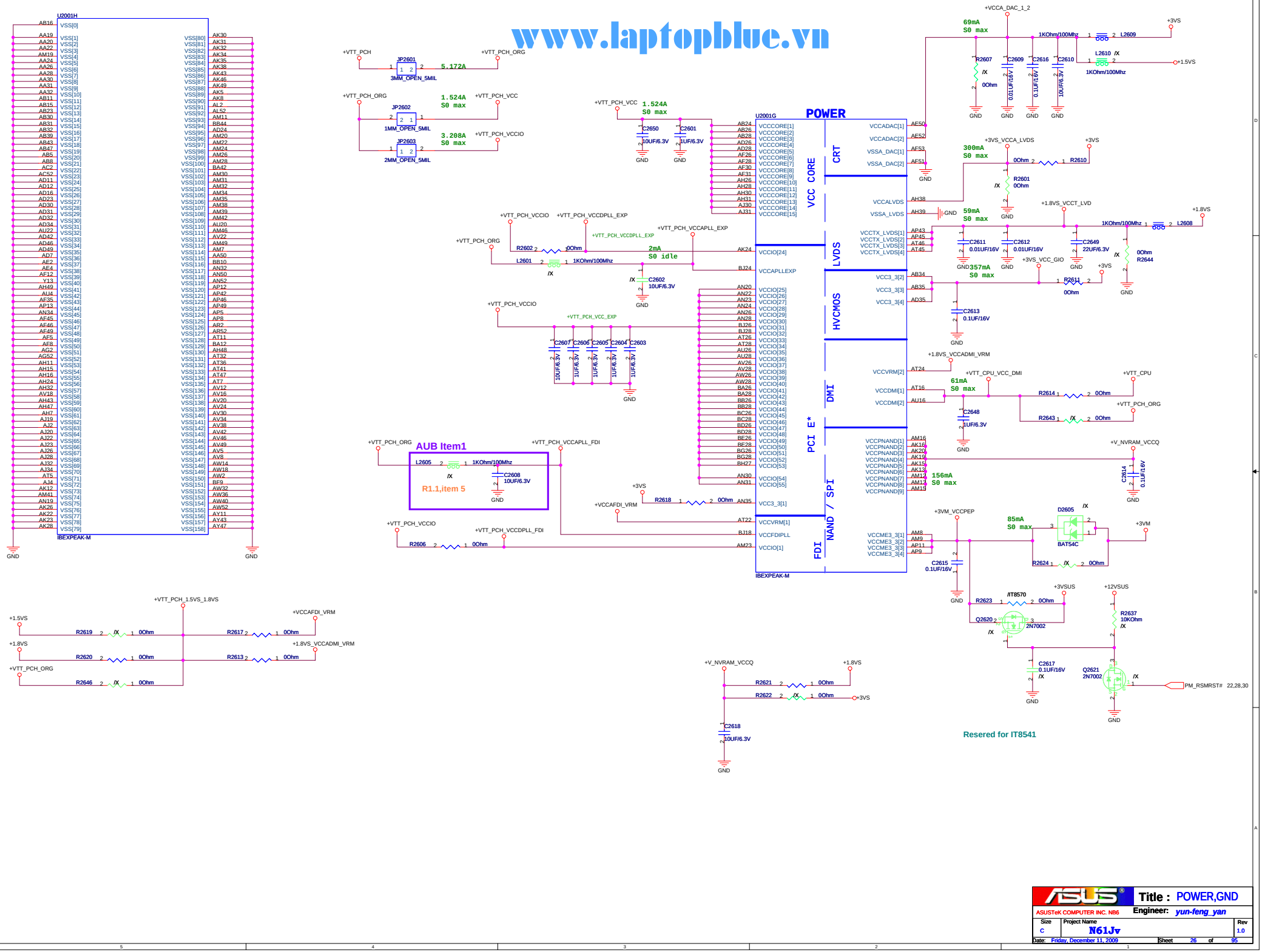
R1.2,item L2

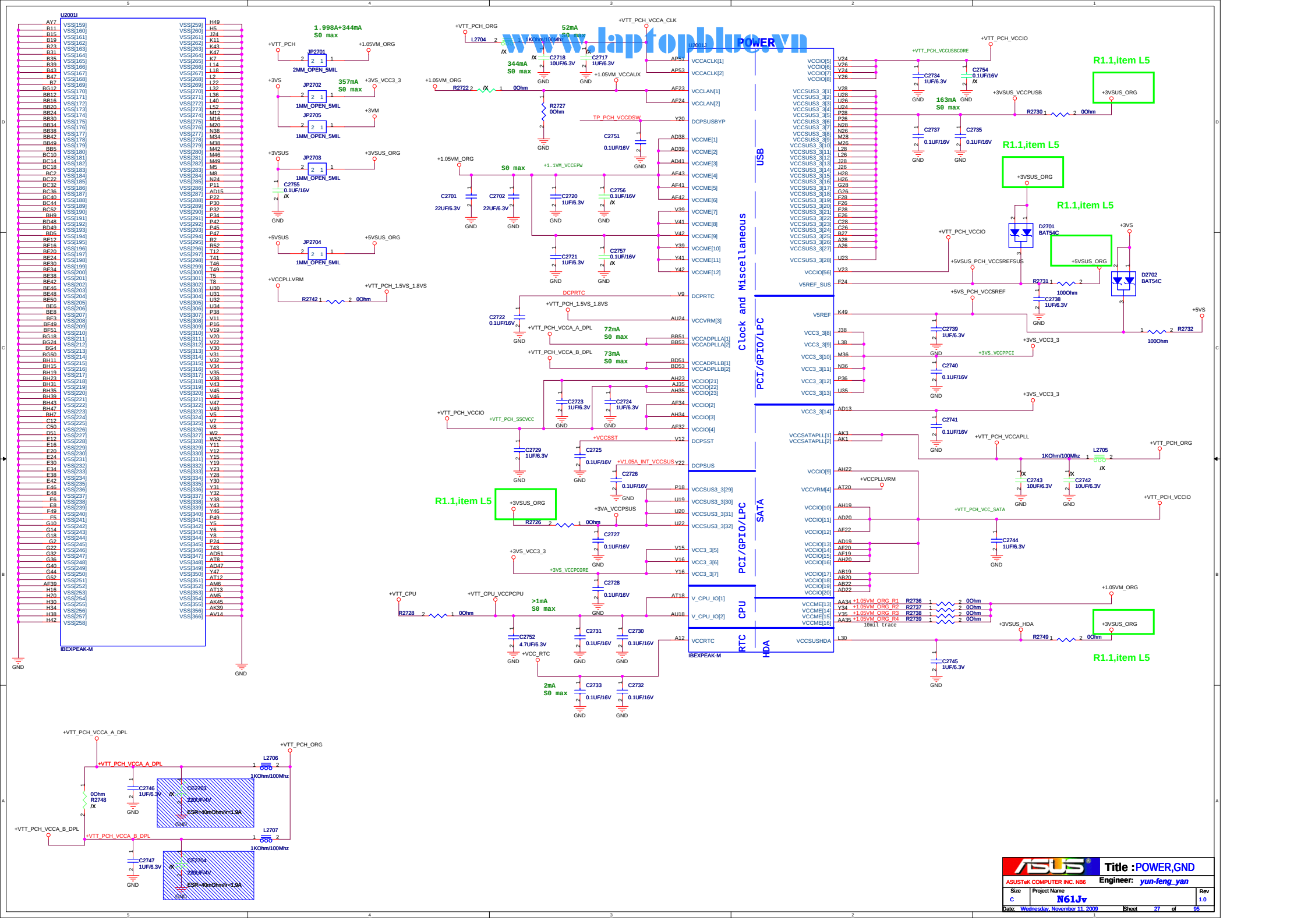


ASUSTeK COMPUTER INC. NB6	Title : PCI,NVRAM,USB		
	Engineer: yun-feng_yan		
Size: Custom	Project Name: N61Jv	Rev: 1.0	
Date: Tuesday, December 15, 2009	Sheet 24 of 95		

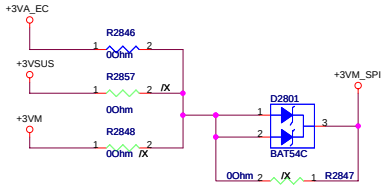


Title :	CPU,GPIO,MISC
ASUSTeK COMPUTER INC. NB6	Engineer: yun-feng_yan
Size: Custom	Project Name: N61Jv
Rev:	1.0
Date:	Friday, December 11, 2009
Sheet	25 of 95




U2001I
iBEXPEAK-M
POWER
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
www.laptopblue.vn
1.998A+344mA
S0 max
52mA
S0 max
344mA
S0 max
357mA
S0 max
163mA
S0 max
72mA
S0 max
73mA
S0 max
>1mA
S0 max
2mA
S0 max
R1.1,item L5
Title :POWER,GND
ASUSTeK COMPUTER INC. NB6
Engineer: yun-feng_yan
Project Name N61Jv
Size C
Rev 1.0
Date: Wednesday, November 11, 2009
Sheet 27 of 95

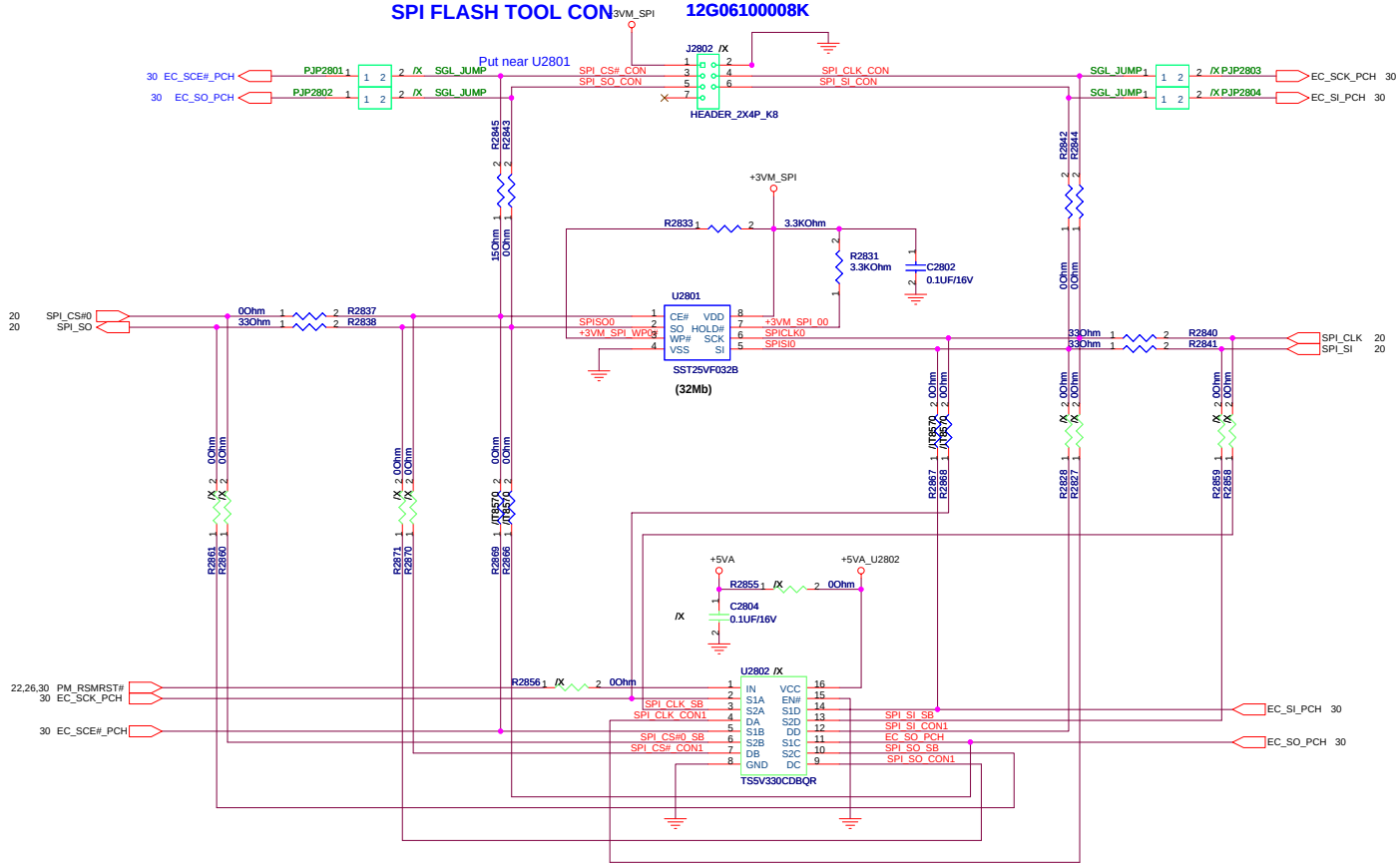
PCH SPI ROM



SPI FLASH TOOL CON

12G06100008K

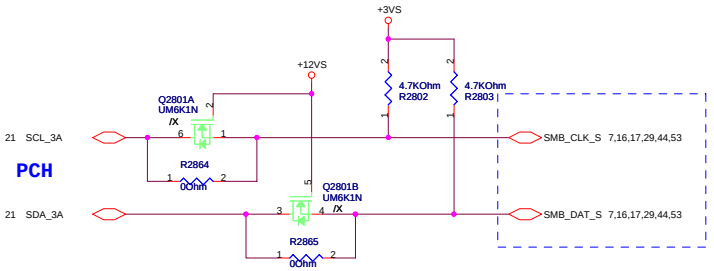
Put near U2801

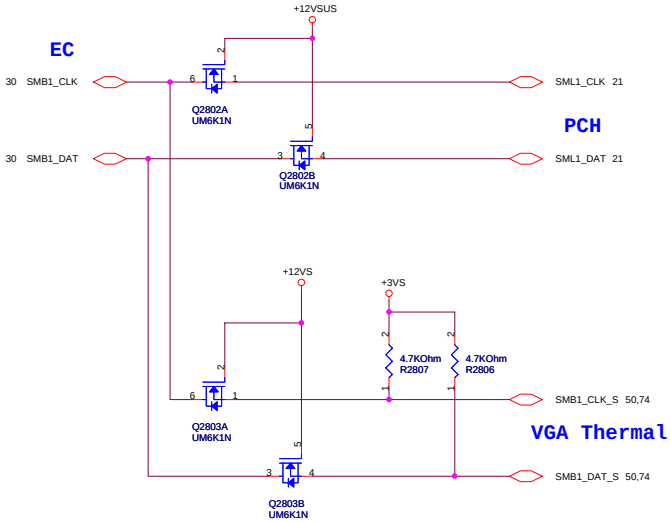


SMBUS Link device:

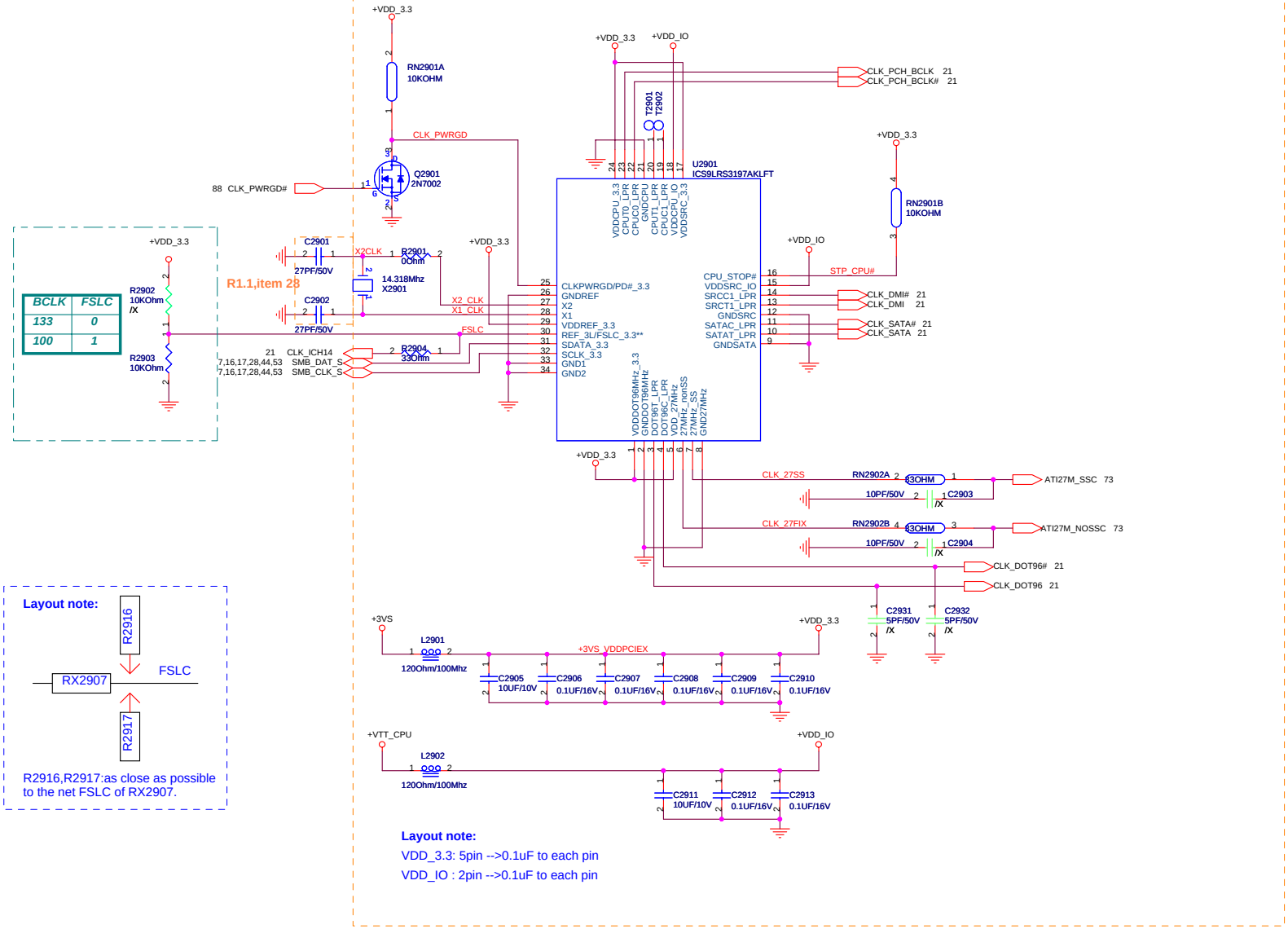
[M52J] SPD, CLKGEN,DEBUG,WLAN,
CPU XDP,PCH XDP,VID CONTROLLER

[G50J] FM2010,GAME LED,





ASUSTeK COMPUTER INC. NB6	Title : SPI ROM,OTH	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 28 of 95	



Layout note:

VDD_3.3: 5pin -->0.1uF to each pin

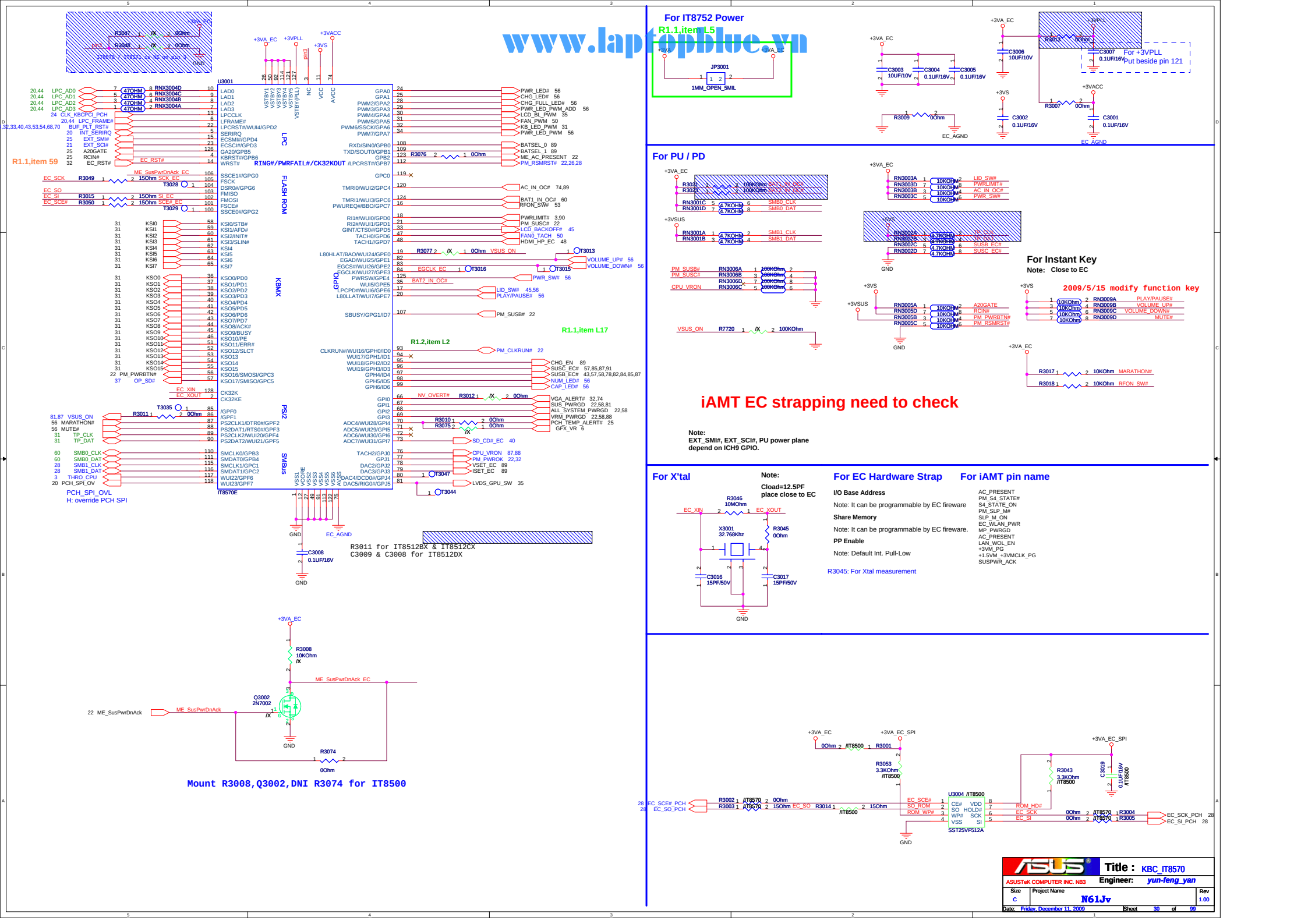
VDD_IO : 2pin -->0.1uF to each pin

R1.1,item 8

Layout note:

R2916,R2917:as close as possible to the net FSLC of RX2907.

ASUSTeK COMPUTER INC. NB4	Title : CLK_ICS9LRS3197		
	Engineer: yun-feng_yan		
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Friday, December 11, 2009	Sheet 29 of 95		


www.laptopblue.vn
For IT8752 Power
R1.1,item L5
JP3001
1MM_OPEN_5MIL
For +3VPLL
Put beside pin 121
For PU / PD
For Instant Key
Note: Close to EC
2009/5/15 modify function key
R1.1,item 59
R1.1,item L17
R1.2,item L2
iAMT EC strapping need to check
Note:
EXT_SMI#, EXT_SCI#, PU power plane
depend on ICH9 GPIO.
For X'tal
Note:
Cload=12.5PF
place close to EC
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
R3045: For Xtal measurement
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
PCH_SPI_OVL
H: override PCH SPI
R3011 for IT8512BX & IT8512CX
C3009 & C3008 for IT8512DX
Mount R3008,Q3002,DNI R3074 for IT8500
U3001
IT8570E
LPC
FLASH ROM
KBMX
GPIO
PS/2
SMBus
RING#/PWRFAIL#/CK32KOUT /LPCRST#/GPB7
Title : KBC_IT8570
ASUSTeK COMPUTER INC. NB3
Engineer: yun-feng_yan
Size C
Project Name N61Jv
Rev 1.00
Date: Friday, December 11, 2009
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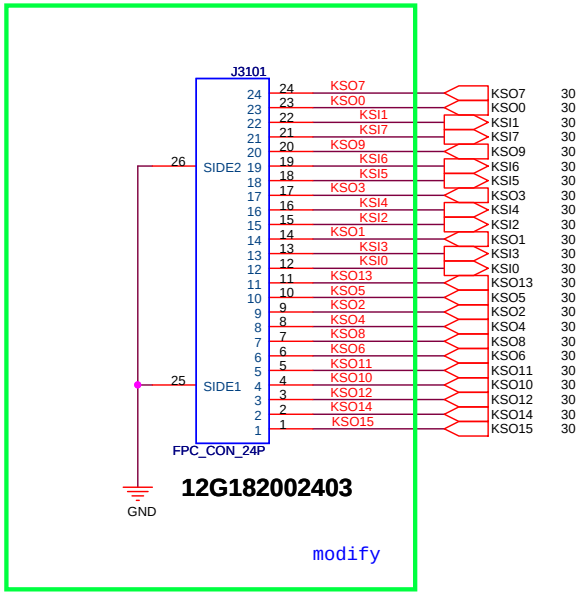
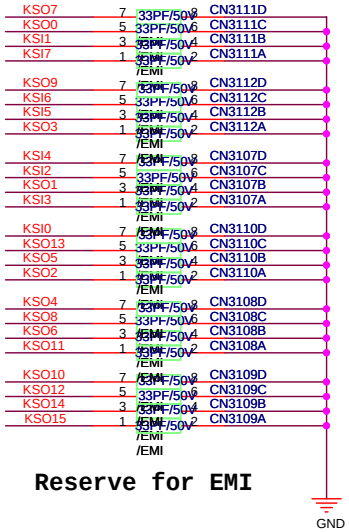
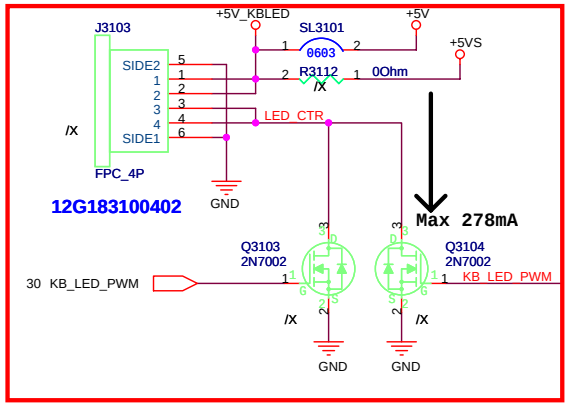
Main Board

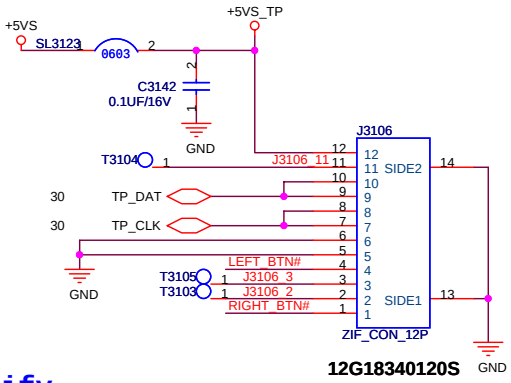
For Keyboard

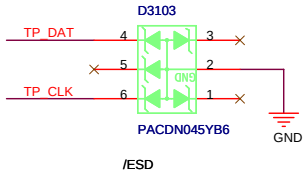


KB LED

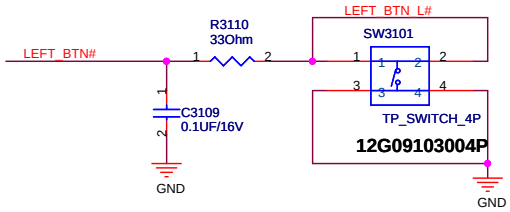


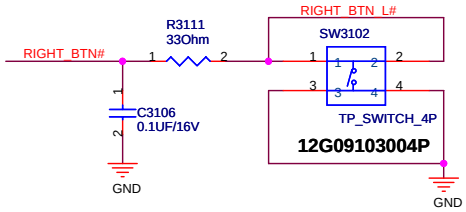




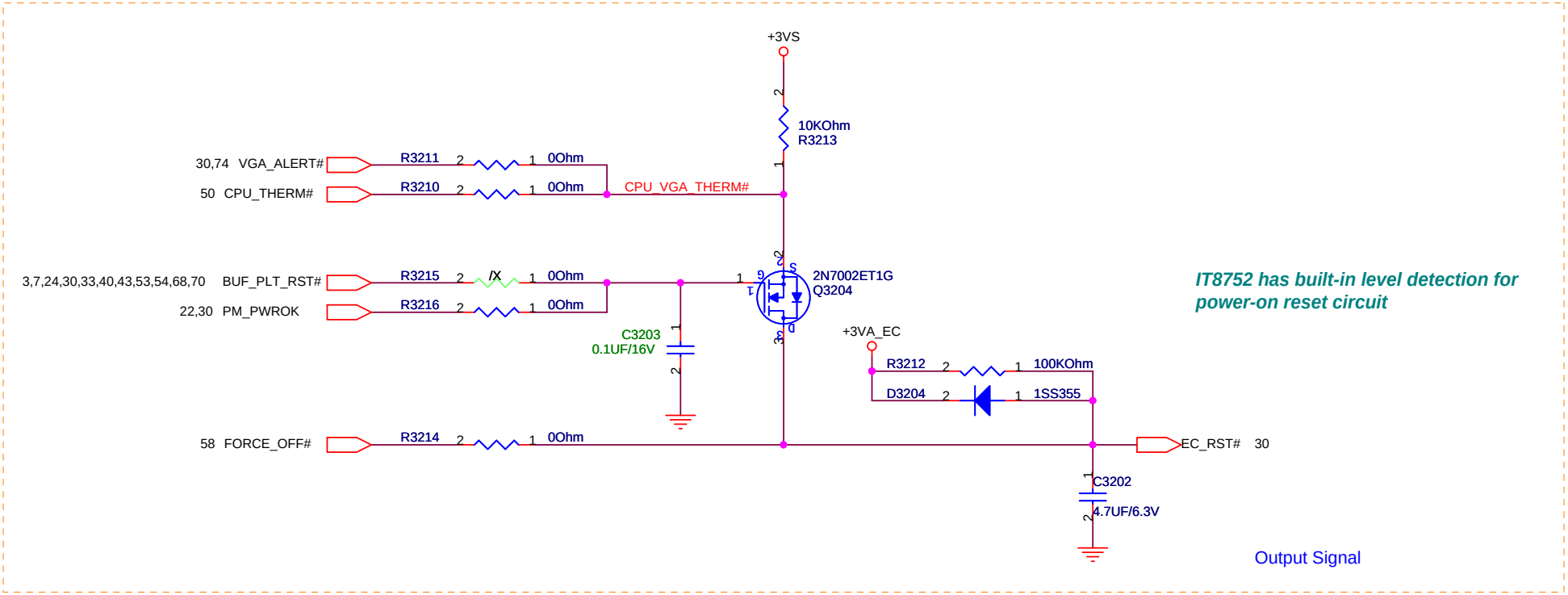


modify





ASUSTeK COMPUTER INC. NB4	Title : IT8512_KB, TP		
	Engineer: yun-feng_yan		
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 31 of 95		



ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 32 of 95	

AR8131:Remove R3301,C3318
AR8121:Remove L3302,C3317,R3302

C3318 close to Pin 1

PIN_1

PIN_6

2009/5/18 change

AR8131:C3319=0.1uF
AR8121:C3319=1uF

AR8131 with overclock: Remove R3315

AR8121:Remove R3315

RF 預留

AR8131:Remove L3303
AR8131:C3321=0.1uF, Remove C3322

With overclock:Remove R3312
Not overclock:Remove R3304

AR8131:L3304=0ohm

For AR8131: Remove R3305,R3306,C3324,C3325,C3326,Q3301
For AR8121: Remove C3327 R3308
Q3301 close to Pin8

PIN_5

AR8121: Remove R3313
AR8131: Remove R3314

AR8121:Remove R3310
AR8131/25MHz:Remove R3310 C3333
AR8131/48MHz:Remove C3333

ground pad要打散熱孔

For AR8131 : Remove R3309

AR8121:Remove C3328
AR8131/25MHz: Remove C3328
AR8131/48MHz: Remove C3329 C3330 X3301

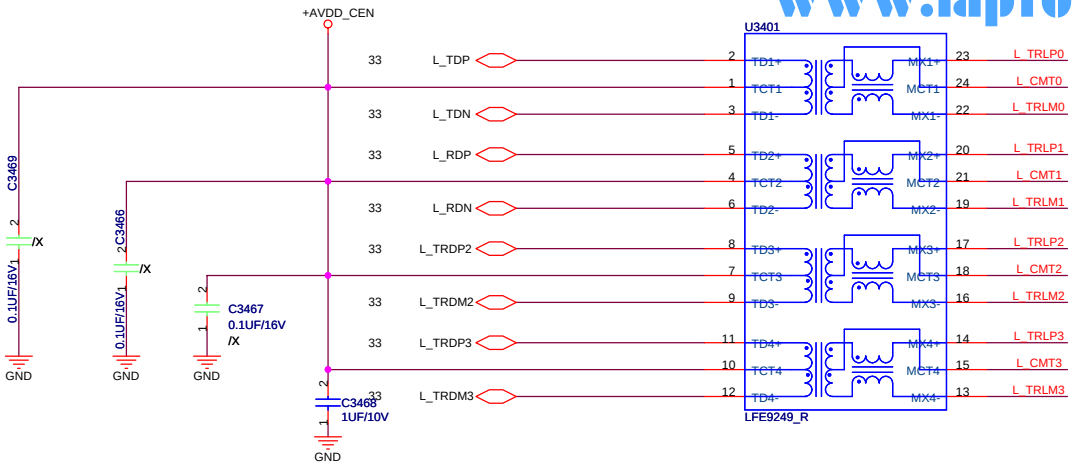
4/10 限高問題, 換料為 07G010S22500

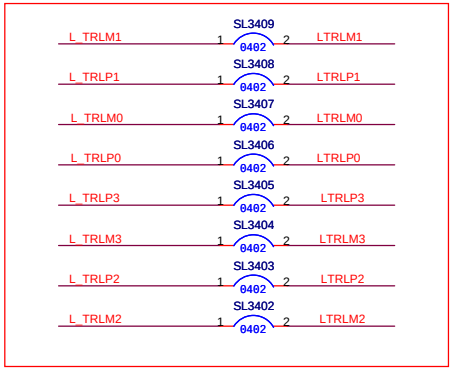
C3301 C3302 C3303 C3304 close to pin2

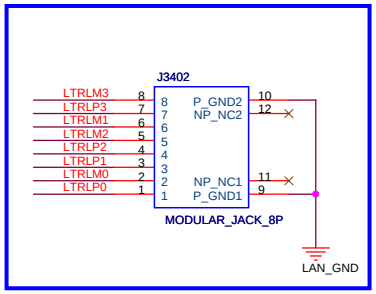
C3305 close to pin15

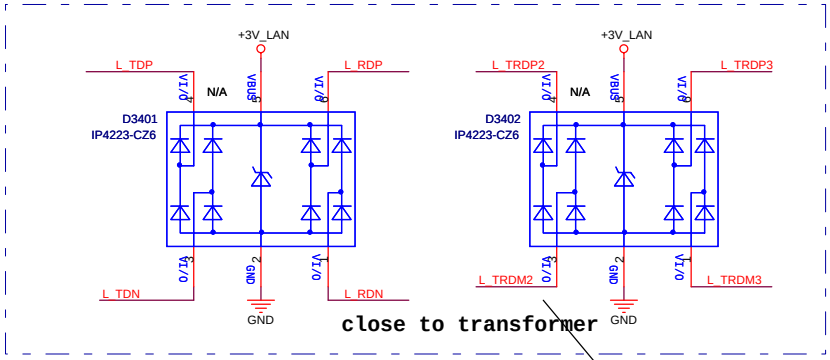
C3308 close to pin45/46

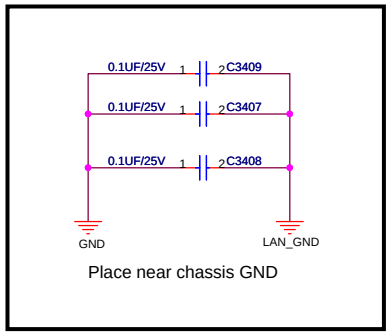
Title :	LAN AR8131
ASUSTeK COMPUTER INC. NB1	Engineer: yun-feng_yan
Size: Custom	Project Name: N61Jv
Rev: 1.0	
Date: Friday, December 11, 2009	Sheet 33 of 95

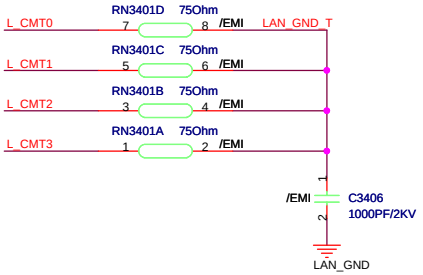


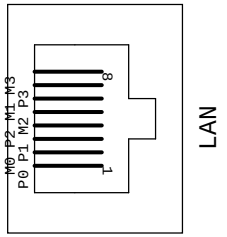












07G001250010 ﻉ 07G028075010 (3/30)

0911, change D3401 and D3402 stuff by default.

ASUSTeK COMPUTER INC. NB1	Title : RJ45	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Monday, December 14, 2009	Sheet 34 of 95	

LVDS Switch

SEL = 0 A+/- TO A0+/-
SEL = 1 A+/- TO A1+/-

Optimus

Optimus

Optimus

該部分零件放置于
LVDS Connector J4502 附近

該部分零件放置于
VGA Connector J4601 附近

Control Signal from PCH

UMA to DGPU Swtich

DGPU to UMA Swtich

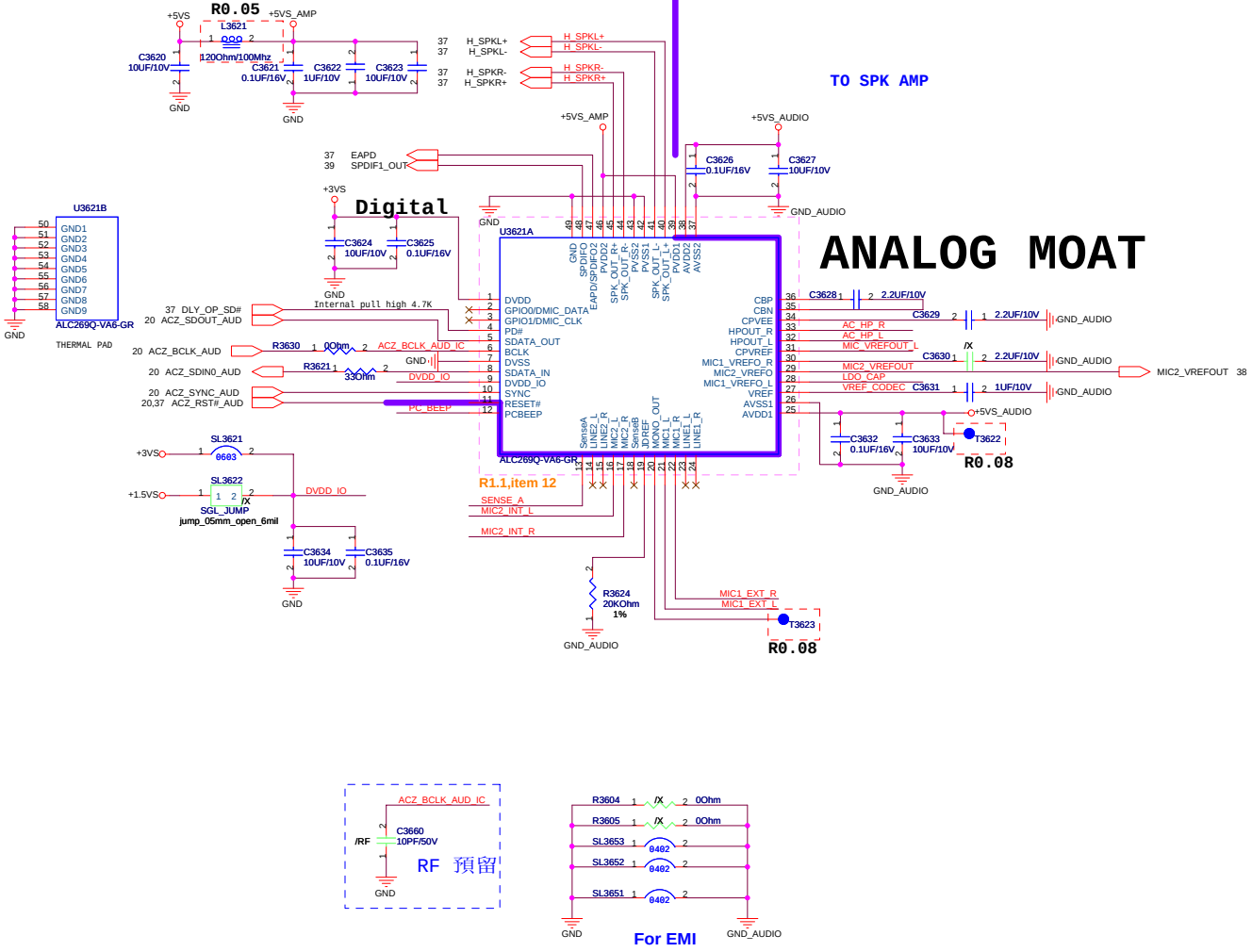
DGPU_SELECT#:
Low : dGPU
High : iGPU

EDID_SELECT#
Low : dGPU
High : iGPU

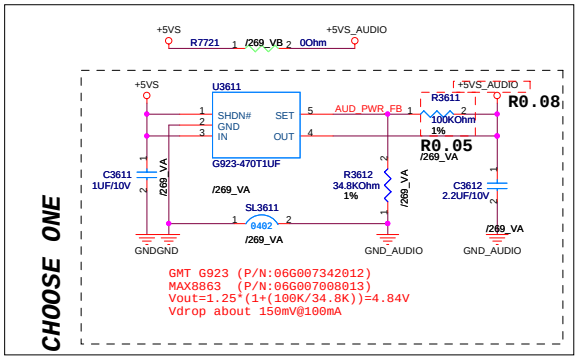
DGPU_PWM_SELECT#_R
Low : EC
High : iGPU

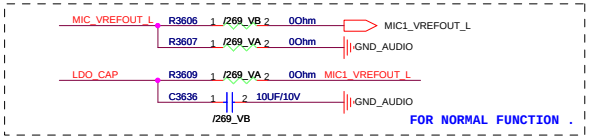
Title : Hybrid Switch
Engineer: yun-feng_yan
ASUSTeK COMPUTER INC. NB1
Size: Custom
Project Name: N61Jv
Rev: 1.0
Date: Tuesday, December 16, 2008
Sheet 35 of 55

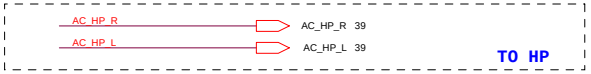
DIGITAL MOAT

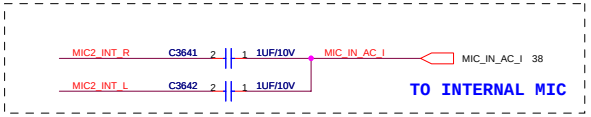


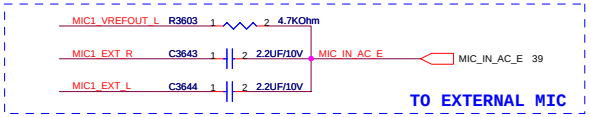
AUDIO POWER

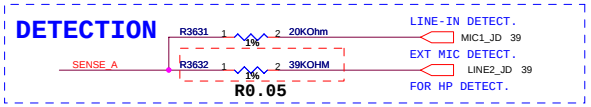


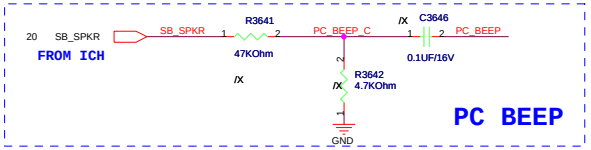






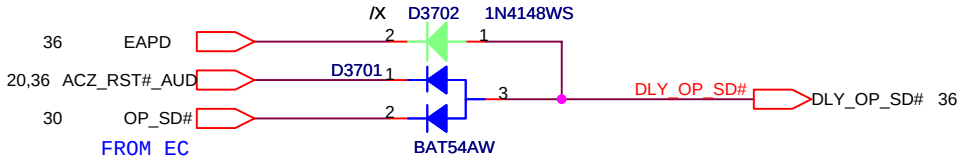


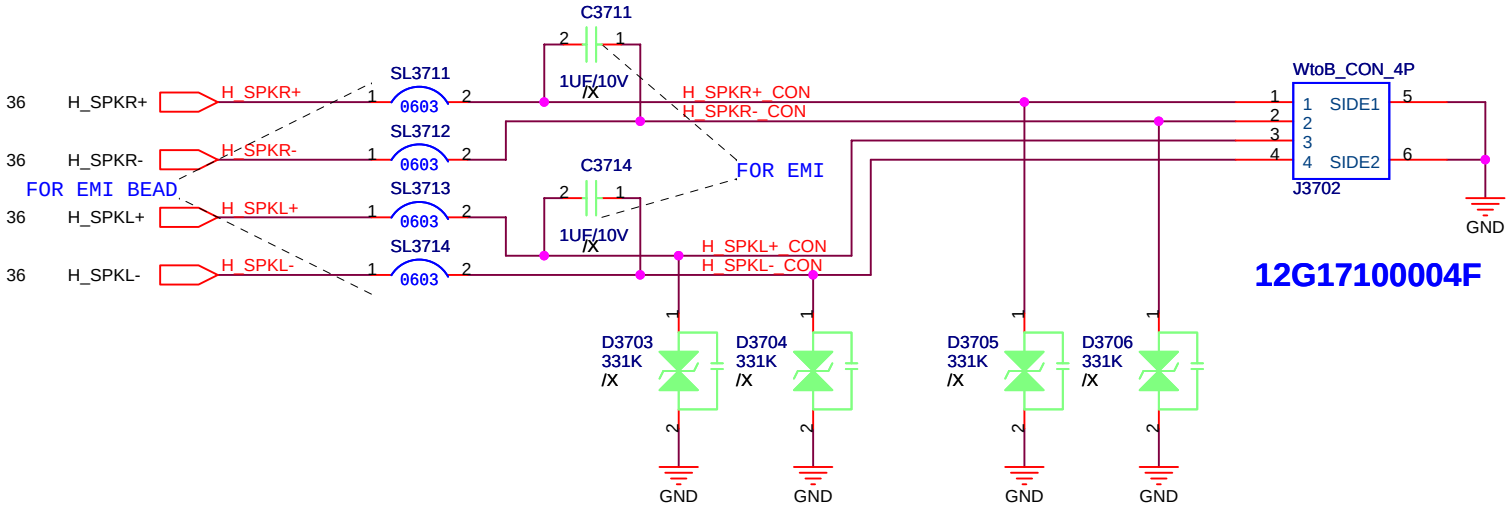




<Variant Name>
Title : CODEC ALC 269
ASUSTeK COMPUTER INC. NB2
Engineer: yun-feng_yan
Size: Custom
Project Name: N61Jv
Rev: 1.0
Date: Friday, December 11, 2009
Sheet 36 of 95

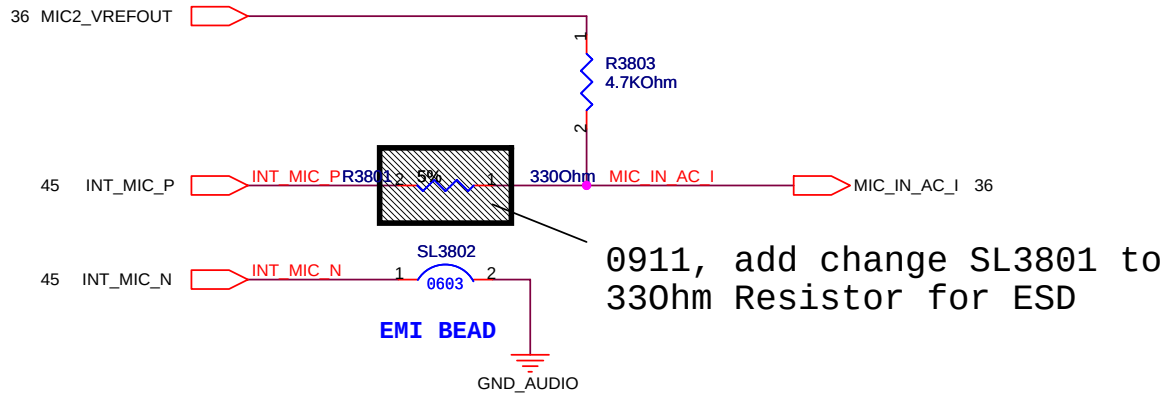
MUTE CONTROL





ASUSTeK COMPUTER INC. NB2	Title : AUDIO AMP		
	Engineer: yun-feng_yan		
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Friday, December 11, 2009	Sheet 37 of 95		

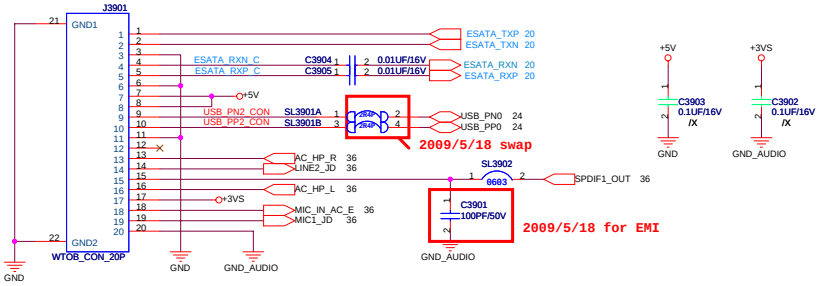
INTERNAL MICROPHONE



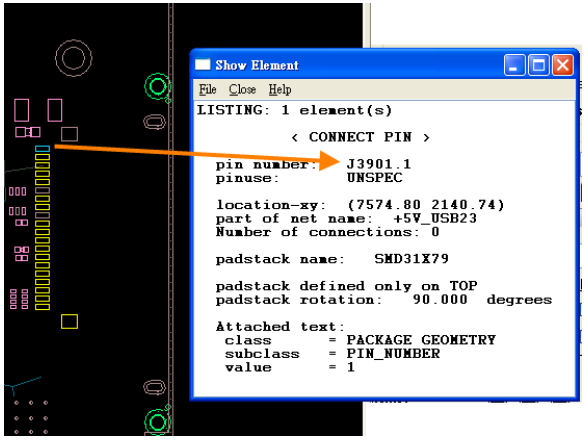
<Variant Name>

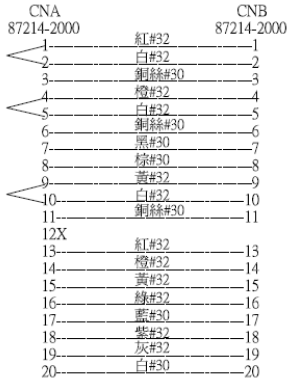
ASUSTeK COMPUTER INC. NB1	Title : MIC Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 38 of 95	

modify 0410

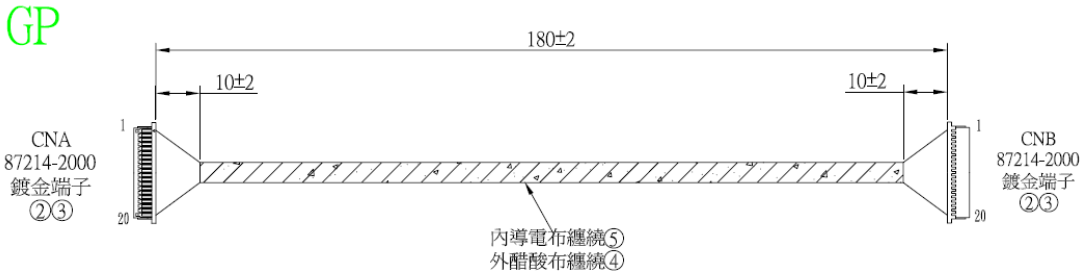


pin define

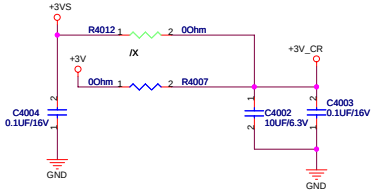


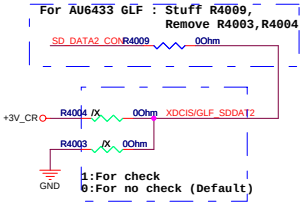


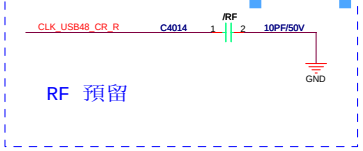
Follow U50 IO cable



ASUSTeK COMPUTER INC. NB1	Title : ****	
	Engineer: CH_Lin	
Size: C	Project Name: N61JA	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 39 of 95	

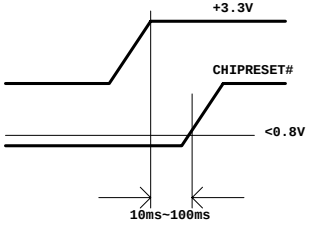


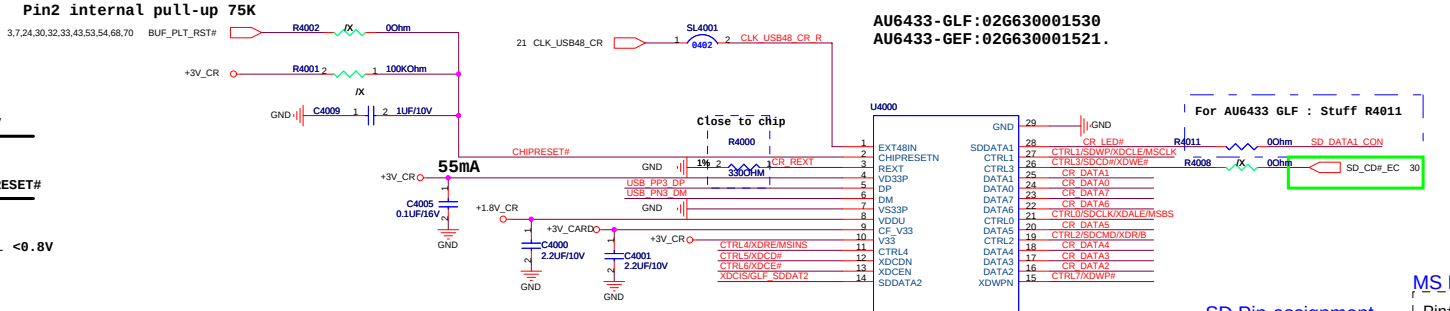




Pin2 internal pull-up 75K

Chip reset Timing:

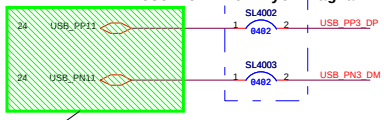




AU6433-GLF:02G630001530
AU6433-GEF:02G630001521.

02G630001530

Reserve R for Eye Diagram



0911, Follow Design Ip swap USB port 3 and Port 11

xD Pin-assignment

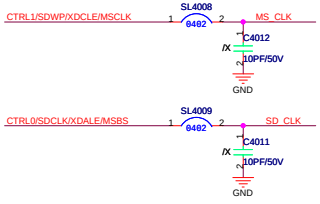
Pin#	PinName
Xd No. 0	CD
Xd No. 1	GND
Xd No. 2	R/-B
Xd No. 3	-RE
Xd No. 4	-CE
Xd No. 5	CLE
Xd No. 6	ALE
Xd No. 7	-WE
Xd No. 8	-WP
Xd No. 9	GND
Xd No.10	D0
Xd No.11	D1
Xd No.12	D2
Xd No.13	D3
Xd No.14	D4
Xd No.15	D5
Xd No.16	D6
Xd No.17	D7
Xd No.18	VCC

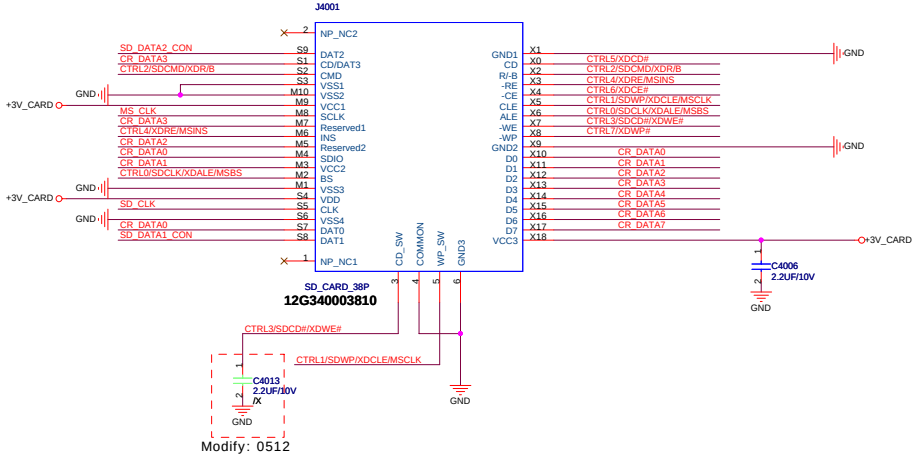
SD Pin-assignment

Pin#	PinName
SD No. 1	CD/DATA3
SD No. 2	CMD
SD No. 3	GND
SD No. 4	VDD
SD No. 5	CLK
SD No. 6	GND
SD No. 7	DATA0
SD No. 8	DATA1
SD No. 9	DATA2

MS Pin-assignment

Pin#	PinName
MS No. 1	GND
MS No. 2	BS
MS No. 3	DATA1
MS No. 4	SDIO/DATA0
MS No. 5	DATA2
MS No. 6	INS
MS No. 7	DATA3
MS No. 8	SCLK
MS No. 9	VCC
MS No.10	GND

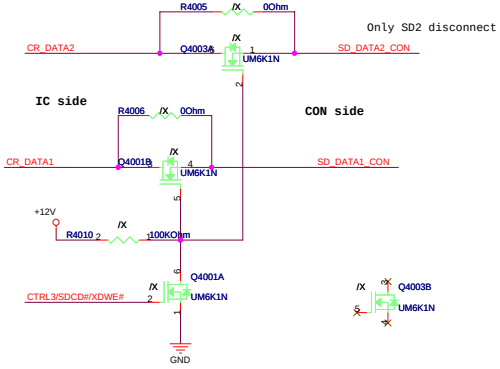




Modify: 0512

Fix MS Duo Adaptor short issue.
(SD_DAT1,SD_DAT2,XD_GND short,XD_CD# may be possible short)

For AU6433-GLF: No stuff All
For AU6433-GEF: Stuff Q4000,Q4001,Q4003,R4010



ASUSTeK COMPUTER INC. NB1	Title : AU6433	
	Engineer: yun-feng_yan	
Size: C	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 40 of 95	

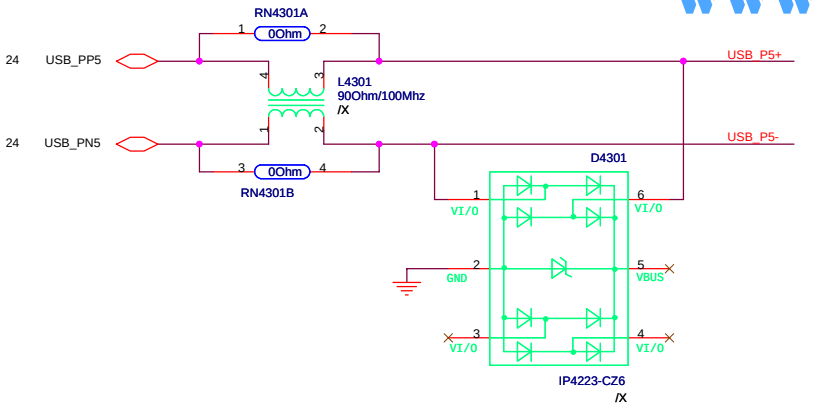
Main Board

ASUSTeK COMPUTER INC. NB4	Title : HMDI Switch		
	Engineer: yun-feng_yan		
Size: B	Project Name: N61Jv		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 41 of 95		

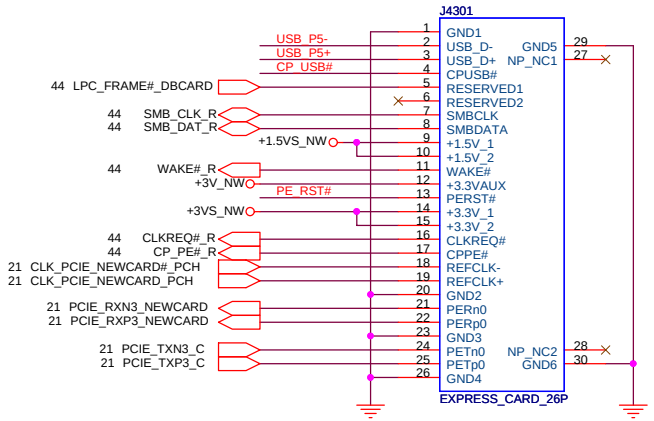
Main Board

ASUSTeK COMPUTER INC. NB4	Title : CB_****	
	Engineer: yun-feng_yan	
Size: A	Project Name: N61Jv	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 42 of 95	

Main Board

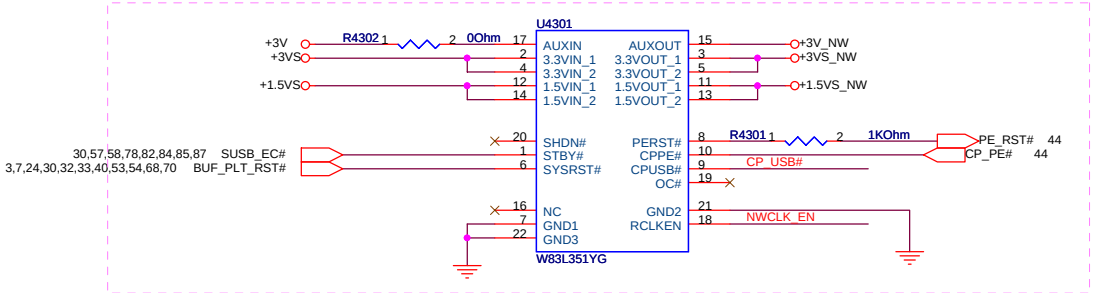


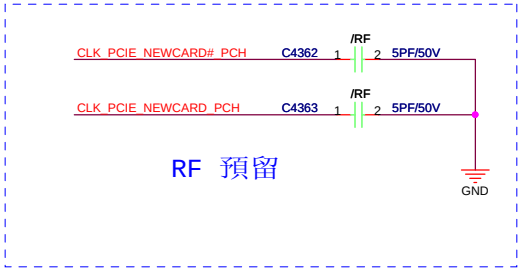
NewCard Header

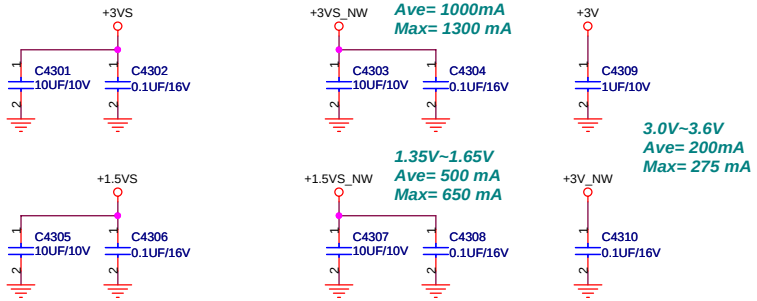


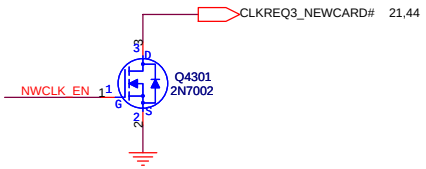
12G161300261

R2.00,item L9

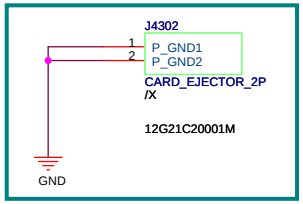








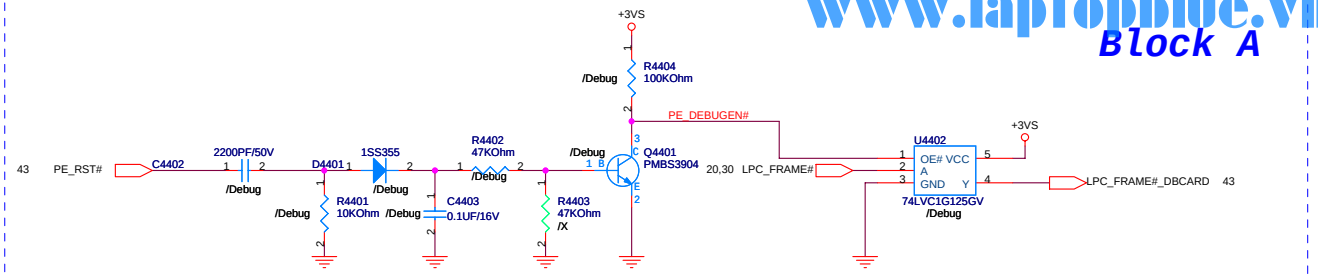
NewCard Ejecter



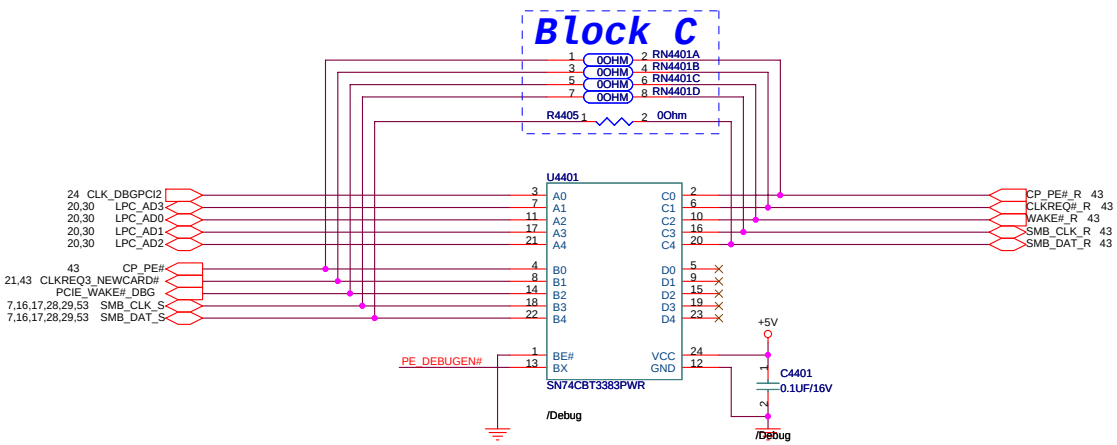
ASUSTeK COMPUTER INC. NB4	Title : CB_NewCard	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 43 of 95	

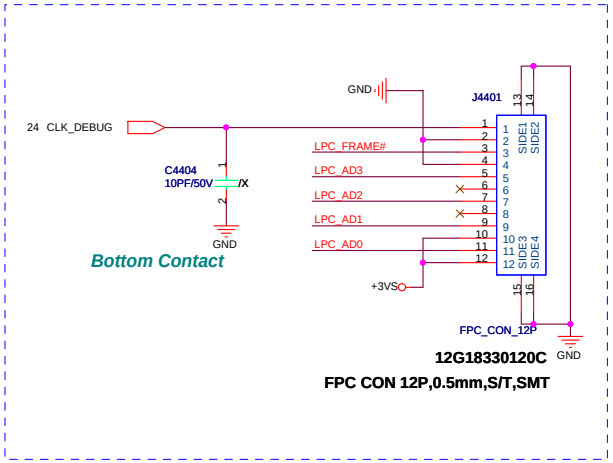
Main Board

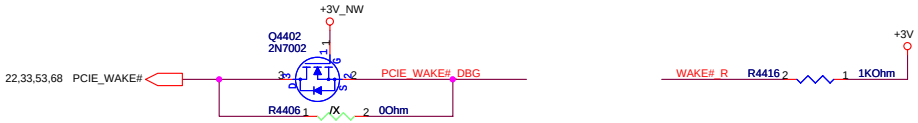
Block A



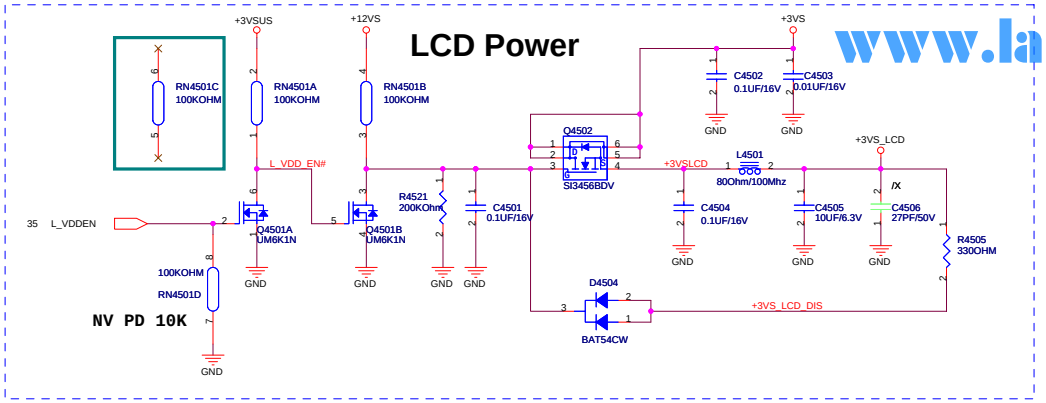
Block C

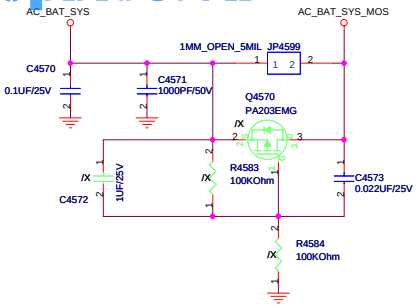


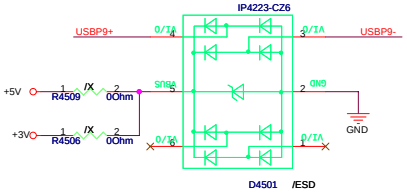


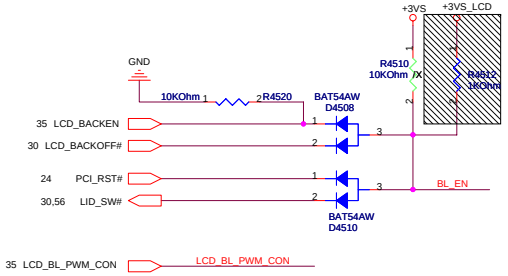


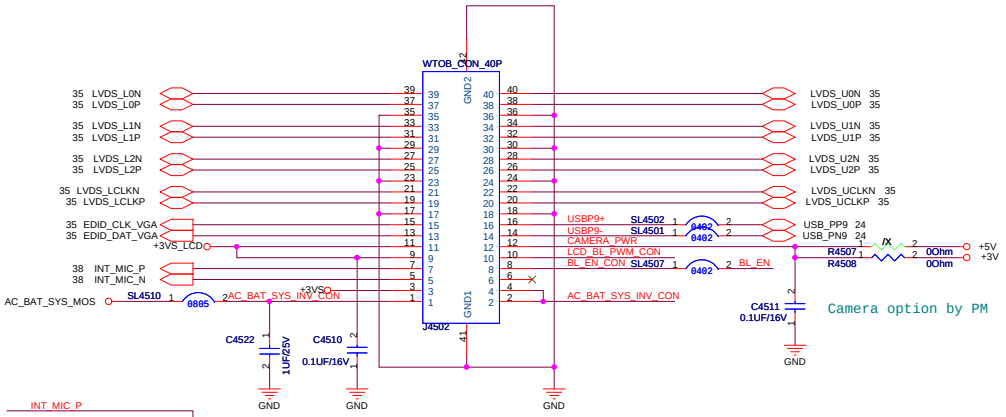
Title : BUG_Debug		
ASUSTeK COMPUTER INC. NB4	Engineer: yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 44 of 95	



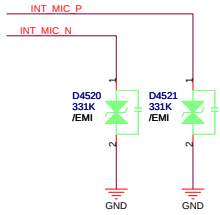






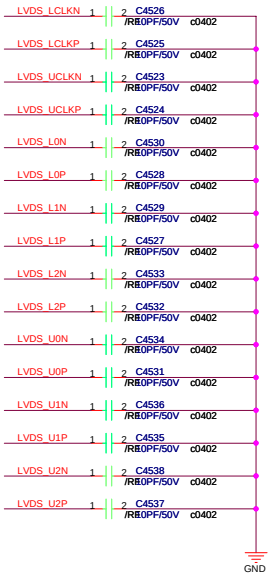


12G170010409

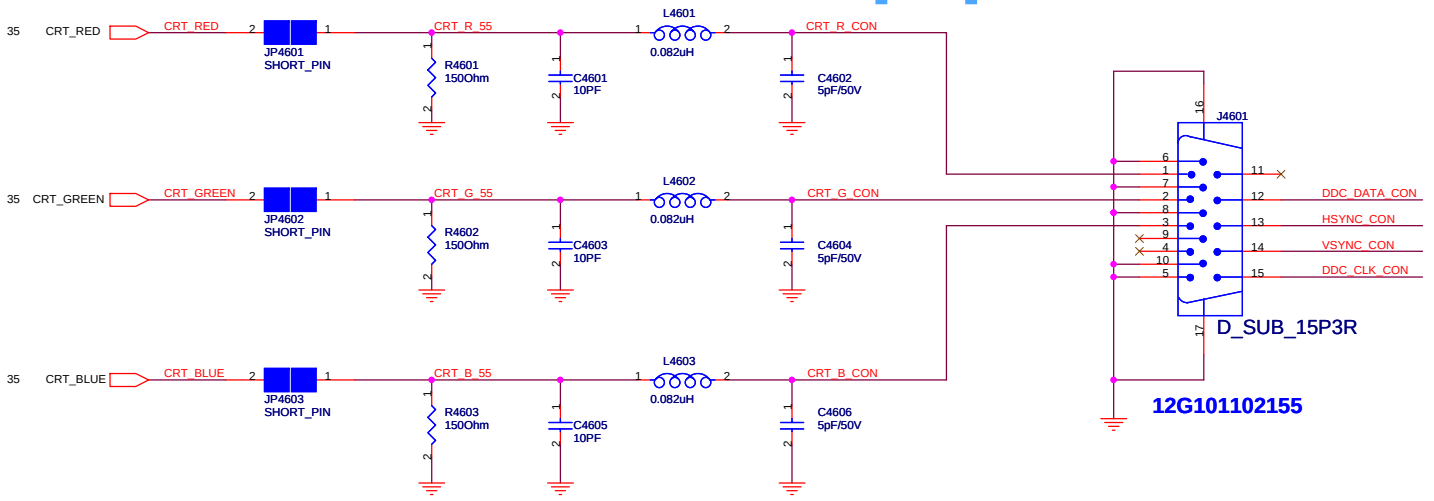


Camera option by PM

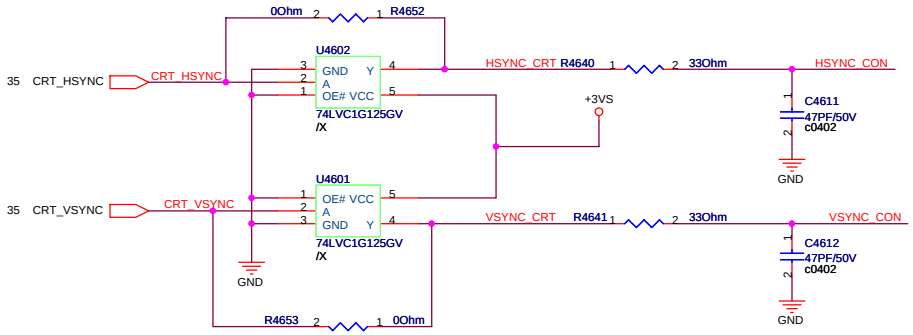
RF request
0723 modify

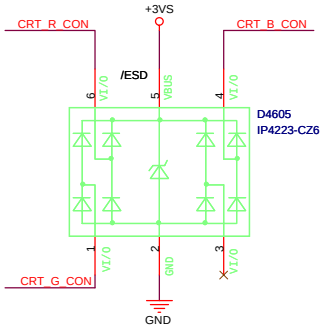


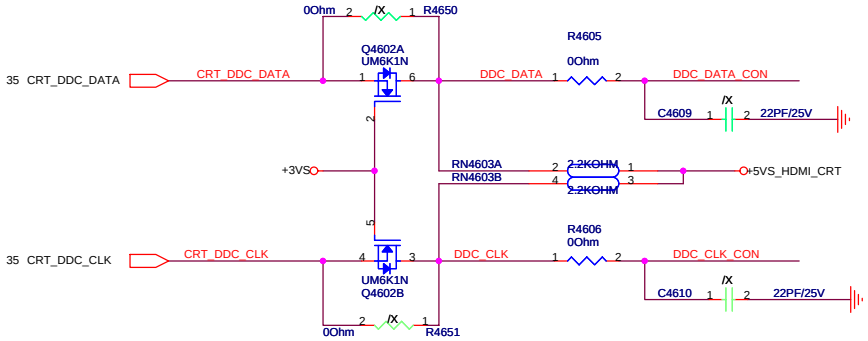
ASUSTeK COMPUTER INC. NB1	Title : LVDS	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 45 of 95	

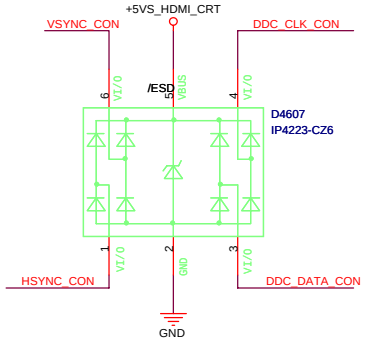


PLACE ESD Diodes near connector







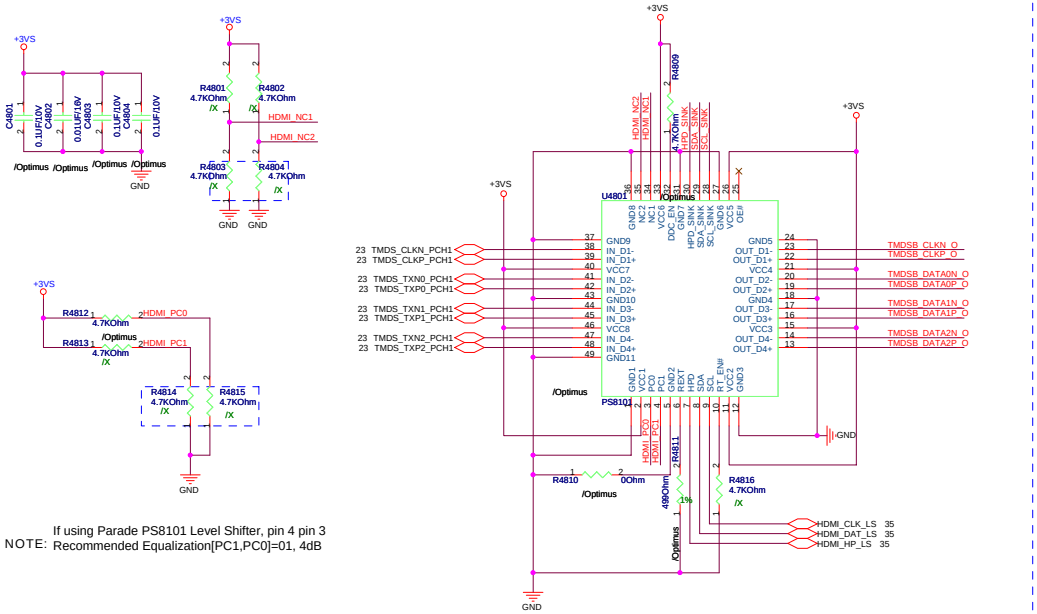


ASUSTeK COMPUTER INC. NB4	Title : CRT_D-Sub	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 46 of 95	

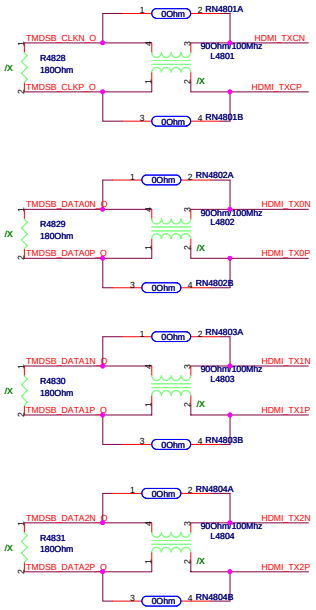
Main Board

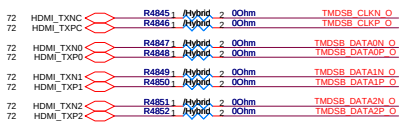
ASUSTeK COMPUTER INC. NB4	Title : Display Port	
	Engineer: Yun-feng_yan	
Size: A	Project Name: N61Jv	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 47 of 95	

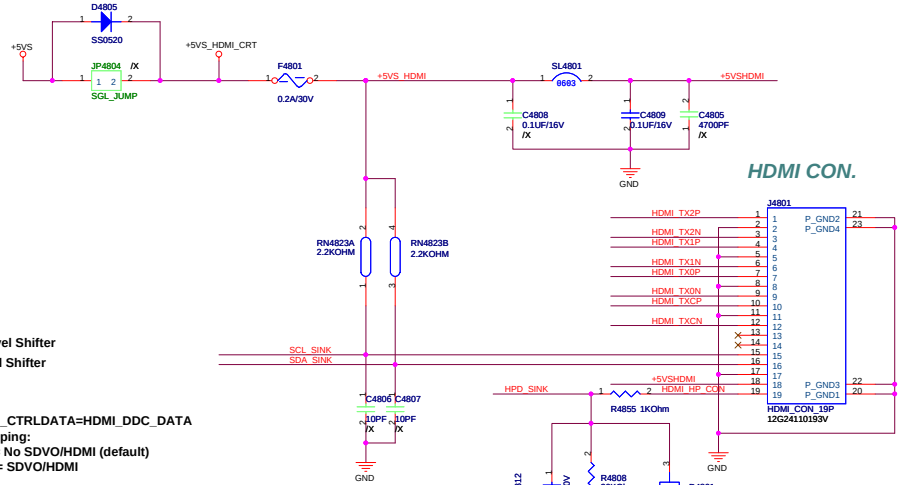
Optimus



NOTE: If using Parade PS8101 Level Shifter, pin 4 pin 3
Recommended Equalization[PC1,PC0]=01, 4dB



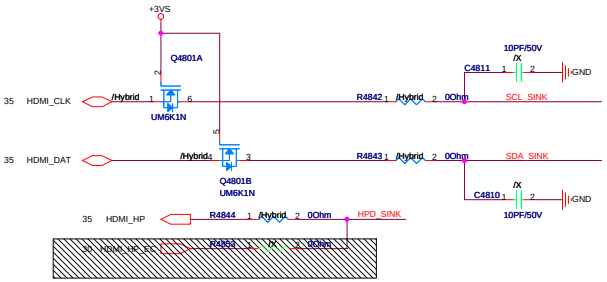




HDMI CON.

From Level Shifter
From Level Shifter

SDVO_CTRLDATA=HDMI_DDC_DATA
Strapping:
Low = No SDVO/HDMI (default)
High = SDVO/HDMI

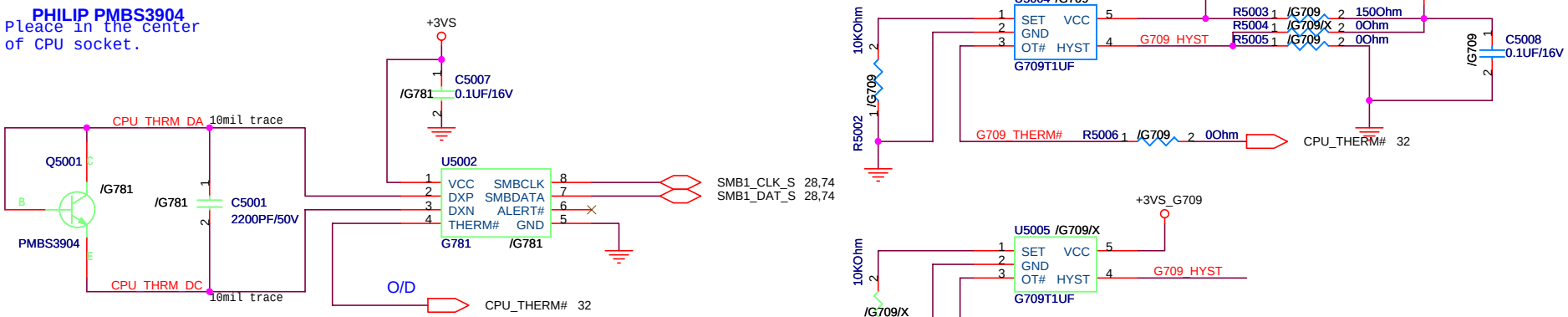


ASUSTeK COMPUTER INC	Title : HDMI		
	Engineer: Yun-feng_yan		
Size: Custom	Project Name: N61Jv		Rev: 1.0
Date: Friday, December 11, 2009	Sheet 48 of 95		

Main Board

ASUSTeK COMPUTER INC. NB4	Title : TV_****	
	Engineer: Yun-feng_yan	
Size: A	Project Name: N61Jv	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 49 of 95	

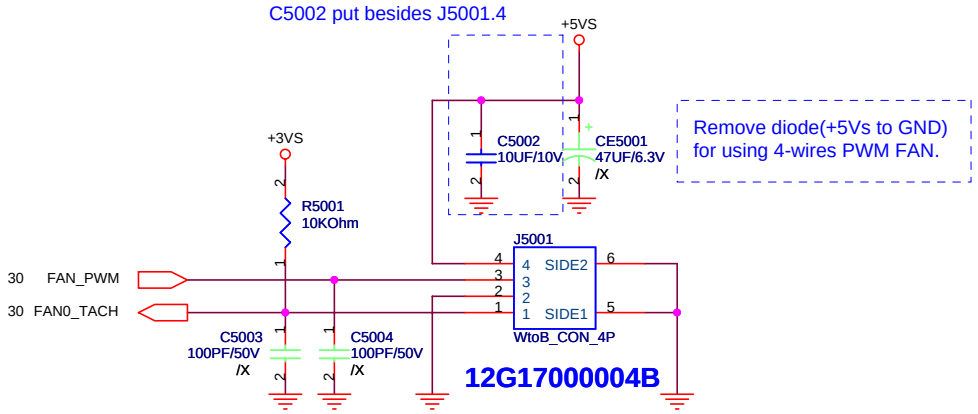
CPU Thermal Sensor



SMBUS addr=1001100x (9A)

U5002: Remote(Local) thermal sensor,use remote mode.

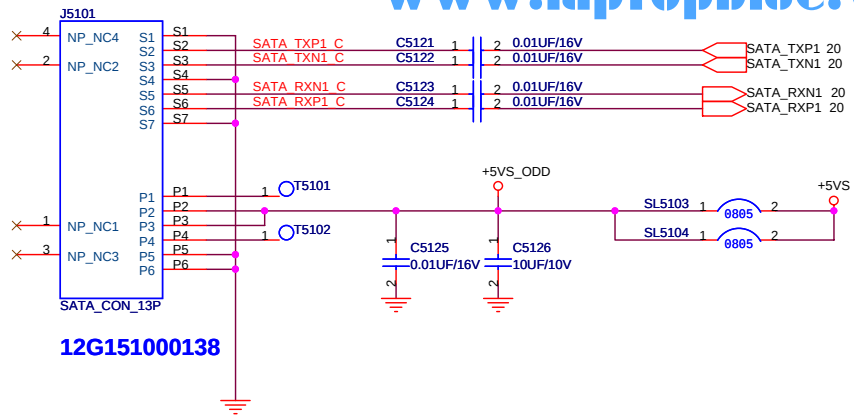
PWM Fan



ASUSTeK COMPUTER INC. NB4	Title : FAN_Fan & Sensor	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 50 of 95	

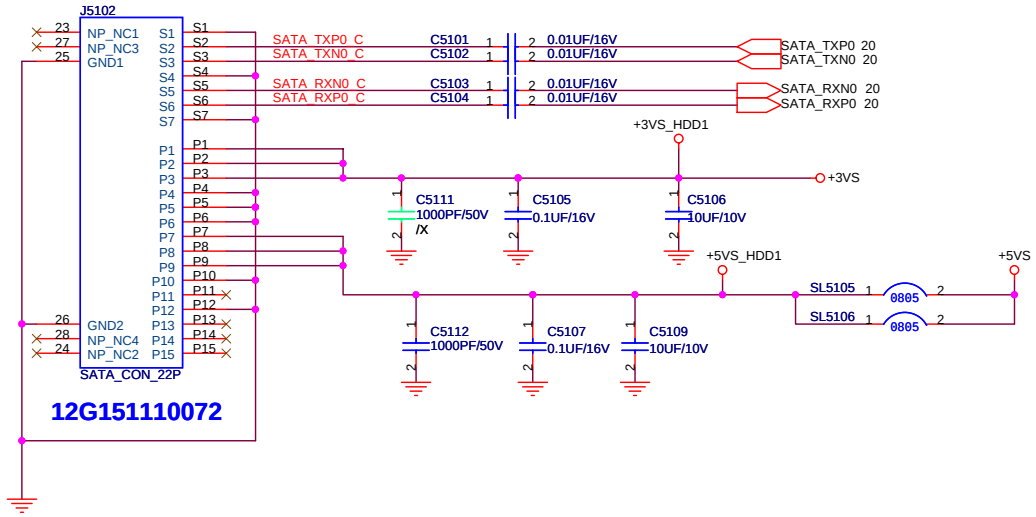
Main Board

ODD



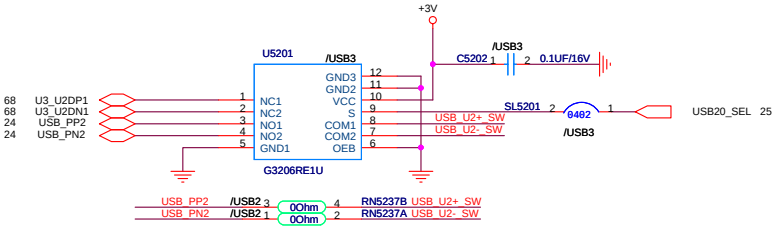
12G151000138

HDD

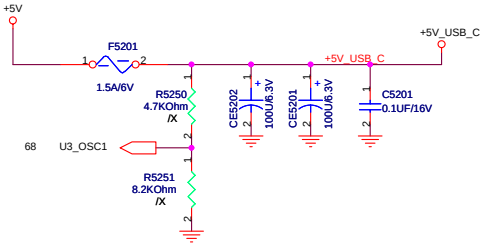


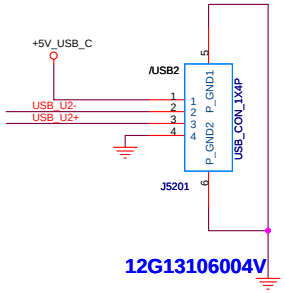
12G151110072

ASUSTeK COMPUTER INC. NB4	Title : HDD & ODD	
	Engineer: Yun-feng_yan	
Size: B	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 51 of 95	

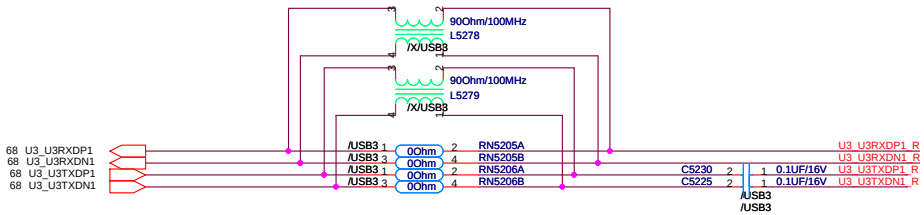


S ="L" COM=NC (USB3.0 chip)
S ="H" COM=NO (PCH)

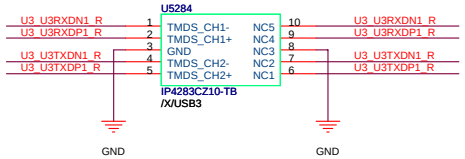


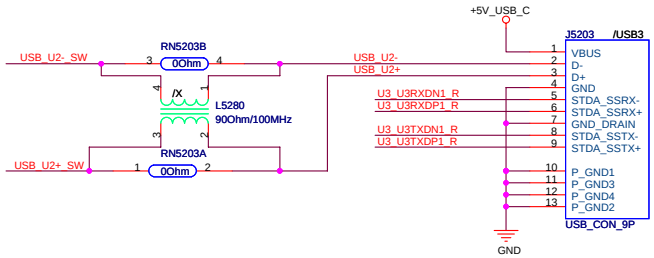


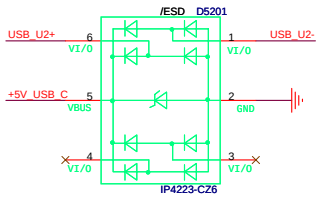
12G13106004V



USB3.0/USB 2.0 ESD-Protection





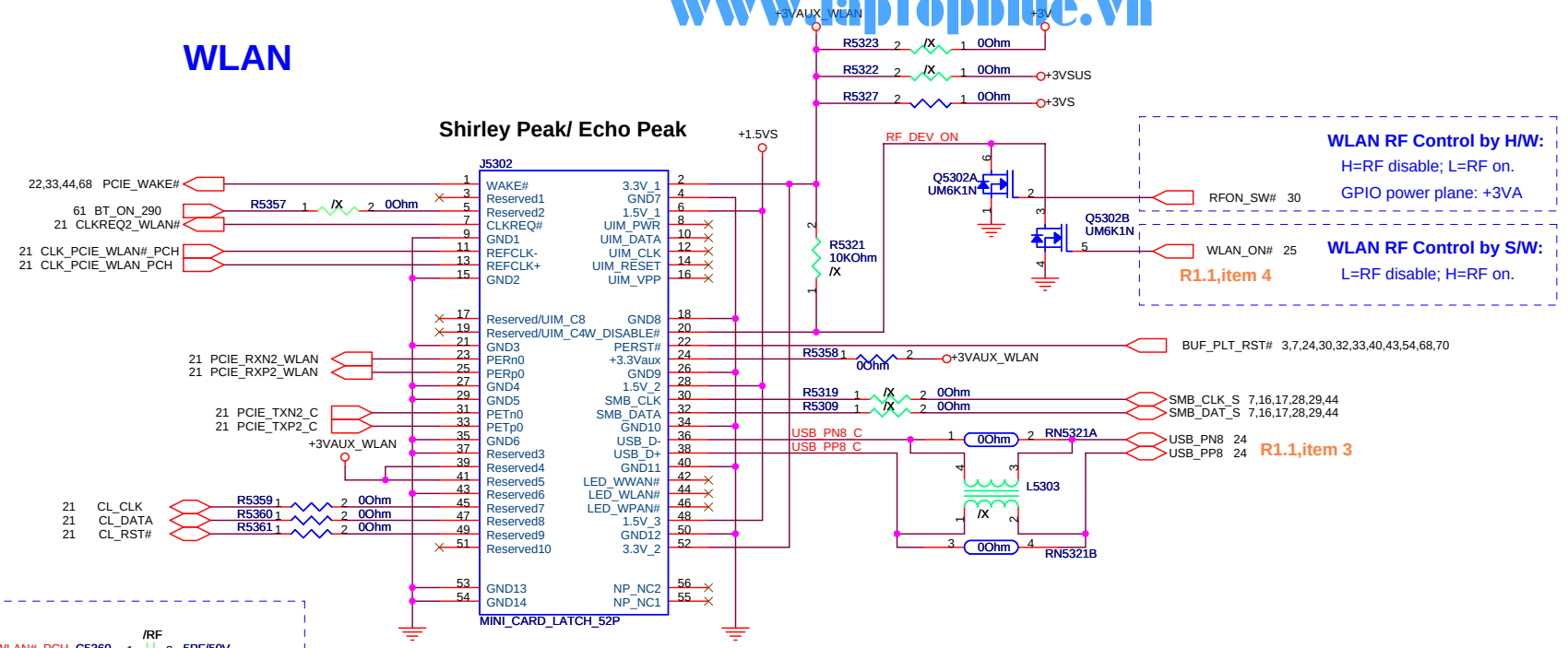


12G131010095----USB3
12G13106004V----USB2

ASUSTeK COMPUTER INC. NB4	Title : USB 3.0 Port *1	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 52 of 95	

WLAN

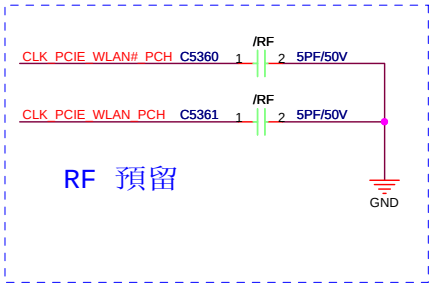
Shirley Peak/ Echo Peak

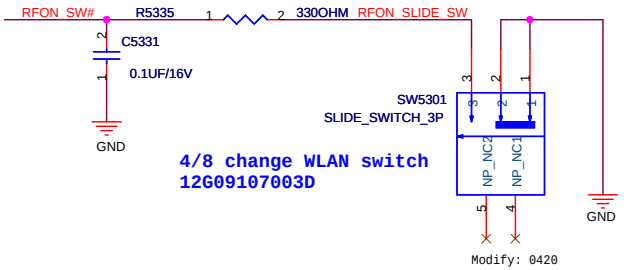


12G03000052B

footprint厂ノ 12G030000526
BOM い惠欣 12G03000052B もゃ

R1.1,item L1

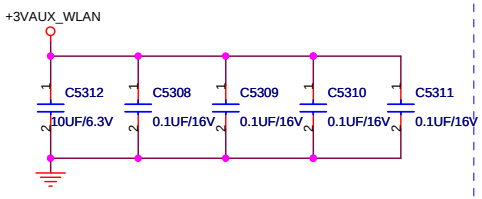




WLAN +3VAUX bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

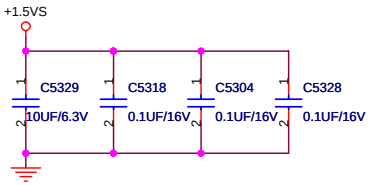
Place 10UF near +3VAUX_WLAN source side.



WLAN +1.5VS bypass capactor:

Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.

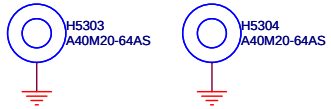


WLAN NUT for :

Minicard spec R1.2:

Full size card= 2pcs.

Half size card= 2pcs.

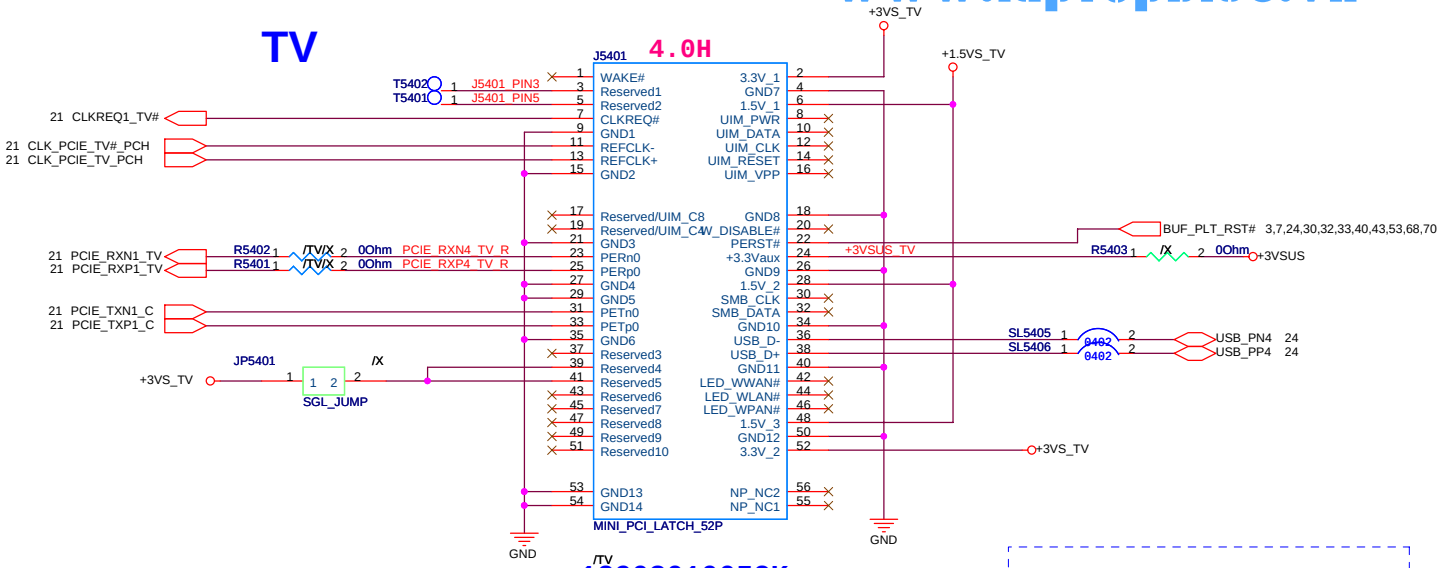


13G021029050

ASUSTeK COMPUTER INC. NB6	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 53 of 95	

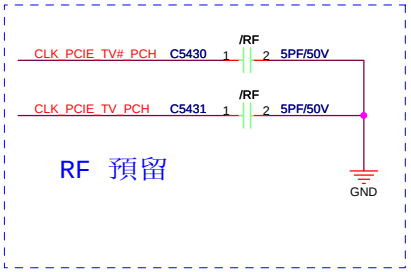
Title : MINICARD(WLAN)

TV



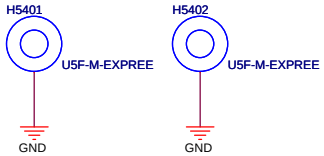
/TV

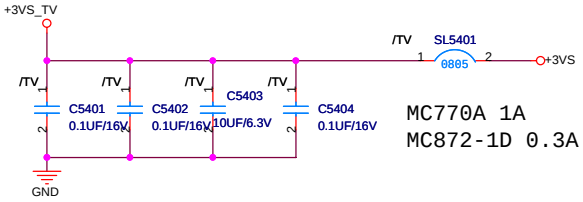
12G03010052K



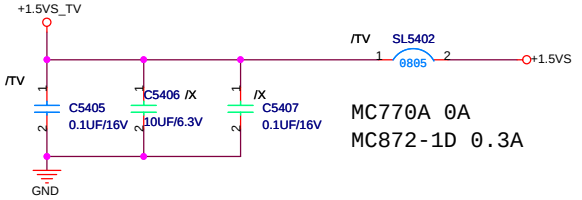
RF 預留

Module Name	Interface	Function
MC770A	USB	ATV+ DVB-T
MC872-1D	USB	DVB-T only





MC770A 1A
MC872-1D 0.3A



MC770A 0A
MC872-1D 0.3A

Parts Difference with Design IP

N52	Design IP
R5438	none
R5439	none
R5440	none
R5441	none
SL5403	none
SL5404	none
R5442	none
R5443	none
none	J5304
none	H5303
none	H5304

箇痙龟喷ノ

い惠ノ

簿 P65

Net Difference with Design IP

N52	Design IP
PCIE_RXN4_TV	PCIE_RXN5_TV
PCIE_RXP4_TV	PCIE_RXP5_TV
PCIE_TXN4_C	PCIE_TXN5_TV
PCIE_TXP4_C	PCIE_TXP5_TV
TV_ON_C	none
USB_PN6	USB_PN6_TV
USB_PP6	USB_PP6_TV

箇痙龟喷ノ

ASUSTeK COMPUTER INC. NB1

Title : TV TUN / 3G

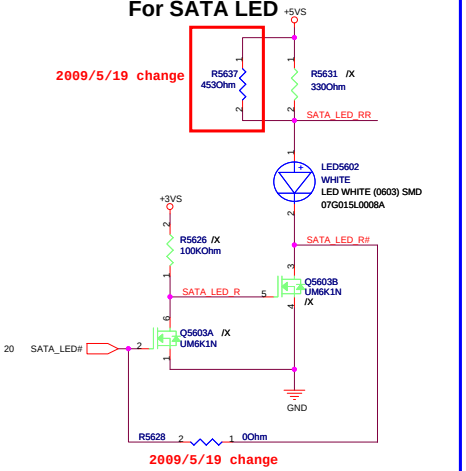
Engineer: Yun-feng_yan

Size	Project Name	Rev
Custom	N61Jv	1.0

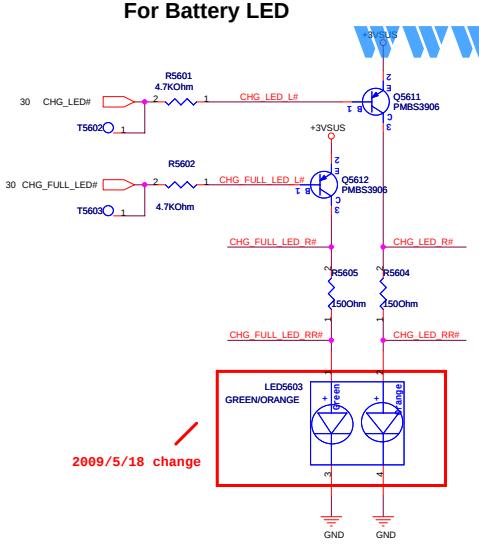
Date: Tuesday, December 15, 2009 Sheet 54 of 95

ASUSTeK COMPUTER INC. NB4	Title : SIO_****		
	Engineer: Yun-feng_yan		
Size: A	Project Name: N61Jv		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 55 of 95		

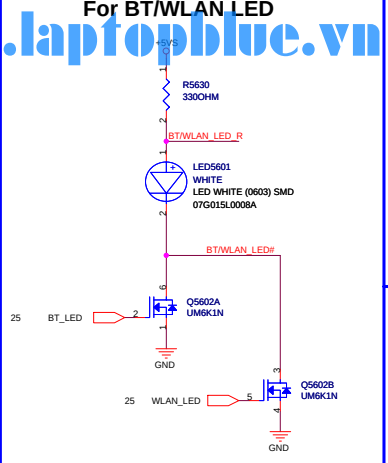
For SATA LED



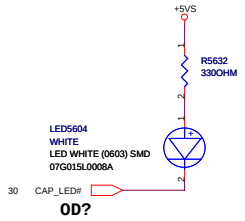
For Battery LED



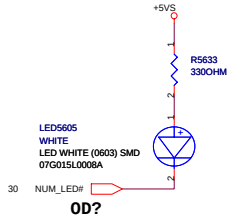
For BT/WLAN LED



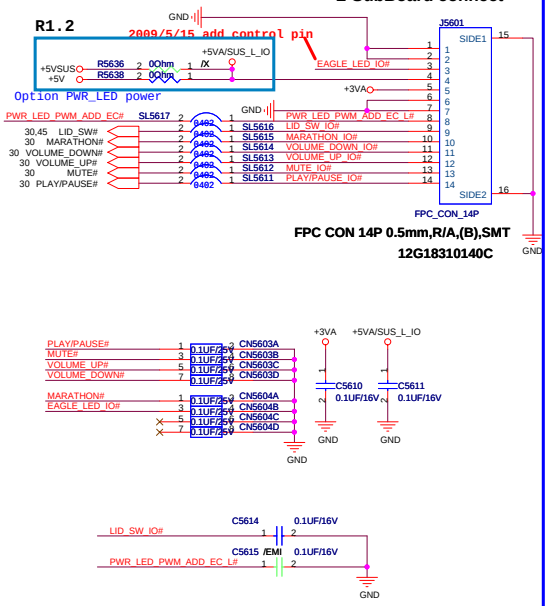
For Caps. Lock



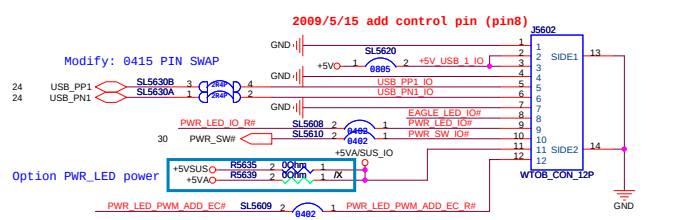
For NUM. Lock



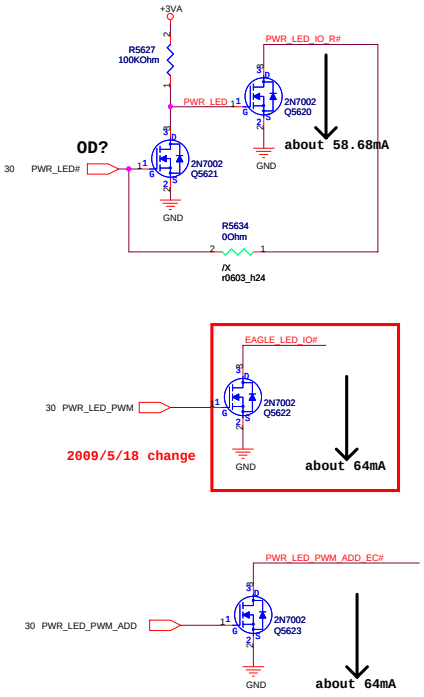
L-SubBoard connect

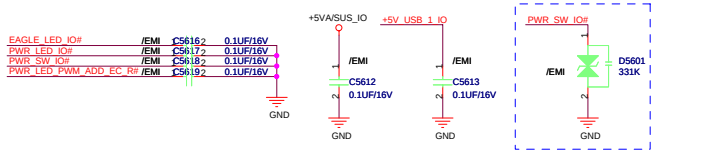


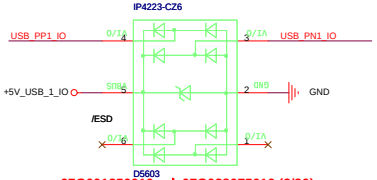
R-SubBoard connect



For PWR LED





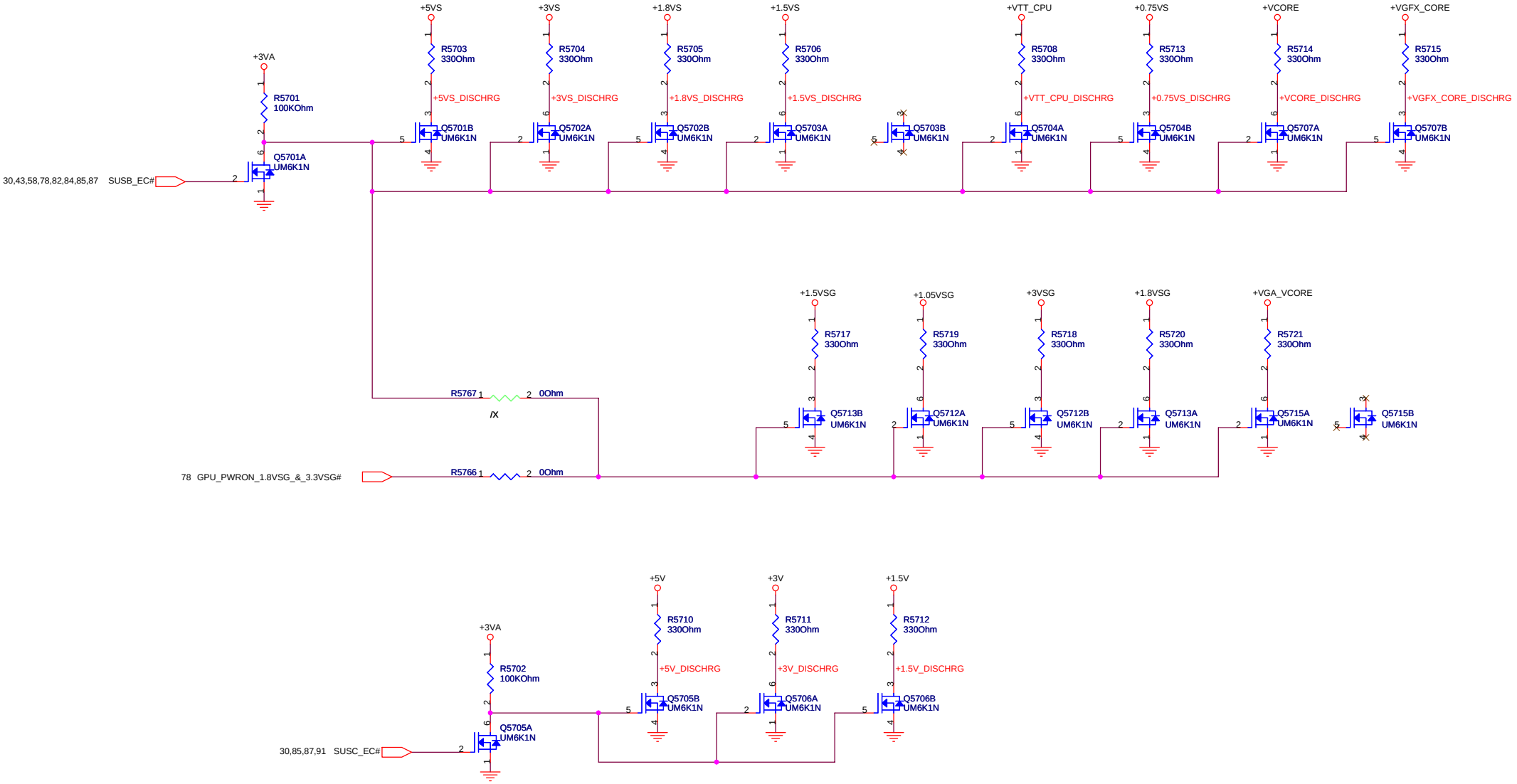


07G001250010 ﻧ 07G028075010 (3/30)

ASUSTeK COMPUTER INC. NB1	Title : LED & SW	
	Engineer: Yun-feng_yan	
Size: C	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 56 of 95	

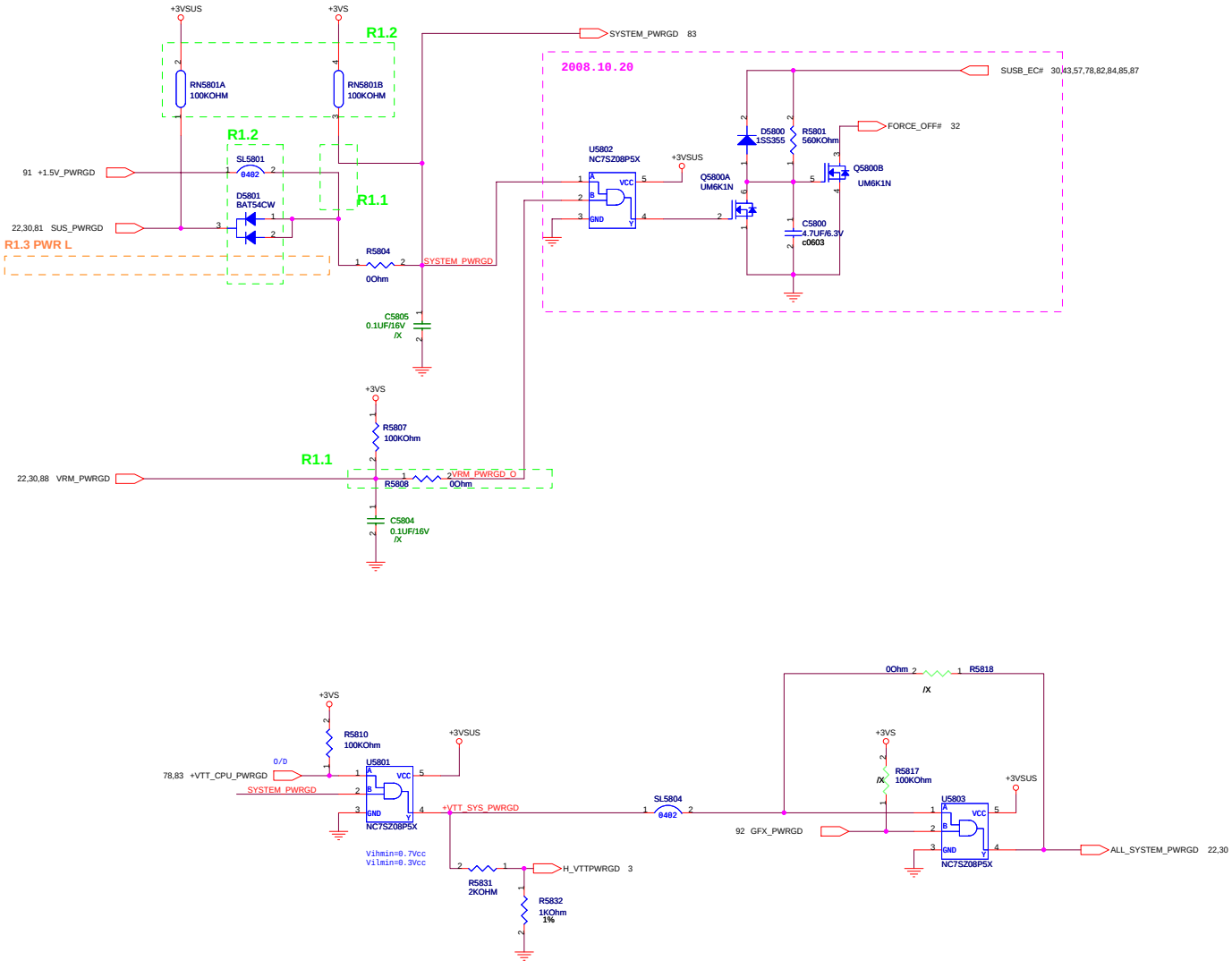
Remove +2.5Vs is for ATI GFX

Main Board



ASUSTeK COMPUTER INC. NB4	Title : DSG_Discharge	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 57 of 95	

POWER GOOD DETECTER



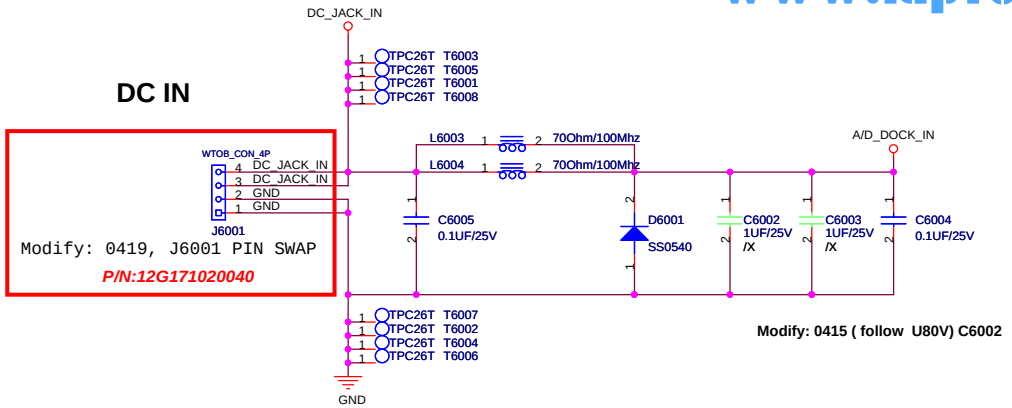
2008-08-04,James Wu add.

ASUSTeK COMPUTER INC. NB3	Title : POWER_PROTECT	
	Engineer: Yun-feng_yan	
Size: C	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 58 of 95	

Main Board

ASUSTeK COMPUTER INC. NB4	Title : DJ **** Engineer: CH_Lin	
Size: C	Project Name: N61JA	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 59 of 95	

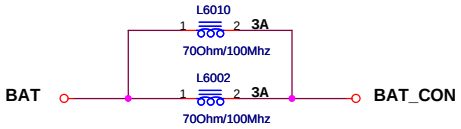
DC IN



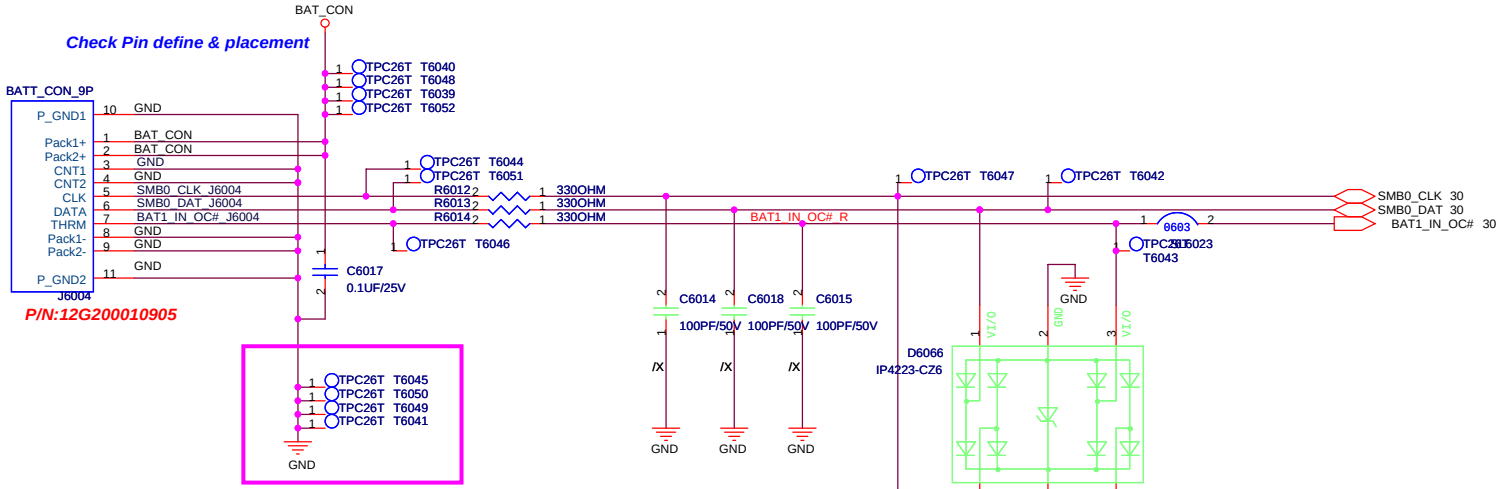
Modify: 0419, J6001 PIN SWAP

P/N:12G171020040

Modify: 0415 (follow U80V) C6002



BAT IN



P/N:12G200010905

07G001250010 э 07G028075010 (3/30)

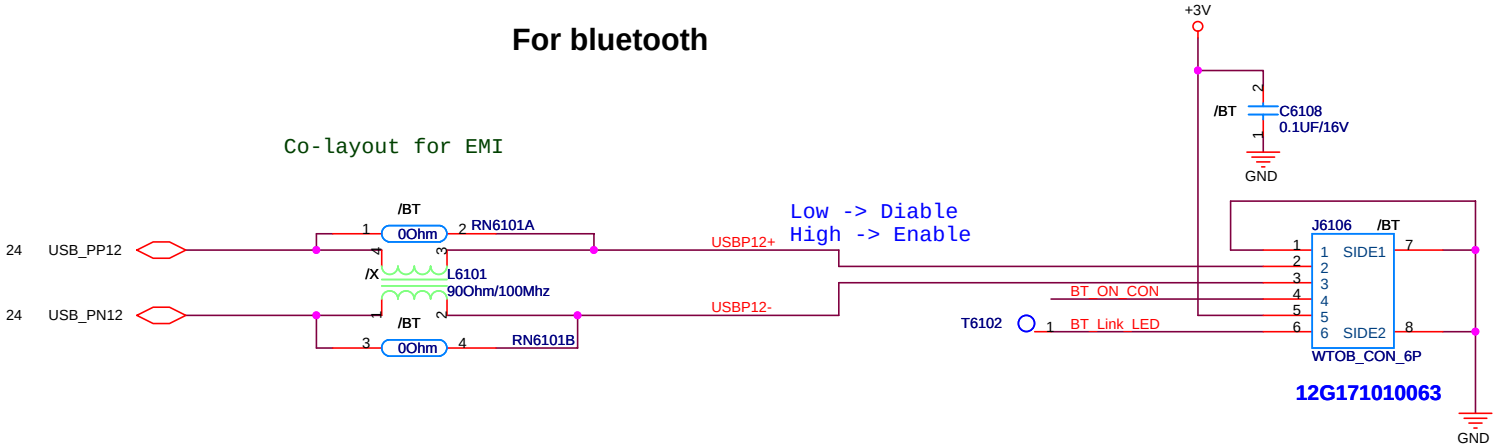
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 60 of 95	

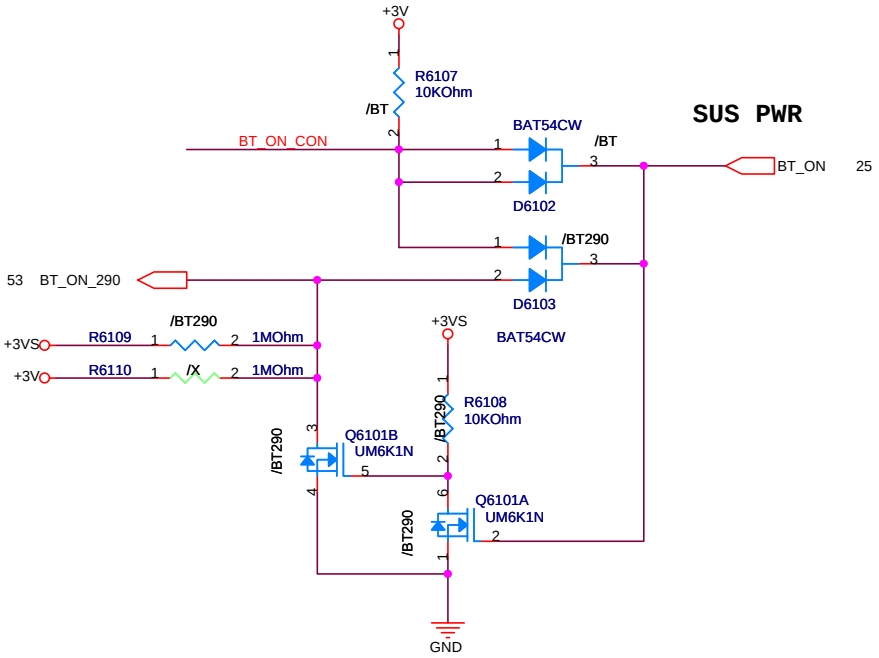
Bluetooth Conn.

For bluetooth

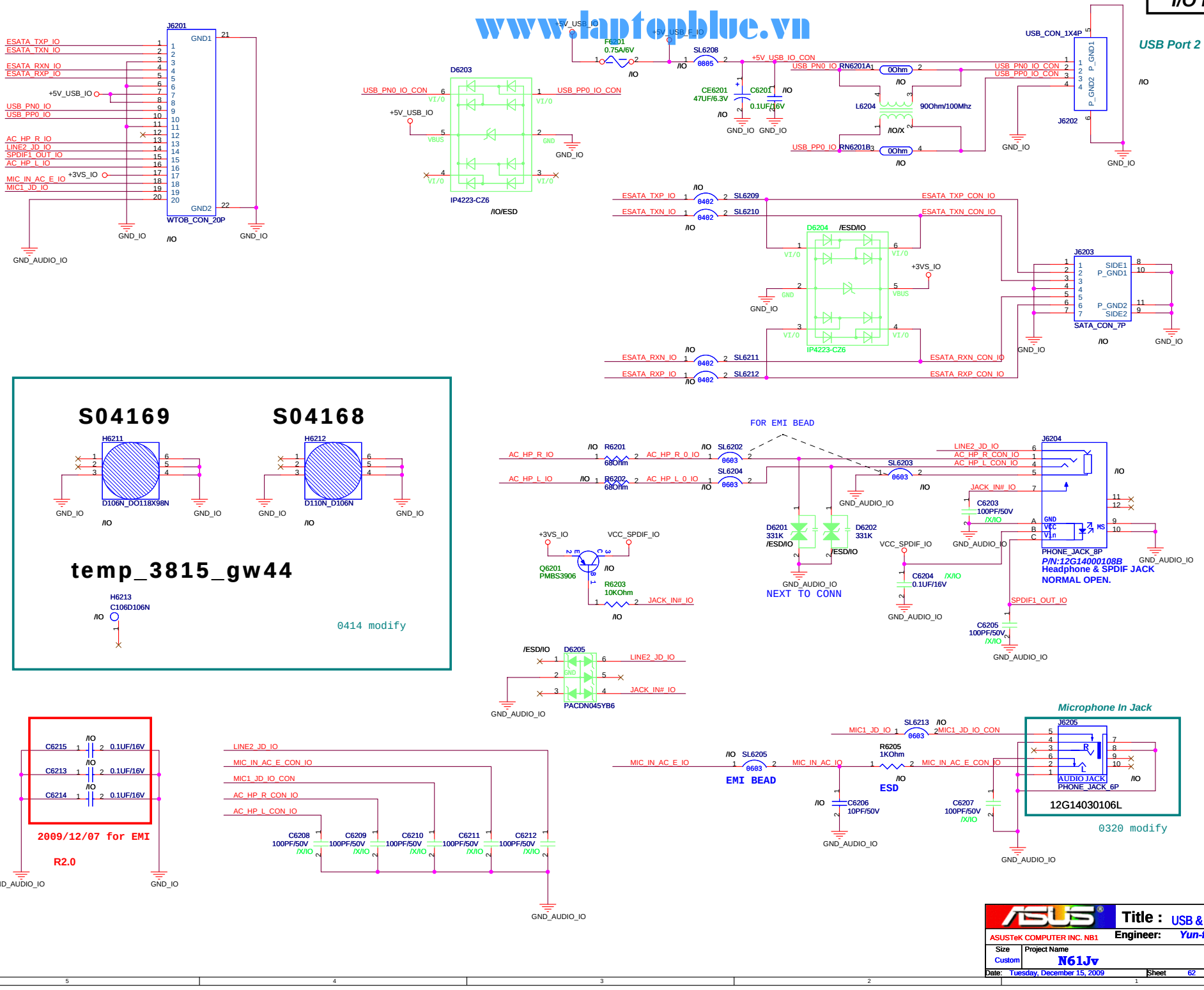
Co-layout for EMI



SUS PWR

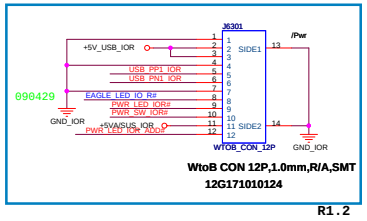


ASUSTeK COMPUTER INC. NB1	Title : BT	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 61 of 95	



ASUSTeK COMPUTER INC. NB1	Title : USB & Audio Jack	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 62 of 95	

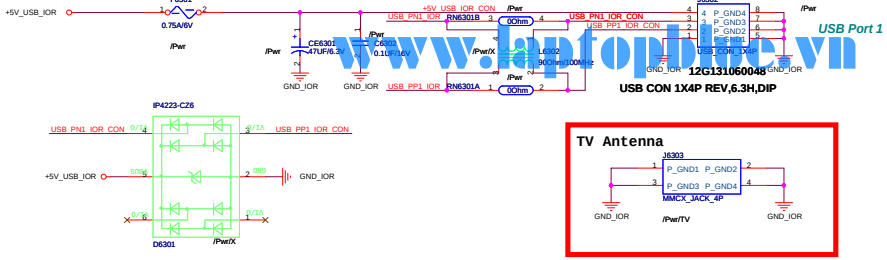
POWER BOARD



WtoB CON 12P,1.0mm,R/A,SMT

12G171010124

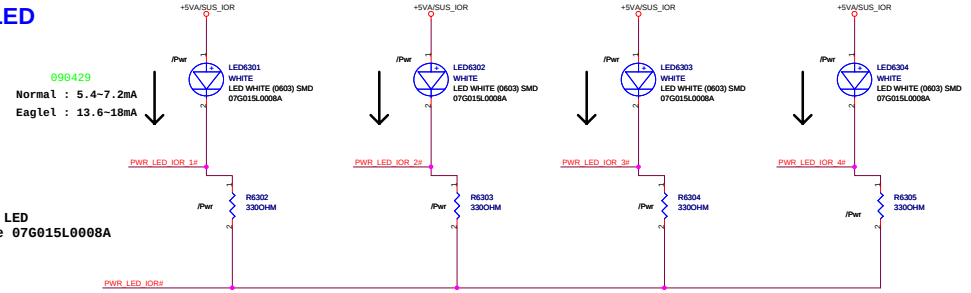
R1.2



TV Antenna

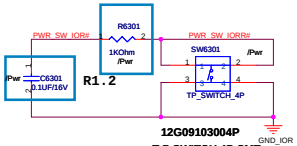
0518 change to P/N:14G152231000

Power LED



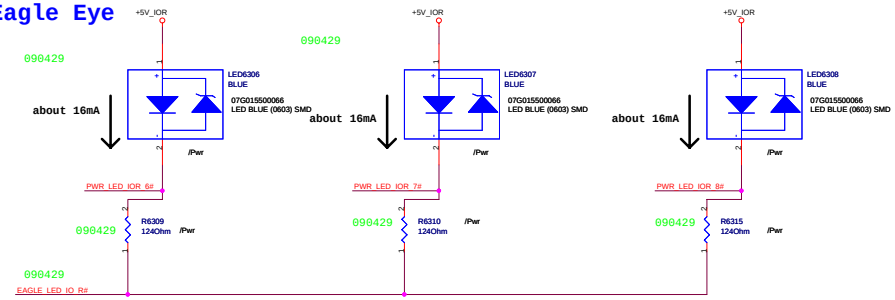
R2.1
ALL POWER LED
P/N change 07G015L0008A

POWER SW

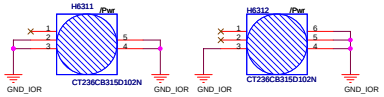


12G09103004P
T.P SWITCH 4P SMT

Eagle Eye



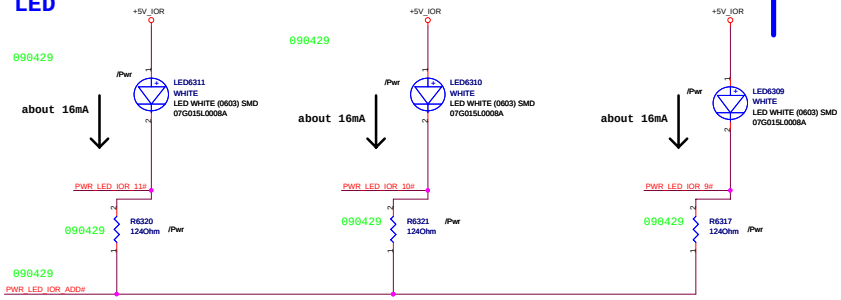
A: S04172 B: S04173

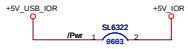


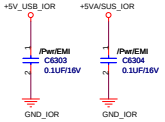
temp_5824_fh05

R1.2

ADD POWER LED

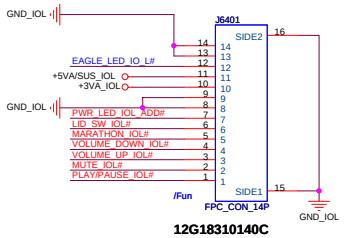






FUNCTION BOARD

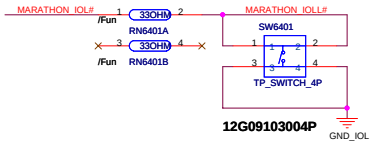
2009/5/18 swap



12G18310140C

FPC CON 14P 0.5mm,R/A,(B),SMT

MARATHON switch

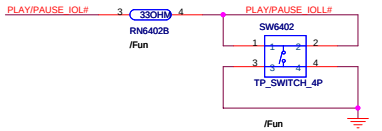


12G09103004P

T.P SWITCH 4P SMT

/Fun

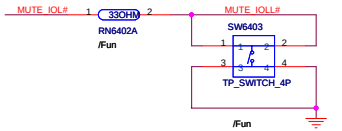
PLAY/PAUSE switch



12G09103004P

T.P SWITCH 4P SMT

MUTE switch



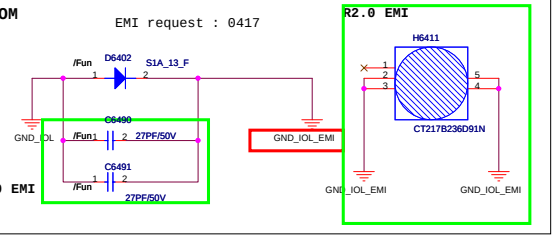
12G09103004P

T.P SWITCH 4P SMT

R1.2

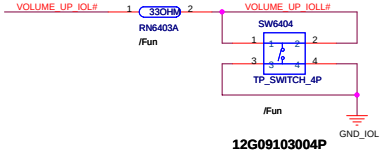
R1.1 BOM

EMI request : 0417



2009/5/18 change for factory

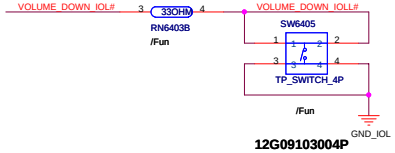
VOLUME UP switch



12G09103004P

T.P SWITCH 4P SMT

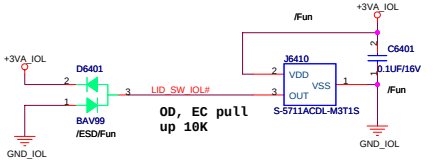
VOLUME DOWN switch

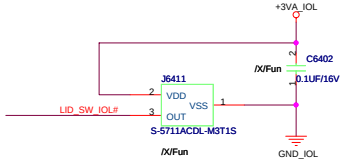


12G09103004P

T.P SWITCH 4P SMT

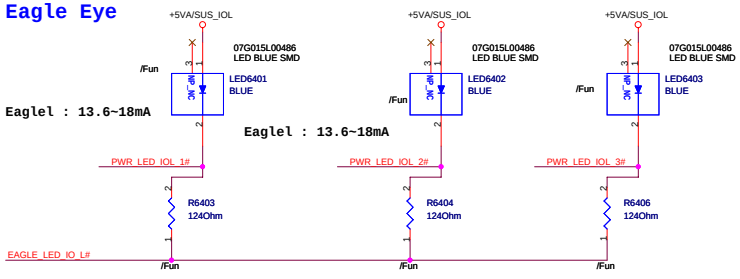
Lid Switch



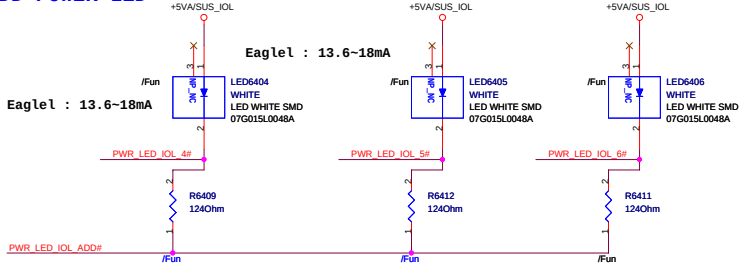


R2.1 LED chang 07G015L0048A

Eagle Eye

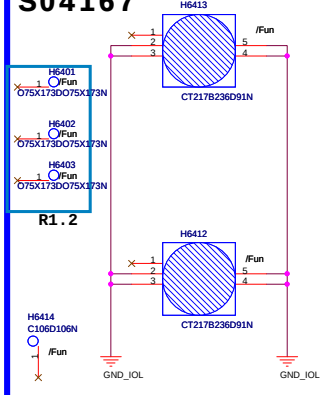


ADD POWER LED



S04167

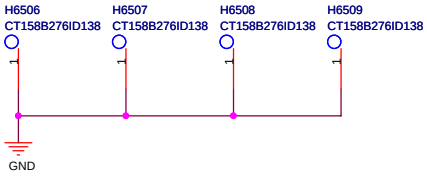
2009/5/18 for ME



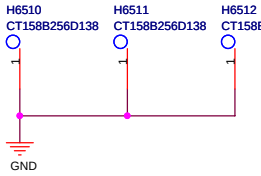
R1.2

ASUSTeK COMPUTER INC. NB1	Title : FUNCTION BOARD	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
Date: Tuesday, December 15, 2009	Sheet 64 of 95	

CPU (F : S04153)



GPU (G : S04170)

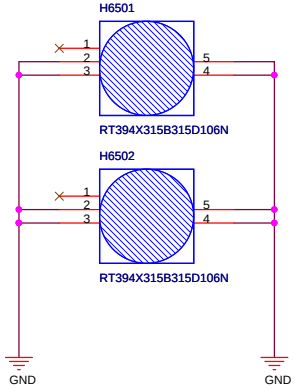


Modify: 0414

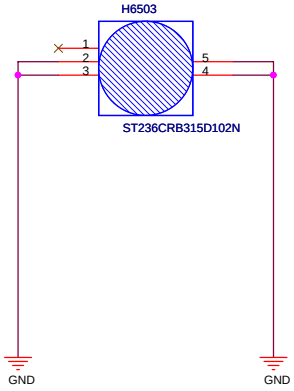
HOLD

Modify: 0415

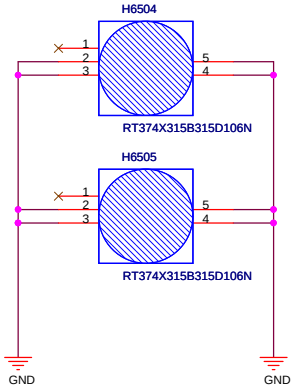
A: S04148



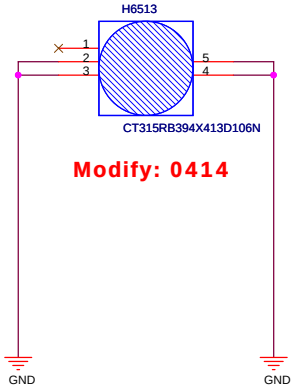
C: S04150



E: S04152

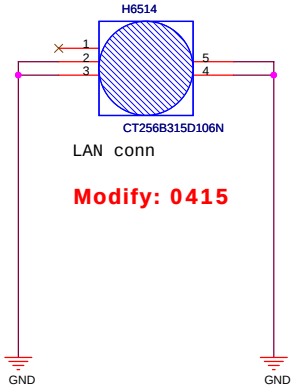


H: S04171



Modify: 0414

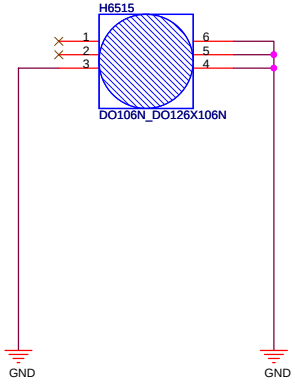
K: S04157



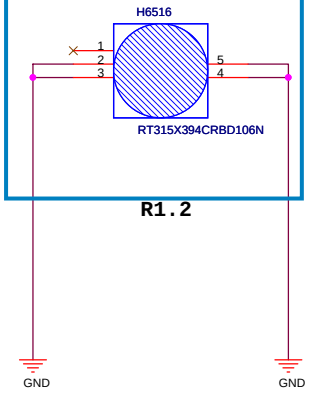
LAN conn

Modify: 0415

L: S04158

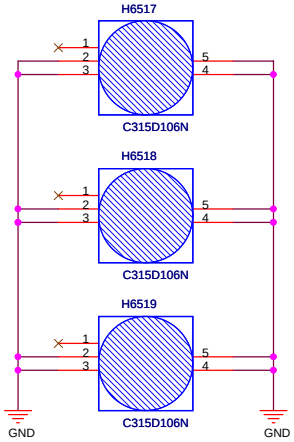


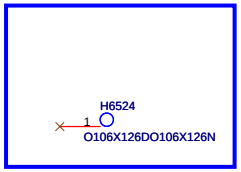
M: S04159



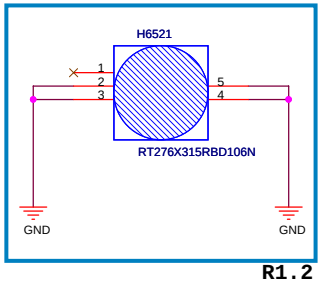
R1.2

N: S04160



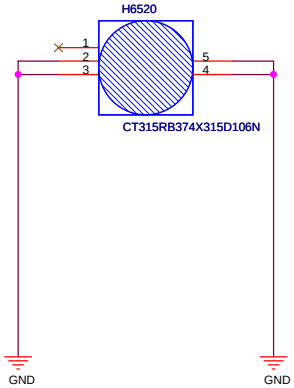


090505 Ellipse



R1.2

O: S04161



ASUSTeK COMPUTER INC. NB1

Title : NUT

Engineer: Yun-feng_yan

Size	Project Name	Rev
Custom	N61Jv	1.0

Date: Sunday, November 15, 2009 Sheet 65 of 95

ASUSTeK COMPUTER INC. NB4	Title : ESA_ESATA		
	Engineer: Yun-feng_yan		
Size: A	Project Name: N61Jv		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 66 of 95		

ASUSTeK COMPUTER INC. NB4	Title : PCH_XDP, ONFI		
	Engineer: *Yun-feng_yan*		
Size: A	Project Name: **N61Jv**		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 67 of 95		

PCI Express Interface
trace最大線長為12.5cm(6 inches).

(1)USB3.0 Interface trace最大線長為10cm(4 inches).
(2)USB Interface differential trace torlerence = 0.12mm(5 mail).

Power on Reset.

從南橋找一根可以發SMI的GPI pin, PWR Plate is Main PWR.

可以接受外部輸入48MHz Clock.
若要拉板子上的Clock,
請參考USB3.0 datasheet.

Close to USB IC

Close to P12

P12腳N12 Layout,
叫叭ㄆ把○NEC Layout guide_Page31.

0.3B Beta

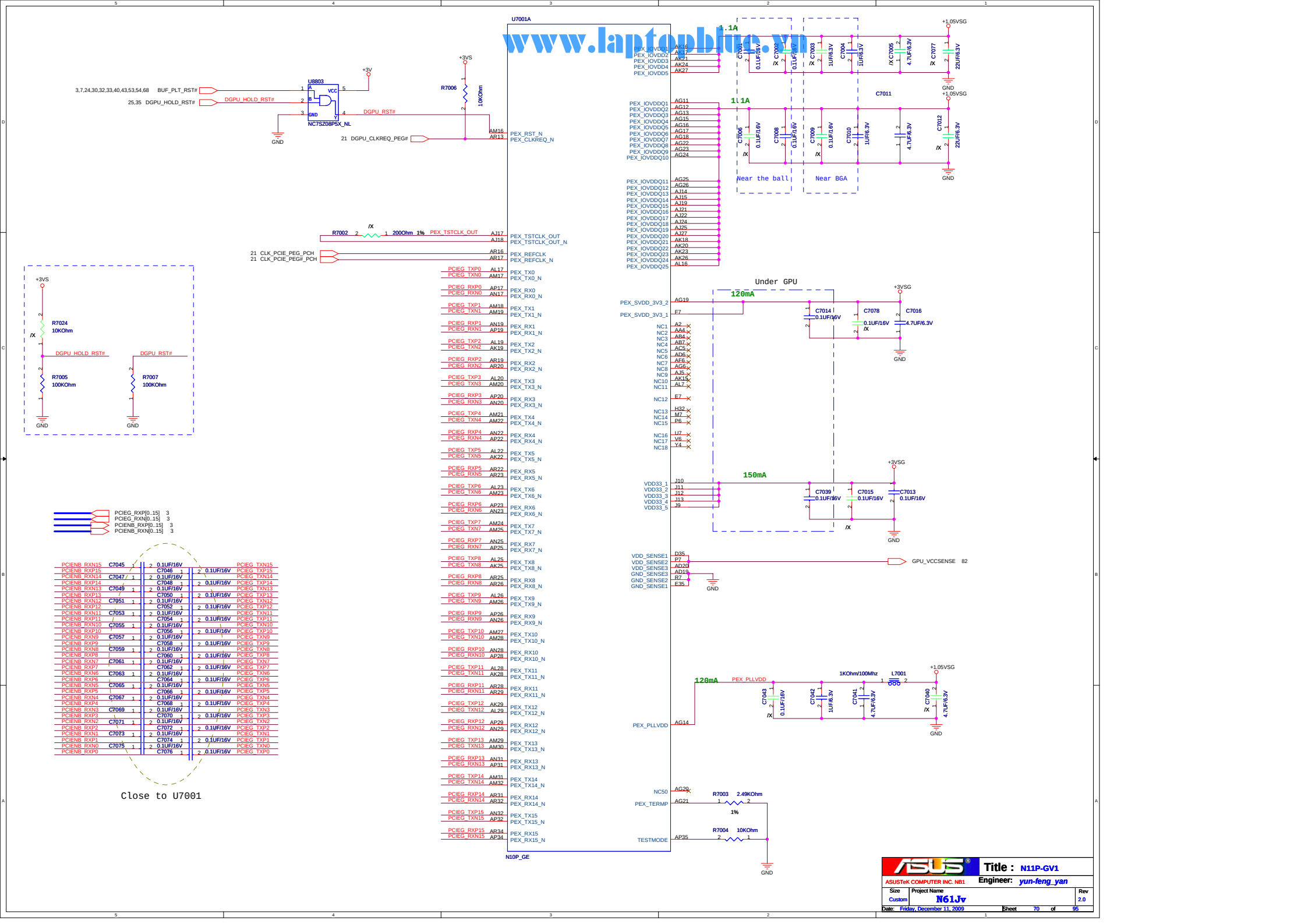
Standard Circuit	
USB3.0	uPD720200
REV.	U3_03B BETA

UPD720200
/X/UPD720200

Title : USB 3.0_NEC
ASUSTeK COMPUTER INC. NB4
Engineer: Yun-feng_yan
Size: Custom
Project Name: N61Jv
Rev: 1.0
Date: Friday, December 11, 2009
Sheet 68 of 95

0.3B Beta

ASUSTeK COMPUTER INC. NB4	Title : USB 3.0_NEC (2)	
	Engineer: yun-feng_yan	
Size: A	Project Name: N61Jv	Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 69 of 95	

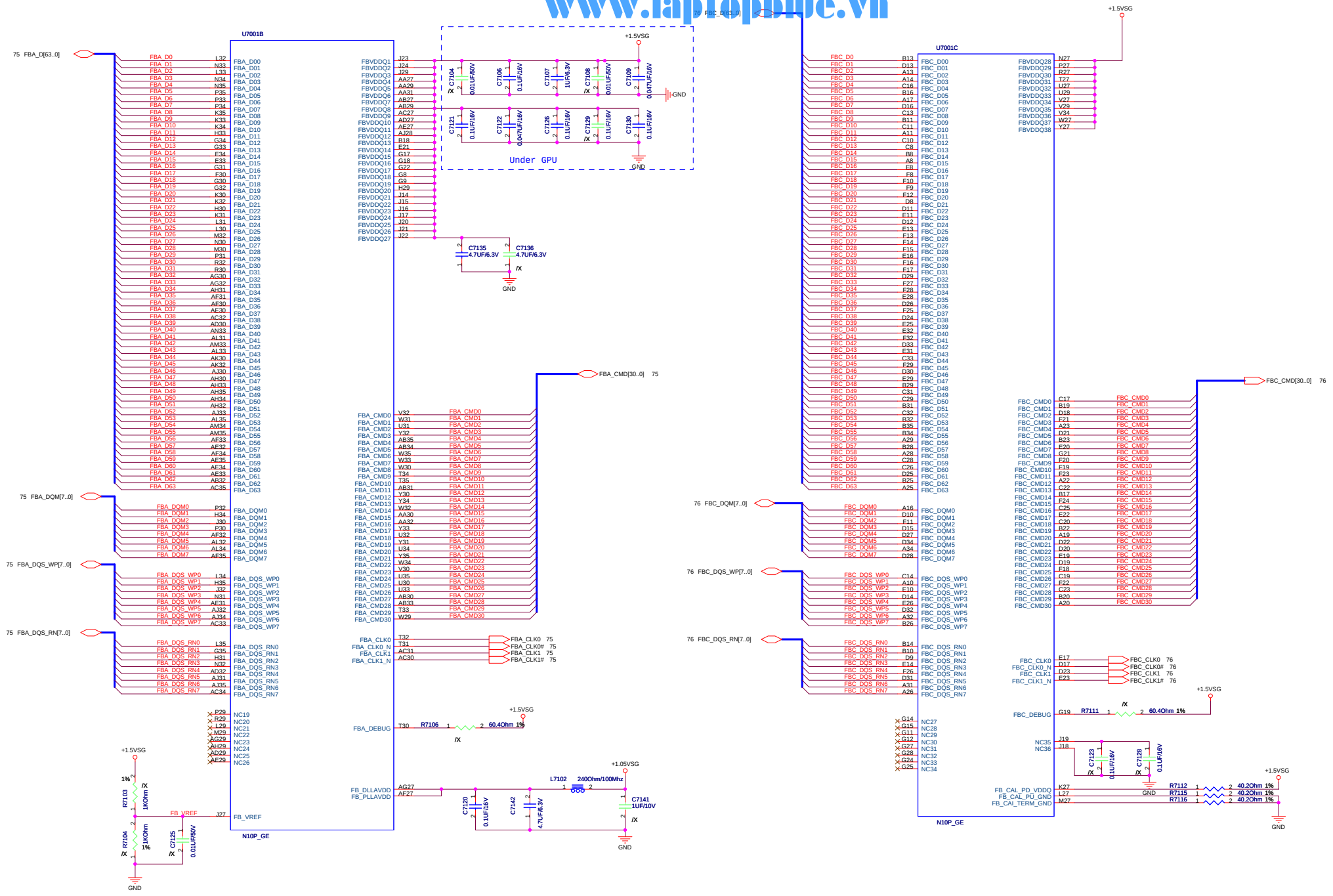


Title : N11P-GV1

Engineer: yun-feng_yan

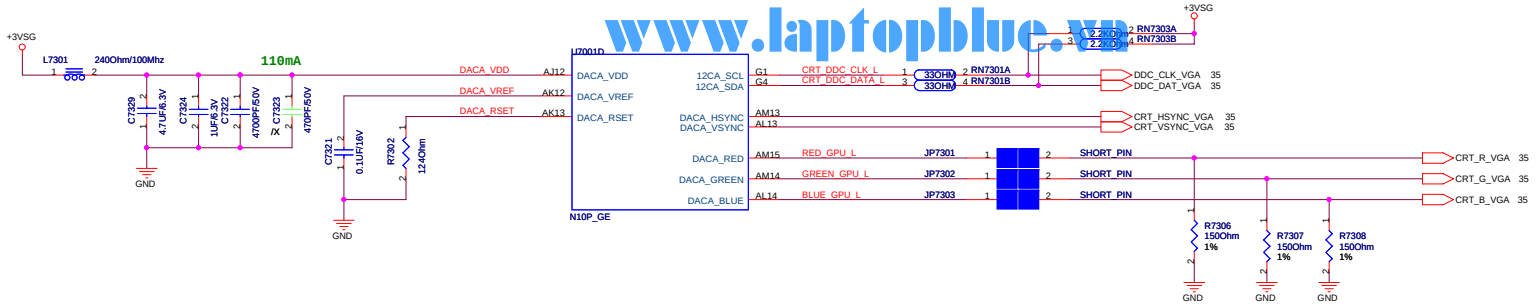
Size	Project Name	Rev
Custom	N61Jv	2.0

Date: Friday, December 11, 2009 Sheet 70 of 95

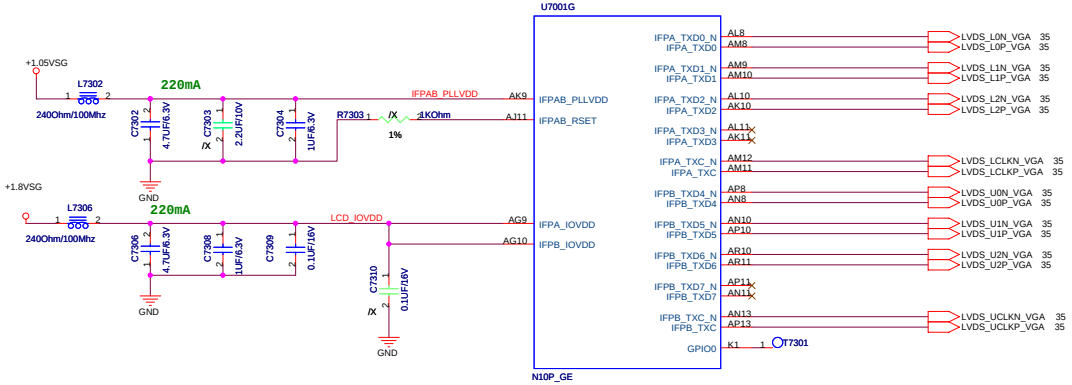


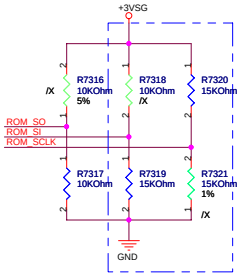
ASUSTeK COMPUTER INC. NB1	Title : N11P-GV1		
	Engineer: Yun-feng_yan		
Size: C	Project Name: N61Jv		Rev: 2.0
Date: Friday, December 11, 2009	Sheet 71 of 95		

VGA



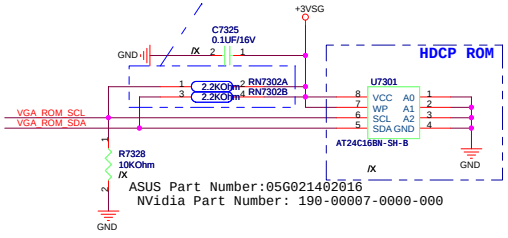
LVDS



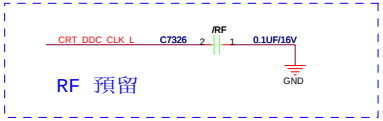


RAM_CFG[3:0]	Definitions	ROM_SI
0010	Hynix 64Mx16 DDR3	R7319 15kohm down
0011	Samsung 64Mx16 DDR3	R7319 20kohm down

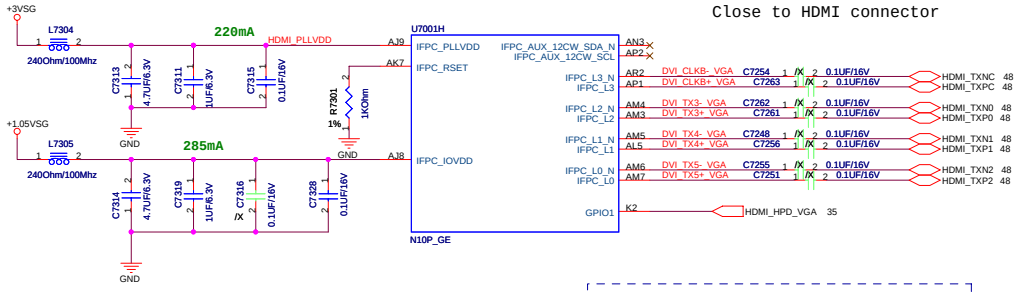
nVidia DG-04131-001_V01_secured.pdf
section 9.3



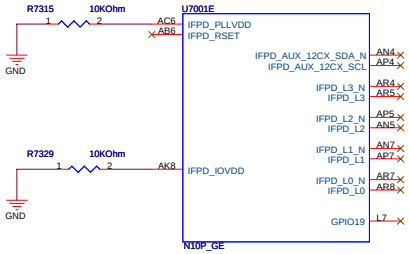
ASUS Part Number:05G021402016
NVidia Part Number: 190-00007-0000-000

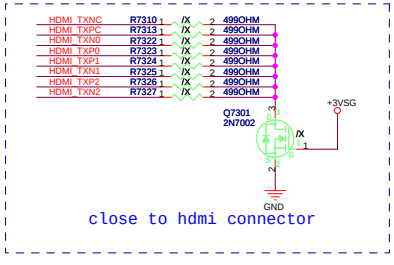


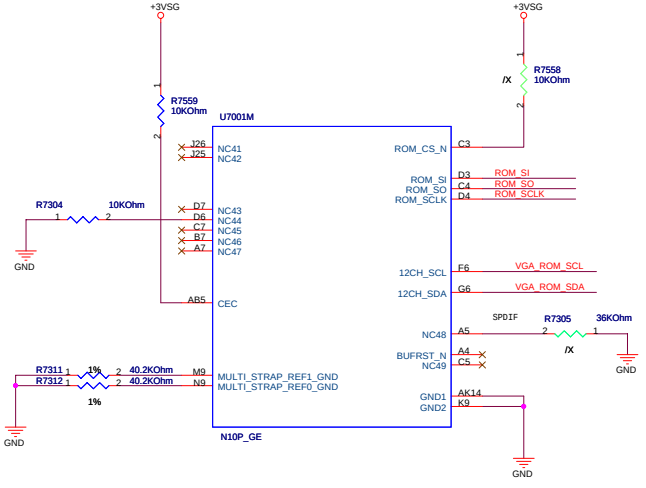
HDMI



Close to HDMI connector







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	Engineer: Yun-feng_yan		
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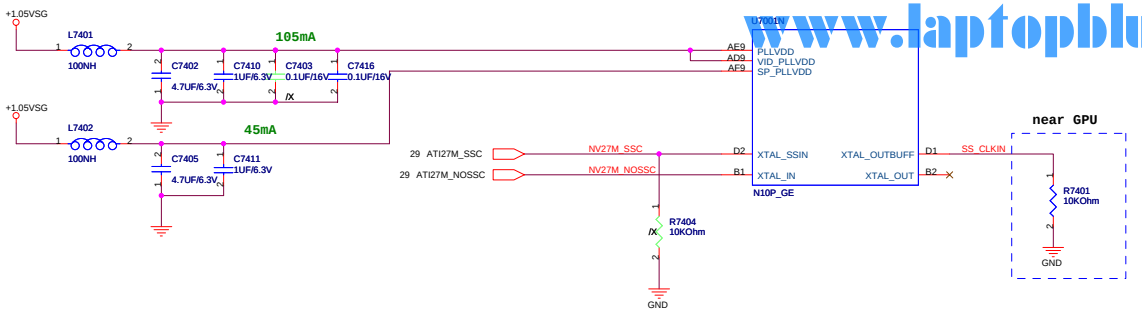
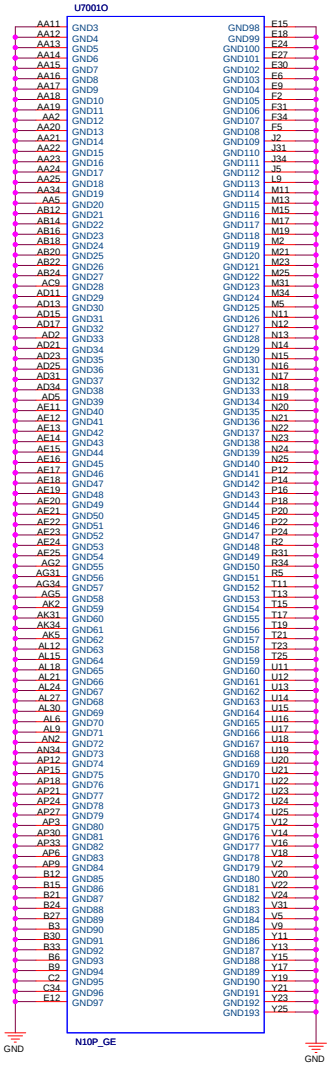
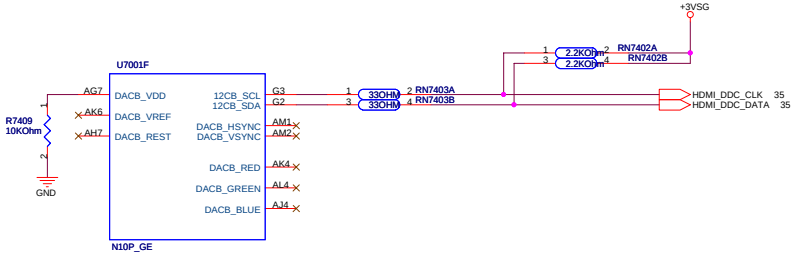
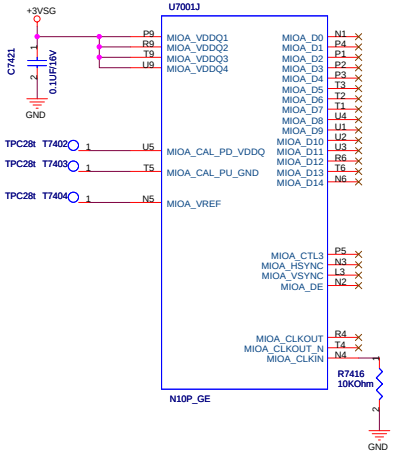
Xtal

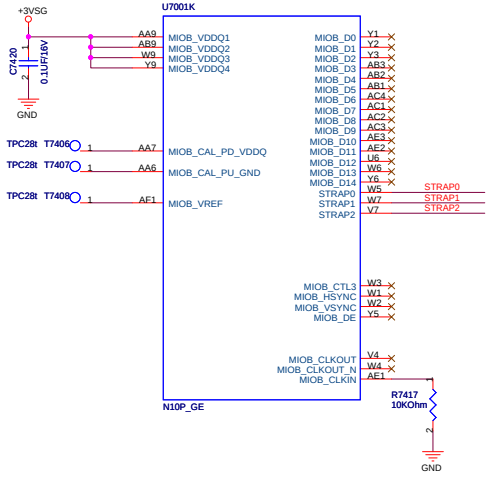


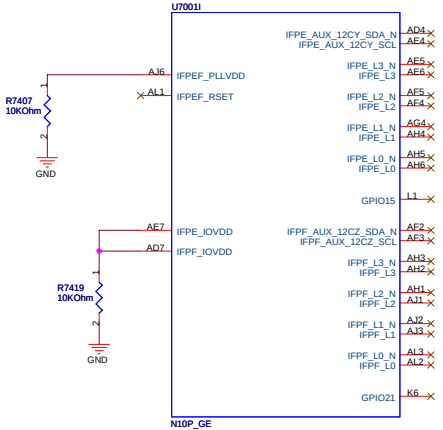


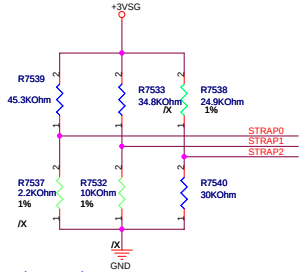
Other











Device ID is 0x0A35, set Strap2 R7540 PD 30K

ASUSTeK COMPUTER INC. NB1	Title : N11P-GV1	
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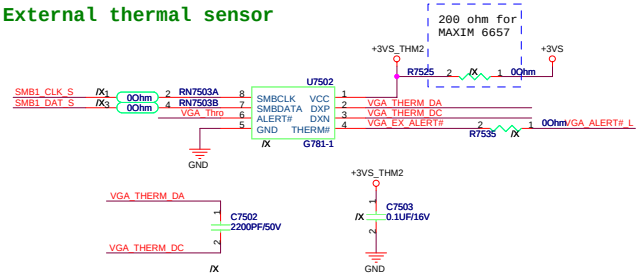
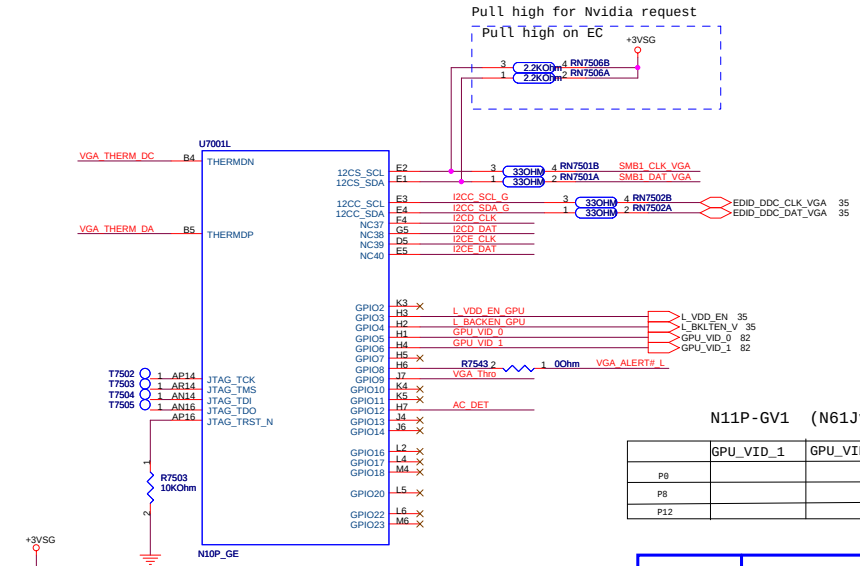
GPIO

External thermal sensor



GPIO ASSIGNMENTS

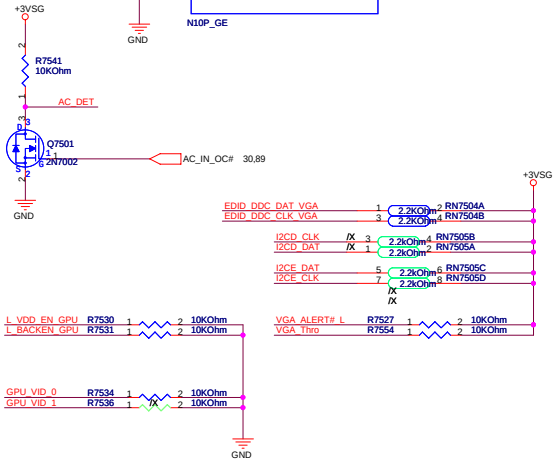
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	NVGEM
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID 0
6	OUT	N/A	NVVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL

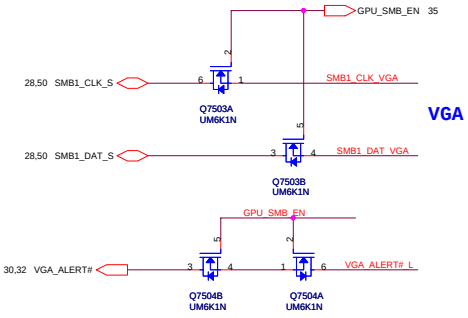


N11P-GV1 (N61Jv)

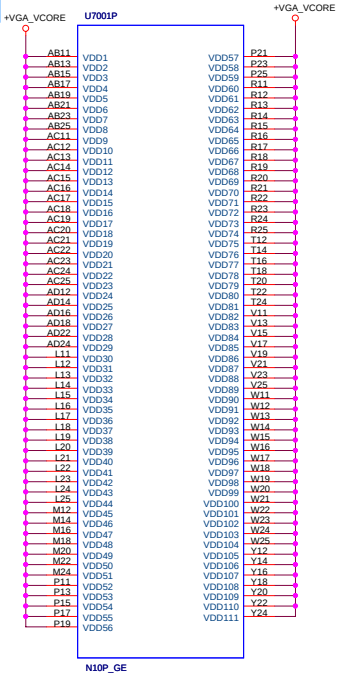
	GPU_VID_1	GPU_VID_0	+VGA_VCORE_0
P0			0.85V
P8			0.85V
P12			0.85V

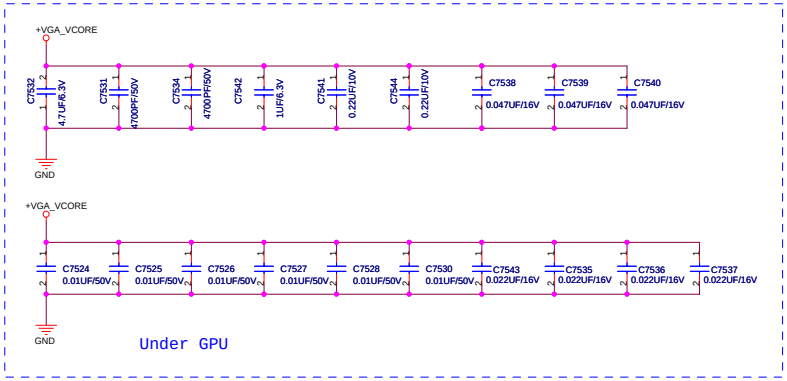
GPIO5	GPIO6	VGA_VCORE	
0	0	0.8	-10%
0	1	0.85	-5%
1	0	0.9	Normal
1	1	0.95	+5%





VGA Thermal





ASUS	Title : N11P-GV1		
ASUSTeK COMPUTER INC. NB1	Engineer: Yun-feng_yan		
Size: C	Project Name: N61Jv		Rev: 2.0
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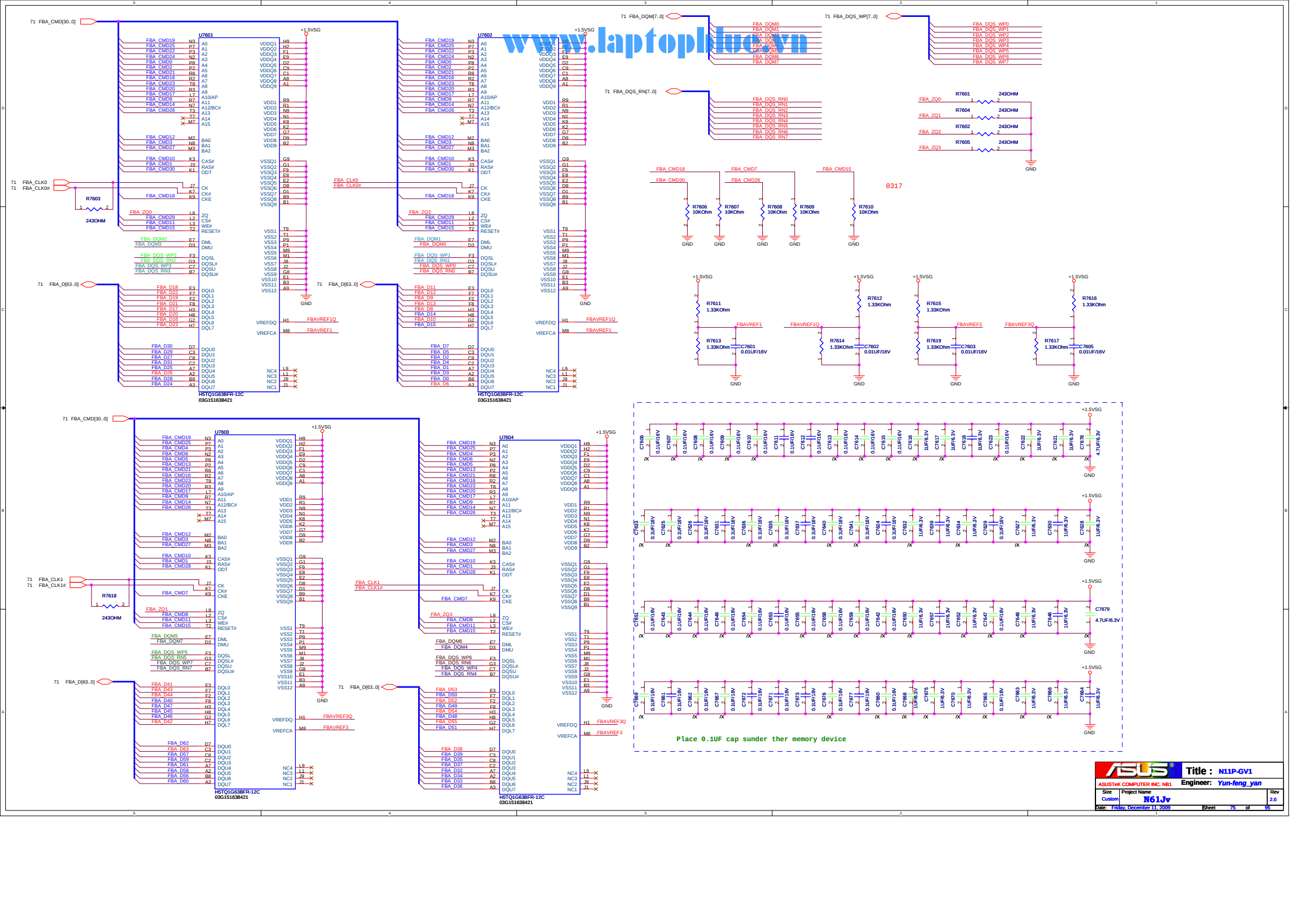

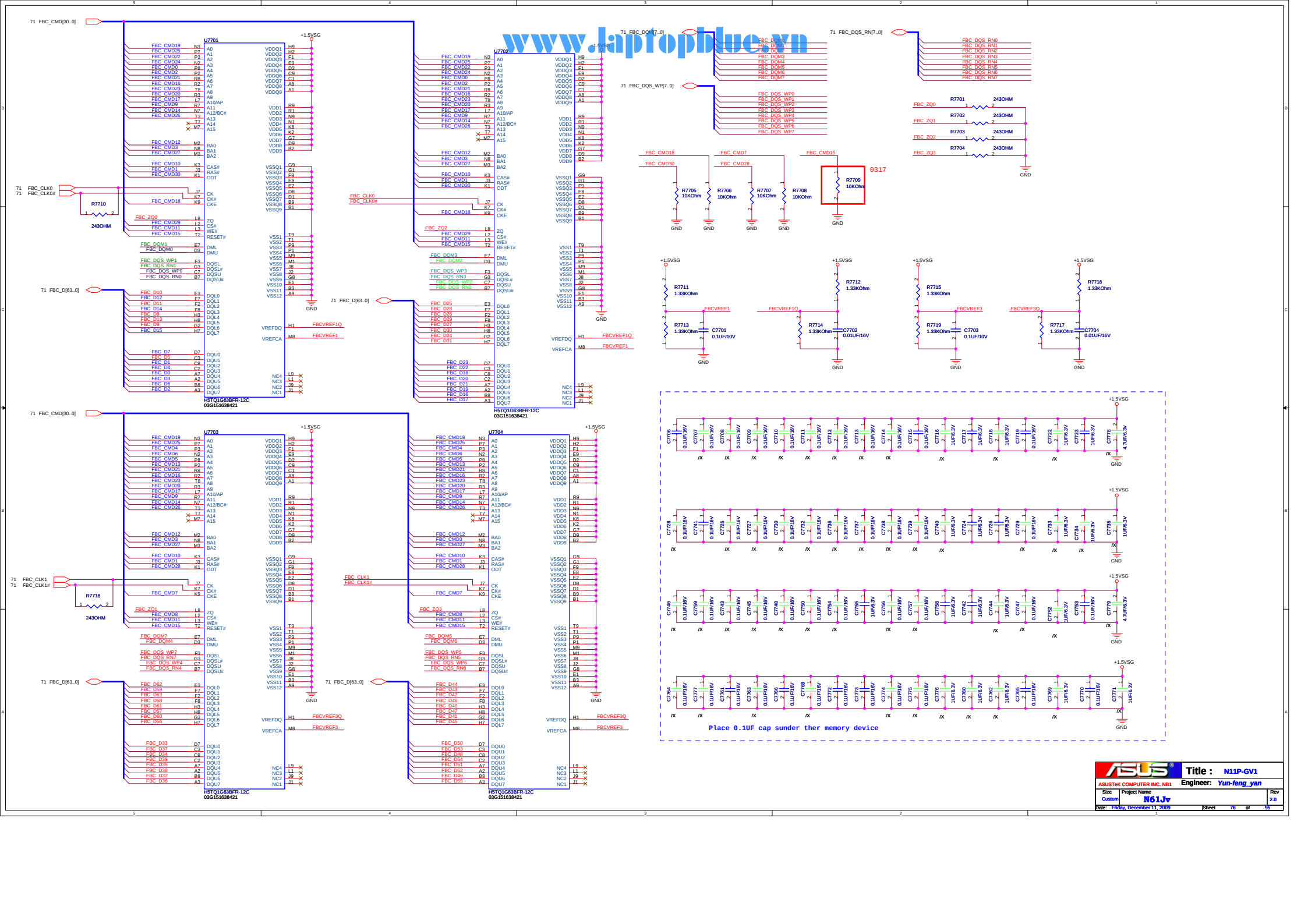

ASUSTeK COMPUTER INC. NB1	Title : N11P-GV1		
	Engineer: Yun-feng_yan		
Size: Custom	Project Name: N61Jv		Rev: 2.0
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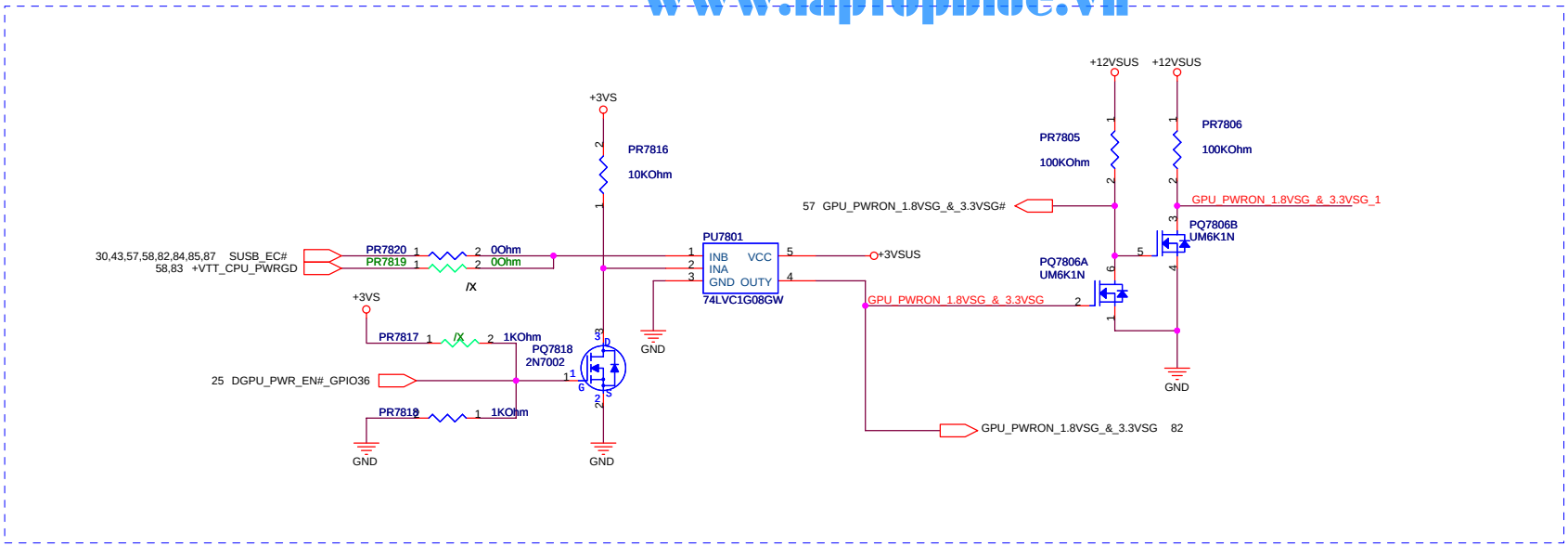
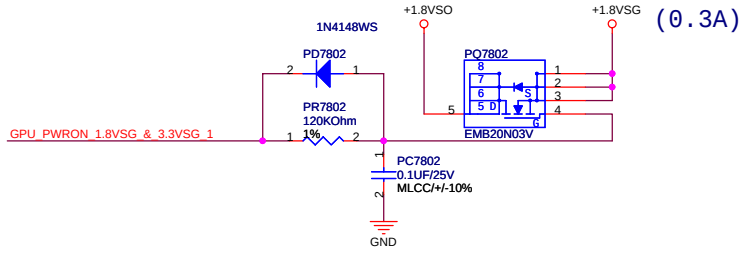
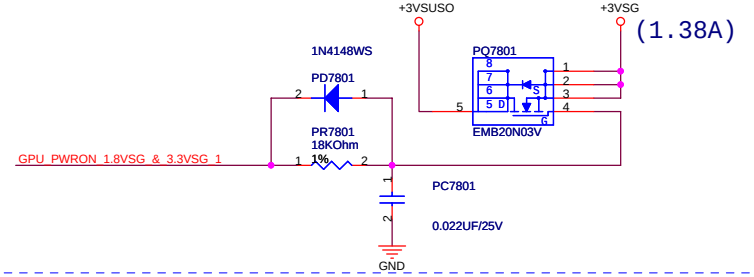
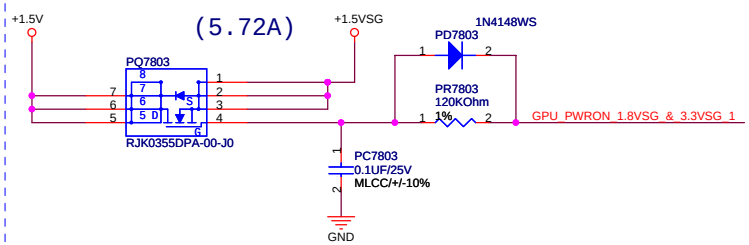
Title	<Title>	
Size A	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, November 11, 2009	Sheet 77 of 95	

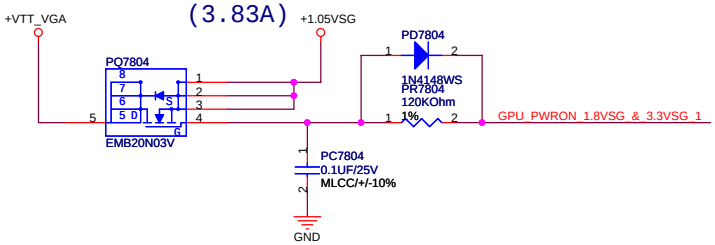


7/15 Change R7606 and C7604 for power on sequence









ASUSTeK COMPUTER INC. NB4	Title : Madison Power Sel	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N61Jv	Rev: 1.0
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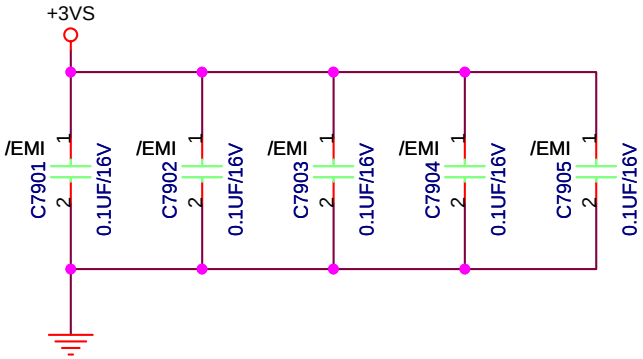

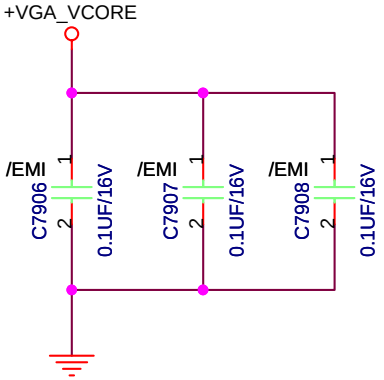

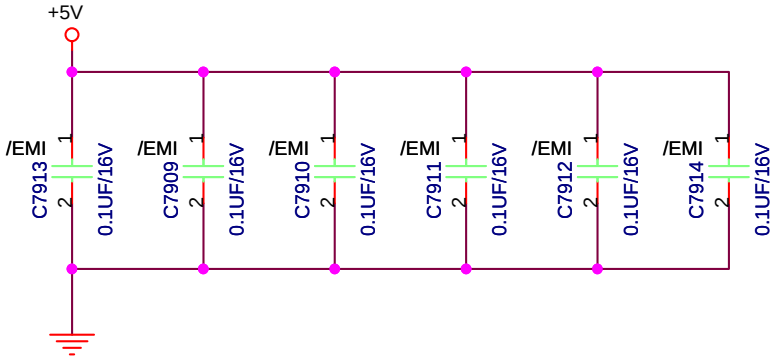

ASUSTeK COMPUTER INC. NB4	Title : EMI	
	Engineer: Yun-feng_yan	
Size: A	Project Name: N61Jv	Rev: 1.0
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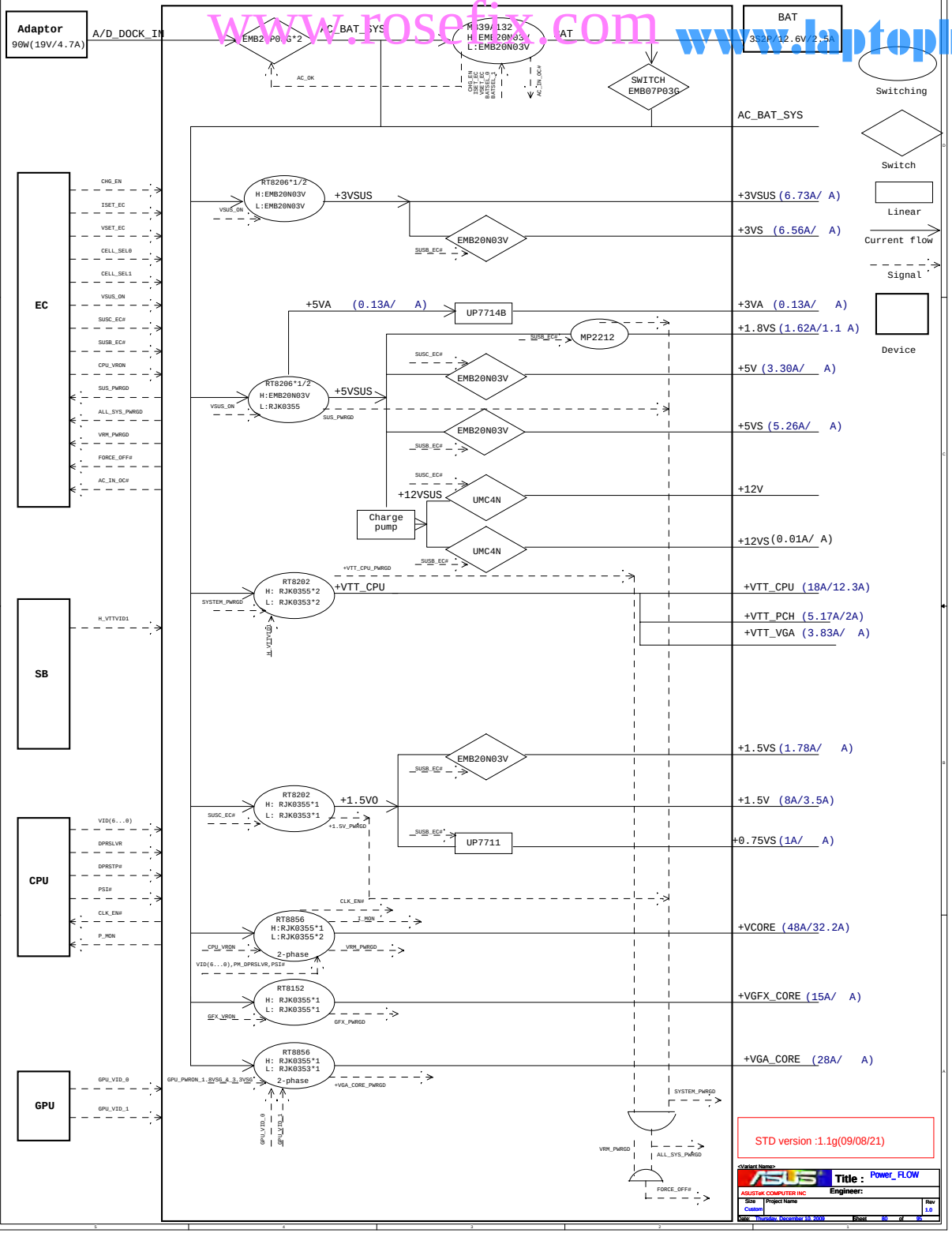

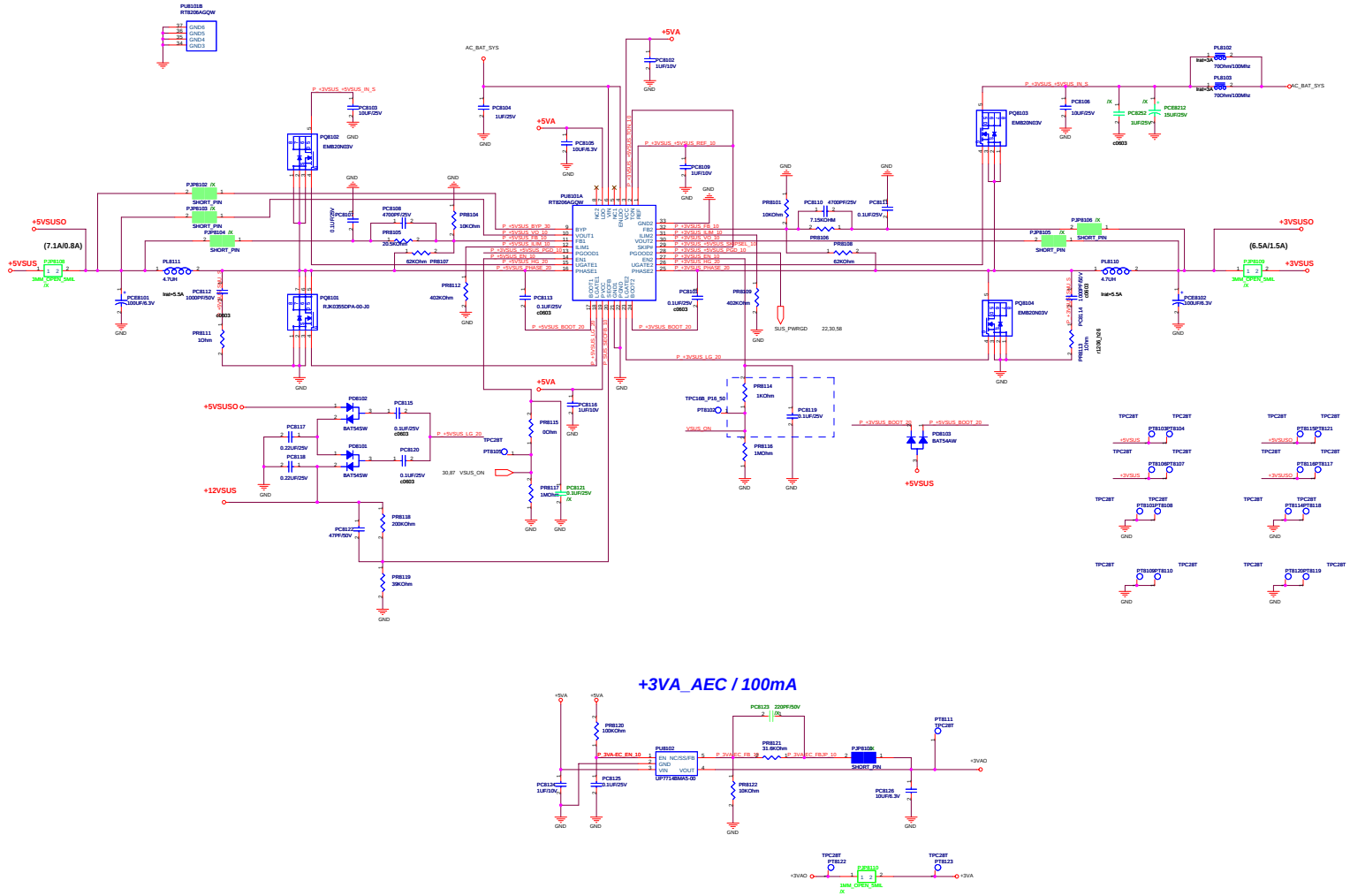

Power stage	+3VSUS
1. I/P Current:	
I in = Vo*Io/(0.8 * Vin) =1.375A	
2. Ripple Current:	
I rip =1.152A	
I spec=2.5A ⊙1	
3. Dynamic:	
Ipeak=(vin-vo)*D/(L*Fsw)=1.55A	
ESR / 1 pcs =15mohm	
》V =23.25mV	
3. Inductor Spec:	
I sat=10 A	
I dc =5.5 A	
DCR=37 mohm	
4. MOSFET Spec:	
H-side MOSFET: EMB20N03V	
Rds(ON)= 23 mohm (Vgs=4.5 V)	
I cont = 8 A (T =25)	
I peak = 32A (Pause ≦10 us)	
L-side MOSFET: EMB20N03V	
Rds(ON)= 23 mohm (Vgs=4.5 V)	
I cont = 8 A (T =25)	
I peak = 32 A (Pause ≦10 us)	

Power stage	+5VSUS
1. I/P Current:	
I in = Vo*Io/(0.8 * Vin) =2.082A	
2. Ripple Current:	
I rip =1.012A	
I spec=2.5A ⊙1	
3. Dynamic:	
Ipeak=(vin-vo)*D/(L*Fsw)=2.58A	
ESR / 1 pcs =15 mohm	
》V =38.72mV	
3. Inductor Spec:	
I sat=10 A	
I dc =5.5 A	
DCR=37 mohm	
4. MOSFET Spec:	
H-side MOSFET: EMB20N03V	
Rds(ON)= 23 mohm (Vgs=4.5 V)	
I cont = 8 A (T =25)	
I peak = 32A (Pause ≦10 us)	
L-side MOSFET: RJK0355DPA-00-J0 WPAK	
Rds(ON)= 11.8 mohm (Vgs=4.5 V)	
I cont = 30 A (T =25)	
I peak = 120 A (Pause ≦10 us)	

Controller	+3VSUS
1. Voltage & Current:	
+3VSUS=3.3V@6.73A	
2. Frequency:	
fosc=375KHz	
3. OCP:	
Set PR8109=402Kohm	
Iocp=8.74A	
4. Soft start time:	
Tss=2ms	
5.Inrush Current:	
C total = 100 uF	
I inrush= 0.165 A	

Controller	+5VSUS
1. Voltage & Current:	
+5VSUS=5V@5.27A	
2. Frequency:	
fosc=300KHz	
3. OCP:	
Set PR8112=402Kohm	
Iocp=17A	
8. Soft start time:	
Tss=2ms	
10.Inrush Current:	
C total = 100 uF	
I inrush= 0.275 A	

ASUSTeK Computer INC

Title : Power +5SUS&+3VSUS&+12VSUS

Engineer: ZHI-KUN_LIU

Size: Custom | Project Name: N61JV | Rev: 1.2

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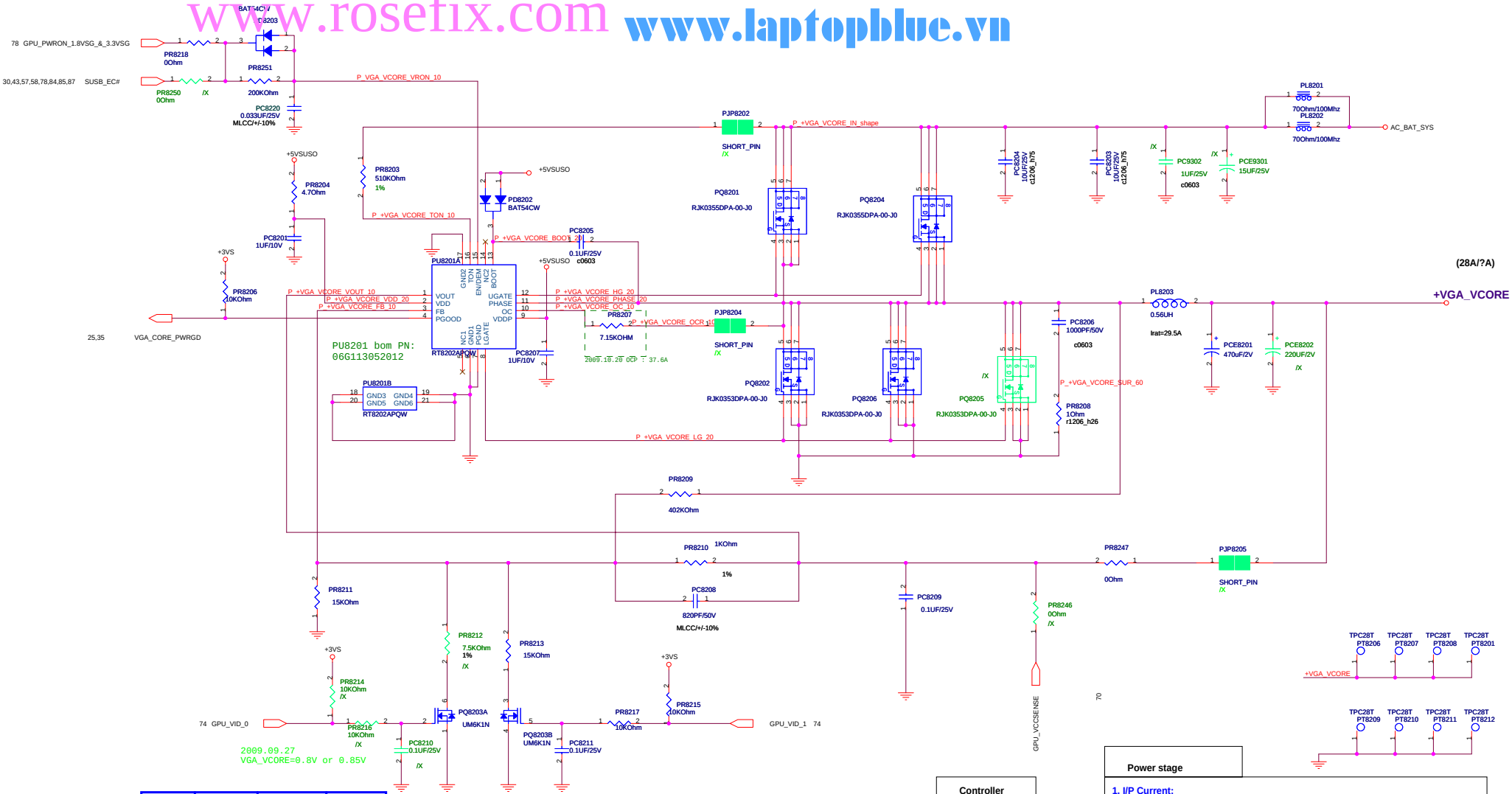

GPU_VID0	GPU_VID1	VGA_VCORE	
0	0	0.8	-10%
0	1	0.85	-5%
1	0	0.9	Normal
1	1	0.95	+5%

Controller

1. Voltage & Current:
   +VGA_VCORE: 28A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR8207=22KOhm
   Iocp=Rocp*20/Rds(on)=57A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =3.73A
2. Ripple Current:
   Iripple=3.74A
3. ripple voltage:
   Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
   DCR=3.3mohm
   V=6.831mV
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. OCP:
5. MOSFET Spec:
   H-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)
   L-side MOSFET: RJK0353
   Rds(on)=7.6mOhm (Vgs=4.5V)
   Icont=35A (T=25)
   Ipeak=140A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_+VGA_VCORE

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

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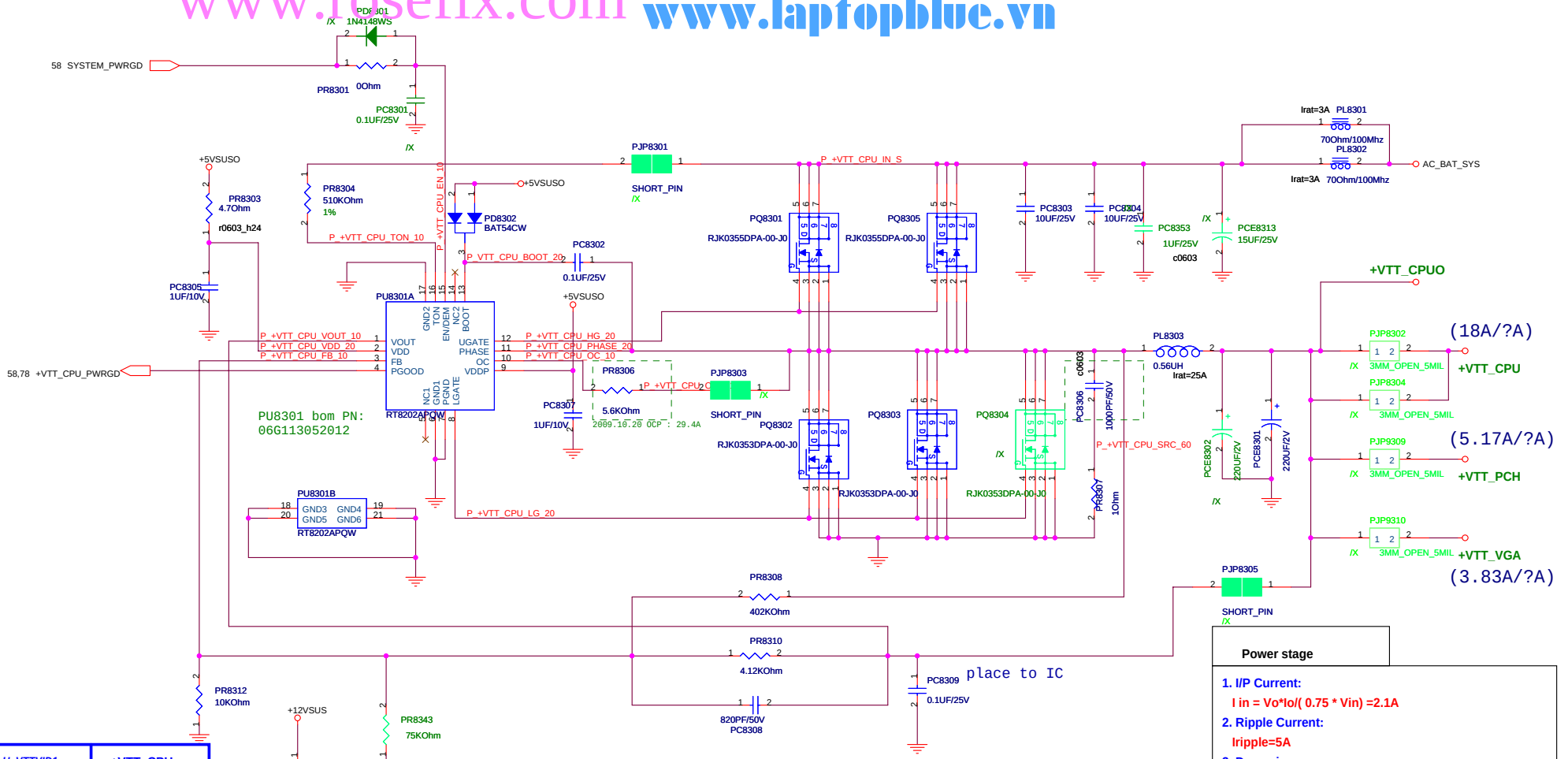

H_VTTVID1	+VTT_CPU
1	1.05V
0	1.1V

Controller

1. Voltage & Current:
   +VTT_CPU:1.05V@25A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR8306=20KOhm
   Iocp=Rocp*20/Rds(on)=52A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total = 220 uF
   I inrush= 0.16 A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =2.1A
2. Ripple Current:
   Iripple=5A
3. Dynamic:
   Ipeak=1.98A
   DCR=3.3mohm
   V=6.534mV
4. Inductor Spec:
   Isat=40A
   Idc=25A
   DCR=1.8mOhm
5. MOSFET Spec:

H-side MOSFET:RJK0355
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

L-side MOSFET: RJK0353
Rds(on)=7.6mOhm (Vgs=4.5V)
Icont=35A (T=25)
Ipeak=140A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_+VTT_CPU

Engineer:

Size	Project Name	Rev
Custom		1.0

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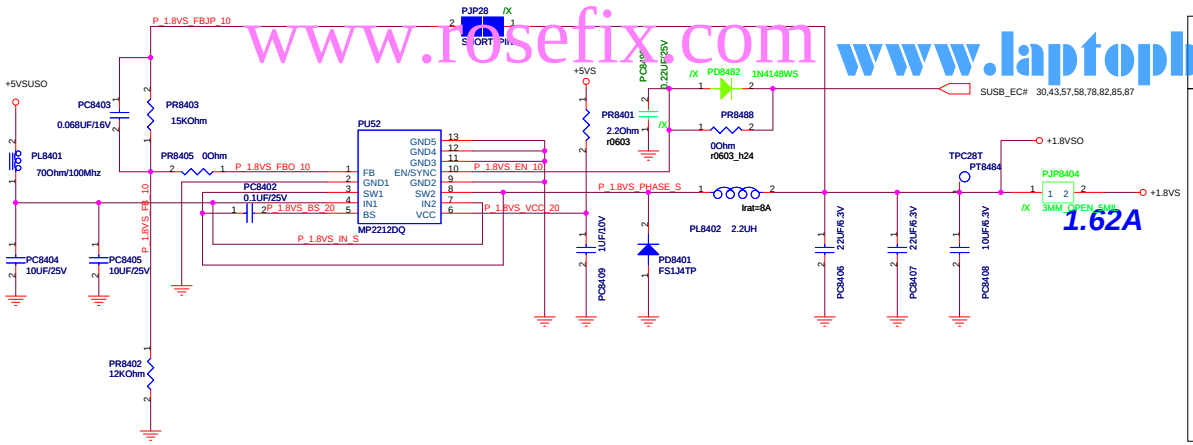


Power stage

1. I/P Current:

I in = Vo*Io/(0.8 * Vin) =0.73A

2. Ripple Current:

I rip =1.08A
I spec=2.5A ⊙1 pcs

3. Inductor Spec:

I sat=14 A
I dc =8 A
DCR=18 mohm

Controller

1. Voltage & Current:

+1.8VS@1.62A

2. Frequency:

Fosc=600KHz

3. Current Limit:

6A

4.Continue Current:

3.75A

5. POR:

POR Hysteresis =0.2V
V on =2.8V

6. Enable Voltage:

V = 1.6V

7. Soft start time:

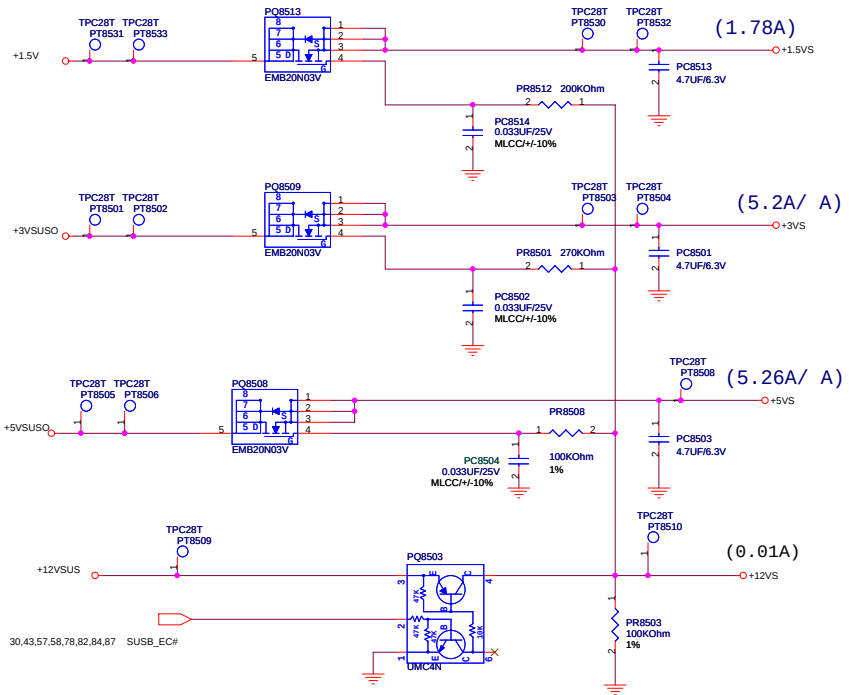
Tss=120us

8.Inrush Current:

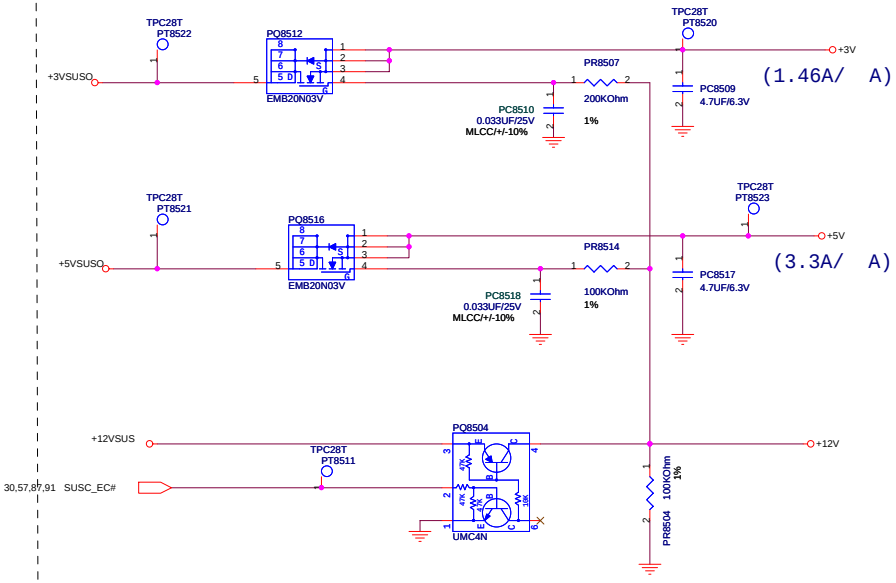
C total = 54 uF
I inrush=
0.473A

ASUSTek Computer INC	Title : +1.8VS	
	Engineer:	
Size: C	Project Name: N61JV	Rev: <RevCode>
Date: Friday, December 11, 2009	Sheet 84 of 95	

SUSB#_PWR POWER



SUSC#_PWR POWER



<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_Load_Switch

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, December 11, 2009 Sheet 85 of 95

<Variant Name>

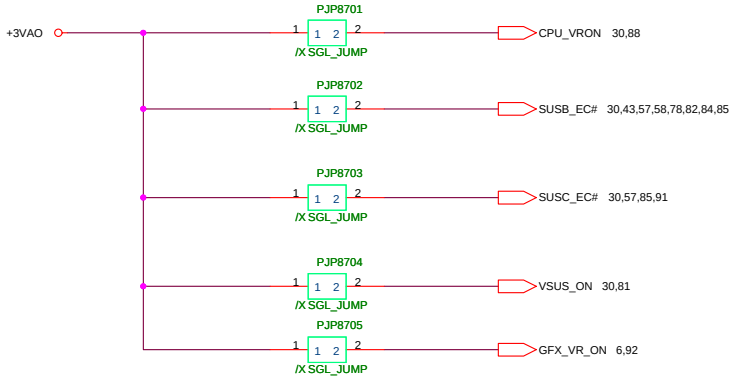
ASUSTeK COMPUTER INC

Title : Power_good_detecter

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, December 10, 2009 Sheet 86 of 95



<Variant Name>

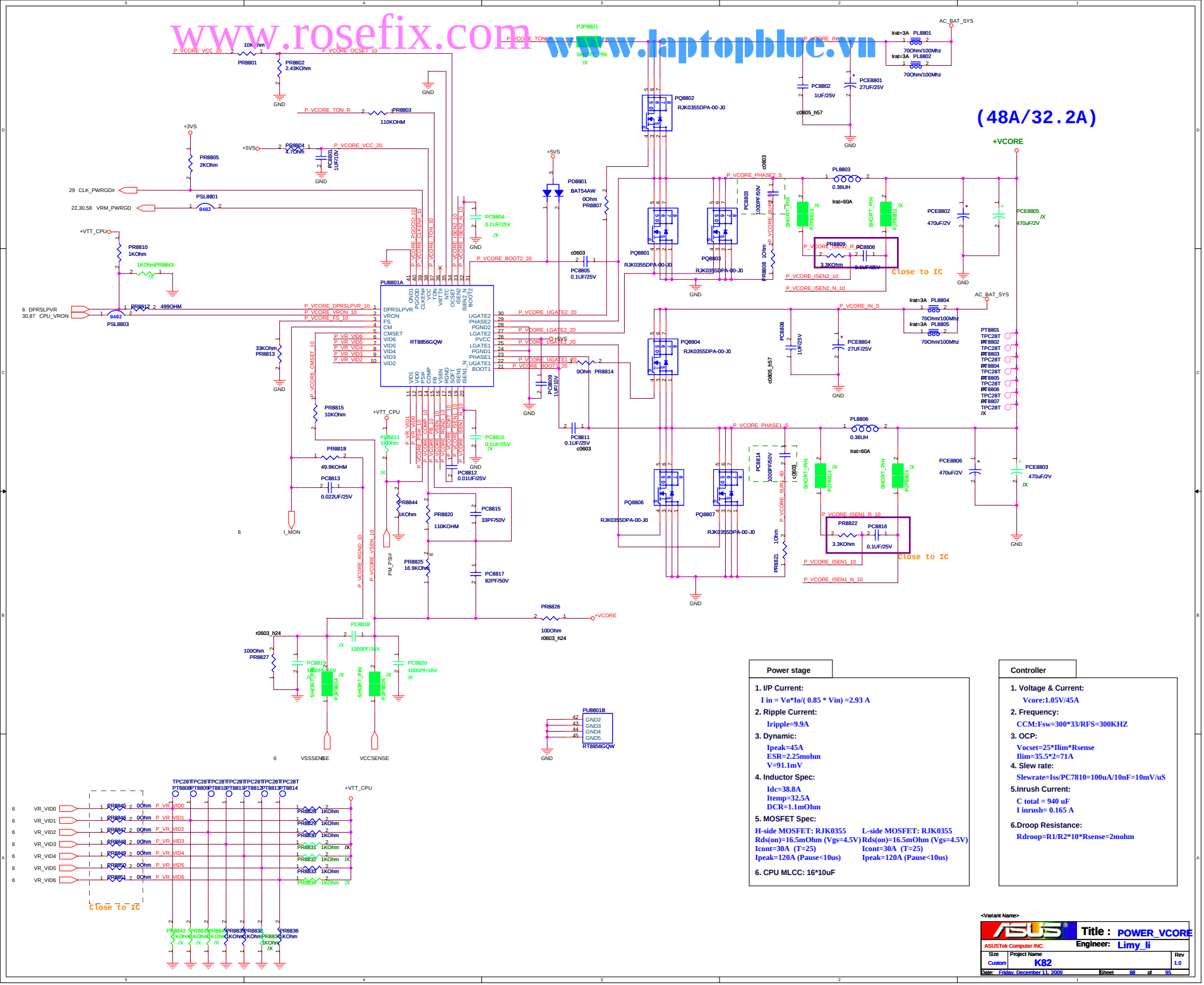
ASUSTeK COMPUTER INC

Title : Power_for_test

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, December 11, 2009 Sheet 87 of 95



Power stage

1. I/P Current:
   I in = Vo*Io/(0.85 * Vin) =2.93 A
2. Ripple Current:
   Iripple=9.9A
3. Dynamic:
   Ipeak=45A
   ESR=2.25mohm
   V=91.1mV
4. Inductor Spec:
   Idc=38.8A
   Itemp=32.5A
   DCR=1.1mOhm
5. MOSFET Spec:

H-side MOSFET: RJK0355	L-side MOSFET: RJK0355
Rds(on)=16.5mOhm (Vgs=4.5V)	Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)	Icont=30A (T=25)
Ipeak=120A (Pause<10us)	Ipeak=120A (Pause<10us)

6. CPU MLCC: 16*10uF

Controller

1. Voltage & Current:
   Vcore:1.05V/45A
2. Frequency:
   CCM:Fsw=300*33/RFS=300KHZ
3. OCP:
   Vocset=25*Ilim*Rsense
   Ilim=35.5*2=71A
4. Slew rate:
   Slewrate=Iss/PC7810=100uA/10nF=10mV/uS
5. Inrush Current:
   C total = 940 uF
   I inrush= 0.165 A
6. Droop Resistance:
   Rdroop=R1/R2*10*Rsense=2mohm

<Variant Name>

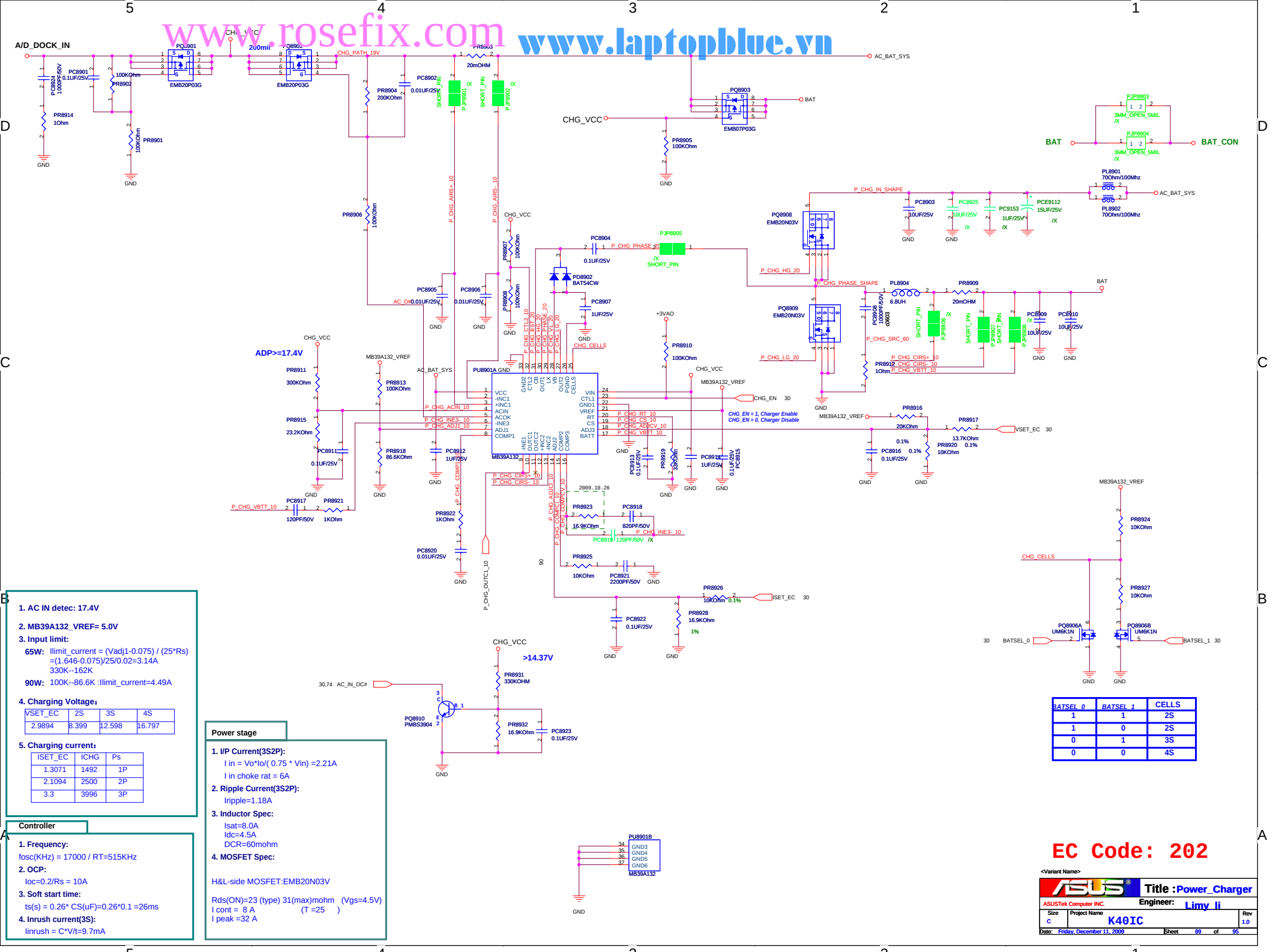
ASUSTek Computer INC.

Title : POWER_VCORE

Engineer: Limy_li

Size	Project Name	Rev
Custom	K82	1.0

Date: Friday, December 11, 2009 Sheet 88 of 95



BATSEL_0	BATSEL_1	CELLS
1	1	2S
1	0	2S
0	1	3S
0	0	4S

1. AC IN detec: 17.4V

2. MB39A132_VREF= 5.0V

3. Input limit:

65W: Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.646-0.075)/25/0.02=3.14A
330K--162K

90W: 100K--86.6K :Ilimit_current=4.49A

4. Charging Voltage:

VSET_EC	2S	3S	4S
2.9894	8.399	12.598	16.797

5. Charging current:

ISET_EC	ICHG	Ps
1.3071	1492	1P
2.1094	2500	2P
3.3	3996	3P

Controller

1. Frequency:
fosc(KHz) = 17000 / RT=515KHz

2. OCP:
Ioc=0.2/Rs = 10A

3. Soft start time:
ts(s) = 0.26* CS(uF)=0.26*0.1 =26ms

4. Inrush current(3S):
Iinrush = C*V/t=9.7mA

Power stage

1. I/P Current(3S2P):
I in = Vo*Io/(0.75 * Vin) =2.21A
I in choke rat = 6A

2. Ripple Current(3S2P):
Iripple=1.18A

3. Inductor Spec:
Isat=8.0A
Idc=4.5A
DCR=60mohm

4. MOSFET Spec:

H&L-side MOSFET:EMB20N03V

Rds(ON)=23 (type) 31(max)mohm (Vgs=4.5V)
I cont = 8 A (T =25)
I peak =32 A

EC Code: 202

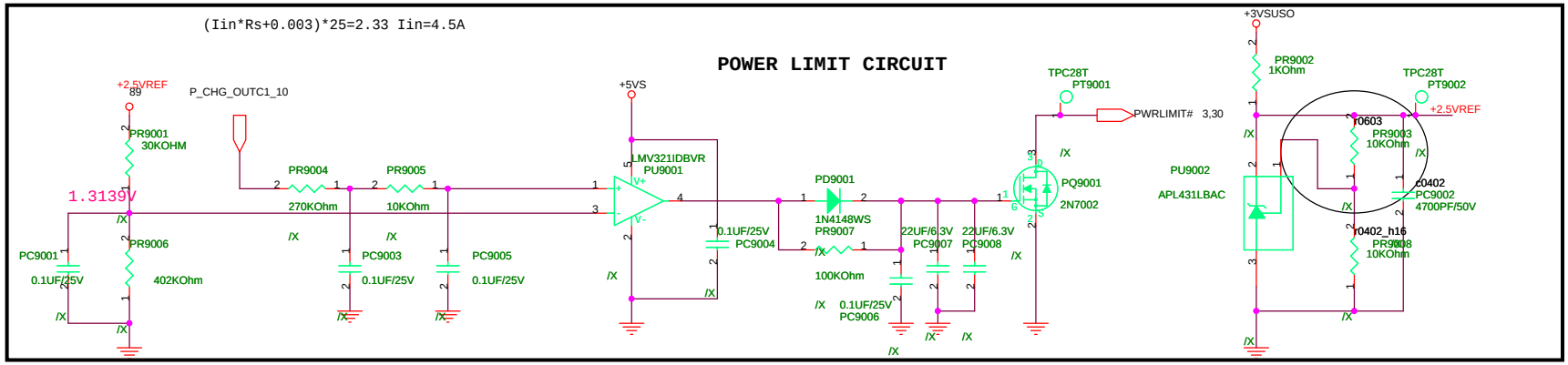
<Variant Name>

Title : Power_Charger

ASUSTek Computer INC. Engineer: Limy_li

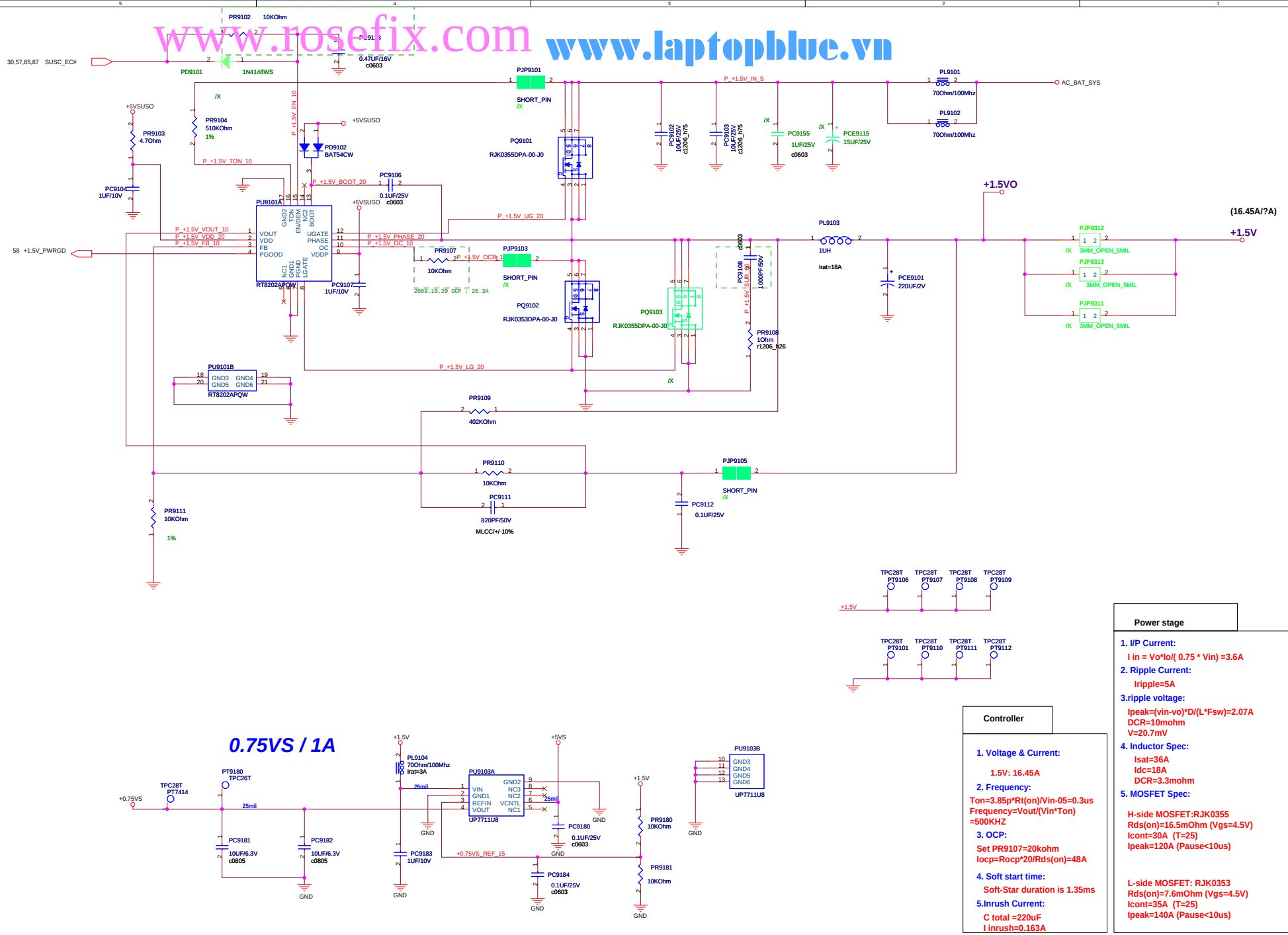
Size	Project Name	Rev
C	K40IC	1.0

Date: Friday, December 11, 2009 Sheet 89 of 95



<Variant Name>

ASUSTek Computer INC.	Title : Power_Charger	
	Engineer: Limy_li	
Size: A3	Project Name: F83T	Rev: 2.1G
Date: Friday, December 11, 2009	Sheet 90 of 95	



0.75VS / 1A

Controller

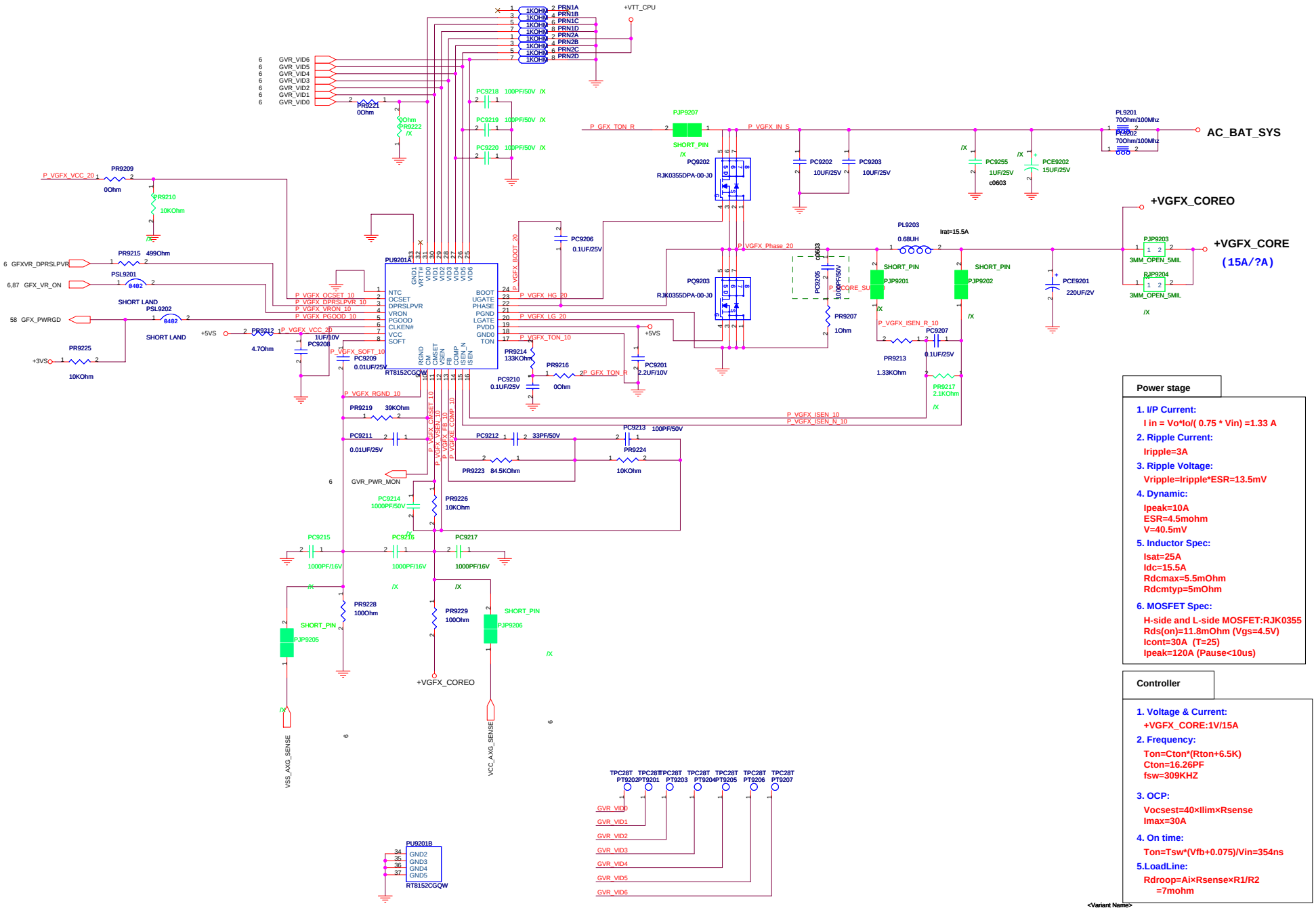
1. Voltage & Current:
   1.5V: 16.45A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR9107=20kohm
   Iocp=Rocp*20/Rds(on)=48A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =3.6A
2. Ripple Current:
   Iripple=5A
3. ripple voltage:
   Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
   DCR=10mohm
   V=20.7mV
4. Inductor Spec:
   Isat=36A
   Idc=18A
   DCR=3.3mohm
5. MOSFET Spec:
   H-side MOSFET:RJK0355
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)
   L-side MOSFET: RJK0353
   Rds(on)=7.6mOhm (Vgs=4.5V)
   Icont=35A (T=25)
   Ipeak=140A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC	Title : +1.5V	
	Engineer:	
Size: C	Project Name: K80F	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 91 of 95	



Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.33 A
2. Ripple Current:
   Iripple=3A
3. Ripple Voltage:
   Vripple=Iripple*ESR=13.5mV
4. Dynamic:
   Ipeak=10A
   ESR=4.5mohm
   V=40.5mV
5. Inductor Spec:
   Isat=25A
   Idc=15.5A
   Rdcmax=5.5mOhm
   Rdcmtyp=5mOhm
6. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355
   Rds(on)=11.8mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

Controller

1. Voltage & Current:
   +VGFX_CORE:1V/15A
2. Frequency:
   Ton=Cton*(Rton+6.5K)
   Cton=16.26PF
   fsw=309KHZ
3. OCP:
   Vocsest=40×Ilim×Rsense
   Imax=30A
4. On time:
   Ton=Tsw*(Vfb+0.075)/Vin=354ns
5. LoadLine:
   Rdroop=Ai×Rsense×R1/R2
   =7mohm

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_VCORE

Engineer: Limy_li

Size	Project Name	Rev
C	UX21	1.0

Date: Friday, December 11, 2009 Sheet 92 of 95

1.將58頁+3V0改為+3VSUS。
2. Add change SL3801 to 330hm Resistor for EVT
3.change D3401 and D3402 stuff by default.
4.Follow Design Ip swap USB port 3 and Port 11
5、Change SL3402,SL3403,SL3404,SL3405,SL3406,SL3407,SL3408,SL3409 to 0402 SL
6.Change R5638 to 5V, eagle eye,add power led to 5V for prevent eagle eye,add power led will flash when insert AC.
7.Mount C3634,C3635,C3409,C5607,D4505,D4506,change R6301 from 27.4ohm to 1K,reverse D6402 for EMI suggestion.
8.Change card reader from port3 to port11 for follow Design IP.
9.Change R4007,R4012 footprint to 0603 for power.
10.Add R0638 for ATS graphic power test.
11.Add U6802,R6811,R6812,C6861,C6862,C6863,C6864 and SL6802 for USB30 +1.05V support.
12.Change R3021,R3023 to 100K for follow EC Design IP.
13.umount R0605.
14.Stuff R0606.
15.Delete SL3313.
16.umount R7404.
17.change EC8512 to EC8570.
18.Add USB2.0 signal Switch U5201.
19.JP5401 don't be short.
20.EC SMB1 Pull High to +3VSUS.
21.Add Support NB290 schematic------Page61.
22.Delete DGPU HDMI output.
23.Add thermal sensor G709 Support.

ER---------->>>>> PR

1.change SL4513 to R4509;----P45
2.change R3554.Pin2 from DGPU_PWROK to DGPU_HOLD_RST# ,Change R3555.Pin1 Pull High to +5VS,Add C3510,C3511;----P35
3.connect U6802.Pin7 to R6811.Pin2;----P68
4.Add SL6322,change LED6306,LED6307,LED6308,LED6309,LED6310,LED6311 Pin1 from +5VA/SUS_IOR to +5V_IOR.----P63
5.Change J6303 part number to 14G152231000;----P63
6.Add C6213,C6214,C6215, Add GND_AUDIO_IO for headphone speaker;----P62
7.Mount D6001;----P60
8.Add USB2.0 Port J5201;----P52
9.Mount C4611,C4612;----P46
10.change R2533 from 10k to 100k;----P25
11.change R4512 to 1k for samsung panel voltage;----P45
12.Umount R5817;------P58
13.Add 07G001007100 Second source 07G001007230---D2205,D2206,D2207,D3207,D4401,D5800
14.Add C3203-------P32;
15.Q3550,R3556,D3510,R3558,C3502 for VGA_CORE_PWRGD;----P35
16.Delete R3602;------P36
17.Umount U5002,C5007,C5001,Q5001;----P50
18.Delete CN5601,Add C5616,C5617,C5618,C5619 for EMI;----P56
19.Add C6303,C6304 for EMI;----P63
20.Add L6204,RN6201,RN6301,L6302,D6301 for EMI;
21.Umount C7254,C7263,C7262,C7261,C7248,C7256,C7255,C7251,R7310,R7313,R7322,R7323,
R7324,R7325,R7326,R7327,Q7301.----P72
22.Mount CN5603,CN5604,C5610,C5611, C5614, C4511;
23.Umount R3509,R3510,R3511,R3512,R3513,R3514,R3515,R3516;----P35
24.Add U2801 secondsource 05G001602110;
25.SKU2 BOM add J6106.
26.Mount C0613,C0654;
27.Umount R5401,R5402.

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_VCORE

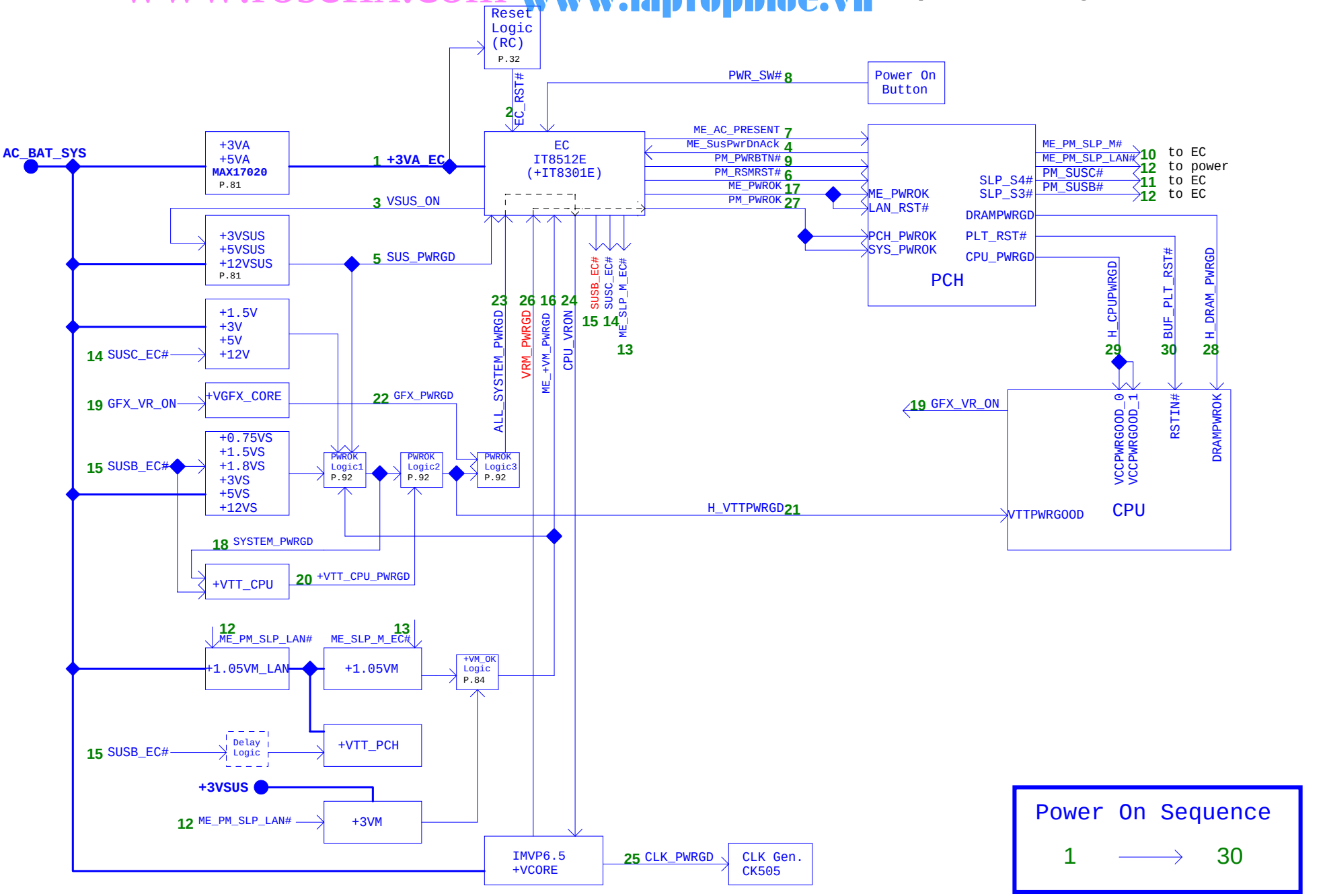
Engineer: yun-feng_yan

Size	Project Name	Rev
B	N61Jv	1.0

Date: Tuesday, December 15, 2009 Sheet 93 of 95

AC-IN Mode

N61Jv Power On Sequence Diagram Rev. 0.31



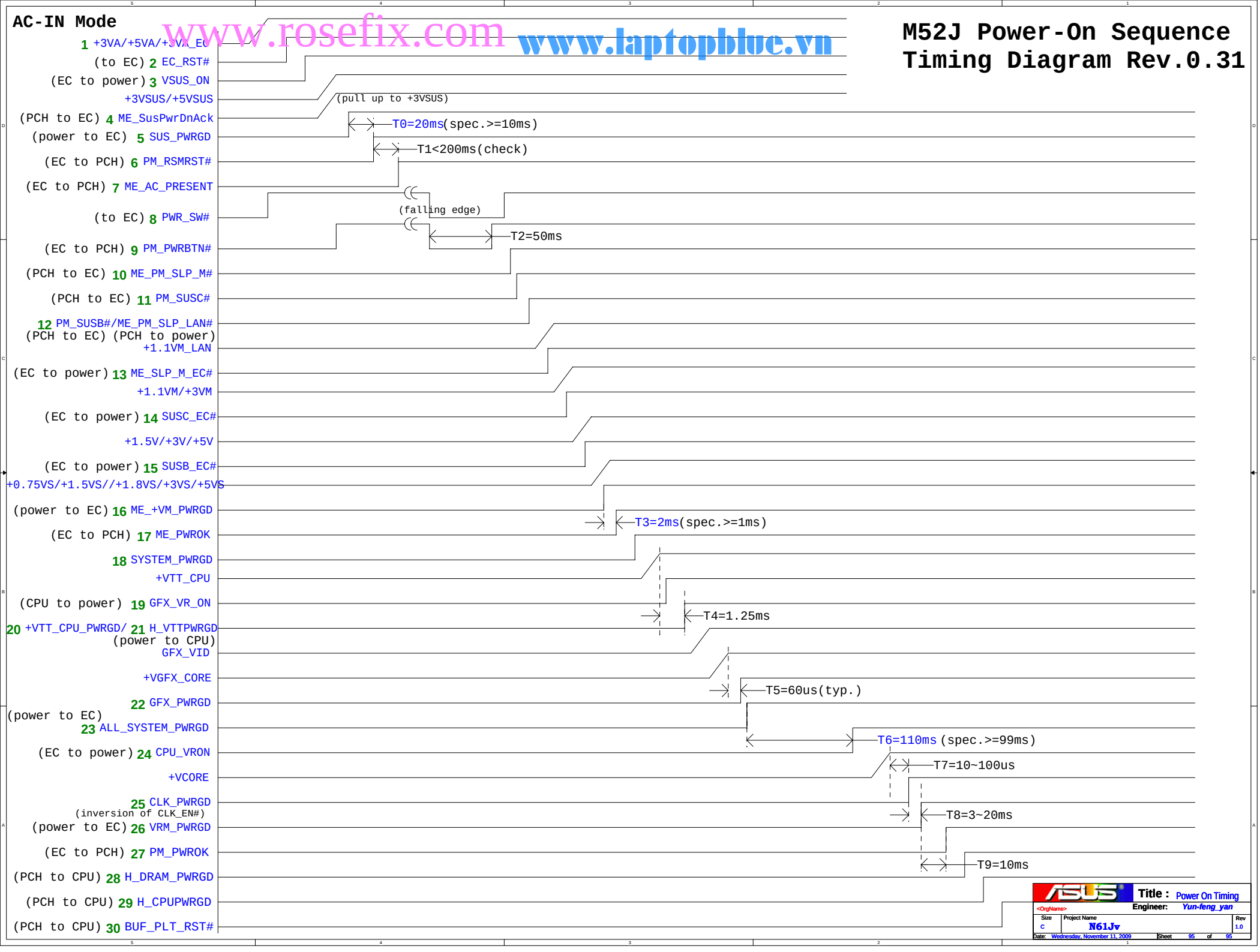
Power On Sequence

1 → 30

ASUSTeK COMPUTER INC	Title : POWER SEQUENCE		
	Engineer: Yun-feng_yan		
Size: C	Project Name: N61Jv		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 94 of 95		

M52J Power-On Sequence Timing Diagram Rev.0.31

AC-IN Mode



Title : Power On Timing			
<OrgName>	Engineer: Yun-feng_yan		
Size: C	Project Name: N61Jv		Rev: 1.0
Date: Wednesday, November 11, 2009	Sheet 95 of 95		