

SYSTEM DC/DC		CPU DC/DC	
APL5916KAI 48		NCP6131S52MNR 42~43	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0	DCBATOUT	VCC_CORE

SYSTEM DC/DC	
UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC	
UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC	
UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC	
NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA	
RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

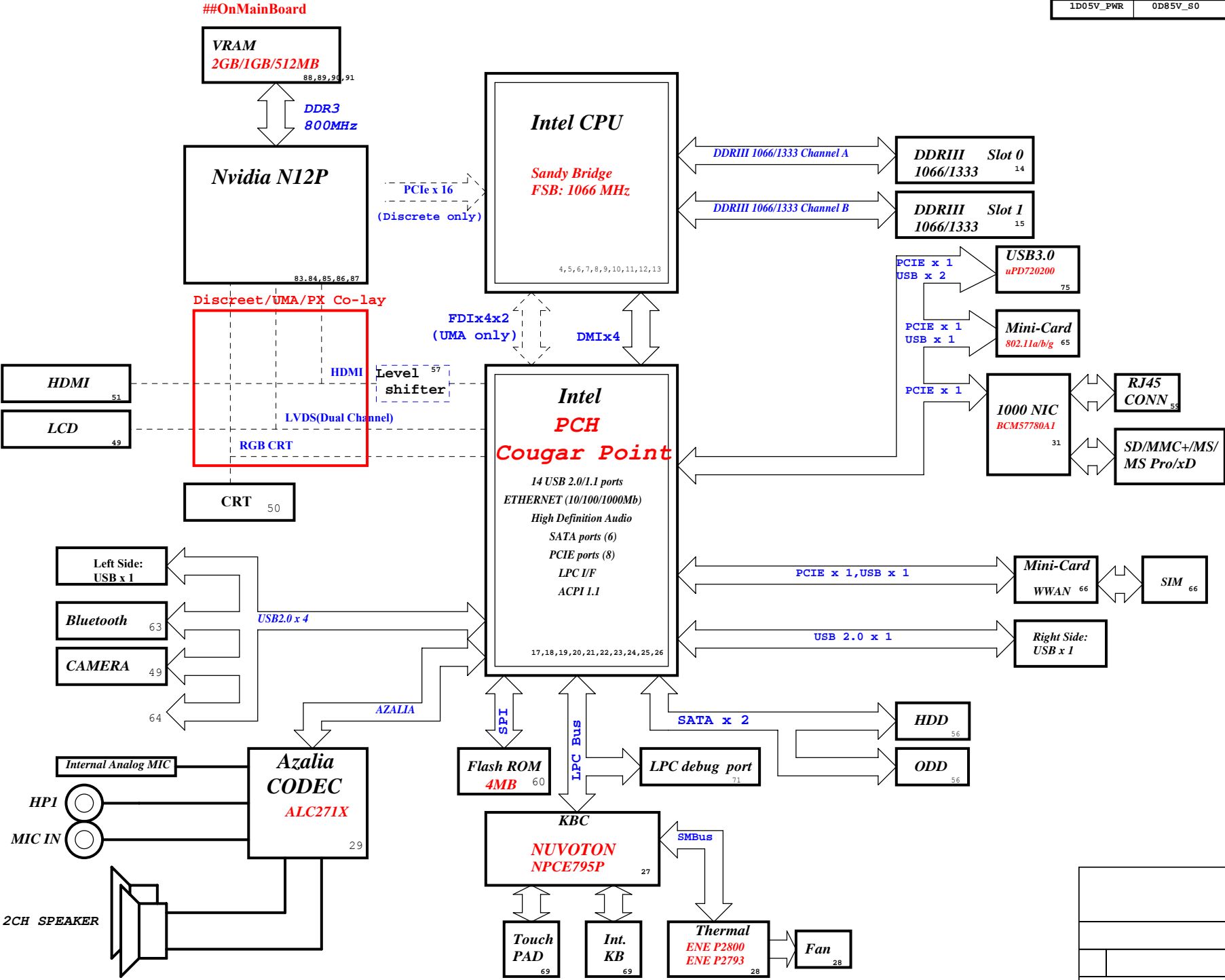
TI CHARGER	
BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC	
RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC	
RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom



Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. <b>Disable Danbury:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] <b>Disable Danbury:</b> Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

Pin Name	Strap Description	Configuration (Default value for each bit is unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connectd to the EMBEDDED display Port 0:	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I2 C / SMBus Addresses		Ref Des	HURON RIVER ORB	
Device			Address	Hex Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SM11_CLK/SM11_DATA SM11_CLK/SM11_DATA SM11_CLK/SM11_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

Note:  
Intel DMI supports both Lane  
Reversal and polarity inversion  
but only at PCH side. This is  
enabled via a soft strap.

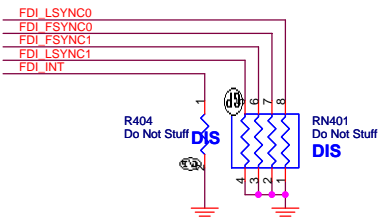
Note:  
Intel FDI supports both Lane  
Reversal and polarity inversion  
but only at PCH side. This is  
enabled via a soft strap.

Note:  
Lane reversal does not apply to  
FDI sideband signals.

Signal Routing Guideline:  
EDP\_ICOMPO keep W/S=12/15 mils and routing  
length less than 500 mils.  
EDP\_COMPIO keep W/S=4/15 mils and routing  
length less than 500 mils.

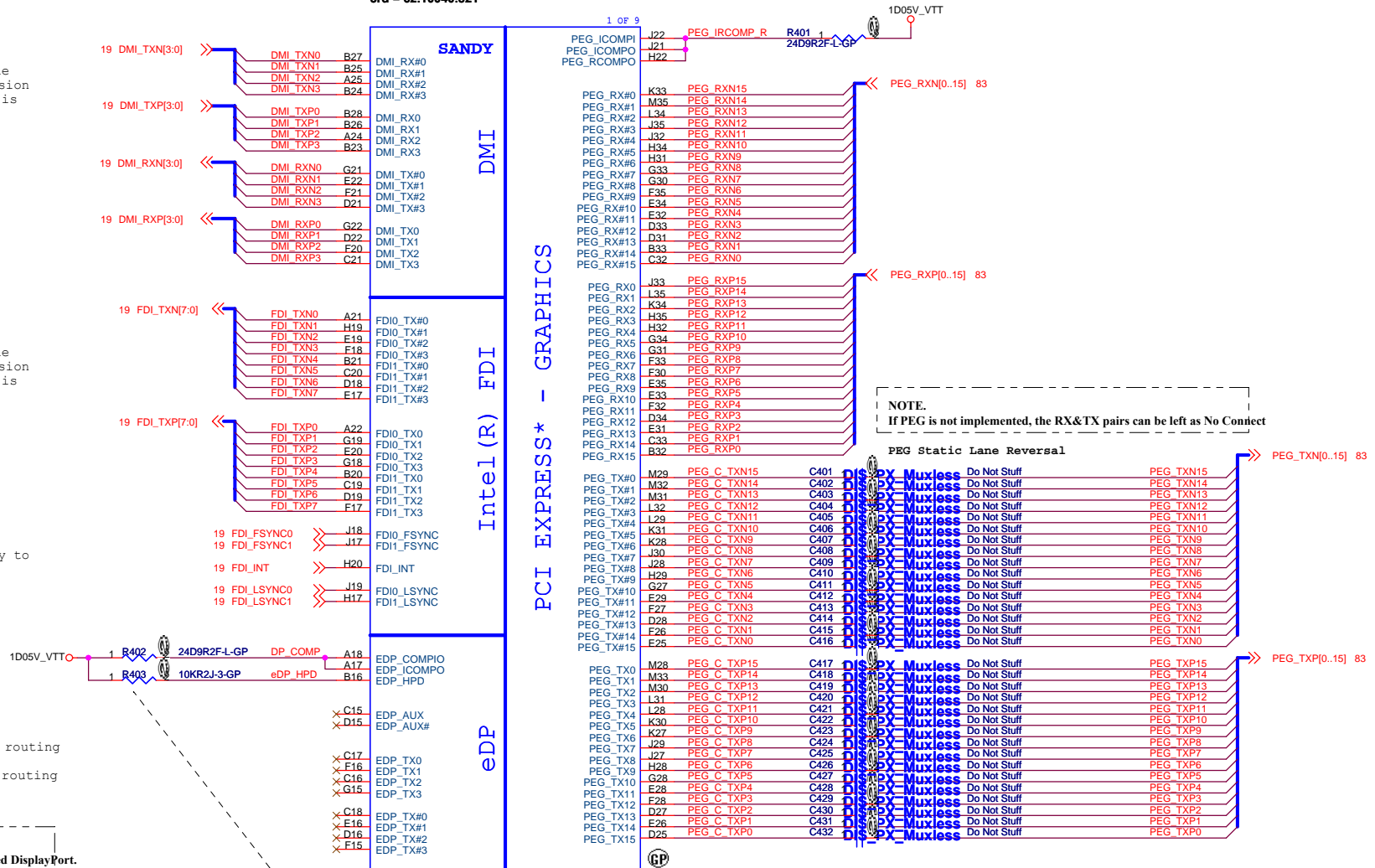
NOTE.  
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics  
function for power saving.



CPU1A  
SANDY  
62.10055.421  
Change:62.10053.611  
2nd = 62.10055.321  
3rd = 62.10040.821

Signal Routing Guideline:  
PEG\_ICOMPO keep W/S=2/15 mils and routing length less than 500 mils.  
PEG\_ICOMPI & PEG\_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

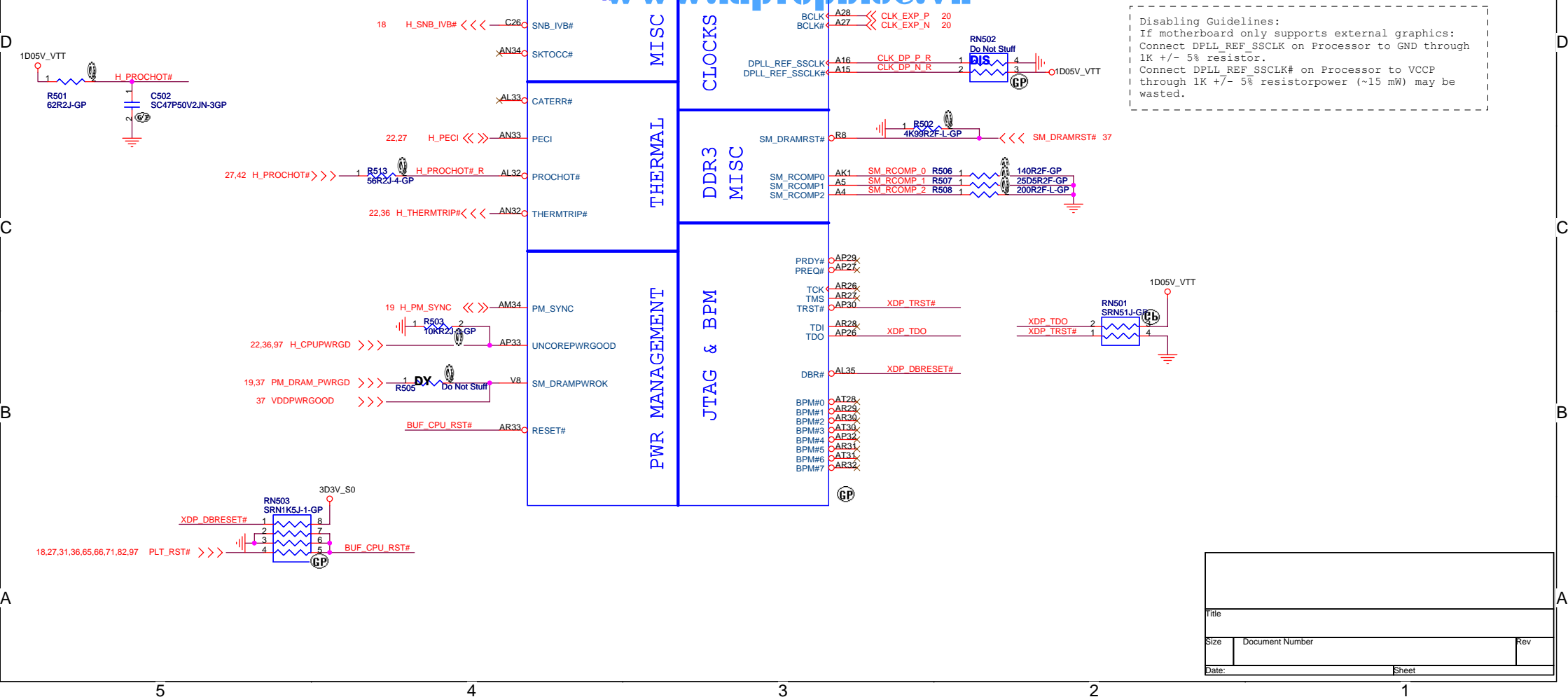


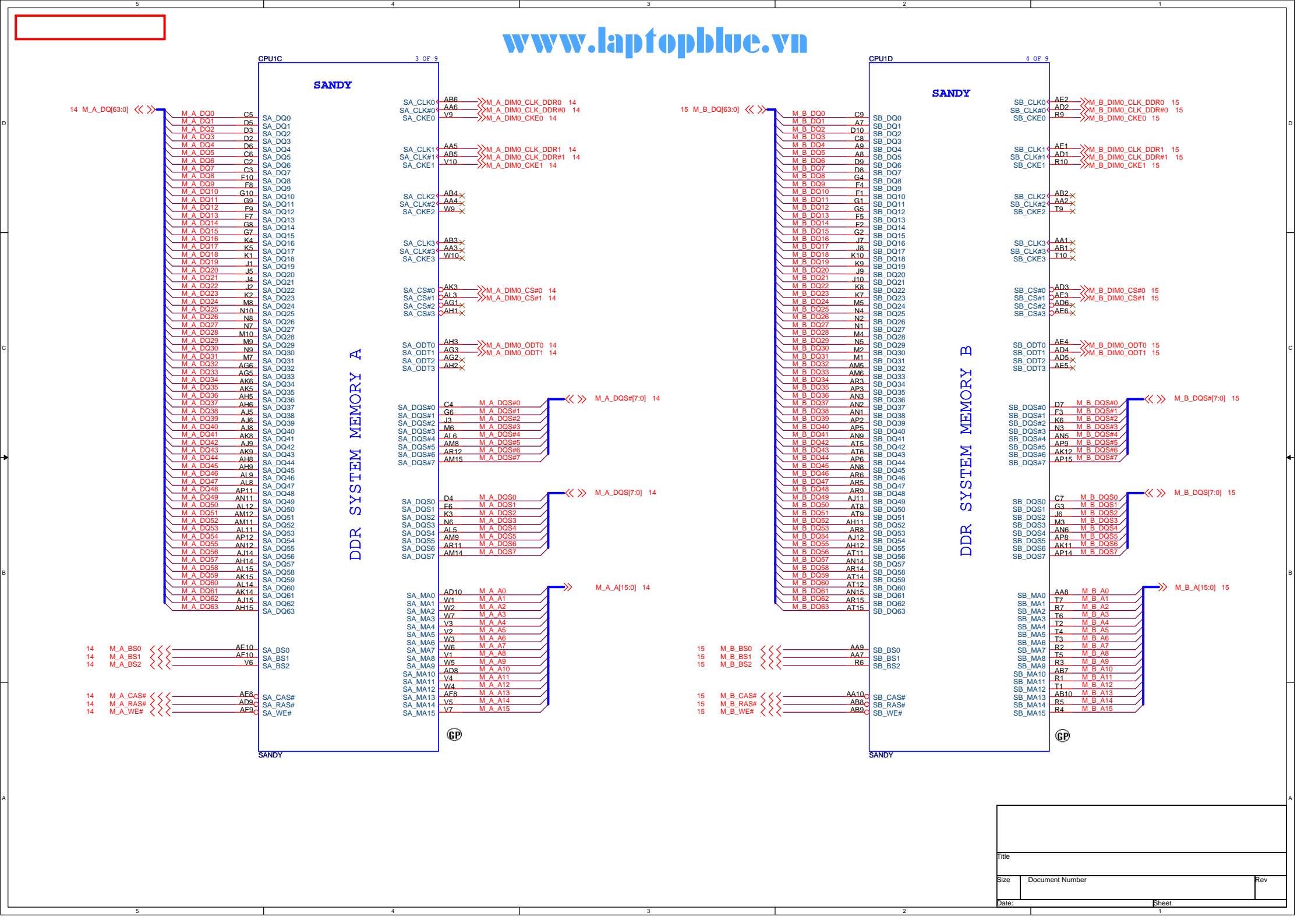
NOTE:  
Select a Fast FET similar to 2N7002E whose rise/  
fall time is less than 6 ns. If HPD on eDP interface is  
disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up  
resistor on the motherboard.

2 OF 9

SANDY

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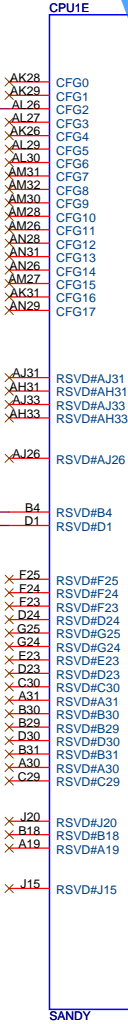
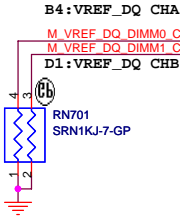




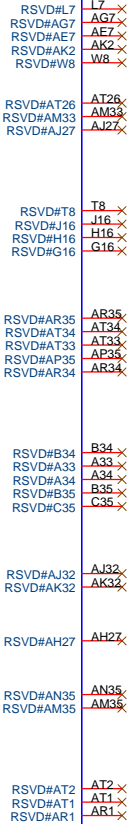


PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

DIS\_PX\_Muxless



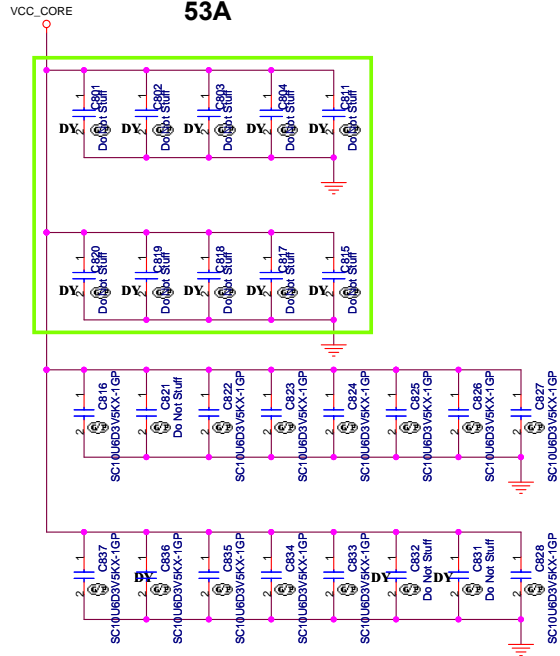
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## PROCESSOR CORE POWER

53A



VCC\_CORE

CPU1F

SANDY

AG35 VCC  
AG34 VCC  
AG33 VCC  
AG32 VCC  
AG31 VCC  
AG30 VCC  
AG29 VCC  
AG28 VCC  
AG27 VCC  
AG26 VCC  
AF35 VCC  
AF34 VCC  
AF33 VCC  
AF32 VCC  
AF31 VCC  
AF30 VCC  
AF29 VCC  
AF28 VCC  
AF27 VCC  
AF26 VCC  
AD35 VCC  
AD34 VCC  
AD33 VCC  
AD32 VCC  
AD31 VCC  
AD30 VCC  
AD29 VCC  
AD28 VCC  
AD27 VCC  
AD26 VCC  
AC35 VCC  
AC34 VCC  
AC33 VCC  
AC32 VCC  
AC31 VCC  
AC30 VCC  
AC29 VCC  
AC28 VCC  
AC27 VCC  
AC26 VCC  
AA35 VCC  
AA34 VCC  
AA33 VCC  
AA32 VCC  
AA31 VCC  
AA30 VCC  
AA29 VCC  
AA28 VCC  
AA27 VCC  
AA26 VCC  
Y35 VCC  
Y34 VCC  
Y33 VCC  
Y32 VCC  
Y31 VCC  
Y30 VCC  
Y29 VCC  
Y28 VCC  
Y27 VCC  
Y26 VCC  
V34 VCC  
V33 VCC  
V32 VCC  
V31 VCC  
V30 VCC  
V29 VCC  
V28 VCC  
V27 VCC  
V26 VCC  
U35 VCC  
U34 VCC  
U33 VCC  
U32 VCC  
U31 VCC  
U30 VCC  
U29 VCC  
U28 VCC  
U27 VCC  
U26 VCC  
R35 VCC  
R34 VCC  
R33 VCC  
R32 VCC  
R31 VCC  
R30 VCC  
R29 VCC  
R28 VCC  
R27 VCC  
R26 VCC  
P35 VCC  
P34 VCC  
P33 VCC  
P32 VCC  
P31 VCC  
P30 VCC  
P29 VCC  
P28 VCC  
P27 VCC  
P26 VCC

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VIDALERT# H\_CPU\_SVIDALRT# 1 R803 43R2J-GP VR\_SVID\_ALERT# 42  
VIDSCLK H\_CPU\_SVIDCLK 42  
VIDSOUT H\_CPU\_SVIDDAT 42

For CRB VIDSOUT need to pull high 130 ohm close to CPU and IMVP7  
For CRB VIDALERT# need to pull high 75 ohm close to CPU

H\_CPU\_SVIDDAT R804 1 130R2F-1-GP

VCC\_SENSE  
VSS\_SENSE

VCCIO\_SENSE  
VSSIO\_SENSE

GP

VCC\_CORE

R801  
100R2F-L1-GP-U

R802  
100R2F-L1-GP-U

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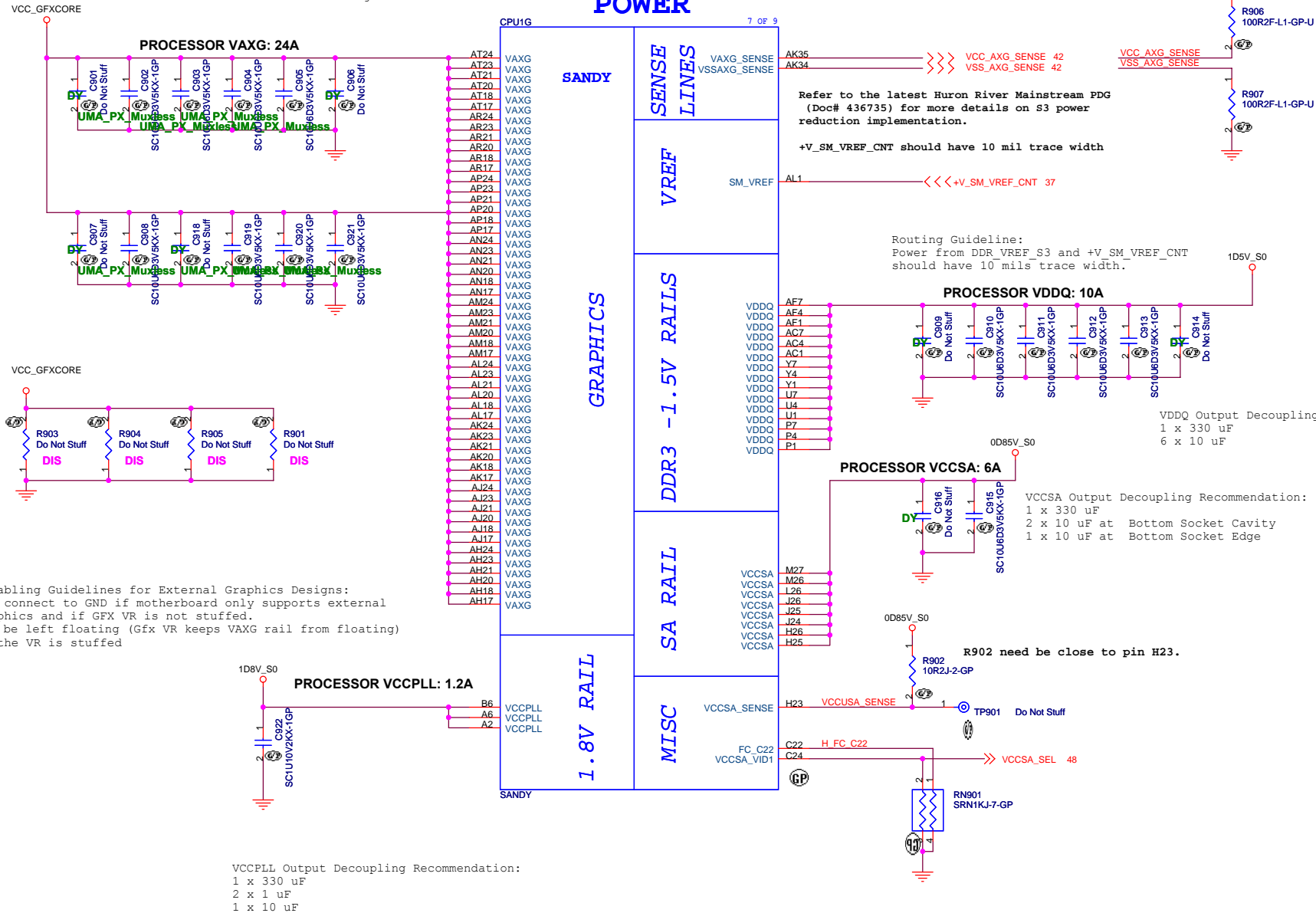
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Date:

Sheet



## POWER



Disabling Guidelines for External Graphics Designs:  
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.  
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

VCCPLL Output Decoupling Recommendation:  
1 x 330 uF  
2 x 1 uF  
1 x 10 uF

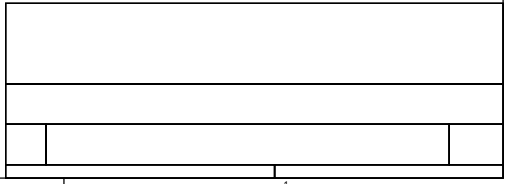
Routing Guideline:  
Power from DDR\_VREF\_S3 and +V\_SM\_VREF\_CNT  
should have 10 mils trace width.

VDDQ Output Decoupling Recommendation:  
1 x 330 uF  
6 x 10 uF

VCCSA Output Decoupling Recommendation:  
1 x 330 uF  
2 x 10 uF at Bottom Socket Cavity  
1 x 10 uF at Bottom Socket Edge

R902 need be close to pin H23.

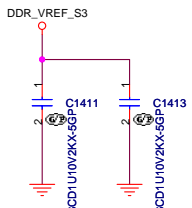
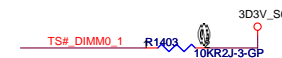




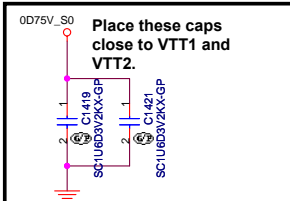
—<> M\_A\_A[15:0] 6

**Note:**  
 If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
 SO-DIMMA SPD Address is 0xA0  
 SO-DIMMA TS Address is 0x30  
  
 If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
 SO-DIMMA SPD Address is 0xA2  
 SO-DIMMA TS Address is 0x32

## Thermal EVENT



-2



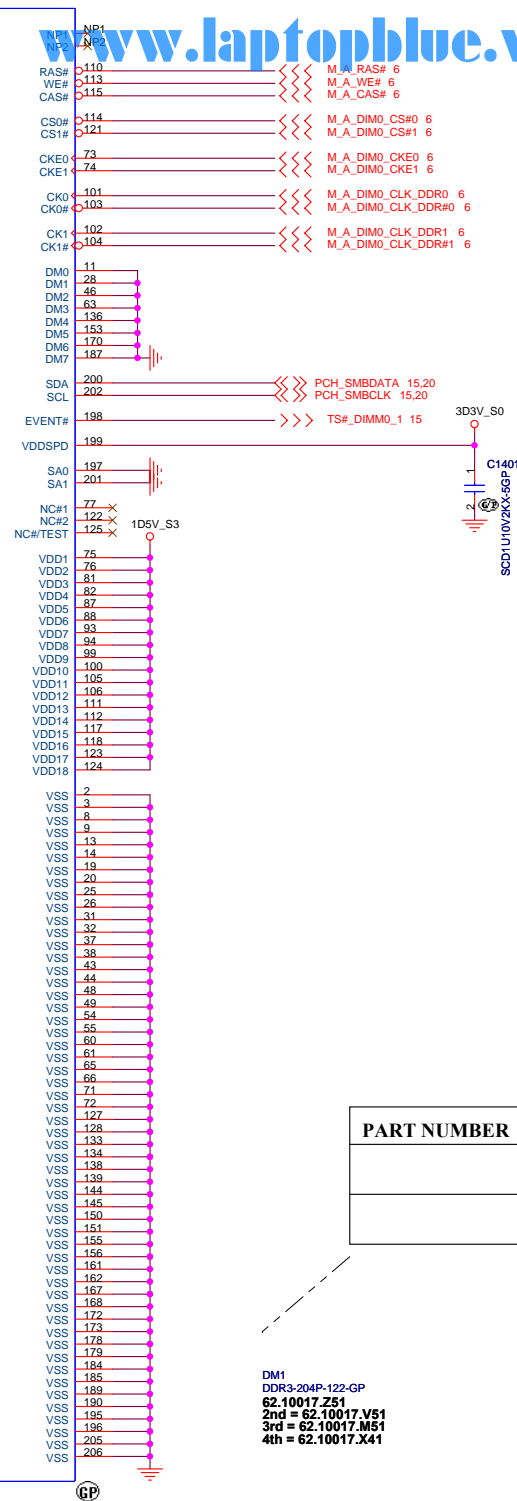
—<< >> M\_A\_DQS#[7:0] 6  
—<< >> M\_A\_DQS[7:0] 6

```

6 M_A_DIM0_ODT0 >>>
6 M_A_DIM0_ODT1 >>>

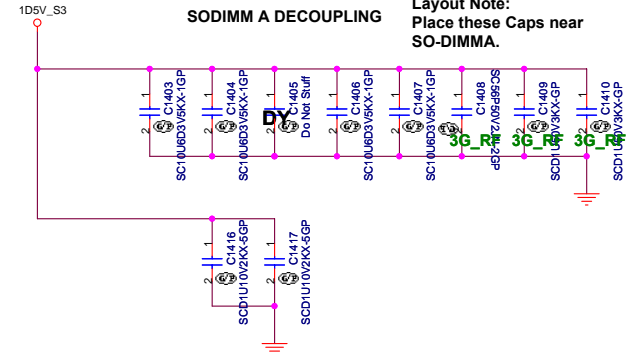
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15,37 DDR3\_DRAMRST# &gt;&gt;&gt;



## SODIMM A DECOUPLING

**Layout Note:**  
Place these Caps near  
SO-DIMMA.



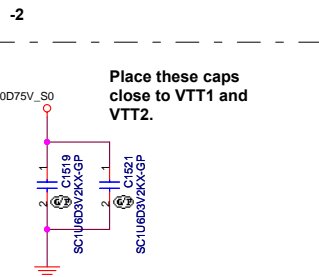
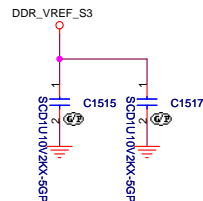
PART NUMBER	Height	TYPE

DM1  
DDR3-204P-122-GP  
62.10017.Z51  
2nd = 62.10017.V51  
3rd = 62.10017.M51  
4th = 62.10017.X41

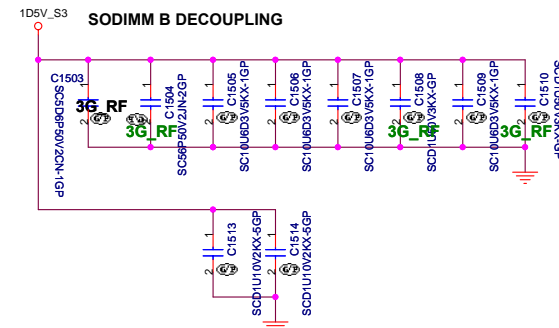
**SSID = MEMORY**

NP1 NP2

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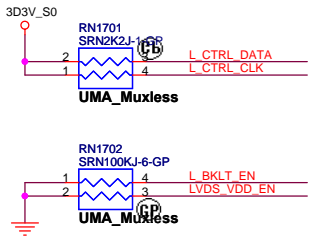
**Layout Note:**  
Place these Caps near  
SO-DIMMB.



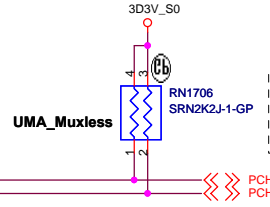
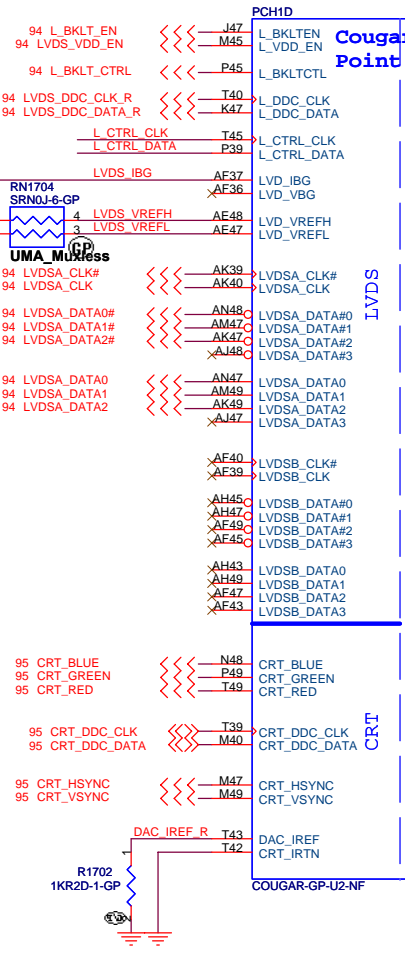
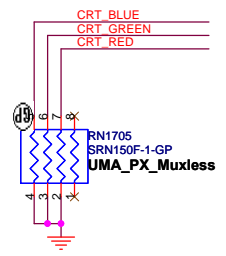
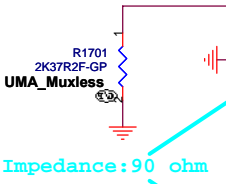
DM2  
DDR3-204P-126-GP  
**62.10024.D41**

2nd = 62.10017.R91  
3rd = 62.10017.V61  
4th = 62.10017.X51

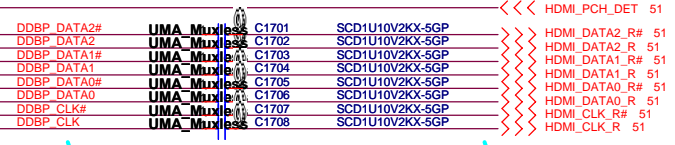
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L\_DDC\_DATA(PAGE17):  
This signal is on the LVDS interface.  
This signal needs to be left NC if eDP is  
used for the local flat panel display



DDI Port B Detect:(SDVO\_CTRL\_DATA)  
1: Port B detected  
0: Port B not detected



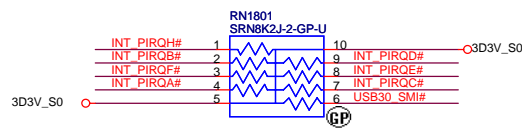
Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPDP	NA	DDPB_HPDP	HDMIIB_HPDP
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIIB_CTRLDATA
	DDPB_0N	SDVO_RED	DDPB_0N	TMDSB_DATA2
	DDPB_0P	SDVO_RED#	DDPB_0P	TMDSB_DATA2#
	DDPB_1N	SDVO_GREEN	DDPB_1N	TMDSB_DATA1

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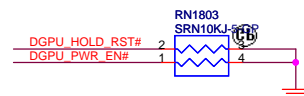
SSID = PCH

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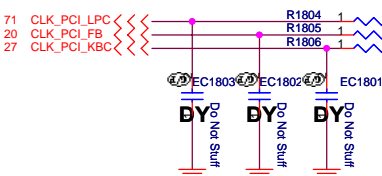
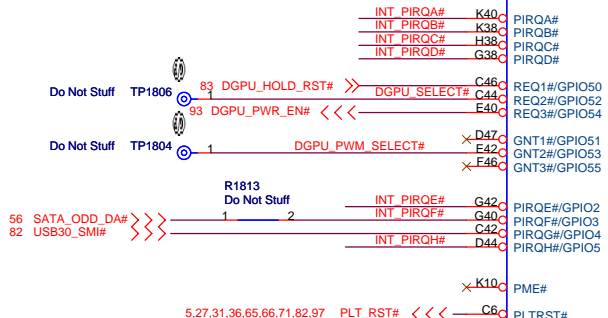


Al6 swap override Strap/Top-Block Swap Override jumper

PCI\_GNT#3 Low = Al6 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
		SPI(Default)



OC[3:0]# for Device 29 (Ports 0-7)  
OC[7:4]# for Device 26 (Ports 8-13)

Cougar Point

NVRAM

RSVD

PCI

USB

5 OF 10

RSVD  
TP1  
TP2  
TP3  
TP4  
TP5  
TP6  
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TP38  
TP39  
TP40

RSVD  
TP1  
TP2  
TP3  
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TP7  
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TP35  
TP36  
TP37  
TP38  
TP39  
TP40

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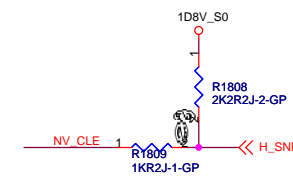
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DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



USB Ext. port 1 (HS)  
External debug port use on Huron river platform

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

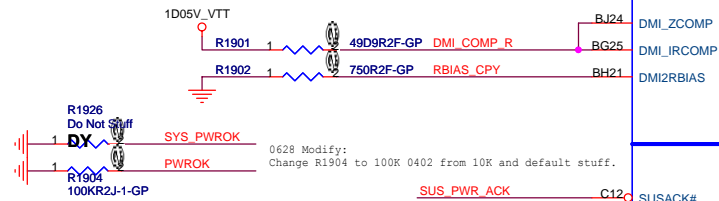
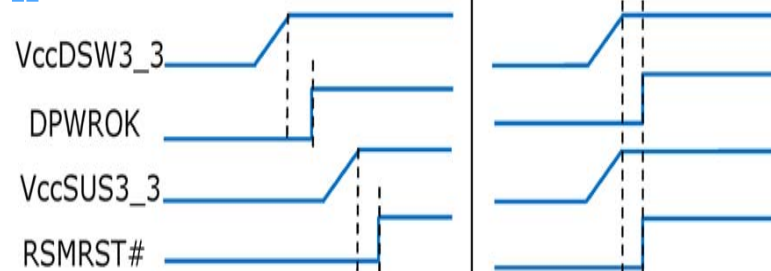
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4 DMI\_RXN[3:0] <<>>====  
4 DMI\_RXP[3:0] <<>>====

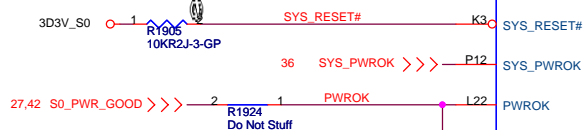
4 DMI\_TXN[3:0] <<>>====  
4 DMI\_TXP[3:0] <<>>====

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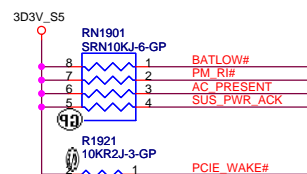
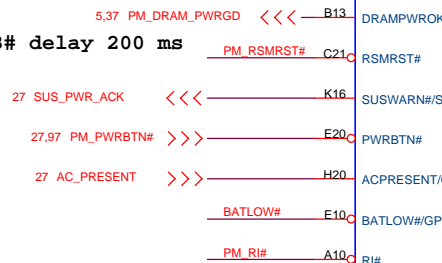
Deep S4/S5 **Not** Supported



0628 Modify:  
Change R1904 to 100K 0402 from 10K and default stuff.

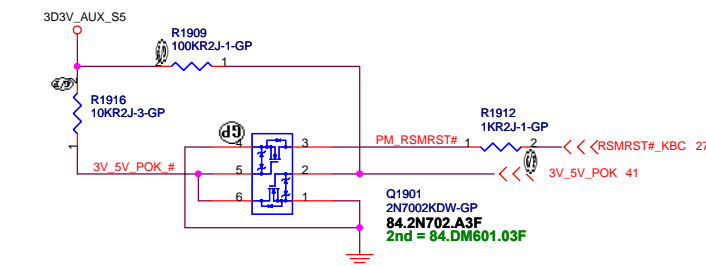
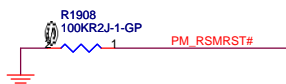


S0\_PWR\_GOOD after PM\_SLP\_S3# delay 200 ms



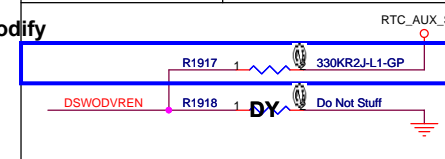
```
PCIE_WAKE#
CRB : 1K
CEKLT: 10K
```

**PWRBTN#**  
This signal has an internal pull-up resistor

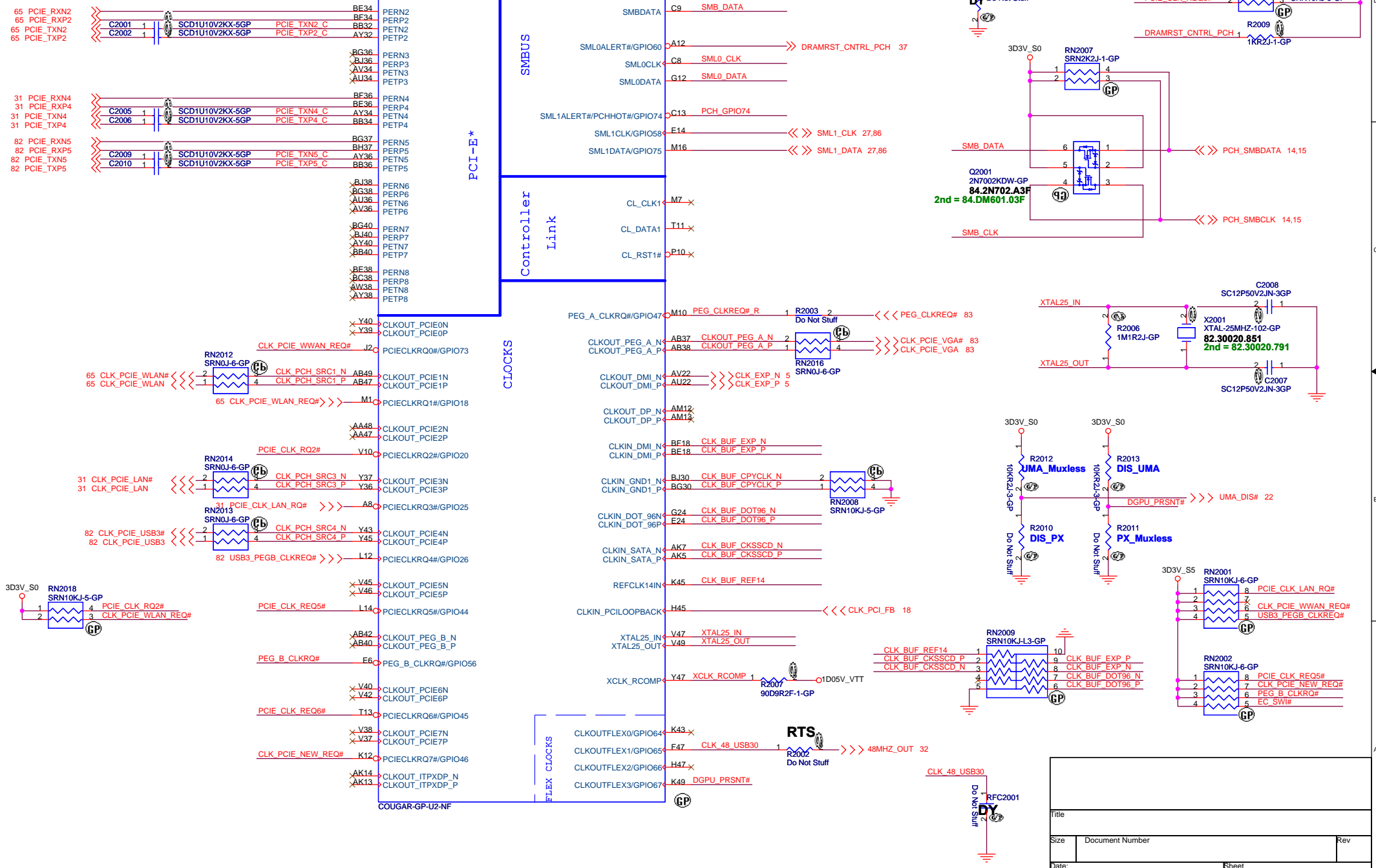


DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SB modify



Title	
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Date	Sheet

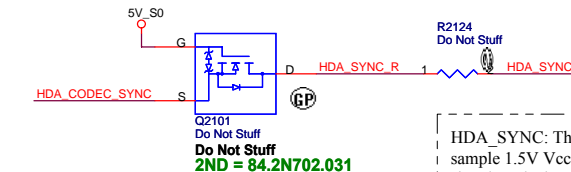
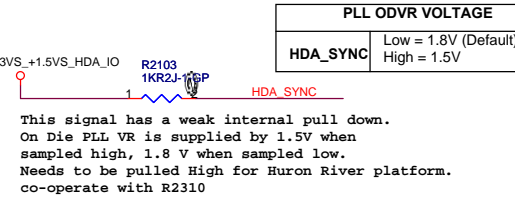
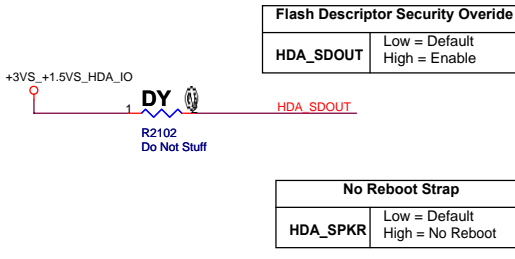
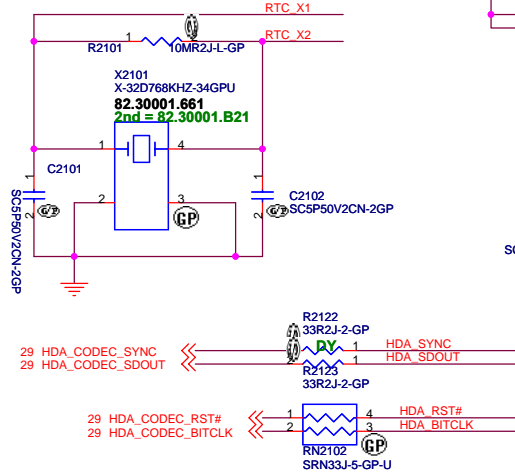




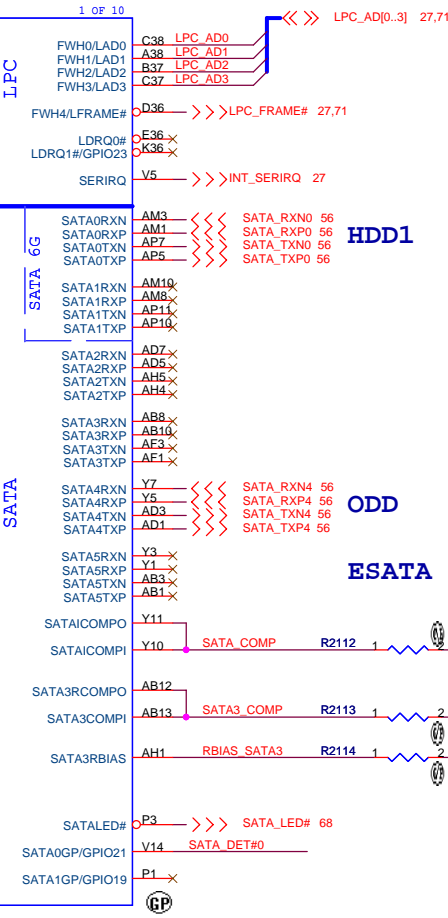
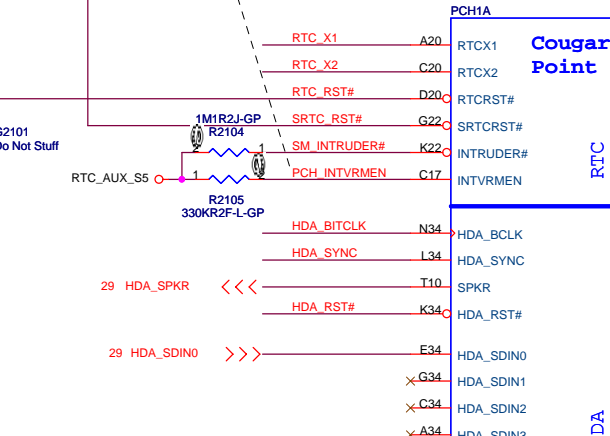
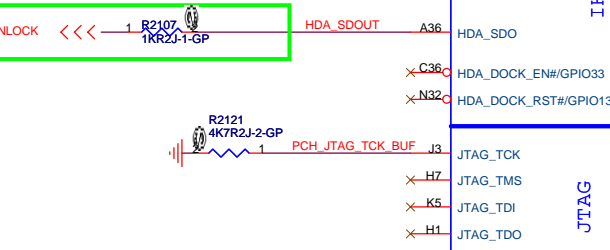
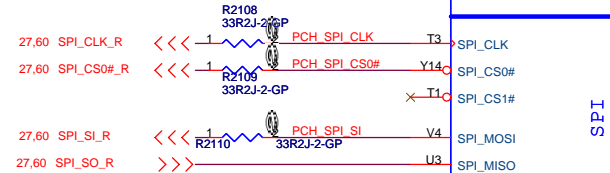
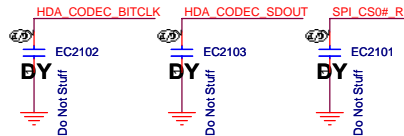
SSID = PCH

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INTVRMEN- Integrated SUS  
1.05V VRM Enable  
High - Enable internal VRs  
Low - Enable external VRs

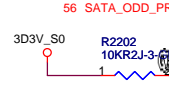
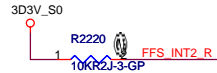
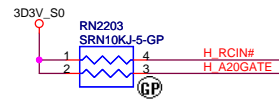


HDA\_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA\_SYNC from the Audio Codec device until after the Strap sampling is complete.

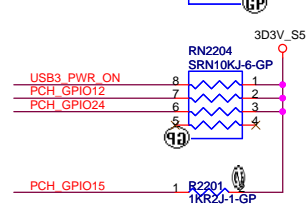
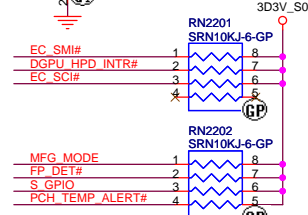


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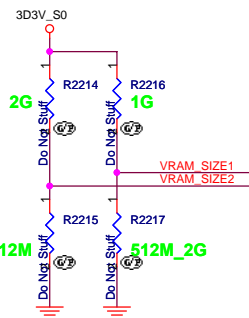
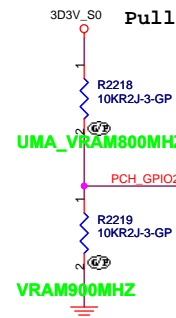
Note:  
For PCH debug with XDP, need to NO STUFF R2218



	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

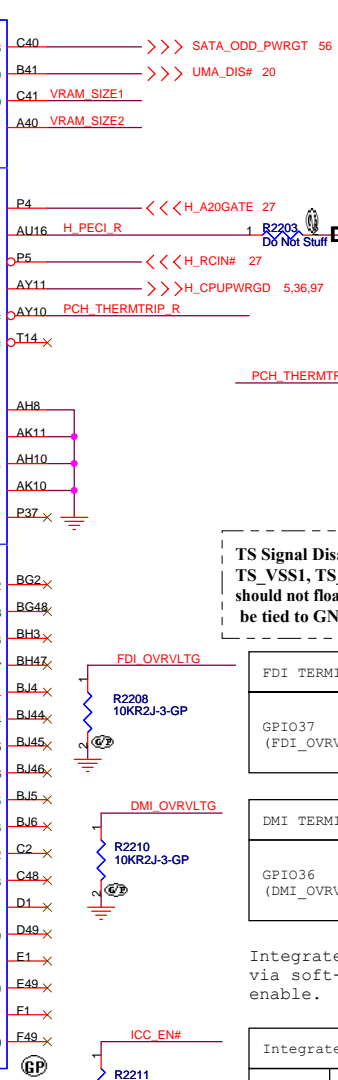
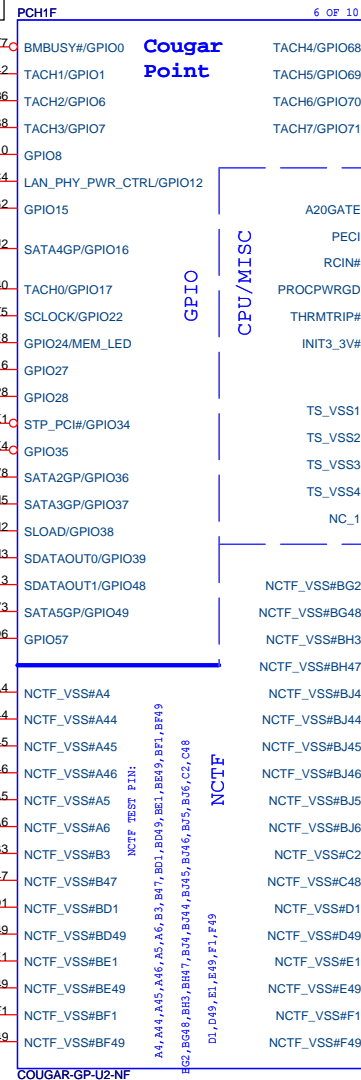


VRAM Frequency  
Pull high: 800MHZ  
Pull low :900MHZ



1G\_512M 512M\_2G

PLL ON DIE VR ENABLE  
NOTE: This signal has a weak internal pull-up 20K  
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT  
DISABLED -- LOW (R2212 STUFFED)



TS Signal Disable Guideline:  
TS\_VSS1, TS\_VSS2, TS\_VSS3 and TS\_VSS4  
should not float on the motherboard. They should  
be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPI037 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

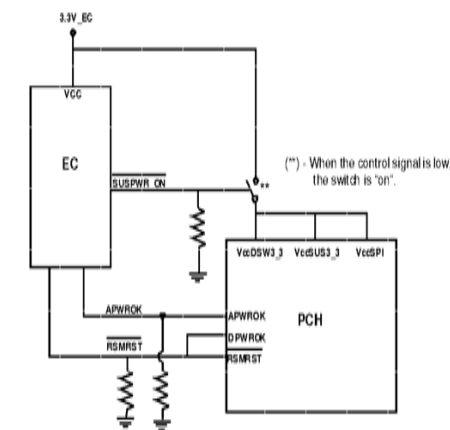
DMI TERMINATION VOLTAGE OVERRIDE	
GPI036 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

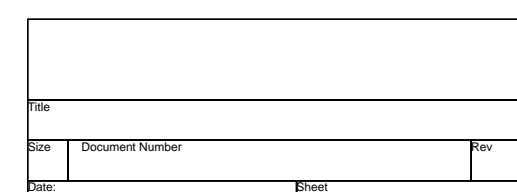
Integrated Clock Enable functionality is achieved  
via soft-strap. The default is integrated clock  
enable.

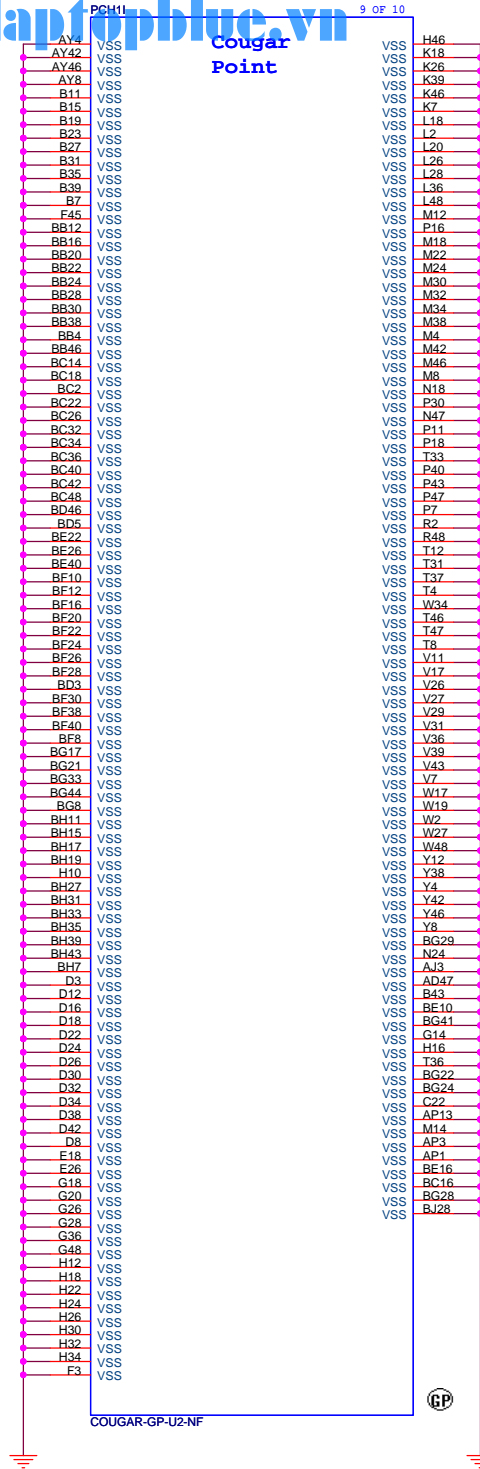
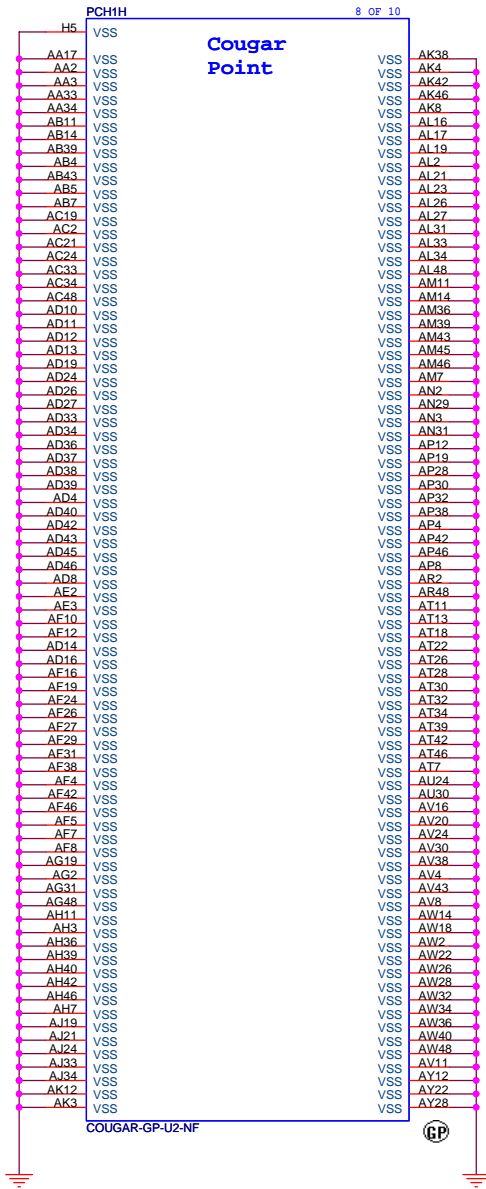
Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT] LOW (R2211) - ENABLED

GPI08 has a weak[20K] internal pull up.  
Integrated Clock Enable functionality is achieved  
via soft-strap. The default is integrated clock  
enable.

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Date:	Sheet

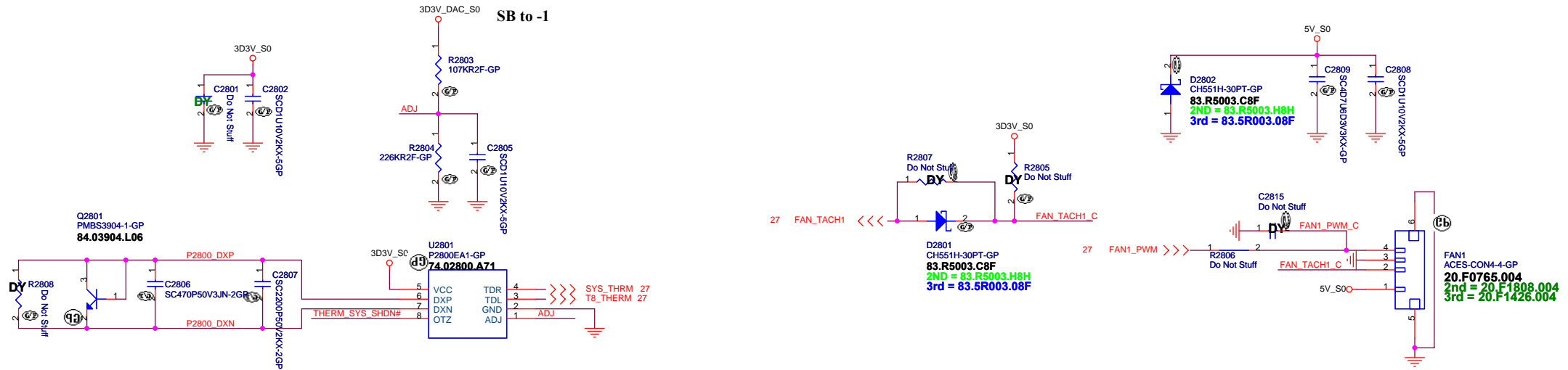






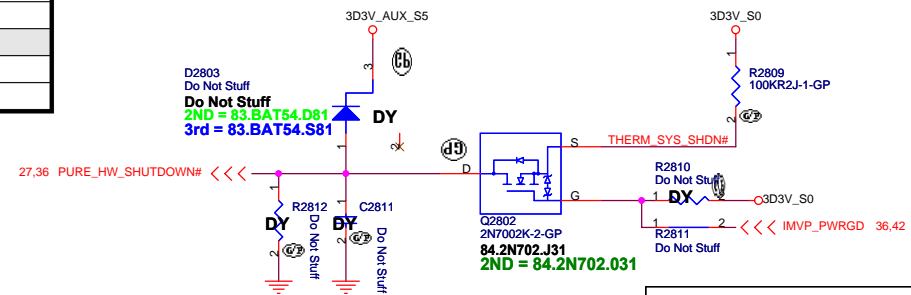
Title		
Size	Document Number	Rev
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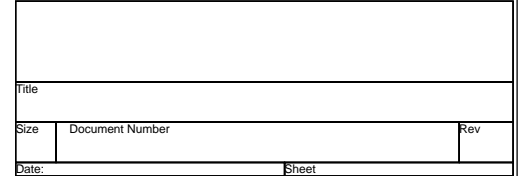
ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

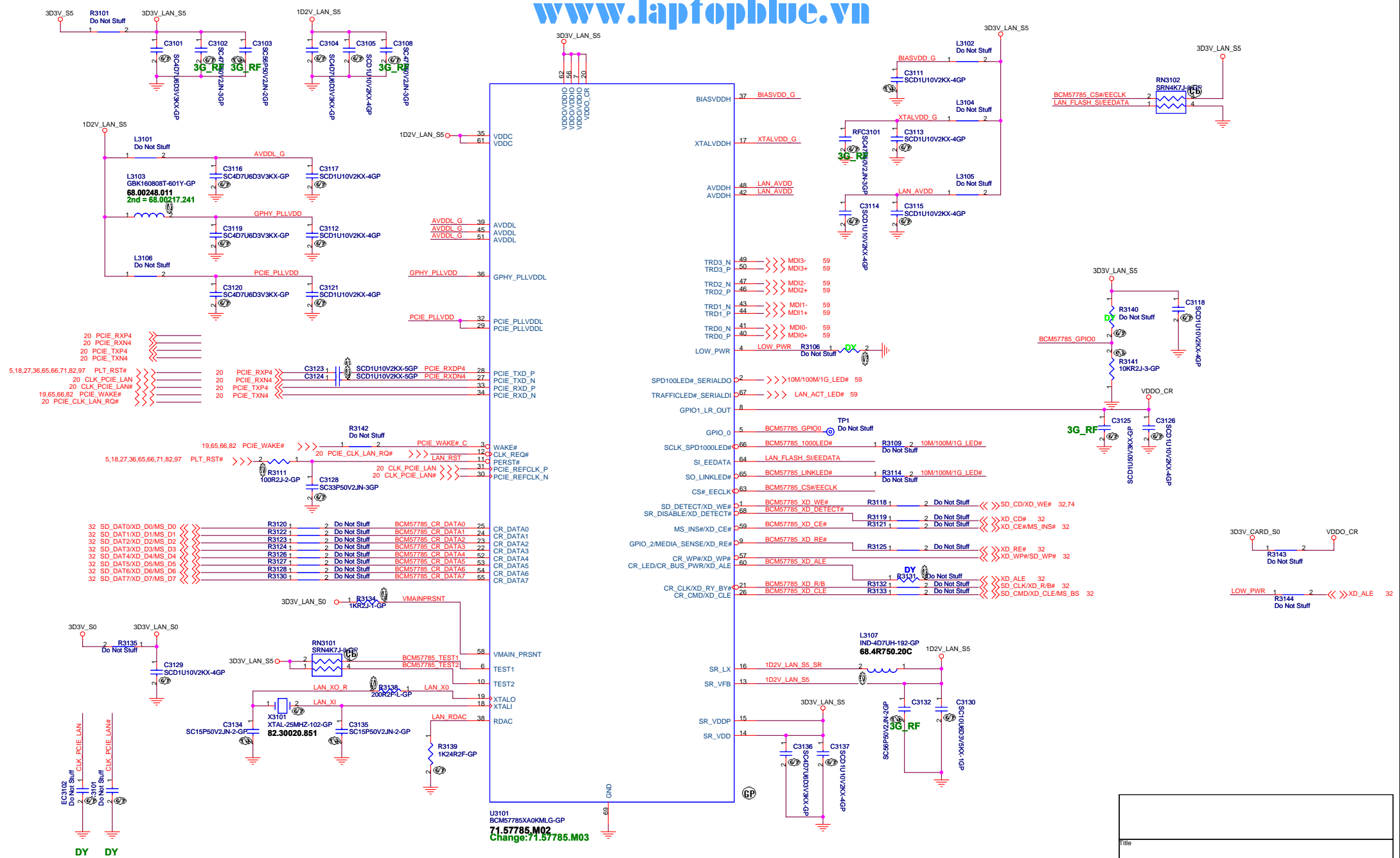
RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9



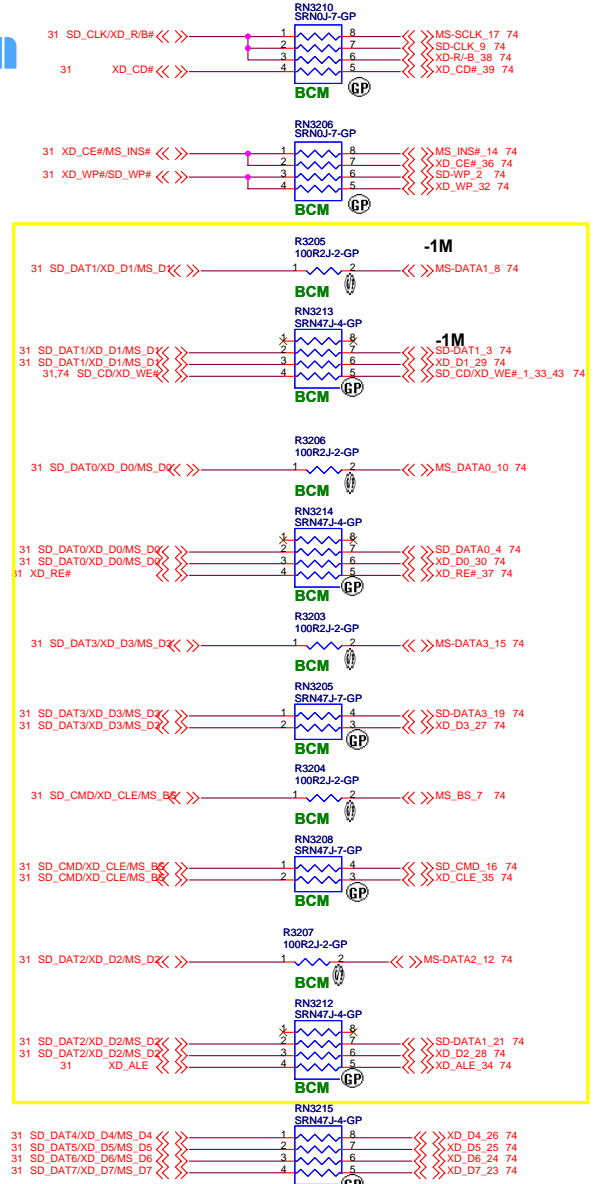
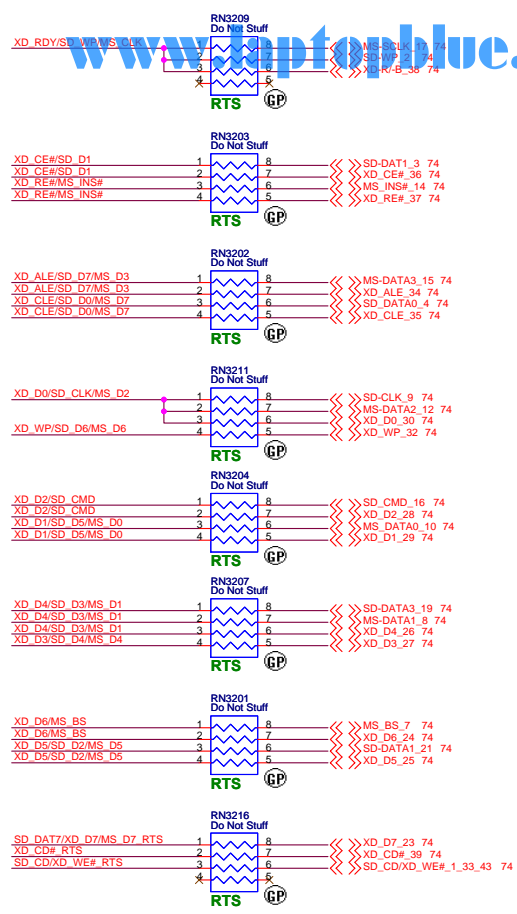
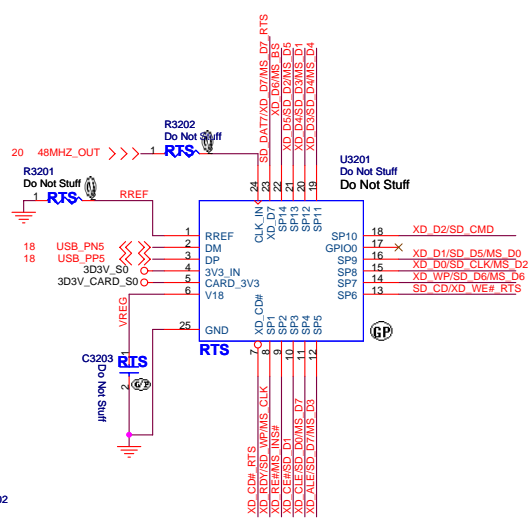
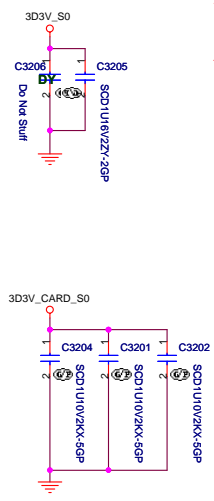


CLOSE TO PIN39 and 46

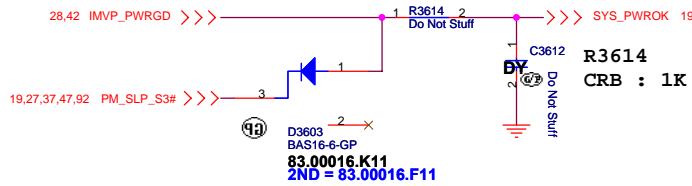




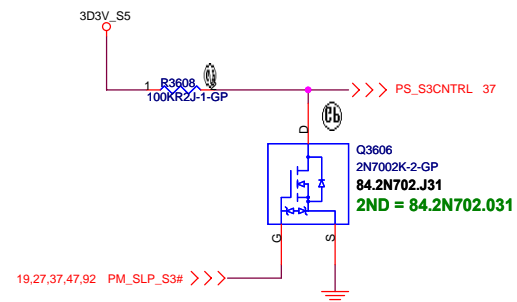
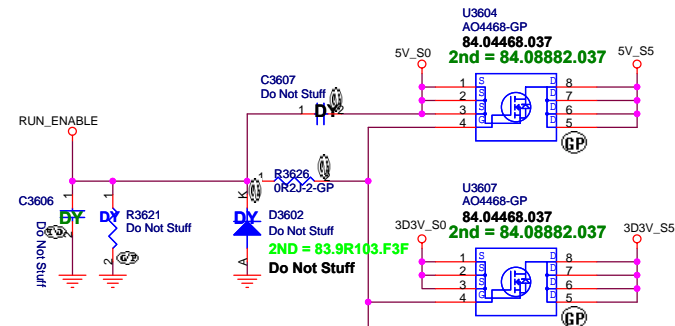
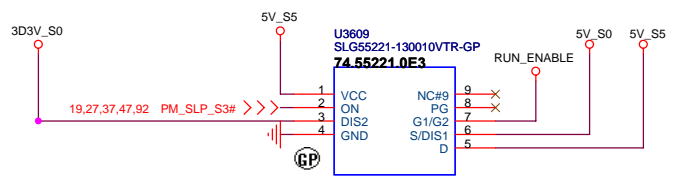
Title		
Size	Document Number	Rev
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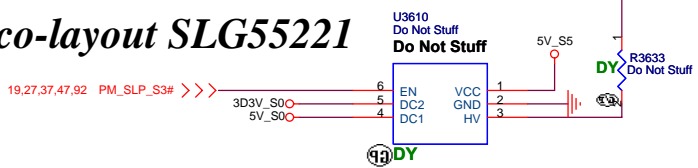
Title		
Size	Document Number	Rev
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# ANNIE Run Power



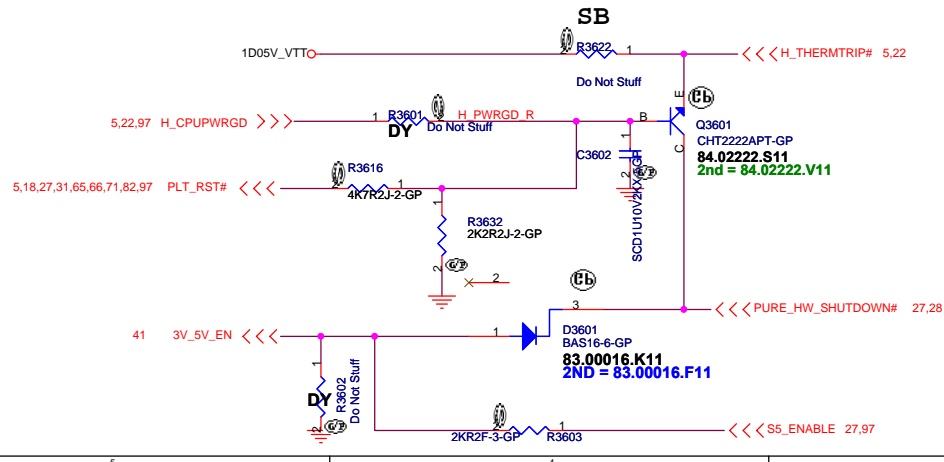
## -1 co-layout SLG55221



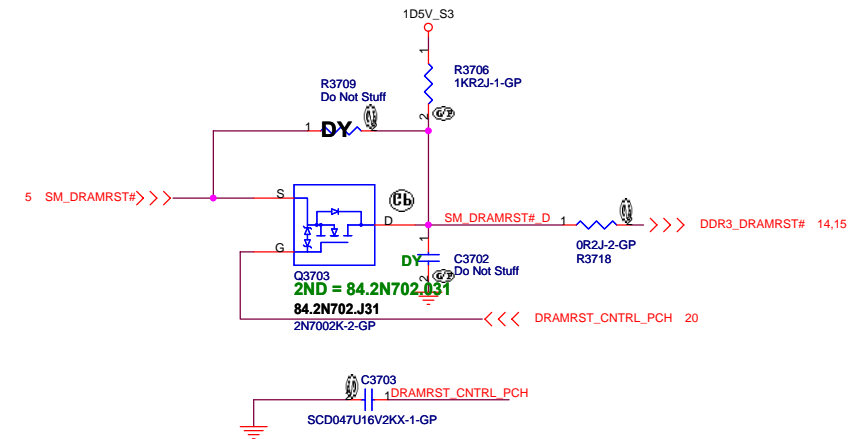
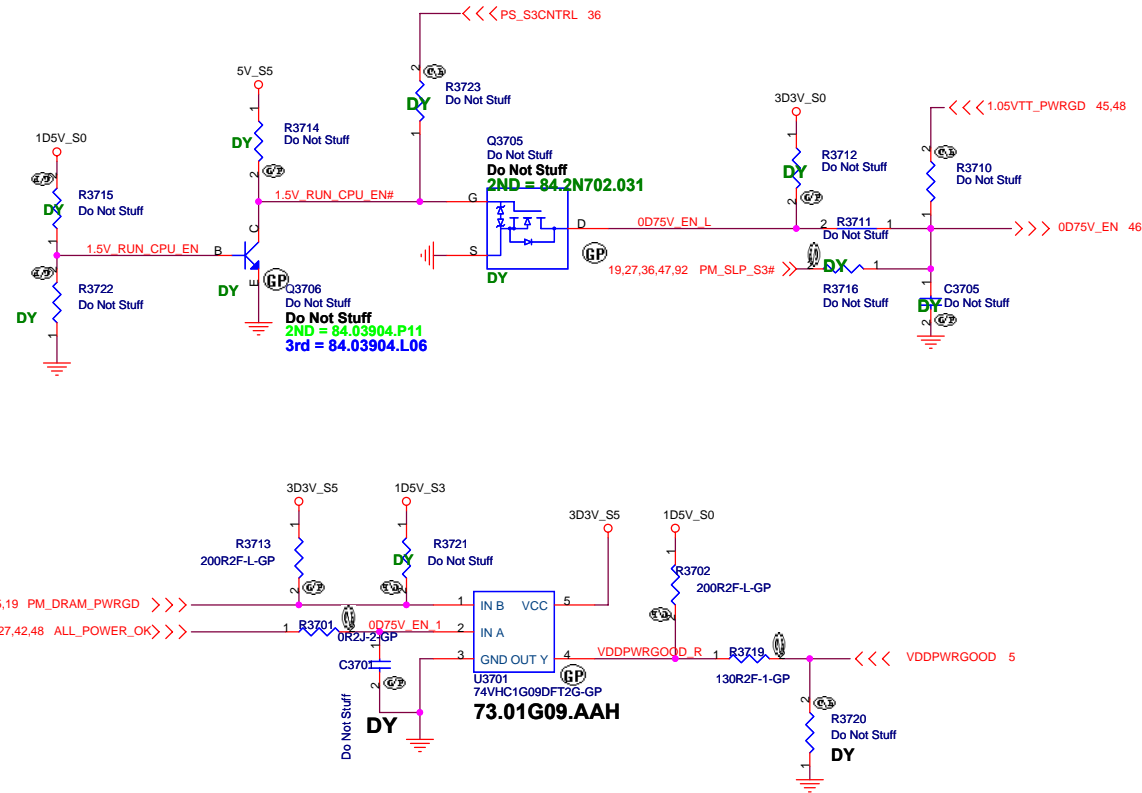
-1 modify R3621,D3602 to DY

SB modify part number

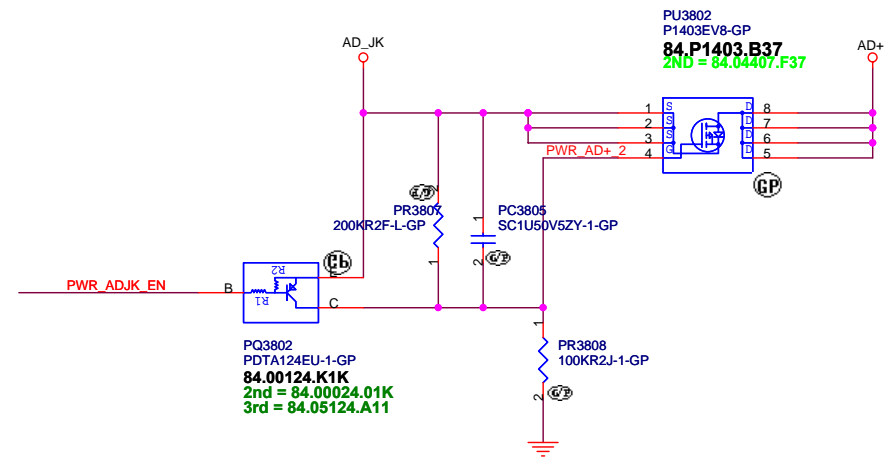
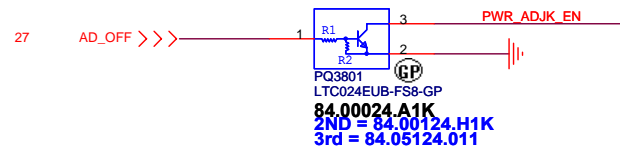
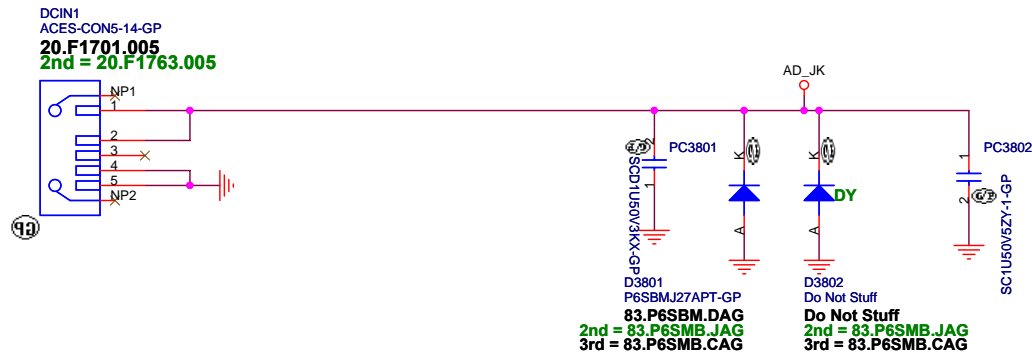
1D5V\_S0  
MAX Current 3000 mA  
Design Current 2100 mA  
Total= 11.39A



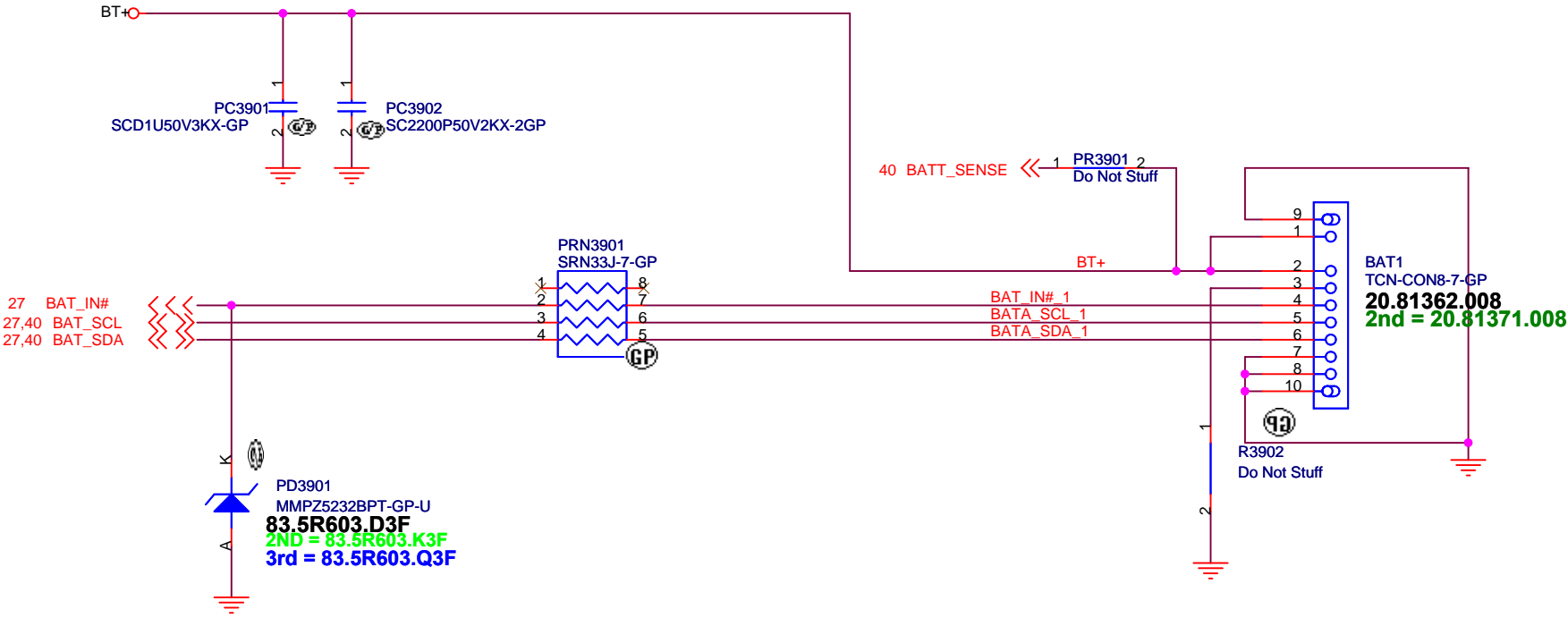
Title		
Size	Document Number	Rev
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Title	
Size	Document Number
Date:	Sheet



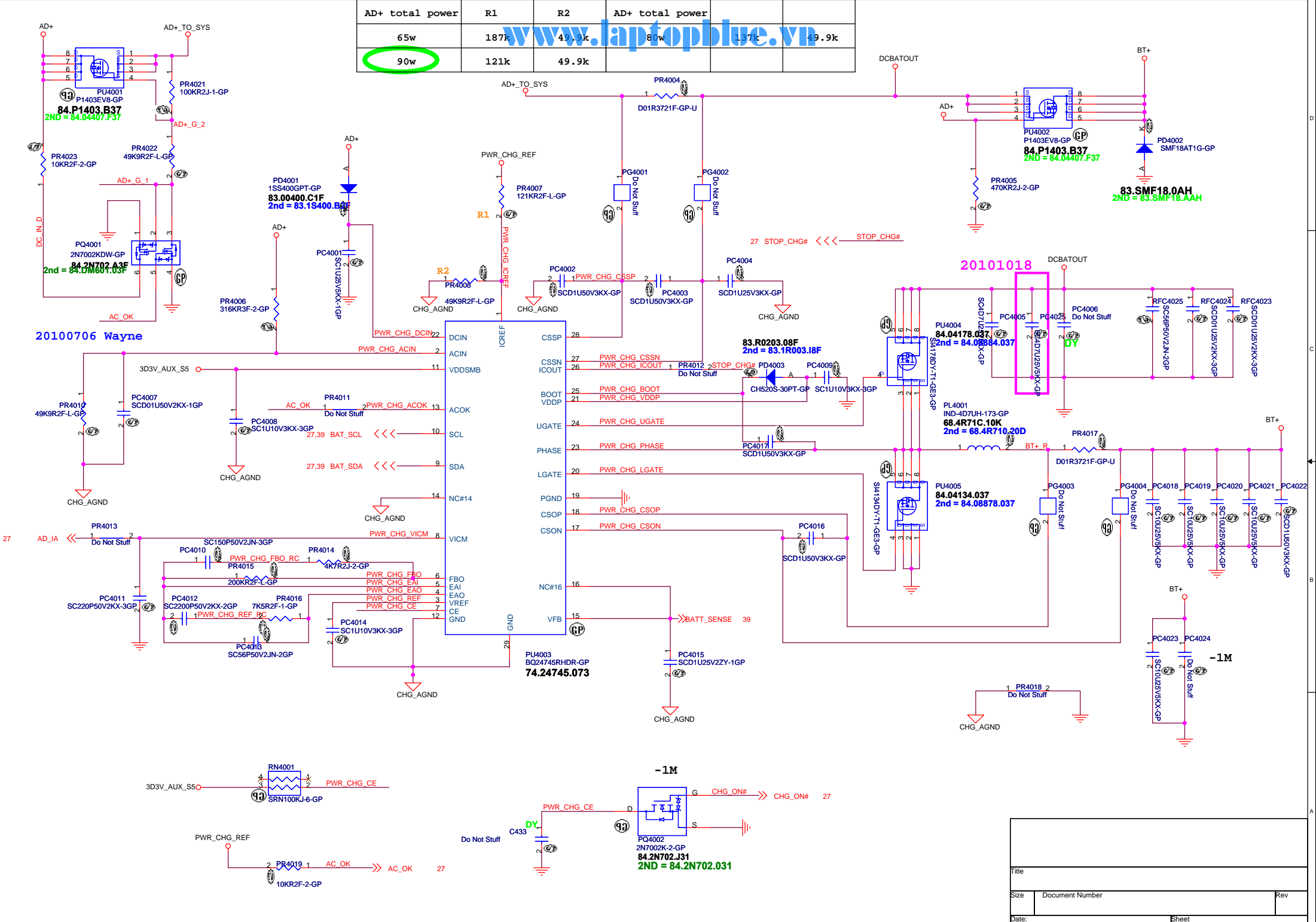
Title		
Size	Document Number	Rev
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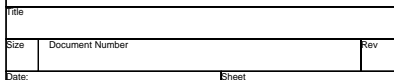
Title		
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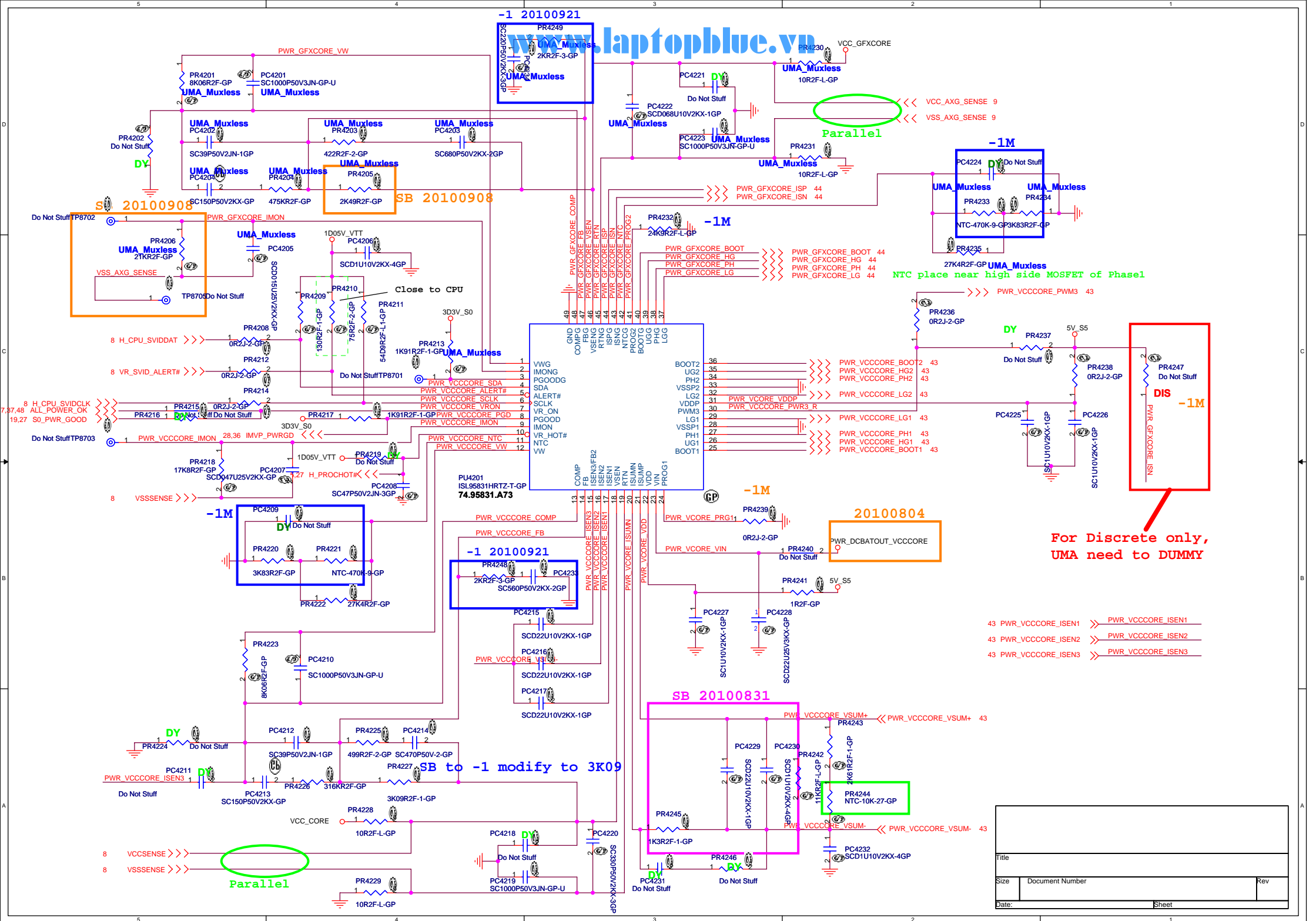


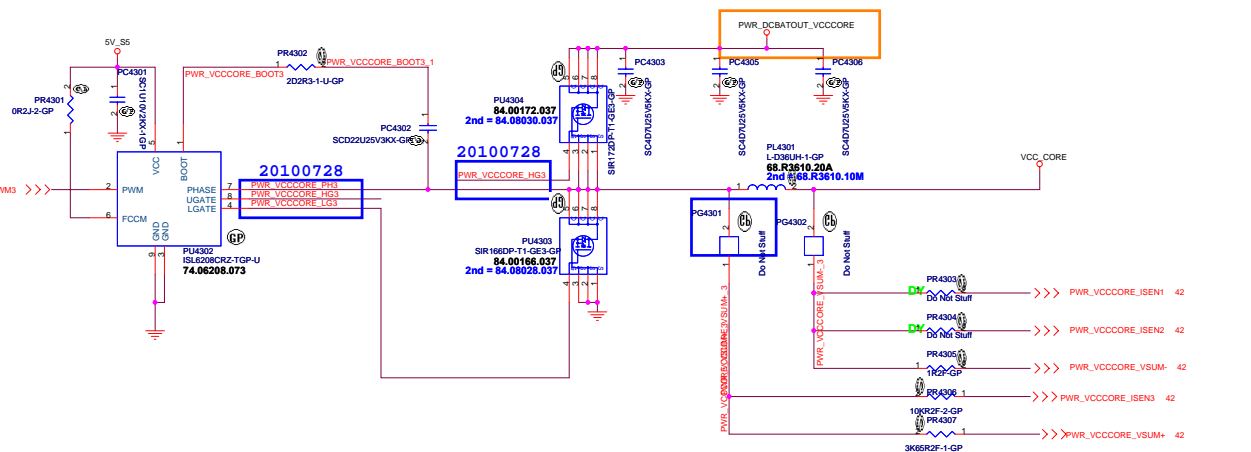
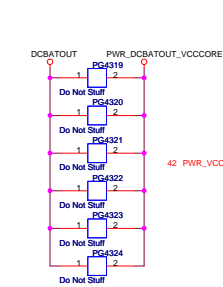
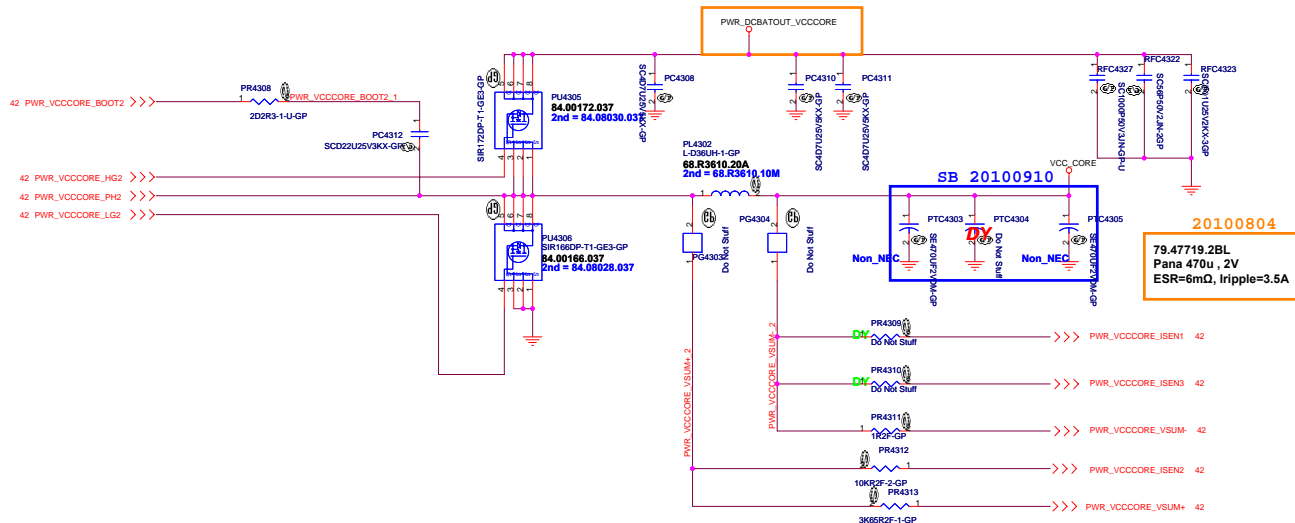
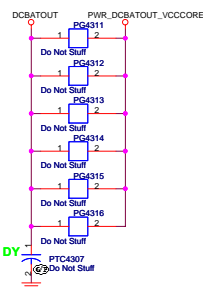
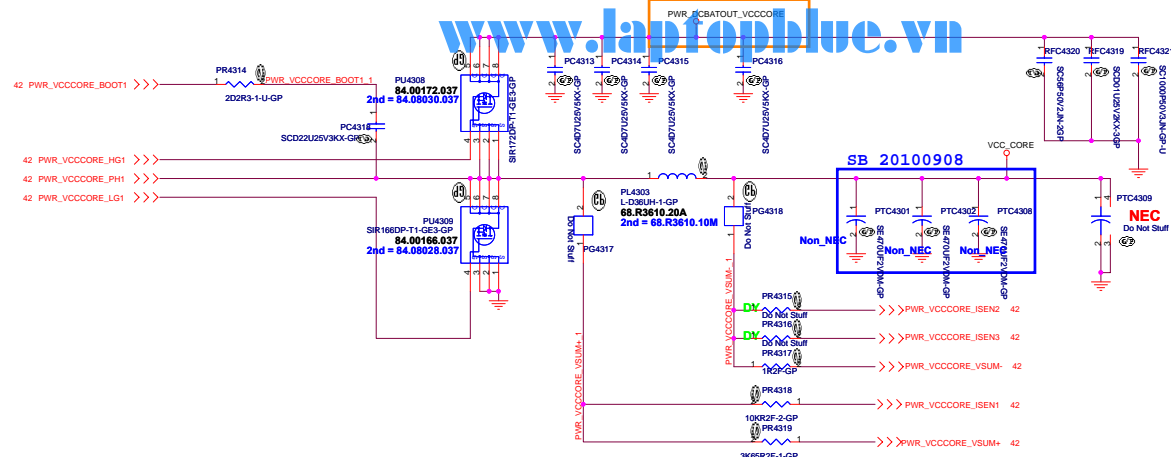
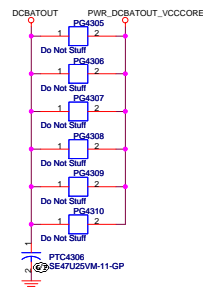
AD+ total power	R1	R2	AD+ total power		
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			



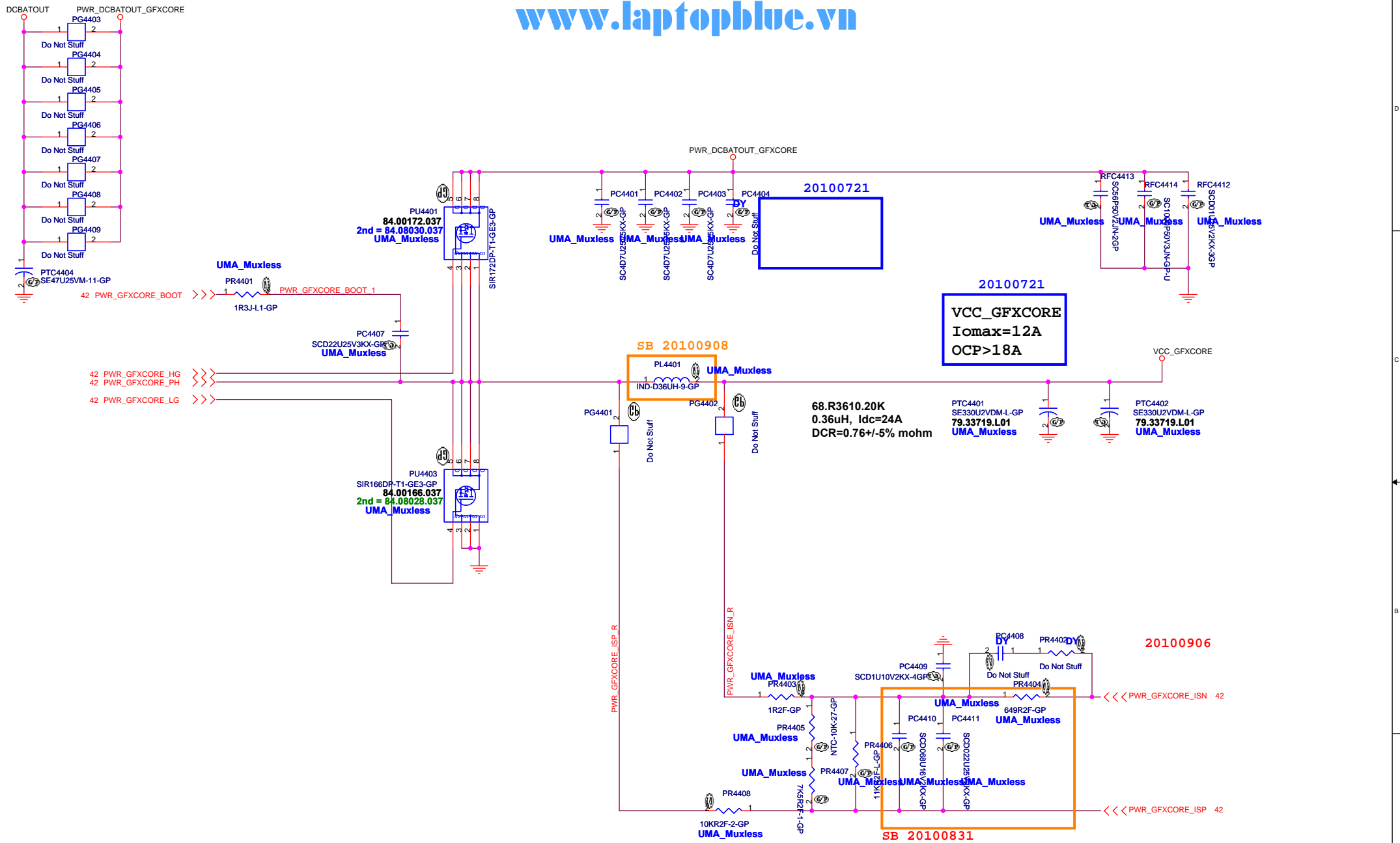
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**+0.75VS**  
**Iomax: 1.2A**

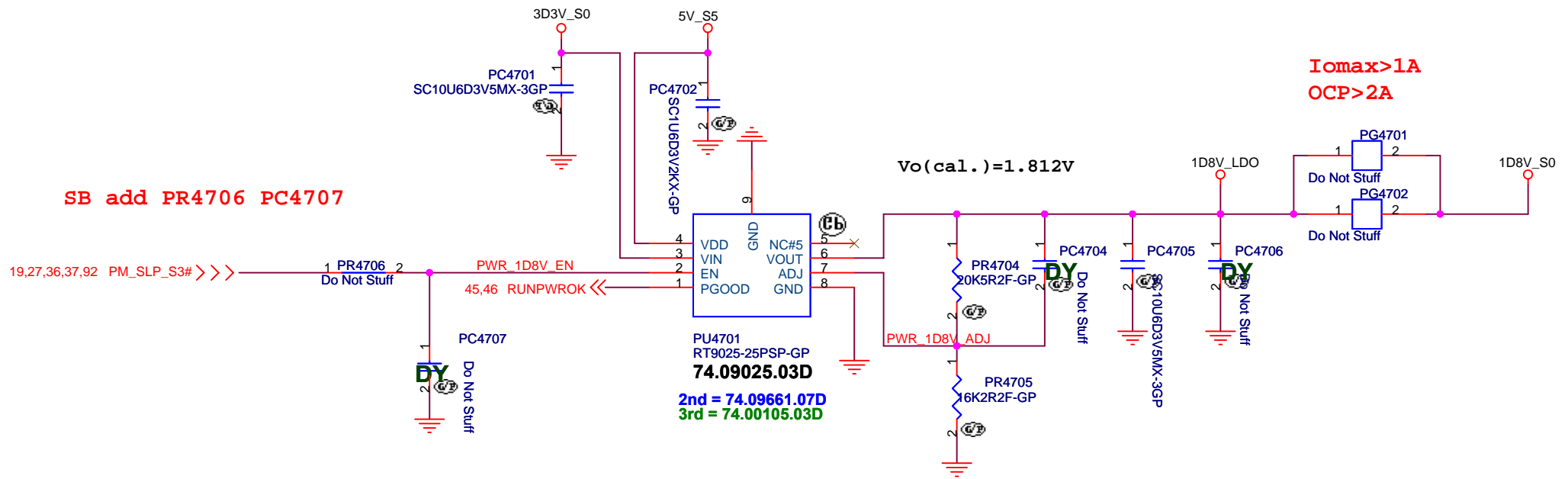
$$V_{out} = 0.75 * (1 + R1/R2)$$

SB R4608 chekc 修改31K6R  
Vout 需再1.55V 以上

37 0D75V\_EN >> 1 PR4615 2 PWR\_0D75V\_EN  
Do Not Stuff

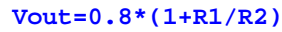
SSID = PWR.Plane.Regulator\_1p8v

## RT9025 for 1D8V\_S0



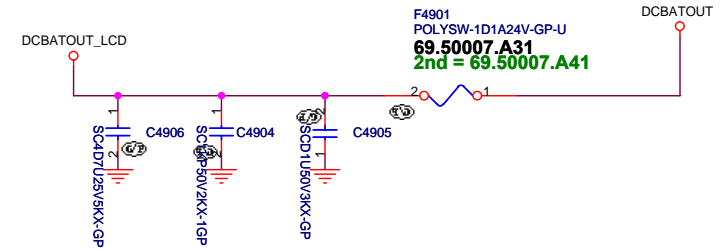
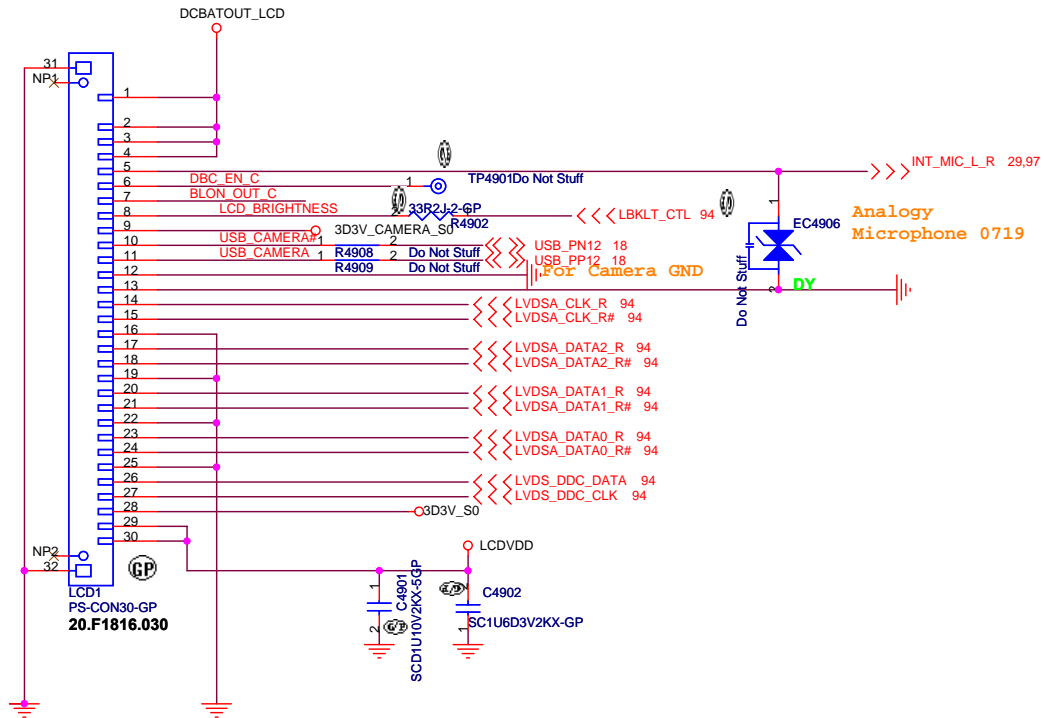
Title		
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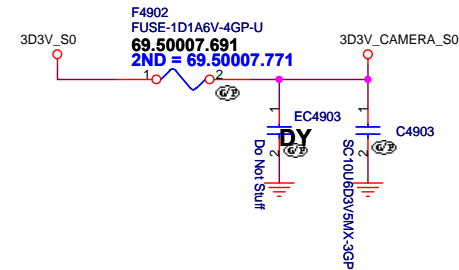


VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

## INVERTER POWER

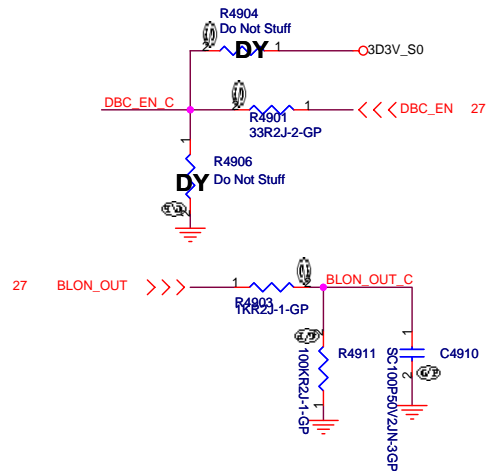
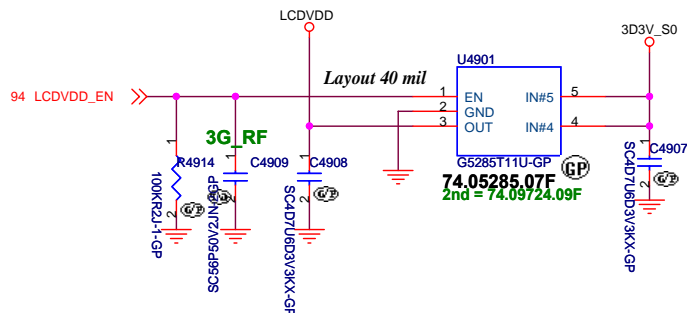


## Camera Power

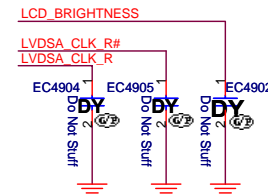


**SSID = VIDEO**

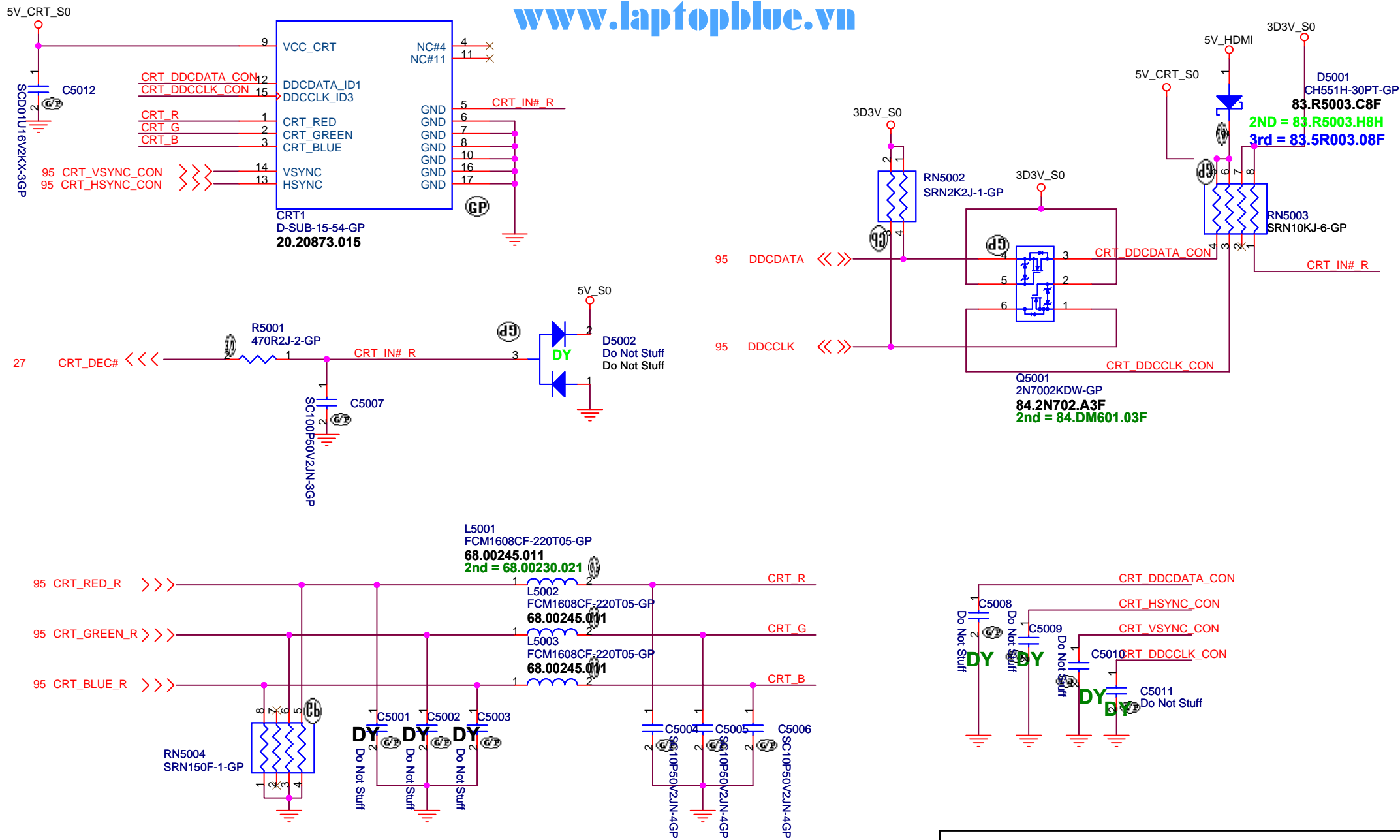
LCD POWER for ANNIE



For EMI request  
Close to LVDS connector



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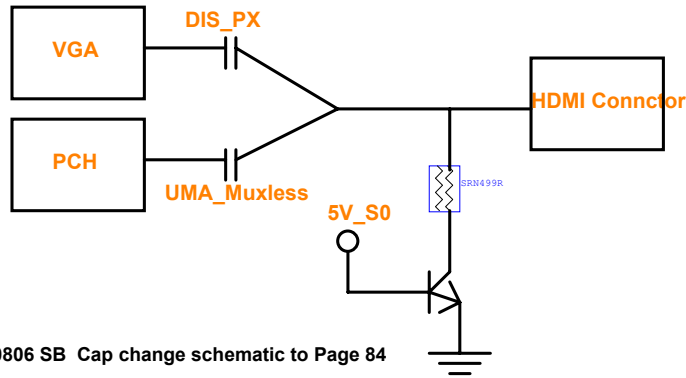
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# HDMI Level Shifter & CONNECTOR

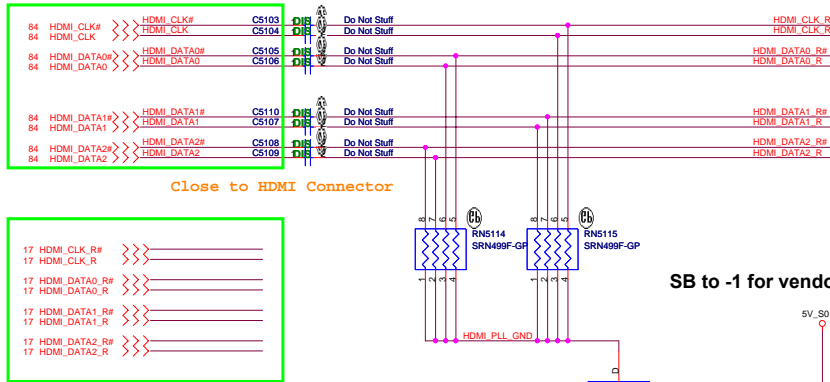
HDMI CONN  
www.laptopblue.vn

UMA\_Muxless : default setting used PS8101. if don't used PS8101  
please change C5103-C5110 to 0 ohm resister

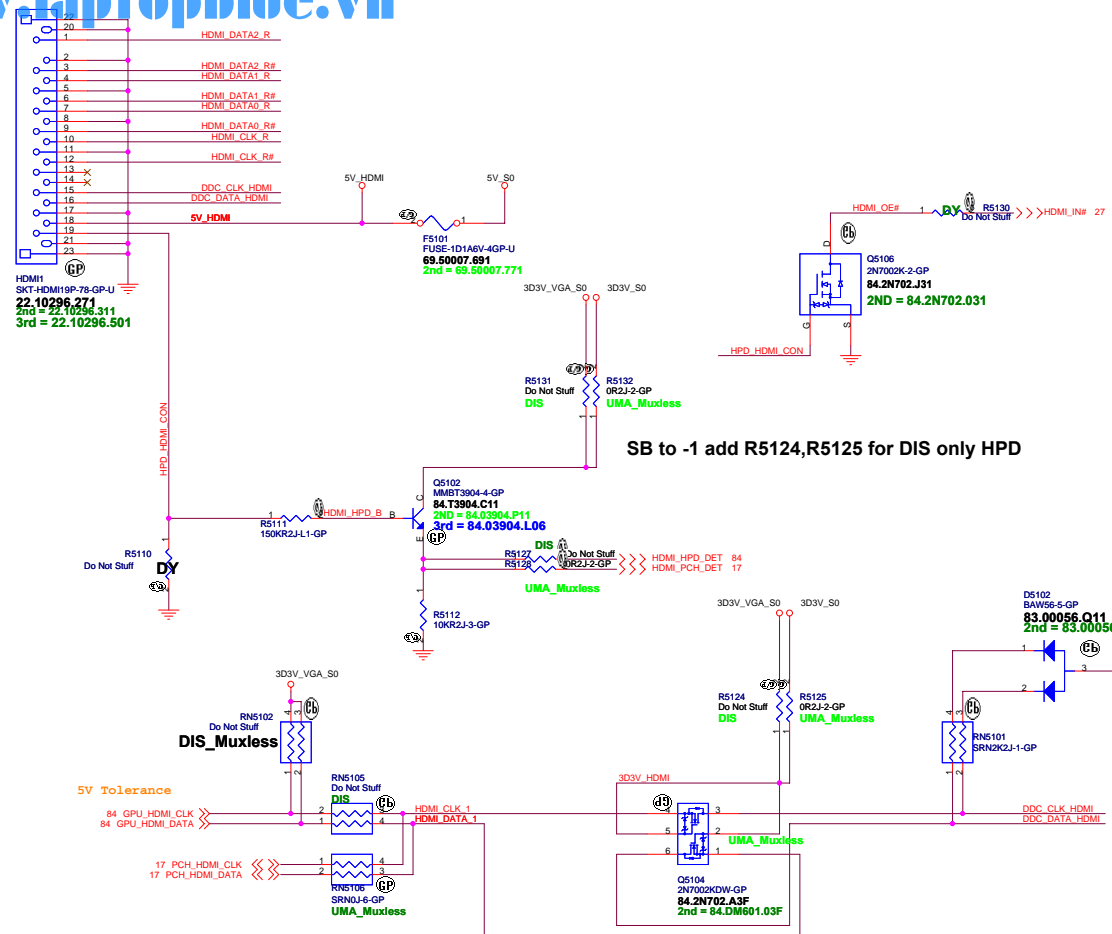
## HDMI DISCRETE/ UMA Co-lay



0806 SB Cap change schematic to Page 84

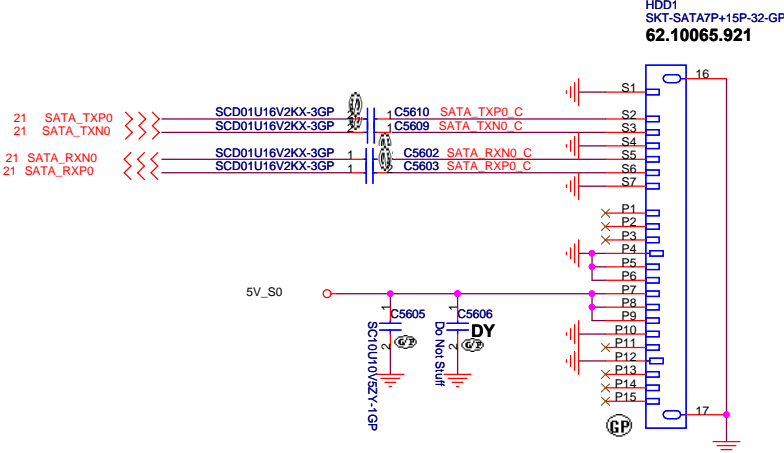


SB to -1 for vendor suggest



SB to -1 add R5124,R5125 for DIS only HPD

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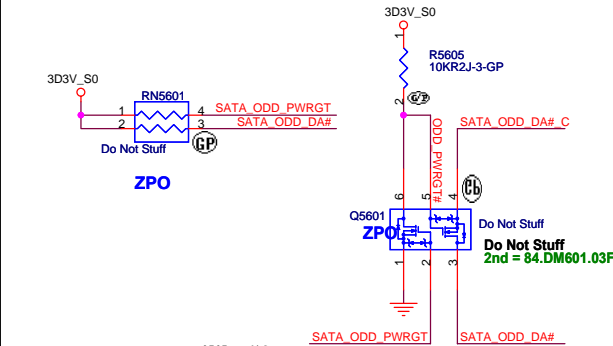
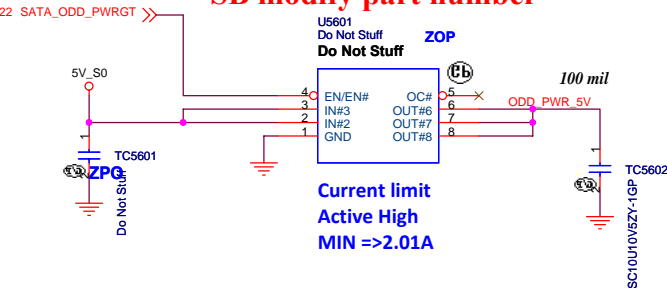
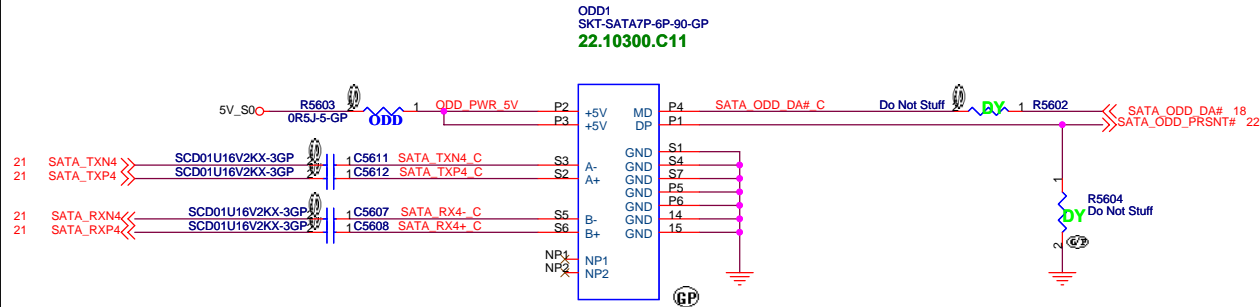


# ODD Connector

SB

SATA Zero Power ODD

SB modify part number



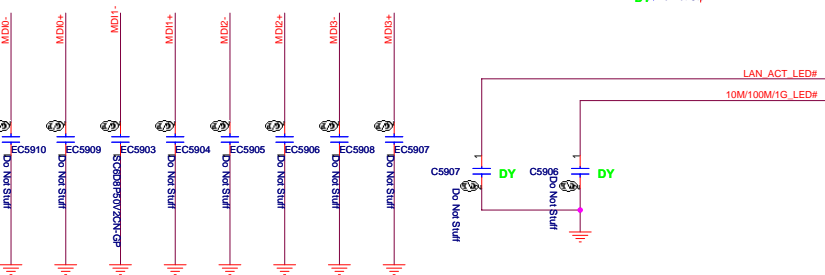
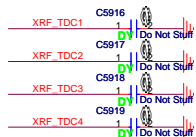
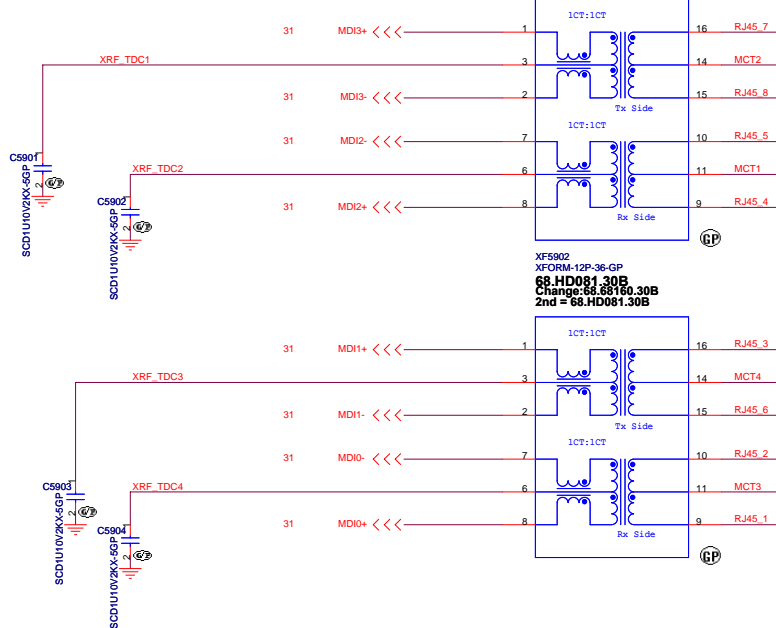
0707 Modify:  
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

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# GIGA Lan Transformer

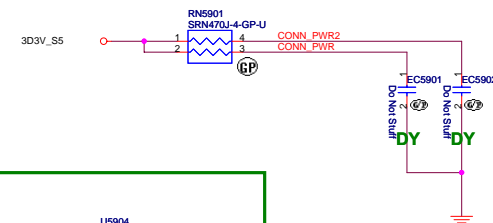
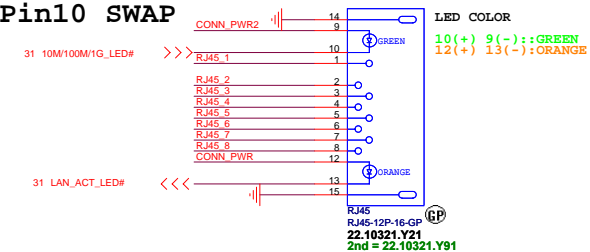
XF5901  
XFORM-12P-36-GP  
68.HD081.30B  
Change:68.68160.30B  
2nd = 68.HD081.30B

LAN MDI Off-Page

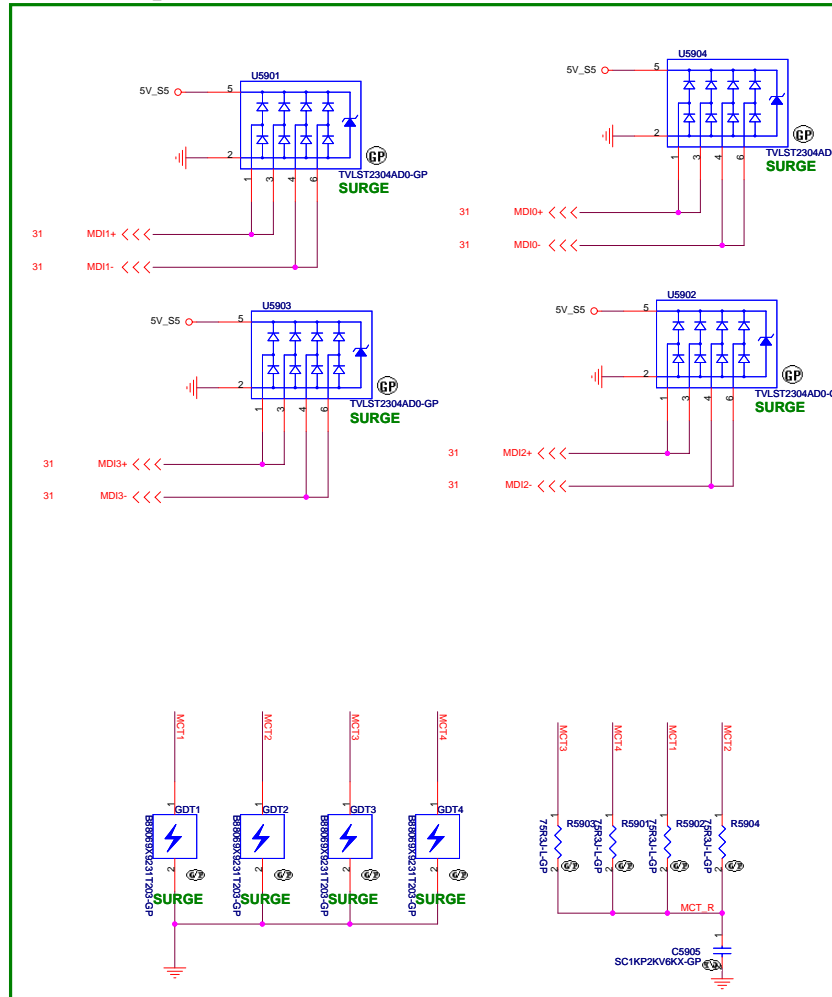


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## SB modifyf Pin9 Pin10 SWAP



## SB modify For EMI



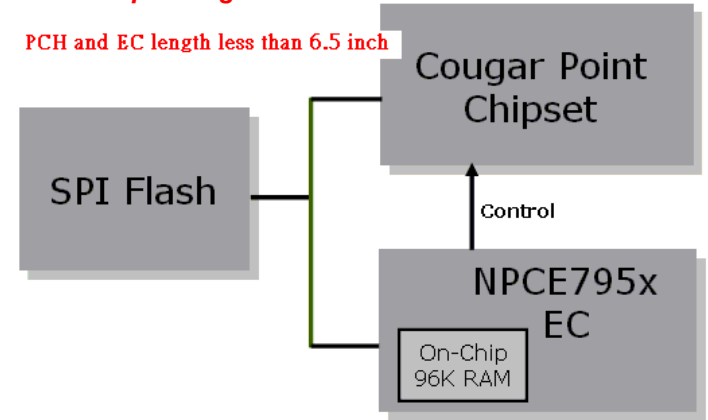
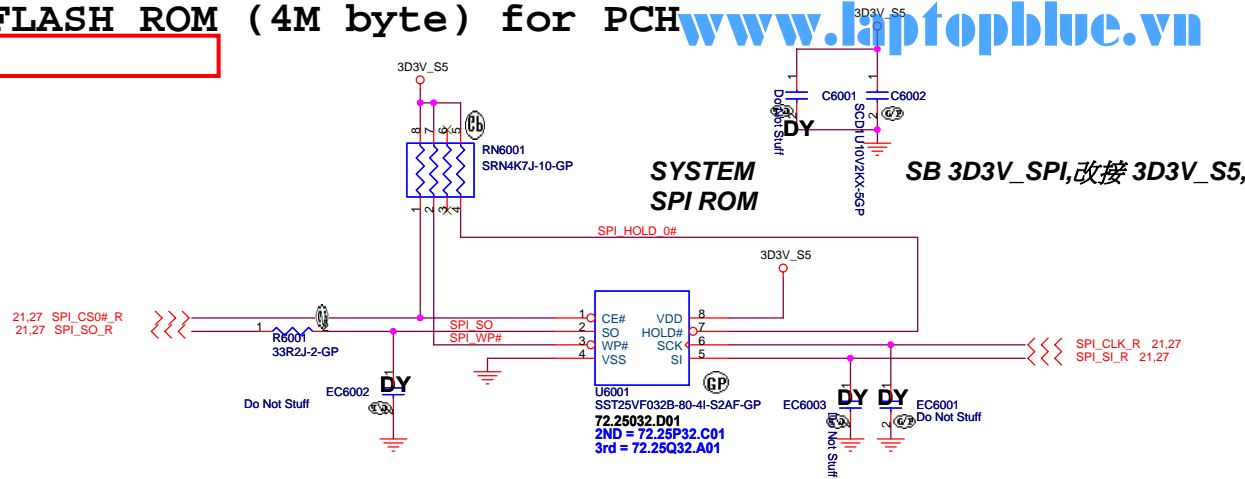
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# SPI FLASH ROM (4M byte) for PCH

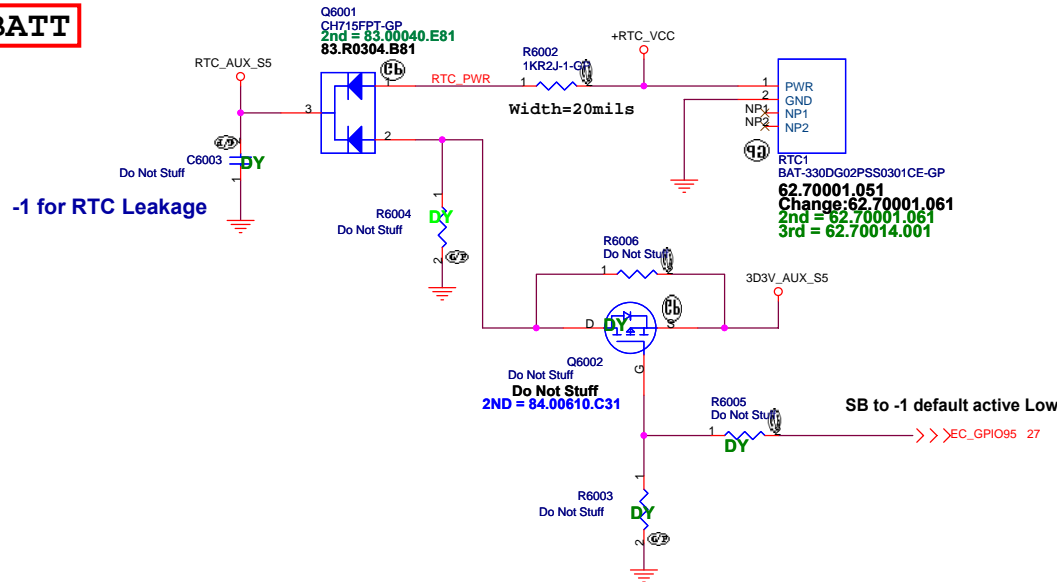
www.laptopblue.vn

SPI ROM Equal length need to less than 500mil

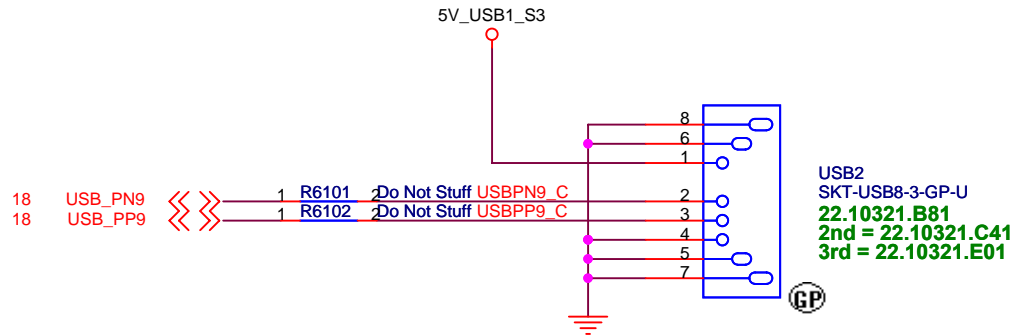
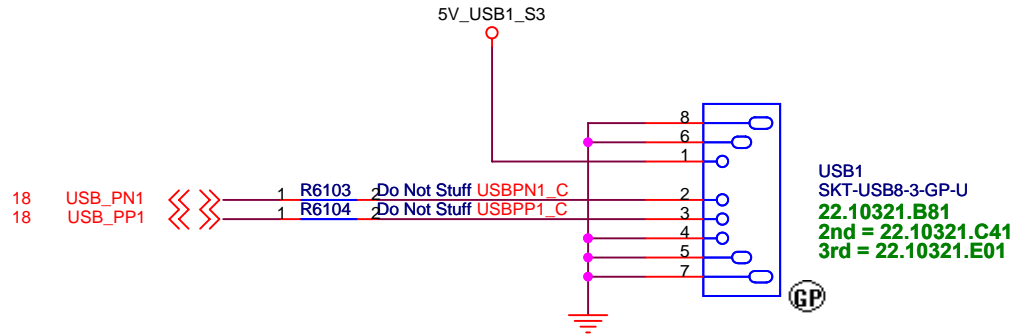
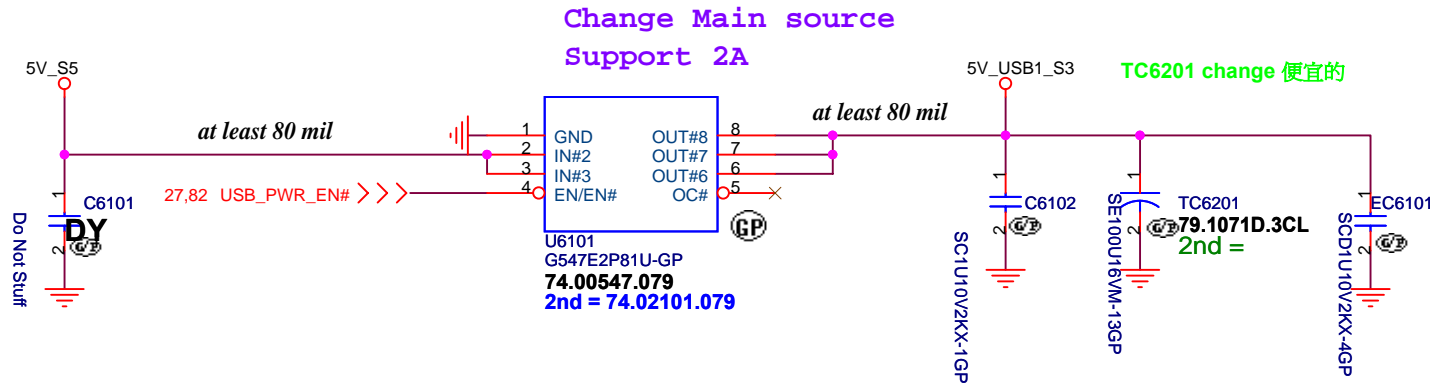
PCH and EC length less than 6.5 inch



SSID = RBATT



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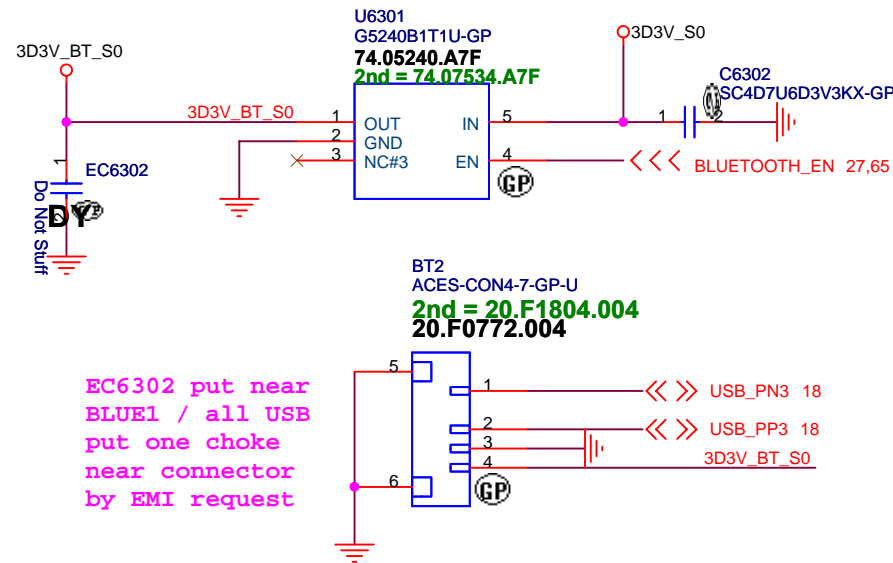


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# Bluetooth Module conn.

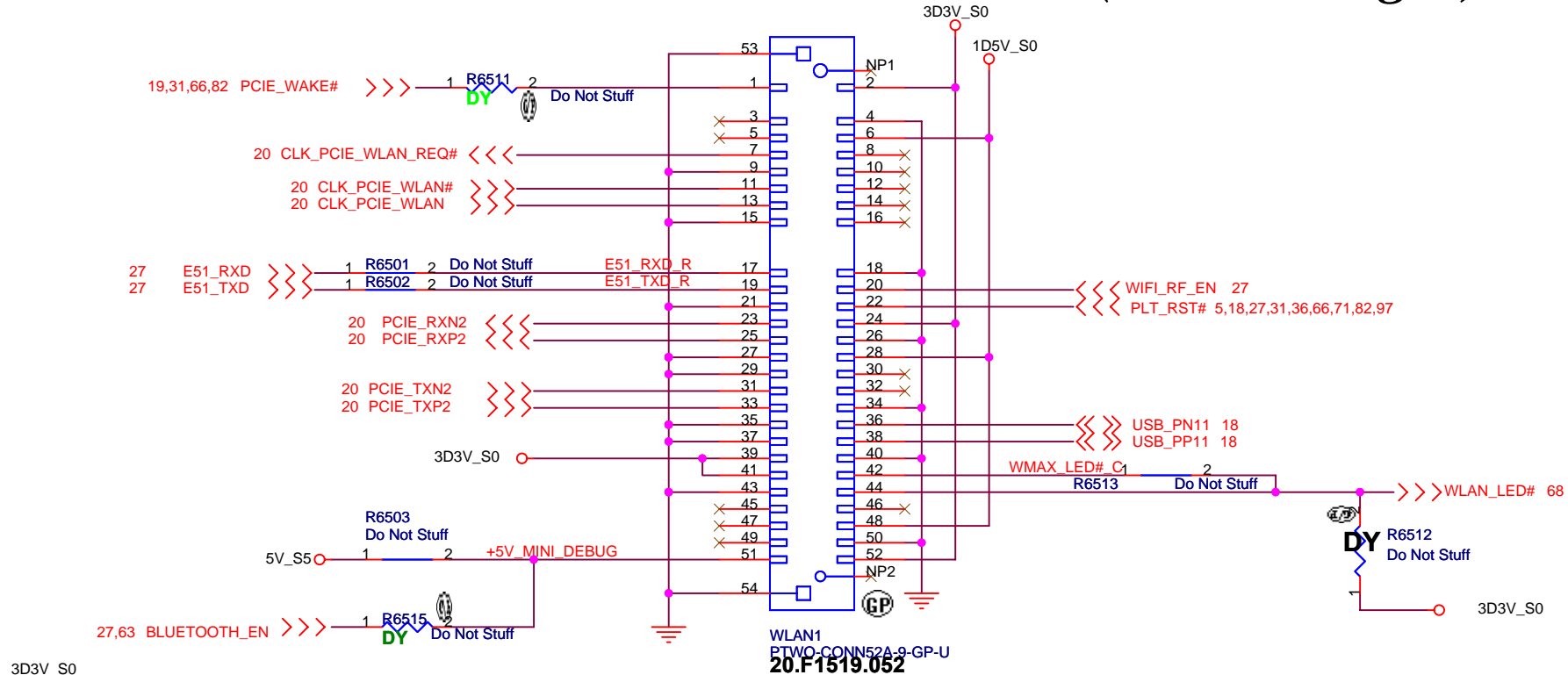
## ANNIE Bluetooth Module



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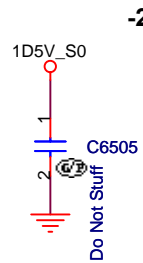
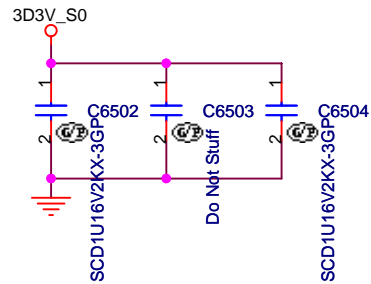
# Mini Card Connector(802.11a/b/g/n)



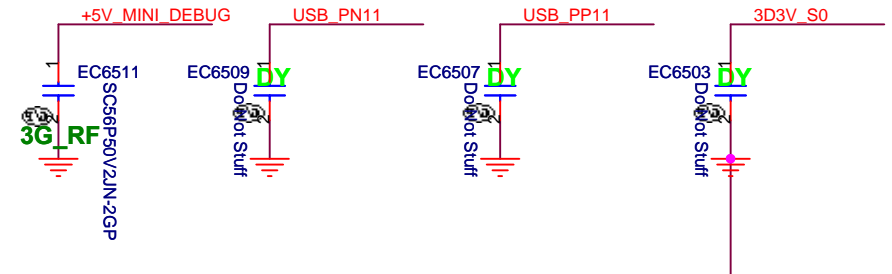
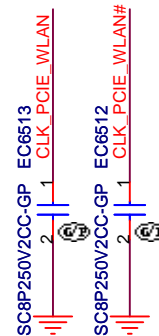
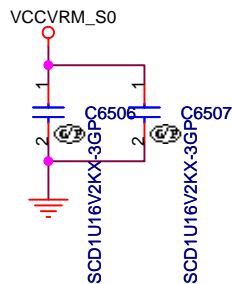
WLAN1  
PTW0-CONN52A-9-GP-U  
20.F1519.052  
2nd = 62.10043.A51  
3rd = 20.F1693.052  
4th = 20.F1743.052

SB modify for SIV

RF suggestion



-2

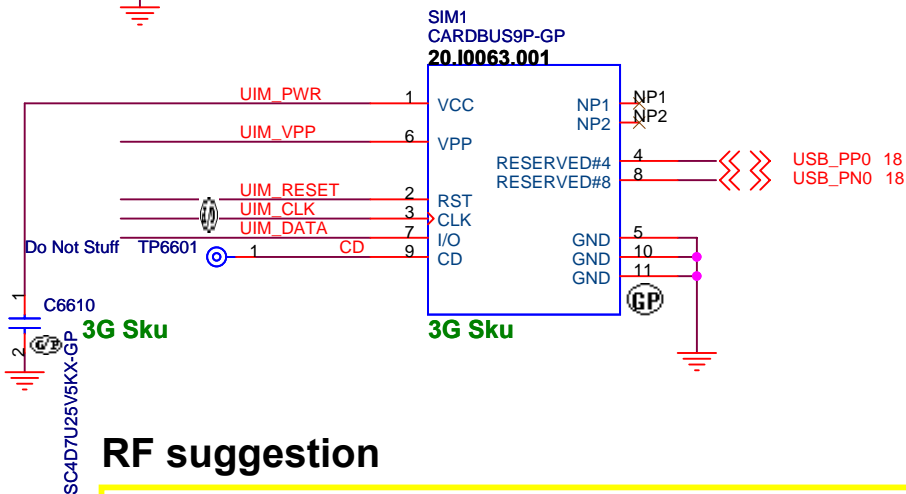
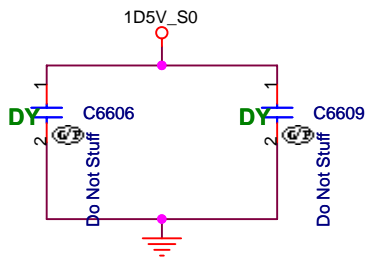
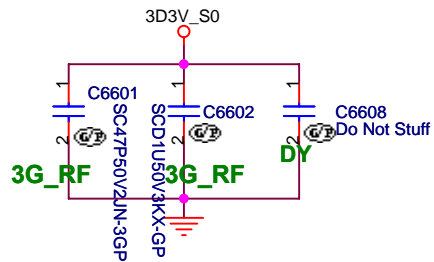


Title		
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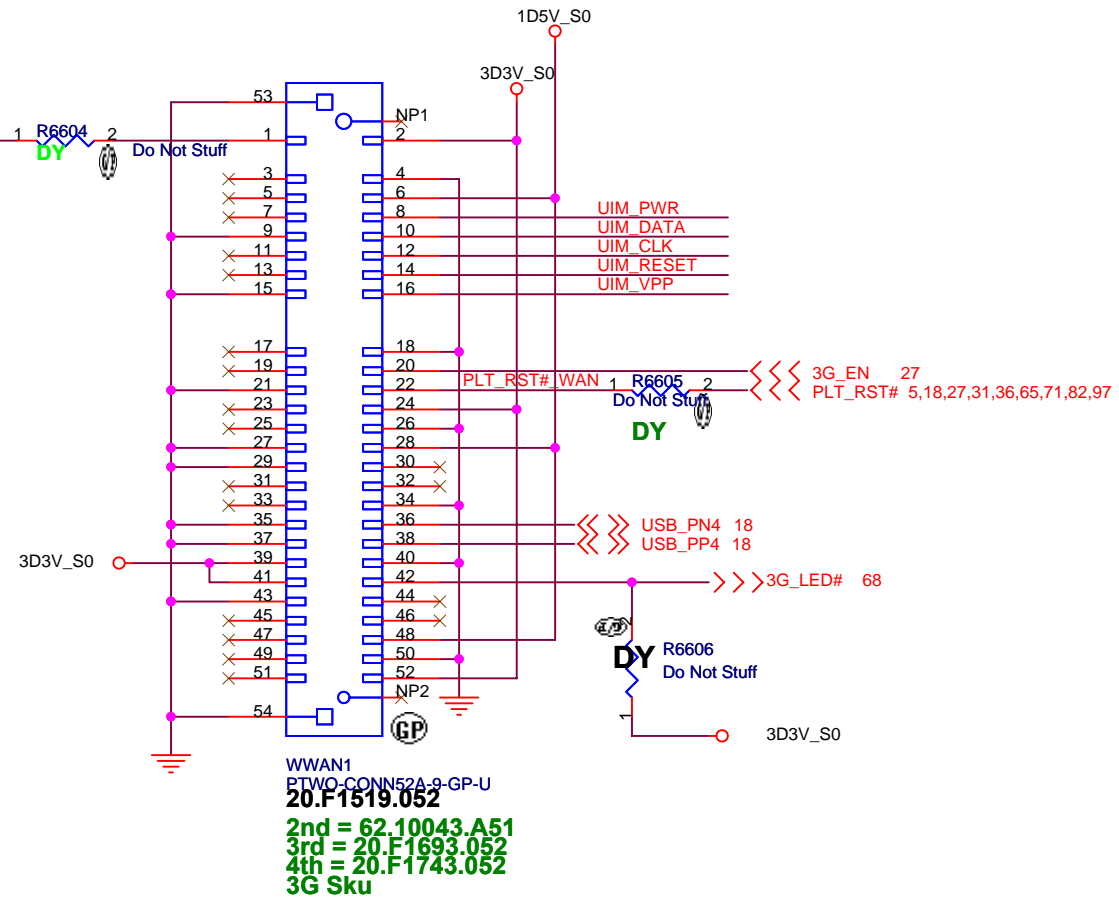
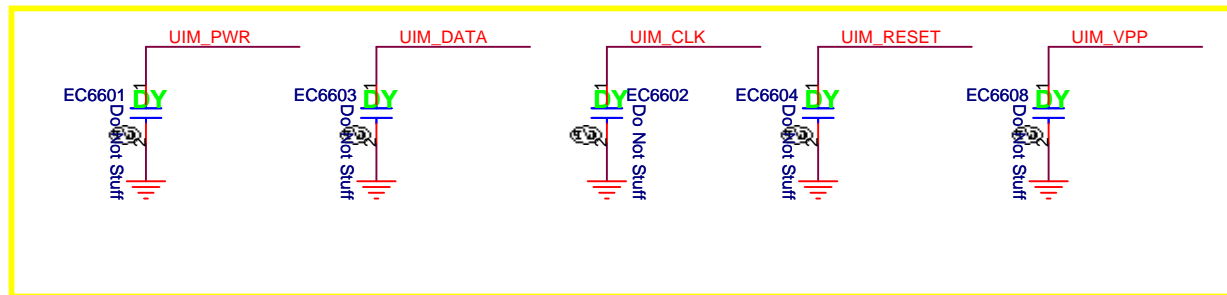
## Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN

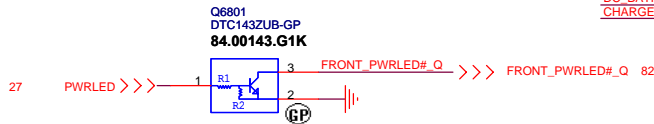


## RF suggestion

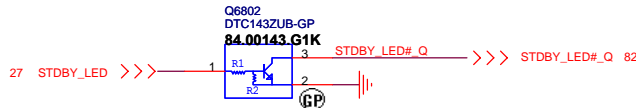


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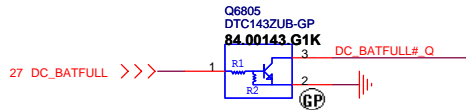
## Power button LED



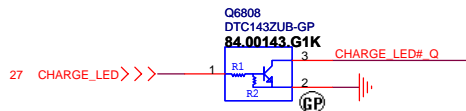
## Power STDBY\_LED



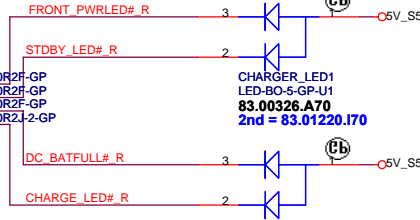
## Battery LED2(DC\_BATFULL)



## Battery LED1(CHARGE)



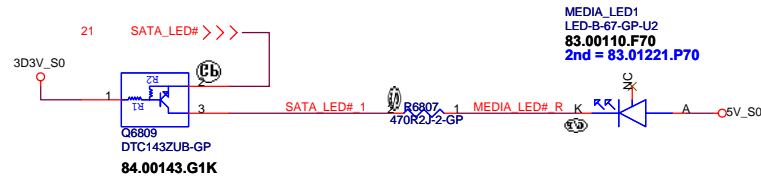
FRONT\_PWRLED#\_Q 1 R6801 300R2F-GP  
STDBY\_LED#\_Q 1 R6802 330R2F-GP  
DC\_BATFULL#\_Q 1 R6803 330R2F-GP  
CHARGE\_LED#\_Q 1 R6804 470R2J-2-GP



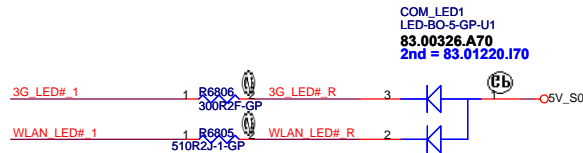
FRONT\_PWRLED#\_Q 1 DY EC6801 Not Stuff  
CHARGE\_LED#\_Q 1 DY EC6802 Do Not Stuff  
STDBY\_LED#\_Q 1 DY EC6803 Not Stuff  
DC\_BATFULL#\_Q 1 DY EC6804 Do Not Stuff

Do Not Stuff/TP6801 1 5V\_AUX\_S5

## SATA HDD LED

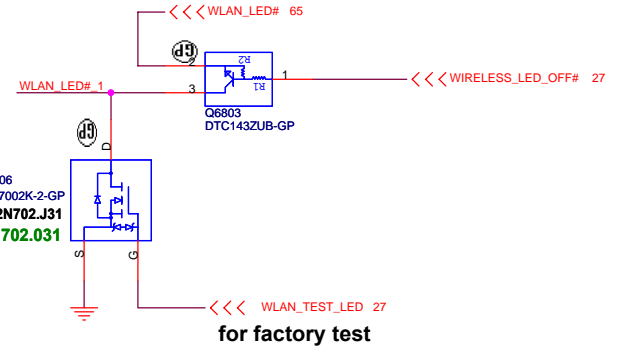


MEDIA\_LED1  
LED-B-67-GP-U2  
83.00110.F70  
2nd = 83.01221.P70



## WLAN\_LED

From module

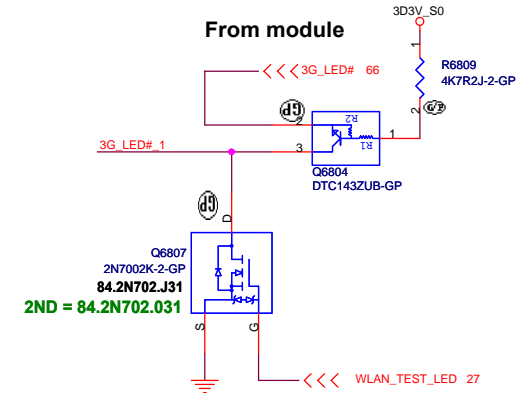


Q6806  
2N7002K-2-GP  
84.2N702.J31  
2ND = 84.2N702.031

for factory test

## 3G LED

From module

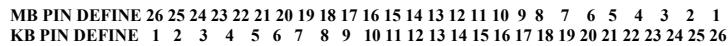


Q6807  
2N7002K-2-GP  
84.2N702.J31  
2ND = 84.2N702.031

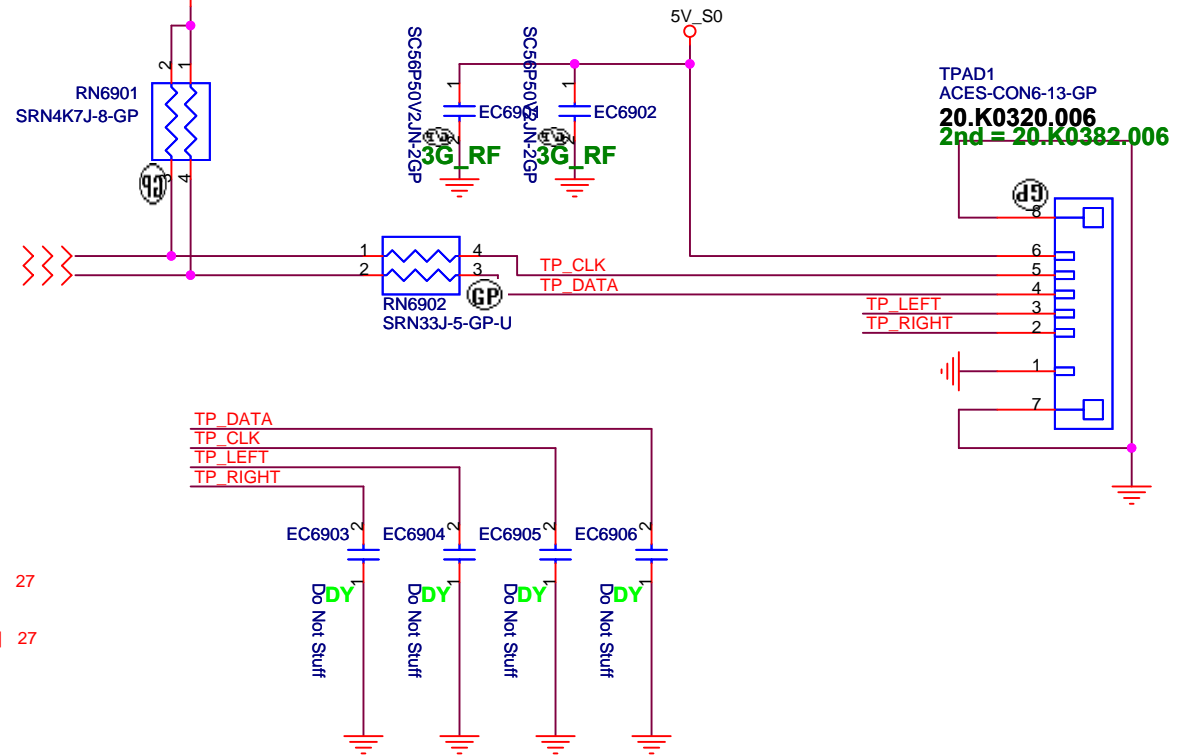
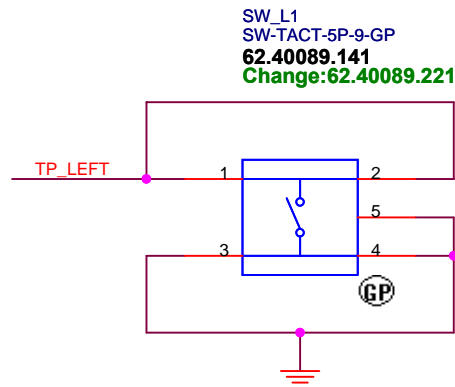
for factory test

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Size	Document Number	Rev
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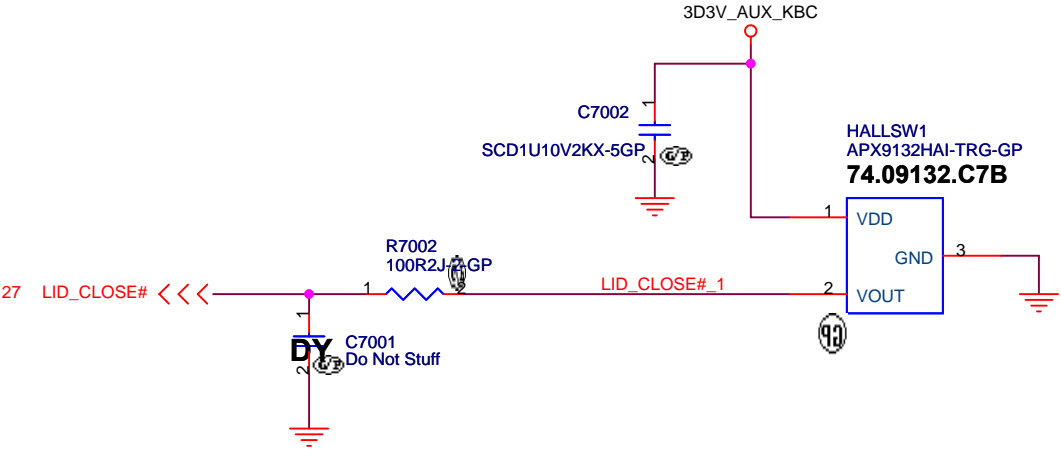
20.K0320.026 KB1  
2nd = 20.K0382.026 ACES-CON26-6GP-U


$$\mathbf{K} / \mathbf{B}$$

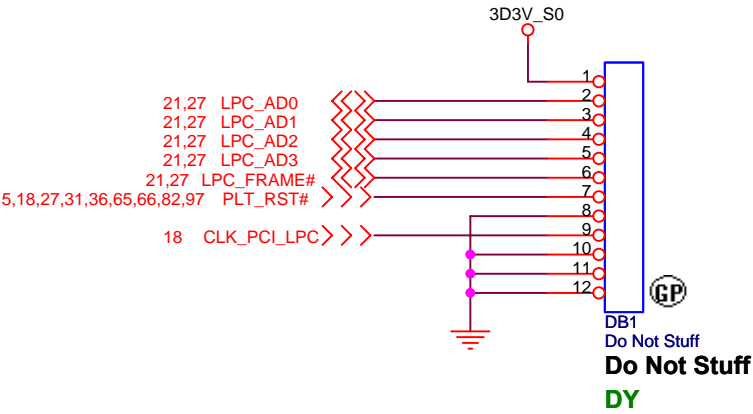
***SB to -1 modify Part number***



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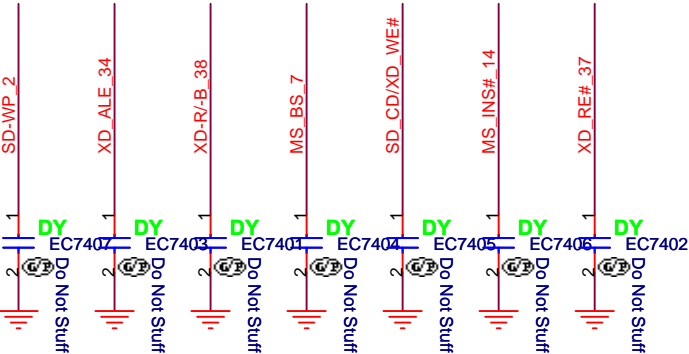
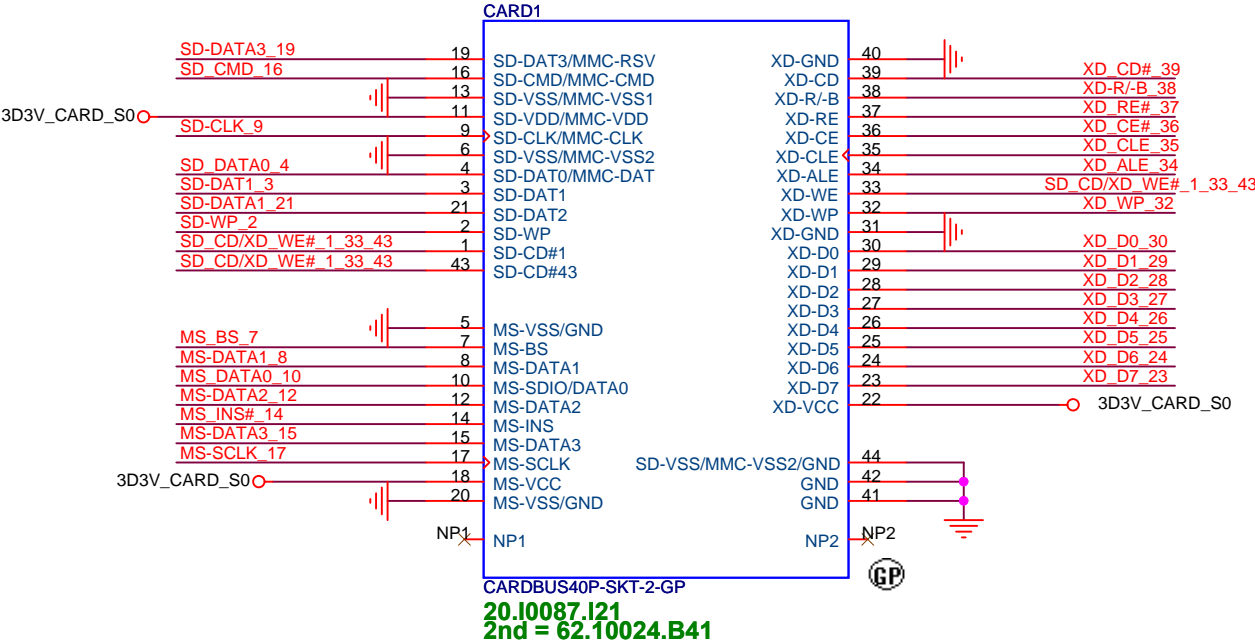
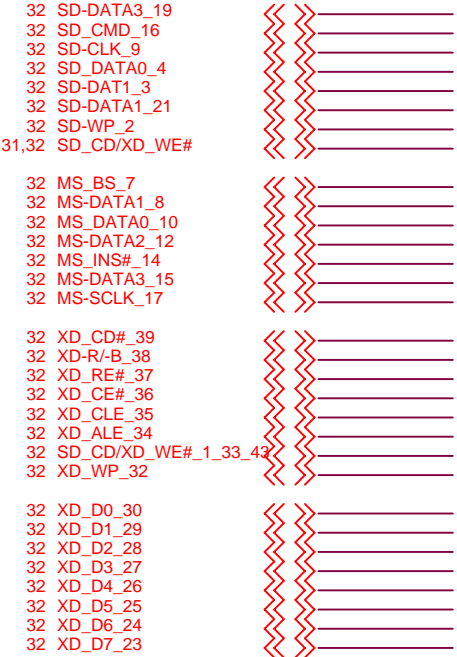


Title		
Size	Document Number	Rev
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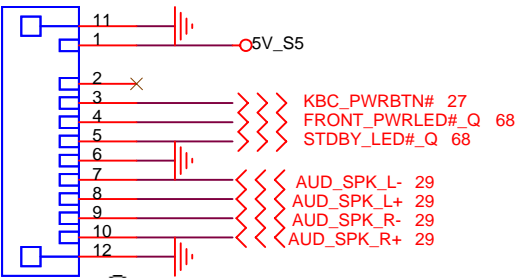
Title		
Size	Document Number	Rev
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SD/XD/MS Card Reader



Title		
Size	Document Number	Rev
Date	Sheet	





PWRCN1  
ACES-CON10-20-GP  
**20.K0422.010**  
2nd = 20.K0382.010

R8105  
Do Not Stuff

AUD\_AGND

1D5V\_S3

29 EXT\_MIC\_JD#  
29 MIC\_IN\_R  
29 MIC\_IN\_L

19,31,65,66 PCIE\_WAKE#<<<  
18 USB30\_SMI#<<<

29 COMBO\_MIC<<<  
29 AUD\_HP1\_JACK\_R2<<<  
29 AUD\_HP1\_JD#<<<  
29 AUD\_HP1\_JACK\_L2<<<

18 USB\_PN8<<<  
18 USB\_PP8<<<

27,61 USB\_PWR\_EN#>>>

5,18,27,31,36,65,66,71,97 PLT\_RST>>>

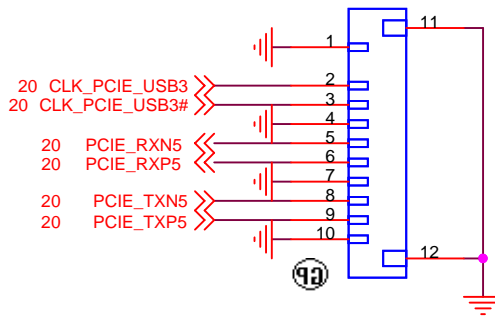
3D3V\_S5

20 USB3\_PEGB\_CLKREQ#<<<

5V\_S5

USBCN1  
ACES-CON26-11-GP  
**20.K0315.026**  
2nd = 20.K0370.026

USBCN2  
ACES-CON10-18-GP  
**20.K0315.010**  
2nd = 20.K0392.010

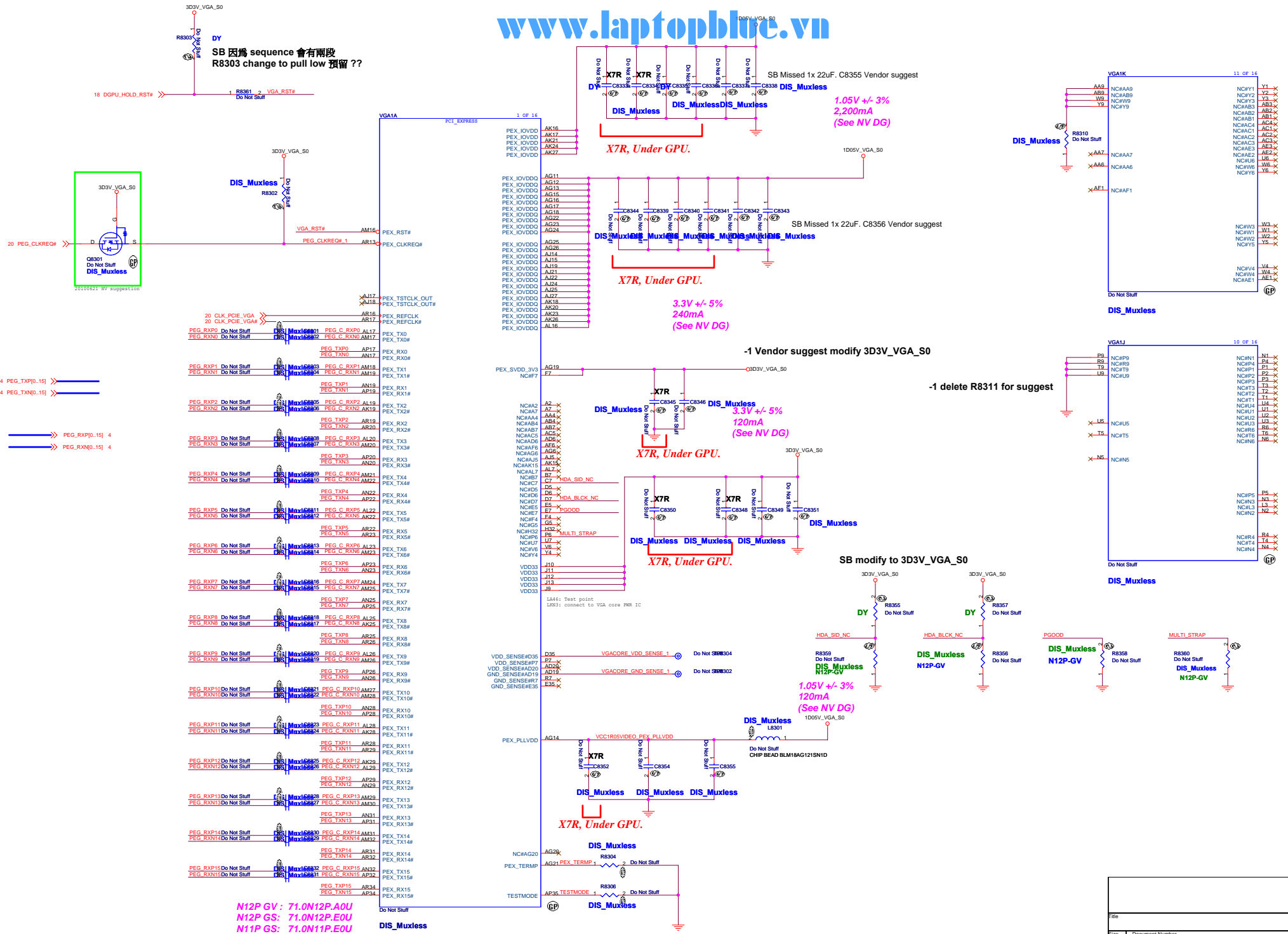


RF\_CN1  
ACES-CON2-11-GP  
**20.F0772.002**

BAE40

27 Wireless\_SW<<<

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## LVDS Interface

www.laptopblue.vn

1.05V +/- 3%  
220mA  
(See NV DG)

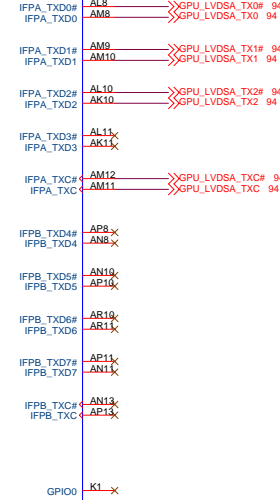
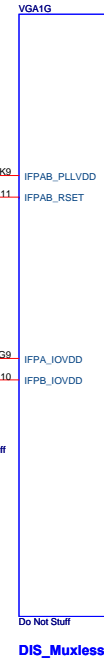
DG requires X7R for  
1uF and 4.7uF as well.

3.3V +/- 5%  
220mA  
(See NV DG)

Missed 1x 0.1uF  
180ohm@100MHz ESR=0.15

DG requires X7R for  
1uF and 4.7uF as well.

X7R, Under GPU.



SB modify connector to IFPCDE\_PLLVDD\_PWR

Under GPU.

SB modify connector to IFPC\_IOVDD\_PWR

SA R8412, R8413 change DY  
SB R8412, R8413 change delete

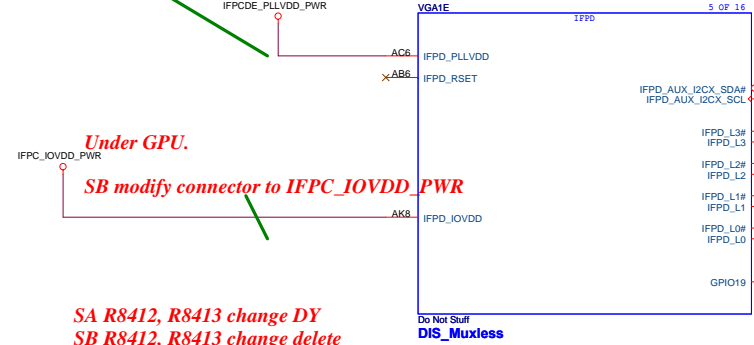
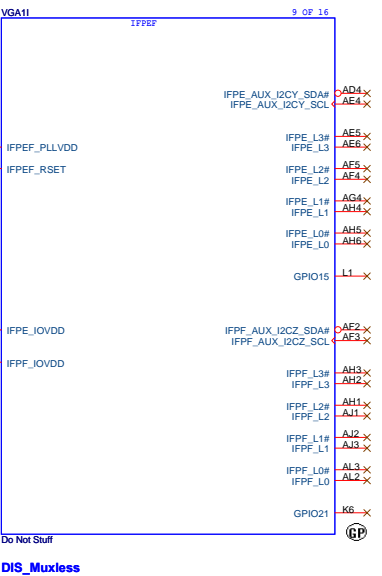
## HDMI Interface

1.05V +/- 3%  
285mA  
(See NV DG)  
220ohm@100MHz ESR=0.05

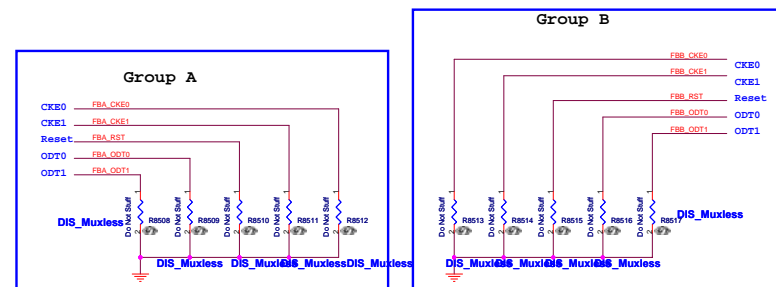
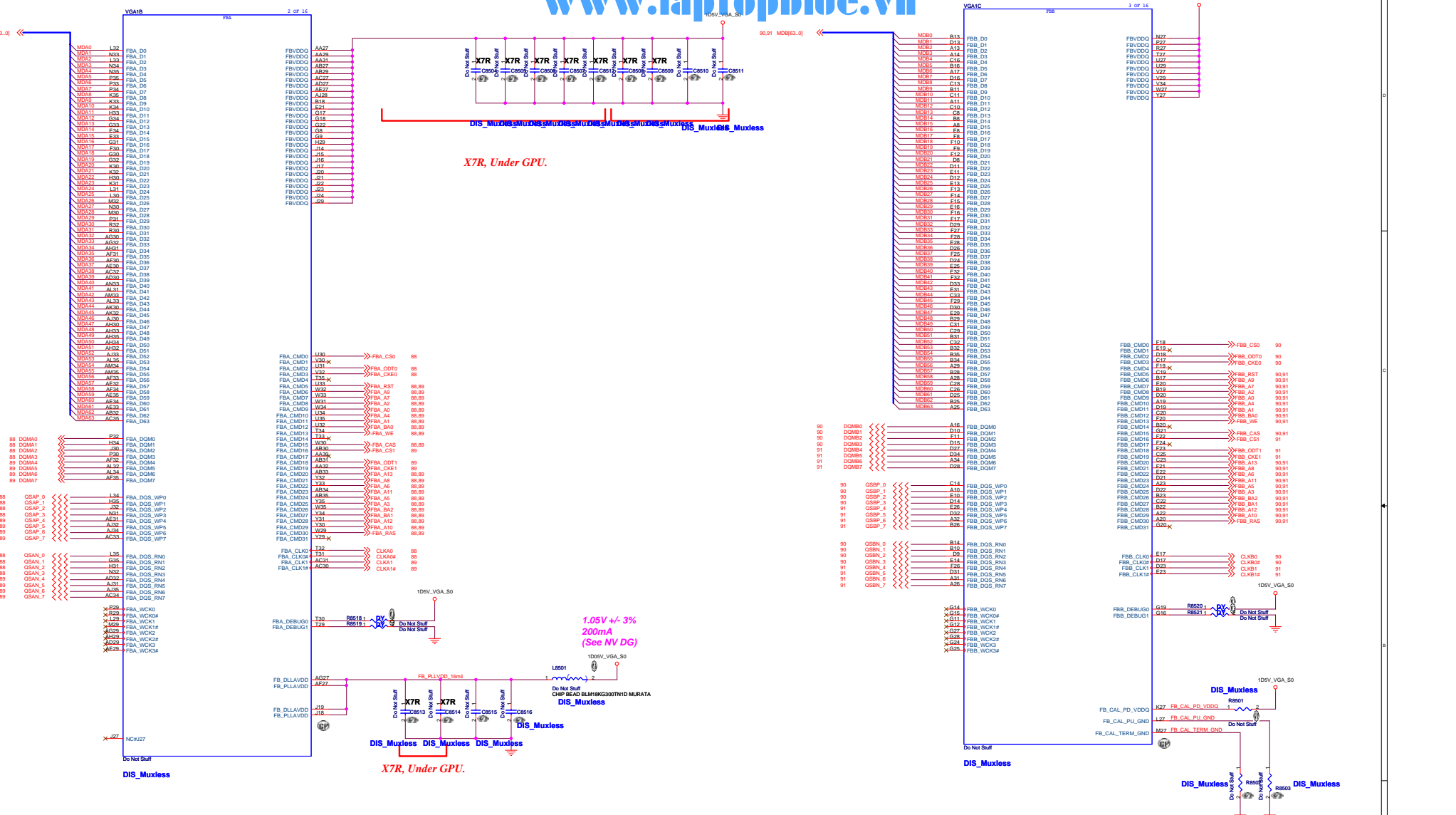
3.3V +/- 5%  
440mA (220mA each, max 2 links)  
(See NV DG) 300ohm@100MHz ESR=0.25

DG requires X7R for  
1uF and 4.7uF as well.

X7R, Under GPU.



Title	
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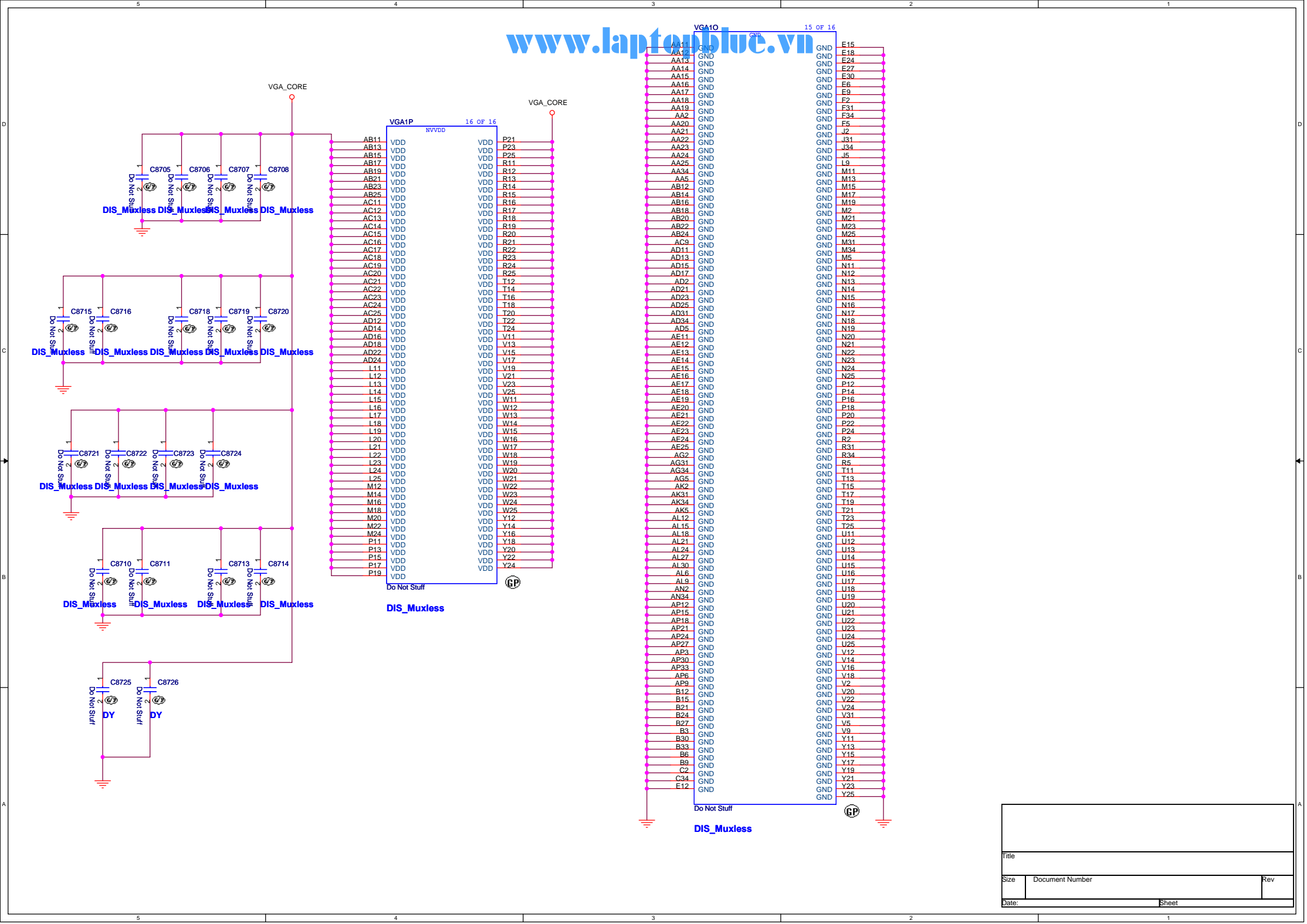


*FBCLK Termination place on VRAM side*

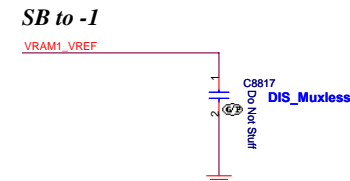
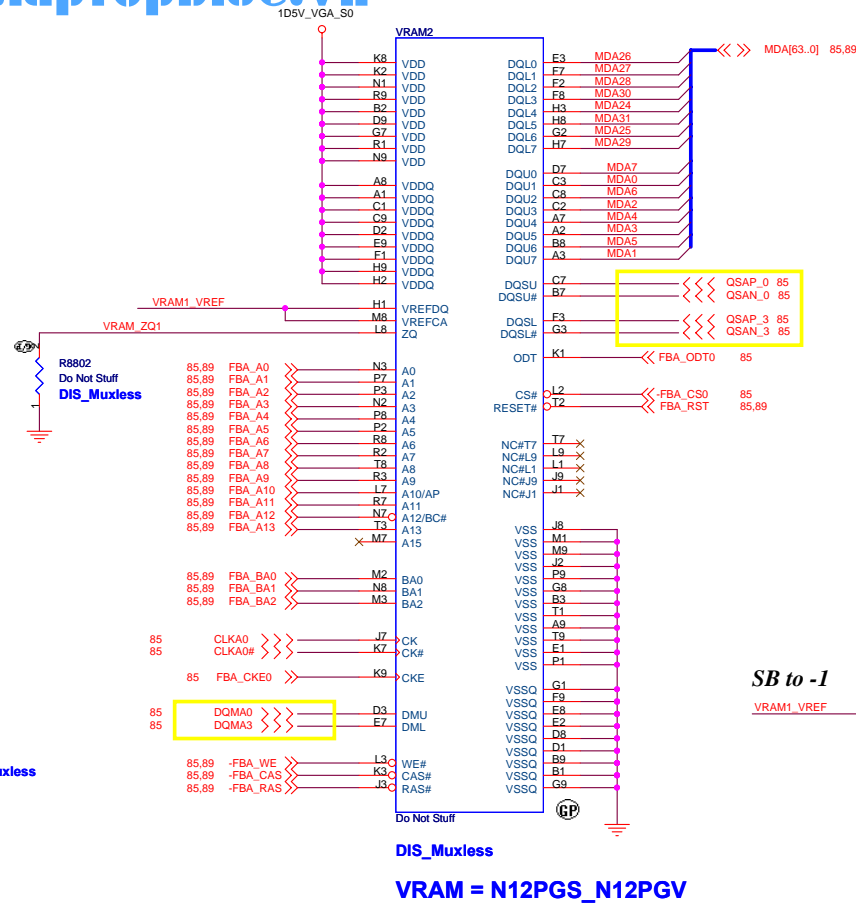
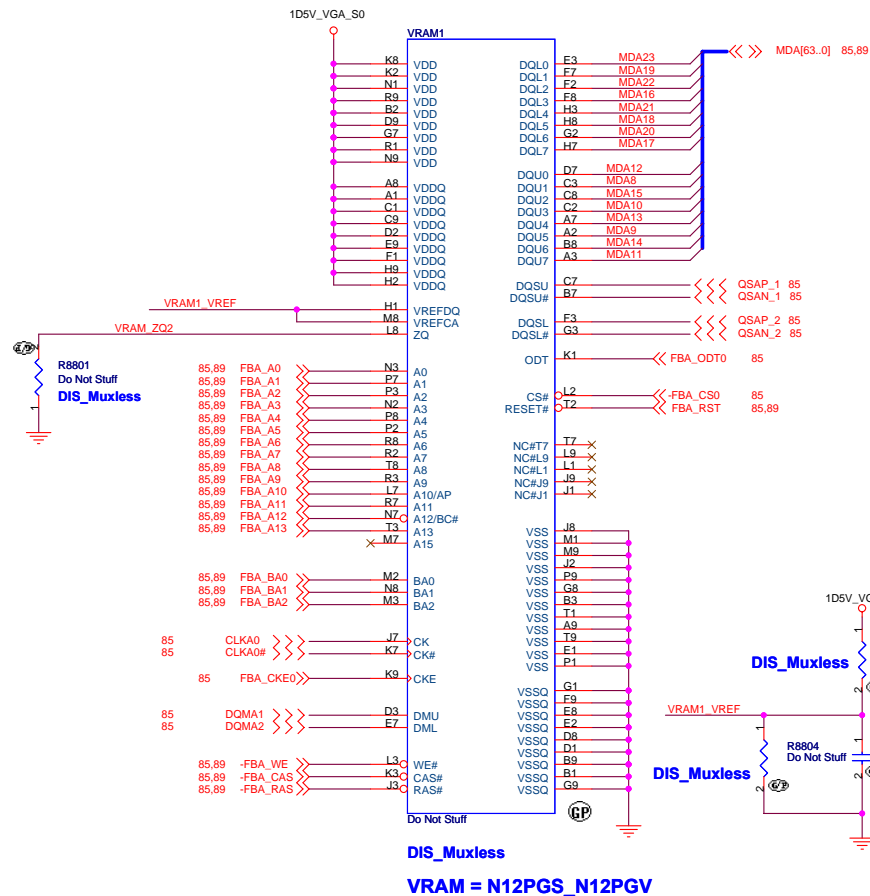
*FBCLK Termination place on VRAM side*

File	
Size	Document Number
Date	Sheet

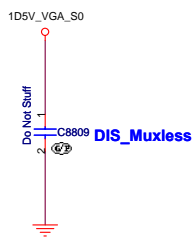
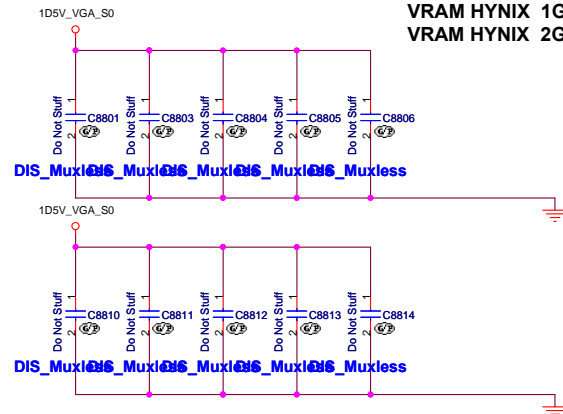




Title	
Size	Document Number
Date:	Sheet

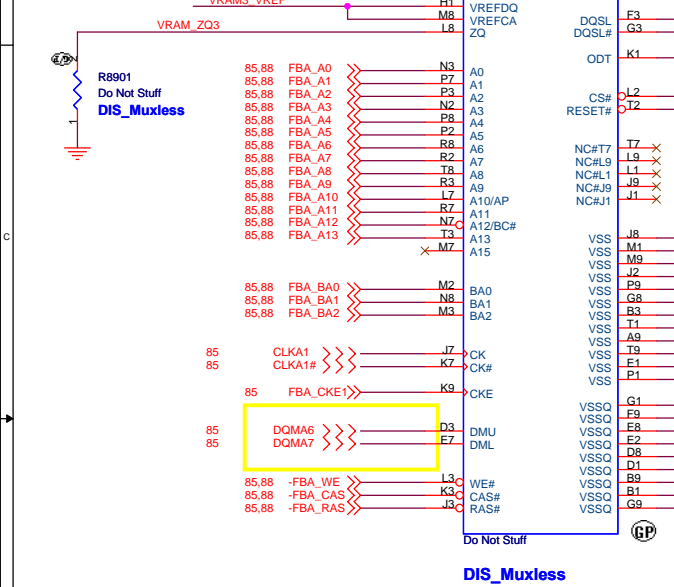


VRAM SAMSUNG 1Gb VR.1GB0B.006  
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005  
VRAM HYNIX 2Gb VR.2GB0G.001

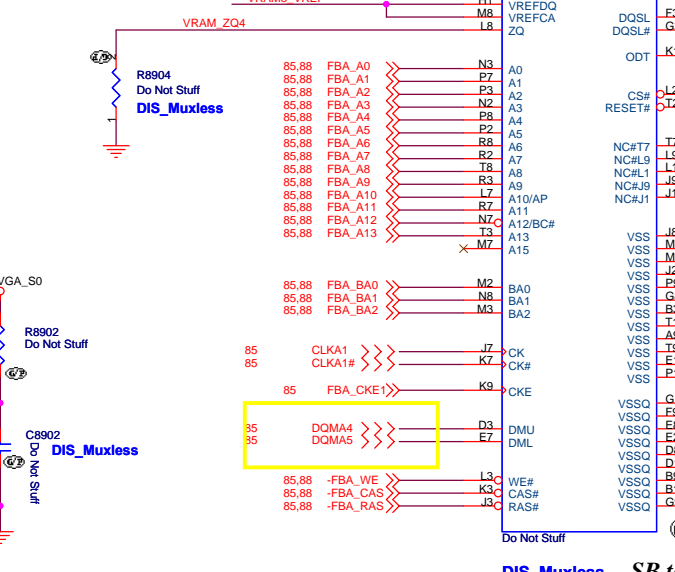


Title		
Size	Document Number	Rev
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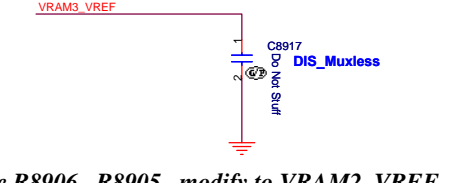
SB to -1 modify to VRAM3\_VREF



SB to -1 modify to VRAM3\_VREF

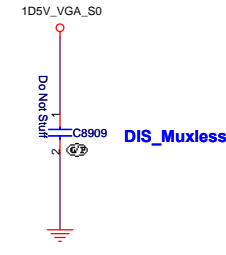
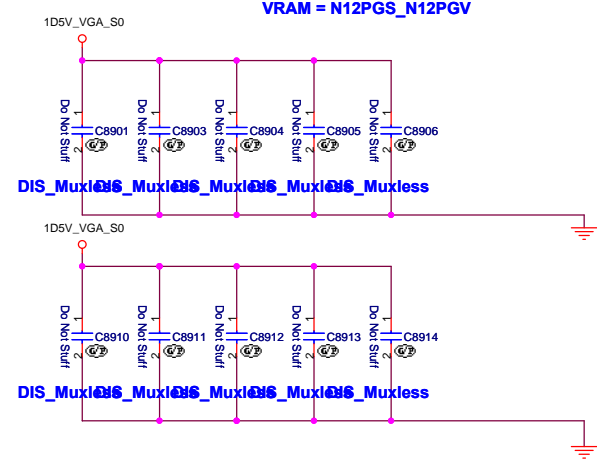


SB to -1 modify to VRAM3\_VREF



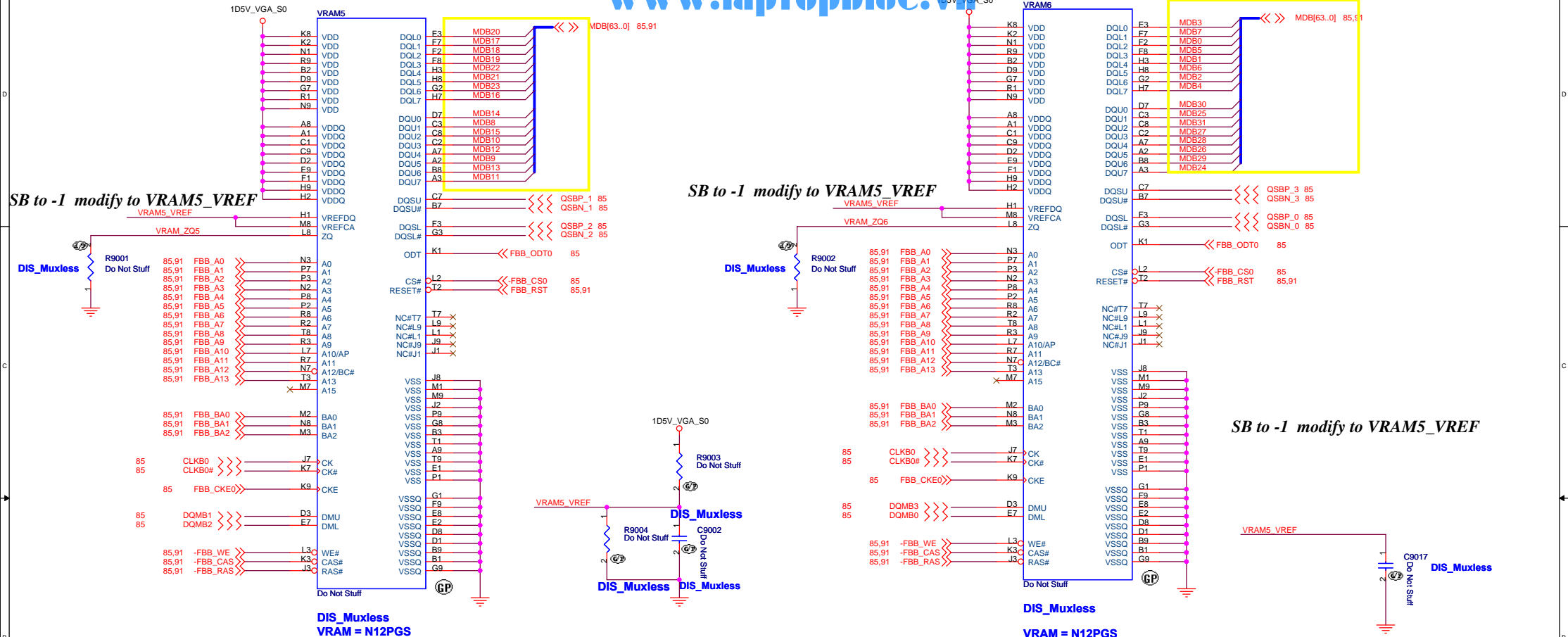
DIS\_Muxless SB to -1 delete R8906, R8905, modify to VRAM2\_VREF  
VRAM = N12PGS\_N12PGV

VRAM SAMSUNG 1Gb VR.1GB0B.006  
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005  
VRAM HYNIX 2Gb VR.2GB0G.001

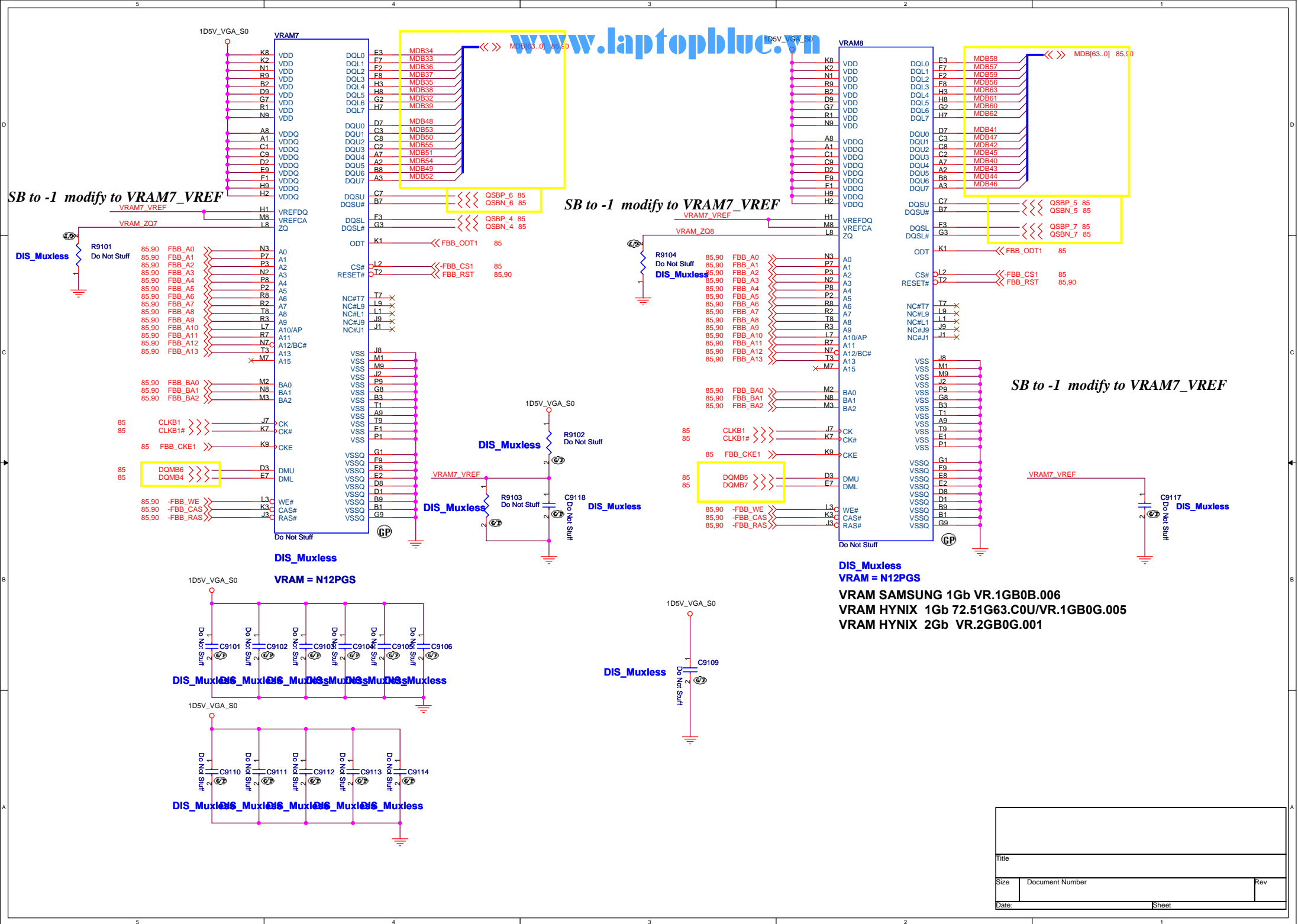


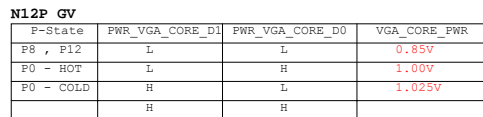
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$$V_{out} = 0.75V * (R1 + R2) / R2$$

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### 1.05V to 1.05V\_VGA\_S0 Transfer



**U9305**  
Do Not Stuff  
**Do Not Stuff**

**DY**

5V\_S5

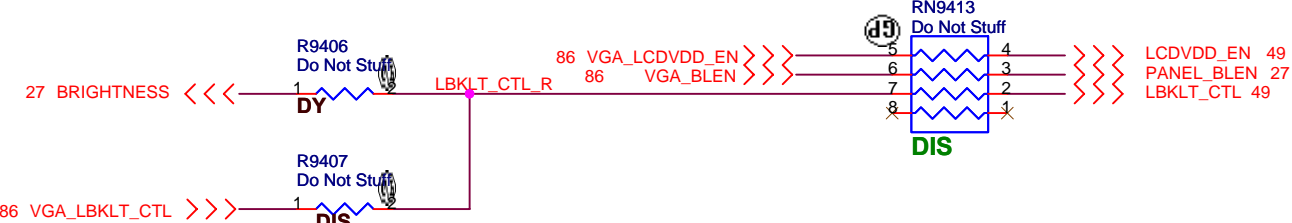
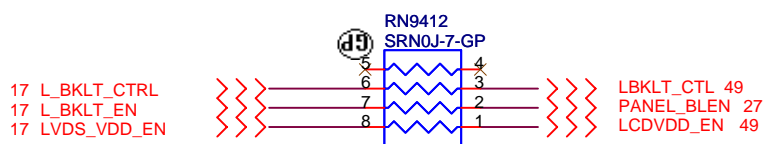
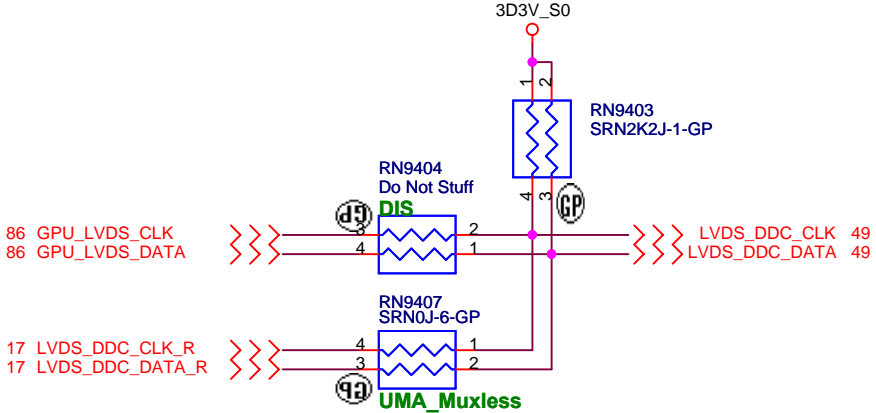
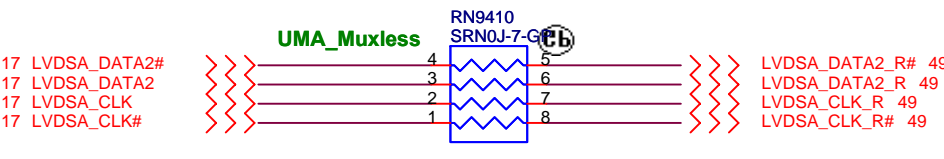
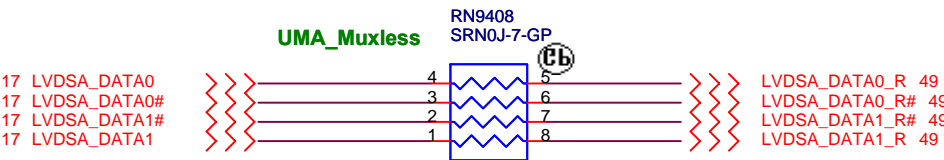
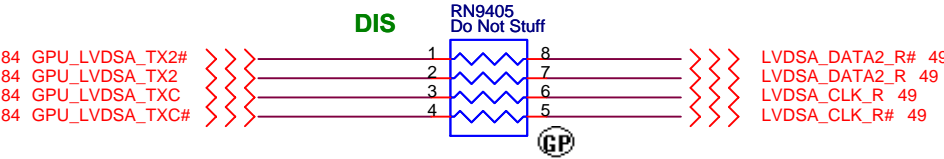
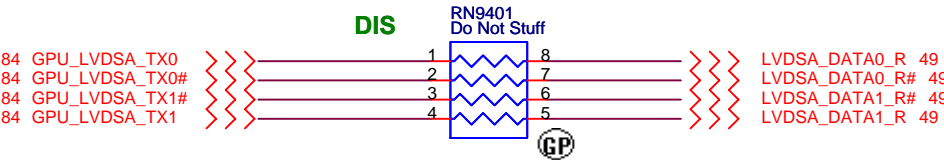
**DY** **R9323**  
Do Not Stuff

22.92 DGPU\_PWROK >>> 6  
1D5V\_VGA\_S0 >>> 5  
5V\_S5 >>> 4

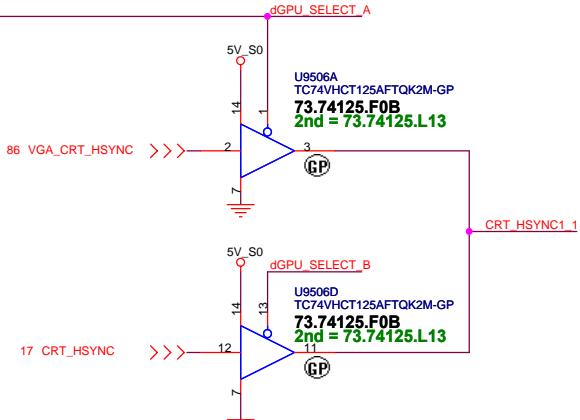
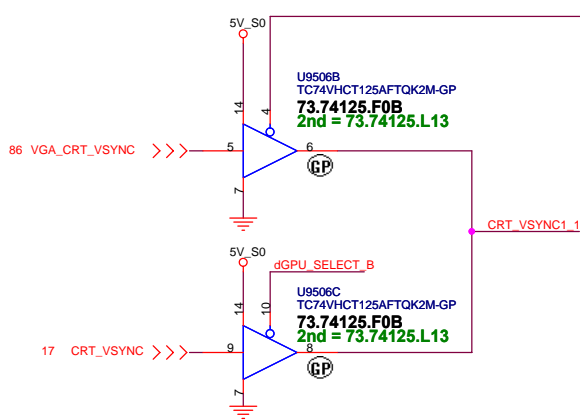
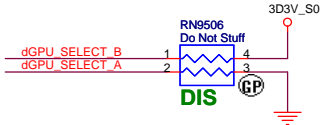
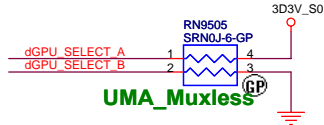
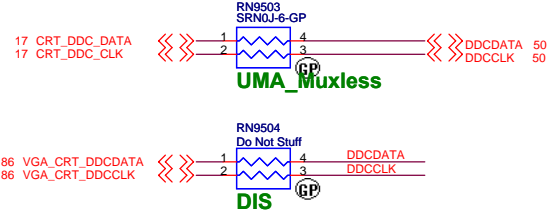
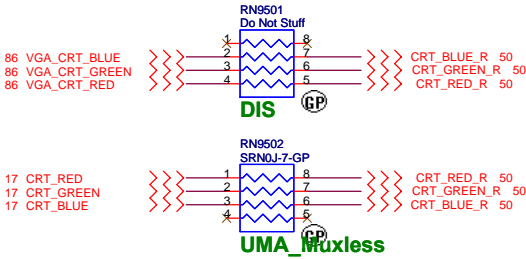
1 EN VCC 2  
DC2 GND 3  
DC1 HV 4

10k

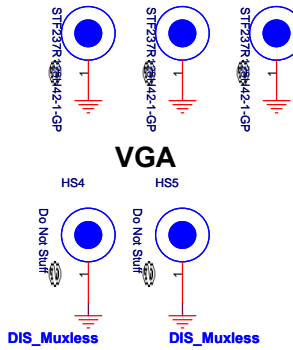
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Size	Document Number	Rev
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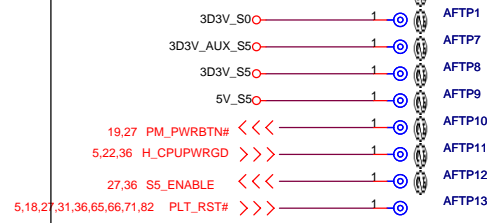
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Size	Document Number	Rev
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Title		
Size	Document Number	Rev
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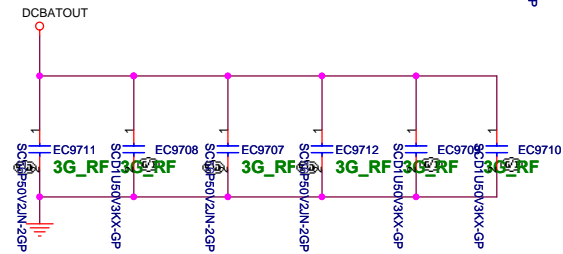
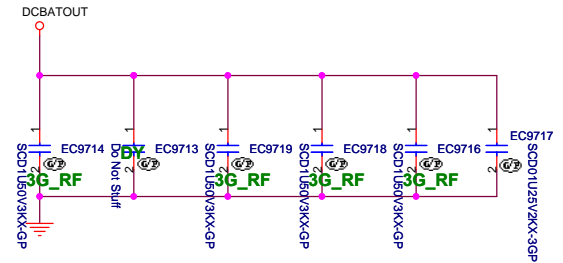
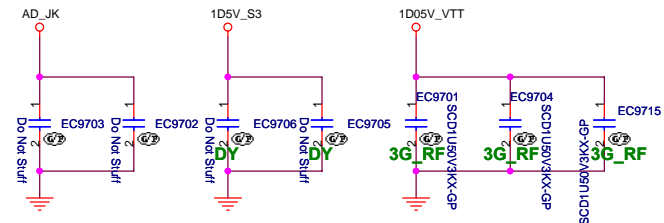
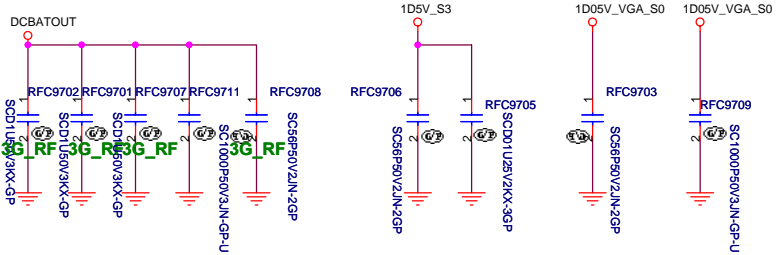
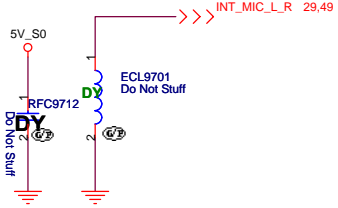
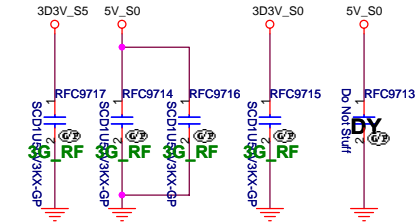
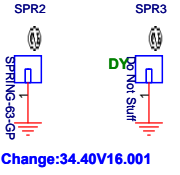
# Check test point



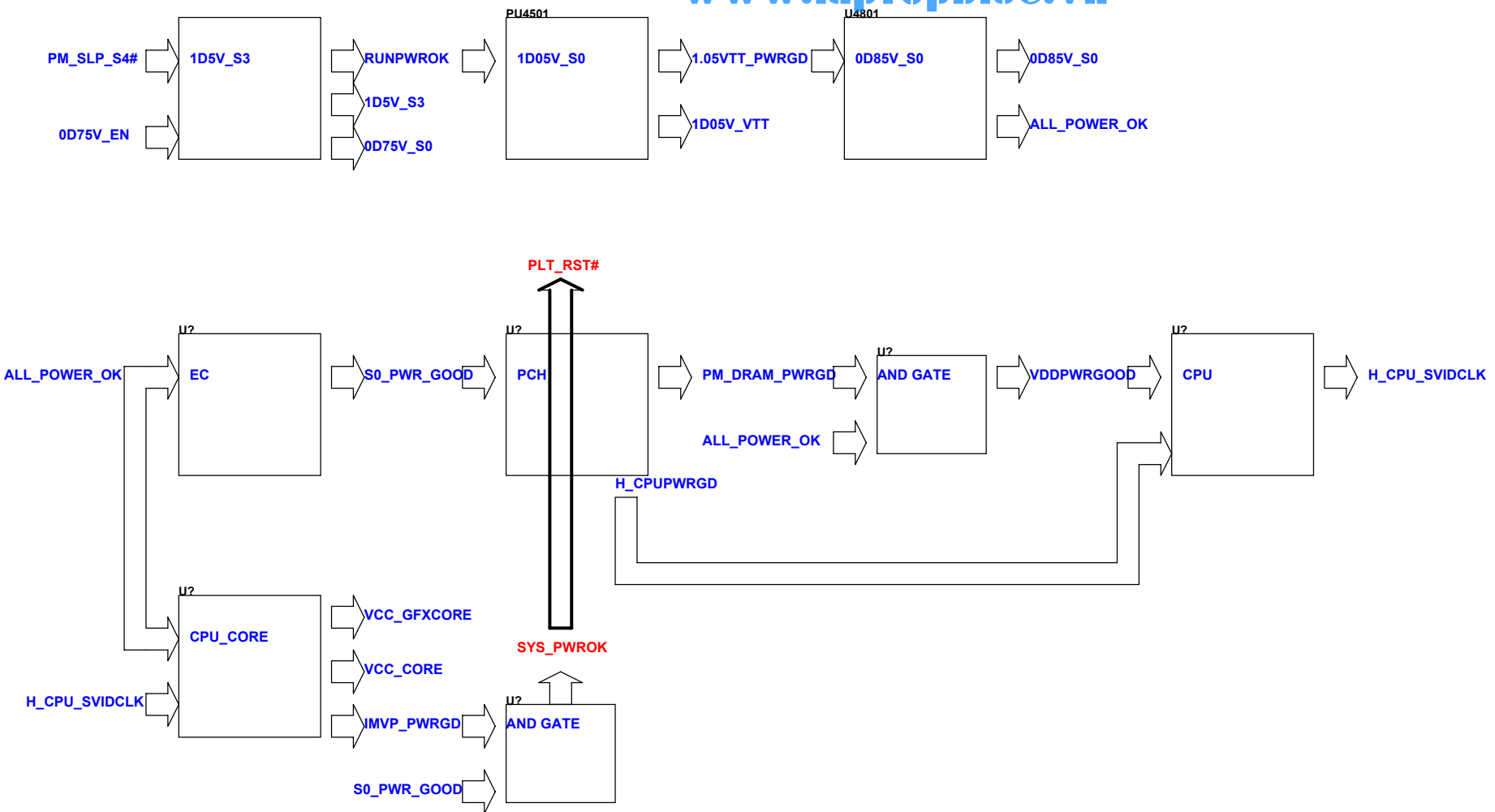
Test Point放在Dimm Door打開可量測處

SB to -1 BOM add SPR2

-2 delete SPR5



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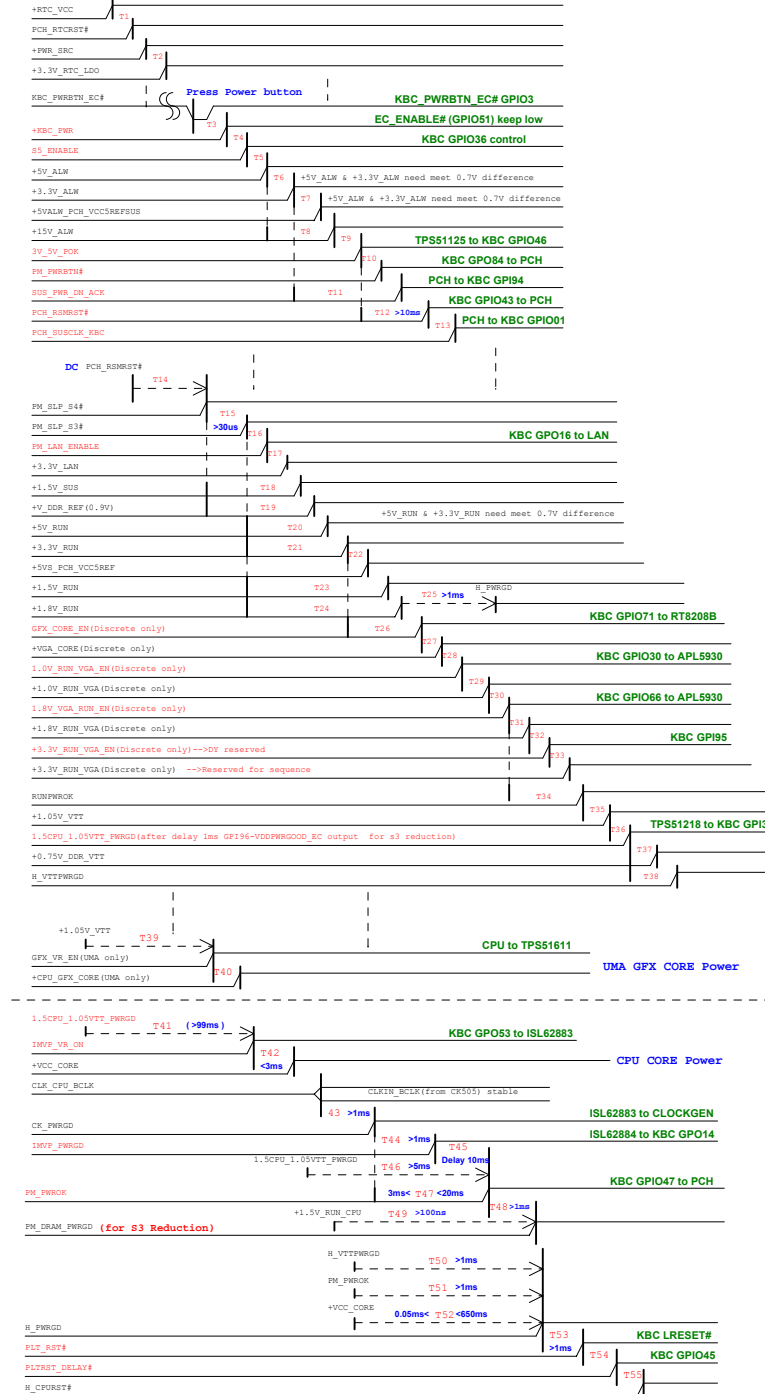


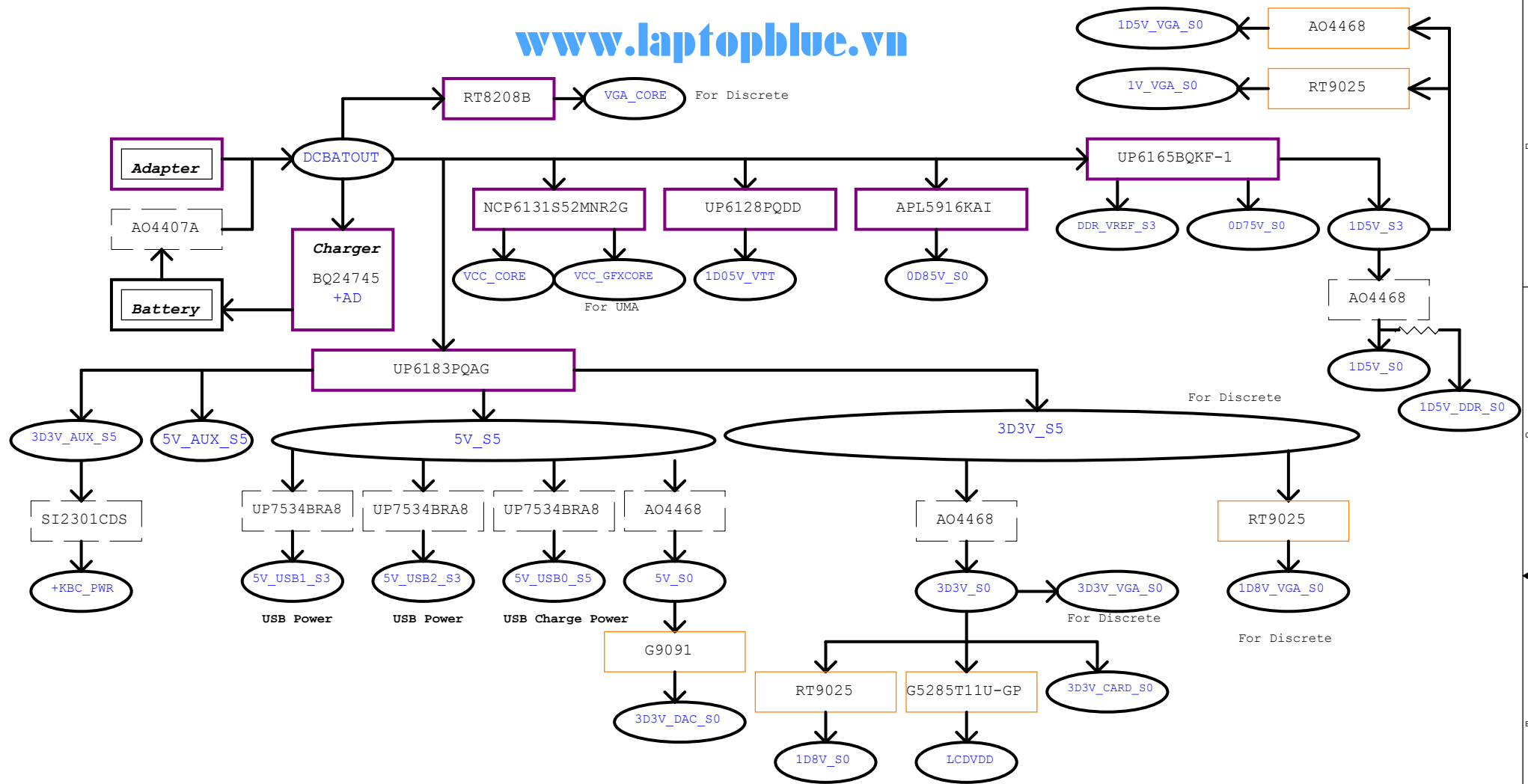
(AC mode)

www.laptopblue.vn (DC mode) red words: XBC GR

(DC mode

red word: KBC GPIC





Power Shape

Regulator

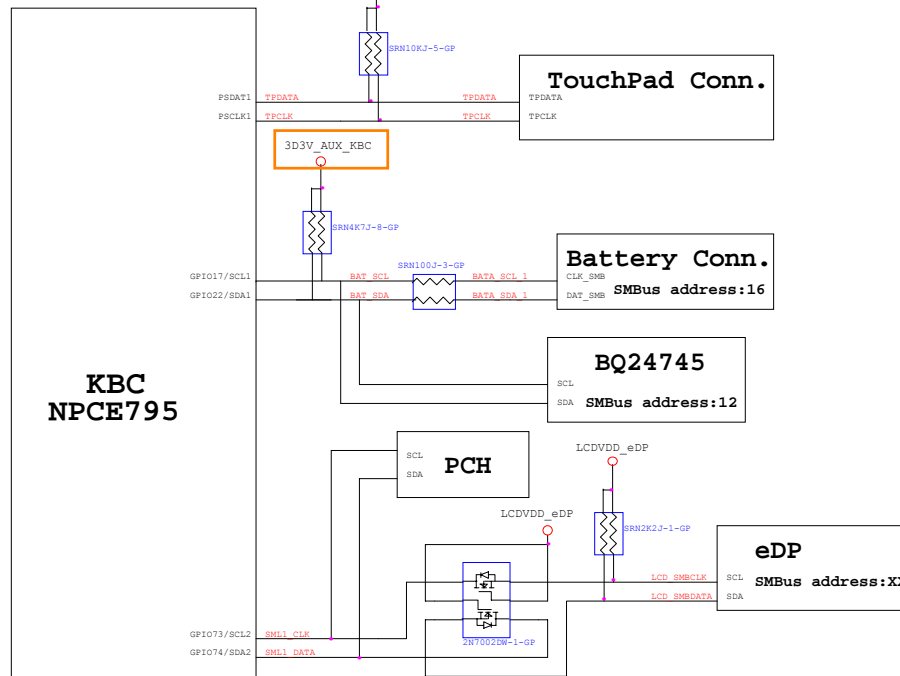
LDO

Switch

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**KBC SMBus 1**

## TouchPad Conn.



KBC  
NPCE795

Battery Conn.

BQ24745

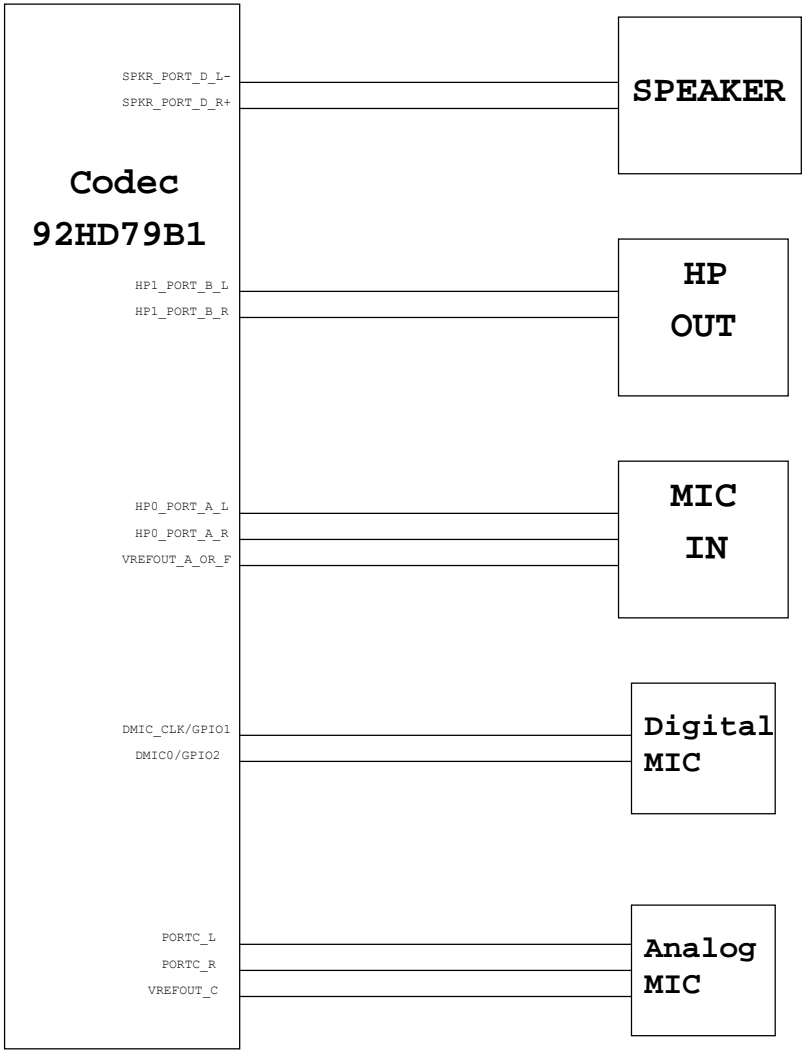
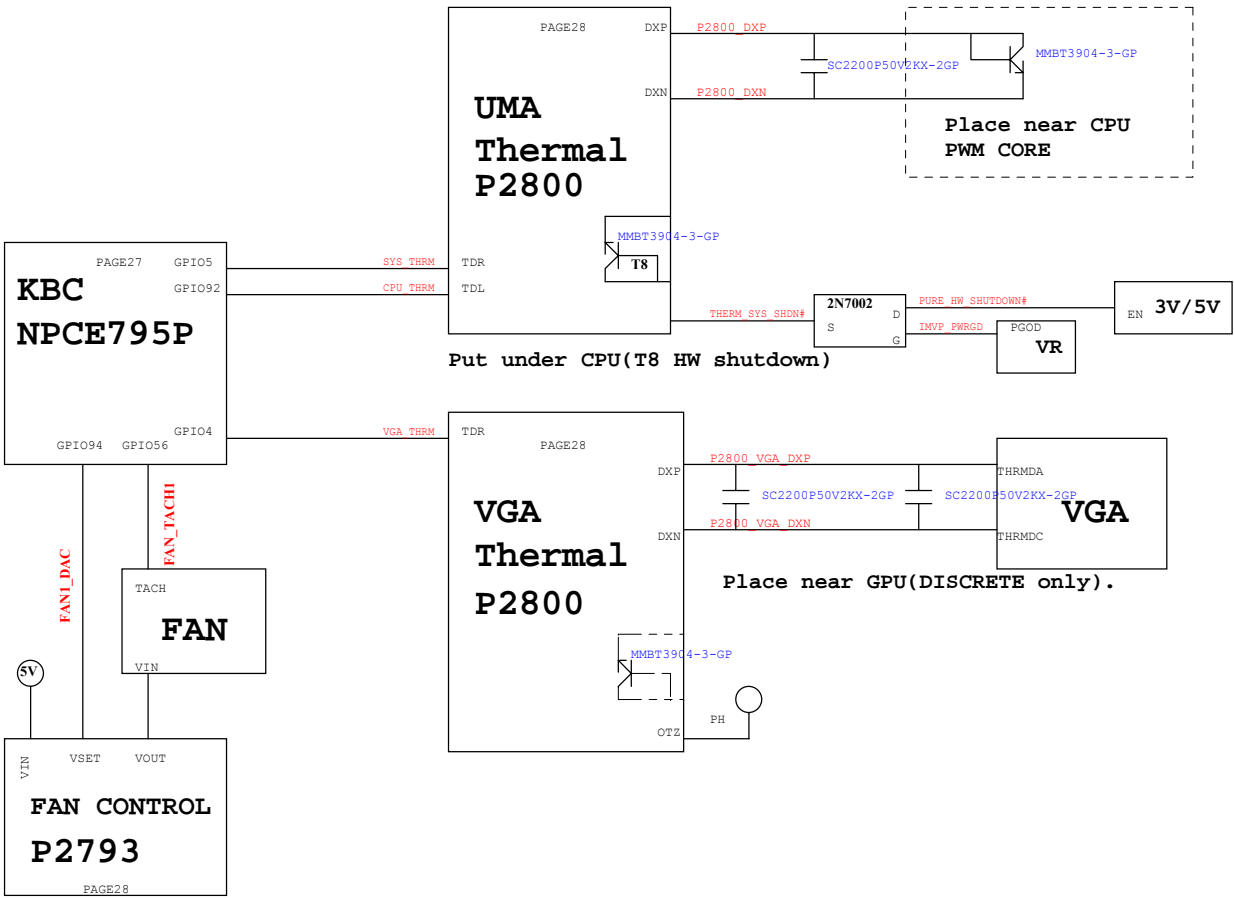
eDP

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Size	Document Number	Rev
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# Thermal Block Diagram

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# Audio Block Diagram



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