1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
		546198			

SCHEM,MLB,M82
PVT
11/14/2007

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7230	1	SCHEM,MLB,M82	SCH	CRITICAL	
820-2179	1	PCBF,MLB,M82	PCB	CRITICAL	

DRAWING
TITLE=M82_MLB
ABBREV=DRAWING
LAST_MODIFIED=Wed Nov 14 17:25:50 2007

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH
NOTED AS
APPLICABLE

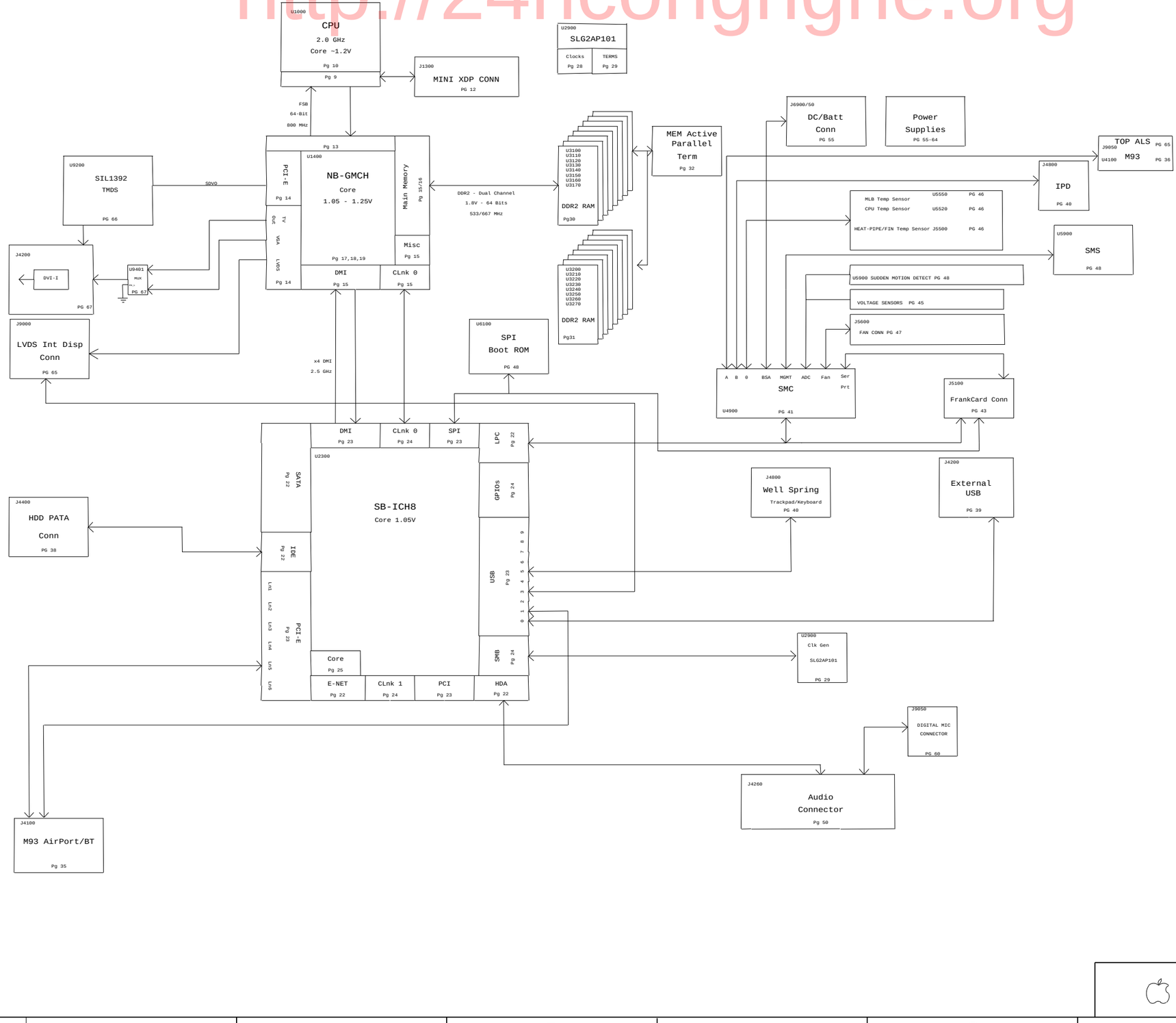
SIZE D

APPLE INC.

TITLE
SCHEM,MLB,M82

DRAWING NUMBER 051-7230
REV. B.0.0

SHT 1 OF 73



System Block Diagram

SYNC_MASTER=WFERRY-WF SYNC_DATE=05/11/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 2 OF 73	

M82 POWER SYSTEM ARCHITECTURE

AC ADAPTER IN — J6980 — PP18V5_DCIN — 6A FUSE F6900 — =PP18V5_G3H_CHGR

=PPDCIN_G3H, PPVBAT_G3H_R, PPBUSB_G3H — D6901 — =PPDCIN_G3H

ENABLE 3.425V G3HOT LT1934 U7790 (PAGE 62) — PP3V42_G3H_REG (? A MAX CURRENT)

PP3V42_G3H_SMC — SMC_PWRGD RN5VD30A-F U5000 (PAGE 41) — SMC_RESET_L

SMC_BATT_CHG_EN

PBUS CONVERTER/ BATTERY CHARGER ISL6258 U7900 (PAGE 63) — ENABLES, VOUT, VIN, CHGR_SMBUS

PPVBAT_G3H_CHGR_REG — 7A FUSE — PPBUSB_G3H — R7980 — =PBUSA_G3H

BATTERY 2S2P

Q7950 — R7930 — CHGR_BGATE — BATT_POS_F

1.05V (S0) PP1V05_S0_REG (9.9 A MAX CURRENT) — 1.5V (S0) PP1V5_S0_REG (3.3 A MAX CURRENT) — TPS51124 U7300 (PAGE 58) — PGOOD_1V5S0, PGOOD_1V05S0

U2803 — VR_PWRGD_CK505 — VR_PWRGD_CLKEN

CLOCK SLG2AP101 U2900 (PAGE 28) — CLK_PWRGD

ICH8M (PAGE 22) — CK_PWRGD, VRMPWRGD, PWRBTN*, PLTRST*, RSMRST*, PWROK, CPU_PWRGD(GPIO49)

NB_RESET_L, TMDS_RST_L, AIRPORT_RST_L, LCDBKLT_PLT_RST_L, PLT_RST_L, U2880, CPU_PWRGD

PM_SB_PWROK — U2801

CPU PWRGOOD, RESET* U1000 (PAGE 9)

CRESTLINE U1400 (PAGE 13) — PWROK, H_CPURST* — FSB_CPURST_L

Q7860 — DELAY R-10K C-0.002uF P5VS3_EN_L (S3); DELAY R-10K C-0.01uF P3V3S3_EN_L (S3)

CPUVCORE U7100 (PAGE 56) — VIN, VOUT, CLKEN#, VR_ON, PGOOD — IMVP_VR_ON — PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU (30 A MAX CURRENT) — VR_PWRGD_CK505_L — VR_PWRGOOD_DELAY

ICH — PM_S4_STATE_L, PM_SLP_S3_L

SMC U4900 (PAGE 40) — PG2, PG3, P60 — SMC_PM_G2_EN (S5)

5V 5VS5_RUNSS (S5) — 3.3V 3VS5_RUNSS (S5) — TPS51120 U7600 (PAGE 60) — PGOOD1,2 — RSMRST_PWRGD

PP5V_S5_REG (? A MAX CURRENT) — PP5V_S5

PP3V3_S5_REG (? A MAX CURRENT) — PP3V3_S5

Q7000 — PP5V_S0 — P5VS0_EN — TPS79933 U2280 (PAGE 21) — P3V3_S0_NB_TVDAC (205mA MAX CURRENT)

Q7865 — PP5V_S3 — P5VS3_EN_L

Q7866 — PP3V3_S3 — P3V3S3_EN_L

1.25V S0 LTC3412A U7750 (PAGE 61) — 1V25S0_RUNSS — P1V25_S0_REG (3 A MAX CURRENT)

Q7001 — PP3V3_S0 — P3V3S0_EN

U7002 — PP1V25_S0_FET, ALL_SYS_PWRGD_AND — ALL_SYS_PWRGD

PGOOD_1V5S0, PGOOD_1V05S0 — PGOOD_SEQUENCER

BATTERY ONLY: 05 — ADAPTER IN : 10-1

SMC U4900 (PAGE 40) — RSMRST_OUT(P15), PWRGD(P12) 99ms DLY, IMVP_VR_ON(P16), RSMRST_IN(P13), PLT_RST*, PWR_BUTTON(P90), P17(BTN_OUT), RST* — PM_RSMRST_L, IMVP_VR_ON, SMC_LRESET_L, PM_PWRBTN_L, SMC_RESET_L — SMC_ONOFF_L — PM_SLP_S5_L, PM_S4_STATE_L, PM_SLP_S3_L — SLP_S5_L(P95), SLP_S4_L(P94), SLP_S3_L(P93)

SMC_ADAPTER_PRESENT — WOW_EN — PM_WLAN_EN_L

GPU_VCORE ADP3209 U7200 (PAGE 57) — VIN, EN, VCC, VOUT — PP5V_S0_NB_GFX_IMVP — GFX_VR_EN, GCORE_EN — =PPVCORE_S0_NB_GFX_IMVP (13 A MAX CURRENT)

Q7004 — =PP1V8_S0_FET — =PP1V8_S0_NB_DPLL — P1V8S0_EN

MCH DPLL TPS731125 U2265 (PAGE 21) — VIN, ENA, VOUT — P1V25_S0_NB_DPLL

PP1V8_S3_FET — PP1V8_S3_REG (11 A MAX CURRENT)

1.8V 1V8S3_RUNSS — 0.9V PM_SLP_S3_L — TPS51116 U7500 (PAGE 59) — VIN, VLDOIN, S5, S3, VOUT1, VOUT2 — PP0V9_S0_REG — PGOOD_1V8S3

R7870

RUNSS_GATE_D — Q7006, Q7007 — DELAY R-330 C-0.022uF 1V5S0_RUNSS (S0); DELAY R-330 C-0.01uF 1V05S0_RUNSS (S0); DELAY R-330 C-1000PF 1V25S0_RUNSS (S0)

U7000 ISL6130IRZA (PAGE 56) — RST*, UVLO_A, UVLO_B, UVLO_C, UVLO)D, ENABLE_1, GATE A, GATE B, GATE C, GATE D — PGOOD_1V8S3, PP5V_S0_FET, PP3V3_S0_FET, PP1V8_S0_FET, PM_SLP_S3_L — P5VS0_EN, P3V3S0_EN, P1V8S0_EN, RUNSS_GATE_D

Power Block Diagram

SYNC_MASTER=POWER — SYNC_DATE=06/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 3 OF 73	

BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7886	PCBA,MLB,1.6GHZ,MI 2GB,SS CAP,M82	EEE_XSC,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_SS_CAP
630-9024	PCBA,MLB,1.6GHZ,HY 2GB,SS CAP,M82	EEE_YMS,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_SS_CAP
630-9133	PCBA,MLB,1.8GHZ,MI 2GB,SS CAP,M82	EEE_Z80,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_SS_CAP
630-9134	PCBA,MLB,1.8GHZ,HY 2GB,SS CAP,M82	EEE_Z81,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_SS_CAP
630-9204	PCBA,MLB,1.6GHZ,HY 2GB,MU CAP,M82	EEE_ZU5,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_MU_CAP
630-9205	PCBA,MLB,1.6GHZ,HY 2GB,TY CAP,M82	EEE_ZU6,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_TY_CAP
630-9206	PCBA,MLB,1.6GHZ,MI 2GB,MU CAP,M82	EEE_ZU7,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_MU_CAP
630-9207	PCBA,MLB,1.6GHZ,MI 2GB,TY CAP,M82	EEE_ZU8,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_TY_CAP
630-9208	PCBA,MLB,1.8GHZ,HY 2GB,MU CAP,M82	EEE_ZU9,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_MU_CAP
630-9209	PCBA,MLB,1.8GHZ,HY 2GB,TY CAP,M82	EEE_ZUA,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_TY_CAP
630-9210	PCBA,MLB,1.8GHZ,MI 2GB,MU CAP,M82	EEE_ZUB,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_MU_CAP
630-9211	PCBA,MLB,1.8GHZ,MI 2GB,TY CAP,M82	EEE_ZUC,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_TY_CAP

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XSC]	CRITICAL	EEE_XSC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:YMS]	CRITICAL	EEE_YMS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z80]	CRITICAL	EEE_Z80
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z81]	CRITICAL	EEE_Z81
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU5]	CRITICAL	EEE_ZU5
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU6]	CRITICAL	EEE_ZU6
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU7]	CRITICAL	EEE_ZU7
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU8]	CRITICAL	EEE_ZU8
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU9]	CRITICAL	EEE_ZU9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUA]	CRITICAL	EEE_ZUA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUB]	CRITICAL	EEE_ZUB
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUC]	CRITICAL	EEE_ZUC

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M82_COMMON	ALTERNATE,COMMON,M82_COMMON1,M82_COMMON2,M82_COMMON3
M82_COMMON1	ISL6258,BOOTROM_DEVEL,SMC_PRGRM
M82_COMMON2	SMS_MOT_DIS,LPCPLUS,XDP,DRAM_2GB
M82_COMMON3	
M82_MICRON	DRAM_MICRON,DRAM_SPD_1
M82_HYNIX	DRAM_HYNIX,DRAM_SPD_2
M82_HYNIX_LP	DRAM_HYNIX_LP,DRAM_SPD_2
M82_SS_CAP	SS_CAP_1UF,SS_CAP_2_2UF,SS_CAP_10UF
M82_MU_CAP	MU_CAP_1UF,MU_CAP_2_2UF,MU_CAP_10UF
M82_TY_CAP	TY_CAP_1UF,TY_CAP_2_2UF,TY_CAP_10UF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3522	1	IC,SANTAYNEZ,MEROM,1.6GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_6GHZ
337S3523	1	IC,SANTAYNEZ,MEROM,1.8GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_8GHZ
338S0420	1	IC,965GM,CRESTLINE,USFF BGA	U1400	CRITICAL	
338S0421	1	IC,ICH8M,USFF BGA	U2300	CRITICAL	
359S0130	1	LOW POWER CLOCK SYNTHESIZER,SLG2AP101,68PIN	U2900	CRITICAL	
335S0510	1	IC, 16MBIT 8-PIN SERIAL FLASH,VWQPN	U6100	CRITICAL	BOOTROM_BLANK_2MB
335S0509	1	IC, 32MBIT 8-PIN SERIAL FLASH, WSON8	U6100	CRITICAL	BOOTROM_BLANK_4MB
341S2111	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M82	U6100	CRITICAL	BOOTROM_DEVEL
341S2112	1	IC,EFI,BOOTROM FINAL (LOCKED),M82	U6100	CRITICAL	BOOTROM_FINAL
337S3477	1	SST89V54RD MICROCONTROLLER	U9300	CRITICAL	SST8051_BLANK
341S2173	1	IC,PRGM,SST SST89V54RD,UCNTRLR,M82	U9300	CRITICAL	SST8051_PRGRM
338S0422	1	IC,SMC,HS8/2117	U4900	CRITICAL	SMC_BLANK
341S2115	1	IC,PRGRM,SMC (NEW),M82	U4900	CRITICAL	SMC_PRGRM
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3140,U3150,U3160,U3170	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3240,U3250,U3260,U3270	CRITICAL	DRAM_MICRON
333S0411	4	HYNIX,DRAM,64M16,8x13	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX_LP
353S1938	1	IC,ISL6258,REV2,BAT CHGR, 28P QFN	U7900	CRITICAL	ISL6258
197S0213	1	14.318MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_14MHZ
197S0231	1	20MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_20MHZ
197S0257	1	33MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_33MHZ
337S3563	1	IC,SANTAYNEZ,MEROM,1.6GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_6GHZ
337S3564	1	IC,SANTAYNEZ,MEROM,1.8GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_8GHZ
338S0514	1	IC,965GM,CRESTLINE,PRQ,USFF BGA	U1400	CRITICAL	NB_PRQ
338S0515	1	IC,ICH8M,PRQ,USFF BGA	U2300	CRITICAL	SB_PRQ

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S0093	128S0092	ALL	33UF 20% 16V DCASE	
376S0466	376S0410	ALL	Si4413 for Si4405	
740S0044	740S0028	ALL	0.5A OC FUSE	
104S0023	104S0018	ALL	1206 1/4W .002 OHM	

CONFIGURATION OPTIONS

SYNC_MASTER=(N/A) SYNC_DATE=(N/A)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 4 OF 73	

1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	5	CAP, 1UF, 6.3V, 10%, 0402	C1801,C1802,C2144,C2151,C2170	CRITICAL	SS_CAP_1UF
138S0629	9	CAP, 1UF, 6.3V, 10%, 0402	C2265,C2280,C2600,C2703,C2805,C2900,C7000,C7100,C7101	CRITICAL	SS_CAP_1UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0628	5	CAP, 1UF, 6.3V, 10%, 0402	C1801,C1802,C2144,C2151,C2170	CRITICAL	MU_CAP_1UF
138S0628	9	CAP, 1UF, 6.3V, 10%, 0402	C2265,C2280,C2600,C2703,C2805,C2900,C7000,C7100,C7101	CRITICAL	MU_CAP_1UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0630	5	CAP, 1UF, 6.3V, 10%, 0402	C1801,C1802,C2144,C2151,C2170	CRITICAL	TY_CAP_1UF
138S0630	9	CAP, 1UF, 6.3V, 10%, 0402	C2265,C2280,C2600,C2703,C2805,C2900,C7000,C7100,C7101	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	SS_CAP_2_2UF
138S0632	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2214,C2215,C2240,C2241,C2242,C2243	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9980,C9981,C9982,C9983,C9984,C9985,C9986,C9987,C9988,C9989	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C9990,C9991,C9992,C9993,C9994,C9995,C9996,C9997	CRITICAL	SS_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1282,C1283,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	SS_CAP_2_2UF
138S0632	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1622,C1624,C4800	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3400,C3401,C3404,C3405,C3410,C3411,C3412,C3414,C3415,C3416	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3420,C3421,C3424,C3425,C3430,C3431,C3434,C3435,C3440,C3441	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3442,C3444,C3445,C3446,C3450,C3451,C3454,C3455	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3540,C3541	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	MU_CAP_2_2UF
138S0633	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2214,C2215,C2240,C2241,C2242,C2243	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9980,C9981,C9982,C9983,C9984,C9985,C9986,C9987,C9988,C9989	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C9990,C9991,C9992,C9993,C9994,C9995,C9996,C9997	CRITICAL	MU_CAP_2_2UF
138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1282,C1283,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	MU_CAP_2_2UF
138S0633	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1622,C1624,C4800	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3400,C3401,C3404,C3405,C3410,C3411,C3412,C3414,C3415,C3416	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3420,C3421,C3424,C3425,C3430,C3431,C3434,C3435,C3440,C3441	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3442,C3444,C3445,C3446,C3450,C3451,C3454,C3455	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3540,C3541	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	TY_CAP_2_2UF
138S0634	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2214,C2215,C2240,C2241,C2242,C2243	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9980,C9981,C9982,C9983,C9984,C9985,C9986,C9987,C9988,C9989	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C9990,C9991,C9992,C9993,C9994,C9995,C9996,C9997	CRITICAL	TY_CAP_2_2UF
138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1282,C1283,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	TY_CAP_2_2UF
138S0634	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1622,C1624,C4800	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3400,C3401,C3404,C3405,C3410,C3411,C3412,C3414,C3415,C3416	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3420,C3421,C3424,C3425,C3430,C3431,C3434,C3435,C3440,C3441	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3442,C3444,C3445,C3446,C3450,C3451,C3454,C3455	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3540,C3541	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	SS_CAP_10UF
138S0626	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1280	CRITICAL	SS_CAP_10UF
138S0626	9	CAP, 10UF, 6.3V, 20%, 0603	C2190,C2195,C2213,C2219,C2231,C2232,C2260,C2266,C2285	CRITICAL	SS_CAP_10UF
138S0626	5	CAP, 10UF, 6.3V, 20%, 0603	C2705,C2706,C2708,C2735,C2901	CRITICAL	SS_CAP_10UF
138S0626	6	CAP, 10UF, 6.3V, 20%, 0603	C3490,C3491,C3492,C3590,C3591,C3592	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4109,C4400,C4613,C5066,C7281,C7301,C7350,C7351	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C7502,C7507,C7508,C7541,C7603,C7604,C7650,C7690	CRITICAL	SS_CAP_10UF
138S0626	5	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9204,C9205,C9213,C9240	CRITICAL	SS_CAP_10UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	MU_CAP_10UF
138S0625	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1280	CRITICAL	MU_CAP_10UF
138S0625	9	CAP, 10UF, 6.3V, 20%, 0603	C2190,C2195,C2213,C2219,C2231,C2232,C2260,C2266,C2285	CRITICAL	MU_CAP_10UF
138S0625	5	CAP, 10UF, 6.3V, 20%, 0603	C2705,C2706,C2708,C2735,C2901	CRITICAL	MU_CAP_10UF
138S0625	6	CAP, 10UF, 6.3V, 20%, 0603	C3490,C3491,C3492,C3590,C3591,C3592	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4109,C4400,C4613,C5066,C7281,C7301,C7350,C7351	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C7502,C7507,C7508,C7541,C7603,C7604,C7650,C7690	CRITICAL	MU_CAP_10UF
138S0625	5	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9204,C9205,C9213,C9240	CRITICAL	MU_CAP_10UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	TY_CAP_10UF
138S0627	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1280	CRITICAL	TY_CAP_10UF
138S0627	9	CAP, 10UF, 6.3V, 20%, 0603	C2190,C2195,C2213,C2219,C2231,C2232,C2260,C2266,C2285	CRITICAL	TY_CAP_10UF
138S0627	5	CAP, 10UF, 6.3V, 20%, 0603	C2705,C2706,C2708,C2735,C2901	CRITICAL	TY_CAP_10UF
138S0627	6	CAP, 10UF, 6.3V, 20%, 0603	C3490,C3491,C3492,C3590,C3591,C3592	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4109,C4400,C4613,C5066,C7281,C7301,C7350,C7351	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C7502,C7507,C7508,C7541,C7603,C7604,C7650,C7690	CRITICAL	TY_CAP_10UF
138S0627	5	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9204,C9205,C9213,C9240	CRITICAL	TY_CAP_10UF

Acoustic Cap BOM Config Tables

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE D | DRAWING NUMBER 051-7230 | REV. 8.0.0

SCALE NONE | SHT 5 OF 73

ICT Test Points

These nets have a ICT_TEST property   This indicates a MUSTHAVE requirement for ICT

ICT_TEST

	TRUE	PP18V5_DCIN	6 7 50 72
I95	TRUE	BATT_POS	57 58 60 72 44 49 51 56
I96	TRUE	PP3V3_S5	27 28 36 43 7 8 24 25 26
I97	TRUE	PP3V42_G3H	41 42 43 44 6 7 8 23 26 27 28 39 40
	TRUE	GND	57 59 72
I100	TRUE	PM_SLP_S3_L	6 7 25 36 37 41 42 51 55
I99	TRUE	PM_S4_STATE_L	6 25 36 41 58
I101	TRUE	PM_SLP_S5_L	6 25 41 42
I102	TRUE	SMC_PM_G2_EN	6 41 56 58
I104	TRUE	IMVP_VR_ON	6 41 52
I103	TRUE	GFX_VR_EN	6 9 16 53
I105	TRUE	SMC_BATT_CHG_EN	6 41 42
I107	TRUE	SMC_ONOFF_L	6 7 40 41 42
I106	TRUE	ALL_SYS_PWRGD_AND	6 51
I108	TRUE	PPVBAT_G3H_CHGR_REG	6 59 72
I109	TRUE	CPU_PWRGD	6 10 13 23 66
I110	TRUE	PM_RSMRST_L	6 25 41
I112	TRUE	PM_PWRBTN_L	6 25 41
I111	TRUE	TP_PCI_RST_L	9 24
I113	TRUE	PLT_RST_L	6 7 24 28 60 64
I115	TRUE	SMC_RESET_L	6 41 42 43 41
I114	TRUE	PM_SYSRST_L	28 6 27 54 72 25
I116	TRUE	PP1V5_S0	11 12 22 26 8 54 6 72
I118	TRUE	PP1V05_S0	23 7 26 27 30 13 14 18 19 6 7 8 10 11 12 42
I117	TRUE	PP1V8_S0	21 61 72 6 7 8 19 22 72 51
I119	TRUE	PP1V8_S3	35 51 55 68 6 7 8 16 18 21 31 32 34
I120	TRUE	PP0V9_S0	6 7 8 33 55 72
I121	TRUE	PP0V9_S3	55 72 6 8 31 32 72
I122	TRUE	PP1V25_S0	26 27 51 57 6 7 8 16 18 19 21
I123	TRUE	PP5V_S5	58 72 6 7 8 27 39 51 54 55 56
I125	TRUE	PP5V_S3	6 7 8 40 58 60 72
I124	TRUE	PP5V_S0	
I292	TRUE	PP3V3_S3	53 60 63 64 44 46 51 52 28 29 30 42
I294	TRUE	PP3V3_A_S0	24 25 26 27 6 7 8 13 16
I293	TRUE	PP3V3_B_S0	63 19 21 22 23 6 8 38 47 51 61 62
I295	TRUE	PPVCORE_S0_CPU	65 72 6 7 8 11 12
I297	TRUE	PPVCORE_S0_NB_GFX	52 65 72 6 7 8 18 22 45 53
I296	TRUE	XDP_TCK	6 7 10 13 66
I298	TRUE	XDP_TDI	6 7 10 13 66
I300	TRUE	XDP_TDO	6 7 10 13 66
I299	TRUE	XDP_TMS	6 7 10 13 66
I301	TRUE	XDP_TRST_L	6 7 10 13 66
I302	TRUE	XDP_CPURST_L	6 7 13 66
I303	TRUE	XDP_BPM_L<4>	6 7 10 13 66
I304	TRUE	XDP_BPM_L<5>	6 7 10 13 66
I305	TRUE	XDP_DBRESET_L	6 7 10 13 28
I307	TRUE	XDP_PWRGD	6 7 13
I306	TRUE	SPI_A_SCLK_R	6 43 49 69
I308	TRUE	SMC_MANUAL_RST_L	6 42
I309	TRUE	SMC_TCK	6 41 42 43
I310	TRUE	SMC_TDI	6 41 42 43
I338	TRUE	SMC_TDO	6 41 42 43
I337	TRUE	SMC_TMS	6 41 42 43
I339	TRUE	SMC_TRST_L	6 41 43
I341	TRUE	CPU_A20M_L	6 10 23 66
I340	TRUE	CPU_DPRSTP_L	6 10 16 23 52 66
I343	TRUE	CPU_DPSLP_L	6 10 23 66
I342	TRUE	CPU_FERR_L	6 10 23 66
I344	TRUE	NB_BSEL<0>	6 7 13 16 30 66
I346	TRUE	NB_BSEL<1>	6 7 13 16 30 66
I345	TRUE	NB_BSEL<2>	6 7 13 16 30 66
I347	TRUE	NB_CFG<16>	6 16
I348	TRUE	NB_CFG<19>	6 16
I349	TRUE	NB_CFG<20>	6 16

I126	TRUE	NB_CFG<3>	6 7 13 16
I128	TRUE	NB_CFG<4>	6 7 13 16
I127	TRUE	NB_CFG<5>	6 7 13 16
I129	TRUE	NB_CFG<6>	6 7 13 16
I131	TRUE	NB_CFG<7>	6 7 13 16
I130	TRUE	NB_CFG<8>	6 7 13 16
I132	TRUE	NB_CFG<9>	6 16
I134	TRUE	NB_RESET_L	6 16 28
I133	TRUE	NB_SB_SYNC_L	6 16 25
I135	TRUE	NB_TEST1	6 16
I136	TRUE	NB_TEST2	6 16
I137	TRUE	1V05S0_RUNSS	51 54
I138	TRUE	1V05S0_TRIP	54
I139	TRUE	1V25S0_RUNSS	51 57
I141	TRUE	1V51V05S0_V5FILT	54
I140	TRUE	1V5S0_RUNSS	51 54
I142	TRUE	1V5S0_TRIP	54
I143	TRUE	1V8S3_CS	55
I144	TRUE	1V8S3_V5FILT	55
I146	TRUE	1V8S3_VDDQSET	55
I145	TRUE	3V3S5_CS	56
I147	TRUE	5V3V3S5_TONSEL	56
I149	TRUE	5V3V3S5_V5FILT	56
I148	TRUE	5V3V3S5_VREF	56
I151	TRUE	5V3V3S5_VREG3	56
I150	TRUE	5VS5_CS	56
I152	TRUE	5VS5_VREG	56
I154	TRUE	ADAPTER_SENSE	50
I153	TRUE	AIRPORT_RST_L	7 28 36
I155	TRUE	ALL_SYSPWRGD_DLY	51
I156	TRUE	ALL_SYS_PWRGD	28 41 51 52
I157	TRUE	ALL_SYS_PWRGD_AND	6 51
I273	TRUE	ARB_DETECT_L	25
I274	TRUE	AUD_MIC_CLK	7 37 60
I275	TRUE	AUD_MIC_CLK_F	60
I276	TRUE	AUD_MIC_DATA	7 37 60
I277	TRUE	AUD_MIC_DATA_F	60
I278	TRUE	BATT_POS	6 7 50
I279	TRUE	BATT_POS_F	50 59
I280	TRUE	BOOTROM_OVR_EN_L	23 25 43
I281	TRUE	CHGR_AGATE	59
I283	TRUE	CHGR_AMON	59
I282	TRUE	CHGR_BGATE	59
I284	TRUE	CHGR_BMON	59
I286	TRUE	CHGR_BOOT	59
I285	TRUE	CHGR_CSIN	59
I287	TRUE	CHGR_CSIP	59
I288	TRUE	CHGR_CSON	59
I289	TRUE	CHGR_CSOP	59
I291	TRUE	CHGR_DCIN	59
I290	TRUE	CHGR_LOWCURRENT_GATE	59
I324	TRUE	CHGR_LOWCURRENT_REF	59
I325	TRUE	CHGR_SGATE	59
I326	TRUE	CHGR_SGATE_DIV	59
I327	TRUE	CHGR_VCOMP_R	59
I328	TRUE	CHGR_VDD	59
I329	TRUE	CHGR_VDDP	59
I330	TRUE	CHGR_VNEG	59
I331	TRUE	CHGR_VNEG_R	59
I332	TRUE	CK505_CLK14P3M_TIMER	29 30
I333	TRUE	CK505_FSA	30 71
I334	TRUE	CK505_FSB_TEST_MODE	29 30
I336	TRUE	CK505_FSC	30 71
I335	TRUE	CK505_PCI3_CLK	29 30 71

I158	TRUE	CK505_PCI5_FCTSEL1	29 30
I160	TRUE	CK505_PCIF0_CLK	29 30
I159	TRUE	CK505_PCIF1_CLK	29 30 71
I161	TRUE	CK505_SRC_CLKREQ6_L	7 29 36
I163	TRUE	CK505_USB48_FSA	29 30
I162	TRUE	CK505_XTAL_OUT	29
I164	TRUE	CLINK_NB_CLK	16 25 70
I166	TRUE	CLINK_NB_DATA	16 25 70
I165	TRUE	CLINK_NB_RESET_L	16 25 70
I167	TRUE	CLK_PWRGD	25 29
I168	TRUE	CPU_A20M_L	6 10 23 66
I169	TRUE	CPU_BSEL<0>	10 30 66
I170	TRUE	CPU_BSEL<1>	10 30 66
I171	TRUE	CPU_BSEL<2>	10 30 66
I173	TRUE	CPU_COMP<0>	10 66
I172	TRUE	CPU_COMP<1>	10 66
I174	TRUE	CPU_COMP<2>	10 66
I175	TRUE	CPU_COMP<3>	10 66
I176	TRUE	CPU_DPRSTP_L	6 10 16 23 52 66
I178	TRUE	CPU_DPSLP_L	6 10 23 66
I177	TRUE	CPU_FERR_L	6 10 23 66
I179	TRUE	CPU_GTLREF	10 66
I181	TRUE	CPU_IERR_L	10 66
I180	TRUE	CPU_IGNNE_L	10 23 66
I183	TRUE	CPU_INIT_L	10 23 66
I182	TRUE	CPU_INTR	10 23 66
I184	TRUE	CPU_NMI	10 23 66
I186	TRUE	CPU_PROCHOT_BUF	42
I185	TRUE	CPU_PROCHOT_L	10 42 52 66
I187	TRUE	CPU_PROCHOT_L_R	42
I188	TRUE	CPU_PWRGD	6 10 13 23 66
I189	TRUE	CPU_SMI_L	10 23 66
I254	TRUE	CPU_STPCLK_L	10 23 66
I255	TRUE	CPU_THERMD_N	10 46 66
I256	TRUE	CPU_THERMD_P	10 46 66
I257	TRUE	CPU_THERMTRIP_R	23
I258	TRUE	CPU_VCCSENSE_N	11 52 66
I259	TRUE	CPU_VCCSENSE_P	11 52 66
I260	TRUE	CPU_VID<6..0>	11 12 52 66
I261	TRUE	CRT_BLUE	15 63 67
I262	TRUE	CRT_GREEN	15 63 67
I264	TRUE	CRT_HSYNC_LS	63
I263	TRUE	CRT_HSYNC_LS_R	63
I265	TRUE	CRT_HSYNC_R	15 63 67
I267	TRUE	CRT_RED	15 63 67
I266	TRUE	CRT_TVO_IREF	15 63 67
I268	TRUE	CRT_VSYNC_LS	63
I269	TRUE	CRT_VSYNC_LS_R	63
I270	TRUE	CRT_VSYNC_R	15 63 67
I272	TRUE	DEBUG_RESET_L	28 43
I271	TRUE	DLY_OFF_A	51
I311	TRUE	DLY_OFF_B	51
I312	TRUE	DLY_OFF_C	51
I313	TRUE	DLY_OFF_D	51
I314	TRUE	DMI_IRCOMP_R	24
I315	TRUE	DMI_N2S_N<3..0>	16 24 67
I316	TRUE	DMI_N2S_P<3..0>	16 24 67
I317	TRUE	DMI_S2N_N<3..0>	16 24 67
I318	TRUE	DMI_S2N_P<3..0>	16 24 67
I319	TRUE	DVI_HOST	7 37 63
I320	TRUE	DVI_HOTPLUG_DET	24 61 62
I321	TRUE	DVI_HOTPLUG_DET_BUF	61 62
I323	TRUE	DVI_HOTPLUG_DET_DEL_L	62
I322	TRUE	DVI_HOTPLUG_DET_INT_L	62

I190	TRUE	DVI_HPDET_RC	62
I192	TRUE	EXCARD_OC_L	24
I191	TRUE	EXTAUSB_OC_F_L	39
I193	TRUE	EXTAUSB_OC_L	7 9 13 24 39
I195	TRUE	EXTBUSB_OC_L	7 9 13 24
I194	TRUE	EXTGPU_LVDS_EN	7 13 24
I196	TRUE	EXT_COMPVID_B	63 67
I198	TRUE	EXT_C_R	63 67
I197	TRUE	EXT_Y_G	63 67
I199	TRUE	FAN_RT_PWM	7 47
I200	TRUE	FAN_RT_TACH	7 47
I201	TRUE	FRANKCARD_GPIO	25 43
I202	TRUE	FSB_CLK_CPU_N	10 29 30 71
I203	TRUE	FSB_CLK_CPU_P	10 29 30 71
I205	TRUE	FSB_CLK_NB_N	14 29 30 71
I204	TRUE	FSB_CLK_NB_P	14 29 30 71
I206	TRUE	FSB_CPURST_L	10 13 14 66
I207	TRUE	FWH_MFG_MODE	25
I208	TRUE	GCORE_BST_D	53
I210	TRUE	GCORE_COMP_R	53
I209	TRUE	GCORE_CSFB	53
I211	TRUE	GCORE_FBRTN	53
I213	TRUE	GCORE_LLINE	53
I212	TRUE	GCORE_PMON	53
I215	TRUE	GCORE_PMONFS	53
I214	TRUE	GCORE_PWRGD	53
I216	TRUE	GCORE_RAMP	53
I218	TRUE	GCORE_RPM	53
I217	TRUE	GCORE_RT	53
I219	TRUE	GCORE_ST	53
I220	TRUE	GCORE_SW	53
I221	TRUE	GCORE_SW_R	53
I222	TRUE	GCORE_VARFREQ	53
I223	TRUE	GCORE_VCC	53
I224	TRUE	GCORE_VDC_DIV	53
I225	TRUE	GCORE_VRPM	53
I226	TRUE	GFX_VID<3..0>	16 22 53
I227	TRUE	GFX_VR_EN	6 9 16 53
I228	TRUE	GLAN_COMP	23 70
I229	TRUE	GND_1V51V05S0_SGND	54
I230	TRUE	GND_1V8S3_CSGND	55
I232	TRUE	GND_1V8S3_SGND	55
I231	TRUE	GND_5V3V3S5_SGND	56
I233	TRUE	GND_ALS_F	
I235	TRUE	GND_CHGR_SGND	59
I234	TRUE	GND_GCORE_PGND	53
I236	TRUE	GND_IMVP6_SGND	52
I237	TRUE	GND_LCDBKLT_GNDA	64
I238	TRUE	GND_P1V2S3_SGND	57
I240	TRUE	GND_SMC_AVSS	41 42 45 53 59
I239	TRUE	HDA_BIT_CLK	7 9 23 37 69
I241	TRUE	HDA_BIT_CLK_R	23 69
I242	TRUE	HDA_DOCK_EN_L	23
I243	TRUE	HDA_RST_L	9 23 37 69
I244	TRUE	HDA_RST_L_R	23 69
I245	TRUE	HDA_SDIN0	7 9 23 37 69
I246	TRUE	HDA_SDIN1	
I247	TRUE	HDA_SDOUT	7 9 23 37 69
I248	TRUE	HDA_SDOUT_R	23 69
I249	TRUE	HDA_SYNC	7 9 23 37 69
I250	TRUE	HDA_SYNC_R	23 69
I251	TRUE	HDMI_HOST	7 37 63
I253	TRUE	I2C_TOP_ALS_SCL_F	60
I252	TRUE	I2C_TOP_ALS_SDA_F	60

I414	TRUE	IDE_IRQ14	23 38 69
I415	TRUE	IDE_PDA<2..0>	23 38 69
I416	TRUE	IDE_PDCS1_L	23 38 69
I417	TRUE	IDE_PDCS3_L	23 38 69
I418	TRUE	IDE_PDD<15..0>	23 38 69
I419	TRUE	IDE_PDDACK_L	23 38 69
I420	TRUE	IDE_PDDREQ	23 38 69
I421	TRUE	IDE_PDIORDY	23 38 69
I422	TRUE	IDE_PDIOR_L	23 38 69
I424	TRUE	IDE_PDIOW_L	23 38 69
I423	TRUE	IDE_RESET_BUF_L	38
I425	TRUE	IDE_RESET_L	24 38
I427	TRUE	IMVP6_BOOT	52
I426	TRUE	IMVP6_BOOT_RC	52
I428	TRUE	IMVP6_COMP_R	52
I429	TRUE	IMVP6_DROOP	52
I430	TRUE	IMVP6_PHASE	52
I432	TRUE	IMVP6_PVCC	52
I431	TRUE	IMVP6_RBIAS	52
I433	TRUE	IMVP6_SOFT	52
I434	TRUE	IMVP6_VDIFF	52
I435	TRUE	IMVP6_VDIFF_RC	52
I436	TRUE	IMVP6_VO_R	52
I437	TRUE	IMVP6_VR_TT	52
I438	TRUE	IMVP6_VSEN_N	52 66
I439	TRUE	IMVP6_VSEN_P	52 66
I440	TRUE	IMVP6_VSUM	52
I441	TRUE	IMVP6_VW	52
I442	TRUE	IMVP_DPRSLPVR	52 66
I443	TRUE	IMVP_VR_ON	6 41 52
I445	TRUE	INT_PIRQA_L	24 70
I444	TRUE	INT_PIRQB_L	24 70
I447	TRUE	INT_PIRQC_L	24 70
I446	TRUE	INT_PIRQD_L	24 70
I448	TRUE	INT_PIRQE_L	24 70
I450	TRUE	INT_PIRQF_L	24 70
I449	TRUE	INT_SERIRQ	25 41 43
I452	TRUE	LAN_ENERGY_DET	23
I451	TRUE	LAN_PHYPC	23 25
I453	TRUE	LCDBKLT_ENA	64
I455	TRUE	LCDBKLT_ISET	64
I454	TRUE	LCDBKLT_OVP	64
I457	TRUE	LCDBKLT_PWM_UNBUF	9 15 64
I456	TRUE	LCDBKLT_PWREN	9 15 64
I458	TRUE	LCDBKLT_RT	64
I460	TRUE	LCDBKLT_RTN<6..1>	7 60 64
I459	TRUE	LCDBKLT_RTN_RC<6..1>	64
I462	TRUE	LCDBKLT_SSTCMP	64
I461	TRUE	LCDBKLT_SSTCMP_RC	64
I463	TRUE	LCDBKLT_VREF	64
I465	TRUE	LCDVDD_PWREN_L	60
I464	TRUE	LCDVDD_PWREN_L_R	60
I466	TRUE	LOCAL_CTRL_CLK	7 13 15
I468	TRUE	LOCAL_CTRL_DATA	7 13 15
I467	TRUE	LPC_AD<3..0>	23 41 43
I470	TRUE	LPC_FRAME_L	23 41 43
I469	TRUE	LSOC_H	
I471	TRUE	LSOC_H_R	7
I473	TRUE	LVDS_A_CLK_F_N	7 60
I472	TRUE	LVDS_A_CLK_F_P	7 60
I475	TRUE	LVDS_A_CLK_N	15 60 67
I474	TRUE	LVDS_A_CLK_P	15 60 67
I476	TRUE	LVDS_A_DATA_F_N<2..0>	60 67
I477	TRUE	LVDS_A_DATA_F_P<2..0>	60 67

I350	TRUE	LVDS_A_DATA_N<2>	7 15 60 67
I351	TRUE	LVDS_A_DATA_P<2>	7 15 60 67
I352	TRUE	LVDS_DDC_CLK	7 15 60
I353	TRUE	LVDS_DDC_DATA	7 15 60
I354	TRUE	LVDS_IBG	15 60 67
I355	TRUE	LVDS_VDD_EN	15 60
I356	TRUE	MEM_ODT<3..0>	16 31 32 33 68
I357	TRUE	MEM_RCOMP	16
I358	TRUE	MEM_RCOMP_L	16
I360	TRUE	MEM_RCOMP_VOH	16
I359	TRUE	MEM_RCOMP_VOL	16
I361	TRUE	NB_BSEL<0>	6 7 13 16 30 66
I363	TRUE	NB_BSEL<1>	6 7 13 16 30 66
I362	TRUE	NB_BSEL<2>	6 7 13 16 30 66
I364	TRUE	NB_CFG<16>	6 16
I365	TRUE	NB_CFG<19>	6 16
I366	TRUE	NB_CFG<20>	6 16
I368	TRUE	NB_CFG<3>	6 7 13 16
I367	TRUE	NB_CFG<4>	6 7 13 16
I369	TRUE	NB_CFG<5>	6 7 13 16
I370	TRUE	NB_CFG<6>	6 7 13 16
I371	TRUE	NB_CFG<7>	6 7 13 16
I372	TRUE	NB_CFG<8>	6 7 13 16
I373	TRUE	NB_CFG<9>	6 16
I374	TRUE	NB_CLINK_VREF	16 70
I375	TRUE	NB_CLK100M_DPLLSS_N	30 71 9 16 29
I376	TRUE	NB_CLK100M_DPLLSS_P	71 9 16 29 30
I377	TRUE	NB_CLK100M_PCIE_N	16 29 30 71
I378	TRUE	NB_CLK100M_PCIE_P	16 29 30 71
I379	TRUE	NB_CLK96M_DOT_N	9 16 29 30 71
I381	TRUE	NB_CLK96M_DOT_P	9 16 29 30 71
I380	TRUE	NB_CLKREQ_L	16 29
I383	TRUE	NB_FSB_RCOMP	14
I382	TRUE	NB_FSB_SCOMP	14
I384	TRUE	NB_FSB_SCOMP_L	14
I386	TRUE	NB_FSB_SWING	14
I385	TRUE	NB_FSB_VREF	14
I388	TRUE	NB_RESET_L	6 16 28
I387	TRUE	NB_SB_SYNC_L	6 16 25
I389	TRUE	NB_TEST1	6 16
I391	TRUE	NB_TEST2	6 16
I390	TRUE	NB_VCCSM_LF1	18 68
I393	TRUE	NB_VCCSM_LF2	18 68
I392	TRUE	NB_VCCSM_LF3	18 68
I394	TRUE	NB_VCCSM_LF4	18 68
I396	TRUE	NB_VCCSM_LF5	18 68
I395	TRUE	NB_VCCSM_LF6	18 68
I398	TRUE	NB_VCCSM_LF7	18 68
I397	TRUE	NB_VTTLF_CAP1	19
I399	TRUE	NB_VTTLF_CAP2	19
I401	TRUE	NB_VTTLF_CAP3	19
I400	TRUE	ODD_PWR_EN_L	24
I402	TRUE	ONEWIRE_DCIN_DIV	50
I404	TRUE	ONEWIRE_EN	50
I403	TRUE	ONEWIRE_ESD	50
I406	TRUE	ONEWIRE_OV	50
I405	TRUE	ONEWIRE_PWR_EN_L	50
I407	TRUE	ONEWIRE_PWR_EN_L_DIV	50
I409	TRUE	P1V25S0NBDPLL_FB	22
I408	TRUE	P1V25S0NBDPLL_RF	22
I411	TRUE	P1V25S0_ITH	57
I410	TRUE	P1V25S0_ITH_RC	57
I412	TRUE	P1V25S0_MODE	57
I413	TRUE	P1V25S0_RT	57

I478	TRUE	P1V8S0_EN	51
I480	TRUE	P3V3S0_EN	51
I479	TRUE	P3V3S3_EN_L	58
I481	TRUE	P3V3TVDAC_EN_RC	22
I482	TRUE	P3V3TVDAC_NOISE	22
I483	TRUE	P3V42G3H5_BOOST	57
I485	TRUE	P3V42G3H_SHDN_L	57
I484	TRUE	P3V42G3H_SHDN_L1	57
I486	TRUE	P5VS0_EN	51
I487	TRUE	P5VS3_EN_L	58
I488	TRUE	PBUS_ISENSE_IN_NEG	59
I490	TRUE	PBUS_ISENSE_VREG	59
I489	TRUE	PBUS_S0_SMC_VSENSE	45
I517	TRUE	PBUS_SMC_VSENSE_EN_L	59 42 45
I519	TRUE	PCIE_CLK100M_MINI_N	
I518	TRUE	PCIE_CLK100M_MINI_N_F	7 36
I520	TRUE	PCIE_CLK100M_MINI_P	
I521	TRUE	PCIE_CLK100M_MINI_P_F	7 36
I522	TRUE	PCIE_E_D2R_N	24 36 70
I523	TRUE	PCIE_E_D2R_N_F	7 36
I524	TRUE	PCIE_E_D2R_P	24 36 70
I525	TRUE	PCIE_E_D2R_P_F	7 36
I527	TRUE	PCIE_E_R2D_C_N	24 36 70
I526	TRUE	PCIE_E_R2D_C_N_F	7 36
I528	TRUE	PCIE_E_R2D_C_P	24 36 70
I529	TRUE	PCIE_E_R2D_C_P_F	7 36
I551	TRUE	PCIE_E_R2D_N	36
I553	TRUE	PCIE_E_R2D_P	36
I552	TRUE	PCIE_WAKE_L	7 25 36
I554	TRUE	PCI_CLK33M_LPCPLUS	30 43 71
I555	TRUE	PCI_CLK33M_SB	24 30 71
I556	TRUE	PCI_CLK33M_SMC	30 41 71
I557	TRUE	PCI_DEVSEL_L	24 70
I558	TRUE	PCI_FRAME_L	24 70
I559	TRUE	PCI_FW_GNT_L	24 70
I561	TRUE	PCI_FW_REQ_L	24 70
I560	TRUE	PCI_IRDY_L	24 70
I562	TRUE	PCI_LOCK_L	24 70
I563	TRUE	PCI_PERR_L	24 70
I564	TRUE	PCI_PME_FW_L	25
I565	TRUE	PCI_REQ1_L	24 70
I566	TRUE	PCI_REQ2_L	24 70
I568	TRUE	PCI_SERR_L	24 70
I567	TRUE	PCI_STOP_L	24 70
I569	TRUE	PCI_TRDY_L	24 70
I571	TRUE	PEG_COMP	15
I570	TRUE	PEG_D2R_N<1>	15 61 67
I577	TRUE	PEG_D2R_P<1>	15 61 67
I578	TRUE	PEG_R2D_C_N<3..0>	15 61 67
I579	TRUE	PEG_R2D_C_P<3..0>	15 61 67
I580	TRUE	PGOOD_1V25S0	51 57
I581	TRUE	PGOOD_1V8S3	51 55
I601	TRUE	PLT_RST_BUF_L	28
I603	TRUE	PLT_RST_L	6 7 24 28 60 64
I602	TRUE	PM_BATLOW_L	25 41
I604	TRUE	PM_BMBUSY_L	16 25
I606	TRUE	PM_CLKRUN_L	25 41 43
I605	TRUE	PM_DPRSLPVR	16 25 52 66
I608	TRUE	PM_EXTTS_L<0>	16 41
I607	TRUE	PM_EXTTS_L<1>	16 41
I609	TRUE	PM_LAN_ENABLE	25 41
I611	TRUE	PM_LAN_PWRGD	41 42
I610	TRUE	PM_LATRIGGER_L	7 13 24
I612	TRUE	PM_PWRBTN_L	6 25 41
I613	TRUE	PM_RI_L	25
I614	TRUE	PM_RSMRST_L	6 25 41
I616	TRUE	PM_S4_STATE_L	6 25 36 41 58
I615	TRUE	PM_SB_PWROK	9 25 28
I618	TRUE	PM_SLP_S3_L	51 55 6 7 25 36 37 41 42
I617	TRUE	PM_SLP_S4_LS5V	39 58
I619	TRUE	PM_SLP_S5_L	6 25 41 42
I836	TRUE	PM_STPCPU_L	25 29 30
I835	TRUE	PM_STPPCI_L	25 29 30
I837	TRUE	PM_SUS_STAT_L	25 41 43
I839	TRUE	PM_SYSRST_L	6 25 28 41
I838	TRUE	PM_THRMTRIP_L	10 16 23 42 66
I849	TRUE	PM_THRM_L	25
I850	TRUE	PM_WLAN_EN_L	36
I851	TRUE	PM_WLAN_EN_L1	36
I853	TRUE	PM_WLAN_EN_L2	36
I852	TRUE	PM_WLAN_EN_L_SS	36
I855	TRUE	PP0V9_S0	6 7 8 33 55 72
I854	TRUE	PP0V9_S3	6 8 31 32 55 72
I856	TRUE	PP18V5_DCIN	6 7 50 72

I493	TRUE	PP18V5_DCIN_ONEWIRE	50 72
I492	TRUE	PP18V5_G3H	7 8 50 59 72
I494	TRUE	PP18V5_S5_CHGR_SW_R	59 72
I495	TRUE	PP1V05_S0	27 30 42 54 72 6 7 8 10 11 12 13 14 18 19 21 23 26
I496	TRUE	PP1V05_S0_NB_VCCPEG	15 19 21 72
I498	TRUE	PP1V25_S0	6 7 8 16 18 19 21 26 27 51 57 72
I497	TRUE	PP1V25_S0M_NB_VCCA_HPLL	19 21 72
I499	TRUE	PP1V25_S0_NB_DPLL	22 72
I500	TRUE	PP1V25_S0_NB_PEGPLL	19 21 72
I501	TRUE	PP1V25_S0_NB_PEGPLL_RC	21 72
I503	TRUE	PP1V25_S0_NB_VCCA_DPLLA	19 22 72
I502	TRUE	PP1V25_S0_NB_VCCA_DPLLB	19 22 72
I508	TRUE	PP1V5_S0	6 7 8 11 12 22 26 27 54 72
I506	TRUE	PP1V5_S0_NB_QDAC	22 72
I507	TRUE	PP1V5_S0_NB_VCCD_CRT	19 22 72
I505	TRUE	PP1V5_S0_NB_VCCD_QDAC	19 22 72
I504	TRUE	PP1V5_S0_SB_VCC1_5_B	23 24 26 27 72
I514	TRUE	PP1V5_S0_SB_VCCDMIPLL	26 27 72
I512	TRUE	PP1V5_S0_SB_VCCDMIPLL_F	27 72
I513	TRUE	PP1V5_S0_SB_VCCSATAPLL	26 27 72
I511	TRUE	PP1V8_S0	6 7 8 19 22 51 61 72
I510	TRUE	PP1V8_S0_ANALOG_SDVO_F	61 72
I509	TRUE	PP1V8_S0_ANALOG_TMDS_F	61 72
I515	TRUE	PP1V8_S0_NB_VCCTXLVDS	19 22 72
I516	TRUE	PP1V8_S0_PVCC1_TMDS_F	61 72
I534	TRUE	PP1V8_S0_PVCC2_TMDS_F	61 72
I532	TRUE	PP1V8_S0_TMDS_F	61 72
I533	TRUE	PP1V8_S3	72 6 7 8 16 18 21 31 32 34 35 51 55 68
I531	TRUE	PP1V8_S3M_NB_VCCSMCK	19 21 72
I530	TRUE	PP1V8_S3_NB_VCCSMCK_RC	21 72
I540	TRUE	PP3V3_A_S0	28 29 30 42 44 46 6 7 8 13 16 19 21 22 23 24 25 26 27
I538	TRUE	PP3V3_B_S0	51 52 53 60 63 64 6 8 38 47 51 61 62 63
I539	TRUE	PP3V3_LCDVDD_SW	60 72
I537	TRUE	PP3V3_LCDVDD_SW_F	7 60 72
I536	TRUE	PP3V3_S0_ANALOG_SDVO_F	61 72
I535	TRUE	PP3V3_S0_CK505_VDD48	72
I544	TRUE	PP3V3_S0_CK505_VDDA	72
I545	TRUE	PP3V3_S0_CK505_VDDA_R	72
I541	TRUE	PP3V3_S0_CK505_VDD_CPU_SRC	29 72
I543	TRUE	PP3V3_S0_CK505_VDD_PCI	72
I542	TRUE	PP3V3_S0_CK505_VDD_REF	72
I549	TRUE	PP3V3_S0_HDCP_F	62
I550	TRUE	PP3V3_S0_IMVP6_3V3	52 72
I546	TRUE	PP3V3_S0_LCD_F	7 60 72
I548	TRUE	PP3V3_S0_NBCORE_FOLLOW_R	21 72
I547	TRUE	PP3V3_S0_NB_CRTDAC_F	22 72
I574	TRUE	PP3V3_S0_NB_TVDAC	22 72
I575	TRUE	PP3V3_S0_NB_TVDAC_F	22 72
I576	TRUE	PP3V3_S0_NB_TVDAC_FOLLOW	22 72
I573	TRUE	PP3V3_S0_NB_VCCA_CRTDAC	19 22 72
I572	TRUE	PP3V3_S0_NB_VCCA_DAC_BG	19 22 72
I582	TRUE	PP3V3_S0_NB_VCCA_TVDACA	19 22 72
I583	TRUE	PP3V3_S0_NB_VCCA_TVDACB	19 22 72
I584	TRUE	PP3V3_S0_NB_VCCA_TVDACC	19 22 72
I589	TRUE	PP3V3_S0_SPVCC_TMDS_F	61 72
I586	TRUE	PP3V3_S3	6 7 8 36 42 44 48 51 58 60 72
I585	TRUE	PP3V3_S3_ALS_F	
I588	TRUE	PP3V3_S3_AP_AUX	7 36 72
I587	TRUE	PP3V3_S5_AVREF_SMC	41 42 72
I594	TRUE	PP3V3_S5_SMC_AVCC	41 72
I591	TRUE	PP3V42G3H_SW	57 72
I590	TRUE	PP3V42_G3H	57 59 72 6 7 8 23 26 27 28 39 40 41 42 43 44
I593	TRUE	PP3V42_G3H_IPD_F	7 40
I592	TRUE	PP3V42_G3H_SMCUSBMUX_R	39 72
I599	TRUE	PP5V_S0	6 7 8 22 27 40 43 47 51 52 53 63 72
I597	TRUE	PP5V_S0_DVIPORT	7 37 63 72
I596	TRUE	PP5V_S0_DVIPORT_D	63 72
I595	TRUE	PP5V_S0_IMVP6_VDD	52 72
I598	TRUE	PP5V_S0_KBDLED_F	7 40 72
I600	TRUE	PP5V_S0_SB_V5REF	26 27 72
I834	TRUE	PP5V_S0_TMDS_FUSE	63 72
I832	TRUE	PP5V_S3	6 7 8 40 58 60 72
I833	TRUE	PP5V_S3_CAMERA_F	7 60 72
I830	TRUE	PP5V_S3_TOPCASE_F	7 40
I831	TRUE	PP5V_S3_USB2_EXTA	39 72
I844	TRUE	PP5V_S3_USB2_EXTA_F	7 37 39 72
I842	TRUE	PP5V_S5	6 7 8 27 39 51 54 55 56 58 72
I843	TRUE	PP5V_S5_SB_V5REF_SUS	26 27 72
I840	TRUE	PPBUS_G3H	7 8 37 45 50 56 59 64 72
I841	TRUE	PPBUS_R_G3H	7 8 42 52 53 54 55 59 72
I847	TRUE	PPDCIN_G3H	7 8 50 57 72
I848	TRUE	PPDCIN_G3H_R	50 72
I846	TRUE	PPVBATT_G3H_R	50 72

I639	TRUE	PPVBAT_G3H_CHGR_OUT	59 72
I641	TRUE	PPVBAT_G3H_CHGR_REG	6 59 72
I640	TRUE	PPVBAT_G3H_CHRGR_REG_0	59 72
I642	TRUE	PPVBAT_G3H_CHRGR_REG_R	59 72
I644	TRUE	PPVCORE_S0_CPU	72 6 7 8 11 12 52 65
I643	TRUE	PPVCORE_S0_NB_GFX	
I646	TRUE	PPVDCIN_G3H_PRE	45 59 72
I645	TRUE	PPVDCIN_G3H_PRE2	59 72
I647	TRUE	PPVDCIN_G3H_PRE_0	59 72
I649	TRUE	PPVDCIN_G3H_PRE_R	59 72
I648	TRUE	PPVIN_S5_IMVP6_VIN	52 72
I650	TRUE	PPVOUT_S0_LCDBKLT	7 60 64 72
I651	TRUE	PPVOUT_S0_LCDBKLT_SW	64 72
I652	TRUE	RSMRST_PWRGD	41 42 56
I654	TRUE	RSVD_EXTGPU_LVDS_EN	25
I653	TRUE	RUNSS_GATE_D	51
I656	TRUE	RUNSS_GATE_D_L	51
I655	TRUE	S0PWRGD_1V8_DIV	51
I657	TRUE	S0PWRGD_3V3_DIV	51
I665	TRUE	S0PWRGD_5V_DIV	51
I664	TRUE	S0SEQ_BEGIN	51
I667	TRUE	SATA_B_DET_L	25
I666	TRUE	SB_A20GATE	23
I668	TRUE	SB_CLINK_VREF0	25 70
I669	TRUE	SB_CLINK_VREF1	25 70
I677	TRUE	SB_CLK100M_DMI_N	24 29 30 71
I676	TRUE	SB_CLK100M_DMI_P	24 29 30 71
I679	TRUE	SB_CLK14P3M_TIMER	25 30 71
I678	TRUE	SB_CLK48M_USBCTLR	25 30 71
I680	TRUE	SB_CRT_TVOUT_MUX_L	25 63
I681	TRUE	SB_GPIO10_CL1	23 25
I687	TRUE	SB_GPIO18	25
I686	TRUE	SB_GPIO30	7 13 24
I685	TRUE	SB_GPIO36	25
I689	TRUE	SB_GPIO40	7 13 24

I620	TRUE	SB_INTVRMEN	23
I621	TRUE	SB_LAN100_SLP	23
I622	TRUE	SB_RCIN_L	23
I627	TRUE	SB_RTC_RST_L	23 28
I624	TRUE	SB_RTC_X1	23 28
I623	TRUE	SB_RTC_X1_R	28
I626	TRUE	SB_RTC_X2	23 28
I625	TRUE	SB_SLOAD	25
I632	TRUE	SB_SM_INTRUDER_L	23 28
I629	TRUE	SB_SPKR	25
I628	TRUE	SDVO_CTRLCLK	16 61
I631	TRUE	SDVO_CTRLDATA	16 61
I630	TRUE	SMBUS_SB_ME_SCL	25 44 69
I637	TRUE	SMBUS_SB_ME_SDA	25 44 69
I635	TRUE	SMBUS_SB_SCL	25 29 44 69
I634	TRUE	SMBUS_SB_SDA	
I633	TRUE	SMBUS_SMC_0_S0_SCL	71 7 41 44 46
I636	TRUE	SMBUS_SMC_0_S0_SDA	7 41 44 46 71
I638	TRUE	SMBUS_SMC_A_S3_SCL	44 71 40 41
I658	TRUE	SMBUS_SMC_A_S3_SDA	7 36 59 71
I659	TRUE	SMBUS_SMC_BSA_SCL	7 41 44 50
I660	TRUE	SMBUS_SMC_BSA_SDA	
I661	TRUE	SMBUS_SMC_B_S3_SCL	7 41 44 60
I662	TRUE	SMBUS_SMC_B_S3_SDA	7 41 44 60
I663	TRUE	SMBUS_SMC_MGMT_SCL	41 44 48 71
I670	TRUE	SMBUS_SMC_MGMT_SDA	41 44 48 71
I671	TRUE	SMB_AIRPORT_CONN_CLK	7 36
I672	TRUE	SMB_AIRPORT_CONN_DATA	7 36
I673	TRUE	SMC_ACIN_VSENSE	41 45
I674	TRUE	SMC_ADAPTER_EN	9 36 41 42
I675	TRUE	SMC_BATTPACK_STAT	41 42
I684	TRUE	SMC_BATT_CHG_EN	6 41 42
I683	TRUE	SMC_BATT_ISENSE	41 59
I682	TRUE	SMC_BC_ACOK	41 42 50 59
I688	TRUE	SMC_BC_ACOK_ONEWIRE_R	50

I726	TRUE	SMC_BS_ALRT_L	7 41 42 50
I725	TRUE	SMC_CASE_OPEN	41 42
I728	TRUE	SMC_DCIN_ISENSE	41 59
I727	TRUE	SMC_EXTAL	41 42
I729	TRUE	SMC_FAN_0_CTL	41 47
I731	TRUE	SMC_FAN_0_TACH	41 47
I730	TRUE	SMC_GPU_ISENSE	41 53
I732	TRUE	SMC_GPU_VSENSE	41 45
I734	TRUE	SMC_KBC_MDE	41
I733	TRUE	SMC_LID	7 40 41 42
I736	TRUE	SMC_LRESET_L	28 41
I735	TRUE	SMC_MANUAL_RST_L	6 42
I737	TRUE	SMC_MANUAL_RST_L1	42
I739	TRUE	SMC_MD1	41 43
I738	TRUE	SMC_NMI	41 43
I741	TRUE	SMC_ODD_DETECT	41 42
I740	TRUE	SMC_ONOFF_H	40 42 57
I742	TRUE	SMC_ONOFF_L	6 7 40 41 42
I744	TRUE	SMC_PBUS_ISENSE	41 59
I743	TRUE	SMC_PBUS_VSENSE	41 45
I746	TRUE	SMC_PF3	41 42
I745	TRUE	SMC_PM_G2_EN	6 41 56 58
I747	TRUE	SMC_PROCHOT	41 42
I749	TRUE	SMC_PROCHOT_3_3_L	41 42
I748	TRUE	SMC_RESET_L	6 41 42 43
I750	TRUE	SMC_RUNTIME_SCI_L	25 41
I751	TRUE	SMC_RX_L	39 41 42 43
I752	TRUE	SMC_SMS_INT	9 41 48
I754	TRUE	SMC_SUS_CLK	41 42
I753	TRUE	SMC_SYS_KBDLED	7 40 41
I755	TRUE	SMC_SYS_LED	7 40 41
I756	TRUE	SMC_TCK	6 41 42 43
I757	TRUE	SMC_TDI	6 41 42 43
I759	TRUE	SMC_TDO	6 41 42 43
I758	TRUE	SMC_THRMTRIP	41 42

I691	TRUE	SMC_TMS	42 6 41 43
I690	TRUE	SMC_TRST_L	
I692	TRUE	SMC_TX_L	42 39 41
I693	TRUE	SMC_VCL	43
I694	TRUE	SMC_WAKE_SCI_L	41 25 7
I695	TRUE	SMC_XTAL	13 41 42
I696	TRUE	SMS_MOT_EN	48
I697	TRUE	SMS_ONOFF_L	41 48
I698	TRUE	SMS_X_AXIS	41 48
I700	TRUE	SMS_Y_AXIS	41 48
I701	TRUE	SMS_Z_AXIS	41 48
I699	TRUE	SPI_A_INT_CLK	49
I702	TRUE	SPI_A_INT_HOLD_L	49
I703	TRUE	SPI_A_INT_SI	49
I704	TRUE	SPI_A_INT_WP_L	69 49
I705	TRUE	SPI_A_SCLK_R	43 6
I706	TRUE	SPI_A_SI_R	69 43 49
I707	TRUE	SPI_A_SO_R	
I711	TRUE	SPI_CE_L<0>	69 43 49
I710	TRUE	SPI_CE_R_L<0>	24 49 69
I709	TRUE	SPI_CE_R_L<1>	
I708	TRUE	SPI_EXT_A_SCLK_R	43
I712	TRUE	SPI_EXT_A_SI_R	43
I713	TRUE	SPI_EXT_CE_L<0>	43
I714	TRUE	SPI_INT_CE_L<0>	43 49
I715	TRUE	SPI_SCLK_R	24 49 69
I716	TRUE	SPI_SI_R	
I717	TRUE	SPI_SO	49 24 43 69
I718	TRUE	SST8051_DDC_CLK	
I719	TRUE	SST8051_DDC_DATA	62
I720	TRUE	SST8051_DDC_EN	62
I722	TRUE	SST8051_DVI_HOTPLUG_DET	62
I721	TRUE	SST8051_EA_L	62
I724	TRUE	SST8051_P25_AUDIO_CONFIG	62
I723	TRUE	SST8051_P34_AUDIO_CONFIG	62

I796	TRUE	SST8051_RST	62
I795	TRUE	SST8051_SW_RESET_L	25 62
I798	TRUE	SST8051_UPDATE_L	25 62
I797	TRUE	SST8051_XTAL1	62
I799	TRUE	SST8051_XTAL2	62
I801	TRUE	SUS_CLK_SB	25 42
I800	TRUE	SYS_ONEWIRE	7 41 42 50
I802	TRUE	SYS_ONEWIRE_BILAT	50
I804	TRUE	THRM_CPU_ALERT_L	46
I803	TRUE	THRM_CPU_DXN	46
I806	TRUE	THRM_CPU_DXP	46
I805	TRUE	THRM_CPU_THM_L	46
I807	TRUE	TMDS_DDC_SCL	7 37 61 62 63 67
I809	TRUE	TMDS_DDC_SDA	7 37 61 62 63 67
I808	TRUE	TMDS_EXT_RES	61
I811	TRUE	TMDS_EXT_SWING	61
I810	TRUE	TMDS_HTPLG	7 37 61 63
I812	TRUE	TMDS_HTPLG_R	61
I814	TRUE	TMDS_HW_RESET_L	28 61 62
I813	TRUE	TMDS_INT_N	61 67
I816	TRUE	TMDS_INT_P	61 67
I815	TRUE	TMDS_LINT_L	61 62
I817	TRUE	TMDS_LSCL	61 62
I819	TRUE	TMDS_LSDA	61 62
I818	TRUE	TMDS_SDB_N	61 67
I820	TRUE	TMDS_SDB_P	61 67
I821	TRUE	TMDS_SDC_N	61 67
I822	TRUE	TMDS_SDC_P	61 67
I824	TRUE	TMDS_SDG_N	61 67
I823	TRUE	TMDS_SDG_P	61 67
I825	TRUE	TMDS_SDR_N	61 67
I826	TRUE	TMDS_SDR_P	61 67
I827	TRUE	TMDS_SW_RESET_L	25 61
I829	TRUE	TMDS_TX<2..0>	61
I828	TRUE	TMDS_TX_CLK	61

I761	TRUE	TMDS_TX_CLK_N	
I760	TRUE	TMDS_TX_CLK_P	
I762	TRUE	TMDS_TX_CONN_CLK_N	
I763	TRUE	TMDS_TX_CONN_CLK_P	
I764	TRUE	TMDS_TX_CONN_N<2..0>	63 7 37
I765	TRUE	TMDS_TX_CONN_P<2..0>	63 7 37
I766	TRUE	TMDS_TX_N<2..0>	
I767	TRUE	TMDS_TX_P<2..0>	
I768	TRUE	TV_A_DAC	
I770	TRUE	TV_B_DAC	
I771	TRUE	TV_C_DAC	
I769	TRUE	TV_DCONSEL<1>	
I772	TRUE	USB2_AIRPORT_N	
I773	TRUE	USB2_AIRPORT_N_F	
I774	TRUE	USB2_AIRPORT_P	
I775	TRUE	USB2_AIRPORT_P_F	
I776	TRUE	USB2_CAMERA_F_N	
I777	TRUE	USB2_CAMERA_F_P	
I781	TRUE	USB2_CAMERA_N	
I780	TRUE	USB2_CAMERA_P	
I779	TRUE	USB2_EXTA_F_N	
I778	TRUE	USB2_EXTA_F_P	
I782	TRUE	USB2_EXTA_N	
I783	TRUE	USB2_EXTA_P	
I784	TRUE	USB2_MUXED_EXTA_N	
I785	TRUE	USB2_MUXED_EXTA_P	
I786	TRUE	USB2_WSPRING_N	7 9 24 40 69
I787	TRUE	USB2_WSPRING_P	7 9 24 40 69
I788	TRUE	USB_DEBUGPRT_EN_L	39 41
I789	TRUE	USB_EXTC_OC_L	24
I790	TRUE	USB_EXTD_OC_L	7 13 24
I792	TRUE	USB_IR_N	7 9 24 40 69
I791	TRUE	USB_IR_P	7 9 24 40 69
I794	TRUE	USB_RBIAS	24 69
I793	TRUE	VCCCL1_5V	26

I857	TRUE	VGA_B	67 63 7 37
I858	TRUE	VGA_G	
I860	TRUE	VGA_HSYNC	67 63 37 7
I859	TRUE	VGA_R	
I864	TRUE	VGA_VSYNC	63 7 37
I863	TRUE	VR_PWRGD_CK505	
I861	TRUE	VR_PWRGD_CK505_L	28 52
I862	TRUE	VR_PWRGOOD_DELAY	28 52 9 16
I866	TRUE	WOL_EN	25
I865	TRUE	WOW_EN	24 7 13
I867	TRUE	XDP_BPM_L<0>	36 66 13 7
I868	TRUE	XDP_BPM_L<1>	10
I869	TRUE	XDP_BPM_L<2>	66 13 10
I870	TRUE	XDP_BPM_L<3>	7
I871	TRUE	XDP_BPM_L<4>	13 6 7 10
I872	TRUE	XDP_BPM_L<5>	66
I874	TRUE	XDP_CLK_N	29 7 13
I873	TRUE	XDP_CLK_P	30 71
I875	TRUE	XDP_CPURST_L	66 6 7 13
I876	TRUE	XDP_DBRESET_L	6 7 10 13 28
I877	TRUE	XDP_OBS20	7 13
I878	TRUE	XDP_PWRGD	6 7 13
I879	TRUE	XDP_TCK	6 7 10 13 66
I880	TRUE	XDP_TDI	6 7 10 13 66
I882	TRUE	XDP_TDO	6 7 10 13 66
I881	TRUE	XDP_TMS	6 7 10 13 66
I883	TRUE	XDP_TRST_L	6 7 10 13 66

ICT Test Points

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE NONE	SHT 6	OF 73

Functional Test Points

Functional Test and No-Tests

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SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 7	OF 73

"S0,S0M" RAILS

(REGULATOR OUTPUT CPU VCORE PWR)

PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE

(CPU VCOR PWRE)

PPVCORE_S0_CPU

PP0V9_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

(DDR2 TERMINATION 0.9V PWR)

PP0V9_S0

(REGULATOR OUTPUT CPU 0.90V PWR)

PP0V9_S3
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

(NB MEM VREF 0.9V PWR)

PP0V9_S3

R0800
0
5%
1/20W
MF
201

PP0V9_S3_MEM_NBVREFA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V

R0801
0
5%
1/20W
MF
201

PP0V9_S3_MEM_NBVREFB
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V

PP1V05_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V25_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE

PP1V5_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP1V8_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

PPVCORE_S0_NB_GFX
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.45V
MAKE_BASE=TRUE

PP5V_S0
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP3V3_A_S0
MIN_LINE_WIDTH=0.38MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

3V3_S0 split into 2
for layout optimization
of plane splits

PP3V3_B_S0
MIN_LINE_WIDTH=0.38MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

3V3_B_S0 plane on right side
(peninsula)

"S3" RAILS

PP1V8_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP3V3_S3
MIN_LINE_WIDTH=0.2mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP5V_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

"S5" RAILS

PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

"G3H" RAILS

PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE

PP18V5_G3H
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPDCIN_G3H
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPBUS_R_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

Power Aliases

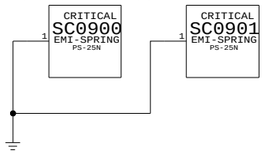
SYNC_MASTER=WFERRY SYNC_DATE=06/15/2006

APPLE INC.

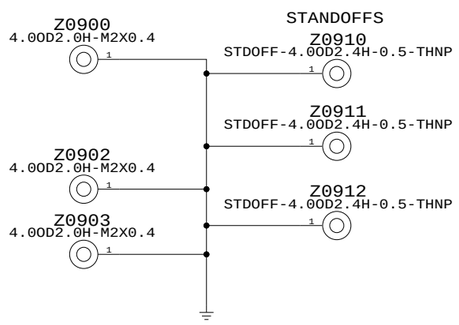
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 8 OF 73	

EMI SPRING CLIPS

PLACE CLIPS PER MCO ON TOPSIDE NEAR BATTERY CONNECTOR J6900



BOSSES TO CONNECT TO HEATSINK



SMC ALIASES

NO-CONNECT UNUSED SMC INTERFACE PORTS

			NO_TEST	
NC_SMC_PA0	NC_SMC_PA0	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_PA1	NC_SMC_PA1	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_PB0	NC_SMC_PB0	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_PG0	NC_SMC_PG0	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P14	NC_SMC_P14	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P20	NC_SMC_P20	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P21	NC_SMC_P21	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P22	NC_SMC_P22	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P23	NC_SMC_P23	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P26	NC_SMC_P26	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P27	NC_SMC_P27	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P41	NC_SMC_P41	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P43	NC_SMC_P43	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P44	NC_SMC_P44	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P46	NC_SMC_P46	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P62	NC_SMC_P62	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P63	NC_SMC_P63	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P64	NC_SMC_P64	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P67	NC_SMC_P67	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_P81	NC_SMC_P81	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_GFX_OVERTEMP_L	NC_SMC_GFX_OVERTEMP_L	TRUE	MAKE_BASE=TRUE	9 41
NC_EXCARD_OC_L	NC_EXCARD_OC_L	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_EXCARD_CP	NC_SMC_EXCARD_CP	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_ENRGYSTR_LDO_EN	NC_SMC_ENRGYSTR_LDO_EN	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_ENRGYSTR_LDO_PGOOD	NC_SMC_ENRGYSTR_LDO_PGOOD	TRUE	MAKE_BASE=TRUE	9 41
NC_ALS_RIGHT	NC_ALS_RIGHT	TRUE	MAKE_BASE=TRUE	9 41
NC_ALS_GAIN	NC_ALS_GAIN	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_EXCARD_PWR_EN	NC_SMC_EXCARD_PWR_EN	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_PF0	NC_SMC_PF0	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_BATT_VSET	NC_SMC_BATT_VSET	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_SYS_VSET	NC_SMC_SYS_VSET	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_RSTGATE_L	NC_SMC_RSTGATE_L	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	TRUE	MAKE_BASE=TRUE	9 41
NC_SYS_ISET	NC_SYS_ISET	TRUE	MAKE_BASE=TRUE	9 41
NC_BATT_ISET	NC_BATT_ISET	TRUE	MAKE_BASE=TRUE	9 41
NC_ISENSE_CAL_EN	NC_ISENSE_CAL_EN	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_FWE	NC_SMC_FWE	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_ANALOG_ID	NC_SMC_ANALOG_ID	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_TEST_DAC1	NC_SMC_TEST_DAC1	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_TEST_DAC2	NC_SMC_TEST_DAC2	TRUE	MAKE_BASE=TRUE	9 41
NC_SMC_TEST_DAC3	NC_SMC_TEST_DAC3	TRUE	MAKE_BASE=TRUE	9 41

48 41 9 6 SMC_SMS_INT — SMC_SMS_INT — 6 9 41 48 (MAKE_BASE=TRUE)

42 41 36 9 6 SMC_ADAPTER_EN — SMC_ADAPTER_EN — 6 9 36 41 42 (MAKE_BASE=TRUE)

LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

			NO_TEST	
NC_LVDS_B_CLK_N	NC_LVDS_B_CLK_N	TRUE	MAKE_BASE=TRUE	9 15 67
NC_LVDS_B_CLK_P	NC_LVDS_B_CLK_P	TRUE	MAKE_BASE=TRUE	9 15 67
NC_LVDS_B_DATA_N0	NC_LVDS_B_DATA_N0	TRUE	MAKE_BASE=TRUE	9 15
NC_LVDS_B_DATA_N1	NC_LVDS_B_DATA_N1	TRUE	MAKE_BASE=TRUE	9 15
NC_LVDS_B_DATA_N2	NC_LVDS_B_DATA_N2	TRUE	MAKE_BASE=TRUE	9 15
NC_LVDS_B_DATA_N3	NC_LVDS_B_DATA_N3	TRUE	MAKE_BASE=TRUE	9 67
NC_LVDS_B_DATA_P0	NC_LVDS_B_DATA_P0	TRUE	MAKE_BASE=TRUE	9 15
NC_LVDS_B_DATA_P1	NC_LVDS_B_DATA_P1	TRUE	MAKE_BASE=TRUE	9 15
NC_LVDS_B_DATA_P2	NC_LVDS_B_DATA_P2	TRUE	MAKE_BASE=TRUE	9 15
NC_LVDS_B_DATA_P3	NC_LVDS_B_DATA_P3	TRUE	MAKE_BASE=TRUE	9 67
NC_LVDS_A_DATA_P3	NC_LVDS_A_DATA_P3	TRUE	MAKE_BASE=TRUE	9 67
NC_LVDS_A_DATA_N3	NC_LVDS_A_DATA_N3	TRUE	MAKE_BASE=TRUE	9 67

PCI_EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

NC_PEG_D2R_N0	NC_PEG_D2R_N0	TRUE	9 15
NC_PEG_D2R_N2	NC_PEG_D2R_N2	TRUE	9 15
NC_PEG_D2R_N3	NC_PEG_D2R_N3	TRUE	9 15
NC_PEG_D2R_N4	NC_PEG_D2R_N4	TRUE	9 15
NC_PEG_D2R_N5	NC_PEG_D2R_N5	TRUE	9 15
NC_PEG_D2R_N6	NC_PEG_D2R_N6	TRUE	9 15
NC_PEG_D2R_N7	NC_PEG_D2R_N7	TRUE	9 15
NC_PEG_D2R_N8	NC_PEG_D2R_N8	TRUE	9 15
NC_PEG_D2R_N9	NC_PEG_D2R_N9	TRUE	9 15
NC_PEG_D2R_N10	NC_PEG_D2R_N10	TRUE	9 15
NC_PEG_D2R_N11	NC_PEG_D2R_N11	TRUE	9 15
NC_PEG_D2R_N12	NC_PEG_D2R_N12	TRUE	9 15
NC_PEG_D2R_N13	NC_PEG_D2R_N13	TRUE	9 15
NC_PEG_D2R_N14	NC_PEG_D2R_N14	TRUE	9 15
NC_PEG_D2R_N15	NC_PEG_D2R_N15	TRUE	9 15
NC_PEG_D2R_P0	NC_PEG_D2R_P0	TRUE	9 15
NC_PEG_D2R_P2	NC_PEG_D2R_P2	TRUE	9 15
NC_PEG_D2R_P3	NC_PEG_D2R_P3	TRUE	9 15
NC_PEG_D2R_P4	NC_PEG_D2R_P4	TRUE	9 15
NC_PEG_D2R_P5	NC_PEG_D2R_P5	TRUE	9 15
NC_PEG_D2R_P6	NC_PEG_D2R_P6	TRUE	9 15
NC_PEG_D2R_P7	NC_PEG_D2R_P7	TRUE	9 15
NC_PEG_D2R_P8	NC_PEG_D2R_P8	TRUE	9 15
NC_PEG_D2R_P9	NC_PEG_D2R_P9	TRUE	9 15
NC_PEG_D2R_P10	NC_PEG_D2R_P10	TRUE	9 15
NC_PEG_D2R_P11	NC_PEG_D2R_P11	TRUE	9 15
NC_PEG_D2R_P12	NC_PEG_D2R_P12	TRUE	9 15
NC_PEG_D2R_P13	NC_PEG_D2R_P13	TRUE	9 15
NC_PEG_D2R_P14	NC_PEG_D2R_P14	TRUE	9 15
NC_PEG_D2R_P15	NC_PEG_D2R_P15	TRUE	9 15
NC_PEG_R2D_C_N4	NC_PEG_R2D_C_N4	TRUE	9 15
NC_PEG_R2D_C_N5	NC_PEG_R2D_C_N5	TRUE	9 15
NC_PEG_R2D_C_N6	NC_PEG_R2D_C_N6	TRUE	9 15
NC_PEG_R2D_C_N7	NC_PEG_R2D_C_N7	TRUE	9 15
NC_PEG_R2D_C_N8	NC_PEG_R2D_C_N8	TRUE	9 15
NC_PEG_R2D_C_N9	NC_PEG_R2D_C_N9	TRUE	9 15
NC_PEG_R2D_C_N10	NC_PEG_R2D_C_N10	TRUE	9 15
NC_PEG_R2D_C_N11	NC_PEG_R2D_C_N11	TRUE	9 15
NC_PEG_R2D_C_N12	NC_PEG_R2D_C_N12	TRUE	9 15
NC_PEG_R2D_C_N13	NC_PEG_R2D_C_N13	TRUE	9 15
NC_PEG_R2D_C_N14	NC_PEG_R2D_C_N14	TRUE	9 15
NC_PEG_R2D_C_N15	NC_PEG_R2D_C_N15	TRUE	9 15
NC_PEG_R2D_C_P4	NC_PEG_R2D_C_P4	TRUE	9 15
NC_PEG_R2D_C_P5	NC_PEG_R2D_C_P5	TRUE	9 15
NC_PEG_R2D_C_P6	NC_PEG_R2D_C_P6	TRUE	9 15
NC_PEG_R2D_C_P7	NC_PEG_R2D_C_P7	TRUE	9 15
NC_PEG_R2D_C_P8	NC_PEG_R2D_C_P8	TRUE	9 15
NC_PEG_R2D_C_P9	NC_PEG_R2D_C_P9	TRUE	9 15
NC_PEG_R2D_C_P10	NC_PEG_R2D_C_P10	TRUE	9 15
NC_PEG_R2D_C_P11	NC_PEG_R2D_C_P11	TRUE	9 15
NC_PEG_R2D_C_P12	NC_PEG_R2D_C_P12	TRUE	9 15
NC_PEG_R2D_C_P13	NC_PEG_R2D_C_P13	TRUE	9 15
NC_PEG_R2D_C_P14	NC_PEG_R2D_C_P14	TRUE	9 15
NC_PEG_R2D_C_P15	NC_PEG_R2D_C_P15	TRUE	9 15

GND — VOLTAGE=0V, MIN_NECK_WIDTH=0.20 MM, MIN_LINE_WIDTH=0.38 MM

SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

NC_SATA_A_D2R_N	NC_SATA_A_D2R_N	TRUE	9 69
NC_SATA_A_D2R_P	NC_SATA_A_D2R_P	TRUE	9 69
NC_SATA_A_R2D_C_N	NC_SATA_A_R2D_C_N	TRUE	9 23 69
NC_SATA_A_R2D_C_P	NC_SATA_A_R2D_C_P	TRUE	9 23 69
NC_SATA_B_D2R_N	NC_SATA_B_D2R_N	TRUE	9 69
NC_SATA_B_D2R_P	NC_SATA_B_D2R_P	TRUE	9 69
NC_SATA_B_R2D_C_N	NC_SATA_B_R2D_C_N	TRUE	9 23 69
NC_SATA_B_R2D_C_P	NC_SATA_B_R2D_C_P	TRUE	9 23 69
NC_SATA_C_D2R_N	NC_SATA_C_D2R_N	TRUE	9 69
NC_SATA_C_D2R_P	NC_SATA_C_D2R_P	TRUE	9 69
NC_SATA_C_R2D_C_N	NC_SATA_C_R2D_C_N	TRUE	9 23 69
NC_SATA_C_R2D_C_P	NC_SATA_C_R2D_C_P	TRUE	9 23 69

CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

NC_CK505_SRC1_N	NC_CK505_SRC1_N	TRUE	9 29
NC_CK505_SRC1_P	NC_CK505_SRC1_P	TRUE	9 29
NC_CK505_SRC_CLKREQ1_L	NC_CK505_SRC_CLKREQ1_L	TRUE	9 29
NC_CK505_SRC3_N	NC_CK505_SRC3_N	TRUE	9 29
NC_CK505_SRC3_P	NC_CK505_SRC3_P	TRUE	9 29
NC_CK505_SRC_CLKREQ3_L	NC_CK505_SRC_CLKREQ3_L	TRUE	9 29
NC_CK505_SRC4_N	NC_CK505_SRC4_N	TRUE	9 29
NC_CK505_SRC4_P	NC_CK505_SRC4_P	TRUE	9 29
NC_CK505_SRC_CLKREQ4_L	NC_CK505_SRC_CLKREQ4_L	TRUE	9 29
NC_CK505_SRC7_N	NC_CK505_SRC7_N	TRUE	9 29
NC_CK505_SRC7_P	NC_CK505_SRC7_P	TRUE	9 29
NC_CK505_PGMODE	NC_CK505_PGMODE	TRUE	9 29
NC_CK505_SRC8_N	NC_CK505_SRC8_N	TRUE	9 29
NC_CK505_SRC8_P	NC_CK505_SRC8_P	TRUE	9 29
NC_CK505_SRC_CLKREQ8_L	NC_CK505_SRC_CLKREQ8_L	TRUE	9 29
NC_GPU_STOP_L	NC_GPU_STOP_L	TRUE	9 29
NC_CK505_PCI1_CLK	NC_CK505_PCI1_CLK	TRUE	9 29
NC_CK505_PCI2_CLK	NC_CK505_PCI2_CLK	TRUE	9 29
NC_CK505_PCI4_CLK	NC_CK505_PCI4_CLK	TRUE	9 29

SB ALIASES

NO-CONNECT UNUSED INTERFACE PORTS

28 25 9 6 VR_PWRGD_CK505	VR_PWRGD_CK505		6 9 25 28
28 25 9 6 PM_SB_PWROK	PM_SB_PWROK		6 9 25 28
70 PCI_AD<0..31>	NC_PCI_AD<0..31>	TRUE	24 70
70 PCI_C_BE_L<0..3>	NC_PCI_C_BE_L<0..3>	TRUE	24
70 24 9 NC_PCI_PAR	NC_PCI_PAR	TRUE	9 24 70
24 9 6 TP_PCI_RST_L	TP_PCI_RST_L		6 9 24

NB ALIASES

53 16 9 6 GFX_VR_EN	GFX_VR_EN		6 9 16 53
52 28 16 9 6 VR_PWRGOOD_DELAY	VR_PWRGOOD_DELAY	MAKE_BASE=TRUE	6 9 16 28 52
71 30 29 16 9 6 NB_CLK96M_DOT_P	NB_CLK96M_DOT_P	MAKE_BASE=TRUE	6 9 16 29 30 71
71 30 29 16 9 6 NB_CLK96M_DOT_N	NB_CLK96M_DOT_N	MAKE_BASE=TRUE	6 9 16 29 30 71
71 30 29 16 9 6 NB_CLK100M_DPLLSS_P	NB_CLK100M_DPLLSS_P	MAKE_BASE=TRUE	6 9 16 29 30 71
71 30 29 16 9 6 NB_CLK100M_DPLLSS_N	NB_CLK100M_DPLLSS_N	MAKE_BASE=TRUE	6 9 16 29 30 71
64 15 9 6 LCDBKLT_PWM_UNBUF	LCDBKLT_PWM_UNBUF	MAKE_BASE=TRUE	6 9 15 64
64 15 9 6 LCDBKLT_PWREN	LCDBKLT_PWREN	MAKE_BASE=TRUE	6 9 15 64

AUDIO ALIASES

69 37 23 9 7 6 HDA_BIT_CLK	HDA_BIT_CLK	MAKE_BASE=TRUE	6 7 9 23 37 69
69 37 23 9 7 6 HDA_SYNC	HDA_SYNC	MAKE_BASE=TRUE	6 7 9 23 37 69
69 37 23 9 6 HDA_RST_L	HDA_RST_L	MAKE_BASE=TRUE	6 9 23 37 69
69 37 23 9 7 6 HDA_SDIN0	HDA_SDIN0	MAKE_BASE=TRUE	6 7 9 23 37 69
69 37 23 9 7 6 HDA_SDOUT	HDA_SDOUT	MAKE_BASE=TRUE	6 7 9 23 37 69

USB ALIASES

USB PORT [0] = External USB2.0 Port A

69 39 24 9 6 USB2_EXTA_P 39 24 9 6	USB2_EXTA_P	MAKE_BASE=TRUE	USB2_EXTA_P 6 9 24 39 69
69 39 24 9 6 USB2_EXTA_N 39 24 9 6	USB2_EXTA_N	MAKE_BASE=TRUE	USB2_EXTA_N 6 9 24 39 69
39 24 13 9 7 6 EXTAUSB_OC_L 13 9 7 6	EXTAUSB_OC_L	MAKE_BASE=TRUE	EXTAUSB_OC_L 6 7 9 13 24 39
69 39 9 6 USB2_MUXED_EXTA_N	USB2_MUXED_EXTA_N	MAKE_BASE=TRUE	USB2_MUXED_EXTA_N 6 9 39 69
69 39 9 6 USB2_MUXED_EXTA_P	USB2_MUXED_EXTA_P	MAKE_BASE=TRUE	USB2_MUXED_EXTA_P 6 9 39 69

USB PORT [1] = PCI-E Mini Card

69 36 24 9 6 USB2_AIRPORT_P 24 9 6	USB2_AIRPORT_P	MAKE_BASE=TRUE	USB2_AIRPORT_P 6 9 24 36 69
69 36 24 9 6 USB2_AIRPORT_N 24 9 6	USB2_AIRPORT_N	MAKE_BASE=TRUE	USB2_AIRPORT_N 6 9 24 36 69

USB PORT [2] = Unused

69 24 9 TP_USB2_3G_P 69 24 9	TP_USB2_3G_P		TP_USB2_3G_P 9 24 69
69 24 9 TP_USB2_3G_N 69 24 9	TP_USB2_3G_N	MAKE_BASE=TRUE	TP_USB2_3G_N 9 24 69

USB PORT [3] = CAMERA

69 60 24 9 6 USB2_CAMERA_P 24 9 6	USB2_CAMERA_P	MAKE_BASE=TRUE	USB2_CAMERA_P 6 9 24 60 69
69 60 24 9 6 USB2_CAMERA_N 24 9 6	USB2_CAMERA_N	MAKE_BASE=TRUE	USB2_CAMERA_N 6 9 24 60 69

USB PORT [4] = IR CONTROLLER

69 40 24 9 7 6 USB_IR_P 40 24 9 7 6	USB_IR_P		USB_IR_P 6 7 9 24 40 69
69 40 24 9 7 6 USB_IR_N	USB_IR_N	MAKE_BASE=TRUE	USB_IR_N 6 7 9 24 40 69

USB PORT [5] = Trackpad(Wellspring)

69 40 24 9 7 6 USB2_WSPRING_P 9 7 6	USB2_WSPRING_P		USB2_WSPRING_P 6 7 9 24 40 69
69 40 24 9 7 6 USB2_WSPRING_N 9 7 6	USB2_WSPRING_N	MAKE_BASE=TRUE	USB2_WSPRING_N 6 7 9 24 40 69

USB PORT [6] = BLUETOOTH

69 24 9 NC_USB_BT_P 69 24 9	NC_USB_BT_P		NC_USB_BT_P 9 24 69
69 24 9 NC_USB_BT_N 69 24 9	NC_USB_BT_N	MAKE_BASE=TRUE	NC_USB_BT_N 9 24 69

USB PORT [7] = Unused

69 24 9 NC_USB2_EXTB_P	NC_USB2_EXTB_P	MAKE_BASE=TRUE	NC_USB2_EXTB_P 9 24 69
69 24 9 NC_USB2_EXTB_N	NC_USB2_EXTB_N	MAKE_BASE=TRUE	NC_USB2_EXTB_N 9 24 69
24 13 9 7 6 EXTBUSB_OC_L 13 9 7 6	EXTBUSB_OC_L	MAKE_BASE=TRUE	EXTBUSB_OC_L 6 7 9 13 24

USB PORT [8] = Unused

69 24 9 TP_USB_EXCARD_P	TP_USB_EXCARD_P		TP_USB_EXCARD_P 9 24 69
69 24 9 TP_USB_EXCARD_N	TP_USB_EXCARD_N	MAKE_BASE=TRUE	TP_USB_EXCARD_N 9 24 69

USB PORT [9] = Unused

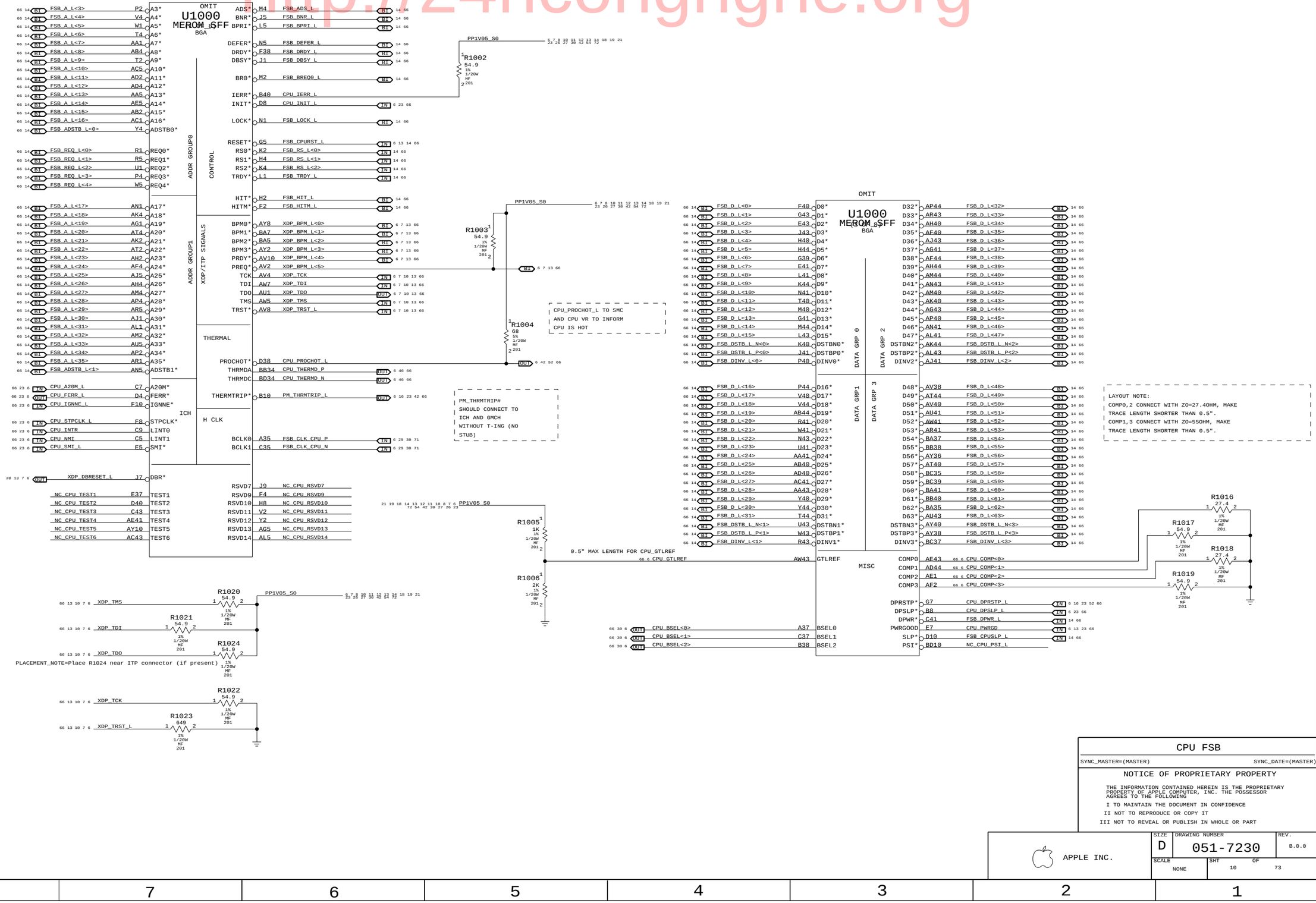
69 24 9 TP_USB_EXTC_P	TP_USB_EXTC_P		TP_USB_EXTC_P 9 24 69
69 24 9 TP_USB_EXTC_N	TP_USB_EXTC_N	MAKE_BASE=TRUE	TP_USB_EXTC_N 9 24 69

SIGNAL ALIAS /RESET

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 9 OF 73	

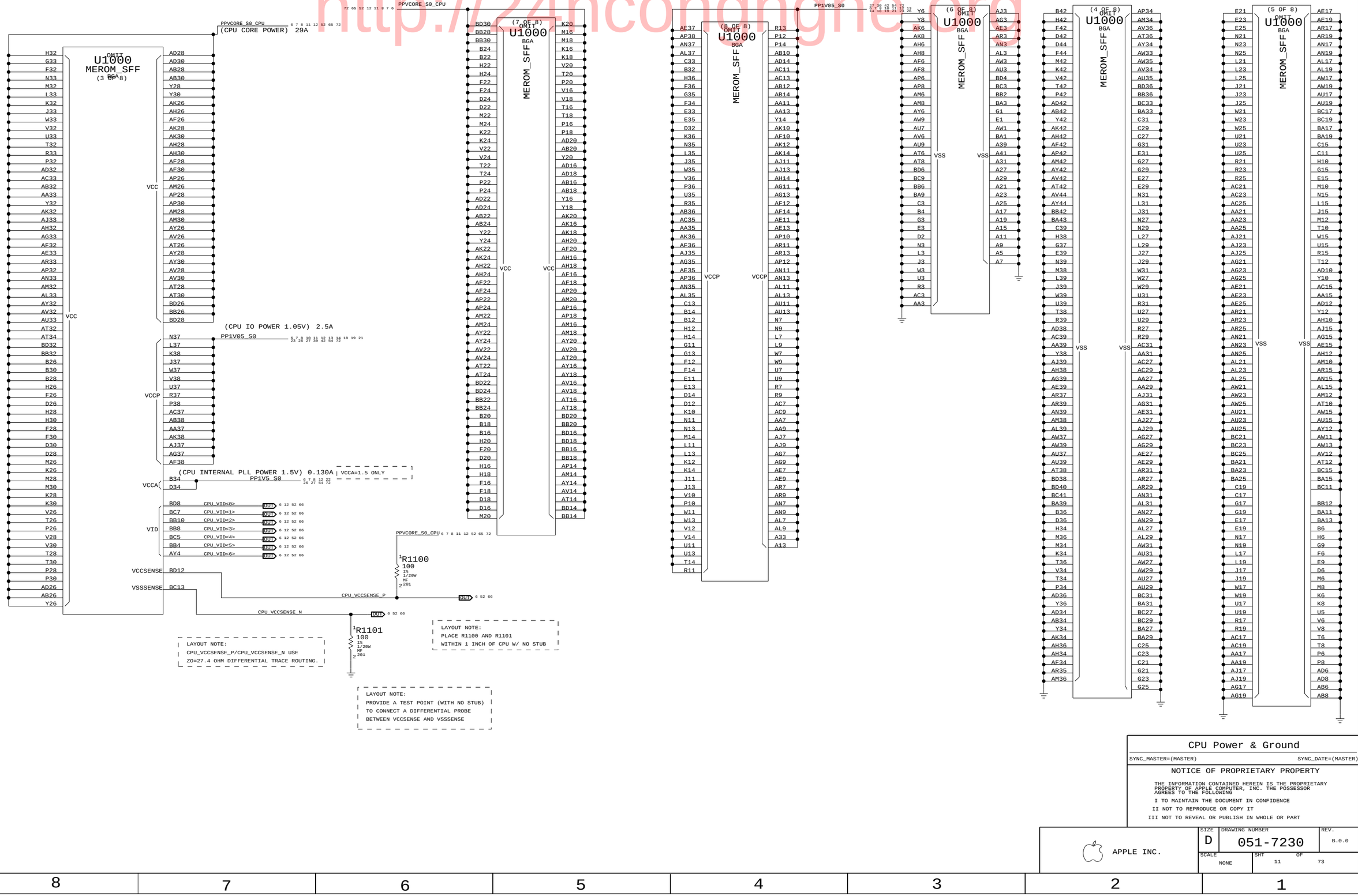


CPU FSB

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 10 OF 73	



CPU Power & Ground

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 11 OF 73	

CPU VCORE HF AND BULK DECOUPLING

3x 330uF. 32x 10uF 0603, 28x 1uF 0402
Intel recommends 32+28 but is evaluating 24+24

72 65 52 11 8 7 6 PPVCORE_S0_CPU

10UF 0603 = APN:138S0568 = MURATA,TAIYO,TDK,SAMSUNG

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1200 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1201 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1202 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1203 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1204 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1205 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1206 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1207 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1208 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1209 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1210 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1211 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1212 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1213 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1214 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1215 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1216 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1217 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1218 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1219 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1220 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1221 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1222 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1223 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1224 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1225 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1226 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1227 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1228 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1229 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1230 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1231 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1240 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1241 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1242 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1243 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1244 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1245 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1246 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1247 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1248 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1249 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1250 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1251 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1252 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1253 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1254 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1255 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1256 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1257 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1258 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1259 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1260 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1261 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1262 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1263 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1264 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1265 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1266 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1267 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

CRITICAL C1270 330UF 20% 2.0V TANT D2T
CRITICAL C1271 330UF 20% 2.0V TANT D2T

CRITICAL C1272 330UF 20% 2.0V TANT D2T

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

Intel recommends 3x220UF @ 9mOHM

CPU VCORE VID CONNECTIONS

66 52 11 6 CPU_VID<0..6> — IMVP6_VID<0..6> 66
MAKE_BASE=TRUE

VCCA (CPU AVdd) DECOUPLING

72 54 27 26 22 11 8 7 6 PP1V5_S0

1x 10uF, 1x 0.01uF

OMIT C1200 10UF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V X5R 201

LAYOUT NOTE:
PLACE C1281 NEAR PIN B34 OF U1000

VCCP (CPU I/O) DECOUPLING

23 21 19 18 14 13 11 10 8 7 6 PP1V05_S0
72 64 42 30 27 26

1X 330UF, 12X 2.2UF

OMIT C1283 2.2UF 20% 6.3V CERM 402-LF
OMIT C1284 2.2UF 20% 6.3V CERM 402-LF
OMIT C1285 2.2UF 20% 6.3V CERM 402-LF
OMIT C1286 2.2UF 20% 6.3V CERM 402-LF
OMIT C1287 2.2UF 20% 6.3V CERM 402-LF
OMIT C1288 2.2UF 20% 6.3V CERM 402-LF

CRITICAL C1290 330UF 20% 2.5V POLY CASE-C2-SM-1

OMIT C1291 2.2UF 20% 6.3V CERM 402-LF
OMIT C1292 2.2UF 20% 6.3V CERM 402-LF
OMIT C1293 2.2UF 20% 6.3V CERM 402-LF
OMIT C1294 2.2UF 20% 6.3V CERM 402-LF
OMIT C1295 2.2UF 20% 6.3V CERM 402-LF
OMIT C1296 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE C1290 CLOSE TO CPU
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

CPU Decoupling & VID

SYNC_MASTER=MSARWAR SYNC_DATE=04/26/2006

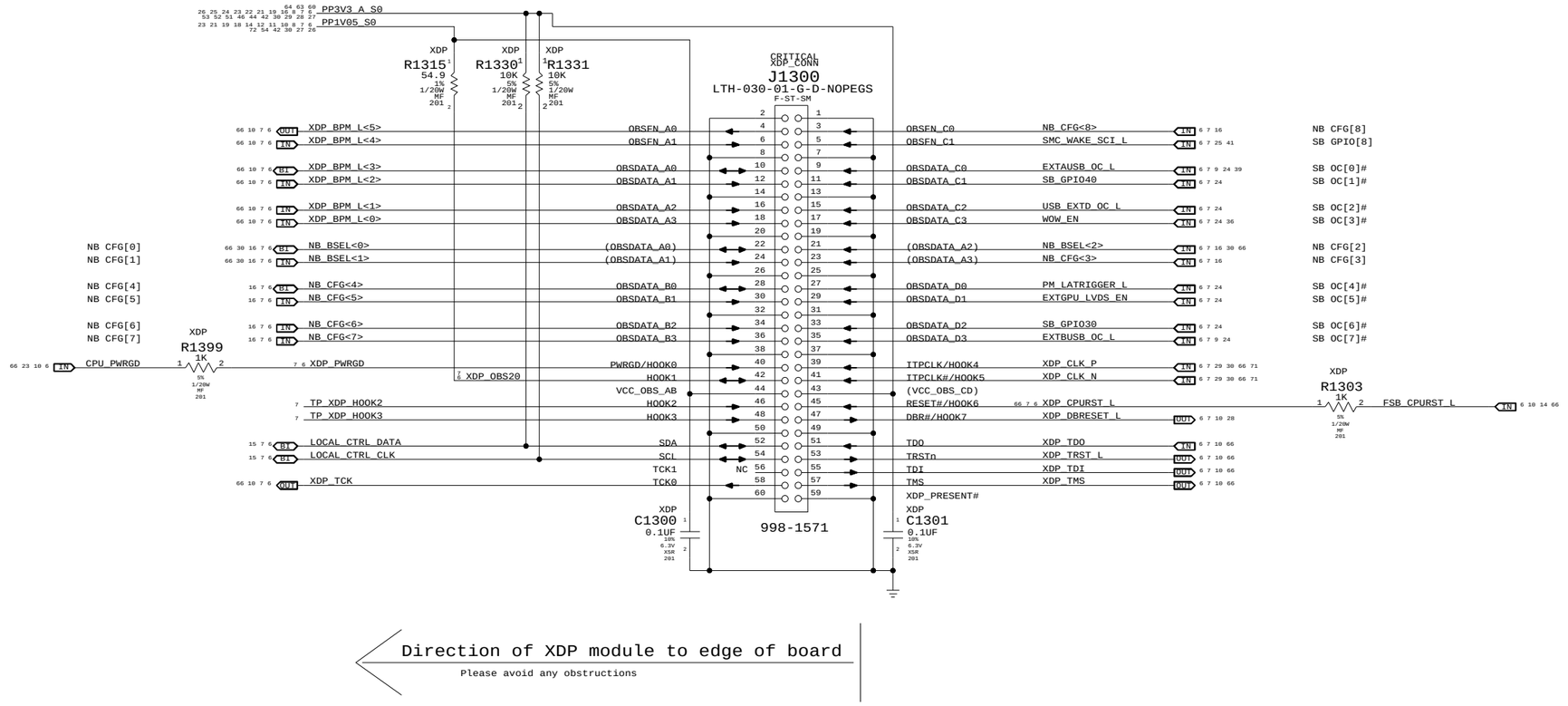
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 12 OF 73	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module to edge of board

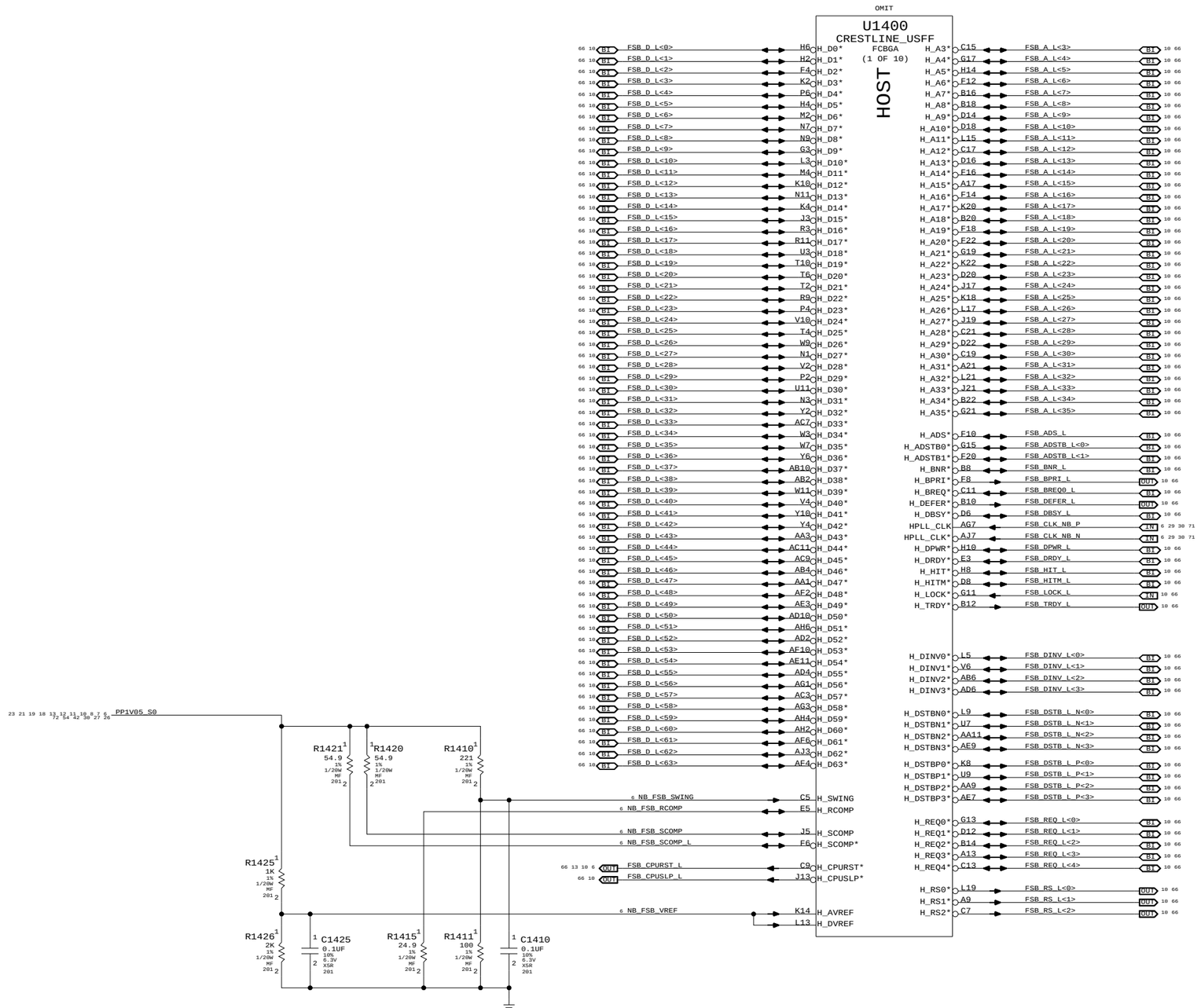
Please avoid any obstructions

eXtended Debug Port (XDP)

SYNC_MASTER=M75 SYNC_DATE=01/24/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 13 OF 73	



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 14 OF 73	

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

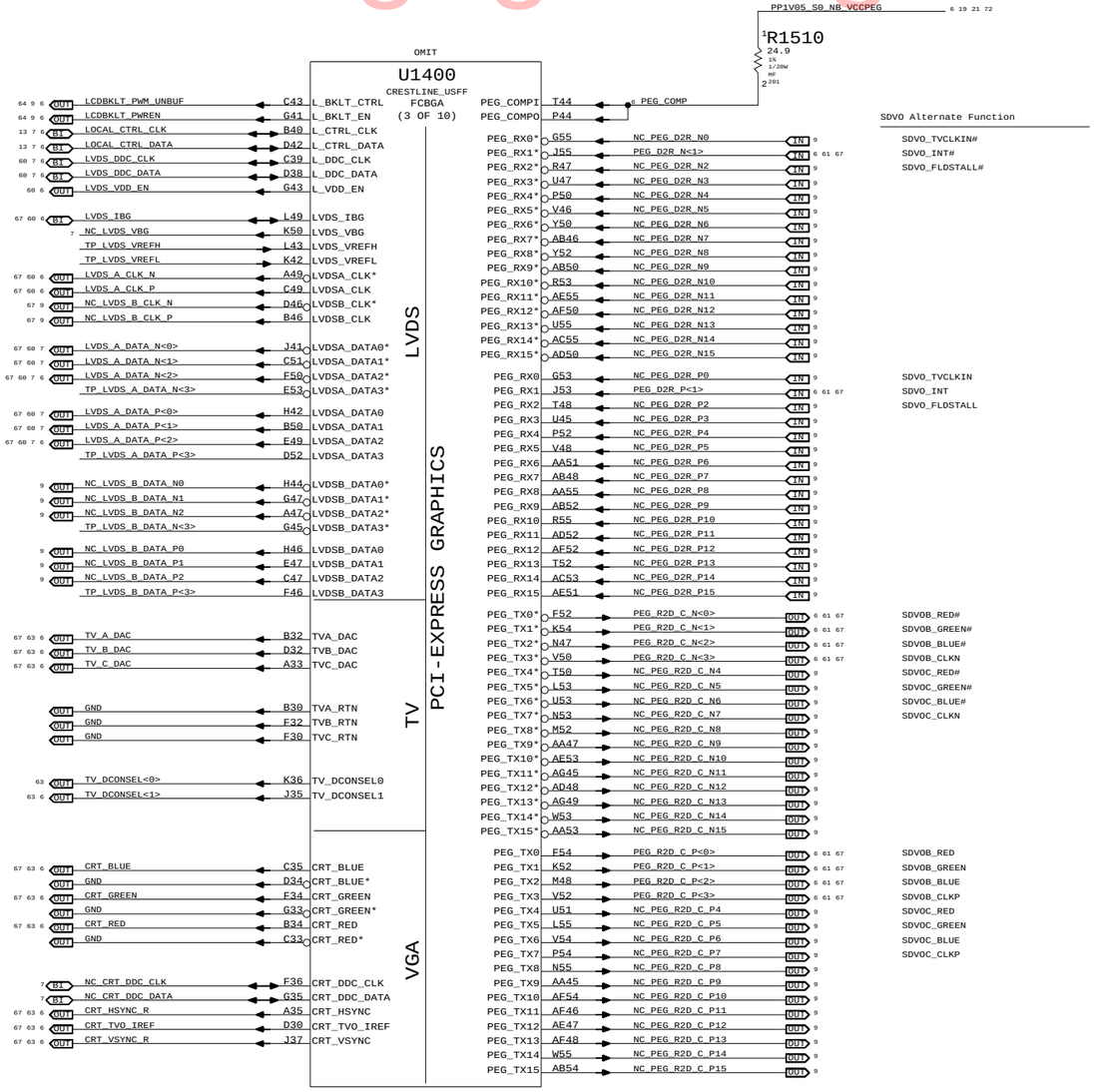
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 15 OF 73	

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB CFG<5> chooses DMI x4 w/ TP

NB_CFG<9> — NBCFG_PEG_REVERSE — R1659 4.02K 1% 1/20W MF 201

NB_CFG<16> — NBCFG_DYN_ODT_DISABLE — R1666 4.02K 1% 1/20W MF 201

PP3V3_A_S0 — NBCFG_SDVO_AND_PCIE — R1669 4.02K 1% 1/20W MF 201 — NB_CFG<19>

PP3V3_A_S0 — R1670 4.02K 1% 1/20W MF 201 — NB_CFG<20>

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

PP3V3_A_S0 — R1630 10K 5% 1/20W MF 201 — R1631 10K 5% 1/20W MF 201

PM_EXTTS_L<0>
PM_EXTTS_L<1>

RSVD bit ordering based on CRB numbering

OMIT

U1400
CRESTLINE_USFF
FCBGA
(2 OF 10)

RSVD

TP_NB_RSVD<42>	A39	
NC_NB_RSVD_8	AG11	
NC_NB_RSVD_7	AG9	
NC_NB_RSVD_5	AH10	
NC_NB_RSVD_6	AJ11	
TP_NB_RSVD<12>	AJ43	
TP_NB_RSVD<11>	AL43	
TP_NB_RSVD<13>	AN43	
TP_NB_RSVD<10>	AR43	
TP_NB_RSVD<45>	B36	
TP_NB_RSVD<41>	B38	
NC_NB_RSVD_21	B55	
NC_NB_RSVD_28	BA33	
NC_NB_RSVD_35	BB22	
NC_NB_RSVD_29	BC33	
NC_NB_RSVD_30	BF22	
NC_NB_RSVD_31	BE23	
NC_NB_RSVD_24	BH18	
NC_NB_RSVD_36	BE27	
NC_NB_RSVD_22	BJ17	
NC_NB_RSVD_25	BK16	
NC_NB_RSVD_27	BK18	
TP_NB_RSVD<34>	BK32	
NC_NB_RSVD_26	BL17	
NC_NB_RSVD_23	BL19	
TP_NB_RSVD<43>	C37	
TP_NB_RSVD<9>	D10	
TP_NB_RSVD<44>	D36	
NC_NB_RSVD_4	G51	
TP_NB_RSVD<20>	G9	
NC_NB_RSVD_3	H52	
NC_NB_RSVD_14	J25	
NC_NB_RSVD_1	M46	
NC_NB_RSVD_2	N45	

DDR MUXING

SM_CK0	BC37	MEM_CLK_P<0>
SM_CK1	BC25	MEM_CLK_P<1>
SM_CK3	BB36	MEM_CLK_P<3>
SM_CK4	BB24	MEM_CLK_P<4>
SM_CK0*	BA37	MEM_CLK_N<0>
SM_CK1*	BC23	MEM_CLK_N<1>
SM_CK3*	BB34	MEM_CLK_N<3>
SM_CK4*	BB26	MEM_CLK_N<4>
SM_CKE0	BE33	MEM_CKE<0>
SM_CKE1	BE35	MEM_CKE<1>
SM_CKE3	BF40	MEM_CKE<3>
SM_CKE4	BE39	MEM_CKE<4>
SM_CS0*	BA23	MEM_CS_L<0>
SM_CS1*	BH16	MEM_CS_L<1>
SM_CS2*	BE15	MEM_CS_L<2>
SM_CS3*	BH14	MEM_CS_L<3>
SM_ODT0	BJ15	MEM_ODT<0>
SM_ODT1	BF20	MEM_ODT<1>
SM_ODT2	BE13	MEM_ODT<2>
SM_ODT3	BH12	MEM_ODT<3>
SM_RCOMP	BL13	MEM_RCOMP
SM_RCOMP*	BK14	MEM_RCOMP_L
SM_RCOMP_VOH	BK36	MEM_RCOMP_VOH
SM_RCOMP_VOL	BL37	MEM_RCOMP_VOL
SM_VREF0	AM54	PP0V9_S3M_MEM_NBVREFA
SM_VREF1	AT12	PP0V9_S3M_MEM_NBVREFB

PP1V8_S3 — R1610 20 1% 1/20W MF 201 — C1623 0.01UF 10% 10V X5R 201 — OMIT C1622 2.2UF 20% 6.3V CERM 402-LF — R1620 1K 1% 1/20W MF 201 — R1622 3.01K 1% 1/20W MF 201

C1615 0.1UF 10% 6.3V X5R 201 — C1616 0.1UF 10% 6.3V X5R 201

R1611 20 1% 1/20W MF 201 — C1625 0.01UF 10% 10V X5R 201 — OMIT C1624 2.2UF 20% 6.3V CERM 402-LF — R1624 1K 1% 1/20W MF 201

CLK

DPLL_REF_CLK	C45	NB_CLK96M_DOT_P
DPLL_REF_CLK*	B44	NB_CLK96M_DOT_N
DPLL_REF_SSCLK	H50	NB_CLK100M_DPLLSS_P
DPLL_REF_SSCLK*	G49	NB_CLK100M_DPLLSS_N
PEG_CLK	N51	NB_CLK100M_PCIE_P
PEG_CLK*	M50	NB_CLK100M_PCIE_N

Clk used for PEG and DMI

DMI

DMI_RXN0	AL45	DMI_S2N_N<0>
DMI_RXN1	AK54	DMI_S2N_N<1>
DMI_RXN2	AJ55	DMI_S2N_N<2>
DMI_RXN3	AH52	DMI_S2N_N<3>
DMI_RXP0	AM46	DMI_S2N_P<0>
DMI_RXP1	AK52	DMI_S2N_P<1>
DMI_RXP2	AJ53	DMI_S2N_P<2>
DMI_RXP3	AH50	DMI_S2N_P<3>
DMI_TXN0	AH48	DMI_N2S_N<0>
DMI_TXN1	AK48	DMI_N2S_N<1>
DMI_TXN2	AG55	DMI_N2S_N<2>
DMI_TXN3	AL53	DMI_N2S_N<3>
DMI_TXP0	AJ47	DMI_N2S_P<0>
DMI_TXP1	AK50	DMI_N2S_P<1>
DMI_TXP2	AG53	DMI_N2S_P<2>
DMI_TXP3	AL55	DMI_N2S_P<3>

CFG

NB_BSEL<0>	H28	CFG0	
NB_BSEL<1>	G25	CFG1	
NB_BSEL<2>	C25	CFG2	
NB_CFG<3>	K24	CFG3	IPU
NB_CFG<4>	B28	CFG4	IPU
NB_CFG<5>	G27	CFG5	IPU
NB_CFG<6>	B26	CFG6	IPU
NB_CFG<7>	D26	CFG7	IPU
NB_CFG<8>	D24	CFG8	IPU
NB_CFG<9>	F26	CFG9	IPU
NC_NB_CFG_10	A25	CFG10	IPU
NC_NB_CFG_11	L23	CFG11	IPU
TP_NB_CFG<12>	D28	CFG12	IPU
TP_NB_CFG<13>	F24	CFG13	IPU
NC_NB_CFG_14	C29	CFG14	IPU
NC_NB_CFG_15	C27	CFG15	IPU
NB_CFG<16>	A29	CFG16	IPU
NC_NB_CFG_17	J27	CFG17	IPU
TP_NB_CFG<18>	G31	CFG18	IPD
NB_CFG<19>	K30	CFG19	IPD
NB_CFG<20>	L37	CFG20	IPD

VID

GFX_VID0	G37	GFX_VID<0>
GFX_VID1	A45	GFX_VID<1>
GFX_VID2	B42	GFX_VID<2>
GFX_VID3	D44	GFX_VID<3>
GFX_VR_EN	F42	GFX_VR_EN

GND

PM

PM_BMBUSY_L	F44	PM_BM_BUSY*
CPU_DPRSTP_L	C41	PM_DPRSTP*
	L39	PM_EXT_TS0*
	J39	PM_EXT_TS1*
VR_PWRGOOD_DELAY	AT50	PWROK
NB_RESET_L	BB20	RSTIN*
PM_THRMTRIP_L	F28	THERMTRIP*
PM_DPRSLPVR	F40	DPRSLPVR

GRAPHICS

ME

CL_CLK	BE52	CLINK_NB_CLK
CL_DATA	BE53	CLINK_NB_DATA
CL_PWROK	AP50	VR_PWRGOOD_DELAY
CL_RST*	BH52	CLINK_NB_RESET_L
CL_VREF	BF54	NB_CLINK_VREF

NC

NC_NB_NC_14	A52
NC_NB_NC_13	A54
NC_NB_NC_12	B54
NC_NB_NC_10	BH1
NC_NB_NC_2	BH55
NC_NB_NC_9	BK1
NC_NB_NC_8	BK2
NC_NB_NC_4	BK54
NC_NB_NC_1	BK55
NC_NB_NC_7	BL2
NC_NB_NC_6	BL4
NC_NB_NC_5	BL52
NC_NB_NC_3	BL54
NC_NB_NC_11	D55

MISC

SDVO_CTRL_CLK	K38	SDVO_CTRLCLK
SDVO_CTRL_DATA	K40	SDVO_CTRLDATA
CLKREQ*	G39	NB_CLKREQ_L
ICH_SYNC*	D40	NB_SB_SYNC_L
TEST1	F38	NB_TEST1
TEST2	K34	NB_TEST2

R1691 20K 5% 1/20W MF 201 — R1690 0 5% 1/20W MF 201

PP1V25_S0 — R1640 1K 1% 1/20W MF 201 — C1640 0.1UF 10% 6.3V X5R 201 — R1641 392 1% 1/20W MF 201

NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

NB Misc Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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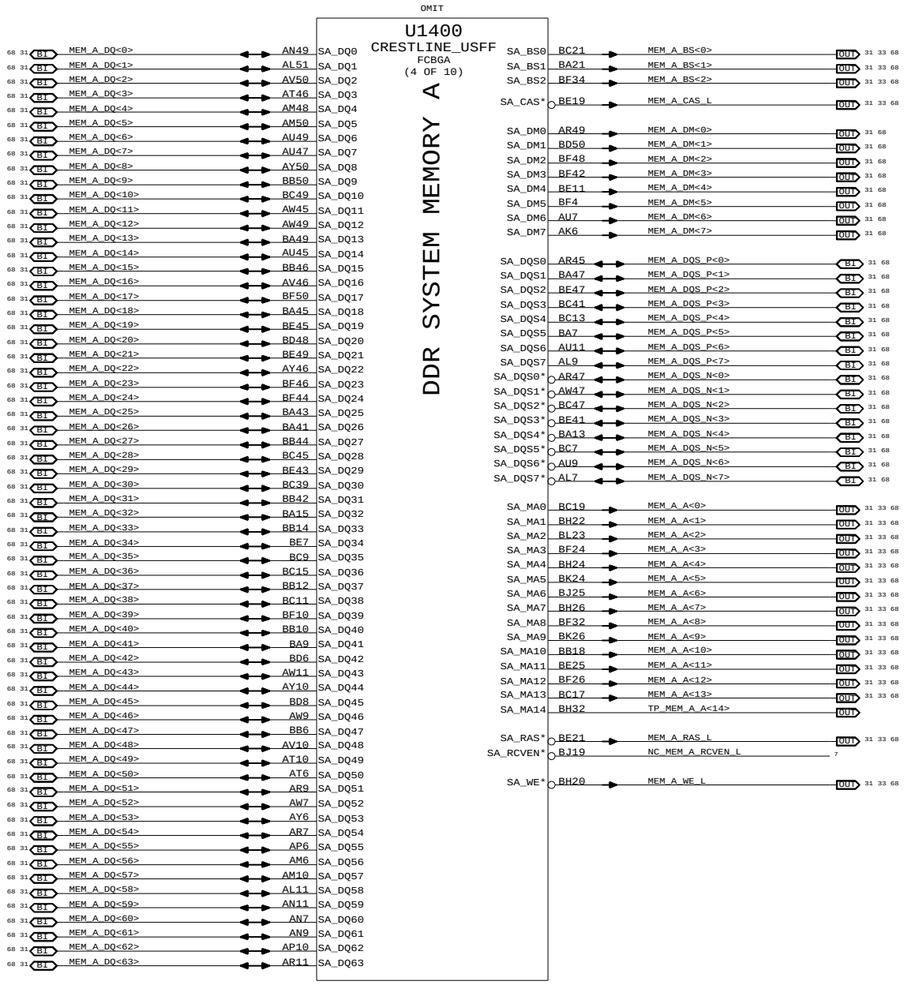
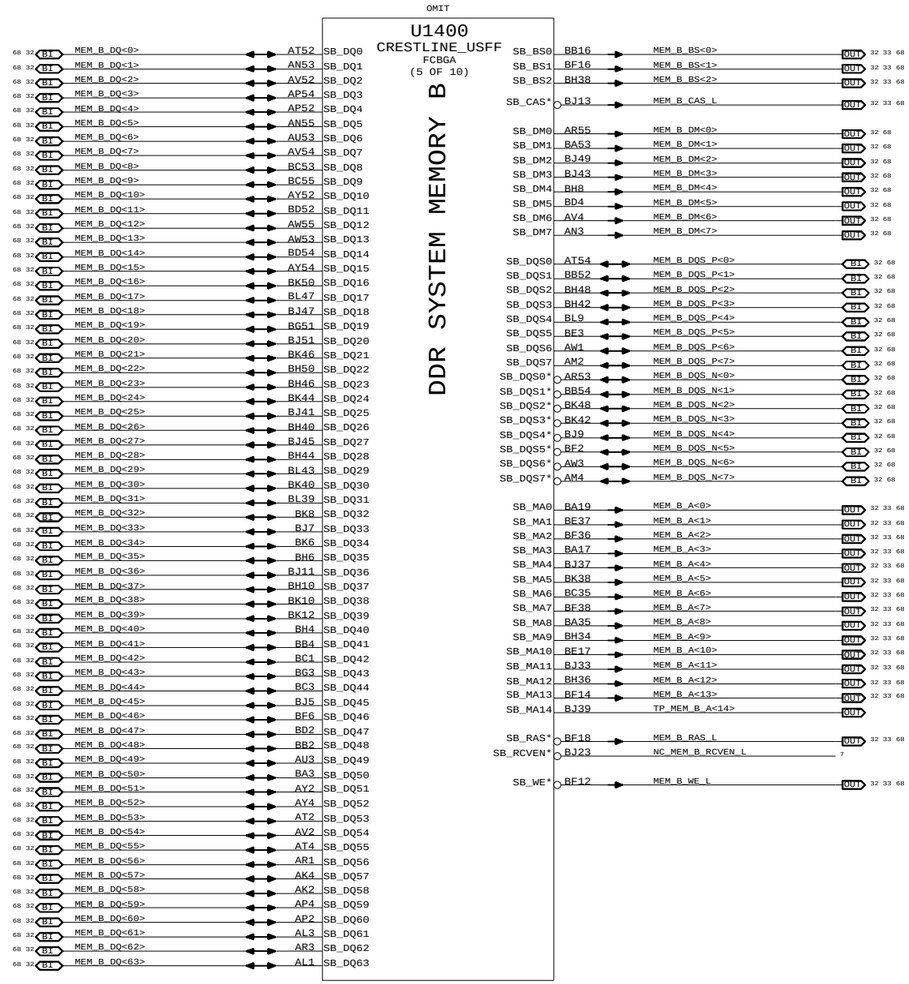
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 16 OF 73	





NB DDR2 Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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D	051-7230	B.0.0
SCALE: NONE	SHT 17 OF 73	

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

PPVCORE_S0_NB_GFX

PP1V05_S0

1310 mA (Ext Graphics)
1600 mA (Int Graphics)

PP1V8_S3

3300 mA (2 ch, 667MHz)
2700 mA (2 ch, 533MHz)
1700 mA (1 ch, 667MHz)
1395 mA (1 ch, 533MHz)
5 mA (standby)

PPVCORE_S0_NB_GFX

7700 mA (Int Graphics)

PP1V05_S0

540mA

PP1V05_S0

PP1V25_S0

640mA

POWER
OMIT
(6 OF 10)
U1400
FCBGA
CRESTLINE_USFF

POWER
OMIT
(7 OF 10)
U1400
FCBGA
CRESTLINE_USFF

VCC_AXG_NCTF
VCC
VCC_SM
VCC_SM_NCTF
VCC_SM_LF
VCC_AXG
VCC_NCTF
VCC_AXM
VCC_AXM_NCTF
VCCA_SM
VCCA_SM_NCTF
VSS_SCB

NB_VCCSM_LF1
NB_VCCSM_LF2
NB_VCCSM_LF3
NB_VCCSM_LF4
NB_VCCSM_LF5
NB_VCCSM_LF6
NB_VCCSM_LF7

C1807 0.1UF 10% 6.3V X5R 201
C1806 0.1UF 10% 6.3V X5R 201
C1805 0.22UF 20% 6.3V X5R 402
C1804 0.22UF 20% 6.3V X5R 402
C1803 0.47UF 10% 6.3V CERM-X5R 402
C1802 OMIT 1uF 10% 6.3V CERM 402
C1801 OMIT 1uF 10% 6.3V CERM 402

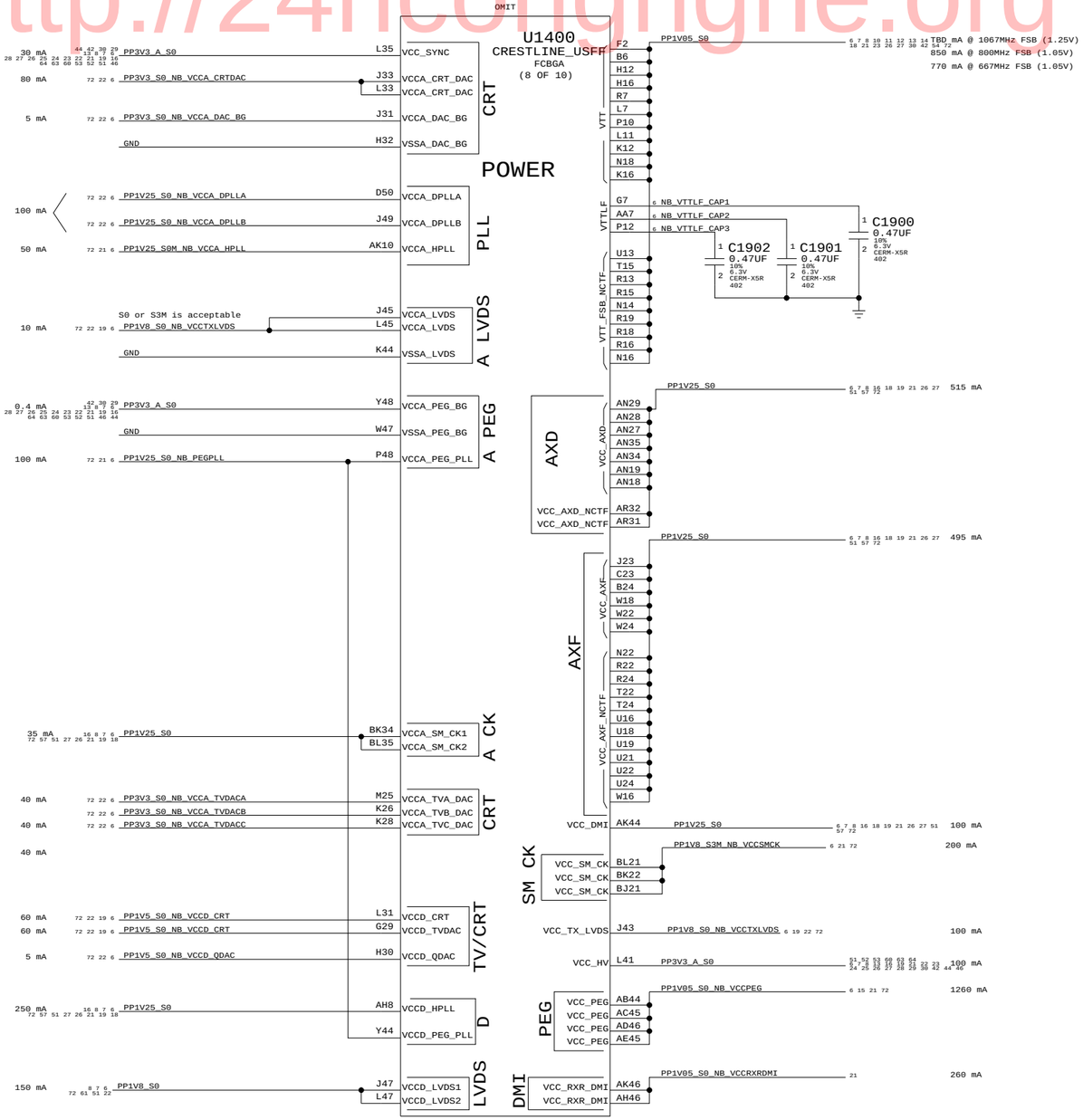
Current numbers from Crestline EDS, doc #21749.

NB Power 1

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 18 OF 73	



Current numbers from Crestline EDS, doc #21749.

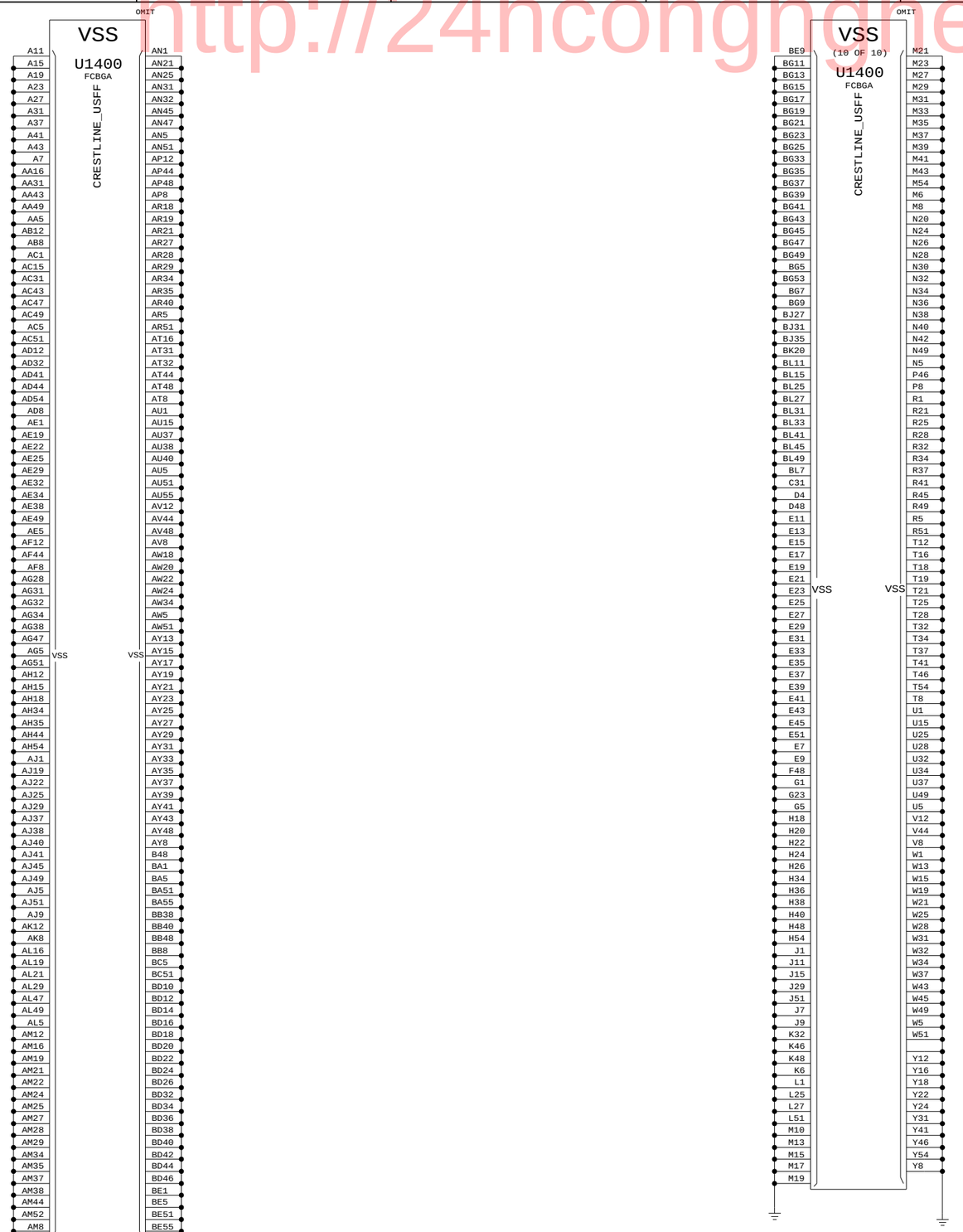
NB Power 2

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE: NONE SHT 19 OF 73



NB Grounds

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	20	73

GMCH Core Power

PP1V05_S0 — 1600 mA

CRITICAL C2100 330UF 20% 2.5V POLY CASE-C2-SM-1

C2101 22UF 20% 6.3V CERM 805

C2102 0.22uF 20% 6.3V XSR 402

C2103 0.22uF 20% 6.3V XSR 402

C2104 0.1UF 10% 6.3V XSR 201

PLACEMENT_NOTE=Place in GMCH cavity

GMCH ME Core Power

PP1V05_S0 — 540 mA

C2110 22UF 20% 6.3V CERM 805

C2111 0.22uF 20% 6.3V XSR 402

C2112 0.22uF 20% 6.3V XSR 402

C2113 0.1UF 10% 6.3V XSR 201

C2114 0.1UF 10% 6.3V XSR 201

C2115 0.1UF 10% 6.3V XSR 201

Place C2110-12 on edge near AH31..AM32

Place C2113-2115 close as possible to AH31..AM32

GMCH FSB I/O Rail

PP1V05_S0 — 850 mA

C2121 4.7uF 20% 6.3V CERM 603

C2122 4.7uF 20% 6.3V CERM 603

C2123 2.2uF 20% 6.3V CERM1 603

C2124 0.47UF 10% 6.3V CERM-X5R 402

PLACEMENT_NOTE=Place C2121-24 close to U1400.F2..K16

GMCH Memory I/O Rail

PP1V8_S3 — 3300 mA

CRITICAL C2130 330UF 20% 2.0V POLY CASE-B2-HF

C2135 0.1UF 10% 6.3V XSR 201

C2132 22UF 20% 6.3V CERM 805

C2133 22UF 20% 6.3V CERM 805

this is "1 of 2" 1.8V bulk decoupling caps.

PLACEMENT_NOTE=Place C2132,C2133 close to U1400.BA27..BL29

Place C2135 where LVDS taps from DDR2 plane.

I/O voltage Supply

PP1V25_S0 — 495 mA — PP1V25_S0 — 450 mA — PP1V25_S0

OMIT C2170 1UF 10% 6.3V CERM 402

Layout Note: PLACE C2170 NEAR J23..W24

Host PLL Digital Supply

PP1V25_S0 — 250 mA

C2180 0.1UF 10% 6.3V XSR 201

Layout Note: Place C2180 Near Pin AH8

250mA,0.5ohm L2181 120-OHM-0.3A-EMI 0402-LF

Host PLL Analog Supply

PP1V25_S0M_NB_VCCA_HPLL — 50 mA

MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.25V

C2181 22UF 20% 6.3V CERM 805

C2182 0.1UF 10% 6.3V XSR 201

Layout Note: Place C2182 Near Pin AK10

250mA,0.5ohm

These supplies are still needed even using external GPU

PP1V05_S0 — 1520 mA

Layout Note: Place L and C close to MCH

CRITICAL L2173 91NH 1210

CRITICAL C2173 220UF 20% 2.5V POLY CASE-B2-HF

Analog,I/O logic,and Term Voltage for PCI-E Graphics

PP1V05_S0_NB_VCCPEG — 1260 mA

MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V

C2174 22UF 20% 6.3V CERM 805

Layout Note: 22uF caps should be close to MCH on opposite side. Place C2174 Near Pins AB44..AE45

RX and I/O Logic for DMI

PP1V05_S0_NB_VCCRXRDMI — 260 mA

C2177 22UF 20% 6.3V CERM 805

Layout Note: 22uF caps should be close to MCH on opposite side. Place C2177 Near Pins AH46,AK46

Memory I/O logic and DLL voltage.

PP1V25_S0 — 675 mA — PP1V25_S0 — 640 mA

CRITICAL C2140 100UF 20% 6.3V POLY B2-HF

C2142 22UF 20% 6.3V CERM 805

C2143 4.7UF 10% 6.3V XSR-CERM 603

OMIT C2144 1UF 10% 6.3V CERM 402

Layout Note: PLACE C2143,C2144 NEAR AL18..AN38

Memory clock logic voltage.

PP1V25_S0 — 35 mA

C2145 22UF 20% 6.3V CERM 805

C2148 0.1UF 10% 6.3V XSR 201

Layout Note: PLACE C2145,C2148 NEAR BL35,BK34

Memory voltage supply.

PP1V25_S0 — 515 mA

OMIT C2151 1UF 10% 6.3V CERM 402

Layout Note: PLACE C2151 NEAR AN29..AN18

Analog PLL Voltage for PCI-E GPU

PP1V25_S0 — 100 mA

L2190 FERR-220-OHM-2.5A 0603

PP1V25_S0_NB_PEGPLL — 100 mA

MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.25V

R2190 1.1 1% 1/10W MF-LF 402

C2191 0.1UF 10% 6.3V XSR 201

C2192 0.1UF 10% 6.3V XSR 201

Layout Note: PLACE C2191 NEAR U1400.P48 PLACE C2192 NEAR U1400.Y44

PP1V25_S0_NB_PEGPLL_RC

MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.25V

OMIT C2190 10UF 20% 6.3V XSR 603

D2186 1SS418 SOD-723

PP1V05_S0 — PP3V3_S0_NBCORE_FOLLOW_R — PP3V3_A_S0

MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V

R2186 10 1% 1/16W MF-LF 402

NOTE: This follower is redundant if VCORE is always 1.05V.

need to find "1uH,220mA,150mohm max"

PP1V8_S3 — 200 mA — L2195 1.0UH-0.23A 0603

PP1V8_S3_NB_VCCSMCK — 200 mA

MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.8V

R2195 1.1 1% 1/16W MF-LF 402

C2196 22UF 20% 6.3V CERM 805

C2197 0.1UF 10% 6.3V XSR 201

Layout Note: PLACE C2197 AND FILTER CLOSE TO BL21..BJ21

PP1V8_S3_NB_VCCSMCK_RC

MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.8V

OMIT C2195 10UF 20% 6.3V XSR 603

PP3V3_A_S0 — 100 mA — PP1V25_S0 — 100 mA

Layout Note: PLACE C2161 NEAR PIN L41

C2160 0.1UF 10% 6.3V XSR 201

Layout Note: PLACE C2160 NEAR PIN AK44

C2161 0.1UF 10% 6.3V XSR 201

PP3V3_A_S0 — 5 mA

C2165 0.1UF 10% 6.3V XSR 201

Layout Note: PLACE C2165 BETWEEN Y48,W47

GND

Layout Note: Route to caps, then GND

PP1V8_S3

NB_VTTREF_DIV R2112 1K 1% 1/20W MF 201

PP0V9_S3M_MEM_NBVREFA

NB_VTTREF_DIV R2113 1K 1% 1/20W MF 201

PP1V8_S3

NB_VTTREF_DIV R2110 1K 1% 1/20W MF 201

PP0V9_S3M_MEM_NBVREFB

NB_VTTREF_DIV R2111 1K 1% 1/20W MF 201

Layout Note: PLACE NEAR NB

Current numbers from Crestline EDS Addendum, doc .....

NB Standard Decoupling

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 21 OF 73	

NOTE: This filter is required even if using only external graphics.

VCCD_TVDAC also powers internal thermal sensors.

PP1V5_S0 — 125 mA

CRITICAL C2201 22000pF-1000mA 16V NFM18

C2202 0.01UF 10% 10V X5R 201

C2200 0.1UF 10% 6.3V X5R 201

PP1V5_S0_NB_VCCD_CRT — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V — 60 mA

PP1V5_S0_NB_VCCD_CRT — 60 mA

PP1V5_S0_NB_VCCD_CRT — PP1V5_S0_NB_VCCD_CRT MAKE_BASE=TRUE

R2205 100 1% 1/10W MF-LF 402

PP1V5_S0_NB_QDAC — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V

CRITICAL C2206 22000pF-1000mA 16V NFM18

PP1V5_S0_NB_VCCD_QDAC — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V — 500 uA

C2205 0.01UF 10% 10V X5R 201

C2207 0.1UF 10% 6.3V X5R 201

C2208 1UF 10% 10V X5R 402-1

Filtering changed per SR MOW # 541194

Layout Note: These 4 caps should be within 6.35 mm of NB edge

PP5V_S0 — 205 mA

R2281 0 5% 1/20W MF 201

OMIT C2280 1UF 10% 6.3V CERM 402

NO STUFF C2281 1UF 10% 6.3V CERM 402

P3V3TVDAC_EN_RC

U2280 TPS79933 SON — IN, EN, NC, GND, OUT, NR, THRML PAD — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=3.3V

PP3V3_S0_NB_TVDAC — 205 mA

P3V3TVDAC_NOISE

C2282 0.01UF 10% 10V X5R 201

OMIT C2285 10UF 20% 6.3V CERM 603

CRITICAL L2288 180-OHM-1.5A 0603

PP3V3_S0_NB_CRTDAC_F — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 80 mA

CRITICAL C2289 22000pF-1000mA 16V NFM18

C2295 0.01UF 10% 10V X5R 201

C2288 0.1UF 10% 6.3V X5R 201

PP3V3_S0_NB_VCCA_CRTDAC — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 80 mA

Layout Note: These 2 caps should be within 6.35 mm of NB edge

PP1V5_S0

NO STUFF D2285 1SS418 SOD-723

NO STUFF R2285 10 1% 1/10W MF-LF 402

PP3V3_S0_NB_TVDAC_FOLLOW — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V

CRITICAL L2290 180-OHM-1.5A 0603

PP3V3_S0_NB_TVDAC_F — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 125 mA

CRITICAL C2292 22000pF-1000mA 16V NFM18

C2293 0.01UF 10% 10V X5R 201

C2291 0.1UF 10% 6.3V X5R 201

PP3V3_S0_NB_VCCA_TVDACA — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 40 mA

CRITICAL C2294 22000pF-1000mA 16V NFM18

PP3V3_S0_NB_VCCA_TVDACB — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 40 mA

Layout Note: These 11 caps should be within 6.35 mm of NB edge

CRITICAL C2296 22000pF-1000mA 16V NFM18

PP3V3_S0_NB_VCCA_TVDACC — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 40 mA

CRITICAL C2298 22000pF-1000mA 16V NFM18

PP3V3_S0_NB_VCCA_DAC_BG — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 5 mA

C2299 0.01UF 10% 10V X5R 201

C2297 0.1UF 10% 6.3V X5R 201

GND

Layout Note: Route to caps, then GND

GMCH Graphics Core Power

PPVCORE_S0_NB_GFX — 7700 mA

CRITICAL C2210 330UF 20% 2.5V POLY CASE-C2-SM-1

OMIT C2219 10uF 20% 6.3V X5R 603

OMIT C2231 10uF 20% 6.3V X5R 603

OMIT C2232 10uF 20% 6.3V X5R 603

OMIT C2240 2.2UF 20% 6.3V CERM 402-LF

OMIT C2241 2.2UF 20% 6.3V CERM 402-LF

OMIT C2242 2.2UF 20% 6.3V CERM 402-LF

OMIT C2243 2.2UF 20% 6.3V CERM 402-LF

OMIT C2213 10uF 20% 6.3V X5R 603

OMIT C2214 2.2UF 20% 6.3V CERM 402-LF

OMIT C2215 2.2UF 20% 6.3V CERM 402-LF

C2216 0.47UF 10% 6.3V CERM-X5R 402

C2217 0.1UF 10% 6.3V X5R 201

C2218 0.1UF 10% 6.3V X5R 201

PLACEMENT_NOTE=Place in GMCH cavity Place smaller caps as close as possible to NB pins.

NEED TO FIND A "1#GH, 500MA, 78MOHM" INDUCTOR L2220

PP1V8_S0 — 260 mA

1.0UH-0.5A-0.675A 1007

CRITICAL C2220 220UF 20% 2.5V POLY CASE-B2-SM-HF

C2221 1000PF 10% 16V X7R 201

PP1V8_S0_NB_VCCTXLVDS — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.8V — 110 mA

C2223 1000PF 10% 16V X7R 201

Place C2221,C2223 close between J45,L45,J43 and K44

GND

Layout Note: Route to cap, then GND

PP1V8_S0 — 150 mA

C2226 22UF 20% 6.3V CERM 805

Place C2226 close to Pins J47, L47

PP3V3_A_S0

R2242 22K 5% 1/20W MF 201

R2243 22K 5% 1/20W MF 201

R2244 22K 5% 1/20W MF 201

R2245 22K 5% 1/20W MF 201

NO STUFF

GFX_VID<0>

GFX_VID<1>

GFX_VID<2>

GFX_VID<3>

R2247 22K 5% 1/20W MF 201

R2248 22K 5% 1/20W MF 201

R2249 22K 5% 1/20W MF 201

R2250 22K 5% 1/20W MF 201

PP3V3_A_S0 — 10 mA

C2230 0.1UF 10% 6.3V X5R 201

Place C2230 close to Pin L35

CRITICAL U2265 TPS731125 SOT23-5

Vout = 1.204V * (Ra + Rb)/Rb

Ra || Rb should be 19Kohms

WARNING VOLTAGE DROP

PP1V8_S0 — (1.7V - 5.5V) 80 mA

OMIT C2265 1UF 10% 6.3V CERM 402

IN, EN, OUT, NR/FB, GND

PP1V25_S0_NB_DPLL — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.25V

P1V25S0NBDPLL_FB

P1V25S0NBDPLL_RF

OMIT C2266 10UF 20% 6.3V X5R 603

C2267 0.01UF 10% 10V X5R 201

R2266 0.300 5% 1/10W FF 603

80 mA

R2261 0 5% 1/16W MF-LF 402

PP1V25_S0_NB_VCCA_DPLLA — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.25V

C2261 0.1UF 10% 6.3V X5R 201

Place C2261 close to Pin D50

80 mA

R2262 0 5% 1/16W MF-LF 402

OMIT C2260 10uF 20% 6.3V X5R 603

PP1V25_S0_NB_VCCA_DPLLB — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.25V

C2262 0.1UF 10% 6.3V X5R 201

Place C2262 close to Pin J49

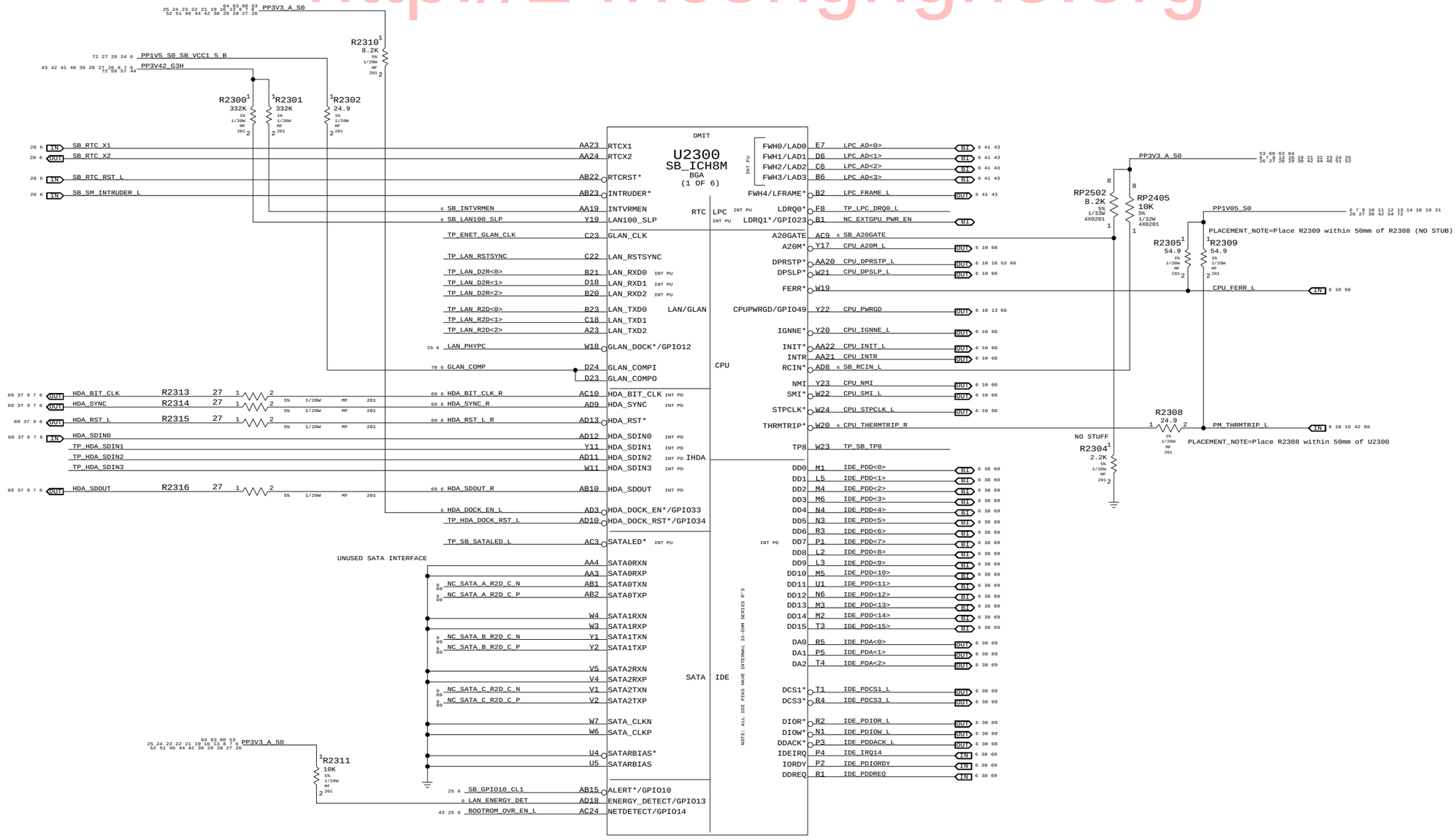
Current numbers from Crestline EDS Addendum, doc #20127.

NB Graphics Decoupling

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 22 OF 73	



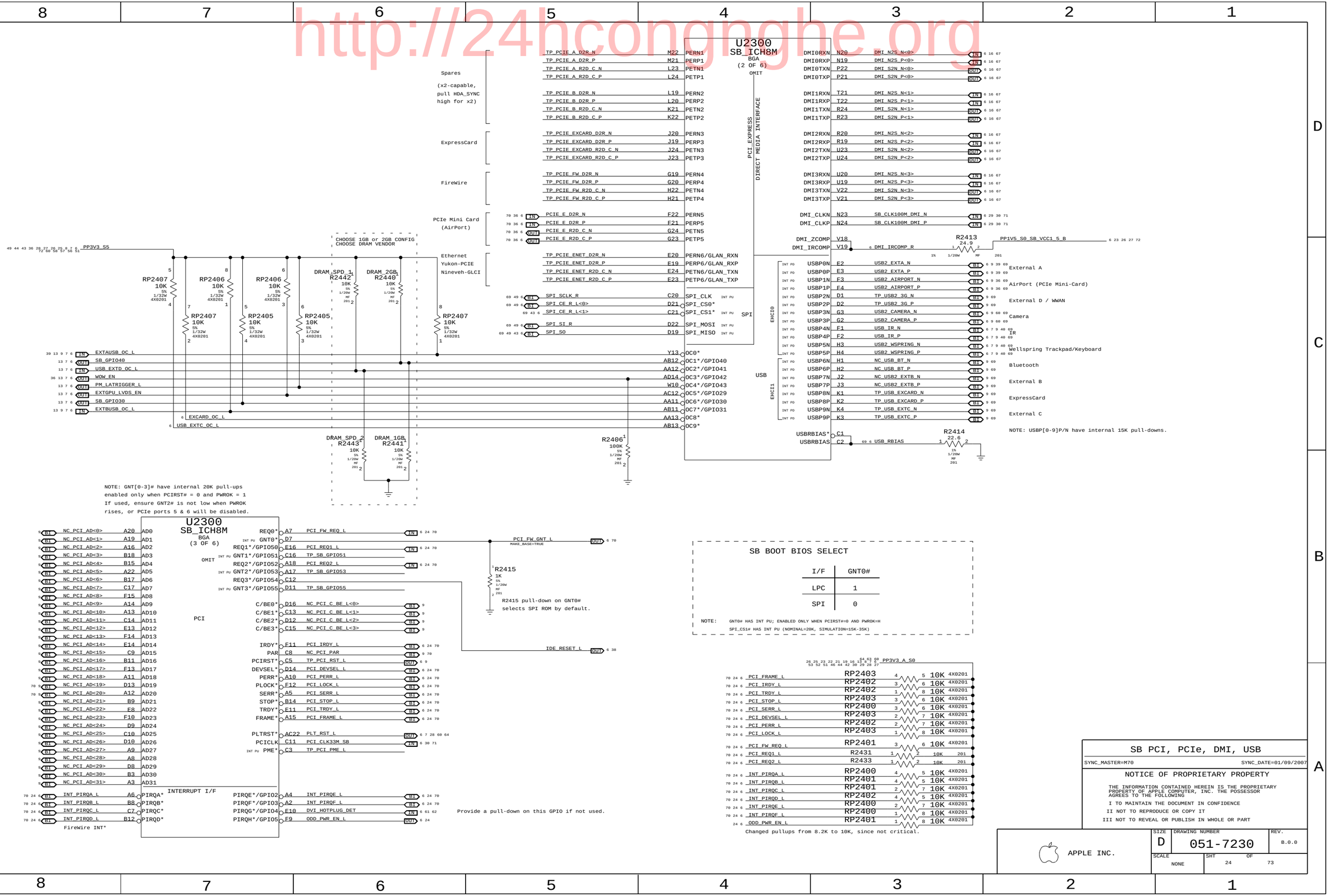
	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 23 OF 73	



SB BOOT BIOS SELECT

I/F	GNT0#
LPC	1
SPI	0

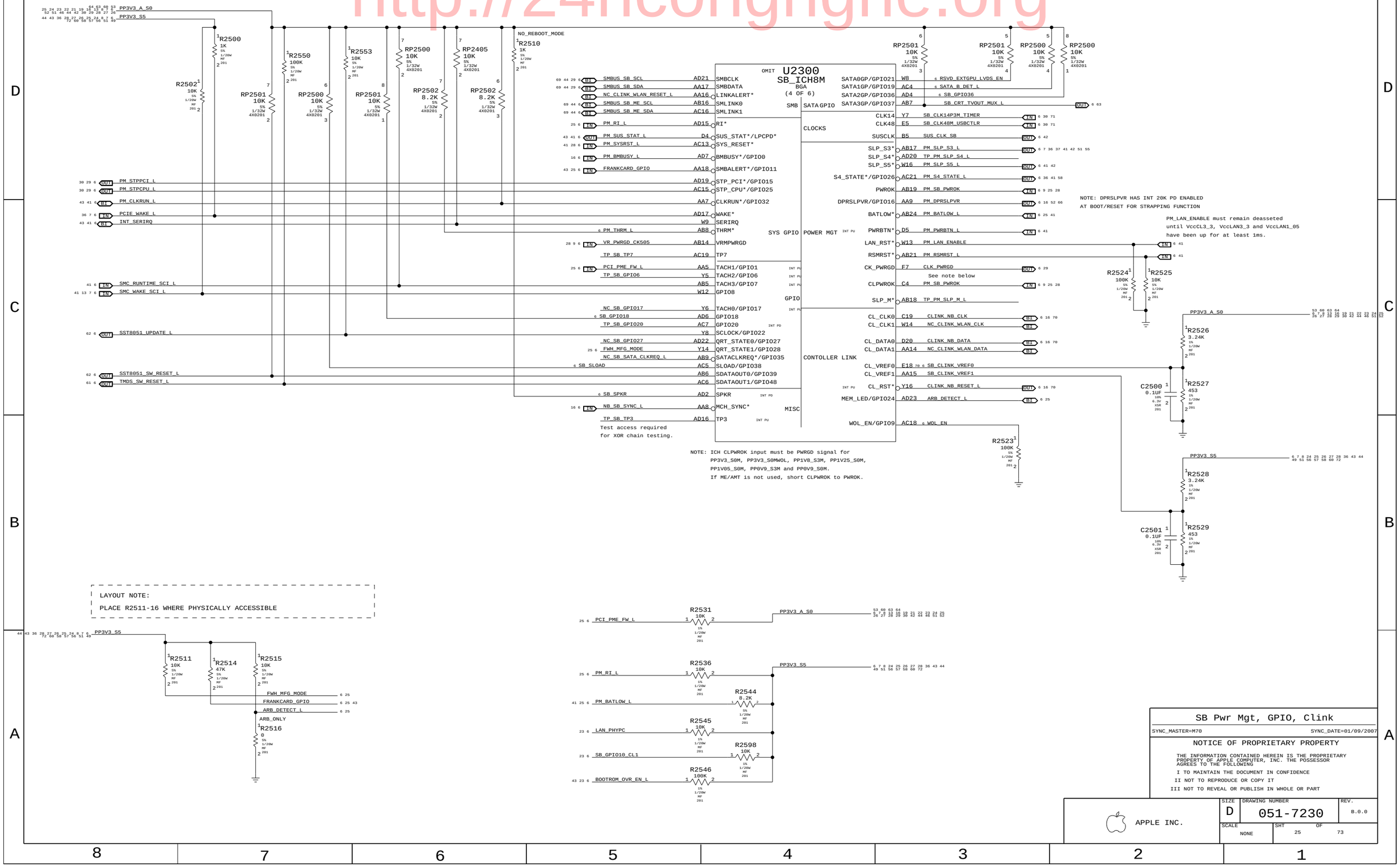
NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

SYNC_MASTER=M70	SYNC_DATE=01/09/2007

SB PCI, PCIe, DMI, USB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 24 OF 73	



SB Pwr Mgt, GPIO, Clink	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

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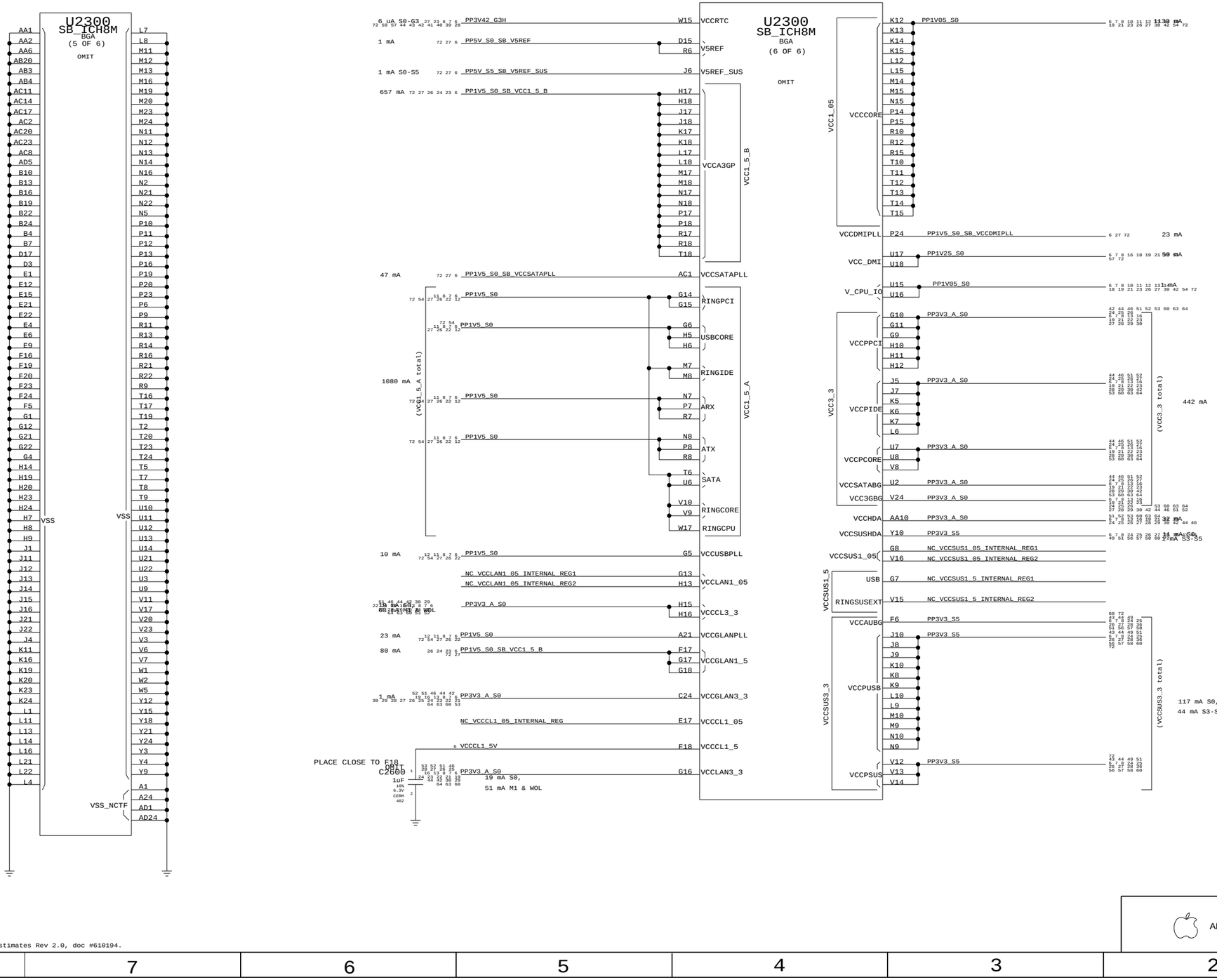
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
	SCALE: NONE	SHT 25 OF 73	



Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

SB Power & Ground

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 26 OF 73	

ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)

PP3V3_A_S0
PP5V_S0
R2702 100 1/20W MF 201 5%
D2702 HN2S02JE SOT-665
PP5V_S0_SB_V5REF
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
OMIT C2703 1UF 10% 6.3V CERM 402

PLACEMENT NOTE:
PLACE C2703 < 2.54MM OF PINS D15,R6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)

PP3V3_S5
PP5V_S5
R2701 10 1/20W MF 201 5%
D2702 HN2S02JE SOT-665
PP5V_S5_SB_V5REF_SUS
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2704 0.1UF 10% 6.3V X5R 201

PLACEMENT NOTE:
PLACE C2704 < 2.54MM OF PIN J6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

L2702 MAY HAVE CHANGE TO 1.0UH PART
L2702 10UH-100MA 0805
PP1V5_S0
PP1V5_S0_SB_VCCSATAPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
OMIT C2735 10UF 20% 6.3V X5R 603
C2717 0.1UF 10% 6.3V X5R 201

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AC1

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
VCCPCORE DOES NOT REQUIRE DECOUPLING PER INTEL RECOMMENDATIONS

COMBINED VCC1_5_A, ARX AND ATX DECOUPLING PER INTEL RECOMMENDATIONS
ICH VCC1_5A/ARX/ATX BYPASS
(ICH LOGIC&IO/[ARX]/[ATX] 1.5V PWR)

PP1V5_S0
PP1V5_S0
PP1V5_S0
C2710 0.1UF 10% 6.3V X5R 201

PLACEMENT NOTE:
PLACE CAP NEAR PINS
T6..U6, N7..R7, N8..R8 OF SB

ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)

PP1V5_S0
CRITICAL L2700 FERR-330-OHM-1.5A 0805-1
PP1V5_S0_SB_VCC1_5_B
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
L2700 MAY HAVE CHANGE TO 0.5UH PART
CRITICAL C2700 220UF 20% 2.5V POLY CASE-B2-HF
OMIT C2705 10UF 20% 6.3V X5R 603
OMIT C2706 10UF 20% 6.3V X5R 603

PLACEMENT NOTE:
PLACE C2700 & C2705-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
DISTRIBUTED BETWEEN H17..T18,
ALSO SHARE WITH F17,G17,G18

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
PP1V5_S0
C2732 2.2uF 20% 6.3V CERM1 603

PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN A21

ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)

PP1V5_S0
C2715 0.1UF 10% 6.3V X5R 201

PLACEMENT NOTE:
PLACE C2715 NEAR PIN G5 OF SB

PP3V3_A_S0
C2738 0.1UF 10% 6.3V X5R 201

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN U2

PP1V5_S0
R2700 1 5% 1/20W MF 201
L2703 1.0UH-0.5A-0.675A 1007
PP1V5_S0_SB_VCCDMIPLL_F
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.20MM
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
C2701 0.01UF 10% 10V X5R 201
OMIT C2708 10UF 20% 6.3V X5R 603

PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY NEAR PIN P24

PP3V3_A_S0
PLACEMENT NOTE:
PLACE CAP < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN V24
C2737 0.1UF 10% 6.3V X5R 201

PP1V25_S0
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN U17,U18
C2739 1UF 10% 10V X5R 402-1

ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)

PP3V42_G3H
PP1V5_S0_SB_VCC1_5_B
MAKE_BASE=TRUE
PP1V5_S0_SB_VCC1_5_B
C2744 1UF 10% 10V X5R 402-1
C2729 0.1UF 10% 6.3V X5R 201
C2730 0.1UF 10% 6.3V X5R 201

PLACEMENT NOTE:
PLACE CAPS NEAR PIN W15 OF SB

PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
PLACE C2718,C2702 NEAR SB K12..T15

ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)

PP1V05_S0
C2718 0.022UF 10% 6.3V X5R 201
C2702 0.022UF 10% 6.3V X5R 201
CRITICAL C2716 330UF 20% 2.5V POLY CASE-C2-HF

PLACEHOLDER FOR 270UF

ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)

PP3V3_A_S0
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PIN G16
C2719 0.1UF 10% 6.3V X5R 201

ICH VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V/1.5V PWR)

PP3V3_A_S0
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AA10
C2721 0.1UF 10% 6.3V X5R 201

ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)

PP1V05_S0
PLACEMENT NOTE:
PLACE NEAR PINS U15,U16 OF SB
C2723 0.1UF 10% 6.3V X5R 201
C2722 0.1UF 10% 6.3V X5R 201
C2724 4.7UF 20% 6.3V CERM 603

ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)

PP3V3_A_S0
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS J5..L6
C2725 0.1UF 10% 6.3V X5R 201

ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)

PP3V3_A_S0
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS G9..H12
C2726 0.1UF 10% 6.3V X5R 201
C2727 0.1UF 10% 6.3V X5R 201
C2728 0.1UF 10% 6.3V X5R 201

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)

PP3V3_S5
PLACEMENT NOTE:
PLACE CAP NEAR PINS
V12..V14 AND F6
C2731 0.1UF 10% 6.3V X5R 201

ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)

PP3V3_S5
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
J10..N9
C2734 0.1UF 10% 6.3V X5R 201
C2733 0.022UF 10% 6.3V X5R 201

ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)

PP1V5_S0
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS G6..H6
C2712 0.1UF 10% 6.3V X5R 201

VCCCL3_3 DOES NOT REQUIRE DECOUPLING PER INTEL RECOMMENDATIONS

ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)

PP3V3_S5
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN Y10
C2741 0.1UF 10% 6.3V X5R 201

SB Decoupling

SYNC_MASTER=M70 SYNC_DATE=02/01/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 27 OF 73	

Platform Reset Connections

Unbuffered

PP3V42_G3H

R2800 20K 5% 1/20W MF 201

C2805 1UF 10% 6.3V X5R 402 (OMIT)

R2806 1M 5% 1/20W MF 201

SB_RTC_RST_L (OUT)

SB_SM_INTRUDER_L (OUT)

PLT_RST_L (IN) MAKE_BASE=TRUE

R2886 100 5% 1/20W MF 201 — NB_RESET_L

R2887 0 5% 1/20W MF 201 — TMDS_HW_RESET_L

R2885 0 5% 1/20W MF 201 — AIRPORT_RST_L

PLT_RST_L

PLT_RST_L

Buffered

PP3V3_A_S0

CRITICAL U2880 TC7SZ08AFEF SOT665

C2880 0.1UF 10% 6.3V X5R 201

R2880 100K 5% 1/20W MF 201

PLT_RST_BUF_L

R2881 0 5% 1/20W MF 201 — DEBUG_RESET_L

Linda Card represents 3 loads

R2883 100 5% 1/20W MF 201 — SMC_LRESET_L

SB RTC Crystal Circuit

SB_RTC_X1

R2810 0 5% 1/20W MF 201

SB_RTC_X1_R

R2809 10M 5% 1/20W MF1 201

CRITICAL Y2800 32.768K 3.2X1.5X.6-SM 197S0187

C2808 10PF 5% 25V C0G 201

C2809 10PF 5% 25V C0G 201

SB_RTC_X2

PP3V3_S5

R2897 10K 5% 1/20W MF 201

R2896 1K 5% 1/20W MF 201

XDP_DBRESET_L (IN)

PM_SYSRST_L

PM_SYSRST_L (OUT) MAKE_BASE=TRUE

R2898 100K 5% 1/10W MF-LF 402 (OMIT)

This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

Place R2898 pads on bottom side near board edge

PP3V3_A_S0

C2811 0.1UF 10% 6.3V X5R 201

CRITICAL U2803 TC7SH00FEF SON

VCC GND

VR_PWRGD_CK505 (OUT)

R2803 100K 5% 1/20W MF 201

VR_PWRGD_CK505_L (IN) MAKE_BASE=TRUE

VR_PWRGD_CK505_L (OUT)

PP3V3_A_S0

C2807 0.1UF 10% 6.3V X5R 201

R2811 1.8K 5% 1/20W MF 201

CRITICAL U2801 TC7SZ08AFEF SOT665

PM_SB_PWROK (OUT)

R2812 10K 5% 1/20W MF 201

VR_PWRGOOD_DELAY (IN)

ALL_SYS_PWRGD (IN)

SB Misc

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	28	73

Silego recommend to remove L2903,R2900,C2907,C2910
R2901,L2902,C2916,C2911,C2914 and R2902

PP3V3_A_S0

CRITICAL
L2901
FERR-120-OHM-1.5A
0402-LF
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V

PP3V3_S0_CK505_VDD_CPU_SRC

OMIT C2900 1UF 10% 6.3V CERM 402

OMIT C2901 10UF 20% 6.3V X5R 603

C2902 0.1UF 10% 6.3V X5R 201
C2903 0.1UF 10% 6.3V X5R 201
C2904 0.1UF 10% 6.3V X5R 201
C2905 0.1UF 10% 6.3V X5R 201
C2906 0.1UF 10% 6.3V X5R 201

C2908 0.1UF 10% 6.3V X5R 201

C2909 0.1UF 10% 6.3V X5R 201

C2912 0.1UF 10% 6.3V X5R 201
C2913 0.1UF 10% 6.3V X5R 201

C2915 0.1UF 10% 6.3V X5R 201

(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

CRITICAL
Y2901
SM-2.5X2.0MM
14.318MHZ-35PPF-20PF

C2989 20PF 5% 25V NP0-C0G 201
C2990 20PF 5% 25V NP0-C0G 201

CK505_XTAL_IN
CK505_XTAL_OUT

PP3V3_A_S0

R2903 10K 5% 1/20W MF 201

(FW PCI 33MHZ)
(TPM LPC 33MHZ)
(SMC LPC 33MHZ)
(PCI SLOT)
(PORT80 LPC 33MHZ)

CK505_PCIF0_CLK

(ICH8M PCI 33MHZ) CK505_PCIF1_CLK

(PULL UP PIN 68 TO ENABLE ITP HOST CLK)

(ICH SM BUS) SMBUS_SB_SCL, SMBUS_SB_SDA

U2900
SLG2AP101
QFN

3	VDD_48			
43	VDD_CPU			
61	VDD_PCI			
67	VDD_REF			
49				
12				
17				
28				
35	VDD_SRC			
38	VDD_A			
39	VSS_A			
51	XTAL_IN			
50	XTAL_OUT			
8	FS_B/TEST_MODE	CK505_FSB_TEST_MODE	IN	
57	PCI_1	NC_CK505_PCI1_CLK	OUT	(FW PCI 33MHZ)
58	PCI_2	NC_CK505_PCI2_CLK	OUT	(TPM LPC 33MHZ)
63	PCI_3	CK505_PCI3_CLK	OUT	(SMC LPC 33MHZ)
64	PCI_4	NC_CK505_PCI4_CLK	OUT	(PCI SLOT)
65	PCI_5/FCI_SEL	CK505_PCI5_FCTSEL1	BI	(PORT80 LPC 33MHZ)
68	PCIF_0/ITP_EN			(NO INT PD) (INT PU)
1	PCIF_1	CK505_PCIF1_CLK	OUT	(NO INT PU) (ICH8M PCI 33MHZ)
47	SCL	SMBUS_SB_SCL	IN	(ICH SM BUS)
48	SDA	SMBUS_SB_SDA	BI	(ICH SM BUS)
5	VSS_48			
46	VSS_CPU			
62				
66	VSS_PCI			
52	VSS_REF			
31	VSS_SRC			
69	THRM_PAD			
56	PCI_STOP*	PM_STPPCI_L	IN	(FROM ICH8M GPIO15 STPPCI*)
55	CPU_STOP*	PM_STPCPU_L	IN	(FROM ICH8M GPIO25 STPCPU*)
44	CPU_0*	FSB_CLK_CPU_N	OUT	(CPU HOST 133/167MHZ)
45	CPU_0	FSB_CLK_CPU_P	OUT	(CPU HOST 133/167MHZ)
41	CPU_1_MCH*	FSB_CLK_NB_N	OUT	(GMCH HOST 133/167MHZ)
42	CPU_1_MCH	FSB_CLK_NB_P	OUT	(GMCH HOST 133/167MHZ)
36	CPU_ITP*/SRC_10*	XDP_CLK_N	OUT	(ITP HOST 133/167MHZ)
37	CPU_ITP/SRC_10	XDP_CLK_P	OUT	(ITP HOST 133/167MHZ)
11	SRC_0*/LCD_CLK*	NB_CLK100M_DPLLSS_N	OUT	(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
10	SRC_0/LCD_CLK	NB_CLK100M_DPLLSS_P	OUT	(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
14	SRC_1*	NC_CK505_SRC1_N	OUT	(SLOT F - GPU PCI-E 100 MHZ)
13	SRC_1	NC_CK505_SRC1_P	OUT	(SLOT F - GPU PCI-E 100 MHZ)
9	CLKREQ_1*	NC_CK505_SRC_CLKREQ1_L	IN	(INT PU)
16	SRC_2*	SB_CLK100M_DMI_N	OUT	(ICH8M DMI 100 MHZ)
15	SRC_2	SB_CLK100M_DMI_P	OUT	(ICH8M DMI 100 MHZ)
19	SRC_3*	NC_CK505_SRC3_N	OUT	(SLOT D - 4 LANE PCI-E FOR EXPRESSCARD)
18	SRC_3	NC_CK505_SRC3_P	OUT	(SLOT D - 4 LANE PCI-E FOR EXPRESSCARD)
59	CLKREQ_3*	NC_CK505_SRC_CLKREQ3_L	IN	(INT PU)
22	SRC_4*	NC_CK505_SRC4_N	OUT	(ICH SATA 100 MHZ) (FROM ICH8M GPIO35)
21	SRC_4	NC_CK505_SRC4_P	OUT	(ICH SATA 100 MHZ) (FROM ICH8M GPIO35)
20	CLKREQ_4*	NC_CK505_SRC_CLKREQ4_L	IN	(INT PU)
24	SRC_5*	NB_CLK100M_PCIE_N	OUT	(GMCH G_CLKIN 100 MHZ) (FROM GMCH CLK_REQ*)
23	SRC_5	NB_CLK100M_PCIE_P	OUT	(GMCH G_CLKIN 100 MHZ) (FROM GMCH CLK_REQ*)
60	CLKREQ_5*	NB_CLKREQ_L	IN	(INT PU)
27	SRC_6*	PCIE_CLK100M_MINI_N	OUT	(WIRELESS PCI-E 100 MHZ)
26	SRC_6	PCIE_CLK100M_MINI_P	OUT	(WIRELESS PCI-E 100 MHZ)
25	CLKREQ_6*	CK505_SRC_CLKREQ6_L	IN	(INT PU)
30	SRC_7*	NC_CK505_SRC7_N	OUT	(DB400 SRC)
29	SRC_7	NC_CK505_SRC7_P	OUT	(DB400 SRC)
40	CLKREQ_7*	NC_CK505_PGMODE		(INT PU)
32	SRC_8*	NC_CK505_SRC8_N	OUT	(SLOT E)
33	SRC_8	NC_CK505_SRC8_P	OUT	(SLOT E)
34	CLKREQ_8*	NC_CK505_SRC_CLKREQ8_L	IN	(INT PU)
7	DOT_96*/27M_SS	NB_CLK96M_DOT_N	OUT	(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
6	DOT_96/27M	NB_CLK96M_DOT_P	OUT	(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
2	CKPWRGD/PD*	CLK_PWRGD	IN	(INT PD)
4	48M/FS_A	CK505_USB48_FSA	OUT	(FROM ICH8M)
54	REF_0/FS_C/TEST_SEL	CK505_CLK14P3M_TIMER	OUT	(ICH8M USB 48MHZ)
53	GPU_STOP*	NC_GPU_STOP_L	BI	(ICH8M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
1	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM

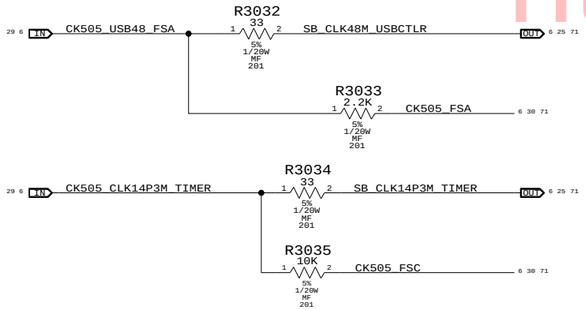
Clock (CK505)

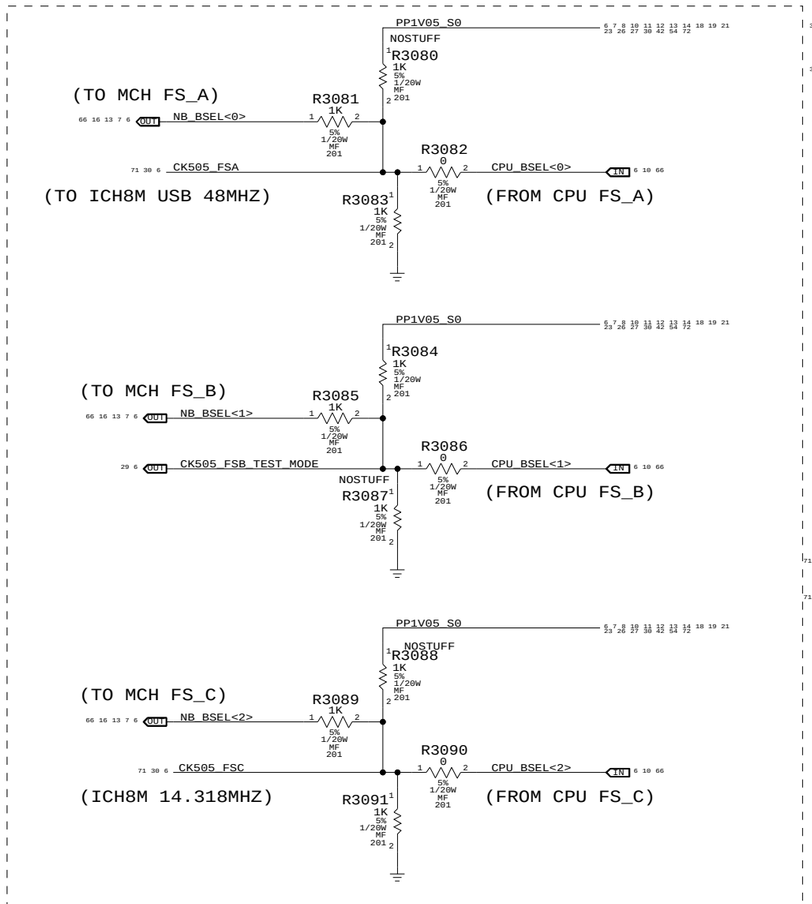
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 29 OF 73	

CLK Termination

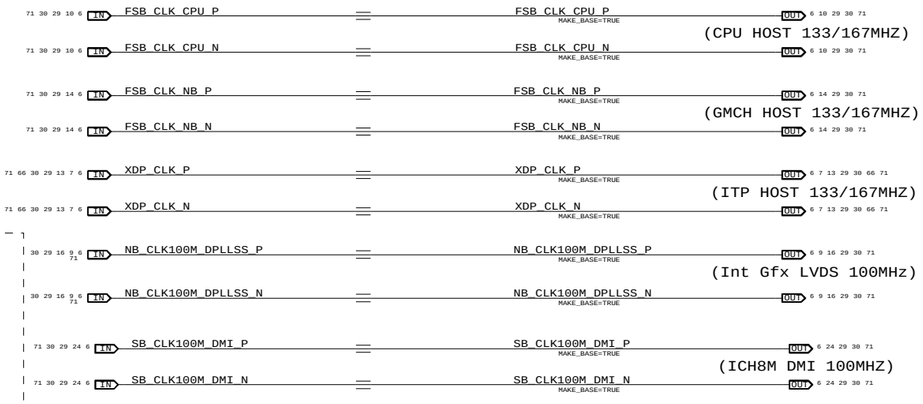


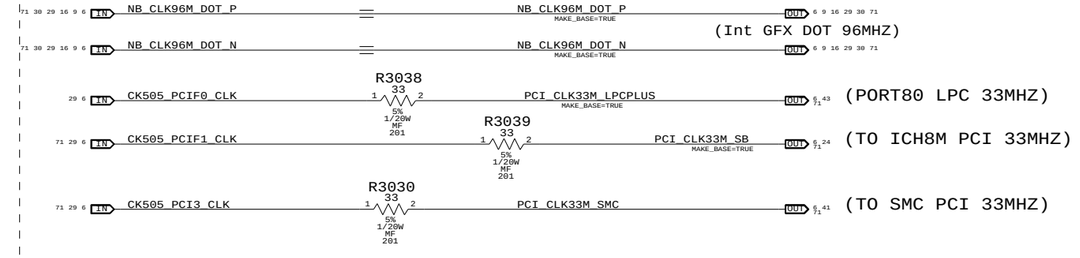


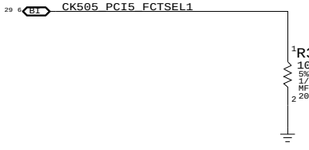
	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
	0	0	1	133M
	0	1	1	166M
*	0	1	0	200M
	1	1	0	400M
	1	1	1	Resrvd
	1	0	1	100M
	1	0	0	333M

NOSTUFF R3082, R3086, R3090
FOR MANUAL CPU FREQUENCY

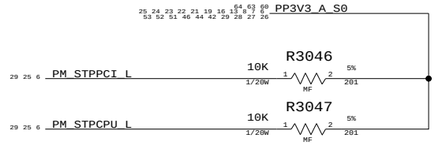
CPU speed is currently set to 200MHz







CLKREQ Controls



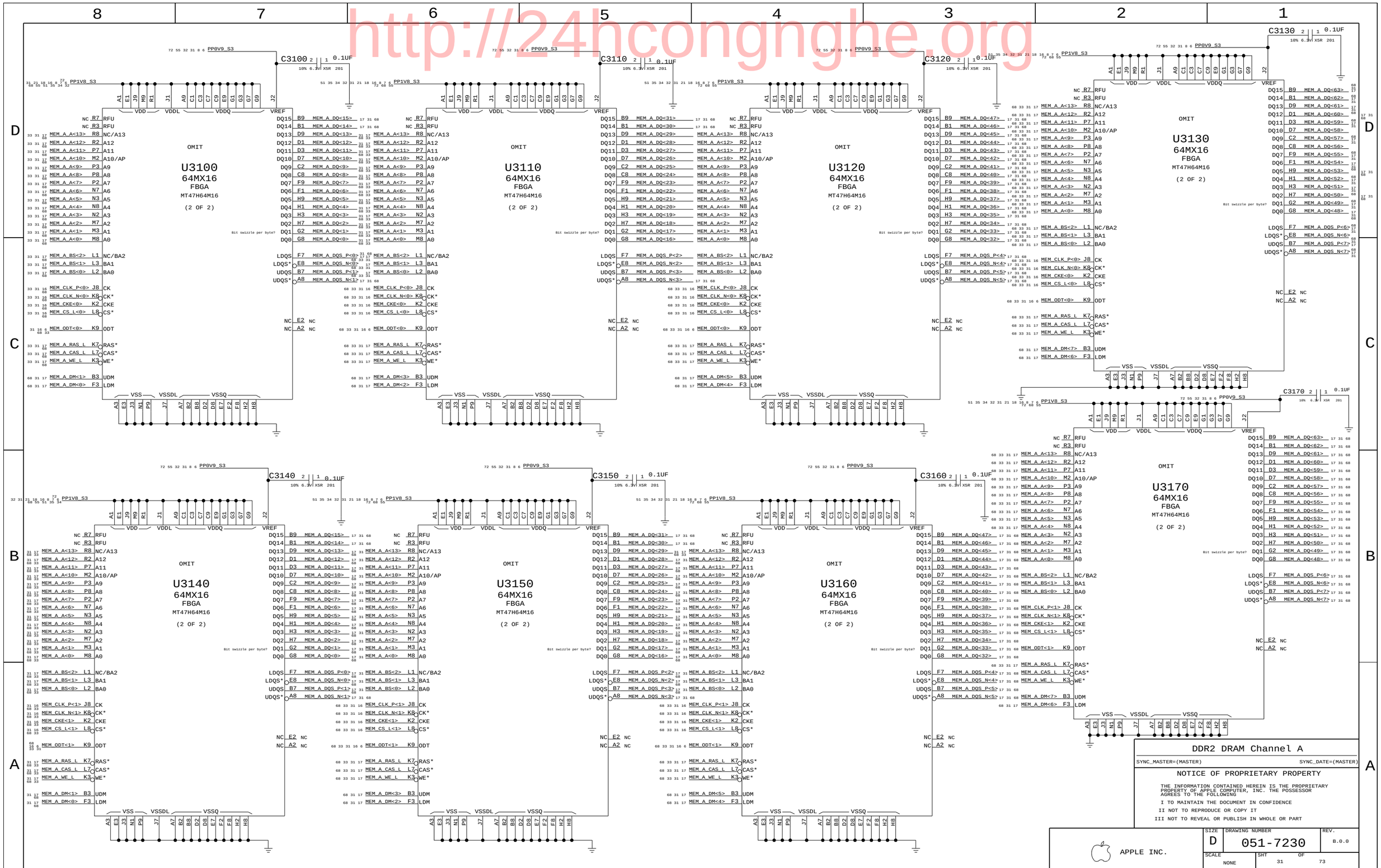
Clock Termination

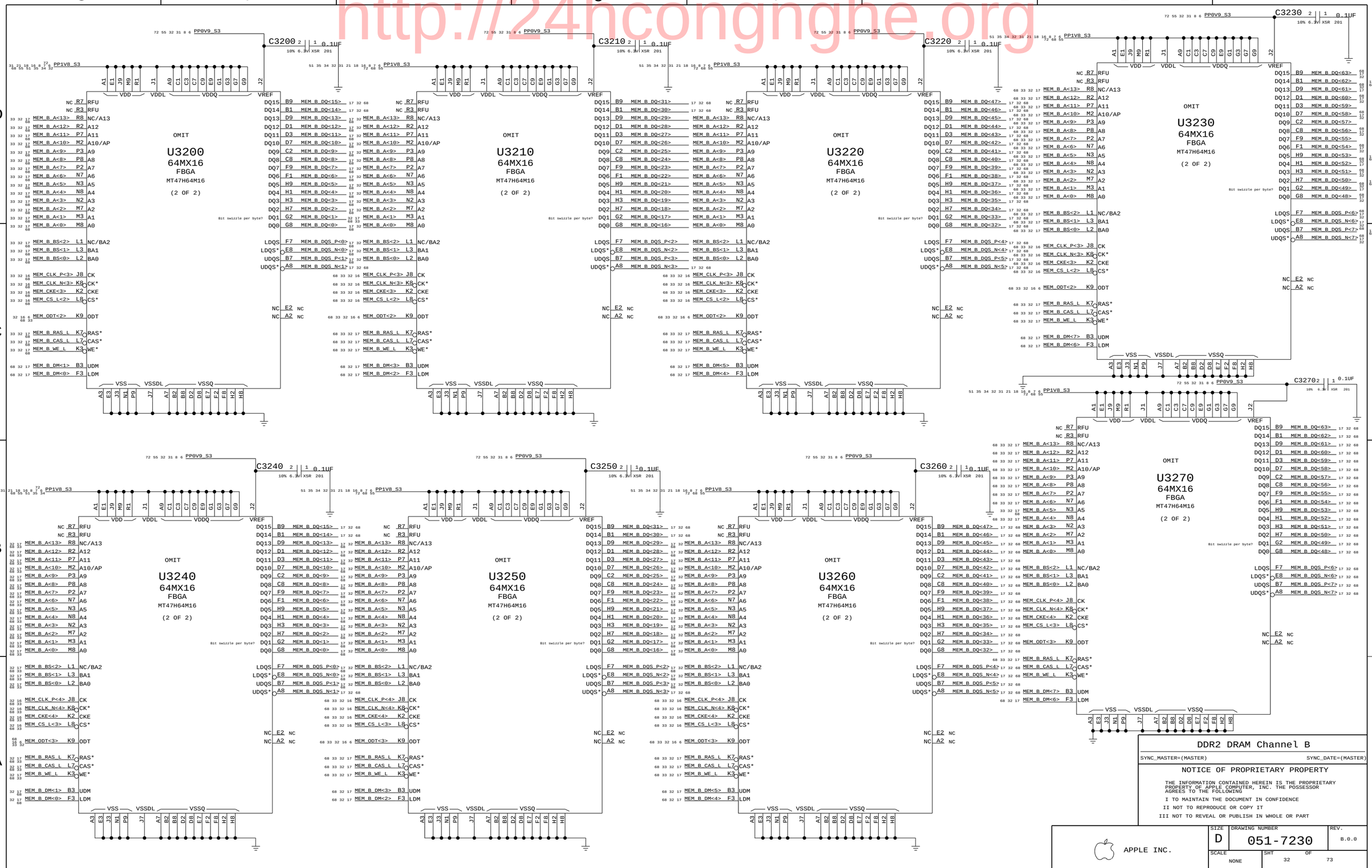
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	30	73





DDR2 DRAM Channel B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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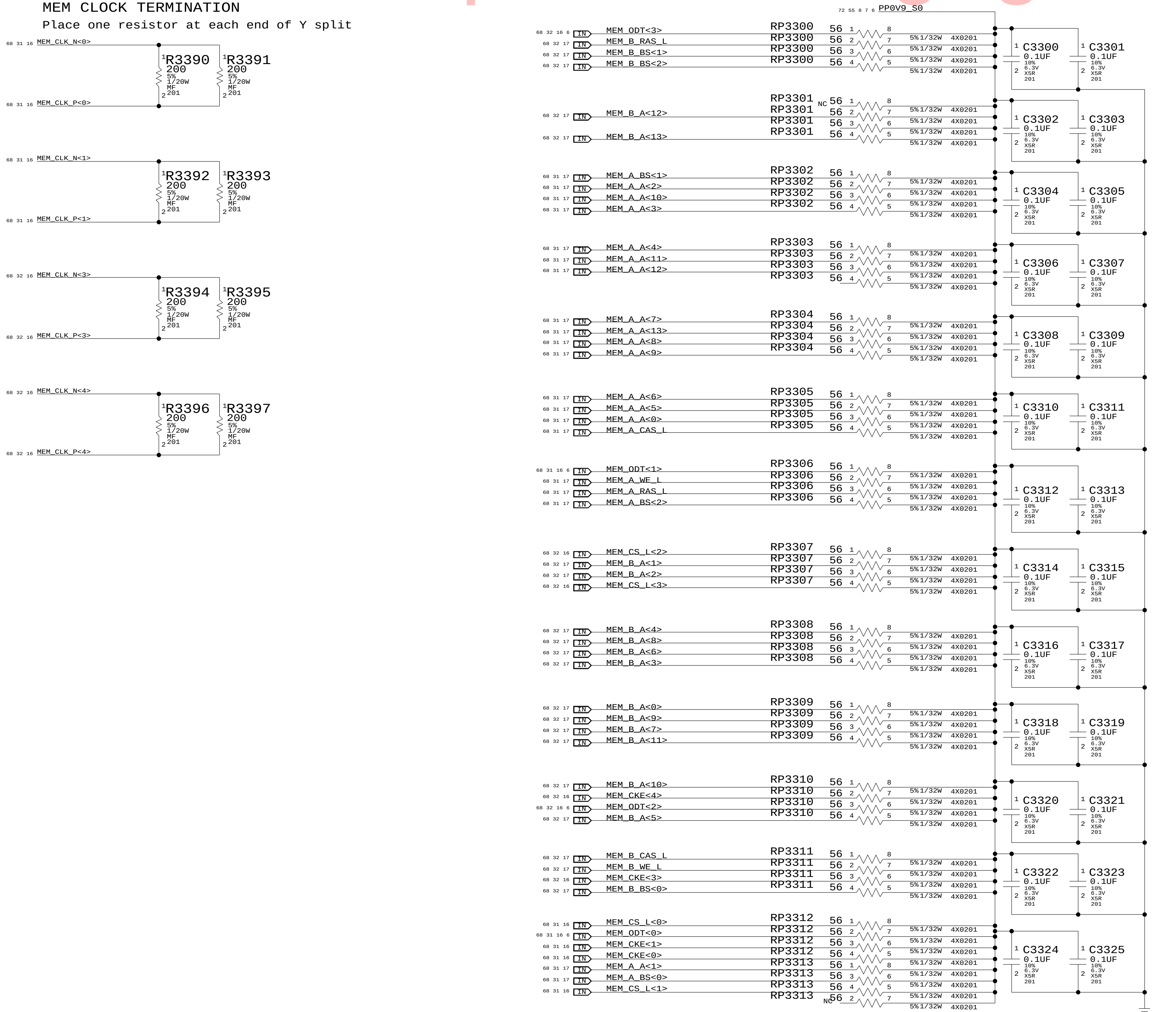
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 32 OF 73	

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it

MEM CLOCK TERMINATION

Place one resistor at each end of Y split

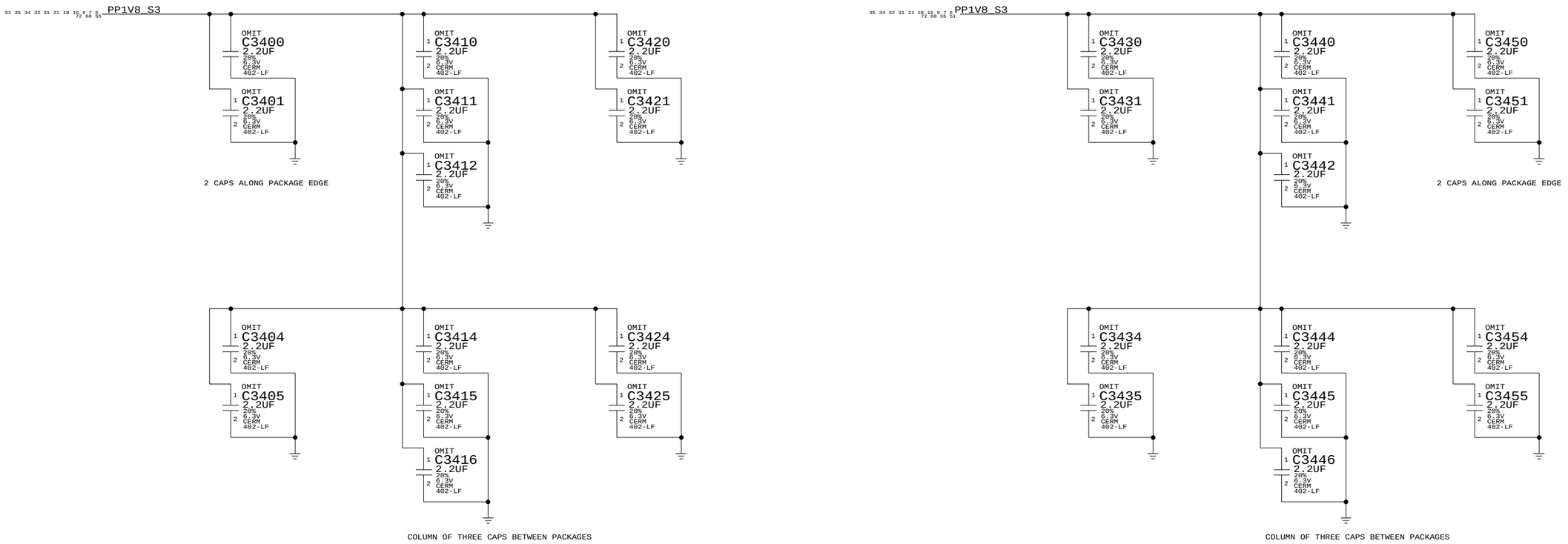


LAYOUT NOTE:PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED
TO PP0V9_S0_MEM_TERM

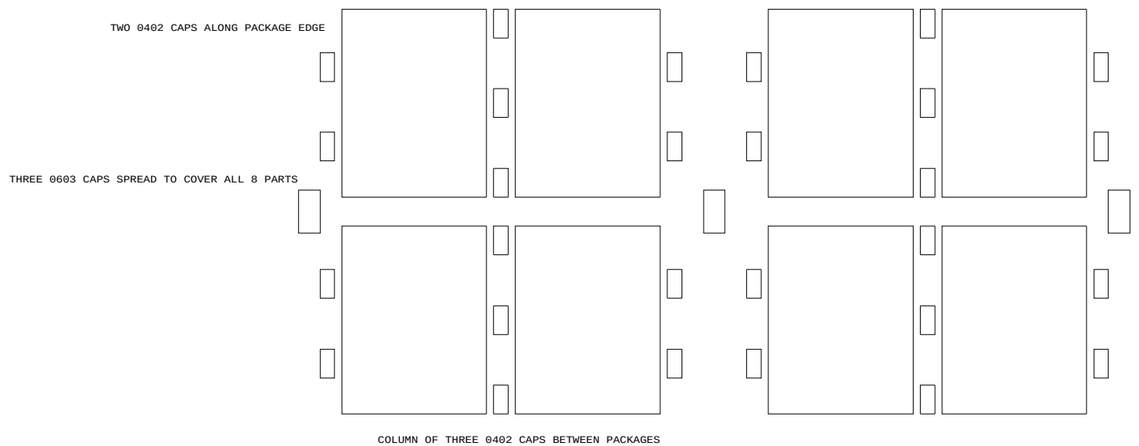
Memory Active Termination

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 33	OF 73



APPROXIMATE CAP ARRANGEMENT

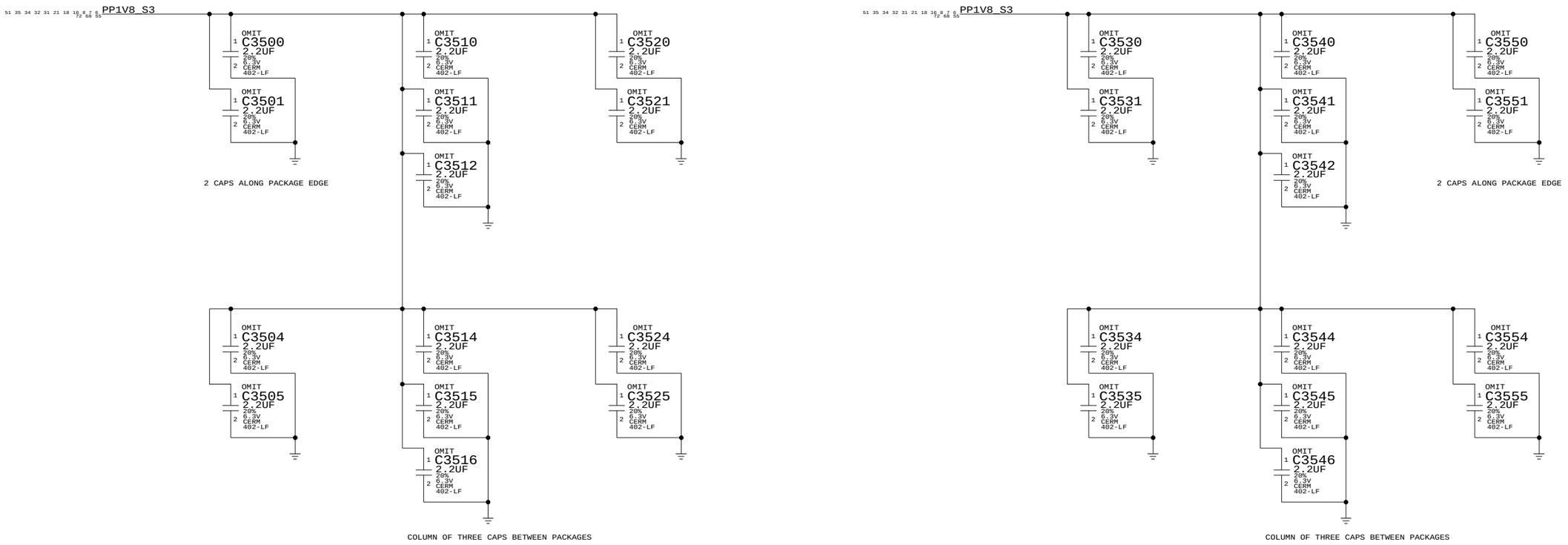


DDR2 BYPASSING 1

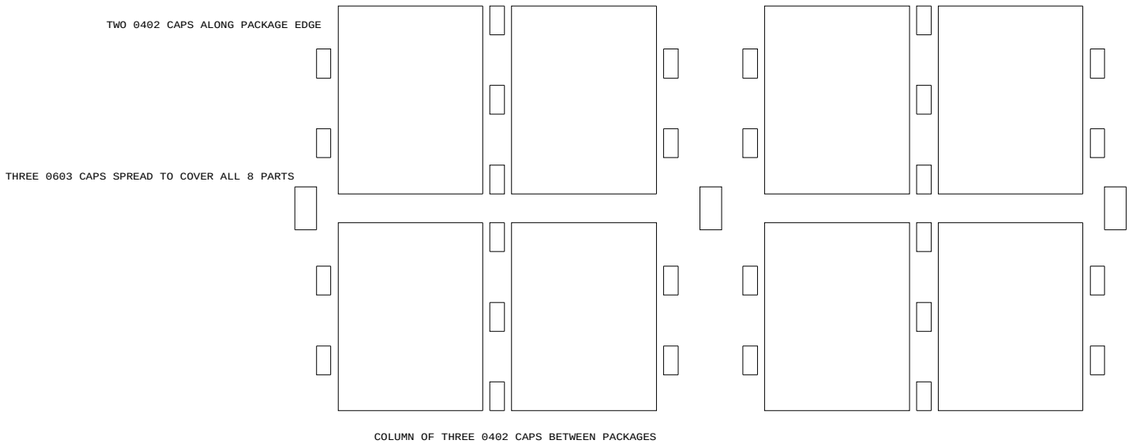
SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 34 OF 73	



APPROXIMATE CAP ARRANGEMENT



DDR2 BYPASSING 2

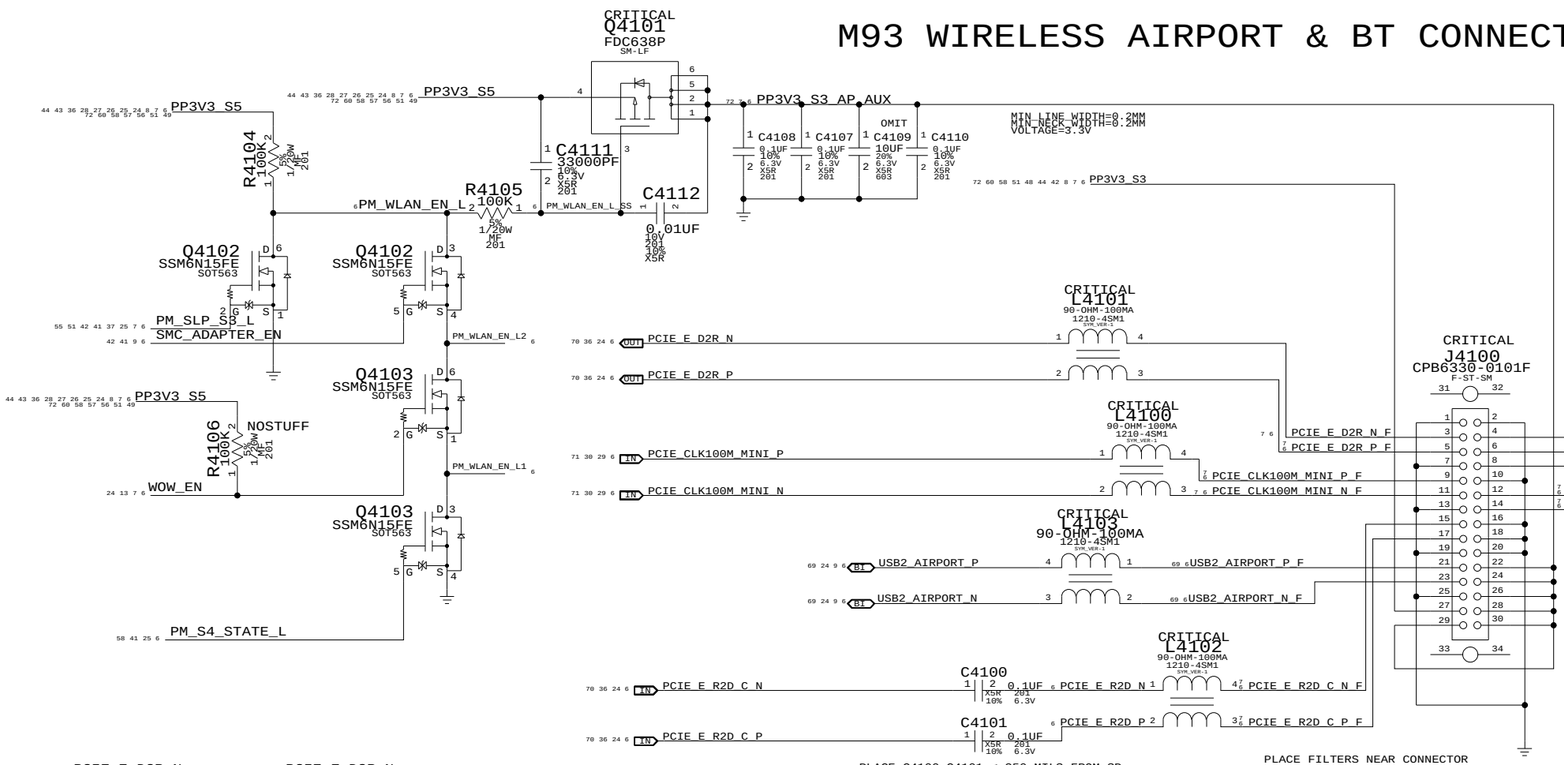
SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	35	73

M93 WIRELESS AIRPORT & BT CONNECTOR



PCIE_E_D2R_N — PCIE_E_D2R_N — MAKE_BASE=TRUE
PCIE_E_D2R_P — PCIE_E_D2R_P — MAKE_BASE=TRUE
PCIE_E_R2D_C_N — PCIE_E_R2D_C_N — MAKE_BASE=TRUE
PCIE_E_R2D_C_P — PCIE_E_R2D_C_P — MAKE_BASE=TRUE

PLACE C4100,C4101 < 250 MILS FROM SB

PLACE FILTERS NEAR CONNECTOR

APN:516S0580

Wireless M93 Connector

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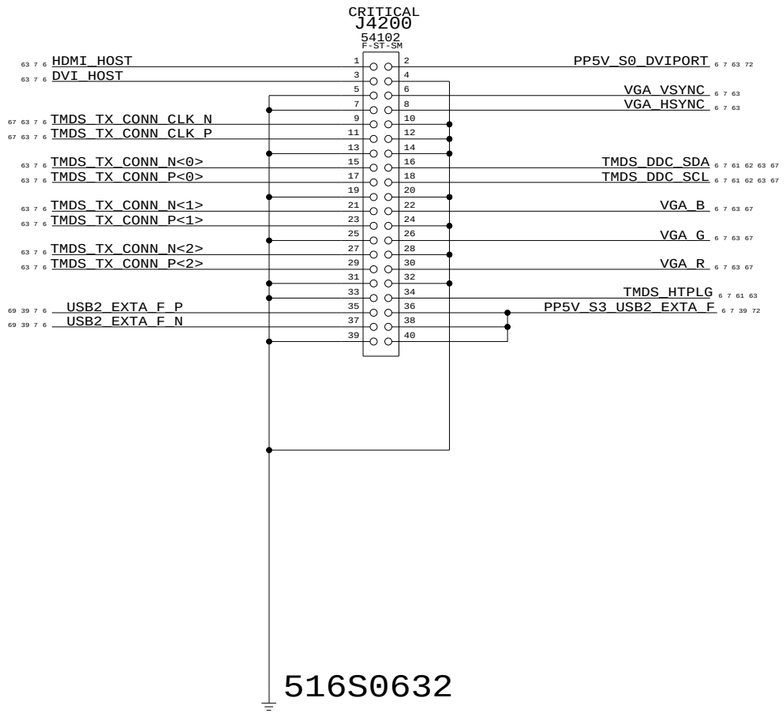
APPLE INC.

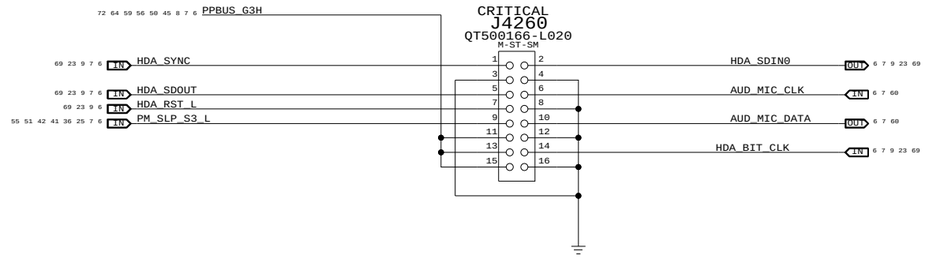
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 36 OF 73	

Micro DVI, USB, to RIO Hatch Assembly



516S0632

Audio Connector



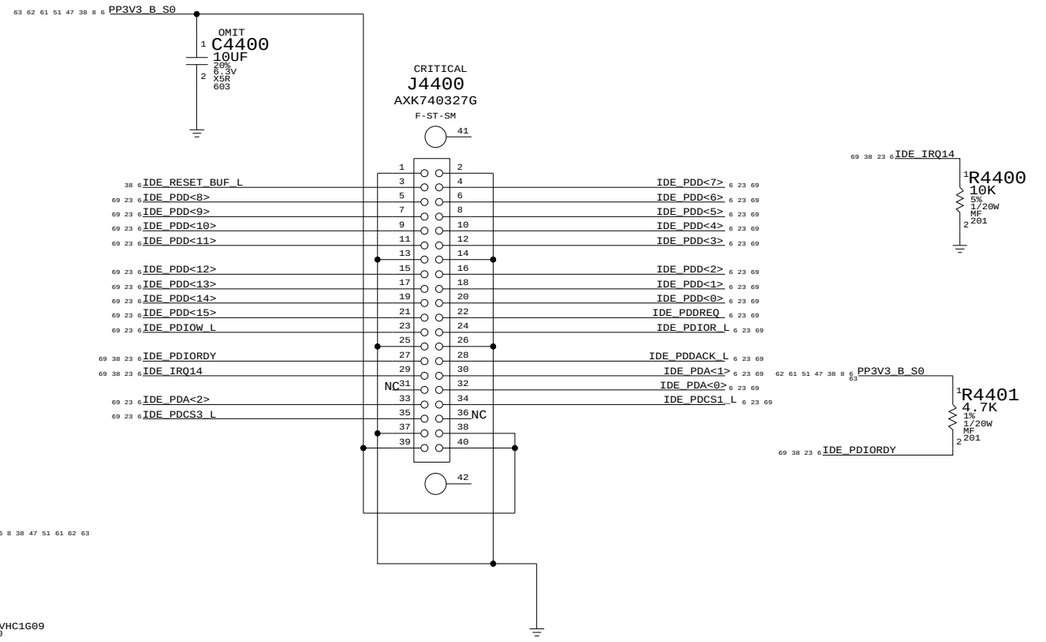
516S0350

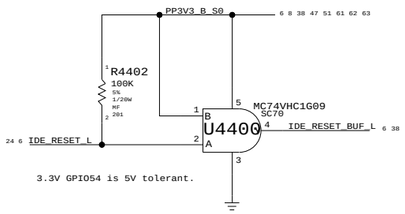
Hatch and Audio Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 37 OF 73	





516S0594

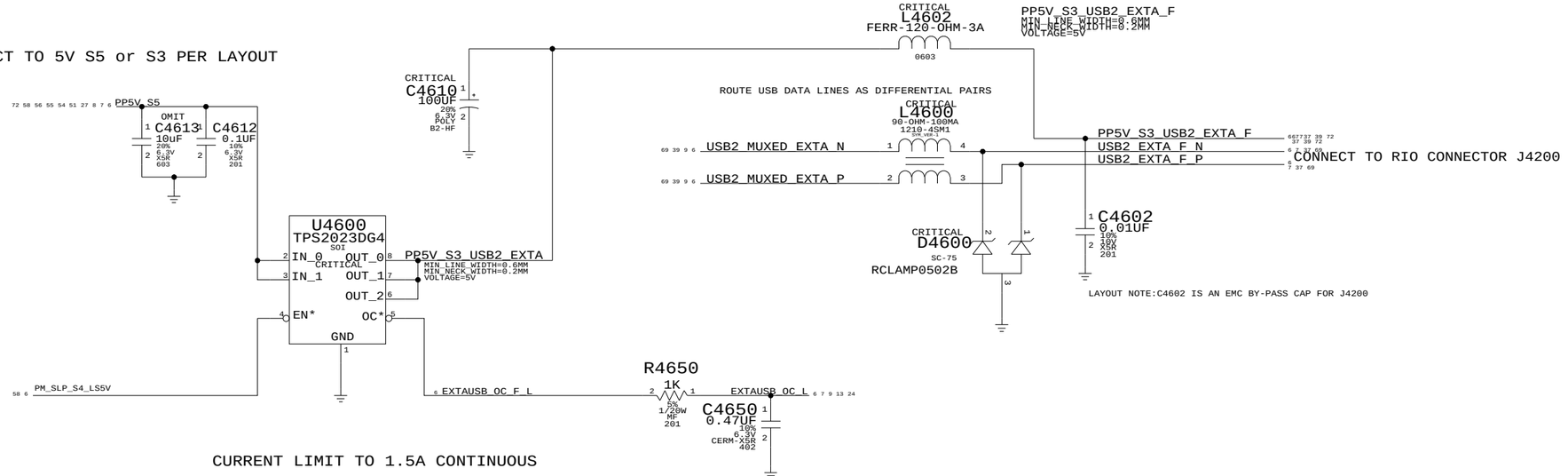
PATA HDD CONNECTOR

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 38 OF 73	

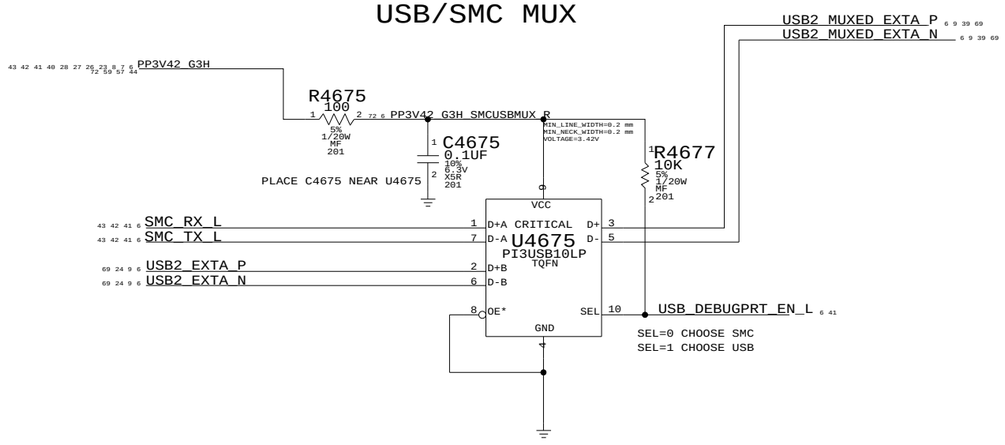
USB 2.0 CONNECTOR

CONNECT TO 5V S5 or S3 PER LAYOUT



CURRENT LIMIT TO 1.5A CONTINUOUS

USB/SMC MUX



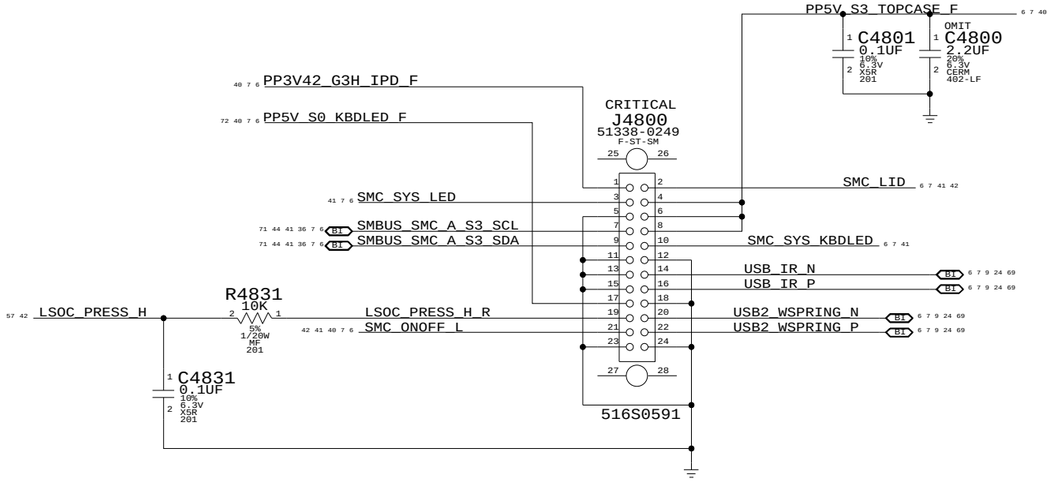
USB EXTERNAL CONNECTORS

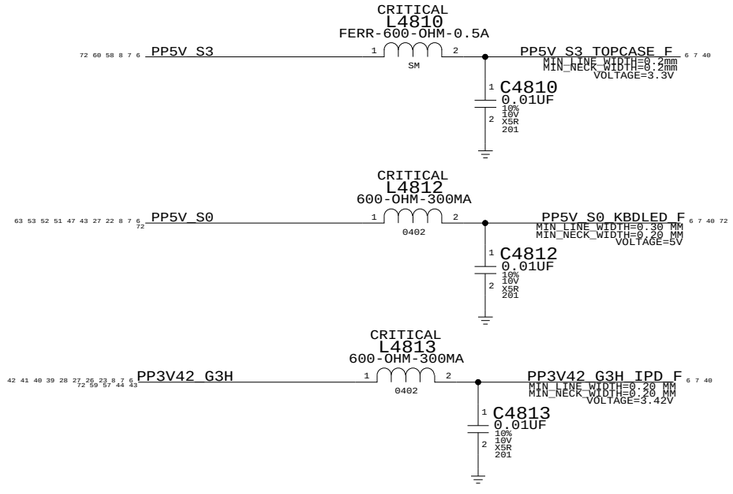
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

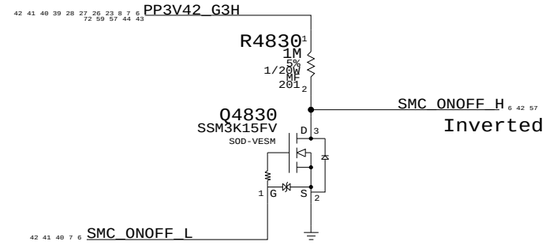
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 39 OF 73	

IPD Connector





Power Button Inverter



IPD Connector

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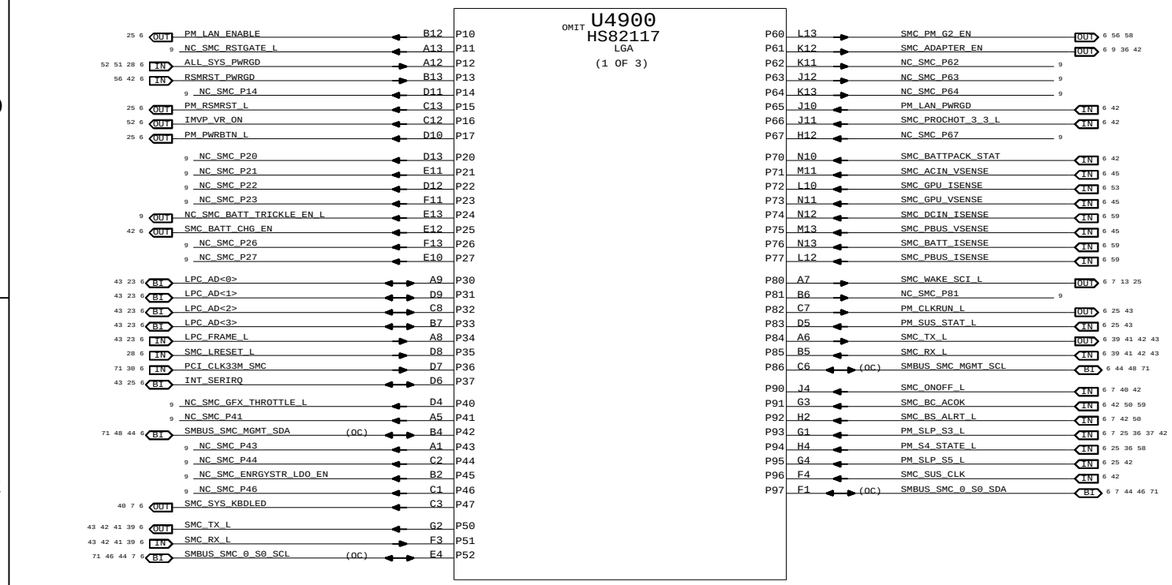
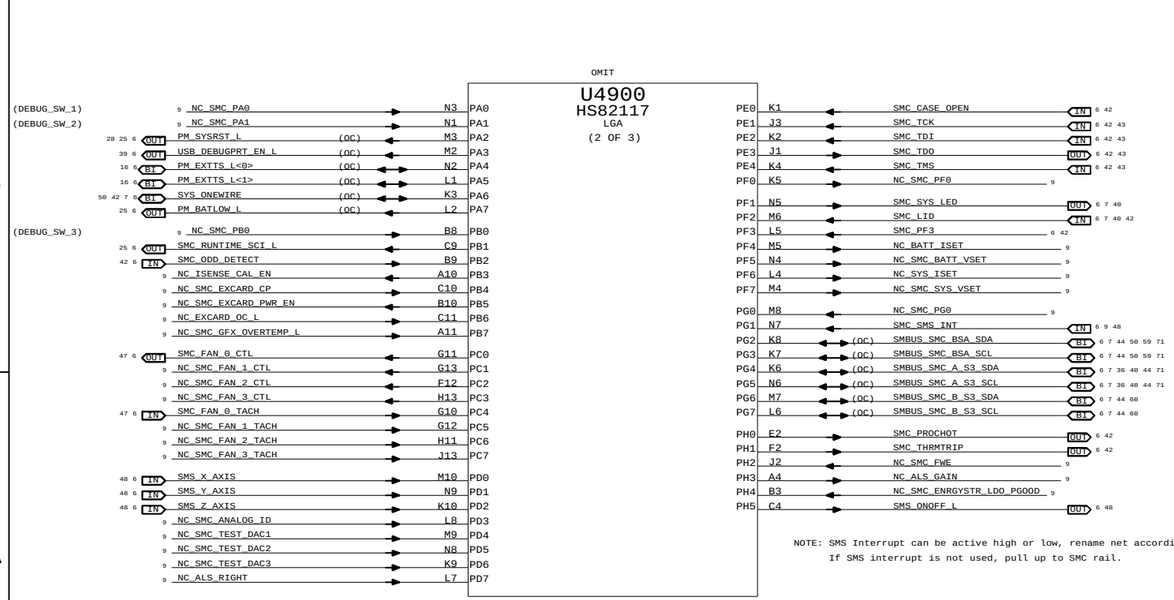
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 40 OF 73	

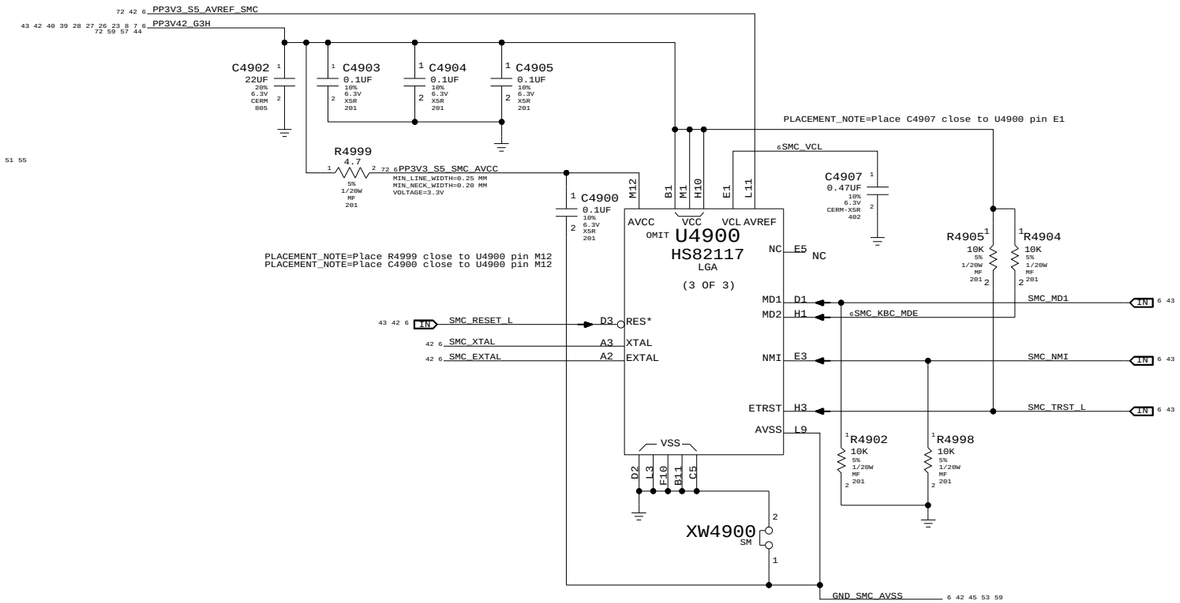
SMC

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SMC		
SYNC_MASTER=M70	SYNC_DATE=01/09/2007	
NOTICE OF PROPRIETARY PROPERTY		
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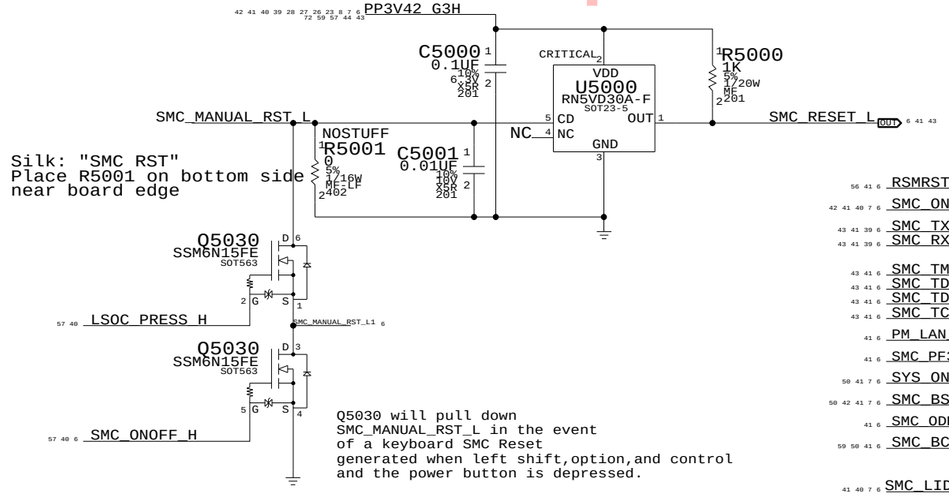
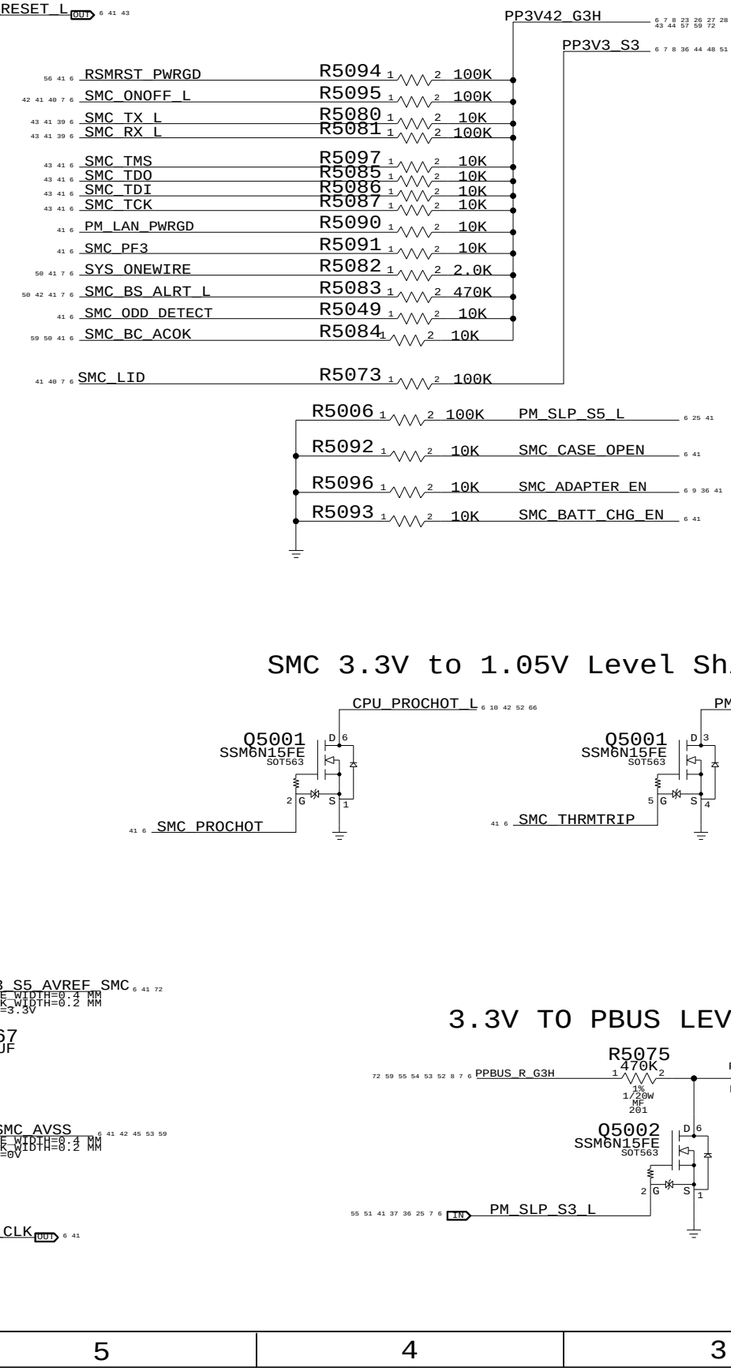
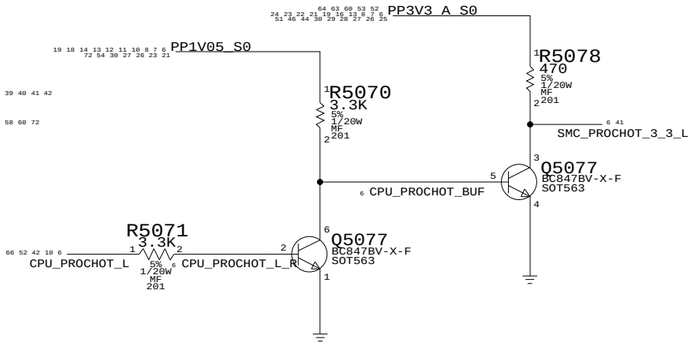
APPLE INC.	SIZE D / DRAWING NUMBER 051-7230 / REV. B.0.0	
	SCALE NONE / SHT 41 OF 73	

SMC Reset Button / Brownout Detect

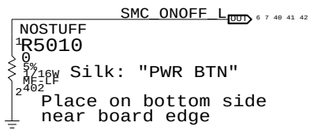


SMC 1.05V to 3.3V Level Shifting

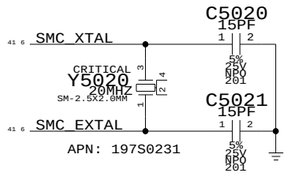




Debug Power Button

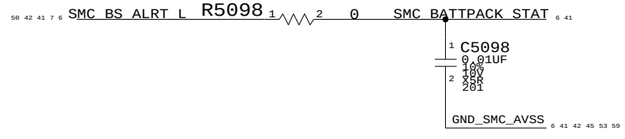


SMC Crystal Circuit

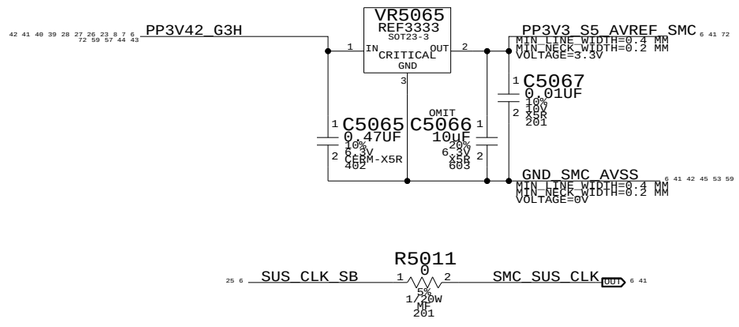


SMC 3.3V to 1.05V Level Shifting

Battery Pack Status



SMC AVREF Supply



3.3V TO PBUS LEVEL SHIFTING

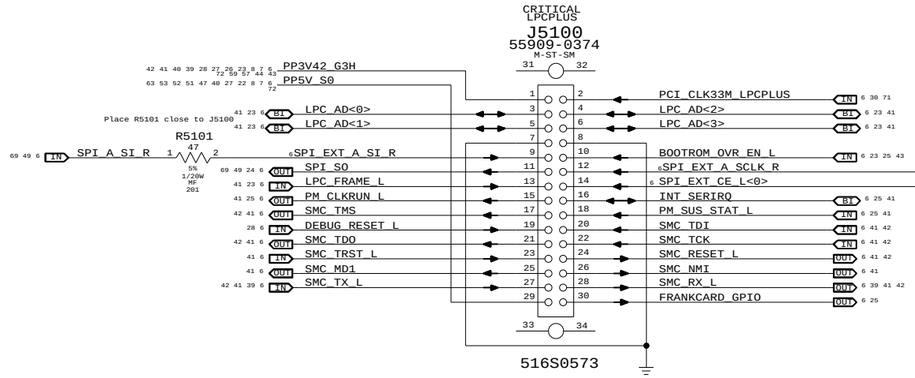
SMC SUPPORT

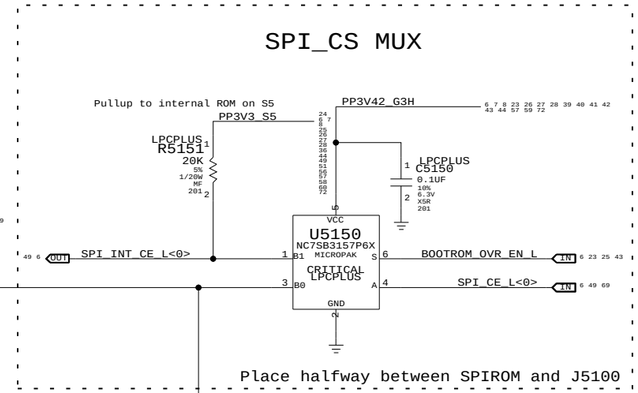
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 42 OF 73	

LPC+SPI Connector





LPC+SPI Debug Connector

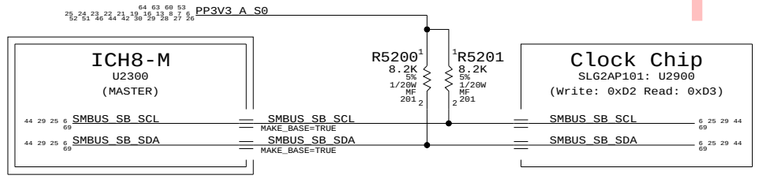
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

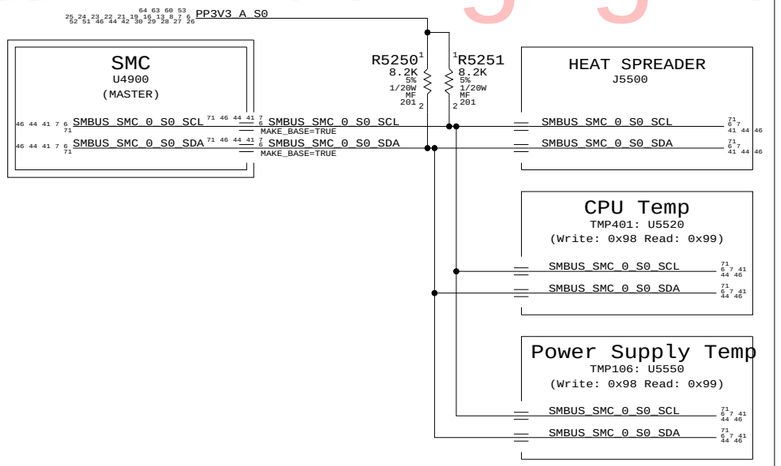
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE: NONE SHT 43 OF 73

ICH8-M SMBus Connections

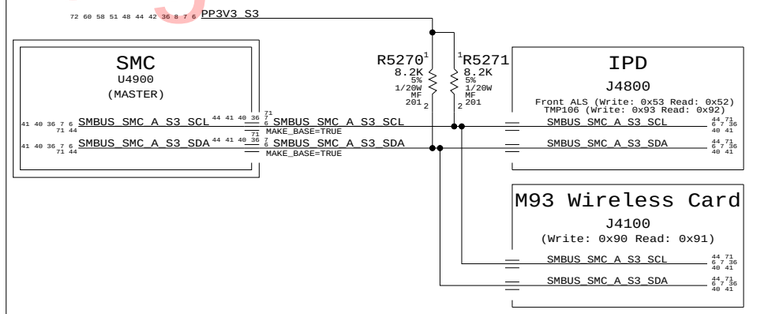


SMC "0" SMBus Connections

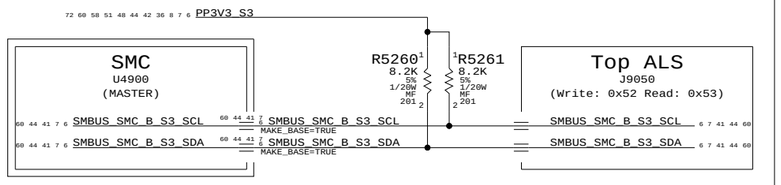


SMC "A" SMBus Connections

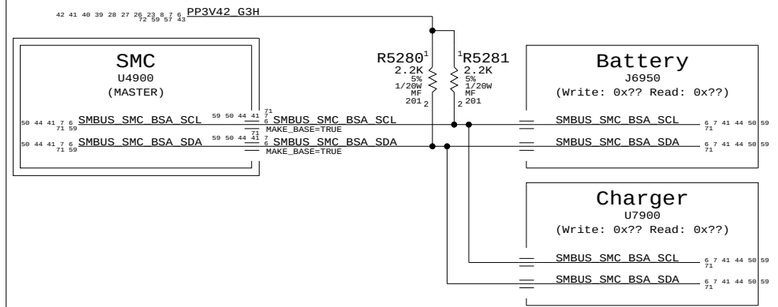
NOTE: SMC RMT bus remains powered and may be active in S3 state



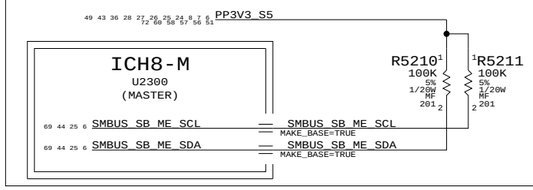
SMC "B" SMBus Connections



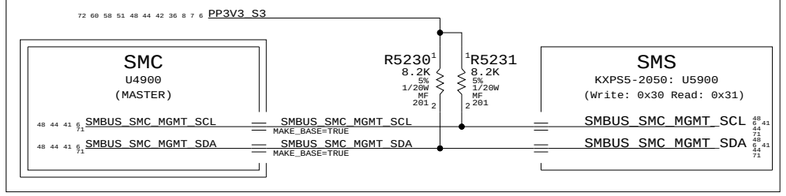
SMC "Battery A" SMBus Connections



ICH8-M ME SMBus Connections



SMC "Management" SMBus Connections



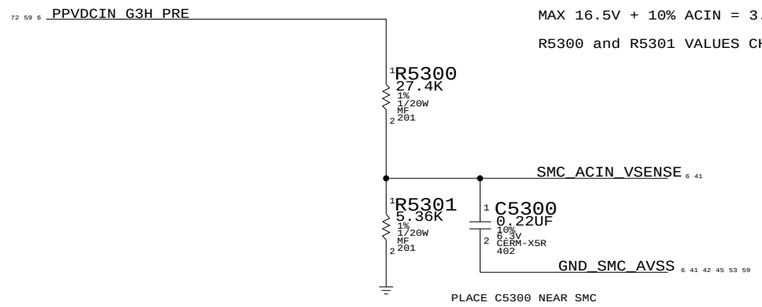
SMBUS CONNECTIONS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 44 OF 73	

ACIN VOLTAGE SENSE

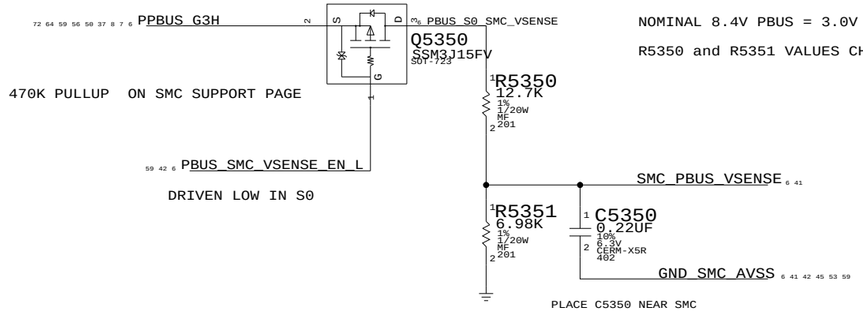


MAX 16.5V + 10% ACIN = 3.0V SMC_PBUS_VSENSE

R5300 and R5301 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

GPU VOLTAGE SENSE

PBUS VOLTAGE SENSE



NOMINAL 8.4V PBUS = 3.0V SMC_PBUS_VSENSE

R5350 and R5351 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

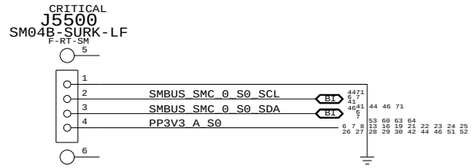
Voltage Sensors

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

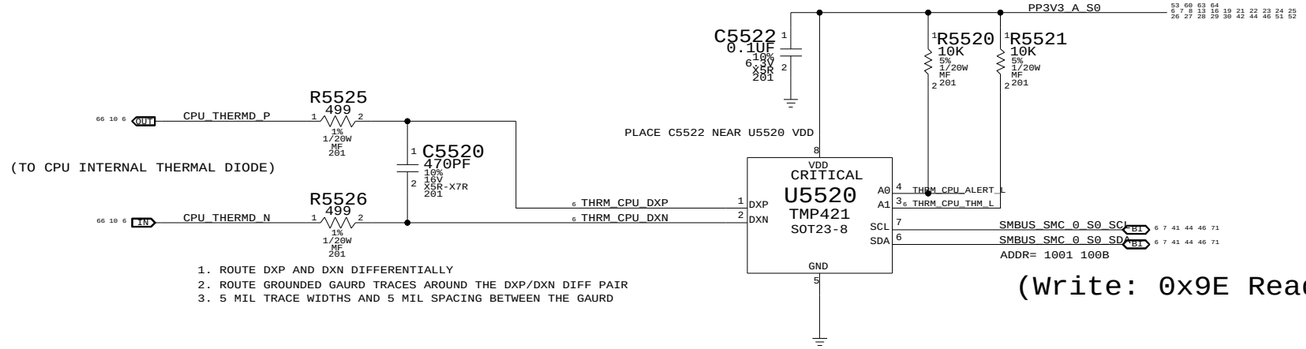
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 45 OF 73	

REMOTE TEMP AT HEAT SPREADER

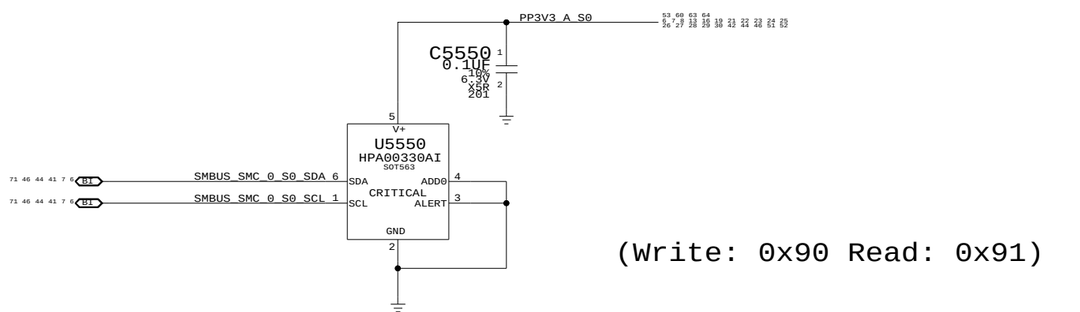


APN:518S0354

CPU THERMAL DIODE



LOCAL TEMP NEAR POWER SUPPLIES



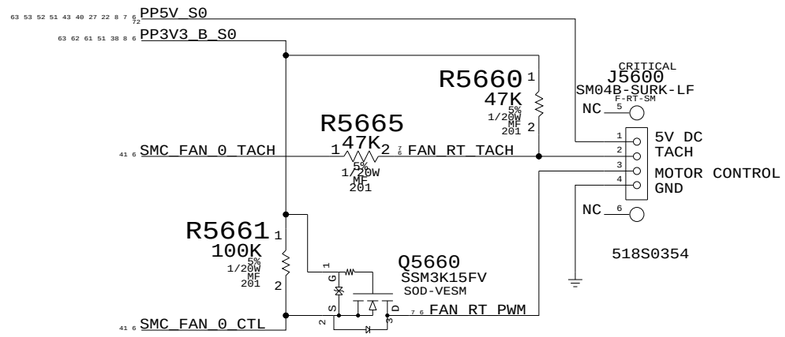
TEMPERATURE SENSORS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT: 46	OF: 73

FAN CONNECTOR



Fan

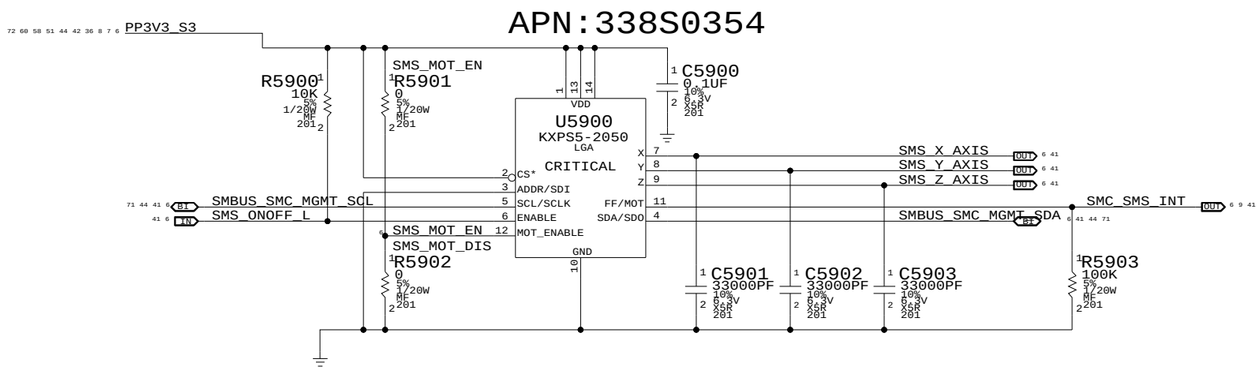
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	47	73

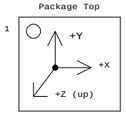
SUDDEN MOTION SENSOR



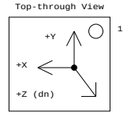
I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:



Desired orientation when placed on board bottom-side:



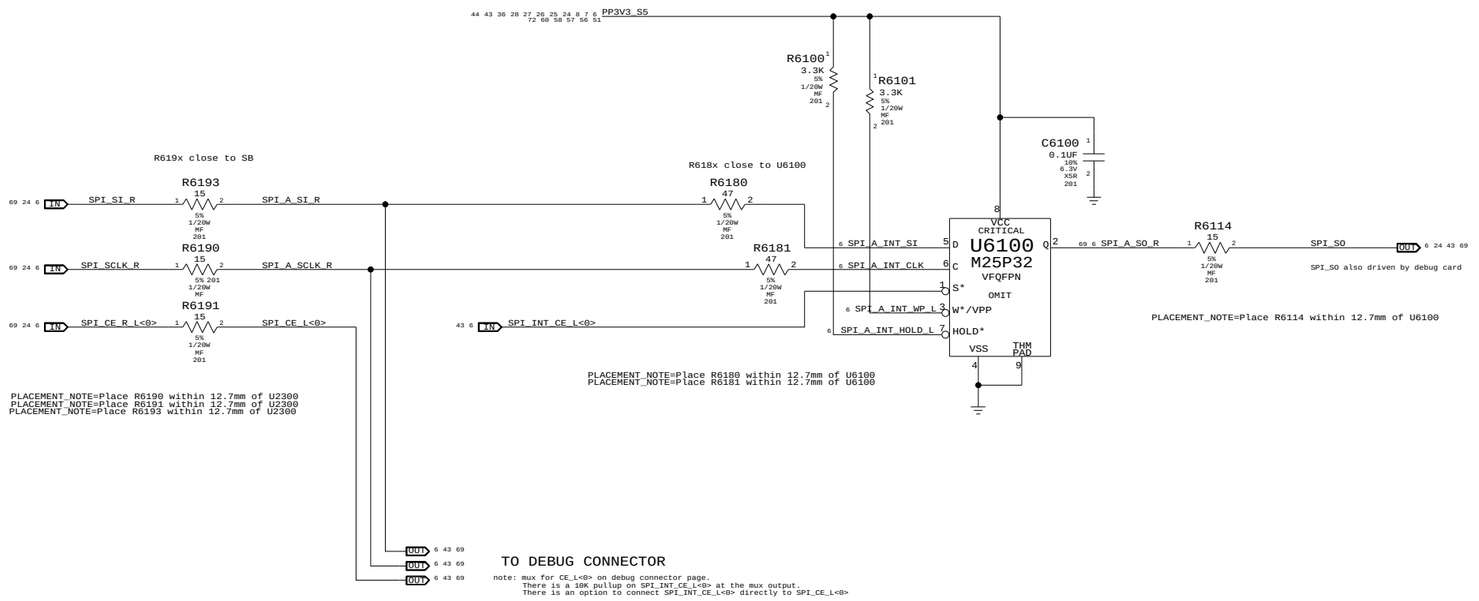
Sudden Motion Sensor (SMS)

SYNC_MASTER=M76_MLB SYNC_DATE=01/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 48 OF 73	

SPI ROM



SPI ROMs

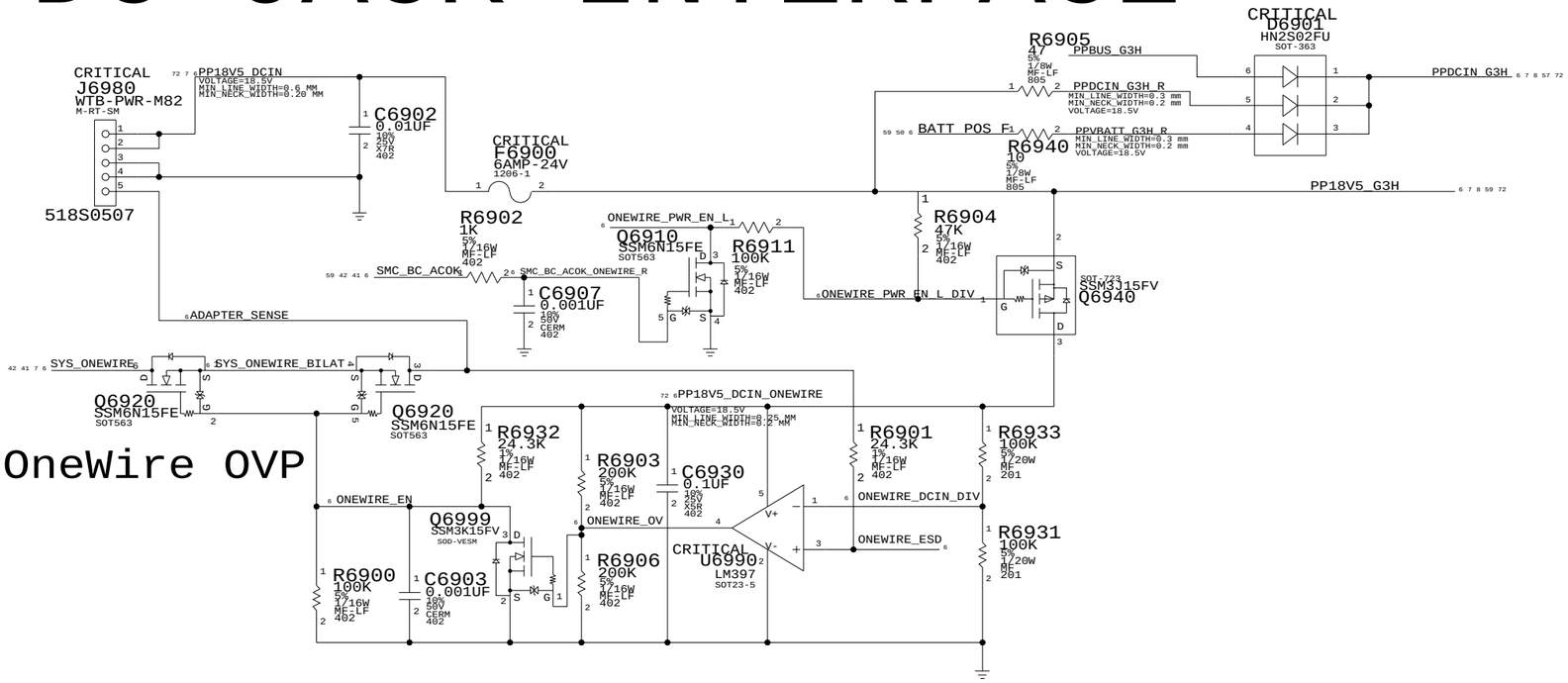
SYNC_MASTER=WFERRY SYNC_DATE=04/26/2006

APPLE INC.

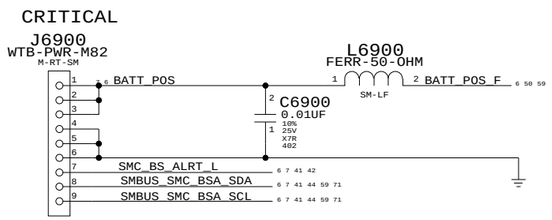
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	49	73

DC-JACK INTERFACE



BATTERY INTERFACE



DC-In & Battery Connectors		
SYNC_MASTER=M70	SYNC_DATE=01/09/2007	

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
	SCALE: NONE	SHT 50 OF 73	

S0 FETS & POWER SEQUENCING & PGOOD

5V S0 FET

MOSFET	FDM6296
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @4.5V
LOADING	4.061 A

3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.063 A

3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	.776 A

1.8V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.120 A

1.05V S0 RUN/SS CONTROL

1.25V S0 RUN/SS CONTROL

1.5V S0 RUN/SS CONTROL

DEASSERTED 160MS
AFTER UVLO_D VALID

~26MS

STUFF R7013,R7014 and UNSTUFF U7002,C7001,C7002
TO USE WIRE-AND OF ALL PGOODs INSTEAD OF TPS3808

U7002.3 has int 90K pull-up

S0 FETS & Power Sequencing	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT: 51	OF: 73

IMVP6 CPU VCORE REGULATOR

PP5V_S0 — R7101 0 5% 1/16W MF-LF 402 — C7101 OMIT 1UF 10% 6.3V CERM 402 — PP5V_S0_IMVP6_VDD (MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V)

IMVP6_PVCC (VOLTAGE=5V) — R7100 0 5% 1/16W MF-LF 402 — C7100 OMIT 1UF 10% 6.3V CERM 402

PPBUS_R_G3H — R7102 0 5% 1/16W MF-LF 402 — C7102 0.22UF 10% 16V X7R 603 — PPVIN_S5_IMVP6_VIN (MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=18.5V)

PM_DPRSLPVR (IN)

PP3V3_A_S0 — R7103 0 5% 1/20W MF 201 — PP3V3_S0_IMVP6_3V3 (MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V) — C7103 1UF 10% 10V X5R 402-1

GND_IMVP6_SGND

PLACE R7110 WITH NO STUB ON PM_DPRSLPVR

R7111 499 1% 1/20W MF 201 — R7110 499 1% 1/20W MF 201

NO STUFF R7115 0 5% 1/20W MF 201

CPU_PROCHOT_L — C7111 0.015uF 10% 16V X7R 402 — R7116 147K 1% 1/20W MF 201

U7100 ISL6261CRZ QFN (CRITICAL)

VIN	18		
VDD	20		
VCCP	27		
CPU_VID<6>	34	VID6	
CPU_VID<5>	33	VID5	
CPU_VID<4>	32	VID4	
CPU_VID<3>	31	VID3	
CPU_VID<2>	30	VID2	
CPU_VID<1>	29	VID1	
CPU_VID<0>	28	VID0	
CPU_DPRSTP_L	37	DPRSTP*	
IMVP_DPRSLPVR	36	DPRSLPVR	
	1	FDE	
ALL_SYS_PWRGD	2	PGD_IN	
	39	3V3	
VR_PWRGD_CK505_L	38	CLK_EN*	
IMVP_VR_ON (FROM SMC)	35	VR_ON	
VR_PWRGOOD_DELAY	40	PGOOD	
IMVP6_VR_TT	4	VR_TT*	
NC	5	NTC	
IMVP6_SOFT	6	SOFT	
IMVP6_RBIAS	3	RBIAS	
IMVP6_VDIFF	11	VDIFF	
IMVP6_FB	10	FB	
IMVP6_COMP	9	COMP	
IMVP6_VW	8	VW	
NC	21	NC	
VSS	19		
TPAD	41		
BOOT	22	IMVP6_BOOT	
LGATE	26	IMVP6_LGATE	
VSSP	25	(GND)	
UGATE	23	IMVP6_UGATE	
PHASE	24	IMVP6_PHASE	
VSUM	17	IMVP6_VSUM	
OCSET	7	IMVP6_OCSET	
VO	16	PPVCORE_S0_CPU (IMVP6_VO)	
DROOP	14	IMVP6_DROOP	
DFB	15	IMVP6_DFB	
VSEN	12	IMVP6_VSEN_N	
RTN	13	IMVP6_VSEN_P	

IMVP6_BOOT — R7104 0 5% 1/16W MF-LF 402 — C7104 0.22UF 10% 16V X7R 603 — IMVP6_BOOT_RC

PPBUS_R_G3H — C7150 CRITICAL 47UF 20% 10.0V POLY CASE-B2-1 — C7151 CRITICAL 47UF 20% 10.0V POLY CASE-B2-1 — C7152 1UF 10% 25V X5R 603 — C7153 1UF 10% 25V X5R 603

Q7100 CRITICAL RJK0305DPB LFPAK

(IMVP6_PHASE) — L7100 CRITICAL SM-IHLP 0.36UH-30A-1.2M-OHM — PPVCORE_S0_CPU

PWM FREQ. = 300kHz
MAX CURRENT = 30A

Q7150 CRITICAL RJK0303DPB LFPAK — Q7151 CRITICAL RJK0303DPB LFPAK

C7141 NO STUFF 1000PF 10% 16V X7R 201 — R7142 20K 1% 1/20W MF 201 — R7143 3.57K 1% 1/20W MF 201 — IMVP6_VO_R — R7144 CRITICAL 10KOHM-5% 0603-LF ERT-J1VR103J — R7145 4.53K 1% 1/20W MF 201

R7140 806 1% 1/20W MF 201 — R7141 6.34K 1% 1/20W MF 201 — C7140 330PF 10% 16V X7R 201

C7130 1000PF 10% 16V X7R 201 — C7131 1000PF 10% 16V X7R 201 — C7132 330PF 10% 16V X7R 201

C7142 0.12UF 10% 10.0V CERM-X5R 402 — C7143 0.01UF 10% 16V X5R 201

R7146 7.68K 1% 1/16W MF-LF 402

(IMVP6_VSUM)
(IMVP6_VO)

R7120 2.21K 1% 1/20W MF 201 — R7122 15K 1% 1/20W MF 201 — C7120 180PF 5% 50V CERM 402 — IMVP6_VDIFF_RC — (IMVP6_FB)

R7121 374K 1% 1/20W MF 201 — IMVP6_FB_RC — C7121 270PF 10% 50V X7R-CERM 402 — C7122 56PF 5% 25V NP0-C0G 201

R7124 1K 1% 1/20W MF 201 — C7124 0.01UF 10% 16V X5R 201 — GND_IMVP6_SGND

(IMVP6_VW) — C7123 1000PF 10% 16V X7R 201 — R7123 6.04K 1% 1/20W MF 201

R7134 100 1% 1/20W MF 201 — C7133 0.1UF 10% 6.3V X5R 201 — OMIT XW7100 SM

R7130 100 1% 1/20W MF 201 — R7131 0 5% 1/20W MF 201 — R7132 0 5% 1/20W MF 201

CPU_VCCSENSE_P
CPU_VCCSENSE_N

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

NOTE 1: C7132,C7133 = 27.4 OHM FOR VALIDATING CPU ONLY.

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE	1.5 MM	0.20 MM
IMVP6_BOOT	0.25 MM	0.20 MM
IMVP6_UGATE	1.5 MM	0.20 MM
IMVP6_LGATE	1.5 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
PPVCORE_S0_CPU	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.20 MM
IMVP6_PVCC	0.25 MM	0.20 MM
IMVP6_COMP_R	0.25 MM	0.20 MM
IMVP6_COMP_RC	0.25 MM	0.20 MM
IMVP6_FB_RC	0.25 MM	0.20 MM
IMVP6_VDIFF_RC	0.25 MM	0.20 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER — SYNC_DATE=07/13/2005

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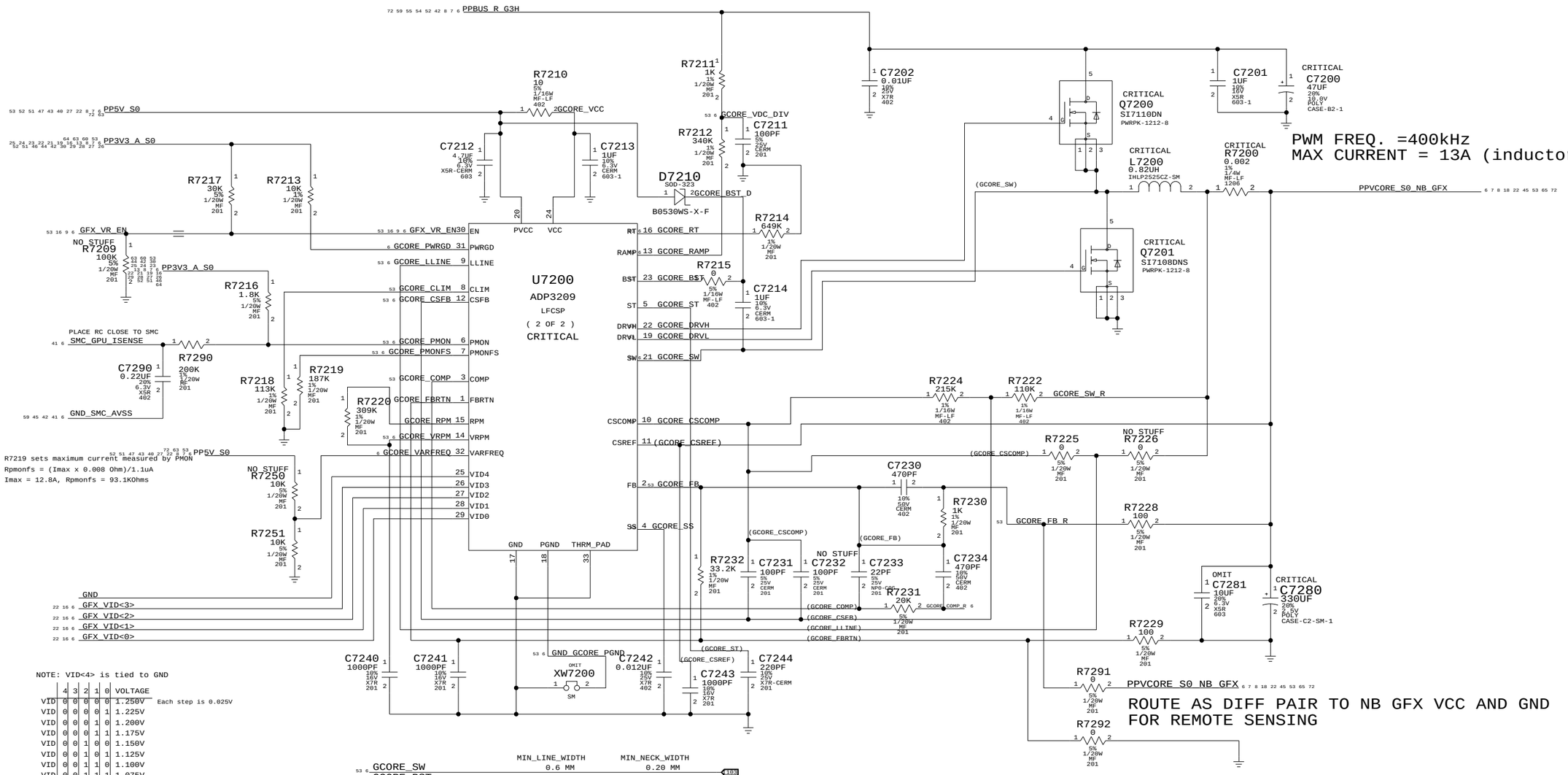
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 52 OF 73	

RENDER VCORE POWER SUPPLY



NOTE: VID<4> is tied to GND

	4	3	2	1	0	VOLTAGE
VID	0	0	0	0	0	1.250V
VID	0	0	0	0	1	1.225V
VID	0	0	0	1	0	1.200V
VID	0	0	0	1	1	1.175V
VID	0	0	1	0	0	1.150V
VID	0	0	1	0	1	1.125V
VID	0	0	1	1	0	1.100V
VID	0	0	1	1	1	1.075V
VID	0	1	0	0	0	1.050V
VID	0	1	0	0	1	1.025V
VID	0	1	0	1	0	1.000V
VID	0	1	0	1	1	0.975V
VID	0	1	1	0	0	0.950V
VID	0	1	1	0	1	0.925V
VID	0	1	1	1	0	0.900V
VID	0	1	1	1	1	0.875V

Each step is 0.025V

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GCORE_SW	0.6 MM	0.20 MM	0.13
GCORE_BST	0.3 MM	0.20 MM	0.14
GCORE_DRVH	0.6 MM	0.20 MM	0.15
GCORE_DRVL	0.6 MM	0.20 MM	0.16
GCORE_BST_D	0.3 MM	0.20 MM	0.17
GND_GCORE_PGND	0.6 MM	0.20 MM	0.18
GCORE_VDC_DIV	0.3 MM	0.20 MM	0.19
GCORE_RAMP	0.3 MM	0.20 MM	0.20
GCORE_CLIM	0.3 MM	0.20 MM	0.21
GCORE_SS	0.3 MM	0.20 MM	0.22
GCORE_ST	0.3 MM	0.20 MM	0.23
GCORE_SW_R	0.6 MM	0.20 MM	0.24

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GCORE_CSCOMP	0.3 MM	0.20 MM	0.25
GCORE_CSFB	0.3 MM	0.20 MM	0.27
GCORE_LLINE	0.3 MM	0.20 MM	0.28
GCORE_RT	0.3 MM	0.20 MM	0.29
GFX_VR_EN	0.3 MM	0.20 MM	0.30
GCORE_COMP	0.3 MM	0.20 MM	0.31
GCORE_FB	0.3 MM	0.20 MM	0.32
GCORE_FBRTN	0.3 MM	0.20 MM	0.33
GCORE_PMON	0.3 MM	0.20 MM	0.34
GCORE_PMONFS	0.3 MM	0.20 MM	0.35
GCORE_RPM	0.3 MM	0.20 MM	0.36
GCORE_VRPM	0.3 MM	0.20 MM	0.37
GCORE_FB_R	0.3 MM	0.20 MM	0.38

Render VCore Supplies

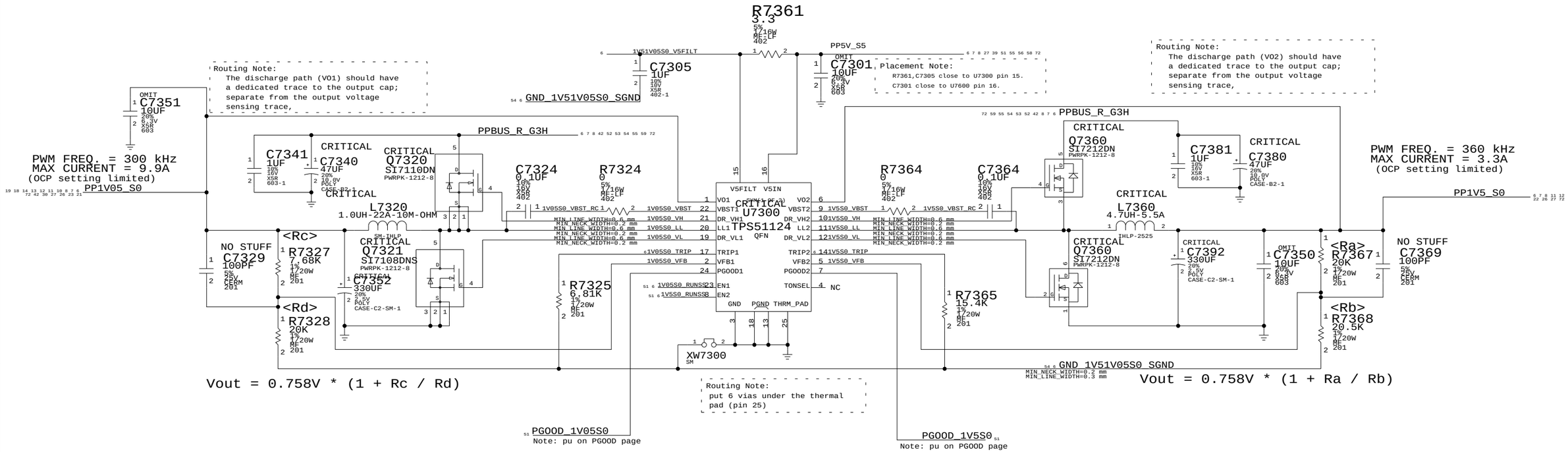
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 53 OF 73	

1.5V/1.05V POWER SUPPLY

State	PM_SLP_S3_L	PP1V5_S0	PP1V05_S0
S0	HIGH	1.5V	1.05V
S3/S5/G3Hot	LOW	0.0V	0.00V



1.5V/1.05V Supplies

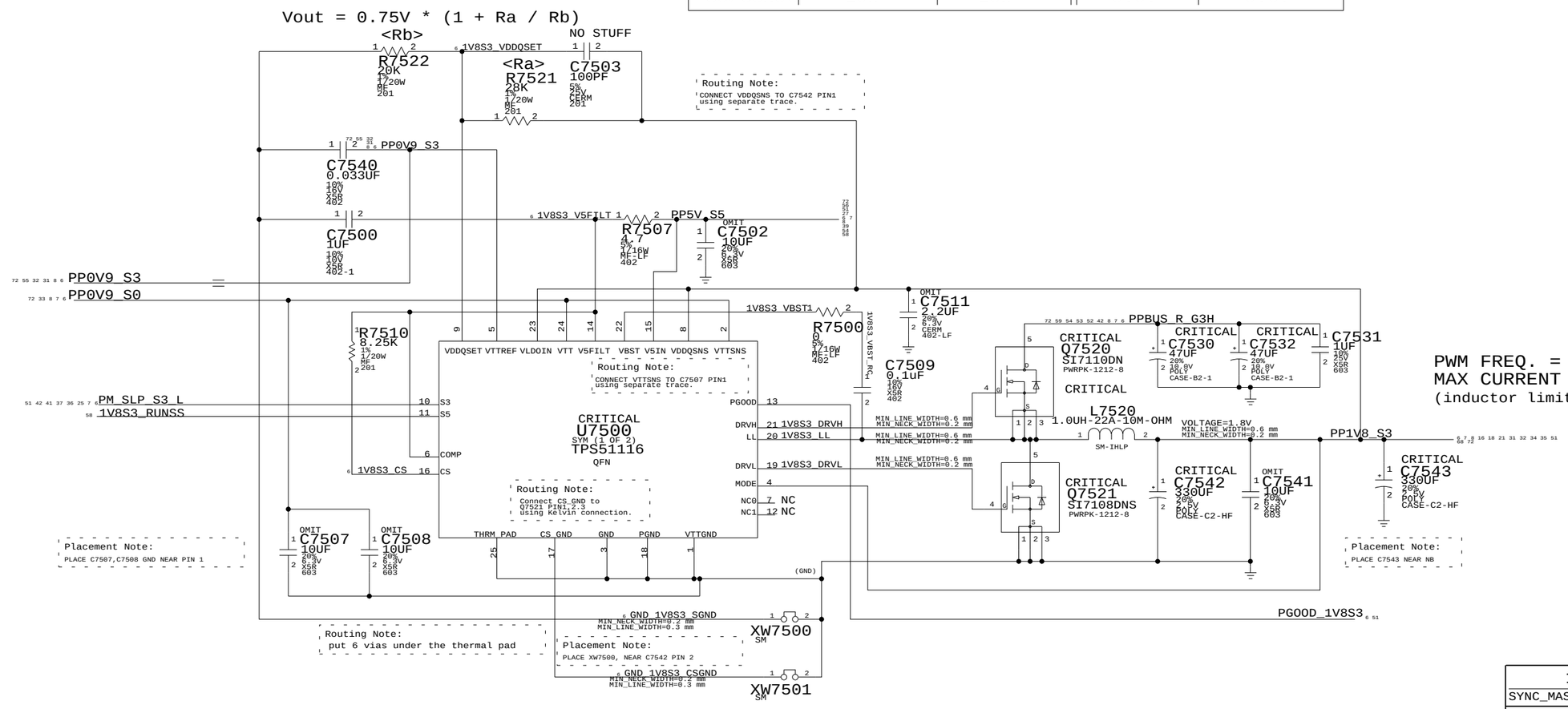
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 54 OF 73	

1.8V/0.9V POWER SUPPLY

State	PM_S4_STATE_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V



1.8V/0.9V Supplies

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 55 OF 73	

5V/3.3V POWER SUPPLY

State	SMC_PM_G2_EN	PP3V3_G3H	PP5V_S5	PP3V3_S5
G3H	LOW	3.3V	0.0V	0.0V
S0/S3/S5	HIGH	3.3V	5.0V	3.3V

Vout = 1V * (1 + Ra / Rb)
5.106V = 1V * (1 + 20K / 4.87K)

<Ra> R7667 20K 1% 1/20W MF 201
<Rb> R7668 4.87K 1% 1/20W MF 201

NO STUFF C7667 100PF 5% 25V CERM 201

GND_5V3V3S5_SGND 6 56

5VS5_FB

R7610 0 5% 1/16W MF 402

C7600 0.001UF 10% 50V CERM 402

25V3V3S5_VREF

5V3V3S5_V5FILT 6 56

GND_5V3V3S5_SGND 56 6

Routing Note:
The discharge path (VO1) should have a dedicated trace to the output cap;

Routing Note:
The discharge path (VO2) should have a dedicated trace to the output cap; separate from the output voltage sensing trace,

PPBUS_G3H

Routing Note:
put 6 vias under the thermal pad (pin 33)

CRITICAL U7600 TPS51120 LLP SYM (2 OF 3)

33	PWPD	VO1 1	TONSEL
32	SKIPSEL	COMP1 2	
31	TONSEL	VFB1 3	
30	PGOOD1	VREF2 4	
29	EN1	GND 5	
28	VBST1	VFB2 6	
27	DRVH1	COMP2 7	
26	LL1	VO2 8	
25	DRVL1	EN5 9	NC
24	PGND1	EN3 10	NC
23	CS1	PGOOD2 11	
22	VIN	EN2 12	SMC_PM_G2_EN
21	VREG5	VBST2 13	
20	V5FILT	DRVH2 14	
19	VREG3	LL2 15	
18	CS2	DRVL2 16	
17	PGND2		

C7680 47UF 20% 10.0V POLY CASE-B2-1
C7681 1UF 10% 16V X5R 603-1
C7660 0.1UF 10% 16V X5R 402
R7660 0 5% 1/16W MF-LF 402
SMC_PM_G2_EN 6 41 56
RSMRST_PWRGD 6 41 42 56
5VS5_TONSEL
5VS5_VBST_R
5VS5_VBST
5VS5_DRVH
5VS5_LL
5VS5_DRVL
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm

CRITICAL Q7660 SI7110DN PWRPK-1212-8

CRITICAL L7660 3.3UH-6.5A IHLP

VOLTAGE=5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm

OMIT C7690 10UF 20% 6.3V X5R 603

CRITICAL C7691 150UF 20% 6.3V POLY CASE-B2-HF

CRITICAL C7692 150UF 20% 6.3V POLY CASE-B2-HF

CRITICAL Q7661 SI7110DN PWRPK-1212-8

PWM FREQ. = 280 kHz
MAX CURRENT = 6.0A
(inductor limited)

PP5V_S5 72 58 55 54 51 39 27 8 7 6

R7605 5.90K 1% 1/20W MF 201

R7603 7.15K 1% 1/20W MF 201

5V3V3S5_V5FILT 6 56

5V3V3S5_VREG3

R7601 4.7 5% 1/16W MF-LF 402

C7602 1UF 10% 16V X5R 603-1

OMIT C7604 10UF 20% 6.3V X5R 603

C7605 1UF 10% 16V X5R 402-1

OMIT C7603 10UF 20% 6.3V X5R 603

XW7601 SM

GND_5V3V3S5_SGND 6 56
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.3 mm

Placement Note:
R7601,C7605 close to U7600 pin 20.
C7602 close to U7600 pin 22.
C7604 close to U7600 pin 21.
C7603 CLOSE TO U7600 PIN 19.
R7605,R7603 close to U7600.

PPBUS_G3H 72 64 59 56 50 45 37 8 7 6

C7641 1UF 10% 16V X5R 603-1

CRITICAL C7640 47UF 20% 10.0V POLY CASE-B2-1

R7620 0 5% 1/16W MF-LF 402

C7620 0.1UF 10% 16V X5R 402

3V3S5_VBST_R

3V3S5_VBST

3V3S5_DRVH

3V3S5_LL

3V3S5_DRVL

CRITICAL Q7620 SI7110DN PWRPK-1212-8

CRITICAL L7620 2.2UH-14A IHLP2525CZ-SM1

CRITICAL Q7621 SI7110DN PWRPK-1212-8

PWM FREQ. = 430 kHz
MAX CURRENT = 7.8A
(OCP setting limited)

PP3V3_S5 6 7 8 24 25 26 27 28 36 43 44 49 51 57 58 60 72

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm

CRITICAL C7652 150UF 20% 6.3V POLY CASE-B2-HF

CRITICAL C7651 150UF 20% 6.3V POLY CASE-B2-HF

OMIT C7650 10UF 20% 6.3V X5R 603

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7682,C7680	KEMET T520V336M016ATE045760
128S0093	128S0092	?	C7640	KEMET T520V336M016ATE045760

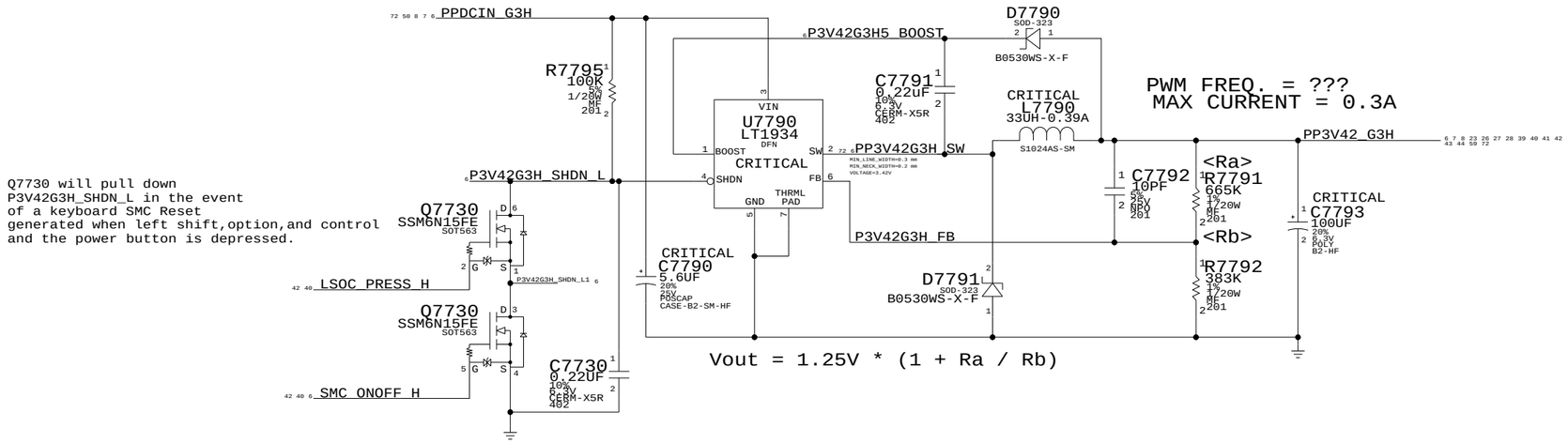
5V/3.3V Supplies
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

APPLE INC.

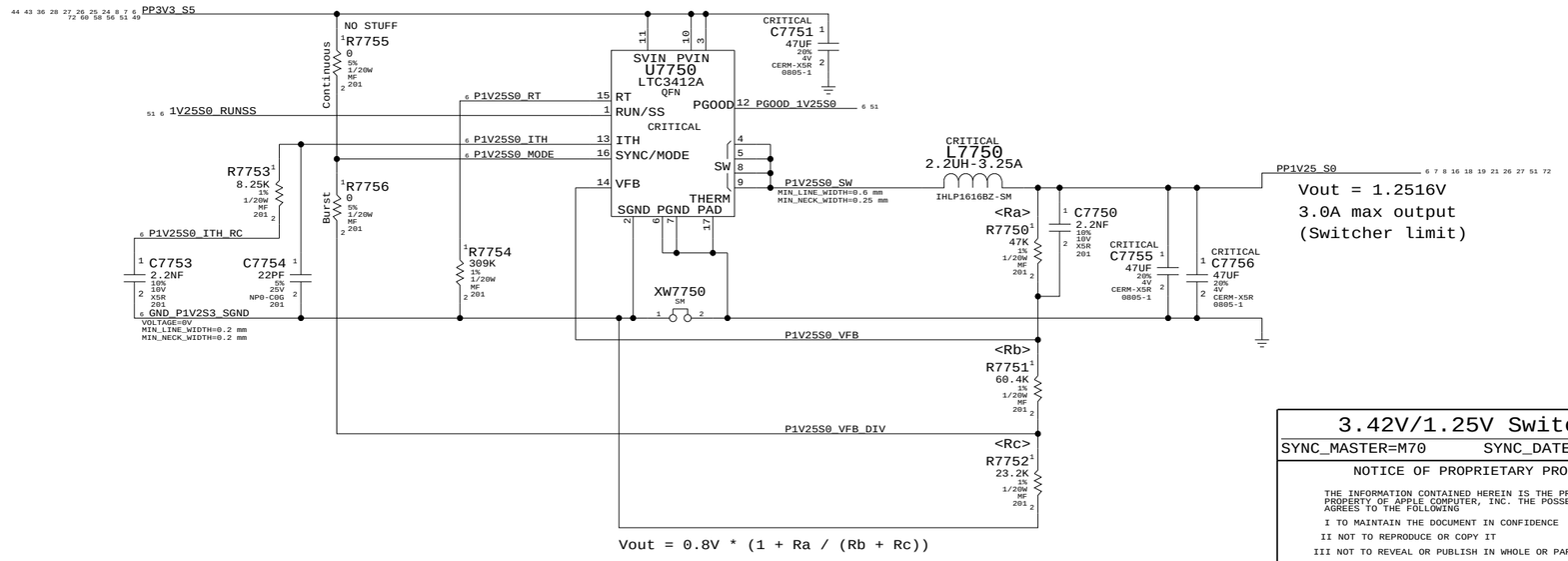
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 56 OF 73	

3.425V G3H SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



1.25V S0 REGULATOR

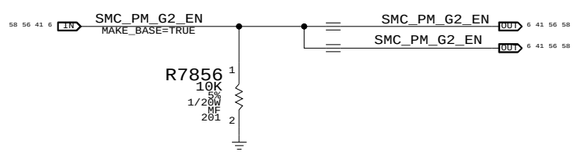


3.42V/1.25V Switcher		
SYNC_MASTER=M70	SYNC_DATE=01/09/2007	

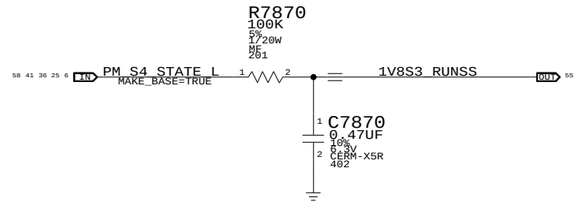
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
	SCALE: NONE	SHT 57 OF 73	

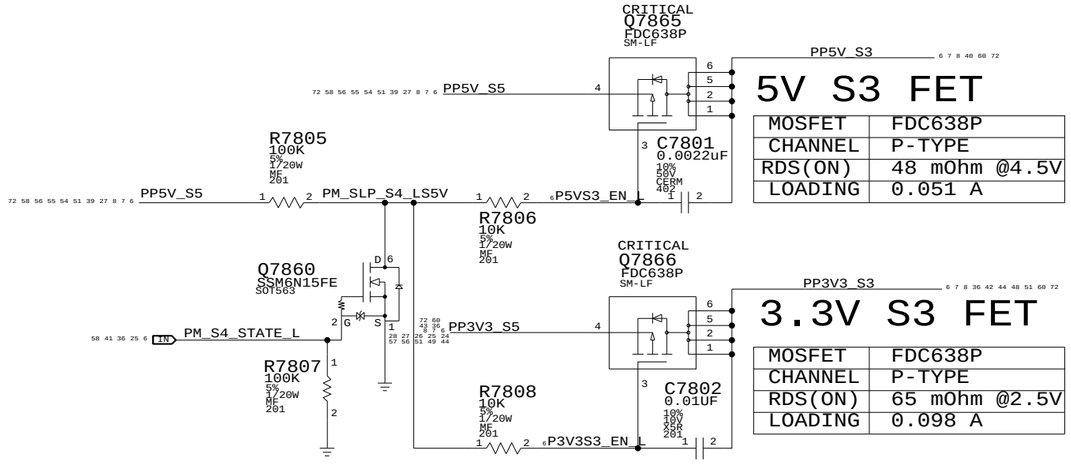
S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL



1.8V S3 RUN/SS CONTROL





5V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.051 A

3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	0.098 A

S3 FET & S3/S5 Control

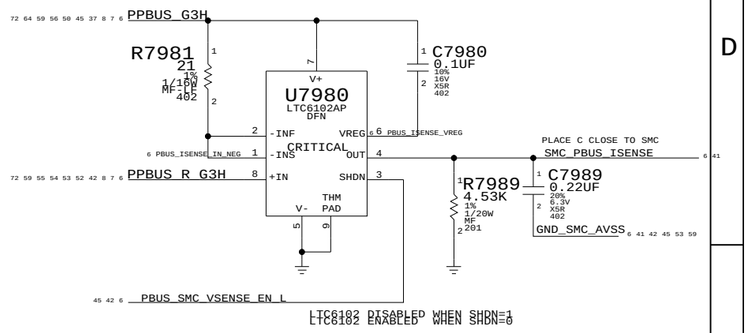
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

APPLE INC.

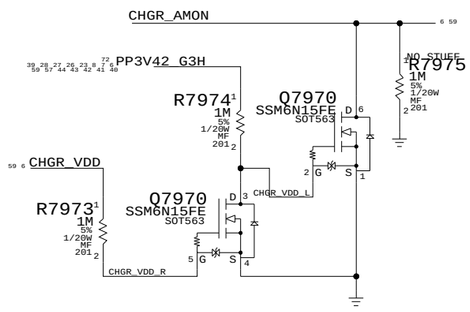
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 58 OF 73	

PBUS SUPPLY / BATTERY CHARGER

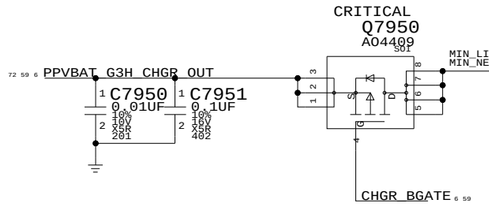
PBUS CURRENT SENSOR



AMON PULLDOWN LOGIC

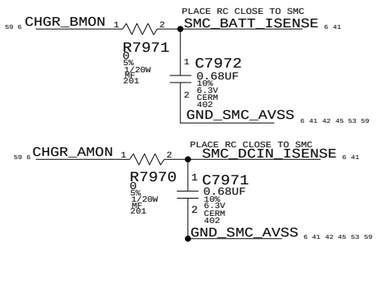


BATTERY CHARGING



ACOK pullup/down on SMC page

SMC_BC_ACOK — SMC_BC_ACOK (MAKE_BASE=TRUE)



PBUS Supply/Battery Charger		
SYNC_MASTER=M70	SYNC_DATE=01/09/2007	
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APPLE INC.	SIZE D / DRAWING NUMBER 051-7230 / REV. B.0.0	
	SCALE NONE / SHT 59 OF 73	

LCD + CAMERA CONNECTOR

PP3V3_S5
R9002 100K 5% 1/20W MF 201
C9040 0.1UF 10% 6.3V X5R 201
Q9004 SSM3K15FV SOD-VESM
LCDVDD_PWREN_L
R9023 10K 5% 1/20W MF 201
CRITICAL Q9003 FDC638P SM-LF
C9013 0.0033UF 10% 50V CERM 402
C9011 0.1UF 10% 6.3V X5R 201
C9012 10UF 20% 6.3V X5R 603 OMIT
PP3V3_LCDVDD_SW
PLT_RST_L
LVDS_VDD_EN
U9040 TC7SZ08AFEF SOT665
LVDS_VDD_GATED_EN
R9014 100K 1% 1/20W MF 201

CRITICAL L9007 90-OHM-100MA 1210-4SM1
USB2_CAMERA_N
USB2_CAMERA_P
CRITICAL L9005 FERR-120-OHM-1.5A 0402-LF
PP5V_S3
C9016 1000PF 10% 16V X7R 201
CRITICAL L9004 FERR-120-OHM-1.5A 0402-LF
C9015 1000PF 10% 16V X7R 201

L9052 240-OHM-0.2A-0.8-OHM 0201
SMBUS_SMC_B_S3_SDA
I2C_TOP_ALS_SDA_F
L9051 240-OHM-0.2A-0.8-OHM 0201
SMBUS_SMC_B_S3_SCL
I2C_TOP_ALS_SCL_F
C9052 10PF 5% 25V NPO 201
C9051 10PF 5% 25V NPO 201

CRITICAL J9000 20347-130E-11 F-RT-SM
518S0433

PLACE FILTERS AND CAPS NEAR PINS ON CONNECTOR

PP5V_S3_CAMERA_F
USB2_CAMERA_F_P
USB2_CAMERA_F_N
PP3V3_LCDVDD_SW_F
PP3V3_S0_LCD_F
CAMERA I/F
LCD I/F

L9008 120-OHM-0.3A-EMI 0402-LF
PP3V3_A_S0
(LVDS_DDC_POWER)
C9010 1000PF 10% 16V X7R 201
R9008 10K 5% 1/20W MF 201
R9009 10K 5% 1/20W MF 201
LVDS_DDC_CLK
LVDS_DDC_DATA

LVDS_A_DATA_F_N<0>
LVDS_A_DATA_F_P<0>
LVDS_A_DATA_F_N<1>
LVDS_A_DATA_F_P<1>
LVDS_A_DATA_F_N<2>
LVDS_A_DATA_F_P<2>
LVDS_A_CLK_F_N
LVDS_A_CLK_F_P
LCDBKLT_RTN<1>
LCDBKLT_RTN<2>
LCDBKLT_RTN<3>
LCDBKLT_RTN<4>
LCDBKLT_RTN<5>
LCDBKLT_RTN<6>
PPVOUT_S0_LCDBKLT

LVDS REFERENCE CURRENT,2.37K OHM PULL DOWN RESISTOR NEEDED

R9013 2.37K 1% 1/20W MF 201
LVDS_IBG
PLACE NEAR NB

CRITICAL L9010 90-OHM-100MA 1210-4SM1
LVDS_A_DATA_N<0>
LVDS_A_DATA_P<0>
CRITICAL L9011 90-OHM-100MA 1210-4SM1
LVDS_A_DATA_N<1>
LVDS_A_DATA_P<1>
CRITICAL L9012 90-OHM-100MA 1210-4SM1
LVDS_A_DATA_N<2>
LVDS_A_DATA_P<2>
CRITICAL L9006 90-OHM-100MA 1210-4SM1
LVDS_A_CLK_N
LVDS_A_CLK_P

MIC CONNECTOR

CRITICAL J9050 GS03067-11131-7F F-RT-SM
PP3V3_S3_MIC_F
NC
NC
GND_MIC_F
L9050 240-OHM-0.2A-0.8-OHM 0201
PP3V3_S3
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.20MM VOLTAGE=3.3V
L9030 240-OHM-0.2A-0.8-OHM 0201
AUD_MIC_DATA_F
AUD_MIC_DATA
L9031 240-OHM-0.2A-0.8-OHM 0201
AUD_MIC_CLK_F
AUD_MIC_CLK
L9053 240-OHM-0.2A-0.8-OHM 0201
C9050 0.01UF 10% 10V X5R 201
C9053 0.01UF 10% 10V X5R 201
C9030 10PF 5% 25V NPO 201 NO STUFF
C9031 10PF 5% 25V NPO 201 NO STUFF

APN:518S0356

LVDS,Camera Conn. and ALS Conn.

SYNC_MASTER=GPU SYNC_DATE=06/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 60 OF 73	

8	7	6	5	4	3	2	1

D

CRITICAL L9206 FERR-120-OHM-1.5A 0402-LF — PP1V8_S0 → PP1V8_S0_ANALOG_TMDS_F (VOLTAGE=1.8V, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM)
C9236 1000PF 10% 16V X7R 201; C9237 1000PF 10% 16V X7R 201; C9238 0.1UF 10% 6.3V X5R 201; C9239 0.1UF 10% 6.3V X5R 201; OMIT C9240 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 1000PF FOR EACH PIN

CRITICAL L9203 FERR-120-OHM-1.5A 0402-LF — PP3V3_B_S0 → PP3V3_S0_ANALOG_SDVO_F (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM)
C9230 1000PF 10% 16V X7R 201; C9231 0.1UF 10% 6.3V X5R 201; C9214 1000PF 10% 16V X7R 201

CRITICAL L9204 FERR-120-OHM-1.5A 0402-LF — PP1V8_S0 → PP1V8_S0_PVCC1_TMDS_F (VOLTAGE=1.8V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM)
C9232 1000PF 10% 16V X7R 201; C9254 1000PF 10% 16V X7R 201; C9233 0.1UF 10% 6.3V X5R 201; C9206 0.1UF 10% 6.3V X5R 201
TWO 0.1UF AND 1000PF FOR EACH PIN

CRITICAL L9205 FERR-120-OHM-1.5A 0402-LF — PP1V8_S0 → PP1V8_S0_PVCC2_TMDS_F (VOLTAGE=1.8V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM)
C9234 1000PF 10% 16V X7R 201; C9235 1000PF 10% 16V X7R 201; C9255 0.1UF 10% 6.3V X5R 201; C9256 0.1UF 10% 6.3V X5R 201
TWO 0.1UF AND 1000PF FOR EACH PIN

CRITICAL L9207 FERR-120-OHM-1.5A 0402-LF — PP3V3_B_S0 → PP3V3_S0_SPVCC_TMDS_F (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM)
C9257 1000PF 10% 16V X7R 201; C9258 1000PF 10% 16V X7R 201; C9259 0.1UF 10% 6.3V X5R 201; C9260 0.1UF 10% 6.3V X5R 201
TWO 0.1UF AND 1000PF FOR EACH PIN

CRITICAL L9201 FERR-120-OHM-1.5A 0402-LF — PP1V8_S0 → PP1V8_S0_TMDS_F (VOLTAGE=1.8V, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM)
C9207 0.1UF 10% 6.3V X5R 201; C9208 1000PF 10% 16V X7R 201; C9209 0.1UF 10% 6.3V X5R 201; C9210 1000PF 10% 16V X7R 201; C9211 0.1UF 10% 6.3V X5R 201; C9212 1000PF 10% 16V X7R 201; OMIT C9213 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 1000PF FOR EACH PIN
C9250 0.1UF 10% 6.3V X5R 201; C9251 1000PF 10% 16V X7R 201; C9252 0.1UF 10% 6.3V X5R 201; C9253 1000PF 10% 16V X7R 201; C9261 0.1UF 10% 6.3V X5R 201; C9262 1000PF 10% 16V X7R 201

CRITICAL L9200 FERR-120-OHM-1.5A 0402-LF — PP1V8_S0 → PP1V8_S0_ANALOG_SDVO_F (VOLTAGE=1.8V, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM)
C9200 1000PF 10% 16V X7R 201; C9201 1000PF 10% 16V X7R 201; C9202 0.1UF 10% 6.3V X5R 201; OMIT C9204 10UF 20% 6.3V X5R 603
ONE 1000PF FOR EACH PIN

R9207 49.9 1% 1/20W MF 201 — TMDS_TX_P<0> → TMDS_TX<0>; C9222 1000PF 10% 16V X7R 201; R9237 49.9 1% 1/20W MF 201 — TMDS_TX_N<0>
R9208 49.9 1% 1/20W MF 201 — TMDS_TX_P<1> → TMDS_TX<1>; C9223 1000PF 10% 16V X7R 201; R9238 49.9 1% 1/20W MF 201 — TMDS_TX_N<1>
R9209 49.9 1% 1/20W MF 201 — TMDS_TX_P<2> → TMDS_TX<2>; C9224 1000PF 10% 16V X7R 201; R9239 49.9 1% 1/20W MF 201 — TMDS_TX_N<2>
R9210 49.9 1% 1/20W MF 201 — TMDS_TX_CLK_P → TMDS_TX_CLK; C9225 1000PF 10% 16V X7R 201; R9240 49.9 1% 1/20W MF 201 — TMDS_TX_CLK_N

C

PP3V3_B_S0 → C9221 0.1UF 10% 6.3V X5R 201; OMIT C9205 10UF 20% 6.3V X5R 603 → PP3V3_S0_SPVCC_TMDS_F
PP3V3_S0_SPVCC_TMDS_F → C9290 0.1UF 10% 6.3V X5R 201; PP3V3_B_S0 → NO STUFF R9254 0 5% 1/20W MF 201 → TMDS_HW_RESET_L

CRITICAL U9290 TC7SZ08AFEAPE SOT665 — TMDS_RST_L → TMDS_SW_RESET_L

PP3V3_S0_ANALOG_SDVO_F
PP1V8_S0_ANALOG_SDVO_F
PP1V8_S0_PVCC2_TMDS_F
PP1V8_S0_PVCC1_TMDS_F
PP1V8_S0_ANALOG_TMDS_F
PP1V8_S0_TMDS_F

CRITICAL U9200 SIL1392 QFN

VCC	2, 9, 33, 38, 43, 48		
SVCC	50, 56		
PVCC1	17		
PVCC2	31		
AVCC1_8	21, 27		
AVCC3_3	32		
HDAVCC	37		
OVCC	64		
SPVCC	62		
TMDS_TX_N<0>	22	TX0-	
TMDS_TX_P<0>	23	TX0+	
TMDS_TX_N<1>	25	TX1-	
TMDS_TX_P<1>	26	TX1+	
TMDS_TX_N<2>	28	TX2-	
TMDS_TX_P<2>	29	TX2+	
TMDS_TX_CLK_N	19	TXC-	
TMDS_TX_CLK_P	20	TXC+	
TMDS_EXT_SWING	16	EXT_SWING	
TMDS_SDR_N	52	SDR-	
TMDS_SDR_P	51	SDR+	
TMDS_SDG_N	55	SDG-	
TMDS_SDG_P	54	SDG+	
TMDS_SDB_N	58	SDB-	
TMDS_SDB_P	57	SDB+	
TMDS_SDC_N	61	SDC-	
TMDS_SDC_P	60	SDC+	
TMDS_INT_N	47	SDI-	
TMDS_INT_P	46	SDI+	
TMDS_EXT_RES	49	EXT_RES	
	44	TEST	
	5, 10, 41, 45	GND	
	53, 59, 63	SGND	
	18, 24, 30	SPGND	
	65	AGND	
		THRM_PAD	

HOST SERIAL DATA RECEIVER CORE; CONFIGURATION /PROGRAMMING; I2C MASTER; AUDIO; LOCAL I2C; DIFFERENTIAL SIGNAL DATA; FACTORY TEST MODE

RESET*	1	TMDS_RST_L
SDSCL	7	SDVO_CTRLCLK
SDSDA	6	SDVO_CTRLDATA
A1	8	ADDRESS=0X70 / ADDRESS=0X72 IF A1 IS PULLED HIGH
HTPLG (int pulldown)	42	DVI_HOTPLUG_DET
SDADDC	12	TMDS_DDC_SDA
SCLDDC	11	TMDS_DDC_SCL
SDAROM (int pullup)	13	NC
SCLROM (int pullup)	14	NC
SPDIF/HDASDO	34	NC
HDASYNC	40	NC
HDABCLK	39	NC
HDASDI	36	NC
HDARST*	35	TMDS_HDARST_L
LSCL/DCEN	4	TMDS_LSCL
LSDA/PREEMP	3	TMDS_LSDA
LINT*	15	TMDS_LINT_L

TMDS_LSCL, TMDS_LSDA: MAKE_BASE=TRUE

MCH SDVO CHANNEL R,G,B,CLK SIGNAL TO TMDS CHIP
PEG_R2D_C_N<0>, PEG_R2D_C_P<0>, PEG_R2D_C_N<1>, PEG_R2D_C_P<1>, PEG_R2D_C_N<2>, PEG_R2D_C_P<2>, PEG_R2D_C_N<3>, PEG_R2D_C_P<3>
PLACE THESE CAPS NEAR NB
C9241 C9242 C9243 C9244 C9245 C9246 C9247 C9248 0.1UF 10% 6.3V X5R 201

R9204 360 5% 1/20W MF 201 — PP1V8_S0_ANALOG_SDVO_F

DVI_HOTPLUG_DET → "Place R9250 near U2300.F12" → R9250 100K 5% 1/20W MF 201

C9219 0.1UF 10% 6.3V X5R 201; C9220 0.1UF 10% 6.3V XSR 201
PEG_D2R_N<1>, PEG_D2R_P<1> → TMDS_INT_N, TMDS_INT_P
TMDS CHIP SDVO INPUT INTERRUPT SIGNAL TO MCH

R9203 1K 1% 1/20W MF 201 — TMDS_EXT_RES

R9251 4.7K 5% 1/20W MF 201 — PP3V3_B_S0

NO STUFF R9253 0 5% 1/20W MF 201 — TMDS_LSCL
NO STUFF R9252 0 5% 1/20W MF 201 — TMDS_LSDA

PP3V3_B_S0 → R9201 2.94K 1% 1/20W MF 201; R9202 2.94K 1% 1/20W MF 201 → SDVO_CTRLCLK, SDVO_CTRLDATA
R9211 9.09K 1% 1/20W MF 201; R9212 9.09K 1% 1/20W MF 201

PLACE R9200,U9201 CLOSE TO RIO CONN J4200

CRITICAL U9201 74LVC1G17DRL SOT-553 — TMDS_HTPLG → R9200 10K 5% 1/20W MF 201 → TMDS_HTPLG_R; 5.5V TOL INPUT; 3.3V ACTIVE OUTPUT → DVI_HOTPLUG_DET_BUF

R9200 INSURES ESD DIODE CURRENT IS SMALL

R9213 270K 5% 1/20W MF 201

SDVO/TMDS Tx

SYNC_MASTER=GRAPHIC — SYNC_DATE=06/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 61 OF 73	

8	7	6	5	4	3	2	1

SST8051 microcontroller for HDCP support

PP3V3_B_S0
SST8051 C9341 0.1UF 10% 6.3V XSR 201
DVI_HOTPLUG_DET_BUF
SST8051 R9340 10K 5% 1/20W MF 201
CRITICAL U9340 74LVC2G132 US8
SST8051 C9340 1UF 10% 6.3V CERM 603-1
10MS RC GENERATES ONE-SHOT LOW PULSE ON INT0# TO ALLOW PART TO WAKE UP AND XTAL TO START

SST8051 CRITICAL L9300 FERR-120-OHM-1.5A 0402-LF
PP3V3_S0_HDCP_F
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM VOLTAGE=3.3V
SST8051 C9302 0.01UF 10% 10V XSR 201
SST8051 C9301 0.1UF 10% 6.3V XSR 201
SST8051 CRITICAL C9300 10UF 20% 6.3V XSR 603

SST8051 C9390 22PF 5% 25V NP0-C0G 201
OMIT Y9390 14.318MHZ-35PPF-20PF SM-2.5X2.0MM
SST8051 C9391 22PF 5% 25V NP0-C0G 201

SST8051 C9326 0.1UF 10% 6.3V XSR 201
CRITICAL U9325 TC7SH00FEF SON SST8051
TMDS_HW_RESET_L
SST8051_SW_RESET_L
SST8051 R9325 10K 1% 1/20W MF 201

SST8051 CRITICAL U9300 SST89V54RD WQFN

DVI_HOTPLUG_DET_INT_L	7	(INT0#)P3.2	
TMDS_LINT_L	8	(INT1#)P3.3	
TP_SST8051_RXD	5	(RXD)P3.0	
SST8051_P34_AUDIO_CONFIG	9	(T0)P3.4	
NC	10	(T1)P3.5	
NC	12	(RD#)P3.7	
NC	11	(WR#)P3.6	
TP_SST8051_TXD	6	(TXD)P3.1	
SST8051_XTAL1	14	XTAL1	
SST8051_XTAL2	13	XTAL2	
SST8051_RST	4	RST	
SST8051_EA_L	26	EA*	
NC	25	ALE/PROG*	
SST8051_UPDATE_L	24	PSEN*	
		P0.0(AD0)	34
		P0.1(AD1)	33
		P0.2(AD2)	32
		P0.3(AD3)	31
		P0.4(AD4)	30 NC
		P0.5(AD5)	29
		P0.6(AD6)	28
		P0.7(AD7)	27
		P1.0(T2)	36 SST8051_UPDATE_L
		P1.1(T2_EX)	37 DVI_HOTPLUG_DET_BUF
		P1.2(ECI)	38 SST8051_DVI_HOTPLUG_DET
		P1.3(CEX0)	39 NC
		P1.4(CEX1/SS*)	40 SST8051_DDC_CLK
		(CEX2/MOSI)P1.5	1 SST8051_DDC_DATA
		(CEX3/MISO)P1.6	2
		(CEX4/SCK)P1.7	3
		A8(P2.0)	16 NC
		A9(P2.1)	17 NC
		A10(P2.2)	18 NC
		A11(P2.3)	19 NC
		A12(P2.4)	20 NC
		P2.5(A13)	21 SST8051_P25_AUDIO_CONFIG
		P2.6(A14)	22 NC
		P2.7(A15)	23 NC
		THRM_PAD	41
		VSS	15

PP3V3_B_S0
SST8051 R9302 2.2K 5% 1/20W MF 201
SST8051 R9303 2.2K 5% 1/20W MF 201
SST8051 R9304 2.2K 5% 1/20W MF 201
SST8051 R9305 2.2K 5% 1/20W MF 201
SST8051 R9306 4.7K 5% 1/20W MF 201
SST8051_DDC_EN
Q9300 SSM6N15FE SOT563
TMDS_DDC_SCL
TMDS_DDC_SDA
TMDS_LSCL
TMDS_LSDA

SST8051_UPDATE_L MAKE_BASE=TRUE SST8051_UPDATE_L
SST8051_UPDATE_L pulled up to 10K at SB
PP3V3_B_S0
SST8051 R9330 4.7K 1% 1/20W MF 201
SST8051_P25_AUDIO_CONFIG

AUDIO CONFIG OPTIONS

P25	P34	OPTION
0	0	HD AUDIO
0	1	SPDIF
1	0	NO AUDIO
1	1	RESERVED

PP3V3_B_S0
SST8051 R9301 10K 1% 1/20W MF 201
SST8051_EA_L
SST8051 R9333 4.7K 1% 1/20W MF 201

NO STUFF
R9350 0 5% 1/20W MF 201
SST8051_DVI_HOTPLUG_DET
DVI_HOTPLUG_DET
R9351 0 5% 1/20W MF 201
DVI_HOTPLUG_DET_BUF
STUFFING OPTION CHOOSES RAW OR CONTROLLER OUTPUT OF DVI_HOTPLUG_DET

HDCP uController

SYNC_MASTER= SYNC_DATE=

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SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 62 OF 73	

Video Connectors

TMDS(MICRO DVI) INTERFACE
EXTERNAL VIDEO (VGA) INTERFACE

NB VIDEO ALIASES

CRT_TVO_IREF = CRT_TVO_IREF
TV_A_DAC = TV_A_DAC
TV_B_DAC = TV_B_DAC
TV_C_DAC = TV_C_DAC
CRT_BLUE = CRT_BLUE
CRT_GREEN = CRT_GREEN
CRT_RED = CRT_RED
CRT_HSYNC_R = CRT_HSYNC_R
CRT_VSYNC_R = CRT_VSYNC_R

Isolation required for DVI power switch

A 1.3K OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND

R9469 1.3K 1% 1/20W MF 201 — CRT_TVO_IREF — GND

CRITICAL F9404 0.5AMP-13.2V SM-LF
PP5V_S0 → PP5V_S0_TMDS_FUSE
VOLTAGE=5V MIN_LINE_WIDTH=0.30 MM MIN_NECK_WIDTH=0.20 MM

L9444 600-OHM-300MA 0402
PP5V_S0_TMDS_FUSE → PP5V_S0_DVIPORT
VOLTAGE=5V MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM

C9404 0.1UF 10% 10V X5R 402

PP5V_S0_DVIPORT → PP5V_S0_DVIPORT_D
VOLTAGE=5V MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.2 MM

D9401 1SS418 SOD-723

PP3V3_A_S0
R9466 2.2K 5% 1/20W MF 201 — TV_DCONSEL<0>
R9467 2.2K 5% 1/20W MF 201 — TV_DCONSEL<1>

R9462 1K 5% 1/20W MF 201
R9463 1K 5% 1/20W MF 201

PP3V3_B_S0
R9480 10K 5% 1/20W MF 201 — DVI_HOST
HDMI_HOST
R9481 100K 5% 1/20W MF 201

TMDS_HTPLG
TMDS_DDC_SDA
TMDS_DDC_SCL
C9410 1000PF 10% 16V X7R 201
NOSTUFF C9411 100PF 5% 25V CERM 201
NOSTUFF C9412 100PF 5% 25V CERM 201

SB_CRT_TVOUT_MUX_L

PLACE R9450 R9451 CLOSE TO NB
TV_A_DAC
CRT_BLUE
R9450 150 1% 1/20W MF 201
R9451 150 1% 1/20W MF 201
GND VOLTAGE=0V

PLACE U9401 NEAR NB
PP3V3_A_S0
C9439 0.1UF 10% 10V X5R 201

U9401 FSAV430 DQFN
CRITICAL
VCC, S, 1B1, 1B2, 1A, 2B1, 2B2, 2A, OE*, 4B1, 4B2, 4A, 3B1, 3B2, 3A, NC, GND, THMPAD

PLACE R9452 R9453 CLOSE TO NB
TV_B_DAC
CRT_GREEN
R9452 150 1% 1/20W MF 201
R9453 150 1% 1/20W MF 201
GND VOLTAGE=0V

PLACE R9454 R9455 CLOSE TO NB
TV_C_DAC
CRT_RED
R9454 150 1% 1/20W MF 201
R9455 150 1% 1/20W MF 201
GND VOLTAGE=0V

EXT_C_R
EXT_Y_G
EXT_COMPVID_B

CRITICAL FL9400 210MHZ MEA2010P-SM

VGA_B
VGA_G
VGA_R

These nets connect to RIO connector J4200

TMDS_TX_CONN_P<2>
TMDS_TX_CONN_N<2>
TMDS_TX_CONN_P<1>
TMDS_TX_CONN_N<1>
TMDS_TX_CONN_P<0>
TMDS_TX_CONN_N<0>
TMDS_TX_CONN_CLK_P
TMDS_TX_CONN_CLK_N

CRITICAL L9405 90-OHM-100MA 1210-4SM1 — TMDS_TX_P<2> / TMDS_TX_N<2>
CRITICAL L9407 90-OHM-100MA 1210-4SM1 — TMDS_TX_P<1> / TMDS_TX_N<1>
CRITICAL L9406 90-OHM-100MA 1210-4SM1 — TMDS_TX_P<0> / TMDS_TX_N<0>
CRITICAL L9404 300-OHM-100MA 1210-4SM — TMDS_TX_CLK_P / TMDS_TX_CLK_N

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

PP3V3_B_S0
C9460 0.1UF 10% 6.3V X5R 201
CRITICAL U9404 SN74LVC2G125DCU VSSOP-8 (VCC, GND)

R9460 39 5% 1/20W MF 201 — CRT_HSYNC_R → CRT_HSYNC_LS_R
R9470 39 5% 1/20W MF 201 — CRT_HSYNC_LS → VGA_HSYNC
NOSTUFF C9442 33PF 5% 25V NP0-C0G 201

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

CRITICAL U9404 SN74LVC2G125DCU VSSOP-8 (VCC, GND)

R9461 39 5% 1/20W MF 201 — CRT_VSYNC_R → CRT_VSYNC_LS_R
R9471 39 5% 1/20W MF 201 — CRT_VSYNC_LS → VGA_VSYNC
NOSTUFF C9443 33PF 5% 25V NP0-C0G 201

Place components near J4200 unless otherwise noted

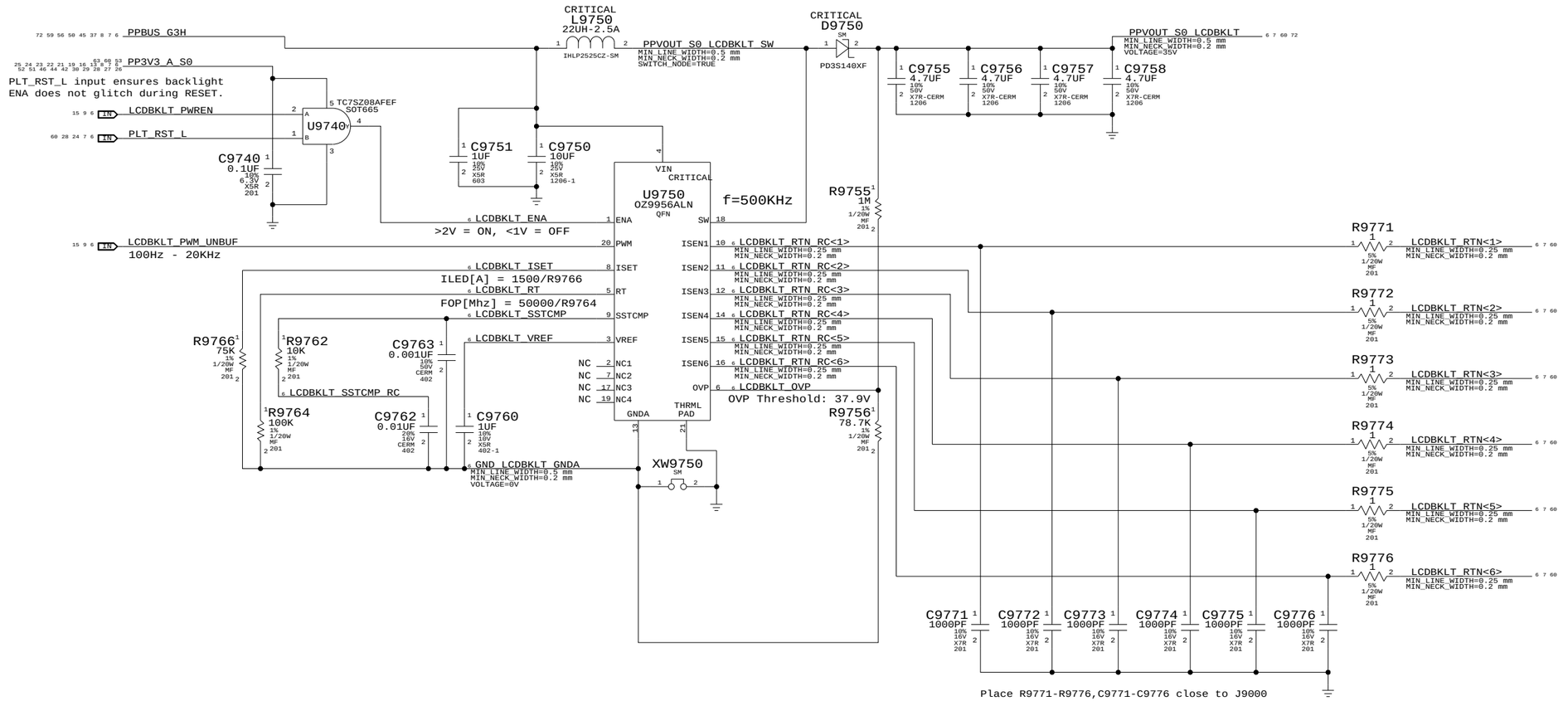
DVI CONNECTIONS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 63 OF 73	

LED Backlight Driver



LED Backlight Driver

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT: 64	OF: 73

ADDITIONAL CPU VCORE HF DECOUPLING

40x 1uF 0402

72 52 12 11 8 7 6 PPVCORE_S0_CPU

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

C9900	C9901	C9902	C9903	C9904	C9905	C9906	C9907	C9908	C9909
C9910	C9911	C9912	C9913	C9914	C9915	C9916	C9917	C9918	C9919
C9920	C9921	C9922	C9923	C9924	C9925	C9926	C9927	C9928	C9929
C9930	C9931	C9932	C9933	C9934	C9935	C9936	C9937	C9938	C9939

OMIT CRITICAL 2.2UF 20% 6.3V CERM 402-LF

ADDITIONAL GPU VCORE HF DECOUPLING

18x 1uF 0402

72 53 45 22 18 8 7 6 PPVCORE_S0_NB_GFX

C9980	C9981	C9982	C9983	C9984	C9985	C9986	C9987	C9988	C9989	
C9990	C9991	C9992	C9993	C9994	C9995	C9996	C9997			

OMIT 2.2UF 20% 6.3V CERM 402-LF

Additional CPU/GPU Decoupling

SYNC_MASTER= SYNC_DATE=

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	65	73

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	ISL3,ISL10	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_4MIL	*	0.100 MM	?
FSB_9MIL	*	0.228 MM	?
FSB_DATA	*	=FSB_4MIL	?
FSB_DATA2DATA	*	=FSB_4MIL	?
FSB_DSTB	*	=FSB_9MIL	?
FSB_DATA2DSTB	*	=FSB_9MIL	?
FSB_ADDR	*	=FSB_4MIL	?
FSB_ADDR2ADDR	*	=FSB_4MIL	?
FSB_ADSTB	*	=FSB_9MIL	?
FSB_ADDR2ADSTB	*	=FSB_9MIL	?
FSB_COMMON	*	=FSB_4MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?
CPU_THERMD	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	6 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	6 10
CPU_FERR_L	CPU_55S		CPU_FERR_L	6 10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	6 10 42 52
CPU_PWRGD	CPU_55S		CPU_PWRGD	6 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	6 10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	6 10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	6 10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_SMI_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	6 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	6 10 16 23 42
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	6 16 25 52
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	6 52
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	6 7 13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	6 7 13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	6 7 13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	6 10 16 23 52
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	6 10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	6 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	6 10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	6 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	6 10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	6 7 10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	6 7 10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	6 7 10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	6 7 10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	6 7 10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	6 7 10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	6 7 10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 29 30 71
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 29 30 71
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	6 7 13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	6 11 12 52
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	12
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	6 11 52
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	6 11 52
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	6 52
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	6 52
	CPU_70D	CPU_THERMD	CPU_THERMD_P	6 10 46
	CPU_70D	CPU_THERMD	CPU_THERMD_N	6 10 46

CPU/FSB Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 66 OF 73	

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
PCIE_R2D_2_PCIE_R2D	*	0.228 MM	?
PCIE_D2R_2_PCIE_D2R	*	0.228 MM	?
PCIE_R2D_2_PCIE_D2R	*	0.300 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_N2S_2_DMI_N2S	*	0.228 MM	?
DMI_S2N_2_DMI_S2N	*	0.228 MM	?
DMI_N2S_2_DMI_S2N	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_R2D_2_PCIE_R2D
PCIE_D2R	PCIE_D2R	*	PCIE_D2R_2_PCIE_D2R
PCIE_R2D	PCIE_D2R	*	PCIE_R2D_2_PCIE_D2R

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_N2S_2_DMI_N2S
DMI_S2N	DMI_S2N	*	DMI_S2N_2_DMI_S2N
DMI_N2S	DMI_S2N	*	DMI_N2S_2_DMI_S2N

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PWR	*	BUS2PWR_GND
PCIE_R2D	GND	*	BUS2PWR_GND
PCIE_D2R	PWR	*	BUS2PWR_GND
PCIE_D2R	GND	*	BUS2PWR_GND
DMI_N2S	PWR	*	BUS2PWR_GND
DMI_N2S	GND	*	BUS2PWR_GND
DMI_S2N	PWR	*	BUS2PWR_GND
DMI_S2N	GND	*	BUS2PWR_GND
LVDS	PWR	*	BUS2PWR_GND
LVDS	GND	*	BUS2PWR_GND
TMDS	PWR	*	BUS2PWR_GND
TMDS	GND	*	BUS2PWR_GND

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?
LVDS2LVDS	*	0.300 MM	?
TMDS	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC
LVDS	LVDS	*	LVDS2LVDS

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
PEG_R2D	PCIE_100D	PCIE_R2D	PEG_R2D_P<15..0>
	PCIE_100D	PCIE_R2D	PEG_R2D_N<15..0>
	PCIE_100D	PCIE_R2D	PEG_R2D_C_P<15..0> 6 15 61
	PCIE_100D	PCIE_R2D	PEG_R2D_C_N<15..0> 6 15 61
PEG_D2R	PCIE_100D	PCIE_D2R	PEG_D2R_P<15..0> 6 15 61
	PCIE_100D	PCIE_D2R	PEG_D2R_N<15..0> 6 15 61
	PCIE_100D	PCIE_D2R	PEG_D2R_C_P<15..0>
	PCIE_100D	PCIE_D2R	PEG_D2R_C_N<15..0>
DMI_N2S	DMI_100D	DMI_N2S	DMI_N2S_P<3..0> 6 16 24
	DMI_100D	DMI_N2S	DMI_N2S_N<3..0> 6 16 24
DMI_S2N	DMI_100D	DMI_S2N	DMI_S2N_P<3..0> 6 16 24
	DMI_100D	DMI_S2N	DMI_S2N_N<3..0> 6 16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P 6 15 60
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N 6 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0> 6 7 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0> 6 7 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_F_P<2..0> 6 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_F_N<2..0> 6 60
LVDS_A_DATA3	LVDS_100D	LVDS	NC_LVDS_A_DATA_P3 9
LVDS_A_DATA3	LVDS_100D	LVDS	NC_LVDS_A_DATA_N3 9
LVDS_B_CLK	LVDS_100D	LVDS	NC_LVDS_B_CLK_P 9 15
LVDS_B_CLK	LVDS_100D	LVDS	NC_LVDS_B_CLK_N 9 15
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>
LVDS_B_DATA3	LVDS_100D	LVDS	NC_LVDS_B_DATA_P3 9
LVDS_B_DATA3	LVDS_100D	LVDS	NC_LVDS_B_DATA_N3 9
LVDS_IBG		LVDS	LVDS_IBG 6 15 60
CRT_TVO_IREF		CRT	CRT_TVO_IREF 6 15 63
CRT_RED	CRT_50S	CRT	CRT_RED 6 15 63
CRT_GREEN	CRT_50S	CRT	CRT_GREEN 6 15 63
CRT_BLUE	CRT_50S	CRT	CRT_BLUE 6 15 63
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R 6 15 63
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R 6 15 63
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC 6 15 63
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC 6 15 63
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC 6 15 63
EXT_COMPVID_B	CRT_50S	CRT	EXT_COMPVID_B 6 63
EXT_Y_G	CRT_50S	CRT	EXT_Y_G 6 63
EXT_C_R	CRT_50S	CRT	EXT_C_R 6 63
VGA_R	CRT_50S	CRT	VGA_R 6 7 37 63
VGA_G	CRT_50S	CRT	VGA_G 6 7 37 63
VGA_B	CRT_50S	CRT	VGA_B 6 7 37 63
	PCIE_100D	PCIE_R2D	TMDS_SDB_P 6 61
	PCIE_100D	PCIE_R2D	TMDS_SDB_N 6 61
	PCIE_100D	PCIE_R2D	TMDS_SDC_P 6 61
	PCIE_100D	PCIE_R2D	TMDS_SDC_N 6 61
	PCIE_100D	PCIE_R2D	TMDS_SDG_P 6 61
	PCIE_100D	PCIE_R2D	TMDS_SDG_N 6 61
	PCIE_100D	PCIE_R2D	TMDS_SDR_P 6 61
	PCIE_100D	PCIE_R2D	TMDS_SDR_N 6 61
	TMDS_100D	TMDS	TMDS_TX_CLK_P 6 61 63
	TMDS_100D	TMDS	TMDS_TX_CLK_N 6 61 63
	PCIE_100D	PCIE_D2R	TMDS_INT_P 6 61
	PCIE_100D	PCIE_D2R	TMDS_INT_N 6 61
	TMDS_100D	TMDS	TMDS_TX_CONN_CLK_P 6 7 37 63
	TMDS_100D	TMDS	TMDS_TX_CONN_CLK_N 6 7 37 63
	TMDS_100D	TMDS	TMDS_CONN_P<3..0>
	TMDS_100D	TMDS	TMDS_CONN_N<3..0>
	TMDS_100D	TMDS	TMDS_TX_P<3..0> 6 61 63
	TMDS_100D	TMDS	TMDS_TX_N<3..0> 6 61 63
	SMB_55S	SMB	TMDS_DDC_SCL 6 7 37 61 62 63
	SMB_55S	SMB	TMDS_DDC_SDA 6 7 37 61 62 63

NB Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 67 OF 73	

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	ISL3,ISL10	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_87D	*	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=2.28:1_SPACING	?
MEM_CTRL2CTRL	*	=1:1_SPACING	?
MEM_CTRL2MEM	*	=2.28:1_SPACING	?
MEM_CMD2CMD	*	=1:1_SPACING	?
MEM_CMD2MEM	*	=2.28:1_SPACING	?
MEM_DATA2DATA	*	=1:1_SPACING	?
MEM_DATA2MEM	*	=2.28:1_SPACING	?
MEM_DQS2MEM	*	=2.28:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	NB_STATIC	*	PWR_P2MM
MEM_CTRL	NB_STATIC	*	PWR_P2MM
MEM_DATA	NB_STATIC	*	PWR_P2MM
MEM_DQS	NB_STATIC	*	PWR_P2MM
MEM_CMD	NB_STATIC	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	PWR	*	BUS2PWR_GND
MEM_CLK	GND	*	BUS2PWR_GND
MEM_CTRL	PWR	*	BUS2PWR_GND
MEM_CTRL	GND	*	BUS2PWR_GND
MEM_CMD	PWR	*	BUS2PWR_GND
MEM_CMD	GND	*	BUS2PWR_GND
MEM_DATA	PWR	*	BUS2PWR_GND
MEM_DATA	GND	*	BUS2PWR_GND
MEM_DQS	PWR	*	BUS2PWR_GND
MEM_DQS	GND	*	BUS2PWR_GND

I93	PP0V9_S3M_MEM_NBVREFB	NET_SPACING_TYPE=NB_STATIC 8 16 21
I95	PP0V9_S3M_MEM_NBVREFA	NET_SPACING_TYPE=NB_STATIC 8 16 21
I94	NB_VCCSM_LF1	NET_SPACING_TYPE=NB_STATIC 6 18
I96	NB_VCCSM_LF2	NET_SPACING_TYPE=NB_STATIC 6 18
I97	NB_VCCSM_LF3	NET_SPACING_TYPE=NB_STATIC 6 18
I98	NB_VCCSM_LF4	NET_SPACING_TYPE=NB_STATIC 6 18
I99	NB_VCCSM_LF5	NET_SPACING_TYPE=NB_STATIC 6 18
I101	NB_VCCSM_LF6	NET_SPACING_TYPE=NB_STATIC 6 18
I610	NB_VCCSM_LF7	NET_SPACING_TYPE=NB_STATIC 6 18
I102	PP1V8_S3	NET_SPACING_TYPE=PP1V8_MEM 6 7 8 16 18 21 31 32 34 35 51 55 72
	GND	NET_SPACING_TYPE=GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_87D	MEM_CLK	MEM_CLK_P<2..0>	16 31 33
	MEM_87D	MEM_CLK	MEM_CLK_N<2..0>	16 31 33
	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	6 16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<13..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	17 31
	MEM_87D	MEM_CLK	MEM_CLK_P<5..3>	16 32 33
	MEM_87D	MEM_CLK	MEM_CLK_N<5..3>	16 32 33
	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	6 16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<13..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	17 32

Memory Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 68 OF 73	

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	PWR	*	BUS2PWR_GND
USB	GND	*	BUS2PWR_GND

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	6 23 38
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	6 23 38
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	6 23 38
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	6 23 38
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ	6 23 38
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	6 23 38
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	6 23 38
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	
SATA_A_R2D	SATA_100D	SATA	NC_SATA_A_R2D_C_P	9 23
	SATA_100D	SATA	NC_SATA_A_R2D_C_N	9 23
	SATA_100D	SATA	SATA_A_R2D_P	
	SATA_100D	SATA	SATA_A_R2D_N	
SATA_A_D2R	SATA_100D	GND	NC_SATA_A_D2R_P	9
	SATA_100D	GND	NC_SATA_A_D2R_N	9
	SATA_100D	SATA	SATA_A_D2R_C_P	
	SATA_100D	SATA	SATA_A_D2R_C_N	
SATA_B_R2D	SATA_100D	SATA	NC_SATA_B_R2D_C_P	9 23
	SATA_100D	SATA	NC_SATA_B_R2D_C_N	9 23
	SATA_100D	SATA	SATA_B_R2D_P	
	SATA_100D	SATA	SATA_B_R2D_N	
SATA_A_D2R	SATA_100D	GND	NC_SATA_B_D2R_P	9
	SATA_100D	GND	NC_SATA_B_D2R_N	9
	SATA_100D	SATA	SATA_B_D2R_C_P	
	SATA_100D	SATA	SATA_B_D2R_C_N	
SATA_C_R2D	SATA_100D	SATA	NC_SATA_C_R2D_C_P	9 23
	SATA_100D	SATA	NC_SATA_C_R2D_C_N	9 23
	SATA_100D	SATA	SATA_C_R2D_P	
	SATA_100D	SATA	SATA_C_R2D_N	
SATA_A_D2R	SATA_100D	GND	NC_SATA_C_D2R_P	9
	SATA_100D	GND	NC_SATA_C_D2R_N	9
	SATA_100D	SATA	SATA_C_D2R_C_P	
	SATA_100D	SATA	SATA_C_D2R_C_N	
SATA_RBIAS	SATA_55S		SATA_RBIAS	
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	6 7 9 23 37
	HDA_55S	HDA	HDA_BIT_CLK_R	6 23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	6 7 9 23 37
	HDA_55S	HDA	HDA_SYNC_R	6 23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	6 9 23 37
	HDA_55S	HDA	HDA_RST_L_R	6 23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	6 7 9 23 37
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	6 7 9 23 37
	HDA_55S	HDA	HDA_SDOUT_R	6 23
USB_EXTA	USB_90D	USB	USB2_EXTA_P	6 9 24 39
	USB_90D	USB	USB2_EXTA_N	6 9 24 39
	USB_90D	USB	USB2_MUXED_EXTA_N	6 9 39
	USB_90D	USB	USB2_MUXED_EXTA_P	6 9 39
USB_MINI	USB_90D	USB	USB2_AIRPORT_P	6 9 24 36
	USB_90D	USB	USB2_AIRPORT_N	6 9 24 36
USB_EXTD	USB_90D	USB	TP_USB2_3G_P	9 24
	USB_90D	USB	TP_USB2_3G_N	9 24
USB_CAMERA	USB_90D	USB	USB2_CAMERA_P	6 9 24 60
	USB_90D	USB	USB2_CAMERA_N	6 9 24 60
USB_BT	USB_90D	USB	NC_USB_BT_P	9 24
	USB_90D	USB	NC_USB_BT_N	9 24
USB_TPAD	USB_90D	USB	USB2_WSPRING_P	6 7 9 24 40
	USB_90D	USB	USB2_WSPRING_N	6 7 9 24 40
USB_IR	USB_90D	USB	USB_IR_P	6 7 9 24 40
	USB_90D	USB	USB_IR_N	6 7 9 24 40
USB_EXTB	USB_90D	USB	NC_USB2_EXTB_P	9 24
	USB_90D	USB	NC_USB2_EXTB_N	9 24
USB_EXCARD	USB_90D	USB	TP_USB_EXCARD_P	9 24
	USB_90D	USB	TP_USB_EXCARD_N	9 24
USB_EXTC	USB_90D	USB	TP_USB_EXTC_P	9 24
	USB_90D	USB	TP_USB_EXTC_N	9 24
	USB_90D	USB	USB2_AIRPORT_P_F	6 36
	USB_90D	USB	USB2_AIRPORT_N_F	6 36
	USB_90D	USB	USB2_CAMERA_F_P	6 7 60
	USB_90D	USB	USB2_CAMERA_F_N	6 7 60
	USB_90D	USB	USB2_EXTA_F_P	6 7 37 39
	USB_90D	USB	USB2_EXTA_F_N	6 7 37 39
			USB2_3G_F_P	
			USB2_3G_F_N	
USB_RBIAS	USB_60S		USB_RBIAS	6 24
SMB_SB_SCL	SMB_55S	SMB	SMBUS_SB_SCL	6 25 29 44
SMB_SB_SDA	SMB_55S	SMB	SMBUS_SB_SDA	6 25 29 44
SMB_SB_ME_SCL	SMB_55S	SMB	SMBUS_SB_ME_SCL	6 25 44
SMB_SB_ME_SDA	SMB_55S	SMB	SMBUS_SB_ME_SDA	6 25 44
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	6 24 49
	SPI_55S	SPI	SPI_SCLK	
	SPI_55S	SPI	SPI_A_SCLK_R	6 43 49
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	6 24 49
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	6 43 49
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	6 24 43 49
	SPI_55S	SPI	SPI_A_SO_R	6 49
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0>	6 24 49
	SPI_55S	SPI	SPI_CE_L<0>	6 43 49
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>	6 24 43
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE NONE	SHT 69 OF 73	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5S	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?
PCIE_R2D	*	=PCIE	?
PCIE_D2R	*	=PCIE	?
PCIE_9MIL	*	0.228 MM	?
PCIE_12MIL	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_9MIL
PCIE_D2R	PCIE_D2R	*	PCIE_9MIL
PCIE_D2R	PCIE_R2D	*	PCIE_12MIL

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Platform LAN (Nineveh) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LAN_5S	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
GLAN_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CLK	*	=2.5:1_SPACING	?
ENET_GLAN	*	20 MILS	?
ENET_LAN	*	=1.5:1_SPACING	?
ENET_MDI	*	25 MILS	?

DG says 30 mils min separation.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_5S	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
PCI_AD	PCI_5S	PCI	PCI_AD<18..0> 9
PCI_AD19	PCI_5S	PCI	NC_PCI_AD<19> 9 24
PCI_AD20	PCI_5S	PCI	NC_PCI_AD<20> 9 24
PCI_AD	PCI_5S	PCI	PCI_AD<31..21> 9
PCI_AD	PCI_5S	PCI	NC_PCI_PAR 9 24
PCI_C_BE_L	PCI_5S	PCI	PCI_C_BE_L<3..0> 9
PCI_CNTL	PCI_5S	PCI	PCI_IRDY_L 6 24
PCI_CNTL	PCI_5S	PCI	PCI_DEVSEL_L 6 24
PCI_CNTL	PCI_5S	PCI	PCI_PERR_L 6 24
PCI_LOCK_L	PCI_5S	PCI	PCI_LOCK_L 6 24
PCI_CNTL	PCI_5S	PCI	PCI_SERR_L 6 24
PCI_CNTL	PCI_5S	PCI	PCI_STOP_L 6 24
PCI_CNTL	PCI_5S	PCI	PCI_TRDY_L 6 24
PCI_CNTL	PCI_5S	PCI	PCI_FRAME_L 6 24
PCI_FW_REQ_L	PCI_5S	PCI	PCI_FW_REQ_L 6 24
PCI_FW_GNT_L	PCI_5S	PCI	PCI_FW_GNT_L 6 24
PCI_REQ1_L	PCI_5S	PCI	PCI_REQ1_L 6 24
PCI_GNT1_L	PCI_5S	PCI	PCI_GNT1_L
PCI_REQ2_L	PCI_5S	PCI	PCI_REQ2_L 6 24
PCI_GNT2_L	PCI_5S	PCI	PCI_GNT2_L
INT_PIRQA_L	PCI_5S	PCI	INT_PIRQA_L 6 24
INT_PIRQB_L	PCI_5S	PCI	INT_PIRQB_L 6 24
INT_PIRQC_L	PCI_5S	PCI	INT_PIRQC_L 6 24
INT_PIRQD_L	PCI_5S	PCI	INT_PIRQD_L 6 24
INT_PIRQE_L	PCI_5S	PCI	INT_PIRQE_L 6 24
INT_PIRQF_L	PCI_5S	PCI	INT_PIRQF_L 6 24
PCIE_A_R2D	PCIE_100D	PCIE_R2D	PCIE_A_R2D_C_P
	PCIE_100D	PCIE_R2D	PCIE_A_R2D_C_N
PCIE_A_D2R	PCIE_100D	PCIE_D2R	PCIE_A_D2R_P
	PCIE_100D	PCIE_D2R	PCIE_A_D2R_N
PCIE_B_R2D	PCIE_100D	PCIE_R2D	PCIE_B_R2D_C_P
	PCIE_100D	PCIE_R2D	PCIE_B_R2D_C_N
PCIE_B_D2R	PCIE_100D	PCIE_D2R	PCIE_B_D2R_P
	PCIE_100D	PCIE_D2R	PCIE_B_D2R_N
			PCIE_EXCARD_R2D_C_P
			PCIE_EXCARD_R2D_C_N
			PCIE_EXCARD_D2R_P
			PCIE_EXCARD_D2R_N
			PCIE_FW_R2D_C_P
			PCIE_FW_R2D_C_N
			PCIE_FW_D2R_P
			PCIE_FW_D2R_N
PCIE_MINI_R2D	PCIE_100D	PCIE_R2D	PCIE_E_R2D_C_P 6 24 36
	PCIE_100D	PCIE_R2D	PCIE_E_R2D_C_N 6 24 36
PCIE_MINI_D2R	PCIE_100D	PCIE_D2R	PCIE_E_D2R_P 6 24 36
	PCIE_100D	PCIE_D2R	PCIE_E_D2R_N 6 24 36
			PCIE_ENET_R2D_C_P
			PCIE_ENET_R2D_C_N
			PCIE_ENET_D2R_P
			PCIE_ENET_D2R_N
GLAN_COMP			GLAN_COMP 6 23
ENET_KBIAS			NINEVEH_KBIAS_P
ENET_RBIAS			NINEVEH_RBIAS
(PCIE_ENET_R2D)	GLAN_100D	ENET_GLAN	ENET_GLAN_R2D_P
	GLAN_100D	ENET_GLAN	ENET_GLAN_R2D_N
(PCIE_ENET_D2R)	GLAN_100D	ENET_GLAN	ENET_GLAN_D2R_C_P
	GLAN_100D	ENET_GLAN	ENET_GLAN_D2R_C_N
ENET_LAN	LAN_5S	ENET_LAN	LAN_RSTSYNC
ENET_LAN	LAN_5S	ENET_LAN	LAN_R2D<2..0>
ENET_LAN	LAN_5S	ENET_LAN	LAN_D2R<2..0>
ENET_GLAN_CLK	LAN_5S	ENET_CLK	ENET_GLAN_CLK_R
	LAN_5S	ENET_CLK	ENET_GLAN_CLK
ENET_MDI0	ENET_100D	ENET_MDI	ENET_MDI_P<0>
	ENET_100D	ENET_MDI	ENET_MDI_N<0>
ENET_MDI1	ENET_100D	ENET_MDI	ENET_MDI_P<1>
	ENET_100D	ENET_MDI	ENET_MDI_N<1>
ENET_MDI2	ENET_100D	ENET_MDI	ENET_MDI_P<2>
	ENET_100D	ENET_MDI	ENET_MDI_N<2>
ENET_MDI3	ENET_100D	ENET_MDI	ENET_MDI_P<3>
	ENET_100D	ENET_MDI	ENET_MDI_N<3>
CLINK_NB	CLINK_5S	CLINK	CLINK_NB_CLK 6 16 25
CLINK_NB	CLINK_5S	CLINK	CLINK_NB_DATA 6 16 25
CLINK_NB_RESET_L	CLINK_5S	CLINK	CLINK_NB_RESET_L 6 16 25
CLINK_WLAN	CLINK_5S	CLINK	CLINK_WLAN_CLK
CLINK_WLAN	CLINK_5S	CLINK	CLINK_WLAN_DATA
CLINK_WLAN_RESET_L	CLINK_5S	CLINK	CLINK_WLAN_RESET_L
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF 6 16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0 6 25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1 6 25

SB Constraints (2 of 2)

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 70 OF 73	

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	PWR	*	BUS2PWR_GND
CLK_FSB	GND	*	BUS2PWR_GND
CLK_PCIE	PWR	*	BUS2PWR_GND
CLK_PCIE	GND	*	BUS2PWR_GND
CLK_MED	PWR	*	BUS2PWR_GND
CLK_MED	GND	*	BUS2PWR_GND

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	6 10 29 30 71
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	6 10 29 30 71
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	6 14 29 30 71
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	6 14 29 30 71
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 29 30 66 71
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 29 30 66 71
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	6 29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	6 29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	6 9 16 29 30 71
	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	6 9 16 29 30 71
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	6 9 16 29 30 71
	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	6 9 16 29 30 71
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	6 24 29 30 71
	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	6 24 29 30 71
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	6 16 29 30 71
	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	6 16 29 30 71
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	6 29 30 36 71
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	6 29 30 36 71
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	6 10 29 30 71
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	6 10 29 30 71
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	6 14 29 30 71
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	6 14 29 30 71
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 29 30 66 71
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 29 30 66 71
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	6 30 43
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	6 24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	6 30 41
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	6 25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	6 25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	6 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	6 30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	6 9 16 29 30 71
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	6 9 16 29 30 71
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	6 9 16 29 30 71
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	6 9 16 29 30 71
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	6 24 29 30 71
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	6 24 29 30 71
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	
(CK505_SRC4)	SATA_100D	GND	SB_CLK100M_SATA_P	
(CK505_SRC4)	SATA_100D	GND	SB_CLK100M_SATA_N	
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	6 16 29 30 71
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	6 16 29 30 71
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	6 29 30 36 71
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	6 29 30 36 71
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	6 7 36 40 41 44
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	6 7 36 40 41 44
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	6 7 41 44 46
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	6 7 41 44 46
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	6 7 41 44 50 59
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	6 7 41 44 50 59
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	6 41 44 48
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	6 41 44 48

Clock & SMC Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE NONE SHT 71 OF 73

1	PPBUS_G3H	NET_SPACING_TYPE=PWR 6 7 8 37 45 50 56 59 64
2	PPBUS_R_G3H	NET_SPACING_TYPE=PWR 6 7 8 42 52 53 54 55 59
3	PPDCIN_G3H	NET_SPACING_TYPE=PWR 6 7 8 50 57
4	PPDCIN_G3H_R	NET_SPACING_TYPE=PWR 6 50
5	PPVBATT_G3H_R	NET_SPACING_TYPE=PWR 6 50
6	PPVBAT_G3H_CHGR_OUT	NET_SPACING_TYPE=PWR 6 59
7	PPVBAT_G3H_CHGR_REG	NET_SPACING_TYPE=PWR 6 59
8	PPVBAT_G3H_CHRGR_REG_R	NET_SPACING_TYPE=PWR 6 59
10	PPVBAT_G3H_CHRGR_REG_0	NET_SPACING_TYPE=PWR 6 59
9	PPVCORE_S0_CPU	NET_SPACING_TYPE=PWR 6 7 8 11 12 52 65
12	PPVCORE_S0_NB_GFX	NET_SPACING_TYPE=PWR 6 7 8 18 22 45 53 65
11	PPVDCIN_G3H_PRE	NET_SPACING_TYPE=PWR 6 45 59
13	PPVDCIN_G3H_PRE_R	NET_SPACING_TYPE=PWR 6 59
14	PPVDCIN_G3H_PRE_0	NET_SPACING_TYPE=PWR 6 59
16	PPVDCIN_G3H_PRE2	NET_SPACING_TYPE=PWR 6 59
15	PPVIN_S5_IMVP6_VIN	NET_SPACING_TYPE=PWR 6 52
18	PPVOUT_S0_LCDBKLT	NET_SPACING_TYPE=PWR 6 7 60 64
17	PPVOUT_S0_LCDBKLT_SW	NET_SPACING_TYPE=PWR 6 64
19	PP0V9_S0	NET_SPACING_TYPE=PWR 6 7 8 33 55
21	PP0V9_S3	NET_SPACING_TYPE=PWR 6 8 31 32 55
20	PP1V5_S0	NET_SPACING_TYPE=PWR 6 7 8 11 12 22 26 27 54
23	PP1V5_S0_NB_QDAC	NET_SPACING_TYPE=PWR 6 22
160	PP1V5_S0_NB_VCCD_CRT	NET_SPACING_TYPE=PWR 6 19 22
161	PP1V5_S0_NB_VCCD_QDAC	NET_SPACING_TYPE=PWR 6 19 22
22	PP1V5_S0_NB_VCCDMIPLL	NET_SPACING_TYPE=PWR
24	PP1V5_S0_NB_VCCDMIPLL_F	NET_SPACING_TYPE=PWR
25	PP1V5_S0_SB_VCCDMIPLL	NET_SPACING_TYPE=PWR 6 26 27
26	PP1V5_S0_SB_VCCDMIPLL_F	NET_SPACING_TYPE=PWR 6 27
28	PP1V5_S0_SB_VCCSATAPLL	NET_SPACING_TYPE=PWR 6 26 27
27	PP1V5_S0_SB_VCC1_5_B	NET_SPACING_TYPE=PWR 6 23 24 26 27
30	PP1V8_S0	NET_SPACING_TYPE=PWR 6 7 8 19 22 51 61
29	PP1V8_S0_ANALOG_SDVO_F	NET_SPACING_TYPE=PWR 6 61
31	PP1V8_S0_ANALOG_TMDS_F	NET_SPACING_TYPE=PWR 6 61
33	PP1V8_S0_NB_VCCTXLVDS	NET_SPACING_TYPE=PWR 6 19 22
32	PP1V8_S0_PVCC1_TMDS_F	NET_SPACING_TYPE=PWR 6 61
35	PP1V8_S0_PVCC2_TMDS_F	NET_SPACING_TYPE=PWR 6 61
34	PP1V8_S0_TMDS_F	NET_SPACING_TYPE=PWR 6 61
36	PP1V8_S3	NET_SPACING_TYPE=PWR 6 7 8 16 18 21 31 32 34 35 51 55 68
38	PP1V8_S3M_NB_VCCSMCK	NET_SPACING_TYPE=PWR 6 19 21
37	PP1V8_S3_NB_VCCSMCK_RC	NET_SPACING_TYPE=PWR 6 21
39	PP1V05_S0	NET_SPACING_TYPE=PWR 6 7 8 10 11 12 13 14 18 19 21 23 26 27 38 42 54
141	PP1V05_S0_NB_VCCPEG	NET_SPACING_TYPE=PWR 6 15 19 21
140	PP1V25_S0	NET_SPACING_TYPE=PWR 6 7 8 16 18 19 21 26 27 51 57
143	PP1V25_S0M_NB_VCCA_HPLL	NET_SPACING_TYPE=PWR 6 19 21
142	PP1V25_S0_NB_DPLL	NET_SPACING_TYPE=PWR 6 22
144	PP1V25_S0_NB_PEGPLL	NET_SPACING_TYPE=PWR 6 19 21
146	PP1V25_S0_NB_PEGPLL_RC	NET_SPACING_TYPE=PWR 6 21
145	PP1V25_S0_NB_VCCA_DPLLA	NET_SPACING_TYPE=PWR 6 19 22
148	PP1V25_S0_NB_VCCA_DPLLB	NET_SPACING_TYPE=PWR 6 19 22
147	PP3V3_LCDVDD_SW	NET_SPACING_TYPE=PWR 6 60
149	PP3V3_LCDVDD_SW_F	NET_SPACING_TYPE=PWR 6 7 60
150	PP3V3_S0	NET_SPACING_TYPE=PWR 7
152	PP3V3_S0_ANALOG_SDVO_F	NET_SPACING_TYPE=PWR 6 61
151	PP3V3_S0_CK505_VDDA	NET_SPACING_TYPE=PWR 6
154	PP3V3_S0_CK505_VDDA_R	NET_SPACING_TYPE=PWR 6
153	PP3V3_S0_CK505_VDD_CPU_SRC	NET_SPACING_TYPE=PWR 6 29
155	PP3V3_S0_CK505_VDD_PCI	NET_SPACING_TYPE=PWR 6
157	PP3V3_S0_CK505_VDD_REF	NET_SPACING_TYPE=PWR 6
156	PP3V3_S0_CK505_VDD48	NET_SPACING_TYPE=PWR 6
159	PP3V3_S0_IMVP6_3V3	NET_SPACING_TYPE=PWR 6 52
158	PP3V3_S0_LCD_F	NET_SPACING_TYPE=PWR 6 7 60
160	PP3V3_S0_NBCORE_FOLLOW_R	NET_SPACING_TYPE=PWR 6 21
162	PP3V3_S0_NB_CRTDAC_F	NET_SPACING_TYPE=PWR 6 22
161	PP3V3_S0_NB_TVDAC	NET_SPACING_TYPE=PWR 6 22
163	PP3V3_S0_NB_TVDAC_F	NET_SPACING_TYPE=PWR 6 22
165	PP3V3_S0_NB_TVDAC_FOLLOW	NET_SPACING_TYPE=PWR 6 22
164	PP3V3_S0_NB_VCCA_CRTDAC	NET_SPACING_TYPE=PWR 6 19 22
167	PP3V3_S0_NB_VCCA_DAC_BG	NET_SPACING_TYPE=PWR 6 19 22
166	PP3V3_S0_NB_VCCA_TVDACA	NET_SPACING_TYPE=PWR 6 19 22
168	PP3V3_S0_NB_VCCA_TVDACB	NET_SPACING_TYPE=PWR 6 19 22
170	PP3V3_S0_NB_VCCA_TVDACC	NET_SPACING_TYPE=PWR 6 19 22
169	PP3V3_S0_SPVCC_TMDS_F	NET_SPACING_TYPE=PWR 6 61
172	PP3V3_S3	NET_SPACING_TYPE=PWR 6 7 8 36 42 44 48 51 58 60
171	PP3V3_S3_AP_AUX	NET_SPACING_TYPE=PWR 6 7 36
173	PP3V3_S3_TOPCASE_F	NET_SPACING_TYPE=PWR
174	PP3V3_S5	NET_SPACING_TYPE=PWR 6 7 16 24 25 26 27 28 36 43 44 49 51 52 57 58 60
176	PP3V3_S5_AVREF_SMC	NET_SPACING_TYPE=PWR 6 41 42
175	PP3V3_S5_SMC_AVCC	NET_SPACING_TYPE=PWR 6 41
178	PP3V42G3H_SW	NET_SPACING_TYPE=PWR 6 57
177	PP3V42_G3H	NET_SPACING_TYPE=PWR 6 7 8 23 26 27 28 39 40 41 42 43 44 57 59
179	PP3V42_G3H_SMC_F	NET_SPACING_TYPE=PWR
181	PP3V42_G3H_SMCUSBMUX_R	NET_SPACING_TYPE=PWR 6 39
180	PP4V5_AUDIO_ANALOG	NET_SPACING_TYPE=PWR
183	PP5V_S0	NET_SPACING_TYPE=PWR 6 7 8 22 27 40 43 47 51 52 53 63
182	PP5V_S0_AUDIO	NET_SPACING_TYPE=PWR
184	PP5V_S0_AUDIO_AMP	NET_SPACING_TYPE=PWR
186	PP5V_S0_DVIPORT	NET_SPACING_TYPE=PWR 6 7 37 63
185	PP5V_S0_DVIPORT_D	NET_SPACING_TYPE=PWR 6 63
187	PP5V_S0_IMVP6_VDD	NET_SPACING_TYPE=PWR 6 52
189	PP5V_S0_KBDLED_F	NET_SPACING_TYPE=PWR 6 7 40
188	PP5V_S0_SB_V5REF	NET_SPACING_TYPE=PWR 6 26 27
191	PP5V_S0_TMDS_FUSE	NET_SPACING_TYPE=PWR 6 63
190	PP5V_S0_3G_F	NET_SPACING_TYPE=PWR
192	PP5V_S3	NET_SPACING_TYPE=PWR 6 7 8 40 58 60
194	PP5V_S3_CAMERA_F	NET_SPACING_TYPE=PWR 6 7 60
193	PP5V_S3_IR_F	NET_SPACING_TYPE=PWR
196	PP5V_S3_USB2_EXTA	NET_SPACING_TYPE=PWR 6 39
195	PP5V_S3_USB2_EXTA_F	NET_SPACING_TYPE=PWR 6 7 37 39
197	PP5V_S5	NET_SPACING_TYPE=PWR 6 7 8 27 39 51 54 55 56 58
198	PP5V_S5_SB_V5REF_SUS	NET_SPACING_TYPE=PWR 6 26 27
199	PP18V5_DCIN	NET_SPACING_TYPE=PWR 6 7 50
1102	PP18V5_DCIN_ONEWIRE	NET_SPACING_TYPE=PWR 6 50
1103	PP18V5_G3H	NET_SPACING_TYPE=PWR 6 7 8 50 59
1104	PP18V5_S5_CHGR_SW_R	NET_SPACING_TYPE=PWR 6 59

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR	*	=STANDARD	?
BUS2PWR_GND	*	0.228 MM	?

M82 Power and Ground Nets

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 72 OF 73	

M82 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,ISL12,ISL13,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL2,ISL4,ISL5	Y	0.215 MM	0.215 MM			
27P4_OHM_SE	ISL10,ISL11,ISL13	Y	0.215 MM	0.215 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.290 MM	0.290 MM			
45_OHM_SE	ISL2,ISL4,ISL5	Y	0.091 MM	0.091 MM			
45_OHM_SE	ISL10,ISL11,ISL13	Y	0.091 MM	0.091 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.235 MM	0.235 MM			
50_OHM_SE	ISL2,ISL4,ISL5	Y	0.070 MM	0.070 MM			
50_OHM_SE	ISL10,ISL11,ISL13	Y	0.070 MM	0.070 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.190 MM	0.190 MM			
55_OHM_SE	ISL2,ISL4,ISL5	Y	0.070 MM	0.070 MM	55OHM SE ON INTERNAL LAYERS NOT ACHIEVABLE IN M82 STACKUP USING 50OHM SE		
55_OHM_SE	ISL10,ISL11,ISL13	Y	0.070 MM	0.070 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.310 MM	0.310 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM
70_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	TOP,BOTTOM	Y	0.230 MM	0.230 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM
85_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
87_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
87_OHM_DIFF	TOP,BOTTOM	Y	0.220 MM	0.220 MM		0.180 MM	0.180 MM
87_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM
87_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.190 MM	0.190 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
90_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.170 MM		0.205 MM	0.205 MM
100_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM
100_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

M82 Rule Definitions

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	73	73