

MODEL NAME : *PLW00*

PCB NO : *LA-7451P*

BOM P/N : *TBD*
TBD

www.laptopblue.vn

Dell/Compal Confidential

Schematic Document

Breitling (Huron River)

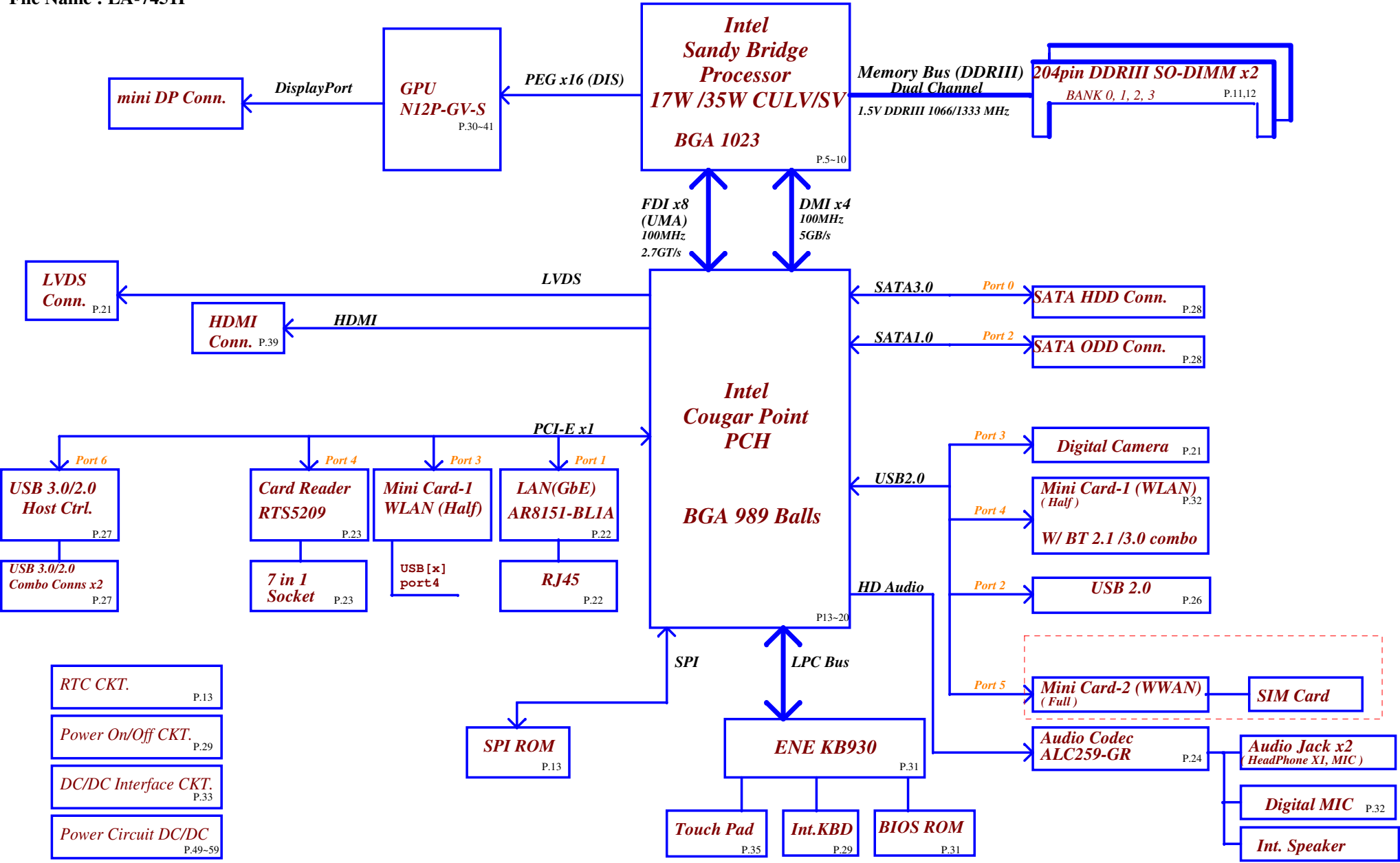
Sandy Bridge (BGA) + Cougar Point (standard)

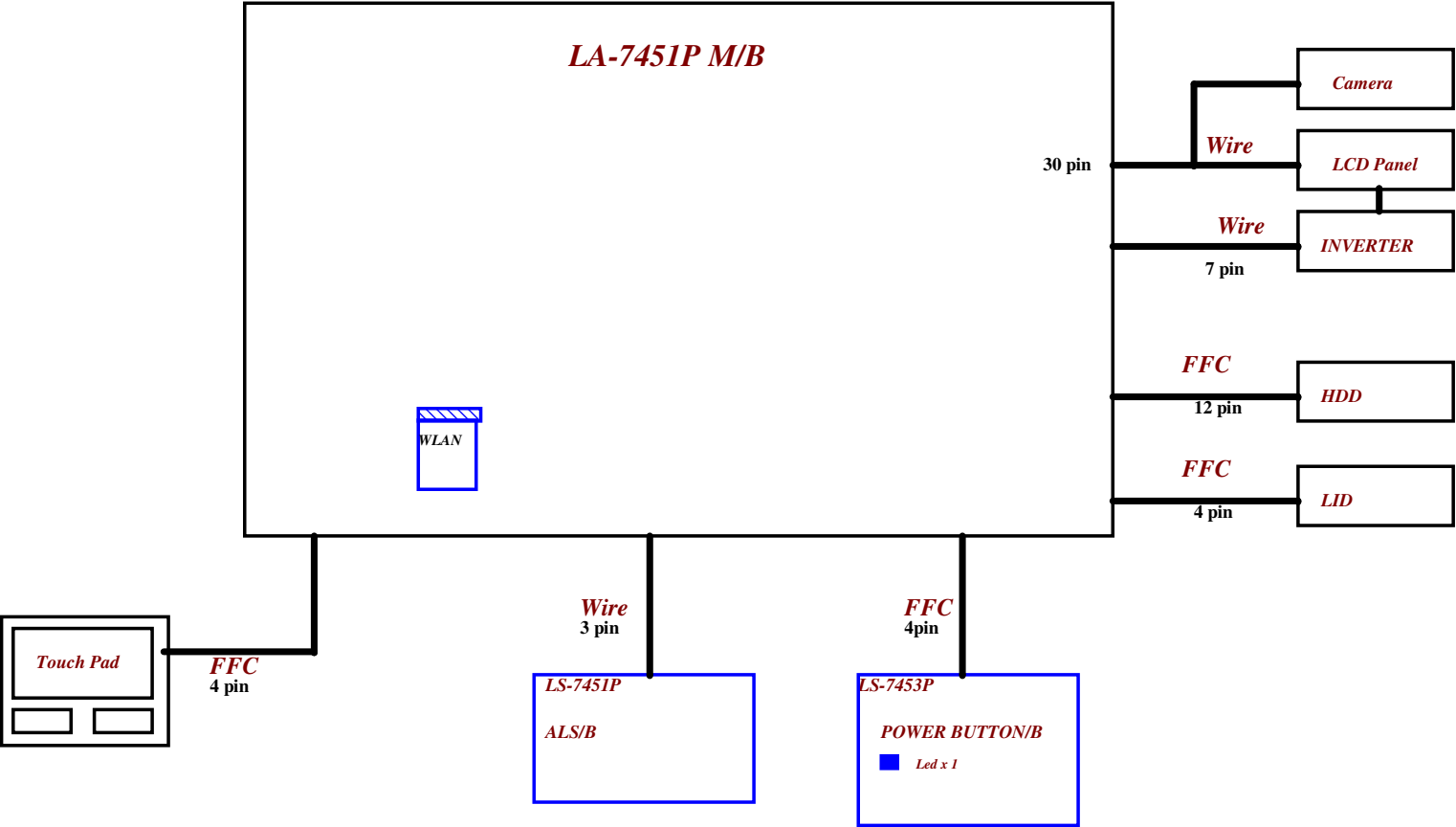
DISCRETE VGA N12P-GV-S-A1 (optimus)

2011-07-12

Rev: 1.0

| | | | | | |
|---|------------|--------------------|------------|--------------------------|-------------------------|
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| | | | | | LA-7451P |
| | | | | Date | Thursday, July 28, 2011 |
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| | | | | Rev | 1.0 |





Board ID Table for AD channel

| | | | | | |
|----------|-------------|-------------|-------------|-------------|-----------|
| Vcc | 3.3V +/- 5% | | | | |
| Ra | 100K +/- 5% | | | | |
| Board ID | Rb | VAD_BID min | VAD_BID typ | VAD_BID max | EC AD3 |
| 0 | 0 | 0 V | 0 V | 0.155 V | 0x00-0x0C |
| 1 | 8.2K +/- 5% | 0.168 V | 0.250 V | 0.362 V | 0x0D-0x1C |
| 2 | 18K +/- 5% | 0.375 V | 0.503 V | 0.621 V | 0x1D-0x30 |
| 3 | 33K +/- 5% | 0.634 V | 0.819 V | 0.945 V | 0x31-0x49 |
| 4 | 56K +/- 5% | 0.958 V | 1.185 V | 1.359 V | 0x4A-0x69 |
| 5 | 100K +/- 5% | 1.372 V | 1.650 V | 1.838 V | 0x6A-0x8E |
| 6 | 200K +/- 5% | 1.851 V | 2.200 V | 2.420 V | 0x8F-0xBB |
| 7 | NC | 2.433 V | 3.300 V | 3.300 V | 0xBC-0xFF |

SMBUS Control Table

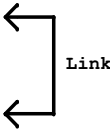
| | SOURCE | BATT | SODIMM | SODIMM | FFS | VGA Thermal Sensor | XDP | Charger |
|-----------------------------|--------|------|--------|--------|-----|--------------------|-----|---------|
| EC_SMB_CK1 EC_SMB_DA1 | KB930 | V | | | | | | |
| EC_SMB_CK2 EC_SMB_DA2 | KB930 | | | | | | | |
| PCH_SML0CLK PCH_SML0DATA | PCH | | | | | | | |
| PCH_SML1CLK PCH_SML1DATA | PCH | | | | | | V | |
| MEM_SMBCLK MEM_SMBDATA | PCH | | V | V | V | | | V |

BOARD ID Table

| Board ID | PCB Revision |
|----------|--------------|
| 0 | 0.1 |
| 1 | 0.2 |
| 2 | 0.3 |
| 3 | 0.4 |
| 4 | 0.5 |
| 5 | |
| 6 | |
| 7 | |

PCH

| USB PORT# | DESTINATION |
|-----------|-------------------------|
| 0 | None |
| 1 | JUSB1 (2.0 Ext UP Side) |
| 2 | None |
| 3 | CAMERA |
| 4 | JMINI1 (WLAN) |
| 5 | JMINI2 (WWAN) |
| 6 | None |
| 7 | None |
| 8 | None |
| 9 | None |
| 10 | None |
| 11 | None |
| 12 | None |
| 13 | None |

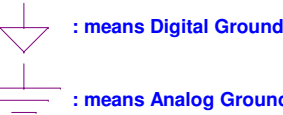


| CLKOUT | DESTINATION |
|--------|--------------|
| PCI0 | PCH_LOOPBACK |
| PCI1 | EC LPC |
| PCI2 | None |
| PCI3 | None |
| PCI4 | None |

| SATA | DESTINATION |
|-------|-------------|
| SATA0 | HDD |
| SATA1 | ODD |
| SATA2 | None |
| SATA3 | None |
| SATA4 | None |
| SATA5 | None |

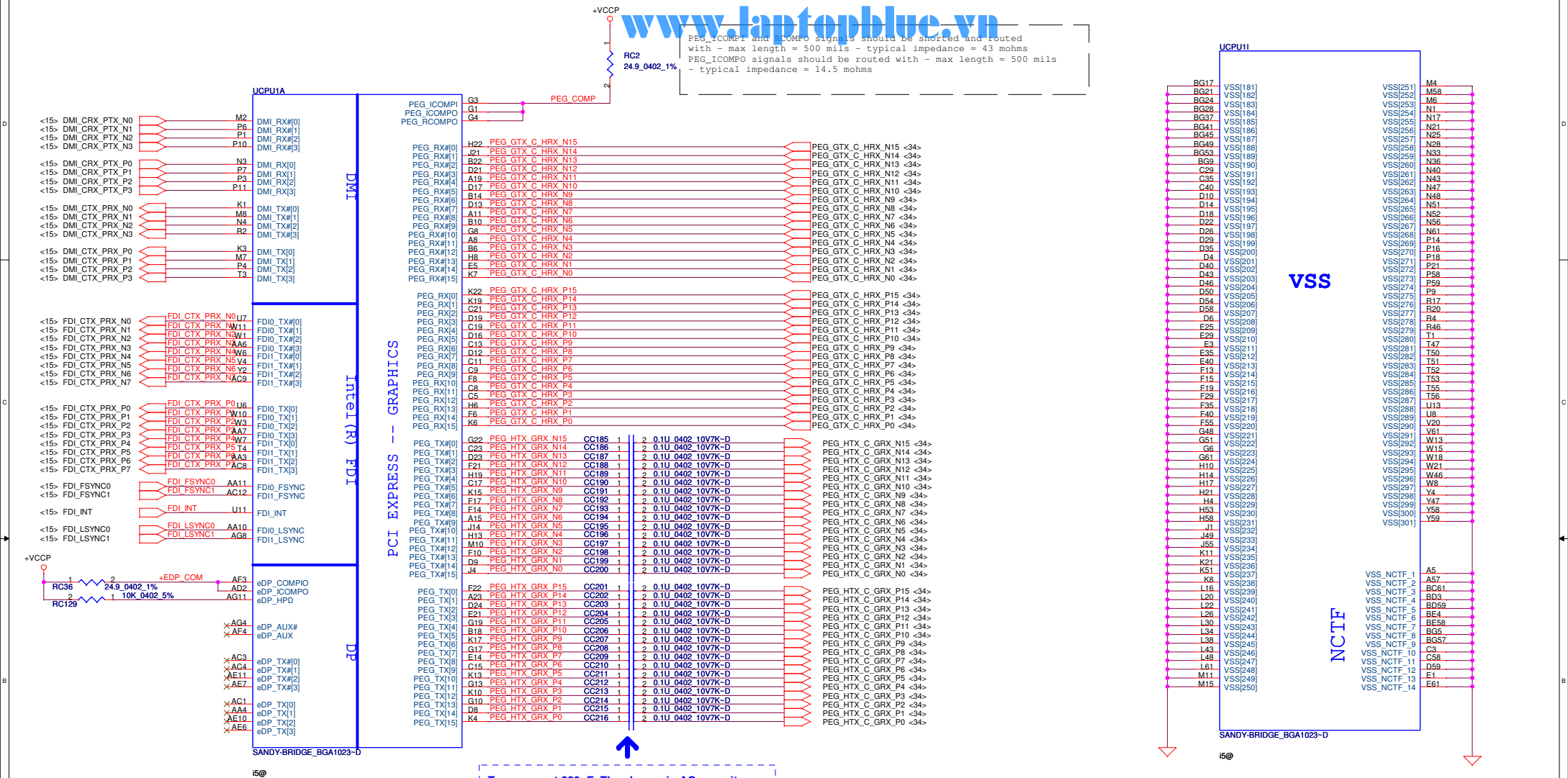
| PCI EXPRESS | DESTINATION |
|-------------|------------------|
| Lane 1 | 10/100/1G LAN |
| Lane 2 | None |
| Lane 3 | MINI CARD-1 WLAN |
| Lane 4 | CARD READER |
| Lane 5 | None |
| Lane 6 | USB 3.0 |
| Lane 7 | None |
| Lane 8 | None |

Symbol Note :

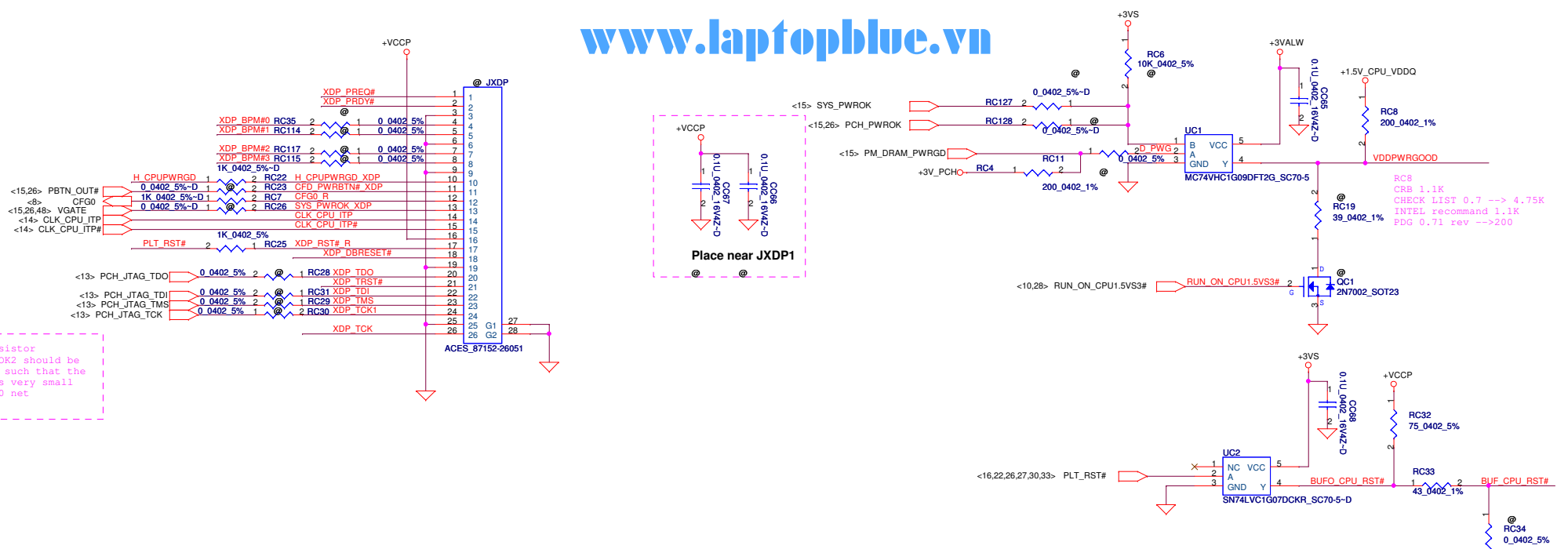


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| | | | | Size | Document Number | Rev |
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| | | | | Date: | Thursday, July 28, 2011 | Sheet 4 of 49 |

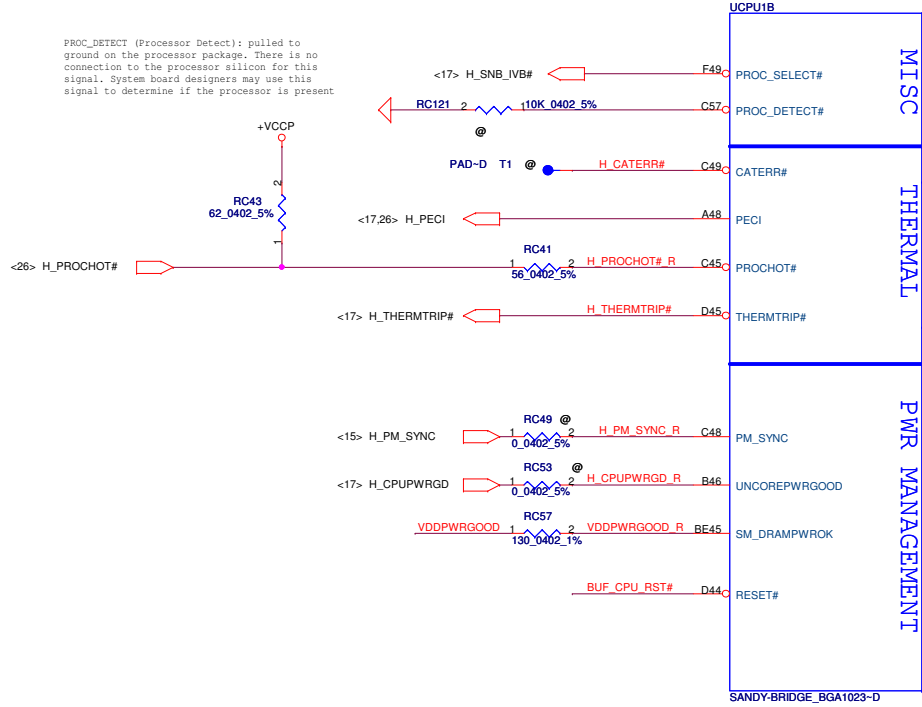
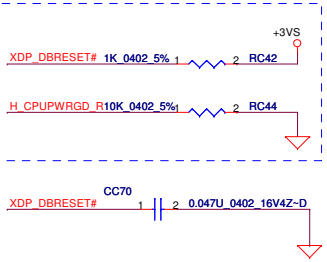
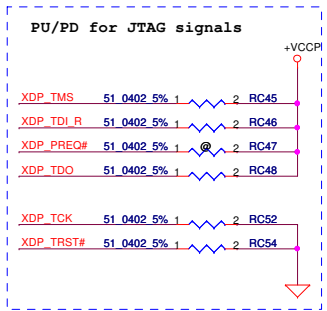
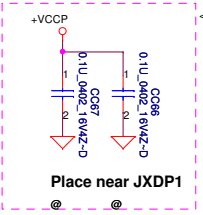
PEG_ICOMP1 and ICOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



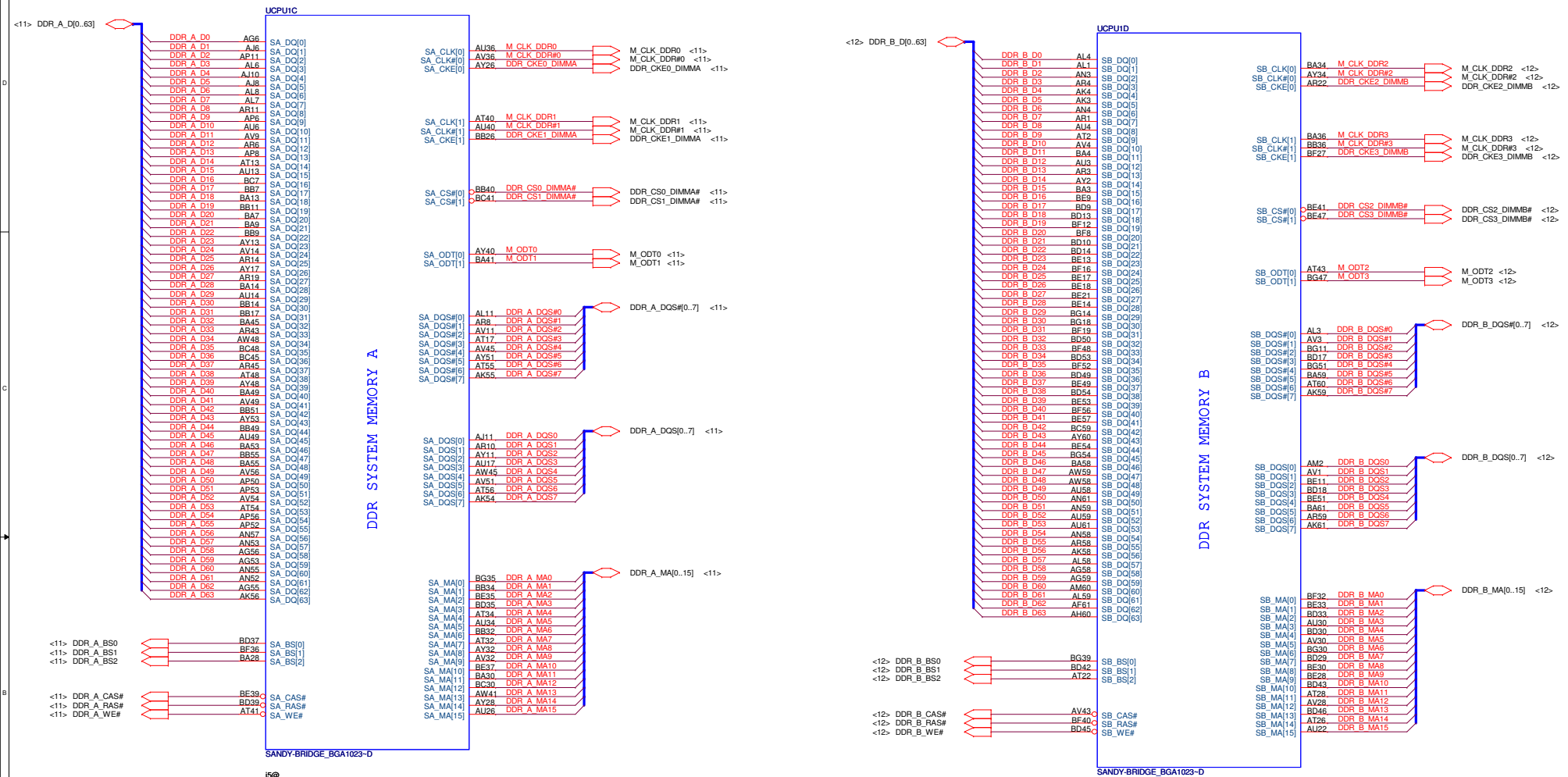
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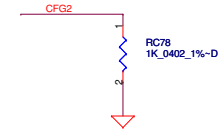
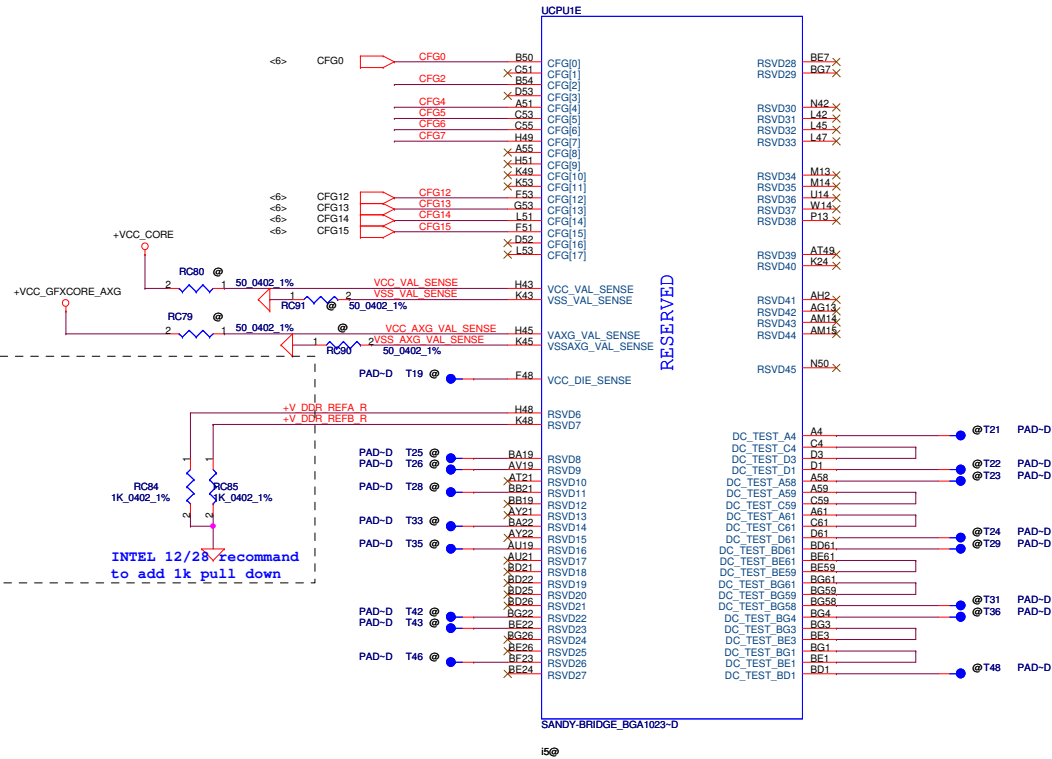
The resistor for HOOK2 should be placed such that the stub is very small on CFG0 net



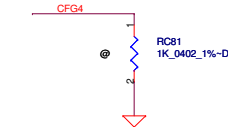
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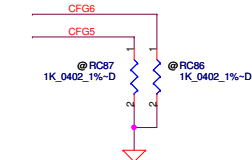
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| Issued Date | 2010/12/20 | Deciphered Date | 2011/12/20 | Title | PROCESSOR(3/6) DDRIII |
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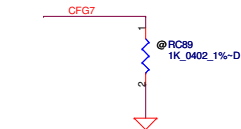
| PEG Static Lane Reversal - CFG2 is for the 16x | |
|--|--|
| CFG2 | <p>★1: (Default) Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p> |



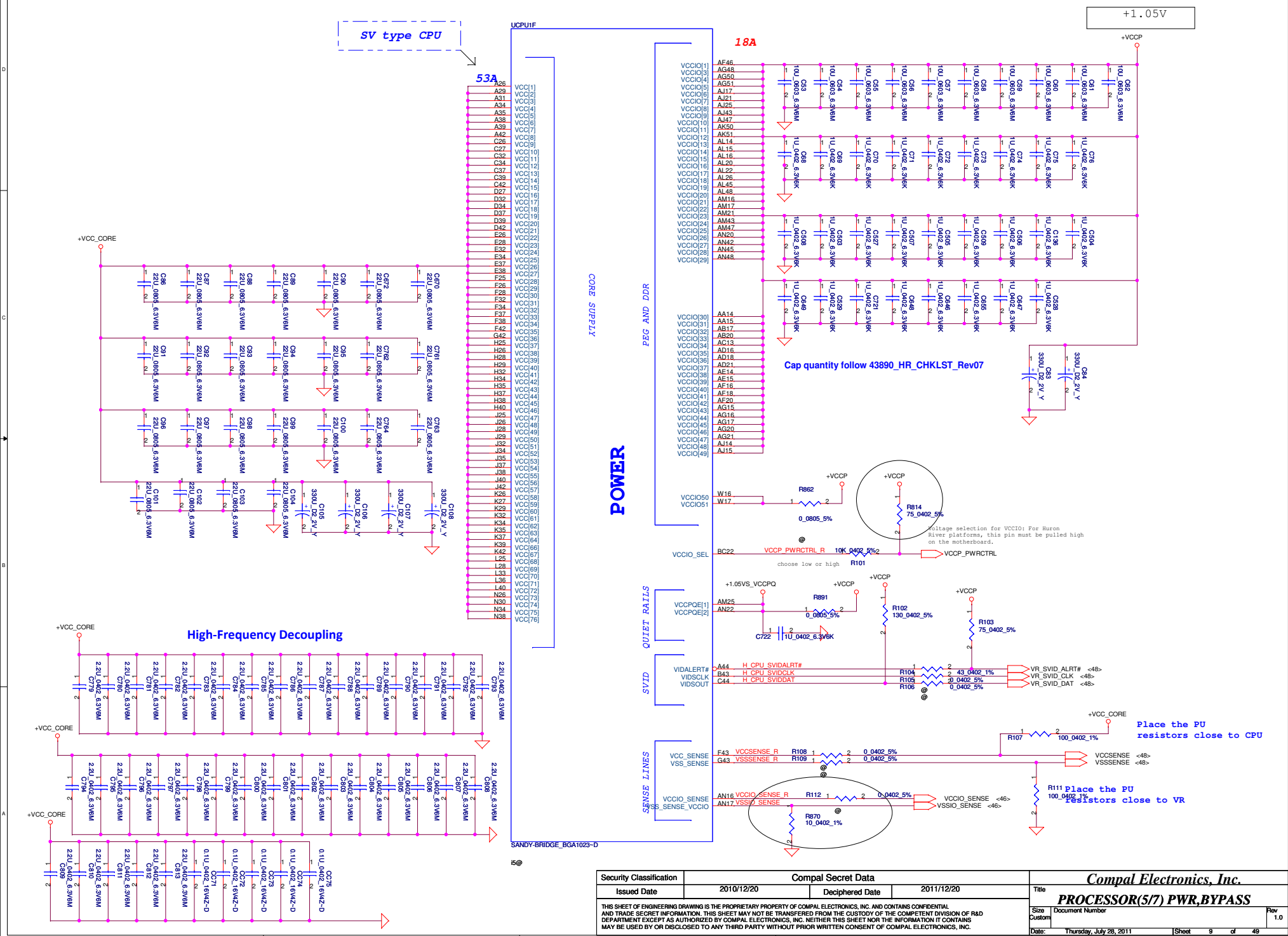
| Display Port Presence Strap | |
|-----------------------------|--|
| CFG4 | <p>★1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p> |

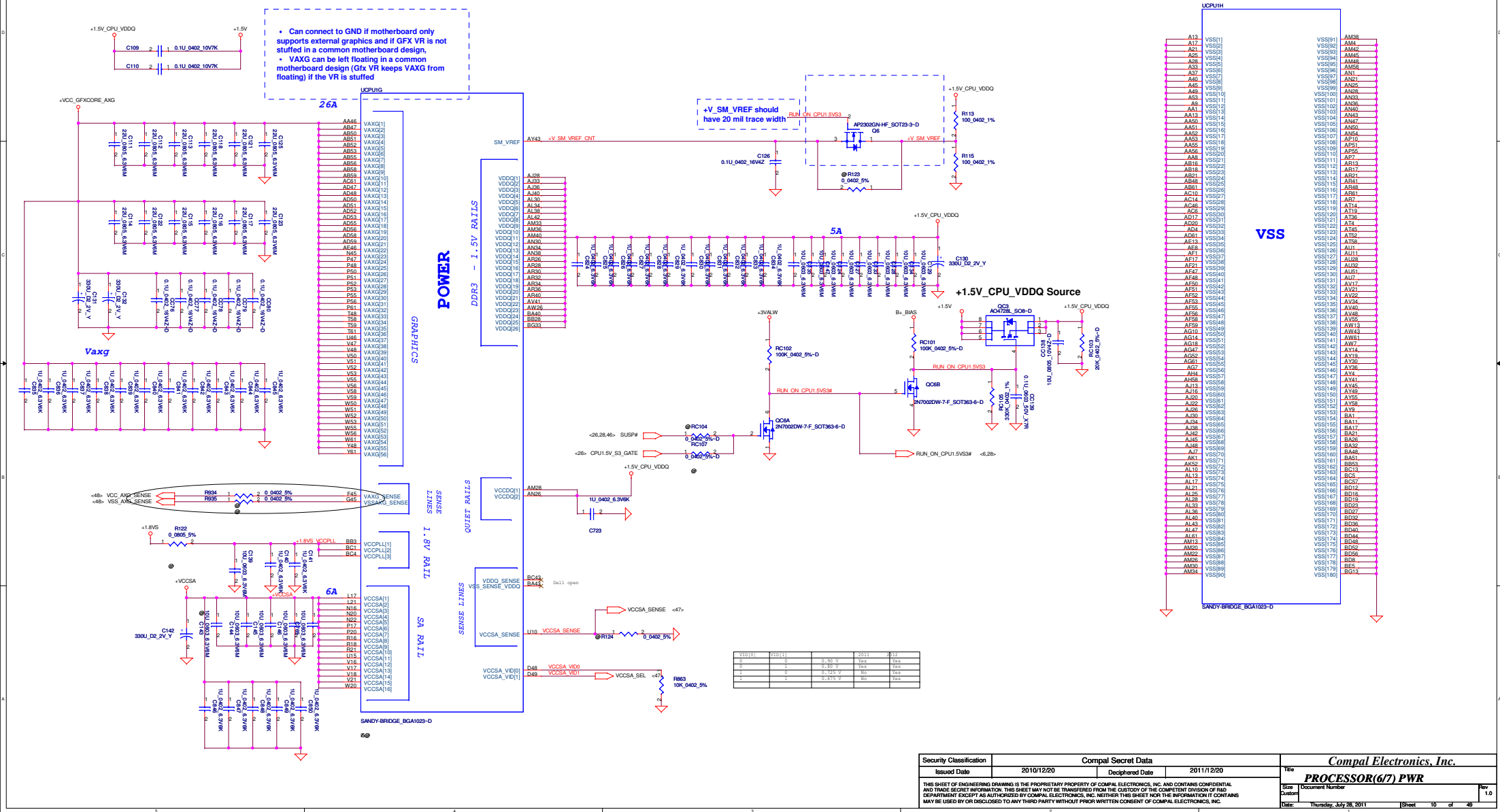


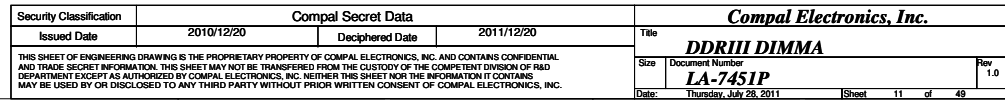
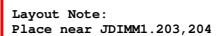
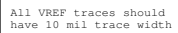
| PCIe Port Bifurcation Straps | |
|------------------------------|--|
| CFG[6:5] | <p>★11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p> |

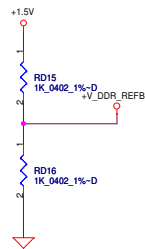


| PEG DEFER TRAINING | |
|--------------------|---|
| CFG7 | <p>★1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p> |

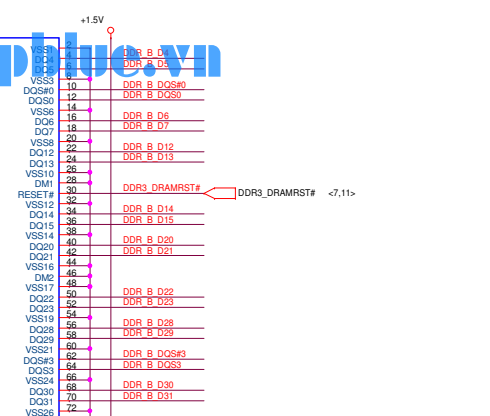
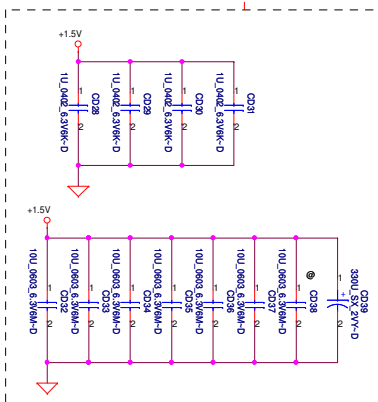






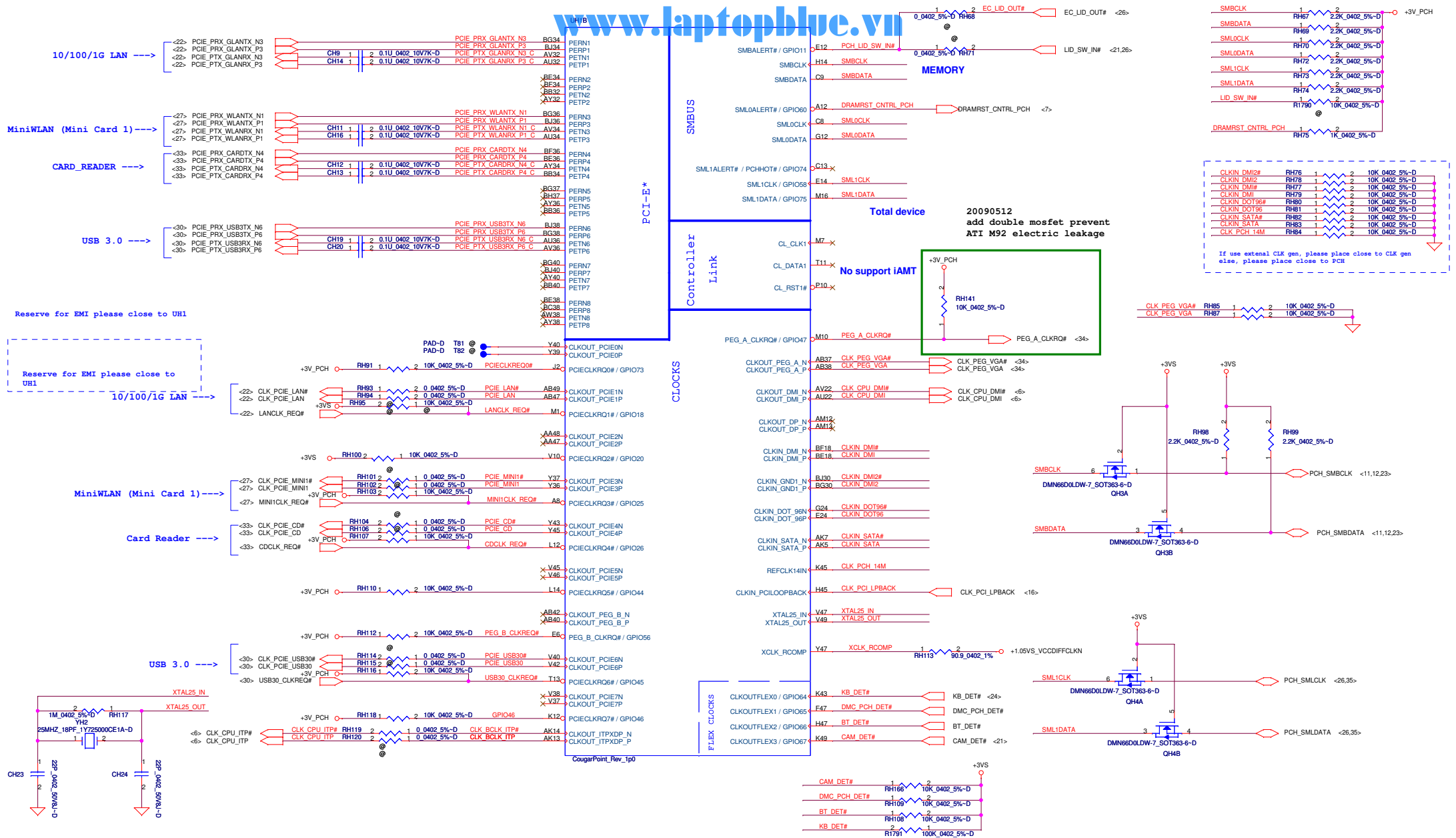


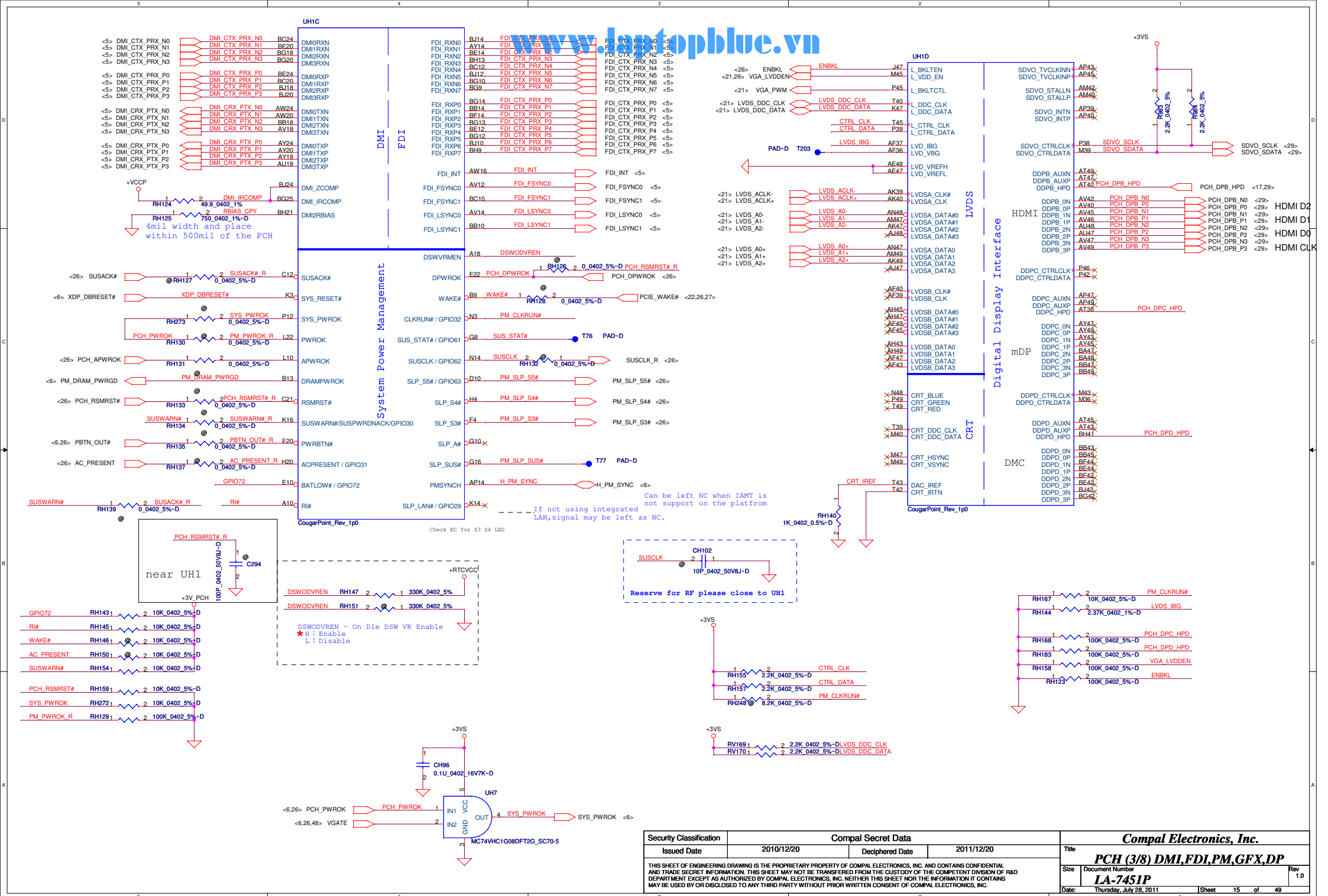
All VREF traces should have 10 mil trace width

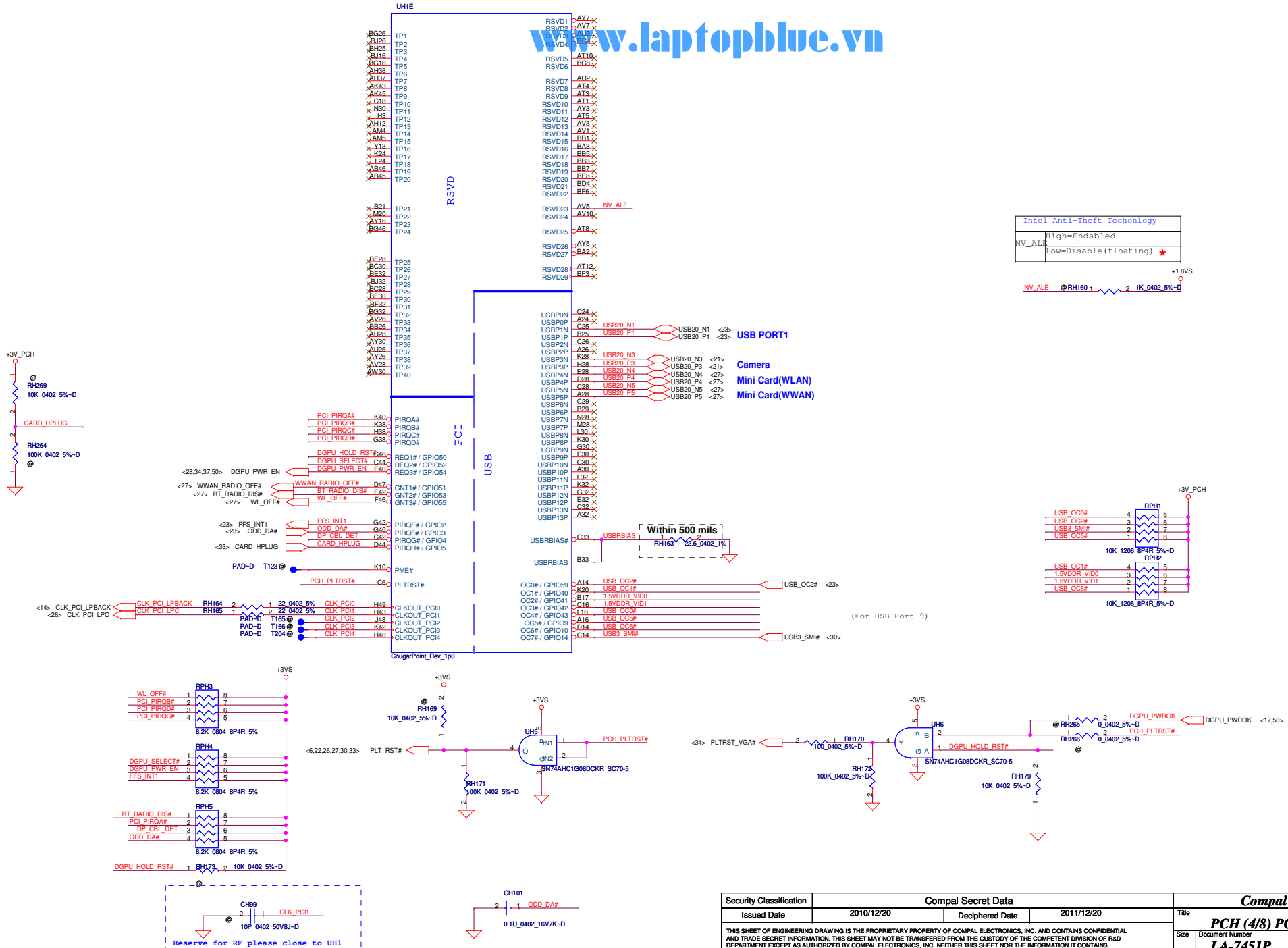
[illegible]

The circuit diagram shows a voltage source of +0.75V connected to a network of four parallel branches. Each branch consists of a capacitor (labeled CD1, CD2, CD3, or CD4) in series with a resistor (labeled U1, U2, U3, or U4). The components are specified as 1U, 0.002, 8.33nF, -D. The bottom terminals of all resistors are connected to a common ground symbol.

| | | | | | |
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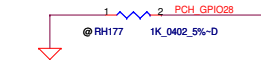




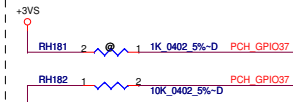


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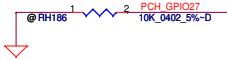
UHF
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H: On-Die voltage regulator enable
L: On-Die PLL Voltage Regulator disable



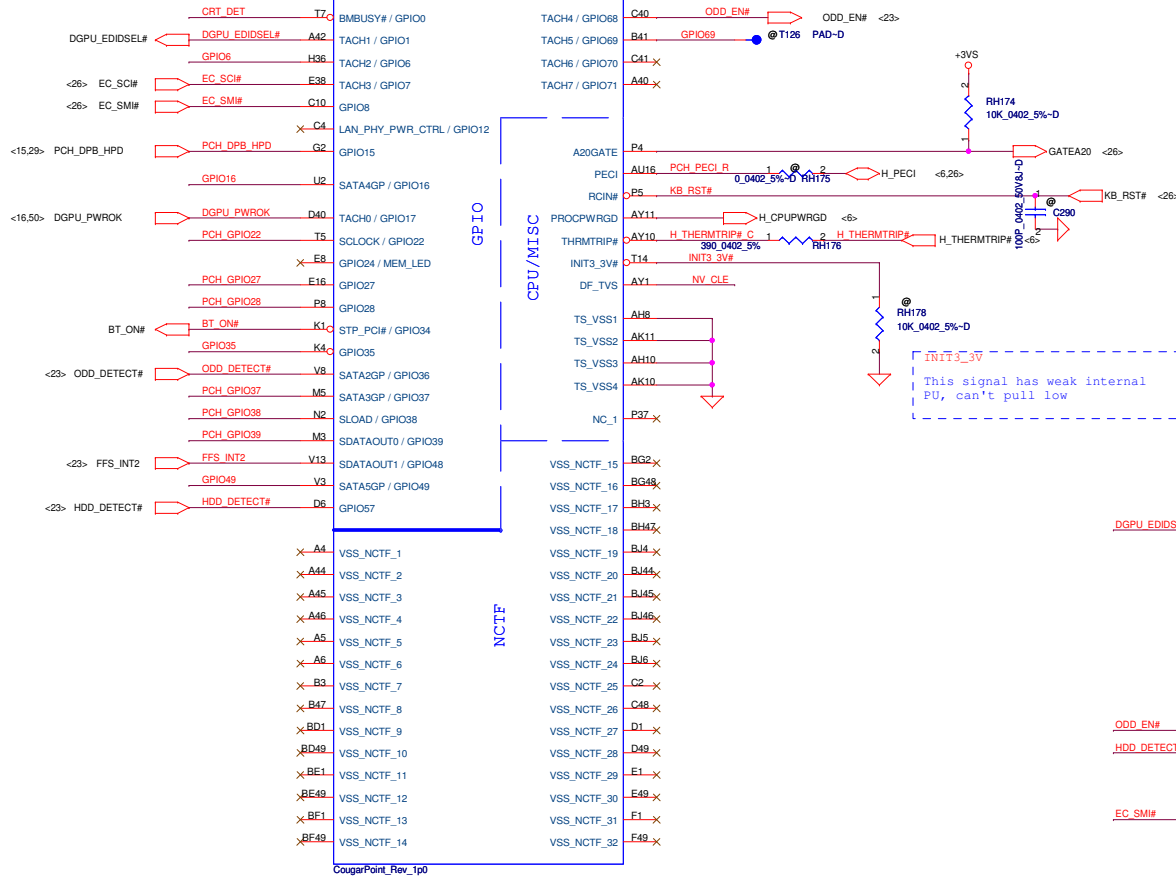
PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE
★ LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)



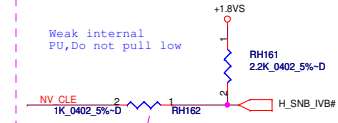
GPIO27
PCH_GPIO27 (Have internal Pull-High)
★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable



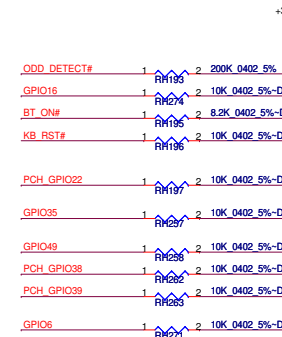
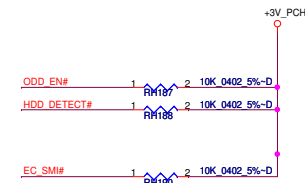
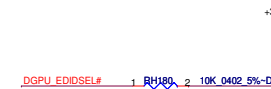
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16
Please refer to Huron River Debug Board DG 0.5



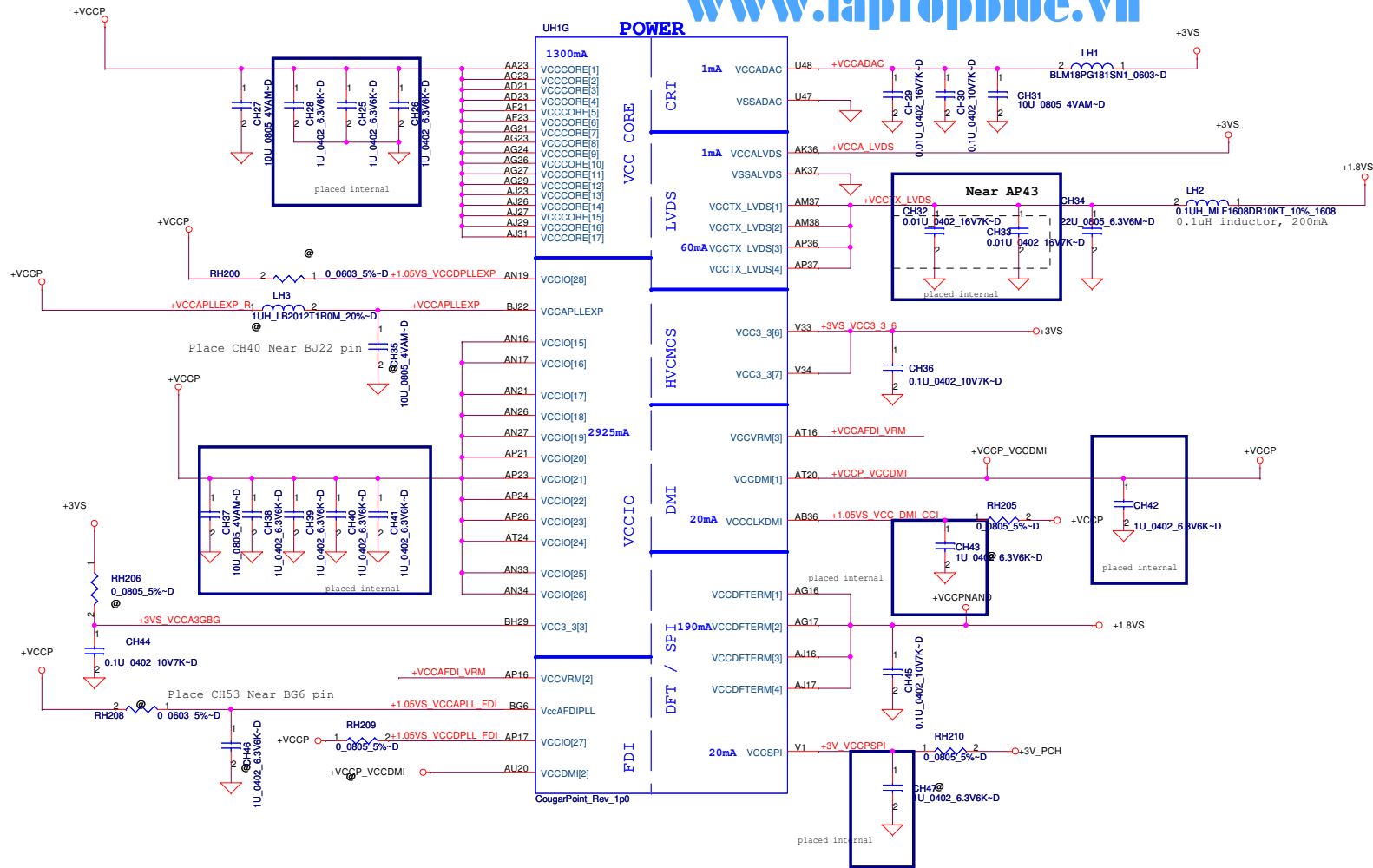
| DMI Termination Voltage | |
|-------------------------|----------------------|
| NV_CLE | Set to Vcc when HIGH |
| | Set to Vss when LOW |



Weak internal PU, Do not pull low
CLOSE TO THE BRANCHING POINT
RH161 and RH162
Follow CRB FAB2 setting

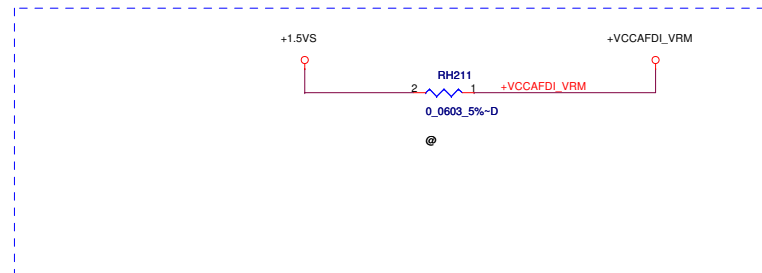


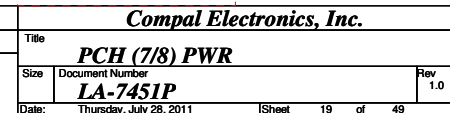
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| Szo | Document Number | LA-7451P | Rev | 1.0 | Date | |
| | | | | | Thursday, July 28, 2011 | Sheet 17 of 49 |

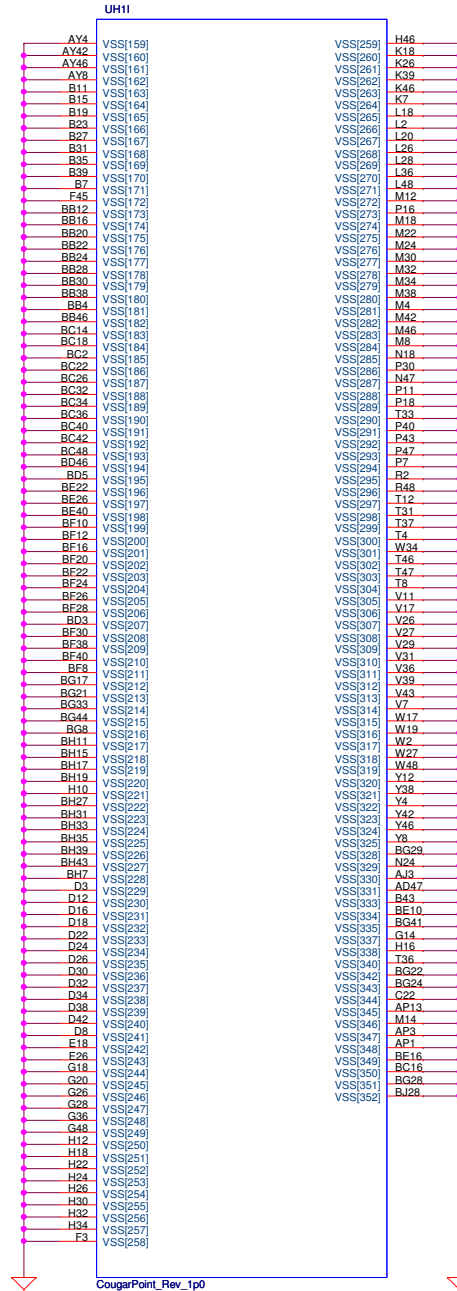
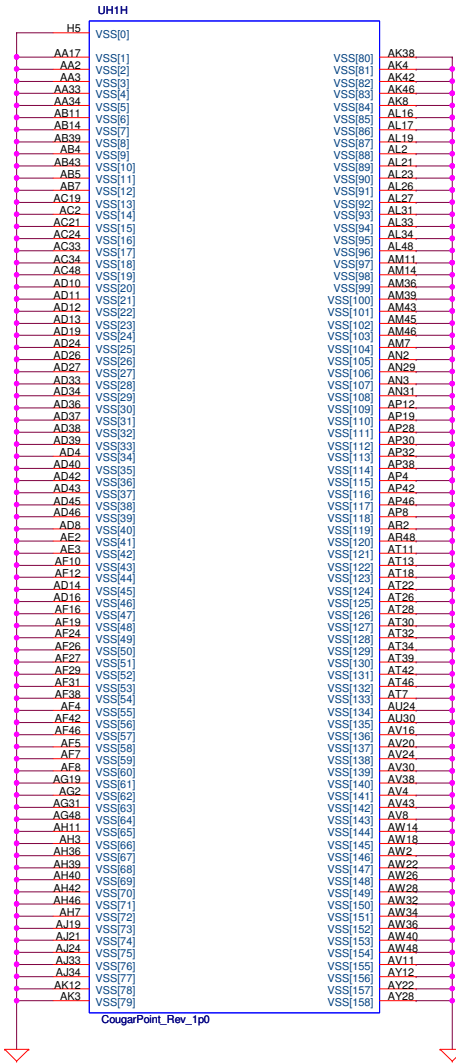


| PCH Power Rail Table | | |
|----------------------|-----------|-----------------------|
| Voltage Rail | Voltage | SO Iccmax Current (A) |
| V_PROC_IO | 1.05 | 0.001 |
| V5REF | 5 | 0.001 |
| V5REF_Sus | 5 | 0.001 |
| Vcc3_3 | 3.3 | 0.266 |
| VccADAC | 3.3 | 0.001 |
| VccADPLLA | 1.05 | 0.08 |
| VccADPLL | 1.05 | 0.08 |
| VccCore | 1.05 | 1.3 |
| VccDMI | 1.05 | 0.042 |
| VccIO | 1.05 | 2.925 |
| VccASW | 1.05 | 1.01 |
| VccSPI | 3.3 | 0.02 |
| VccDSW | 3.3 | 0.003 |
| VccpNAND | 1.8 | 0.19 |
| VccRTC | 3.3 | 6 uA |
| VccSus3_3 | 3.3 | 0.119 |
| VccSusHDA | 3.3 / 1.5 | 0.01 |
| VccVRM | 1.8 / 1.5 | 0.16 |
| VccCLKDMI | 1.05 | 0.02 |
| VccSSC | 1.05 | 0.095 |
| VccDIFFCLKN | 1.05 | 0.055 |
| VccALVDS | 3.3 | 0.001 |
| VccTX_LVDS | 1.8 | 0.06 |

VCCVRM = 160mA detal waiting for newest spec







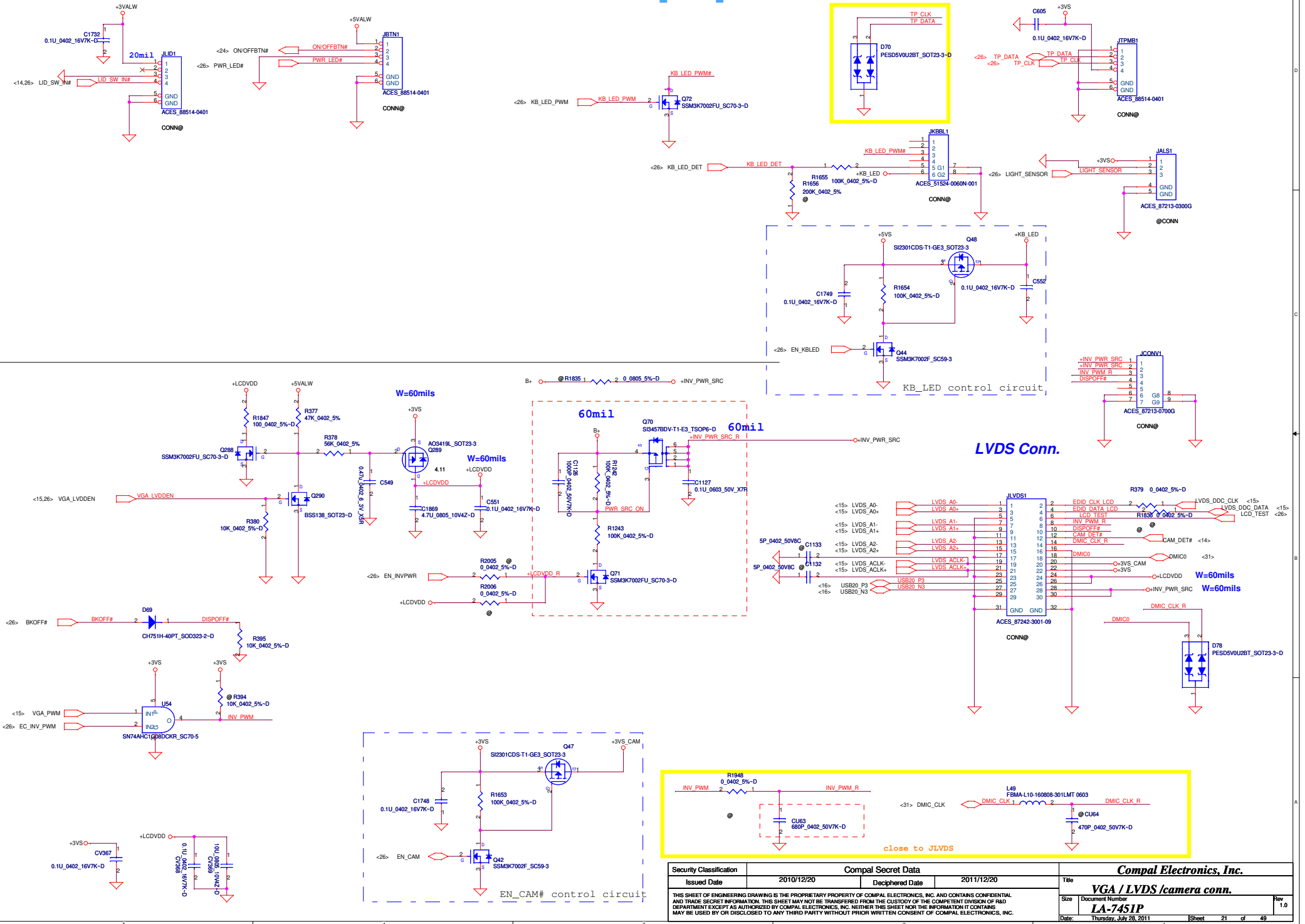
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| Issued Date | 2010/12/20 | Deciphered Date | 2011/12/20 | Title | PCH (8/8) VSS |
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| | | | | Date | Thursday, July 28, 2011 |
| | | | | Sheet | 20 of 49 |

LOGO Board CONN

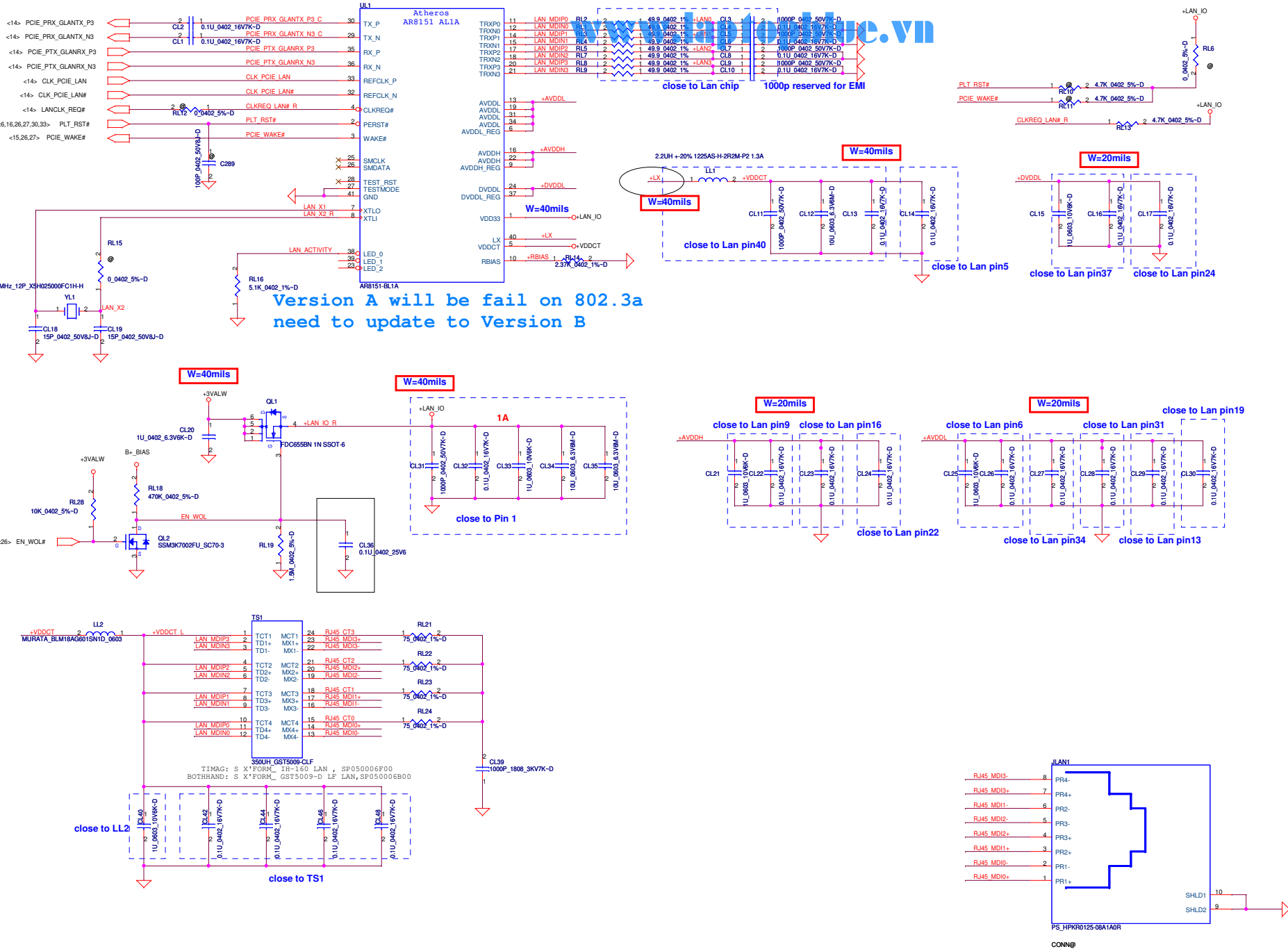
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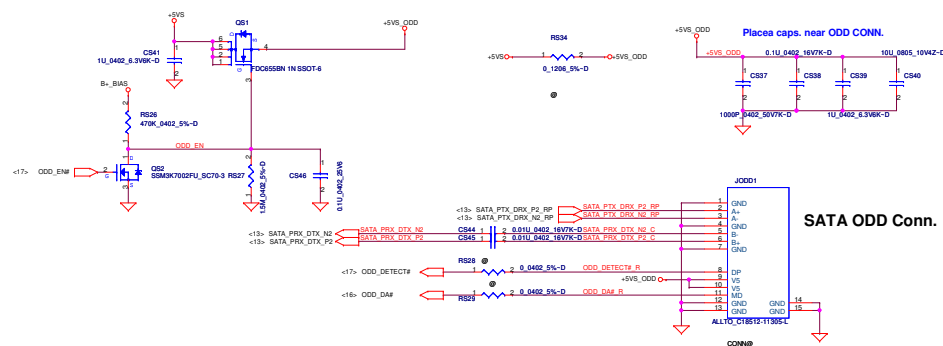
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Touchpad CONN



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| | | | | Size |
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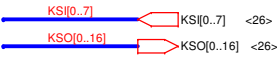
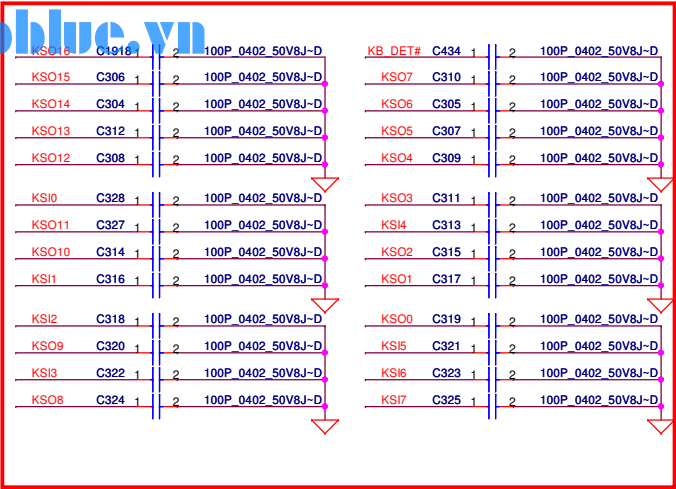
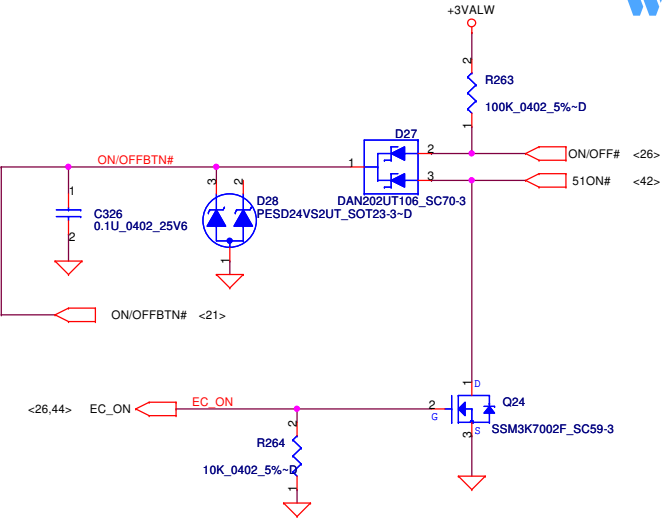
ON/OFF switch Power Button

www.laptopblue.vn

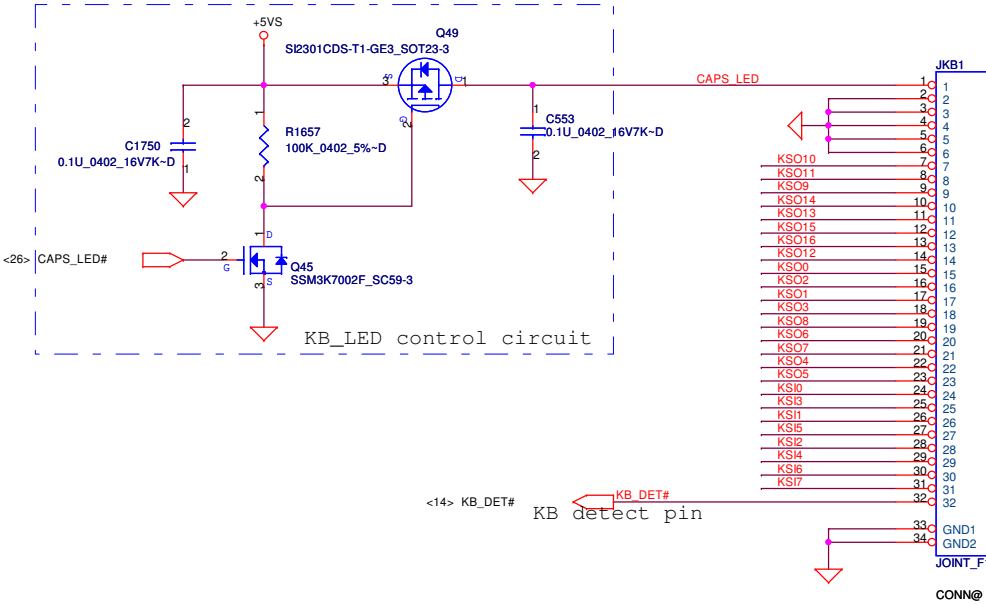
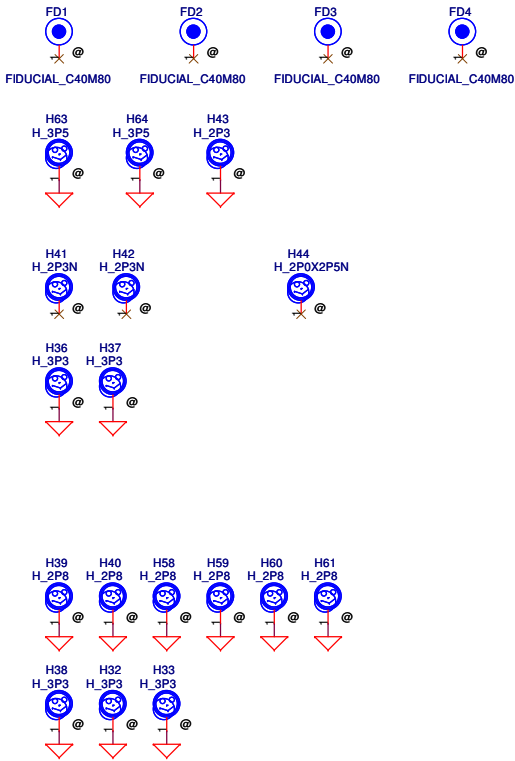
TOP Side

Bottom Side

Test Only

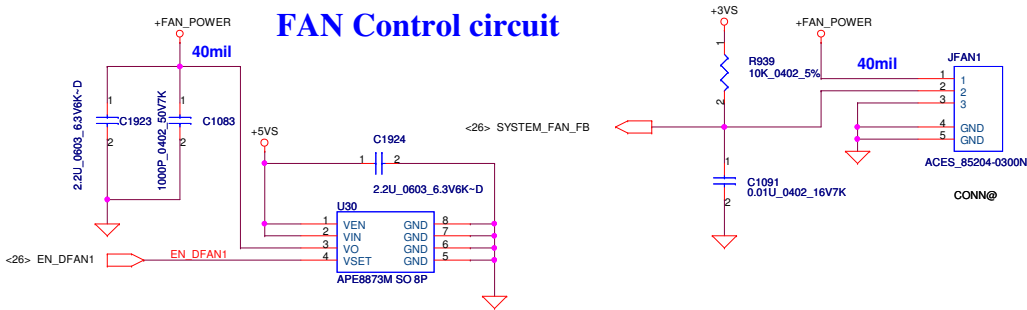


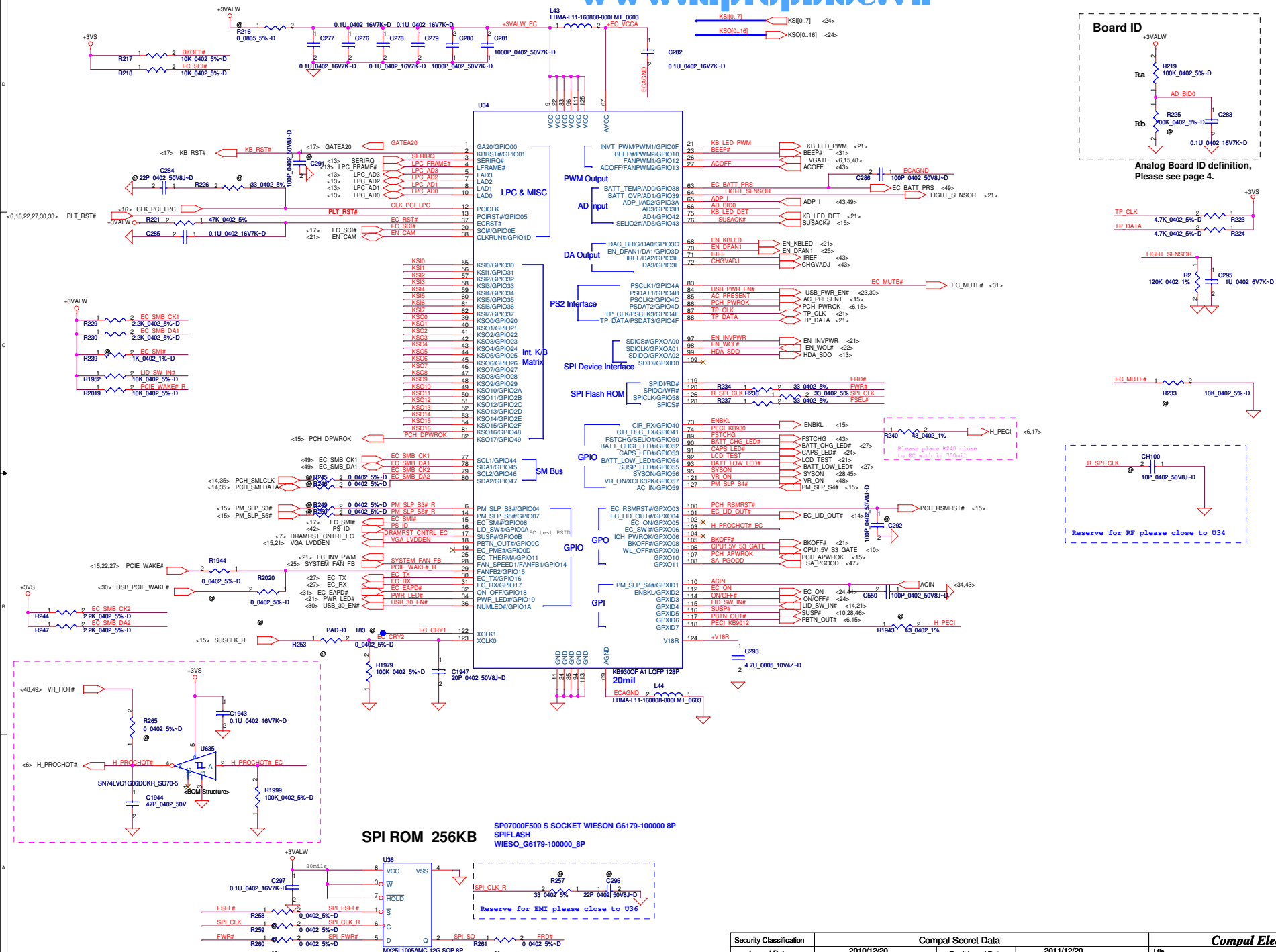
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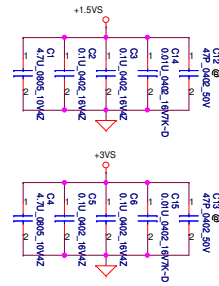
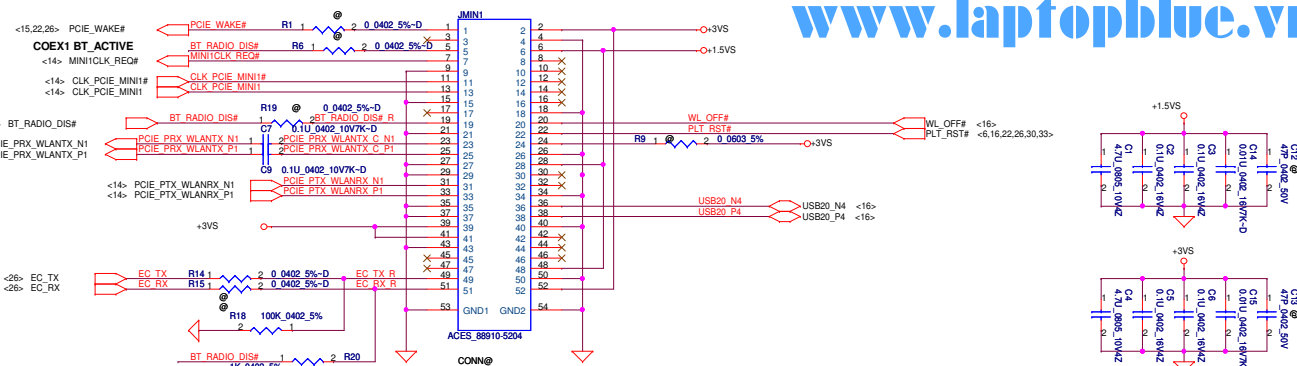


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| | | | | Size | Document Number |
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| | | | | Date | Thursday, July 28, 2011 |
| | | | | Sheet | 24 of 51 |
| | | | | Rev | 1.0 |

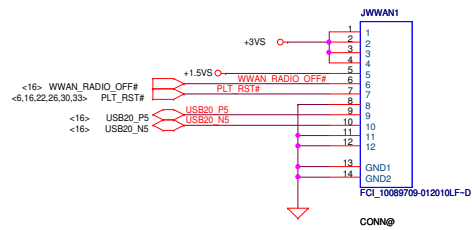
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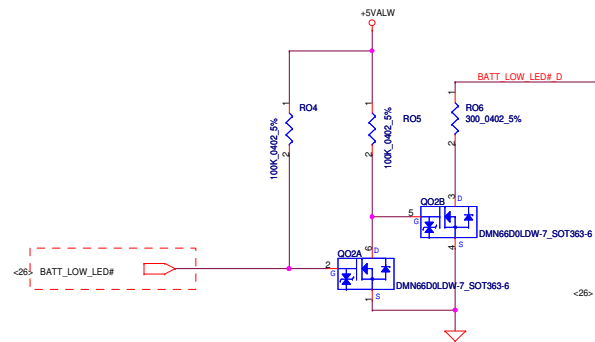




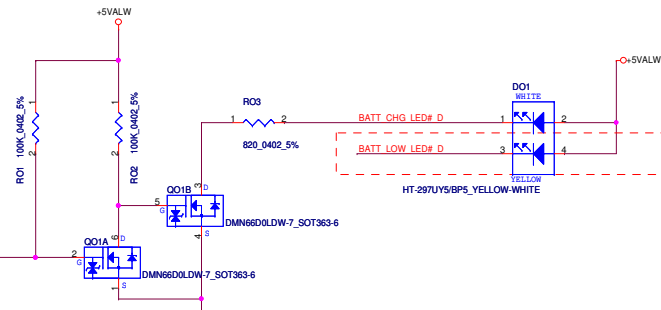
TO WWAN BOARD



BATT LOW

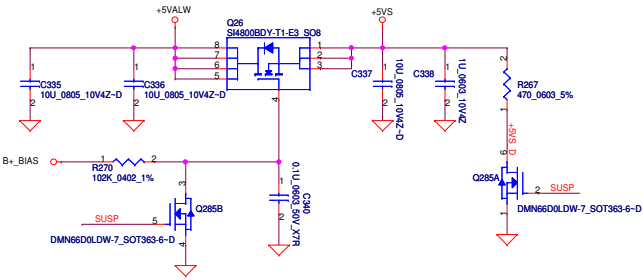


BATT CHARGE

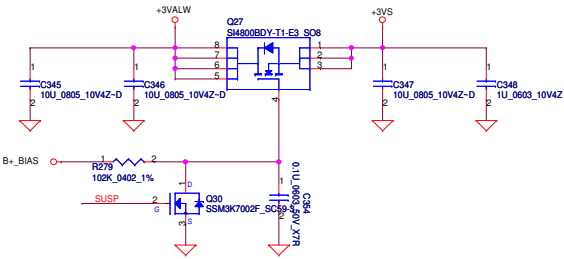


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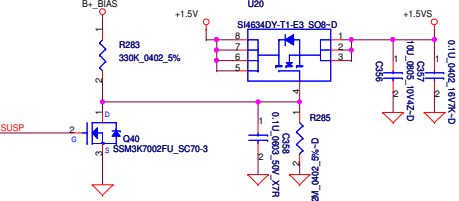
+5VALW to +5VS



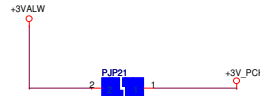
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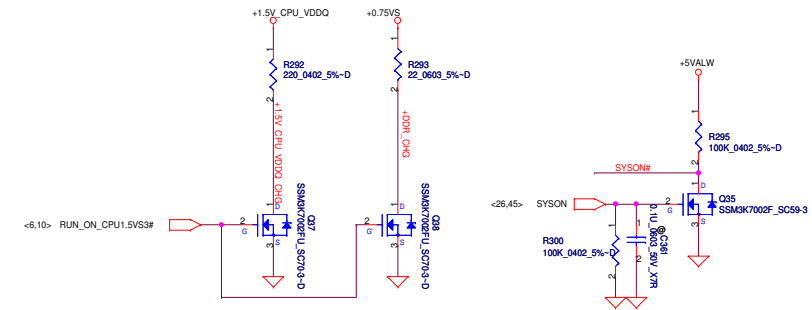
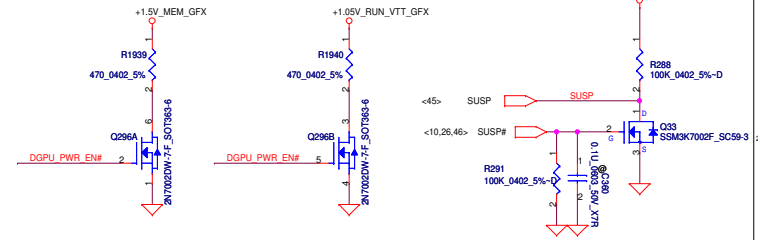
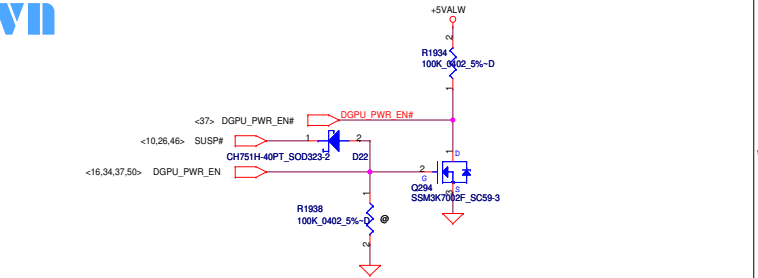
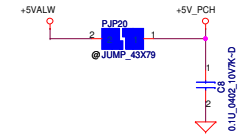
+1.5V To +1.5VS



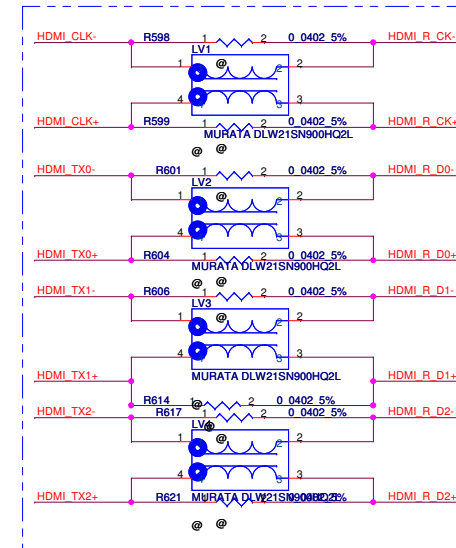
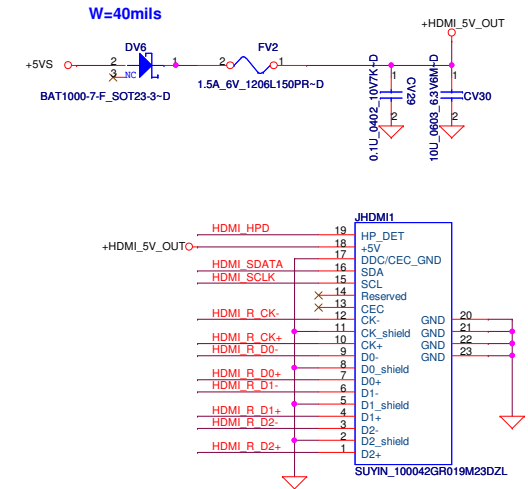
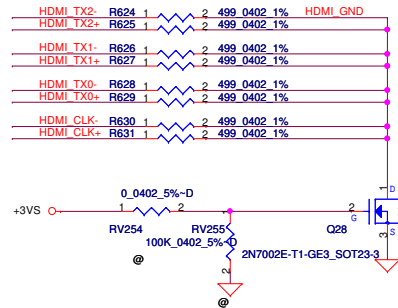
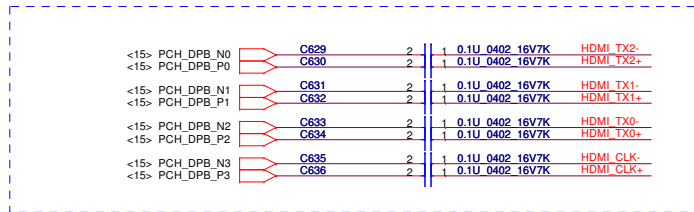
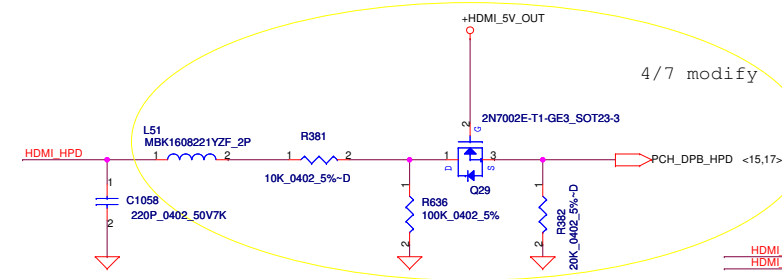
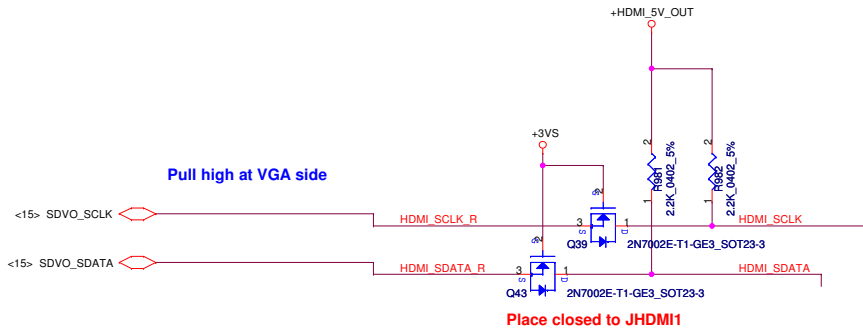
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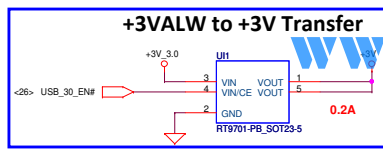
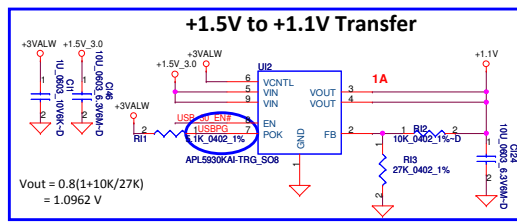
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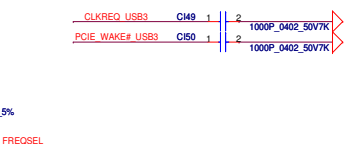
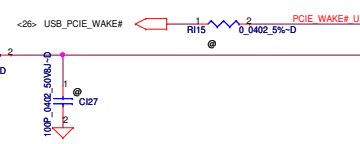
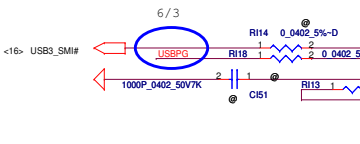
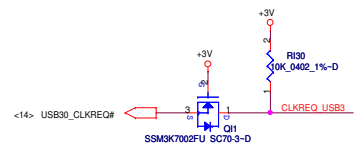
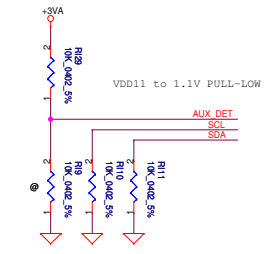
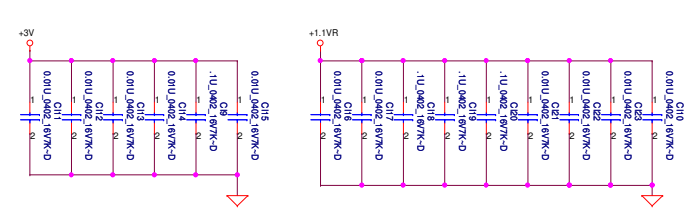
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| | | | | Size | Rev |
| | | | | Customer | 1.0 |
| | | | | Document Number | |
| | | | | LA-7451P | |
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| | | | | Sheet | 29 of 51 |



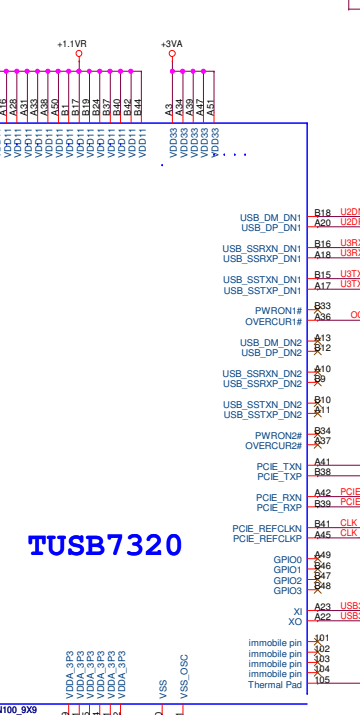
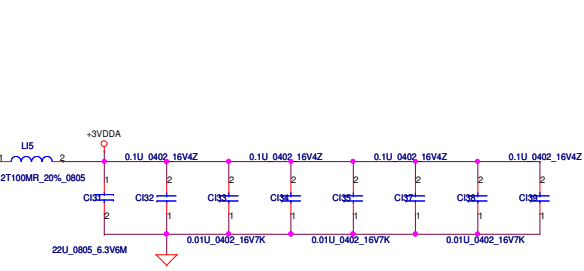
7K for customer request, can use other kind of capacitor, like Y5V.



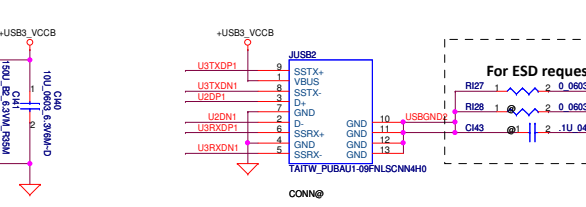
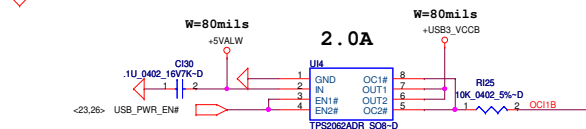
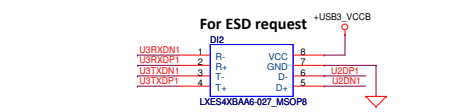
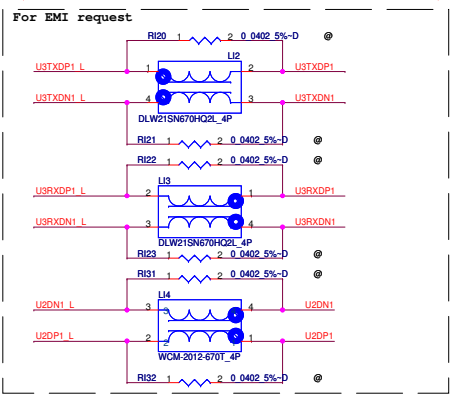
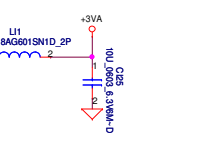
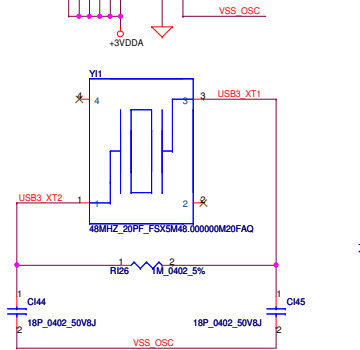
FREQSEL

H = non 48MHz

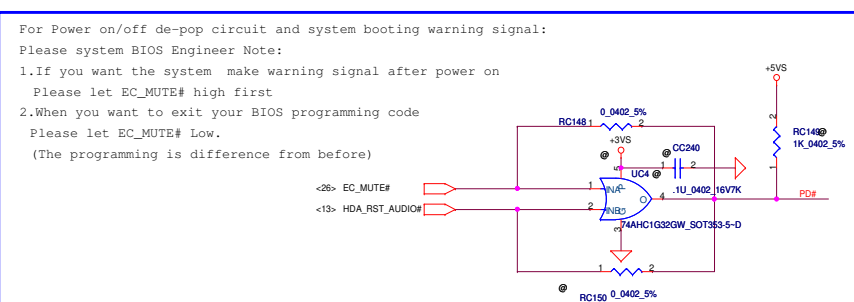
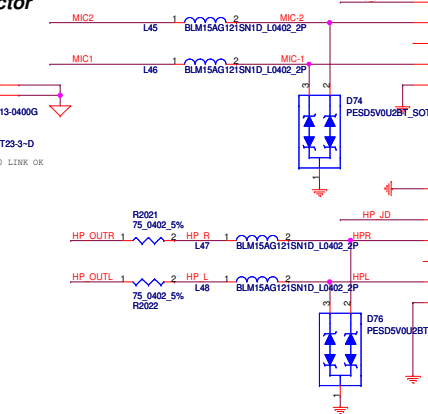
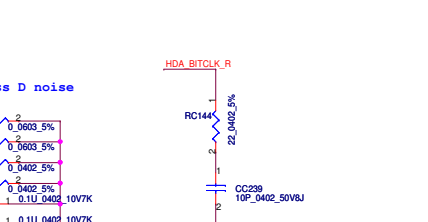
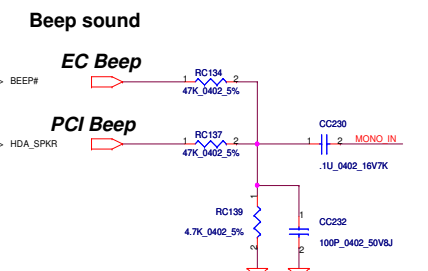
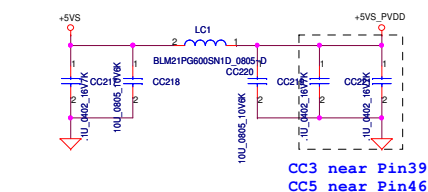
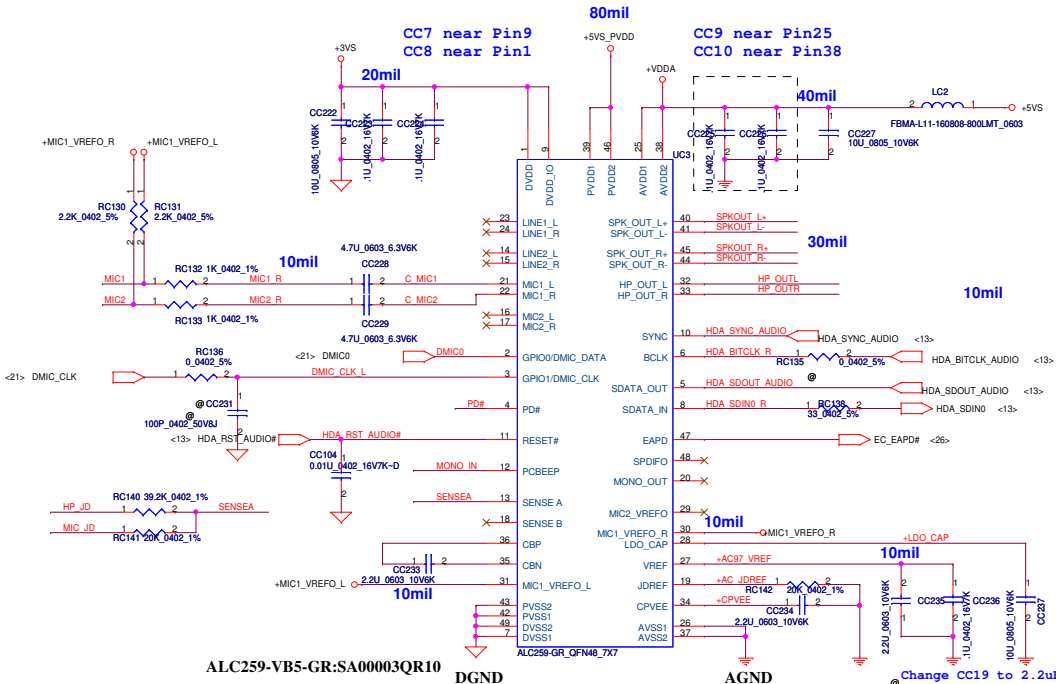
* L = 48MHz (default)



TUSB7320



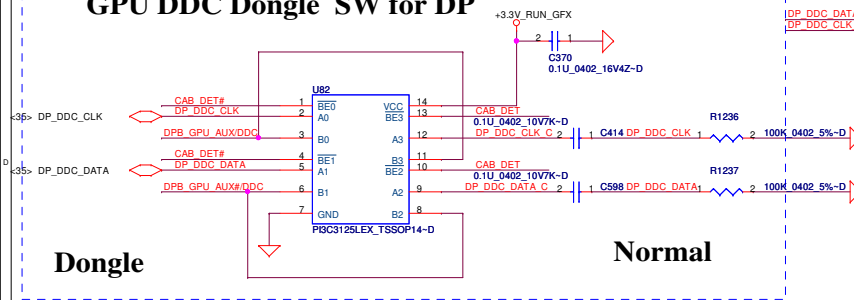
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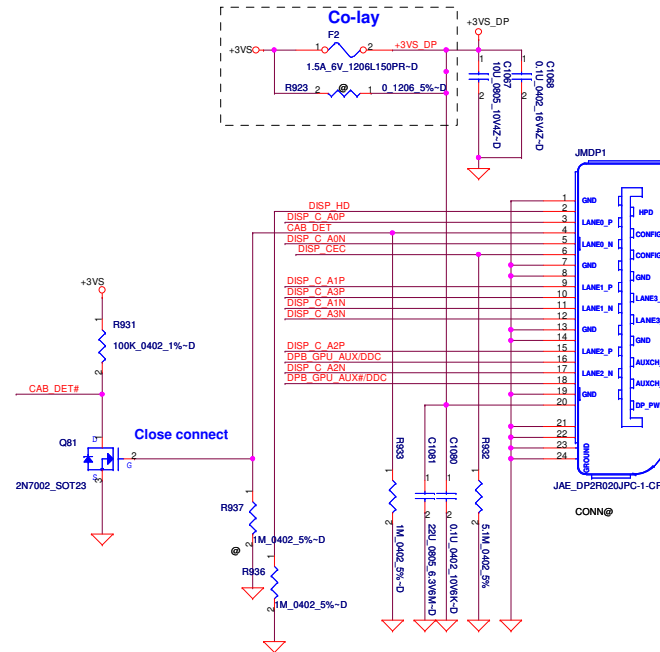
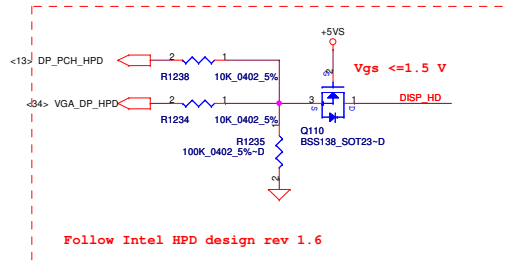
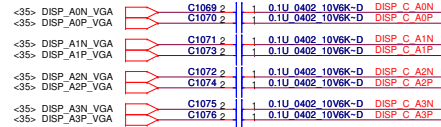
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GPU DDC Dongle SW for DP

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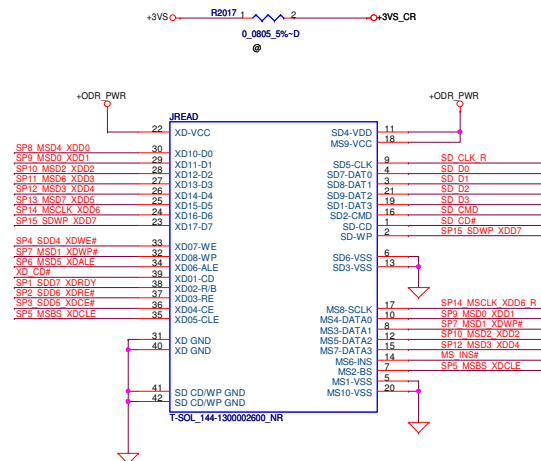
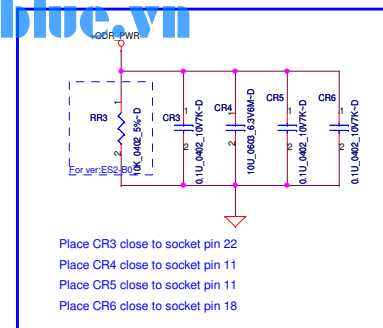
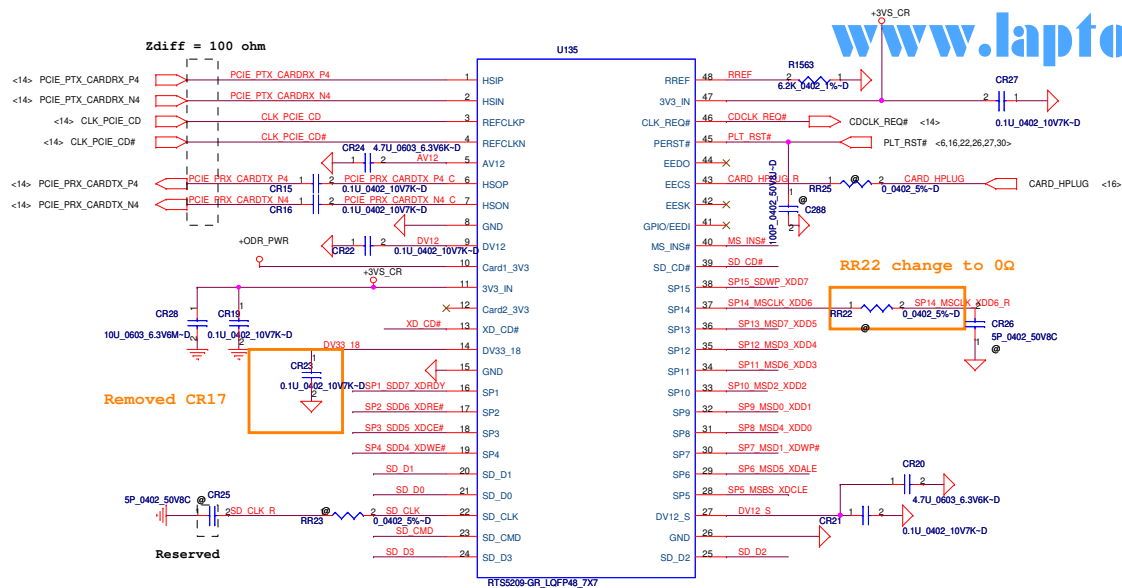


Near to NV

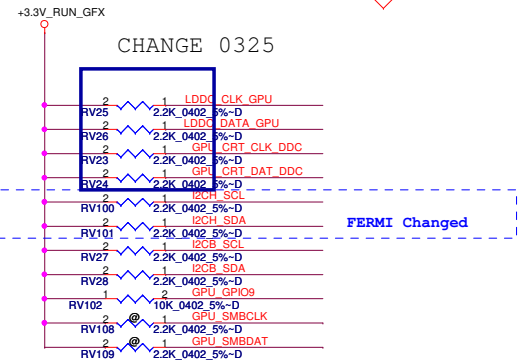
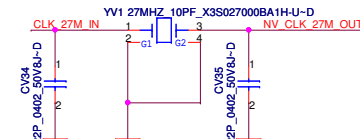
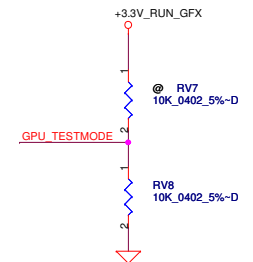
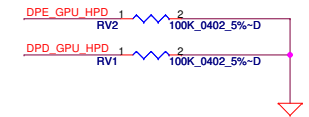
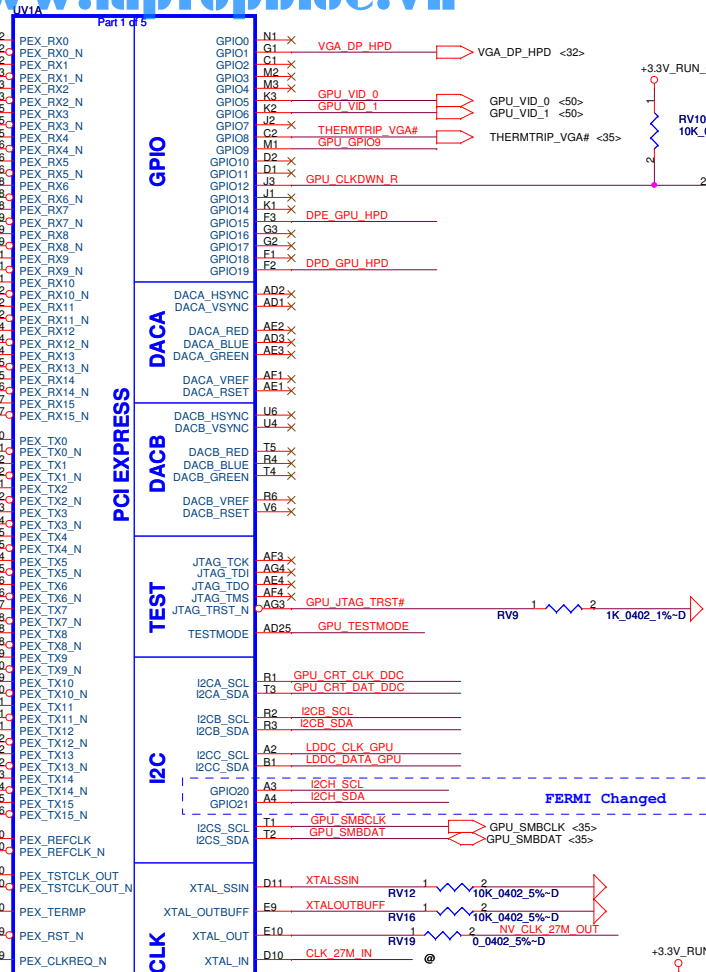
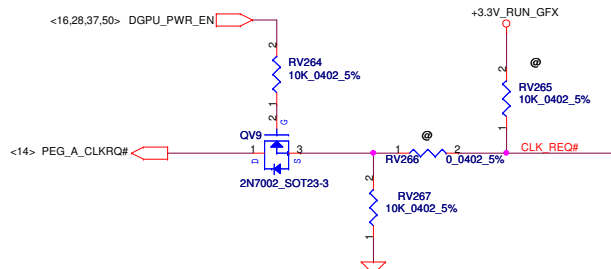
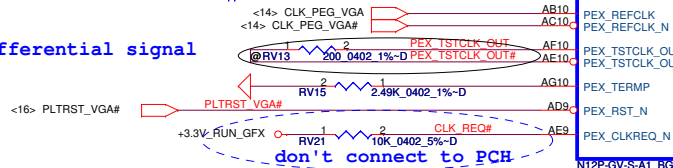
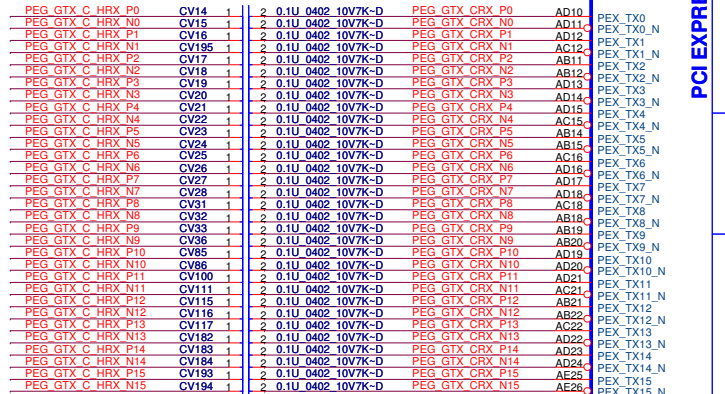


DELL CONFIDENTIAL/PROPRIETARY

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| | | | | Custom | LA-7451P | 1.0 |
| | | | | Date | Thursday, July 28, 2011 | Sheet 32 of 51 |

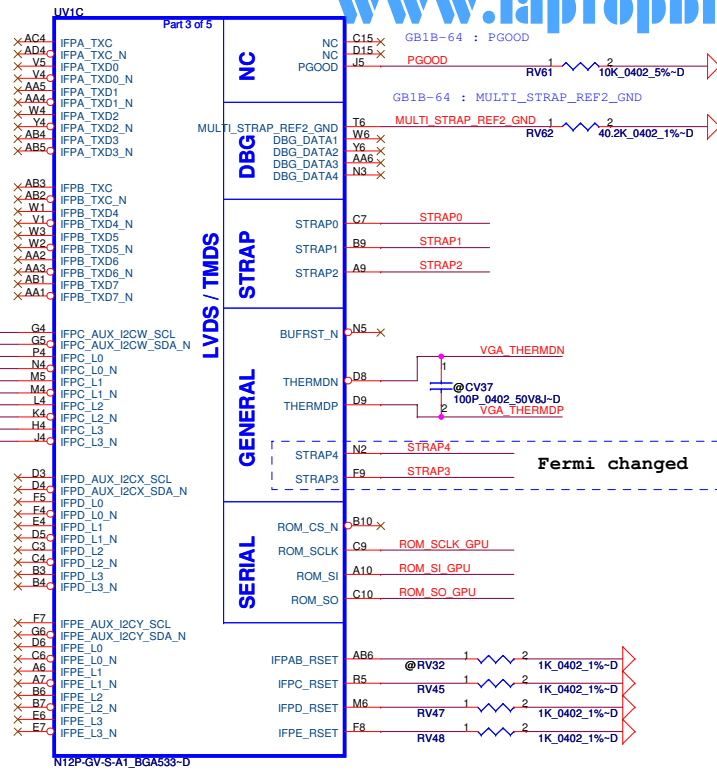


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| | | | | LA-7451P | | | 1.0 | |
| | | | | Date: | Thursday, July 28, 2011 | Sheet | 33 | of |



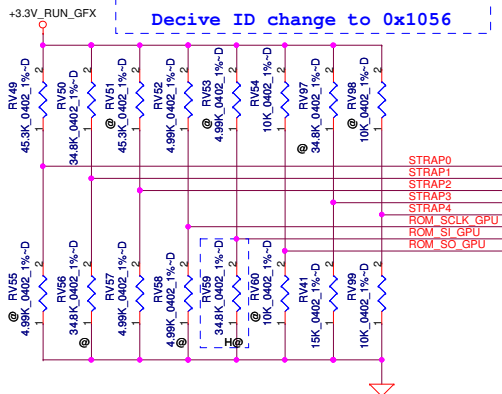
DP

<32> DP DDC_CLK
<32> DP DDC_DATA
<32> DISP_A0P_VGA
<32> DISP_A0N_VGA
<32> DISP_A1P_VGA
<32> DISP_A1N_VGA
<32> DISP_A2P_VGA
<32> DISP_A2N_VGA
<32> DISP_A3P_VGA
<32> DISP_A3N_VGA



N12P-GV-S-A1_BGA533-D

Decive ID change to 0x1056

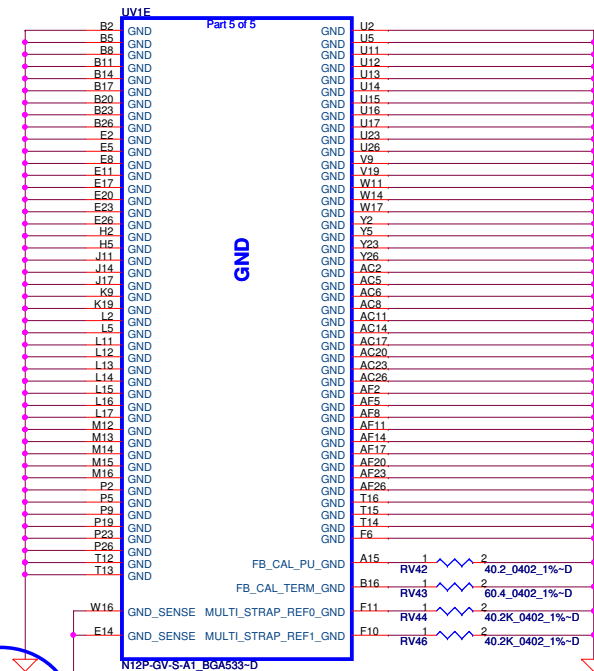


★★ Hynix 64Mx16 DDR3 part stuff RV59=15K
Samsung 64Mx16 DDR3 part stuff RV59=20K
Hynix 128Mx16 DDR3 part stuff RV59=35K
Samsung 128Mx16 DDR3 part stuff RV59=45.3K

| | |
|--------|--------------------------|
| STRAP0 | USER[3:0] |
| STRAP1 | 3GIO_PADCFG_LUT_ADR[3:0] |
| STRAP2 | PCI_DEVID[3:0] |

| Resistor Values | Pull-up to +3V | Pull-down to Gnd |
|-----------------|----------------|------------------|
| 5K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 25K | 1100 | 0100 |
| 30K | 1101 | 0101 |
| 35K | 1110 | 0110 |
| 45K | 1111 | 0111 |

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FB_CAL_PU_GND

FB_CAL_TERM_GND

GND_SENSE MULTI_STRAP_REF0_GND

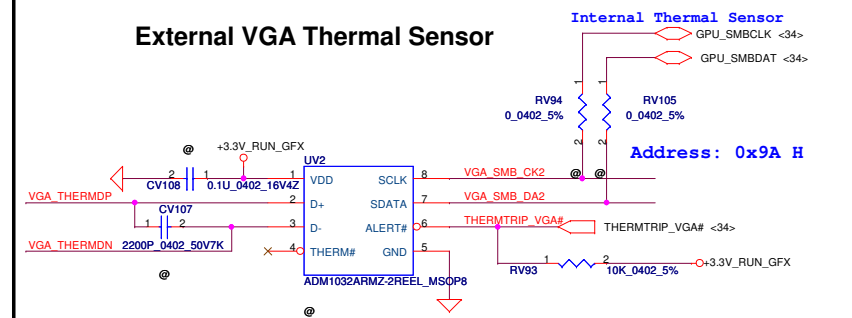
GND_SENSE MULTI_STRAP_REF1_GND

N12P-GV-S-A1_BGA533-D

add 0408

set to multi-level straps

External VGA Thermal Sensor



Internal Thermal Sensor

GPU_SMBCLK <34>

GPU_SMBDATA <34>

RV94 0_0402_5%

RV105 0_0402_5%

Address: 0x9A H

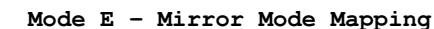
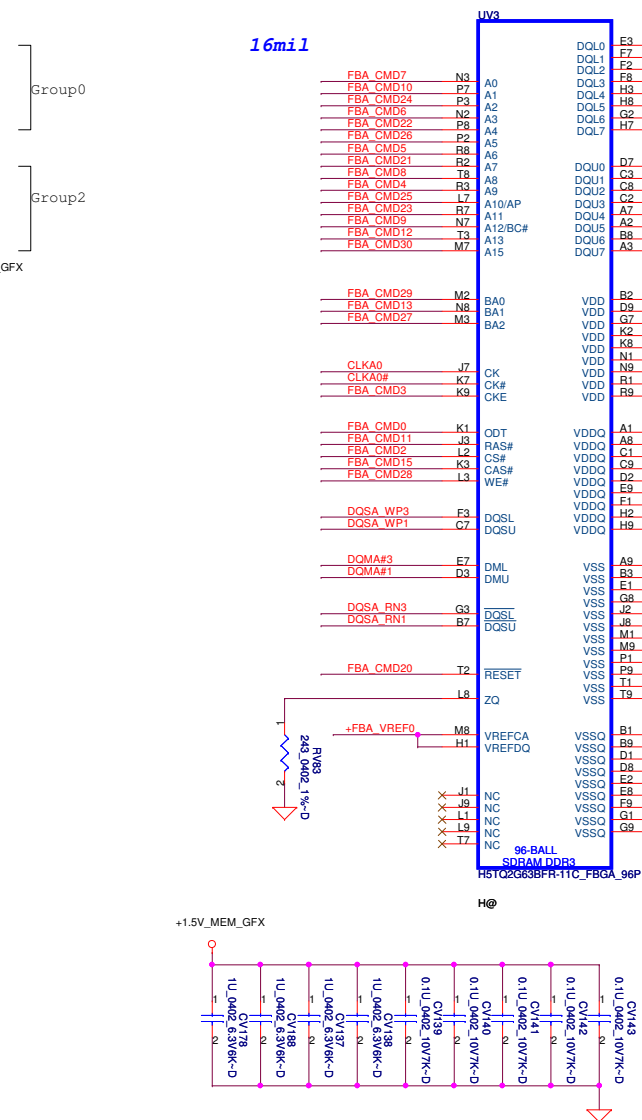
| | |
|----------|--|
| ROM_SCLK | PCIDEVID_EXT, SUB_VENDOR, SLOT_CLK, PEX_PLL_EN |
| ROM_SI | RAM_CFG[3:0] |
| ROM_SO | XCLK_417, FB_0_BAR_SIZE, ALT_ADOOR, VGA_DEVICE |



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| | | | |
|-------|---------------------|------|-------------------------|
| Title | N12P DP, STRAP, GND | Rev | 1.0 |
| Size | Document Number | Date | Thursday, July 28, 2011 |
| Sheet | 35 | of | 51 |

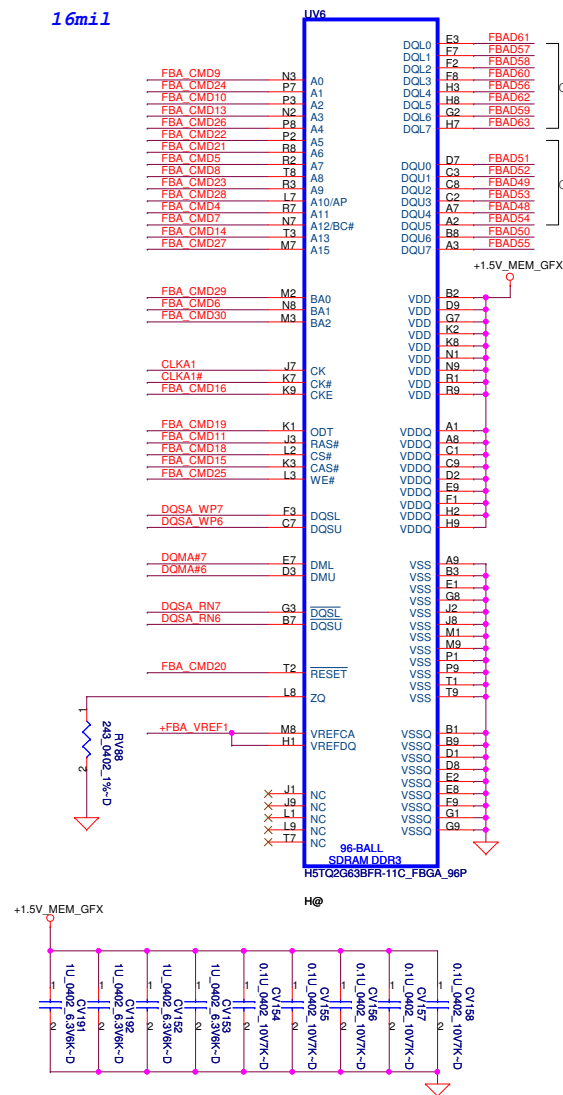
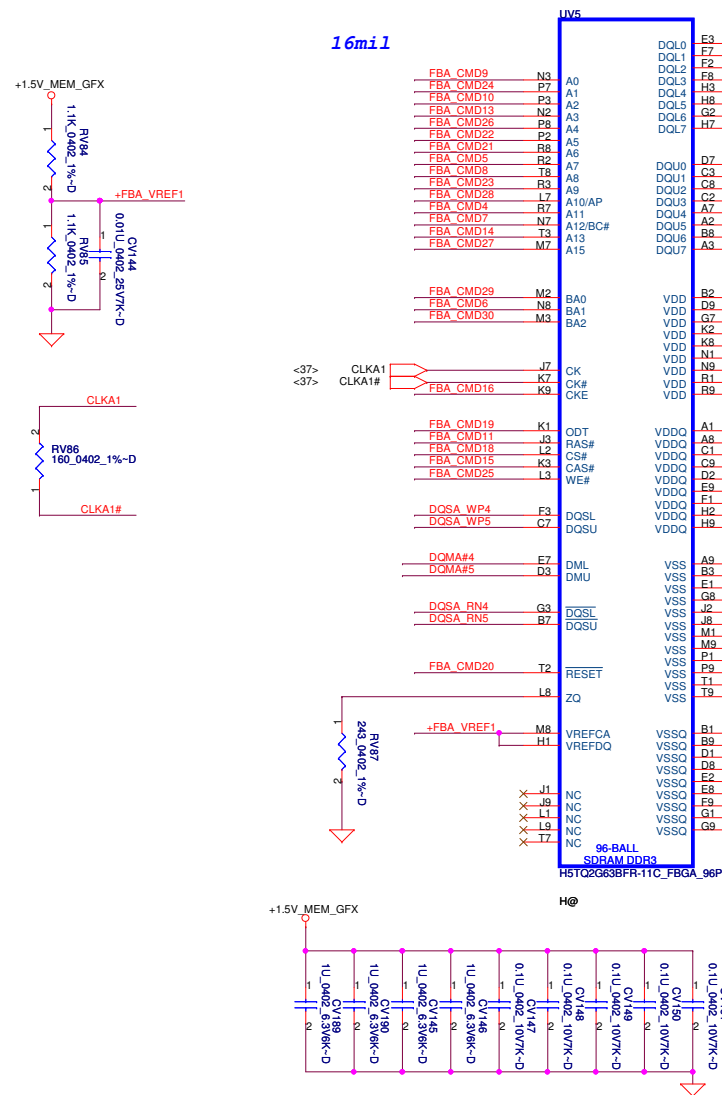
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| | DATA Bus | |
|---------|----------|--------|
| Address | 0..31 | 32..63 |
| CMD0 | ODT_L | |
| CMD1 | CS1#_L | |
| CMD2 | CS0#_L | |
| CMD3 | CKE_L | |
| CMD4 | A9 | A11 |
| CMD5 | A6 | A7 |
| CMD6 | A3 | BA1 |
| CMD7 | A0 | A12 |
| CMD8 | A8 | A8 |
| CMD9 | A12 | A0 |
| CMD10 | A1 | A2 |
| CMD11 | RAS# | RAS# |
| CMD12 | A13 | A14 |
| CMD13 | BA1 | A3 |
| CMD14 | A14 | A13 |
| CMD15 | CAS# | CAS# |
| CMD16 | | CKE_H |
| CMD17 | | CS1#_H |
| CMD18 | | CS0#_H |
| CMD19 | | ODT_H |
| CMD20 | RST | RST |
| CMD21 | A7 | A6 |
| CMD22 | A4 | A5 |
| CMD23 | A11 | A9 |
| CMD24 | A2 | A1 |
| CMD25 | A10 | WE# |
| CMD26 | A5 | A4 |
| CMD27 | BA2 | A15 |
| CMD28 | WE# | A10 |
| CMD29 | BA0 | BA0 |
| CMD30 | A15 | BA2 |



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Mode E - Mirror Mode Mapping

| | DATA Bus | |
|---------|----------|---------|
| Address | 0...31 | 32...63 |
| CMD0 | ODT_L | |
| CMD1 | CS1#_L | |
| CMD2 | CS0#_L | |
| CMD3 | CKE_L | |
| CMD4 | A9 | A11 |
| CMD5 | A6 | A7 |
| CMD6 | A3 | BA1 |
| CMD7 | A0 | A12 |
| CMD8 | A8 | A8 |
| CMD9 | A12 | A0 |
| CMD10 | A1 | A2 |
| CMD11 | RAS# | RAS# |
| CMD12 | A13 | A14 |
| CMD13 | BA1 | A3 |
| CMD14 | A14 | A13 |
| CMD15 | CAS# | CAS# |
| CMD16 | | CKE_H |
| CMD17 | | CS1#_H |
| CMD18 | | CS0#_H |
| CMD19 | | ODT_H |
| CMD20 | RST | RST |
| CMD21 | A7 | A6 |
| CMD22 | A4 | A5 |
| CMD23 | A11 | A9 |
| CMD24 | A2 | A1 |
| CMD25 | A10 | WE# |
| CMD26 | A5 | A4 |
| CMD27 | BA2 | A15 |
| CMD28 | WE# | A10 |
| CMD29 | BA0 | BA0 |
| CMD30 | A15 | BA2 |

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VRAM A Upper

LA-7451P

| Size |
|------|
|------|

LA-7
Date: Thursday, July 28, 2011

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| | |
|-----|--|
| Rev | |
| 1.0 | |

Version change list (P.I.R. List)

EE section

Page 1 of 2

| Item | Reason for change | PG# | Modify List | Date | Phase |
|------|----------------------------|-----|--|------------|-------|
| 1 | SMBus signal Pull HIGH | 15 | Add R983,R984 | 2011/04/07 | PT |
| 2 | SMBus signal Pull HIGH | 25 | Add RV22~,RV29,QV7 | 2011/04/07 | PT |
| 3 | vss pull low | 35 | Add RV106 | 2011/04/07 | PT |
| 4 | hdmi HPD | 29 | Add R636 | 2011/04/07 | PT |
| 5 | GPU_CLKDOWN_R PULL HIGH | 34 | Add RV10 | 2011/04/07 | PT |
| 6 | PEG_A_CLKREQ# CONTROL | 34 | Add RV264, RV265, RV266, RV267, QV9 | 2011/04/07 | PT |
| 7 | sounds too small | 31 | Change RC134, RC137 from 47K to 560ohm | 2010/10/15 | PT |
| 8 | protect HDMI plug in noise | 29 | add CV101 | 2010/10/15 | PT |
| 9 | Modify USB3.0 Solution | 30 | | 2010/10/15 | PT |
| 10 | change Lan symbol | 22 | JLAN1 | 2010/10/15 | PT |
| 11 | Power LED no light when S3 | 21 | Change JBTN1 Pin1 from +5VS to +5VALW net | 2010/10/15 | PT |
| 12 | ESD request | | Add CC70 | 2010/10/15 | PT |
| 13 | ESD request | | Add CHI01 | 2010/10/17 | PT |
| 14 | ESD request | | Add CC71-CC75 | 2010/10/17 | PT |
| 15 | ESD request | | Add CC76-CC80 | 2010/10/17 | PT |
| 16 | ESD request | | Del CF61,3,8,9,10,11,16,17 | 2010/10/20 | PT |
| 17 | USB 3.0 Wake Issue | 30 | Del RI19,Add CI51 | 2010/10/20 | PT |
| 18 | USB 3.0 Wake Issue | 30 | Change RI18 Pin1 to UI2 pin7 | 2010/10/22 | PT |
| 19 | T | | Change BOM UV2,CV107,CV108,RV108,RV109 to remove | 2010/10/22 | ST |
| 20 | LCD timing | | Change BOM C549 to SEI24474K80 | 2010/10/22 | ST |
| 21 | | | Change BOM U48 to SA00003R80 | 2010/10/22 | ST |
| 22 | | | Change BOM UV1 to SA00004Q40L | 2010/10/22 | ST |
| 23 | | | | 2010/10/24 | |
| 24 | | | | 2010/10/24 | PT |
| 25 | | | | 2010/10/26 | PT |
| 26 | | | | 2010/12/1 | ST |
| 27 | | | | 2010/12/1 | ST |
| 28 | | | | 2010/12/1 | ST |
| 29 | | | | 2010/12/1 | ST |
| 30 | | | | 2010/12/1 | ST |
| 31 | | | | 2010/12/6 | ST |
| 32 | | | | 2010/12/6 | ST |
| 33 | | | | 2010/12/6 | ST |
| 34 | | | | 2010/12/6 | ST |
| 35 | | | | 2010/12/8 | ST |
| 36 | | | | 2010/12/8 | ST |
| 37 | | | | 2010/12/8 | ST |
| 38 | | | | 2010/12/8 | ST |
| 39 | | | | 2010/12/9 | ST |
| 40 | | | | | |
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| | | | | | LA-6961P | 1.0 |
| | | | | Date: | Thursday, July 28, 2011 | Sheet 40 of 51 |

RV59
45.3K_0402_1%~D
1 2
S @

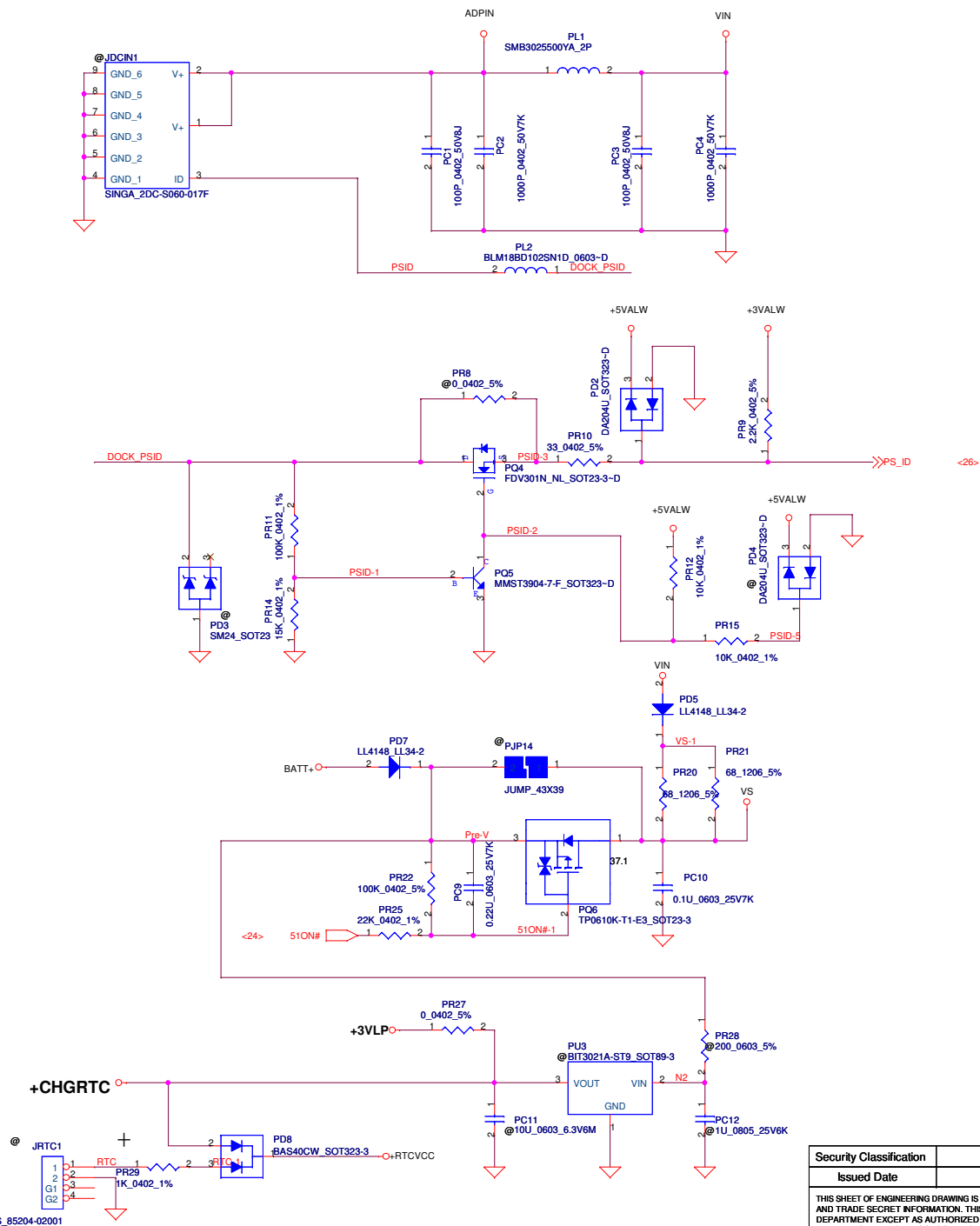
UV3
243_0402_1%~D
1 2
S @

UV4
243_0402_1%~D
1 2
S @

UV5
243_0402_1%~D
1 2
S @

UV6
243_0402_1%~D
1 2
S @

| | | | |
|---------|-------------------------|-------|----------|
| | | | |
| Title | | | |
| <Title> | | | |
| Size | Document Number | | Rev |
| A | LA-7451P | | 0.2 |
| Date: | Thursday, July 28, 2011 | Sheet | 41 of 51 |



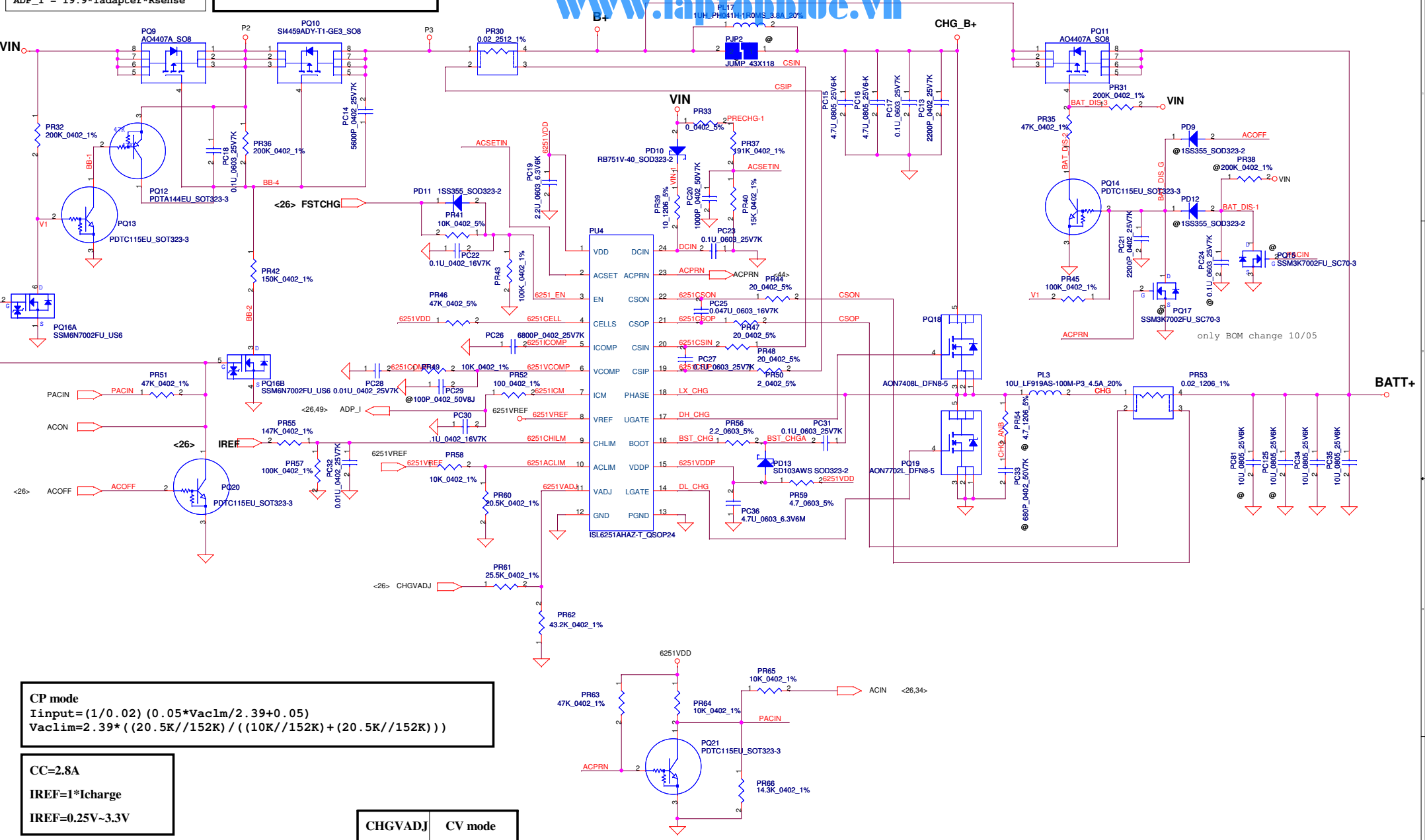
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| Size | Custom | Document Number | | Rev | 1.0 |
| Date: | Thursday, July 28, 2011 | Sheet | 42 of 51 | | |

Iada=0~4.615A (90W/19.5V=4.615A)

ADP_I = 19.9*Iadapter*Rsense

CP = 90%*Iada ; CP = 4.15A

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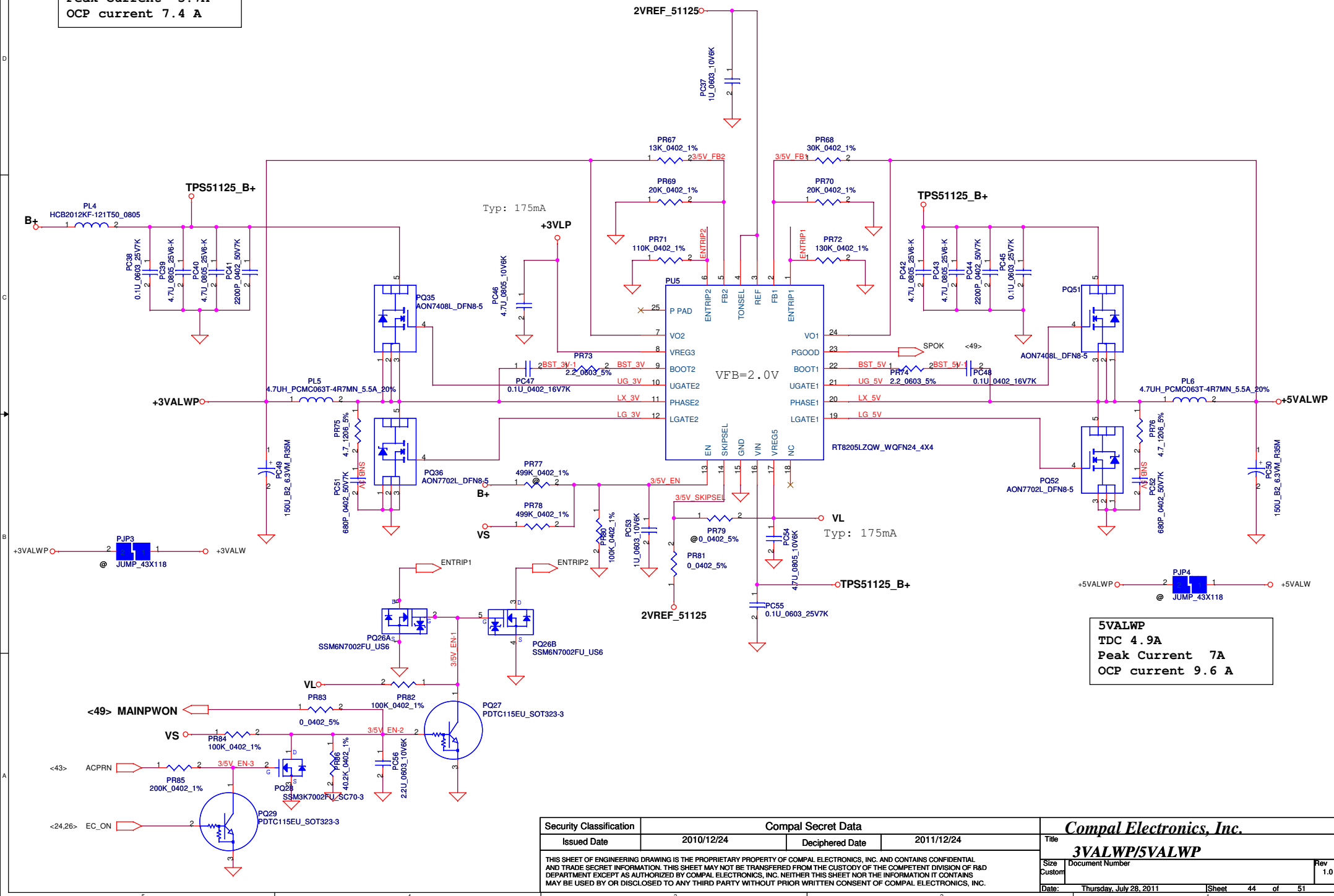
CP mode
 $I_{input} = (1/0.02) (0.05 \cdot V_{ac1m} / 2.39 + 0.05)$
 $V_{ac1m} = 2.39 \cdot ((20.5K / 152K) / ((10K / 152K) + (20.5K / 152K)))$

CC=2.8A
IREF=1*Icharge
IREF=0.25V~3.3V

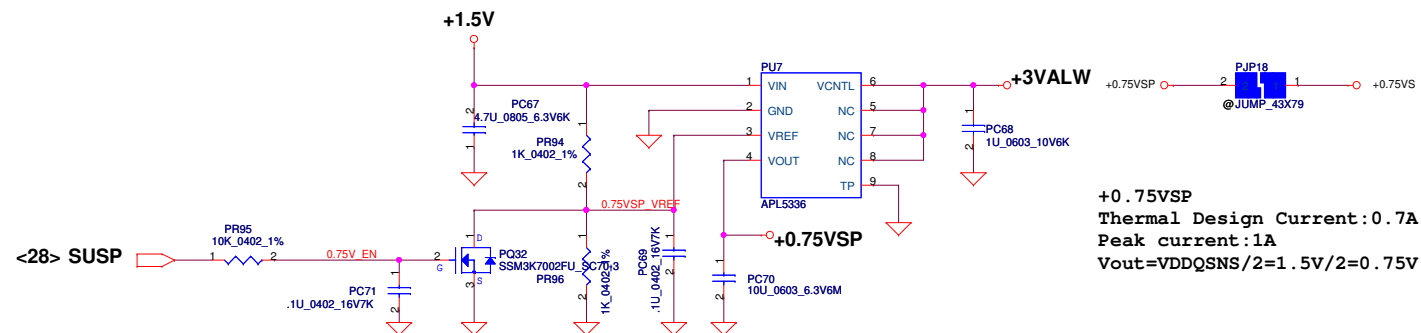
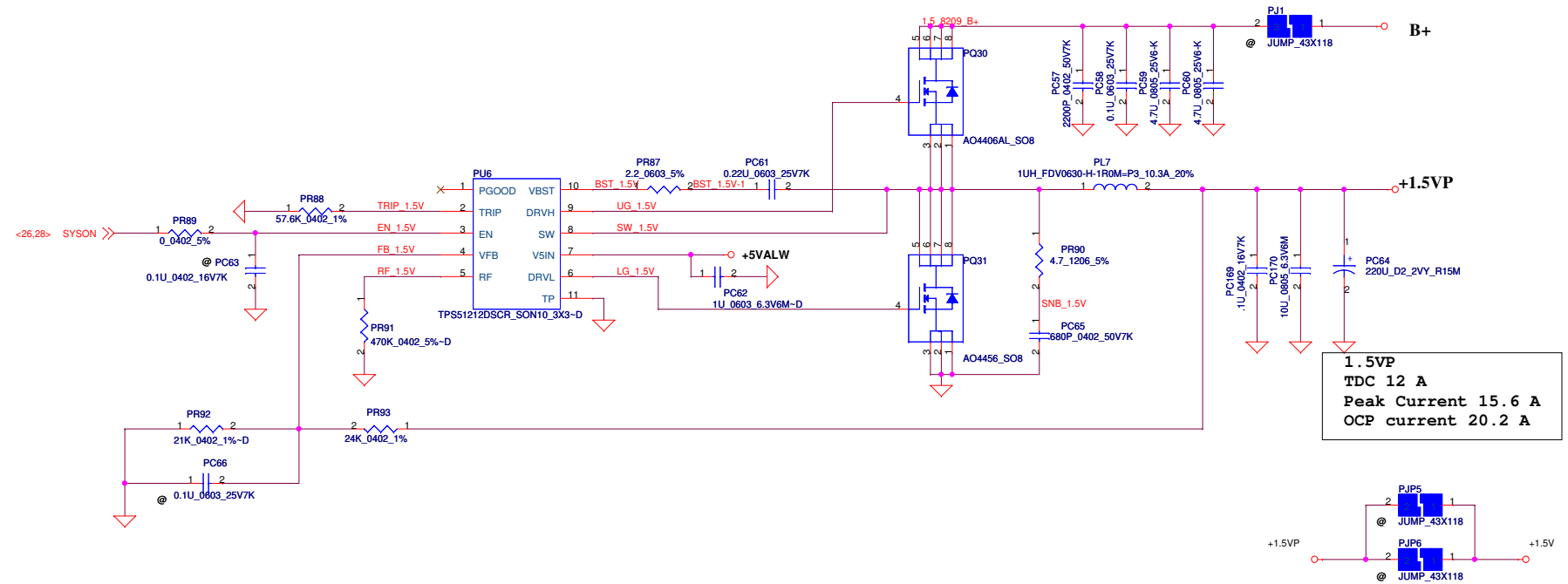
| BATT Type | Charging Voltage (0x15) | CV mode |
|-----------------------|-------------------------|---------|
| Normal 4S LI-ON Cells | 14800mV | 14.80V |

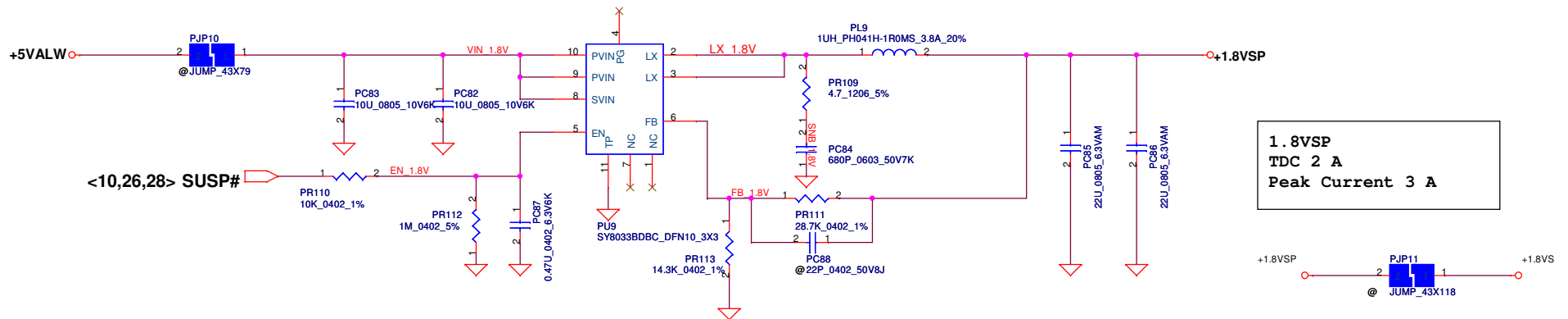
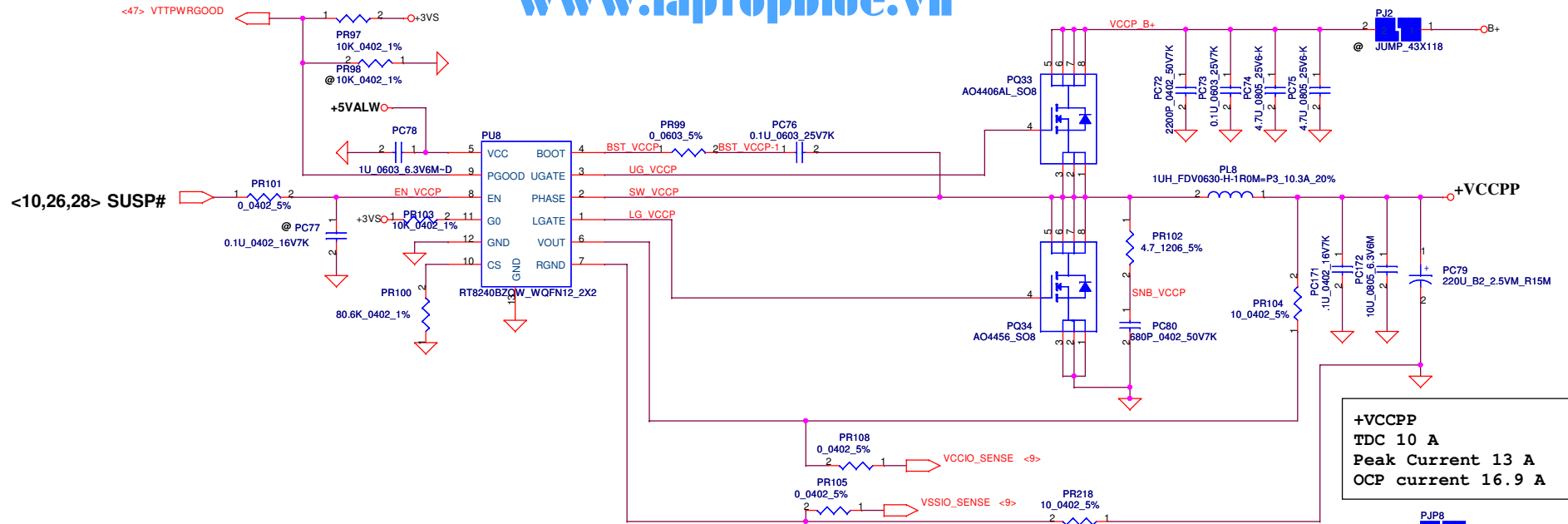
| CHGVADJ | CV mode |
|---------|----------------|
| 0V | 3.99V per cell |
| 1.93V | 4.2V per cell |
| 3.3V | 4.35V per cell |

3.3VALWP
TDC 4.02 A
Peak Current 5.7A
OCP current 7.4 A

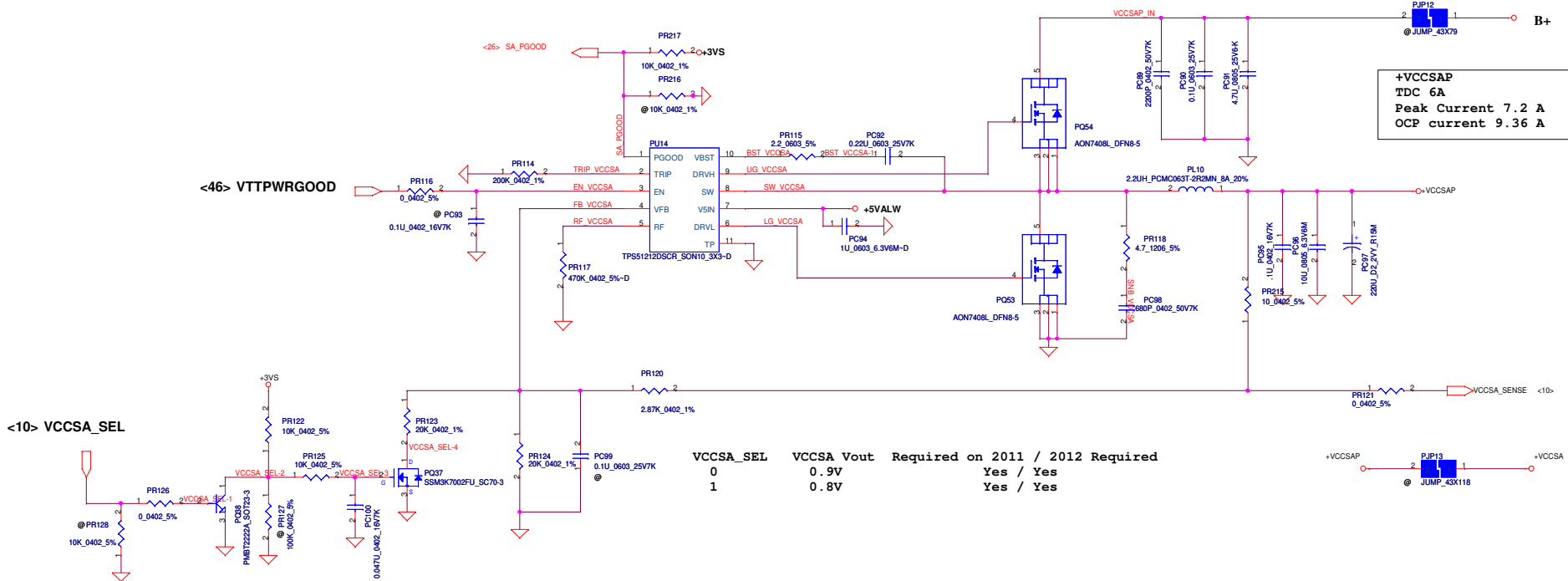


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| | | | | Sheet | 44 of 51 |
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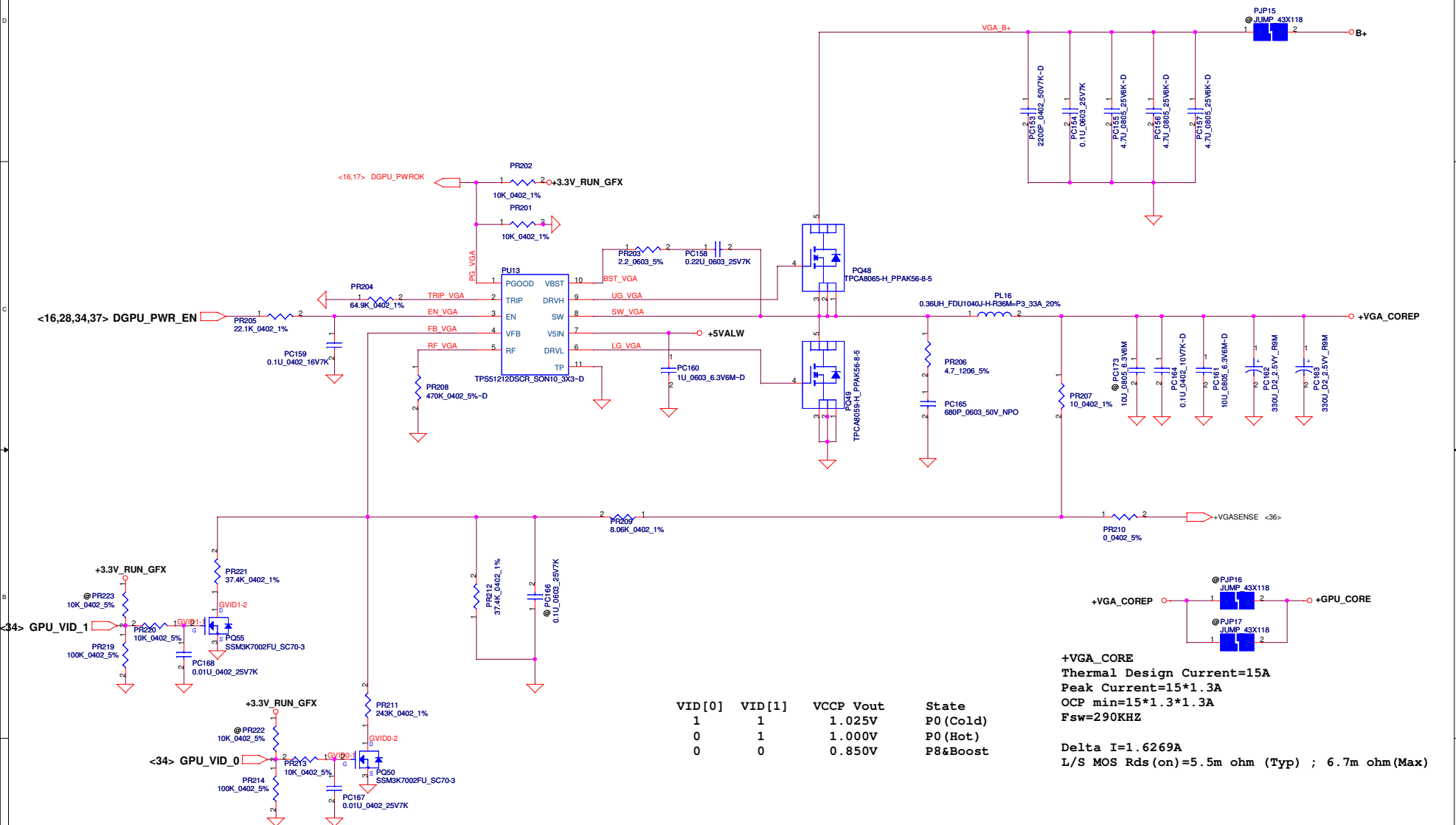


| | | | | | |
|---|------------|--------------------|------------|-------------------------------|-----------------------|
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2 2 p p h · P R R 7 2 3 0 6 9 K V W 8 8 6 F Q Y

| | | | | | | |
|---|--------------------|-----------------|------------|--------------------------|-------------------------|----------------|
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| | | | | Custom | Document Number | 1.0 |
| | | | | Date: | Thursday, July 28, 2011 | Sheet 48 of 51 |



Version change list (P.I.R. List)

Page 1 of 1 for PWR

| Item | Reason for change | Rev. | PG# | Modify List | Date | Phase |
|------|--|------|--------------------------|--|-----------|------------|
| 1 | modify Vcore and GFX boost resistance | | P48 | change PR136,PR163,PR179 to 2.2 +-5% 0603. | 2011.2.10 | before SSI |
| 2 | modify VGA FB resistance | | P50 | change PR211 to 243K +-1% 0402. PR221 to 37.4K +-1% 0402. | 2011.3.24 | SSI |
| 3 | modify 1.5V Enable signal | | P45 | change PR81 connect to SYSON. | 2011.3.24 | SSI |
| 4 | modify ADP_I protection | | P49 | change PR189 to 12.1k +-5% 0402. | 2011.3.24 | SSI |
| 5 | integrate mosfet | | P45 | change PQ53 PQ54 to AON7408L | | |
| 6 | modify Vcore and GFX's loadline and OCP | | P48 | change PR171 to 1.62K +-1% 0402 change PR170 to 3.48K +-1% 0402 change PR149 to 1.18K +-1% 0402 change PR131 to 2.7K +-1% 0402 change PC115 to .033U 16V K X7R 0402 | | |
| 7 | modify VGA for HW team suggest item | | P50 | add PR219 100K +-5% 0402 remove PR223 10K +-5% 0402 change PR205 to 22.1K +-1% 0402 | | |
| 8 | integrate mosfet | | P45 P47 | change PQ32 to SSM3K7002FU 1N SC70-3 change PQ37 to SSM3K7002FU 1N SC70-3 | | |
| 9 | add capacitance for RF team suggest item | | P43 P45 P46 P50 | change PC81 PC125 to 10U 25V K X5R 0805 H1.25 change PC169 to .1U 16V K X7R 0402 change PC170 to 10U 6.3V M X5R 0805 H1.25 change PC171 to .1U 16V K X7R 0402 change PC172 to 10U 6.3V M X5R 0805 H1.25 change PC173 to 10U 6.3V M X5R 0805 H1.25 | | |
| 10 | modify 1.5V OCP resistance | | P45 | change PR88 to 57.6K +-1% 0402 | | |
| 11 | modify VCCP OCP resistance | | P46 | change PR100 to 80.6K +-1% 0402 | | |
| 12 | modify choke footprint for DFX requirement | | | change PL5,PL6,PL7,PL8,PL10 to TAI-T_VMPI0703AR-100M-Z01_2P | | |
| 13 | modify PQ11 Vgs resistance | | P43 | change PR31 to 200K +-1% 0402 change PR35 to 47K +-1% 0402 | | |
| 14 | modify the net name of SPOK-' | | P49 | change the net name of PQ47 pin2 to SPOK1 change the net name of PQ47 pin1 to SPOK2 change the net name of PQ46 pin2 to SPOK3 | | |
| 15 | modify PU12 vcc power from +3VALW to +3VLP | | P49 | change PR190.1 to +3VLP change PR149.1 to +3VLP change PU12.1 to +3VLP | | |
| 16 | modify OTP resistance | | P49 | change PR190 to 23.2K +-1% 0402 change PR194 to 10K +-1% 0402 | | |
| 17 | modify VCORE VCCP resistance | | P48 | change PR145 to 1 +-5% 0603 | | |

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| | | | | Date: | Thursday, July 28, 2011 | Sheet 51 of 51 |