

Poseidon
Schematics Document

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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Cover Page			
Size A3	Document Number		Rev -1
Date: Tuesday, June 17, 2014	Sheet 1 of 102		

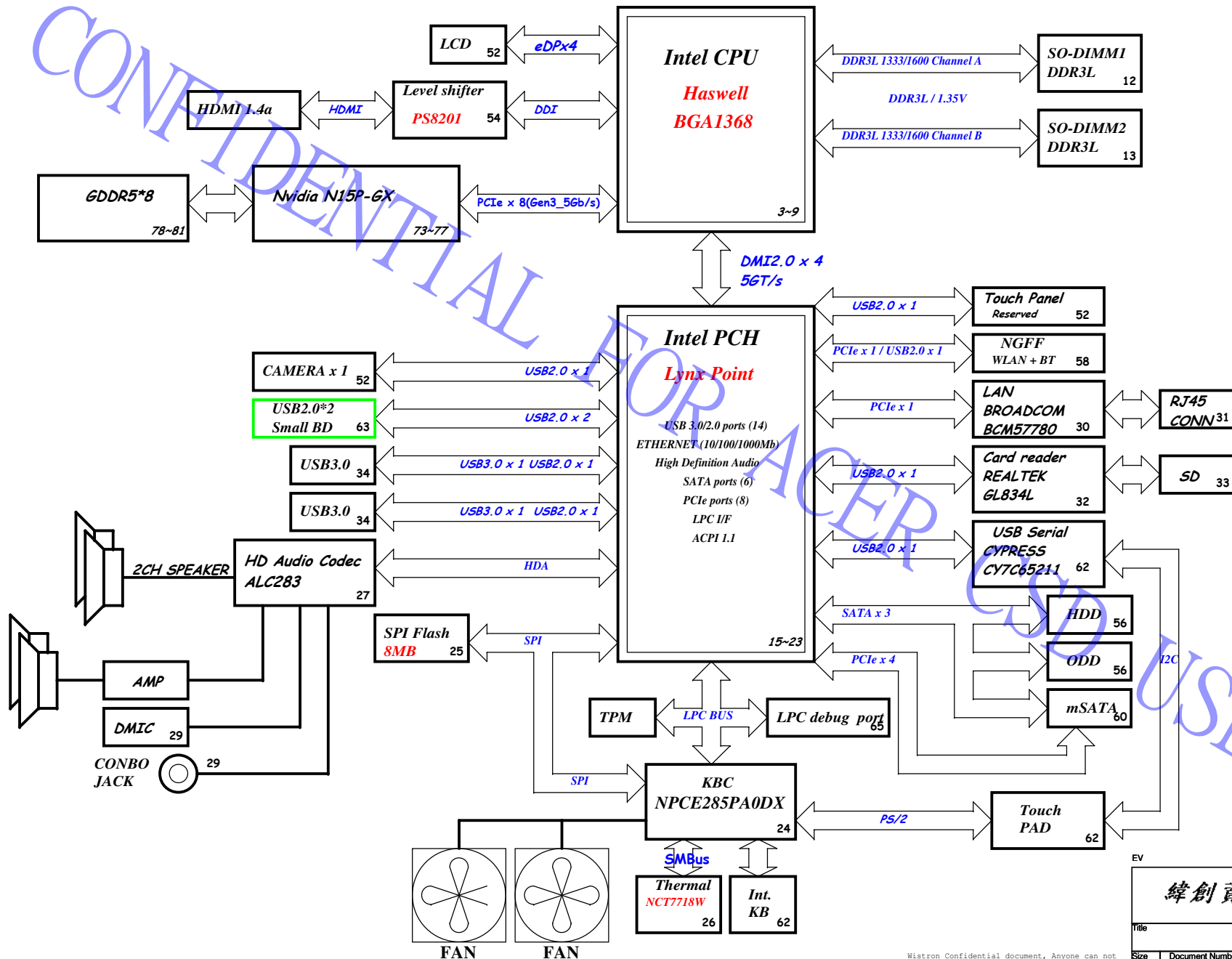
Poseidon Board Block Diagram

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Project code : 4PD02G010001

PCB NO : 14203

Revision : -2



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Title			
Block Diagram			
Size	Document Number	Rev	
Custom	Poseidon 860M	-1	
Date:	tuesday, June 17, 2014	Sheet 2 of	102

SSID = CPU

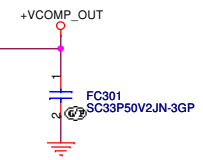
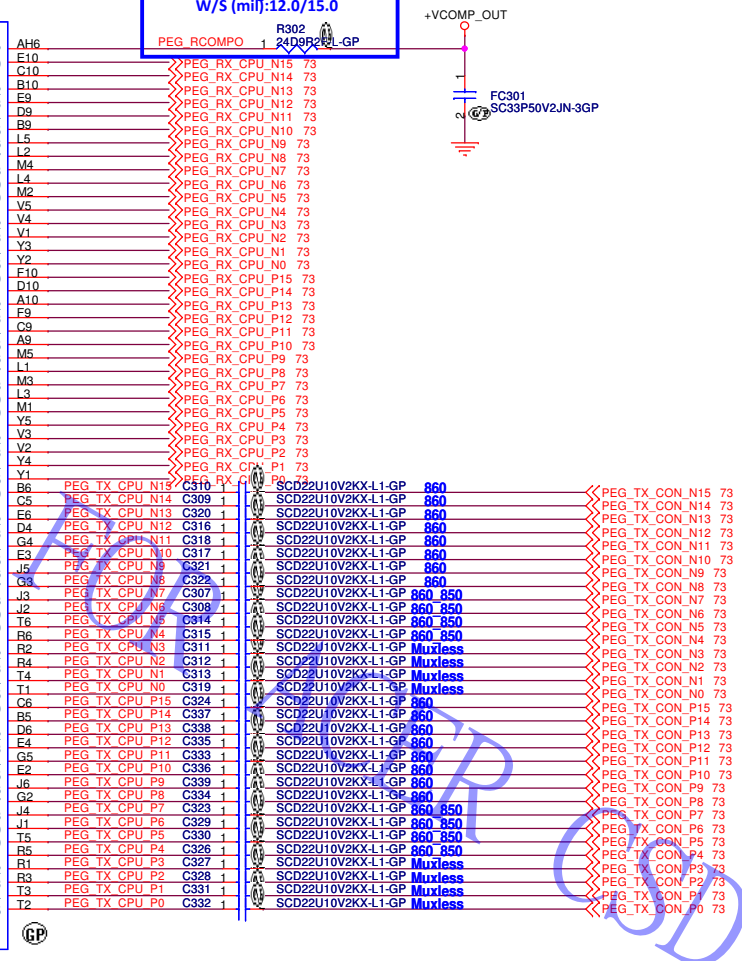
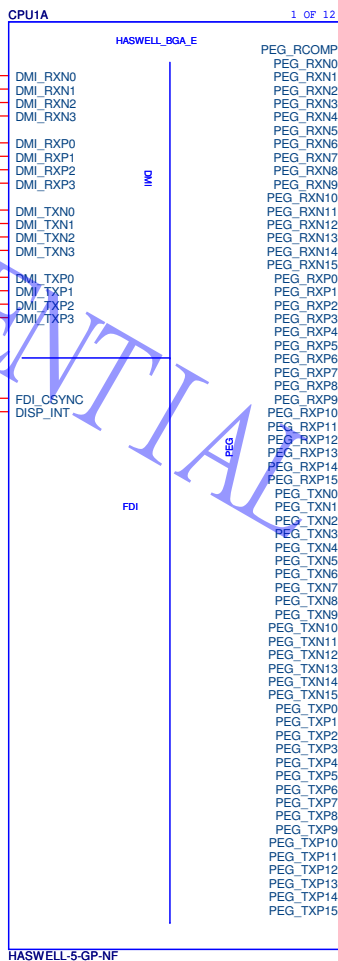
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Max Length : 400 Mil
W/S (mil):12.0/15.0

Max Length : 1000~8000 Mil
Max Via : 3

- 17 DMI_TX_CPU_N0 << DMI_TX_CPU_N0 AB2 DMI_RXN0
- 17 DMI_TX_CPU_N1 << DMI_TX_CPU_N1 AB3 DMI_RXN1
- 17 DMI_TX_CPU_N2 << DMI_TX_CPU_N2 AC3 DMI_RXN2
- 17 DMI_TX_CPU_N3 << DMI_TX_CPU_N3 AC1 DMI_RXN3
- 17 DMI_TX_CPU_P0 << DMI_TX_CPU_P0 AB1 DMI_RXP0
- 17 DMI_TX_CPU_P1 << DMI_TX_CPU_P1 AB4 DMI_RXP1
- 17 DMI_TX_CPU_P2 << DMI_TX_CPU_P2 AC4 DMI_RXP2
- 17 DMI_TX_CPU_P3 << DMI_TX_CPU_P3 AC2 DMI_RXP3
- 17 DMI_RX_CPU_N0 << DMI_RX_CPU_N0 AE2 DMI_TXN0
- 17 DMI_RX_CPU_N1 << DMI_RX_CPU_N1 AE4 DMI_TXN1
- 17 DMI_RX_CPU_N2 << DMI_RX_CPU_N2 AG4 DMI_TXN2
- 17 DMI_RX_CPU_N3 << DMI_RX_CPU_N3 AG2 DMI_TXN3
- 17 DMI_RX_CPU_P0 << DMI_RX_CPU_P0 AE1 DMI_TXP0
- 17 DMI_RX_CPU_P1 << DMI_RX_CPU_P1 AE3 DMI_TXP1
- 17 DMI_RX_CPU_P2 << DMI_RX_CPU_P2 AG3 DMI_TXP2
- 17 DMI_RX_CPU_P3 << DMI_RX_CPU_P3 AG1 DMI_TXP3

- 17 FDLCSYNC_CPU << F11 FDLCSYNC
- 17 FDL_INT_CPU << F12 FDL_DISP_INT



71.HASWE.D0U

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Pro- cessor	Physical Lanes													
				0	1	2	3	4	5	6	7	8	9	10	11	12	13
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1
x16	Off	Off	Reverse	1	1	1	1	1	1	2	2	7	6	5	4	3	2
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2

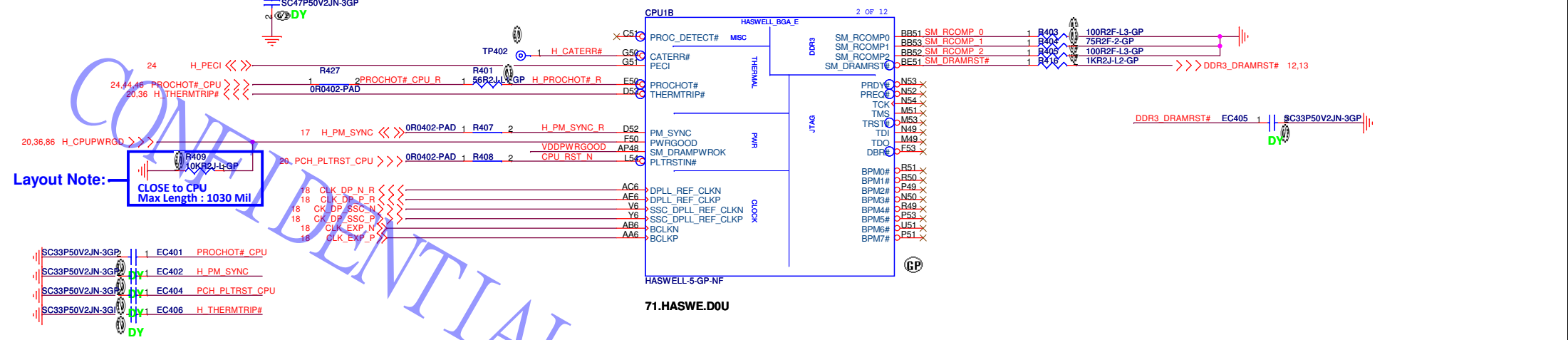
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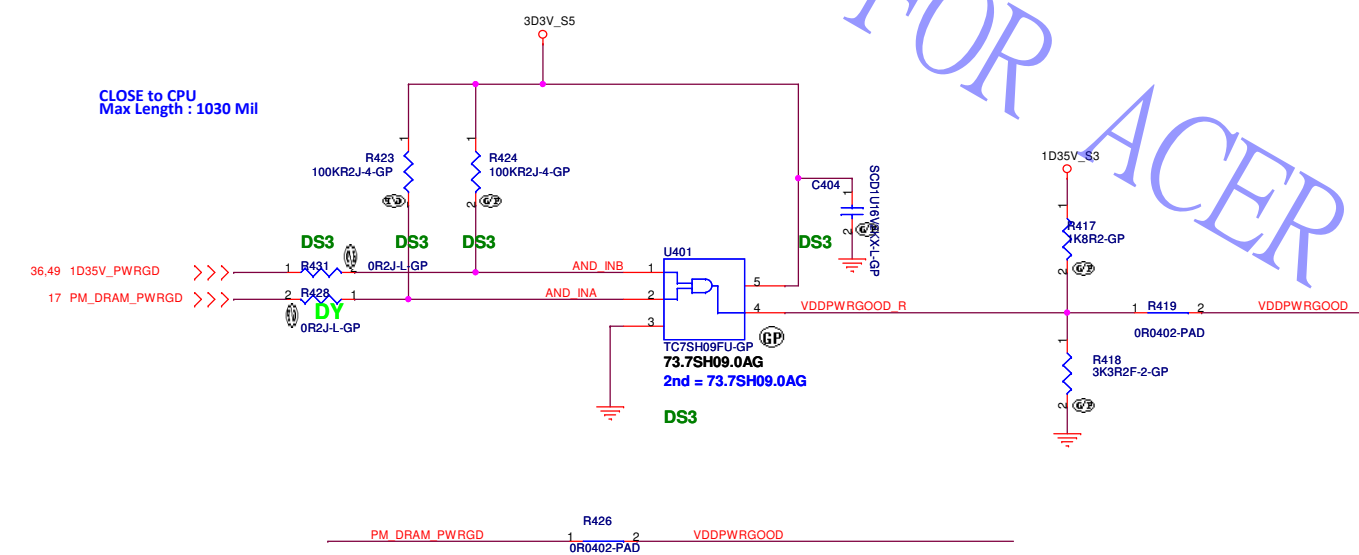
Title		
CPU (PCIe/DMI/FDI)		
Size A3	Document Number	Rev
	Poseidon 860M	-1
Date	Tuesday, June 17, 2014	
Sheet	3	of 102

SSID = CPU

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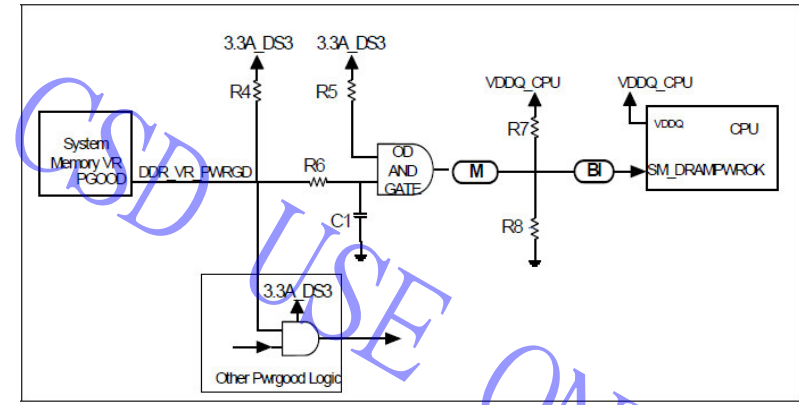


Layout Note:
CLOSE to CPU
Max Length : 1030 Mil

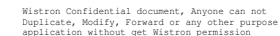


S3 Power Reduction Circuit
SM_DRAMRST#

SM_DRAMPWROK Topology for platforms supporting Deep S3



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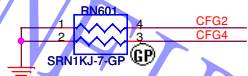


Title			
CPU (DDR)			
Size Custom	Document Number		Rev
	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014		Sheet 5 of 102

SSID = CPU

PEG Static Lane Reversal

CFG2 1: Normal Operation; Lane # definition matches socket pin map definition
0: Lane Reversed

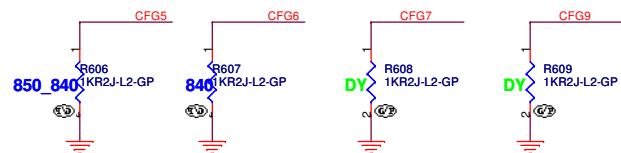


eDP Enable

CFG4 1: Disable
0: Enable

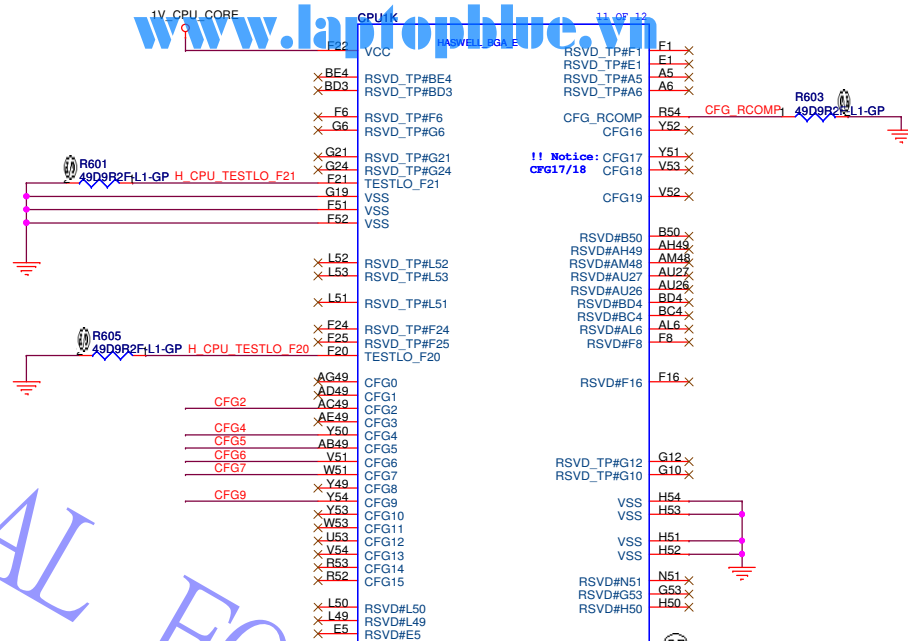
PCIe Port Bifurcation Straps

CFG[6:5] 11: x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

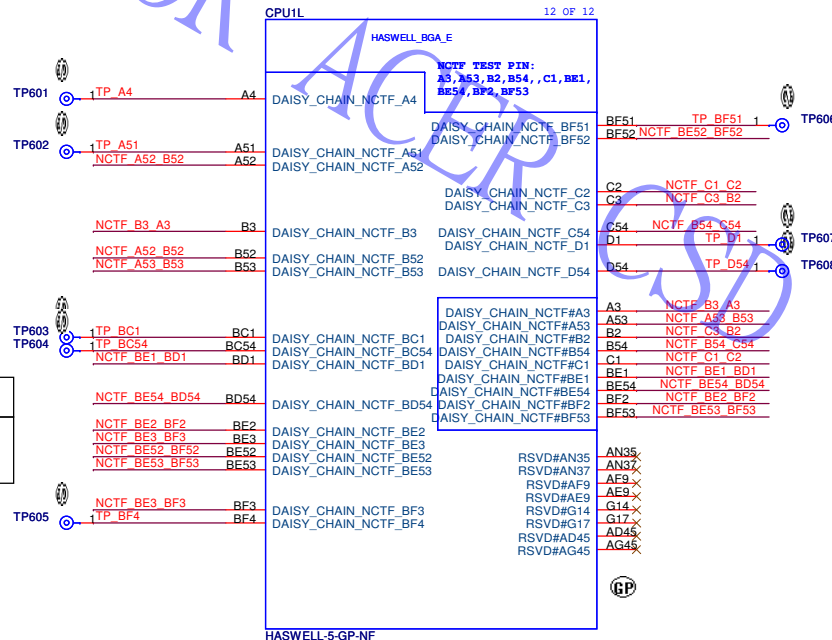


Reserved configuration lanes. A test point may be placed on the board for these lands.

CFG[19:7]



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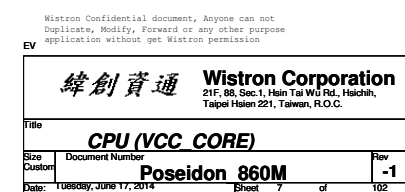
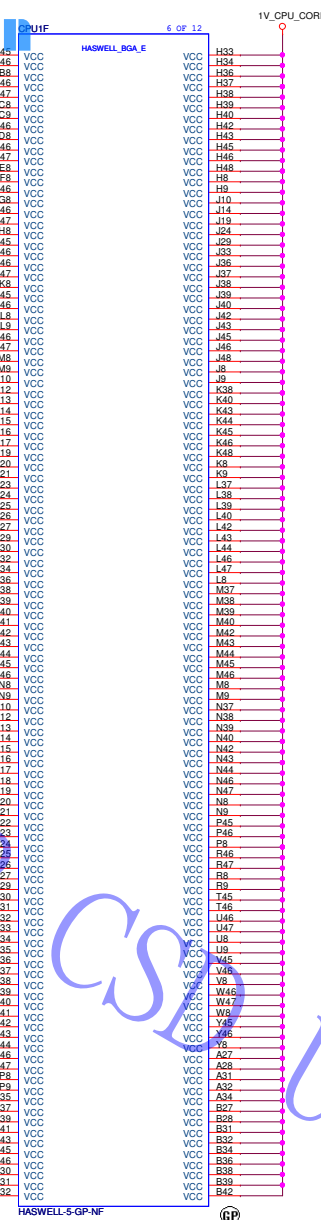
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Title		
CPU (CFG)		
Size	Document Number	Rev
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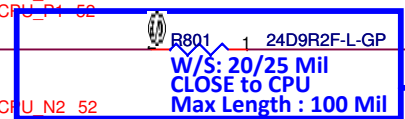
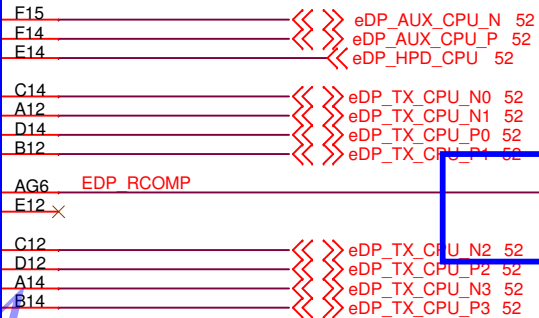
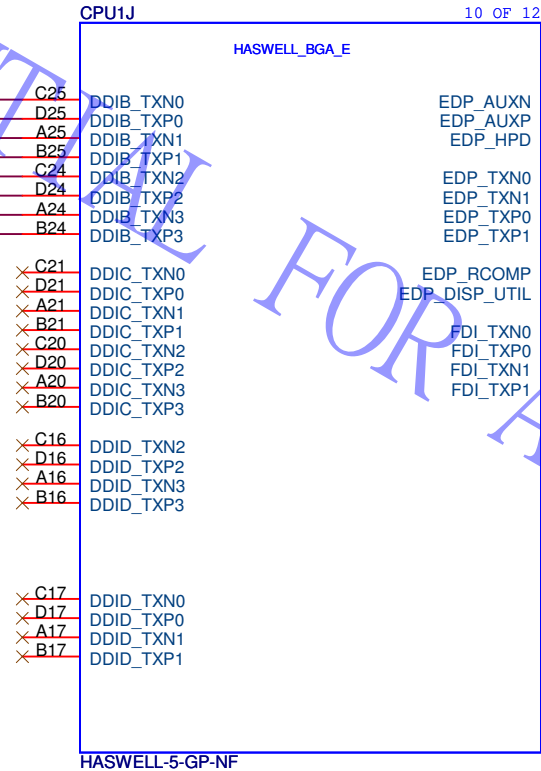
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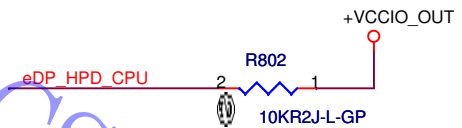
HDMI

54 HDMI_DATA_CPU_N2
54 HDMI_DATA_CPU_P2
54 HDMI_DATA_CPU_N1
54 HDMI_DATA_CPU_P1
54 HDMI_DATA_CPU_N0
54 HDMI_DATA_CPU_P0
54 HDMI_DATA_CPU_N3
54 HDMI_DATA_CPU_P3



+VCOMP_OUT

Layout Note:



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Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU (DDI/EDP)

Size A4	Document Number Poseidon 860M	Rev -1
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SSID = CPU

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CPU11 9 OF 12

CPU1G 7 OF 12

CPU1H 8 OF 12

CPU11 9 OF 12

A11 VSS	HASWELL_BGA_E	VSS	AJ48
A15 VSS		VSS	AJ51
A19 VSS		VSS	AJ54
A22 VSS		VSS	AK48
A26 VSS		VSS	AK5
A30 VSS		VSS	AK50
A34 VSS		VSS	AK7
A37 VSS		VSS	AL1
A40 VSS		VSS	AL4
A44 VSS		VSS	AL48
AA1 VSS		VSS	AL5
AA2 VSS		VSS	AL7
AA3 VSS		VSS	AM5
AA4 VSS		VSS	AM51
AA48 VSS		VSS	AM52
AA5 VSS		VSS	AM53
AA7 VSS		VSS	AM54
AB5 VSS		VSS	AM7
AB51 VSS		VSS	AU25
AB52 VSS		VSS	AU29
AB53 VSS		VSS	AU33
AB54 VSS		VSS	AU37
AB7 VSS		VSS	AN4
AB9 VSS		VSS	AN48
AC48 VSS		VSS	AN5
AC5 VSS		VSS	AN50
AC50 VSS		VSS	AN7
AC7 VSS		VSS	AP51
AD48 VSS		VSS	AP54
AD51 VSS		VSS	AP7
AD54 VSS		VSS	AR12
AD7 VSS		VSS	AR14
AD9 VSS		VSS	AR16
AE1 VSS		VSS	AR18
AE2 VSS		VSS	AR20
AE3 VSS		VSS	AR24
AE4 VSS		VSS	AR26
AE48 VSS		VSS	AR48
AE5 VSS		VSS	AR5
AE50 VSS		VSS	AR50
AE7 VSS		VSS	AR7
AF5 VSS		VSS	AW37
AF6 VSS		VSS	AW42
AF7 VSS		VSS	AT1
AG48 VSS		VSS	AT10
AG5 VSS		VSS	AT12
AG51 VSS		VSS	AT15
AG52 VSS		VSS	AT16
AG53 VSS		VSS	AT18
AG54 VSS		VSS	AT20
AG7 VSS		VSS	AT22
AG9 VSS		VSS	AT25
AH1 VSS		VSS	AT26
AH2 VSS		VSS	AT29
AH3 VSS		VSS	AT33
AH4 VSS		VSS	AT35
AH48 VSS		VSS	AT37
AH5 VSS		VSS	AT39
AH50 VSS		VSS	AT4
AH7 VSS		VSS	

HASWELL-5-GP-NF

71.HASWE.D0U

AT40 VSS	HASWELL_BGA_E	VSS	AY50
AT42 VSS		VSS	AY9
AT43 VSS		VSS	B11
AT44 VSS		VSS	B15
AT46 VSS		VSS	B19
AT47 VSS		VSS	B22
AT49 VSS		VSS	B26
AT5 VSS		VSS	B30
AT50 VSS		VSS	B33
AT51 VSS		VSS	B37
AT52 VSS		VSS	B40
AT53 VSS		VSS	B44
AT54 VSS		VSS	B49
AT55 VSS		VSS	B8
AT56 VSS		VSS	BA13
AT57 VSS		VSS	BA18
AT58 VSS		VSS	BA22
AT59 VSS		VSS	BA25
AT6 VSS		VSS	BA29
AT61 VSS		VSS	BA33
AT62 VSS		VSS	BA37
AT63 VSS		VSS	BA4
AT64 VSS		VSS	BA42
AT65 VSS		VSS	BA5
AT66 VSS		VSS	BA50
AT67 VSS		VSS	BA51
AT68 VSS		VSS	BA52
AT69 VSS		VSS	BA53
AT7 VSS		VSS	BA9
AT71 VSS		VSS	BB10
AT72 VSS		VSS	BB11
AT73 VSS		VSS	BB12
AT74 VSS		VSS	BB14
AT75 VSS		VSS	BB15
AT76 VSS		VSS	BB16
AT77 VSS		VSS	BB17
AT78 VSS		VSS	BB18
AT79 VSS		VSS	BB20
AT8 VSS		VSS	BB23
AT81 VSS		VSS	BB25
AT82 VSS		VSS	BB28
AT83 VSS		VSS	BB32
AT84 VSS		VSS	BB33
AT85 VSS		VSS	BB37
AT86 VSS		VSS	BB38
AT87 VSS		VSS	BB39
AT88 VSS		VSS	BB41
AT89 VSS		VSS	BB42
AT9 VSS		VSS	BB43
AT91 VSS		VSS	BB44
AT92 VSS		VSS	BB46
AT93 VSS		VSS	BB47
AT94 VSS		VSS	BB48
AT95 VSS		VSS	BB49
AT96 VSS		VSS	BB5
AT97 VSS		VSS	BB6
AT98 VSS		VSS	BB7
AT99 VSS		VSS	BB9

HASWELL-5-GP-NF

71.HASWE.D0U

BC10 VSS	HASWELL_BGA_E	VSS	G80
BC12 VSS		VSS	G23
BC15 VSS		VSS	G25
BC18 VSS		VSS	G26
BC22 VSS		VSS	G30
BC26 VSS		VSS	G33
BC3 VSS		VSS	G37
BC30 VSS		VSS	G40
BC33 VSS		VSS	G44
BC36 VSS		VSS	G49
BC38 VSS		VSS	G52
BC41 VSS		VSS	G54
BC43 VSS		VSS	G7
BC46 VSS		VSS	G8
BC48 VSS		VSS	G9
BC5 VSS		VSS	H44
BC50 VSS		VSS	H49
BC52 VSS		VSS	H7
BC7 VSS		VSS	J4
BD10 VSS		VSS	J49
BD15 VSS		VSS	J51
BD18 VSS		VSS	J54
BD2 VSS		VSS	J7
BD41 VSS		VSS	K1
BD46 VSS		VSS	K2
BD5 VSS		VSS	K3
BD51 VSS		VSS	K4
BE10 VSS		VSS	K5
BE15 VSS		VSS	K6
BE36 VSS		VSS	K7
BE41 VSS		VSS	L48
BE46 VSS		VSS	L7
BF10 VSS		VSS	L9
BF12 VSS		VSS	M48
BF18 VSS		VSS	M50
BF22 VSS		VSS	M52
BF26 VSS		VSS	M54
BF30 VSS		VSS	M7
BF33 VSS		VSS	N48
BF36 VSS		VSS	N7
BF43 VSS		VSS	P1
BF46 VSS		VSS	P2
BF48 VSS		VSS	P3
BF7 VSS		VSS	P4
C11 VSS		VSS	P48
C15 VSS		VSS	P5
C19 VSS		VSS	P50
C22 VSS		VSS	P52
C23 VSS		VSS	P54
C26 VSS		VSS	P6
C30 VSS		VSS	P7
C33 VSS		VSS	P48
C37 VSS		VSS	R7
C40 VSS		VSS	T48
C44 VSS		VSS	U1
C49 VSS		VSS	U2
C5 VSS		VSS	U3
C52 VSS		VSS	U4
C53 VSS		VSS	U48
C54 VSS		VSS	U5
D11 VSS		VSS	U50
D15 VSS		VSS	U52
D19 VSS		VSS	U54
D22 VSS		VSS	U6
D26 VSS		VSS	V48
D30 VSS		VSS	V7
D33 VSS		VSS	V5
D37 VSS		VSS	V48
D40 VSS		VSS	W50
D44 VSS		VSS	W52
D49 VSS		VSS	W54
D8 VSS		VSS	W7
E11 VSS		VSS	Y48
E15 VSS		VSS	Y7
E16 VSS		VSS	Y9
E17 VSS		VSS	
E19 VSS		VSS	AR22
E20 VSS		VSS	AB48
E21 VSS		VSS	P9
E22 VSS		VSS	G18
E24 VSS		VSS	
E25 VSS		VSS	A49
E26 VSS		VSS	A50
E30 VSS		VSS	A8
E33 VSS		VSS	B4
E37 VSS		VSS	BA1
E40 VSS		VSS	BA54
E44 VSS		VSS	BB1
E48 VSS		VSS	BB54
E51 VSS		VSS	BD2
E53 VSS		VSS	BD53
E8 VSS		VSS	BF49
F2 VSS		VSS	BF5
F26 VSS		VSS	BF50
F3 VSS		VSS	BF6
F30 VSS		VSS	C53
F33 VSS		VSS	D2
F37 VSS		VSS	E54
F4 VSS		VSS	F54
F40 VSS		VSS	G1
F44 VSS		VSS	
F48 VSS		VSS	
F5 VSS		VSS	
G11 VSS		VSS	
G13 VSS		VSS	
G16 VSS		VSS	

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71.HASWE.D0U

VSS_NCTF#A49
VSS_NCTF#A50
VSS_NCTF#A8
VSS_NCTF#B4
VSS_NCTF#B41
VSS_NCTF#BA54
VSS_NCTF#BB1
VSS_NCTF#BB54
VSS_NCTF#BD2
VSS_NCTF#BD53
VSS_NCTF#BF49
VSS_NCTF#BF5
VSS_NCTF#BF50
VSS_NCTF#BF6
VSS_NCTF#C53
VSS_NCTF#D2
VSS_NCTF#E54
VSS_NCTF#F54
VSS_NCTF#G1
VSS_SENSE
D50

>>> VSS_SENSE 7,46

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CPU (VSS)			
Size	Document Number	Rev	
Custom	Poseidon 860M	-1	
Date:	Tuesday, June 17, 2014	Sheet	9 of 102



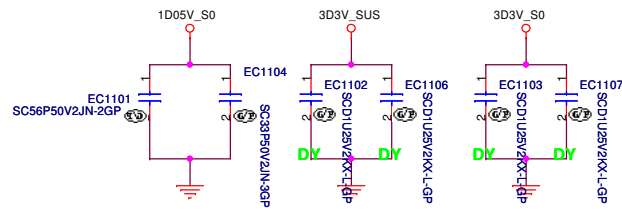
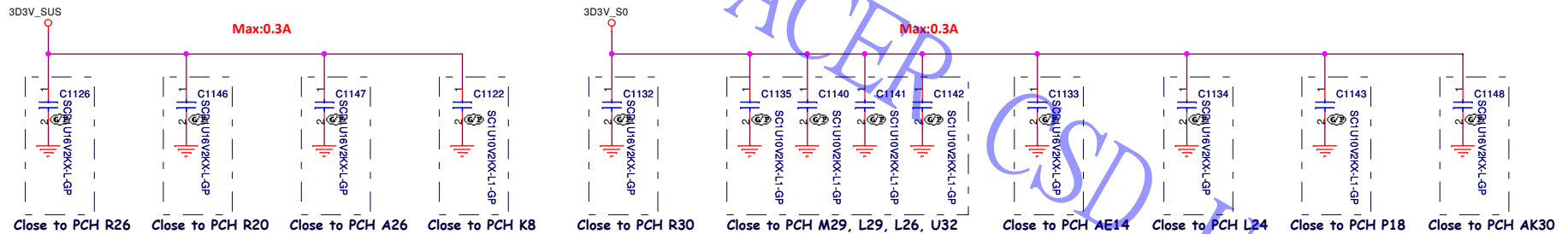
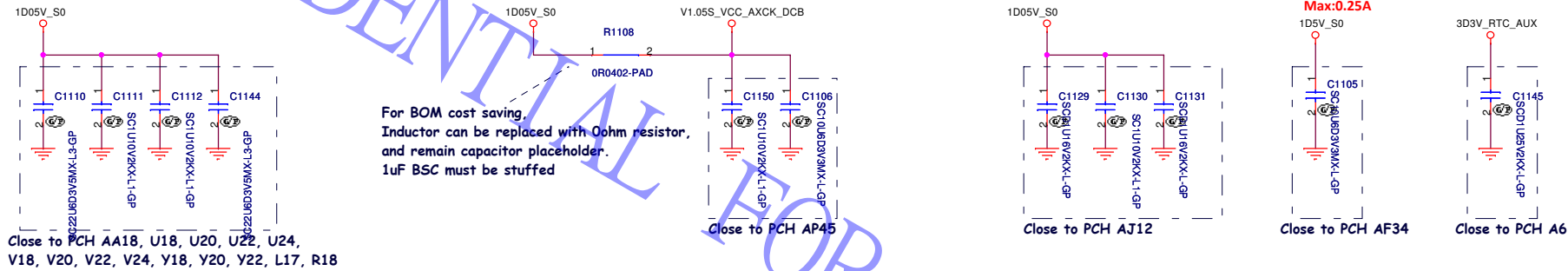
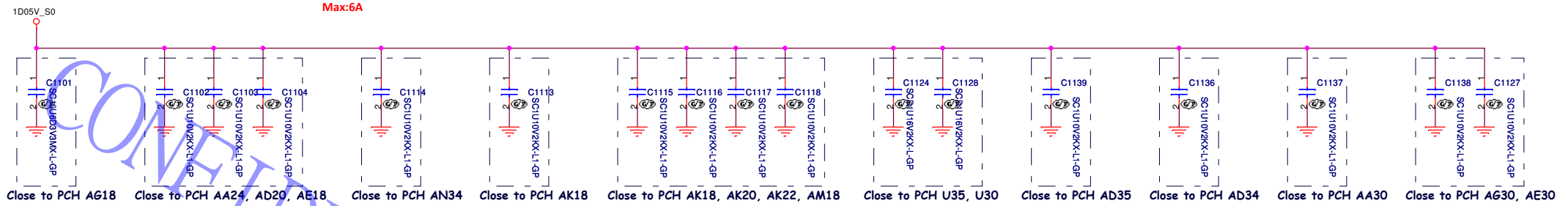
CPU (Power CAP1)

Rev

Poseidon 860M

-1

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SSID = MEMORY

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Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

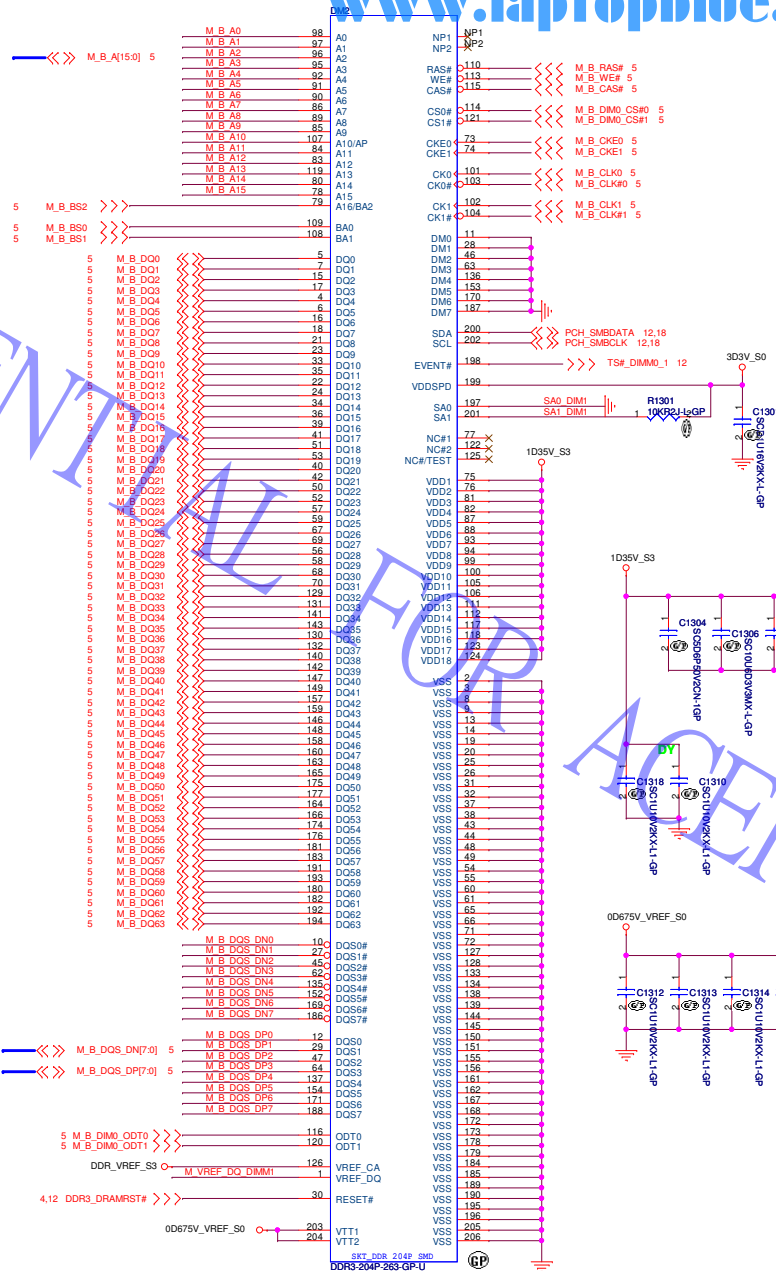
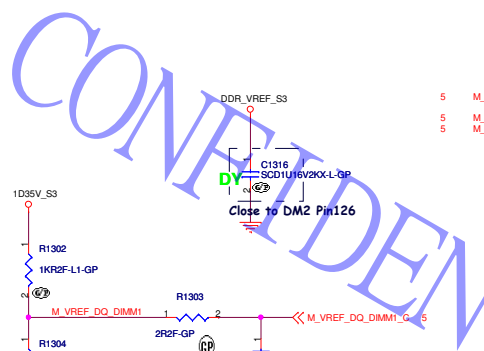
Layout Note:
Place these Caps near
SO-DIMMA.
SODIMMA A DECOUPLING

Place these caps
close to VTT1 and
VTT2.

62.10024.S21
2nd = 62.10024.M31
3rd = 62.10024.Q61

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Title		
DDR3-SODIMM1		
Size	Document Number	Rev
Custom	Poseidon 860M	-1
Date:	1065day, June 17, 2014	Sheet 12 of 102

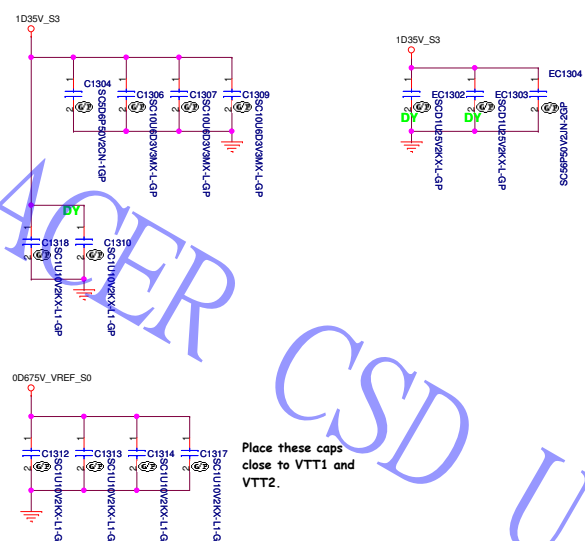
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Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

Layout Note:
Place these Caps near
SO-DIMMB.



Place these caps close to VTT1 and VTT2.

62.10024.S61
2nd = 62.10024.M51
3rd = 62.10024.Q71

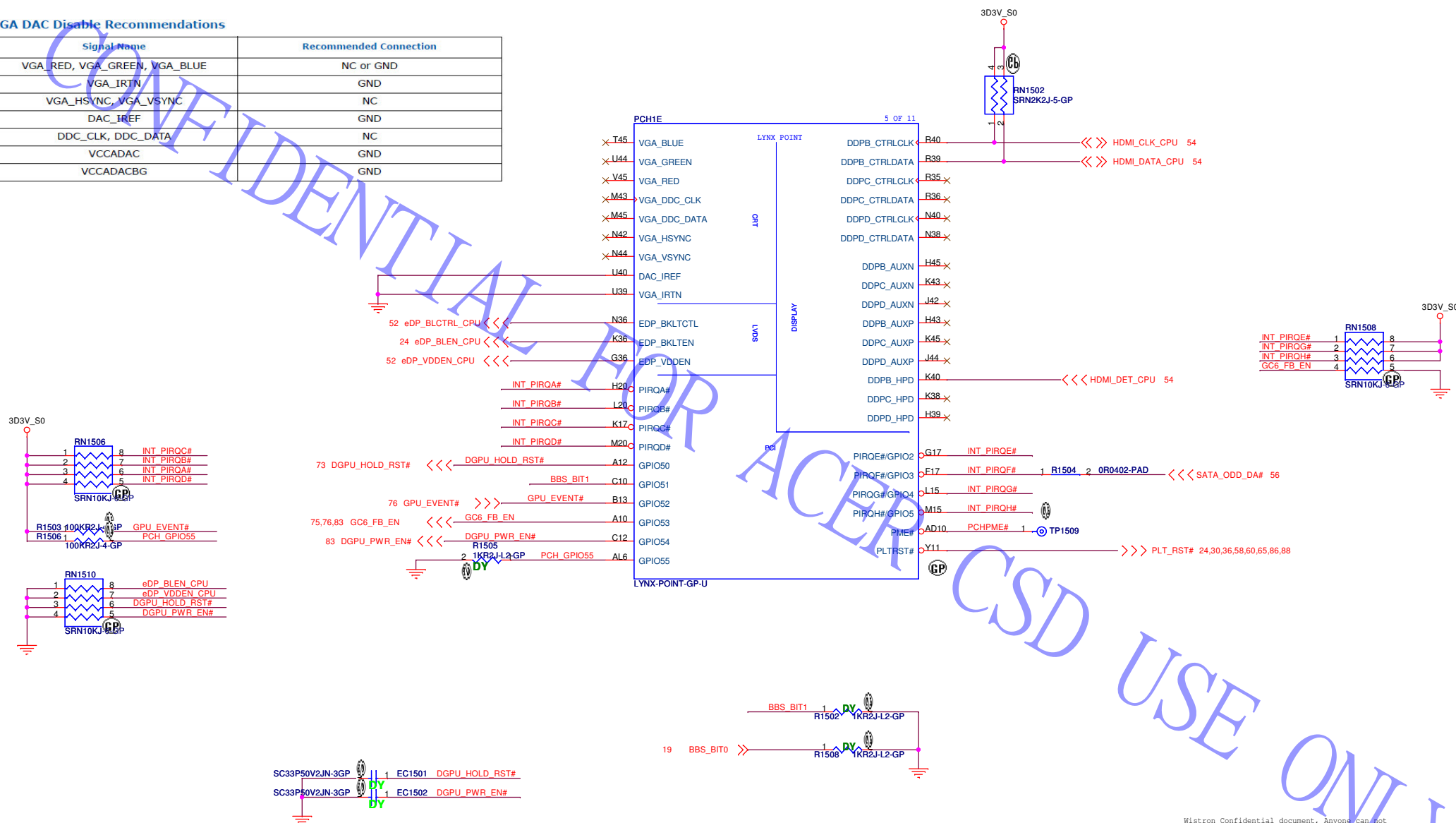
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Title			
(Reserved) SODIMM SODIMM4			
Size	Document Number		Rev
A4	Poseidon 860M		-1
Date: Tuesday, June 17, 2014		Sheet 14	of 102

Signal Name	Recommended Connection
VGA_RED, VGA_GREEN, VGA_BLUE	NC or GND
VGA_IRTN	GND
VGA_HSYNC, VGA_VSYNC	NC
DAC_IREF	GND
DDC_CLK, DDC_DATA	NC
VCCADAC	GND
VCCADACBG	GND



BOOT BIOS Strap		
GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

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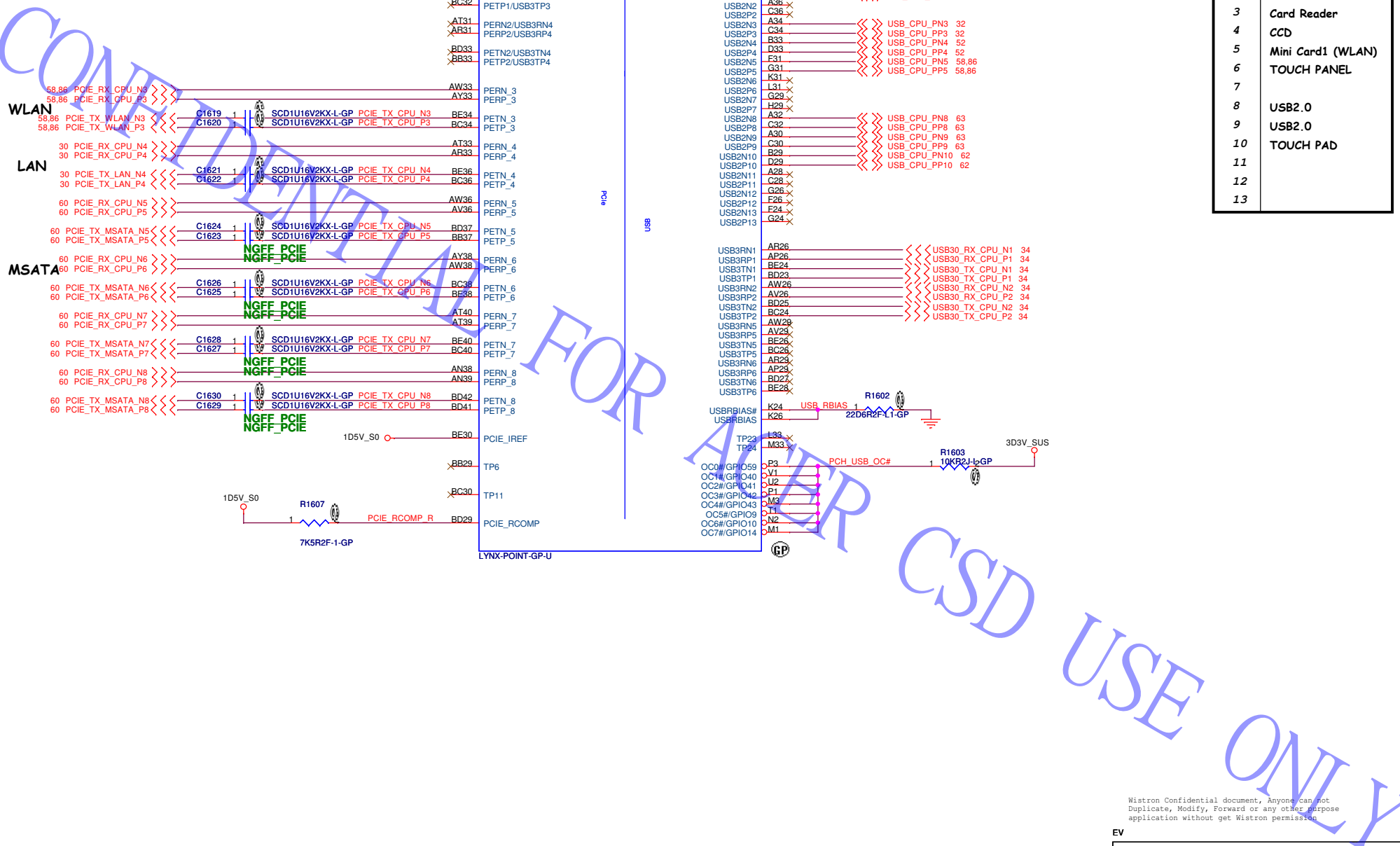
Title			
CPU(EDP SIDEBAND/GPIO/DDI)			
Size	Document Number		Rev
A3		Poseidon 860M	-1
Date:	Tuesday, June 17, 2014	Sheet 15 of	102

SSID = PCH

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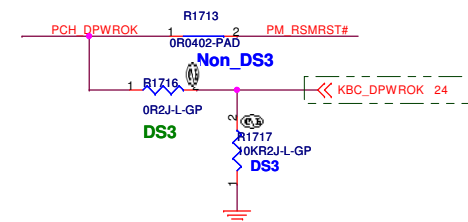
USB Table

Pair	Device
0	USB3.0(port0)
1	USB3.0(port1)
2	
3	Card Reader
4	CCD
5	Mini Card1 (WLAN)
6	TOUCH PANEL
7	
8	USB2.0
9	USB2.0
10	TOUCH PAD
11	
12	
13	



Intel® FDI Signal Disabling and Termination Guidelines

Signal	Description	Disable Guidelines
FDI_RXP[0:1] FDI_RXN[0:1]	Intel FDI Receive Differential Pair on PCH	Float
FDI_TXP[0:1] FDI_TXN[0:1]	Intel FDI Transmit Differential Pair on Processor	Float
FDI_CSYN	Intel FDI Composite Sync	Connect to Processor and PCH
DISP_INT	Intel FDI Hot Plug Interrupt	Connect to Processor and PCH
FDI_RCOMP	FDI Resistor Compensation	Float
FDI_IOREF	FDI Reference Voltage	Float

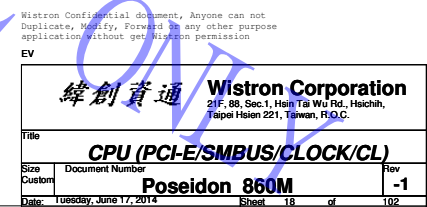


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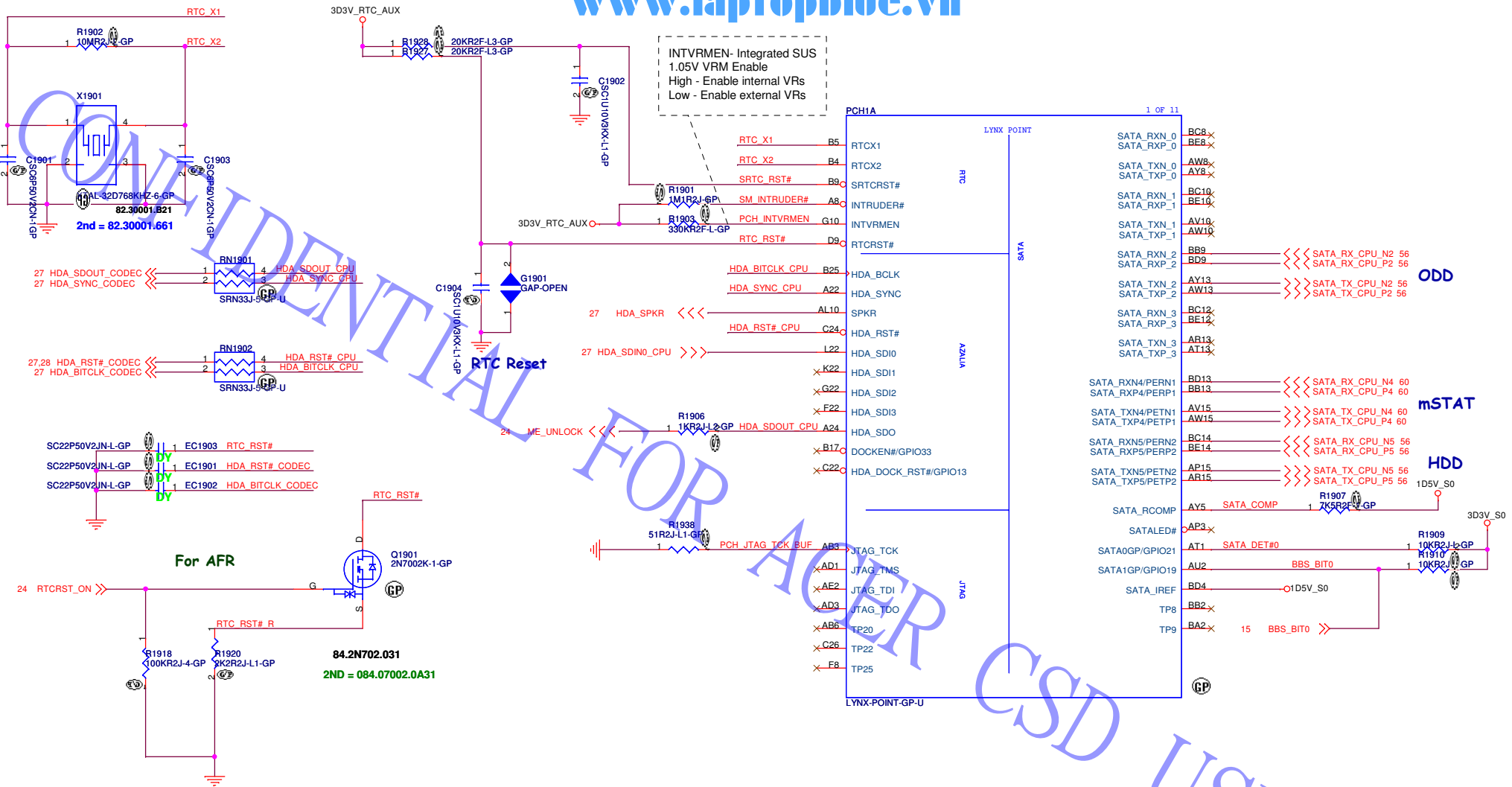
Title			
CPU (DMI/FDI/PM)			
Size A3	Document Number		Rev
	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014	Sheet 17 of	102

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SSID = PCH

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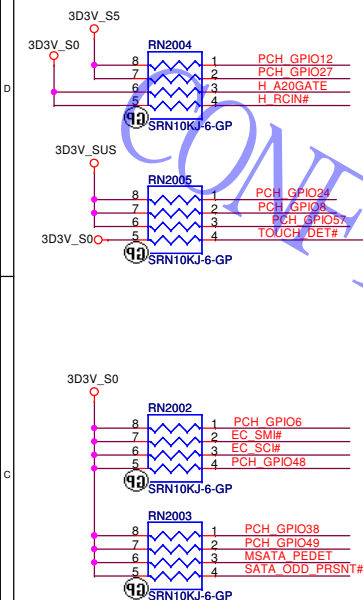
HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

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CPU (RTC/LPC/SATA/HDA)	
Title Size Custom	Document Number Poseidon 860M
Date: Tuesday, June 17, 2014	Sheet 19 of 102

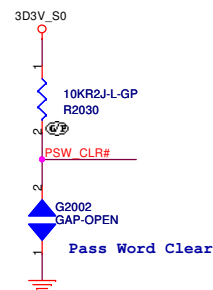
SSID = PCH

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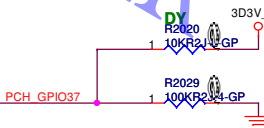
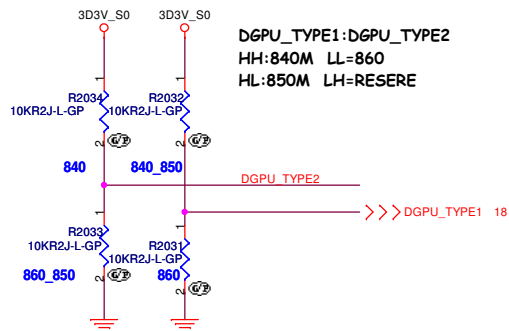


56

56

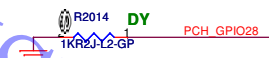
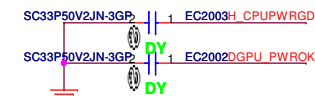


DGPU_TYPE1:DGPU_TYPE2
HH:840M LL=860
HL:850M LH=RESERE



TLS Confidentiality

0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality)



PLL ON DIE VR ENABLE

ENABLED -- HIGH (R2013 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2013 STUFFED)

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1D05V_S0

AA24 VCC
AA26 VCC
AD20 VCC
AD22 VCC
AD24 VCC
AD26 VCC
AD28 VCC
AE18 VCC
AE20 VCC
AE22 VCC
AE24 VCC
AE26 VCC
AG18 VCC
AG20 VCC
AG22 VCC
AG24 VCC
Y26 VCC

1D05V_S0

+PCH_VCCDSW

U14 DCPSUSBYP
AA18 VCCASW
U18 VCCASW
U20 VCCASW
U22 VCCASW
U24 VCCASW
V18 VCCASW
V20 VCCASW
V22 VCCASW
V24 VCCASW
Y18 VCCASW
Y20 VCCASW
Y22 VCCASW

Core

LYNX POINT

VCCADAC1_5

CRT DAC

VSS

VCCADACBG3_3

FDI

VCCVRM

VCCIO

VCCIO

HVCMOS

VCC3_3_R30

VCC3_3_R32

DCPSUS1

VCCSUS3_3

VCCSUS3_3

USB3

DCPSUS3#AJ26

DCPSUS3#AJ28

VCCIO

VCCVRM

VCCVRM

PCIe/DMI

VCCVRM

VCCIO

SATA

VCCVRM

VCCIO

VCCMPHY

VCCIO

VCCIO

VCCIO

VCCIO

VCCIO

VCCIO

LYNX-POINT-GP-U



EV

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Title

CPU (POWER1)

Size

A4

Document Number

Poseidon 860M

Rev

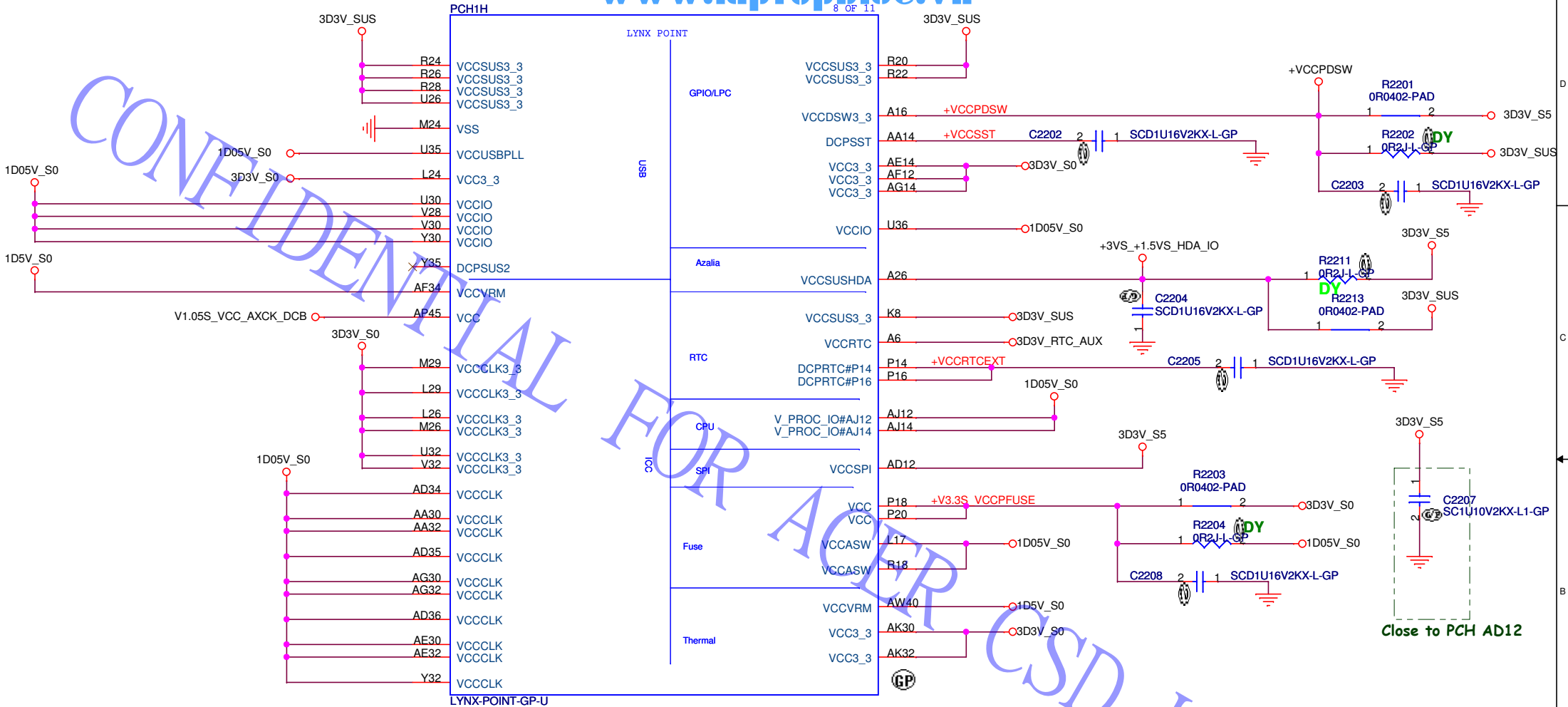
-1

Date: Tuesday, June 17, 2014

Sheet 21

of

102

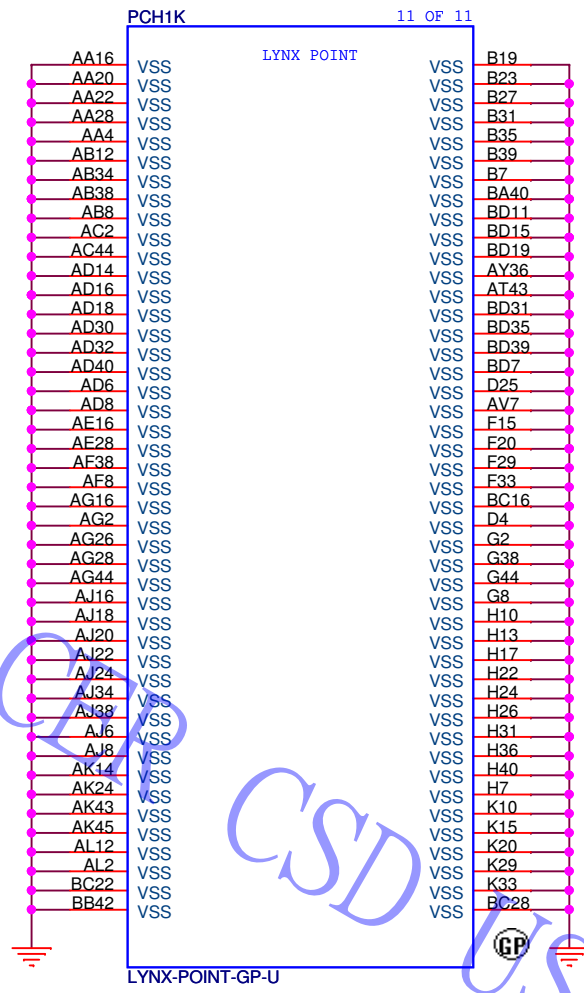
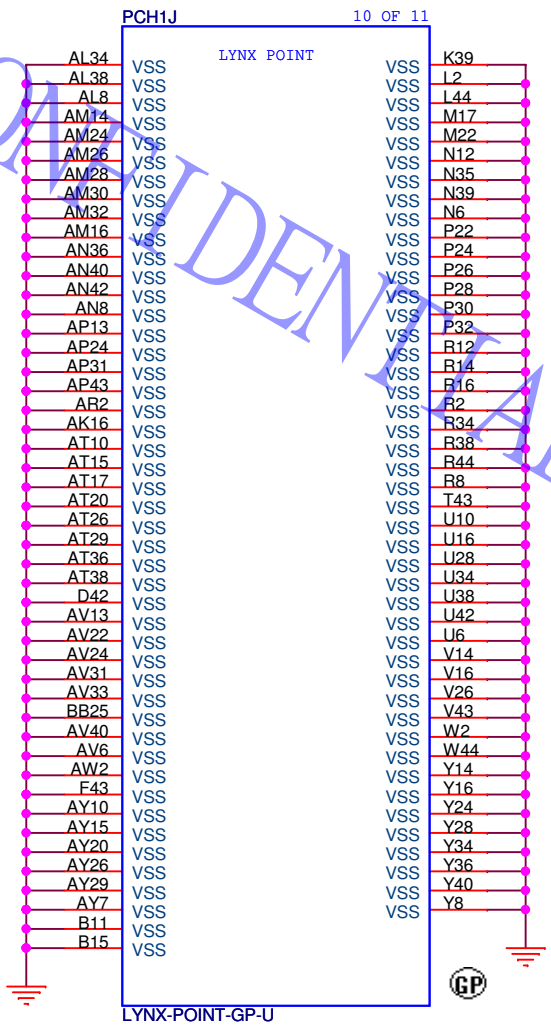


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<p>Title</p> <p>CPU (RSVD)</p>	
<p>Size</p> <p>Custom</p>	<p>Document Number</p> <p>Poseidon 860M</p>
<p>Date: Tuesday, June 17, 2014</p>	<p>Sheet 22 of 102</p>
<p>Rev</p> <p>-1</p>	

SSID = PCH



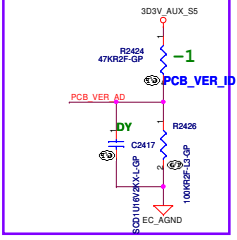
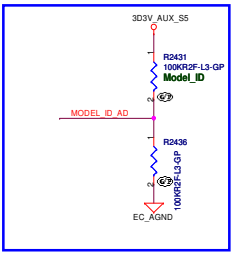
SSID = KBC

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BATTERY / CHARGER-->

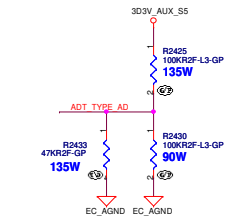
Thermal/eDP/GPU-->

Touch Pad-->



Model_ID	AD	Pull-Low Register	Pull-High Register	Typical Voltage
VA30		100.0 K	10.0 K	3.000 V
Hades UMA		100.0 K	20.0 K	2.750 V
Hades DIS 840		100.0 K	33.0 K	2.481 V
Hades DIS 850		100.0 K	47.0 K	2.245 V
Poseidon UMA		100.0 K	64.9 K	2.001 V
Poseidon DIS 840		100.0 K	76.8 K	1.867 V
Poseidon DIS 860		100.0 K	100.0 K	1.650 V
Poseidon DIS 850		100.0 K	143.0 K	1.358 V
Reserved for project use		100.0 K	174.0 K	1.204 V
Reserved for project use		100.0 K	215.0 K	1.048 V

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	< 2.616 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	< 1.758 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	< 1.281 V



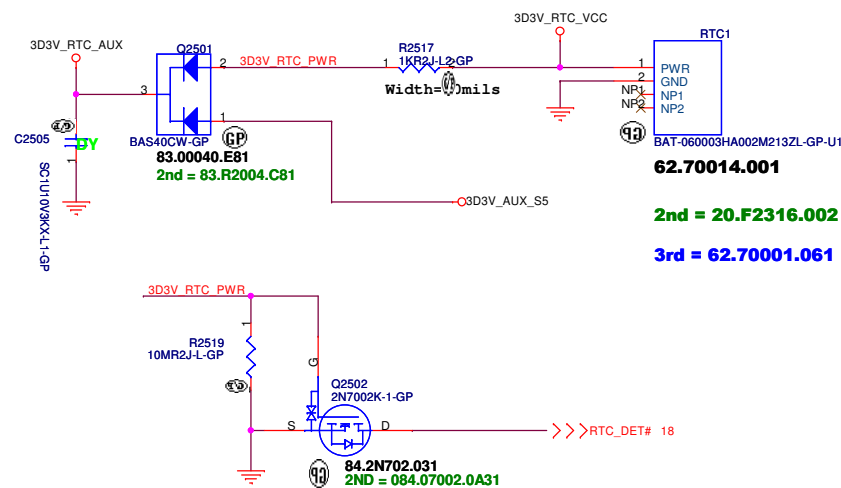
ADT_TYP_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
65W	N/A	100.0 K	3.300 V	0.000 V		>= 3.000 V
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.3055	0.2945	>= 0.150 V
40W	20.0 K	100.0 K	0.550 V	0.5592	0.5409	>= 0.425 V
120W	33.0 K	100.0 K	0.819 V	0.8312	0.8065	>= 0.684 V
130W	47.0 K	100.0 K	1.055 V	1.0695	1.0408	>= 0.937 V
150W	64.9 K	100.0 K	1.299 V	1.3146	1.2831	>= 1.177 V
Reserved	76.8 K	100.0 K	1.433 V	1.4497	1.4173	>= 1.366 V
Reserved	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.542 V

SPI FLASH ROM (8M byte) for PCH

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[illegible]

SSID = RBAT



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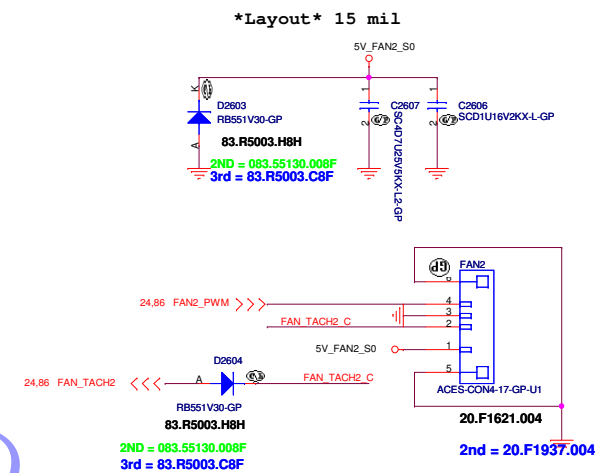
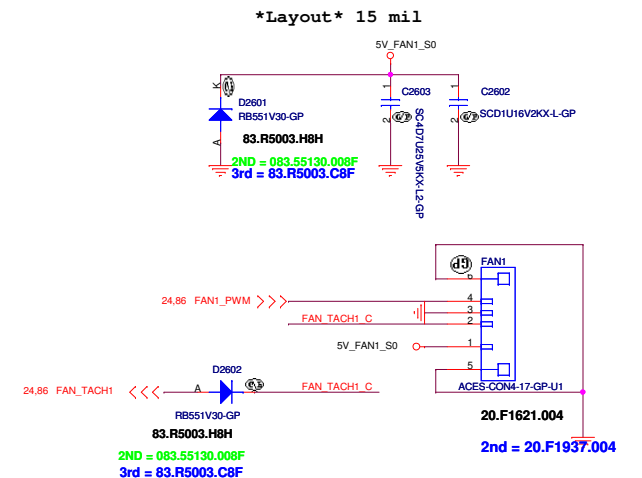
緯創資通

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Title			
Flash(KBC+PCH)/RTC			
Size A3	Document Number		Rev
	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014	Sheet 25 of	102

Thermal sensor NCT 7718W

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	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5					
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

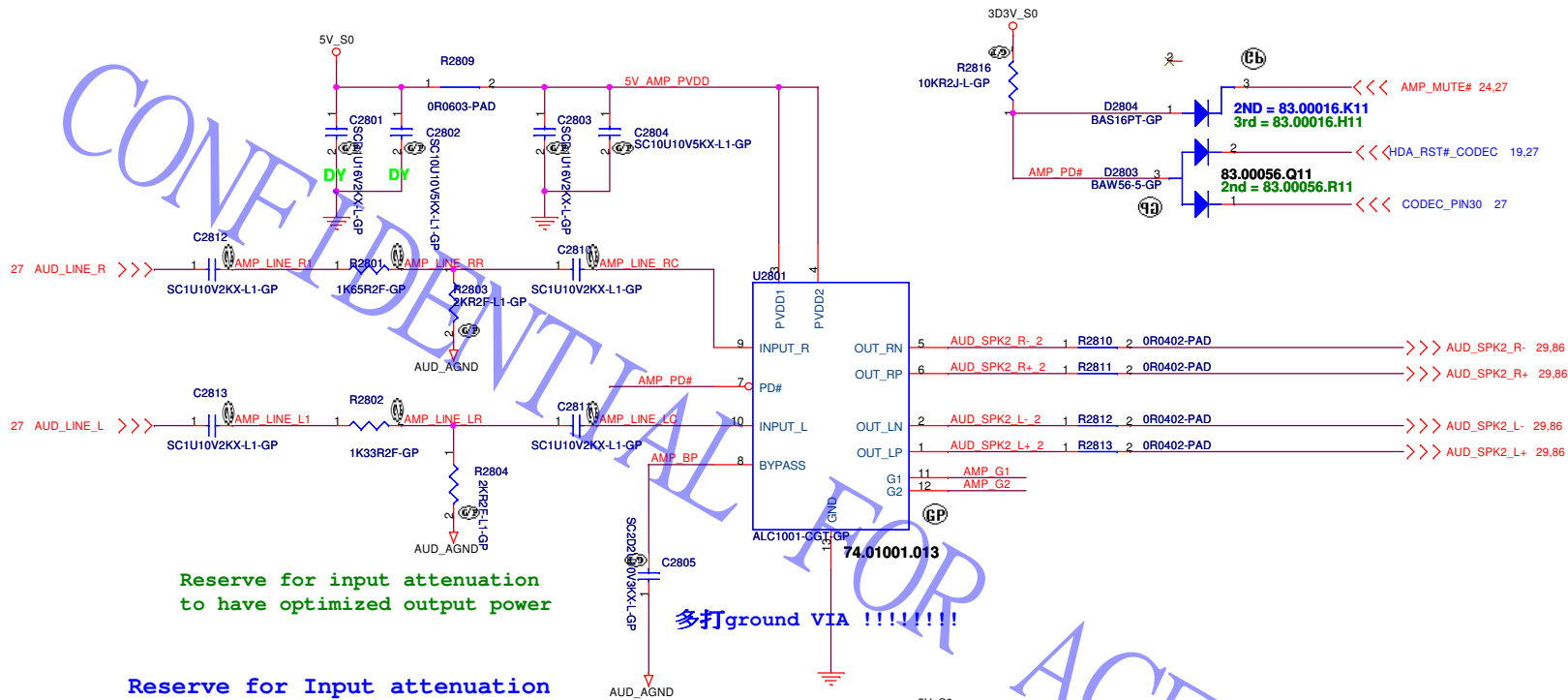
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Title		
Thermal 7718/Fan Controllor P2793		
Size Custom	Document Number	Rev
	Poseidon 860M	-1
Date:	Tuesday, June 17, 2014	Sheet 26 of 102

F

Title			
Audio Codec ALC283			
Size	Document Number	Rev	
C	Poseidon 860M	-1	
Date:	Tuesday, June 17, 2014	Sheet 27 of	102



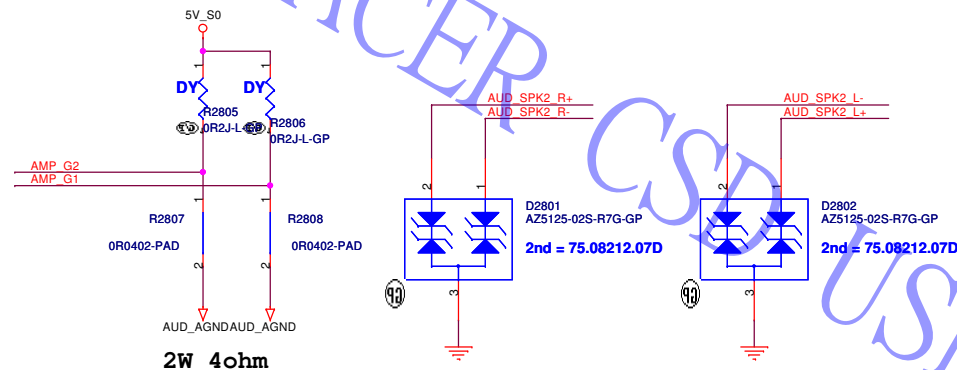
Reserve for input attenuation
to have optimized output power

Reserve for Input attenuation
To have optimization output power

Table 6. Amplifier Gain

G2	G1	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

*Condition is at 5V/40hm



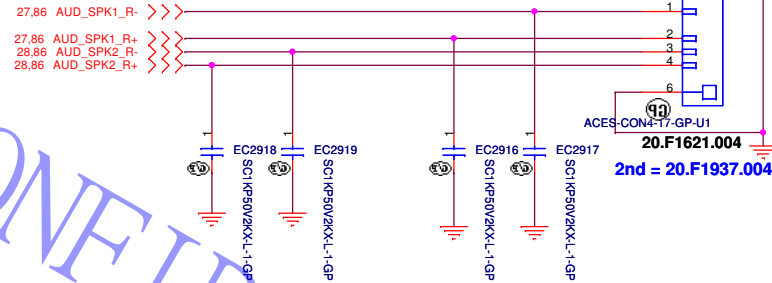
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EV

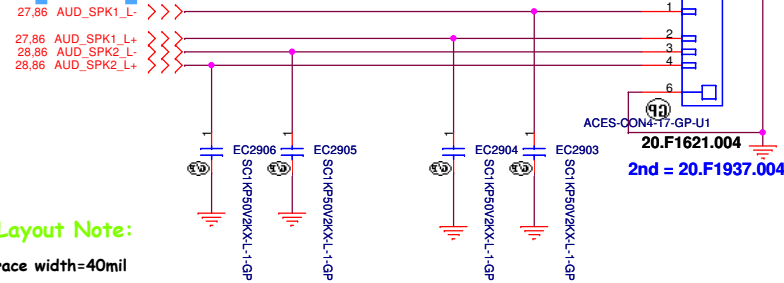
SSID = AUDIO

Speaker

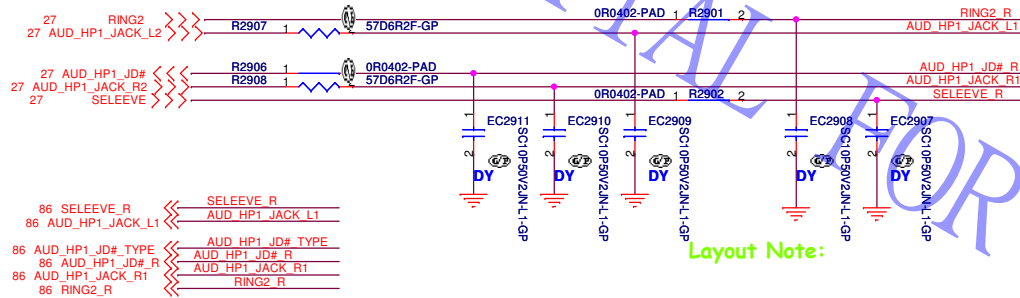
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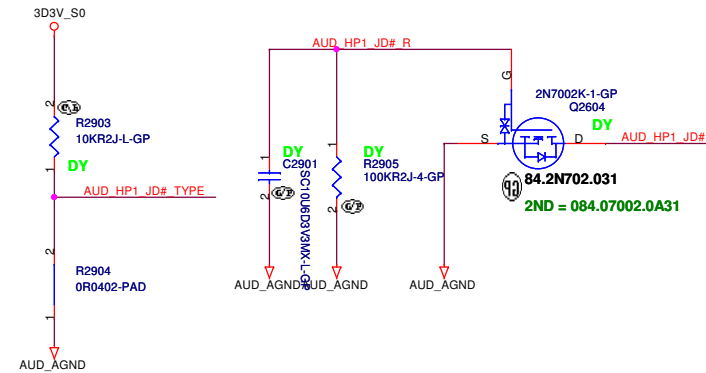
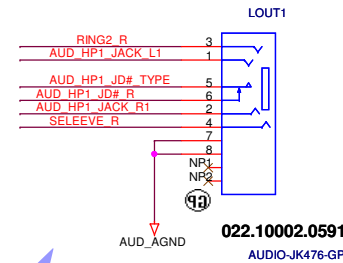
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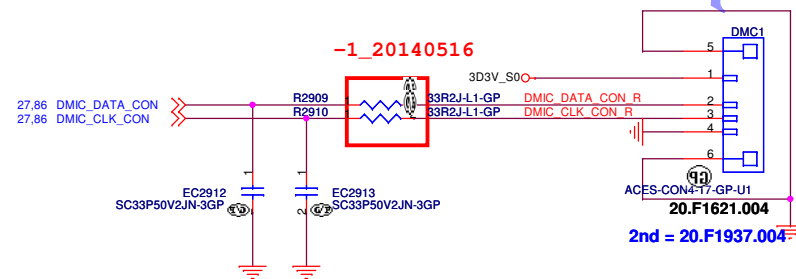
Combo Jack



Layout Note:

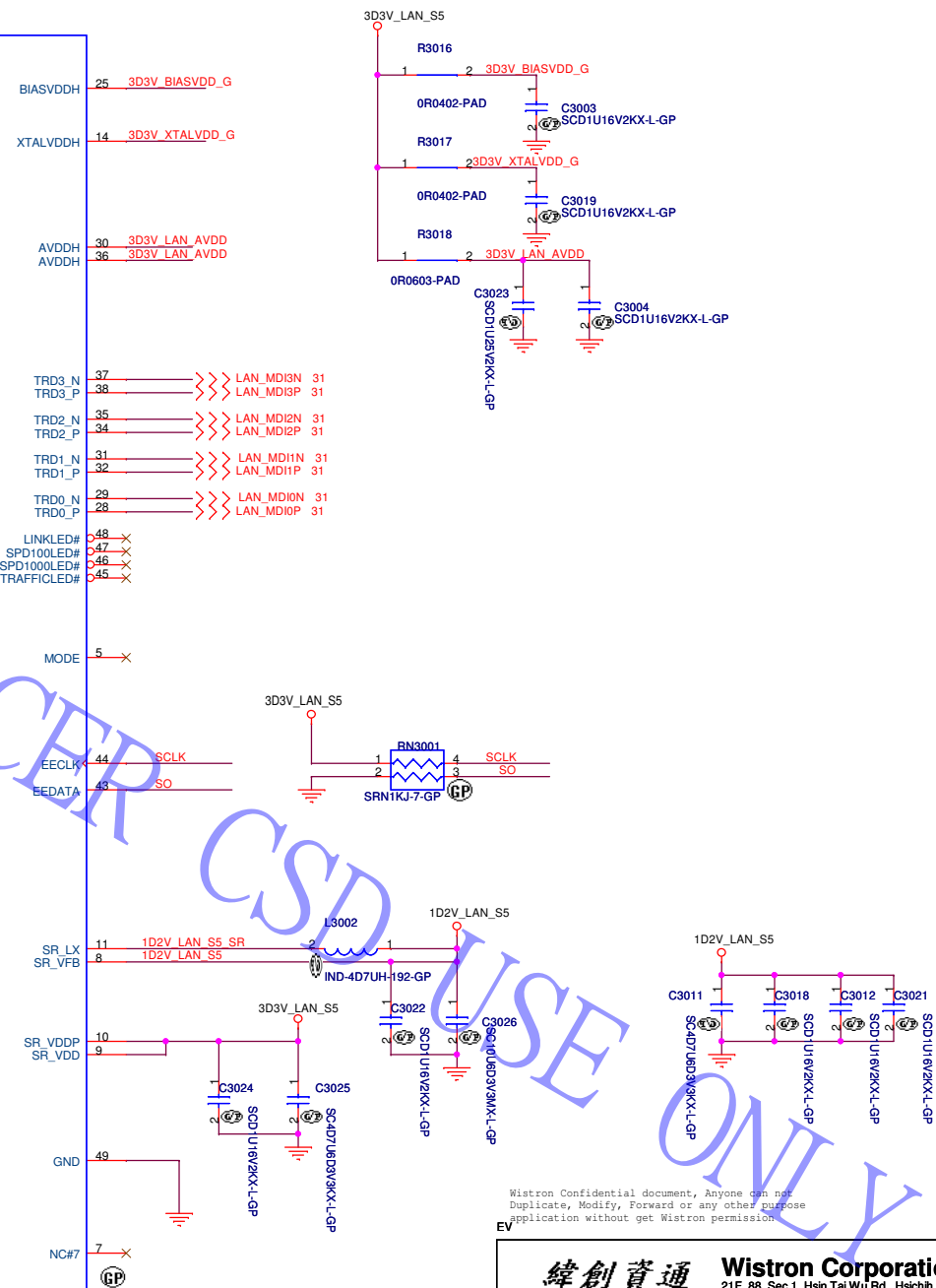


DMIC



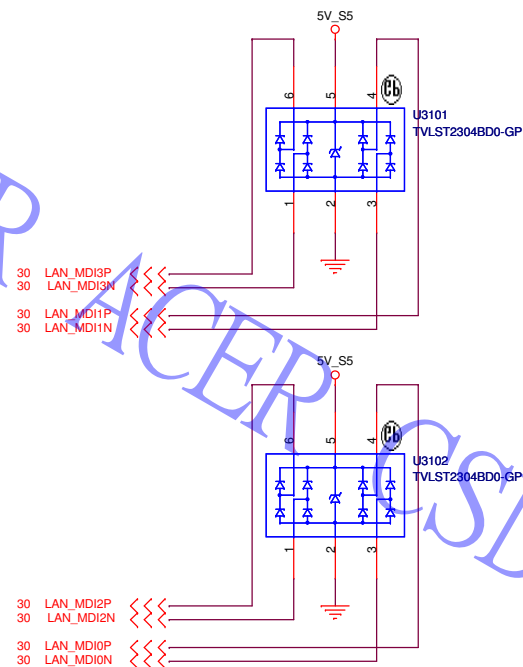
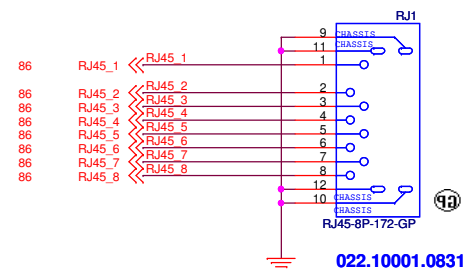
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<p>Title Audio Jack</p>	
Size Custom	Document Number Poseidon 860M
Date: Tuesday, June 17, 2014	Sheet 29 of 102
<p>Rev -1</p>	



Title			
LAN (BCM57780)			
Size A3	Document Number		Rev
	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014	Sheet 30 of	102

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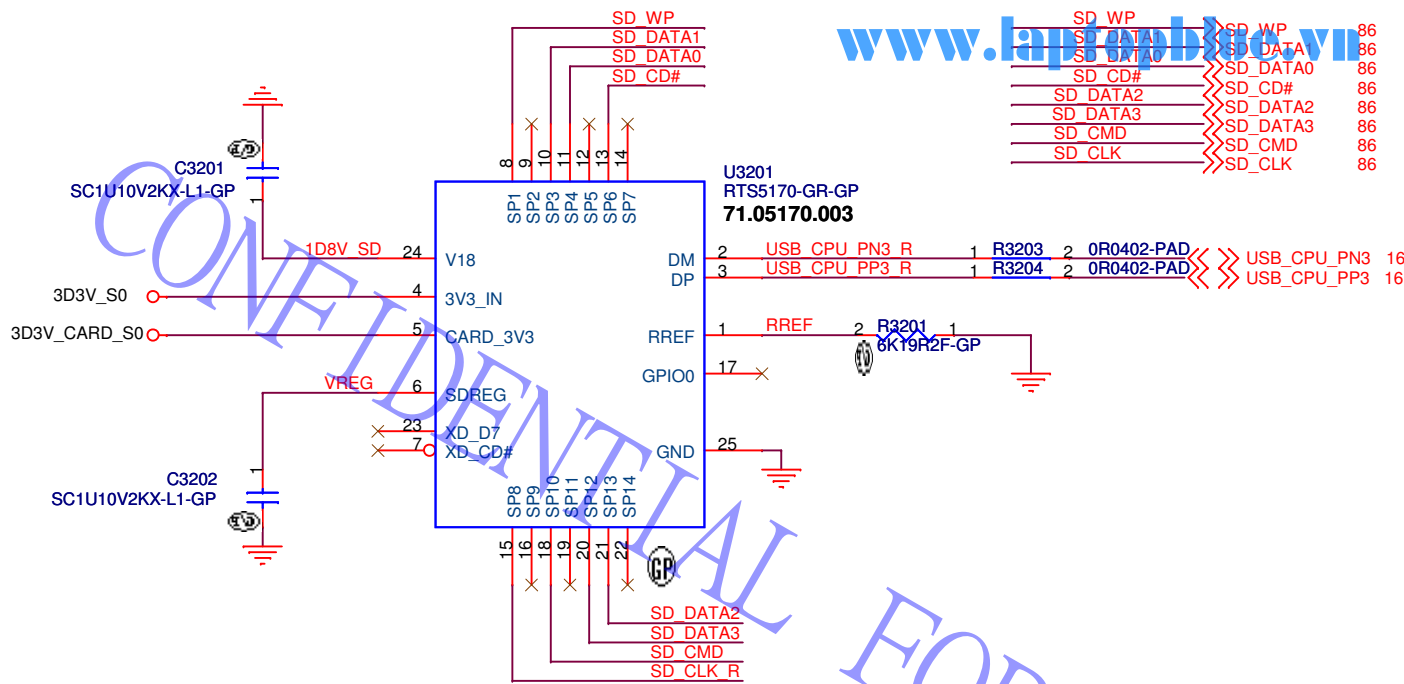
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(LAN+VGA) CONNECTOR

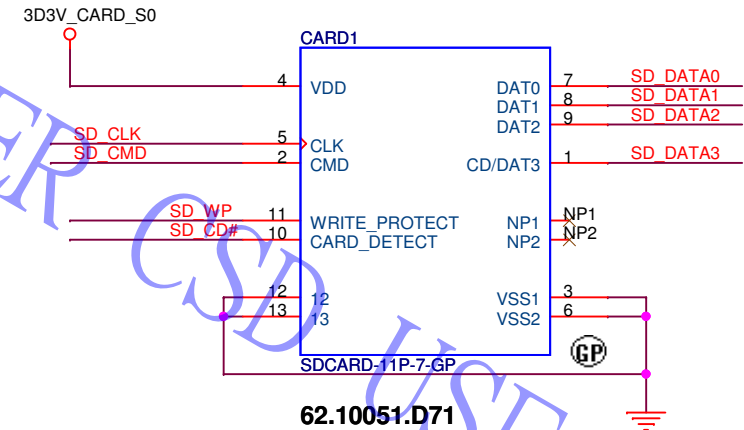
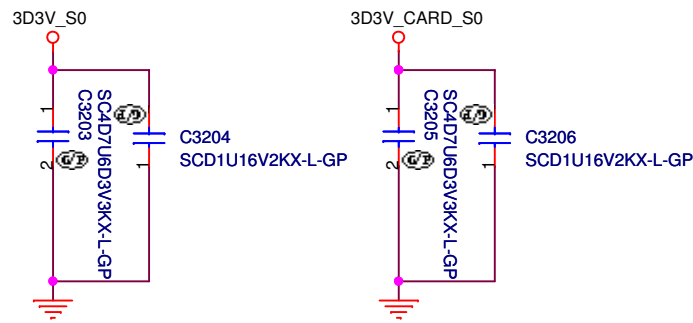
Rev

-1

Sheet 31 of 102



SP1	XD_CD#	SD_WP	MS_CLK
SP2	XD_RDY	SD_RE#	MS_INS#
SP3	XD_CE#	SD_D1	MS_D7
SP4	XD_CLE	SD_D0	MS_D3
SP5	XD_ALE	SD_D7	MS_D6
SP6	XD_WE#	SD_CD#	MS_D6
SP7	XD_WP	SD_D6	MS_D2
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	MS_D0
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6	SD_D2	MS_BS
	XD_D7		

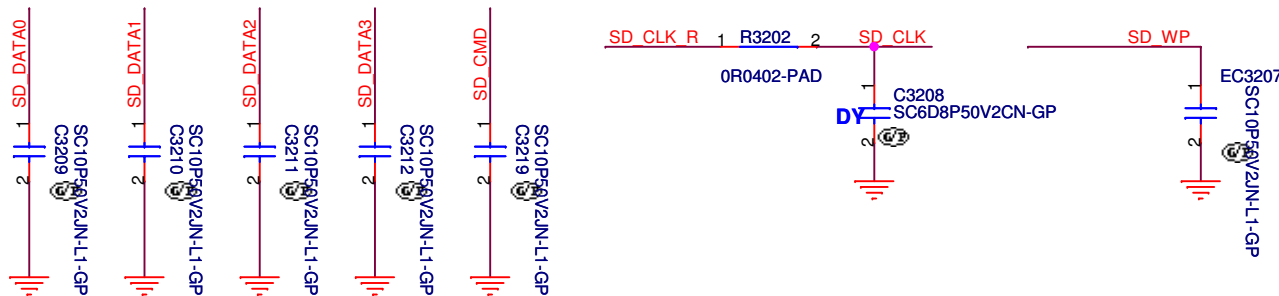


2nd = 62.10051.C41

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<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title: RTS5170 (CARD READER)</p>		
Size: A4	Document Number: Poseidon 860M	Rev: -1
Date: Tuesday, June 17, 2014	Sheet 32	of 102



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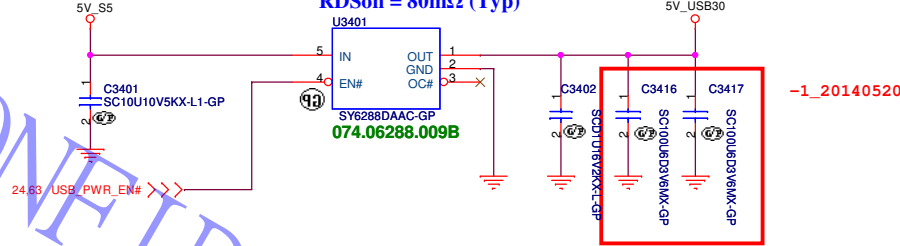
EV

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Card Reader CONN (Reserved)			
Size	Document Number		Rev
Custom	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014		Sheet 33 of 102

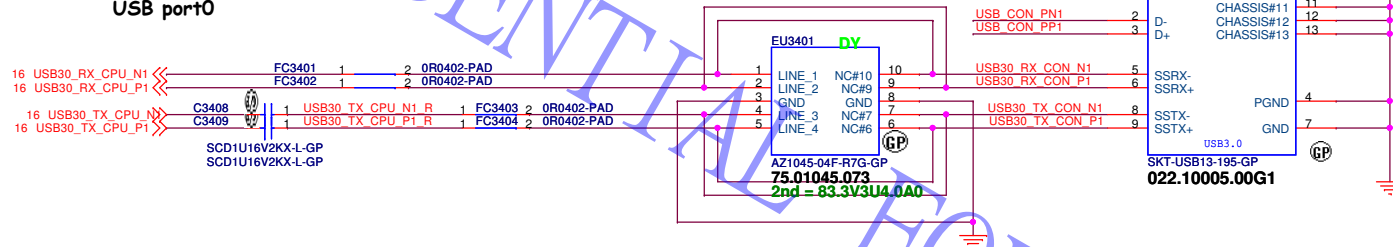
USB 3.0 Connector
Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

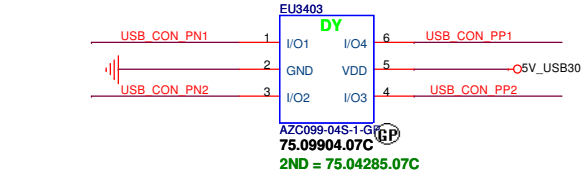
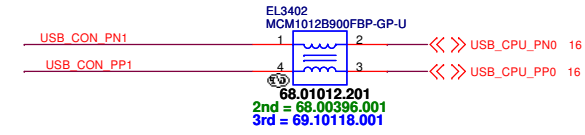
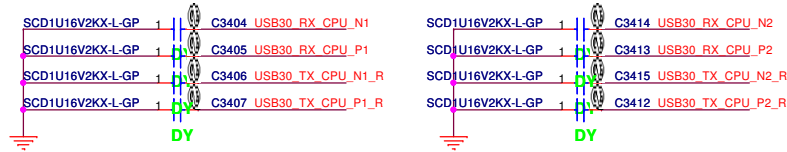
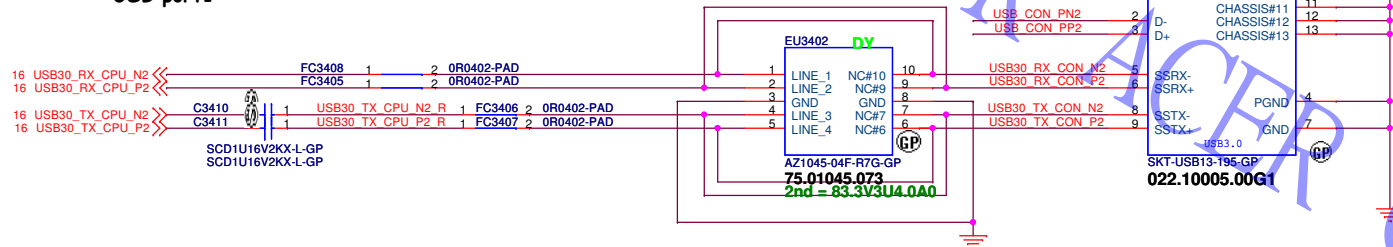
Low Active 2A
RDSon = 80mΩ (Typ)



USB port0



USB port1



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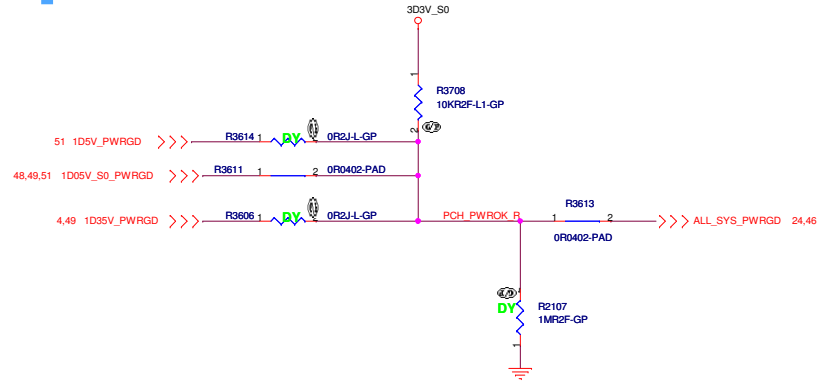
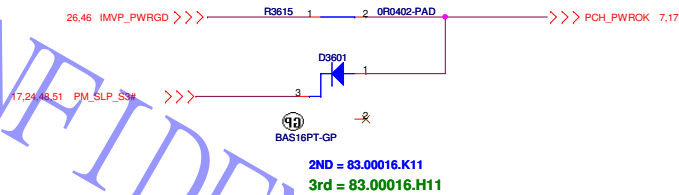
EV

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB CHARGER			
Size	Document Number		Rev
A4	Poseidon 860M		-1
Date: Tuesday, June 17, 2014		Sheet 35	of 102

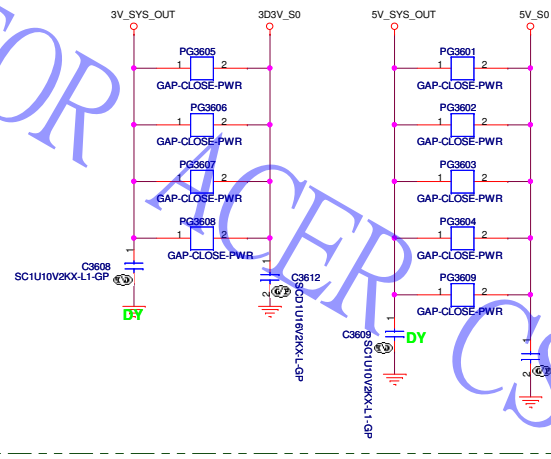
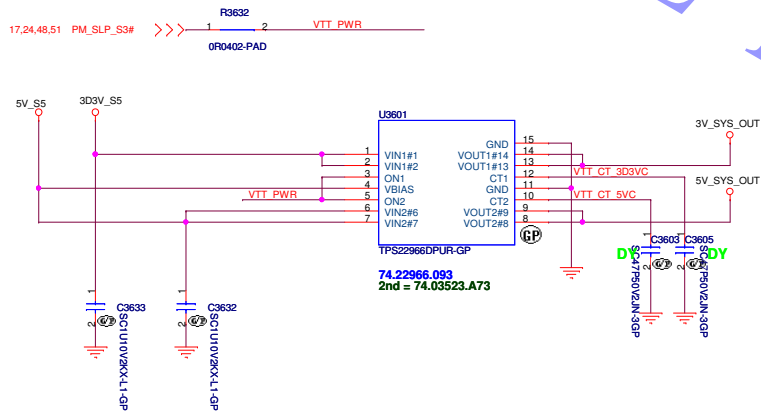
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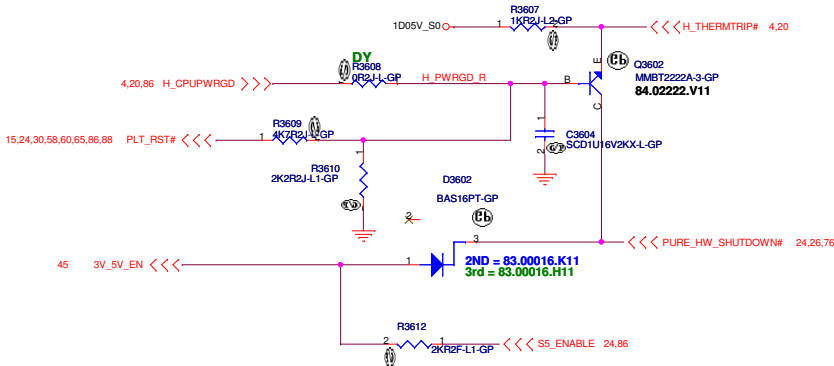
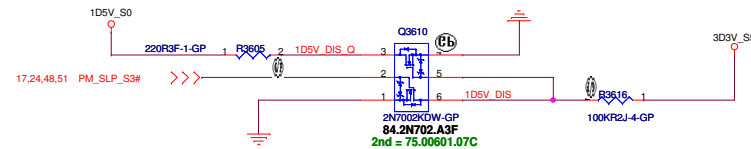
USE ONLY



ANNIE Run Power



Discharge circuit



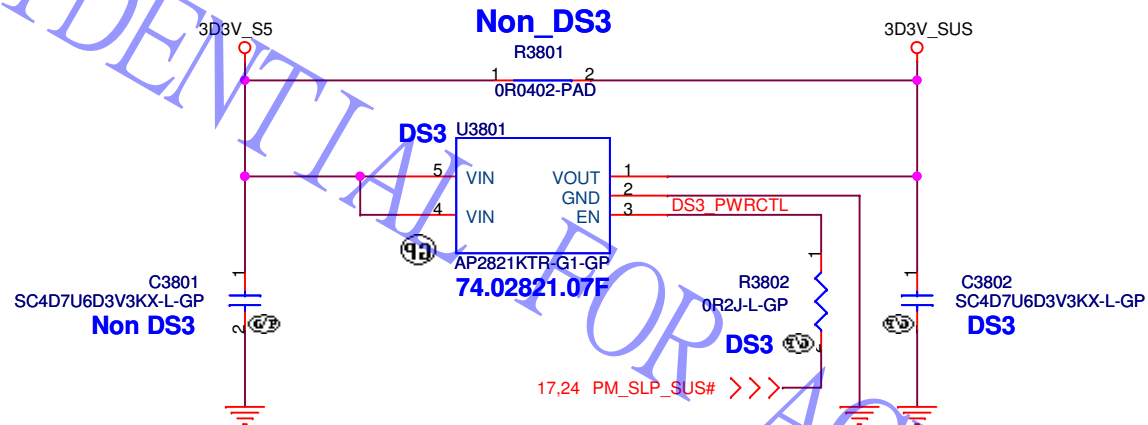
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Title			
ADAPTER OCP / S3 reduction			
Size	Document Number		Rev
Custom	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014	Sheet 37 of	102



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Title

DS3

Size
A4

Document Number

Poseidon 860M

Rev
-1

Date: Tuesday, June 17, 2014

Sheet 38 of 102

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Title

1D05 M

Size

A4

Document Number

Poseidon 860M

Rev

-1

Date: Tuesday, June 17, 2014

Sheet 39 of 102

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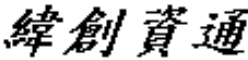
EV

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Connected Standby1			
Size	Document Number		Rev
A	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014		Sheet 40 of 102

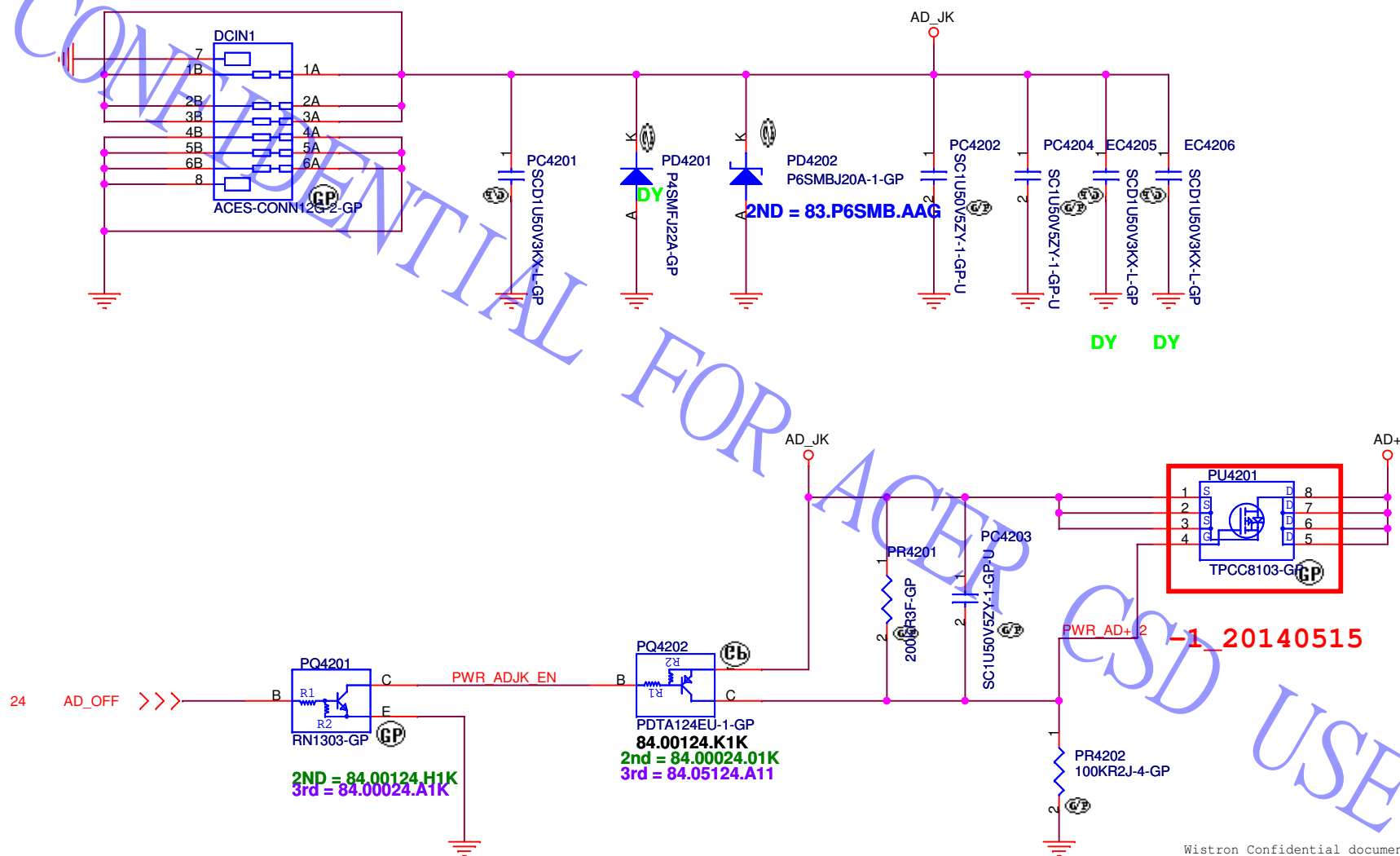
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Connected Standby2			
Size A	Document Number		Rev
	Poseidon 860M		-1
Date: Tuesday, June 17, 2014	Sheet	41	of 102

Adaptor in to generate DCBATOUT



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Taipei Hsien 221, Taiwan, R.O.C.

Title

DCIN JACK

Size
A4

Document Number

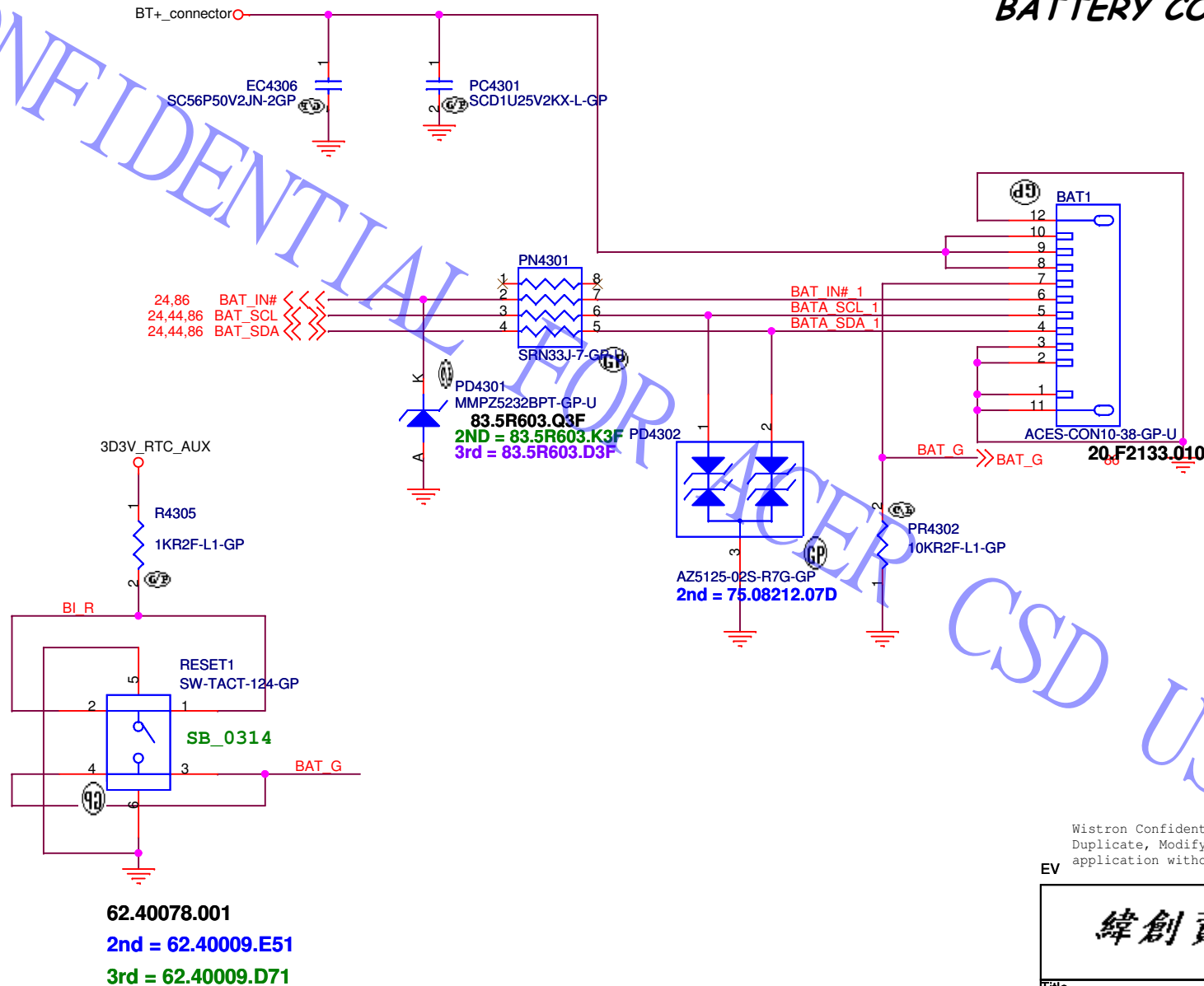
Poseidon_860M

Rev
-1

Date: Tuesday, June 17, 2014

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BATTERY CONNECTOR



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Title

BATT CONN

Size
A4

Document Number

Poseidon 860M

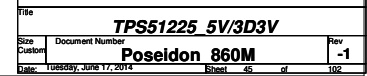
Rev

-1

Date: Tuesday, June 17, 2014

Sheet 43 of 102





SSID = CPU.Regulator

www.laptopblue.vn

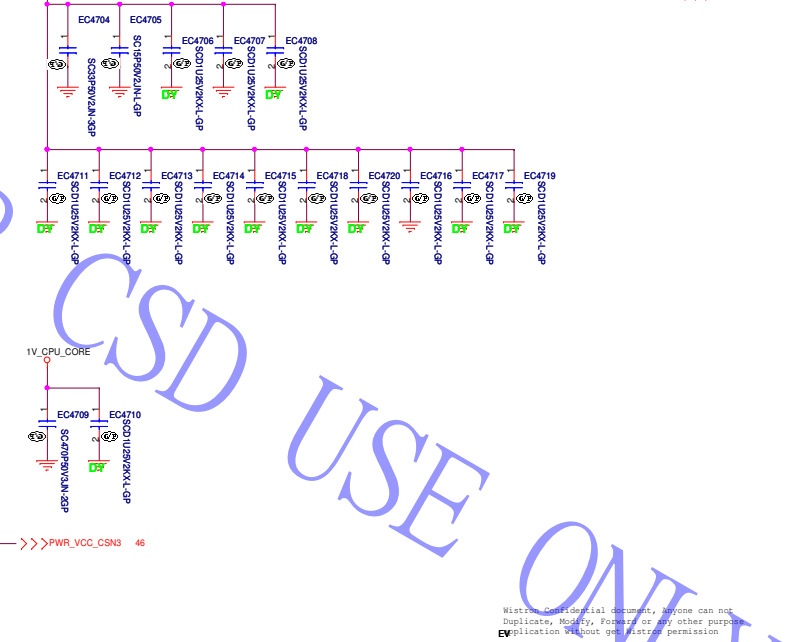
-1_20140515

074.51633.0073 for BDW CPU

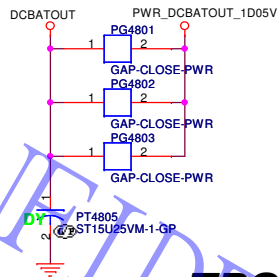
2nd = 74.51631.073

-1_20140515

	47W
PC4602	4.7nF
	78.47224.2FL
PR4611	95.3k
	64.95325.6DL
PR4614	150k
	64.15035.6DL
PR4617	75k
	63.75334.1DL
PR4615	36.5k
	64.36525.6DL
PR4618	20k
	64.20025.6DL
PR4626	DY
PR4630	DY
PR4602	6.98k
	64.69815.6DL
PR4607	2.87k
	64.28715.6DL



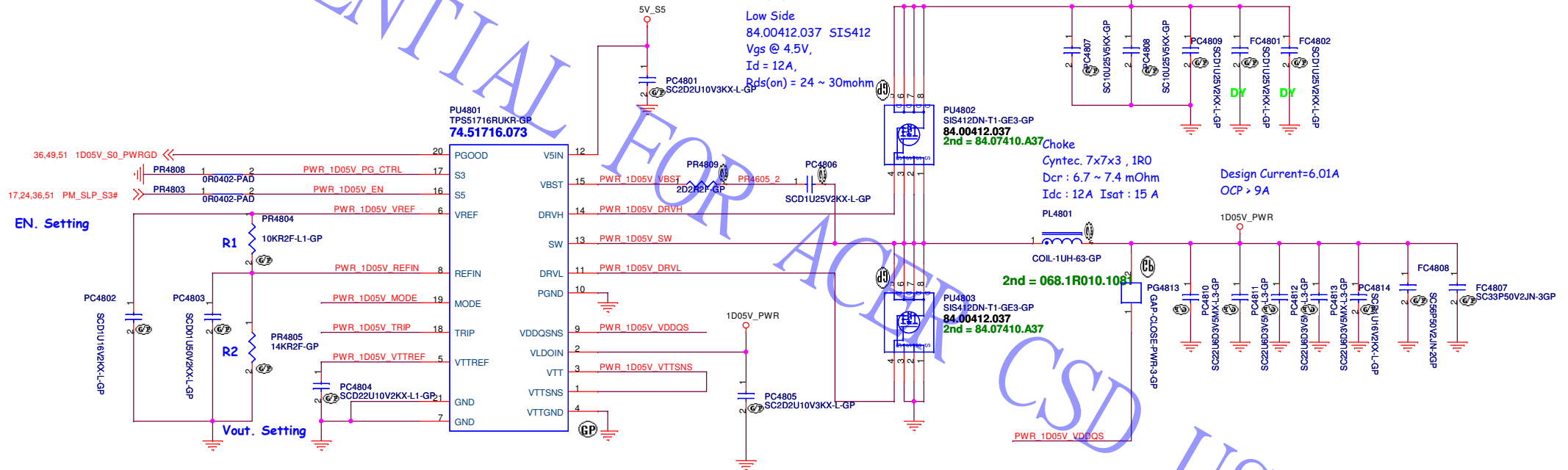
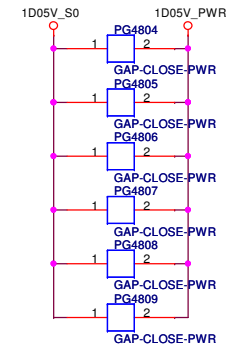
Title			
TPS51361 CPUCORE(2/2)			
Size Custom	Document Number		Rev
	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014	Sheet 47 of	102



TPS51716 for 1D05V

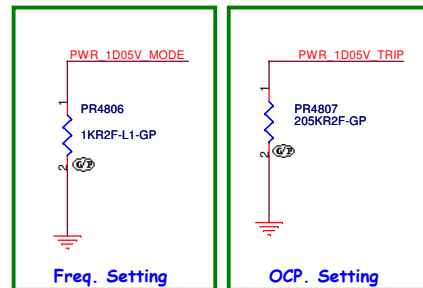
High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm



MODE		
PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	
1k ohm	500kHz	Tracking Discharge

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



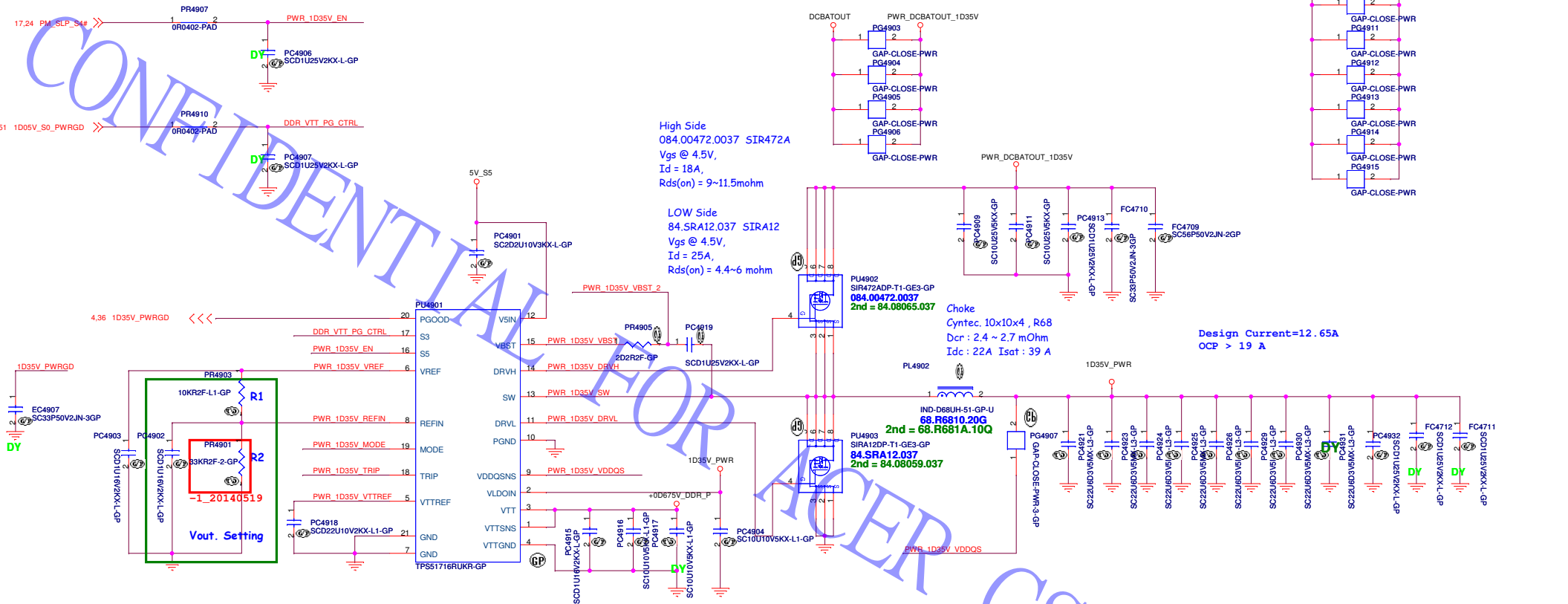
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Title			
DC to DC 1D05V(TPS51716)			
Size A3	Document Number		Rev
	Poseidon 860M		-1
Date:	Wednesday, June 18, 2014	Sheet 48 of	102

SSID = PWR.Plane.Regulator 1p35v0p675v



High Side
084.00472.0037 SIR472A
Vgs @ 4.5V,
Id = 18A,
Rds(on) = 9~11.5mohm

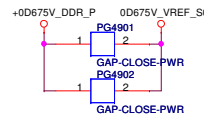
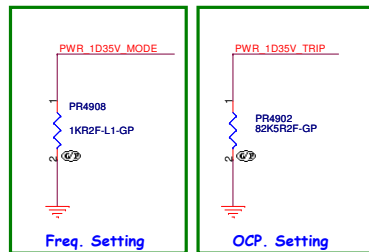
LOW Side
84.SRA12.037 SIRA12
Vgs @ 4.5V,
Id = 25A,
Rds(on) = 4.4~6 mohm

Choke
Cyntec. 10x10x4, R68
Dcr : 2.4 ~ 2.7 mOhm
Idc : 22A Isat : 39 A

Design Current=12.65A
OCP > 19 A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

PR4908	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	



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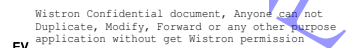
Title		
TPS51716 (VDDQ VTT)		
Size	Document Number	Rev
Custom	Poseidon 860M	-1
Date: Wednesday, June 18, 2014	Sheet 49 of 102	

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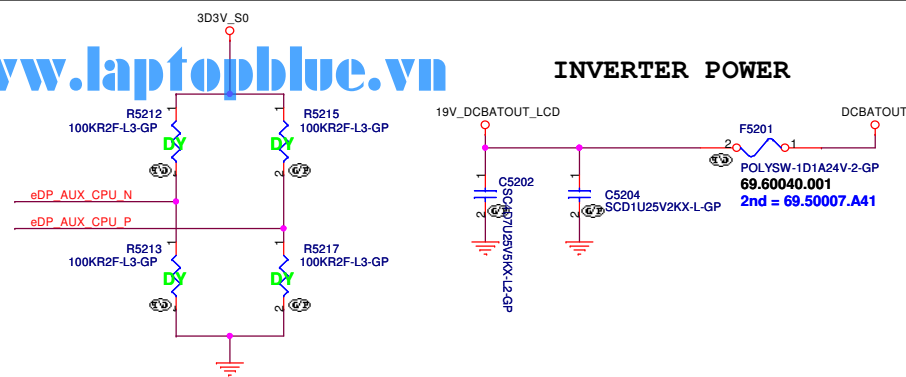
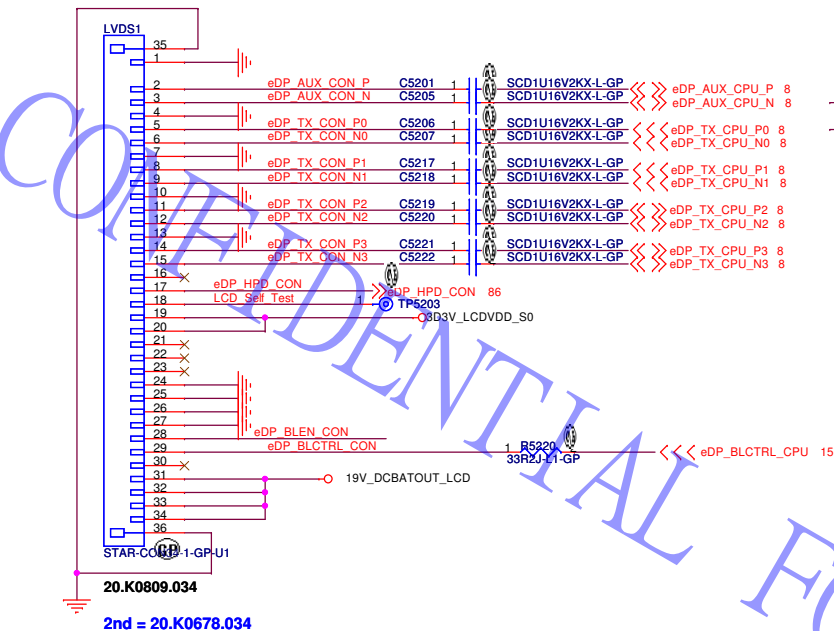
EV

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Title			
1D8V_S0_TLV62065			
Size	Document Number		Rev
A4	Poseidon_860M		-1
Date: Tuesday, June 17, 2014		Sheet 50 of	102

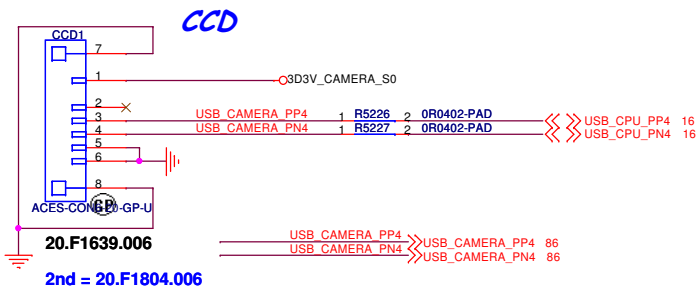
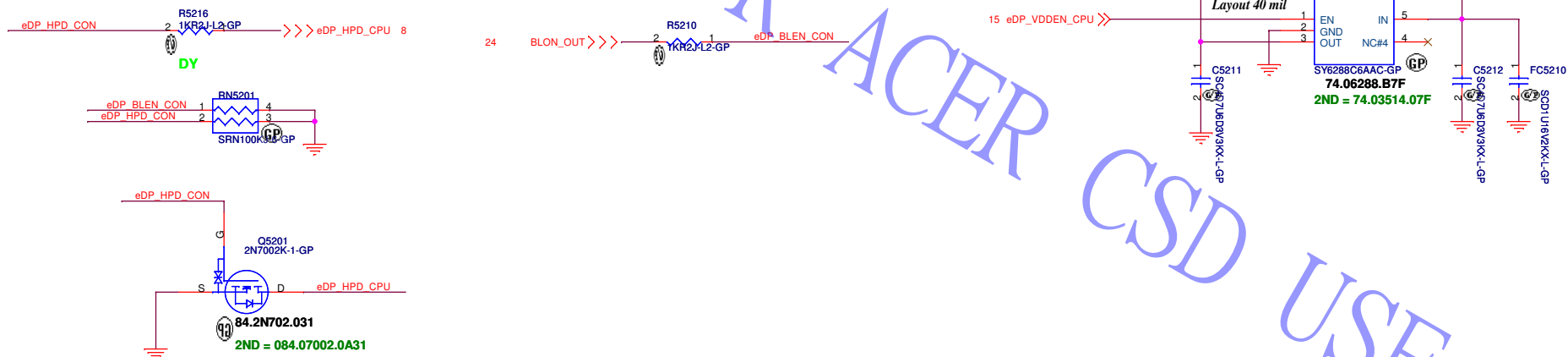
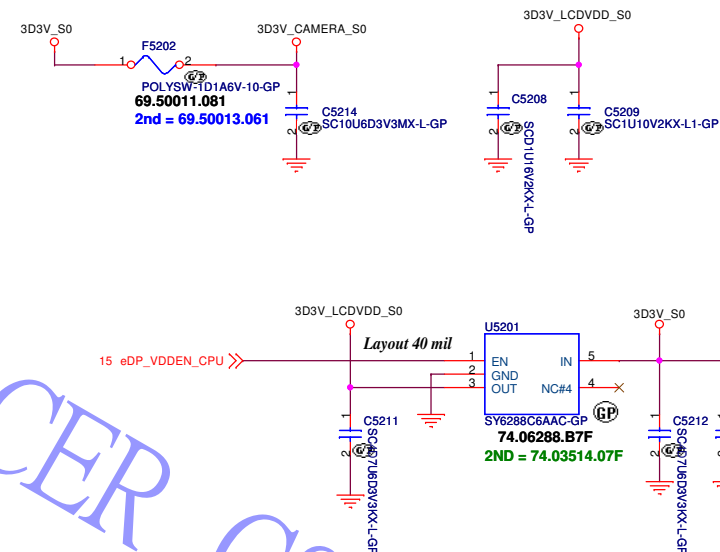


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Taipei Hsien 221, Taiwan, R.O.C.

Title			
1D5V_S0_TLV70215			
Size A3	Document Number		Rev
	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014	Sheet 51 of	102



Camera Power



eDP_AUX_CON_P >>> eDP_AUX_CON_P 86
eDP_AUX_CON_N >>> eDP_AUX_CON_N 86
eDP_TX_CON_P0 >>> eDP_TX_CON_P0 86
eDP_TX_CON_N0 >>> eDP_TX_CON_N0 86
eDP_TX_CON_P1 >>> eDP_TX_CON_P1 86
eDP_TX_CON_N1 >>> eDP_TX_CON_N1 86
eDP_TX_CON_P2 >>> eDP_TX_CON_P2 86
eDP_TX_CON_N2 >>> eDP_TX_CON_N2 86
eDP_TX_CON_P3 >>> eDP_TX_CON_P3 86
eDP_TX_CON_N3 >>> eDP_TX_CON_N3 86
eDP_HPDCON >>> eDP_HPDCON 86
eDP_BLENCON >>> eDP_BLENCON 86
eDP_BLCCTRL_CON >>> eDP_BLCCTRL_CON 86

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緯創資通 Wistron Corporation		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LCD Connector			
Size A3	Document Number	Rev -1	
Date: Tuesday, June 17, 2014	Sheet 52	of 102	

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Title			
CRT Board Connector (Reserved)			
Size	Document Number		Rev
A3	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014	Sheet	53 of 102

HDMI Level Shifter & CONNECTOR www.toptophblue.vn

HDMI1

22
20
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
21
23

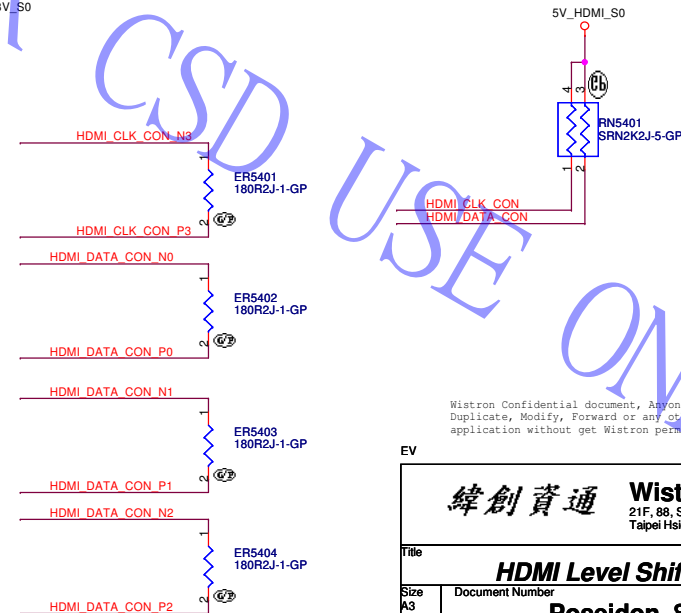
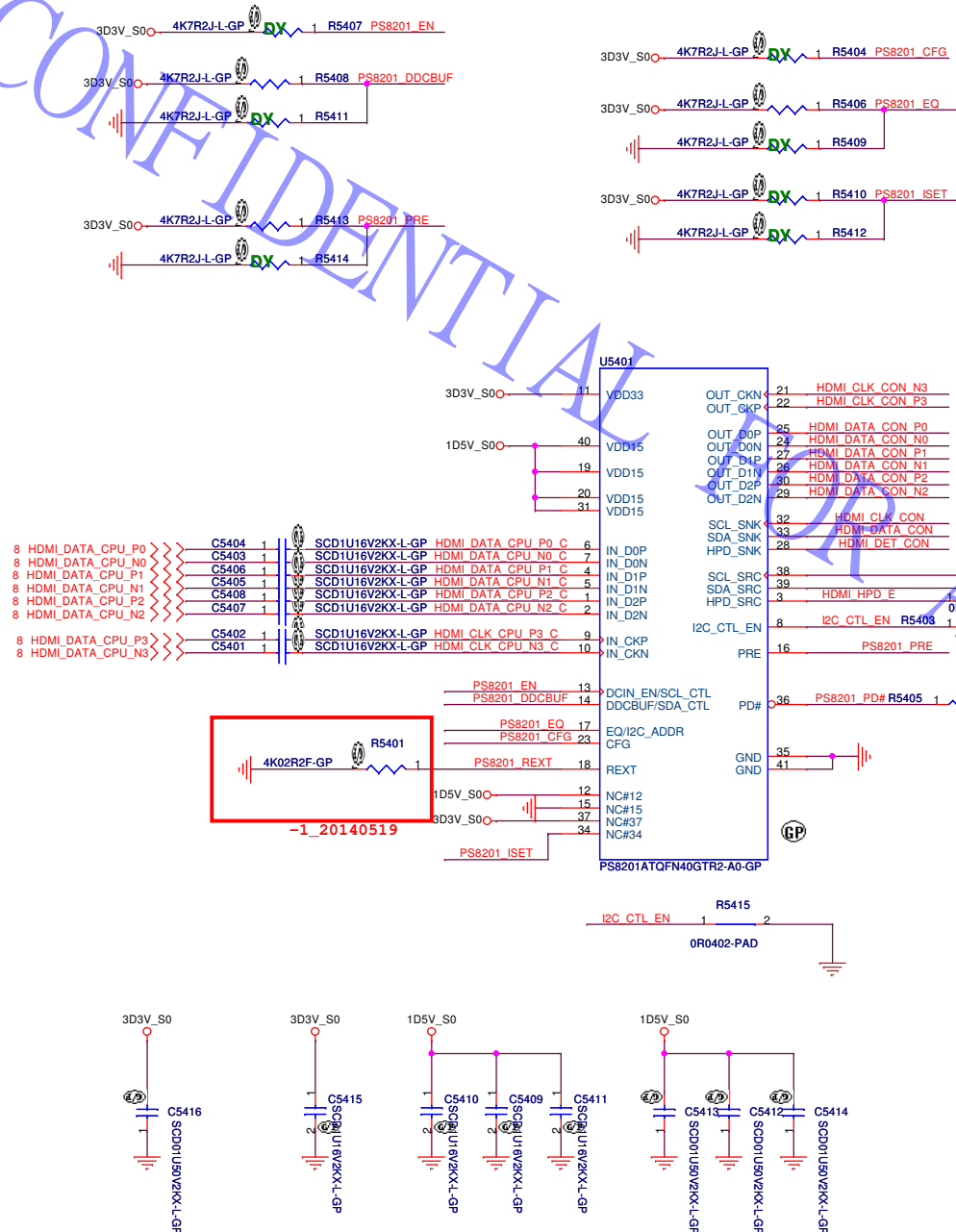
HDMI DATA CON P2
HDMI DATA CON N2
HDMI DATA CON P1
HDMI DATA CON N1
HDMI DATA CON P0
HDMI DATA CON N0
HDMI CLK CON P3
HDMI CLK CON N3
HDMI CLK CON
HDMI DATA CON
5V HDMI S0
HDMI DET CON

5V_HDMI_S0
F5401
POLYSW-TD1A6V-10-GP
69.50011.081
2nd = 69.50013.061

C5417
SC10U10V5KX-L1-GP

SKT-HDMI21-2-GP-1T

22.10296.661
2nd = 22.10296.A71



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Title			
HDMI Level Shifter/Connector			
Size A3	Document Number		Rev
	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014	Sheet 54 of	102

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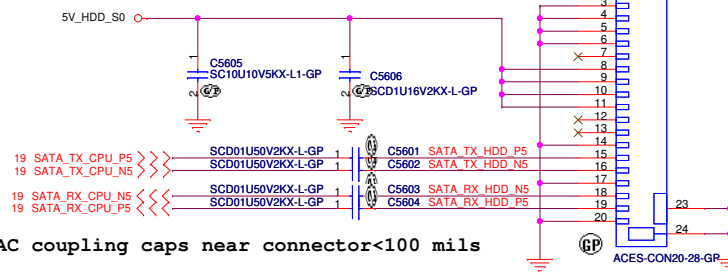
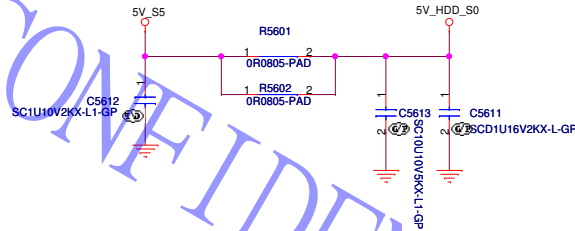
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Display Port			
Size	Document Number		Rev
A3	Poseidon 860M		-1
Date: Tuesday, June 17, 2014		Sheet 55	of 102

SSID = SATA

SATA HDD Connector

SB_0327



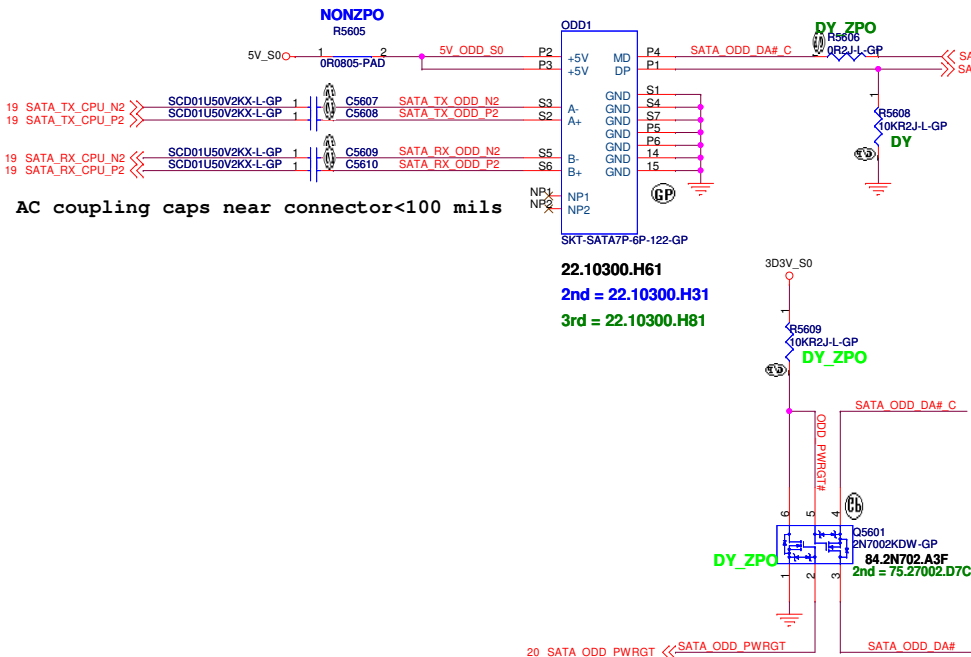
AC coupling caps near connector<100 mils

20.F2036.020

2nd = 20.F2480.020

3rd = 20.F2030.020

ODD Connector



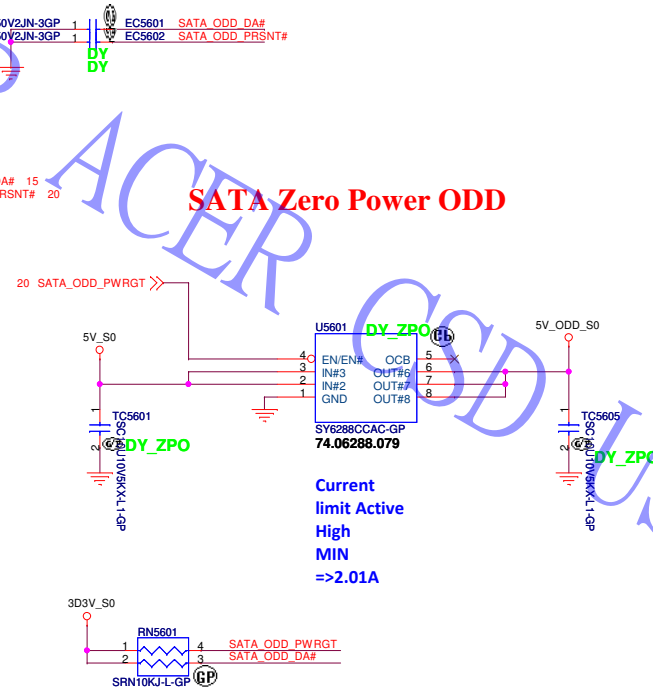
AC coupling caps near connector<100 mils

22.10300.H61

2nd = 22.10300.H31

3rd = 22.10300.H81

SATA Zero Power ODD



Current
limit Active
High
MIN
=>2.01A

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EV		application without get Wistron permission	
			
Title			
HDD / ODD / NGFF SSD			
Size	Document Number	Rev	
Custom	Poseidon 860M	-1	
Date:	Tuesday, June 17, 2014	Sheet	56 of 102

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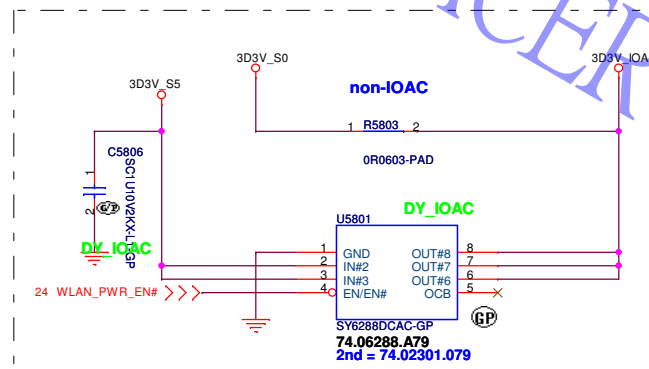
EV

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Title			
E-SATA			
Size	Document Number		Rev
A4	Poseidon 860M		-1
Date: Tuesday, June 17, 2014		Sheet 57	of 102

SSID = Wireless *Mini Card Connector(802.11a/b/g/n)*

Mini Card Connector(802.11a/b/g/n)

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F

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Taipei Hsien 221, Taiwan, R.O.C.

MINICARD(WLAN)

Rev

1

102

102

SSID = Wireless

Mini Card Connector(mSATA)

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Title

WWAN CONN

Size
A4

Document Number
Poseidon 860M

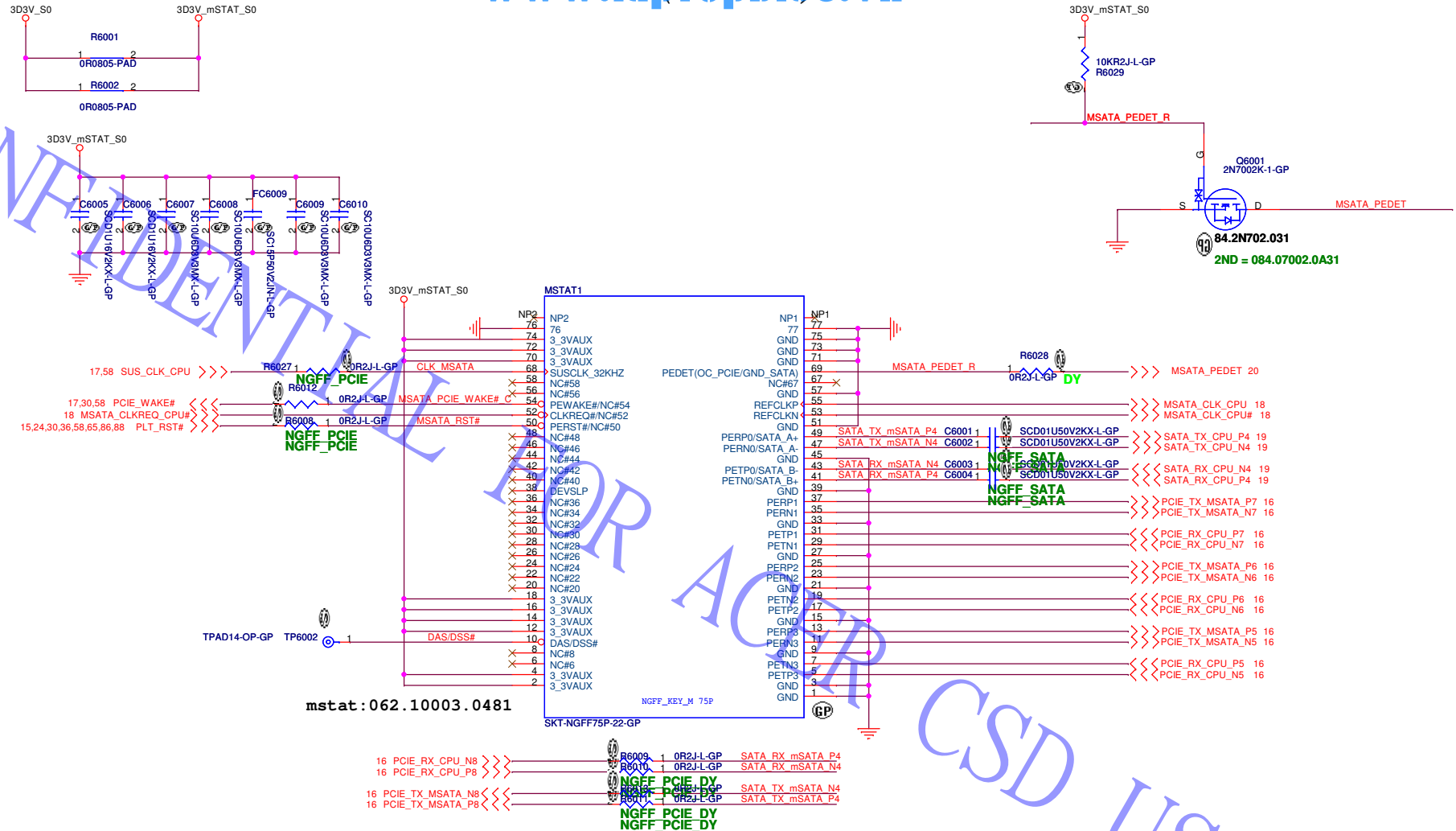
Date: Tuesday, June 17, 2014

Rev
-1

Sheet 59 of 102

SSID = mSATA

Mini Card Connector(mSATA)



SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF ²	None ³

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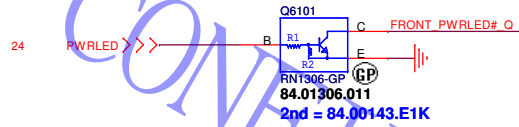
EV

緯創資通		Wistron Corporation	
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Title			
mSATA Connector			
Size A3	Document Number	Rev	
	Poseidon 860M	-1	
Date: Tuesday, June 17, 2014	Sheet 60	of 102	

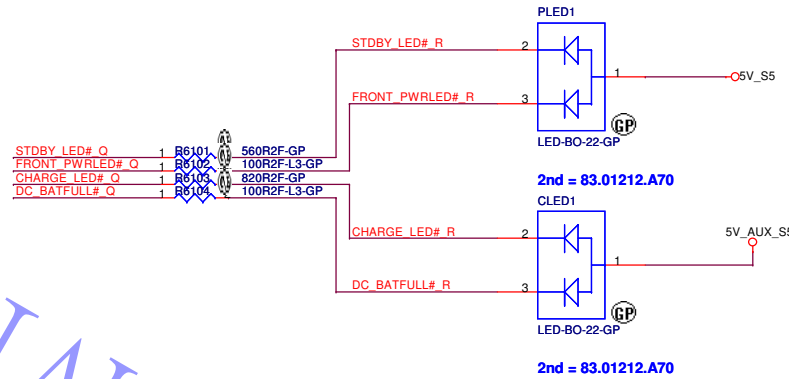
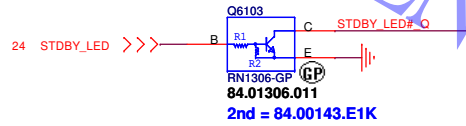
SSID = User.Interface

www.laptopblue.vn

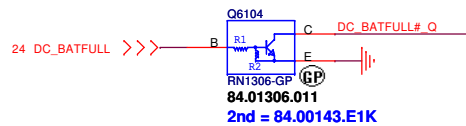
Power button LED



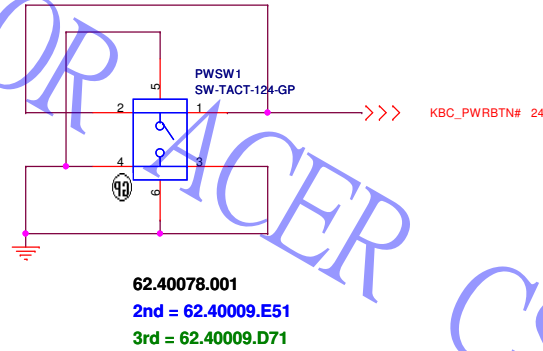
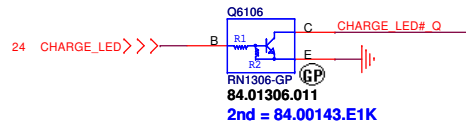
Power STDBY_LED



Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)



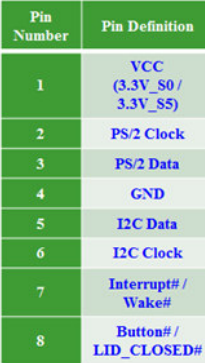
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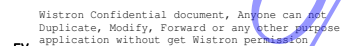
Title		
LED Bard/Power Button		
Size A3	Document Number	Rev
	Poseidon 860M	-1
Date: Tuesday, June 17, 2014	Sheet 61	of 102

The image shows two circuit diagrams. The left diagram shows a 3D3V_TP_S3 component connected to a 3D3V_TP_S3 component. The right diagram shows a 3D3V_TP_S3 component connected to a 3D3V_TP_S3 component.



MB PIN DEFINE	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
KB PIN DEFINE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26

26 K/B 1

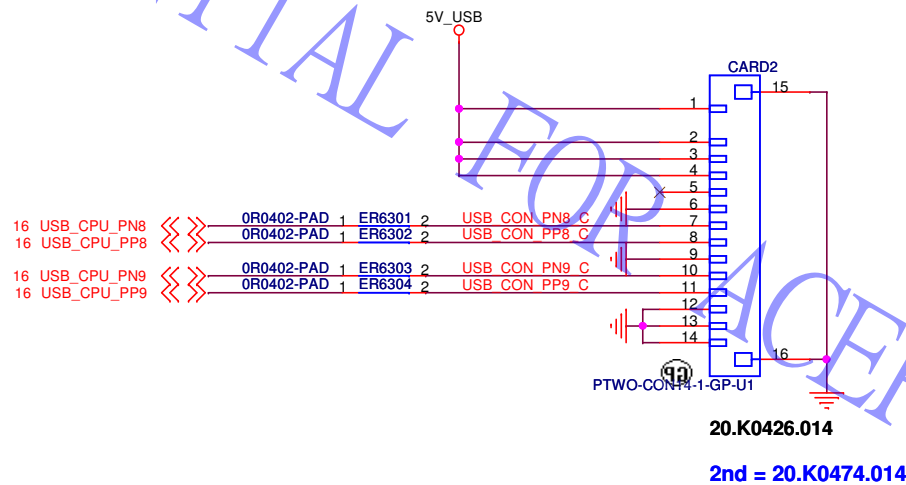
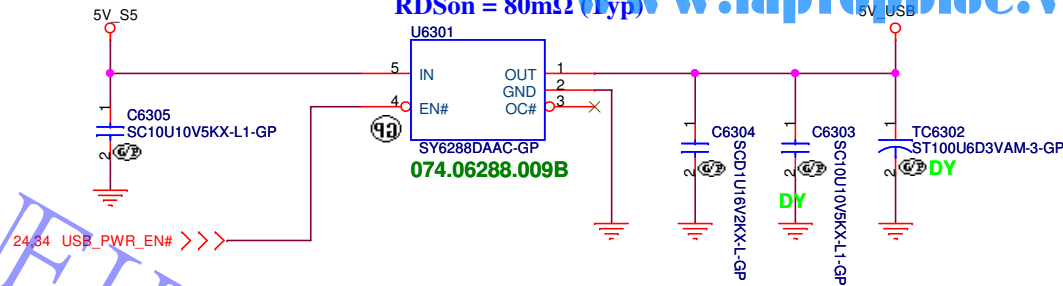


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Title			
Key Board/Touch Pad			
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Low Active 2A
RDSon = 80mΩ (Typ)



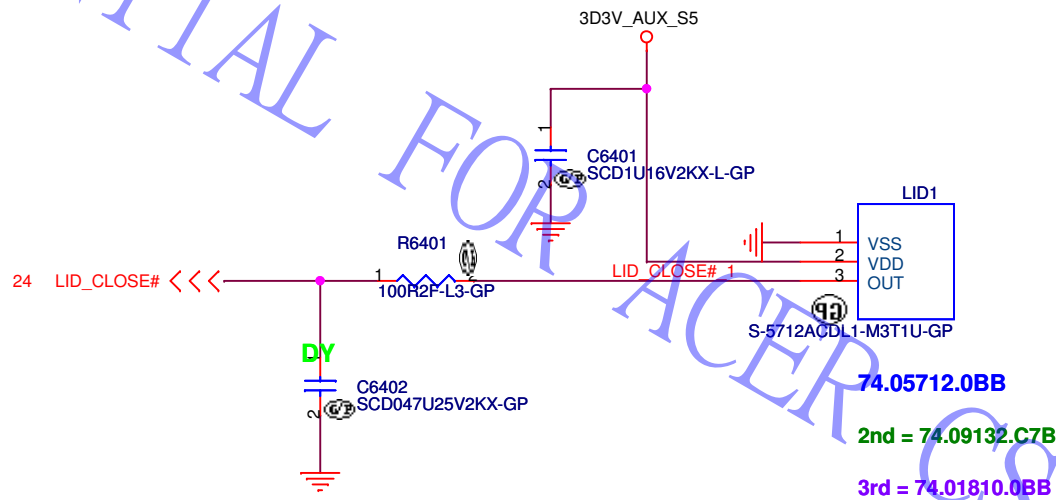
86 USB_CON_PN8_C <<< USB_CON_PN8_C
86 USB_CON_PP8_C <<< USB_CON_PP8_C
86 USB_CON_PN9_C <<< USB_CON_PN9_C
86 USB_CON_PP9_C <<< USB_CON_PP9_C

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Title

Hall Sensor

Size
A4

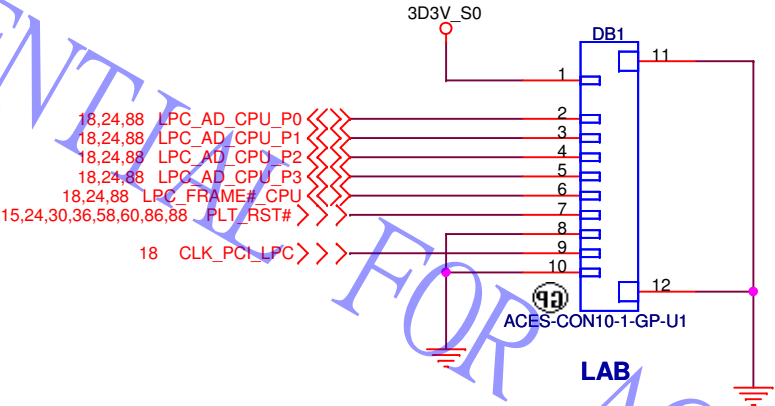
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Dubug connector			
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G Sensor		
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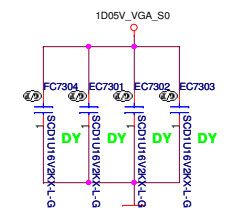
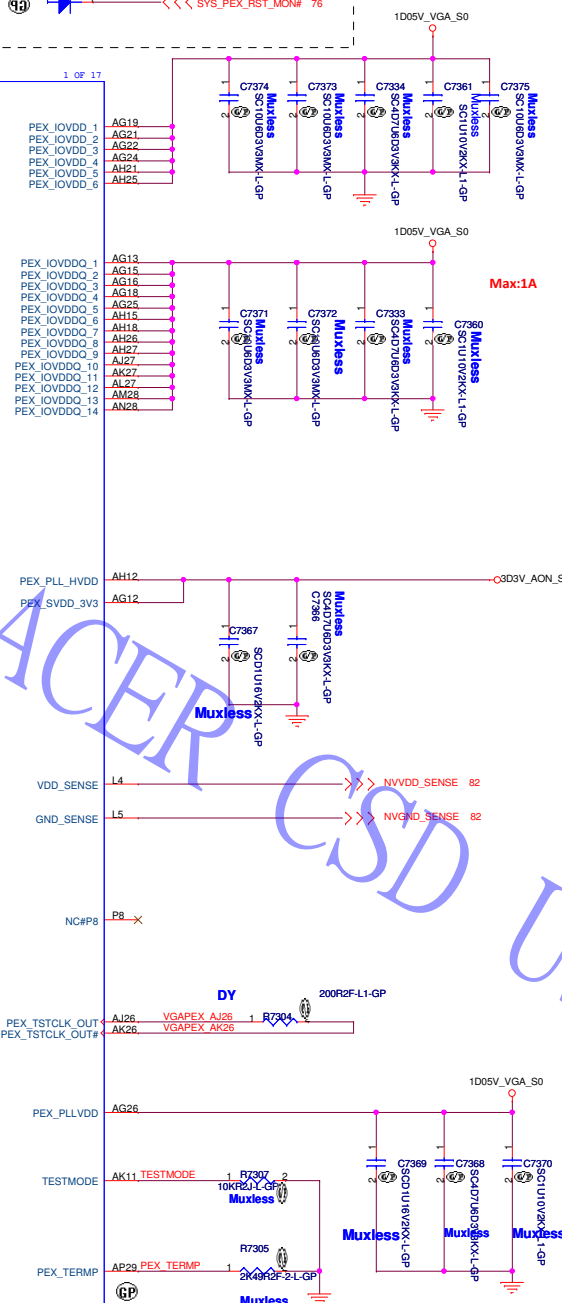
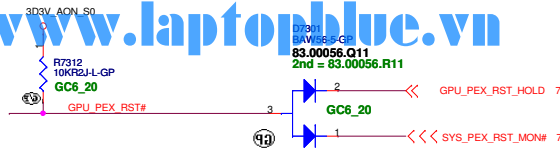
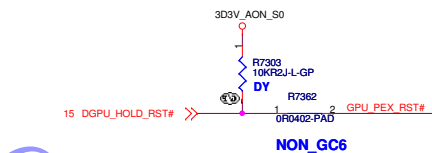
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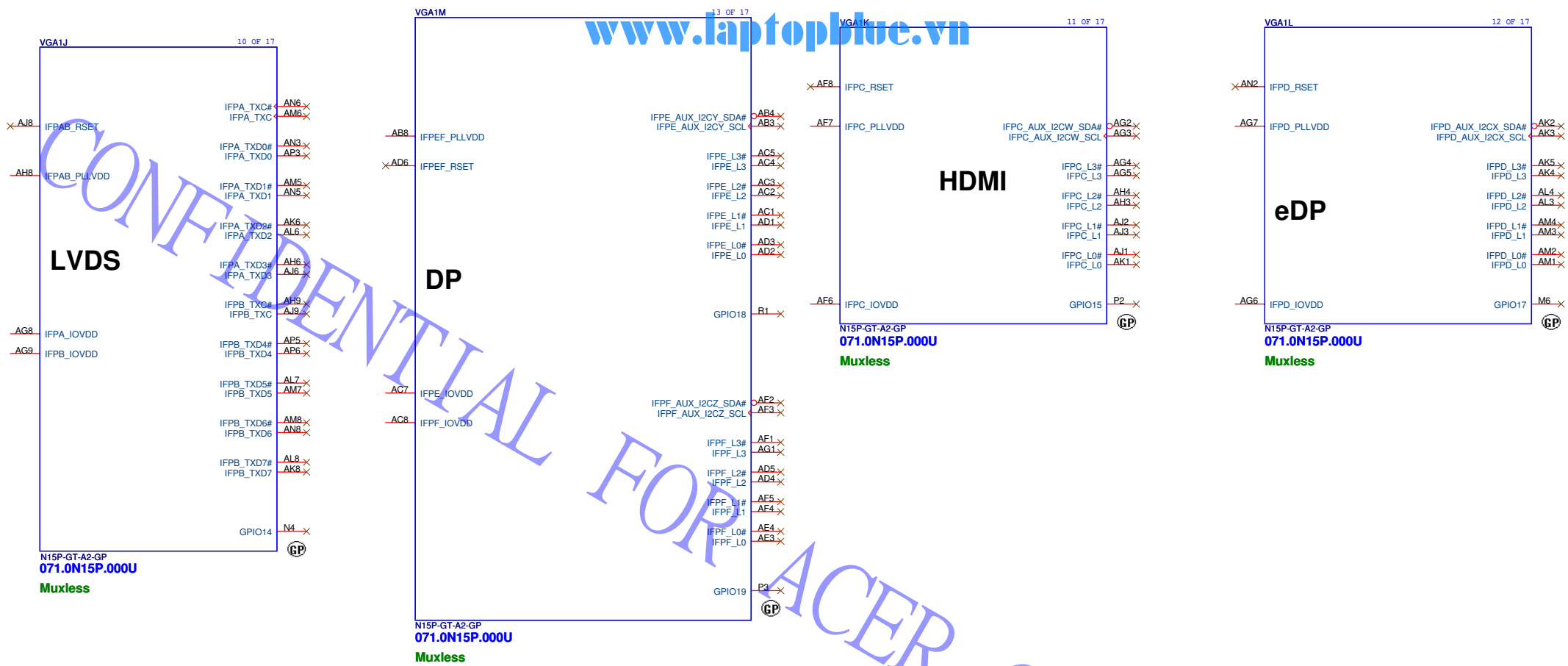
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071.0N15P.000U
Muxless



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Title GPU (DIGITALOUT)		
Size A3	Document Number Poseidon 860M	Rev -1
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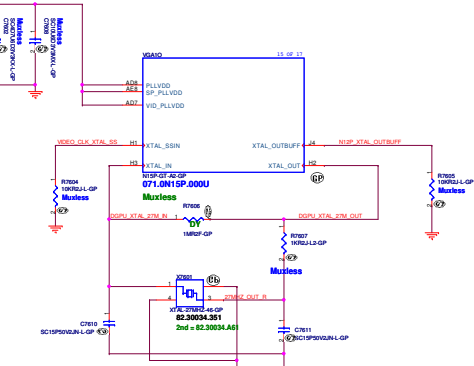
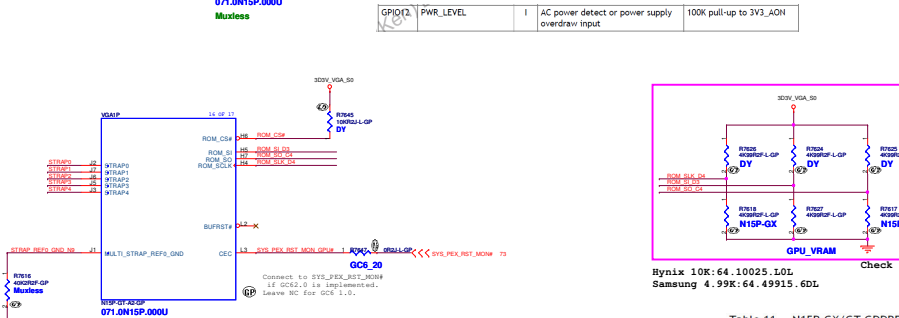
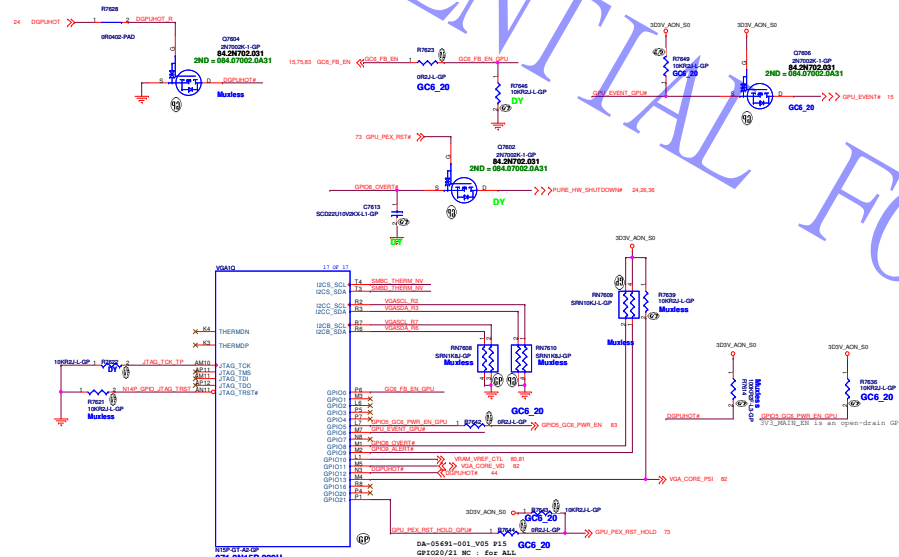
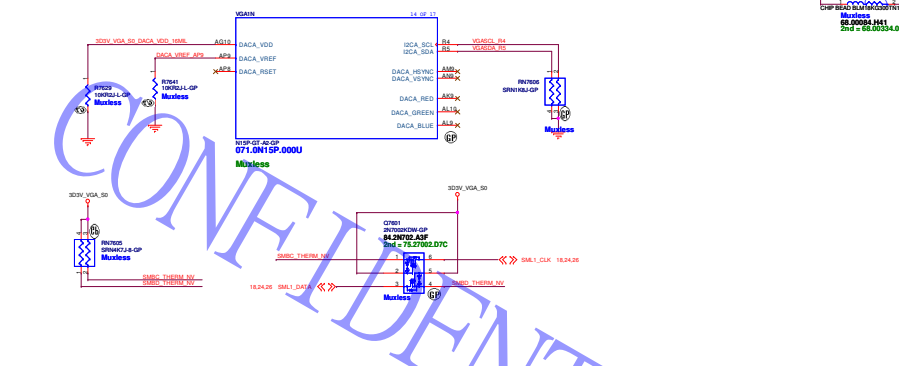


Table 2. Memory Configurations for Testing

Products	Type	VRAM Voltage	Vendor	Qty Parts	Memory Bus Width	Density	Speed Bin (MHz)	Part Number
H155-GX	DDR3	1.5V	Hynix	8	128 bits	256MX16	1000	H5TC4G63AFR-11C
H15P-GT	DDR3	1.5V	Hynix	8	128 bits	256MX16	1000	H5TC4G63AFR-11C
	GDDR5	1.35V	Hynix	8	128 bits	256MX16	2500	H5GC4H24MFR-T2C
H15P-GX	GDDR5	1.35V	Hynix	8	128 bits	256MX16	2500	H5GC4H24MFR-T2C

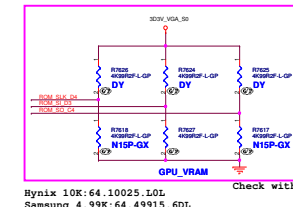
Table 15-3. G828-64 and G848-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bin 3	Logical Strapping Bin 2	Logical Strapping Bin 1	Logical Strapping Bin 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PEEK_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_A0H and pull-down to GND and stuff 50K pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_A0H and pull-down to GND for forward compatibility.			
STRAP2				
STRAP3				
STRAP4				

Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

4.99Kohm 64.49915.6DL
10Kohm 64.10025.10L
15Kohm 64.15025.6DL
20Kohm 64.20025.6DL
24.9Kohm 64.24925.6DL
30.1Kohm 64.30125.6DL
34.8Kohm 64.34825.6DL
45Kohm 64.45325.6DL

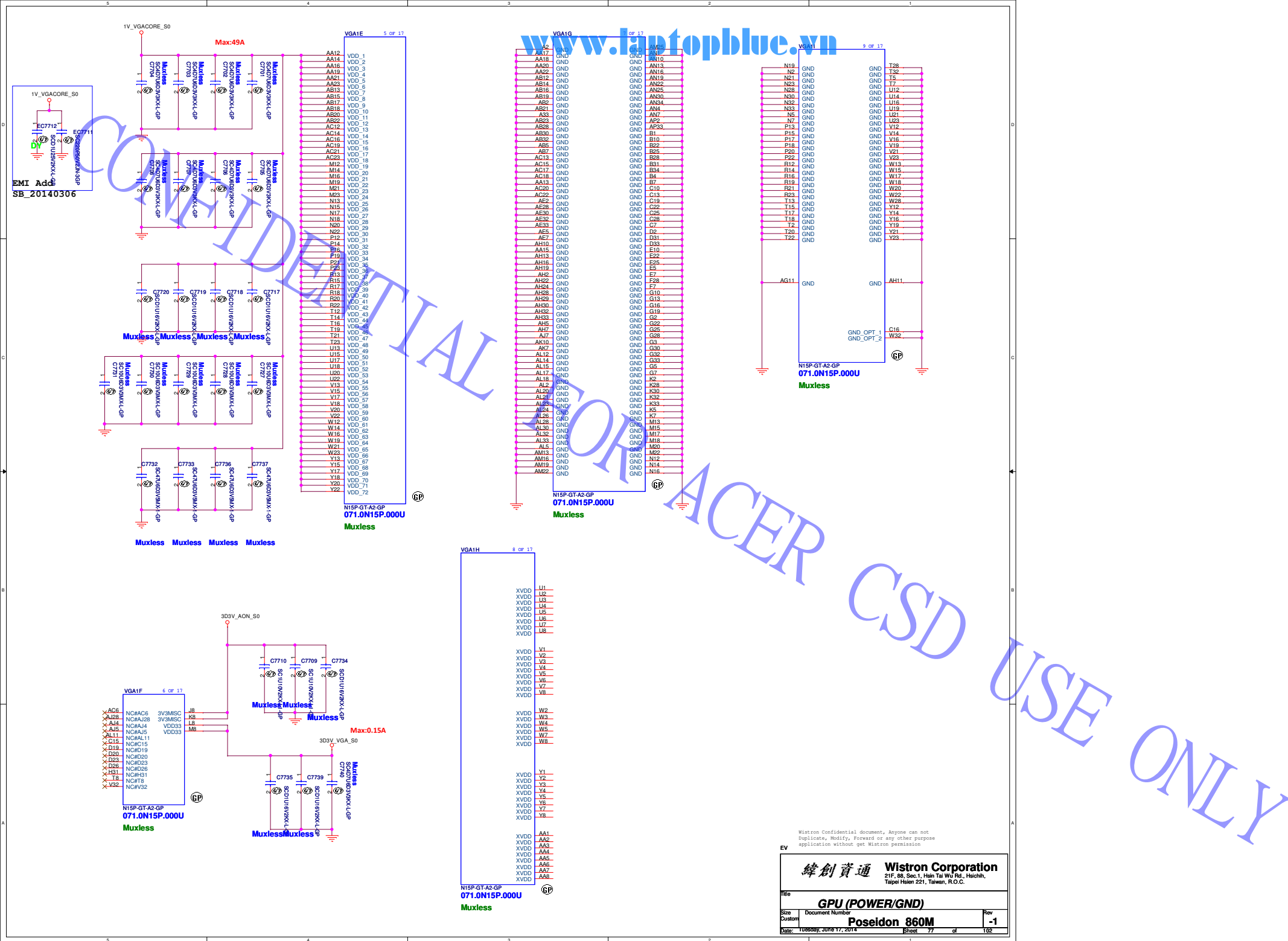


Check with NV

Xen

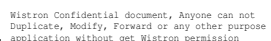
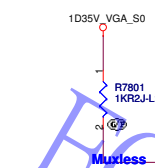
Table 11. N15P-GX/GT GDDR5 Recommended Memories

Memory Type	FVBDQ/FVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade (MHz)
GDDR5	1.35V/1.35V	1280x16	Samsung	K4G20325FD-FC03	D-die	0x0	2500
			Hynix	H5GC2H24BFR-T2C	B-die	0x1	2500
			Allicon	EDV2032B8B-6A-F	B-die	0x3	2500
		2560x16	Hynix	H5GC4H24MFR-T2C	W-die	0x2	2500
			Samsung	K4G41325F-CH03	C-die	0x3	2500
			Allicon	EPH4032B8B-60-F	A-die	0x4	2500



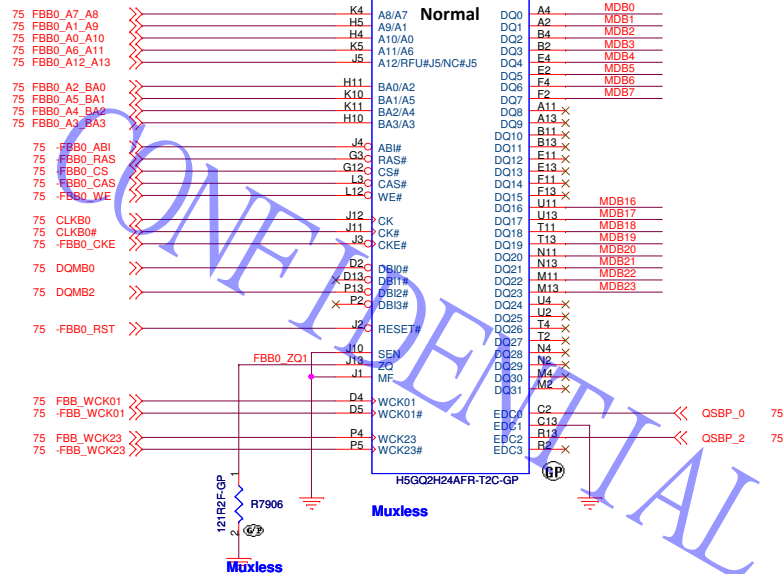
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(tentative)

↑
LOGIC



VRAM5B 2 OF 2

Normal



1D35V_VGA_S0

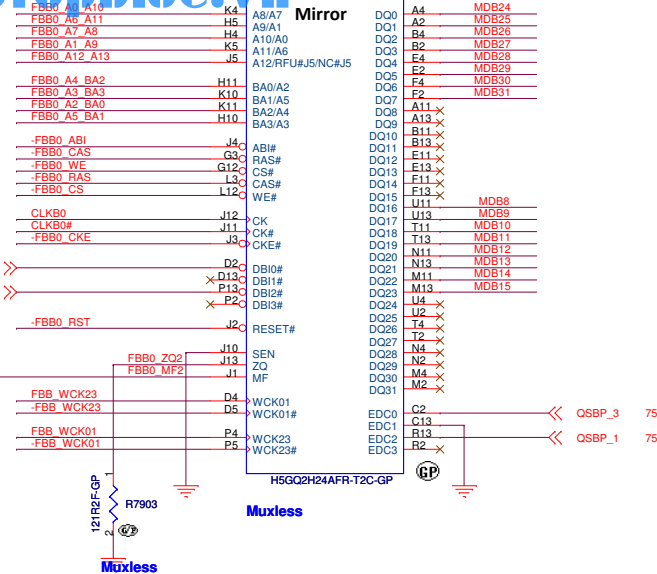
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75 DQMB1

Muxless

VRAM5B 2 OF 2

Mirror



1D35V_VGA_S0

DY

DY

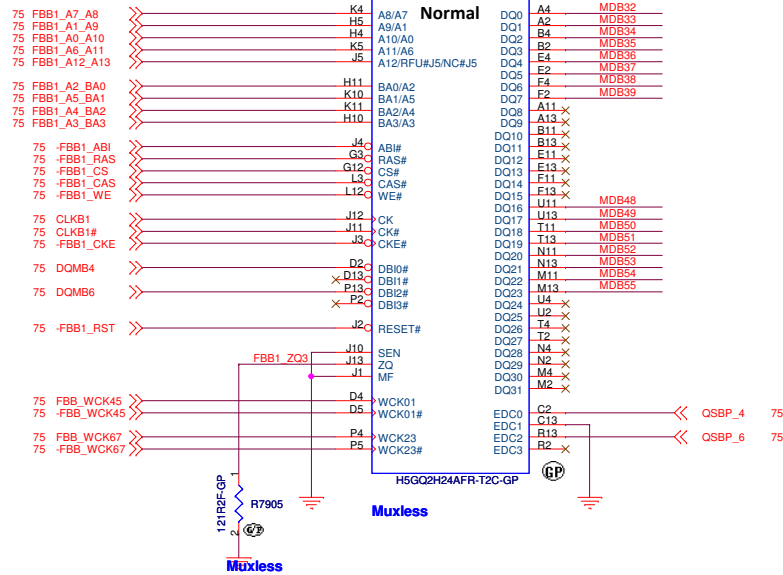
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DY

DY

VRAM7B 2 OF 2

Normal



1D35V_VGA_S0

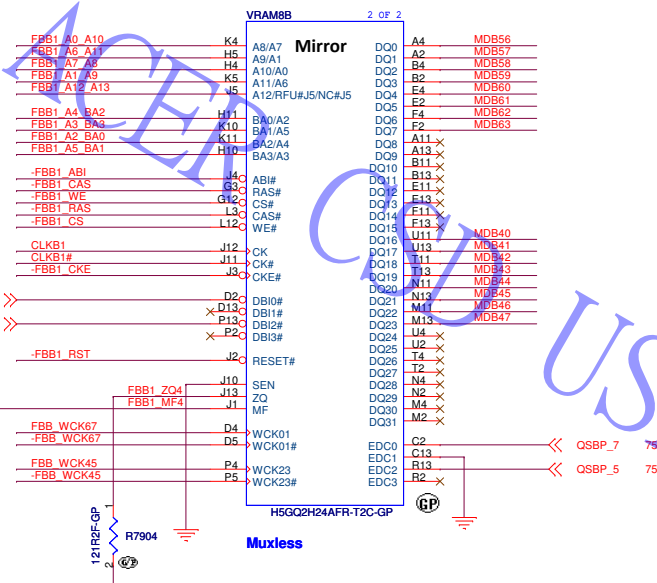
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75 DQMB5

Muxless

VRAM7B 2 OF 2

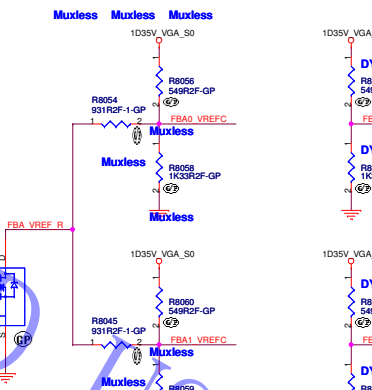
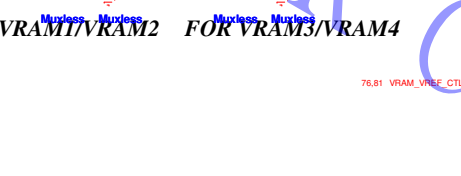
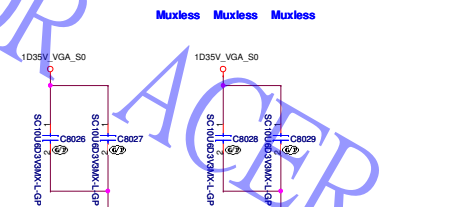
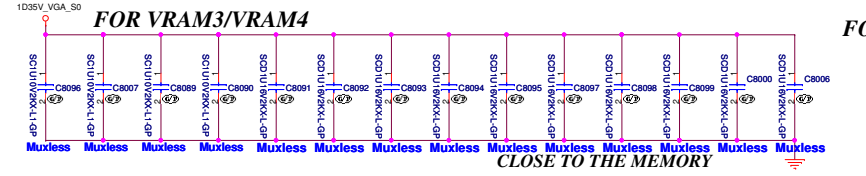
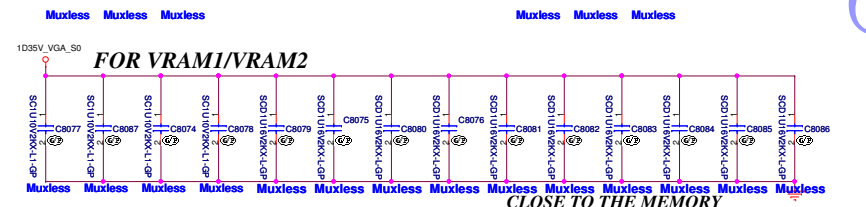
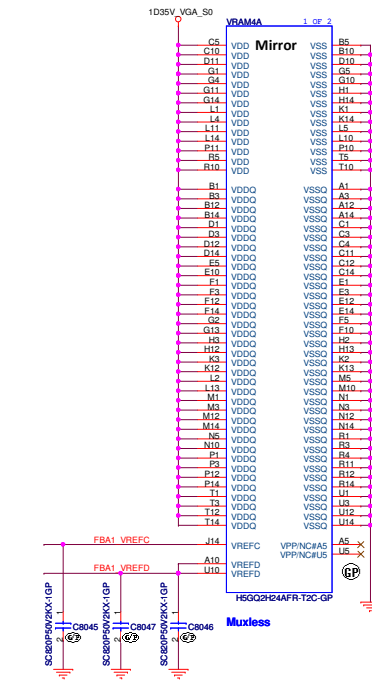
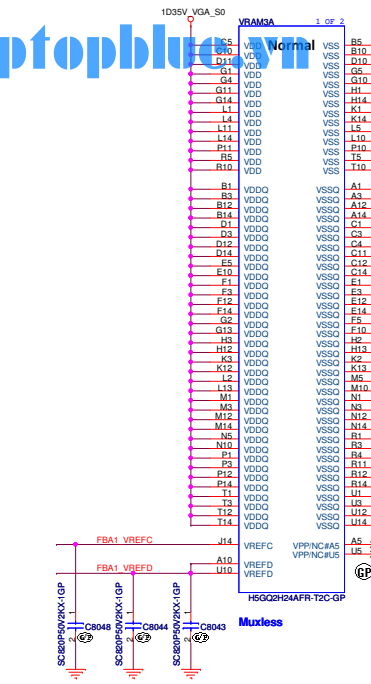
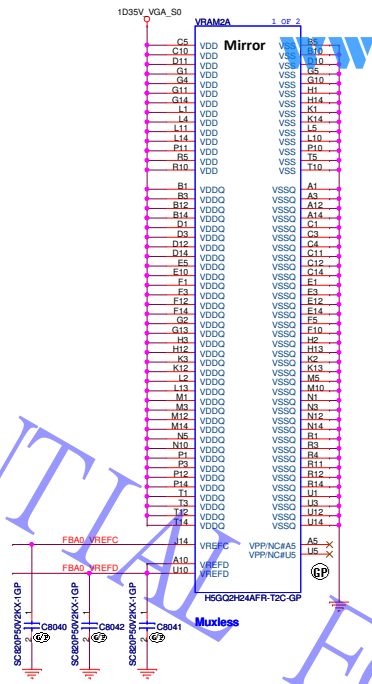
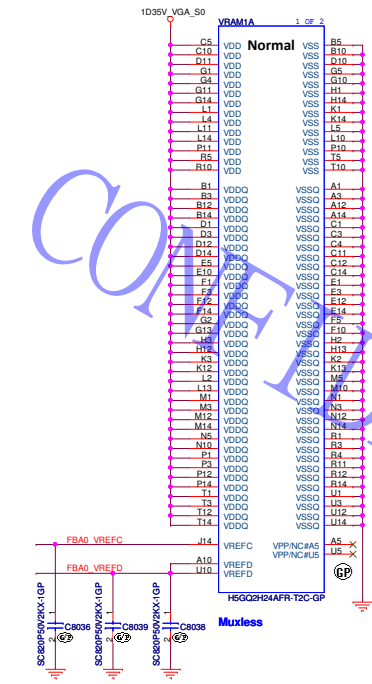
Mirror

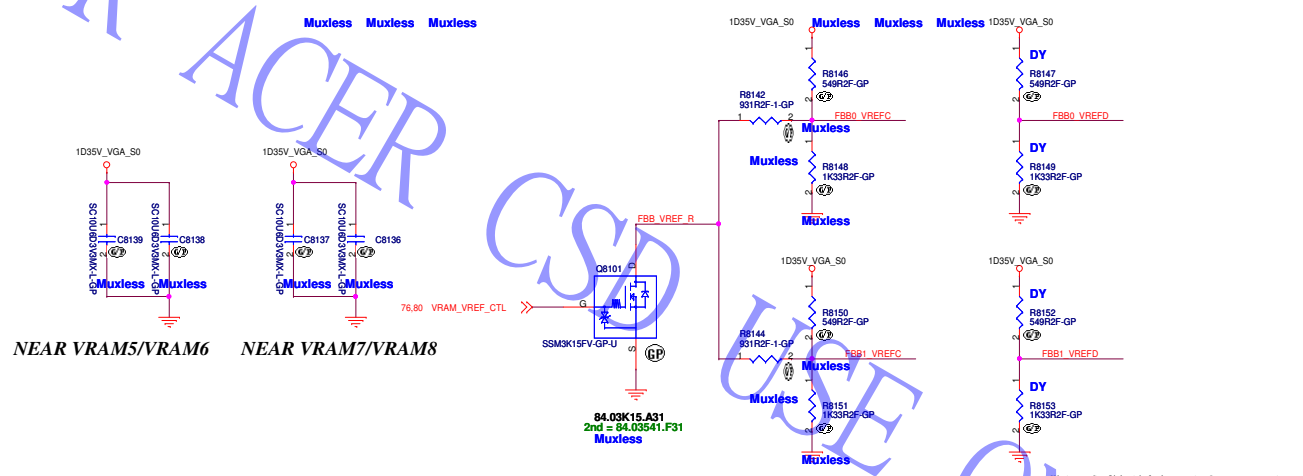
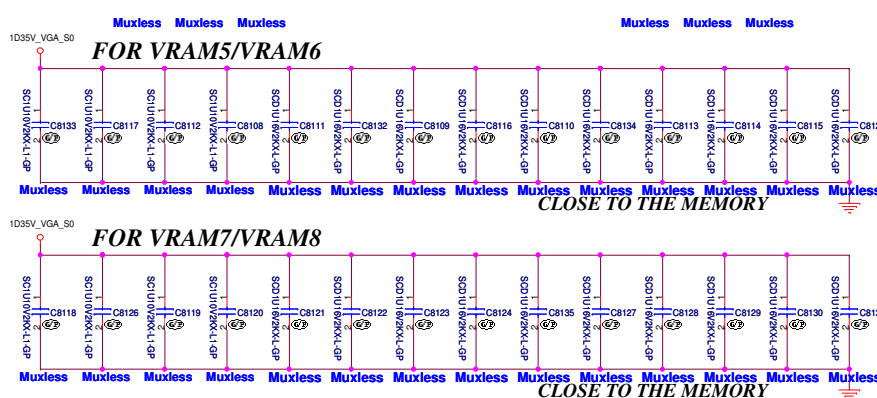
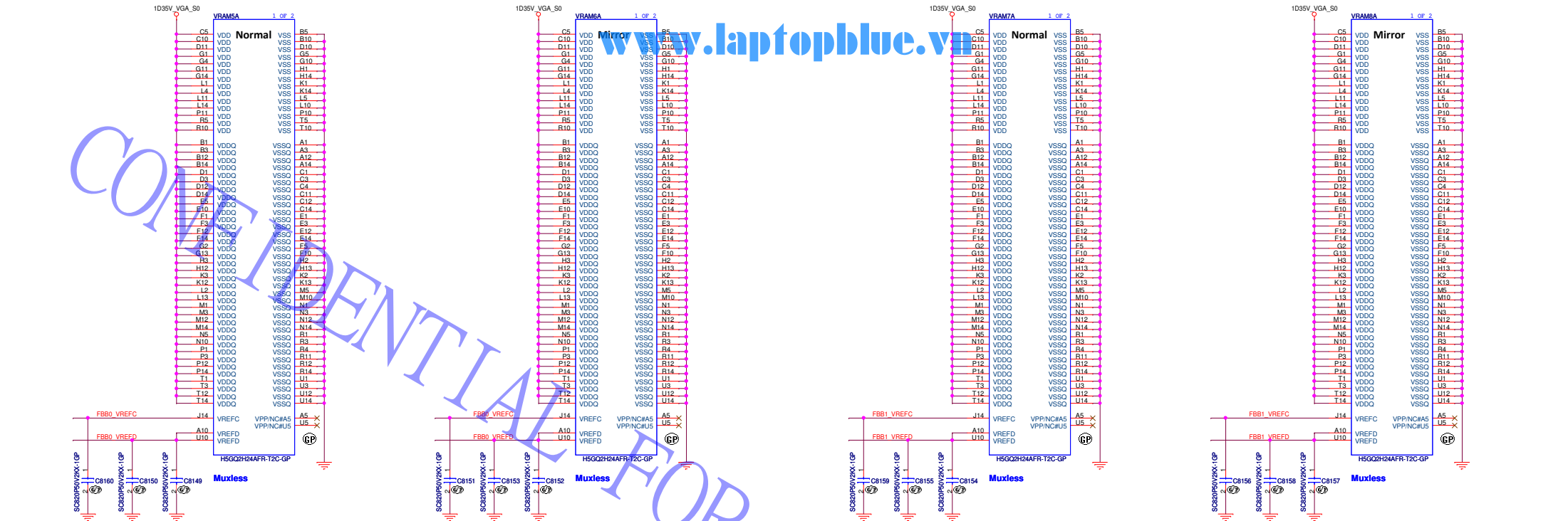


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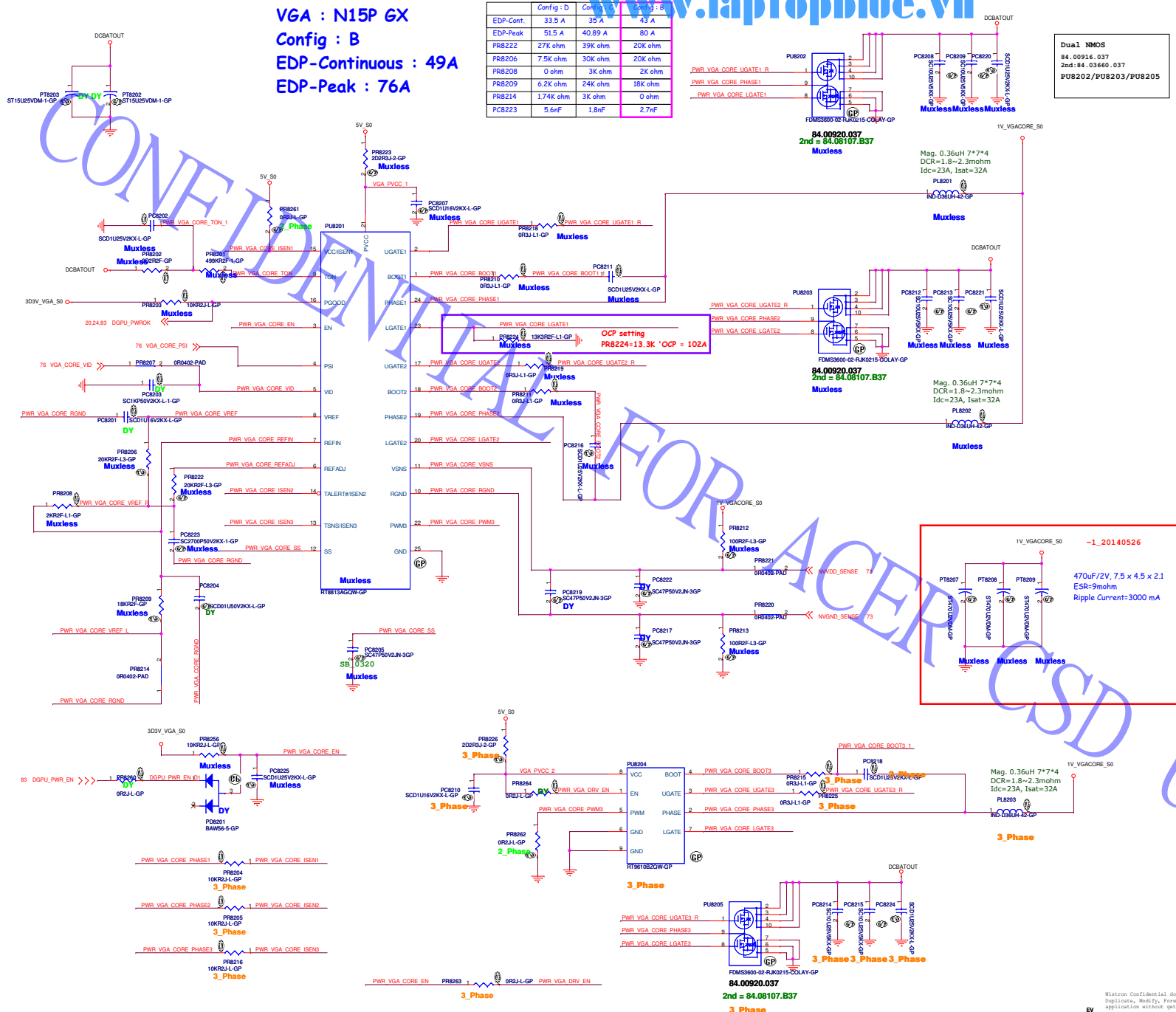
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VRAM B
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Poseidon 860M
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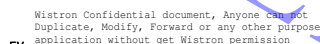
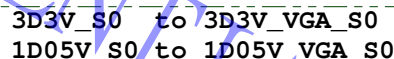




	Config : D	Config : A	Config : B
EDP-Cont.	33.5 A	35 A	43 A
EDP-Peak	51.5 A	40.89 A	80 A
PR8222	27K ohm	39K ohm	20K ohm
PR8206	7.5K ohm	30K ohm	20K ohm
PR8208	0 ohm	3K ohm	2K ohm
PR8209	6.2K ohm	24K ohm	18K ohm
PR8214	1.74K ohm	3K ohm	0 ohm
PC8223	5.6nF	1.8nF	2.7nF



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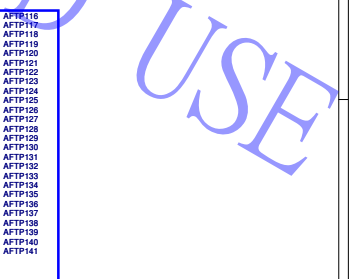
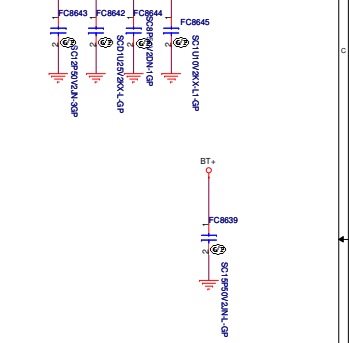
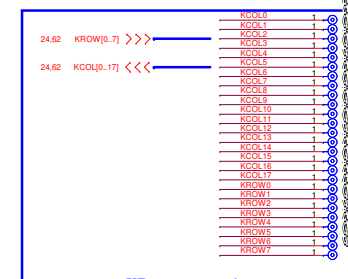
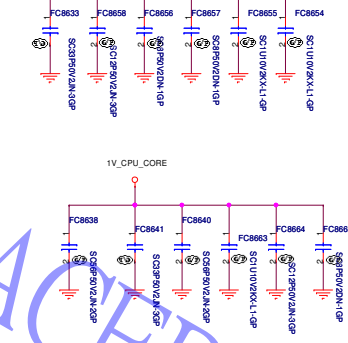
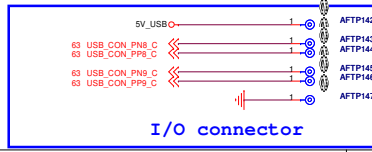
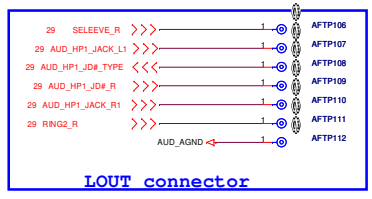
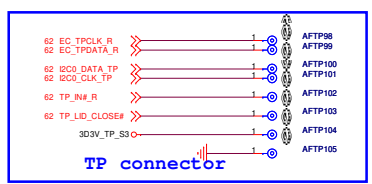
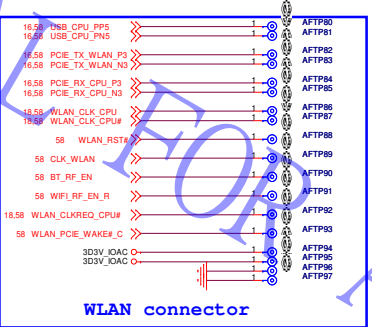
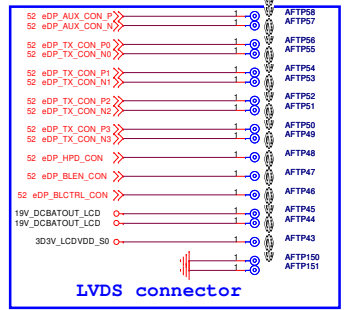
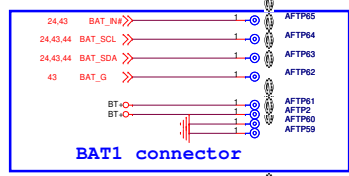
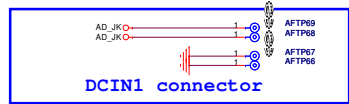
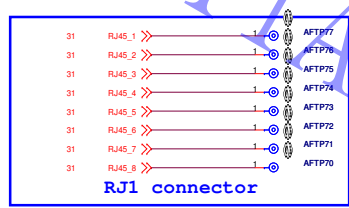
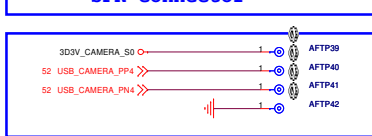
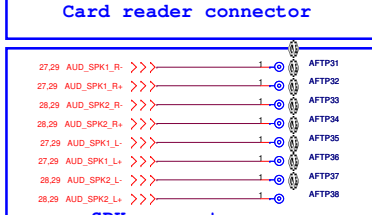
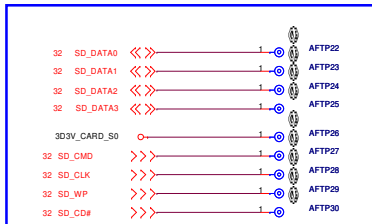
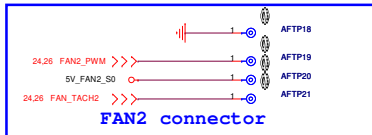
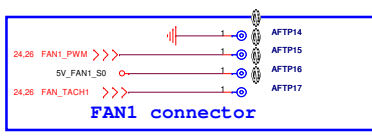
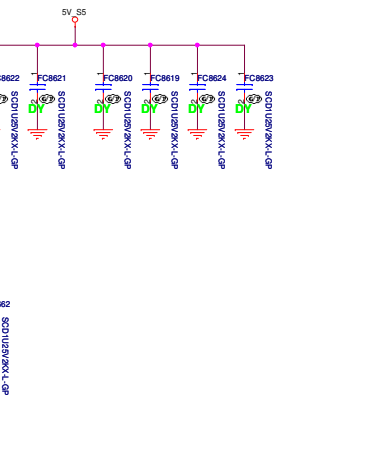
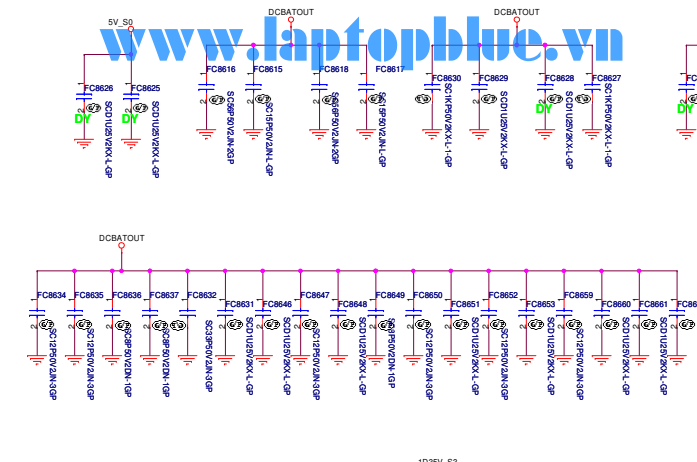
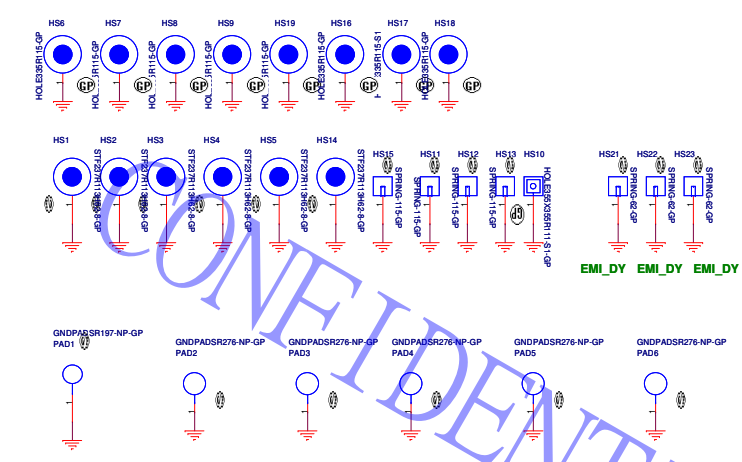
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Switchable GFX LCD(2/2)			
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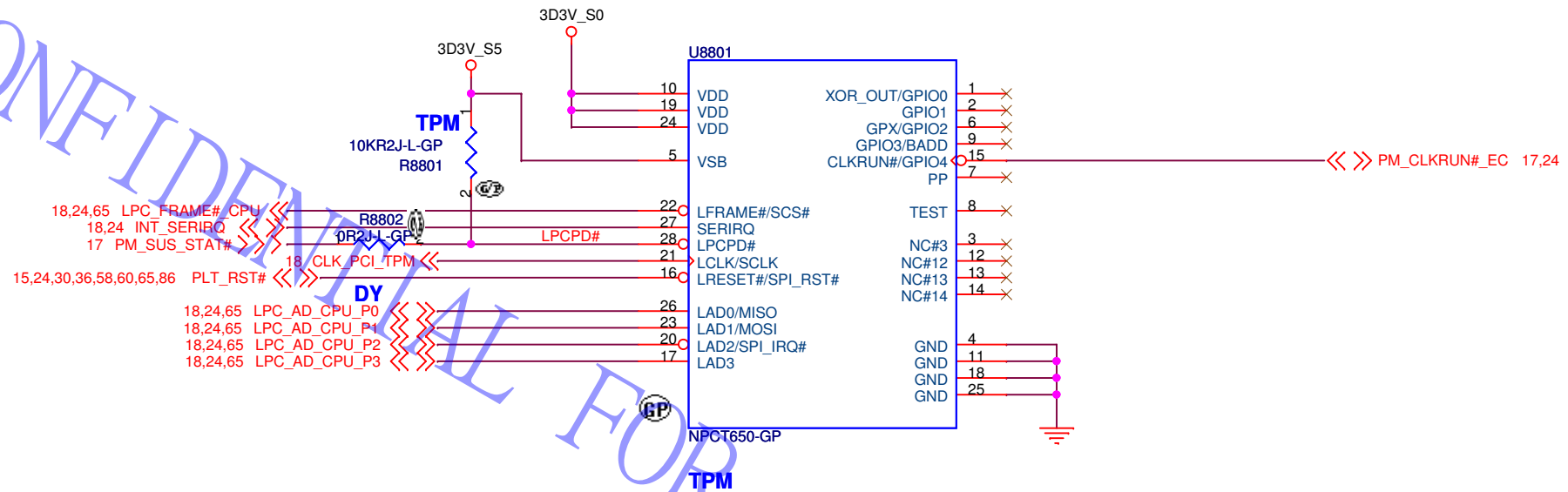


UNUSED PARTS/EMI Capacitors			
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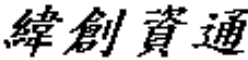
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Express Card			
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Title Smart Card socket		
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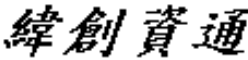
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Title Switchable GFX eDP			
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Title Bottom Docking		
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Title		
Inter LAN WG1217LM		
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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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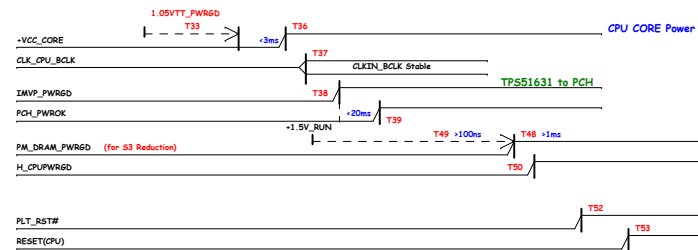
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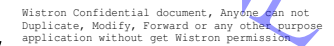
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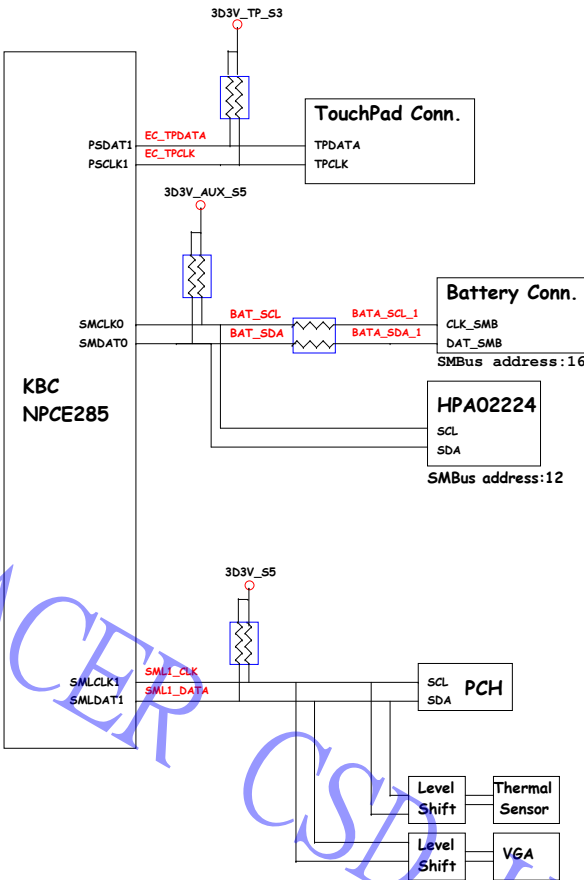
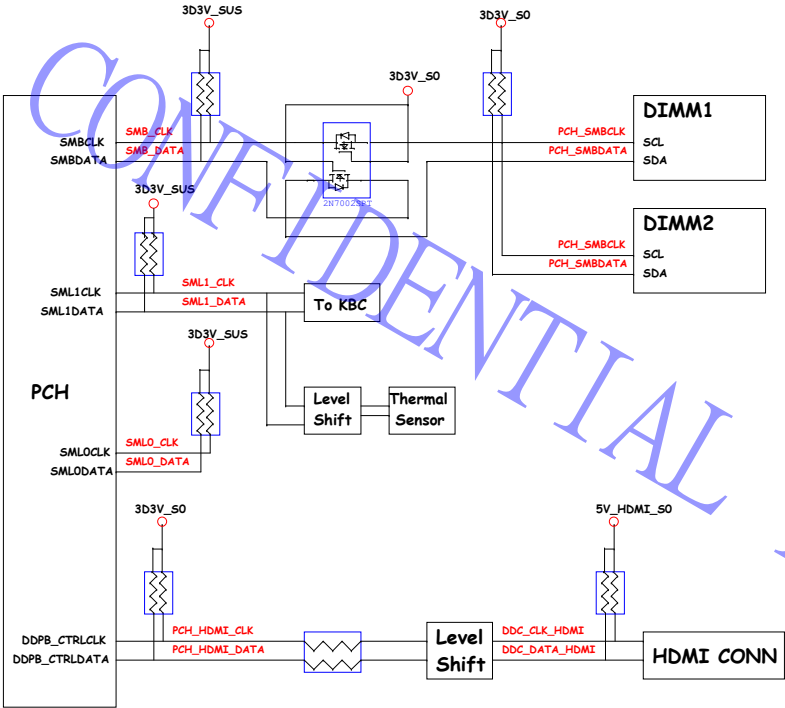
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PCH SMBus Block Diagram

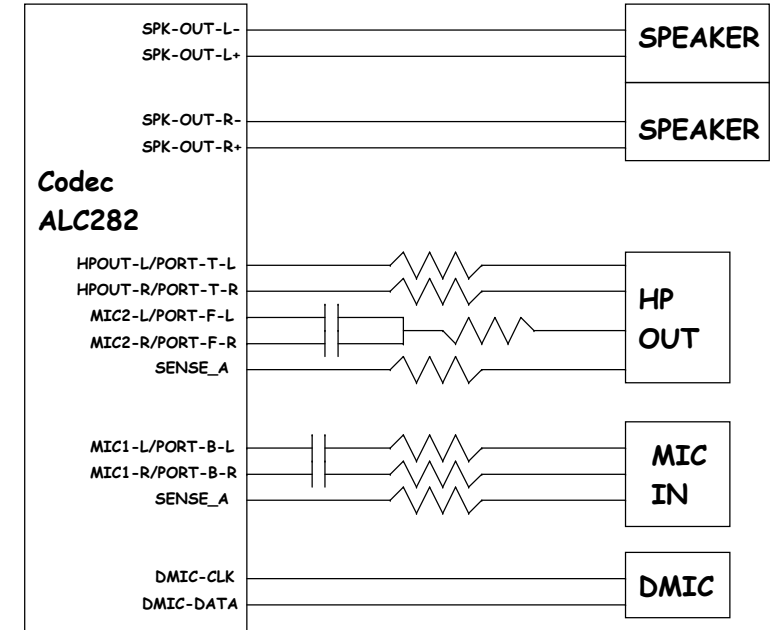
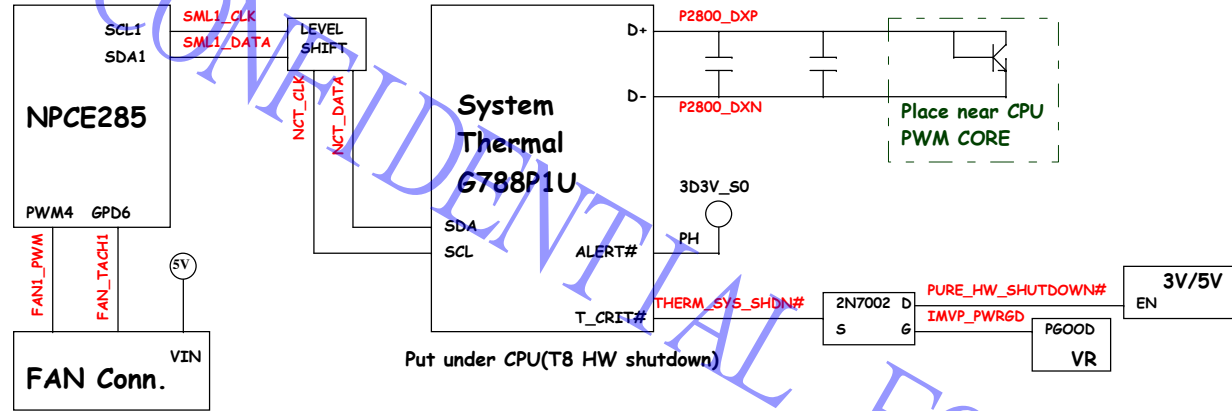
KBC SMBus Block Diagram



Thermal Block Diagram

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Audio Block Diagram



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