

Compal Confidential

NELA0 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M
Nvida N11P-GE1/N11M-OP1

2010-04-01

REV:1.0

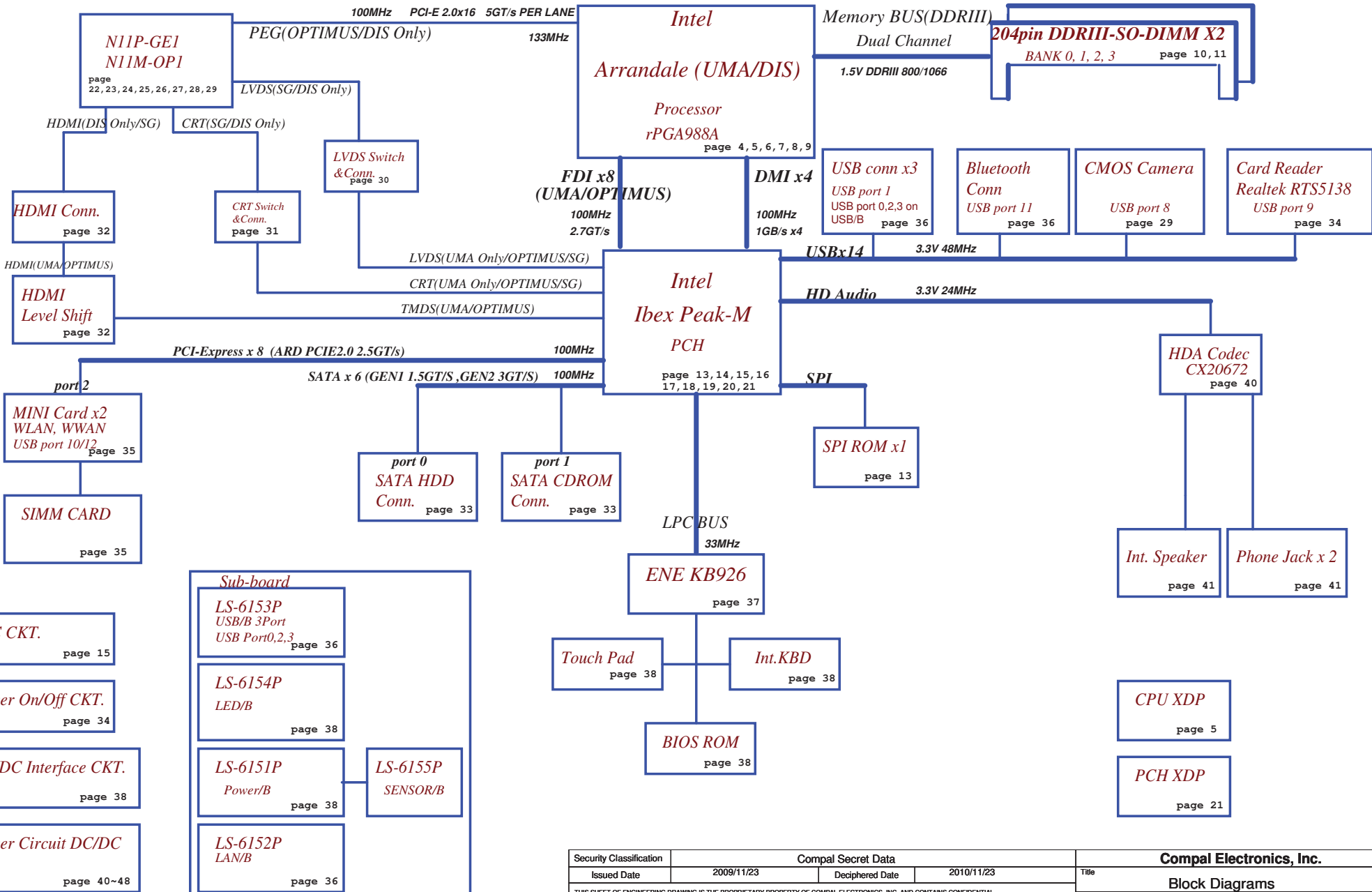
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				Size Custom	Document Number NELA0 M/B LA-6151P Schematic Date: Wednesday, April 21, 2010
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Model Name : NELA0
File Name : LA6151P

Clock Generator
IDT: 9LVS3199AKLFT
Realtek: RTM890N-631-GRT
133/120/100/96/14.318MHZ to PCH
page 12

Fan Control
page 38



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Config	
UMA Only	BT@,UMOP@,UMAO@,UMA@
OPTIMUS:	BT@,VGA@,OPT@,UMOP@,UMA@,VENTURA@,X76@
Discrete Only:	BT@,VGA@,DISO@,DIS@,VENTURA@,X76@
SWITCHABLE:	BT@,SG@,UMA@,VGA@,DIS@,VENTURA@,X76@

VRAM BOM Config	
X761@: X76198BOL01	Samsung 512MB
X762@: X76198BOL02	Hynix 512MB
X763@: X76198BOL03	Samsung 1024MB
X764@: X76198BOL04	Hynix 1024MB

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

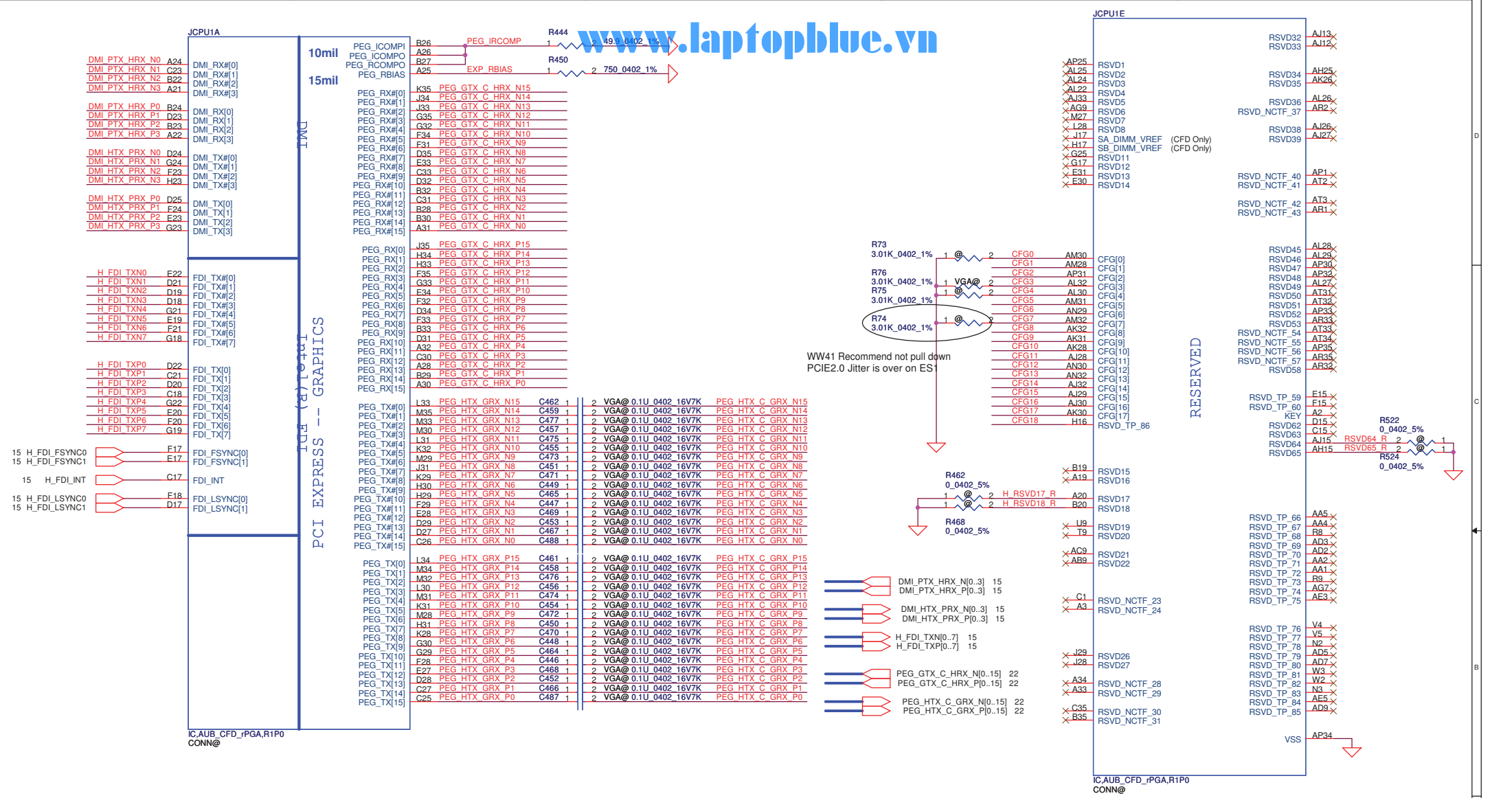
BTO Option Table

BTO Item	BOM Structure
UMA/OPT/SG	UMA@
UMA only &OPTIMUS	UMOP@
OPTIMUS	OPT@
Discrete Only	DISO@
GPU	VGA@
SWITCHABLE	SG@
VRAM	X76@
DIS only&SG	DIS@
Connector	CONN@
Ventura	VENTURA@
Blue Tooth	BT@
Unpop	@
3G	3G@

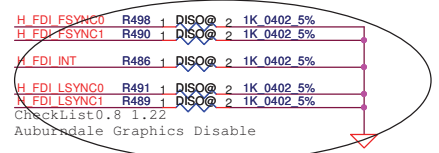
USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	USB/B (Right Side)
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Card Reader
	UHCI5	10	Mini Card(SIMM)
		11	Blue Tooth
	UHCI6	12	Mini Card(WLAN)
		13	SIMM CARD

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eDP Signals Mapping		
eDP Signal	PEG Signals	Lane Reversal
eDP_TX0	PEG HTX_C_GRX_P15	PEG HTX_C_GRX_P0
eDP_TX#0	PEG HTX_C_GRX_N15	PEG HTX_C_GRX_N0
eDP_TX1	PEG HTX_C_GRX_P14	PEG HTX_C_GRX_P1
eDP_TX#1	PEG HTX_C_GRX_N14	PEG HTX_C_GRX_N1
eDP_TX2	PEG HTX_C_GRX_P13	PEG HTX_C_GRX_P2
eDP_TX#2	PEG HTX_C_GRX_N13	PEG HTX_C_GRX_N2
eDP_TX3	PEG HTX_C_GRX_P12	PEG HTX_C_GRX_P3
eDP_TX#3	PEG HTX_C_GRX_N12	PEG HTX_C_GRX_N3
eDP_AUX	PEG GTX_C_HRX_P13	PEG GTX_C_HRX_P2
eDP_AUX#	PEG GTX_C_HRX_N13	PEG GTX_C_HRX_N2
eDP_HPD#	PEG GTX_C_HRX_P12	PEG GTX_C_HRX_P3



CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

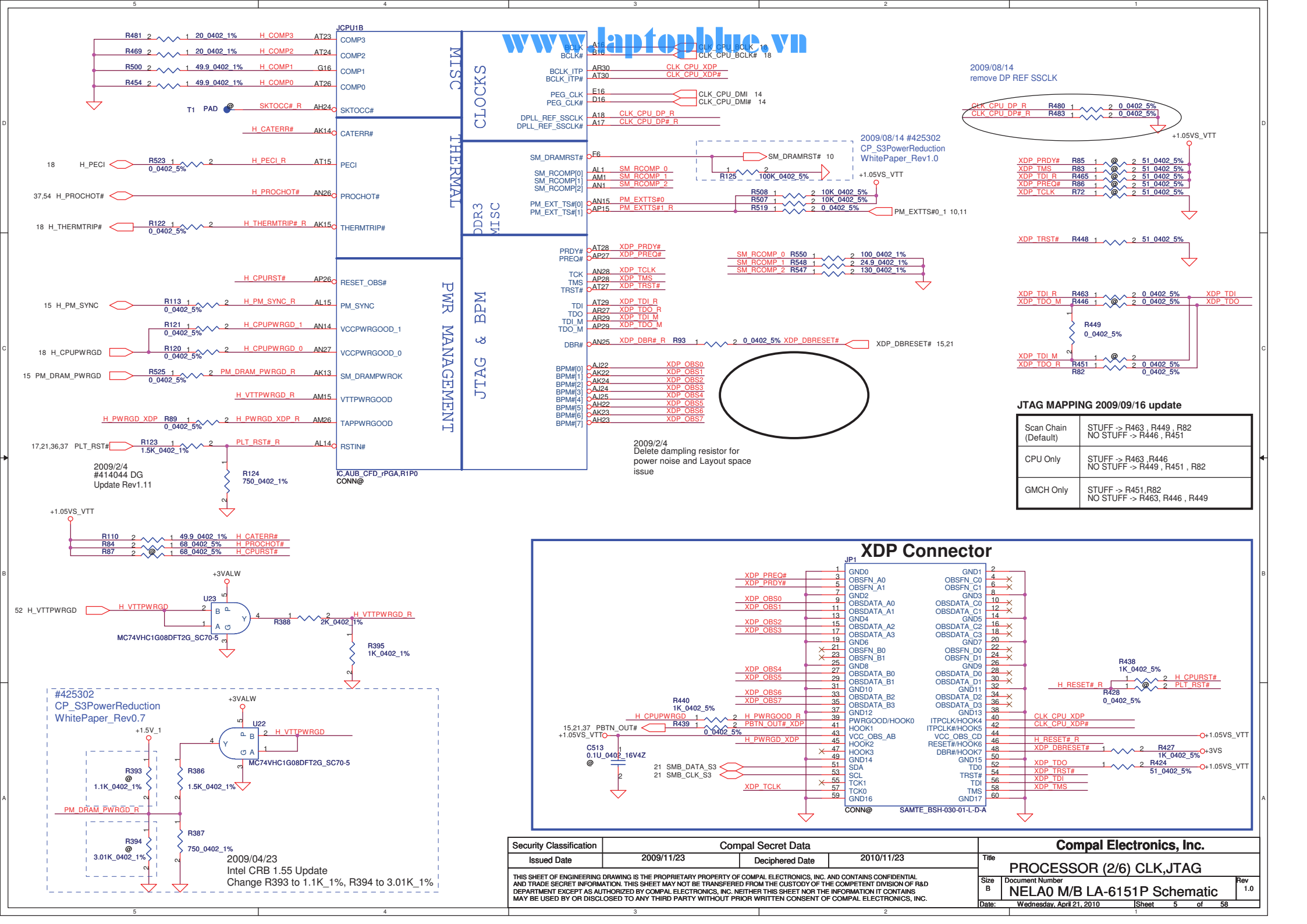
CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 > 0, 14 > 1, ...

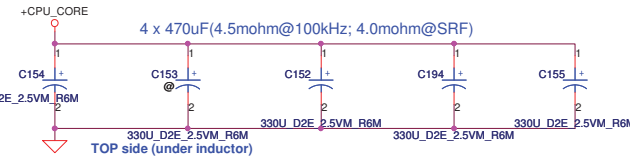
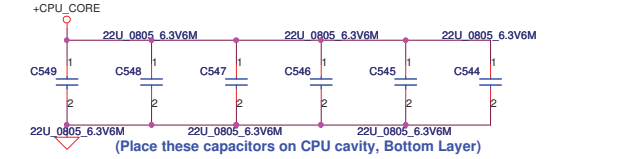
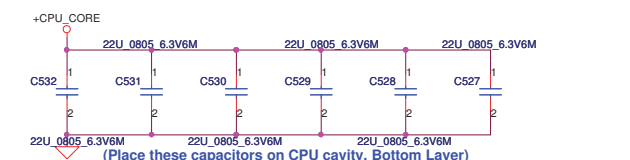
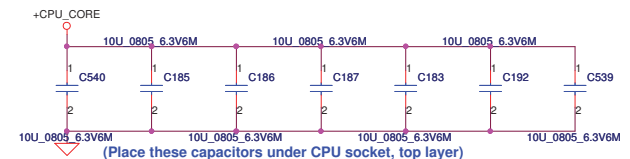
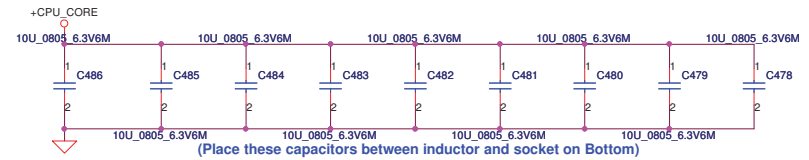
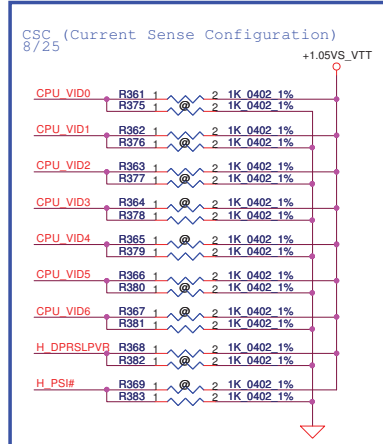
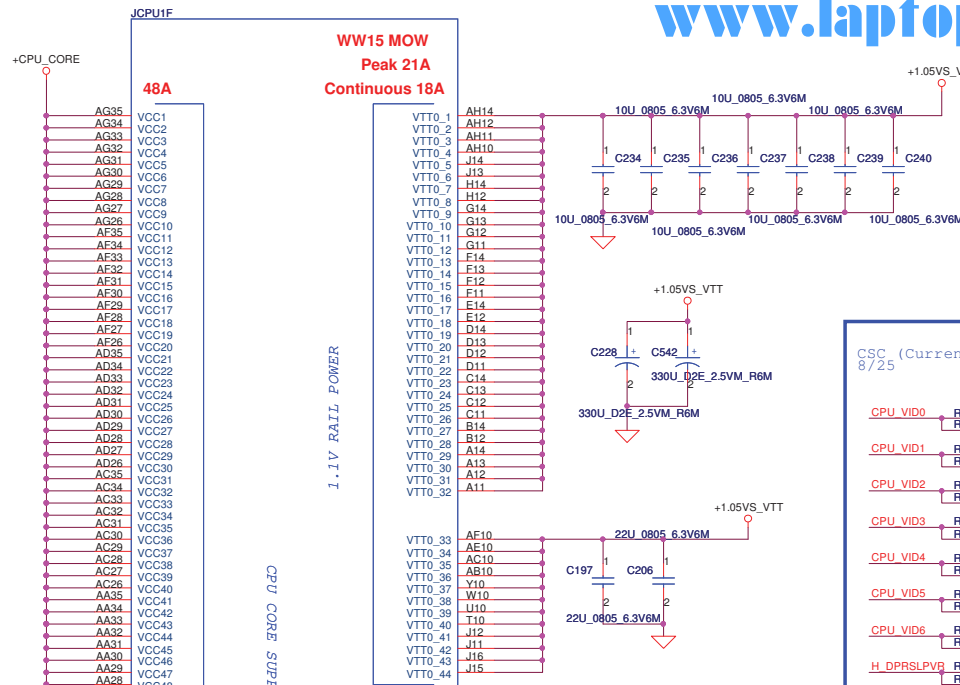
CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

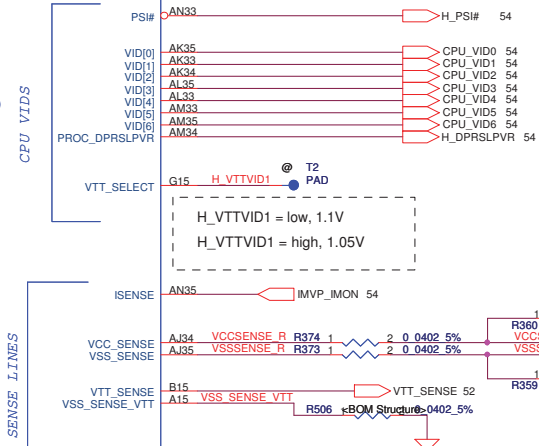
Default



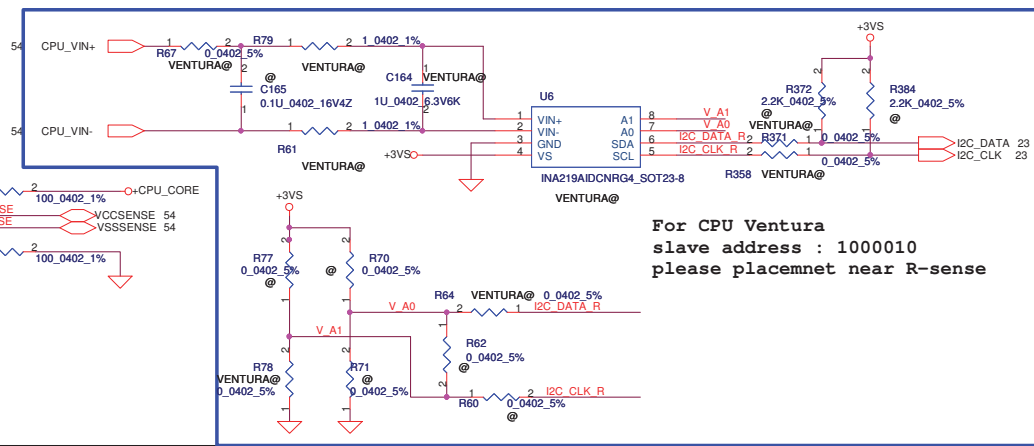
+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP, Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	



POWER



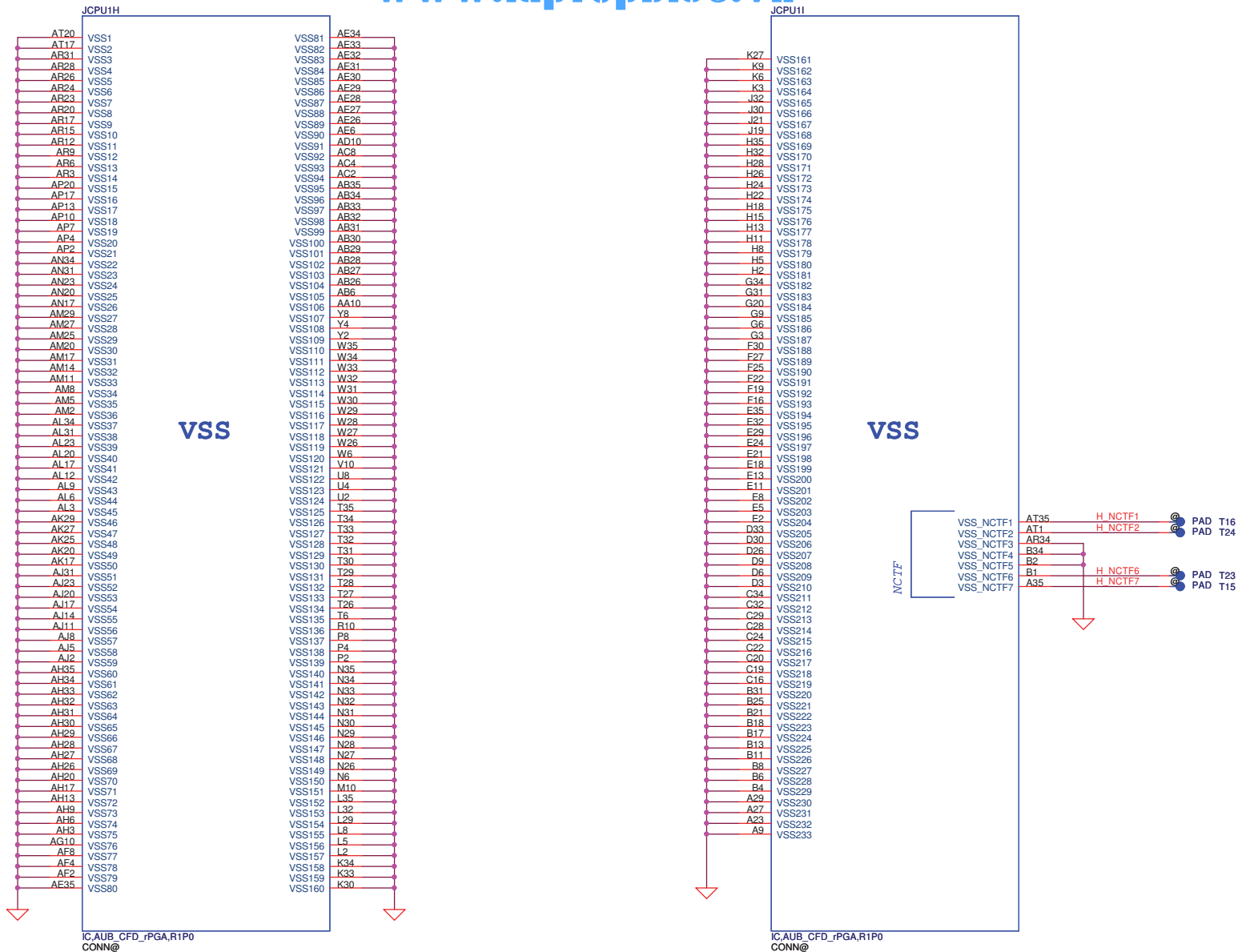
VTT Rail
Auburndale +1.1VS_VTT=1.05V
Clarkfield +1.1VS_VTT=1.1V



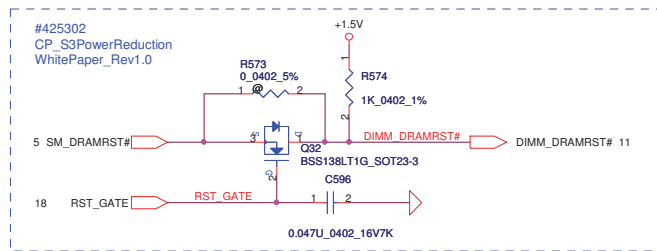
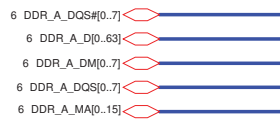
For CPU Ventura
slave address : 1000010
please placemnet near R-sense

IC_AUB_CFD_PGA_R1P0
CONN@

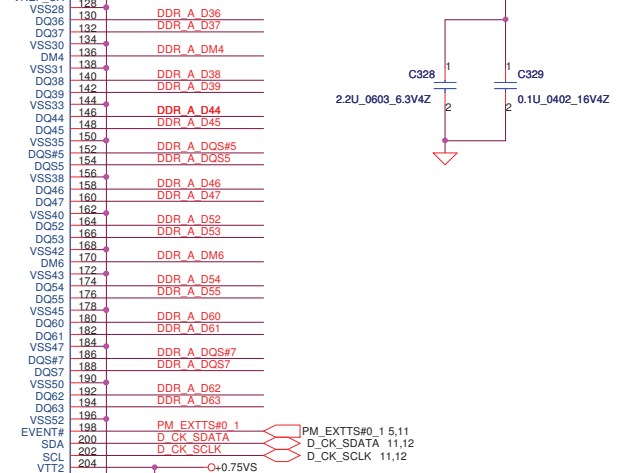
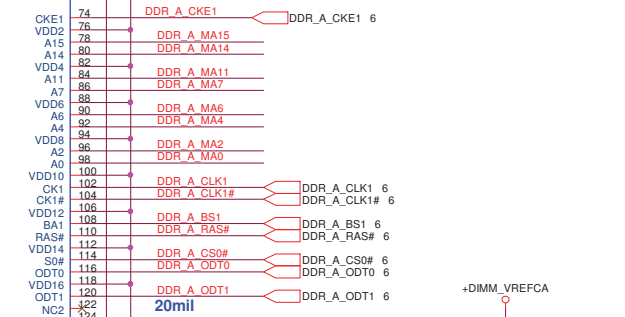
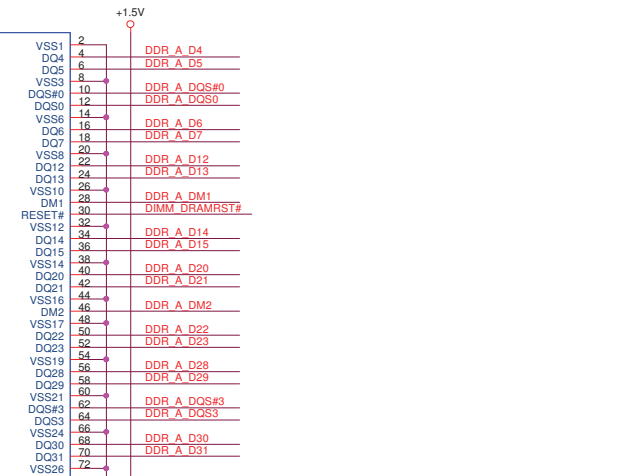
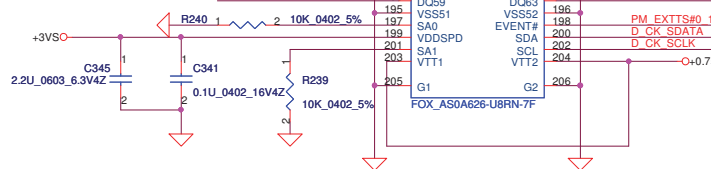
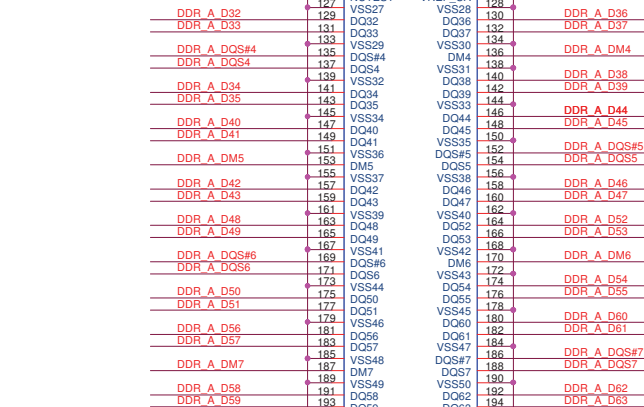
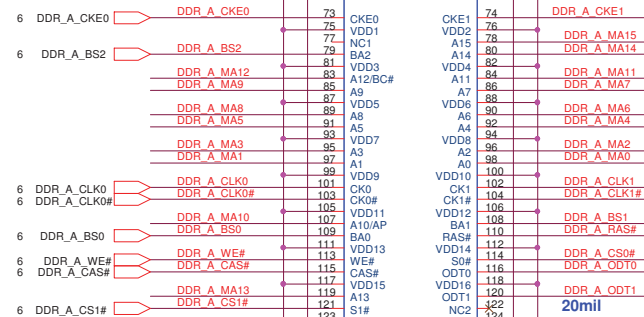
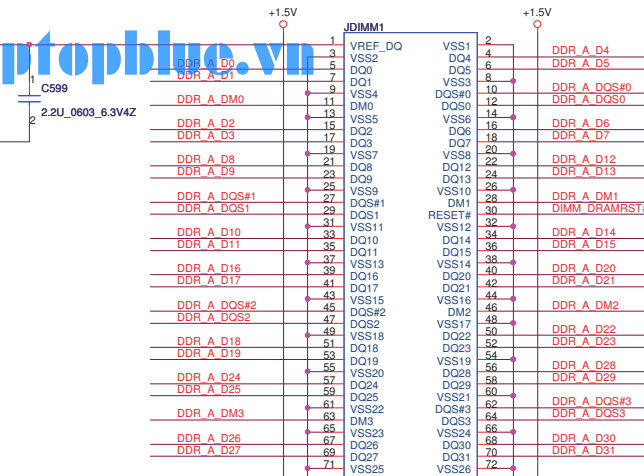
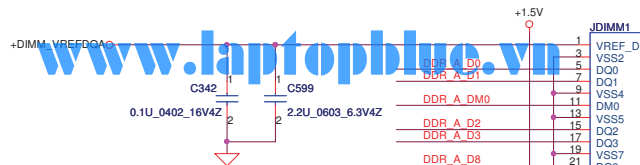
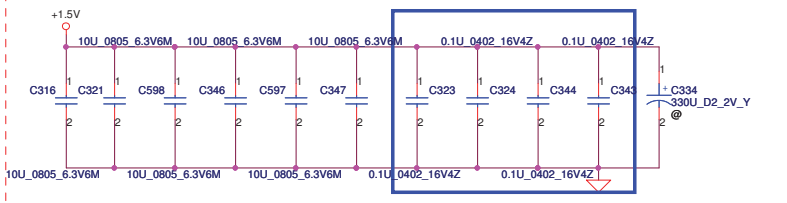
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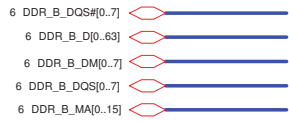


Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



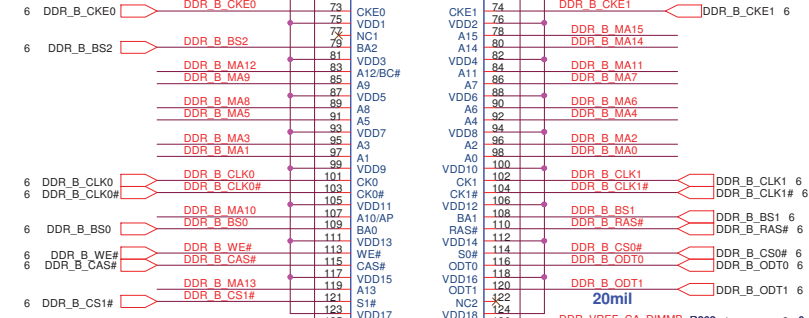
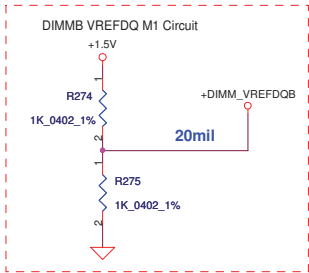
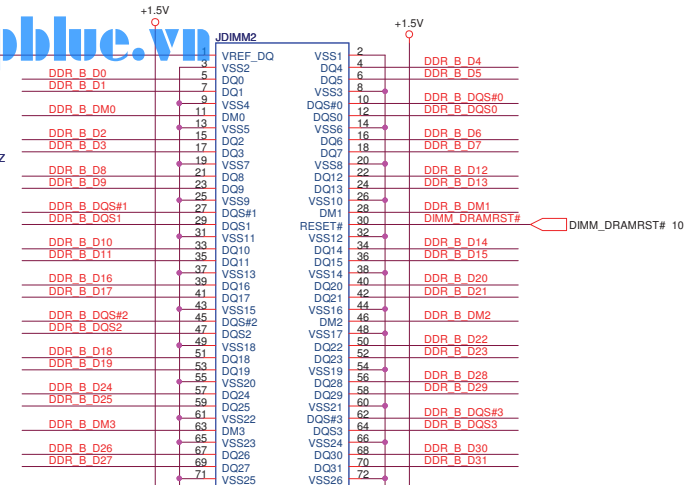
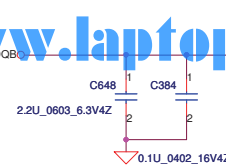
DDRIII-SODIMM SLOT1

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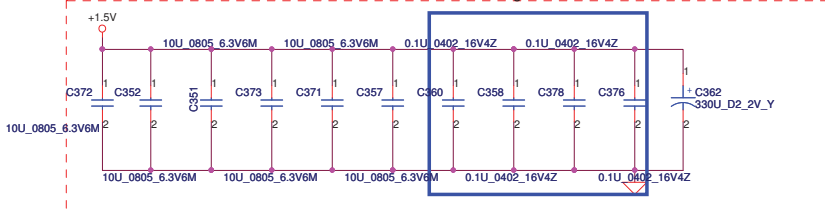
2008/9/8 #400755
Calpella Clarkfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

www.laptopblue.vn

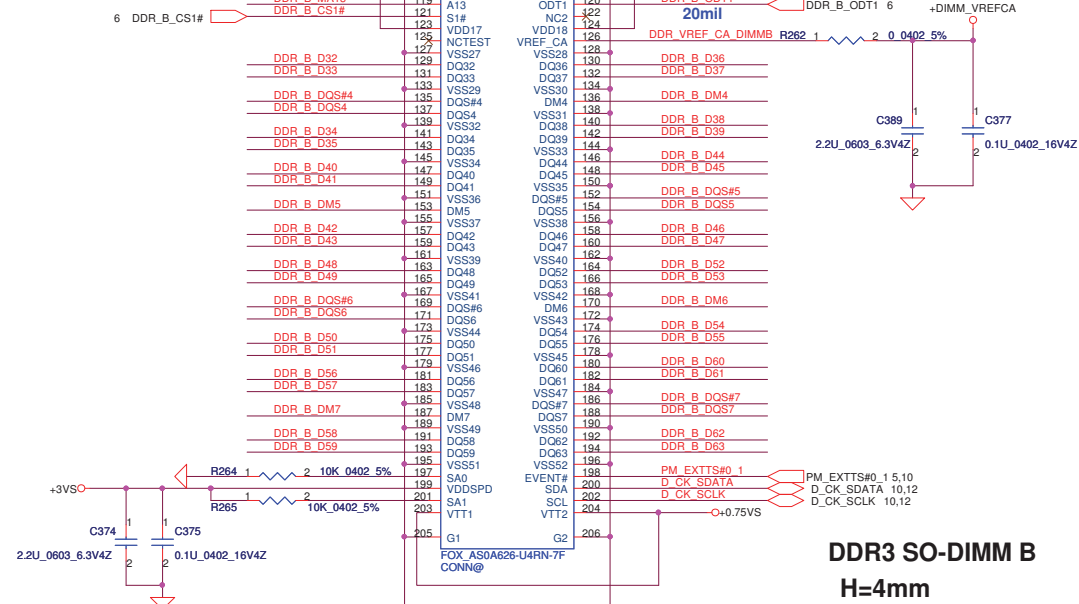
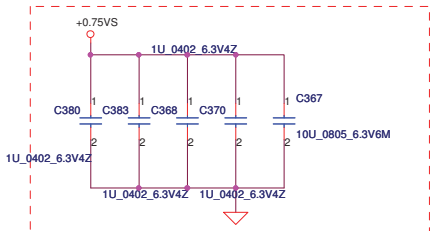


Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command
and Control signals of DIMM



Layout Note:
Place near JDIMM2.203 & JDIMM2.204

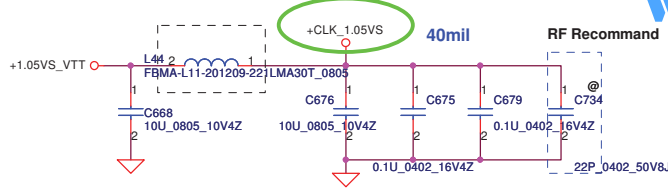


DDR3 SO-DIMM B
H=4mm

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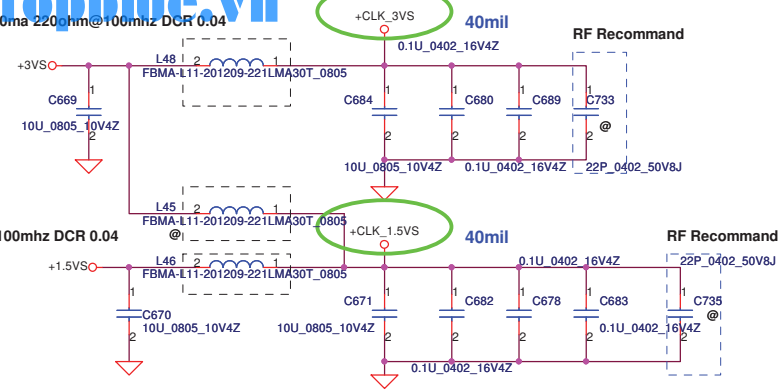
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SM010014520 3000ma 220ohm@100mhz DCR 0.04

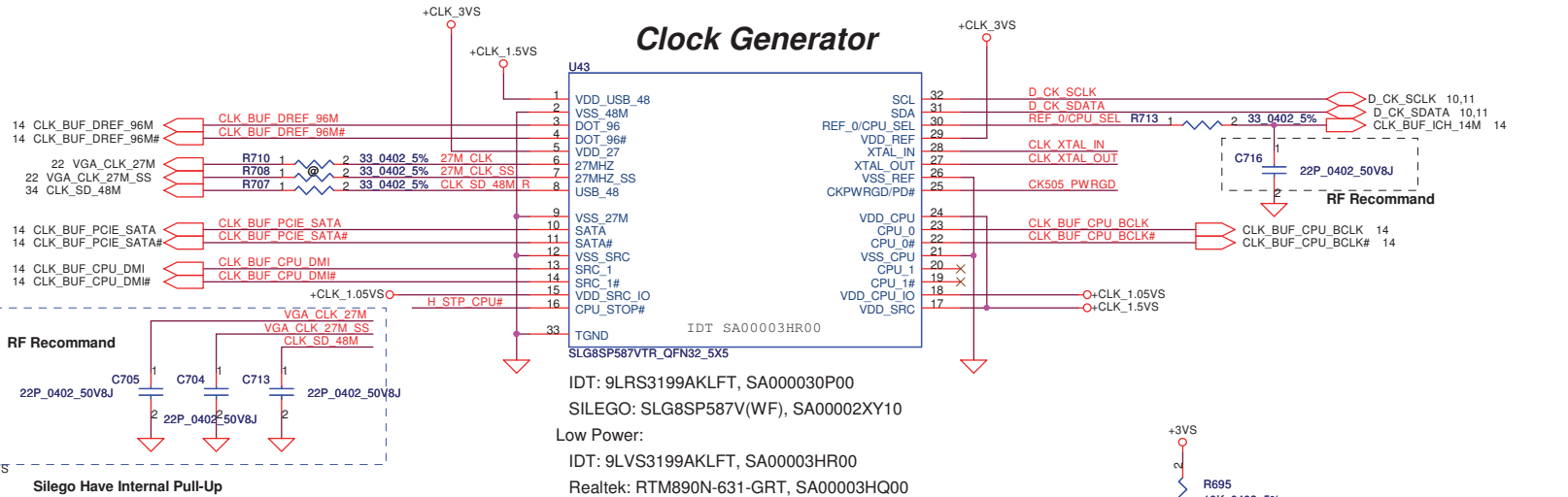


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SM010014520 3000ma 220ohm@100mhz DCR 0.04



SM010014520 3000ma 220ohm@100mhz DCR 0.04



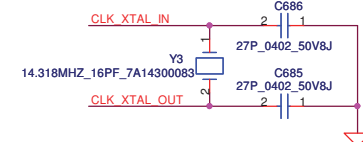
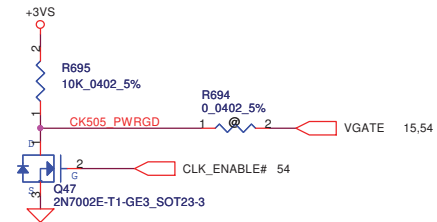
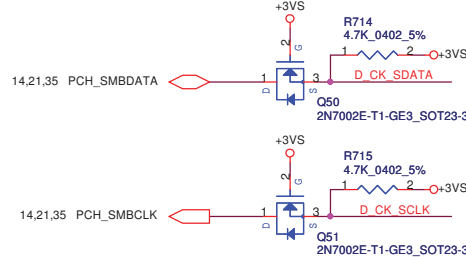
IDT 9LVS3199AKLFT NC

Silego Have Internal Pull-Up

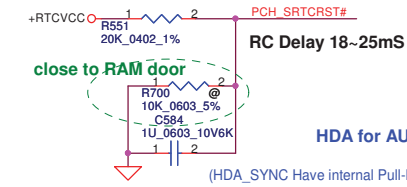
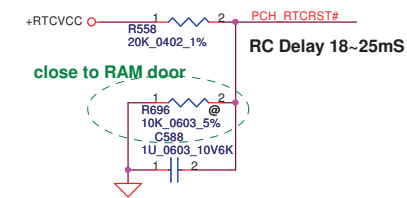
IDT Have Internal Pull-Down

FOR Realtek

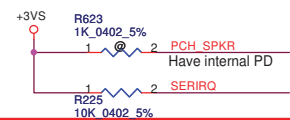
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



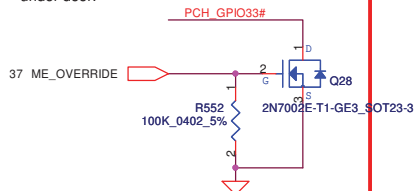
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Issued Date				2009/11/23				Deciphered Date			
2010/11/23				Title				Clock Generator (CK505)			
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Date: Wednesday, April 21, 2010				Sheet 12 of 58				Rev 1.0			



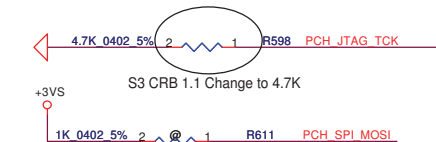
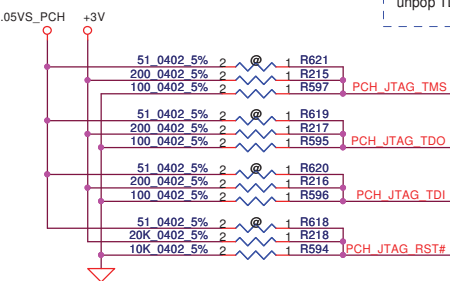
HDA_SYNC
On Die PLL VR is supplied by 1.5V when sampled High, 1.8V when sampled Low.



If GPIO33 pull down, ME will not working.
For factory update ME, pull down resistor pull under door.

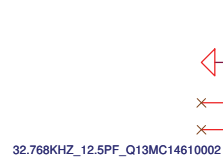


GPIO33 has a weak internal pull-up
NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel Management Engine after chipset bringup and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.

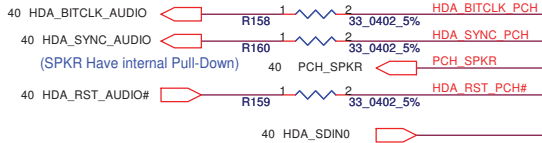


enable iTPM: SPI_MOSI High

MOSI This signal has a weak internal pull-down resistor. This signal must be sampled low.

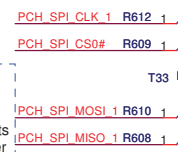


INTRVREN - Integrated SUS 1.05V VRM Enable High - Enable Internal VRs



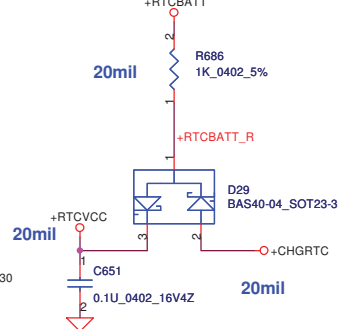
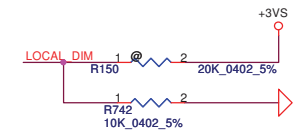
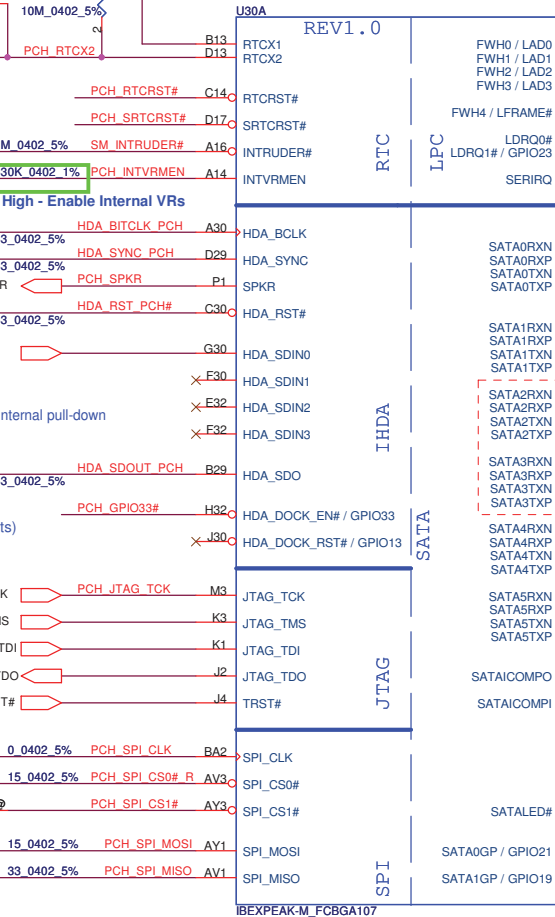
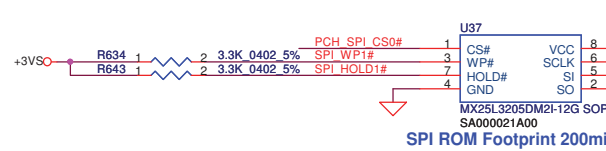
HDA_SDO, This signal has a weak internal pull-down resistor. Should not be Pull High

GPIO33 can not pull down (manufacturing environments)



2008 Intel MOW36/MOW50
TDO:
Reserved on ES1 Sample
Mount R217, R595 on ES2 Sample

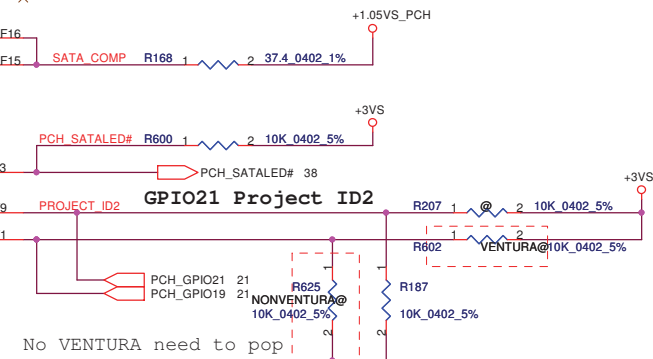
MP mount R621, R619, R620, R618 and remove others



SATA for HDD1

SATA for ODD

2/10 SATA2, SATA3 not support on HM55

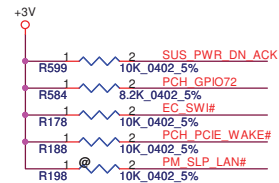
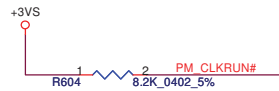


SKU Structure	
GPIO19	Structure
0	NO VENTURA
1	VENTURA

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				Customer	NELA0 M/B LA-6151P Schematic
				Date	Wednesday, April 21, 2010
				Sheet	13 of 58

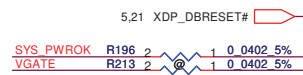
4 DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
 4 DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
 4 DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
 4 DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

4 H_FDI_TXN[0..7] H_FDI_TXN[0..7]
 4 H_FDI_TXP[0..7] H_FDI_TXP[0..7]



+1.05VS_PCH

09/09/14 WW37 PCH WAKE# PU 10K



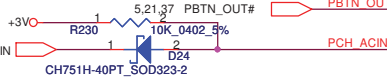
SYS_PWROK

LAN_RST#

5 PM_DRAM_PWRGD

PCH_RSMRST#

37 SUS_PWR_DN_ACK



PCH_ACIN

37 EC_SWI#

+3VS

21 SYS_PWROK

SYS_PWROK

EC_PWROK

LAN_RST#

No used Integrated LAN,
connecting LAN_RST# to GND

DMI_HTX_PRX_N0 BC24
 DMI_HTX_PRX_N1 BJ22
 DMI_HTX_PRX_N2 AW20
 DMI_HTX_PRX_N3 BJ20

DMI_HTX_PRX_P0 BD24
 DMI_HTX_PRX_P1 BG22
 DMI_HTX_PRX_P2 BA20
 DMI_HTX_PRX_P3 BG20

DMI_PTX_HRX_N0 BE22
 DMI_PTX_HRX_N1 BF21
 DMI_PTX_HRX_N2 BD20
 DMI_PTX_HRX_N3 BE18

DMI_PTX_HRX_P0 BD22
 DMI_PTX_HRX_P1 BH21
 DMI_PTX_HRX_P2 BC20
 DMI_PTX_HRX_P3 BD18

U30C

REV1.0

DMIORXN
 DMI1RXN
 DMI2RXN
 DMI3RXN

DMIORXP
 DMI1RXP
 DMI2RXP
 DMI3RXP

DMIOTXN
 DMI1TXN
 DMI2TXN
 DMI3TXN

DMIOTXP
 DMI1TXP
 DMI2TXP
 DMI3TXP

DMI_ZCOMP

DMI_IRCOMP

System Power Management

SYS_RESET#

SYS_PWROK

PWROK

MEPWROK

LAN_RST#

DRAMPWROK

RSMRST#

SUS_PWR_DN_ACK / GPIO30

PWRBTN#

ACPRESENT / GPIO31

BATLOW# / GPIO72

RI#

IBEXPEAK-M_FCBGA107

FDI_RXN0

FDI_RXN1

FDI_RXN2

FDI_RXN3

FDI_RXN4

FDI_RXN5

FDI_RXN6

FDI_RXN7

FDI_RXP0

FDI_RXP1

FDI_RXP2

FDI_RXP3

FDI_RXP4

FDI_RXP5

FDI_RXP6

FDI_RXP7

FDI_INT

FDI_FSYNC0

FDI_FSYNC1

FDI_LSYNC0

FDI_LSYNC1

WAKE#

CLKRUN# / GPIO32

SUS_STAT# / GPIO61

SUSCLK / GPIO62

SLP_S5# / GPIO63

SLP_S4#

SLP_S3#

SLP_M#

TP23

PMSYNCH

SLP_LAN# / GPIO29

BA18

BH17

BD16

BJ16

BA16

BE14

BA14

BG12

BB18

BE17

BC16

BG16

AW16

BD14

BB14

BD12

H_FDI_TXN0

H_FDI_TXN1

H_FDI_TXN2

H_FDI_TXN3

H_FDI_TXN4

H_FDI_TXN5

H_FDI_TXN6

H_FDI_TXN7

H_FDI_TXP0

H_FDI_TXP1

H_FDI_TXP2

H_FDI_TXP3

H_FDI_TXP4

H_FDI_TXP5

H_FDI_TXP6

H_FDI_TXP7

H_FDI_INT 4

H_FDI_FSYNC0 4

H_FDI_FSYNC1 4

H_FDI_LSYNC0 4

H_FDI_LSYNC1 4

PCH_PCIE_WAKE# 35

PM_CLKRUN# 37

PCH_GPIO61 @ PAD T7

PCH_GPIO62 @ PAD T31

PM_SLP_S5# 37

PM_SLP_S4# 37

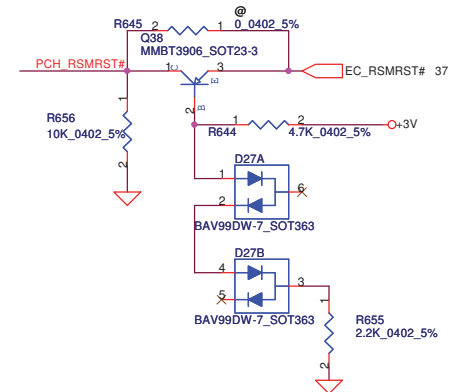
PM_SLP_S3# 37

PM_SLP_M# @ PAD T8

PM_SLP_DSW# @ PAD T29

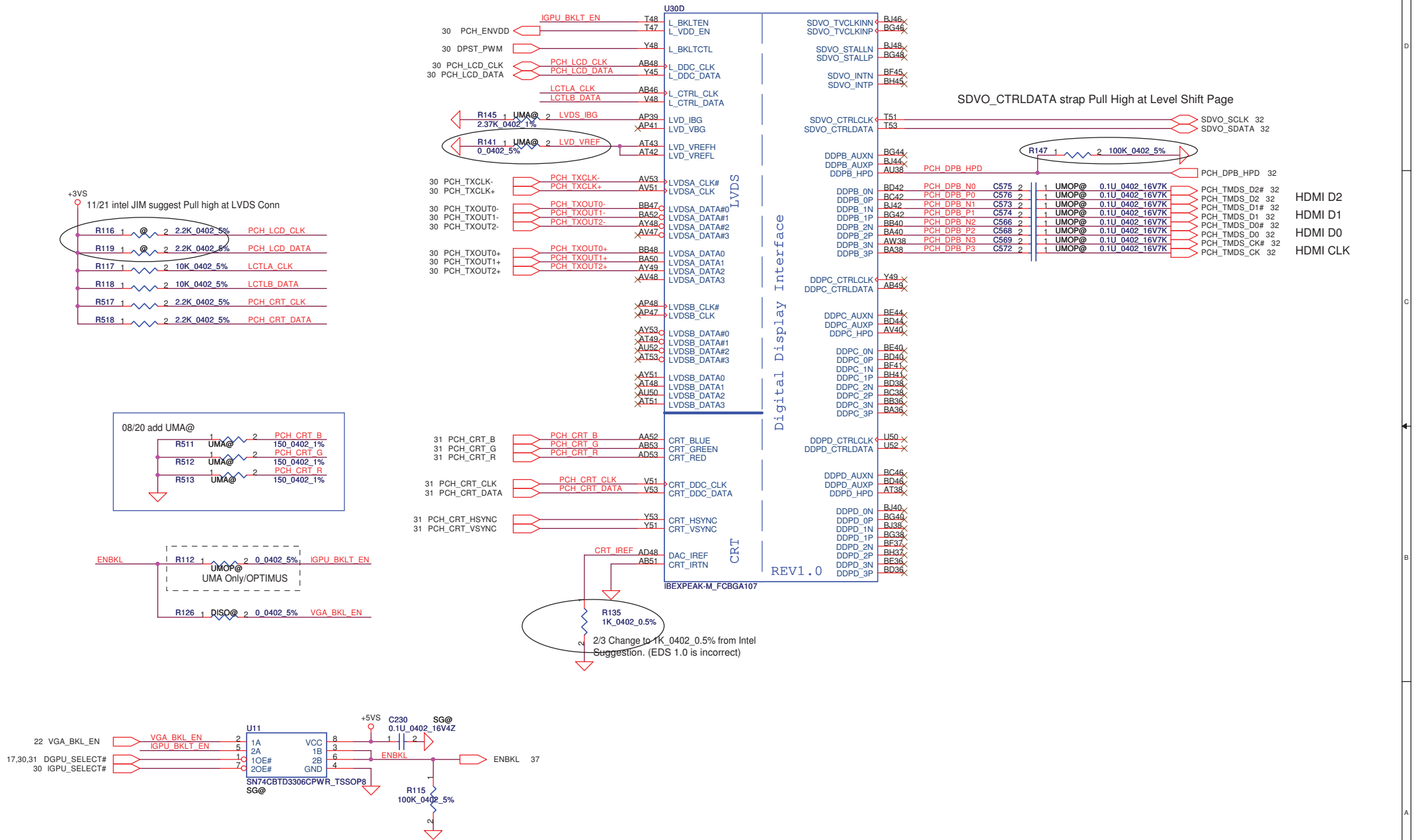
H_PM_SYNC 5

PM_SLP_LAN#

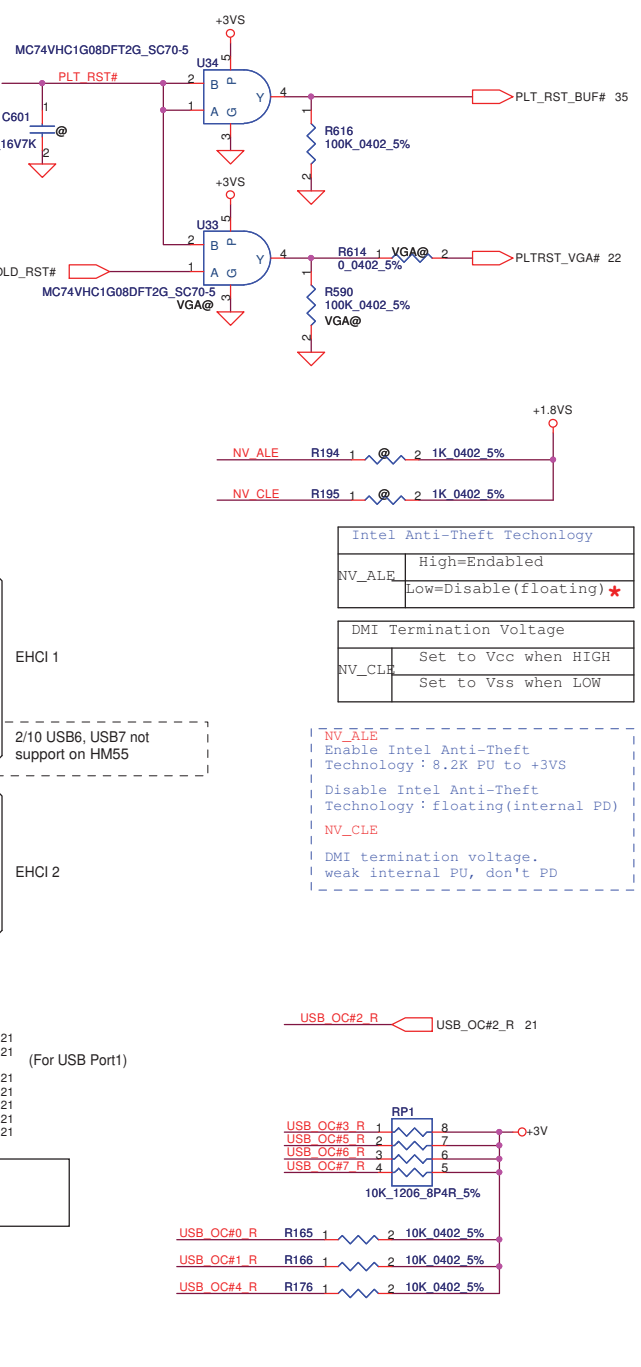
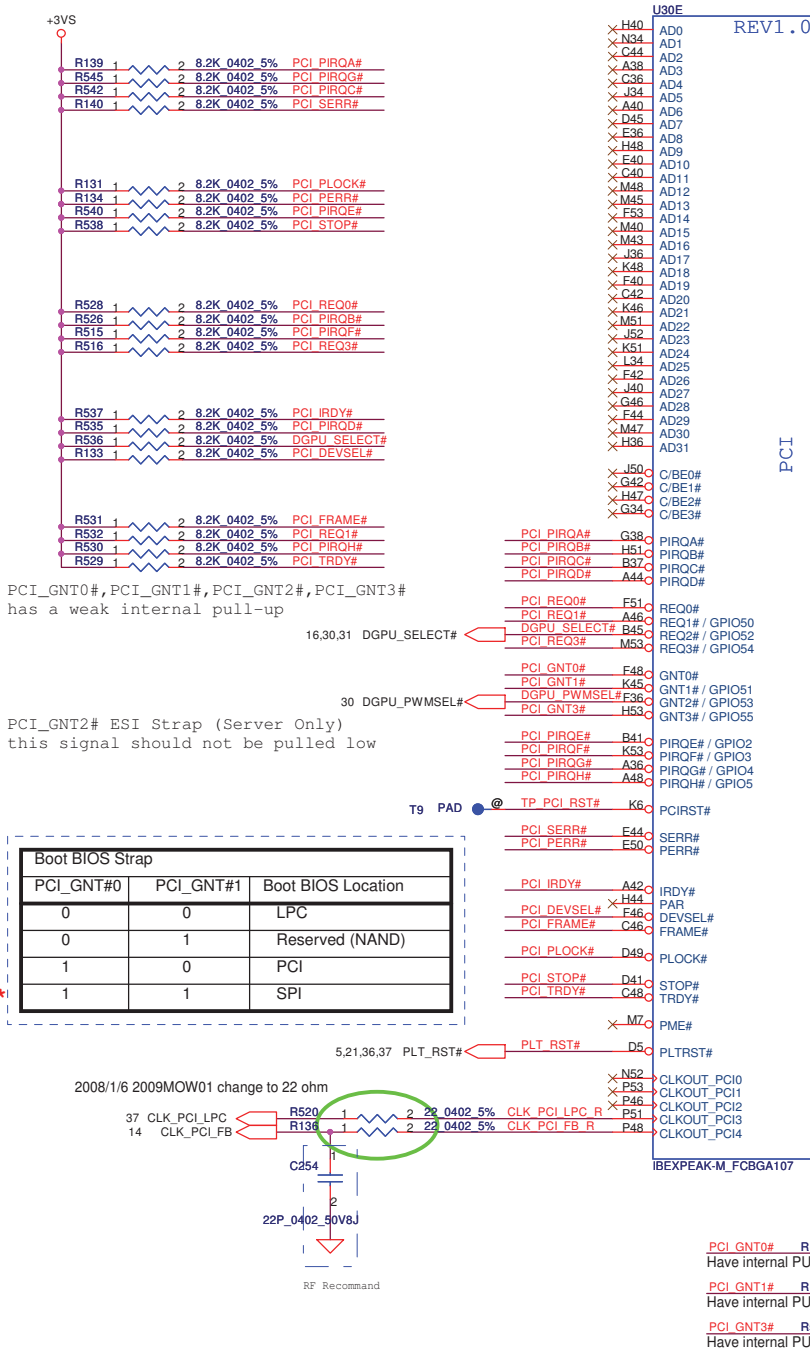


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Issued Date		2009/11/23		Deciphered Date		2010/11/23		Title			
								PCH (3/9) DMI, FDI, PM			
Size		Document Number		Customer		Date		Wednesday, April 21, 2010		Sheet 15 of 58	
								NELA0 M/B LA-6151P Schematic		Rev 1.0	

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				Customer	NELA0 M/B LA-6151P Schematic
				Date	Wednesday, April 21, 2010
				Sheet	16 of 58
				Rev	1.0

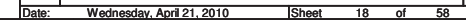


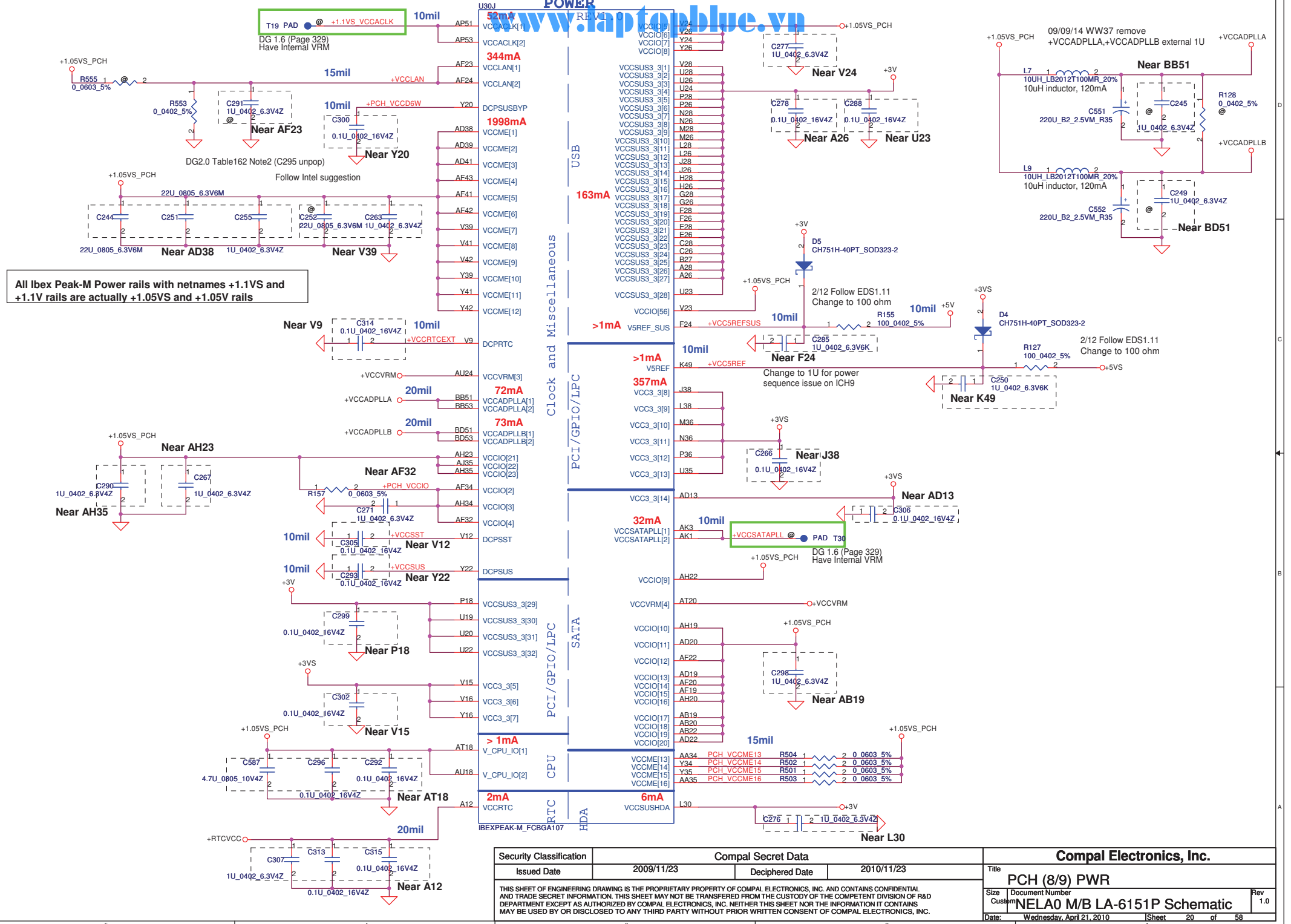
A16 swap override Strap/Top-Block Swap Override jumper

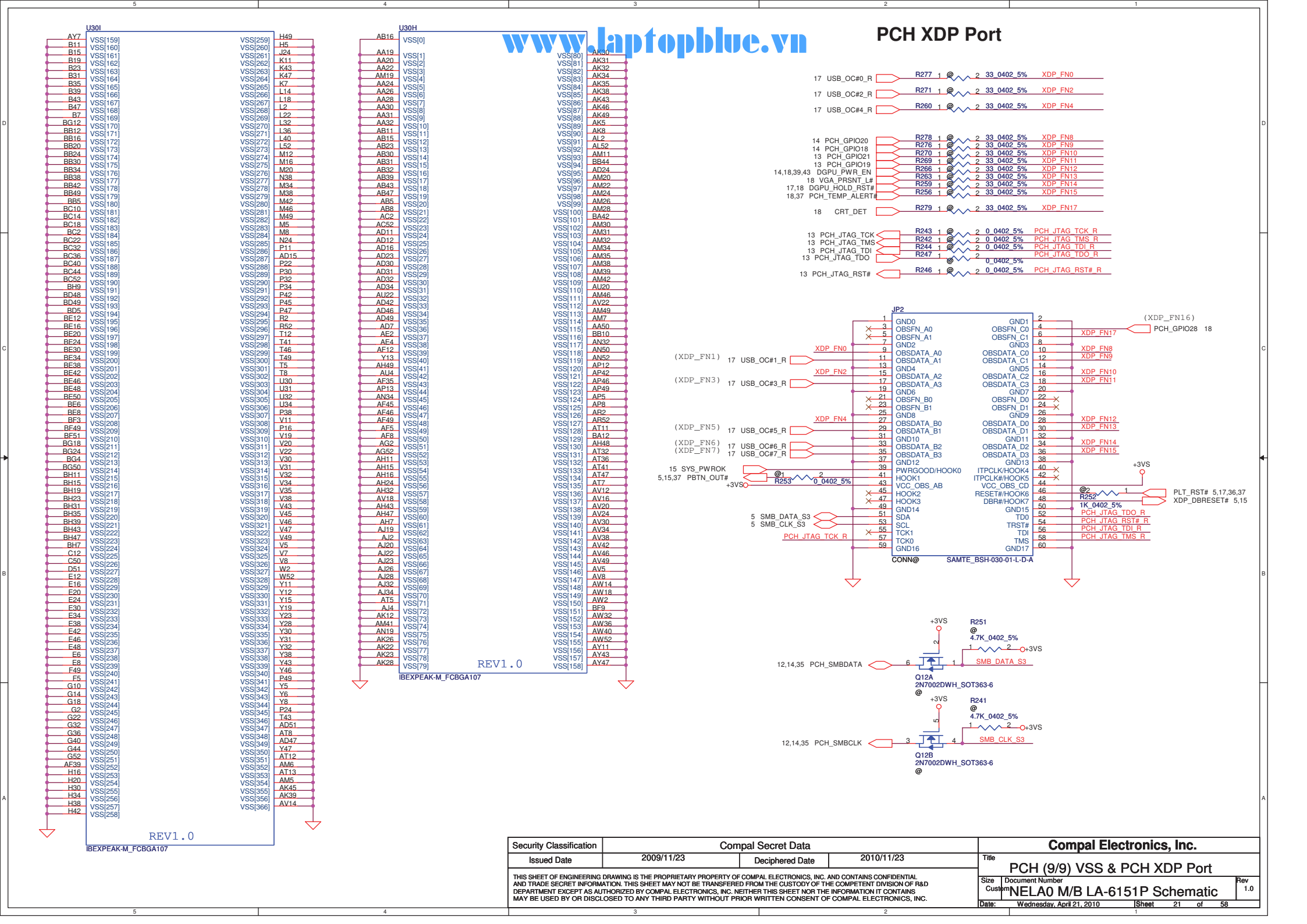
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled
	High=Default *

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Compal Electronics, Inc.			
Title PCH (5/9) PCI, USB, VRAM			
Size Customer	Document Number NELA0 M/B LA-6151P Schematic		Rev 1.0
Date	Wednesday, April 21, 2010	Sheet	17 of 58







GPIO

PCI EXPRESS

DVO

CLK

I2C

DACS

CRT

LVDS

I2C

DACS

CRT

LVDS

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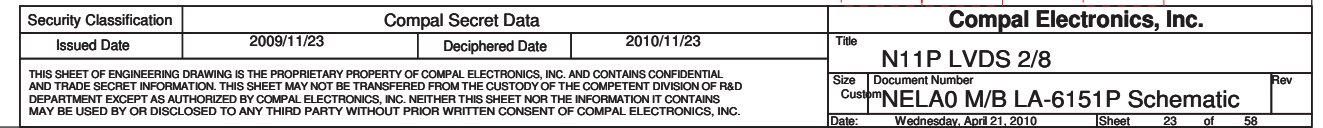
I2C

DACS

CRT

LVDS

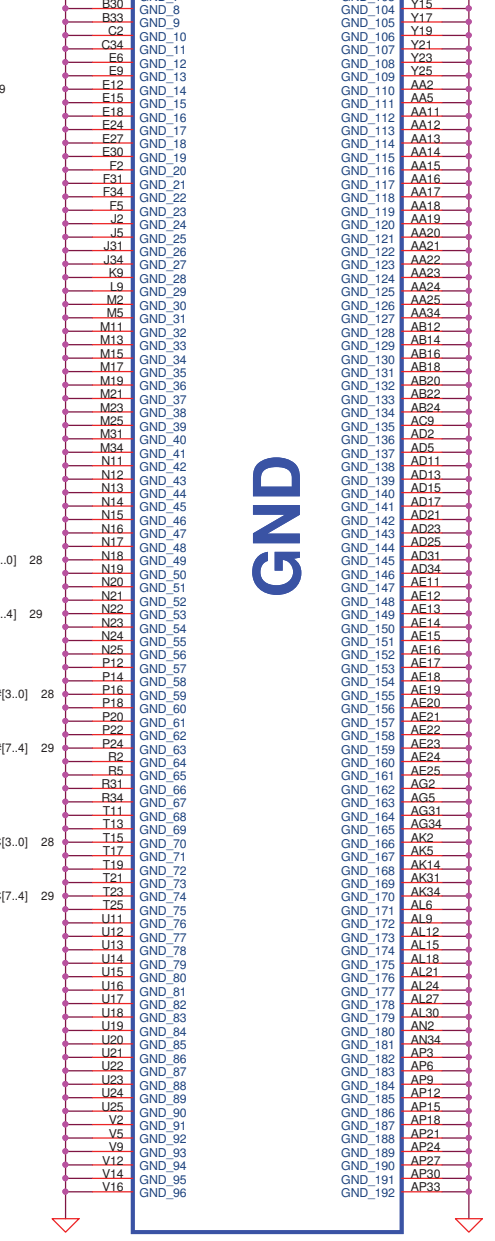
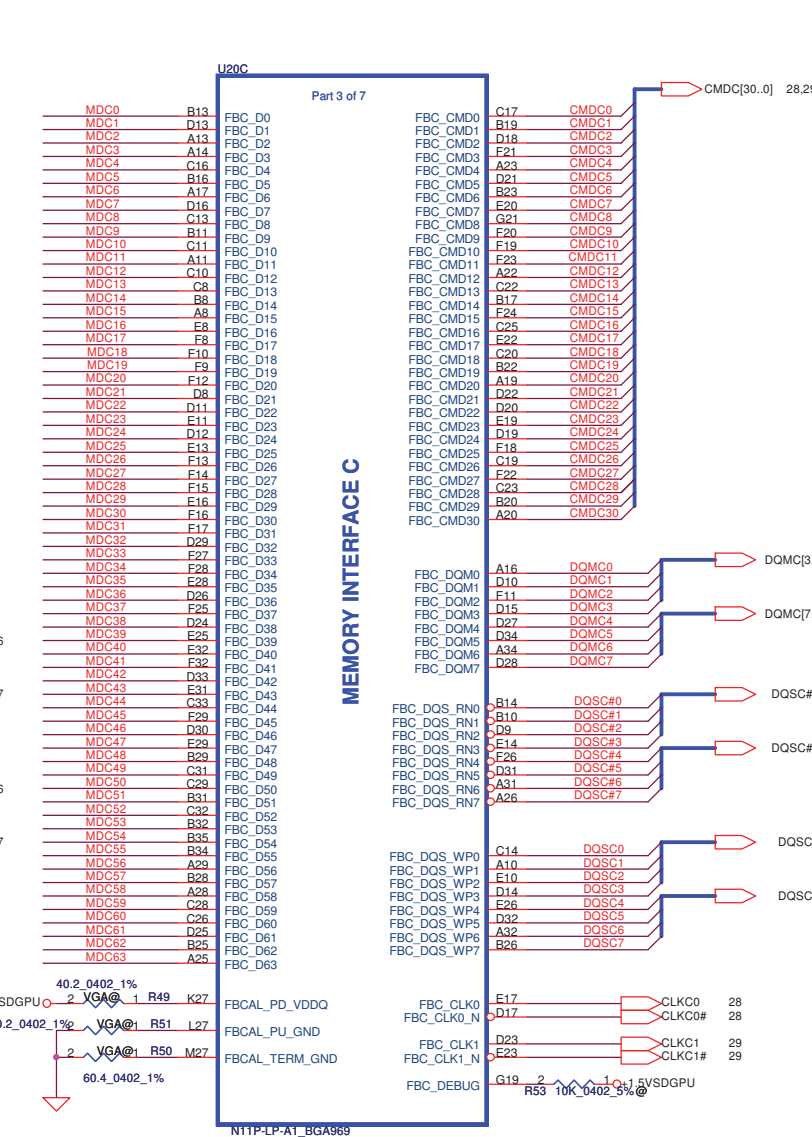
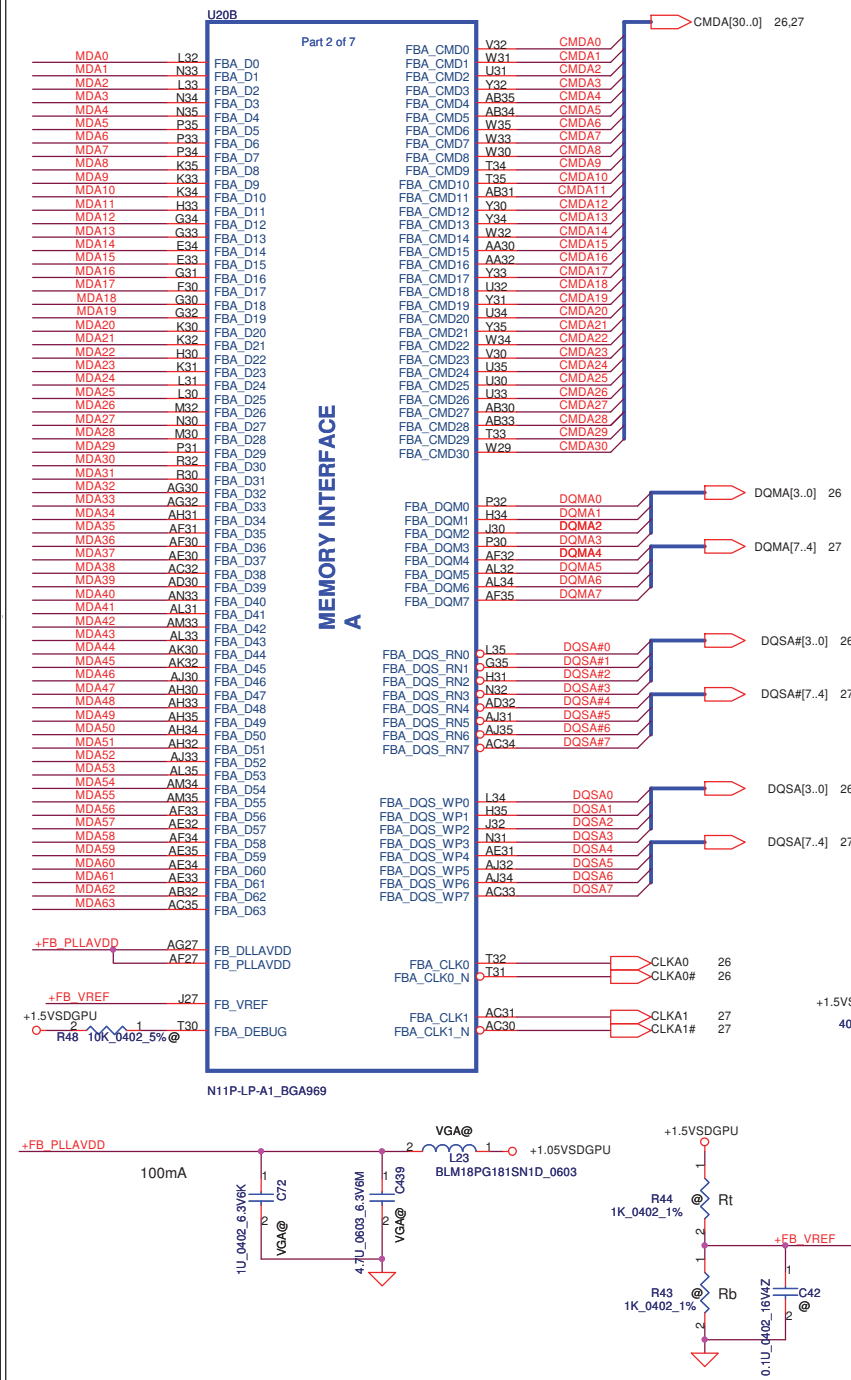
I2C





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						Size	Document Number				Rev
						Custom	NELA0 M/B LA-6151P Schematic				1.0
						Date:	Wednesday, April 21, 2010		Sheet	24	of 58

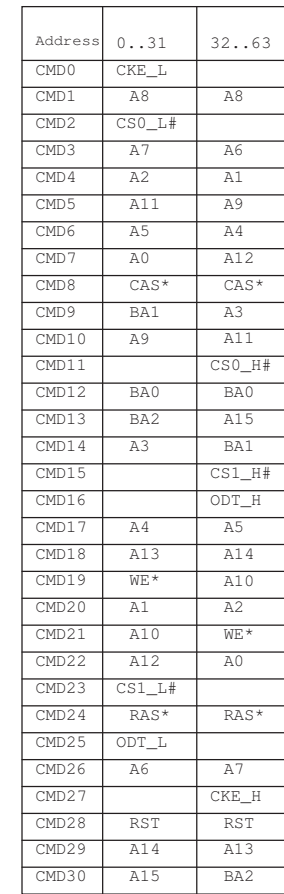
VRAM Interface



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				Date: Wednesday, April 21, 2010	Rev 1.0
				Sheet 25	of 58

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N11P LP1:64Mx16 DDR3 *8==>1GB



LOW HIGH

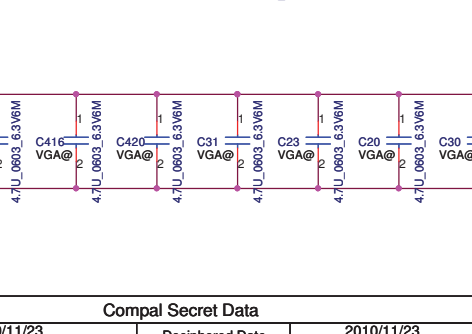
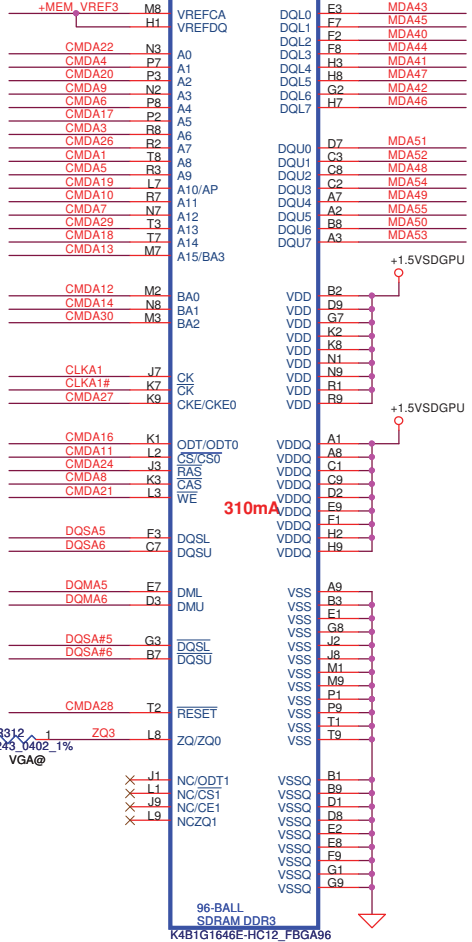
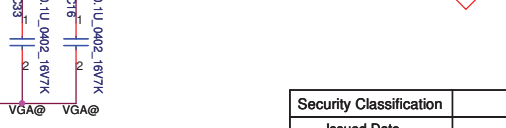
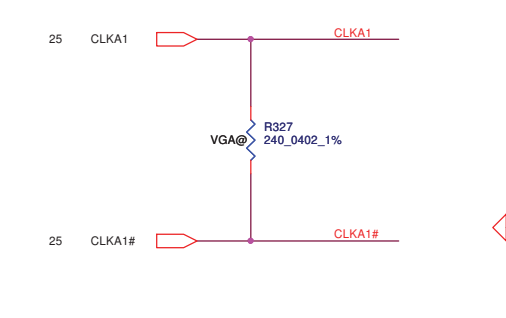
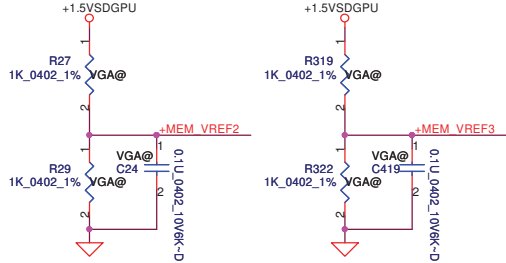
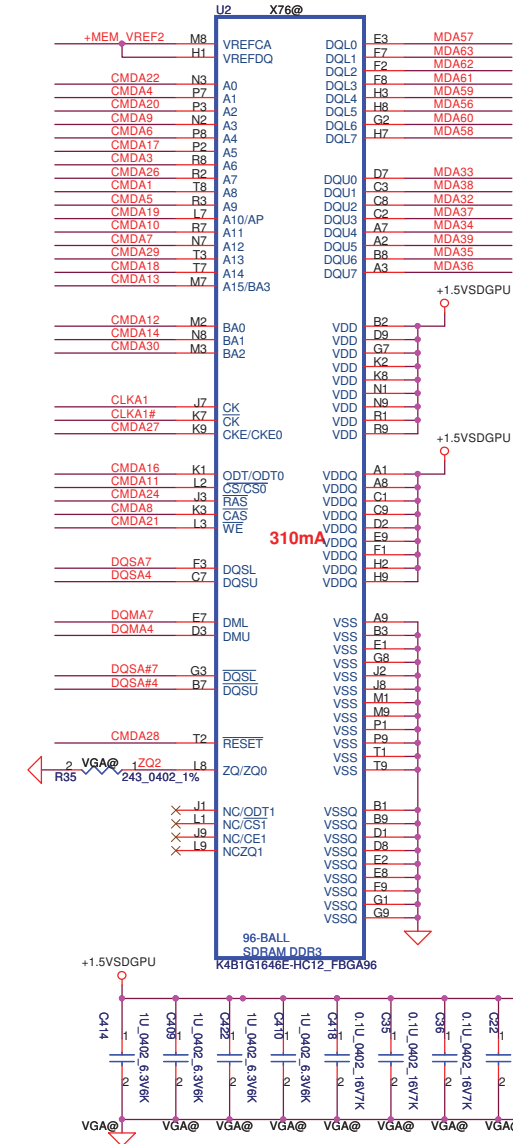
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *4==>512MB N11M GE2 :128Mx16 DDR3 *4==>1GB



64Mx16 DDR3 *8==>1GB

- 25,26 DQMA[7..0] DQMA[7..0]
- 25,26 CMDA[30..0] CMDA[30..0]
- 25,26 DQSA# [7..0] DQSA# [7..0]
- 25,26 DQSA[7..0] DQSA[7..0]
- 25,26 MDA[63..0] MDA[63..0]



Address	0...31	32...63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0_L#	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS*	CAS*
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0_H#
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1_H#
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE*	A10
CMD20	A1	A2
CMD21	A10	WE*
CMD22	A12	A0
CMD23	CS1_L#	
CMD24	RAS*	RAS*
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	
CMD29	A14	A13
CMD30	A15	BA2

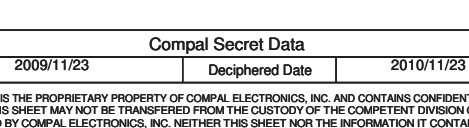
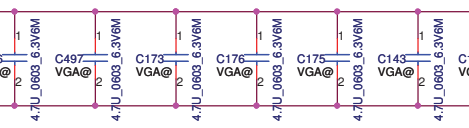
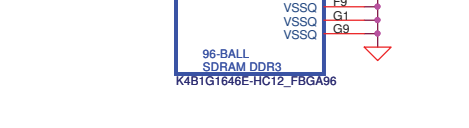
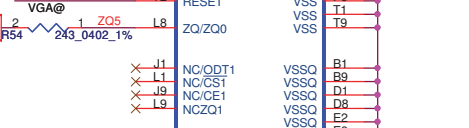
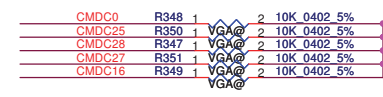
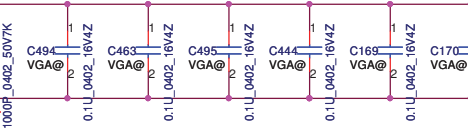
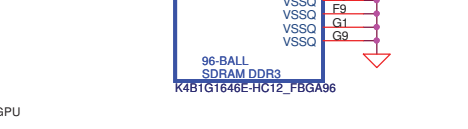
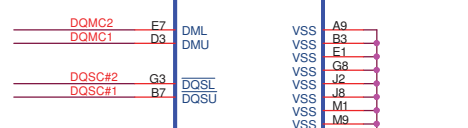
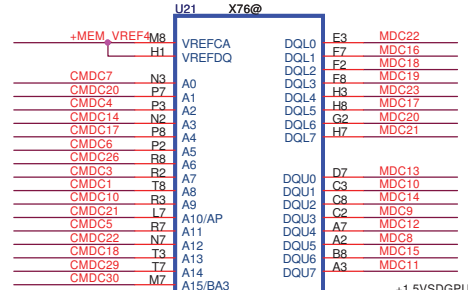
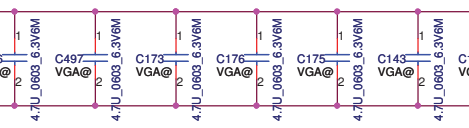
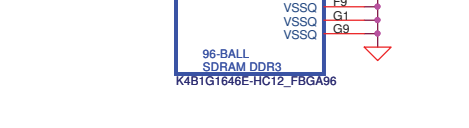
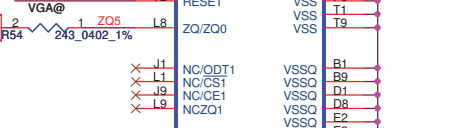
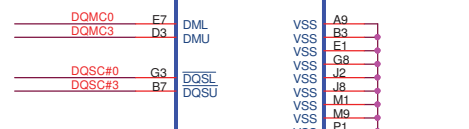
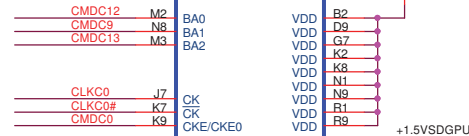
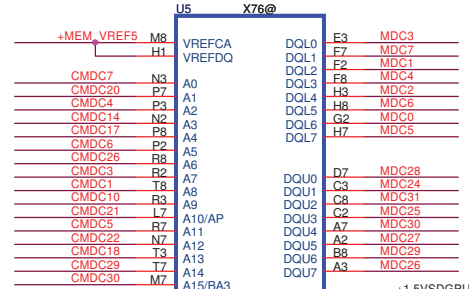
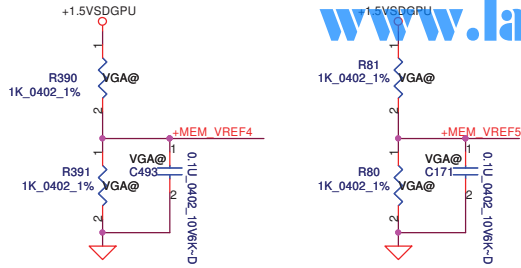
LOW HIGH

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

www.laptopblue.vn

25,29 DQSC[7..0] DQSC[7..0]
25,29 DQSC#[7..0] DQSC#[7..0]
25,29 DQMC[7..0] DQMC[7..0]
25,29 MDC[63..0] MDC[63..0]
25,29 CMDC[30..0] CMDC[30..0]



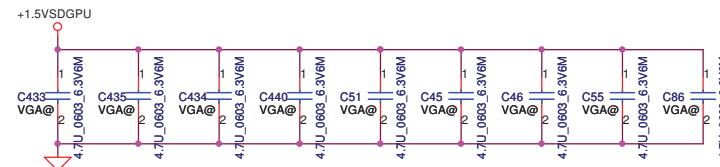
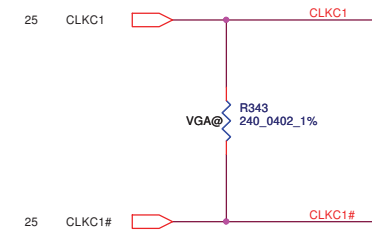
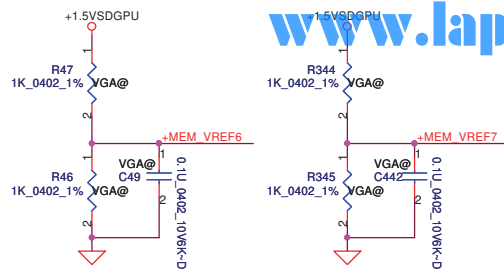
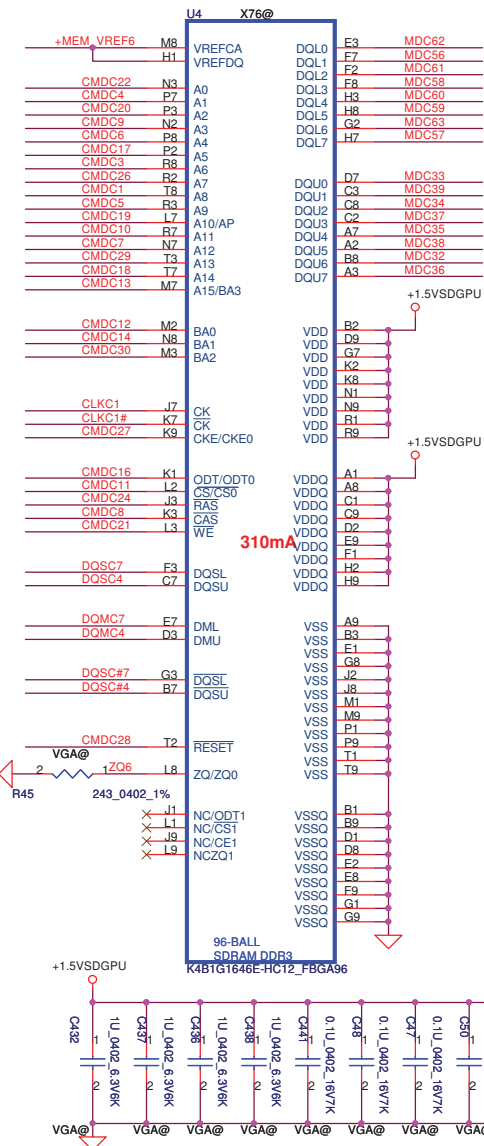
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0_L#	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS*	CAS*
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0_H#
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1_H#
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE*	A10
CMD20	A1	A2
CMD21	A10	WE*
CMD22	A12	A0
CMD23	CS1_L#	
CMD24	RAS*	RAS*
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

LOW HIGH

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Issued Date	2009/11/23	Deciphered Date	2010/11/23	Title	
				N11P DDR3 7/8	
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				Customer	
				Date	
				Wednesday, April 21, 2010	
				Sheet	
				28 of 58	

64Mx16 DDR3 *8==>1GB

5,28	DQMC[7..0]		DQMC[7..0]
5,28	CMDC[30..0]		CMDC[30..0]
25,28	DQSC#[7..0]		DQSC#[7..0]
25,28	DQSC[7..0]		DQSC[7..0]
5,28	MDC[63..0]		MDC[63..0]



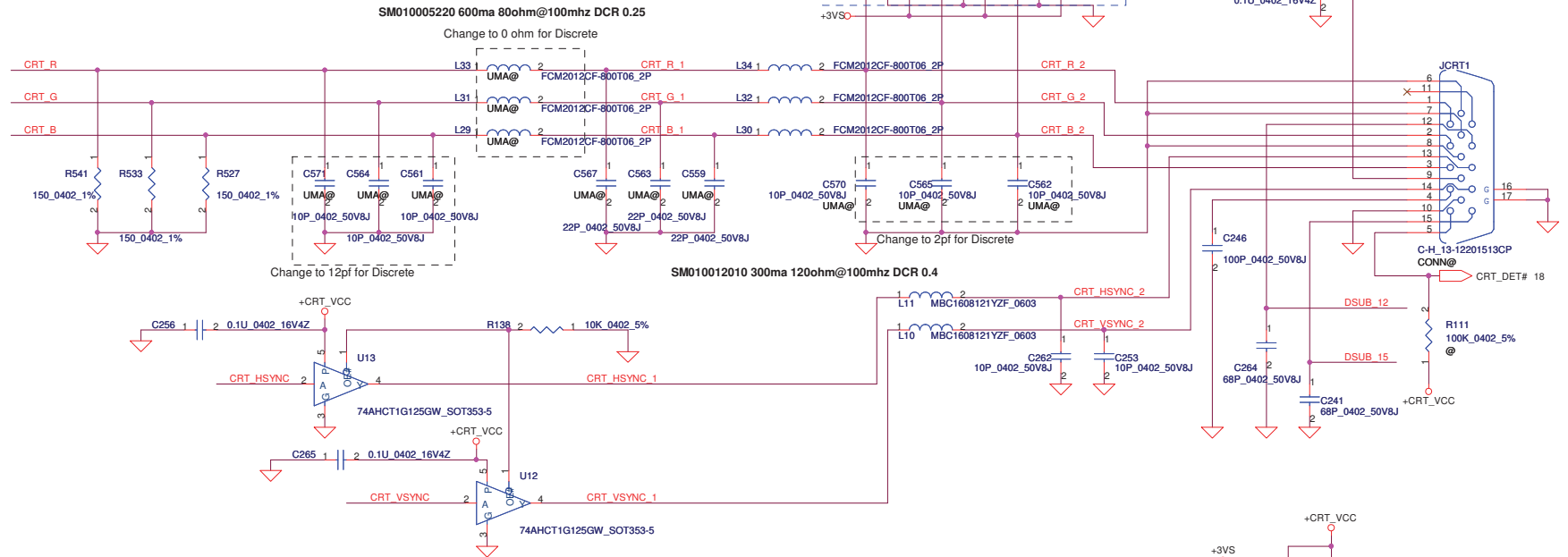
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CMD1	A8	A8
CMD2	CS0_L#	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS*	CAS*
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0_H#
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1_H#
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE*	A10
CMD20	A1	A2
CMD21	A10	WE*
CMD22	A12	A0
CMD23	CS1_L#	
CMD24	RAS*	RAS*
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

LOW HIGH

	1
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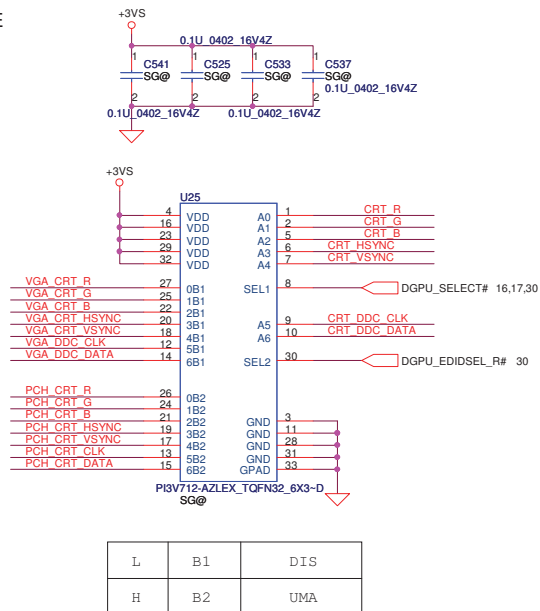
CRT Connector

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EMI suggestion
SC60000H00 change to SCA0000A00



SWITCHABLE

2009/08/27

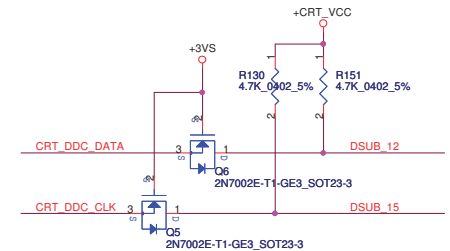


UMA Only & Optimus

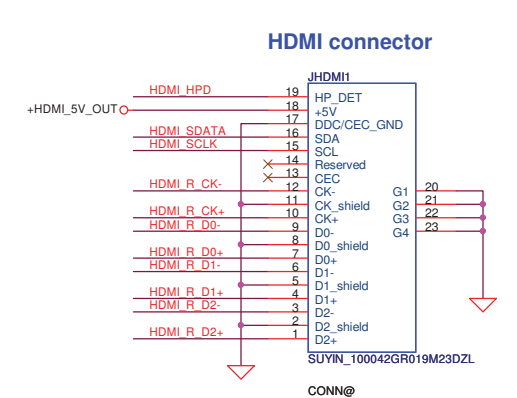
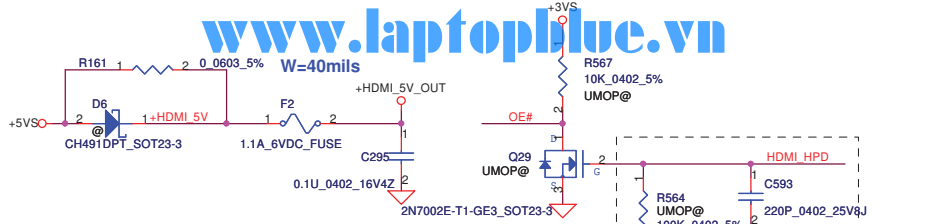
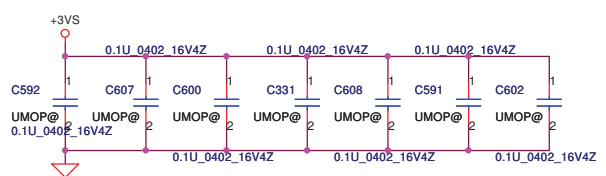
16	PCH_CRT_R	PCH CRT R	R493	2	UMOP	1	0.0402 5%	CRT_R
16	PCH_CRT_G	PCH CRT G	R494	2	UMOP	1	0.0402 5%	CRT_G
16	PCH_CRT_B	PCH CRT B	R495	2	UMOP	1	0.0402 5%	CRT_B
16	PCH_CRT_HSYNC	PCH CRT HSYNC	R496	2	UMOP	1	0.0402 5%	CRT_HSYNC
16	PCH_CRT_VSYNC	PCH CRT VSYNC	R497	2	UMOP	1	0.0402 5%	CRT_VSYNC
16	PCH_CRT_CLK	PCH CRT CLK	R485	2	UMOP	1	0.0402 5%	CRT_DDC_CLK
16	PCH_CRT_DATA	PCH CRT DATA	R479	2	UMOP	1	0.0402 5%	CRT_DDC_DATA

Discrete only

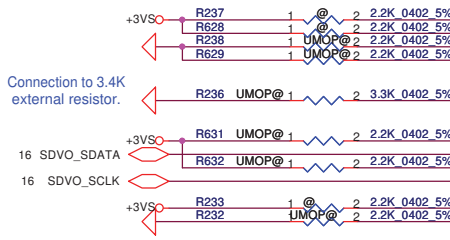
22	VGA_CRT_R	VGA CRT R	R455	2	DISO	1	0.0402 5%	CRT_R
22	VGA_CRT_G	VGA CRT G	R456	2	DISO	1	0.0402 5%	CRT_G
22	VGA_CRT_B	VGA CRT B	R457	2	DISO	1	0.0402 5%	CRT_B
22	VGA_CRT_HSYNC	VGA CRT HSYNC	R458	2	DISO	1	0.0402 5%	CRT_HSYNC
22	VGA_CRT_VSYNC	VGA CRT VSYNC	R459	2	DISO	1	0.0402 5%	CRT_VSYNC
22	VGA_DDC_CLK	VGA DDC CLK	R488	2	DISO	1	0.0402 5%	CRT_DDC_CLK
22	VGA_DDC_DATA	VGA DDC DATA	R482	2	DISO	1	0.0402 5%	CRT_DDC_DATA



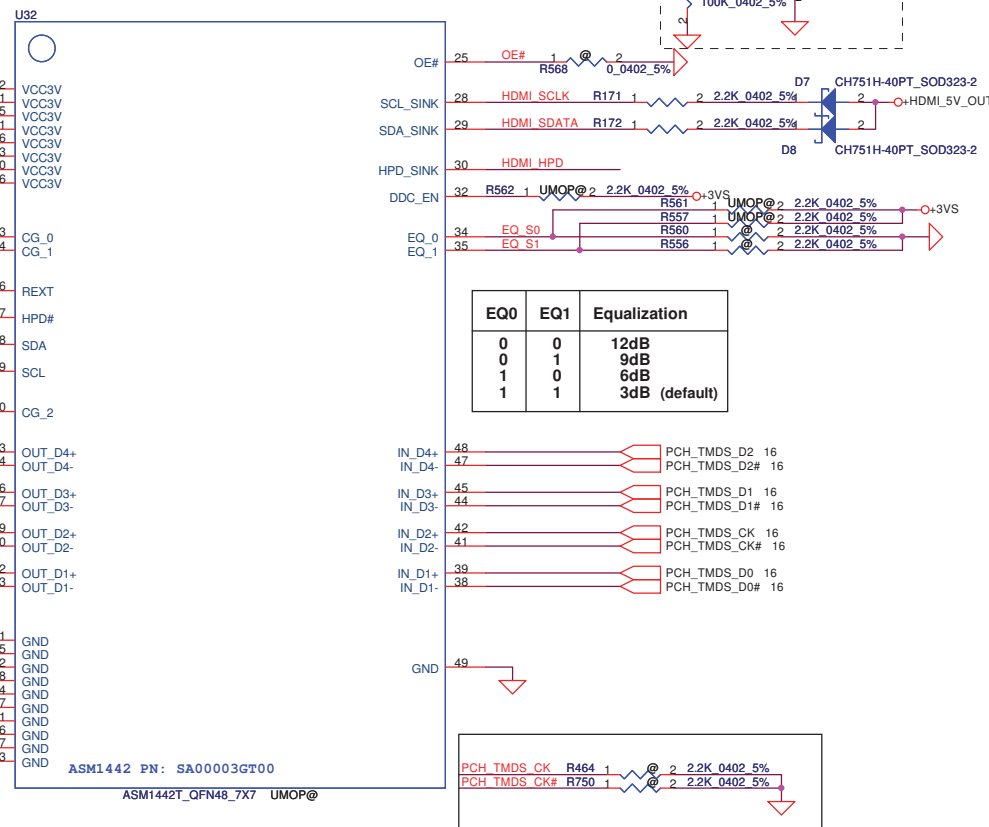
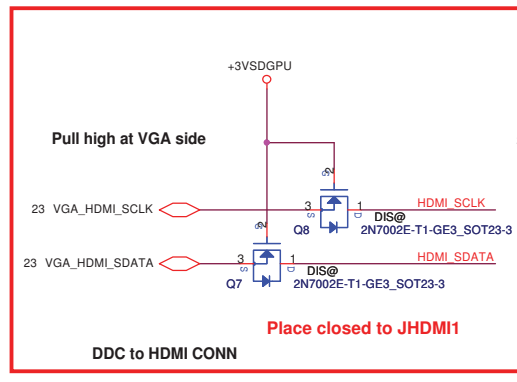
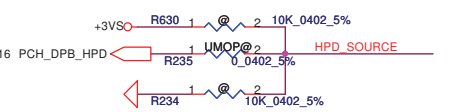
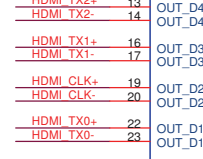
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/11/23	Deciphered Date	2010/11/23	Title	
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Size	B	Document Number	NELA0 M/B LA-6151P Schematic	Rev	1.0
Date	Wednesday, April 21, 2010	Sheet	31	of	58



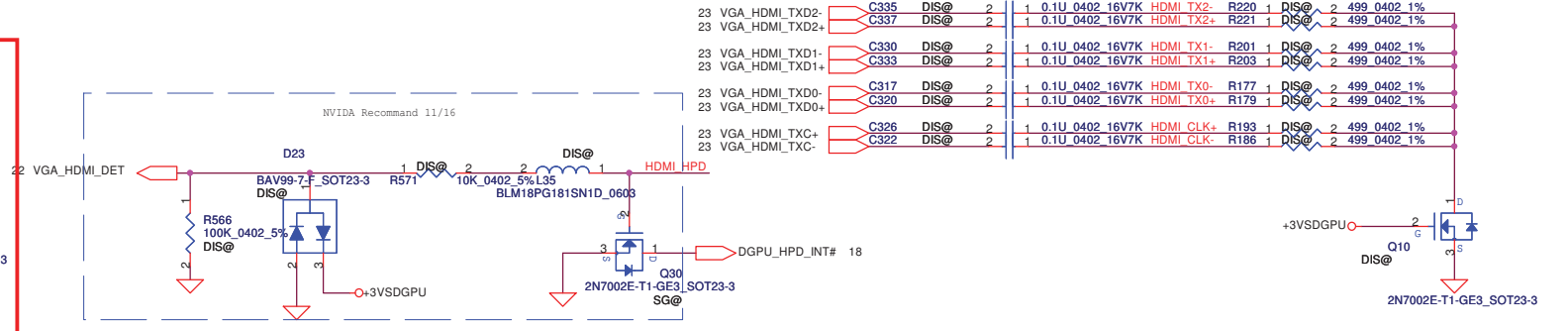
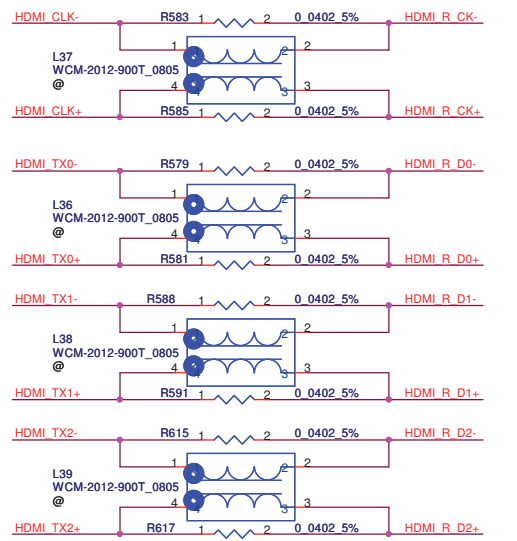
Vendor Recommend : CFG SETTING 000



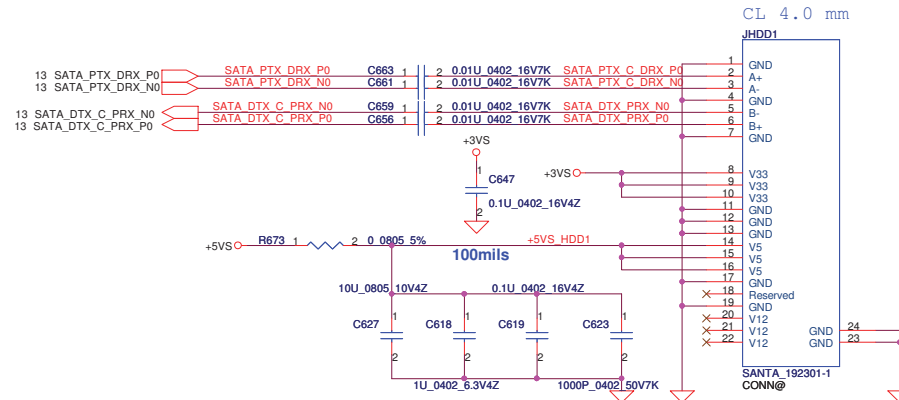
CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0



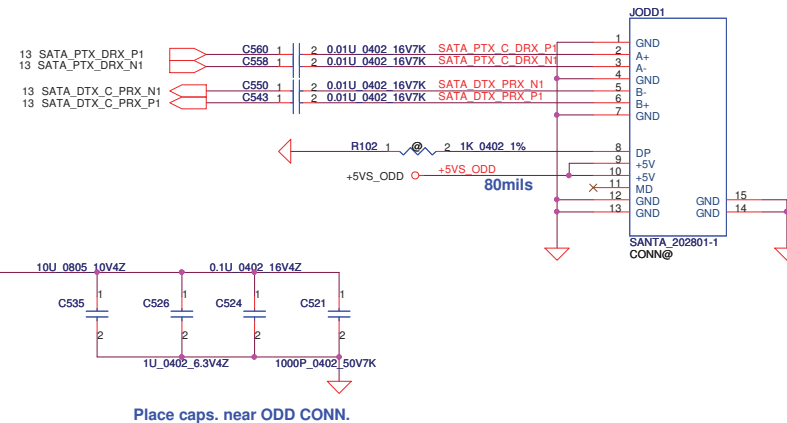
SM070001310 400ma 90ohm@100mhz DCR 0.3



SATA HDD1 Conn.



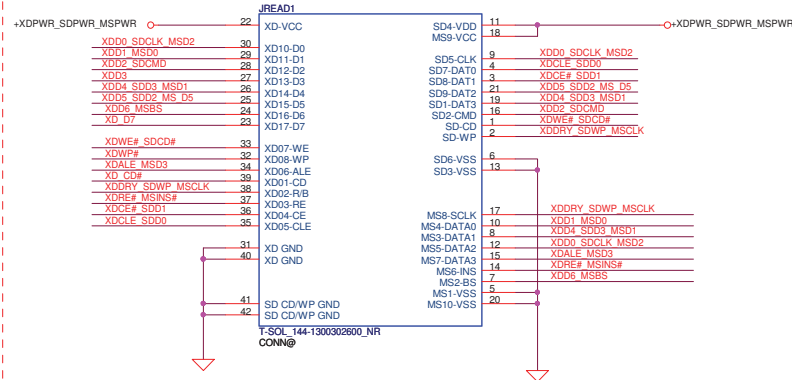
SATA ODD Conn.

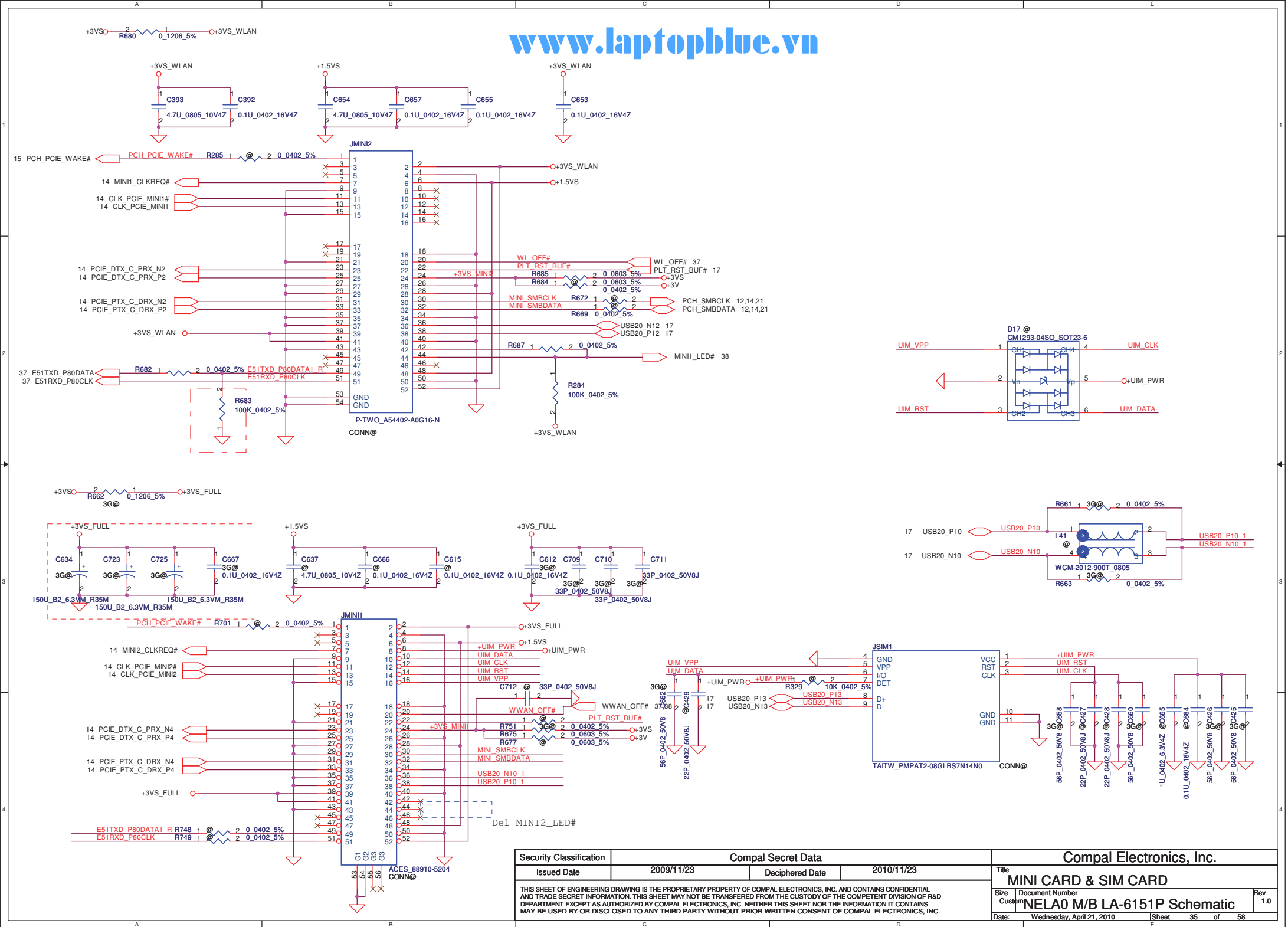


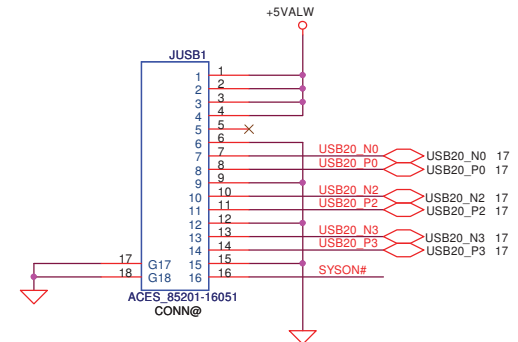
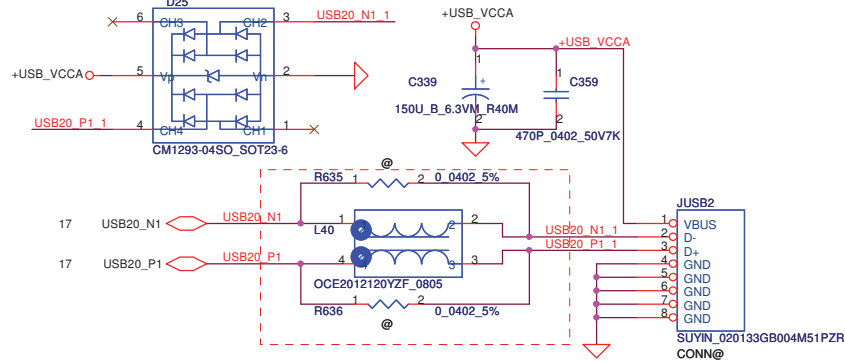
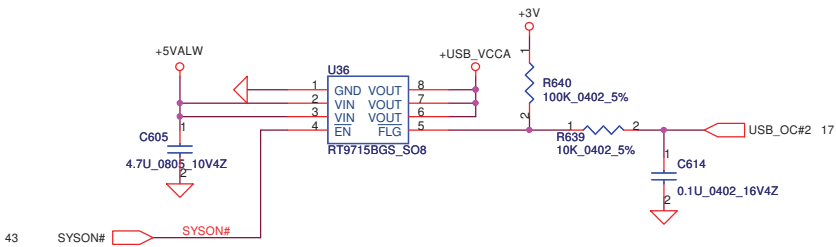
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/11/23	Deciphered Date	2010/11/23	Title	HDD & ODD Connector
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				Customer	1.0
				Date	Wednesday, April 21, 2010
				Sheet	33 of 58

Card Reader Connector

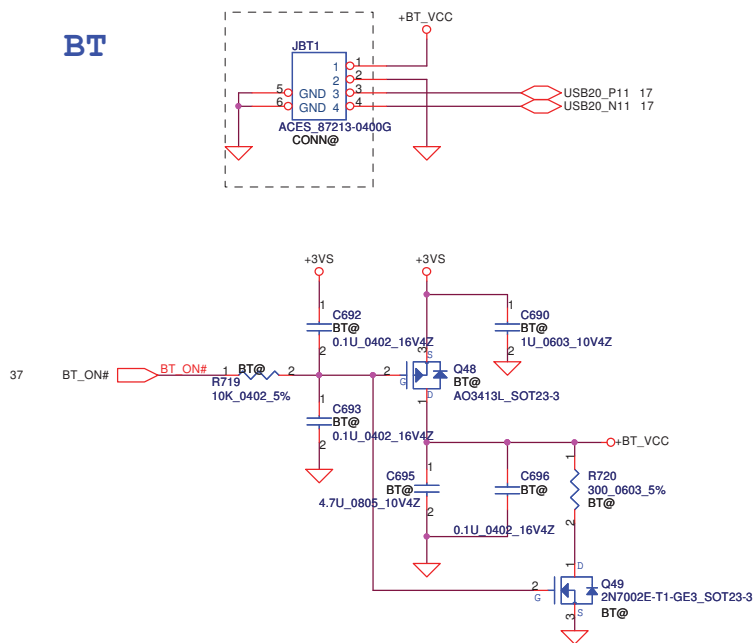
Card Reader Connector



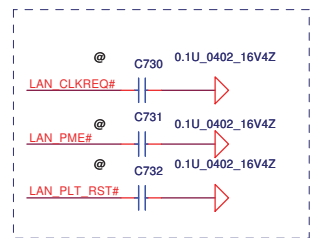
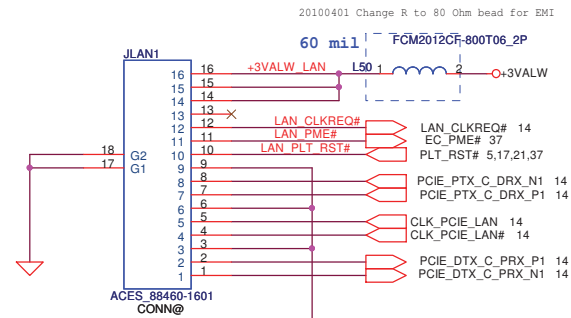




BT



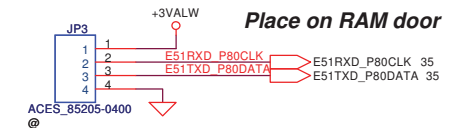
LAN CONN.



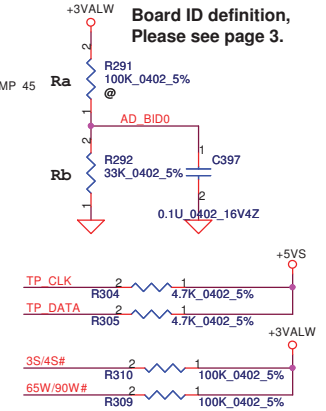
EMI request:
close to conn side

CONFIRM LAN CON.

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Size	Document Number	Customer		Rev	
1	NELA0 M/B LA-6151P Schematic	1.0		Date: Wednesday, April 21, 2010	
Sheet		36		of 58	

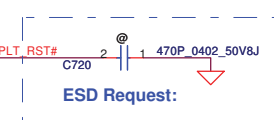
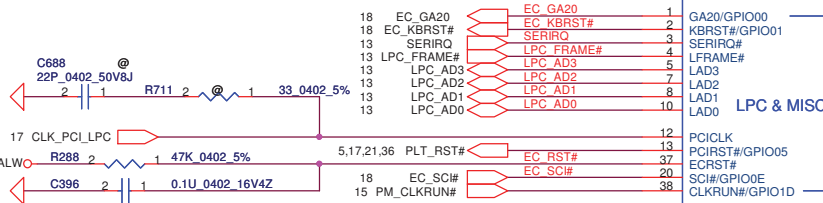
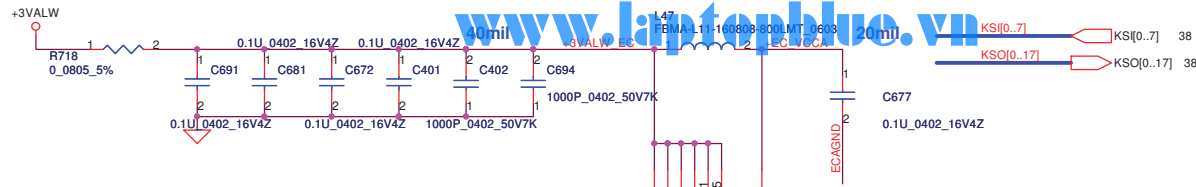
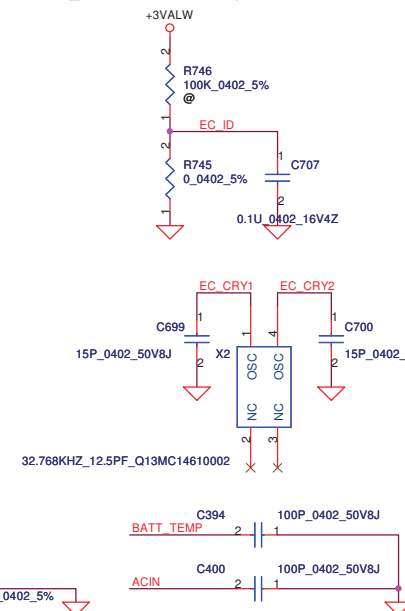


Board ID definition,
Please see page 3.

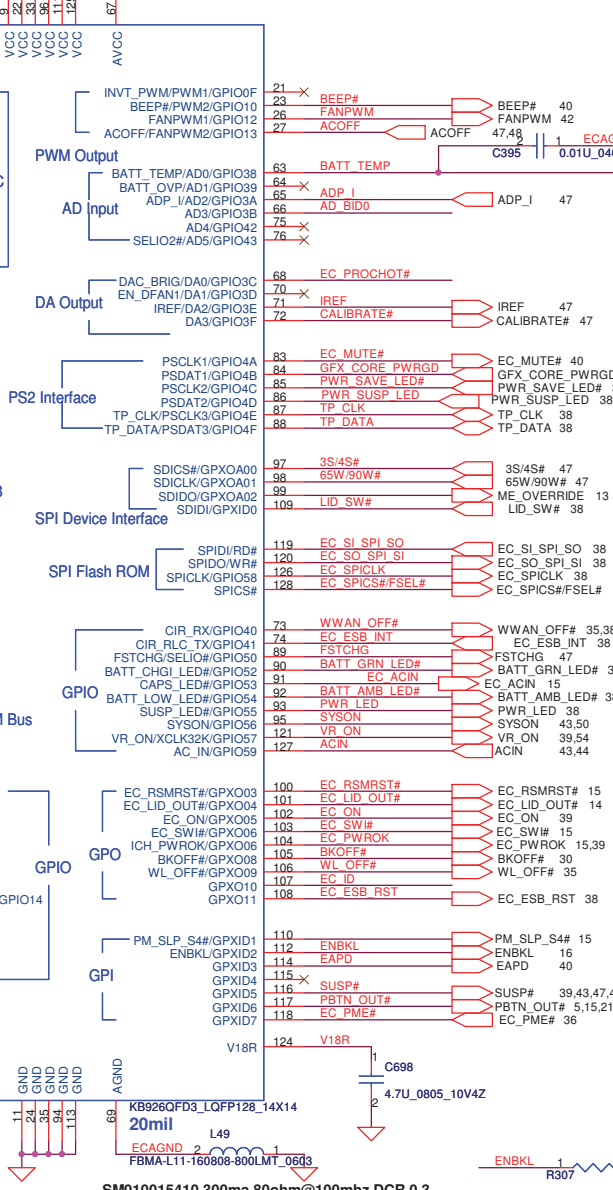
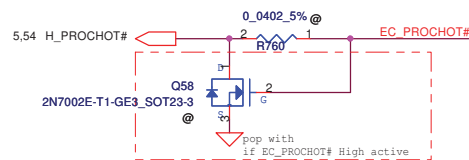
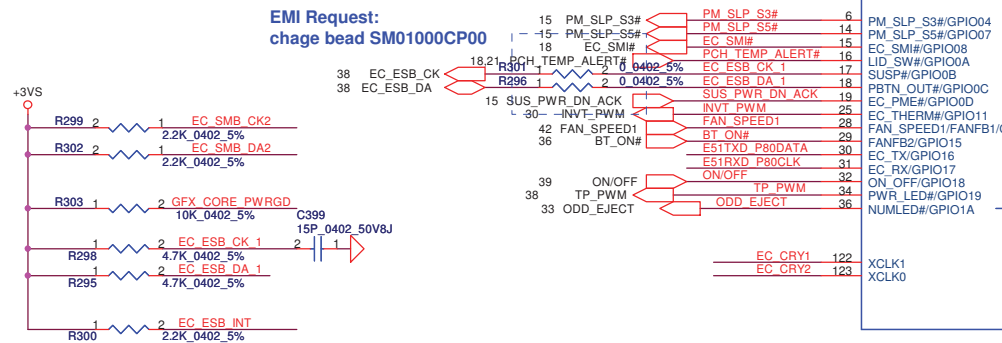


PCH_TEMP_ALERT# Pull high at Page 18 (PCH side)

EC_ID: HIGH is D3 ; LOW is E0

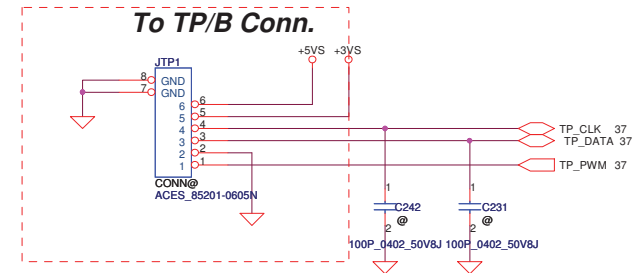
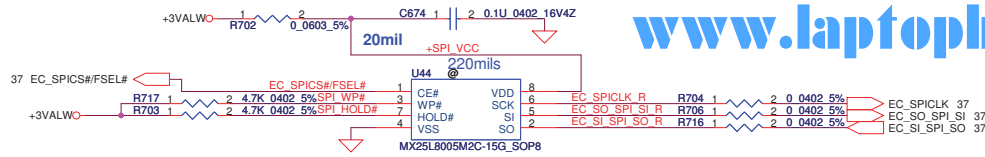


EMI Request:
change bead SM01000CP00

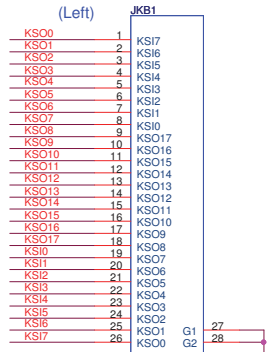


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Issued Date				2009/11/23				EC ENE KB926			
Deciphered Date				2010/11/23				NELA0 M/B LA-6151P Schematic			
Title				Size B				Date: Wednesday, April 21, 2010			
Document Number				Rev 1.0				Sheet 37 of 58			

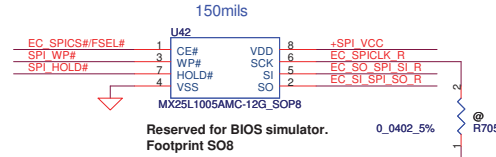
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INT_KBD Conn.



KSI0..7] KSI[0..7] 37
KSI0..17] KSI[0..17] 37

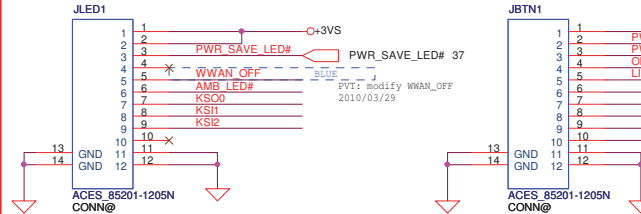


Reserved for BIOS simulator.
Footprint SO8

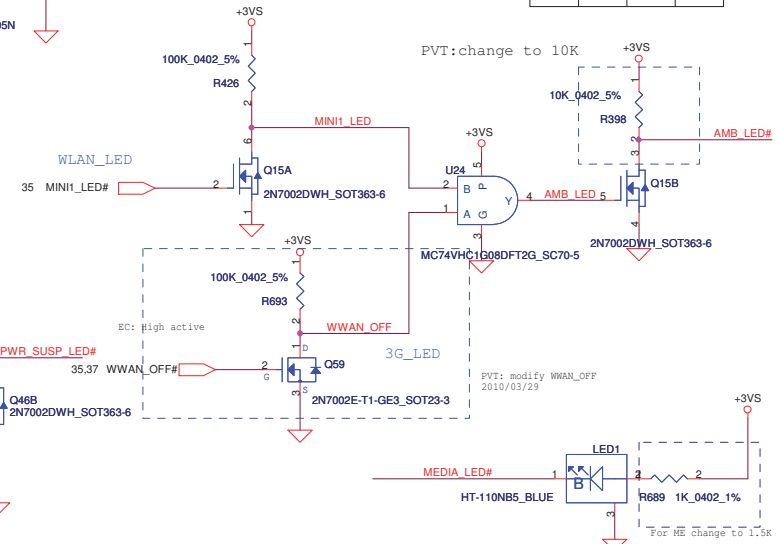
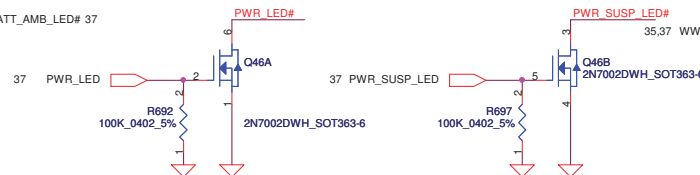
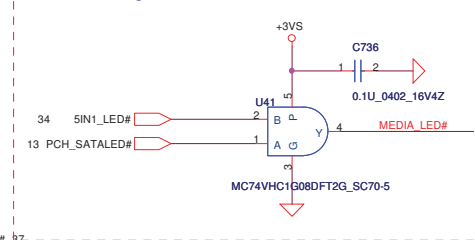
KSO0	
KSI1	PWR SAVE BTN
KSI2	Communication BTN
KSI3	
KSI4	

LED/B LEFT

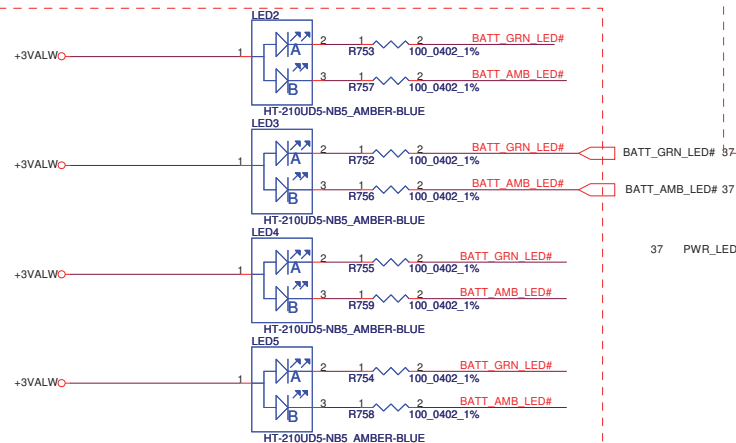
PWR/B RIGHT



20100331 change mos to AND

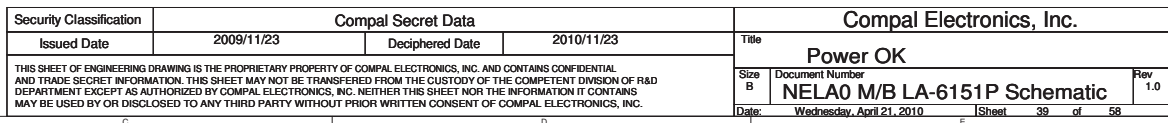


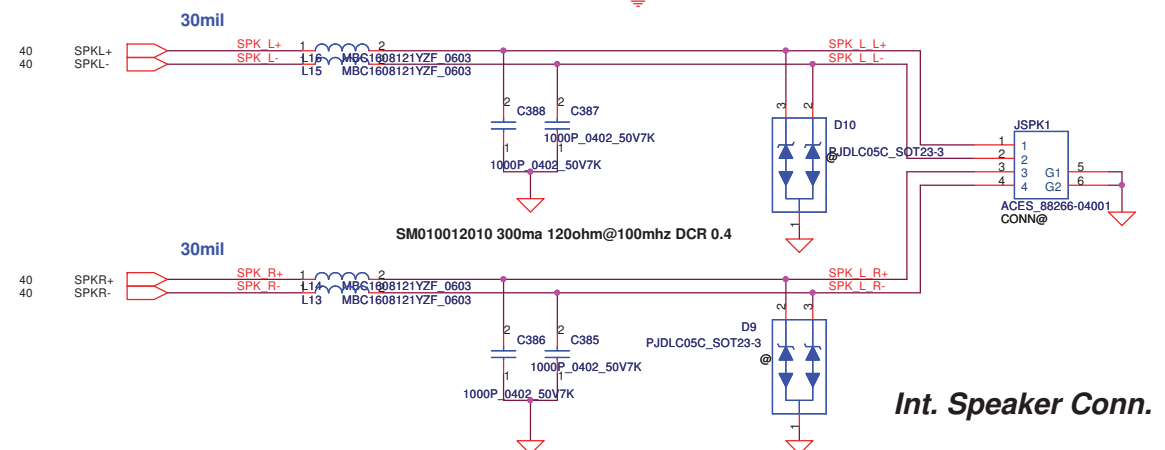
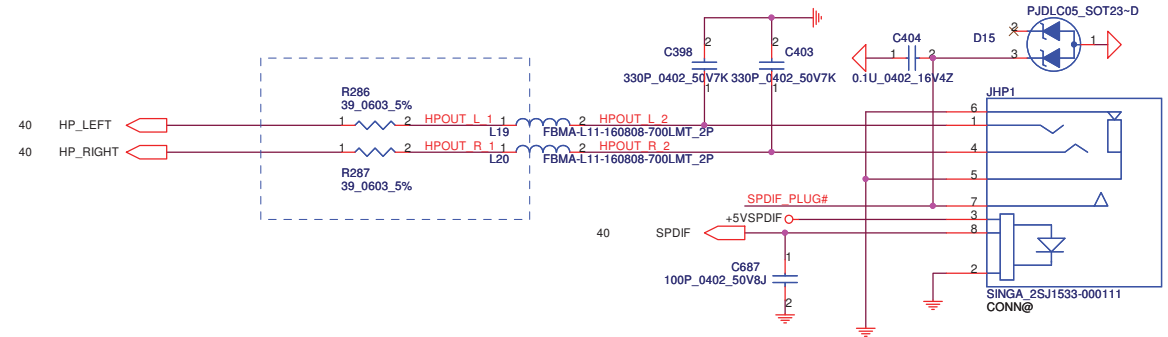
WLAN	3G	AMB	BLUE
L	L	H	L
H	L	H	L
L	H	L	H
H	H	H	H



For ME change to 100 ohm

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				Sheet				38 of 58			
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				NELA0 M/B LA-6151P Schematic							





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				Customer	NELA0 M/B LA-6151P Schematic	1.0
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2009/12/18

40mil

ACES_85205-0400
CONN@

37 FAN_SPEED1

37 FANPWM

+5V

+3V

+VCC_FAN1

R417 0.0603_5%

R429 10K_0402_5%

C500 10U_0805_10V4Z

C515 1000P_0402_50V7K

C516 1000P_0402_50V7K

C518 10U_0805_10V4Z

D18 1SS355_SOD323-2

D19 BAS16_SOT23-3

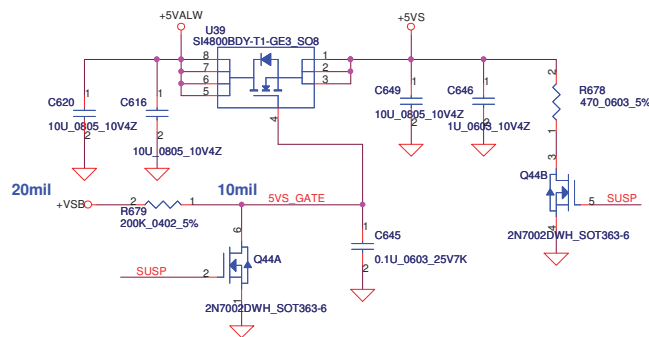
JFAN1

1 2 3 4

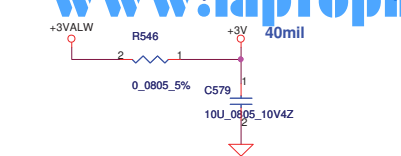
1 2 3 4

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Issued Date	2009/11/23	Deciphered Date	2010/11/23	Title FAN & Screw Hole		
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				NELA0 M/B LA-6151P Schematic		
				Date: Wednesday, April 21, 2010	Sheet 42 of 58	

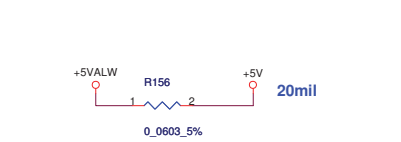
+5VALW TO +5VS



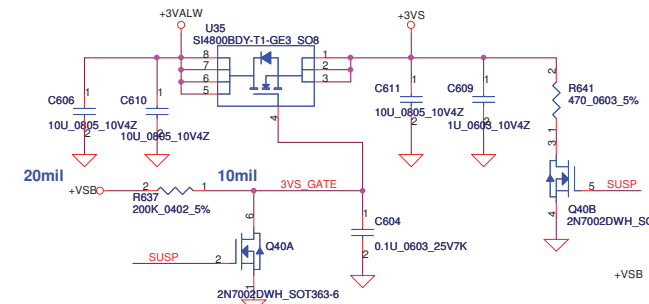
+3VALW TO +3V(PCH AUX Power)



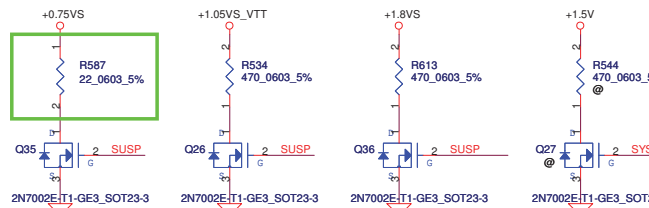
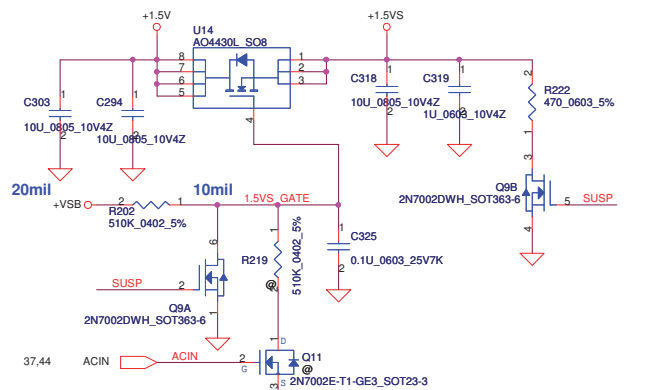
+5VALW TO +5V(PCH AUX Power)



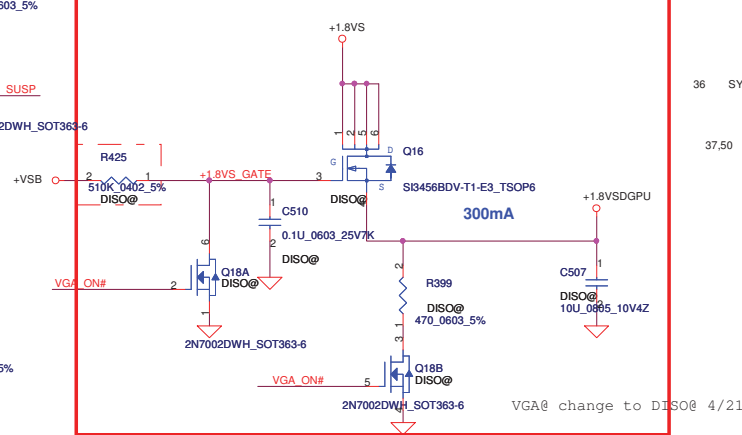
+3VALW TO +3VS



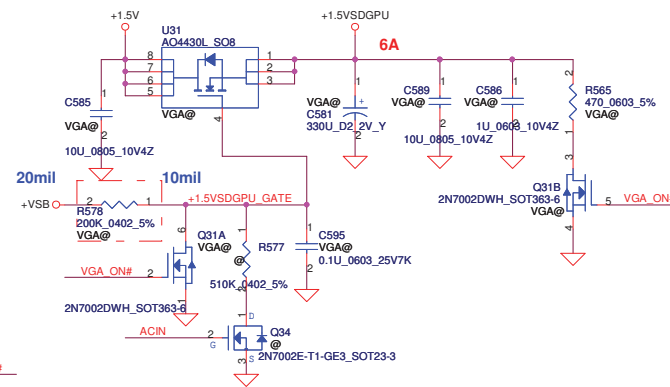
+1.5V to +1.5VS



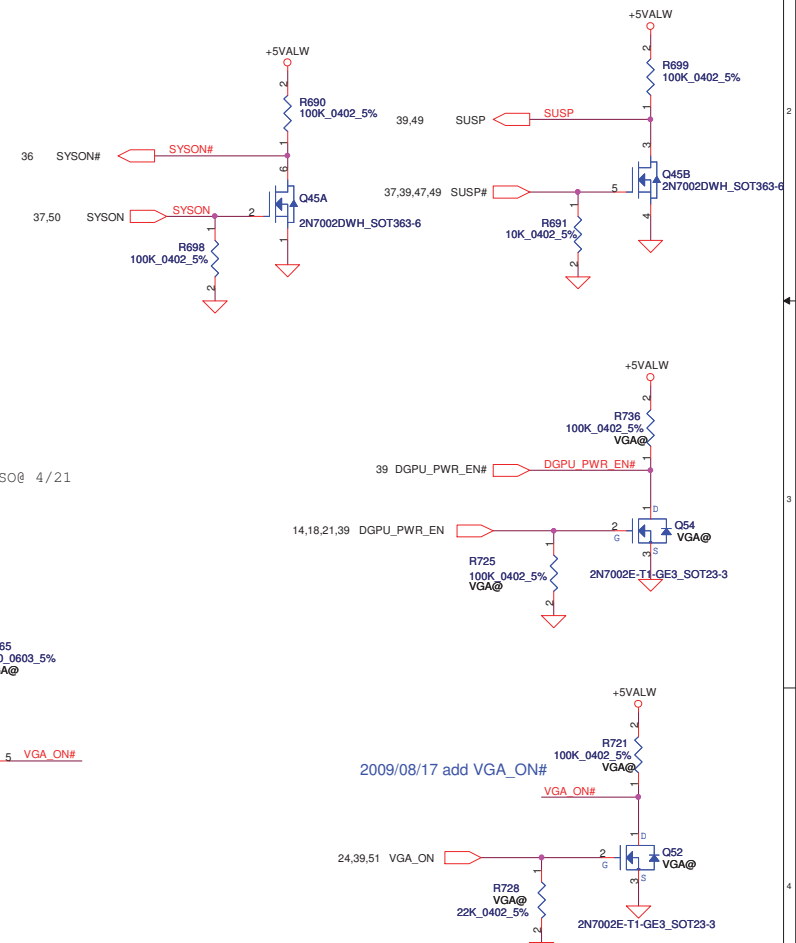
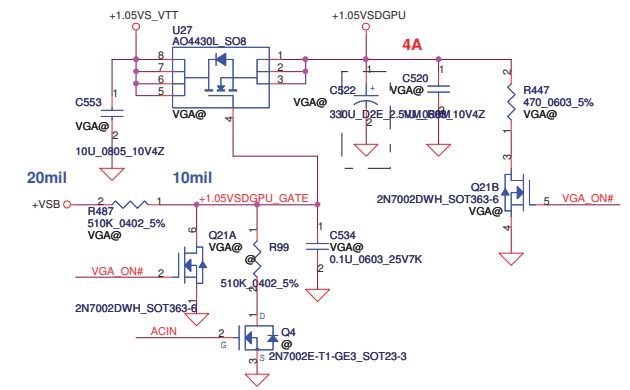
+1.8VS to +1.8VSDGPU for GPU



+1.5V to +1.5VSDGPU for GPU

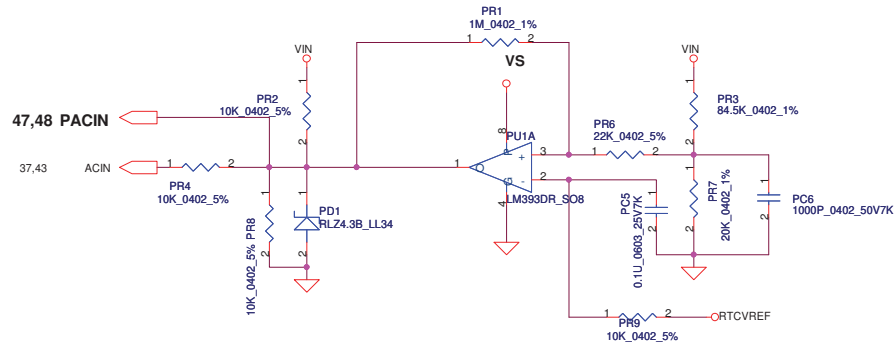
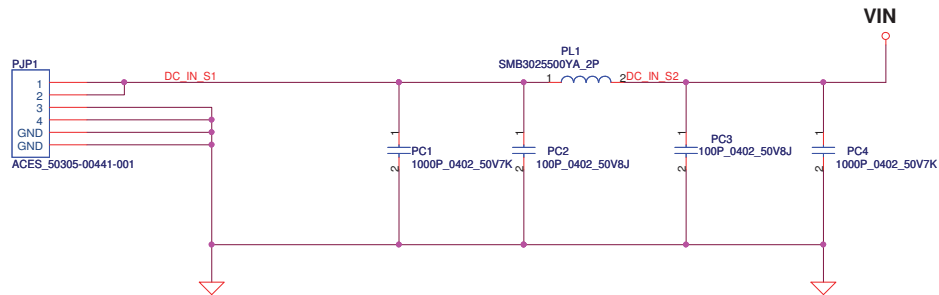


+1.05VS_VTT to +1.05VSDGPU for GPU



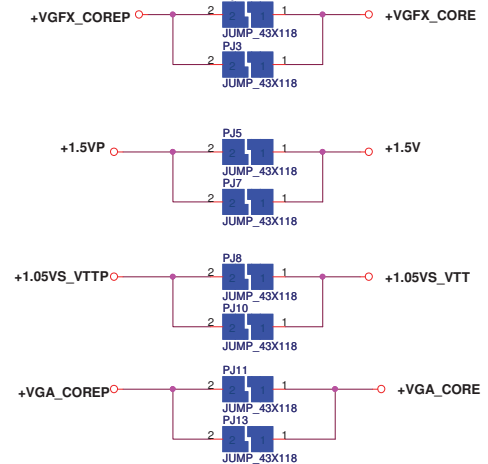
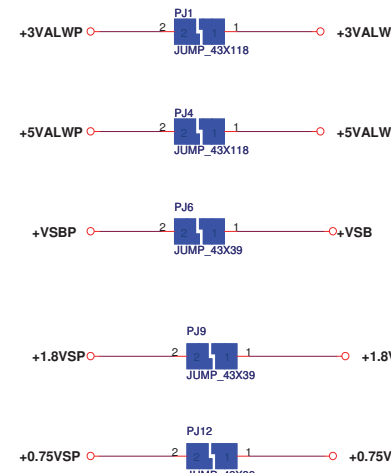
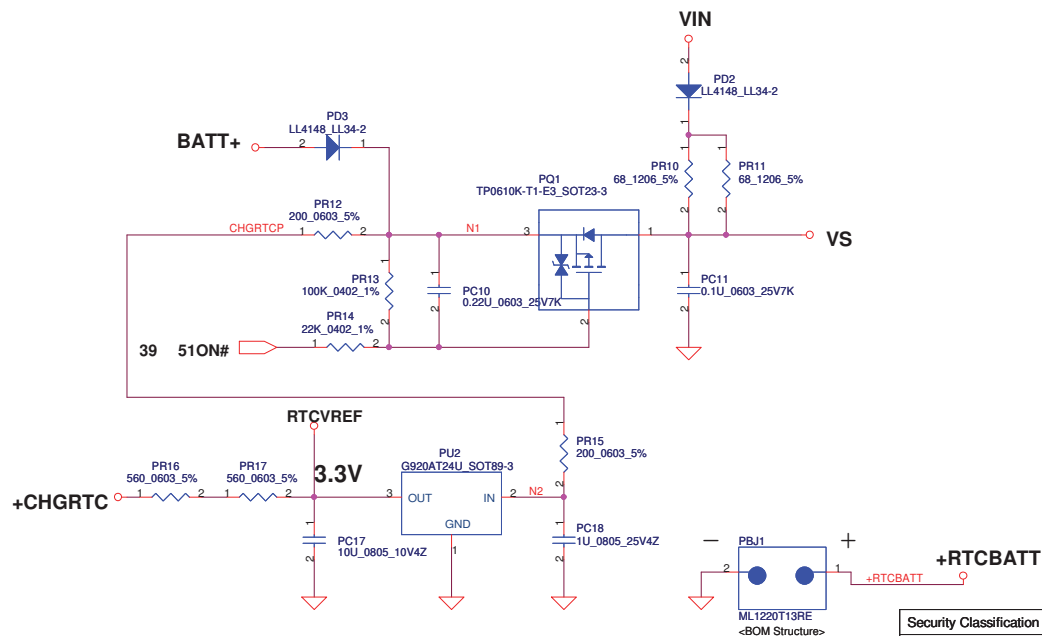
2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

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Issued Date				2009/11/23				Title			
				Deciphered Date				2010/11/23			
								DC Interface			
								NELA0 M/B LA-6151P Schematic			
								Rev 1.0			
								Date: Wednesday, April 21, 2010			
								Sheet 43 of 58			



Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

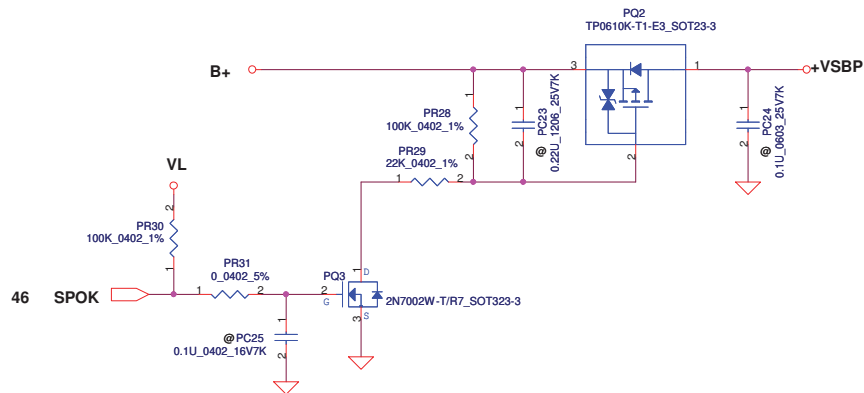
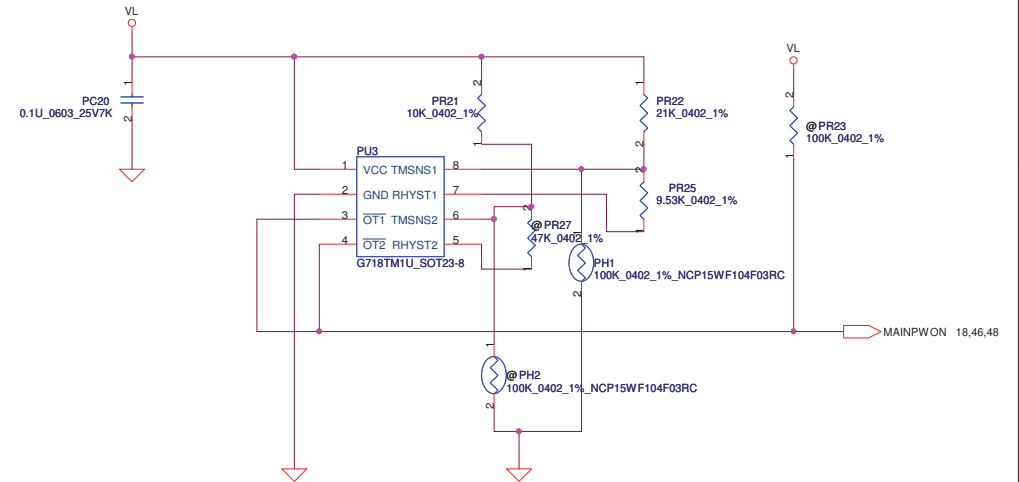
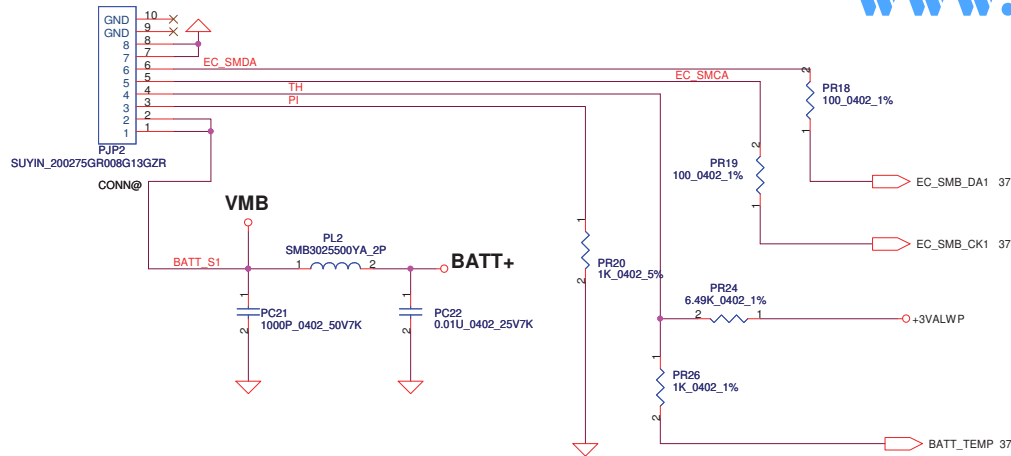


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										DCIN & DETECTOR	
										Size	
										Document Number	
										NELAO M/B LA-6151P Schematic	
										Rev	
										1.0	
										Date:	
										Wednesday, April 21, 2010	
										Sheet	
										44 of 58	

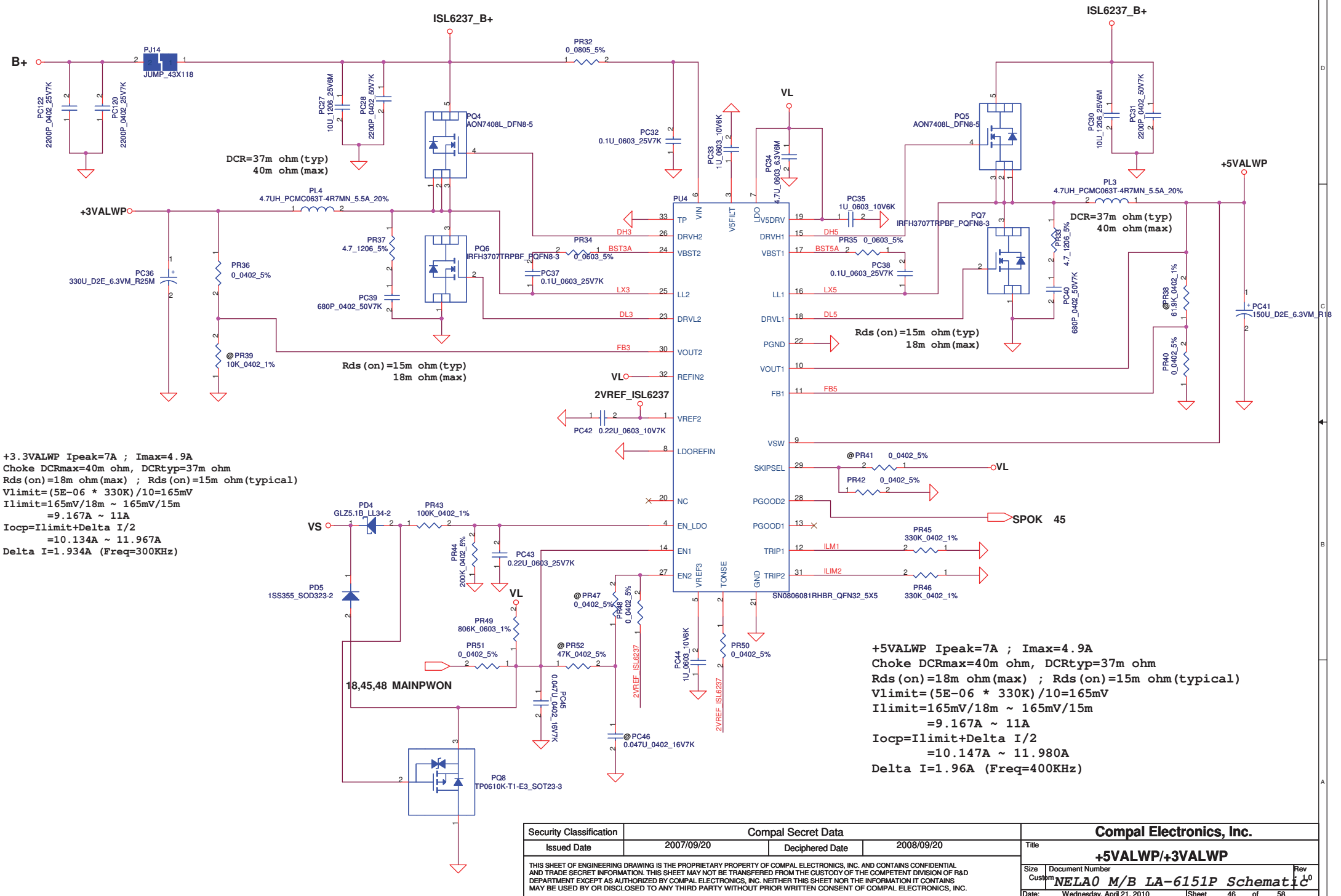
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PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 56 degree C



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Size	Document Number	Rev			1.0
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+3.3VALWP Ipeak=7A ; Imax=4.9A
 Choke DCRmax=40m ohm, DCRtyp=37m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.134A ~ 11.967A
 Delta I=1.934A (Freq=300KHz)

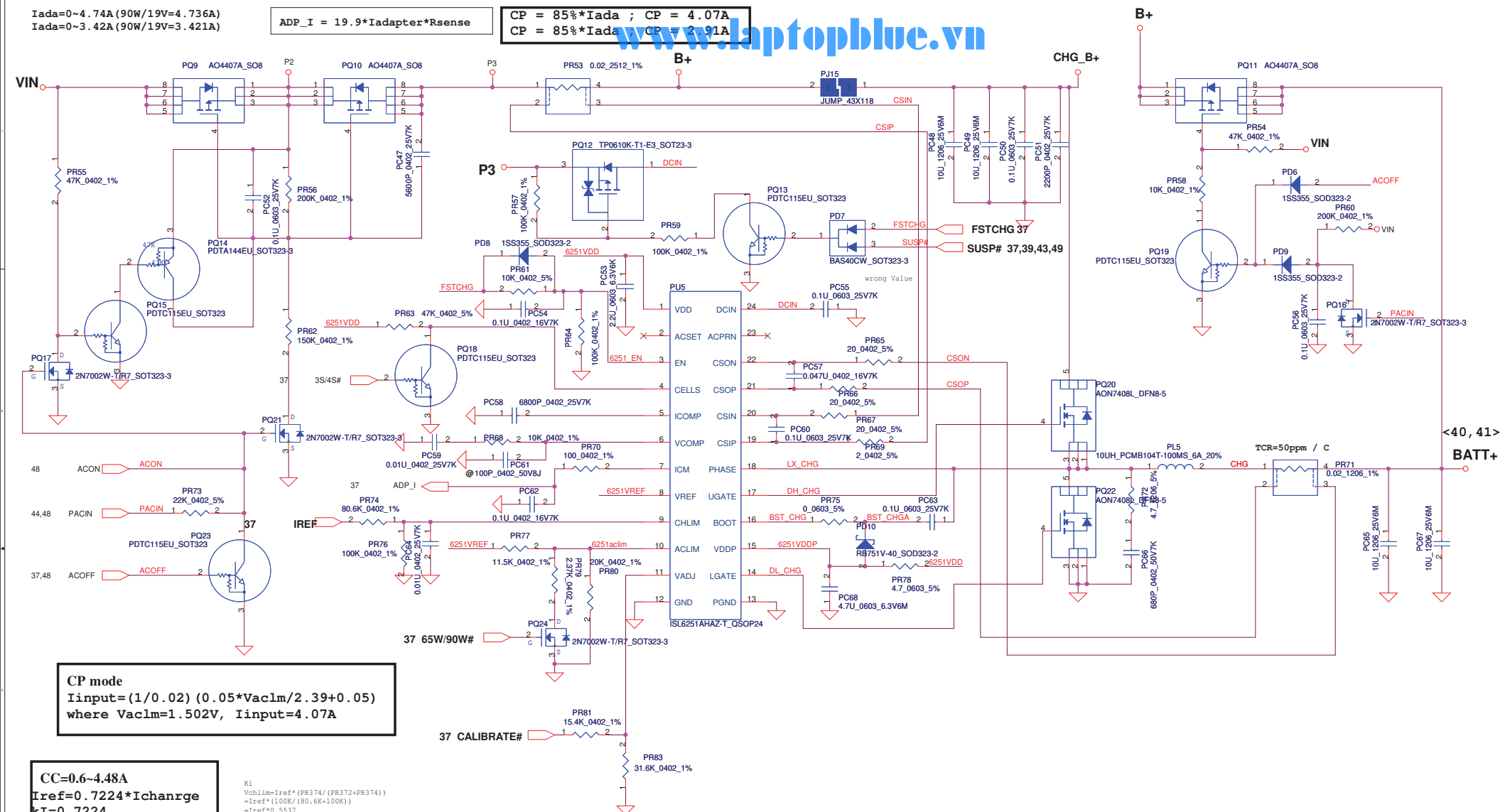
+5VALWP Ipeak=7A ; Imax=4.9A
 Choke DCRmax=40m ohm, DCRtyp=37m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.147A ~ 11.980A
 Delta I=1.96A (Freq=400KHz)

I_{ada}=0~4.74A (90W/19V=4.736A)
I_{ada}=0~3.42A (90W/19V=3.421A)

ADP_I = 19.9*I_{adapter}*R_{sense}

CP = 85%*I_{ada} ; CP = 4.07A
CP = 85%*I_{ada} ; CP = 2.91A

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CP mode
I_{input}=(1/0.02) (0.05*V_{ac1m}/2.39+0.05)
where V_{ac1m}=1.502V, I_{input}=4.07A

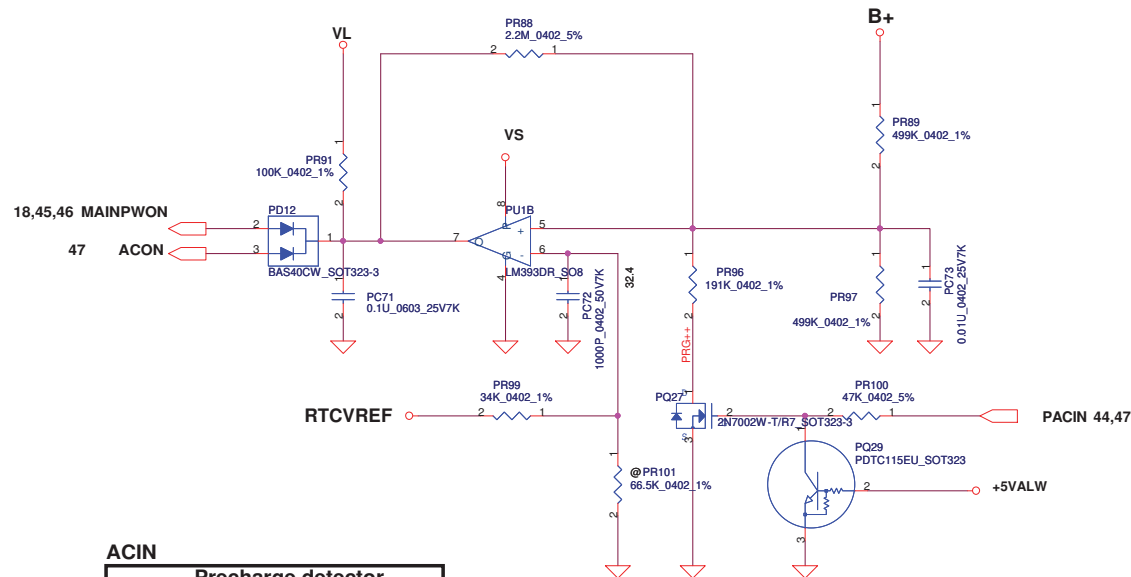
CC=0.6~4.48A
I_{ref}=0.7224*I_{charge}
K_I=0.7224
I_{REF}=0.43V~3.24V

K_I
V_{chlim}=I_{ref}*(PR374/(PR372+PR374))
=I_{ref}*(100K/(80.6K+100K))
=I_{ref}*0.5537
I_{charge}=(165mV/PR369)*(V_{chlim}/3.3V)
=(165mV/20m)*(1/3.3V)*I_{ref}*0.5537
=1.3842*I_{ref}
I_{ref}=0.7224*I_{charge} => K_I=0.7224

R_v
R_{internal} ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K/31.6K/(15.4K+3K)=11.372K
r=514K/514K/31.6K=28.14K
V_{cell}=0.175*V_{adj}+3.99V
4.2V=0.175*V_{adj}+3.99V => V_{adj}=1.2V
V_{adj}=V_{ref}*(R/(R+514K))+CALIBRATE*(r/(r+514K))
1.1483=CALIBRATE*0.6046 => CALIBRATE=1.899
1.899=(4.2-(V_{cell}+A*0.175))*K_v=(4.2-(4.2+A*0.175))*K_v
A=V_{ref}*(R/(R+514K))=0.052
K_v=9.451

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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ACIN

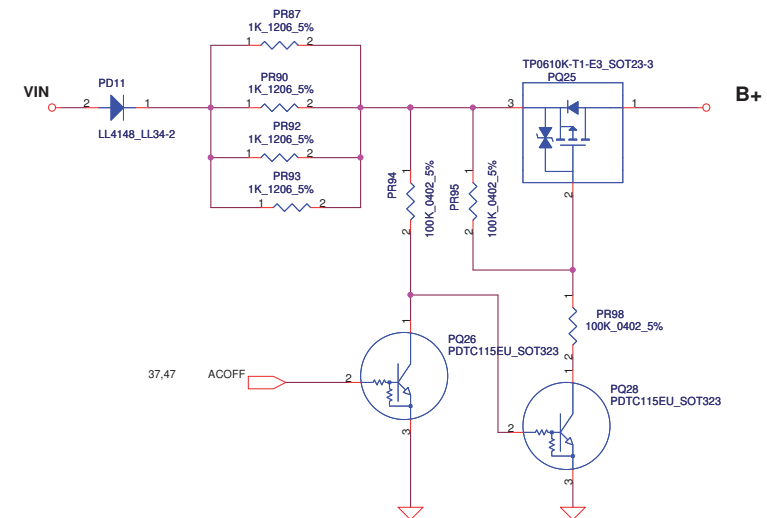
Precharge detector

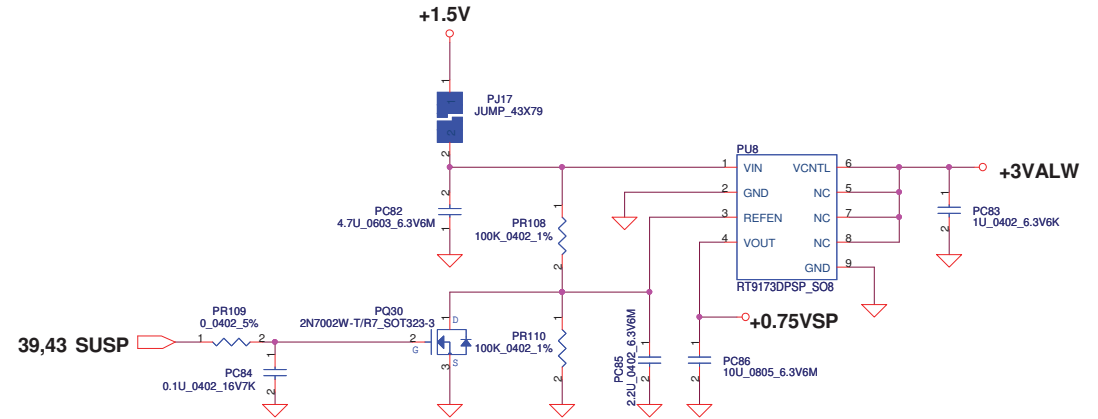
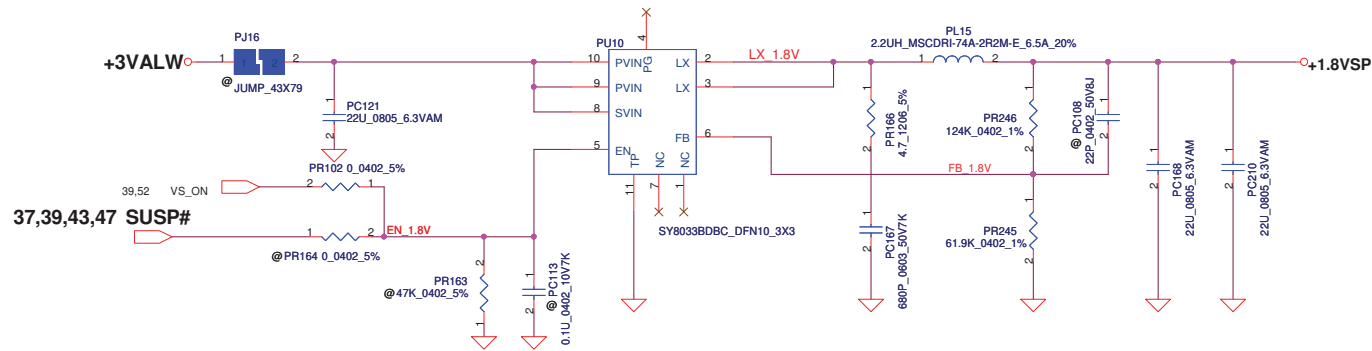
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

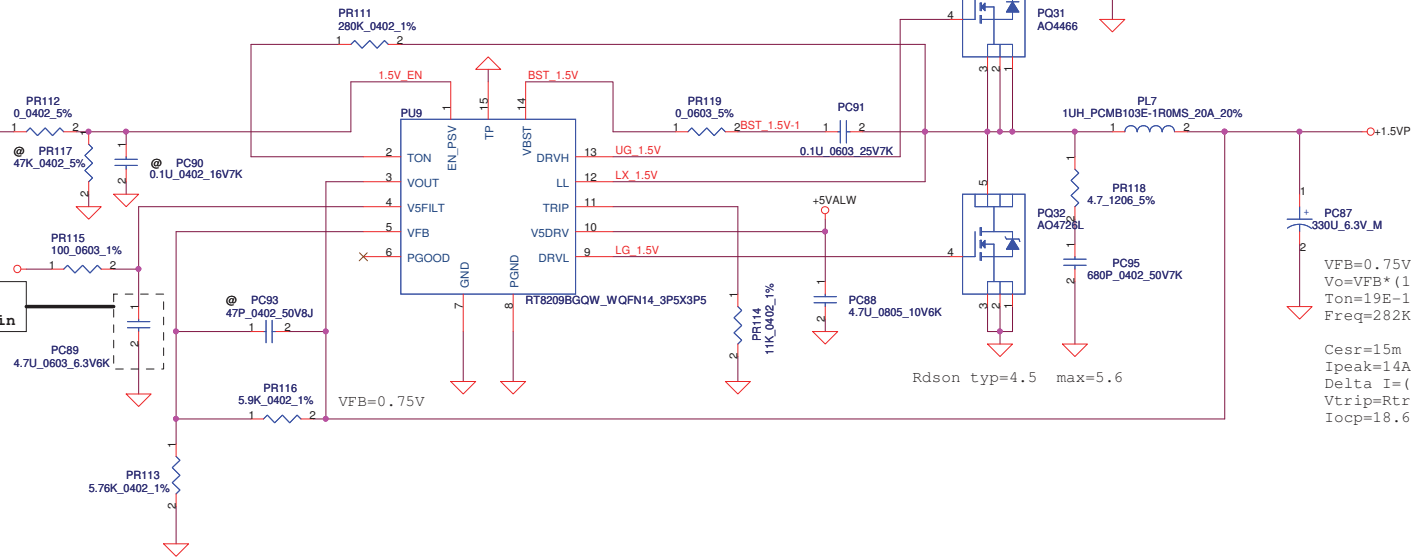




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				Document Number NELA0 M/B LA-6151P Schematic
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37,43 SYSON

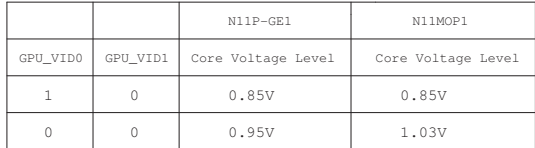
Layout Note:
Place near V5FILT Pin



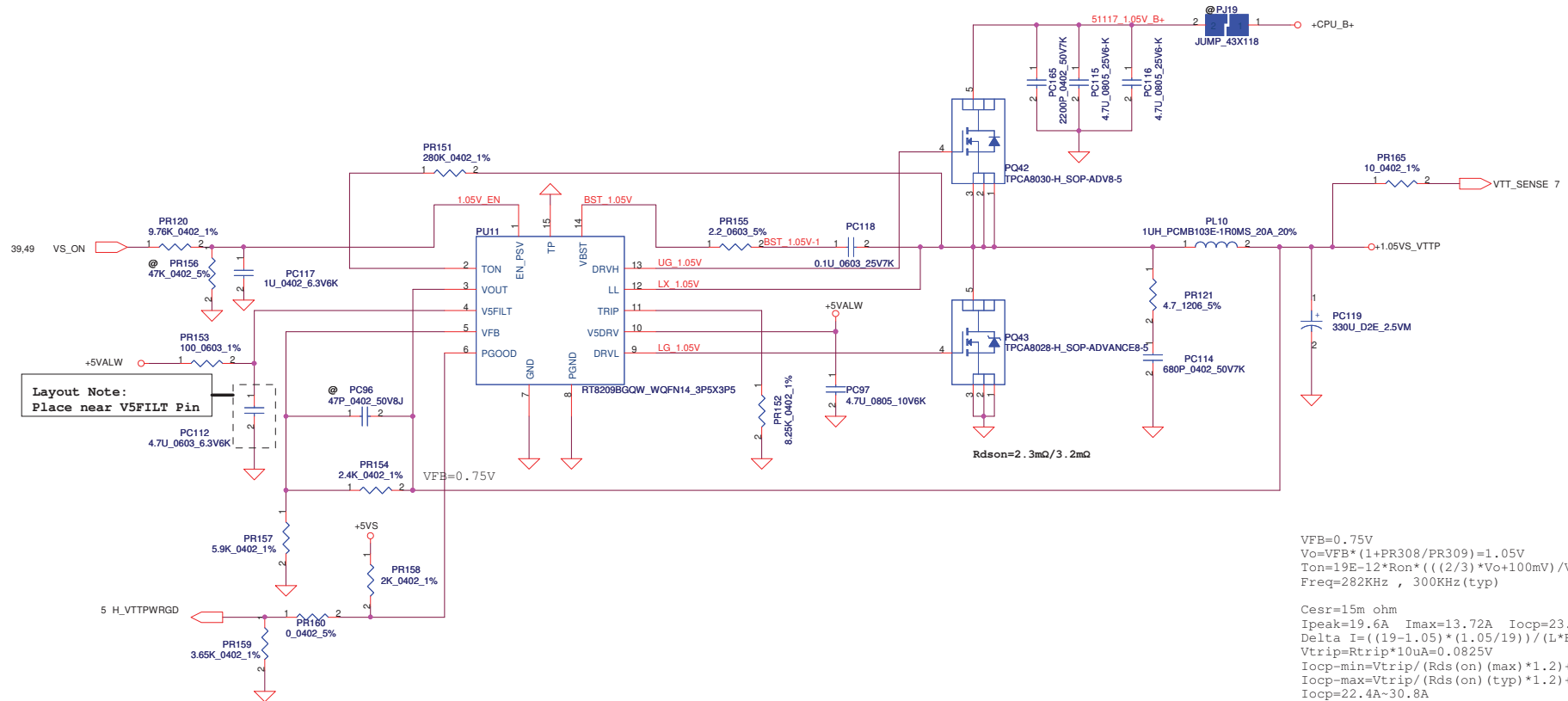
$V_{FB} = 0.75V$
 $V_o = V_{FB} * (1 + PR116 / PR119) = 1.52V$
 $Ton = 19E-12 * Ron * ((2/3) * V_o + 100mV) / V_{in} + 50ns = 3.8E-7$
 $Freq = 282KHz(min) , 300KHz(typ)$
 $Cesr = 15m\ ohm$
 $I_{peak} = 14A$ $I_{max} = 9.8A$ $I_{ocp} = 16.8A$
 $\Delta I = ((19-1.5) * (1.5/19)) / (L * Freq) = 4.61A$
 $V_{trip} = R_{trip} * I_{ocp} = 0.11V$
 $I_{ocp} = 18.674 \sim 22.675A$

Rdson typ=4.5 max=5.6

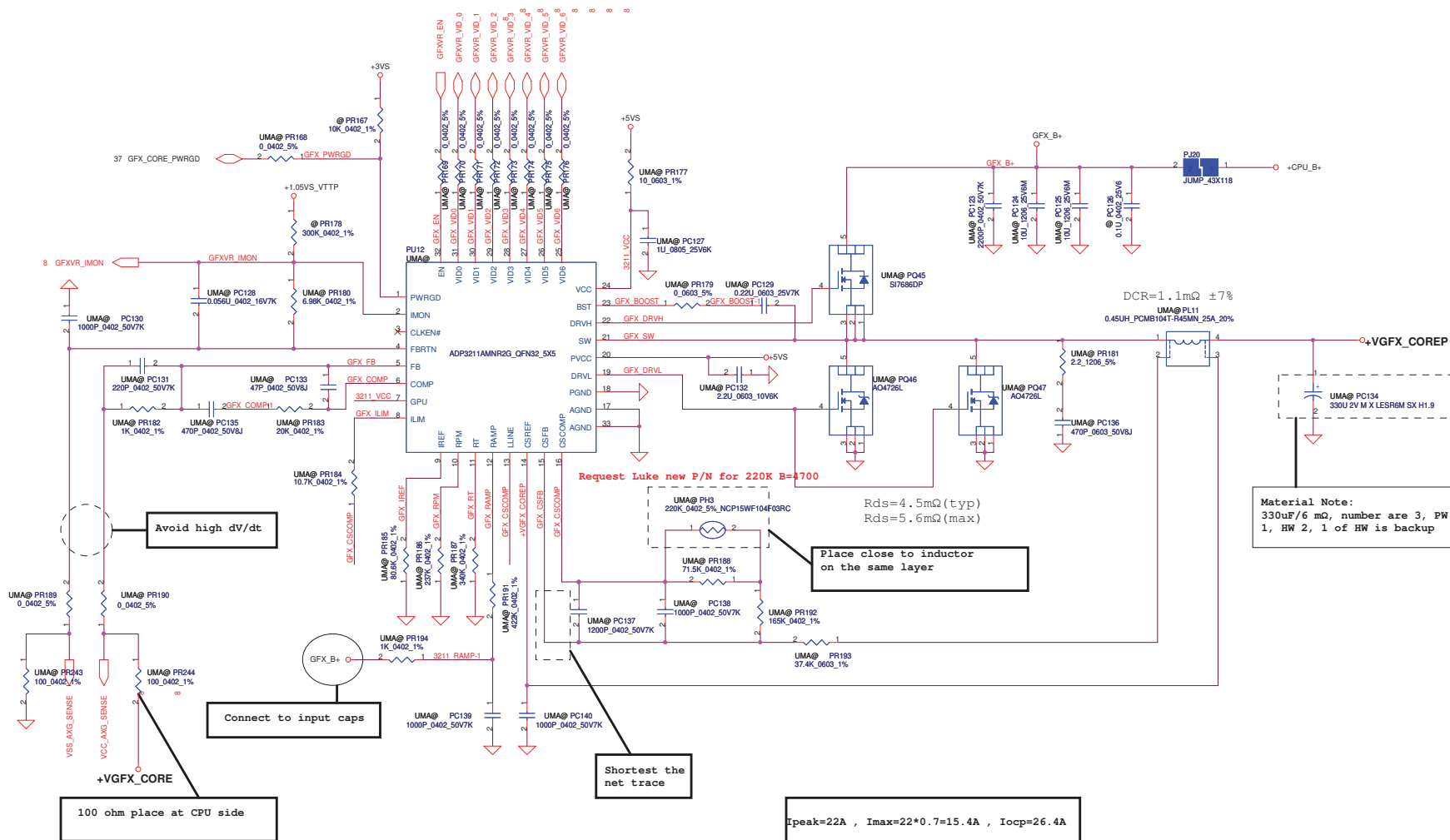
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Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	
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Size	Document Number	Rev			1.0
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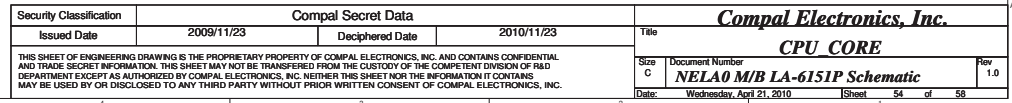


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Size		Document Number		Rev	
Custom		NELA0 M/B LA-6151P Schematic		1.0	
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify APW7138 location	for X76 BOM Level	0.1	48	modify PU10 to PU999		DVT
2	Modify VGA core ocp setting	OCF setting	0.1	50	modify PR131 to SD00000K980 (S RES 1/16W 4.64K +-1% 0402)		DVT
3	Modify 1.05V PWRGOOD circuit	BOM error	0.1	51	modify PR160 to SD028000080 (S RES 1/16W 0 +-5% 0402) modify PR159 to SD034365180 (S RES 1/16W 3.65K +-1% 0402) modify PR158 to SD034200180 (S RES 1/16W 2K +-1% 0402)		DVT
4	Modify 1.05V VTT_SENSE circuit	BOM error	0.1	51	Delete PR165 SD034100A80 (S RES 1/16W 10 +-1% 0402)		DVT
5	Modify OTP circuit pull high R	BOM error	0.1	52	Delete PR23 SD034100380 (S RES 1/16W 100K +-1% 0402)		DVT
6	Modify VGA_CORE SENSE circuit	BOM error	0.1	53	modify PR162 to SD028100A80 (S RES 1/16W 10 +-5% 0402)		DVT
7	Modify CPU_CORE choke	BOM modify	0.1	46	modify PL13,PL14 to SH000005680 (S COIL 0.36UH +-20% PCMC104T-R36MNDPL7)		DVT
8	Modify charger choke	Cyntec burnning issue	0.1	47	modify PL5 to SH000009R00 (S COIL 10UH +-20% MMD-10DZ-100M-X1 6A)		DVT
9	Modify GFX and CPU CORE thermistor	OCF setting	0.1	52	Modify PH3,PH4 to SL200000500 (S THERM_ 220K +-5% ERTJ0EV224J 0402)		DVT
10	BOM change	cost down	0.1	48	Modify PL9,PL13,PL14 to SH12036BM00 (S COIL .36UH +-20% ETQP4LR36WFC0V2HA)		DVT
11	BOM change	cost down	0.1	52	Modify PL11 to SH000005080 (S COIL 0.45UH -25+20% ETQP4LR45XFC 25A)		DVT
12	BOM change	cost down	0.1	52	Modify PQ34,PQ45 to SB000008L80 (S TR SI7686DP-T1-E3 1N POWERPAK 808D)		DVT
13			0.2	46			
14			0.2	51			
15			0.2	52			
16			0.2	53			
17			0.2	52			
18			0.2	50			
19			0.2	55			
20			0.2	53			
21			0.2	55			
22			0.2	48			
23			0.2	52			

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/11/23	Deciphered Date	2010/11/23	Title	
				PIR (PWR)	
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				NAV70 M/B LA-5891P Schematic	
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0.1->0.2

Reason for change

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PG#			Date		Phase
2010/01/05	38	TP PIN Define error	SWAP JTP1 PIN DEFINE		
	14	VGA REQUEST ISSUE	CHANGE R668 to VGA@;CHANGE R593 to DISO@; ADD R747@		
2010/01/11	40	EXTERNAL MIC Can't record	ADD C714,C715		2010/01/05
	43		CHANGE C522 to SGA000002380 (6moh)		2010/01/05
2010/01/13	35	For HUAWEI 3G module Card	ADD R748,R749,R751		2010/01/11
2010/01/14			Change Q13/19/20 CIS Symbol to 2N7002DWH_SOT363-6		2010/01/11
			CHANGE ALL DUAL 2N7002 P/N to SB00000EO10		2010/01/11
	43	VGA Sequence	change R425 from 200K to 510K, R578 from 510K to 200K		2010/01/13
2010/01/15	8		change R88 to 470 ohm		2010/01/14
	32	asmedia issue	ADD R464, R750		2010/01/14
	18	CRT_DET	Q37/R41 Change BOM Structure to @		2010/01/14
	30	DFB ISSUE	DEL C2		2010/01/15
	19	CRT flick issue	CHANGE c229 to 22U, ADD C717 (22U) , Reserve C718(22U)		2010/01/15
	36/40	EMI/ESD Request	POP D25/L40, Un-pop R635/R636, R649 change to SM010027780		2010/01/15
	14	EMI/ESD Request	ADD C719 (470Pf)		2010/01/15
	37	EMI/ESD Request	ADD C720 (470Pf)		2010/01/15
	41	EMI/ESD Request	ADD C721/C722(100Pf) for DMIC CLK/DATA, Chage ESD Dioad p/n to SCA00000200		2010/01/15
	12	RF Request	POP C704/705/C713		
	13	RF Request	POP C603		
	17	RF Request	POP C254		
	32	Vendor Recommand ; CFG Setting is 000	POP R238/R629/R232 ; UnPop R237/R628/R233		
	40	Codec No sound issue & beep issue	Unpop R650; Change R664 to 30K		
2010/01/21		Change P/N	Change C104/C110/C127/C67/C68/C80/C82/C90/C93/C96 to SE076103K80		
			Change C151 to SE076104K80		
			Change C34 to SE107475M80		
		Change P/N	Change C510/C538 to 0603 SIZE		
2010/01/26	35	EC Team recommand	Change R683 to 100k		

0.2->0.3	5	4	3	2	1
DATE	PAGE	Reason for change & Action			
2010/03/04	35	1. ADD 3G@ 2. DEL C723;ADDC723,C725,C667			
	41	MIC NOISE DEL C721,C722			
	38	LED LIGHT DEL R726,R731,R724,R723 ADD R753,R757,R752,R756,R755,R759,R754,R758			
		Change TP Pin define			
	41	Change R286,R287 to 39ohm			
	36	Change L40 to SM070001600			
	37	Change Board ID ; Change R292 to 18K			
2010/03/09	37	Add R760 Q58 for H_PROCHOT#			
	12	Add C716 RF request			
2010/03/10	35	C709, C710, C711 change to 3G@			
2010/03/11	40	EMI request R723, R724, R726, R731 @ Add C726, C727, C728, C729 to 0.1U Remove J5			
	36	EMI request Add C730, C731, C732 to 0.1U			
	12	RF request reserved C733, C734, C735			
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5	4	3	2	1	

0.3 --> 1.0

DATE		PAGE	Reason for change & Action
2010/03/29	35		1. Del R658, R657
	38		1. JLED1 pin5 mini2_LED# change to WWAN_OFF 2. Add Q59, R693 for WWAN_OFF 3. R398 100K change to 10K
	38		1. Delete Q57 , R688 2. Add U41 , C736
2010/03/29	38		1. Delete Q57 , R688 2. Add U41 , C736
2010/04/01	38		1.For EMI : Delete R741 , add L50
	7		1.R79, R61 10ohm change to 0ohm 2.C164 0.1U change to @
	23		1.R331, R330 10ohm change to 0ohm 2.C431 0.1U change to @
2010/04/19	13		1.R625 change to @ ,No VENTURA need to pop 2.R602 change to VENTURA@
	22		1.R401, R432 Ventura@ change to VGA@ 2.R402, R421, R420, R419 DIS@ change to VGA@ 3.R402, R421, R420, R419 2K change to 2.2K
	7		1.R372 , R384 Ventura@ change to @
2010/04/20	30		1.R39 100K change to 10K
	7		1.R79, R61 0ohm change to 1ohm 2.C164 0.1U change to 1U change to VENTURA@
	23		1.R331, R330 0ohm change to 1ohm 2.C431 0.1U change to 1U change to VENTURA@
2010/04/21	43		1.Q16, Q18, R399, R425, C510, C507 VGA@ change to DISO@

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