

Compal Confidential

NIUM1

U260 12.5" M/B Schematics Document
Intel Arrandale SFF Processor with DDRIII + Ibex Peak-M

LA6232P

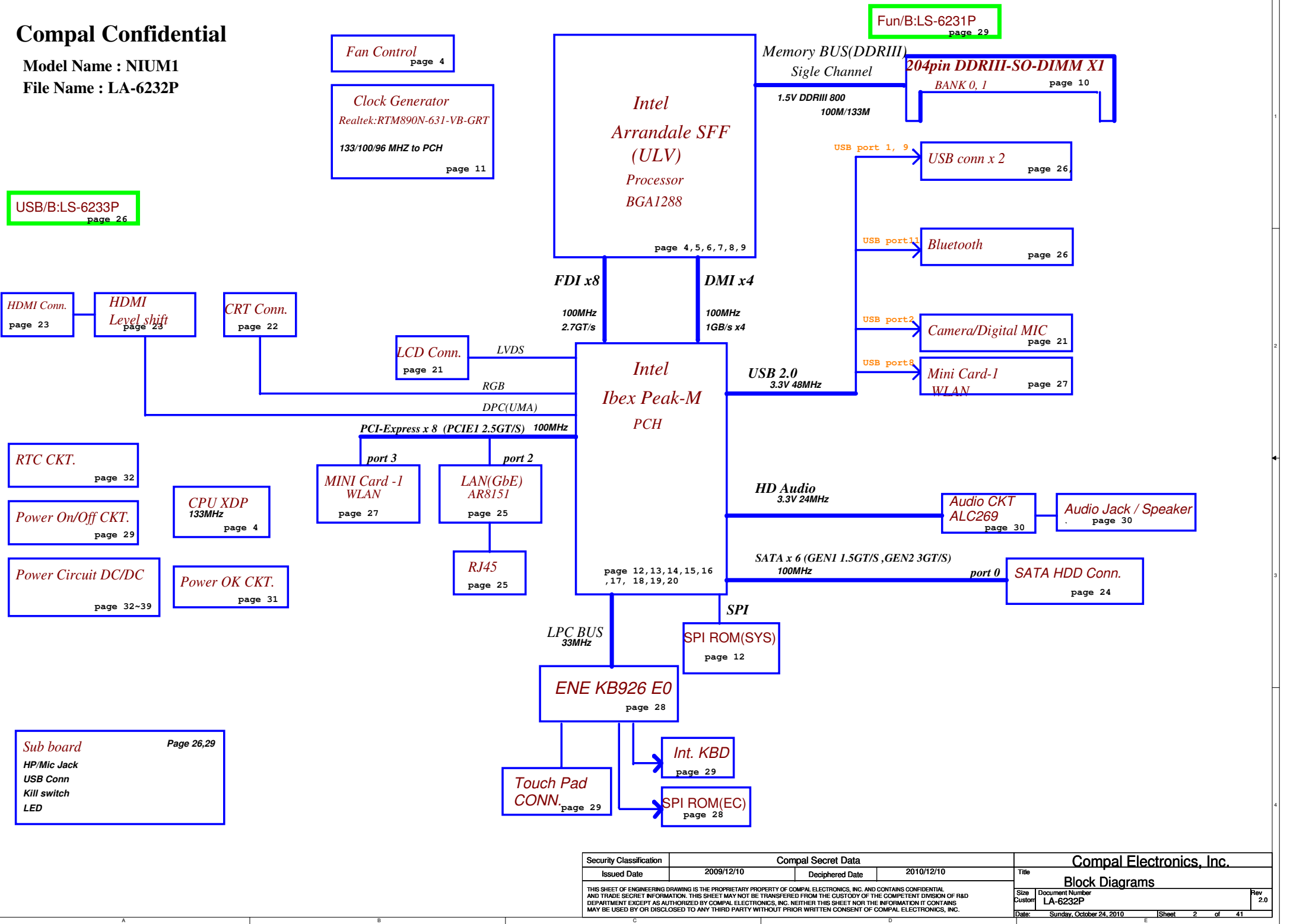
2010-10-22

REV: 2.0

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Model Name : NIUM1
File Name : LA-6232P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+VCCP	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for PCH	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Ambient Light Sensor	0110 XXXX XXXX b

EC SM Bus2 address

HEX
70/72,R/W

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1010 0000b
DDR DIMM2	1010 0100b
ISL90727	0101 1100b
ISL90728	0111 1100b

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BTO Item	BOM Structure

PCIE PORT LIST

PORT	DEVICE
1	
2	WLAN
3	LAN
4	
5	
6	
7	
8	

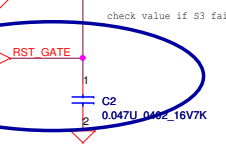
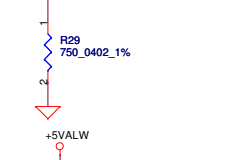
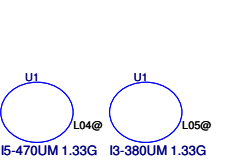
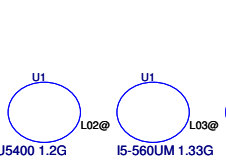
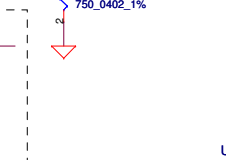
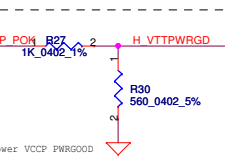
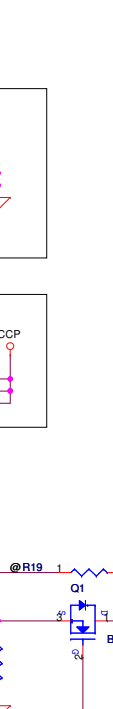
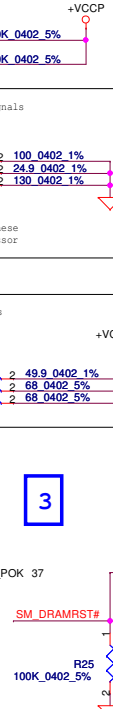
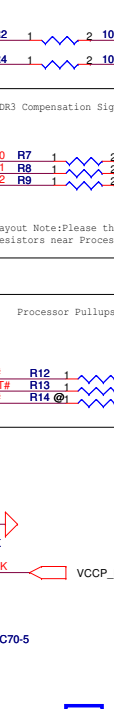
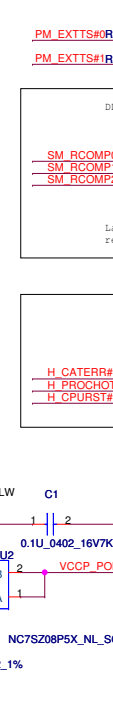
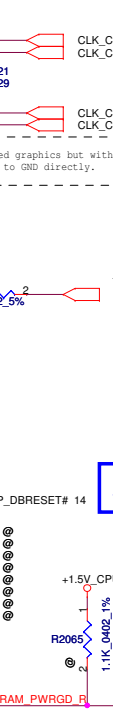
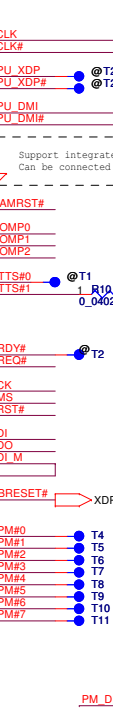
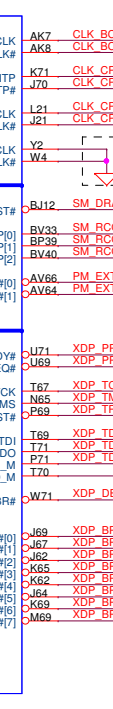
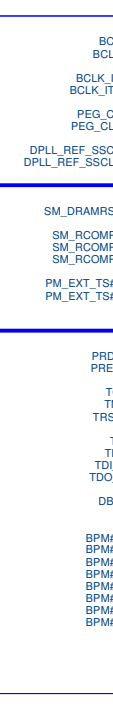
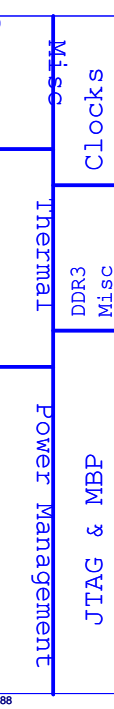
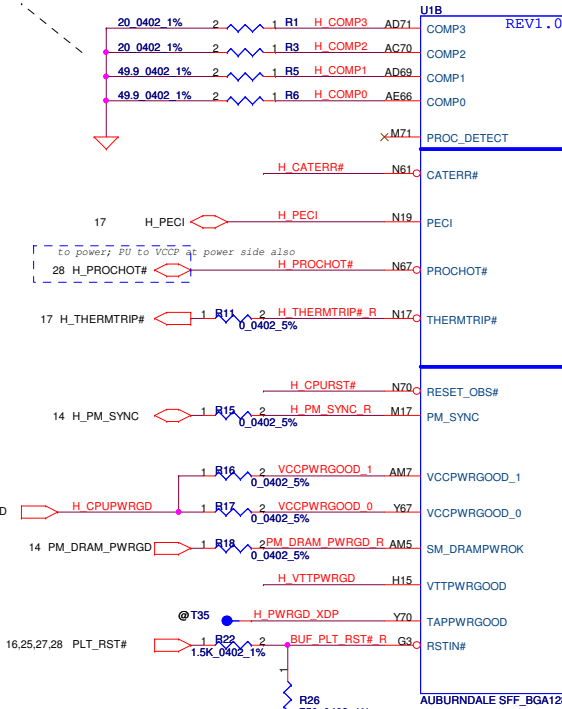
USB PORT LIST

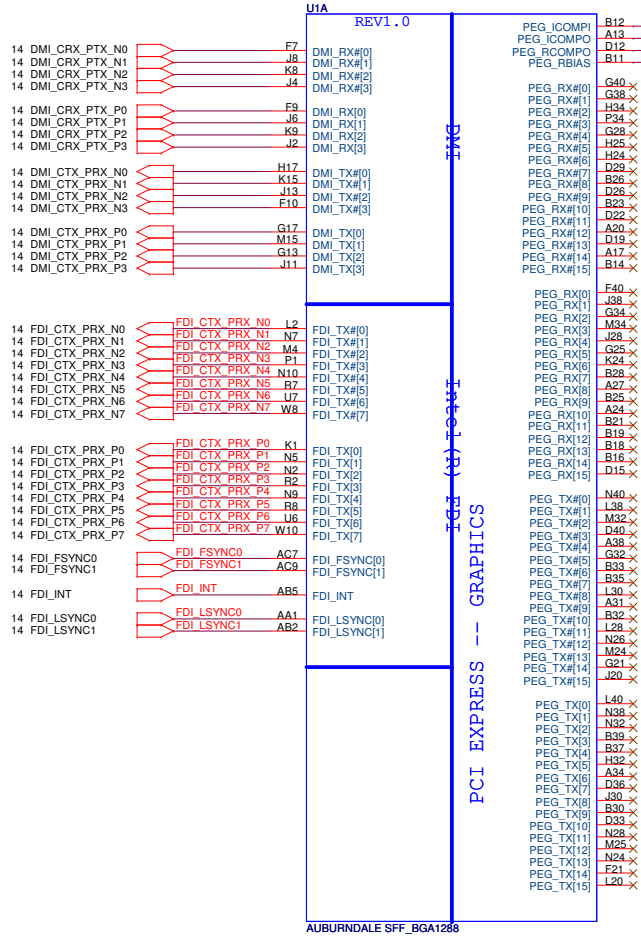
PORT	DEVICE
0	
1	USB Conn.
2	Camera
3	
4	
5	
6	
7	
8	MiniCard-1 (WLAN)
9	USB Conn.
10	
11	Bluetooth
12	
13	

SATA PORT LIST

PORT	DEVICE
0	HDD
1	
2, 3	
4	
5	

Layout rule: 10mil width trace
length < 0.5", spacing 20mil





Layout rule: trace
length < 0.5"



CFG Straps for PROCESSOR

CFG0 R44 1 @ 2 3.01K 0.0402 1%

PCI-Express Configuration Select	
CFG0	1: Single PEG 0: Sifurcation enabled Not applicable for Clarkfield Processor

CFG3 R45 1 @ 2 3.01K 0.0402 1%

CFG3-PCI Express Static Lane Reversal	
CFG3	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1,

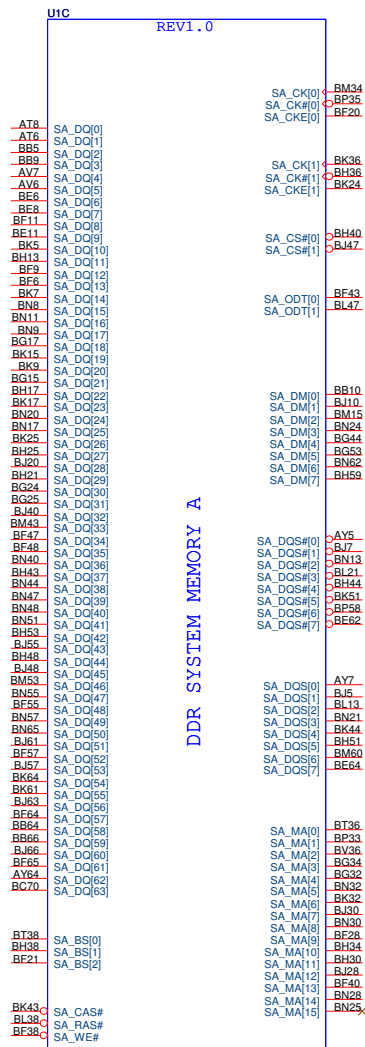
CFG4 R46 1 @ 2 3.01K 0.0402 1%

CFG4-Display Port Presence	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

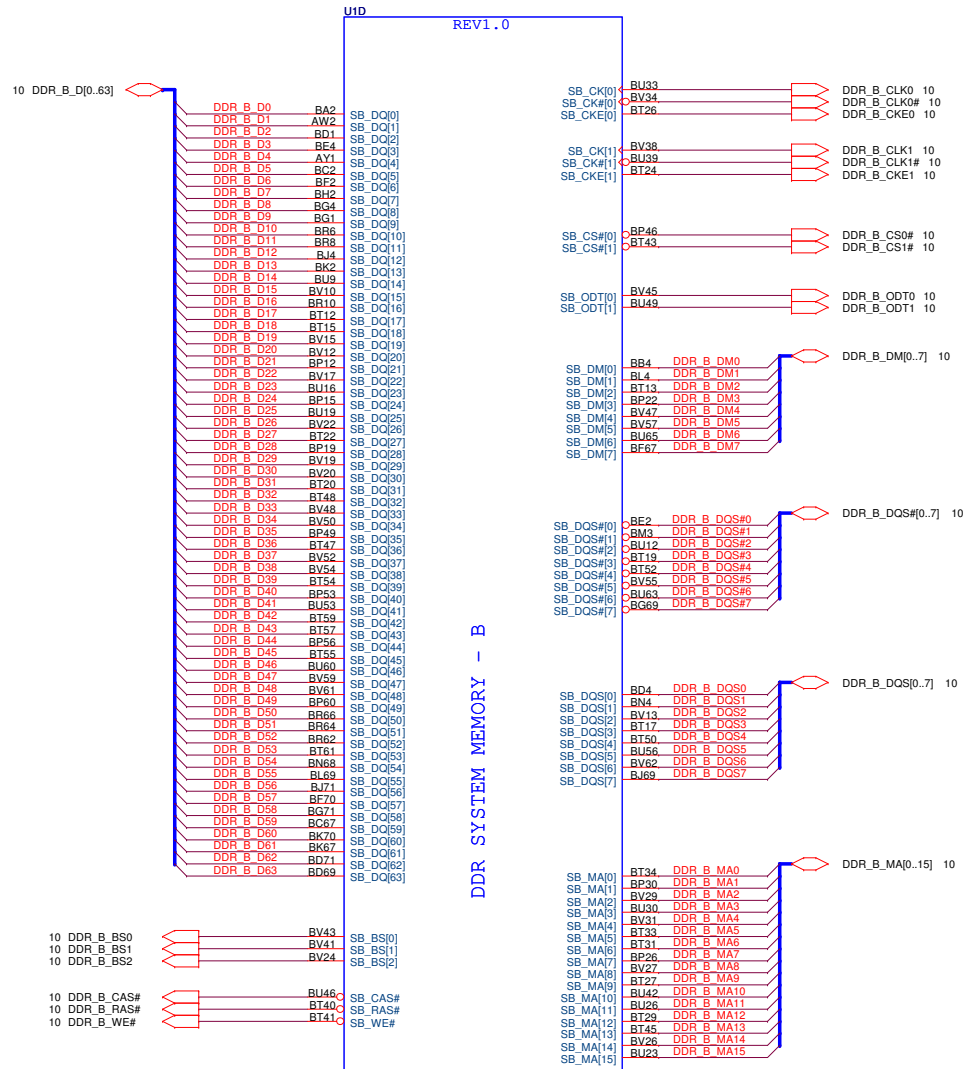
Package Daisy Chain: Daisy Chain Recommendation for SMT Connectivity

- 1: BR71 - pkg - BT71- board - BT69 - pkg - BV71 - board - BV69 - pkg - BV68
- 2: A68 - pkg - A69 - board - C69 - pkg - A71 - board - C71 - pkg - E71
- 3: A5 - pkg - C3
- 4: BR1 - pkg - BT1 - board - BV1 - pkg - BT3 - board - BV3 - pkg - BV5

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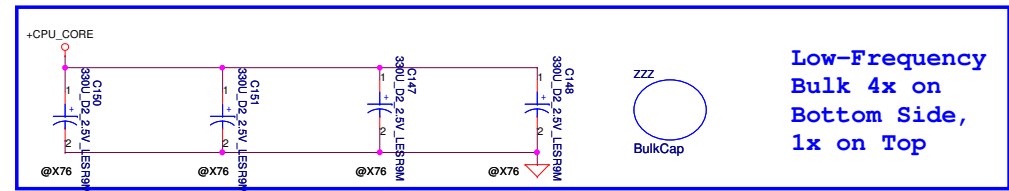
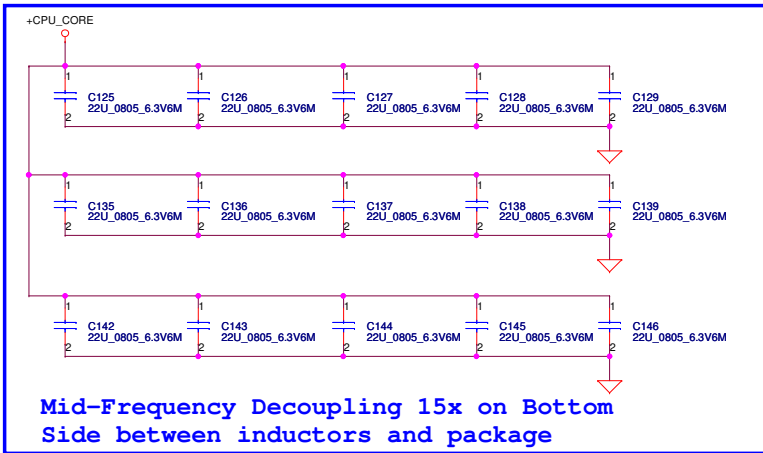
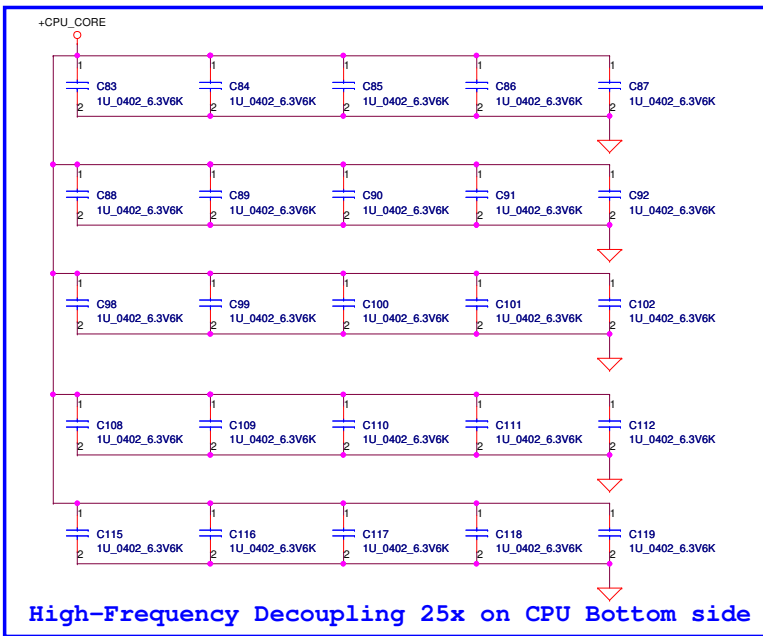


AUBURNDALE SFF_BGA1288

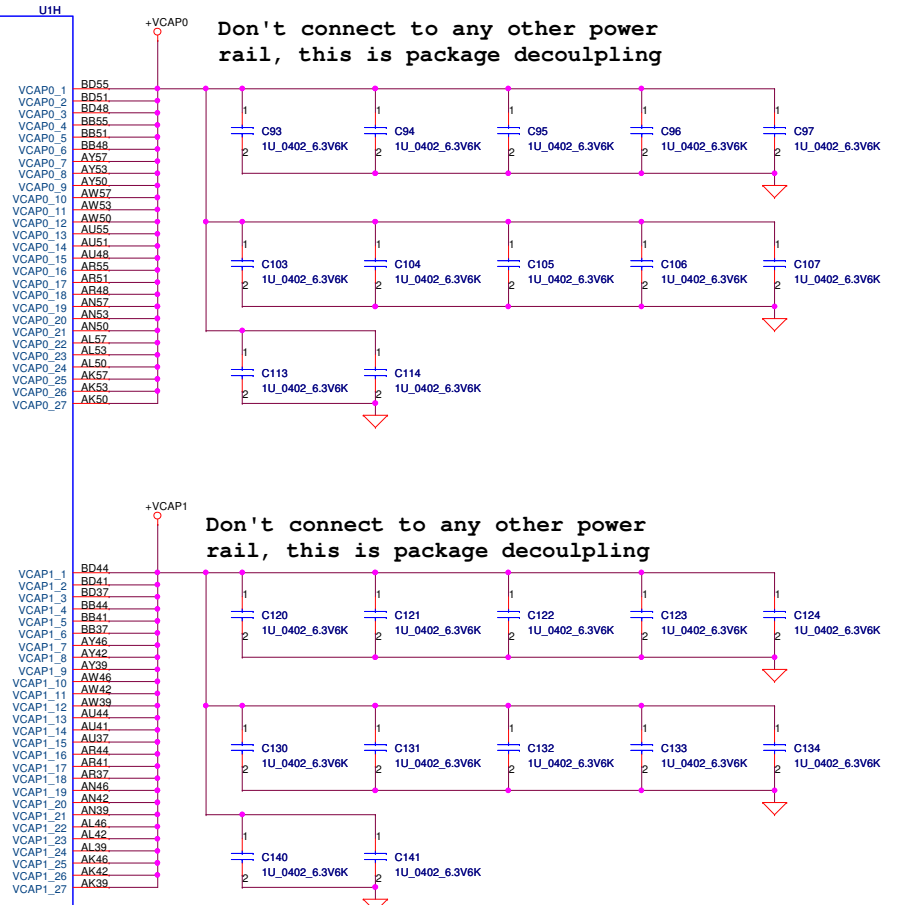
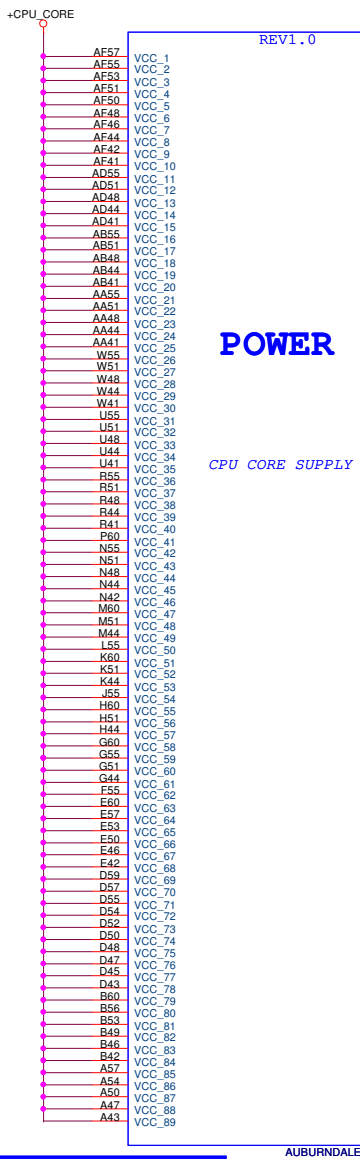


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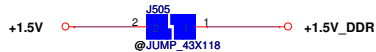


Current = 274A

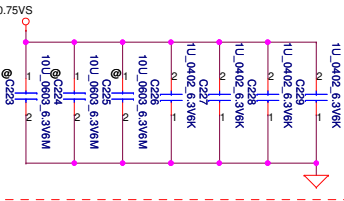


PROCESSOR Power Rail Table (EDS V1.0)		
Voltage Rail	Voltage	SO Iccmax Current (A)
VAXG	1.5	22
VccPLL	1.8	1.35
VCORE	0.75	48
VDDR	1.5	3
VTT	1.05	18

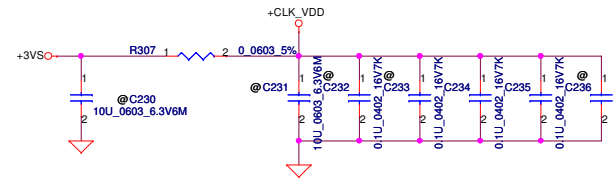
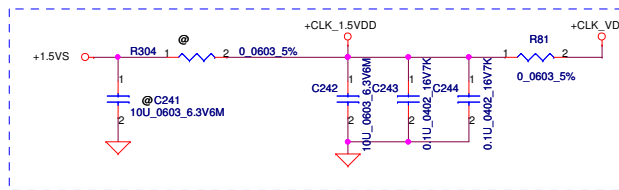
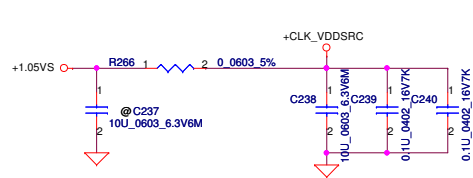
1



Layout Note:
Place near JDIMM1.203 & JDIMM1.204

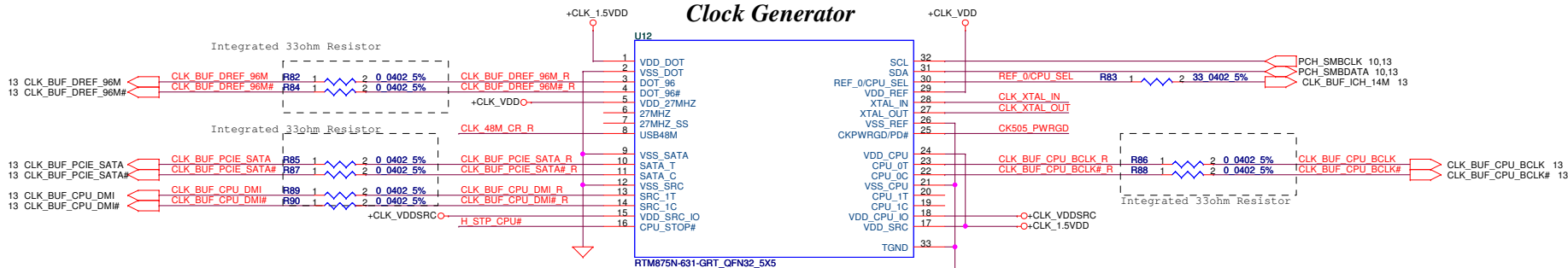


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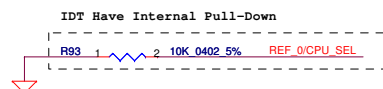
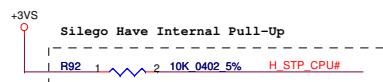


change to standard voltage of clock gen 7/23
non-stuff R304, stuff R81
change U12 to SA00003ET00

Clock Generator

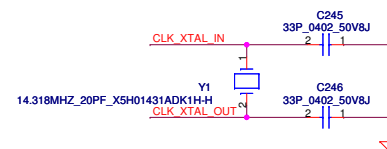
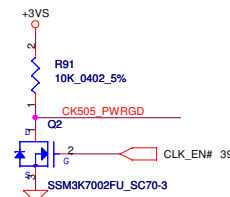


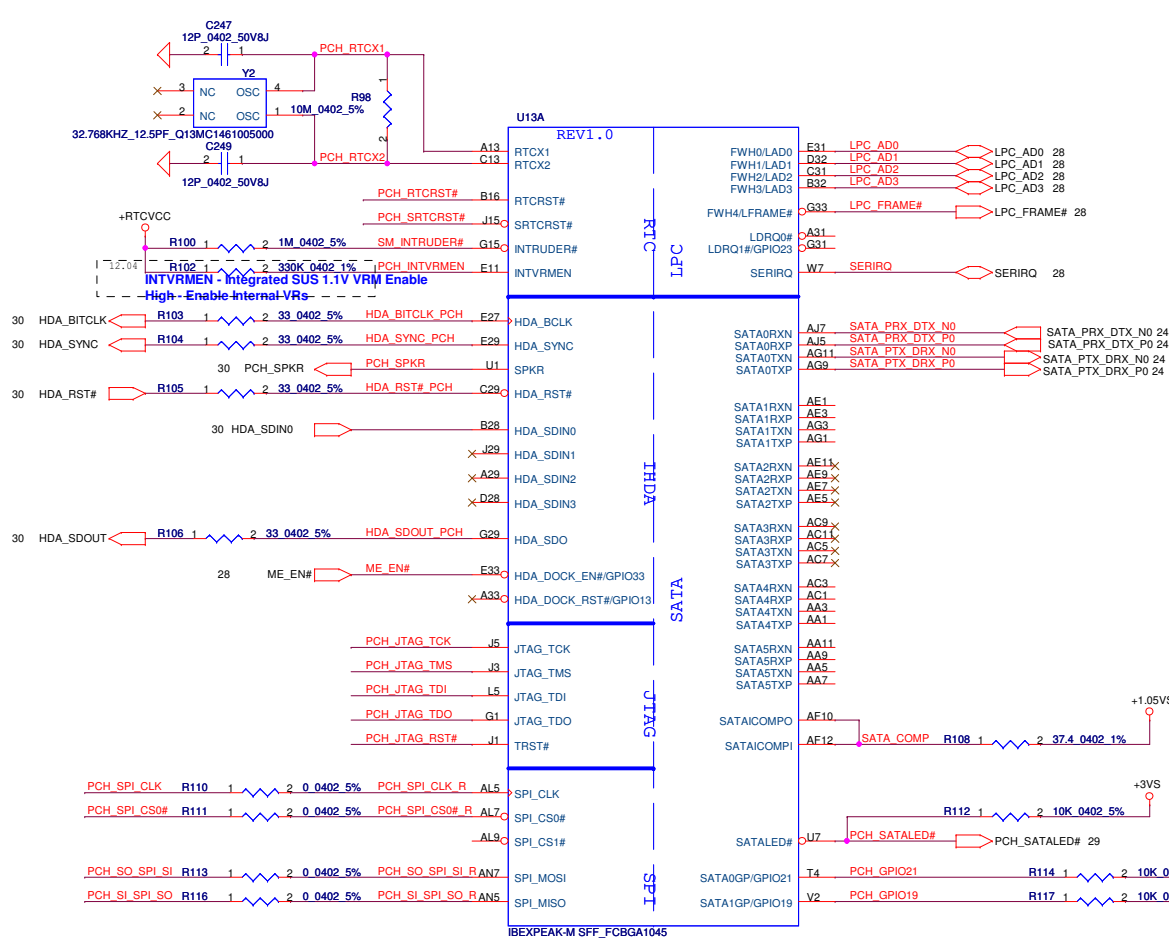
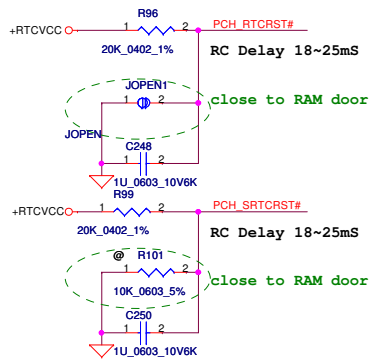
Realtek: SA00003ET00, S IC RTM875N-631-GRT QFN 32P CLK GEN



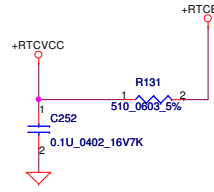
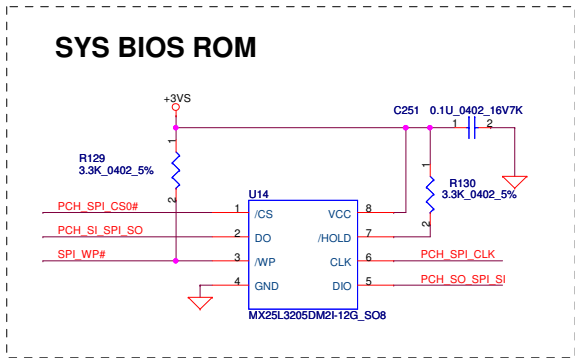
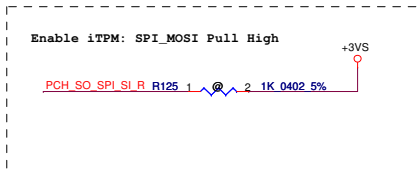
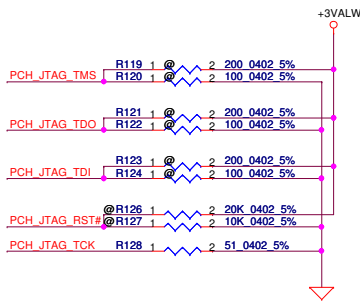
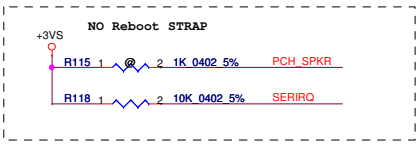
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

PIN8 IS GND FOR ICS3197
PIN8 IS 48MHz FOR ICS3199

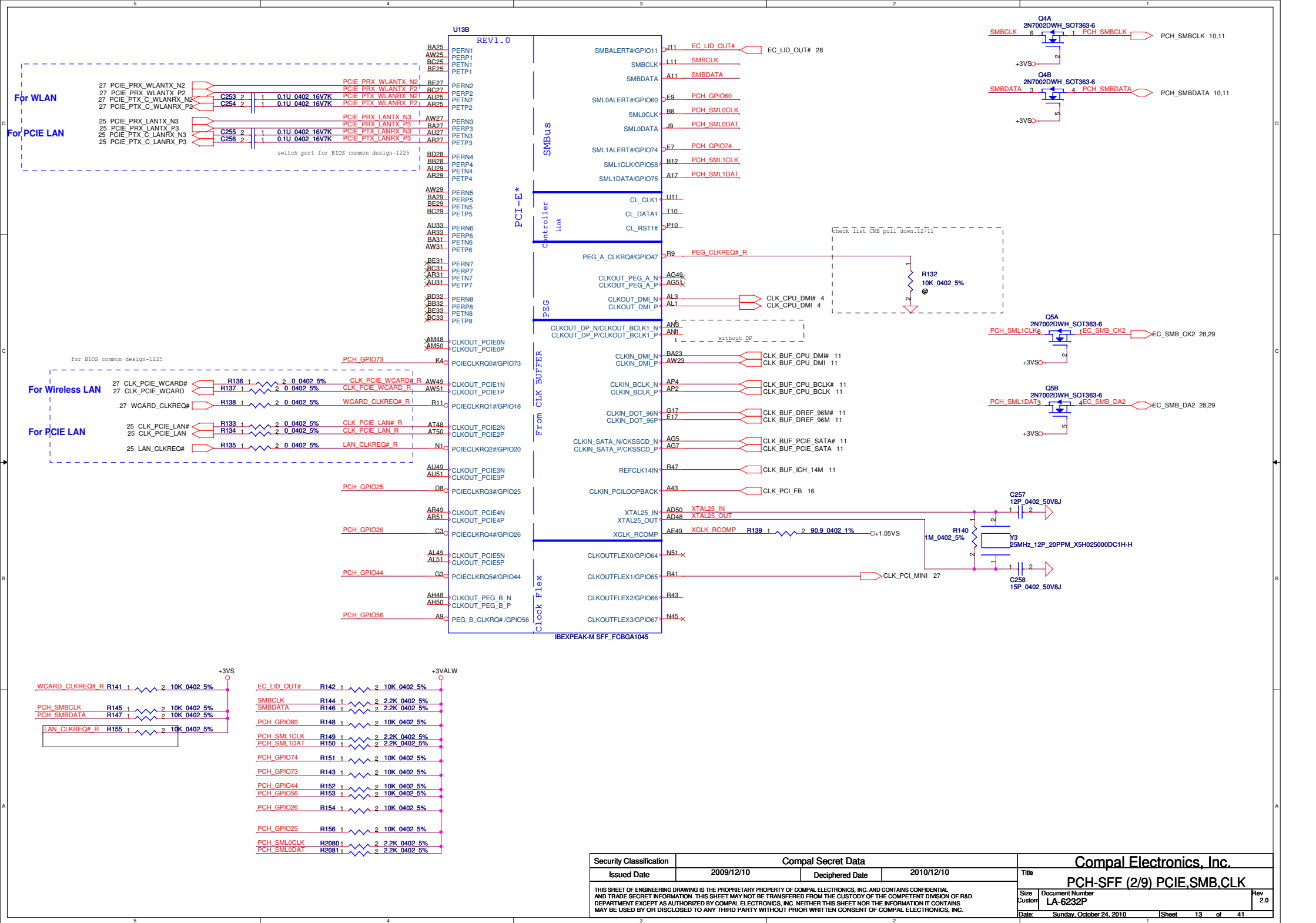




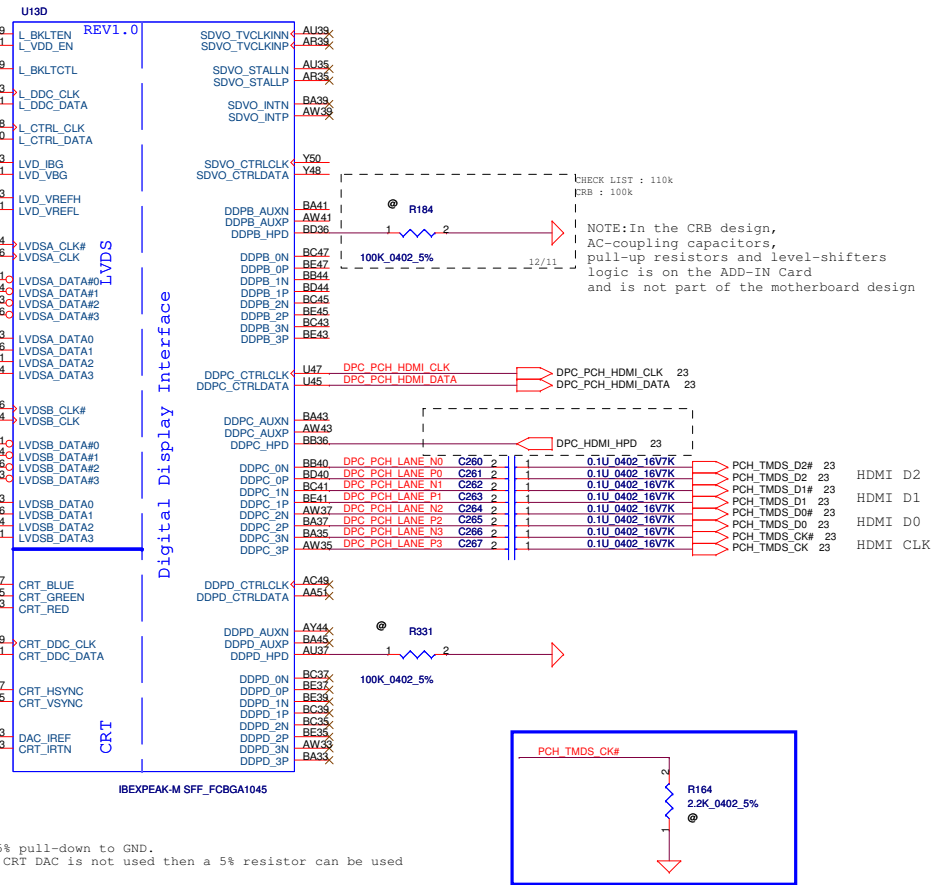
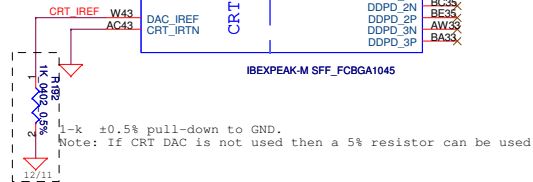
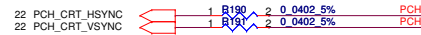
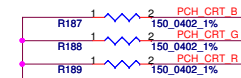
SATA for HDD1



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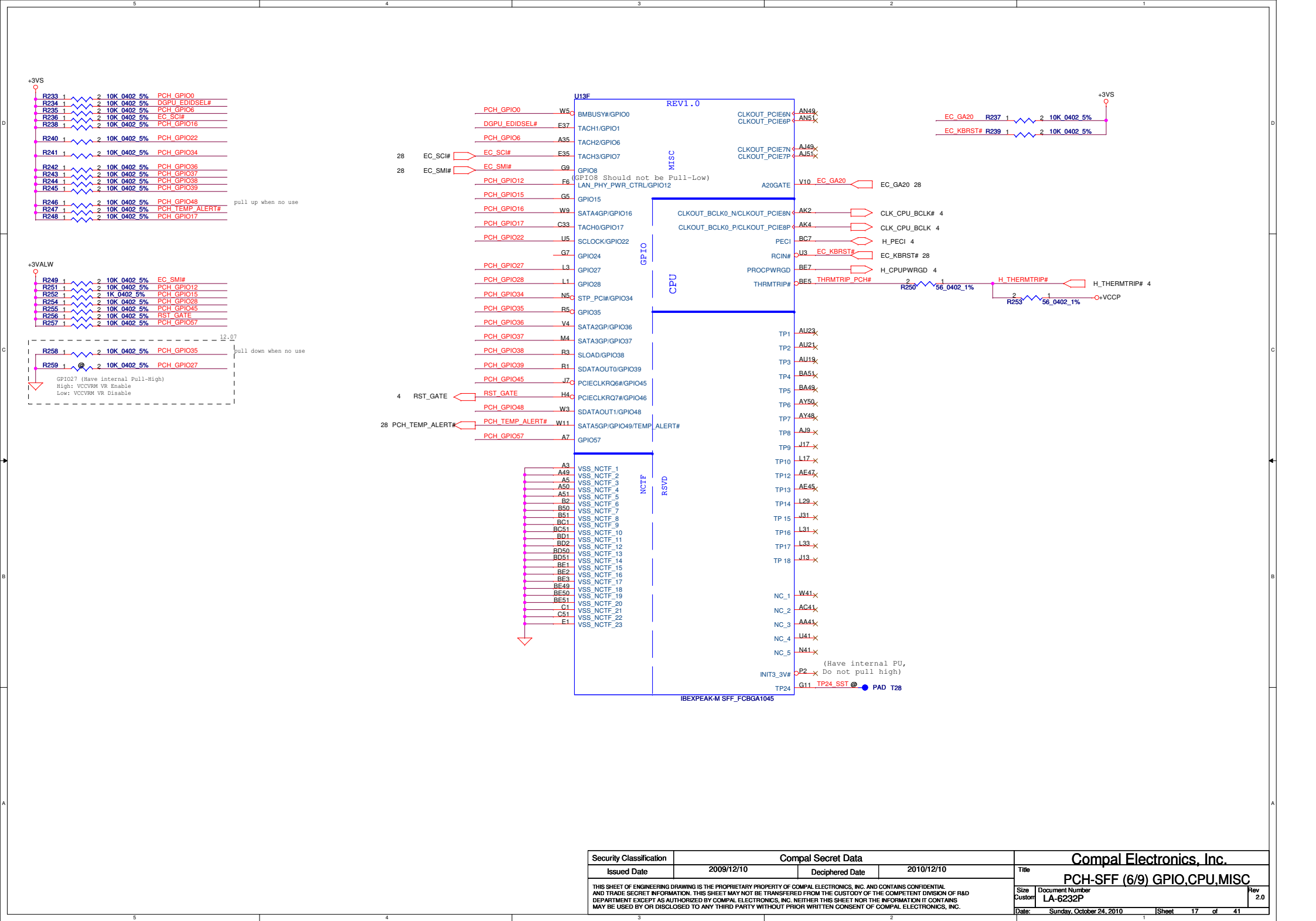


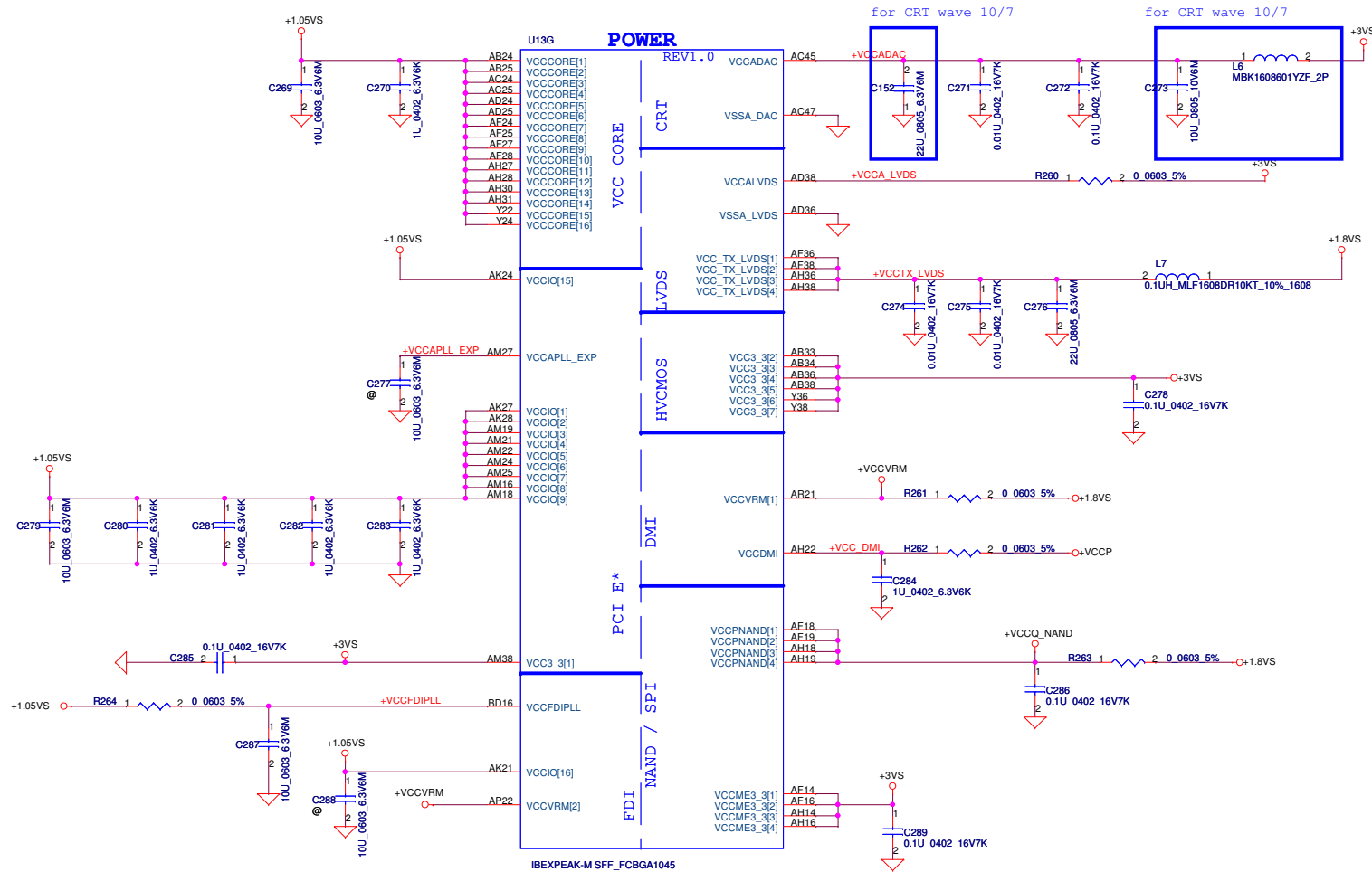
BACKLIGHT_PWM (DPST)

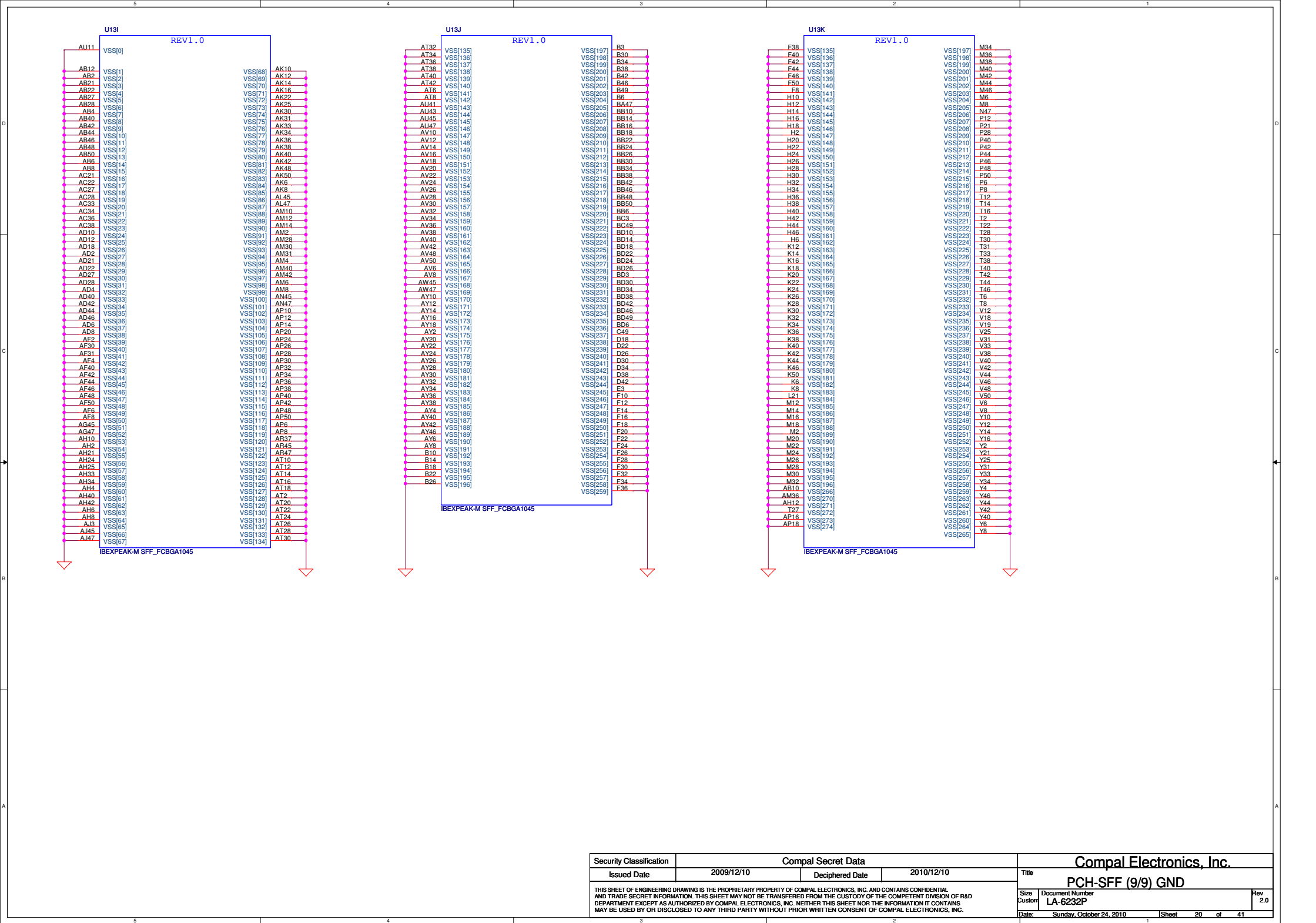


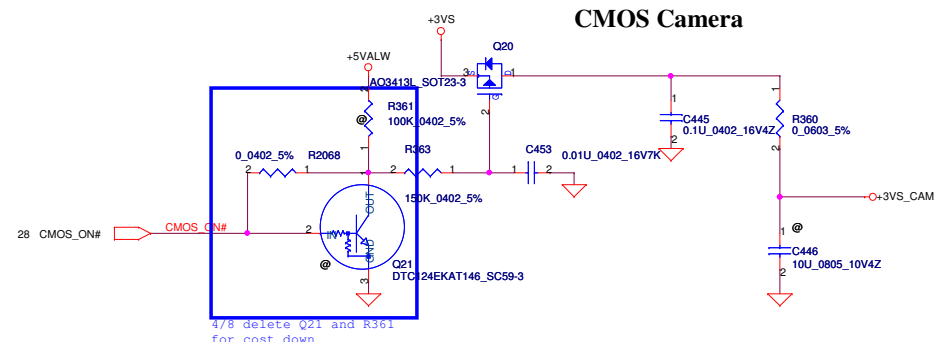
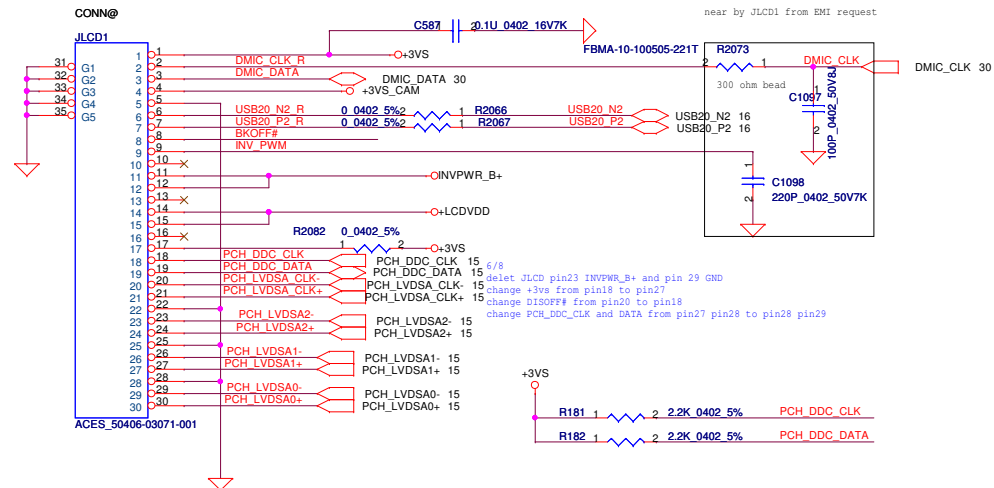
modify 12/24

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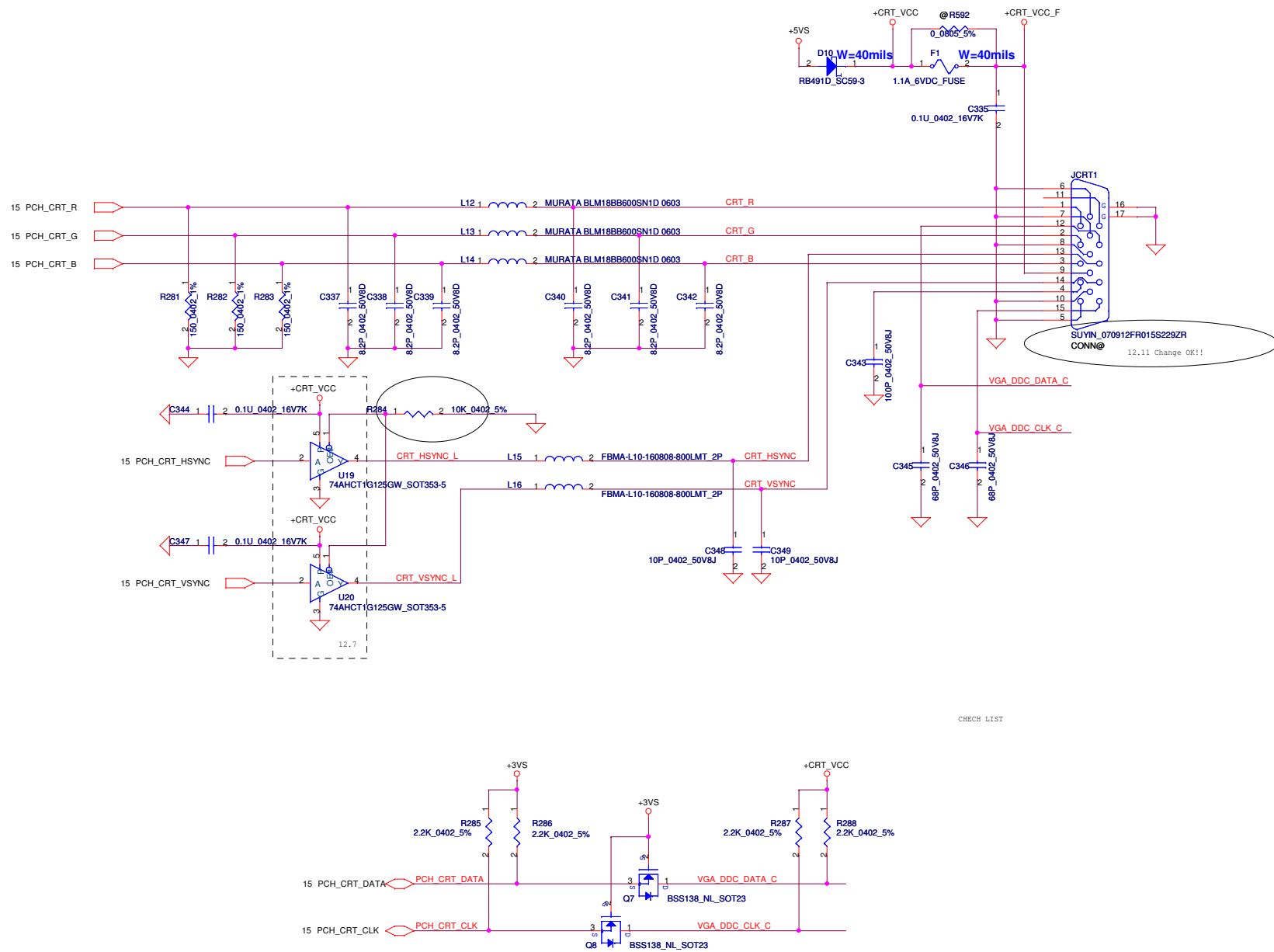






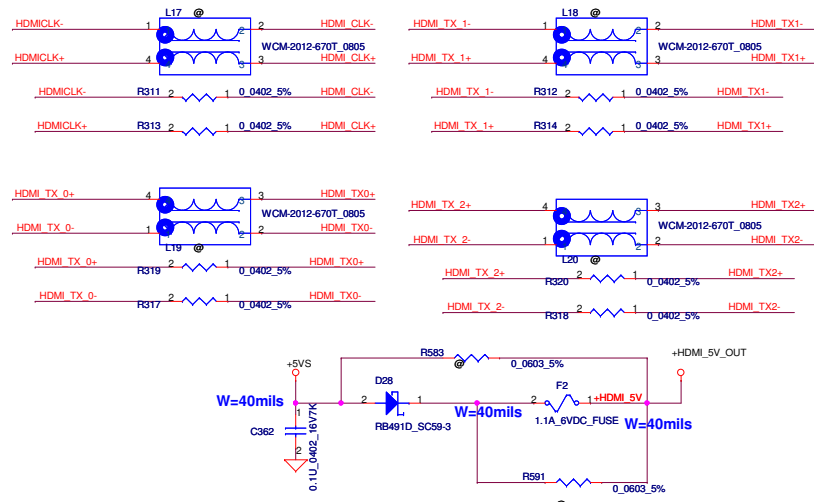
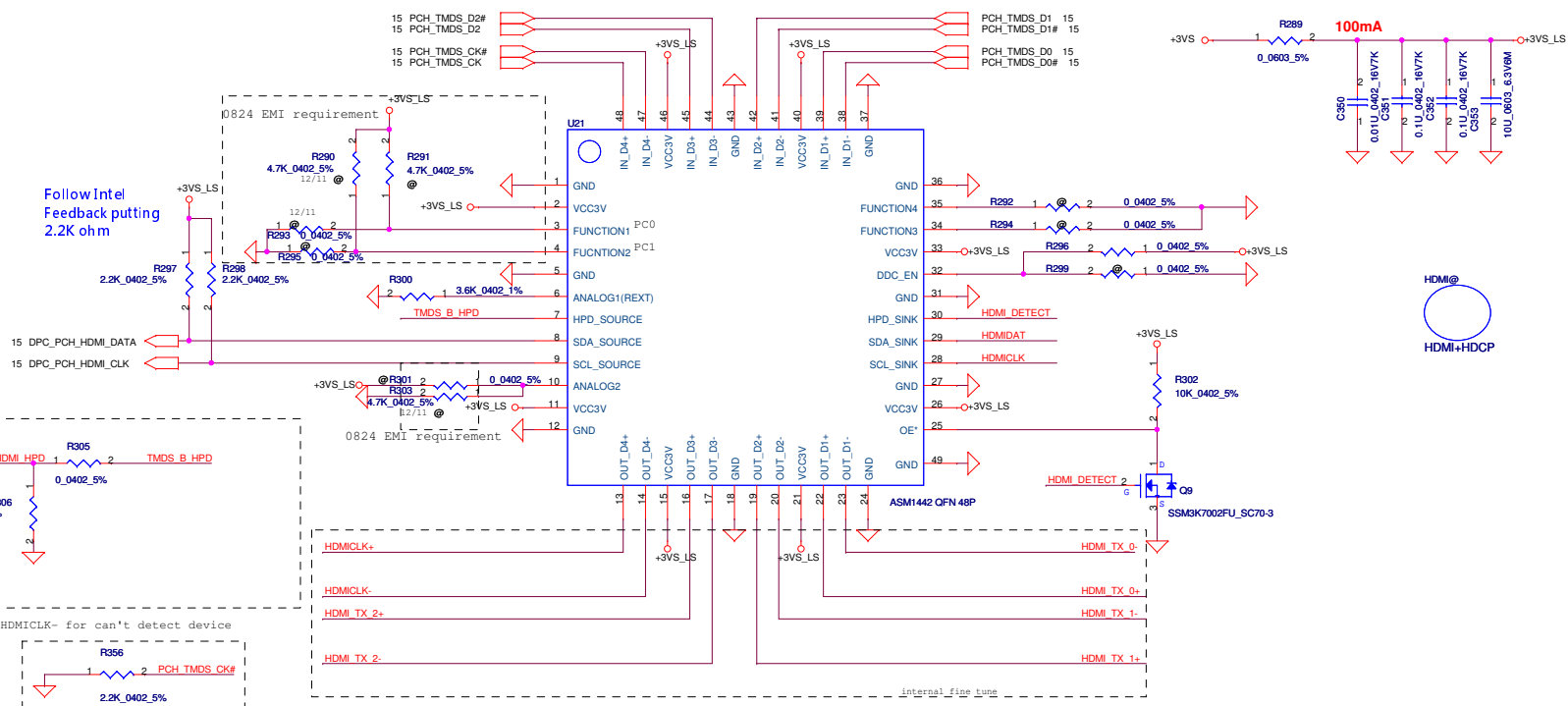


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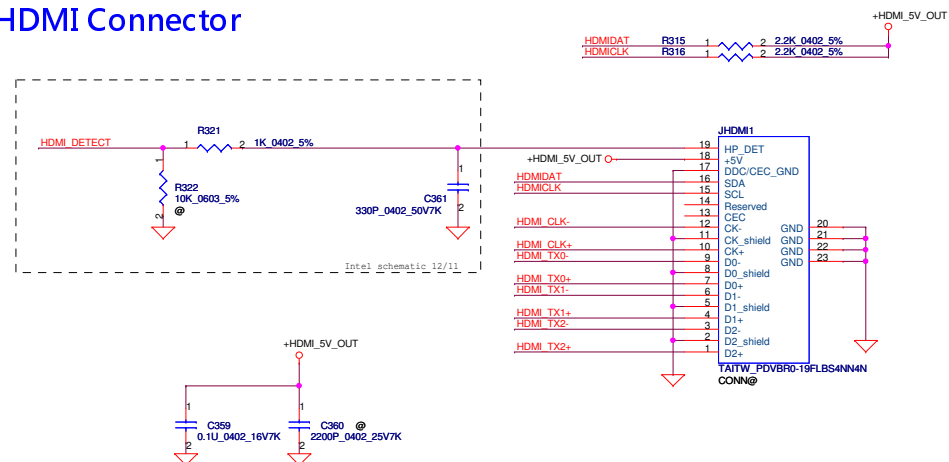


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				CRT Conn			
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EQUALIZATION SETTING:
[PC1,PC0]=00,8dB
[PC1,PC0]=01,4dB (Recommended)
[PC1,PC0]=10,12dB
[PC1,PC0]=11,0dB

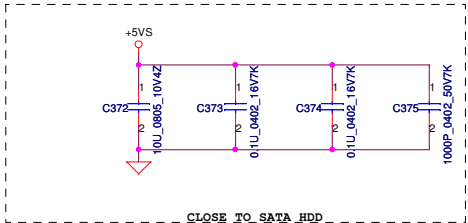
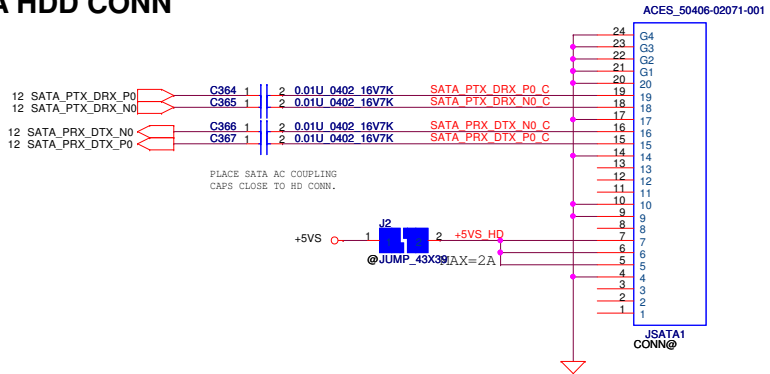


HDMI Connector

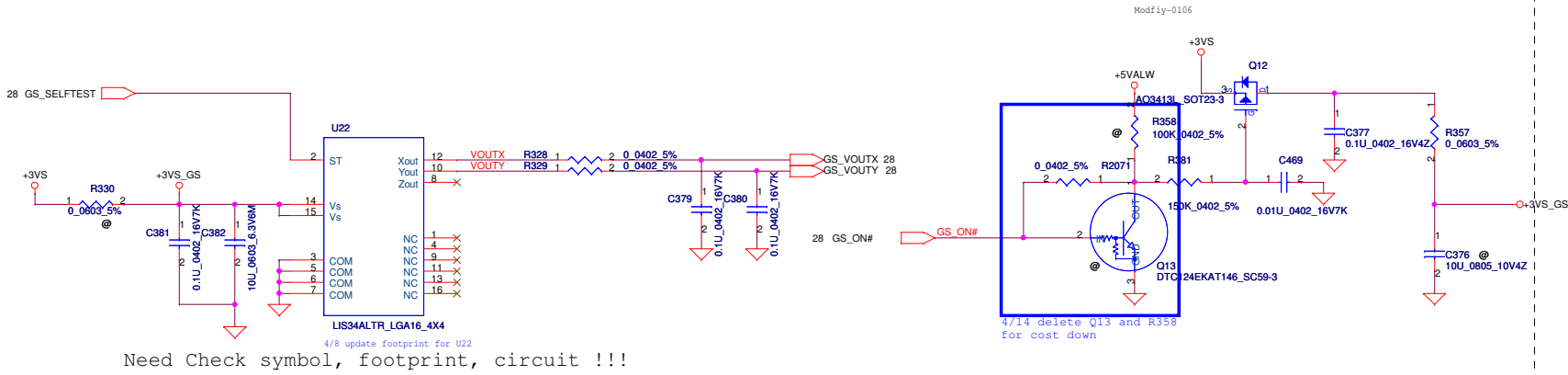


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Issued Date	2009/12/10	Deciphered Date	2010/12/10	Title	HDMI LS & Conn	
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				Custom	LA-6232P	2.0
Date:				Sunday, October 24, 2010	Sheet	23 of 41

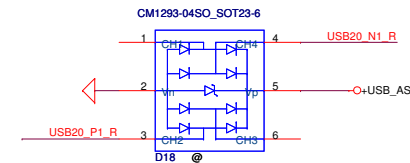
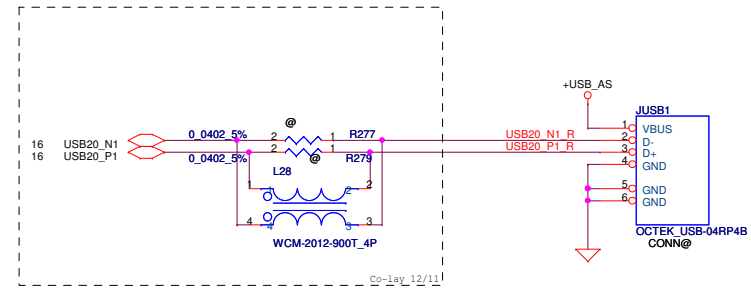
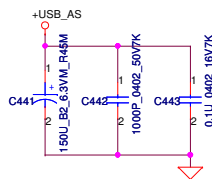
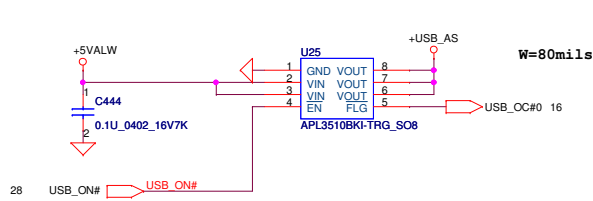
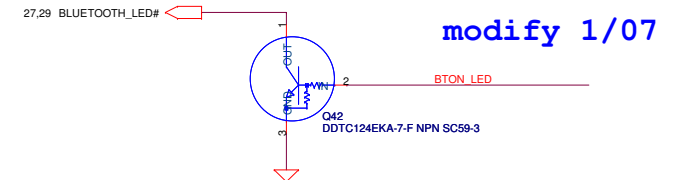
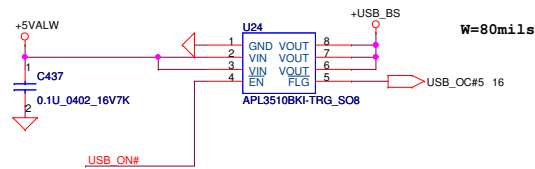
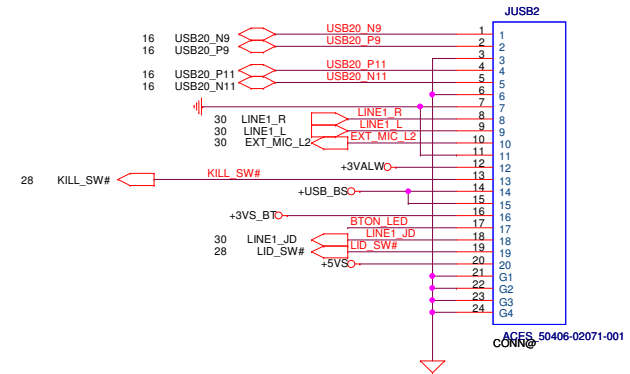
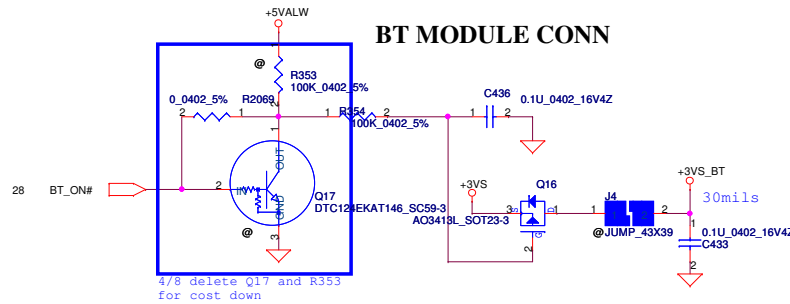
SATA HDD CONN



APS G-Sensor

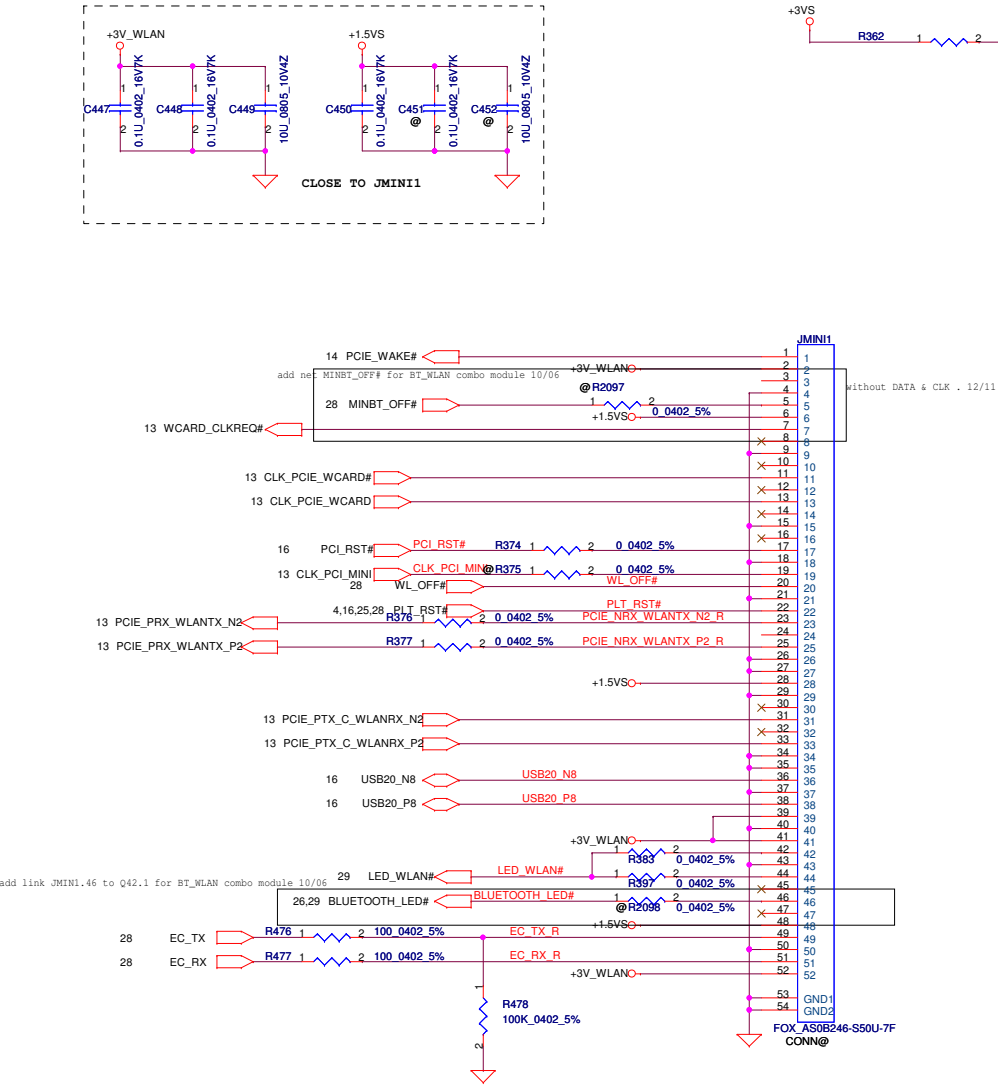


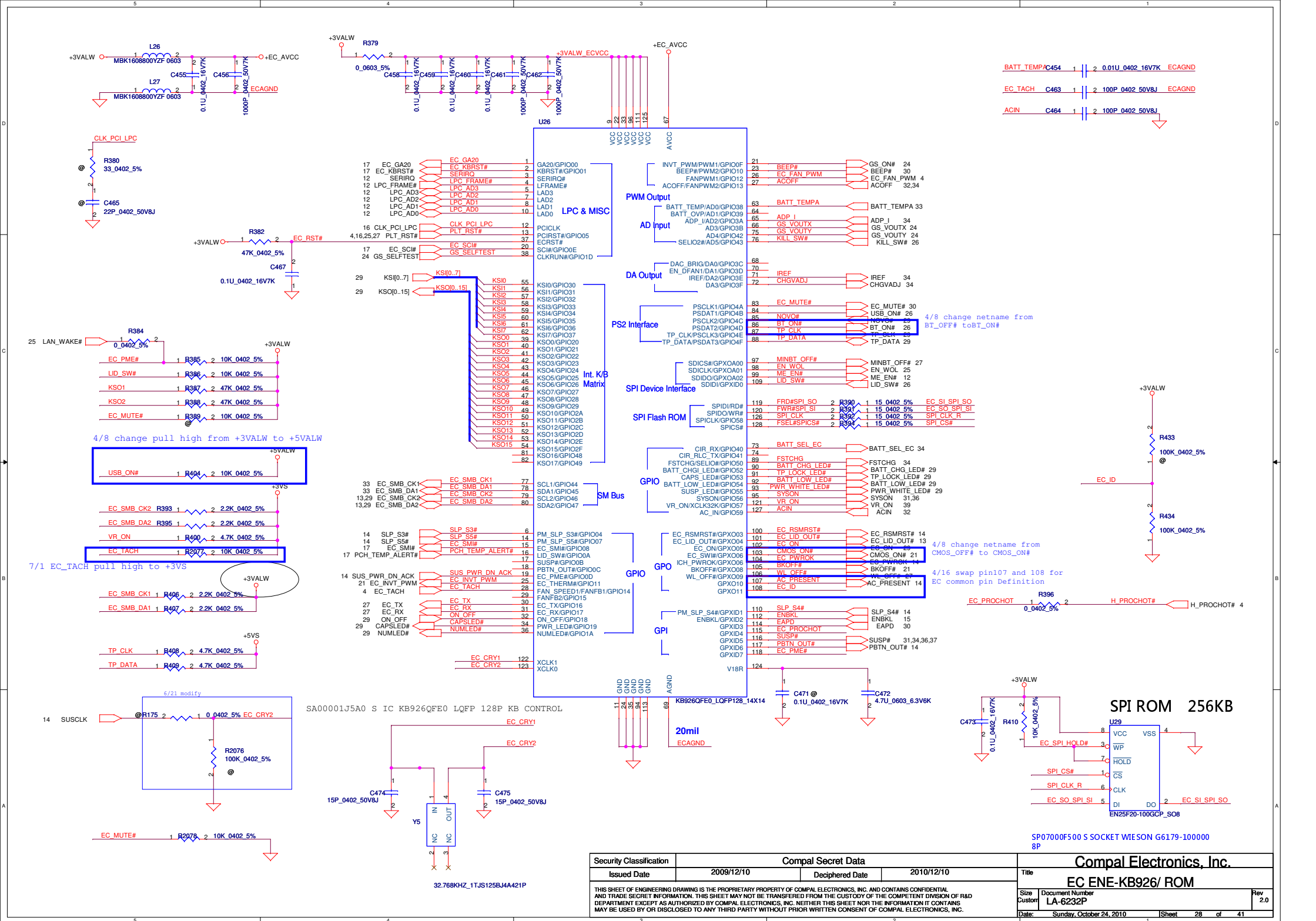
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2009/12/10		2010/12/10		Size	Rev
CUSTOM		LA-6232P		24	2.0
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				USB/ BT/ FP			
				Size		Document Number	
				LA-6232P		2.0	
				Date: Sunday, October 24, 2010		Sheet 26 of 41	

MINI-EXPRESS CARD - WLAN





28 KSI[0..7] ← KSI[0..7]

28 KSO[0..15] ← KSO[0..15]



	JKB1
KS11	1
KS17	2
KS16	3
KS09	4
KS4	5
KS15	6
KS00	7
KS12	8
KS13	9
KS05	10
KS01	11
KS10	12
KS02	13
KS04	14
KS07	15
KS08	16
KS06	17
KS03	18
KS012	19
KS013	20
KS014	21
KS011	22
KS010	23
KS015	24

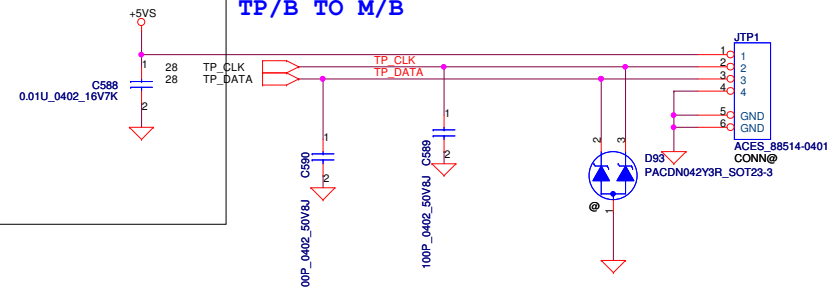
25
26

GN1
GN2

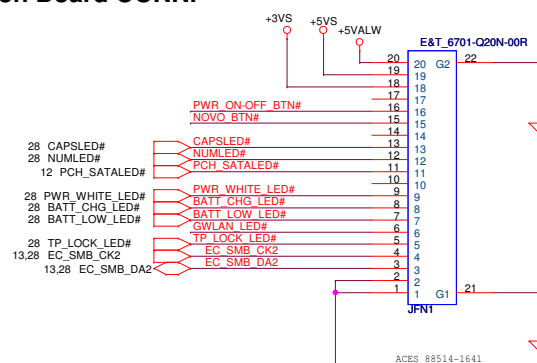
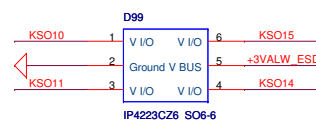
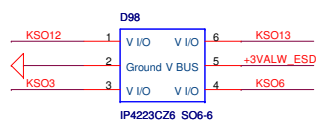
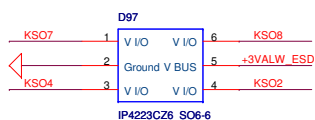
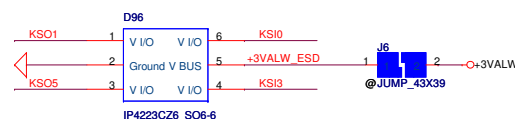
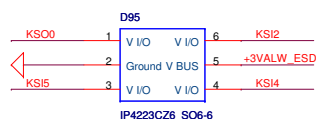
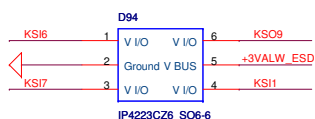
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CONN®

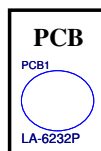
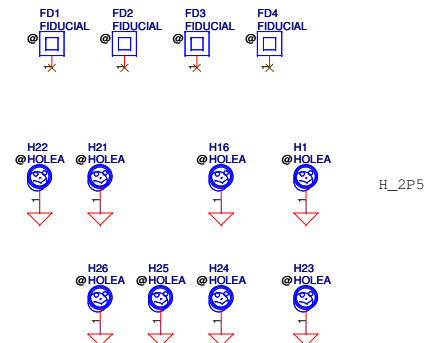
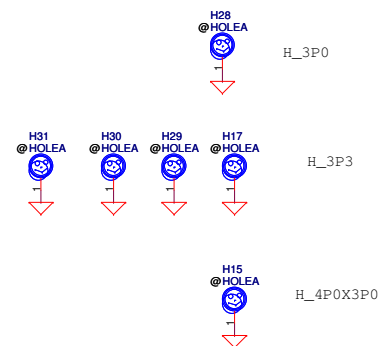
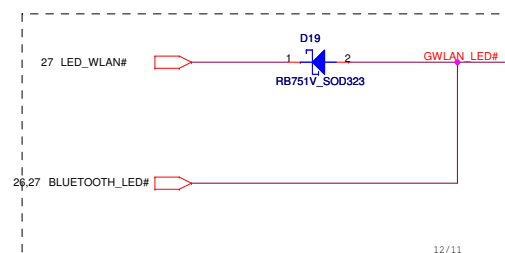
TP/B TO M/B



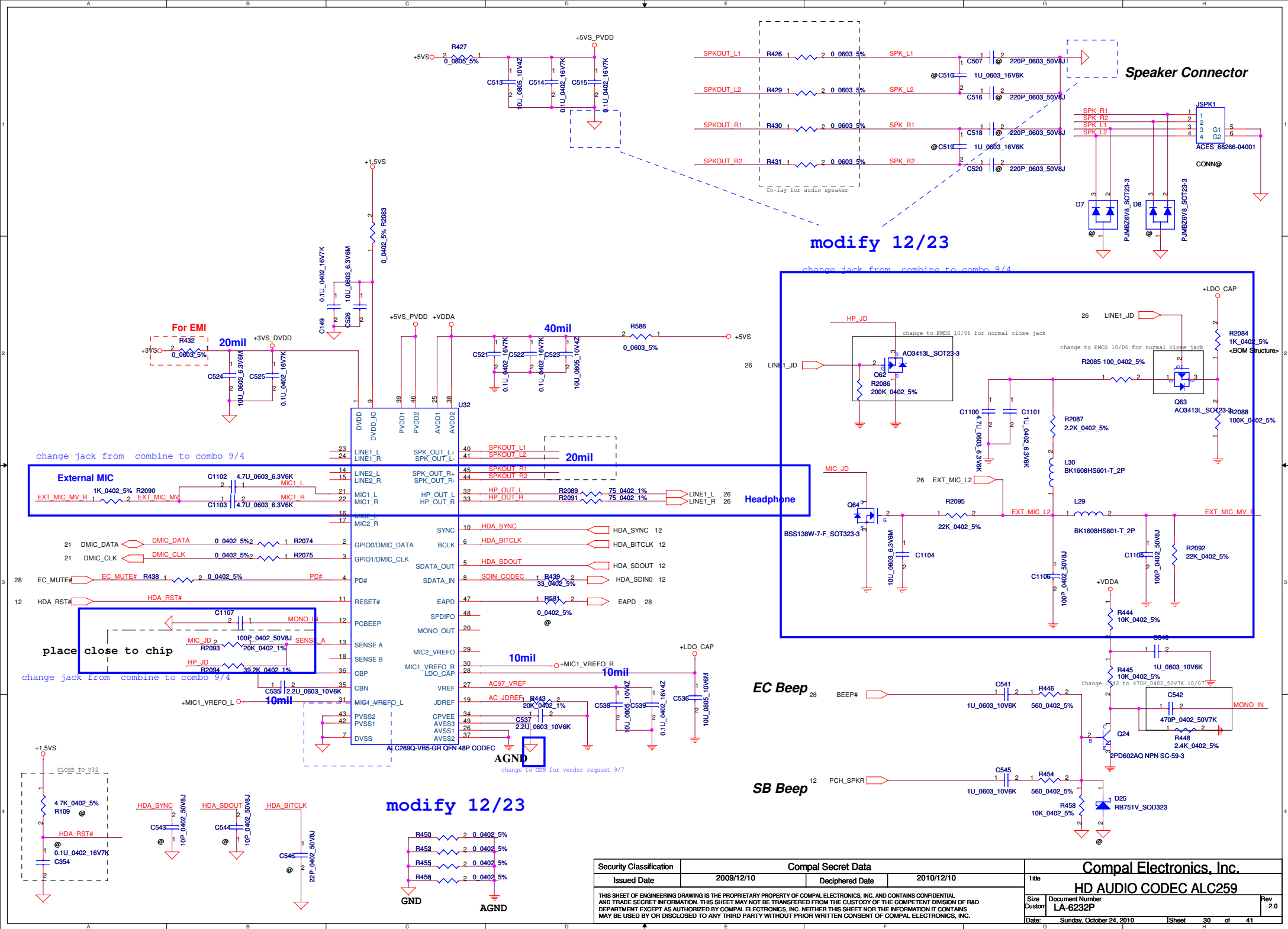
near by JKB1 from ESD request



The schematic diagram shows the internal circuit of a button. A +3VALW supply is connected to a 100K_0402_5% resistor R423. The other end of R423 is connected to a diode D21 (cathode to +3VALW, anode to pin 2 of DAN202U_SC70). Pin 1 of DAN202U_SC70 is connected to PWR_ON_OFF_BTN#. Pin 3 of DAN202U_SC70 is connected to a MOSFET Q22 (SSM3K7002FU_SC70-3) and a 51_ON# signal. The MOSFET Q22 has its gate connected to pin 2 of DAN202U_SC70, its drain connected to a 10K_0402_5% resistor R2072, and its source connected to ground. The MOSFET Q22 is also connected to an EC_ON signal. The MOSFET Q22 is labeled with 'D' and 'G' on its gate, 'D' on its drain, and 'S' on its source. The MOSFET Q22 is also connected to a +3VALW supply.

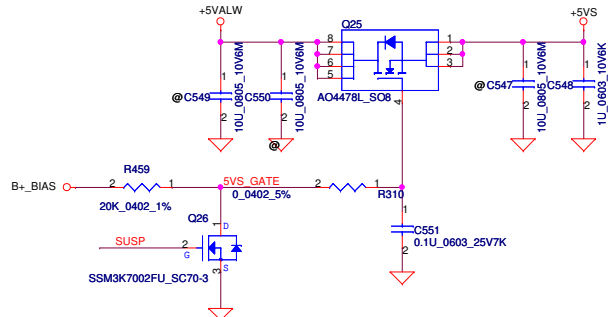


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						KB/ TP/ FUNC/ LED		
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						Custom	LA-6232P	2.
						Date:	Sunday, October 24, 2010	Sheet

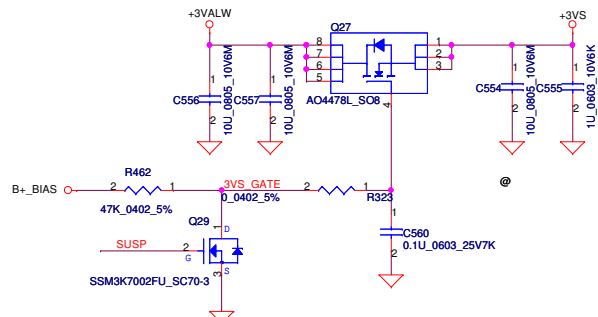


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				Document Number	2.0
				LA-6232P	
Date: Sunday, October 24, 2010		Sheet 30 of 41			

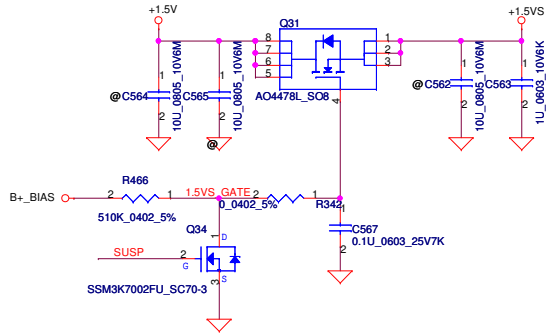
+5VALW TO +5VS



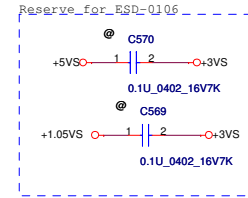
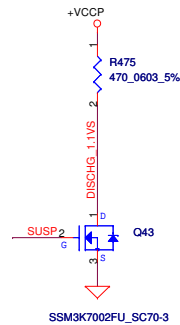
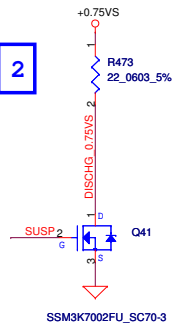
+3VALW TO +3VS



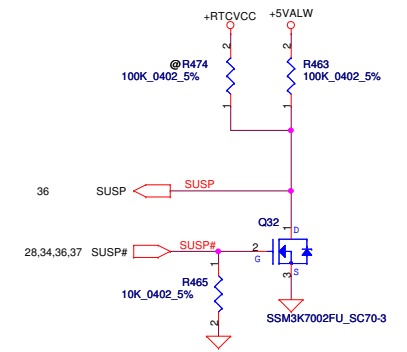
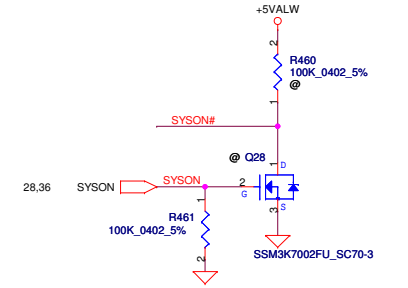
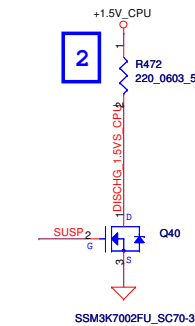
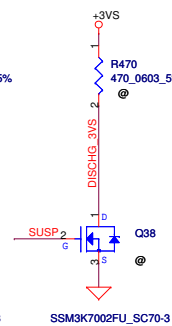
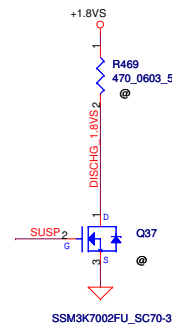
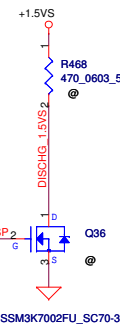
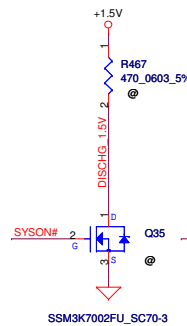
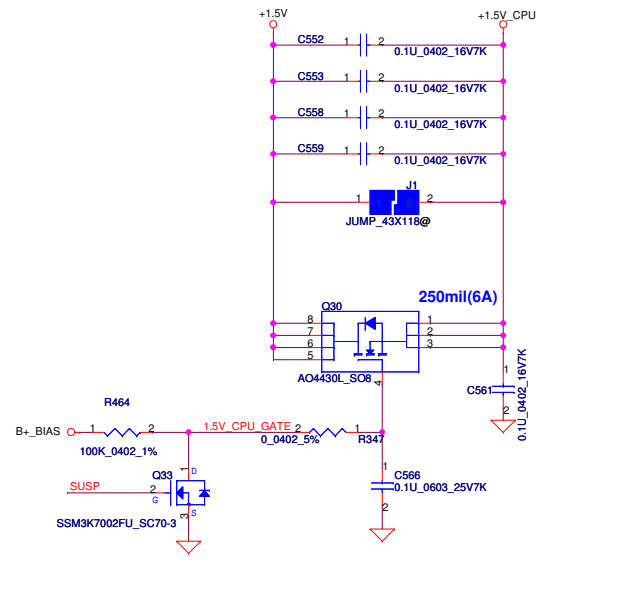
+1.5V to +1.5VS



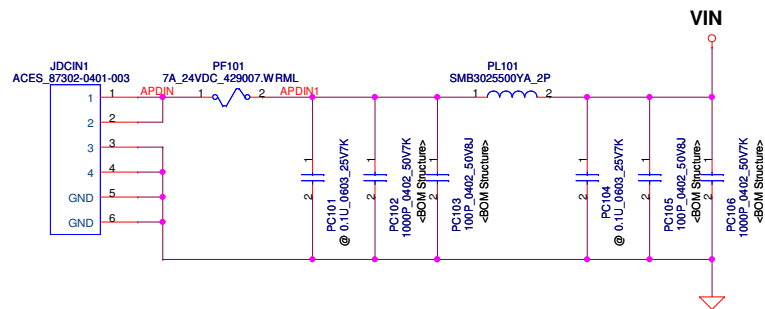
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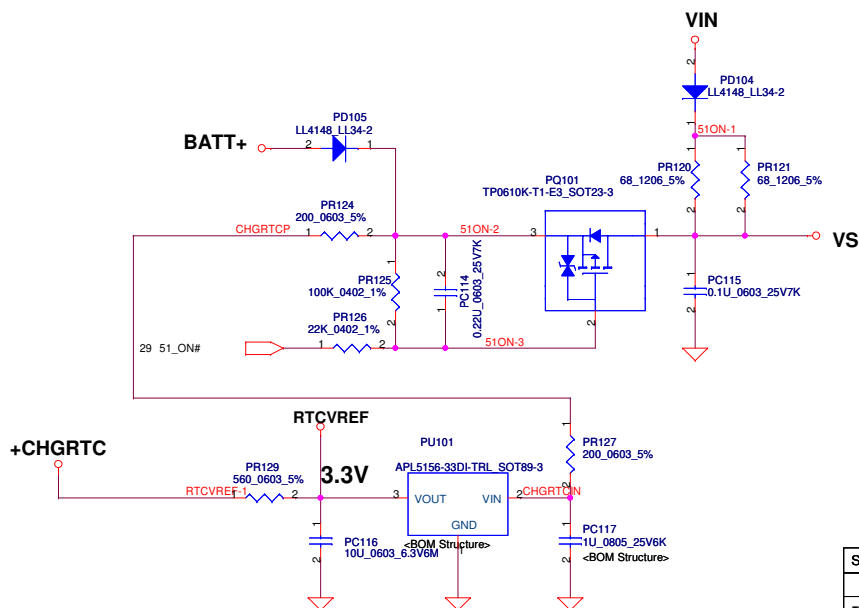
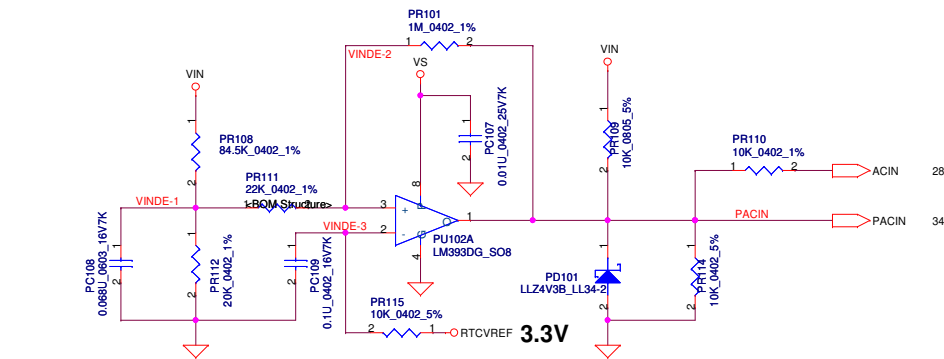
For Calpella CPU S3 DRAM Power (1.5V_CPU VDDQ)



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Size	Custom	Document Number	LA-6232P	Rev	2.0
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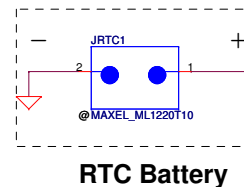
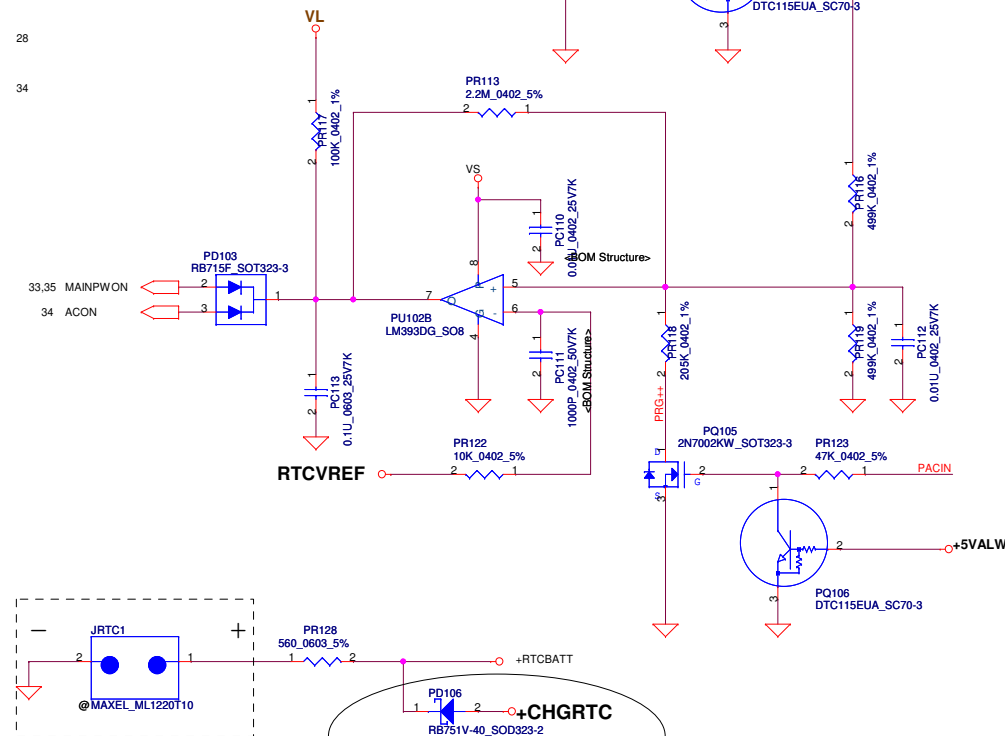
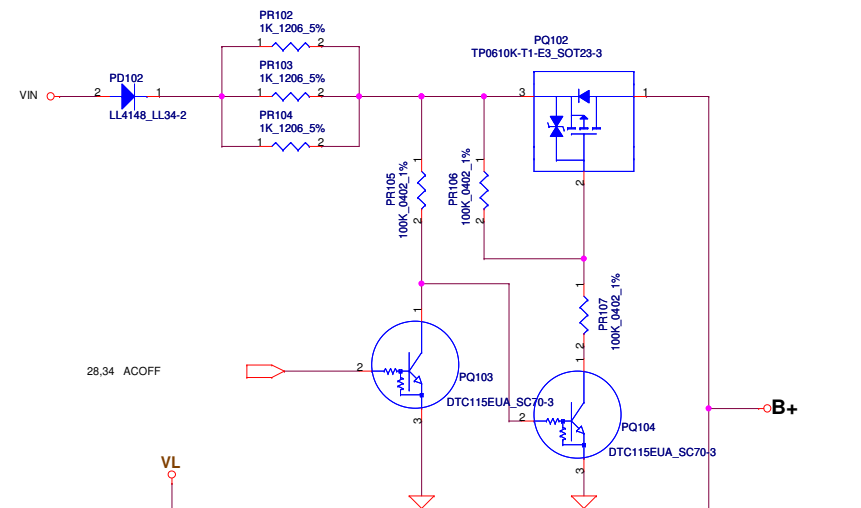


Vin Detector			
	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

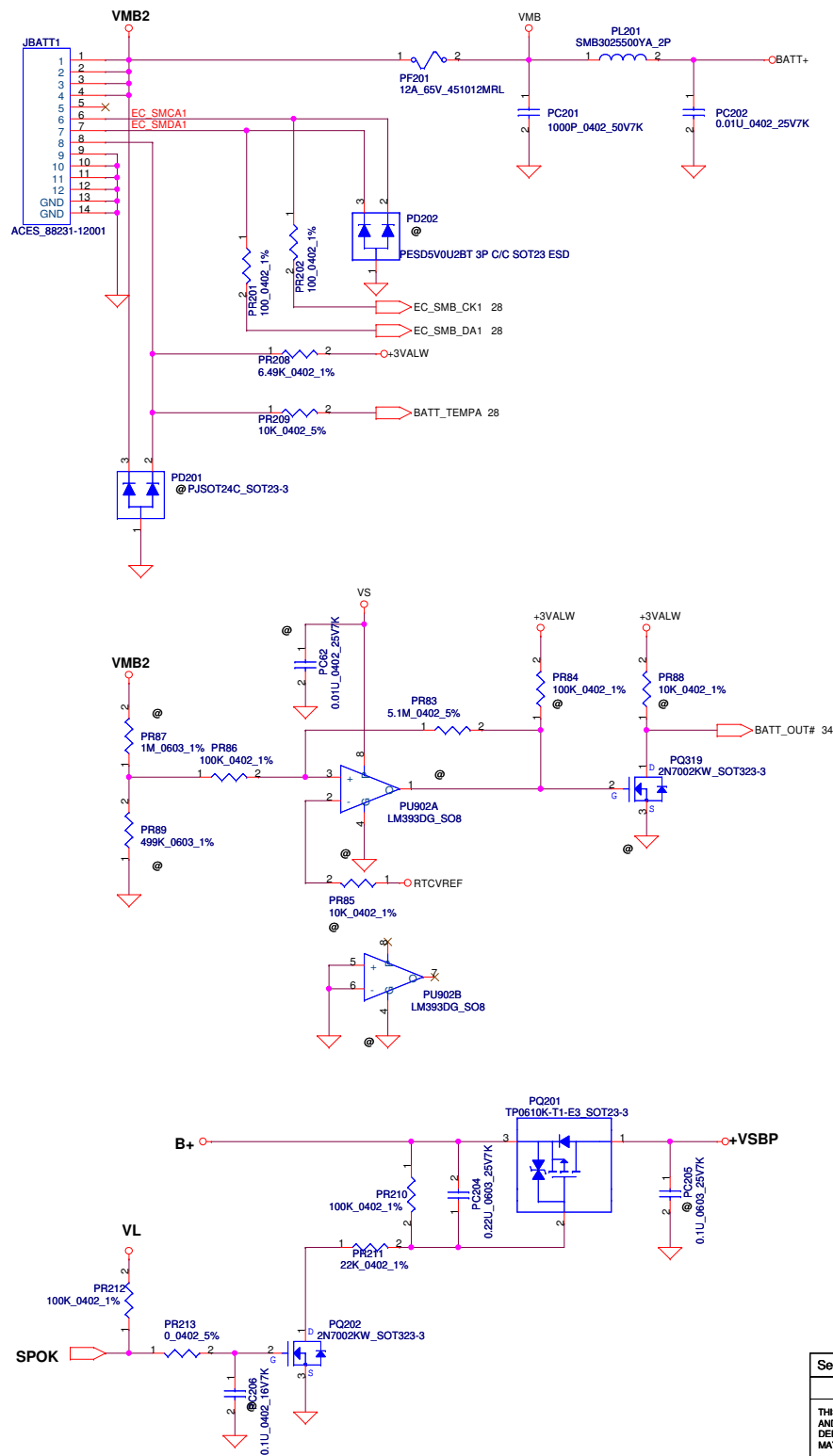


ACIN			
Precharge detector			
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

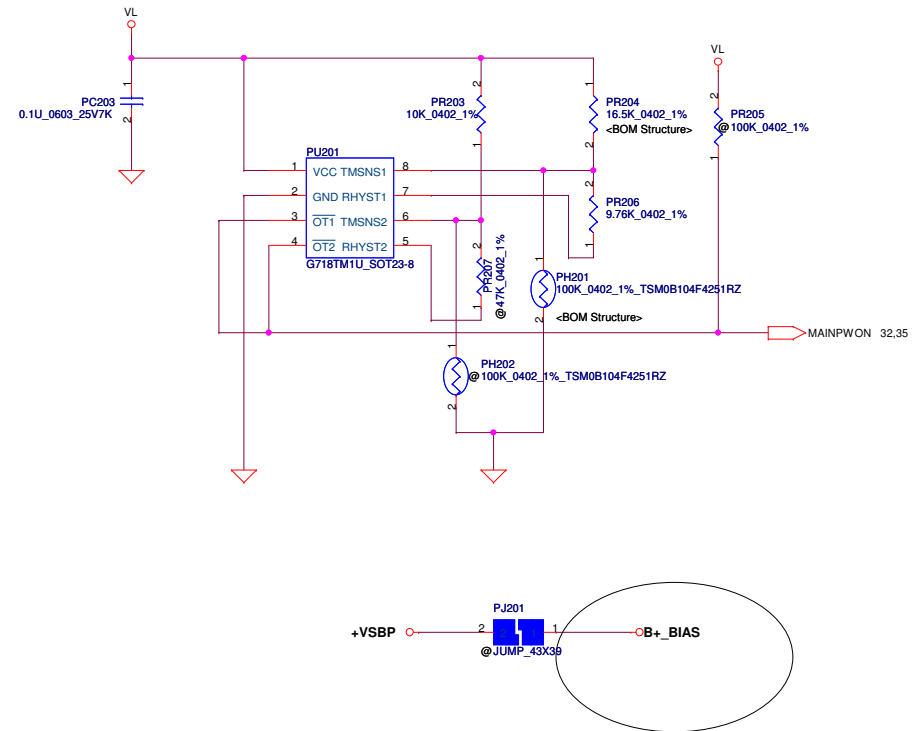
BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



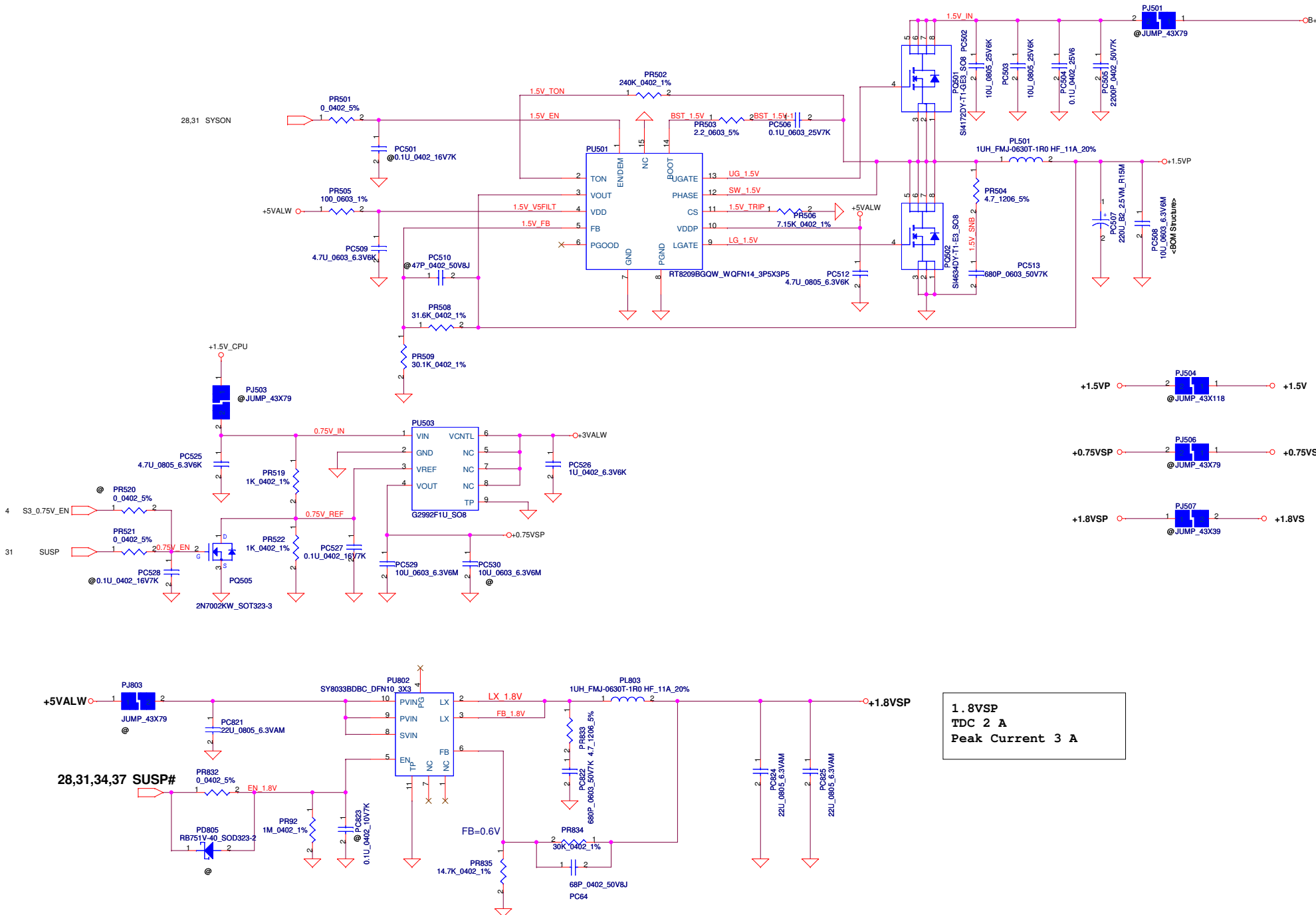
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Compal Electronics, Inc.			
DCIN & DETECTOR			
Size	Document Number	Rev	
Custom	NAU01_MB LA-6102P Schematics	2.0	
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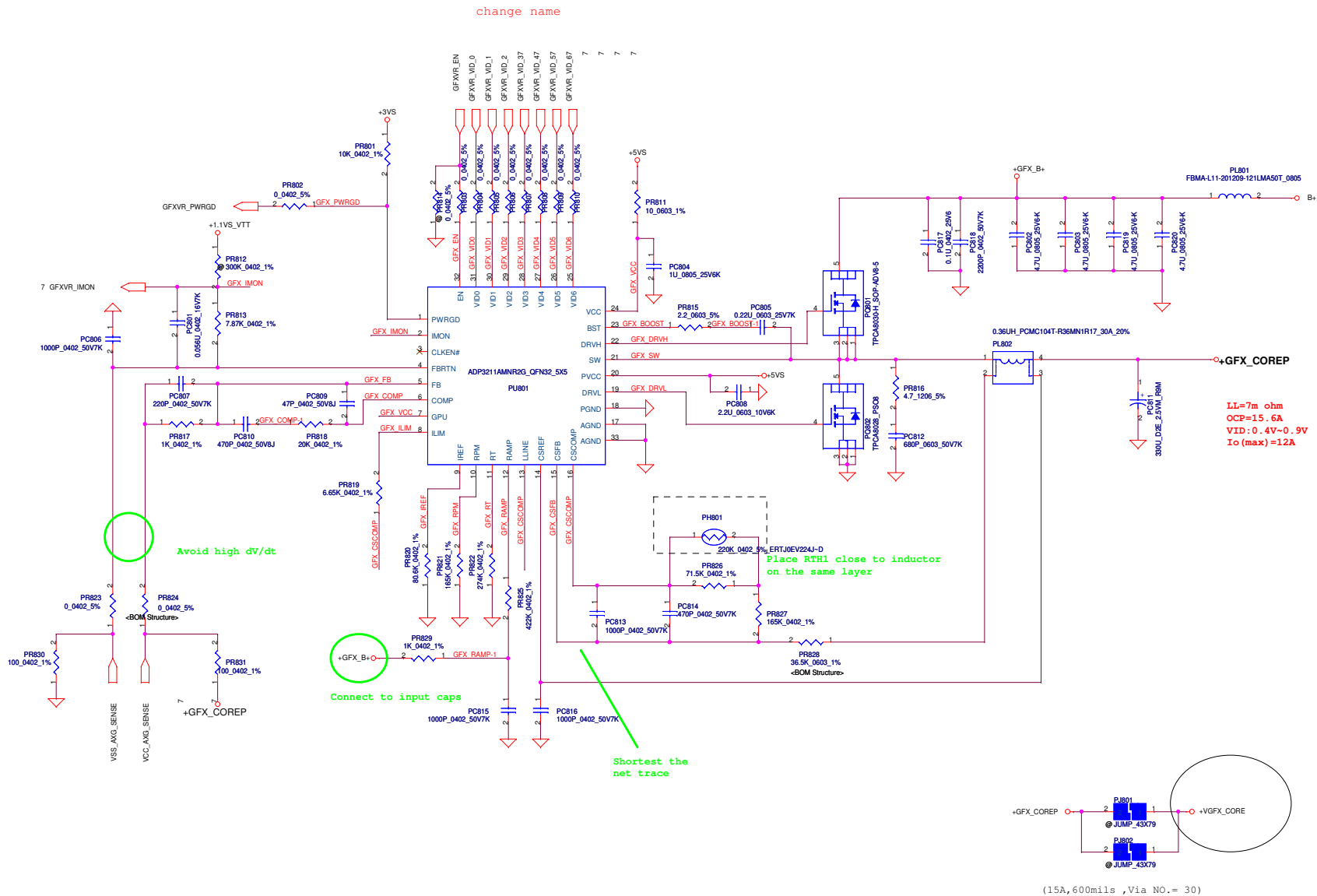
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



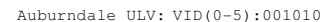
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								Size	Document Number						Rev	
									NAU01_MB LA-6102P Schematics						2.0	
								Date:		Sunday, October 24, 2010			Sheet		33	of 41



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Size		Document Number			Rev
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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	For improve the trainsent of GFX	P38	Modify PR828 from 42.2k to 36.5k and PC814 from 270P to 470P	2010.06.07	EVT
2	For improve the trainsent of CPU	P39	Modify PR928 from 95.3k to 91k and PC917 from 270P to 1200P	2010.06.07	EVT
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17				20081022	

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	For current leakage	P07	Change L2 from +1.5V to +1.5V_CPU	2010-0119	EVT
2	For pin swap of JTP1	P31	Pin1->VDD, Pin2->NC, Pin3->DATA, Pin4->NC, Pin5->CLK, Pin6->GND	2010-0119	EVT
3	For internal speaker no sound	P32	non stuff C506, C516, C518, C520	2010-0128	EVT
4	For can't detect some HDMI divce(module design)	P25	Add R356 for HDMICLK-	2010-0128	EVT
5	For LVDS cable fail rate improve	P23	Swap LED panel power pin and camera and digital mic pin	2010-0128	EVT
6	add for EC circuit	P23	Add R405 for CLK_RUN use by GPIO pull down 10k	2010-0210	EVT
7	For cost down	P21 P26	non stuff Q21 and R361 non stuff Q17 and R353 change netname from CMOS_OFF# to CMOS_ON# change netname from BT_OFF# to BT_ON#	2010-0408	EVT
8	For USB flash when plugging AC	P28	change USB_ON# pull high from +3VALW to +5VALW	2010-0408	EVT
9	For G sensor footprint	P24	update footprint for G sensor(U22)	2010-0408	EVT
10	For cost down	P24	non stuff Q13 and R358 change netname from GS_OFF# to GS_ON#	2010-0414	EVT
11	refer Keyboard spec	P29	Swap JKB1 connector	2010-0413	EVT
12	for EC common pin Definition	P28	swap pin107 and 108	2010-0416	EVT
13	For wireless re-detect after resume from S3	P26	Move pull hi on KILL_SW# to LS-6233P-R595	2010-0531	DVT
14					
15					
16					
17				20081022	