

Hades_HBS 860M SV
Schematics Document

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EV

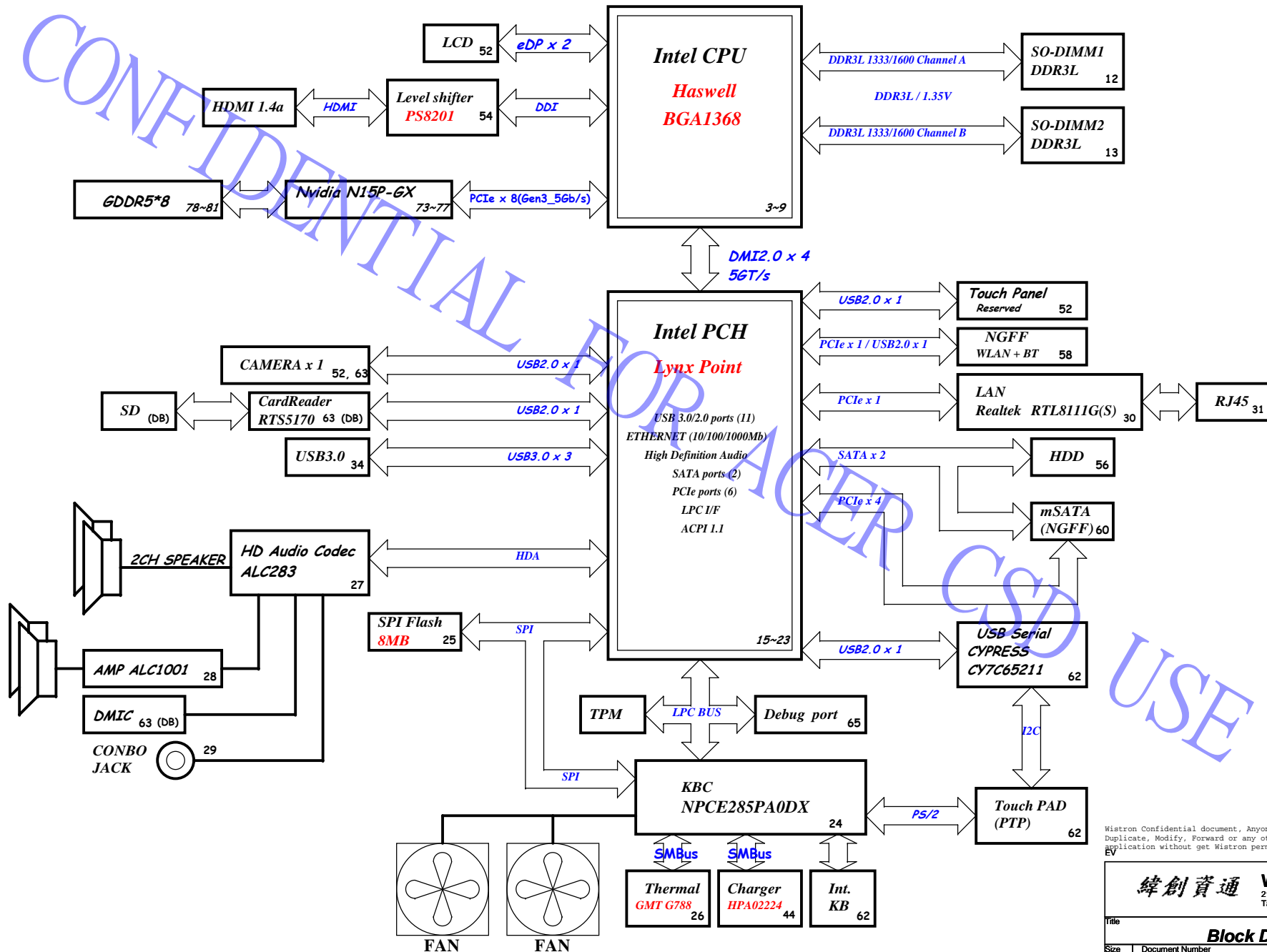
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Title			
Cover Page			
Size A3	Document Number	Rev SB	
Date: Friday, April 11, 2014	Sheet 1 of 102		

Hades_HBS Board Block Diagram

Project code : 4PD02W010001

PCB P/N : 14206

Revision : SB



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Block Diagram		
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SSID = CPU

Layout Note:

Max Length : 400 Mil
W/S (mil):12.0/15.0



<u>x16</u> <u>Controller</u> <u>Negotiated</u> <u>Width</u>	<u>x8</u> <u>Controller</u> <u>Negotiated</u> <u>Width</u>	<u>x4</u> <u>Controller</u> <u>Negotiated</u> <u>Width</u>	<u>Pro-</u> <u>cessor</u>	<u>Physical Lanes</u>															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
<u>x16</u>	<u>Off</u>	<u>Off</u>	<u>Direct</u>	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
<u>x8</u>	<u>x8</u>	<u>Off</u>	<u>Direct</u>	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
<u>x8</u>	<u>x4</u>	<u>x4</u>	<u>Direct</u>	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
<u>x16</u>	<u>Off</u>	<u>Off</u>	<u>Reverse</u>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<u>x8</u>	<u>x8</u>	<u>Off</u>	<u>Reverse</u>	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
<u>x8</u>	<u>x4</u>	<u>x4</u>	<u>Reverse</u>	3	2	1	0	3	2	1	0	2	6	5	4	3	2	1	0

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Title

CPU (PCIe/DMI/FDI)

Size

Document Number	
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Hades HBS 860M

Rev

Date: Friday, April 11, 2014

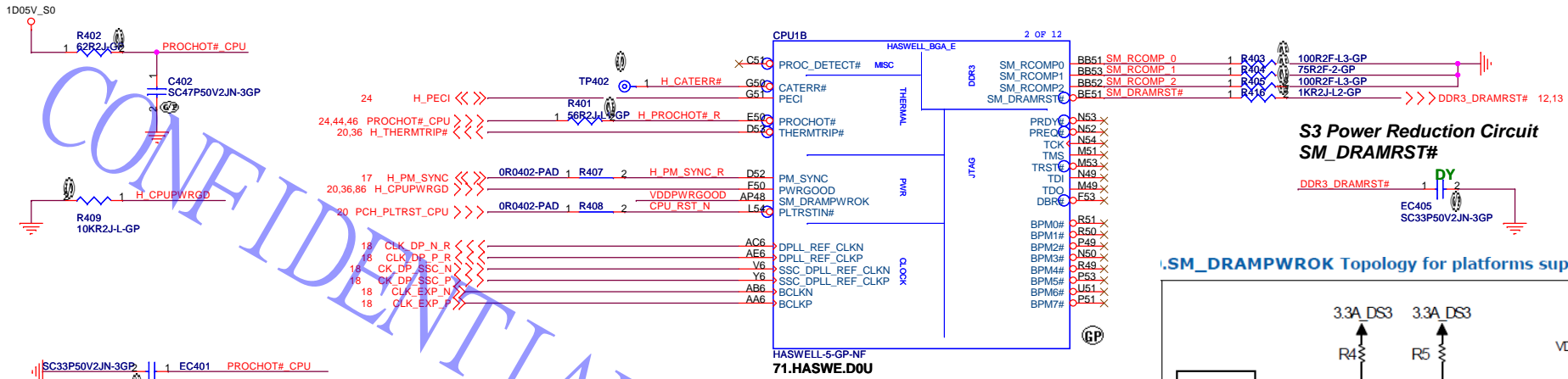
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of

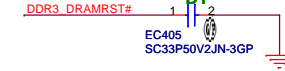
10

SSID = CPU

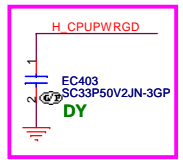
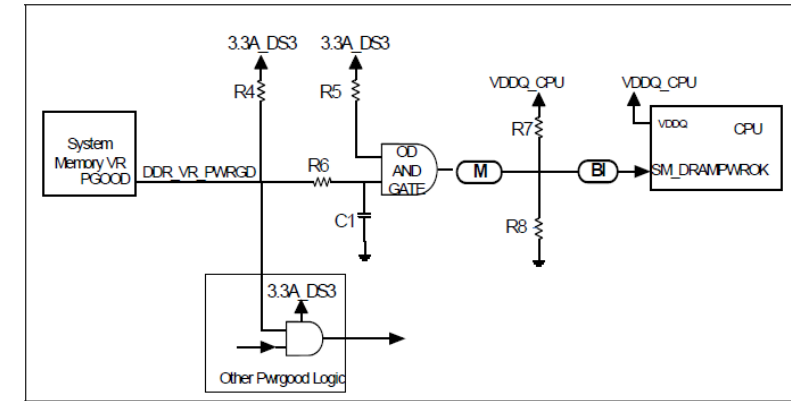
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S3 Power Reduction Circuit SM_DRAMRST#



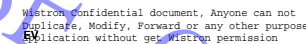
SM_DRAMPWROK Topology for platforms supporting Deep S3

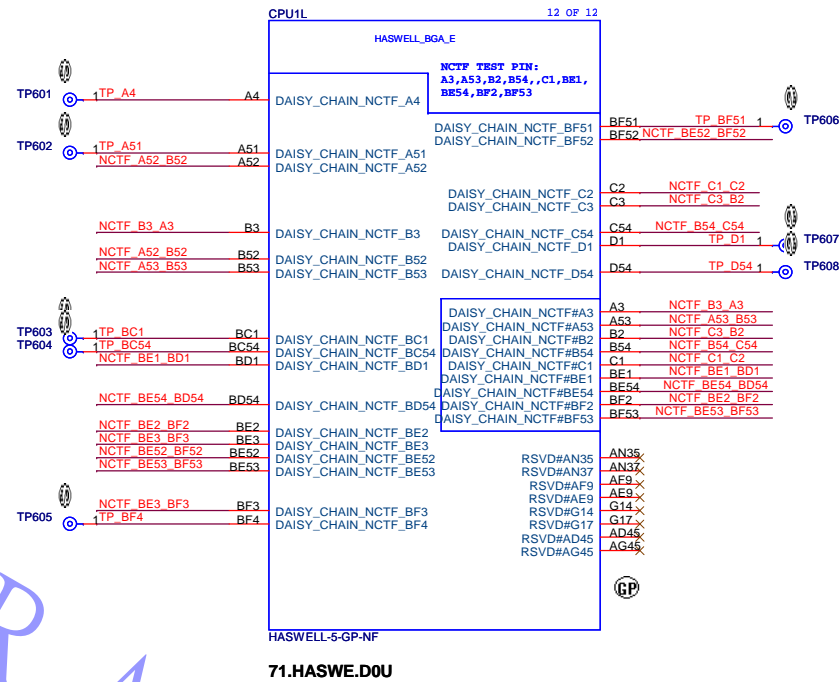


Reserve for EMC

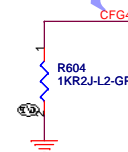
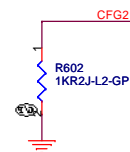
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CPU (THERMAL/CLOCK/PM)			
Size	Document Number	Hades_HBS 860M	
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Date:	Wednesday, May 28, 2014	Sheet 4	of 102

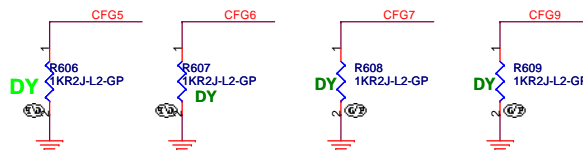




eDP Enable	
CFG4	1:Disable 0:Enable



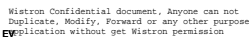
PCIE Port Bifurcation Straps	
CFG[6:5]	<p>11: x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8, x4, x4 - Device 1 functions 1 and 2 enabled</p>



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Title			
CPU (CFG)			
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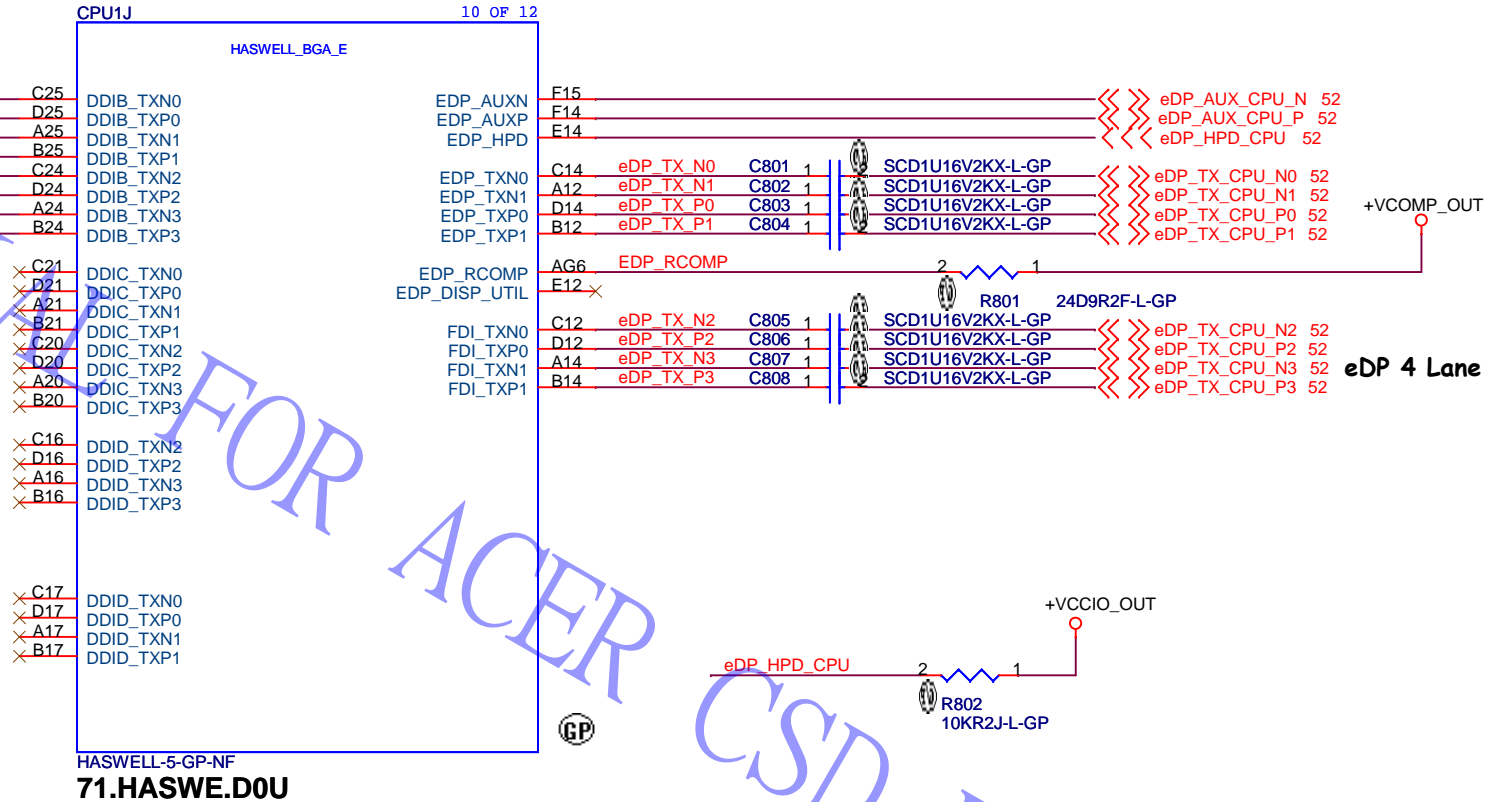


Title			
CPU (VCC_CORE)			
Size	Document Number		Rev
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SSID = CPU

HDMI

54 HDMI_DATA_CPU_N2
54 HDMI_DATA_CPU_P2
54 HDMI_DATA_CPU_N1
54 HDMI_DATA_CPU_P1
54 HDMI_DATA_CPU_N0
54 HDMI_DATA_CPU_P0
54 HDMI_DATA_CPU_N3
54 HDMI_DATA_CPU_P3



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CPU (DDI/EDP)

Size
A4

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SSID = CPU

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CPU1I 9 OF 12

CPU1G 7 OF 12

CPU1H 12 OF 12

HASWELL_BGA_E

HASWELL_BGA_E

HASWELL_BGA_E

HASWELL-5-GP-NF

HASWELL-5-GP-NF

HASWELL-5-GP-NF

71.HASWE.D0U

71.HASWE.D0U

71.HASWE.D0U

VSS_NCTF#A49
VSS_NCTF#A50
VSS_NCTF#A8
VSS_NCTF#B4
VSS_NCTF#BA1
VSS_NCTF#BA54
VSS_NCTF#BB1
VSS_NCTF#BB54
VSS_NCTF#BD2
VSS_NCTF#BD53
VSS_NCTF#BF49
VSS_NCTF#BF5
VSS_NCTF#BF50
VSS_NCTF#BF6
VSS_NCTF#C53
VSS_NCTF#D2
VSS_NCTF#E54
VSS_NCTF#F54
VSS_NCTF#G1

VSS_SENSE

>>> VSS_SENSE 746

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CPU (VSS)

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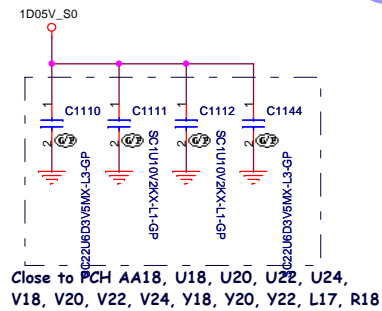
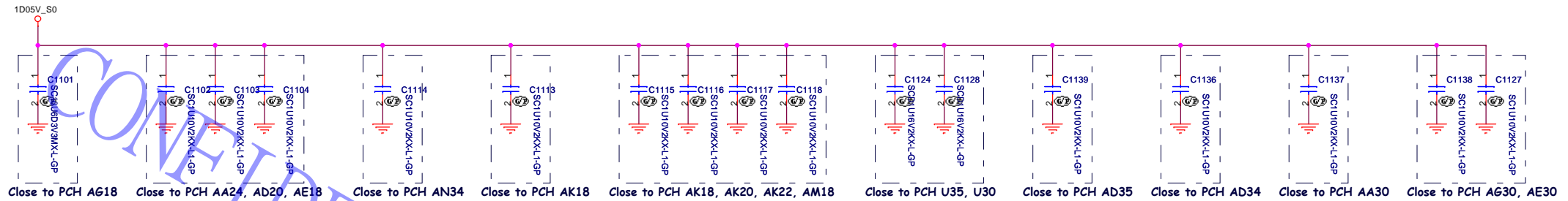
CPU (Power CAP1)

Rev

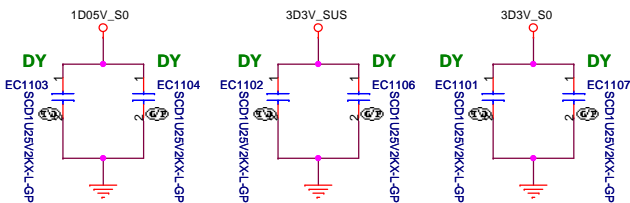
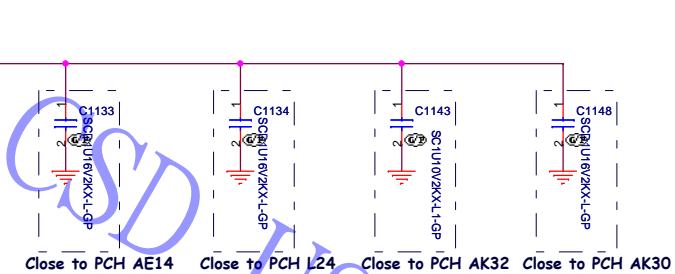
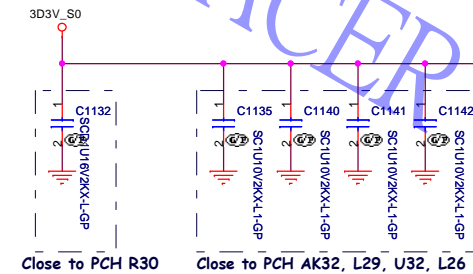
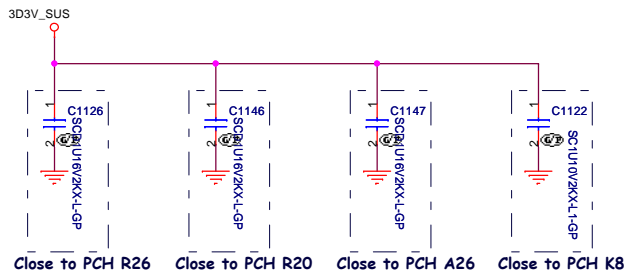
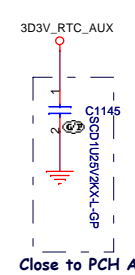
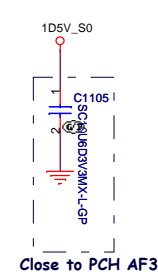
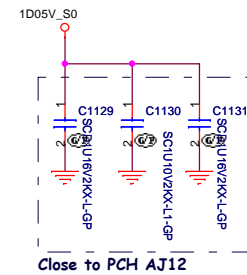
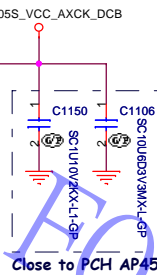
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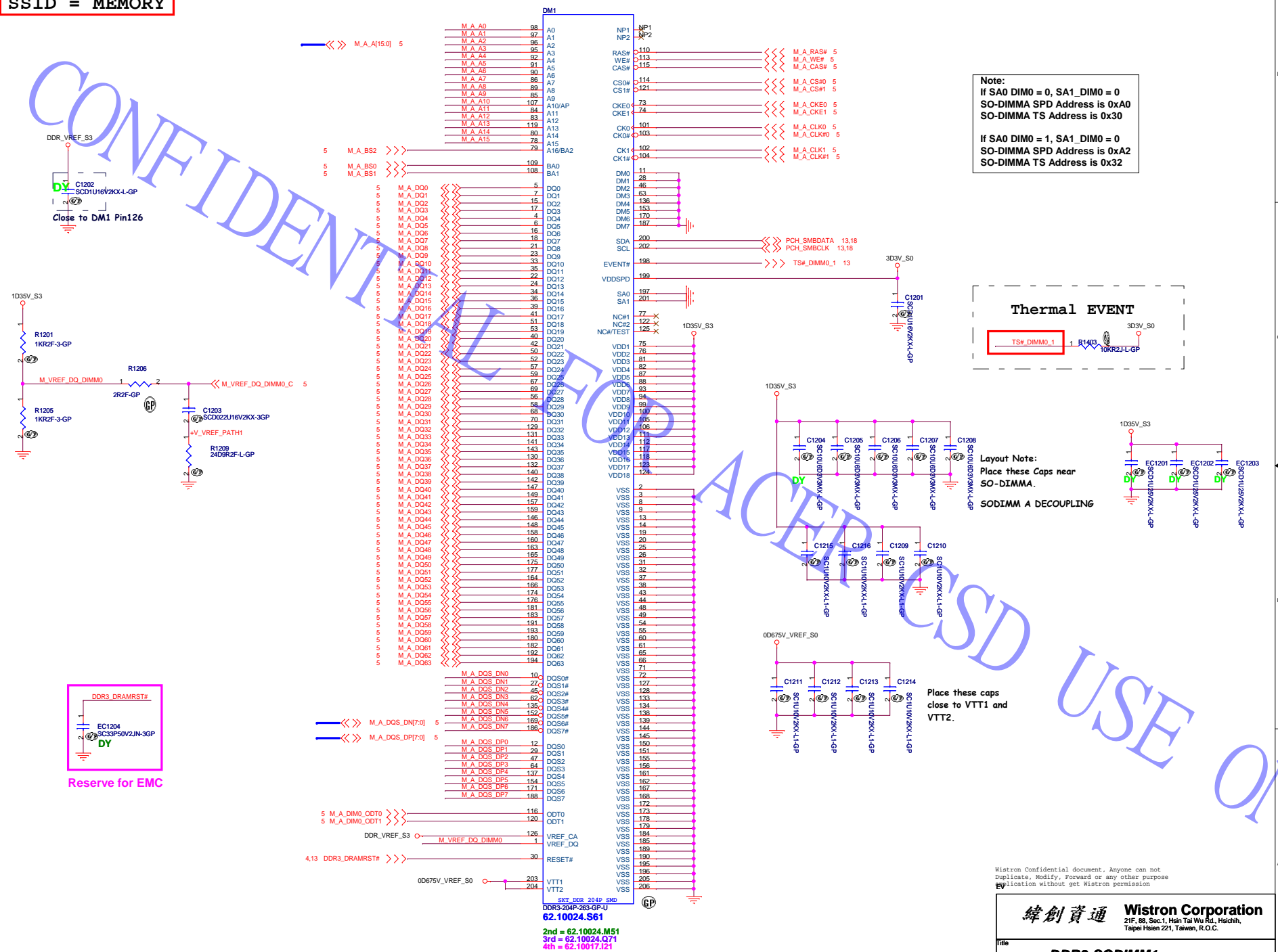
For BOM cost saving,
Inductor can be replaced with 0ohm resistor,
and remain capacitor placeholder.
1uF BSC must be stuffed



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CPU (Power CAP2)			
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SSID = MEMORY



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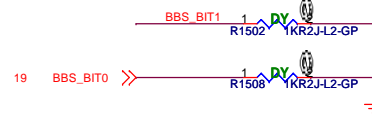
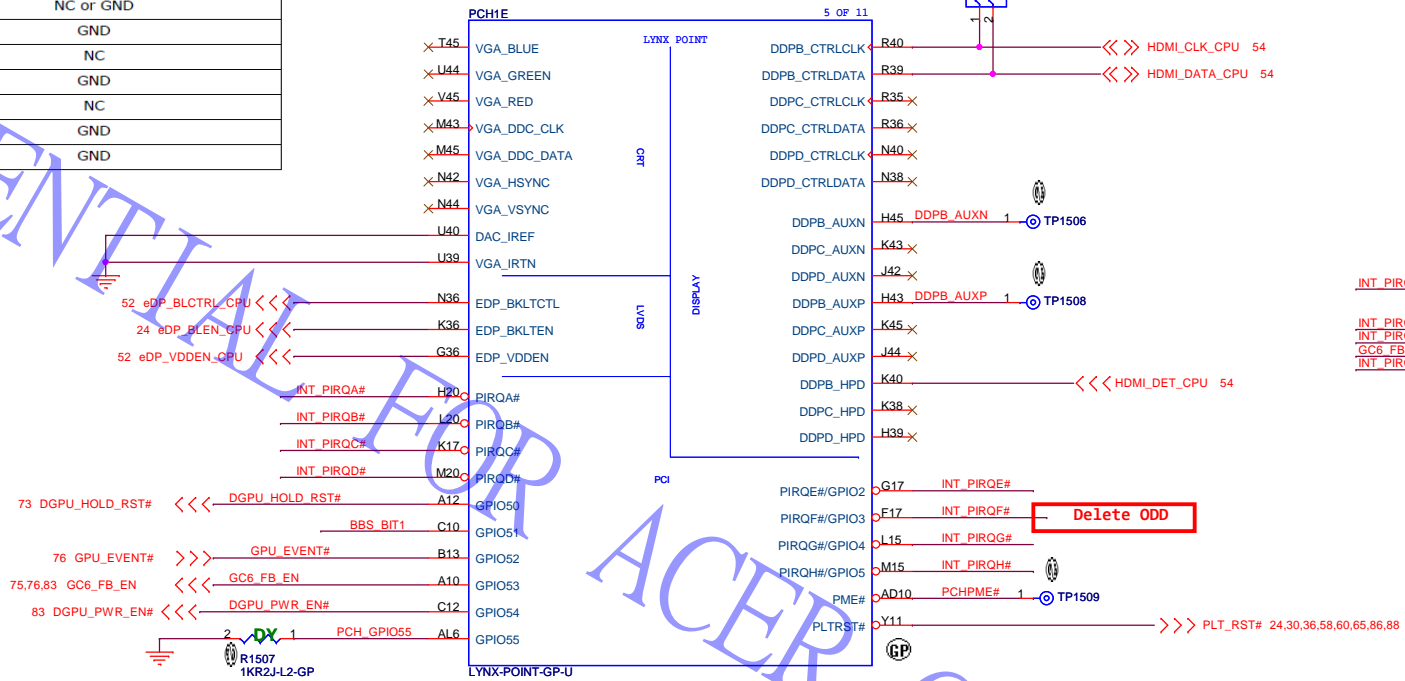
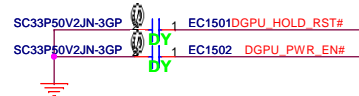
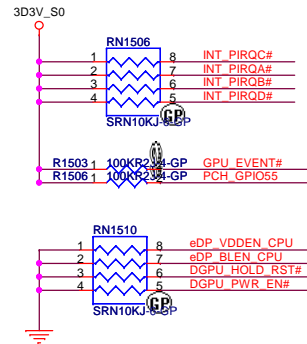
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File		(Reserved) SODIMM_SODIMM4	
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SSID = PCH

VGA DAC Disable Recommendations

Signal Name	Recommended Connection
VGA_RED, VGA_GREEN, VGA_BLUE	NC or GND
VGA_IRTN	GND
VGA_HSYNC, VGA_VSYNC	NC
DAC_IREF	GND
DDC_CLK, DDC_DATA	NC
VCCADAC	GND
VCCADACBG	GND



BOOT BIOS Strap		
GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

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CPU(EDP SIDE BAND/GPIO/DDI)		SB	
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SSID = PCH

USB port2

34 USB30_RX_CPU_N3 >>> AW31
 34 USB30_RX_CPU_P3 >>> AY31
 34 USB30_TX_CPU_N3 <<< BE32
 34 USB30_TX_CPU_P3 <<< BC32

AW31 PERN1/USB3RN3
 AY31 PERP1/USB3RP3
 BE32 PETN1/USB3TN3
 BC32 PETP1/USB3TP3
 AT31 PERN2/USB3RN4
 AR31 PERP2/USB3RP4
 BD33 PETN2/USB3TN4
 BB33 PETP2/USB3TP4

WLAN

58.86 PCIE_RX_CPU_N3 >>>
 58.86 PCIE_RX_CPU_P3 >>>
 58.86 PCIE_TX_WLAN_N3 >>>
 58.86 PCIE_TX_WLAN_P3 >>>

LAN

30 PCIE_RX_CPU_N4 >>>
 30 PCIE_RX_CPU_P4 >>>
 30 PCIE_TX_LAN_N4 >>>
 30 PCIE_TX_LAN_P4 >>>

MSATA

PCIE_RX_MSATA_N5 >>>
 PCIE_RX_MSATA_P5 >>>

PCIE_TX_MSATA_N5 >>>
 PCIE_TX_MSATA_P5 >>>

PCIE_RX_MSATA_N6 >>>
 PCIE_RX_MSATA_P6 >>>

PCIE_TX_MSATA_N6 >>>
 PCIE_TX_MSATA_P6 >>>

PCIE_RX_MSATA_N7 >>>
 PCIE_RX_MSATA_P7 >>>

PCIE_TX_MSATA_N7 >>>
 PCIE_TX_MSATA_P7 >>>

60 PCIE_RX_MSATA_N8 >>>
 60 PCIE_RX_MSATA_P8 >>>

60 PCIE_TX_MSATA_N8 >>>
 60 PCIE_TX_MSATA_P8 >>>

60 PCIE_RX_MSATA_N8 >>>
 60 PCIE_RX_MSATA_P8 >>>

60 PCIE_TX_MSATA_N8 >>>
 60 PCIE_TX_MSATA_P8 >>>

NGFF PCIE R1604 1
 NGFF PCIE R1605 1

NGFF PCIE C1624 1
 NGFF PCIE C1623 1

NGFF PCIE R1606 1
 NGFF PCIE R1608 1

NGFF PCIE C1626 1
 NGFF PCIE C1625 1

NGFF PCIE R1609 1
 NGFF PCIE R1610 1

NGFF PCIE C1628 1
 NGFF PCIE C1627 1

NGFF PCIE R1811 1
 NGFF PCIE R1812 1

NGFF PCIE C1630 1
 NGFF PCIE C1629 1

SCD1U16V2KX-L-GP PCIE TX CPU N3
 SCD1U16V2KX-L-GP PCIE TX CPU P3

SCD1U16V2KX-L-GP PCIE TX CPU N4
 SCD1U16V2KX-L-GP PCIE TX CPU P4

SCD1U16V2KX-L-GP PCIE RX CPU N5
 SCD1U16V2KX-L-GP PCIE RX CPU P5

SCD1U16V2KX-L-GP PCIE TX CPU N6
 SCD1U16V2KX-L-GP PCIE TX CPU P6

SCD1U16V2KX-L-GP PCIE RX CPU N7
 SCD1U16V2KX-L-GP PCIE RX CPU P7

SCD1U16V2KX-L-GP PCIE TX CPU N7
 SCD1U16V2KX-L-GP PCIE TX CPU P7

SCD1U16V2KX-L-GP PCIE RX CPU N8
 SCD1U16V2KX-L-GP PCIE RX CPU P8

SCD1U16V2KX-L-GP PCIE TX CPU N8
 SCD1U16V2KX-L-GP PCIE TX CPU P8

SCD1U16V2KX-L-GP PCIE RX CPU N8
 SCD1U16V2KX-L-GP PCIE RX CPU P8

SCD1U16V2KX-L-GP PCIE TX CPU N8
 SCD1U16V2KX-L-GP PCIE TX CPU P8

0R2J-L-GP PCIE RX CPU N5
 0R2J-L-GP PCIE RX CPU P5

0R2J-L-GP PCIE RX CPU N6
 0R2J-L-GP PCIE RX CPU P6

0R2J-L-GP PCIE TX CPU N6
 0R2J-L-GP PCIE TX CPU P6

0R2J-L-GP PCIE RX CPU N7
 0R2J-L-GP PCIE RX CPU P7

0R2J-L-GP PCIE TX CPU N7
 0R2J-L-GP PCIE TX CPU P7

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 0R2J-L-GP PCIE TX CPU P8

0R2J-L-GP PCIE RX CPU N8
 0R2J-L-GP PCIE RX CPU P8

0R2J-L-GP PCIE TX CPU N8
 0R2J-L-GP PCIE TX CPU P8

LYNX POINT

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B37 USB2N0
 D37 USB2P0
 A38 USB2N1
 C38 USB2P1
 A36 USB2N2
 C36 USB2P2
 A34 USB2N3
 C34 USB2P3
 B33 USB2N4
 D33 USB2P4
 F31 USB2N5
 G31 USB2P5
 K31 USB2N6
 L31 USB2P6
 G29 USB2N7
 H29 USB2P7
 A32 USB2N8
 C32 USB2P8
 A30 USB2N9
 C30 USB2P9
 B29 USB2N10
 D29 USB2P10
 A28 USB2N11
 C28 USB2P11
 G26 USB2N12
 F26 USB2P12
 F24 USB2N13
 G24 USB2P13

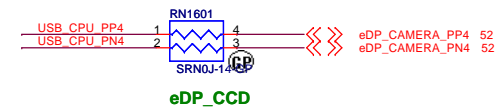
USB port0
 USB port1
 USB port2
 Card Reader
 CCD
 BT

Touch Pad

USB port0
 USB port1

USB 2.0 Table

Pair	Device
0	USB3.0 Port0
1	USB3.0 Port1
2	USB3.0 Port3
3	Card Reader
4	CCD
5	BT
6	
7	
8	
9	
10	Touch Pad
11	
12	
13	

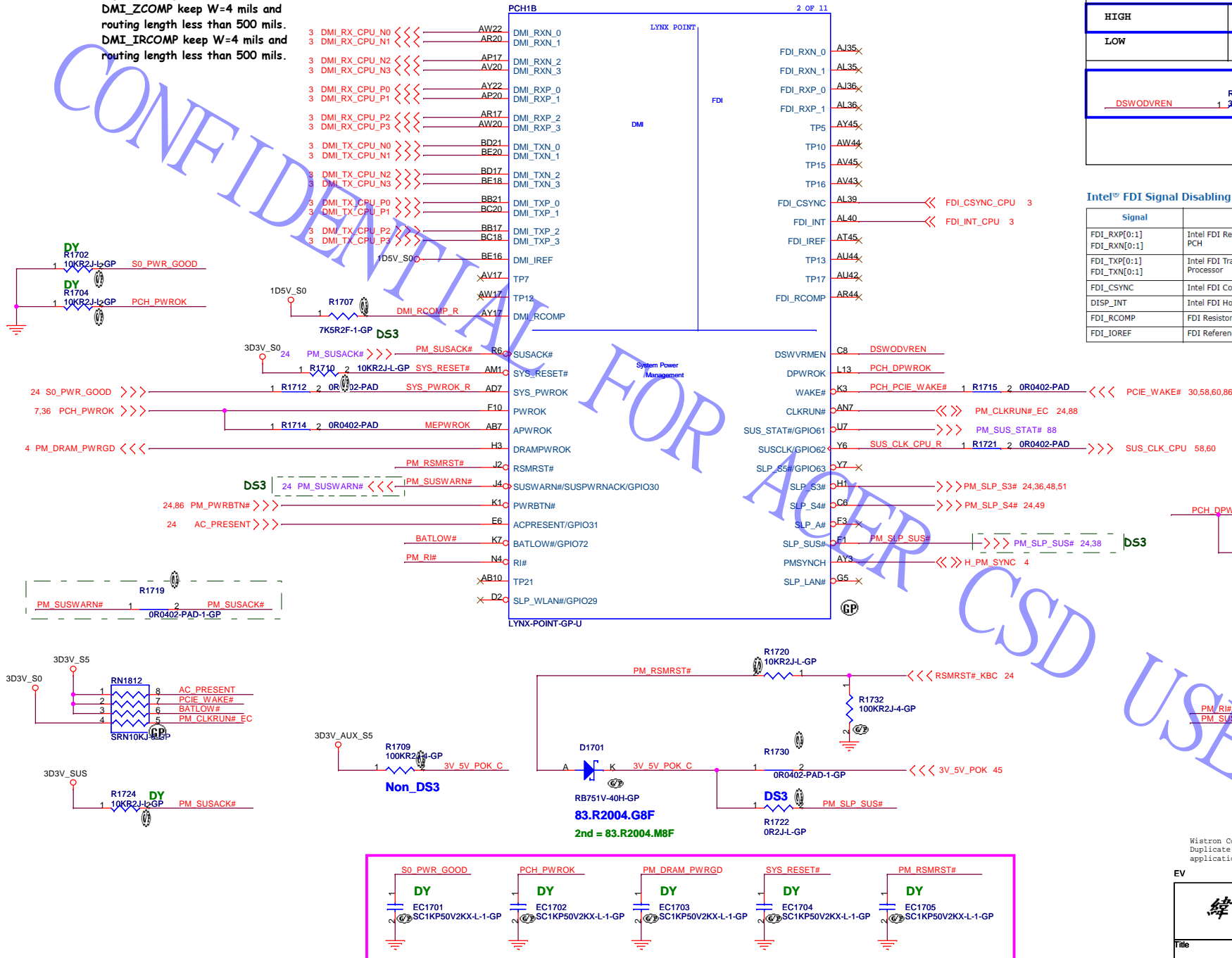


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CPU (PCI/USB)		
Size	Document Number	Rev
Custom	Hades HBS 860M	SB
Date: Friday, May 23, 2014	Sheet 16 of 102	

DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

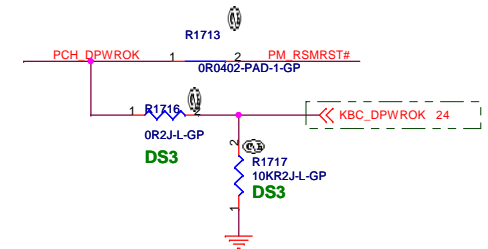
DSWODVREN

R1706
330k

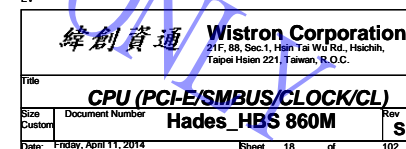
3D3V_RTC_AUX

GP

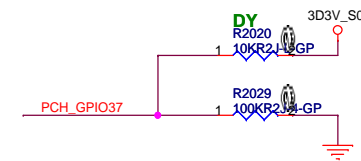
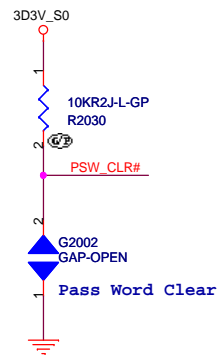
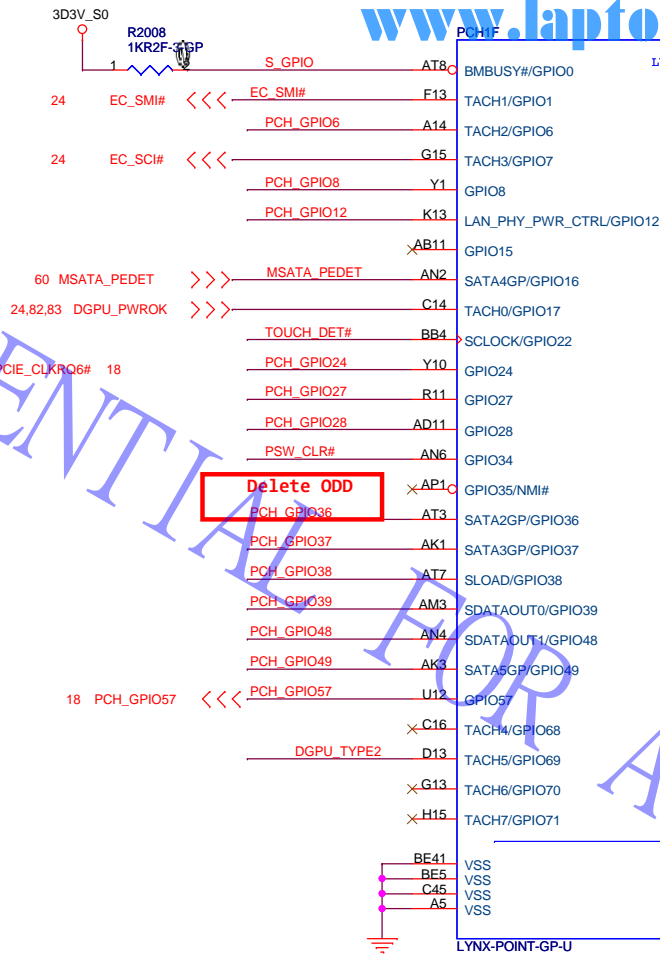
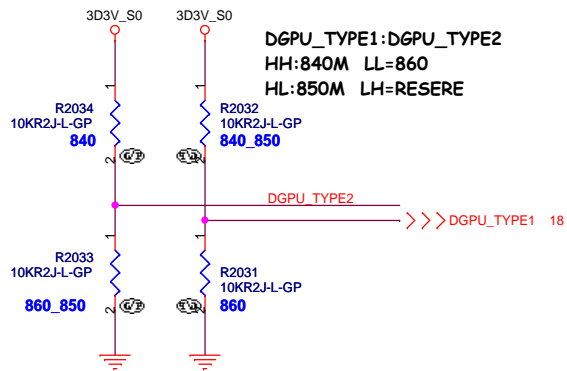
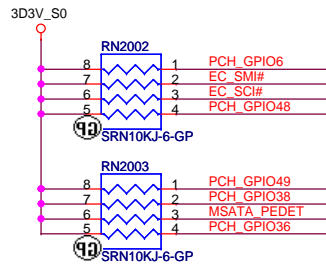
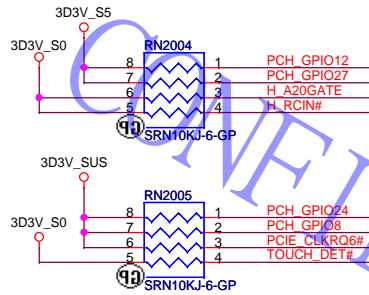
Signal	Description	Disable Guidelines
FDI_RXP[0:1] FDI_RXN[0:1]	Intel FDI Receive Differential Pair on PCH	Float
FDI_TXP[0:1] FDI_TXN[0:1]	Intel FDI Transmit Differential Pair on Processor	Float
FDI_CSNC	Intel FDI Composite Sync	Connect to Processor and PCH
DISP_INT	Intel FDI Hot Plug Interrupt	Connect to Processor and PCH
FDI_RCOMP	FDI Resistor Compensation	Float
FDI_IREF	FDI Reference Voltage	Float



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SSID = PCH



TLS Confidentiality

0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)

1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality)

PLL ON DIE VR ENABLE

ENABLED -- HIGH (R2013 UNSTUFFED) DEFAULT

DISABLED -- LOW (R2013 STUFFED)

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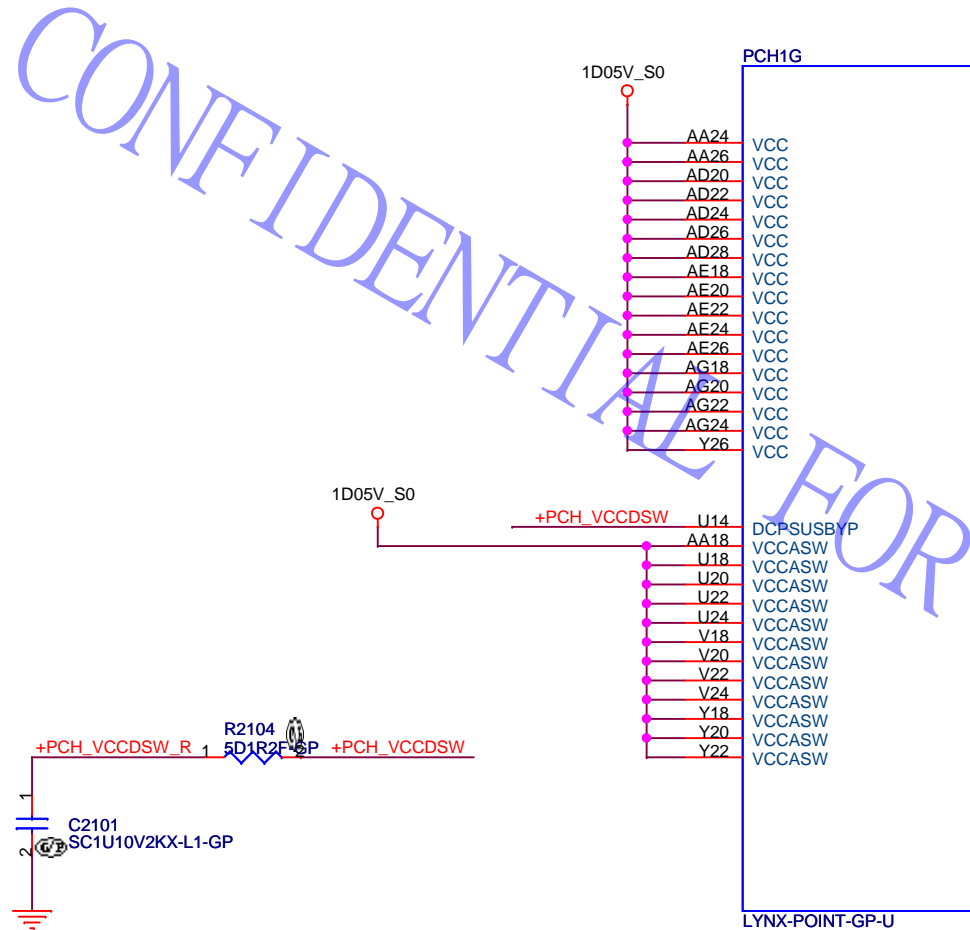
緯創資通 Wistron Corporation
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Title: **CPU (GPIO/MISC)**

Size: Custom Document Number: **Hades_HBS 860M** Rev: **SB**

Date: Thursday, May 29, 2014 Sheet: 20 of 102

SSID = PCH



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EV

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Title

CPU (POWER1)

Size
A4

Document Number

Hades_HBS 860M

Rev
SB

Date: Friday, April 11, 2014

Sheet 21 of 102



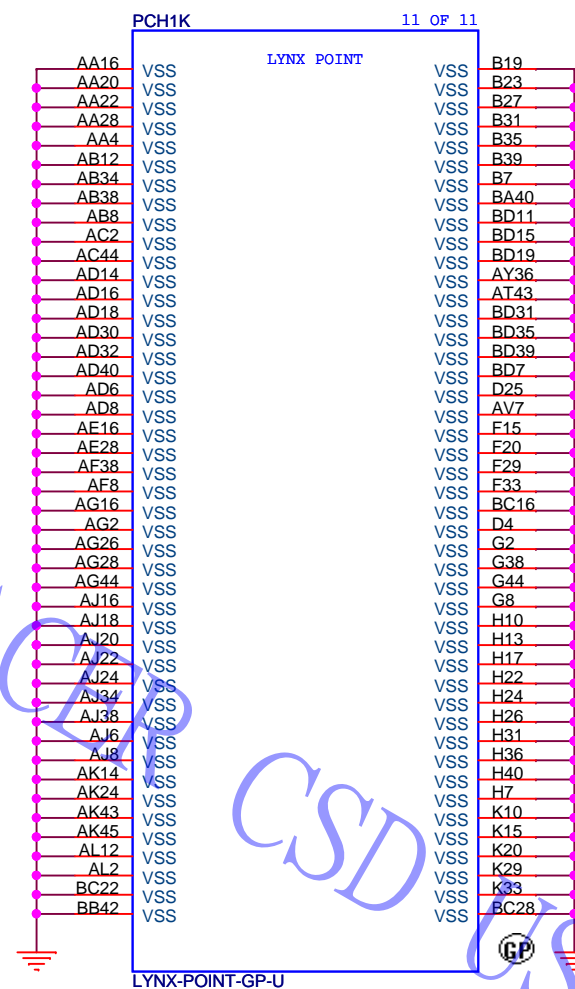
緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

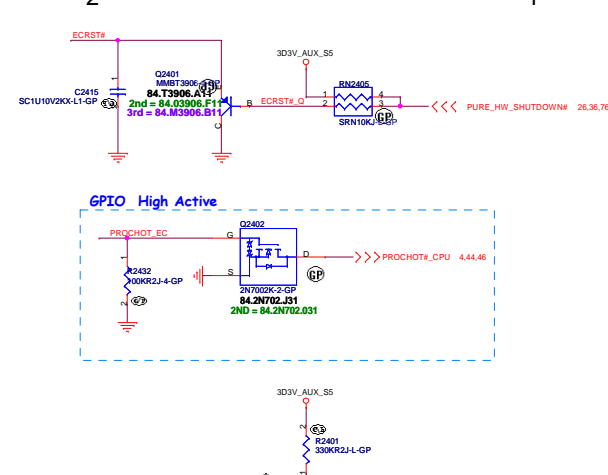
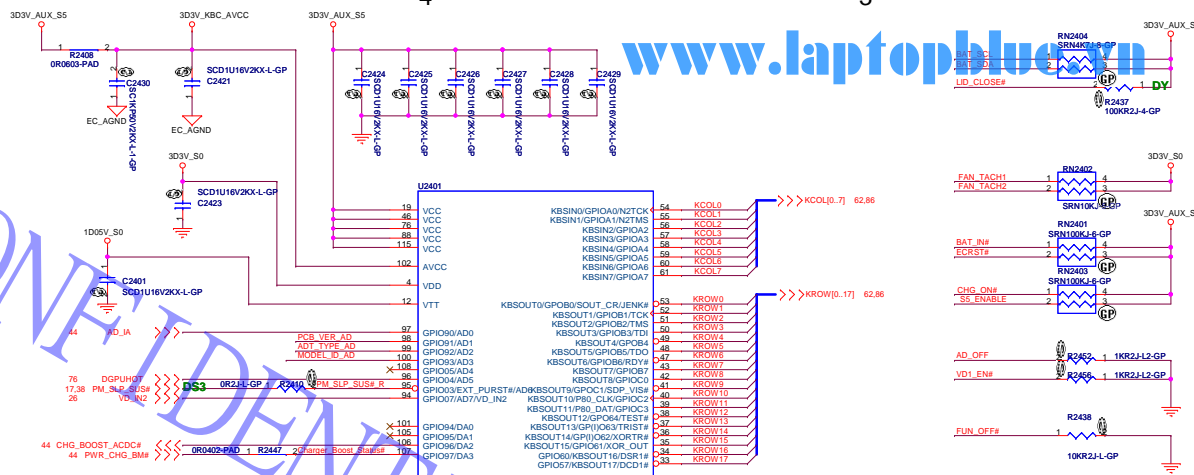
Title	CPU (RSVD)
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Size Custom	Document Number Hades_HBS 860M	Rev SB
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Date: Wednesday, May 28, 2014 Sheet 22 of 102

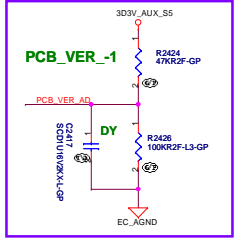
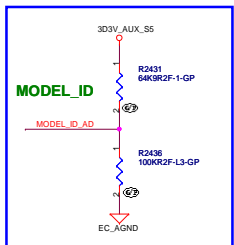
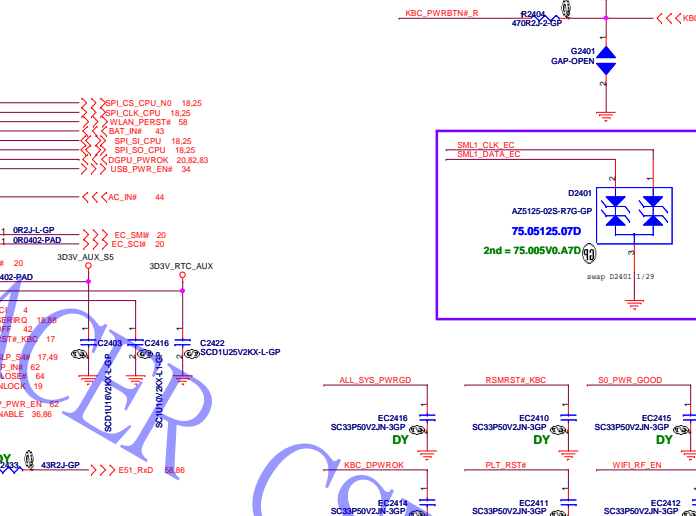
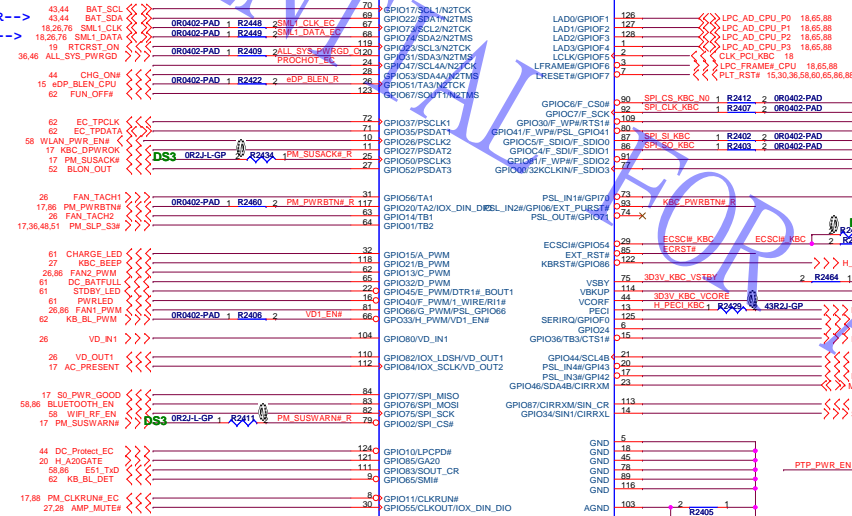


Sheet 23 of 102



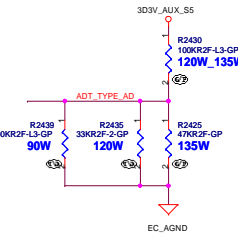
BATTERY / CHAR
Thermal/eDP/GP

Touch Pad--->



Model #)	Full-Low Register	Full-High Register	Typical Voltage	Max Voltage	XBC Firmware Setting
VA30	100 0 K	3 000 K	3 005 V	≈ 2 875 V	
Hades UMA	100 0 K	20 0 K	2 750 V	2 750 V	< 2 875 V
Hades DIS 840	100 0 K	33 0 K	2 481 V	2 4935	< 2 610 V
Hades DIS 850	100 0 K	47 0 K	2 245 V	2 259	≈ 1 123 V
Hades DIS 850	100 0 K	54 9 K	2 001 V	2 0166	≈ 1 934 V
Poseidon DIS 840	100 0 K	76 8 K	1 947 V	1 9527	≈ 1 934 V
Poseidon DIS 850	100 0 K	120 0 K	1 650 V	1 6655	≈ 1 594 V
Poseidon DIS 850	100 0 K	143 0 K	1 355 V	1 3740	≈ 1 281 V
Reserved for project use	100 0 K	174 0 K	1 204 V	1 2197	≈ 1 126 V
Reserved for project use	100 0 K	215 0 K	1 048 V	1 0620	≈ 0 524 V

PCN, VER, AU	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.0054	≥ 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.7591	≥ 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4895	≥ 2.363 V	< 2.616 V
-I	100.0 K	47.0 K	2.245 V	2.2592	≥ 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	≥ 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	≥ 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	≥ 1.594 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	≥ 1.281 V	< 1.594 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	≥ 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	≥ 0.924 V	< 1.126 V



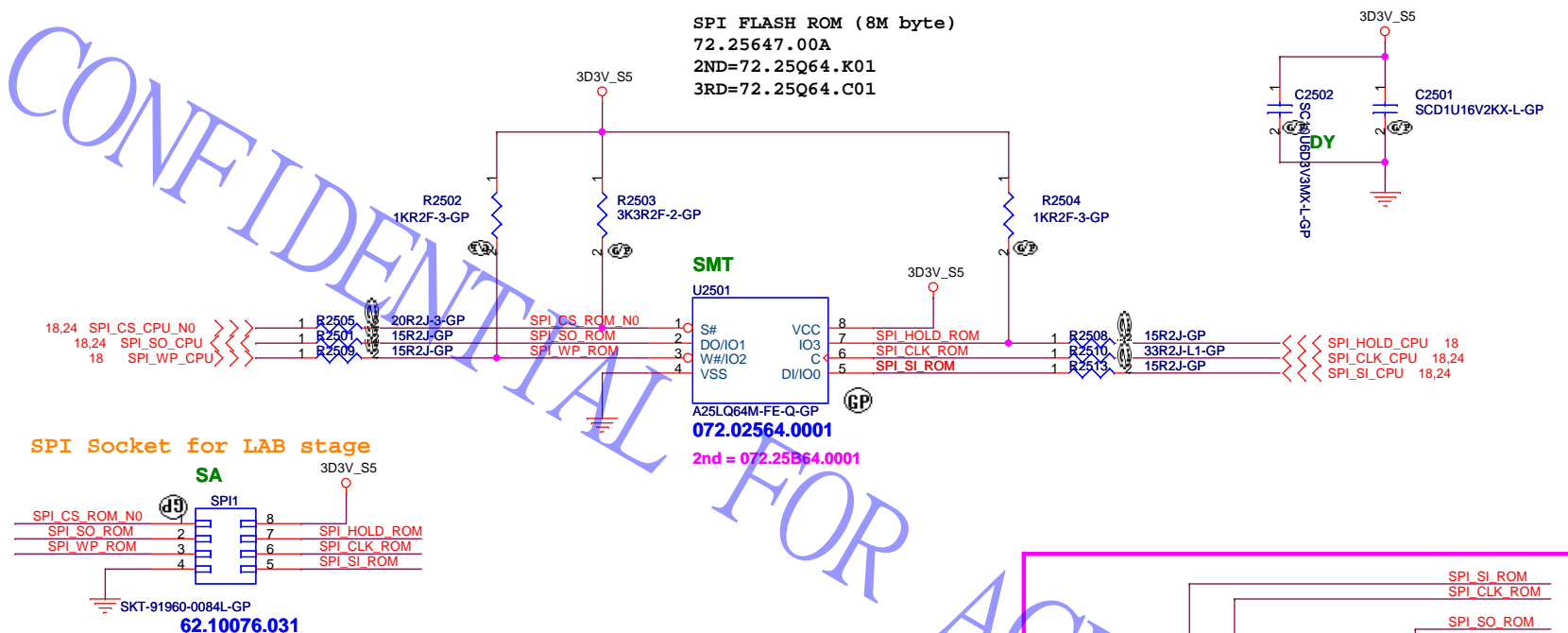
ANAL. TYPE	Pull-Load Regulator	Pull-High Regulator	Typical Voltage	Max Voltage	ASIC Firmware Setting
65W	N/A	100.0 K	3.300 V		≥ 3.000 V
90W	100.0 K	N/A	0.000 V		
30W	10.0 K	100.0 K	0.300 V	0.3055	> 0.150 V
45W	20.0 K	100.0 K	0.550 V	0.5592	> 0.425 V
120W	33.0 K	100.0 K	0.819 V	0.8312	> 0.684 V
135W	47.0 K	100.0 K	1.055 V	1.0685	> 0.937 V
150W	64.9 K	100.0 K	1.299 V	1.3140	> 1.177 V
Reserved	76.8 K	100.0 K	1.433 V	1.4497	> 1.366 V
Reserved	100.0 K	100.0 K	1.660 V	1.6855	> 1.542 V

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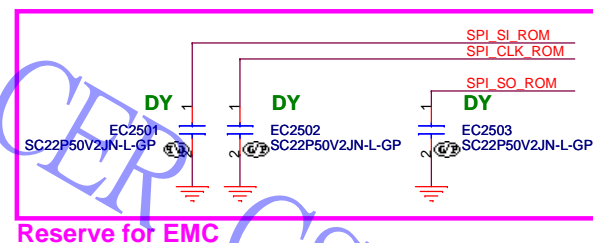
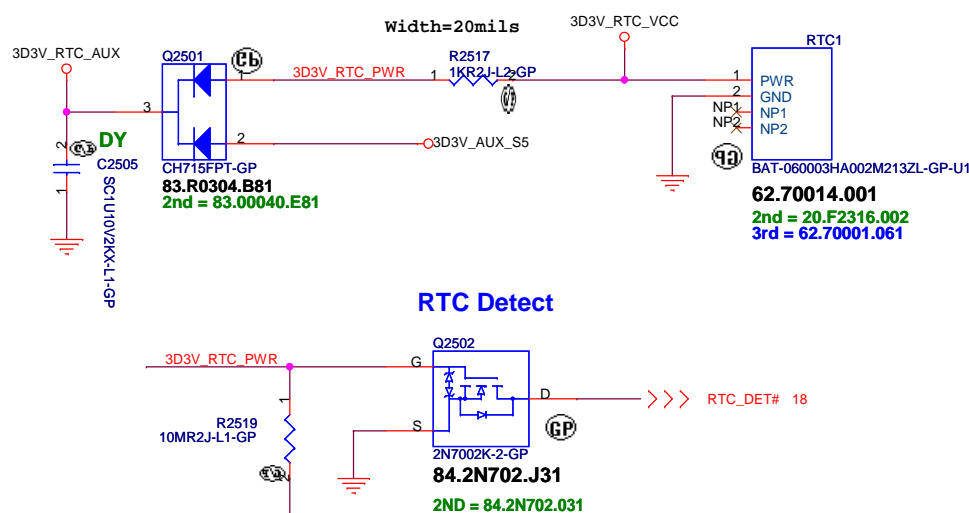
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil



SSID = RBAT



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Flash(KBC+PCH)/RTC

Size	Custom
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Document Number

Hades_HBS 860M

Re

SB

Date: Friday, April 11, 2014

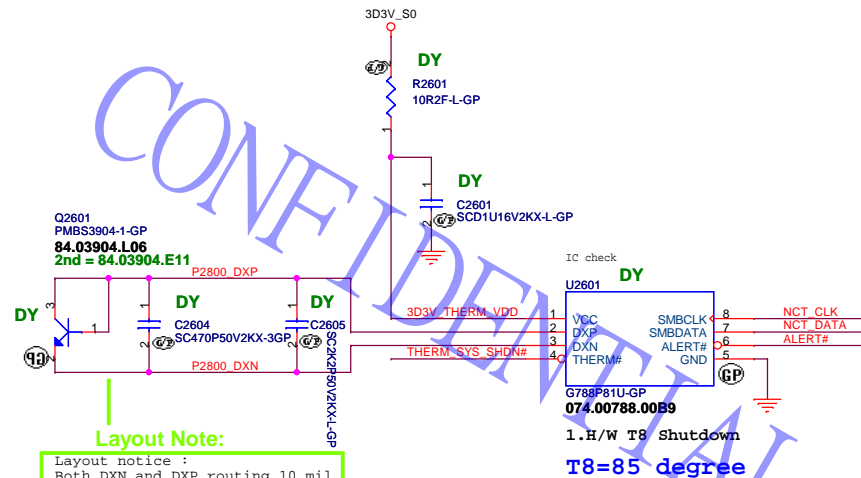
Sheet 25 of

102

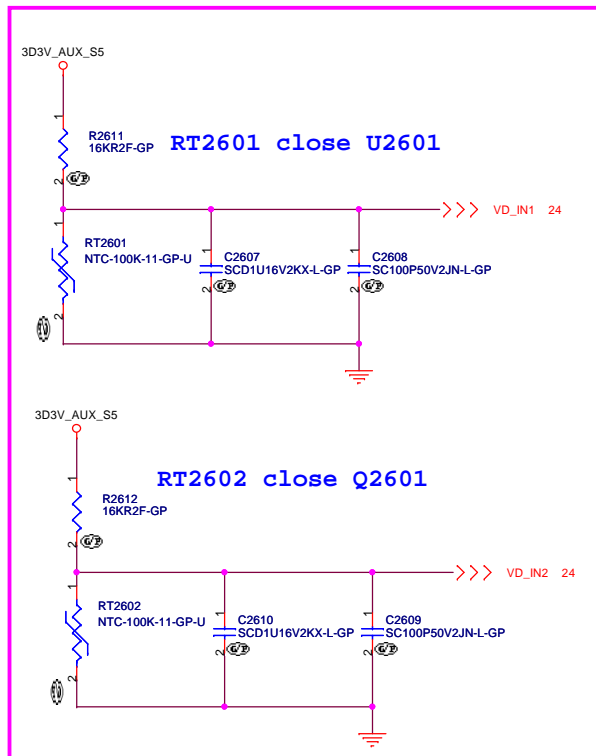
102

SSID = Thermal

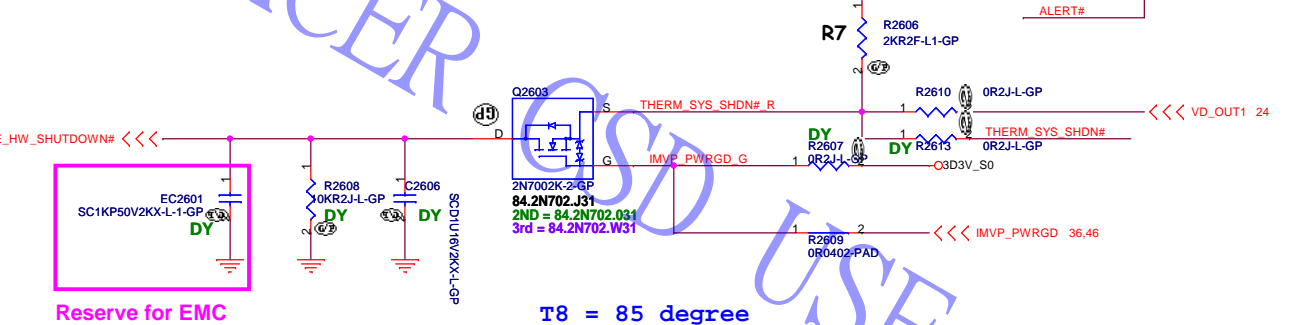
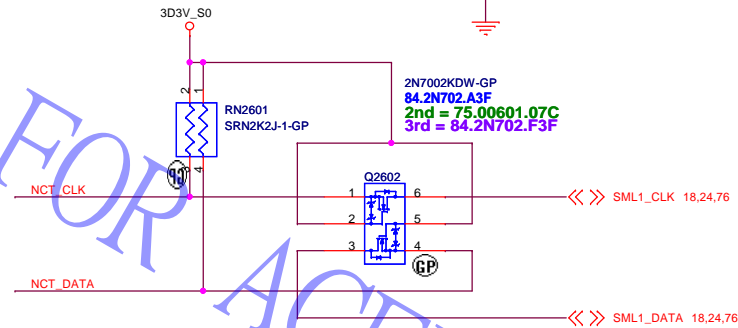
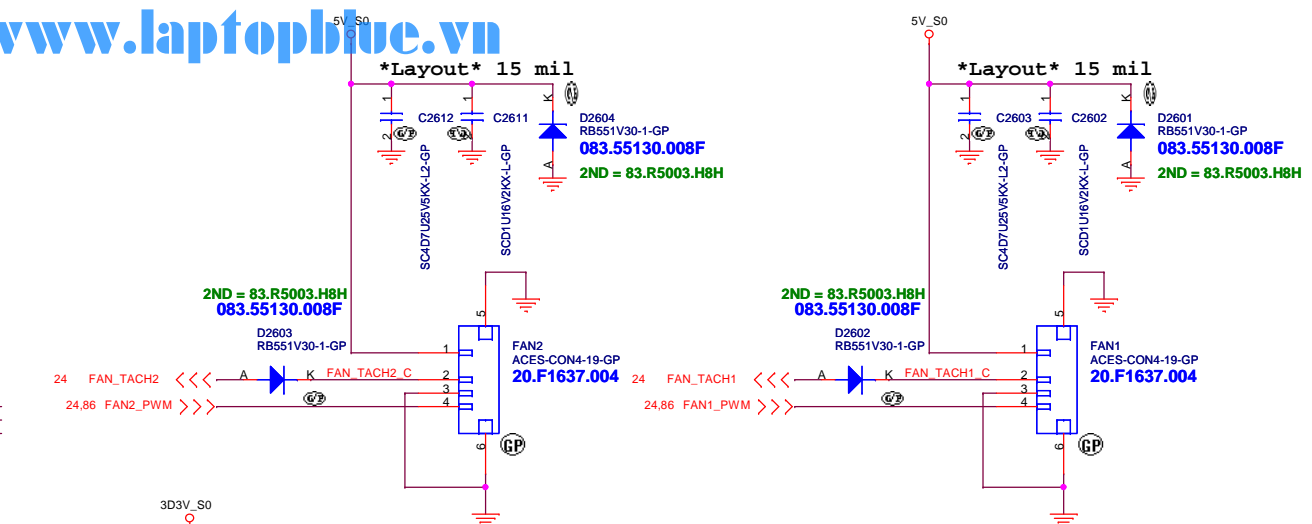
Thermal sensor GMT G788



2.System Sensor, Put on palm rest



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Reserve for EMC

ALERT# /T CRIT#
Pull-up Resistor

R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
77°C	77°C	77°C	77°C	77°C	77°C
79°C	79°C	79°C	79°C	79°C	79°C
81°C	81°C	81°C	81°C	81°C	81°C
83°C	83°C	83°C	83°C	83°C	83°C
85°C	85°C	85°C	85°C	85°C	85°C

T_CRIT temperature strapping point

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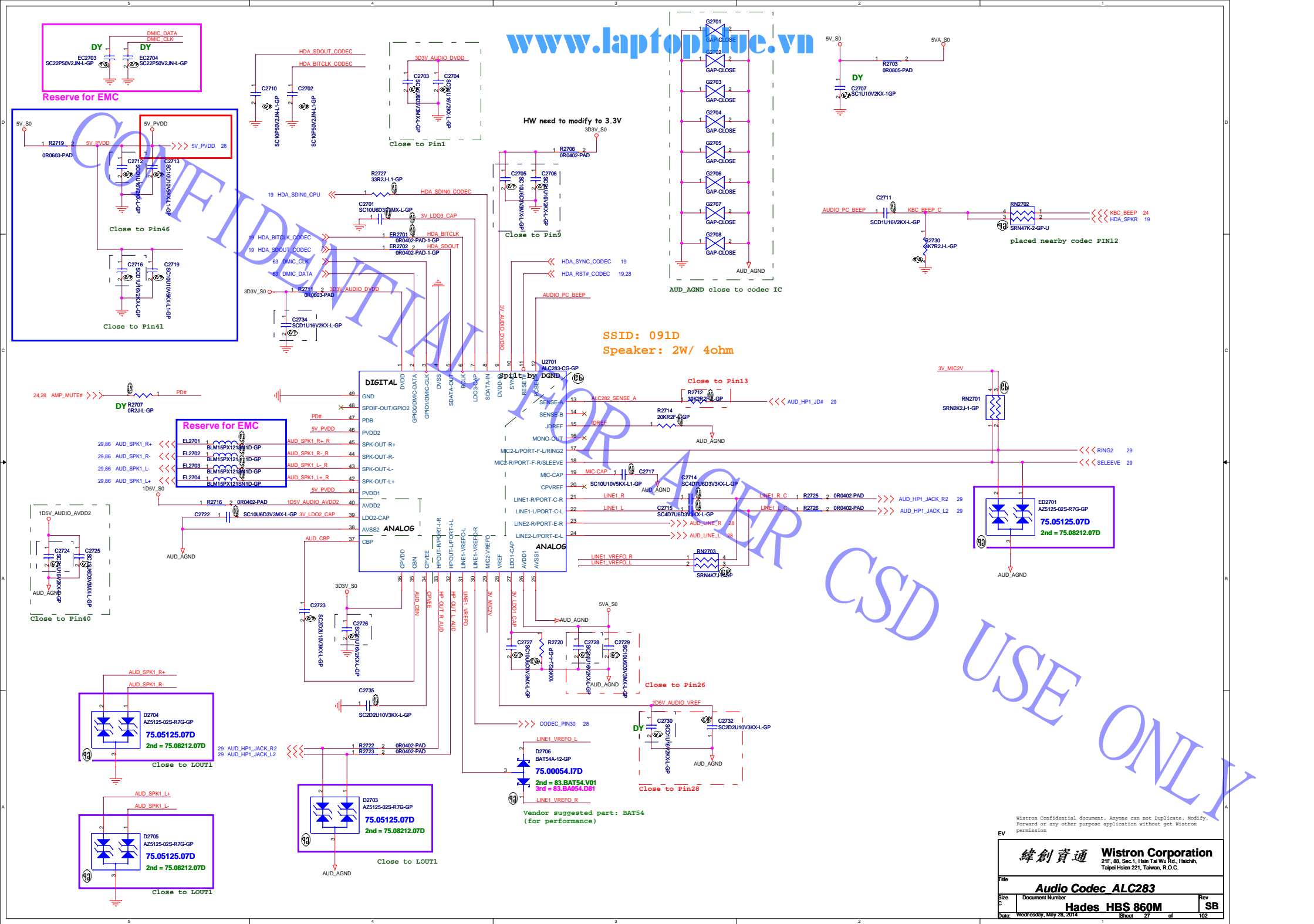
EV

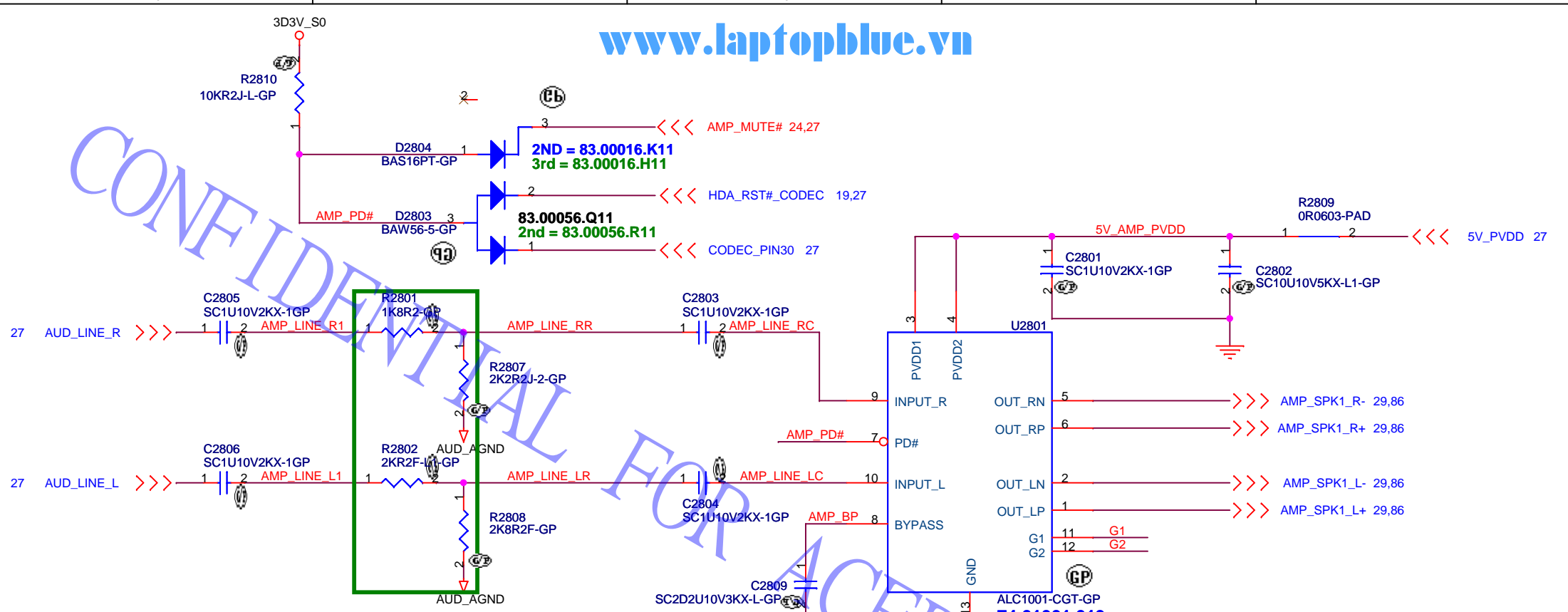
7718/Fan Controller P2793

Hades HBS 860M

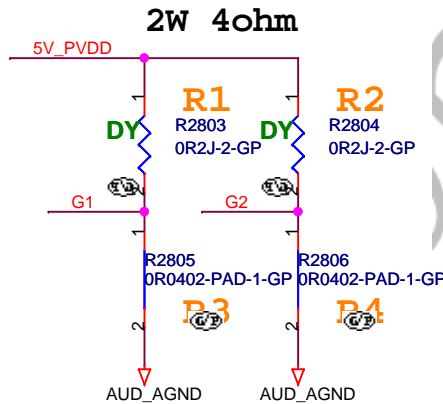
Date: Wednesday, May 28, 2014

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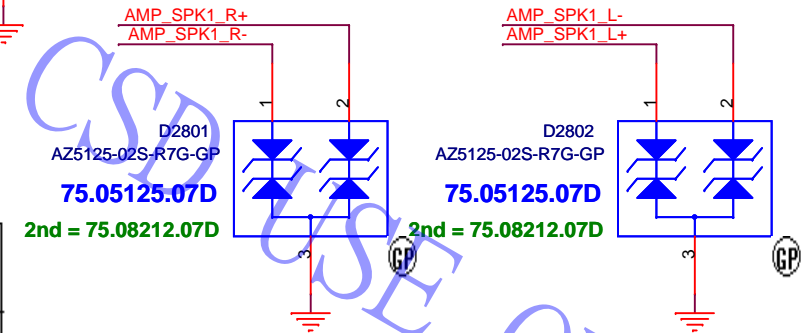


Reserve for input attenuation
to have optimized output power
2Watt



Output Gain Table

R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB



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<p>Title</p> <p>Audio AMP ALC1001</p>	
<p>Size</p> <p>A4</p>	<p>Document Number</p> <p>Hades HBS 860M</p>
<p>Date:</p> <p>Wednesday, May 28, 2014</p>	<p>Rev</p> <p>SB</p>
<p>Sheet 28 of 102</p>	

SSID = AUDIO

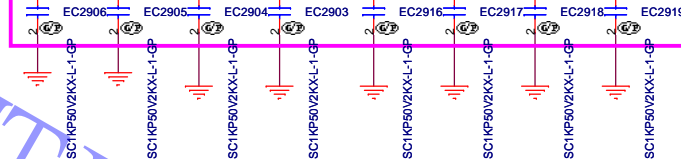
www.laptopblue.vn

28,86 AMP_SPK1_L-
28,86 AMP_SPK1_L+
27,86 AUD_SPK1_L-
27,86 AUD_SPK1_L+
28,86 AMP_SPK1_R-
28,86 AMP_SPK1_R+
27,86 AUD_SPK1_R-
27,86 AUD_SPK1_R+ >>>

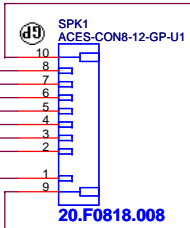
Speaker

Layout Note:
Trace width=40mil

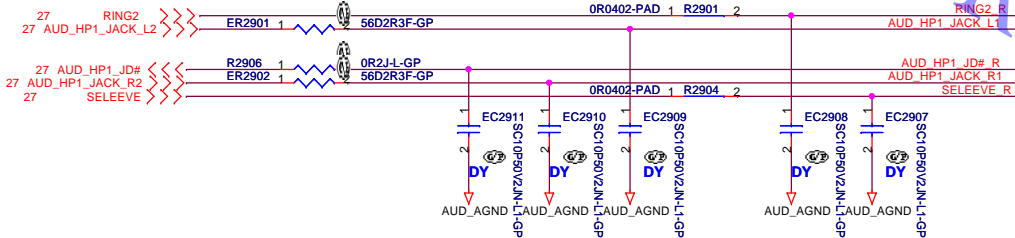
12/17



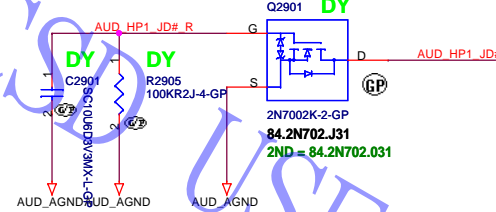
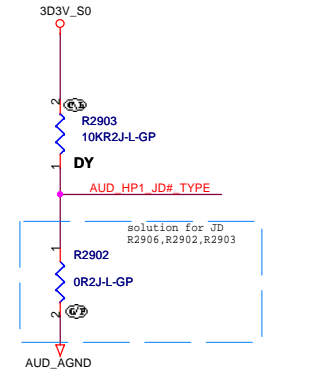
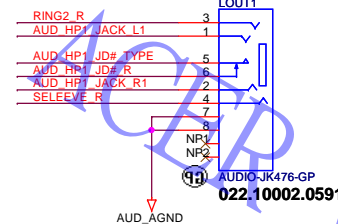
1nd = 20.F0818.008
2nd = 20.F2348.008



Combo Jack



86 SELEEVE_R <<< SELEEVE_R
86 AUD_HP1_JACK_L1 <<< AUD_HP1_JACK_L1
86 AUD_HP1_JD#_TYPE <<< AUD_HP1_JD#_TYPE
86 AUD_HP1_JD#_R <<< AUD_HP1_JD#_R
86 AUD_HP1_JACK_R1 <<< AUD_HP1_JACK_R1
86 RING2_R <<< RING2_R



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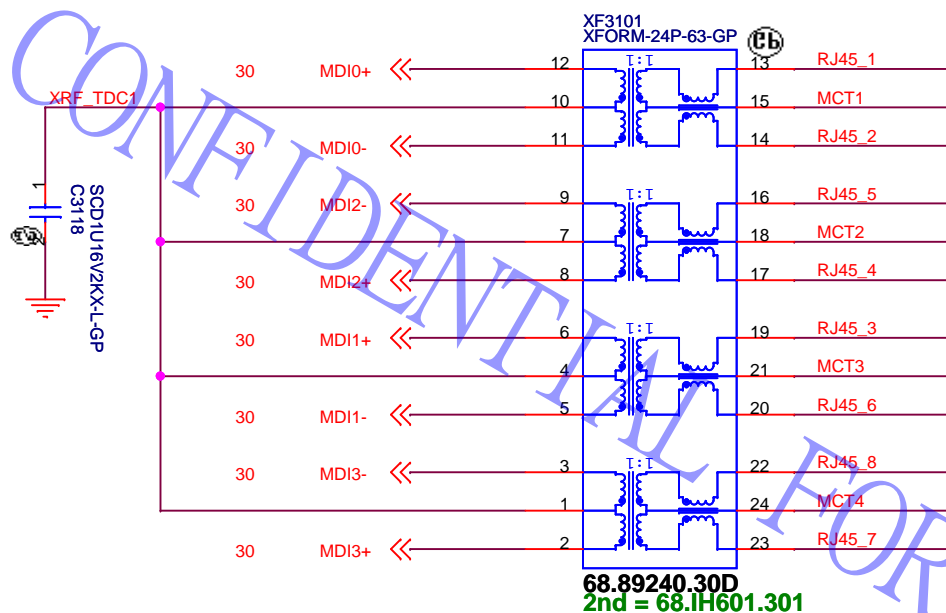
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Title			Audio Jack
Size	Document Number	Rev	SB
Custom	Hades HBS 860M		
Date: Wednesday, May 28, 2014	Sheet 29	of 102	

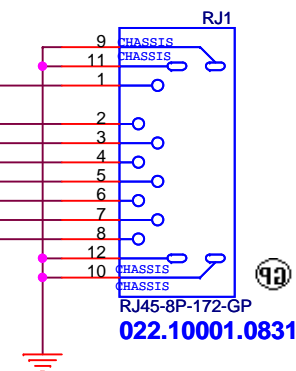
W	Wistron Confidential document. Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission.	E	
V			

SSID = LAN

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86 RJ45_1 << RJ45_1
86 RJ45_2 << RJ45_2
86 RJ45_3 << RJ45_3
86 RJ45_4 << RJ45_4
86 RJ45_5 << RJ45_5
86 RJ45_6 << RJ45_6
86 RJ45_7 << RJ45_7
86 RJ45_8 << RJ45_8

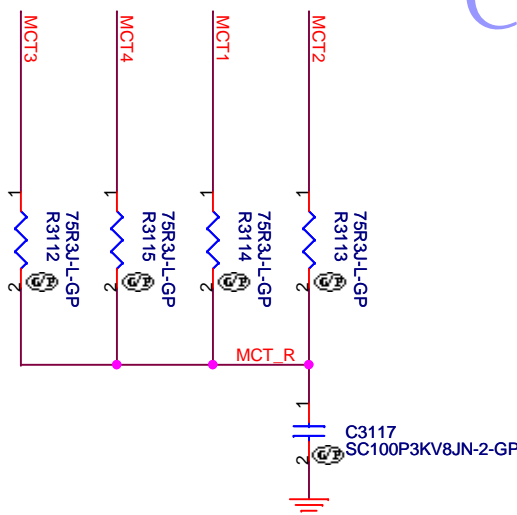
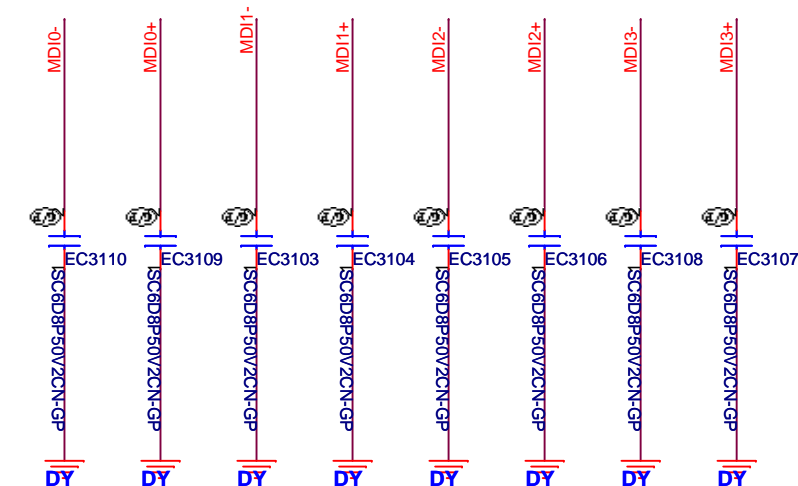


U3101
TVLST2304BD0-GP
075.02304.007C
2nd = 75.04223.07C
3rd = 75.09904.07C

MDI1+ << 30
MDI1- << 30
MDI3+ << 30
MDI3- << 30

U3102
TVLST2304BD0-GP
075.02304.007C
2nd = 75.04223.07C
3rd = 75.09904.07C

MDI0+ << 30
MDI0- << 30
MDI2+ << 30
MDI2- << 30



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Title (LAN+VGA) CONNECTOR		
Size A4	Document Number Hades HBS 860M	Rev SB
Date Wednesday, May 28, 2014	Sheet 31	of 102

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Title			
RTS5170(CARD READER)			
Size A4	Document Number		Rev
	Hades HBS 860M		SB
Date:	Friday, April 11, 2014		Sheet 32 of 102

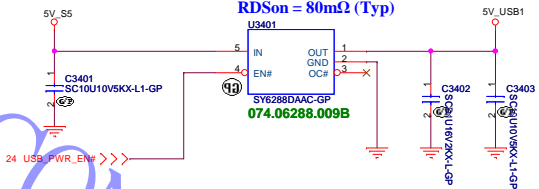
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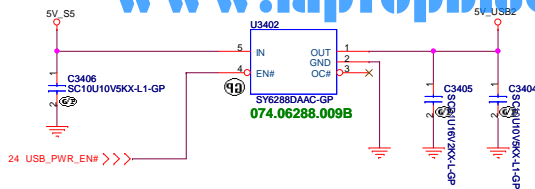
EV

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Card Reader CONN (Reserved)			
Size	Document Number		Rev
Custom	Hades HBS 860M		SB
Date:	Friday, April 11, 2014		Sheet 33 of 102

Low Active 2A
RDSON = 80mΩ (Typ)



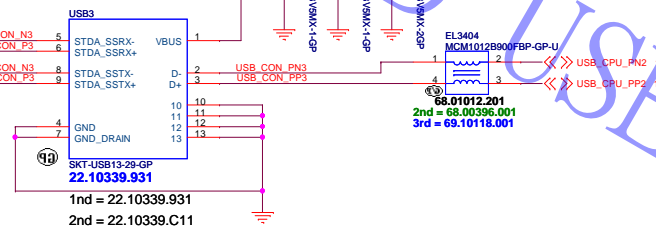
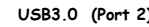
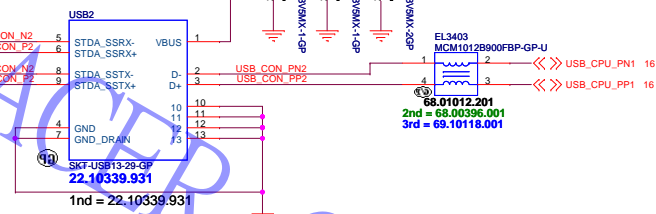
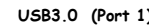
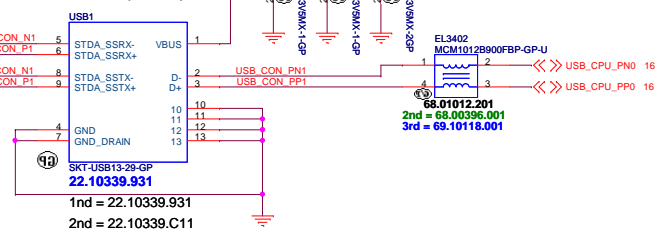
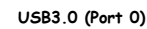
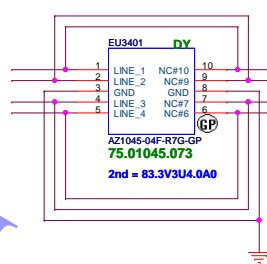
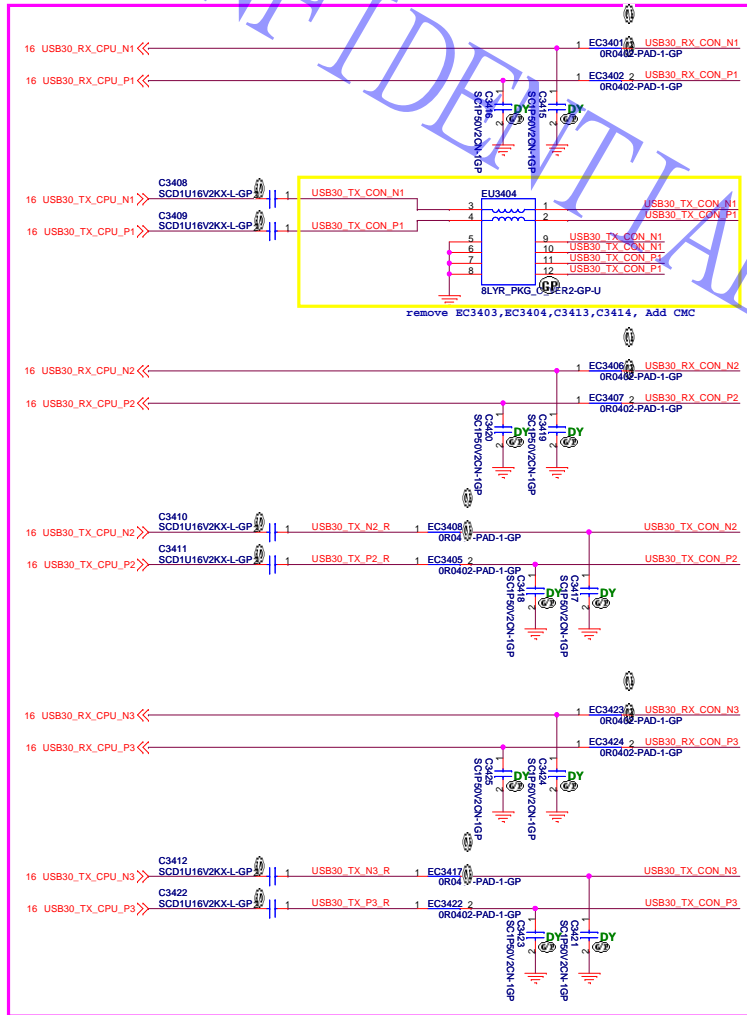
Low Active 2A
RDSon = 80mΩ (Typ)



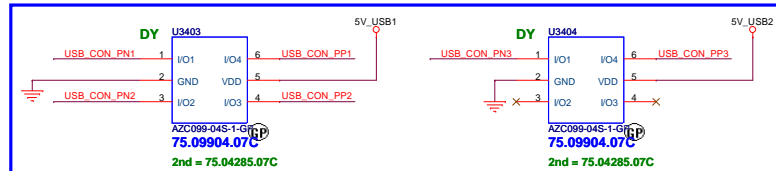
USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

Reserve for RF



ESD for USB



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Title				USB 3.0 Port			
Size	Document Number						Rev
Custom	Hades_HBS 860M						SI
Date:	Tuesday, May 27, 2014			Sheet	34	of	102

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Title

USB CHARGER

Size

A4

Document Number

Hades HBS 860M

Rev

SB

Date:

Friday, April 11, 2014

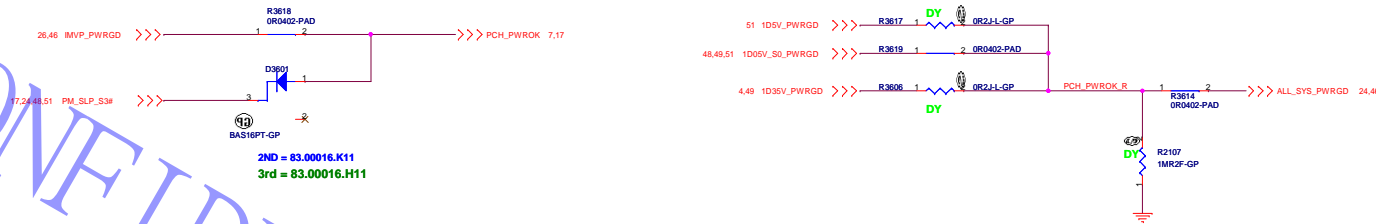
Sheet

35

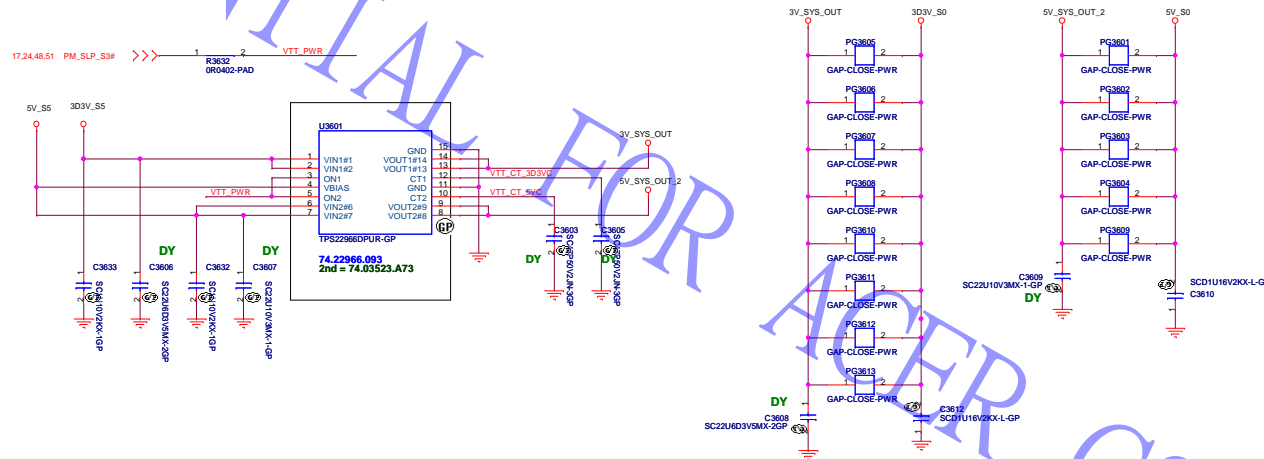
of

102

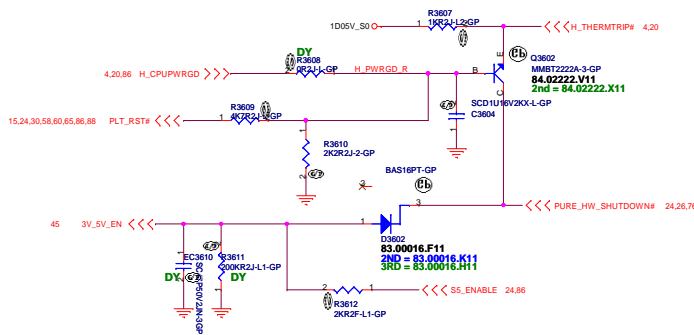
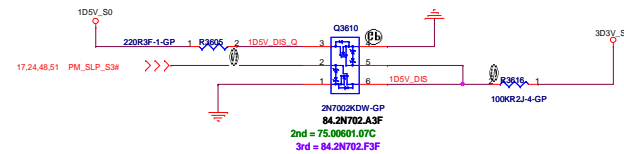
Power Sequence



ANNIE Run Power



Discharge Circuit

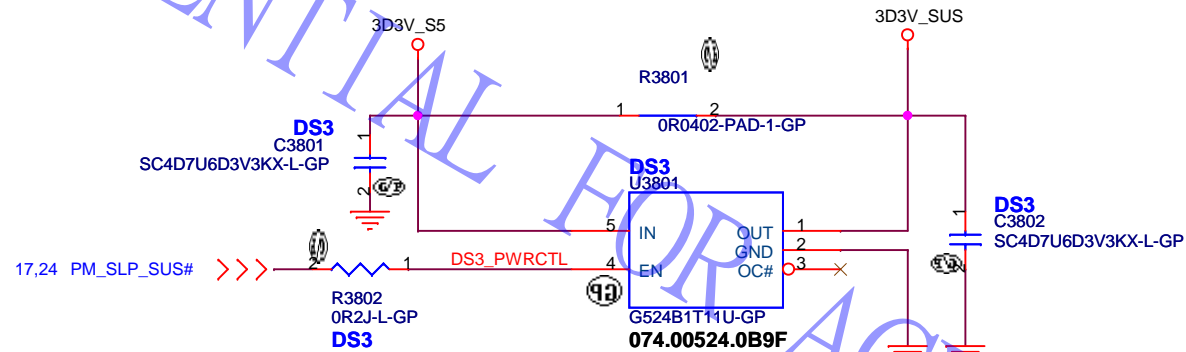


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Title		
ADAPTER OCP / S3 reduction		
Size	Document Number	Rev
Custom	Hades HBS 860M	SB
Date:	Friday, April 11, 2014	Sheet 37 of 102



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Title

DS3

Size
A4

Document Number

Hades HBS 860M

Rev
SB

Date: Thursday, May 22, 2014

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Power Sequence

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Title			
1D05 M			
Size	Document Number	Rev	
Custom	Hades HBS 860M	SB	
Date: Friday, April 11, 2014	Sheet 39	of	102

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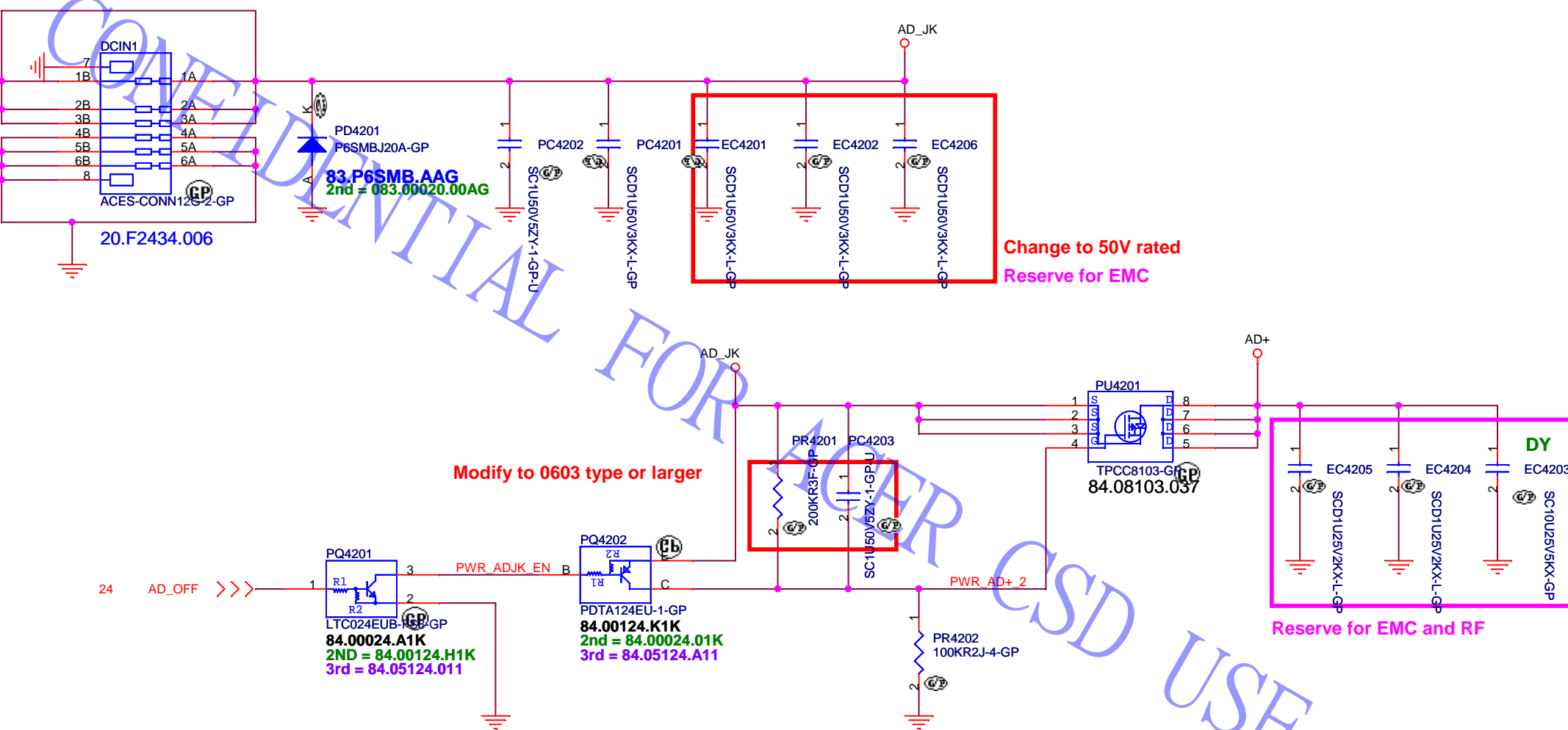
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Connected Standby1			
Size	Document Number		Rev
A	Hades HBS 860M		SB
Date:	Friday, April 11, 2014		Sheet 40 of 102

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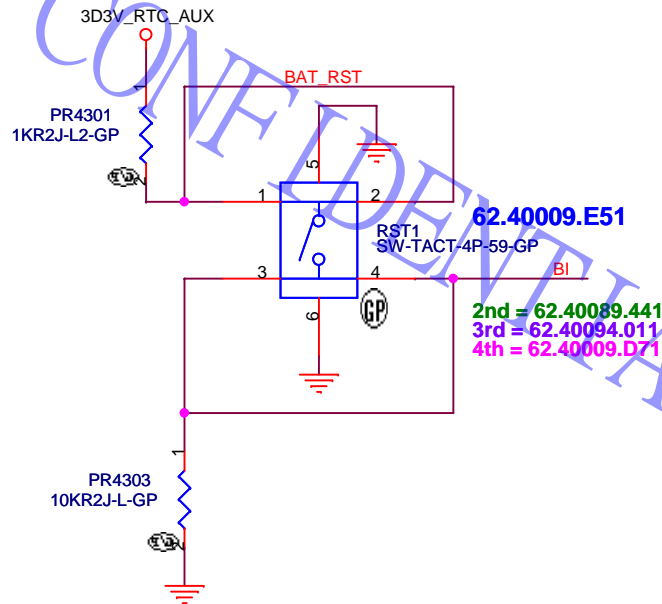
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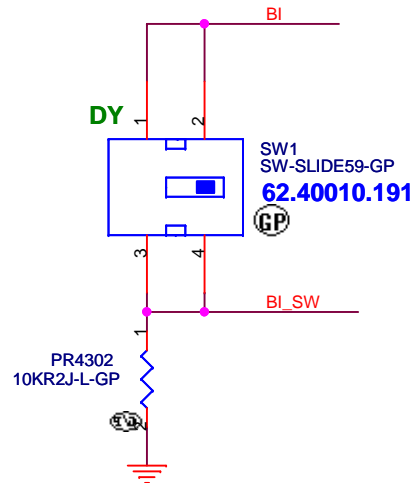
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Connected Standby2			
Size	Document Number		Rev
A	Hades HBS 860M		SB
Date:	Friday, April 11, 2014		Sheet 41 of 102



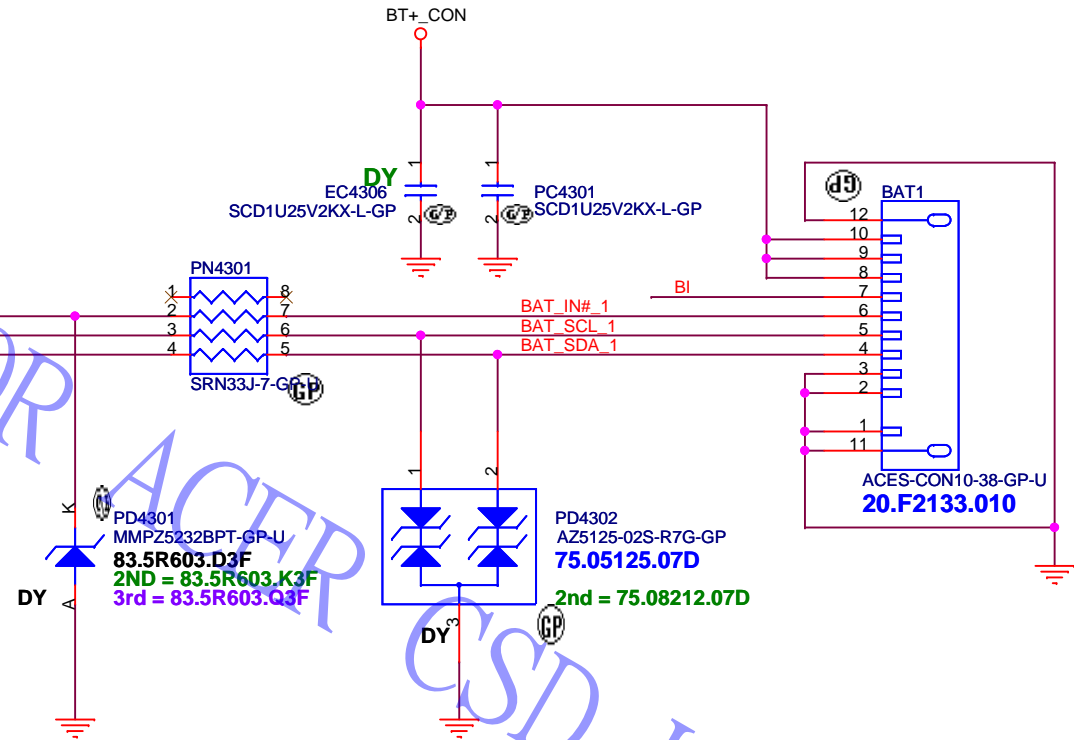
Battery Reset



Battery Insert



Battery Connector



86 BI

86 BAT_IN#_1

86 BAT_SCL_1

86 BAT_SDA_1

BI

BAT_IN#_1

BAT_SCL_1

BAT_SDA_1

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Title

BATT CONN

Size

Document Number

Rev

Hades HBS 860M

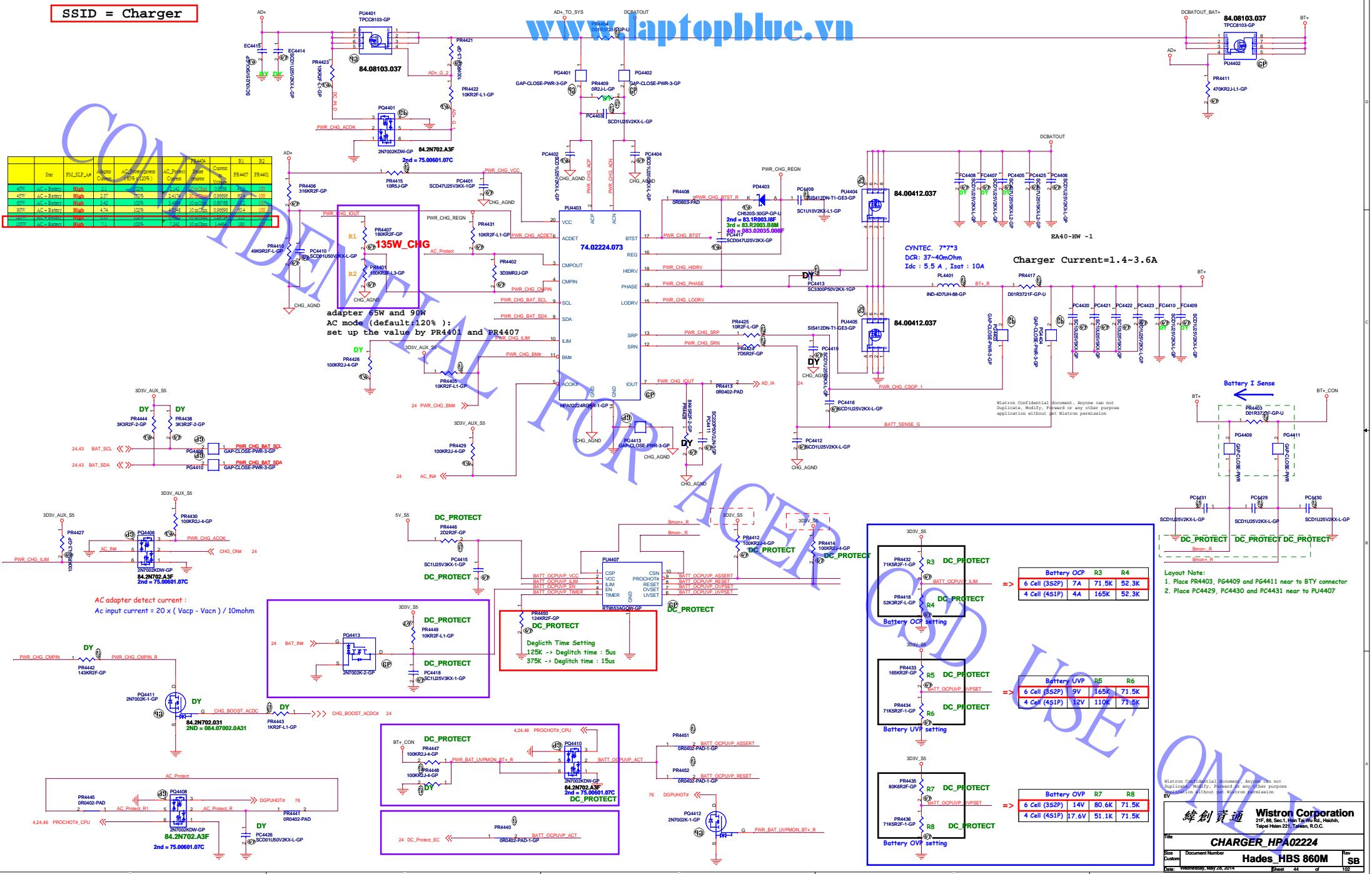
SB


Date: Friday, April 11, 2014

Sheet 43 of 102

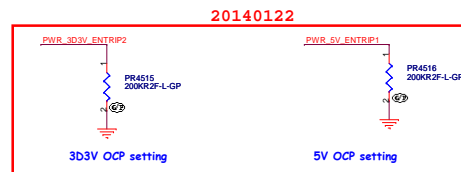
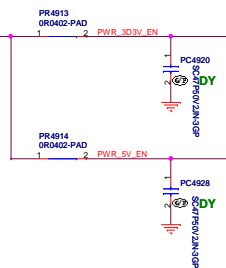
www.laptopblue.vn

	Stat	SLP_SLP_Air	Current Current	AC_Power Current (100% = 200%)	AC_Power Current	Power Power	Current Current	R1	R2
							Power407	Power407	Power407
407	AC = Battery	High	2.1	100%	2.142	200%	0.8659	73%	100%
407	AC = Battery	High	2.37	100%	2.4176	200%	0.86594	63%	100%
407	AC = Battery	High	4.0	100%	4.0892	200%	0.86586	67%	100%
407	AC = Battery	High	4.4	100%	4.4854	100%	0.86605	55.4%	100%
407	AC = Battery	High	5.1	100%	5.241	100%	0.8661	50%	100%

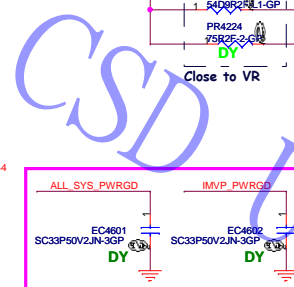


 緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei HSPA 221, Taiwan, R.O.C.	
Title			
CHARGER_HPA02224			
Size	Document Number	Hades_HBS 860M	
Custom			Rev SB
Date: wctw020501, May 28, 2014		Sheet 44 of	102

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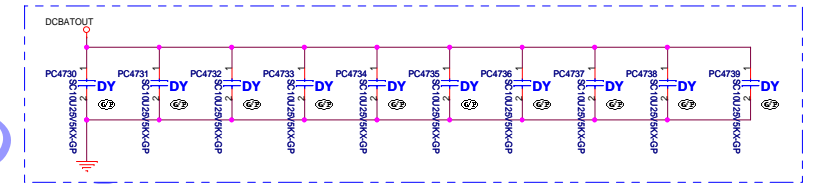
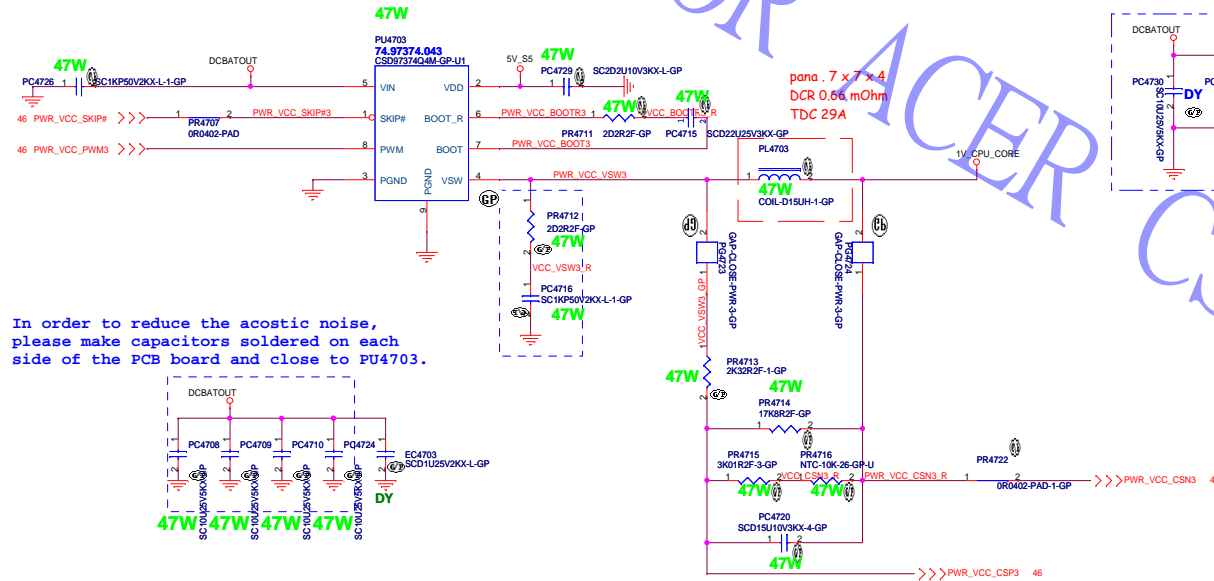
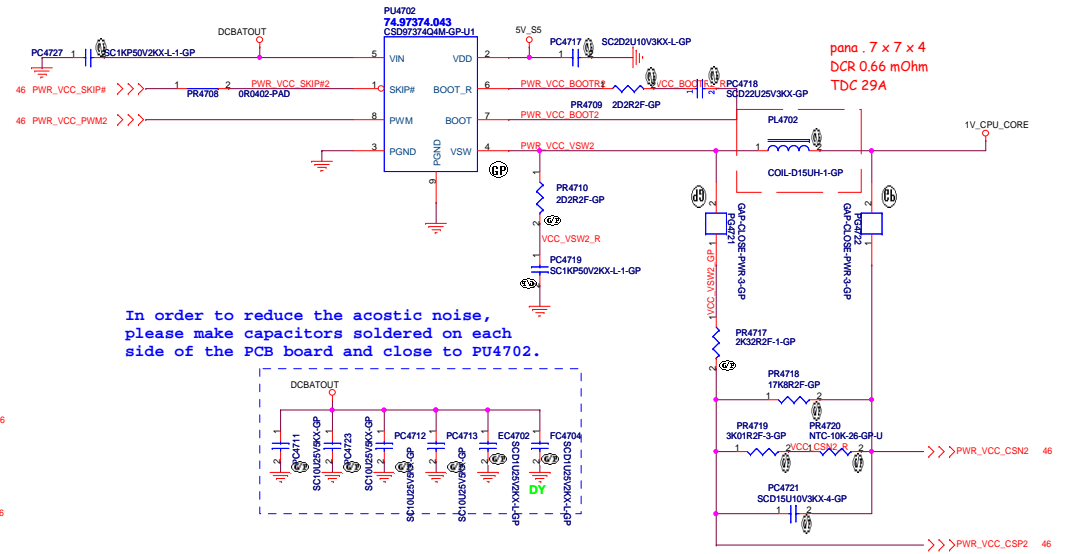
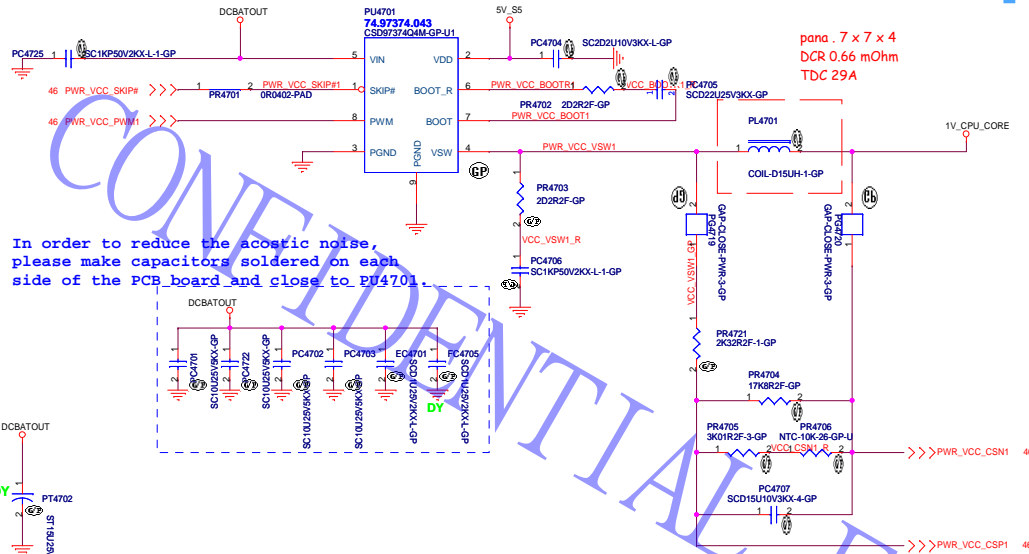


EV	<p>Wistron Confidential document. Anyone can buy, Duplicate, Modify, Forward or any other purpose application without get Wistron permission</p>
	<div style="display: flex; justify-content: space-between;"> <div style="width: 40%;"> <p>緯創資通</p> </div> <div style="width: 60%;"> <p>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichah, Taipei Hsien 221, Taiwan, R.O.C.</p> </div> </div>
Title	
Size	<p style="text-align: center;">TPPS1225 5V3D3V</p>
Document Number	<p style="text-align: center;">Hades_HBS 860M</p>
Date	<p>Wednesday, May 28, 2014</p>
Sheet	<p>1 of 102</p>
Rev	<p style="text-align: right;">SB</p>

[illegible]

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Title			
TPSS51624 CPUCORE(1/2)			
Size Custom	Document Number	Hades HBS 860M	Rev SB
Date: Thursday, May 25, 2014	Sheet 46	of	102

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TPS51716 for 1D05V

High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

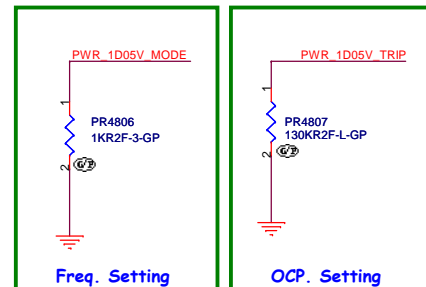
Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

EN. Setting

Vout. Setting

MODE		
PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



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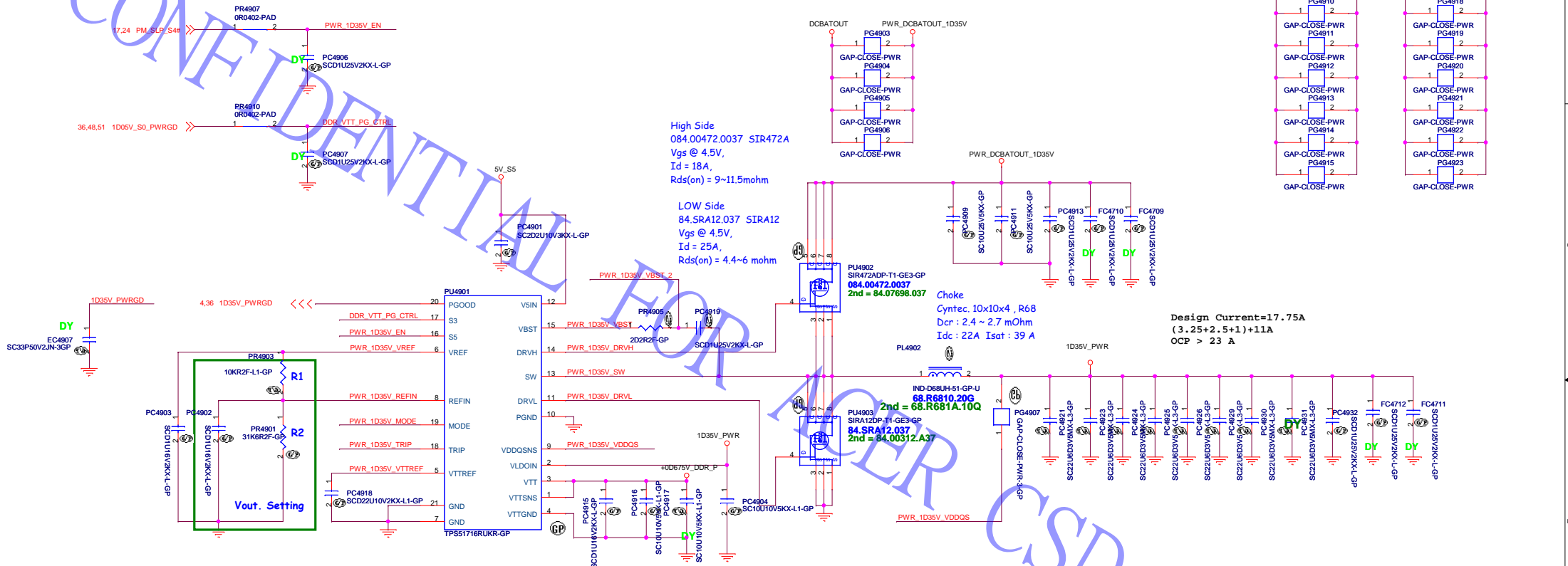
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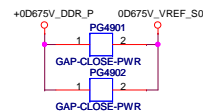
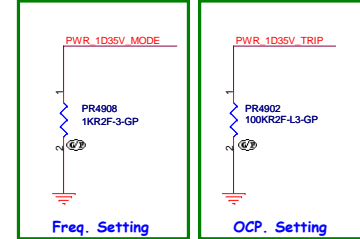
Title		
DC to DC 1D05V (TPS51716)		
Size	Document Number	Rev
A3	Hades HBS 860M	SB
Date: Wednesday, May 28, 2014		Sheet 48 of 102

SSID = PWR.Plane.Regulator_1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	PR4908	Frequency	Discharge Mode
	33k ohm	500kHz	Non-tracking Discharge
	22k ohm	670kHz	
	12k ohm	670kHz	Tracking Discharge
	1k ohm	500kHz	



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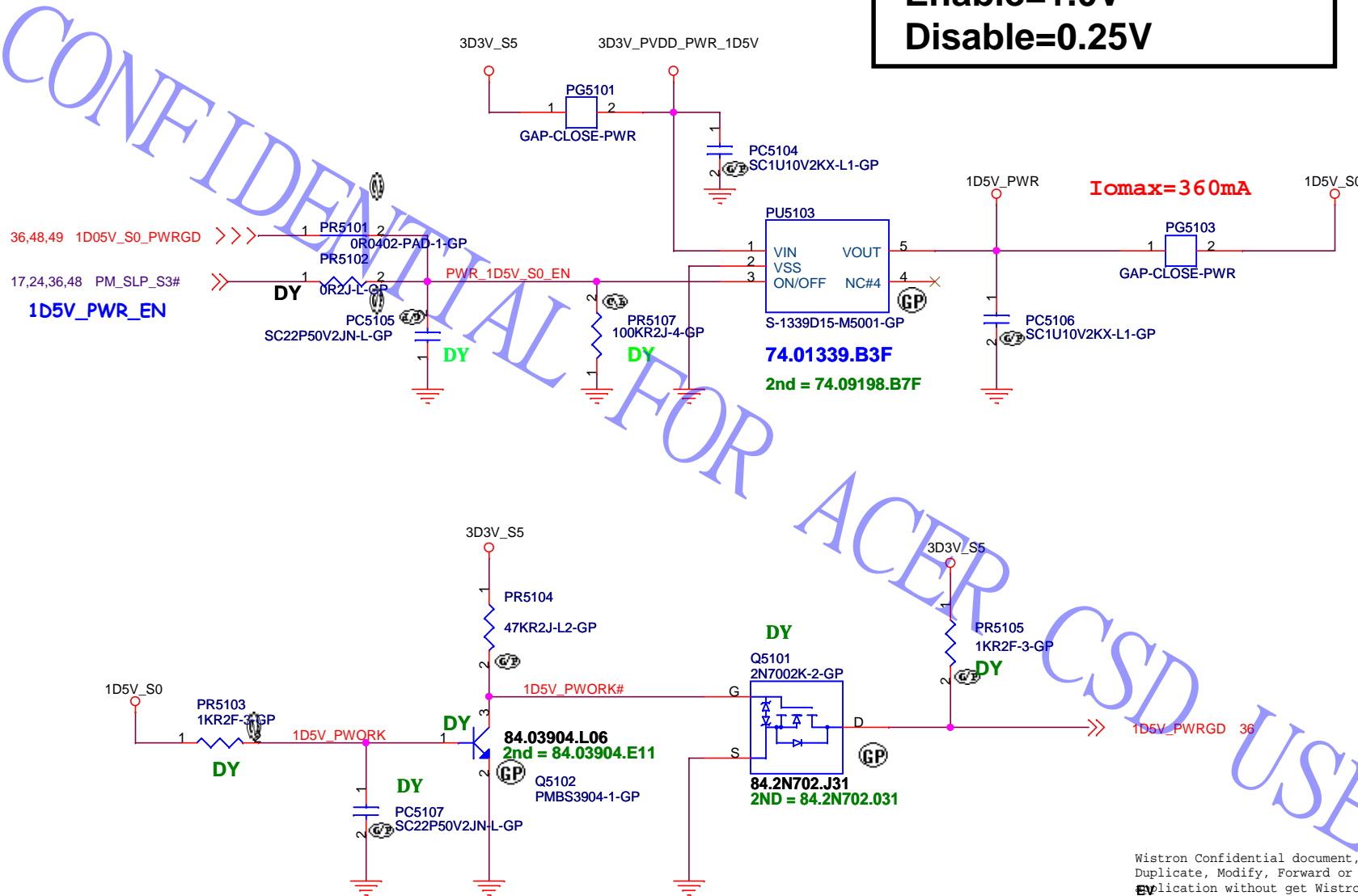
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Title			
1D8V_S0 TLV62065			
Size	Document Number		Rev
A4	Hades HBS 860M		SB
Date:	Friday, April 11, 2014		Sheet 50 of 102

S-1339D15 for 1D5V_S0
Enable=1.0V
Disable=0.25V

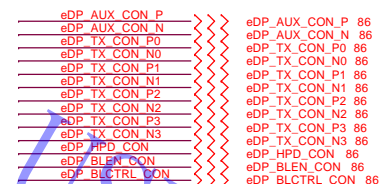
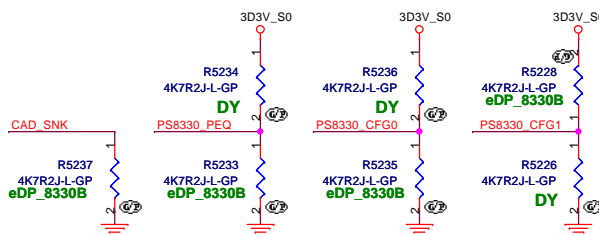
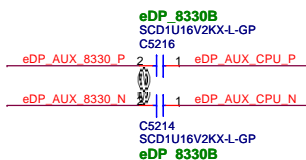
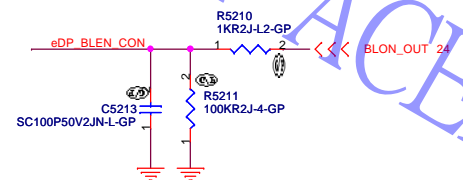
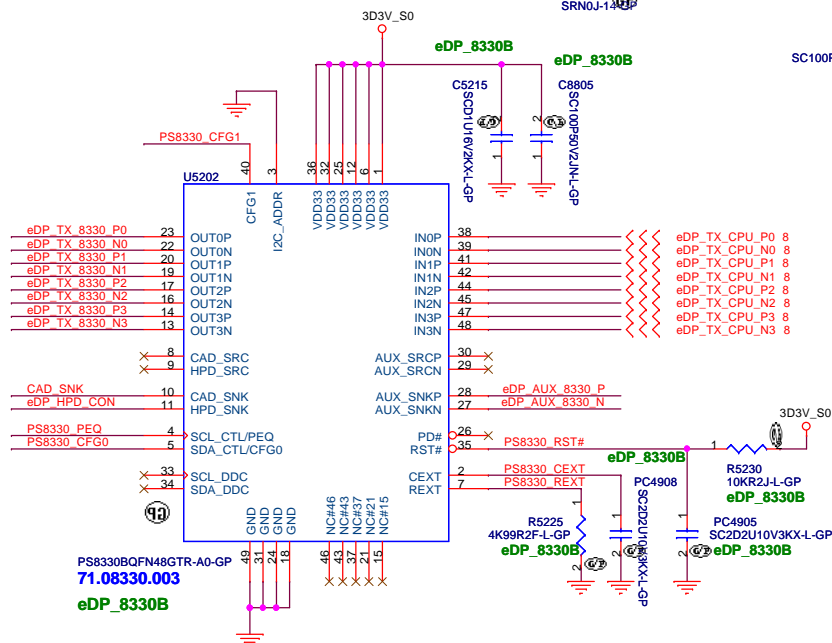
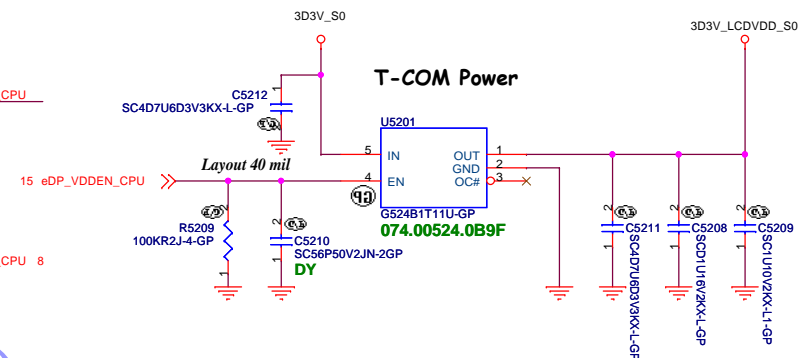
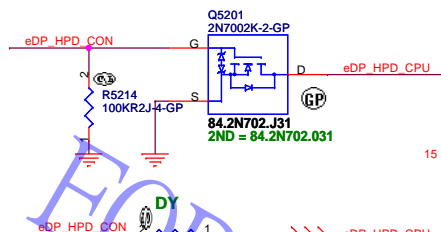
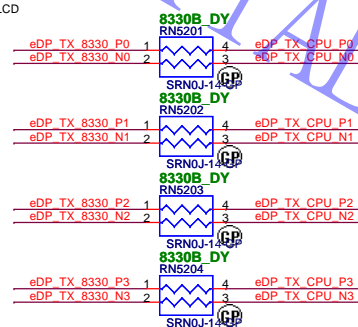
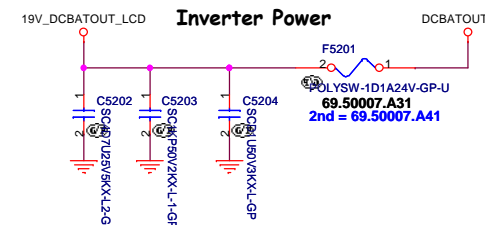
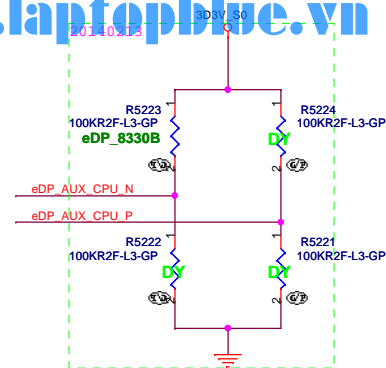


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Title		
1D5V_S0 SYW232		
Size	Document Number	Rev
Custom	Hades_HBS 860M	SB
Date:	Wednesday, May 21, 2014	Sheet 51 of 102

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Title

LCD Connector

Size	
------	--

Document Number

Hades HBS 860M

Date: Wednesday, May 28, 2014

Sheet

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of

10

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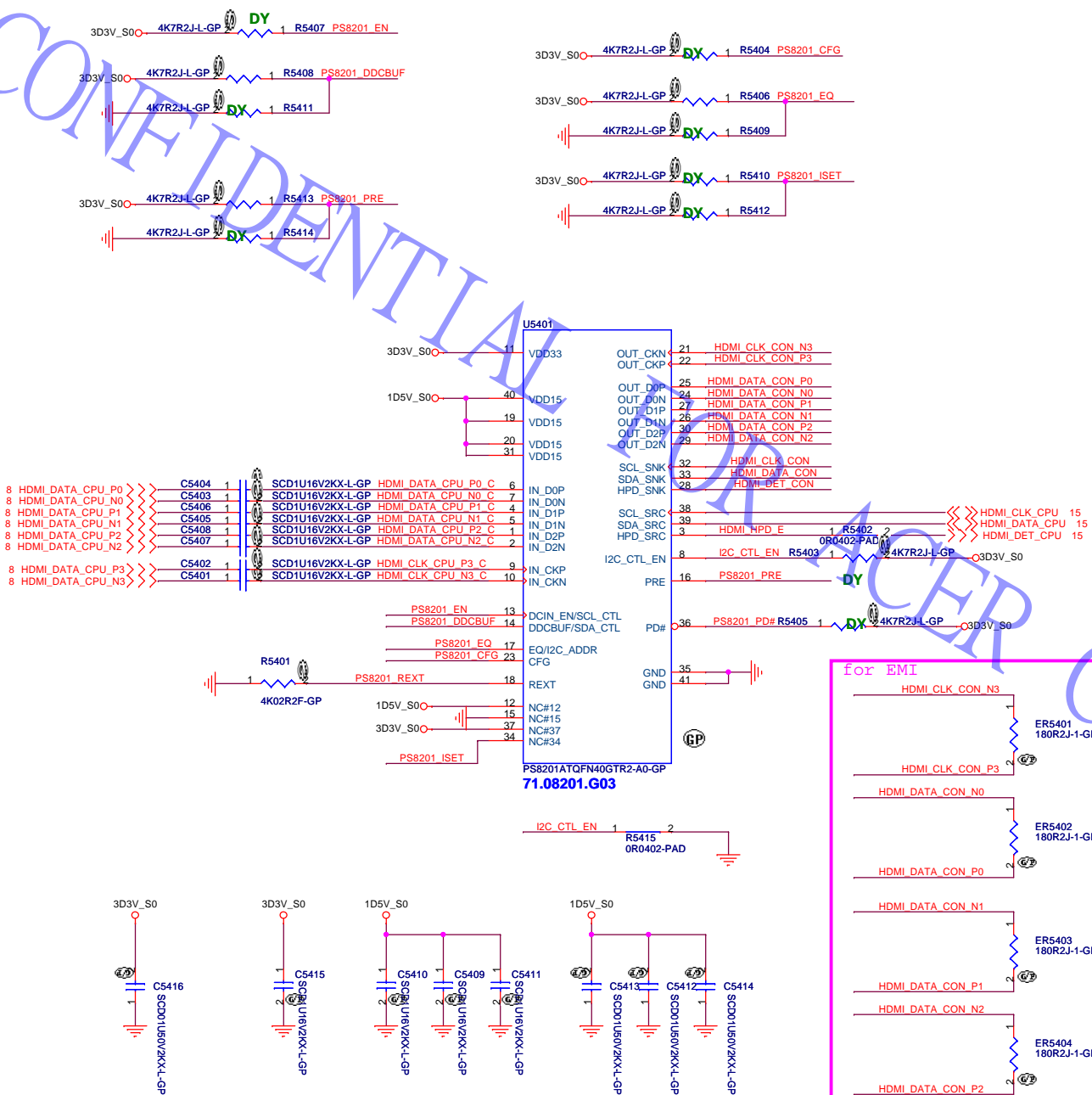
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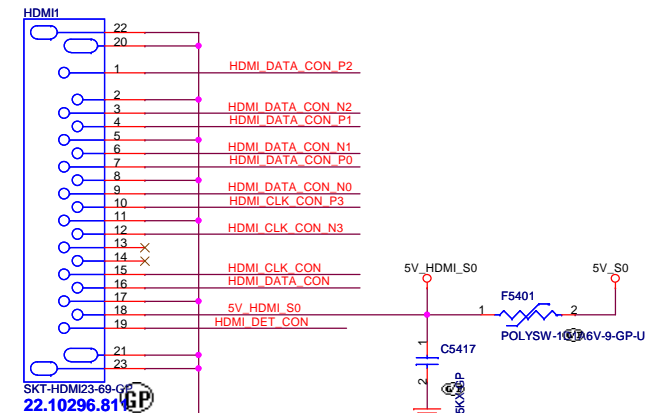
緯創資通		Wistron Corporation	
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Title			
CRT Board Connector (Reserved)			
Size	Document Number		Rev
A3	Hades HBS 860M		SB
Date: Friday, April 11, 2014		Sheet 53 of	102

SSID = VIDEO

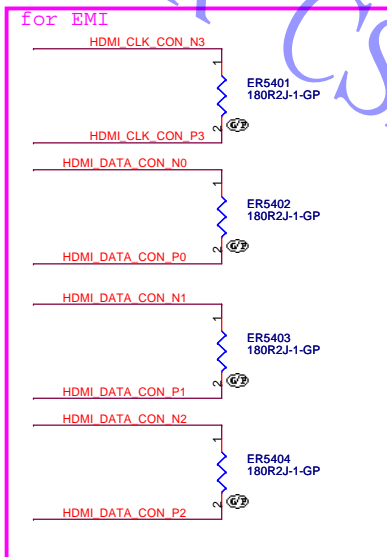
HDMI Level Shifter & CONNECTOR



HDMI CONN



1nd = 22.10296.811
2nd = 22.10296.661



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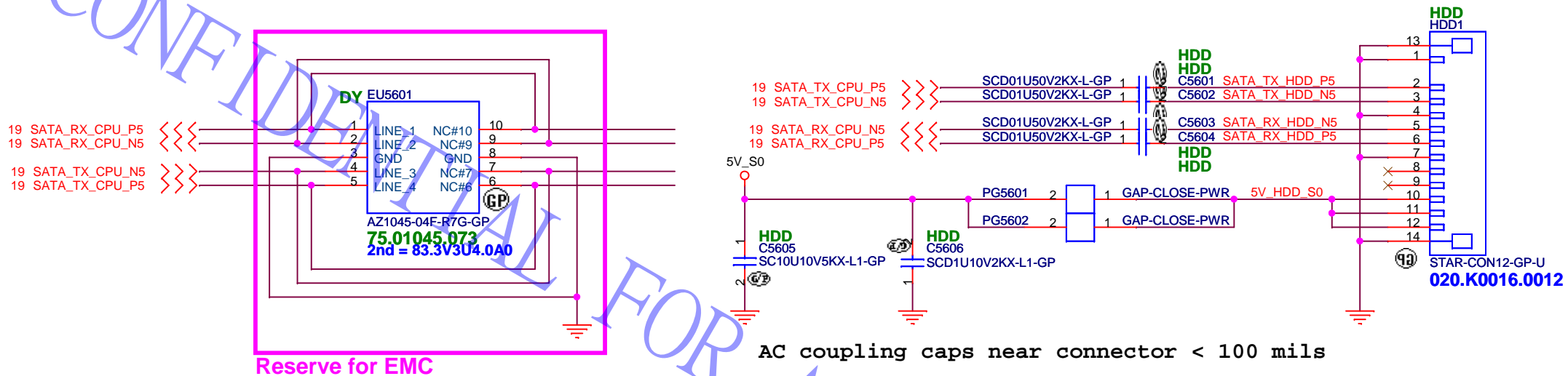
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Title			
Display Port			
Size	Document Number		Rev
Custom	Hades HBS 860M		SB
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SSID = SATA

SATA HDD Connector



SATA ODD Connector

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Title			
HDD / ODD			
Size A4	Document Number		Rev
	Hades HBS 860M		SB
Date:	Friday, April 11, 2014	Sheet	56 of 102

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Title			
E-SATA			
Size A4	Document Number		Rev
	Hades HBS 860M		SB
Date:	Friday, April 11, 2014		Sheet 57 of 102

NGFF Connector (802.11a/b/g/n)

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3D3V_LOAC

WLAN1

76
3_3Vaux
74
3_3Vaux
72
70
68
66
64
62

RESERVED#70
RESERVED#68
RESERVED#66
GPIO_NFC_RESET#N
NFC_IRQ_GPIO

Diagram illustrating the pin connections for the USB module, showing the connection of various signals to the module pins:

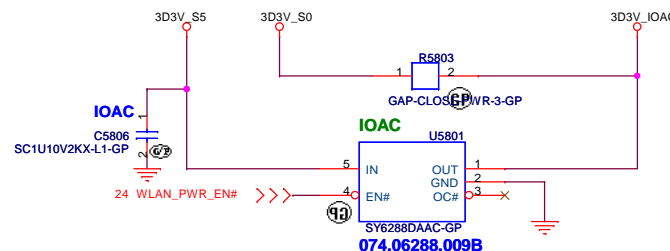
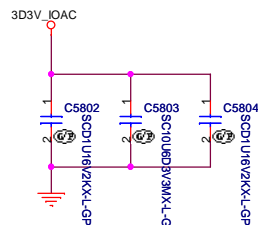
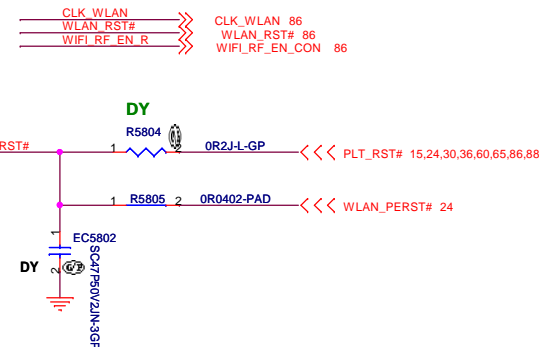
Module Pin	Signal	Value / Note
61	CLKREQ_N	18,86
49	REFCLK_N0	18,86
47	REFCLK_P0	18,86
45	GND	
43	PER_N0	16,86
41	PER_P0	16,86
39	GND	
37	PET_N0	16,86
35	PET_P0	16,86
33	GND	
23	SDIO_RESET	
21	SDIO_WAKE	
19	SDIO_DAT3	
17	SDIO_DAT2	
15	SDIO_DAT1	
13	SDIO_DAT0	
11	SDIO_CMD	
9	SDIO_CLK	
7	GND	
5	USB_D-	16,86
3	USB_D+	16,86
1	GND	
NP1	NP1	

Additional connections shown:

- WLAN_CLK_CPU# 18,86
- WLAN_CLK_CPU 18,86
- PCIE_RX_CPU_N3 16,86
- PCIE_RX_CPU_P3 16,86
- PCIE_TX_WLAN_N3 16,86
- PCIE_TX_WLAN_P3 16,86
- USB_CPU_PN5 16,86
- USB_CPU_PP5 16,86

Key_E_75P

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
MINICARD(WLAN)			
Size	Document Number	Rev	
Custom	Hades HBS 860M	SB	
Date:	Wednesday, May 28, 2014	Sheet 58 of	102

SSID = Wireless

Mini Card Connector(mSATA)

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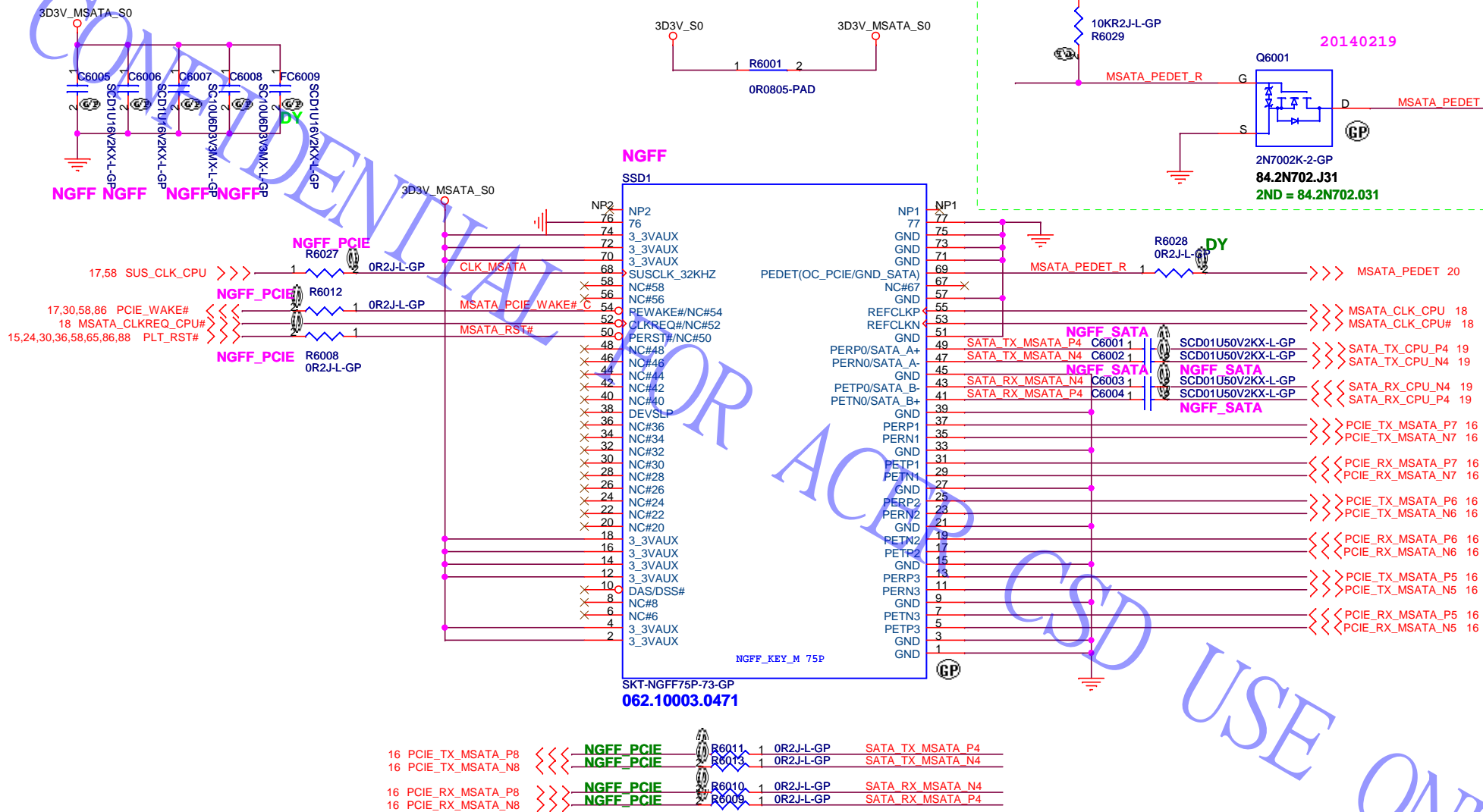
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Title			
WWAN CONN			
Size	Document Number		Rev
A4	Hades HBS 860M		SB
Date:	Friday, April 11, 2014		Sheet 59 of 102

SSID = m-SATA

Mini Card Connector (NGFF m-SATA)



SATA/PCIe Gen 2 and Gen 3 Capacitor Values

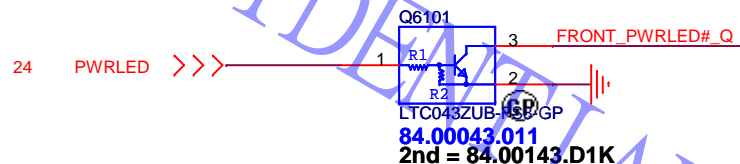
Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF ²	None ³

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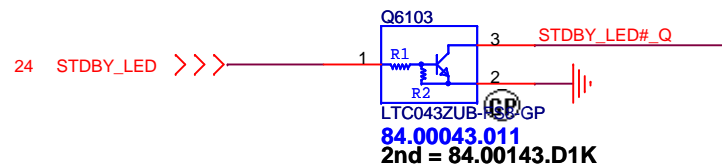
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Title: NGFF m-SATA Connector	
Size: Custom	Document Number: Hades_HBS 860M
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SSID = User.Interface

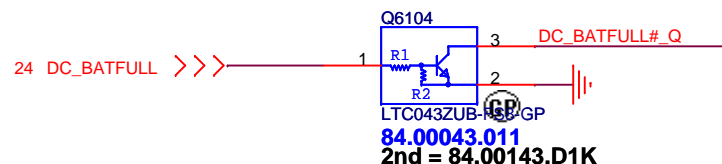
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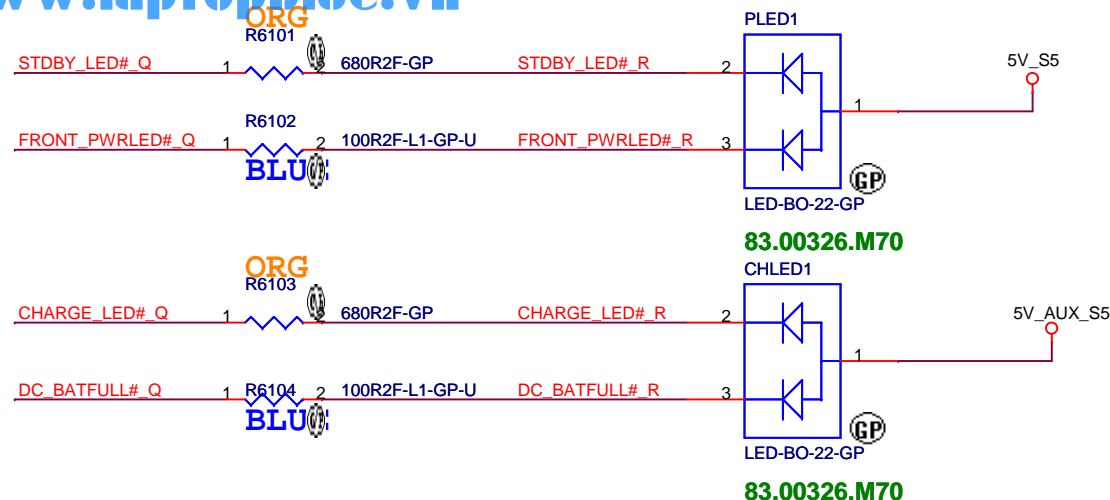
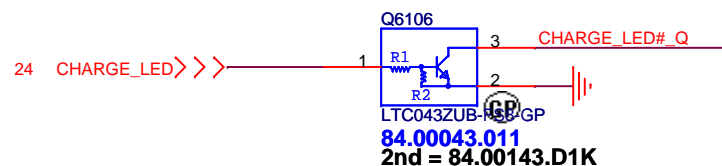
Power STDBY_LED



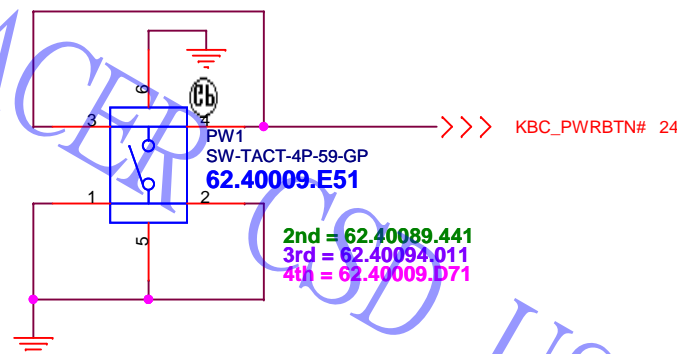
Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)



Power Button



24 KBC_PWRBTN# >>> 1 AFTP31

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Title

LED Bard/Power Button

Size
A4

Document Number

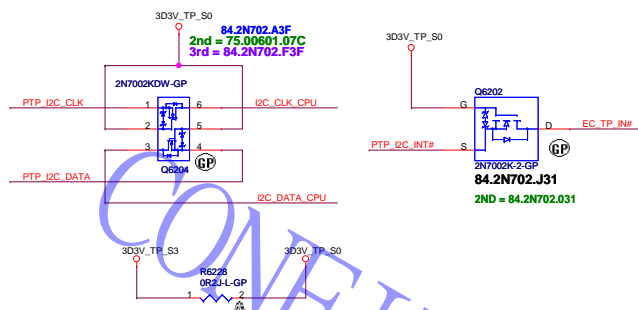
Hades HBS 860M

Rev
SB

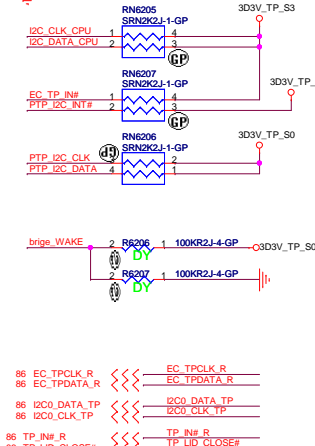
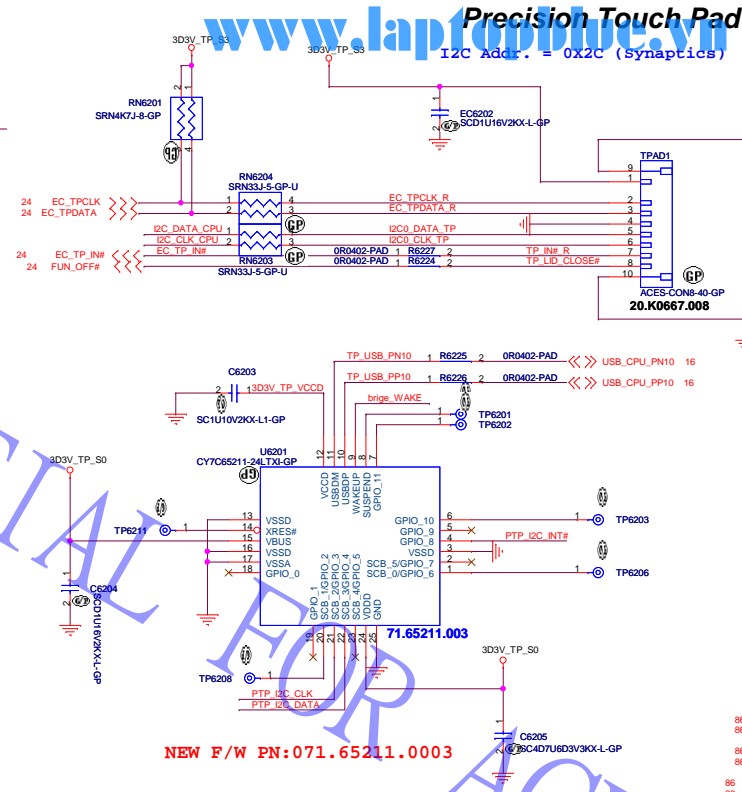
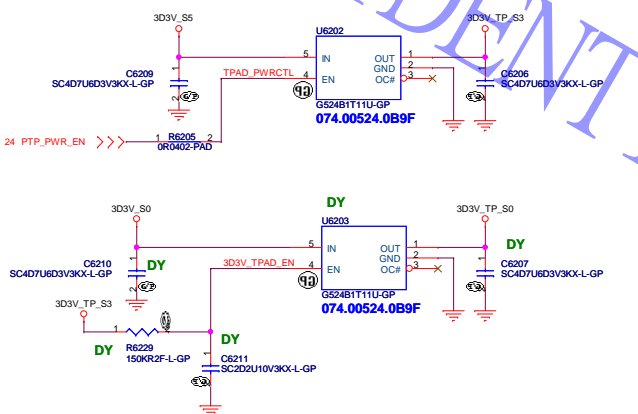
Date: Monday, May 26, 2014

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Pin Number	Pin Definition
1	VCC (3.3V_50 / 3.3V_55)
2	PS/2 Clock
3	PS/2 Data
4	GND
5	I2C Data
6	I2C Clock
7	Interrupt# / Wake#
8	Button# / LID_CLOSED

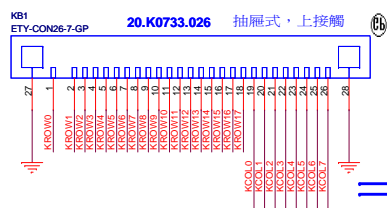


Firmware adds to delay 90ms to access TP device



NEW F/W PN:071.65211.0003

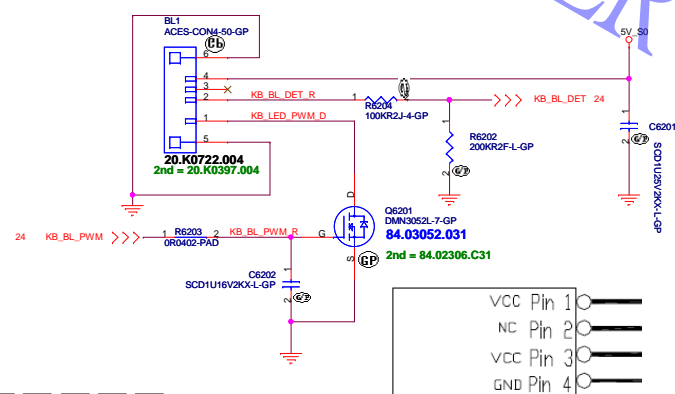
Internal KeyBoard Connector



```

MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

```



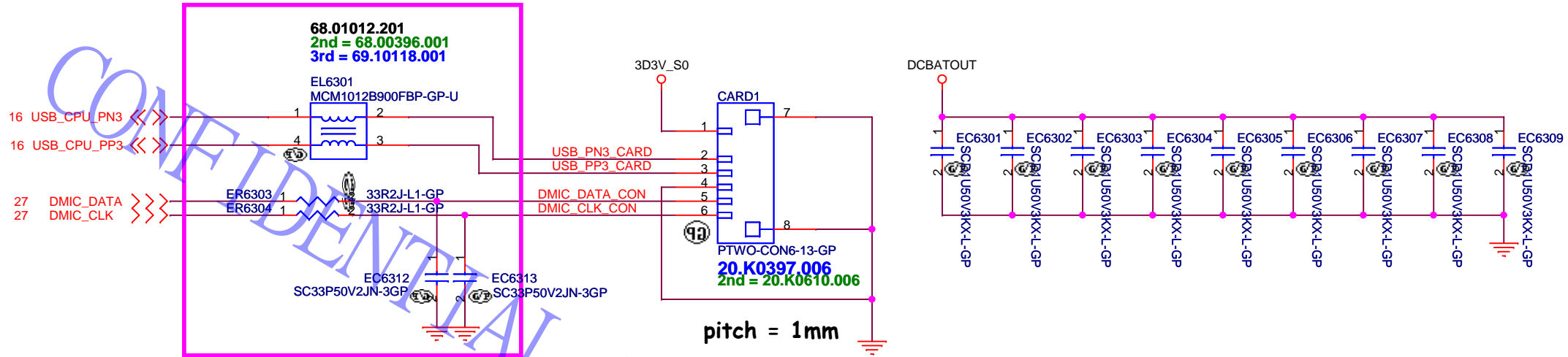
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2 (C07)		14				46	62	131	49	50	61	129	41	5	79	84	76	102
3 (C06)		31				47	60	48	34	51	53	132	54	55	80	40	101	86
4 (C05)		30	57			32	EZ3	33	35	36	52	130	€		83	29	85	104
5 (C04)		16			127	18	EZ4	19	20	22	38	100	39	27	45	43	99	56
6 (C03)		1		58		3	EZ6	5	6	8	24	91	25	11	13	15	92	98
7 (C02)		112	44			113	EZ5	115	7	9	119	105	10	123	124	126	106	93
8 (C01)	59	110				114	EZ2	116	117	118	120	96	121	122	90	81	95	108
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
	R01	R02	R03	R04	R05	R06	R07	R08	R09	R10	R11	R12	R13	R14	R15	R16	R17	R18

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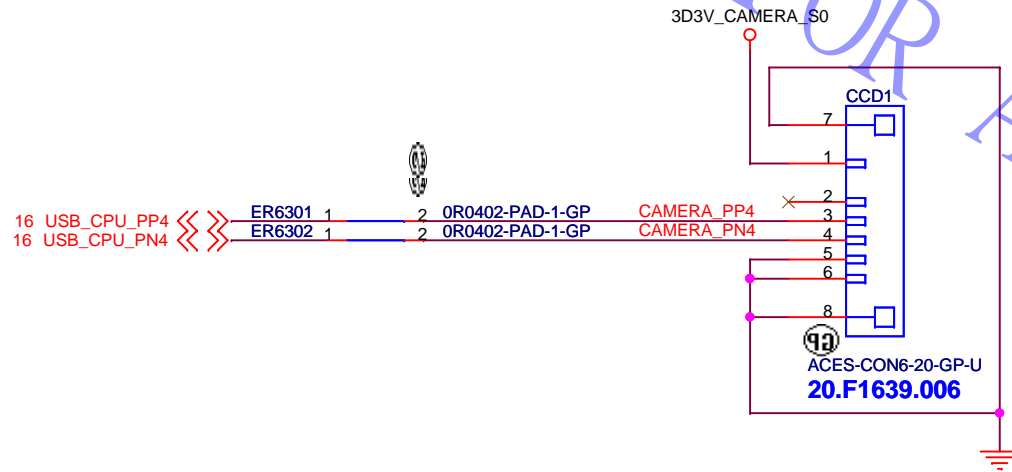
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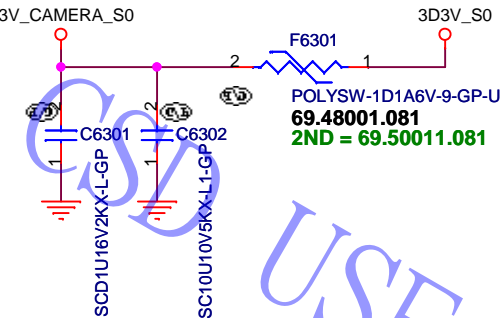
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Key Board/Touch Pad			
Size	Document Number		Rev
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Date:	Wednesday, June 04, 2014	Sheet 62 of	102



Reserve for EMC



Camera Power



86 USB_PN3_CARD <<<>>> USB_PN3_CARD
86 USB_PP3_CARD <<<>>> USB_PP3_CARD
86 DMIC_DATA_CON <<<>>> DMIC_DATA_CON
86 DMIC_CLK_CON <<<>>> DMIC_CLK_CON

86 CAMERA_PP4 <<<>>> CAMERA_PP4
86 CAMERA_PN4 <<<>>> CAMERA_PN4

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Title

IO Board Connector

Size
A4

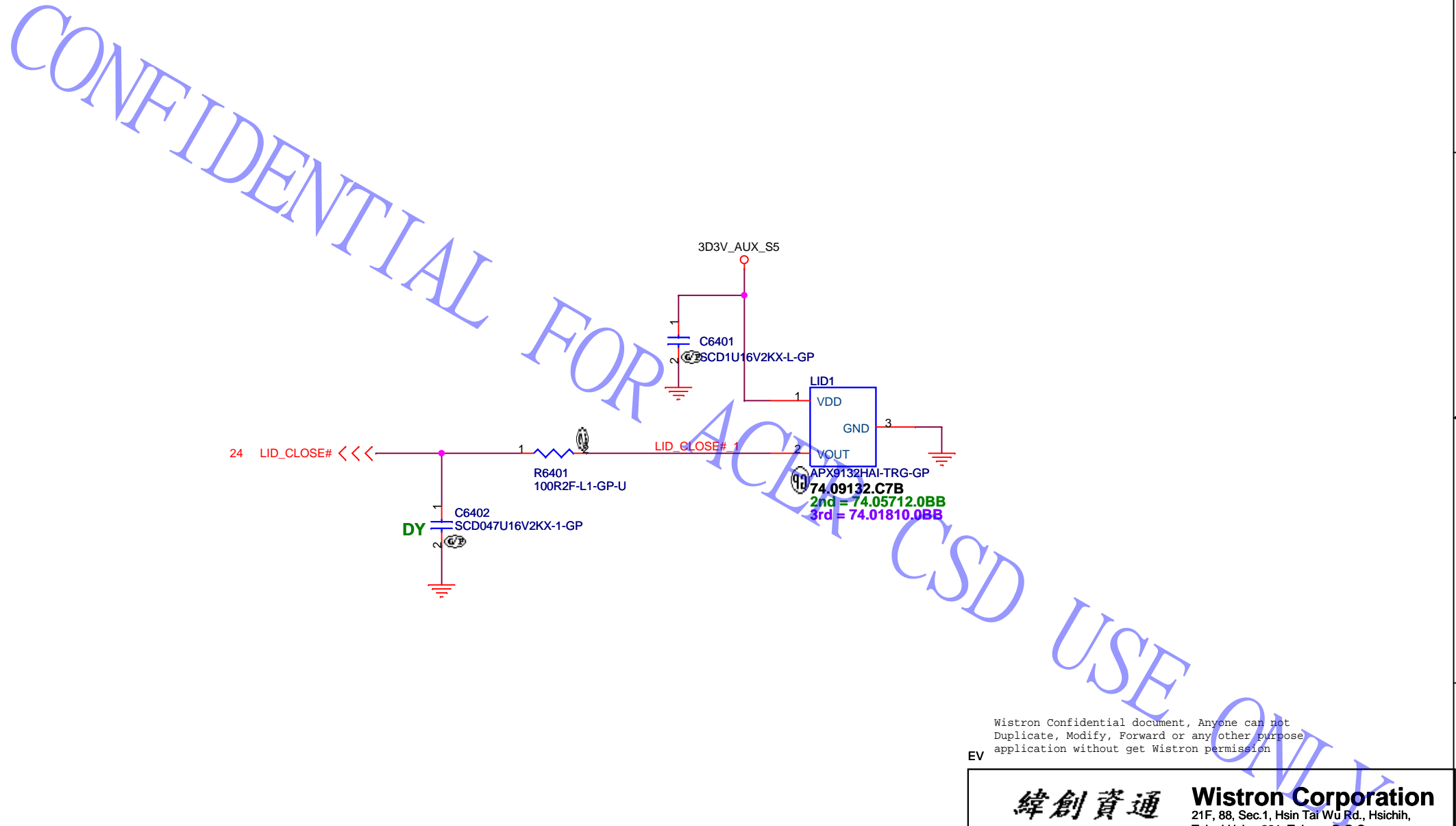
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SB

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Title

Hall Sensor

Size
A4

Document Number

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Rev
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Date: Friday, April 11, 2014

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Title			
SENSOR HUB			
Size	Document Number		Rev
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Free Fall Sensor

Note www.laptopblue.vn

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

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Title			
G Sensor			
Size A	Document Number		Rev
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Thunderbolt (1/5)	
Size	Document Number
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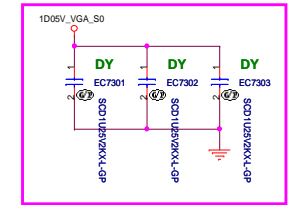
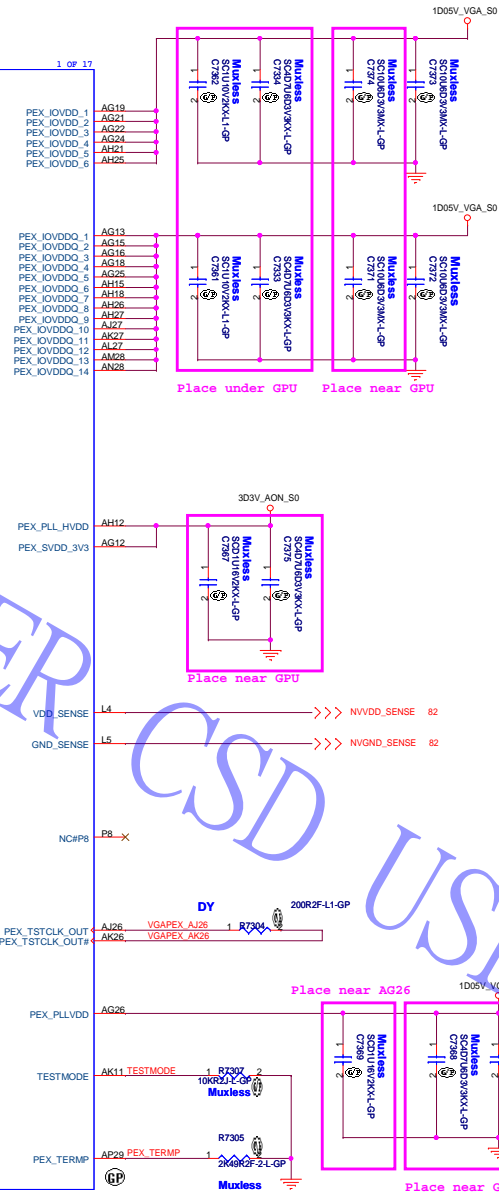
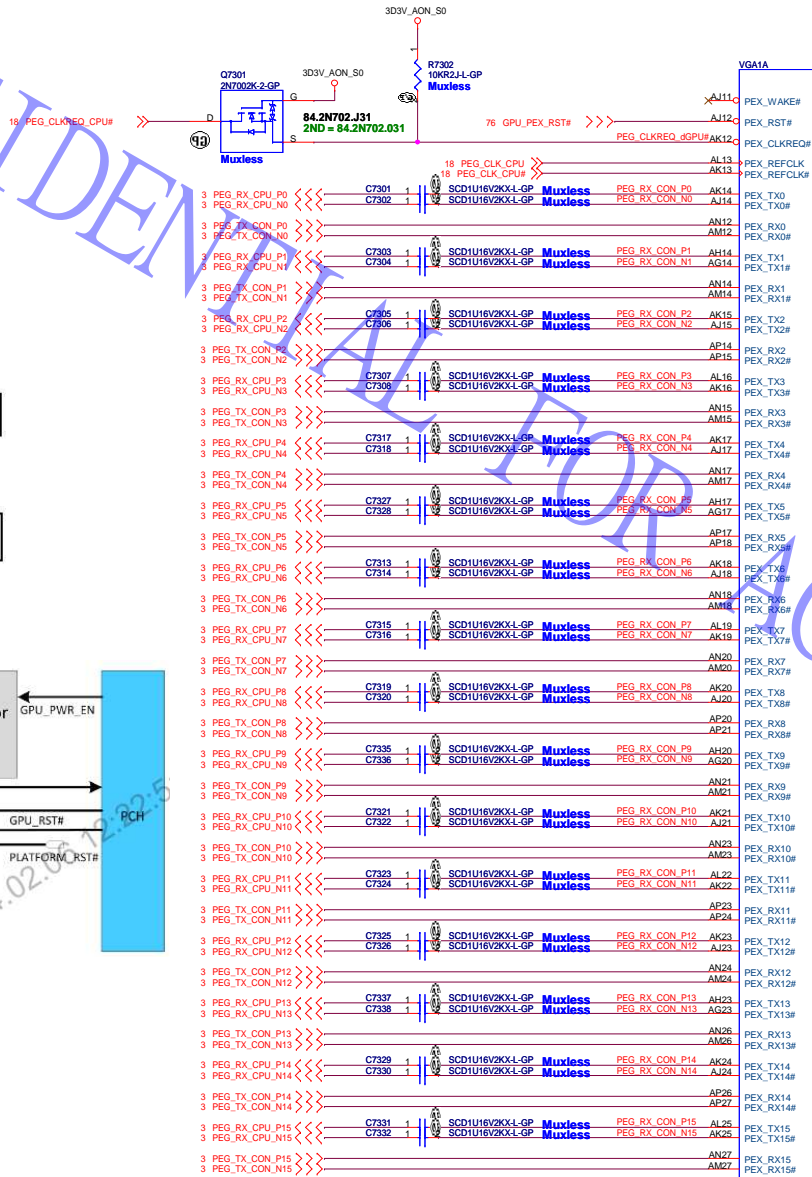
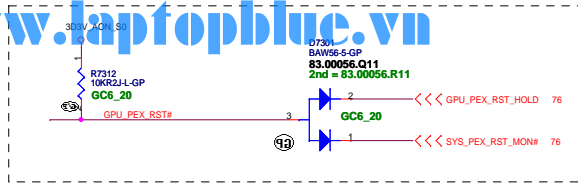
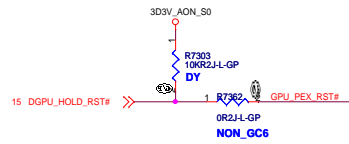
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Thunderbolt (4/5)					
Size	Document Number				Rev
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Title Thunderbolt (5/5)			
Size A4	Document Number Hades HBS 860M		Rev SB
Date: Friday, April 11, 2014		Sheet 72 of	102

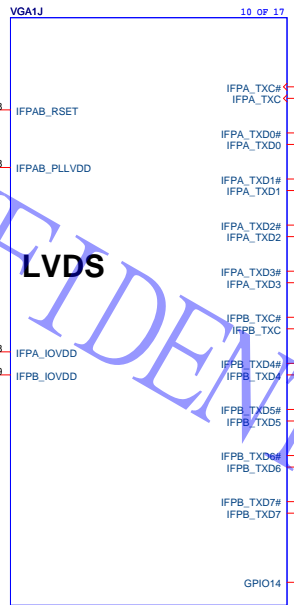


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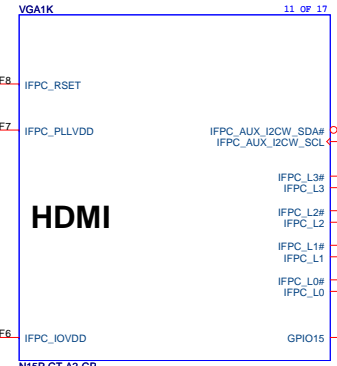
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Size	Document Number	Rev	
Custom	Hades HBS 860M	SB	
Date:	Friday, April 11, 2014	Sheet 73 of	102



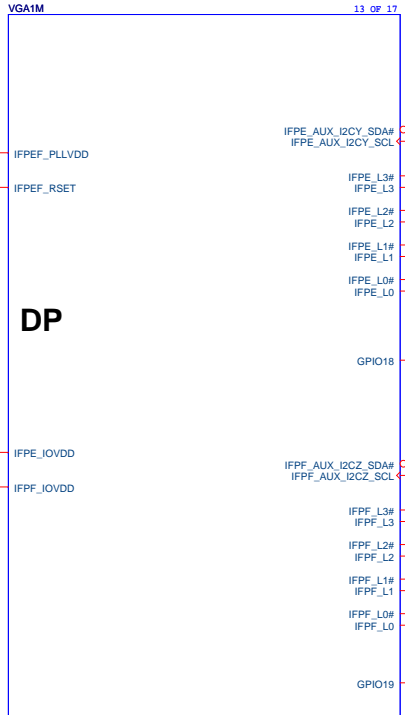
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Muxless



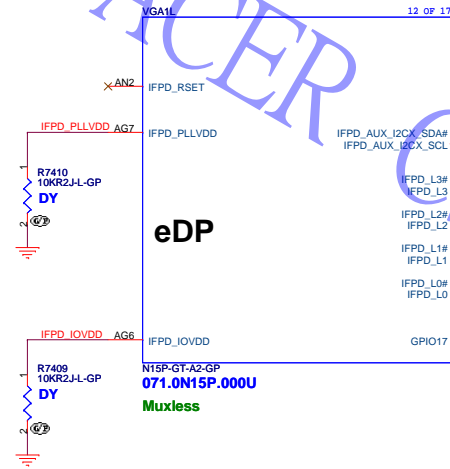
HDMI

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071.0N15P.000U
Muxless



DP

N15P-GT-A2-GP
071.0N15P.000U
Muxless



eDP

N15P-GT-A2-GP
071.0N15P.000U
Muxless

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GPU (DIGITALOUT)			
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HW.3 I2CS RESERVED SLAVE ADDRESS

The N155-GX and N15P-GX/GT GPUs use the I2CS slave address 0x6 for NVIDIA internal testing. To avoid address conflict, the I2C address 0x6 should not be used by other I2C devices on the same bus as the GPU. The SMB_ALT_ADDR strap does not affect this 0x6 address.

Table 2. Memory Configurations for Testing

Products	Type	VRAM Voltage	Vendor	Qty Parts	Memory Bus Width	Density	Speed Bin (MHz)	Part Number
H155-GX	DDR3	1.5V	Hynix	8	128 bits	256MX16	1000	H5TC4G63AFR-11C
H15P-GT	DDR3	1.5V	Hynix	8	128 bits	256MX16	1000	H5TC4G63AFR-11C
	GDDR5	1.35V	Hynix	8	128 bits	256MX16	2500	H5GC4H24MFR-T2C
H15P-GX	GDDR5	1.35V	Hynix	8	128 bits	256MX16	2500	H5GC4H24MFR-T2C

Table 11. N15P-GX/GT GDDR5 Recommended Memories

Memory Type	FBVDD/FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CL Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V, 1.35V	128Mx16	Samsung	K4G20325FD-FC03	D-die	0x0	2500	H/A	Post-production candidate
			Hynix	H5GC2H24BFR-T2C	B-die	0x1	2500	H/A	Post-production candidate
			Micron	EDW2032B8E-4A-F	B-die	0x6	2500	H/A	Post-production candidate
	1.35V, 1.35V	256Mx16	Hynix	H5GC4H24MFR-T2C	A-die	0x2	2500	H/A	Production candidate
			Samsung	K4G41325FD-FC03	C-die	0x3	2500	H/A	Production candidate
			Micron	EDW2032B8E-4A-F	A-die	0x4	2500	H/A	Post-production candidate

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kOhm	1000	0000
10 kOhm	1001	0001
15.0 kOhm	1010	0010
20.0 kOhm	1011	0011
24.9 kOhm	1100	0100
30.1 kOhm	1101	0101
34.8 kOhm	1110	0110
45.3 kOhm	1111	0111

4.99kOhm 64.49915.6DL
10kOhm 64.10025.10L
15kOhm 64.15025.6DL
20kOhm 64.20025.6DL
24.9kOhm 64.24925.6DL
30.1kOhm 64.30125.6DL
34.8kOhm 64.34825.6DL
45kOhm 64.45325.6DL

Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCL	S0R3_EXPOSED	S0R2_EXPOSED	S0R1_EXPOSED	S0R0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND and stuff 50k pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND for forward compatibility.			
STRAP2				
STRAP3				
STRAP4				

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TABLE
GDDR5 VIDEO MEMORY

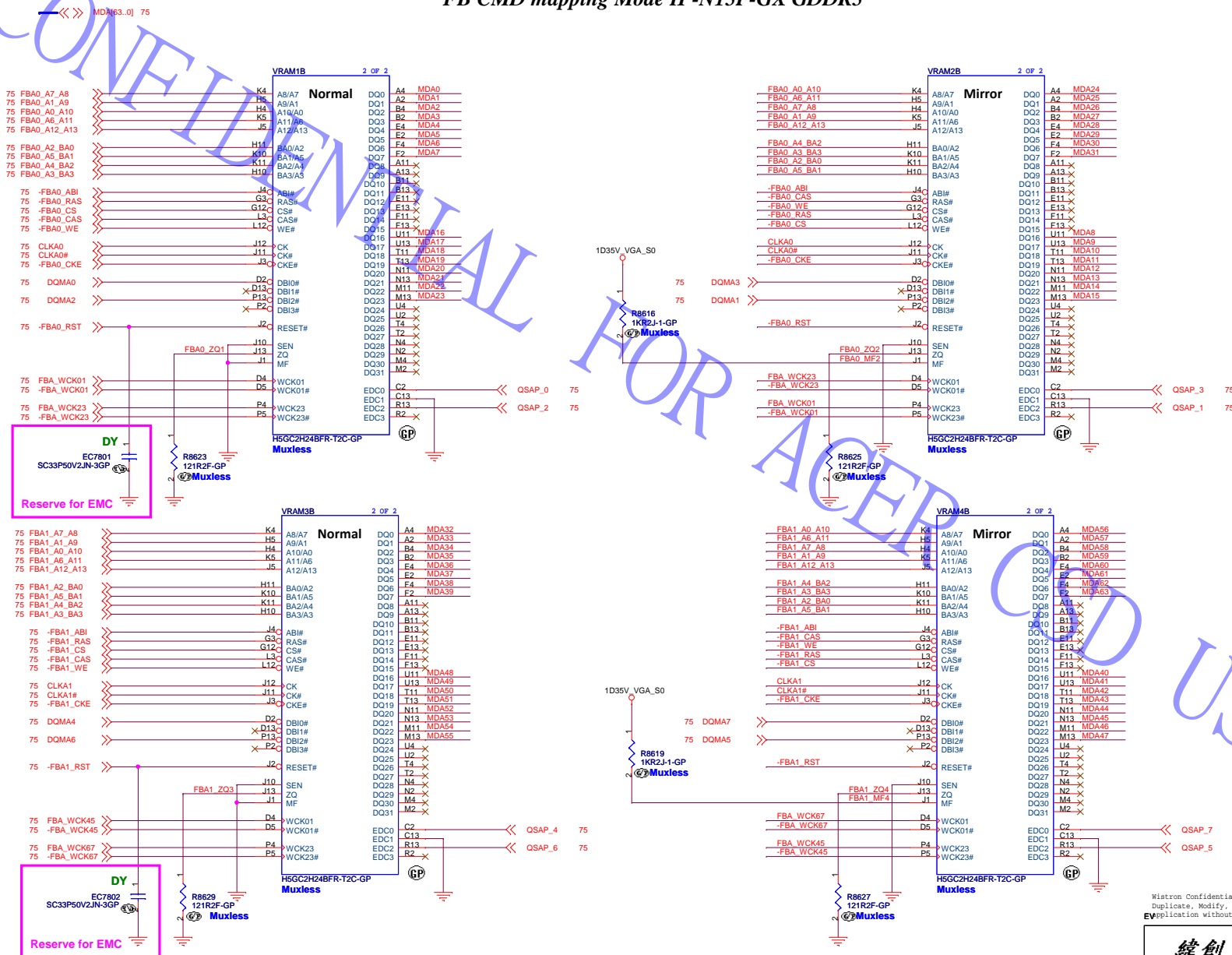
72.05224.A0U

72.20325.B0U

	HYNIX 2GBITS (64Mx32)	SAMSUNG 2GBITS (64Mx32)	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)
U91 U92 U93 U94 U95 U96 U97 U98	H5GQ2H24AFR-T2C	K4G20325FD-FC04	H5GC4H24MFR (tentative)	K4G41325FC-HC03 (tentative)

FB CMD mapping Mode H -N15P-GX GDDR5

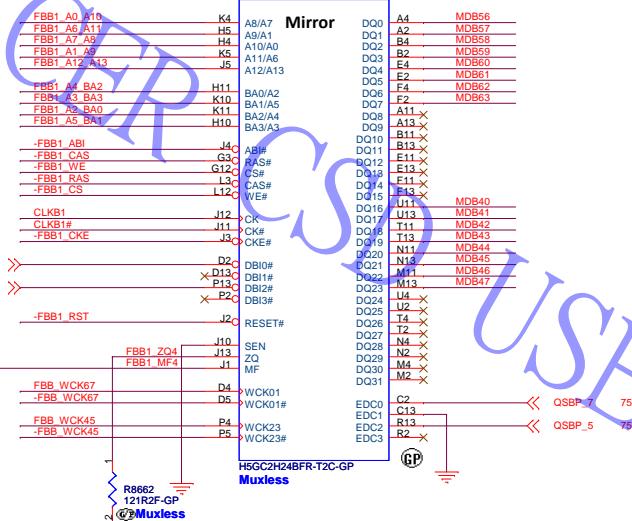
LOGIC



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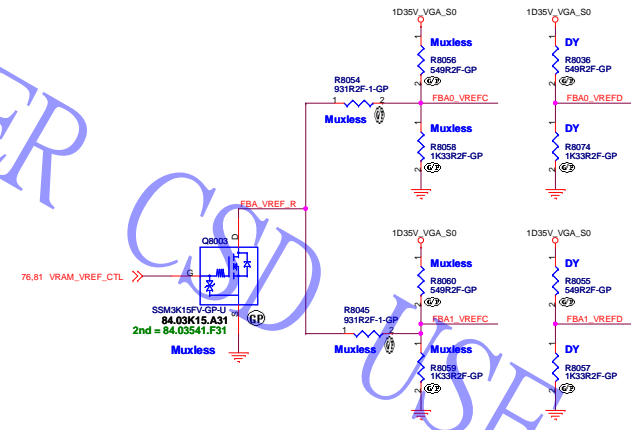
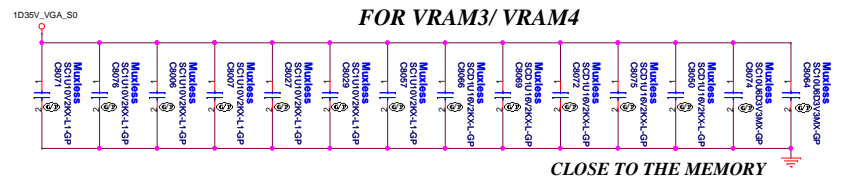
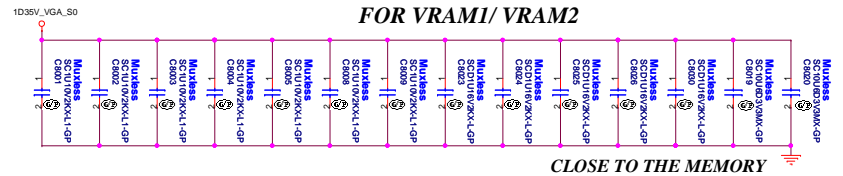
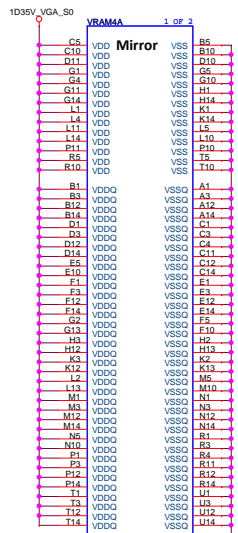
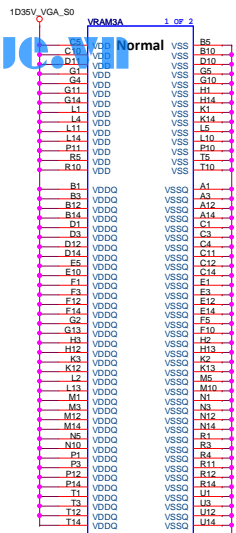
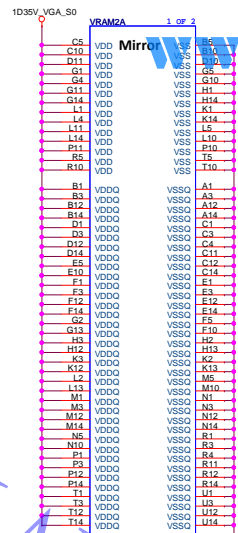
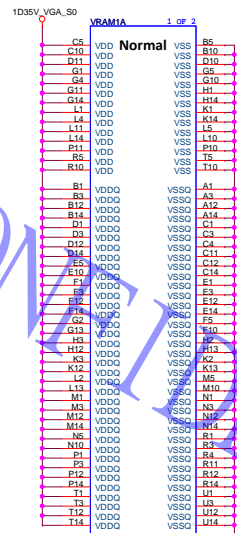
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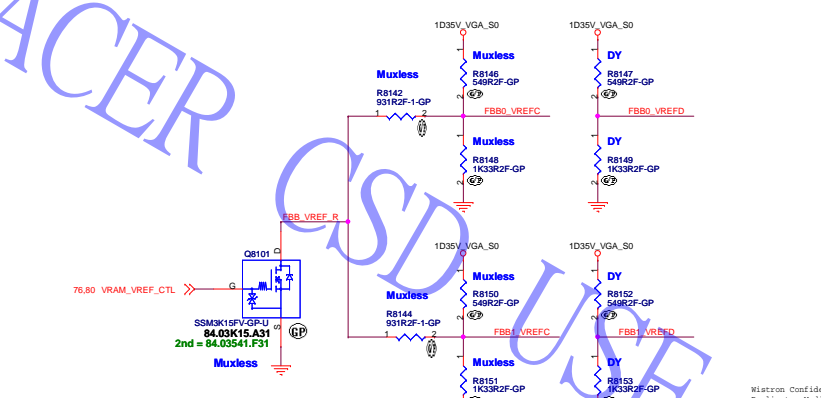
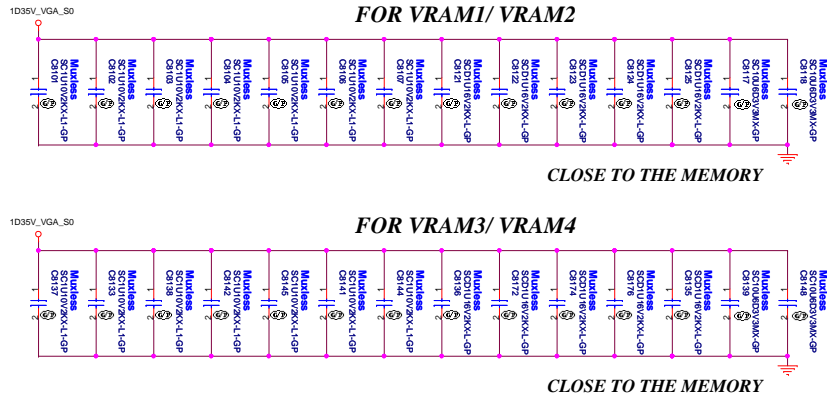
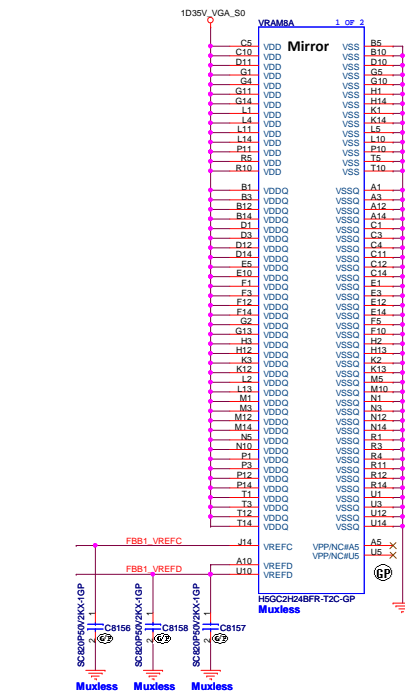
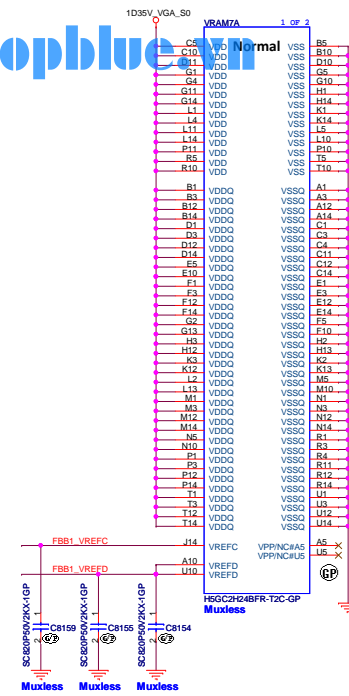
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Custom			SB
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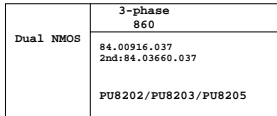
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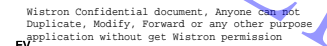
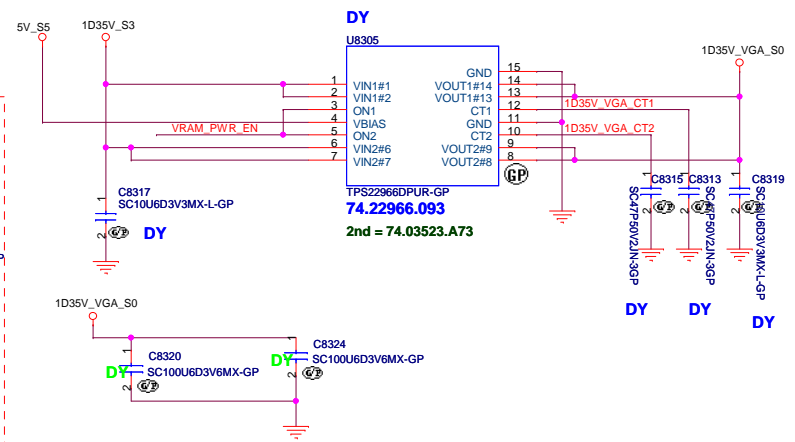


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EDP-Cont.	515 A	40.89 A	43 A
EDP-Peak	515 A	40.89 A	80 A
PR8222	27K ohm	39K ohm	20K ohm
PR8206	7.5K ohm	30K ohm	20K ohm
PR8208	0 ohm	3K ohm	2K ohm
PR8209	6.2K ohm	24K ohm	18K ohm
PR8214	1.74K ohm	3K ohm	0 ohm
PC8223	5.6nF	1.8nF	2.7nF



Title			
RT8813A VGA CORE			
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0.35V(For VRAM GDDR5)



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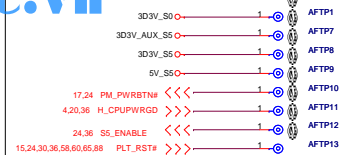
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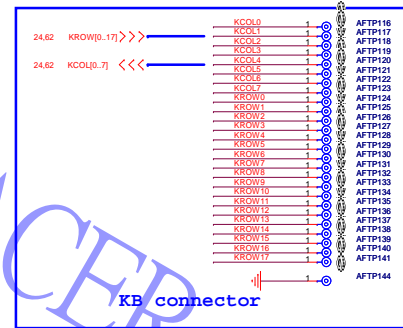
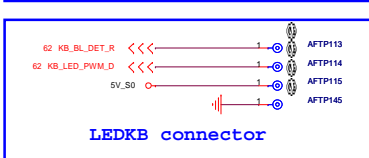
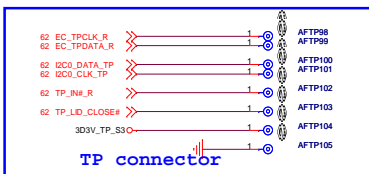
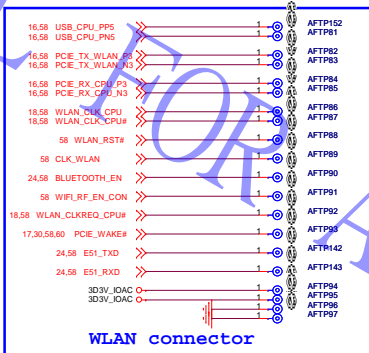
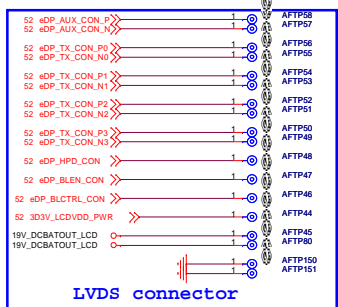
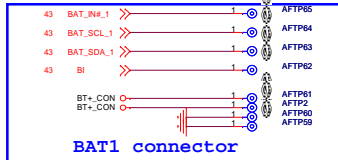
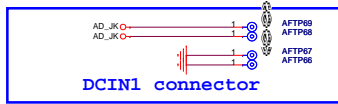
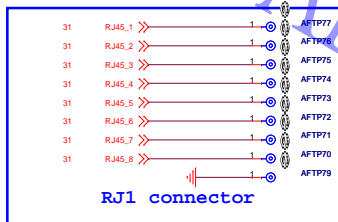
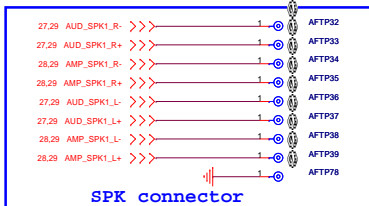
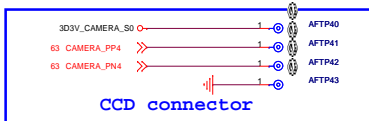
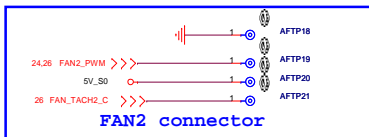
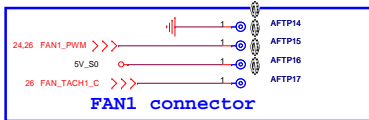
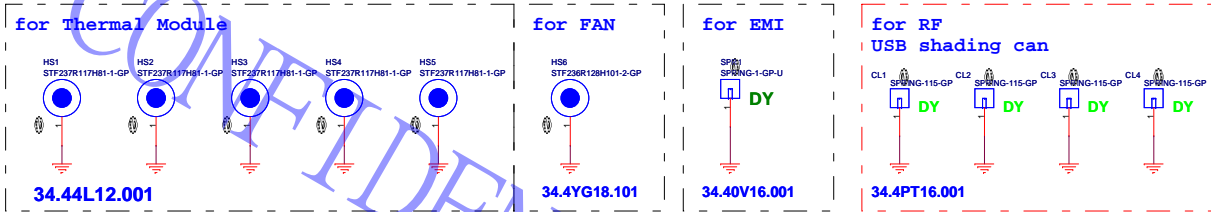
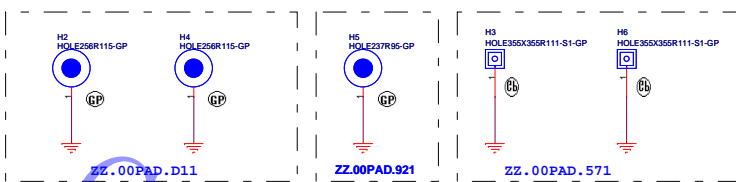
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Test Point放在Dimm Door打開可量測處



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Title			
UNUSED PARTS/EMI Capacitors			
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Title Express Card			
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Title			
Smart Card socket			
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Bottom Docking			
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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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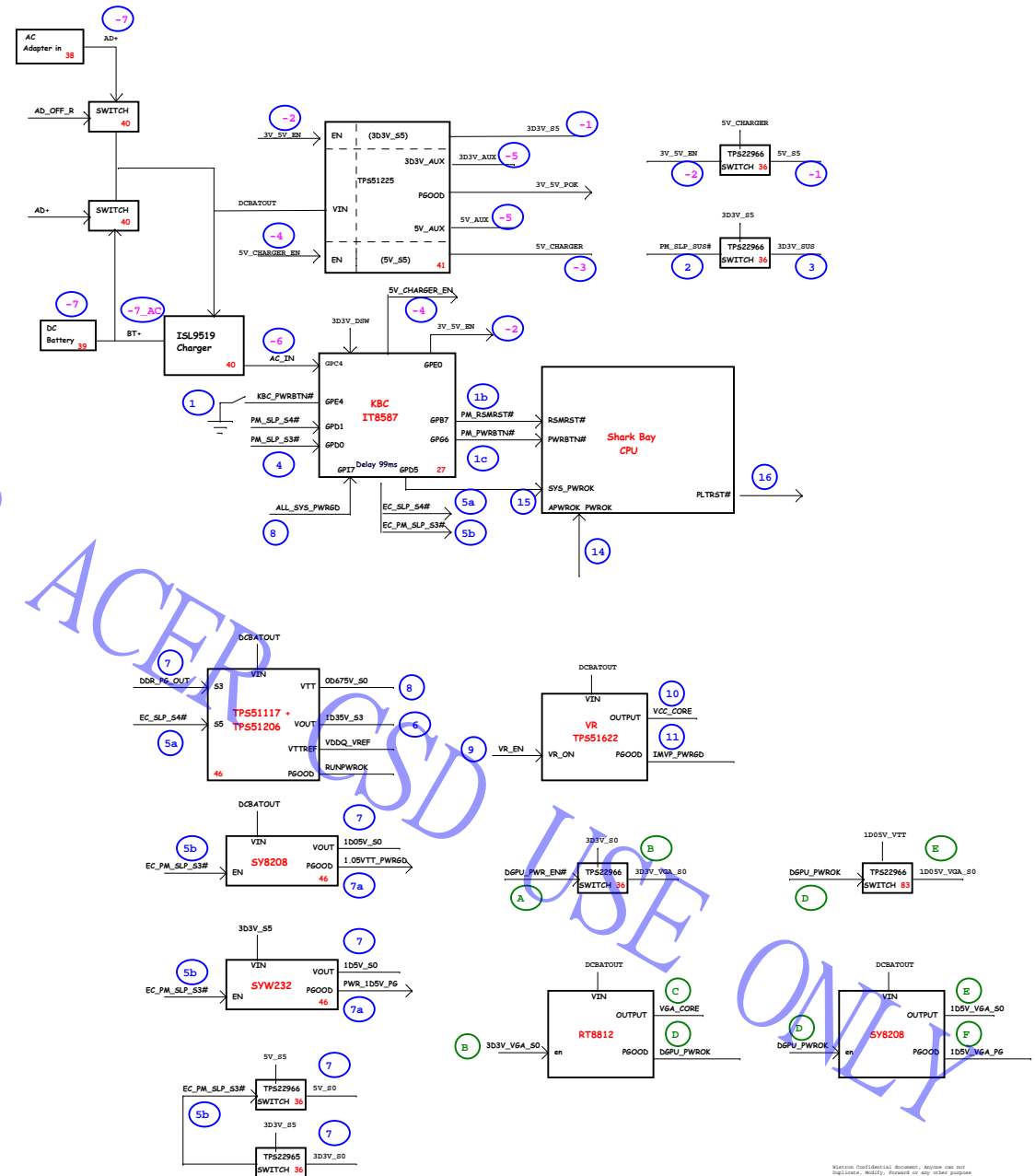
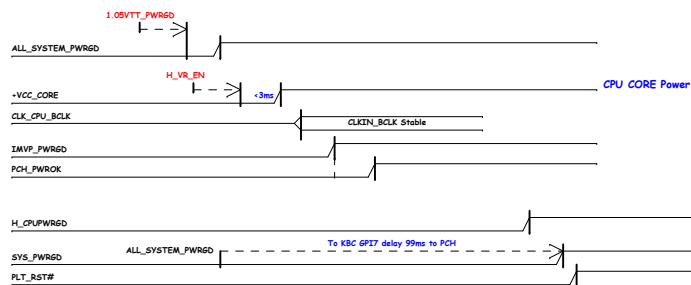
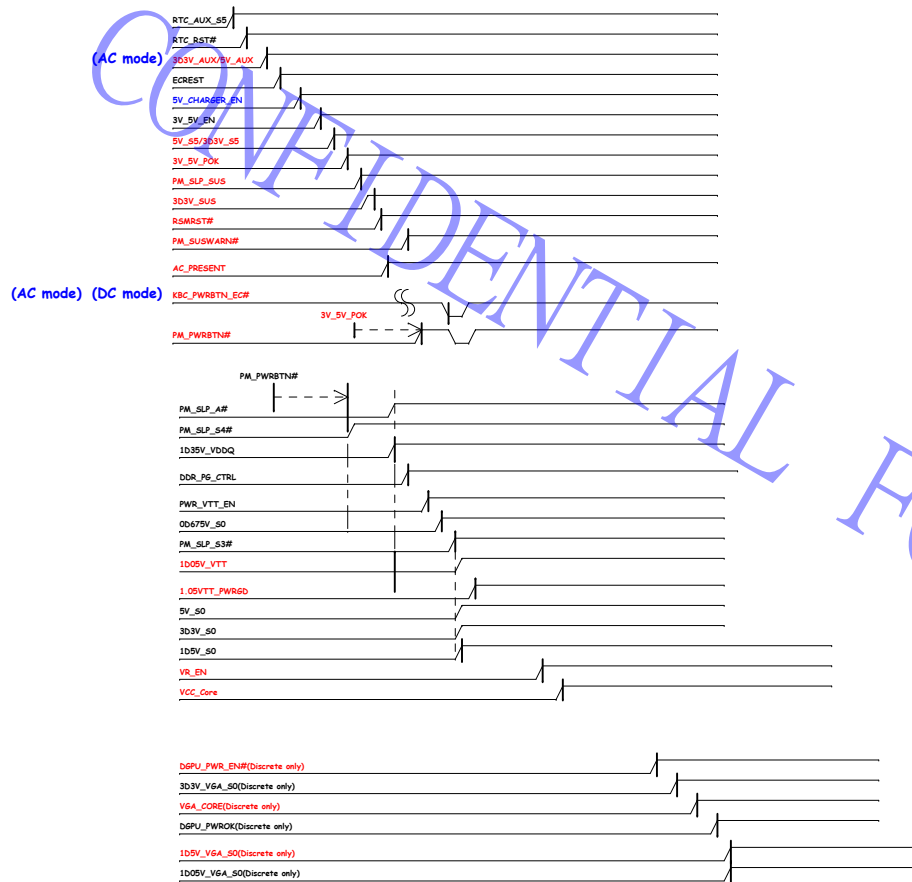
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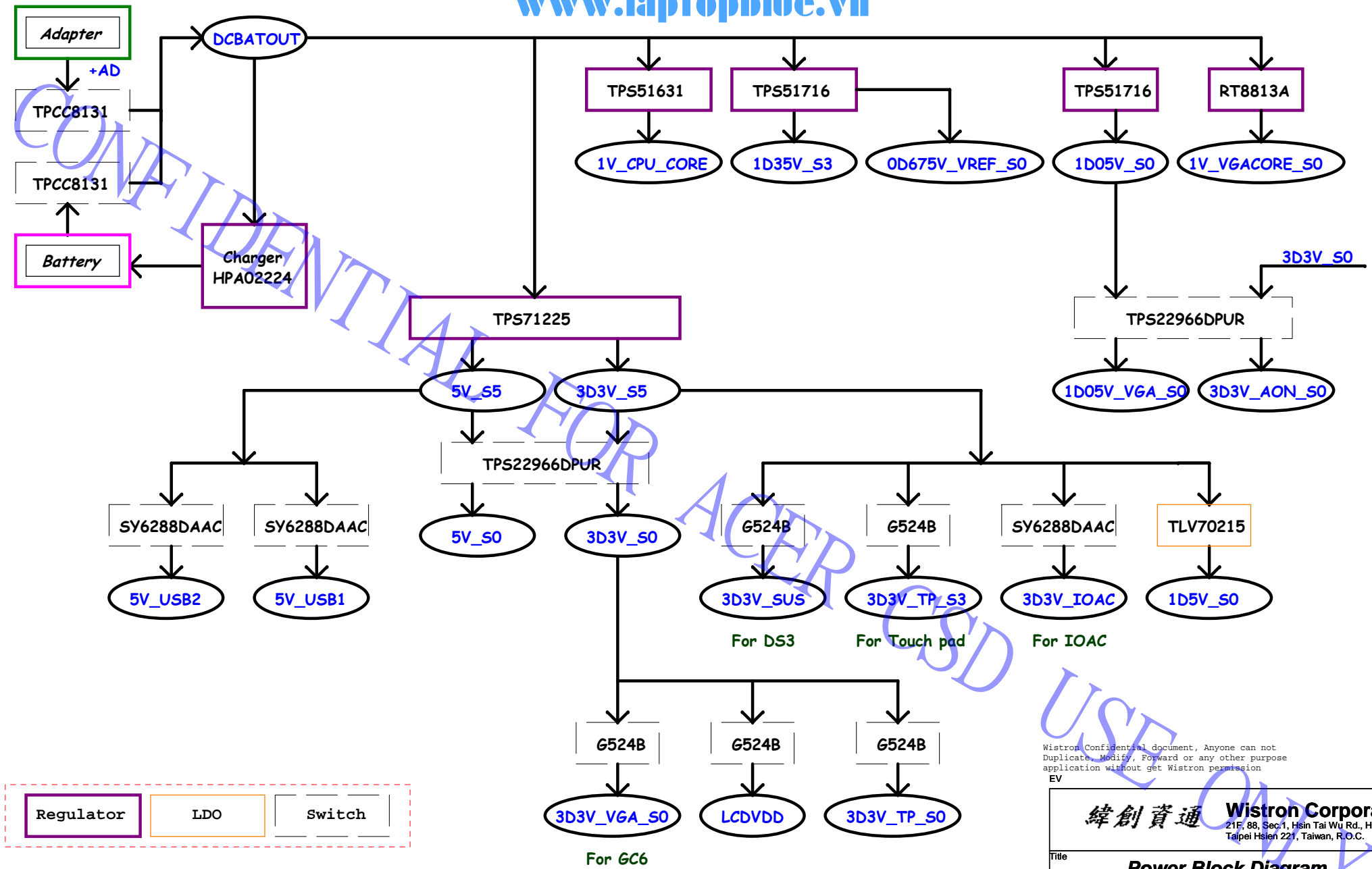
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Intel-Power Up Sequence

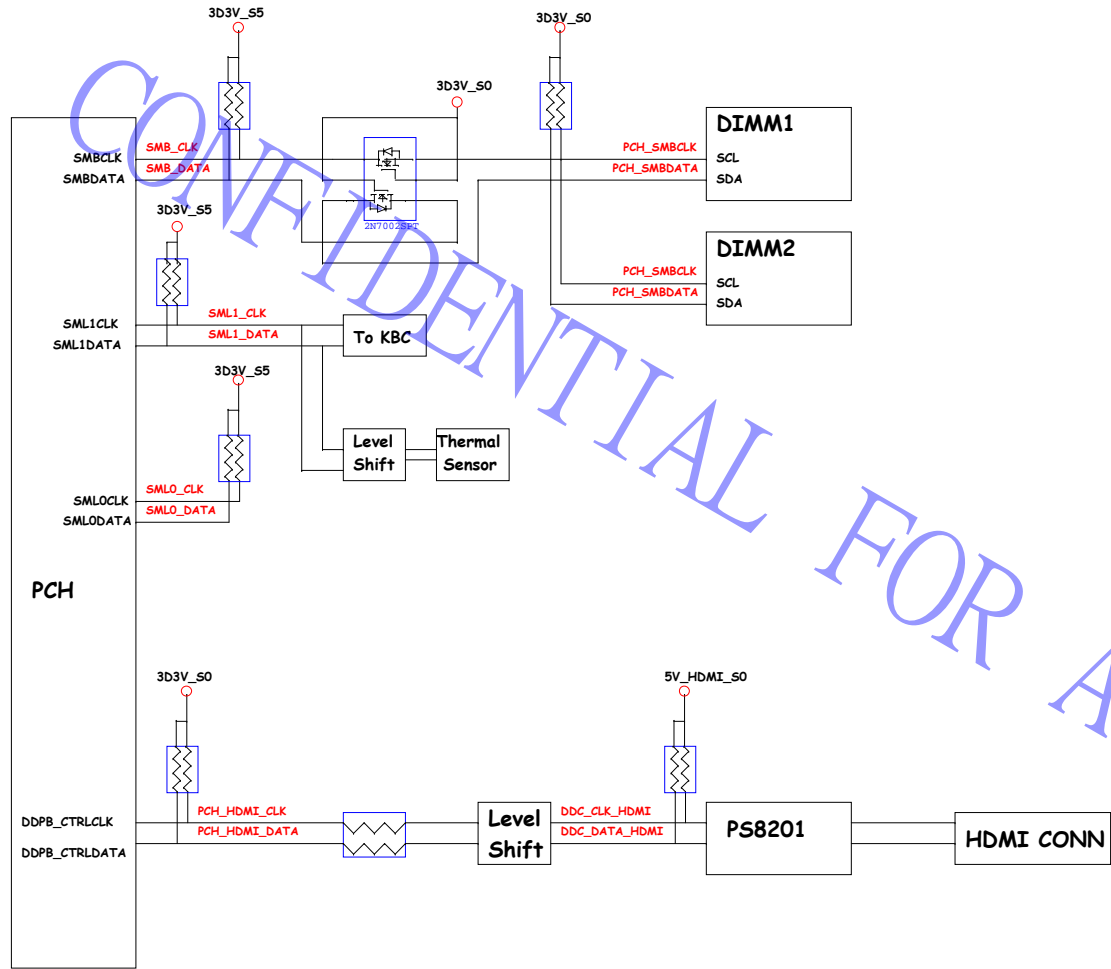




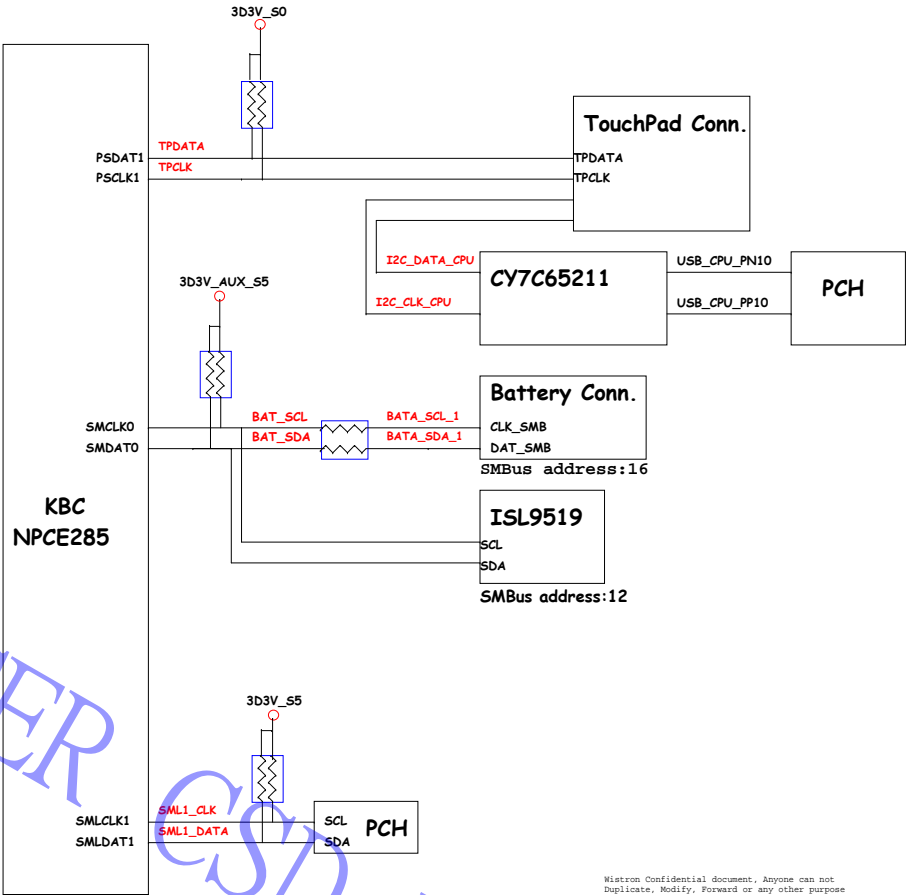
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PCH SMBus Block Diagram



www.laptopblue.com KBC SMBus Block Diagram

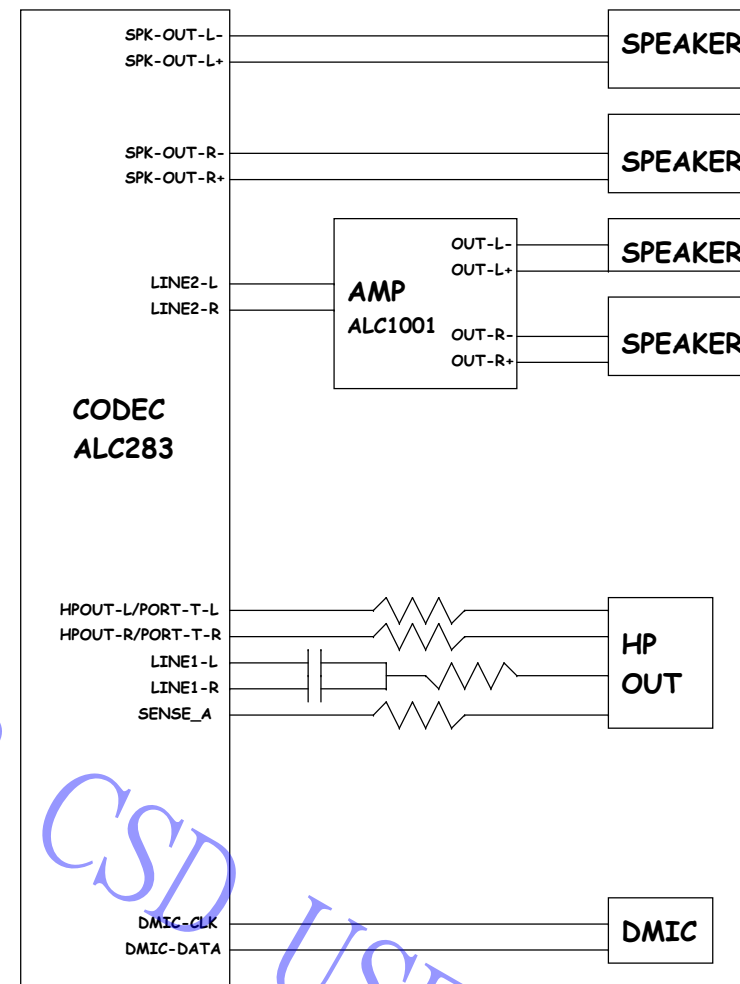


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Audio Block Diagram



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