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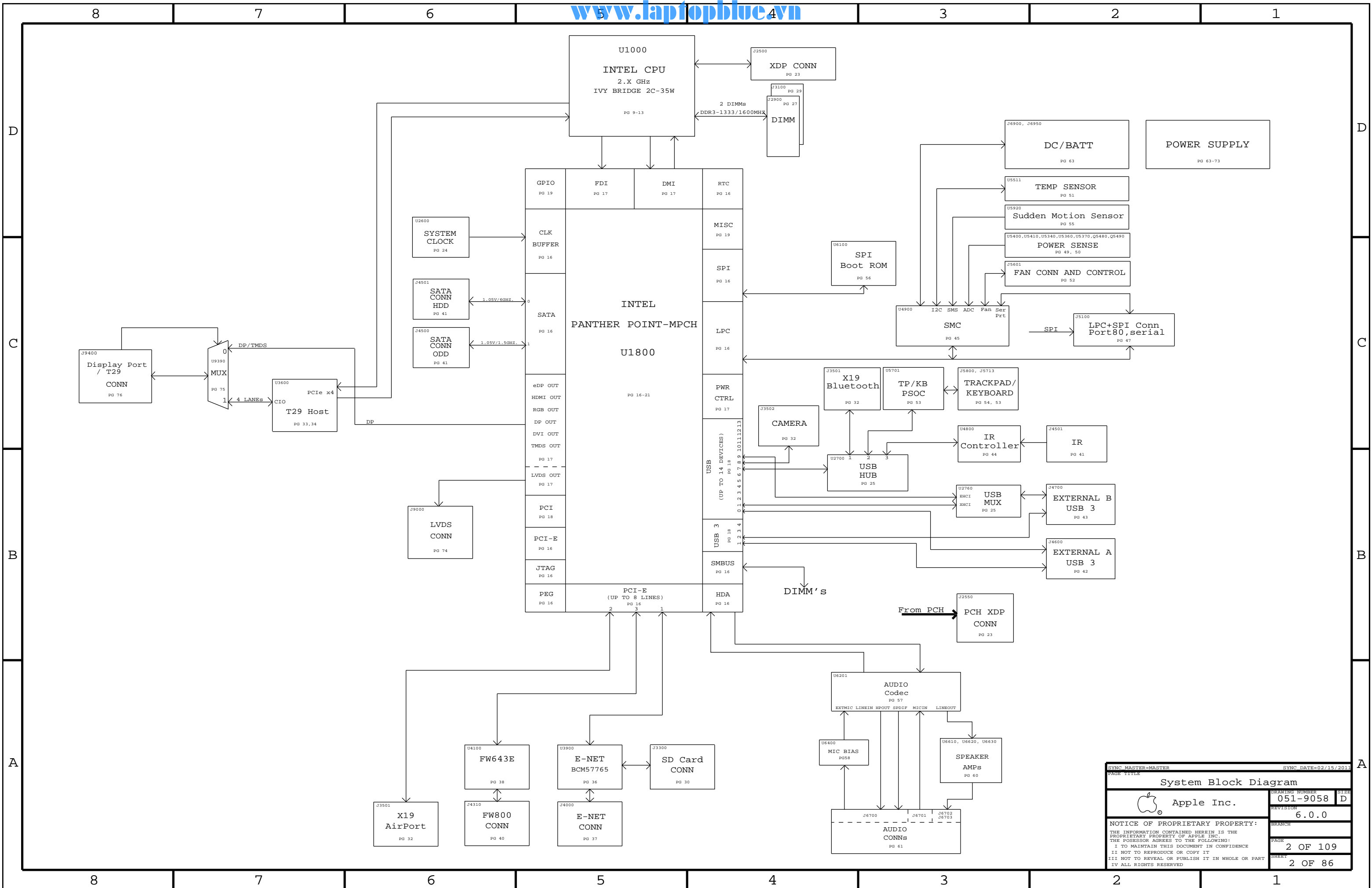
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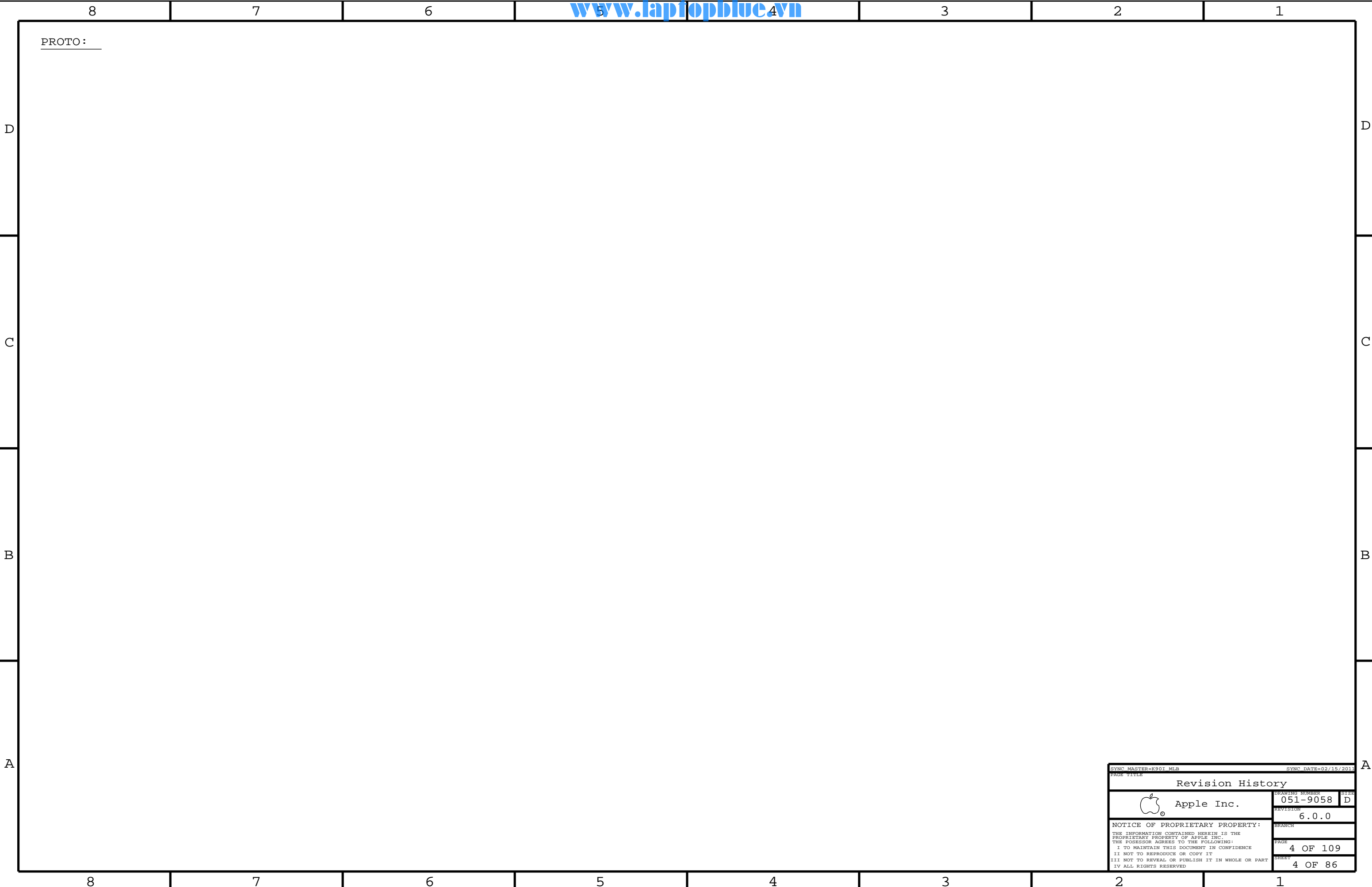
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DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Mar 13 14:00:17 2012

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PROTO:

SYNC MASTER=K901 MLB

SYNC DATE=02/15/2011

Revision History

 Apple Inc.

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DRAWING NUMBER
051-9058

REVISION
6.0.0

BRANCH

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SIZE
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
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SYNC MASTER-K901 MLB		SYNC DATE=02/15/2013	
PAGE TITLE			
BOM Configuration			
	Apple Inc.		DRAWING NUMBER
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Functional Test Points

Fan Connectors

612	TRUE	PP5V_S0	6 7
615	TRUE	FAN_RT_PWM	52
616	TRUE	FAN_RT_TACH	52

(NEED TO ADD 1 GND TP)

MIC_FUNC_TEST

650	TRUE	BI_MIC_LO	61 62
655	TRUE	BI_MIC_HI	61 62
656	TRUE	BI_MIC_SHIELD	61 62

(NEED TO ADD 1 GND TP)

SPEAKER_FUNC_TEST

660	TRUE	SPKRAMP_L_N_OUT	60 61 85
660	TRUE	SPKRAMP_L_P_OUT	60 61 85
660	TRUE	SPKRAMP_R_N_OUT	60 61 85
660	TRUE	SPKRAMP_R_P_OUT	60 61 85
660	TRUE	SPKRAMP_SUB_N_OUT	60 61 85
660	TRUE	SPKRAMP_SUB_P_OUT	60 61 85

X19_CONN

660	TRUE	PP3V3_WLAN	(NEED 3 TP) 6 32 46
660	TRUE	PCIE_AP_D2R_PI_P	32 81
660	TRUE	PCIE_AP_D2R_PI_N	32 81
660	TRUE	PCIE_AP_R2D_P	32 81
660	TRUE	PCIE_AP_R2D_N	32 81
660	TRUE	PCIE_CLK100M_AP_CONN_P	32 85
660	TRUE	PCIE_CLK100M_AP_CONN_N	32 85
660	TRUE	PP3V3_S3RS4_BT_F	32
660	TRUE	PCIE_WAKE_L	17 24 32
660	TRUE	USB_BT_CONN_P	32 80
660	TRUE	USB_BT_CONN_N	32 80
660	TRUE	AP_CLKREQ_Q_L	32
660	TRUE	AP_RESET_CONN_L	32
660	TRUE	AP_TEMP_SMB_SDA_R	32
660	TRUE	AP_TEMP_SMB_SCL_R	32
660	TRUE	WIFI_EVENT_L_R	32

(NEED TO ADD 5 GND TP)

IPD_FLEX_CONN

660	TRUE	PP3V3_S4	6 7
660	TRUE	PP18V5_Z2	6 54
660	TRUE	Z2_CS_L	53 54
660	TRUE	Z2_DEBUG3	53 54
660	TRUE	Z2_M0S1	53 54
660	TRUE	Z2_MISO	53 54
660	TRUE	Z2_SCLK	53 54
660	TRUE	Z2_BOOST_EN	54
660	TRUE	Z2_HOST_INTN	53 54
660	TRUE	Z2_CLKIN	53 54
660	TRUE	Z2_KEY_ACT_L	53 54
660	TRUE	Z2_RESET	53 54
660	TRUE	PSOC_MISO	53 54
660	TRUE	PSOC_MOSI	53 54
660	TRUE	PSOC_SCLK	53 54
660	TRUE	SMBUS_SMC_2_S3_SCL	6 45 48 84
660	TRUE	SMBUS_SMC_2_S3_SDA	6 45 48 84
660	TRUE	PSOC_F_CS_L	53 54
660	TRUE	PICKB_L	53 54
660	TRUE	PP5V_S5_CUMULUS	54

(NEED TO ADD 2 GND TP)

KEYBOARD_CONN

660	TRUE	PP3V3_S4	6 7
660	TRUE	PP3V42_G3H	6 7
660	TRUE	WS_KBD1	53
660	TRUE	WS_KBD2	53
660	TRUE	WS_KBD3	53
660	TRUE	WS_KBD5	53
660	TRUE	WS_KBD6	53
660	TRUE	WS_KBD7	53
660	TRUE	WS_KBD8	53
660	TRUE	WS_KBD9	53
660	TRUE	WS_KBD10	53
660	TRUE	WS_KBD11	53
660	TRUE	WS_KBD12	53
660	TRUE	WS_KBD13	53
660	TRUE	WS_KBD14	53
660	TRUE	WS_KBD15_CAP	53
660	TRUE	WS_KBD16_NUM	53
660	TRUE	WS_KBD17	53
660	TRUE	WS_KBD18	53
660	TRUE	WS_KBD19	53
660	TRUE	WS_KBD20	53
660	TRUE	WS_KBD21	53
660	TRUE	WS_KBD22	53
660	TRUE	WS_KBD23	53
660	TRUE	WS_KBD_ONOFF_L	53
660	TRUE	WS_LEFT_SHIFT_KBD	53
660	TRUE	WS_LEFT_OPTION_KBD	53
660	TRUE	WS_CONTROL_KBD	53

(NEED TO ADD 2 GND TP)

BATT_POWER_CONN

660	TRUE	SMBUS_SMC_5_G3_SCL	6 45 48 84
660	TRUE	SMBUS_SMC_5_G3_SDA	6 45 48 84
660	TRUE	SYS_DETECT_L	63
660	TRUE	PPVBAT_G3H_CONN	(NEED 5 TP) 63 64

(NEED TO ADD 5 GND TP)

BIL_CONN

660	TRUE	PP3V42_G3H	6 7
660	TRUE	SMBUS_SMC_5_G3_SCL	6 45 48 84
660	TRUE	SMBUS_SMC_5_G3_SDA	6 45 48 84
660	TRUE	SMC_BIL_BUTTON_L	45 46 63
660	TRUE	SMC_LID_R	63

(NEED TO ADD 2 GND TP)

CAMERA/ALS_CONN

660	TRUE	PP5V_S3_ALSCAMERA_F	32
660	TRUE	SMBUS_SMC_2_S3_SCL	6 45 48 84
660	TRUE	SMBUS_SMC_2_S3_SDA	6 45 48 84
660	TRUE	USB_CAMERA_CONN_P	32 80
660	TRUE	USB_CAMERA_CONN_N	32 80

(NEED TO ADD 2 GND TP)

DEBUG_VOLTAGE

660	TRUE	PPVCORE_S0_CPU	7
660	TRUE	PPVCORE_S0_AXG	7
660	TRUE	PP1V2_S3_ENET_INTREG	71
660	TRUE	PP1V05_S0	7
660	TRUE	PP1V5_S3RS0	7 85
660	TRUE	PP1V8_S0	7
660	TRUE	PP3V3_S0	7 85
660	TRUE	PP5V_S0	6 7
660	TRUE	PP3V3_S3	7
660	TRUE	PP5V_S3	7
660	TRUE	PPVCCSA_S0_CPU	7
660	TRUE	PP3V3_S5	7 85
660	TRUE	PP3V42_G3H	6 7
660	TRUE	PPBUS_G3H	7
660	TRUE	PP3V3_ENET	7
660	TRUE	PP3V3_WLAN	6 32 46
660	TRUE	PP5V_SW_ODD	6 41
660	TRUE	PP5V_S0_HDD_FLT	6 41
660	TRUE	PP18V5_Z2	6 54
660	TRUE	PP3V3_S0_LCD_F	6 74
660	TRUE	PP3V3_LCDVDD_SW_F	6 74
660	TRUE	PP4V5_AUDIO_ANALOG	57 62
660	TRUE	PP1V5_S3	7
660	TRUE	SMC_PM_G2_EN	45 73
660	TRUE	PM_SLP_S4_L	17 26 32 45 73
660	TRUE	PM_SLP_S3_L	8 17 26 45 73

(NEED TO ADD 6 GND TP)

DC_POWER_CONN

660	TRUE	PP18V5_DCIN_FUSE	63
660	TRUE	ADAPTER_SENSE	63

(NEED TO ADD 4 GND TP)

LPC+SPI_DEBUG_CONN

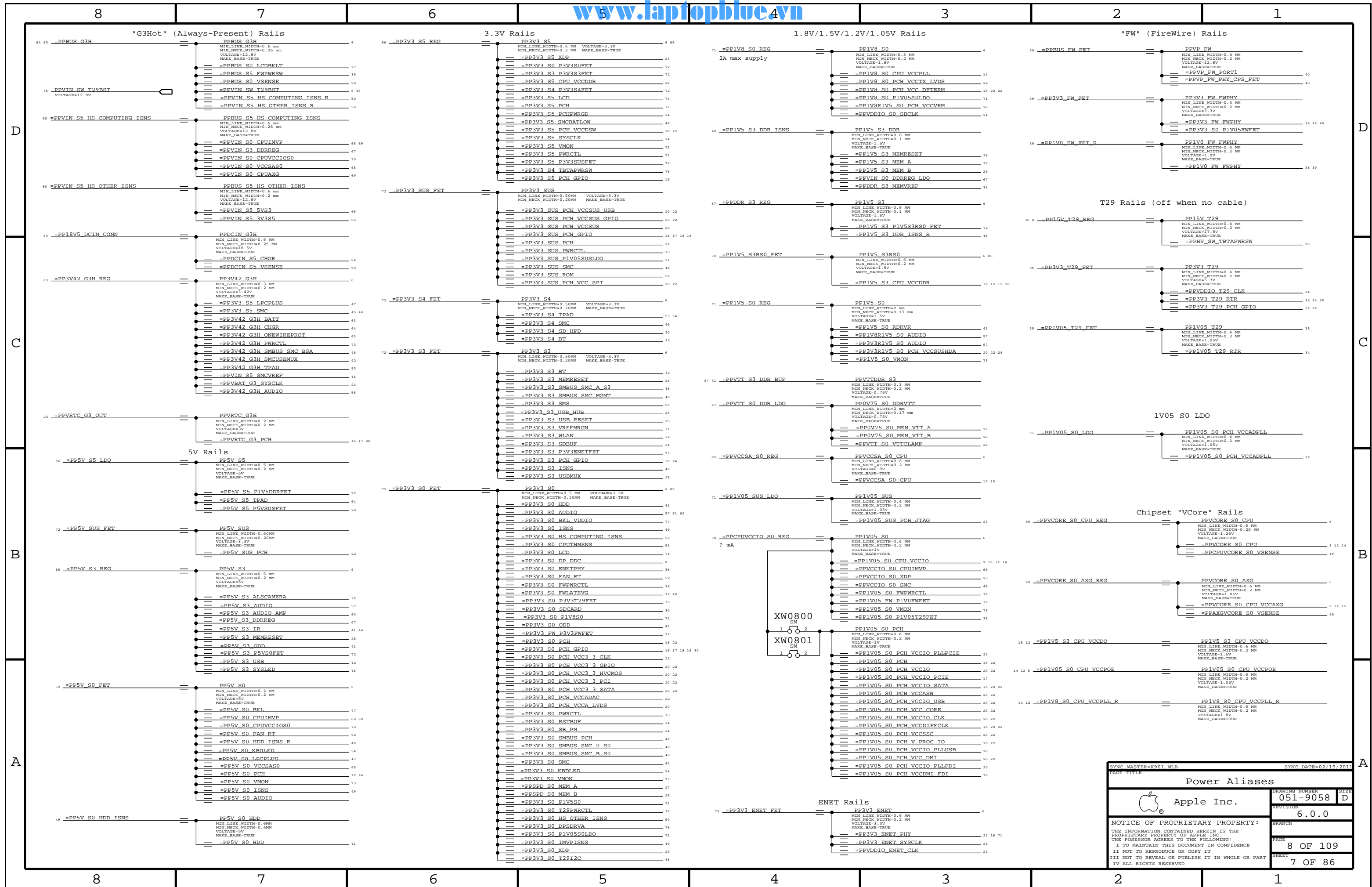
660	TRUE	LEC_AD<0>	16 45 47 81
660	TRUE	LPC_AD<1>	16 45 47 81
660	TRUE	LPC_AD<2>	16 45 47 81
660	TRUE	LPC_AD<3>	16 45 47 81
660	TRUE	LPC_CLK33M_LPCPLUS	24 47 81
660	TRUE	LPC_FRAME_L	16 45 47 81
660	TRUE	LPC_PWRDWN_L	17 45 47
660	TRUE	LPC_SERIRO	16 45 47
660	TRUE	LPCPLUS_GPIO	19 47
660	TRUE	LPCPLUS_RESET_L	24 47
660	TRUE	PM_CLKRUN_L	17 45 47
660	TRUE	PP3V42_G3H	6 7
660	TRUE	PP5V_S0	6 7
660	TRUE	SMC_RX_L	45 46 47
660	TRUE	SMC_TCK	45 46 47
660	TRUE	SMC_TDI	45 46 47
660	TRUE	SMC_TDO	45 46 47
660	TRUE	SMC_TMS	45 46 47
660	TRUE	SMC_TX_L	45 46 47
660	TRUE	SPI_ALT_CLK	47
660	TRUE	SPI_ALT_CS_L	47
660	TRUE	SPI_ALT_MISO	47
660	TRUE	SPI_ALT_MOSI	47
660	TRUE	SPIROM_USE_MLB	19 47 56

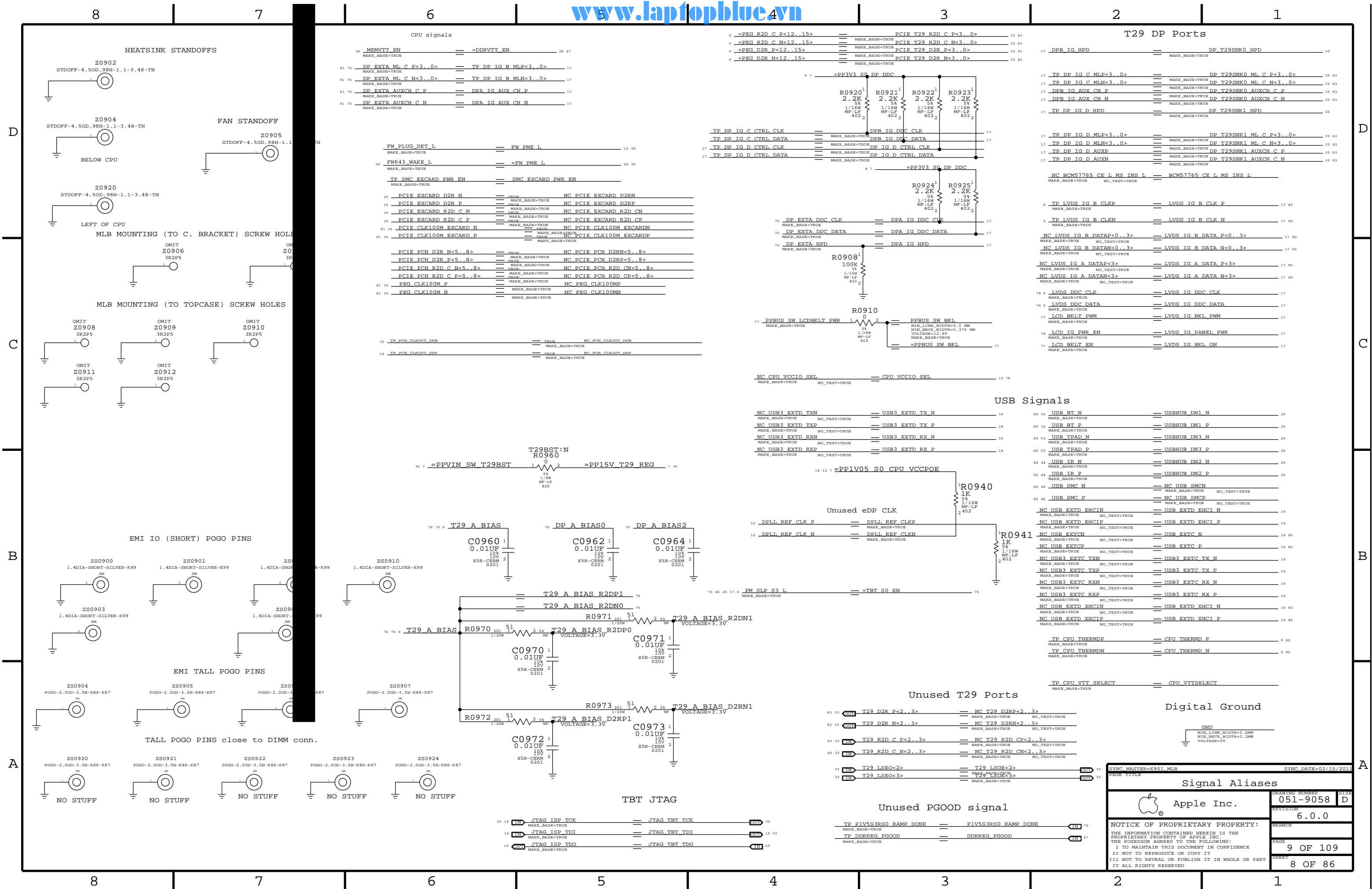
(NEED TO ADD 2 GND TP)

NC_NO_TESTS

NO_TEST				
17	TP CRT IG BLUE	==	TRUE	NC CRT IG BLUE
17	TP CRT IG GREEN	==	MAKE_BASE=TRUE	NC CRT IG GREEN
17	TP CRT IG RED	==	MAKE_BASE=TRUE	NC CRT IG RED
17	TP CRT IG DDC CLK	==	TRUE	NC CRT IG DDC CLK
17	TP CRT IG DDC DATA	==	MAKE_BASE=TRUE	NC CRT IG DDC DATA
17	TP CRT IG HSYNC	==	TRUE	NC CRT IG HSYNC
17	TP CRT IG VSYNC	==	MAKE_BASE=TRUE	NC CRT IG VSYNC
17	TP LVDS IG CTRL CLK	==	TRUE	NC LVDS IG CTRL CLK
17	TP LVDS IG CTRL DATA	==	MAKE_BASE=TRUE	NC LVDS IG CTRL DATA
17	TP PCH LVDS VBG	==	MAKE_BASE=TRUE	NC PCH LVDS VBG
16	TP HDA SDIN1	==	TRUE	NC HDA SDIN1
16	TP HDA SDIN2	==	MAKE_BASE=TRUE	NC HDA SDIN2
16	TP HDA SDIN3	==	MAKE_BASE=TRUE	NC HDA SDIN3
18	TP PCI PME L	==	TRUE	NC PCI PME L
18	TP PCI CLK33M OUT3	==	MAKE_BASE=TRUE	NC PCI CLK33M OUT3
16	TP CLINK CLK	==	TRUE	NC CLINK CLK
16	TP CLINK DATA	==	MAKE_BASE=TRUE	NC CLINK DATA
16	TP CLINK RESET L	==	MAKE_BASE=TRUE	NC CLINK RESET L
16	TP PCIE CLK100M PEBN	==	TRUE	NC PCIE CLK100M PEBN
16	TP PCIE CLK100M PEBP	==	MAKE_BASE=TRUE	NC PCIE CLK100M PEBP
38	TP FW643 SDA	==	TRUE	NC FW643 SDA
38	TP FW643 SM	==	MAKE_BASE=TRUE	NC FW643 SM
38	TP FW643 TCK	==	TRUE	NC FW643 TCK
38	TP FW643 TMS	==	MAKE_BASE=TRUE	NC FW643 TMS
38	TP FW643 FW620 L	==	TRUE	NC FW643 FW620 L
38	TP FW643 VBUE	==	MAKE_BASE=TRUE	NC FW643 VBUE
38	TP FW643 OCR10 CTL	==	MAKE_BASE=TRUE	NC FW643 OCR10 CTL
38	TP FW643 AVREG	==	TRUE	NC FW643 AVREG
38	TP FW643 TDI	==	MAKE_BASE=TRUE	NC FW643 TDI
23	TP XDP PCH OBSFN A<0..1>	==	TRUE	NC TP XDP PCH OBSFN A<0..1>
23	TP XDP PCH OBSFN B<0..1>	==	MAKE_BASE=TRUE	NC TP XDP PCH OBSFN B<0..1>
23	TP XDPPCH HOOK2	==	TRUE	NC TP XDPPCH HOOK2
23	TP XDPPCH HOOK3	==	MAKE_BASE=TRUE	NC TP XDPPCH HOOK3
23	TP XDP PCH OBSFN D<0..1>	==	TRUE	NC TP XDP PCH OBSFN D<0..1>
23	TP XDP PCH HOOK4	==	MAKE_BASE=TRUE	NC TP XDP PCH HOOK4
23	TP XDP PCH HOOK5	==	TRUE	NC TP XDP PCH HOOK5
16	TP PCH GPIO64 CLKOUTFLEX0	==	TRUE	NC PCH GPIO64 CLKOUTFLEX0
16	TP PCH GPIO65 CLKOUTFLEX1	==	MAKE_BASE=TRUE	NC PCH GPIO65 CLKOUTFLEX1
16	TP PCH GPIO66 CLKOUTFLEX2	==	TRUE	NC PCH GPIO66 CLKOUTFLEX2
16	TP PCH GPIO67 CLKOUTFLEX3	==	MAKE_BASE=TRUE	NC PCH GPIO67 CLKOUTFLEX3
660	TRUE	NC FW2 TPBP	40	
660	TRUE	NC FW2 TPBN	40	
660	TRUE	NC FW2 TPBIAS	40	
660	TRUE	NC FW2 TPAP	40	
660	TRUE	NC FW2 TPAN	40	
660	TRUE	NC FW0 TPBP	40	
660	TRUE	NC FW0 TPBN	40	
660	TRUE	NC FW0 TPAP	40	
660	TRUE	XDP PCH AP PWR EN		
660	TRUE	XDP PCH USB HUB SOFT RST L		
660	TRUE	XDP PCH SDCONN STATE RST L		
660	TRUE	XDP PCH ENET PWR EN		
660	TRUE	XDP PCH SDCONN DET L		
660	TRUE	XDP PCH S5 PWRGD	23	
660	TRUE	XDP PCH PWRBTN L	23	
660	TRUE	XDP PCH ISOLATE CPU MEM L		
660	TRUE	XDP FW CLKREQ L		
660	TRUE	XDP AP CLKREQ L		
660	TRUE	XDP PCH AUD IPHS SWITCH EN		
17	TP SDVO TVCLKINN	==	TRUE	NC SDVO TVCLKINN
17	TP SDVO TVCLKINP	==	MAKE_BASE=TRUE	NC SDVO TVCLKINP
17	TP SDVO STALLN	==	TRUE	NC SDVO STALLN
17	TP SDVO STALLP	==	MAKE_BASE=TRUE	NC SDVO STALLP
17	TP SDVO INTN	==	TRUE	NC SDVO INTN
17	TP SDVO INTP	==	MAKE_BASE=TRUE	NC SDVO INTP

NC_EDP_TXP<0..3>	==	TRUE	TP_EDP_TX_P<0..3>				
MAKE_BASE=TRUE							
NC_EDP_TXN<0..3>	==	TRUE	TP_EDP_TX_N<0..3>				
MAKE_BASE=TRUE							
NC_EDP_AUXP	==	TRUE	TP_EDP_AUX_P				
MAKE_BASE=TRUE							
NC_EDP_AUXN	==	TRUE	TP_EDP_AUX_N				
MAKE_BASE=TRUE							
NC_CPU_THERMDA	==	TRUE	TP_CPU_THERMDA				
MAKE_BASE=TRUE							
NC_CPU_THERMDC	==	TRUE	TP_CPU_THERMDC				
MAKE_BASE=TRUE							
NC_CPU_RSVD<30..45>	==	TRUE	TP_CPU_RSVD<30..45>				
MAKE_BASE=TRUE							
NC_CPU_RSVD<8..27>	==	TRUE	TP_CPU_RSVD<8..27>				
MAKE_BASE=TRUE							
PEG_R2D_CP<0..7>	==	TRUE	=PEG_R2D_C_P<0..7>				
E_BASE=TRUE							
PEG_R2D_CN<0..7>	==	TRUE	=PEG_R2D_C_N<0..7>				
E_BASE=TRUE							
NC_PEG_D2RP<0..7>	==	TRUE	=PEG_D2R_P<0..7>				
MAKE_BASE=TRUE							
NC_PEG_D2RN<0..7>	==	TRUE	=PEG_D2R_N<0..7>				
MAKE_BASE=TRUE							
PEG_R2D_CP<8..11>	==	TRUE	=PEG_R2D_C_P<8..11>				
E_BASE=TRUE							
PEG_R2D_CN<8..11>	==	TRUE	=PEG_R2D_C_N<8..11>				
E_BASE=TRUE							
NC_PEG_D2RP<8..11>	==	TRUE	=PEG_D2R_P<8..11>				
MAKE_BASE=TRUE							
NC_PEG_D2RN<8..11>	==	TRUE	=PEG_D2R_N<8..11>				
MAKE_BASE=TRUE							
TP_PCIE_CLK100M_PEA4N	==	TRUE	NC_PCIE_CLK100M_PEA4N				
TP_PCIE_CLK100M_PEA4P	==	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEA4P				
TP_PCIE_CLK100M_PEA5N	==	TRUE	NC_PCIE_CLK100M_PEA5N				
TP_PCIE_CLK100M_PEA5P	==	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEA5P				
TP_PCIE_CLK100M_PEB6N	==	TRUE	NC_PCIE_CLK100M_PEB6N				
TP_PCIE_CLK100M_PEB6P	==	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEB6P				
TP_PCIE_CLK100M_PEB7N	==	TRUE	NC_PCIE_CLK100M_PEB7N				
TP_PCIE_CLK100M_PEB7P	==	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEB7P				
TP_PSOC_P1_3	==	TRUE	NC_PSOC_P1_3				
TP_SATA_C_D2RN	==	TRUE	NC_SATA_C_D2RN				
TP_SATA_C_D2RP	==	MAKE_BASE=TRUE	NC_SATA_C_D2RP				
TP_SATA_C_R2D_CN	==	TRUE	NC_SATA_C_R2D_CN				
TP_SATA_C_R2D_CP	==	MAKE_BASE=TRUE	NC_SATA_C_R2D_CP				
TP_SATA_D_D2RN	==	TRUE	NC_SATA_D_D2RN				
TP_SATA_D_D2RP	==	MAKE_BASE=TRUE	NC_SATA_D_D2RP				
TP_SATA_D_R2D_CN	==	TRUE	NC_SATA_D_R2D_CN				
TP_SATA_D_R2D_CP	==	MAKE_BASE=TRUE	NC_SATA_D_R2D_CP				
TP_SATA_E_D2RN	==	TRUE	NC_SATA_E_D2RN				
TP_SATA_E_D2RP	==	MAKE_BASE=TRUE	NC_SATA_E_D2RP				
TP_SATA_E_R2D_CN	==	TRUE	NC_SATA_E_R2D_CN				
TP_SATA_E_R2D_CP	==	MAKE_BASE=TRUE	NC_SATA_E_R2D_CP				
TP_SATA_F_D2RN	==	TRUE	NC_SATA_F_D2RN				
TP_SATA_F_D2RP	==	MAKE_BASE=TRUE	NC_SATA_F_D2RP				
TP_SATA_F_R2D_CN	==	TRUE	NC_SATA_F_R2D_CN				
TP_SATA_F_R2D_CP	==	MAKE_BASE=TRUE	NC_SATA_F_R2D_CP				
33	TP_TBT_MONDC0	==	TRUE	NC_TBT_MONDC0			
33	TP_TBT_MONDC1	==	TRUE	NC_TBT_MONDC1			
33	TP_TBT_MONOBSP	==	TRUE	NC_TBT_MONOBSP			
33	TP_TBT_MONOBSN	==	TRUE	NC_TBT_MONOBSN			
33	TP_DP_T29SRC_ML_CP<0..3>	==	TRUE	NC_DP_T29SRC_ML_CP<0..3>			
33	TP_DP_T29SRC_ML_CN<0..3>	==	TRUE	NC_DP_T29SRC_ML_CN<0..3>			
33	TP_DP_T29SRC_AUXCH_CP	==	TRUE	NC_DP_T29SRC_AUXCH_CP			
33	TP_DP_T29SRC_AUXCH_CN	==	TRUE	NC_DP_T29SRC_AUXCH_CN			
33	TP_T29_PCIE_RESET0_L	==	TRUE	TP_T29_PCIE_RESET0_L			
33	TP_T29_PCIE_RESET1_L	==	TRUE	TP_T29_PCIE_RESET1_L			
33	TP_T29_PCIE_RESET2_L	==	TRUE	TP_T29_PCIE_RESET2_L			
33	TP_T29_PCIE_RESET3_L	==	TRUE	TP_T29_PCIE_RESET3_L			
660	TRUE	PCH_VSS_NCTF<1>	81	660	TRUE	PCH_VSS_NCTF<15>	81
660	TRUE	PCH_VSS_NCTF<2>	81	660	TRUE	PCH_VSS_NCTF<17>	81
660	TRUE	PCH_VSS_NCTF<5>	81	660	TRUE	PCH_VSS_NCTF<19>	81
660	TRUE	PCH_VSS_NCTF<9>	81	660	TRUE	PCH_VSS_NCTF<19>	81
660	TRUE	PCH_VSS_NCTF<9>	81	660	TRUE	PCH_VSS_NCTF<21>	81
660	TRUE	PCH_VSS_NCTF<11>	81	660	TRUE	PCH_VSS_NCTF<25>	81
660	TRUE	PCH_VSS_NCTF<12>	81	660	TRUE	PCH_VSS_NCTF<27>	81
660	TRUE	PCH_VSS_NCTF<12>	81	660	TRUE	PCH_VSS_NCTF<29>	81
8	TP_LVDS_IG_B_CLKN	==	TRUE	NC_LVDS_IG_B_CLKN			
8	TP_LVDS_IG_B_CLKP	==	MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP			
	TP_LVDS_IG_BKL_PWM	==	MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM			
			MAKE_BASE=TRUE				
	SMC_BS_ALRT_L	==	TRUE	NC_SMC_BS_ALRT_L			

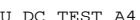
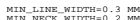




MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM



NOTE: Intel does not recommend to use



NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if Internal Graphics is disabled since they are shared with other interfaces.

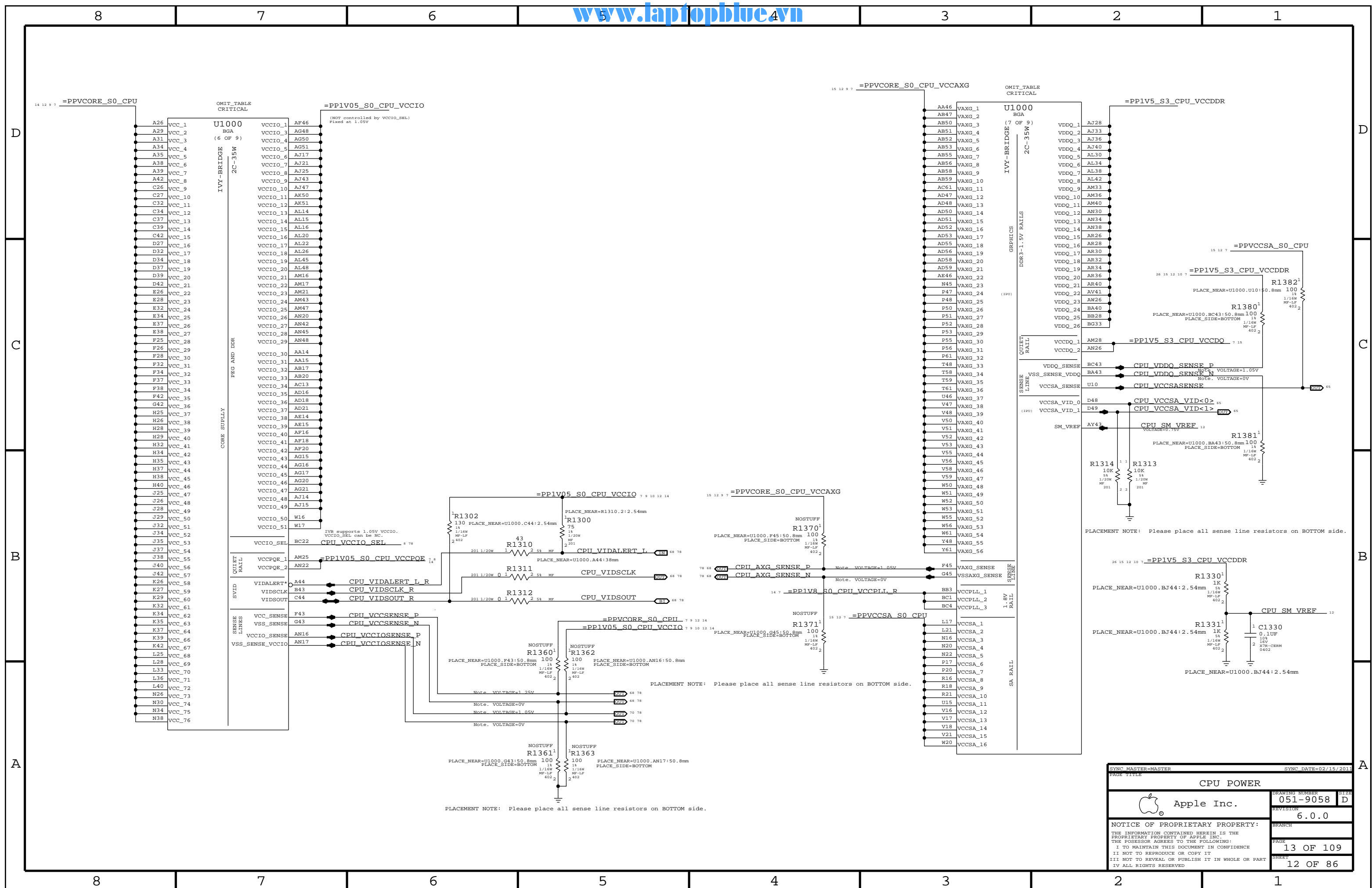
If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

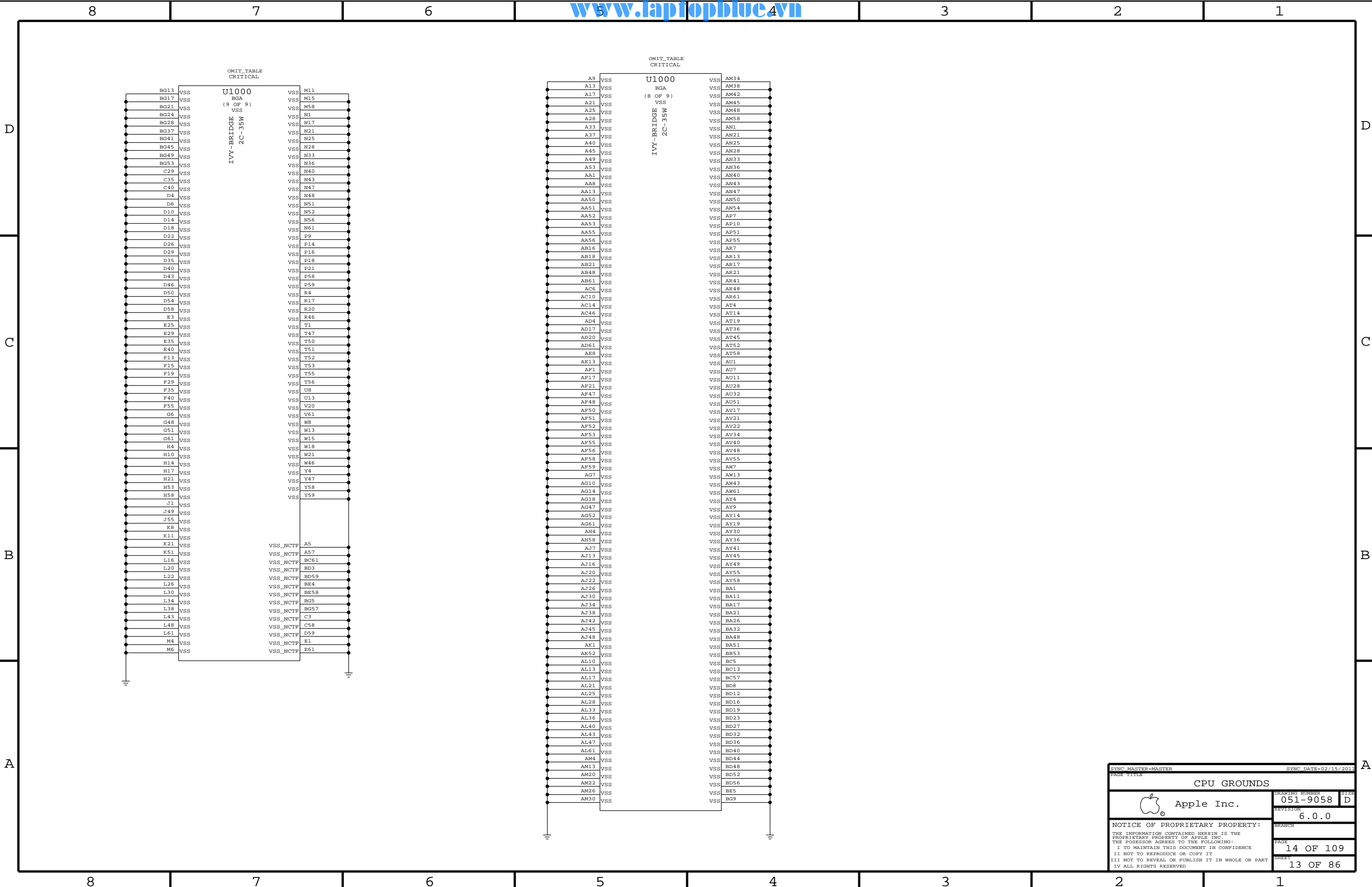
If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.



CFG [7] :PRG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETS	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT)	10 = 2 X8 01 = RSVD 00 = X8, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED







CPU VCCPLL Low pass filter

C1655,C1660,C1661,C1664,C1666,C1667,C1670,C1677,C1678,C1679,C1657,C1672,C1658,C1669,C1668,C1656

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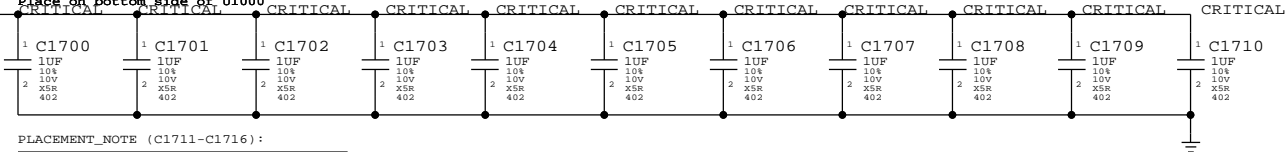
VAXG DECOUPLING

Intel recommendation (section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

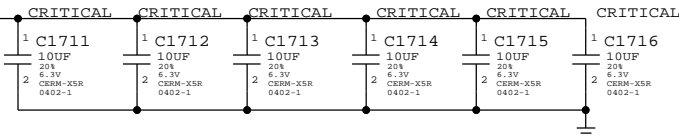
12 9 7 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

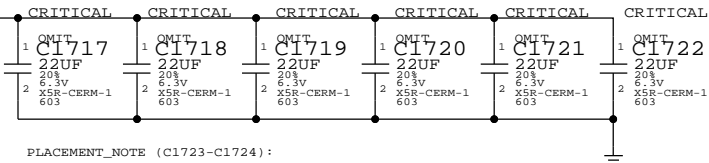
Place on bottom side of U1000



PLACEMENT_NOTE (C1711-C1716):

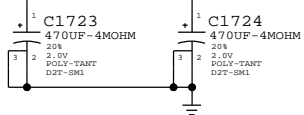


PLACEMENT_NOTE (C1717-C1722):



PLACEMENT_NOTE (C1723-C1724):

Place near inductors on bottom side.



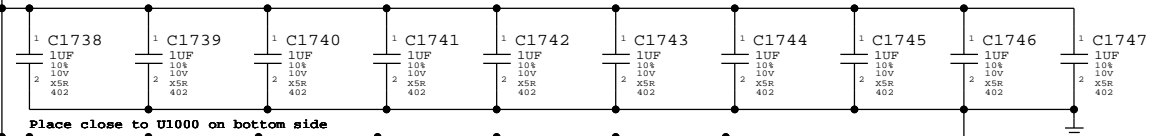
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	6	CAP, CER, XSR, 22uF, 20%, 6.3V, 0603, SAMSUNG	C1717, C1718, C1719, C1720, C1721, C1722	CRITICAL	

CPU VDDQ/VCCDQ DECOUPLING

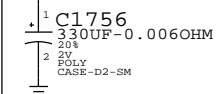
Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

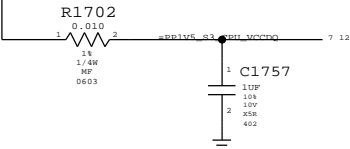
Place on bottom side of U1000



Place close to U1000 on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



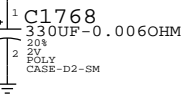
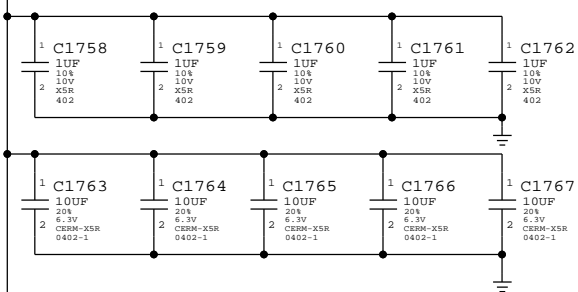
CPU VCCSA DECOUPLING


Intel recommendation (Section 6.6): 6x 1uF, 5x 10uF, 1x 330uF

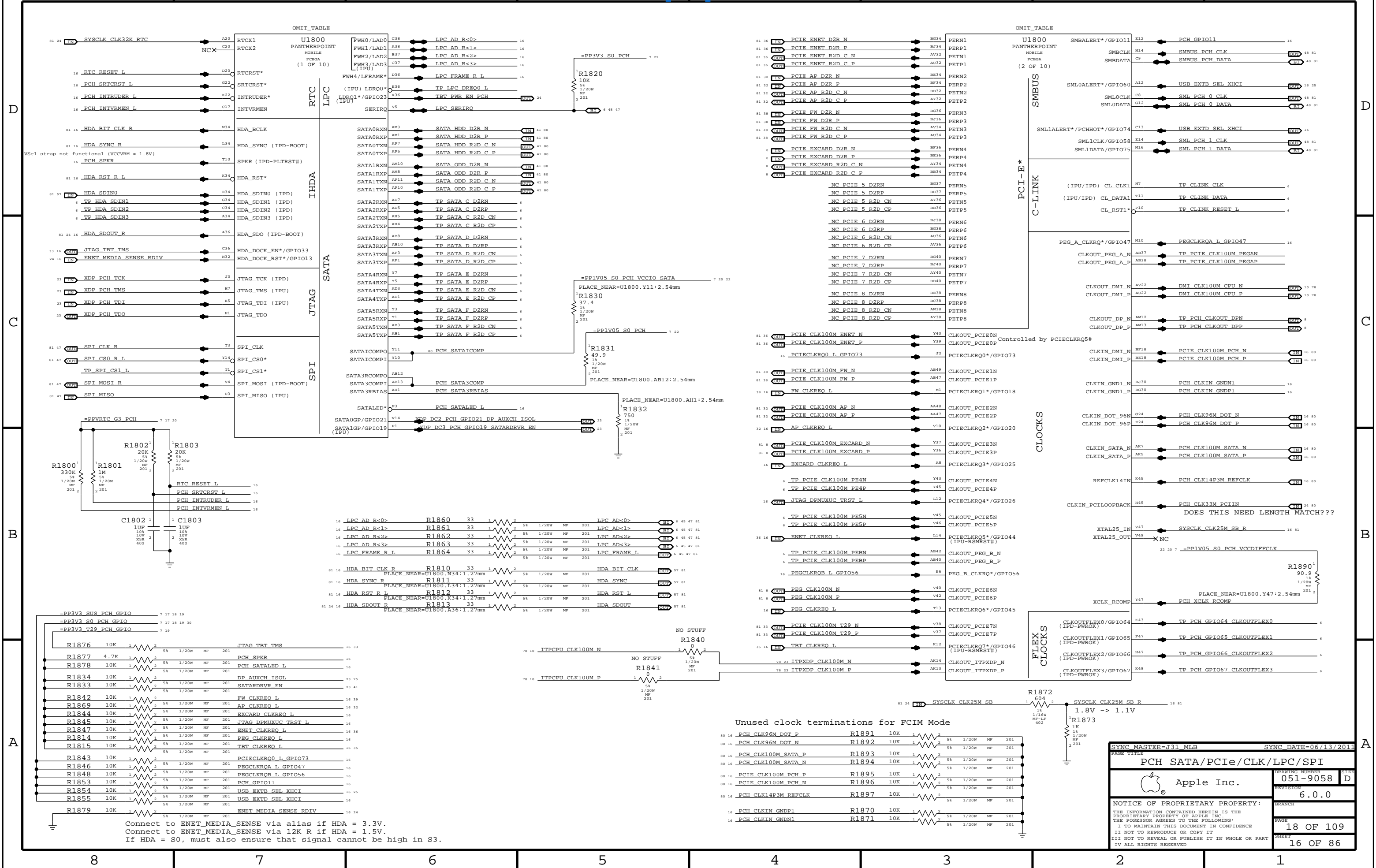
PLACEMENT_NOTE (C1758-C1767):

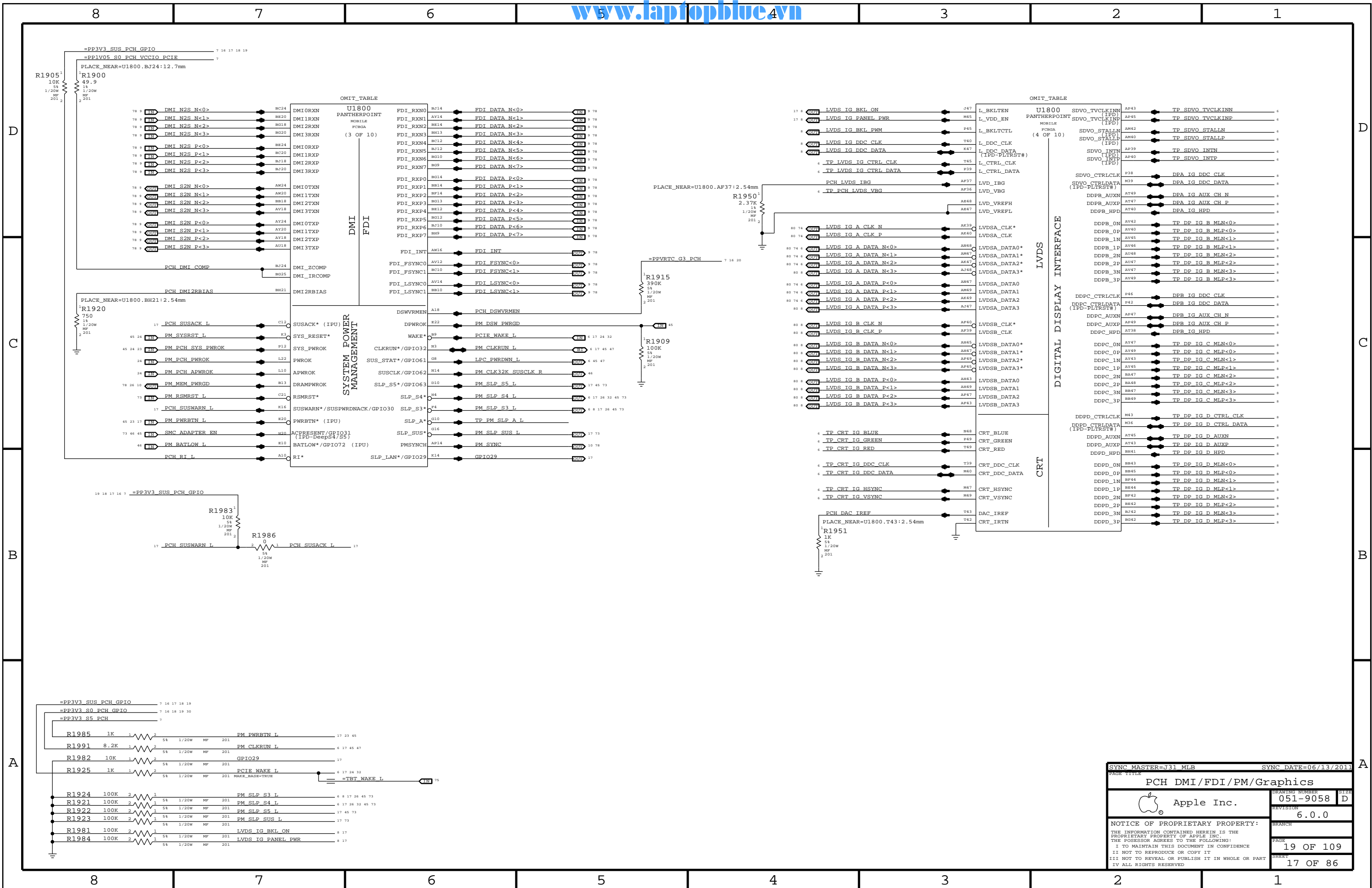
12 7 =PPVCCSA_S0_CPU

Place on bottom side of U1000



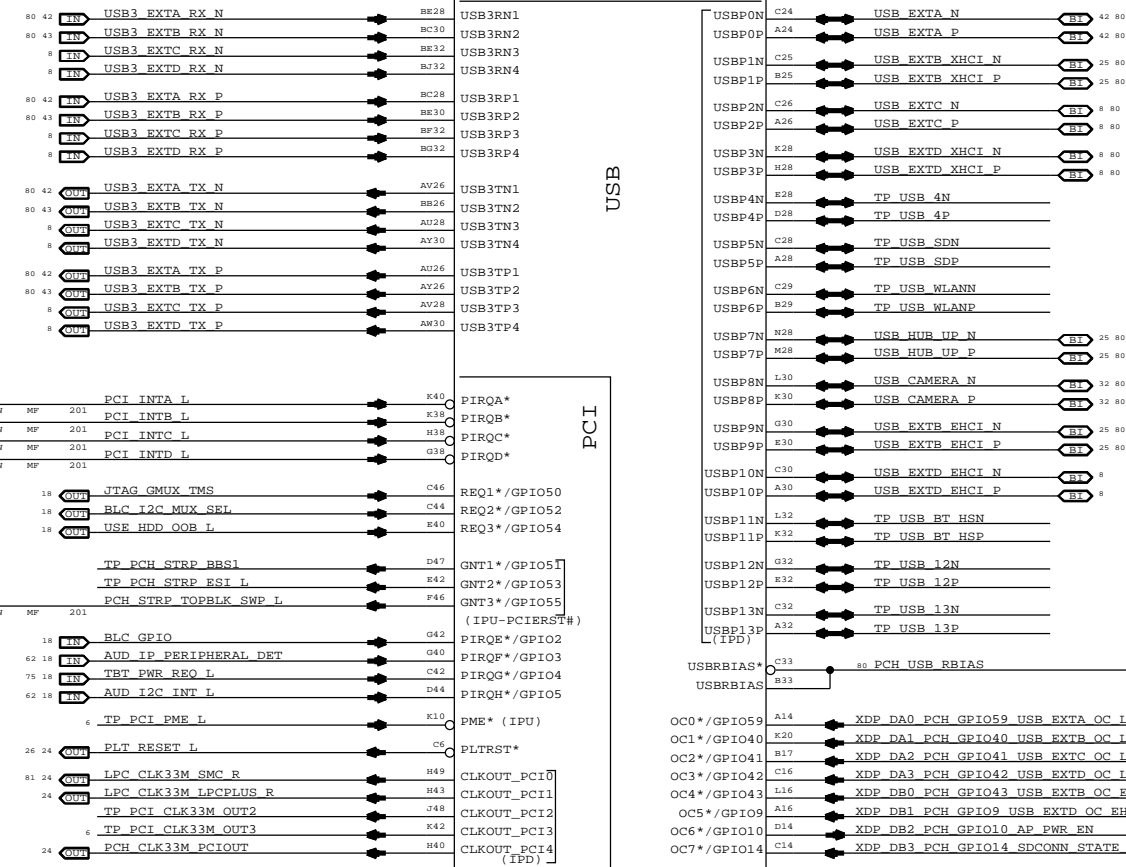
SYNC MASTER=MASTER		SYNC DATE=02/15/2013	
PAGE TITLE			
CPU DECOUPLING-II			
 Apple Inc.	DRAWING NUMBER	051-9058	SIZE D
	REVISION	6.0.0	
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OMIT_TABLE			
		U1800	
NCX	BQ226	PANTHERPOINT	RSVD1 AY7
NCX	SJ226		RSVD2 AY7
NCX	BM225	MOBILE	RSVD3 AT3
NCX	BQ16	FCBGA	RSVD3 AT3
NCX	BQ16	(5 OF 10)	RSVD4 BM4
NCX	BM16		RSVD5 AT8
NCX	AM38		RSVD6 BC10
NCX	AM37		
NCX	AK43	TP8	RSVD7 AU2
NCX	AK45	TP9	RSVD8 AT4
NCX	C18	TP10	RSVD9 AT3
NCX	N30	TP11	RSVD10 AT1
NCX	H3	TP12	RSVD11 AY3
NCX	AM12	TP13	RSVD12 AT5
NCX	AM4	TP14	RSVD13 AY3
NCX	AM5	TP15	RSVD14 AV1
NCX	Y13	TP16	RSVD15 BM1
NCX	K24	TP17	RSVD16 BM3
NCX	L24	TP18	RSVD17 BM5
NCX	AB46	TP19	RSVD18 BM3
NCX	AB45	TP20	RSVD19 BM7
			RSVD20 BE8
NCX	B21	TP21	RSVD21 BD4
NCX	M20	TP22	RSVD22 BF6
	AY16	TP23	
		TP24	RSVD23 AV5
NCX	BM46		RSVD24 AV10
			RSVD25 AT8
			RSVD26 AY5
			RSVD27 BA2
			RSVD28 AT12
			RSVD29 BF3



```
Ext A (XHCI/EHCI)

Ext B (XHCI)

Ext C (XHCI/EHCI)

Ext D (XHCI) (Mobiles: Trackpad?)

Unused

RSVD: SD

RSVD: WiFi

USB Hub (All LS/FS Devices)

Camera

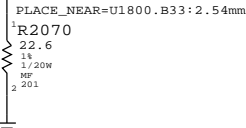
Ext B (EHCI)


Ext D (EHCI)

RSVD: BT (HS)

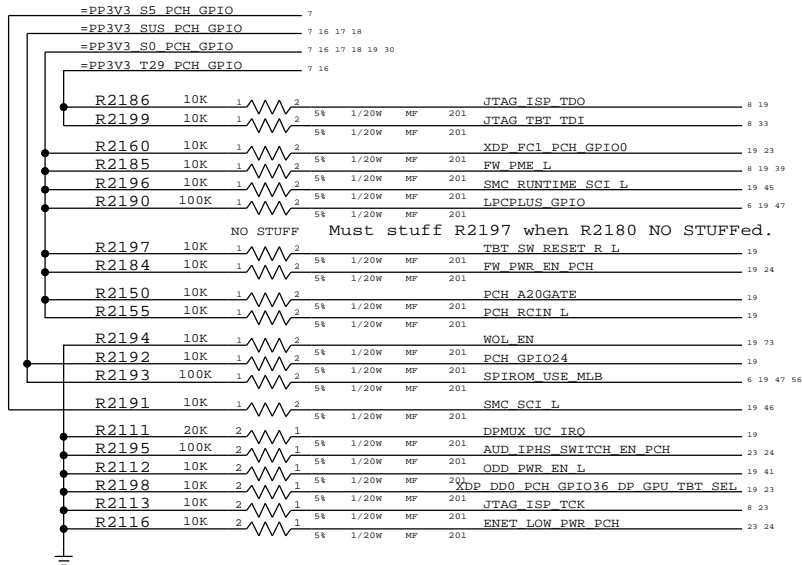
Unused


Unused
```

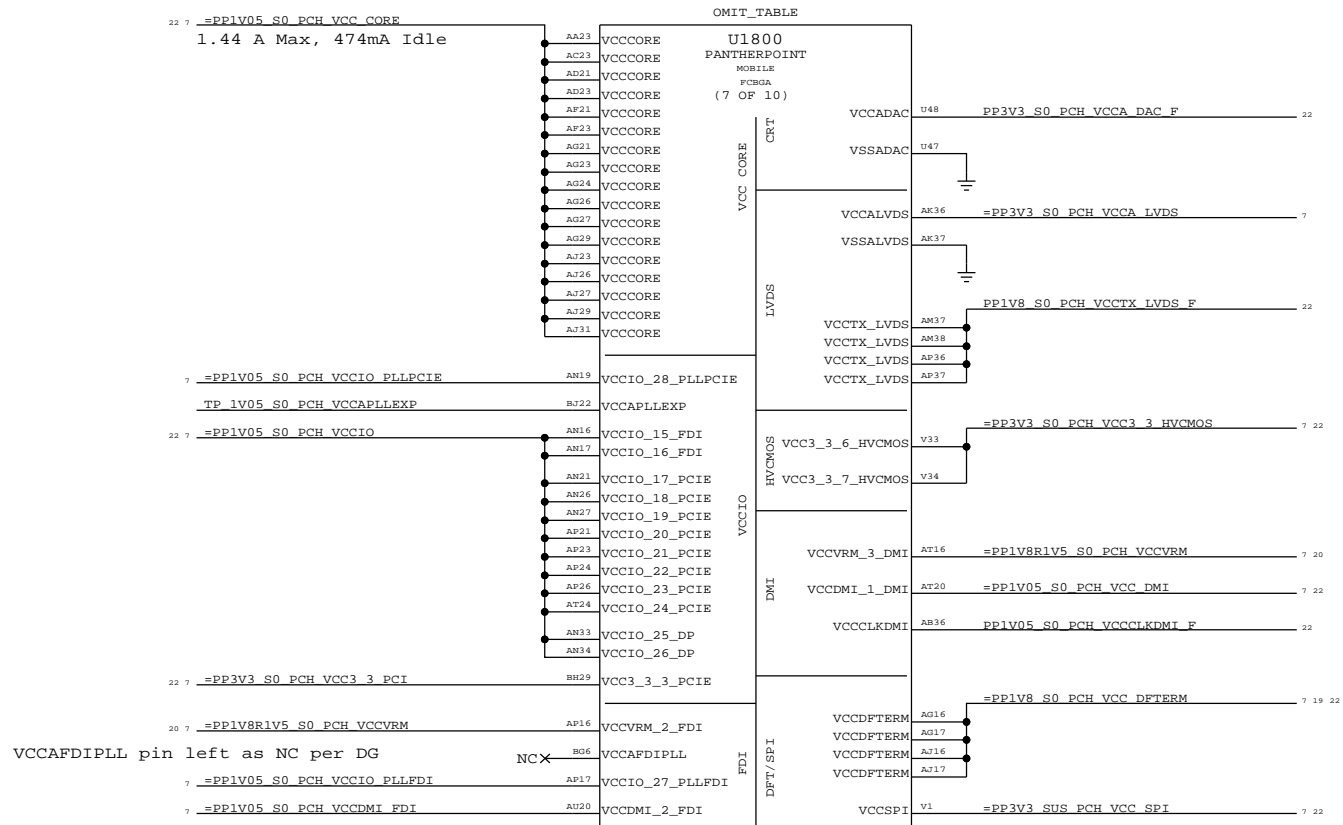
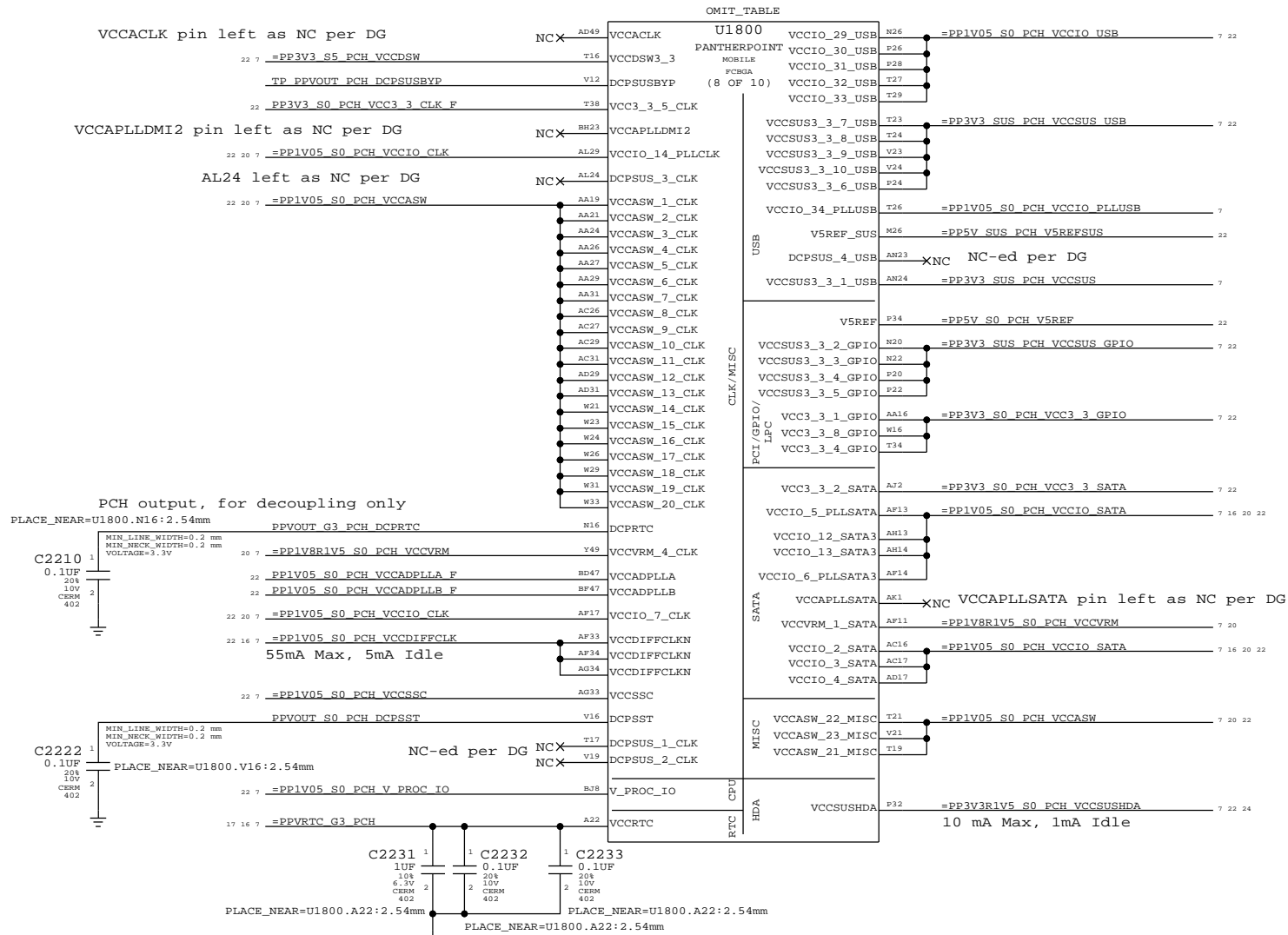


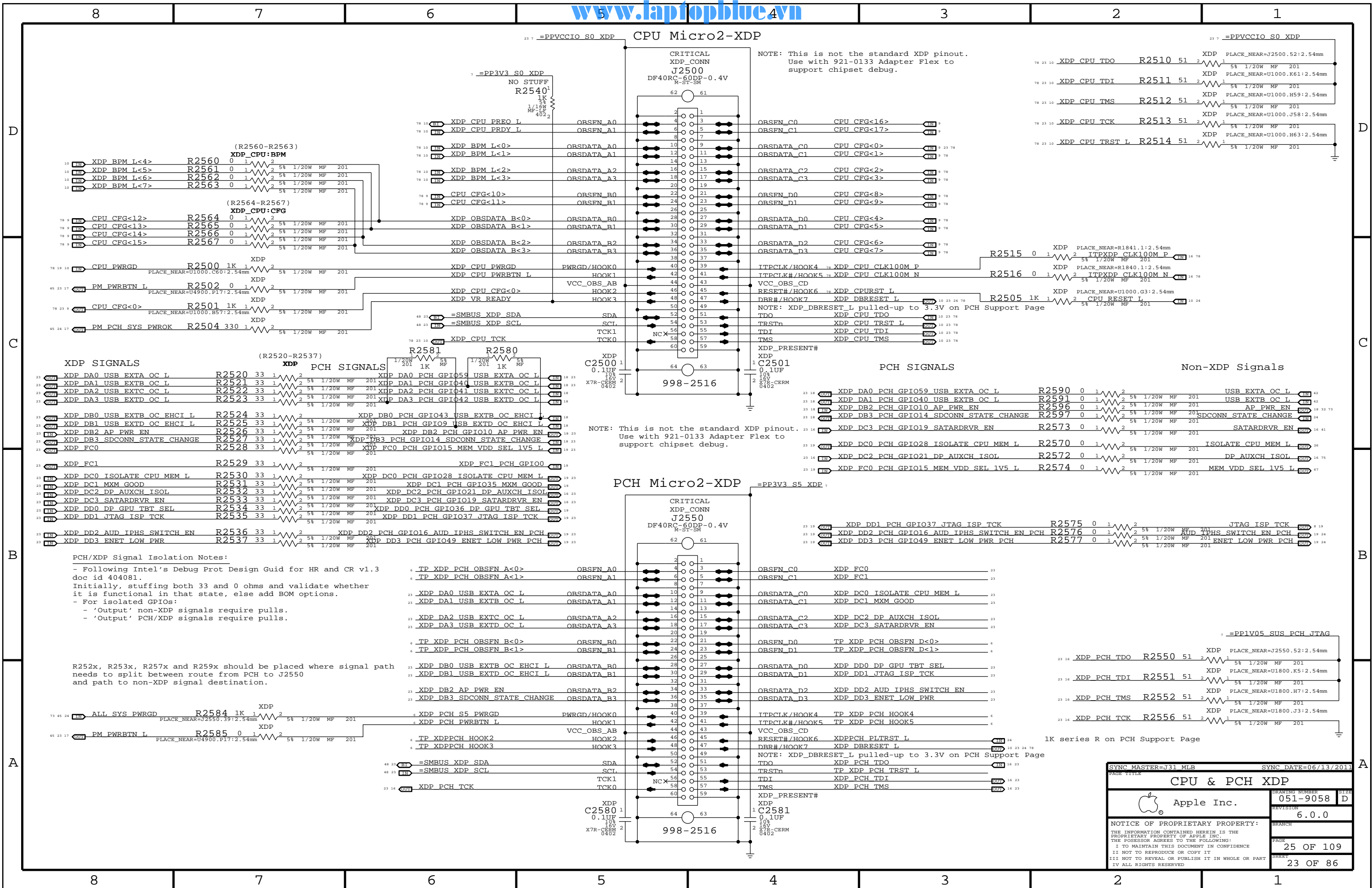
SYNC MASTER=J31 MLB		SYNC DATE=06/13/2011	
PAGE TITLE			
PCH PCI/USB/TP/RSVD			
	Apple Inc.	DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
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Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
 A memory should add pull-downs on another page and set straps per software.

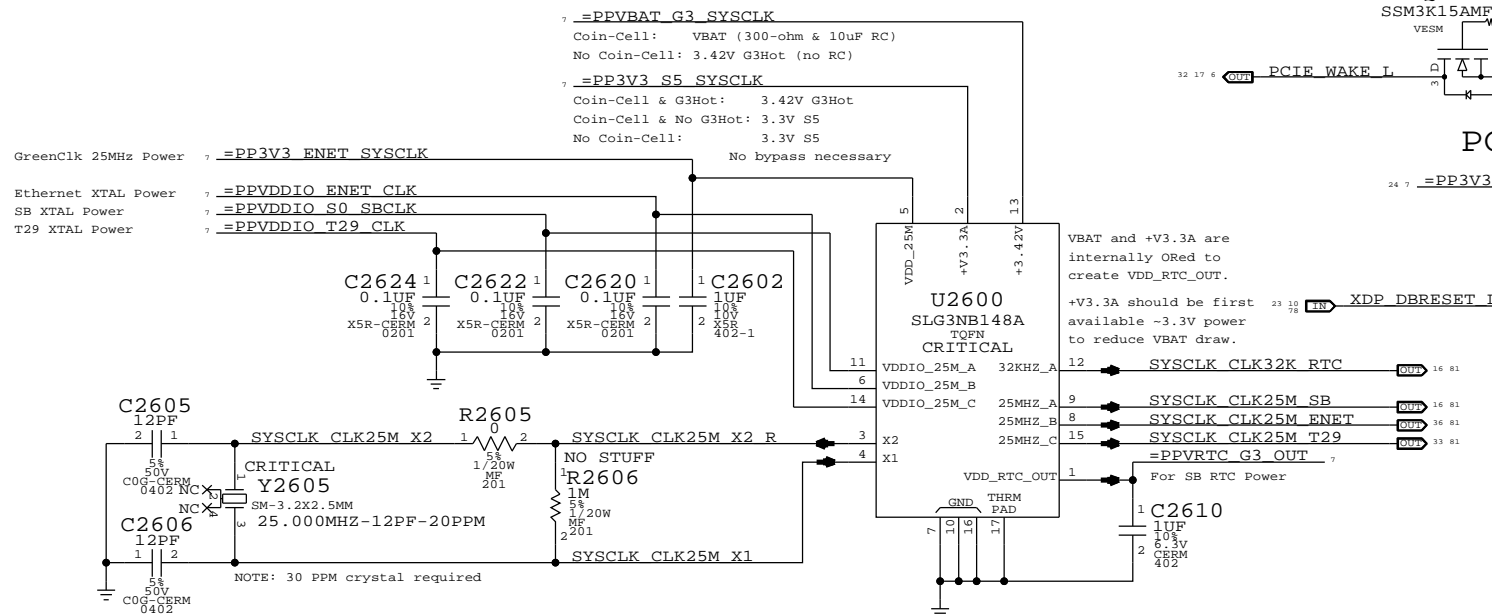


SYNCH MASTER=J31 MLB		SYNCH DATE=06/13/2011	
PAGE TITLE			
PCH GPIO/MISC/NCTF			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-9058		D
	REVISION		
	6.0.0		
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BRANCH		PAGE	
		21 OF 109	
SHEET		19 OF 86	

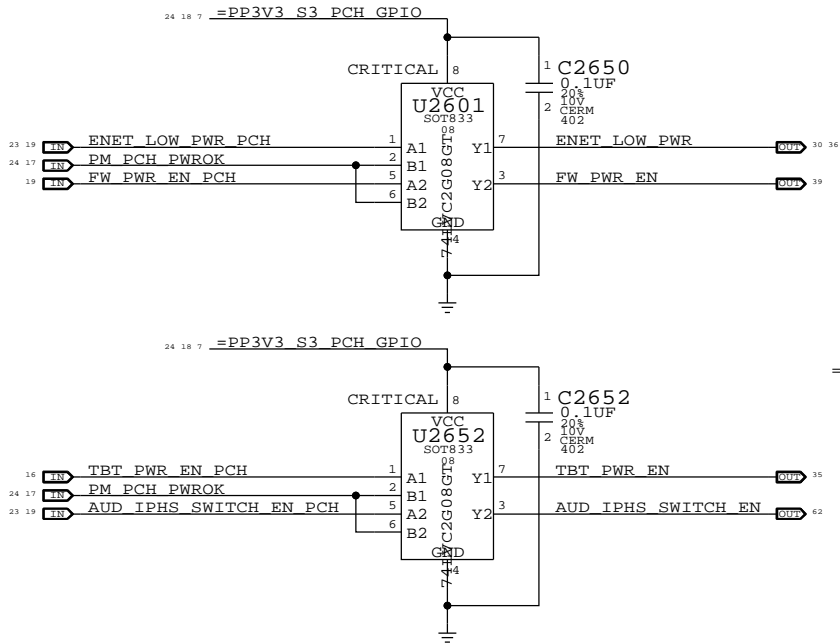




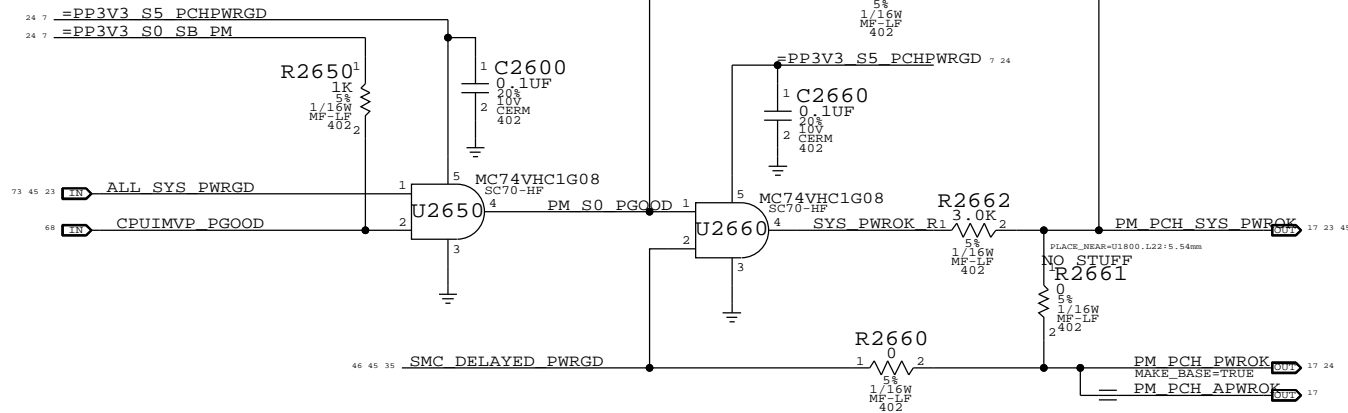
System RTC Power Source & 32kHz / 25MHz Clock Generator



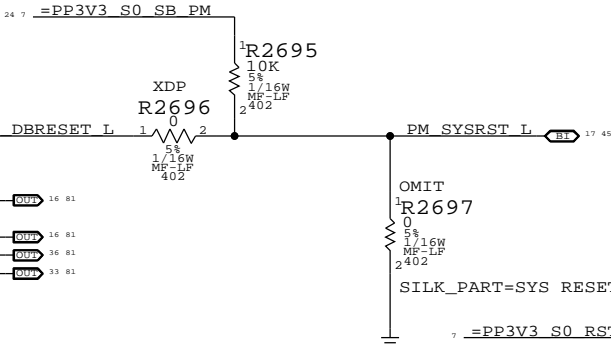
GPIO Glitch Prevention



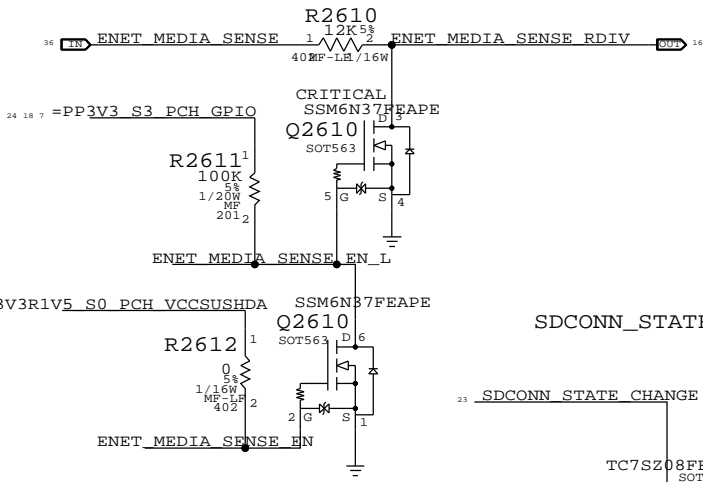
PCH S0 PWRGD



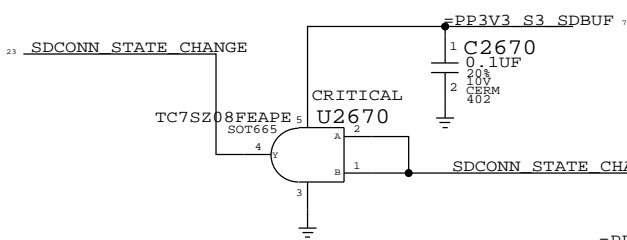
PCH Reset Button



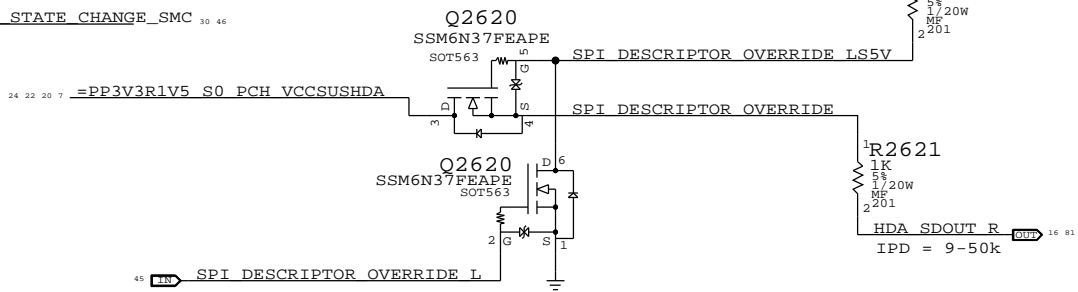
ENET_MEDIA_SENSE ISOLATION CIRCUIT




SDCONN_STATE_CHANGE ISOLATION



PCH ME Disable Strap



SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
Chipset Support			
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		REVISION	D
		6.0.0	
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USB MUX FOR LS/FS INTERNAL DEVICES

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0, HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0, HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1, HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1, HUB_NONREM0_1

NON_REM 1 : NON_REM 0
0 : 0
1 : 1
1 : 1

STRAP PIN CFG
ALL PORTS ARE REMOVABLE
PORT 1 IS NON REMOVABLE
PORT 1&2 ARE NON REMOVABLE
PORT 1&2&3 ARE NON REMOVABLE

CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STARPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB2512B

J5 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B

D

D

C

C

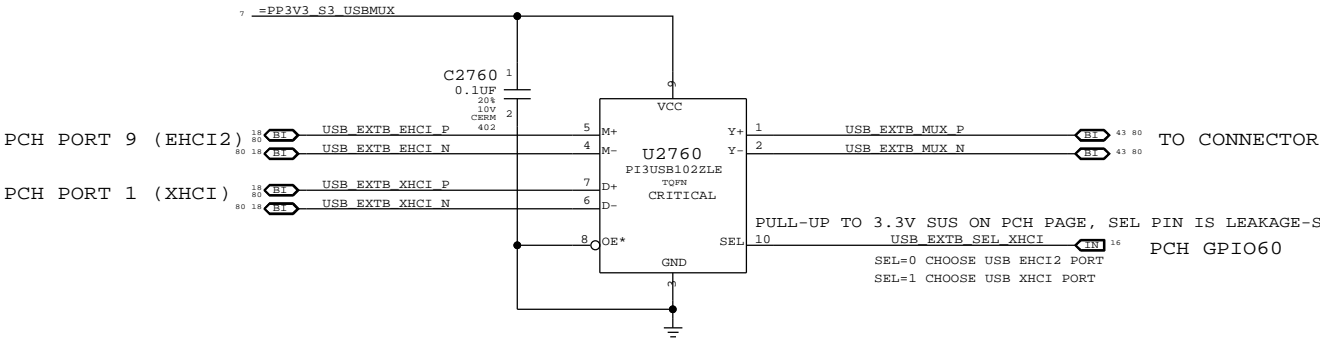
B

B

A

A

USB XHCI/EHCI2 PORT MUX FOR EXT B



PAGE TITLE		PAGE NUMBER	
USB HUB & MUX		051-9058	
Apple Inc.		6.0.0	
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

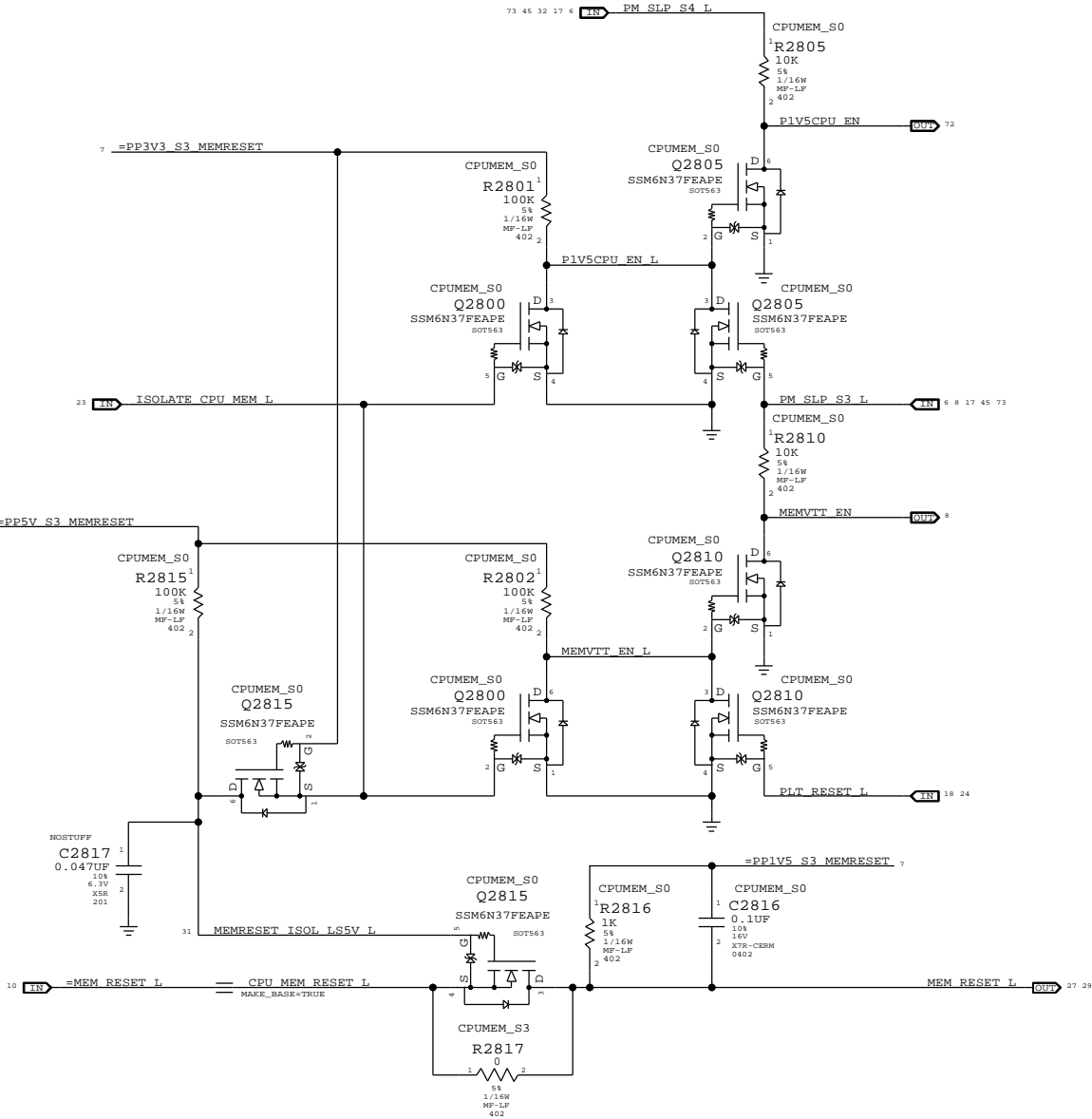
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

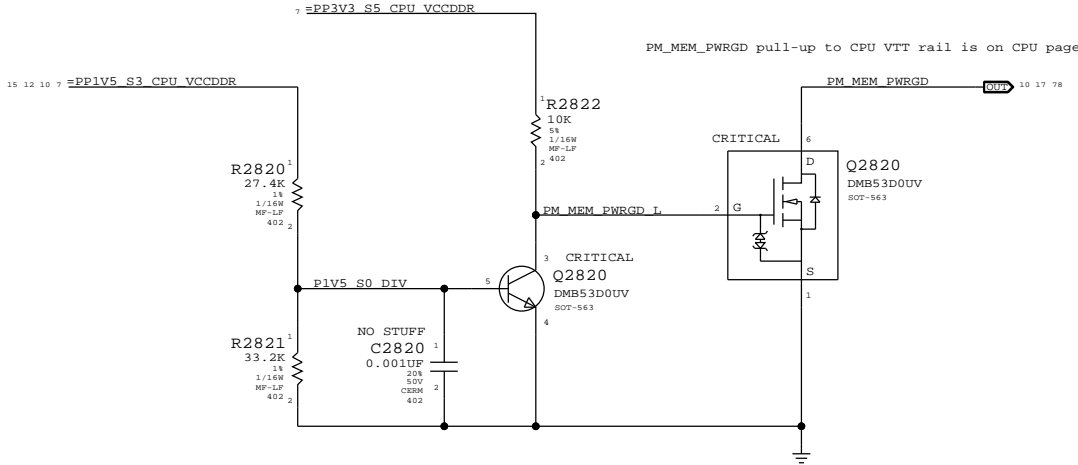
P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

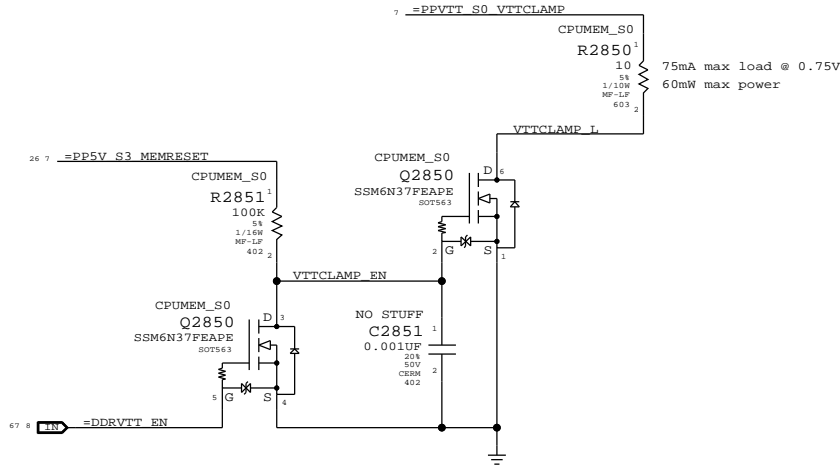


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPUMEM_RESET_L	1	1
1	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPUMEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=K901 MLB

SYNC DATE=02/15/2011

CPU Memory S3 Support

Apple Inc.

051-9058

6.0.0

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```

Power aliases required by this page:
- #PPIV5_S3_MEM_A
- #PPIV5_S3_MEM_A
- #PPIV5_S3_MEM_VTT_A
- #PPIV5_S3_MEM_A (2.5 - 3.3V)

```

```

Signal aliases required by this page:
- #I2C_S0D19MA_SCL
- #I2C_S0D19MA_SDA

```

```

BCM options provided by this page:
(BCM)

```

Power aliases required by this page:

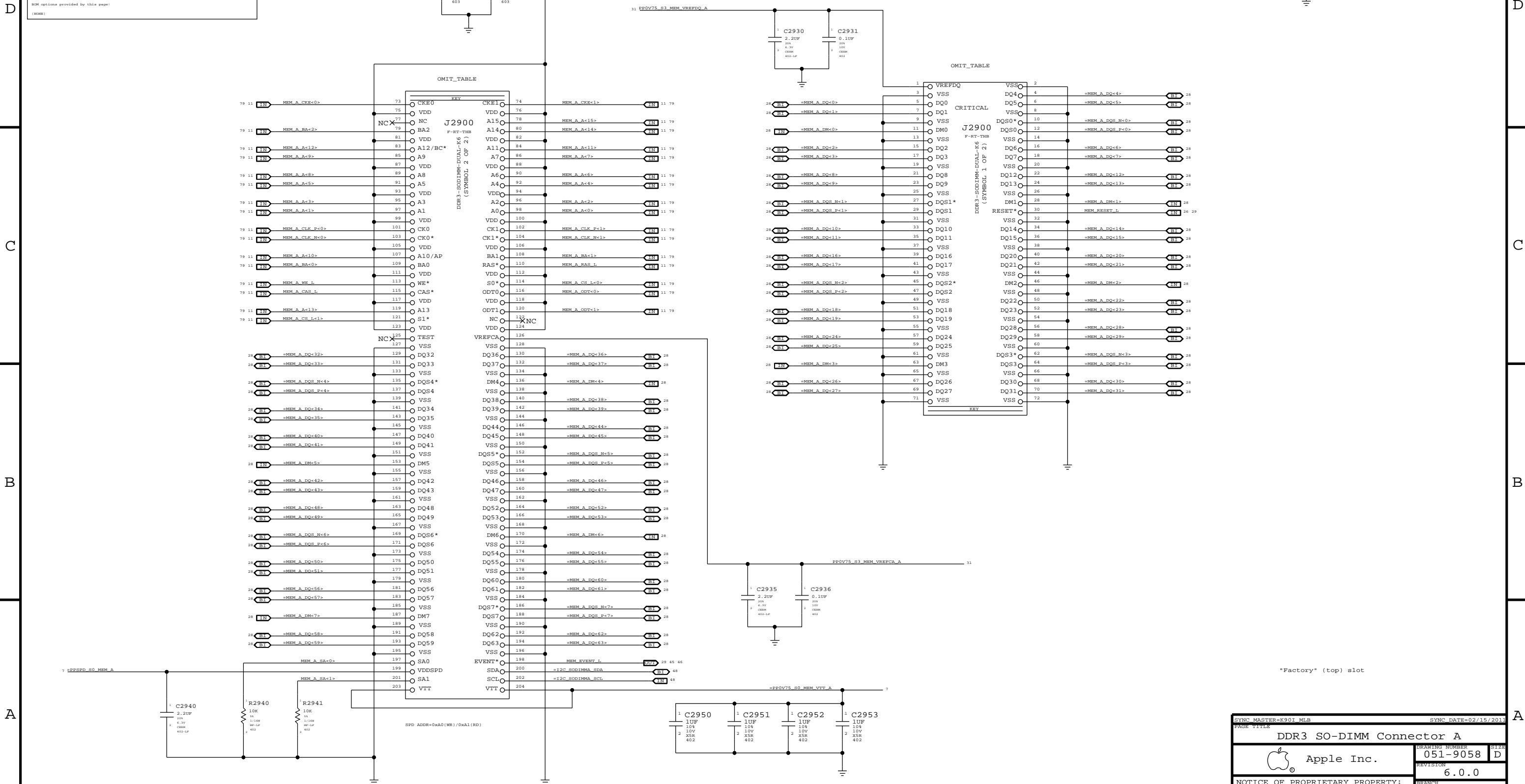
- SP1V5_S0_MEM_A
- SP1V5_S3_MEM_A
- SP0V75_S0_MEM_VTT_A
- SP0SD_S0_MEM_A (2.5 - 3.3V)


Signal aliases required by this page:

- I2C_S0DIN0A_SCL
- I2C_S0DIN0A_SDA

BCM options provided by this page:

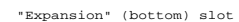
(NONE)




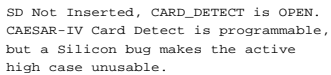
SYNC MASTER-K901 MLB		SYNC DATE=02/15/2013	
PAGE TITLE			
DDR3 SO-DIMM Connector A			
 Apple Inc.		DRAWING NUMBER 051-9058	SIZE D
		REVISION 6.0.0	
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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

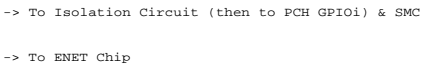
7 =PP1V5 S3 MEM B



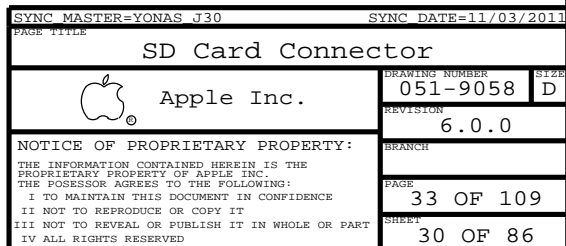
SYNC MASTER#K901 MLB PRICE TITLE		SYNC DATE=02/15/2011	
DDR3 SO-DIMM Connector B			
 Apple Inc.		DRAWING NUMBER 051-9058	SIZE D
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SDCONN_DETECT Debounce, Inversion, Detect-Changed PCH GPIO Latch Circuit
Converts SDCONN from active-low level signal to active-high pulses.



TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:


DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

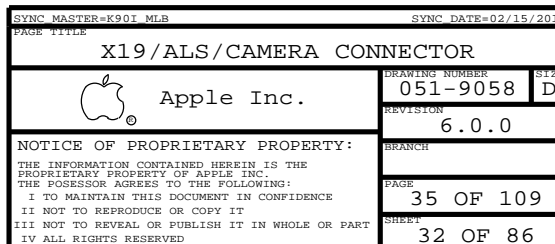
RST* on 'platform reset' so that system watchdog will disable margining.
NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

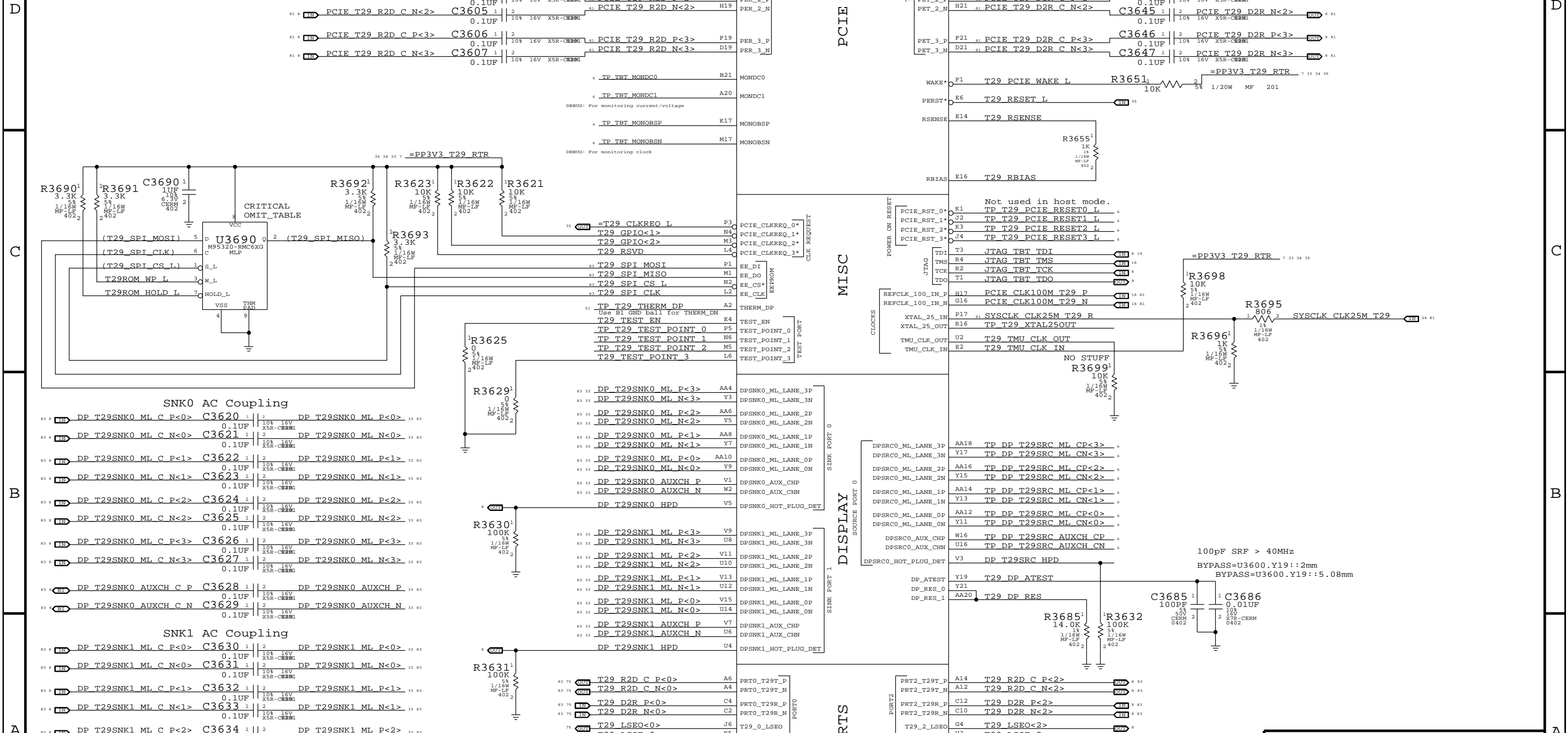
	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.000V (0x00 - 0xFF)
VRef current:		+3.4mA - -3.4mA (= sourced)			+61uA - -61uA (= sourced)	+6.0mA - -5.0mA (= sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

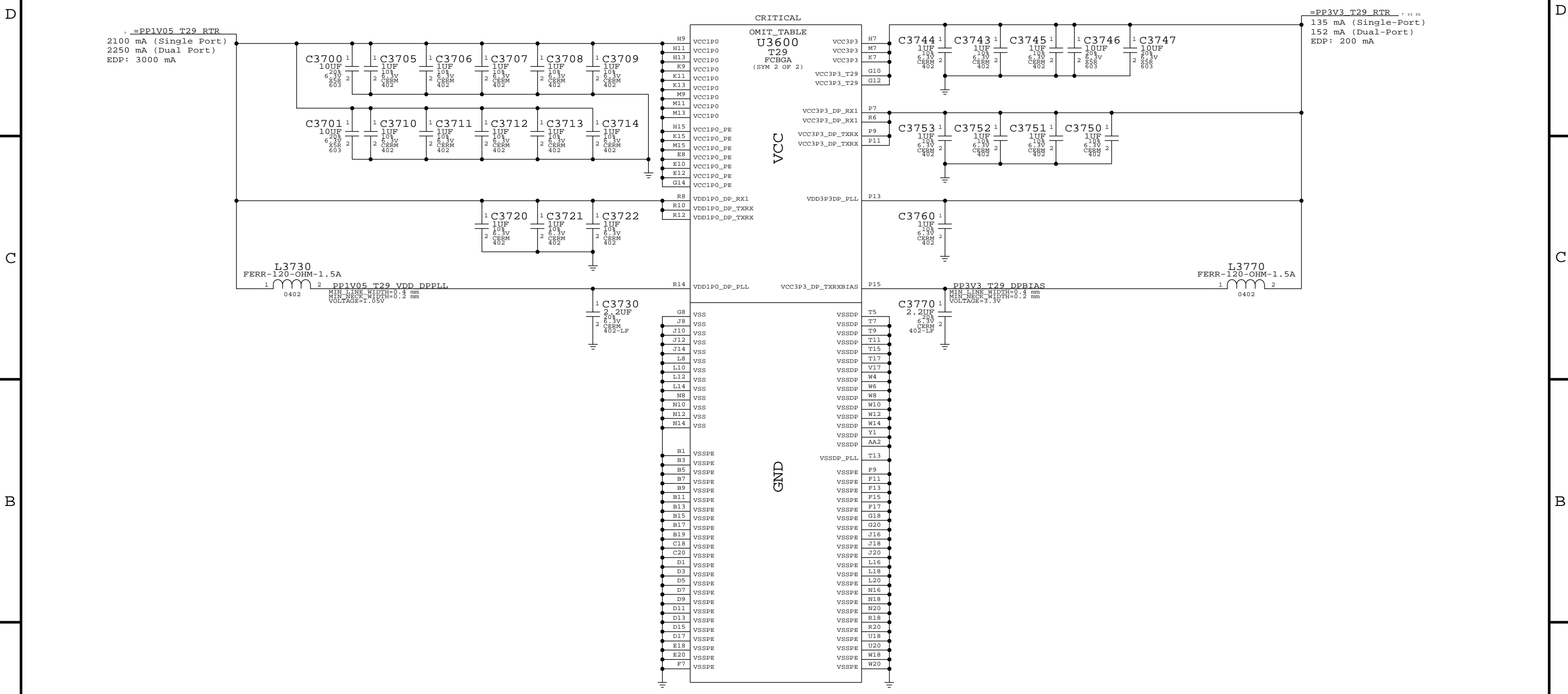
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1%,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

SYNC MASTER=J31 MLB		SYNC DATE=06/13/2011	
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DDR3/FRAMEBUF VREF MARGINING			
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Page Notes

Power aliases required by this page:

- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

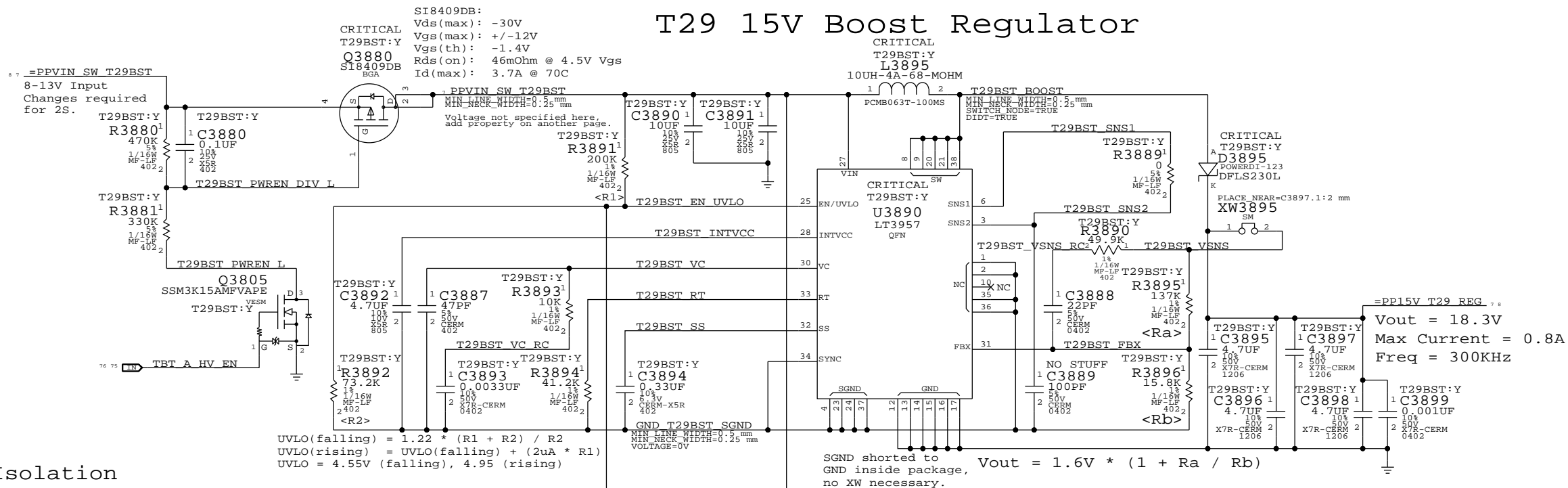
Signal aliases required by this page:

- =T29_CLKREQ_L
- =T29_RESET_L

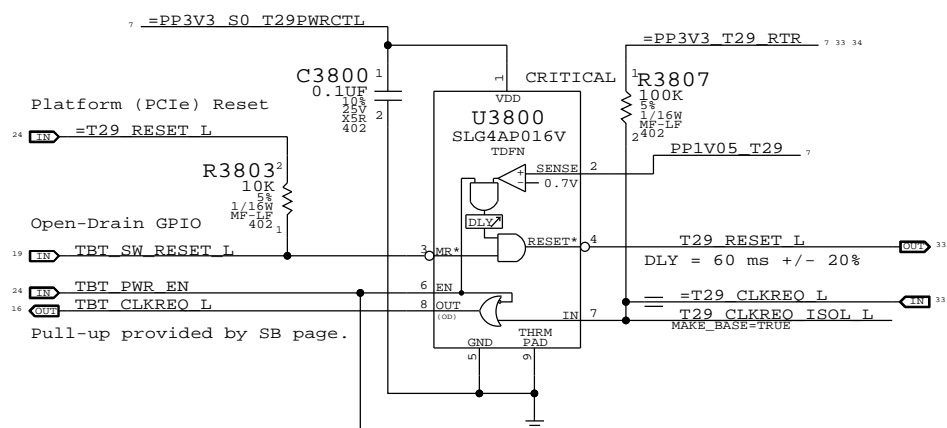
BOM options provided by this page:

T29BST:Y - Stuffs 18V boost circuitry.

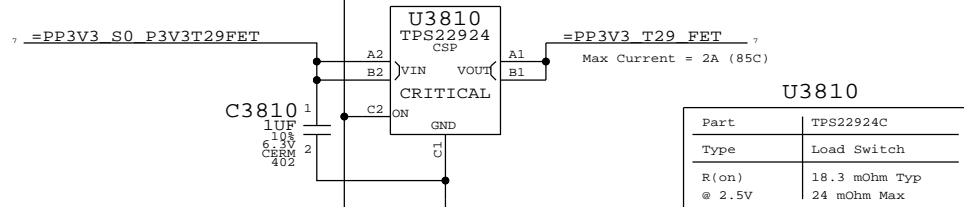
T29 15V Boost Regulator



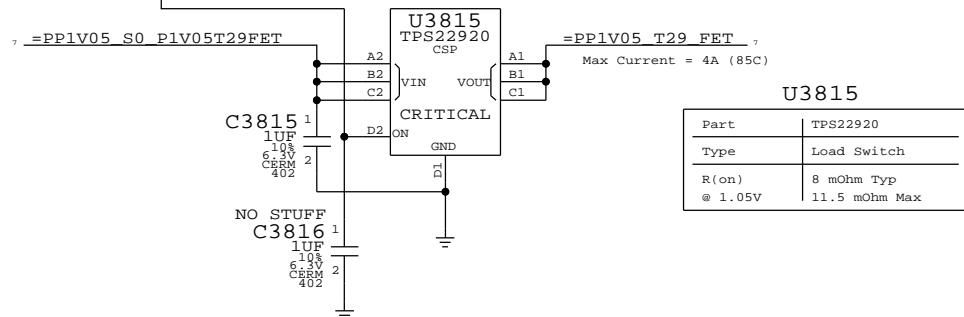
Supervisor & CLKREQ# Isolation




3.3V T29 Switch

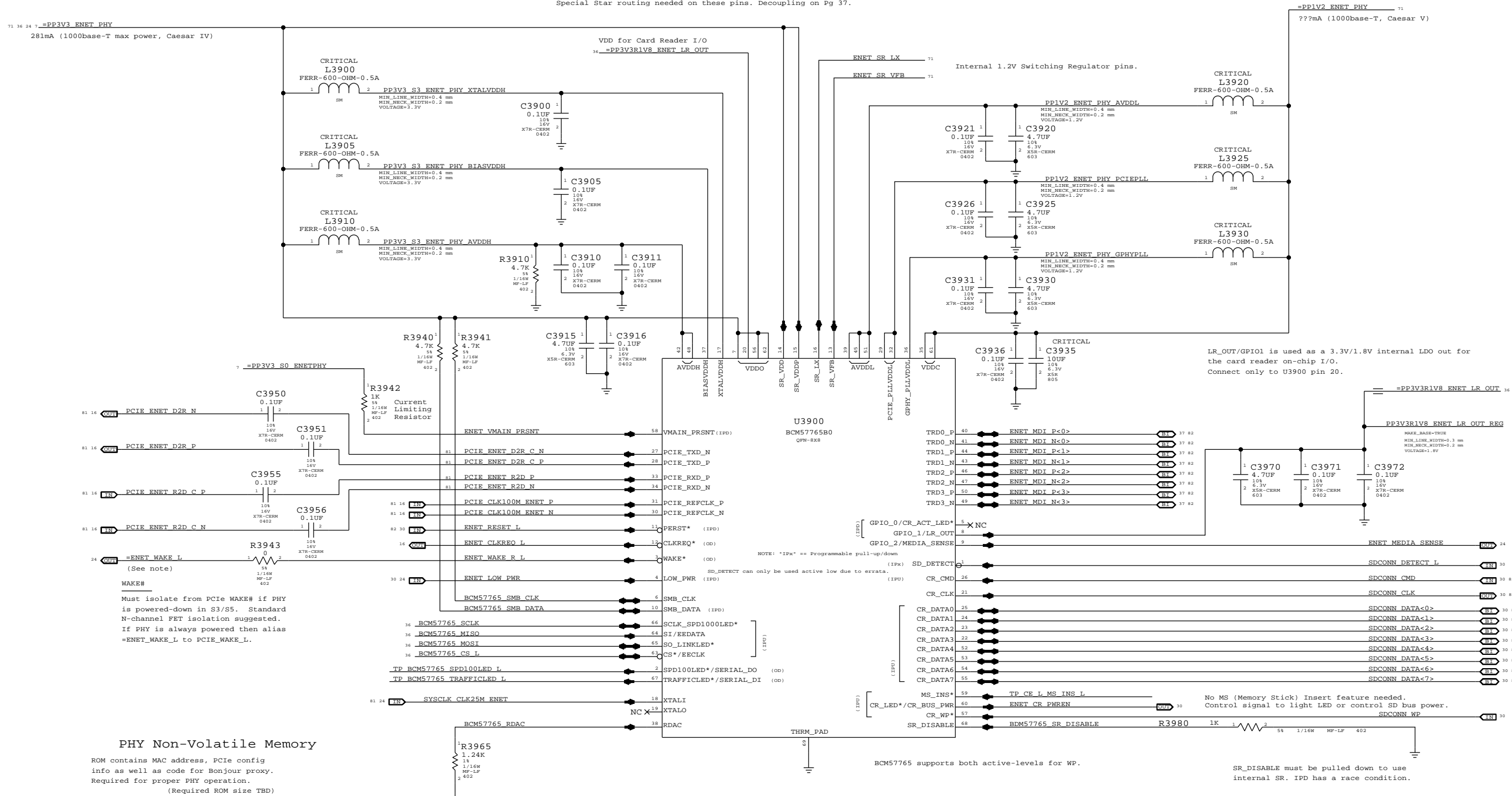


1.05V T29 Switch



SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
T29 Power Support			
 Apple Inc.	DRAWING NUMBER	051-9058	SIZE
	REVISION	6.0.0	D
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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

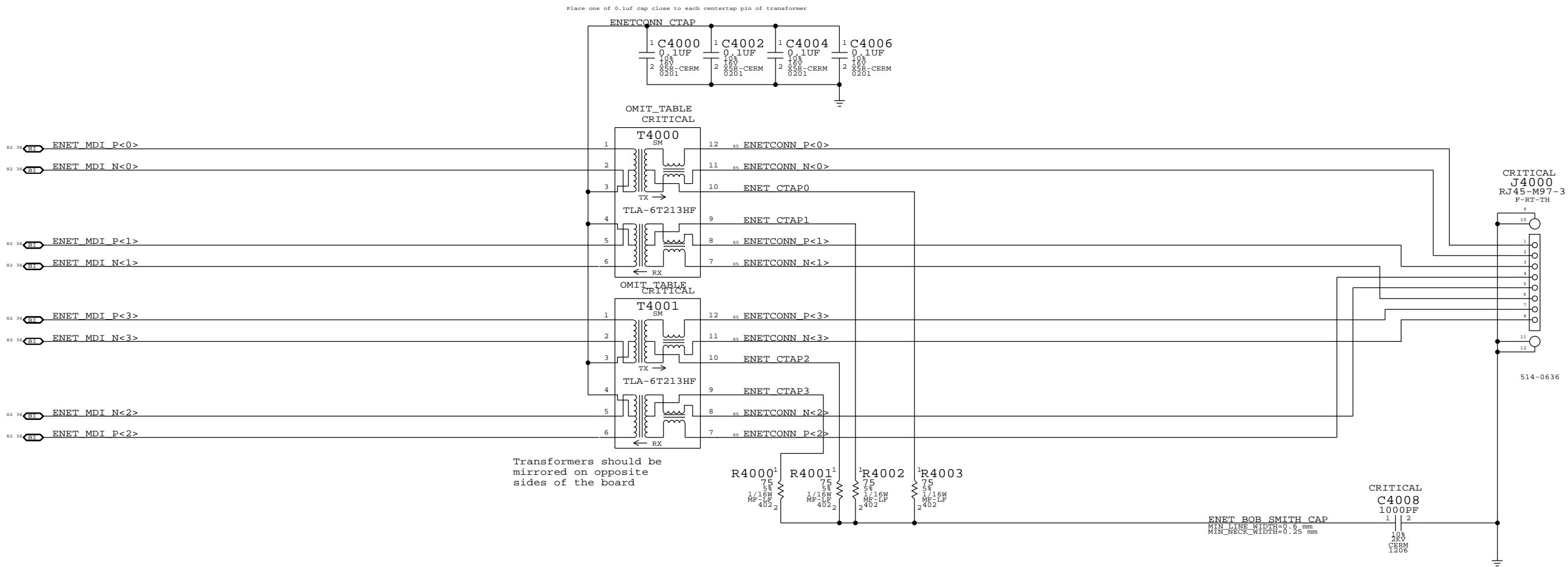


Page Notes


Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

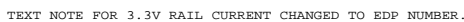
BOM options provided by this page:
(NONE)




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
157S0084	2	XFMR, ISO, HALF-PORT, 1000T, 12P, SMD, HF	T4000, T4001	CRITICAL	

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2013	
PAGE TITLE			
Ethernet Connector			
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		REVISION	6.0.0
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BOM options provided by this page:
(NONE)

Max Output: 2A

SYNCH MASTER#K901 MLB		SYNCH DATE=06/23/2011	
PAGE TITLE			
FireWire Port & PHY Power			
 Apple Inc.		DRAWING NUMBER	D SIZE
		051-9058	A
		REVISION	
		6.0.0	
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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:

- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

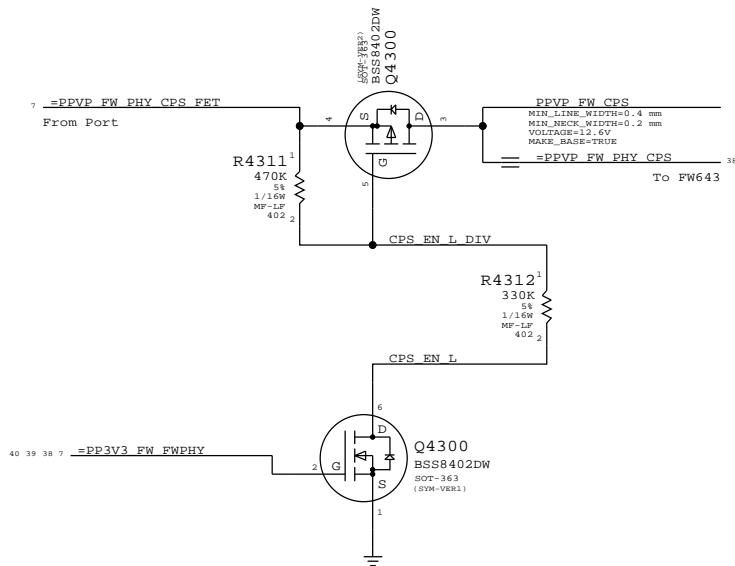
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:

(NONE)
1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

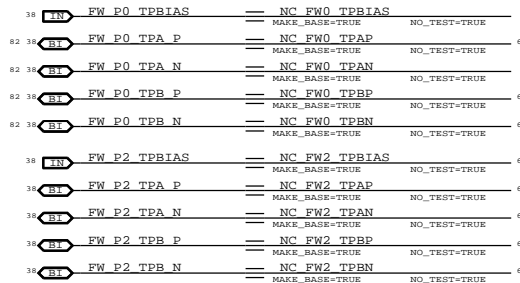
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



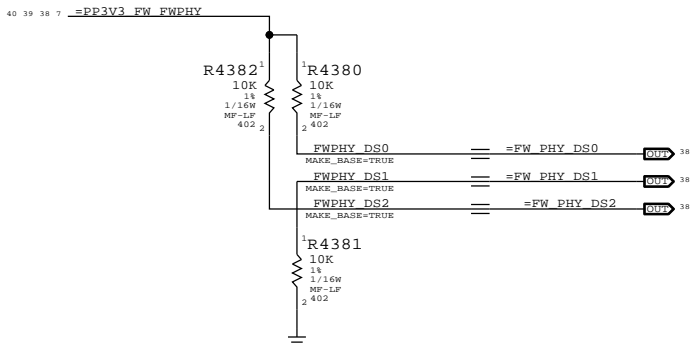
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



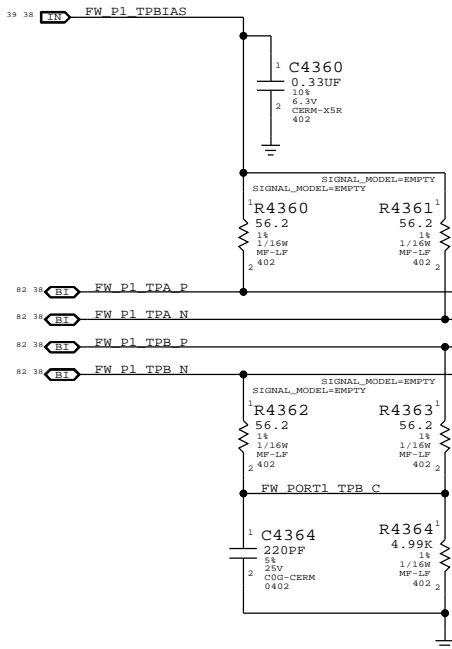
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)



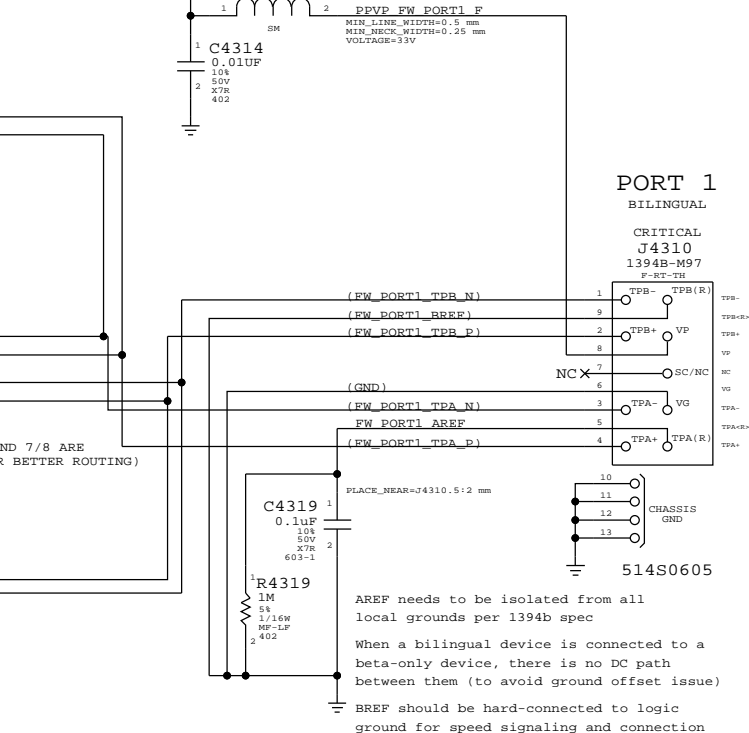
Termination

Place close to FireWire PHY



Cable Power

PPVP FW_PORT1



PORT 1

BILINGUAL

CRITICAL

J4310

1394B-M97

F-RT-TH

TPB(R)

TPB(L)

VP

SC/NC

VG

TPA(R)

TPA(L)

CHASSIS GND

514S0605

AREF needs to be isolated from all local grounds per 1394b spec
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)
BREF should be hard-connected to logic ground for speed signaling and connection

CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

FireWire Connector

Apple Inc.

DRAWING NUMBER

051-9058

REVISION

6.0.0

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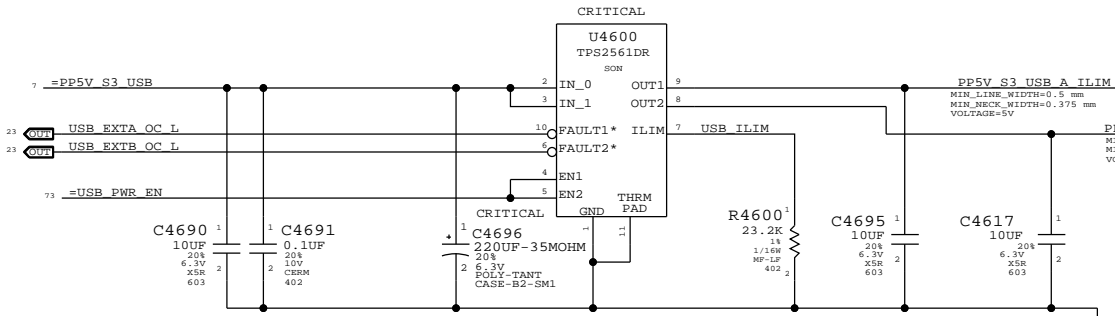
43 OF 109

SHEET

40 OF 86

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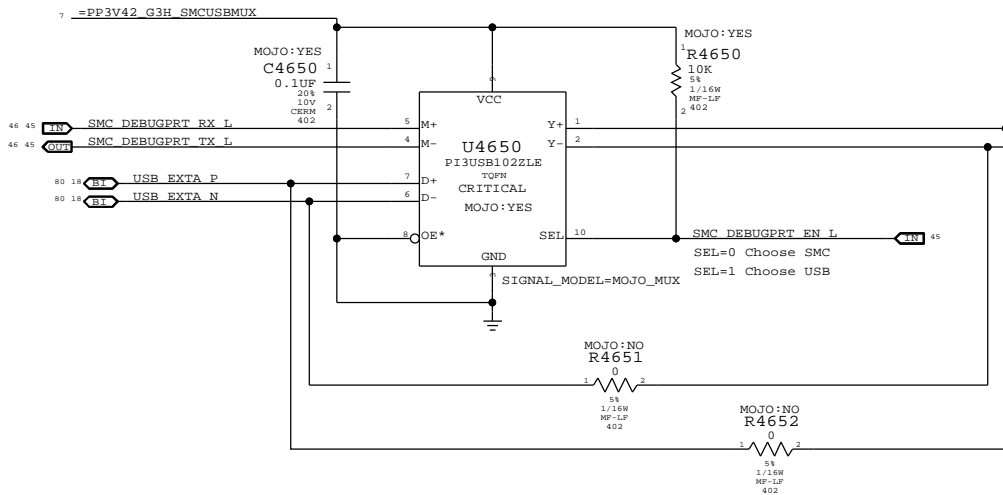
USB Port Power Switch



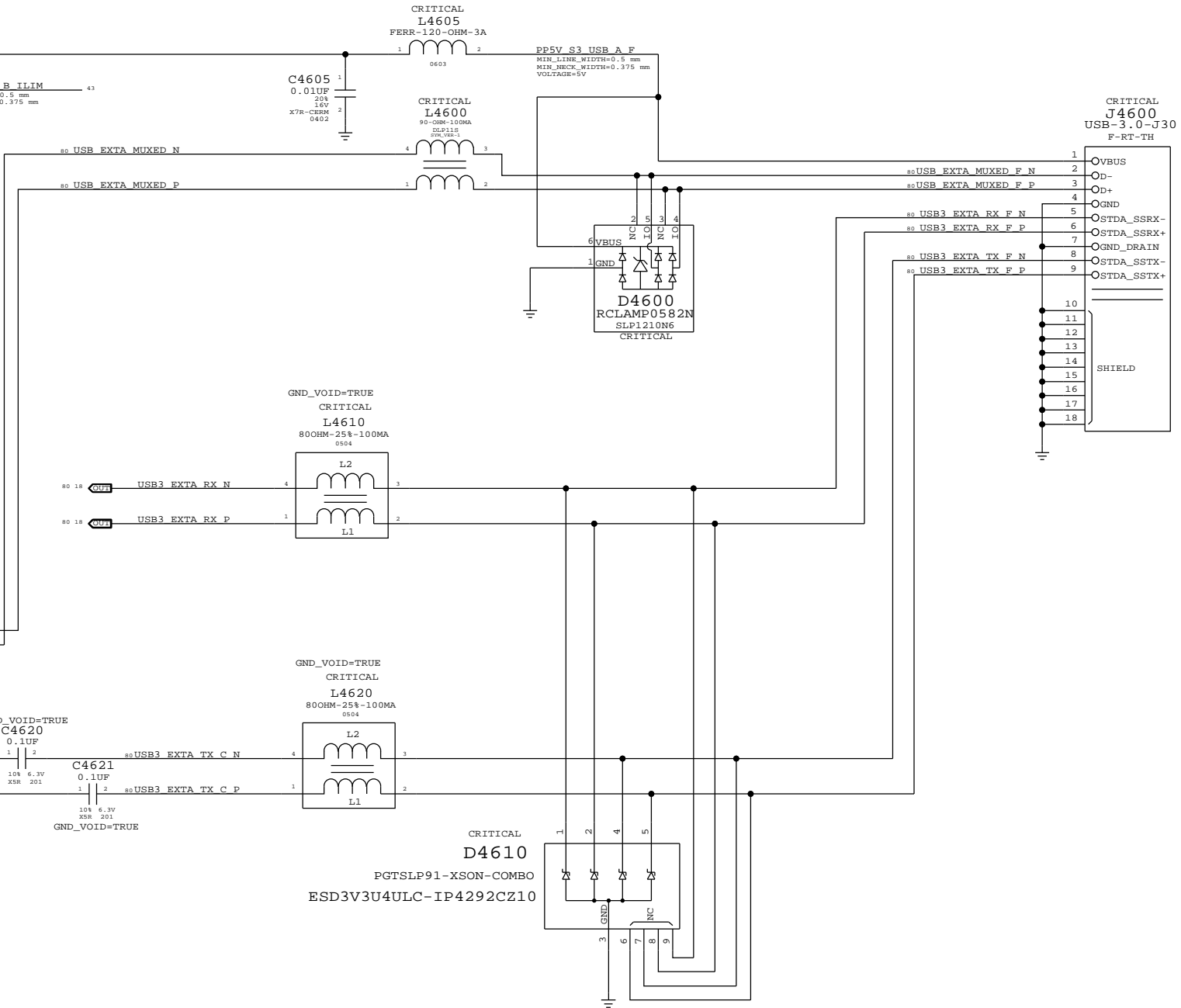
Current limit per port (R4600): 2.18A min / 2.63A max

www.qdzbwx.com

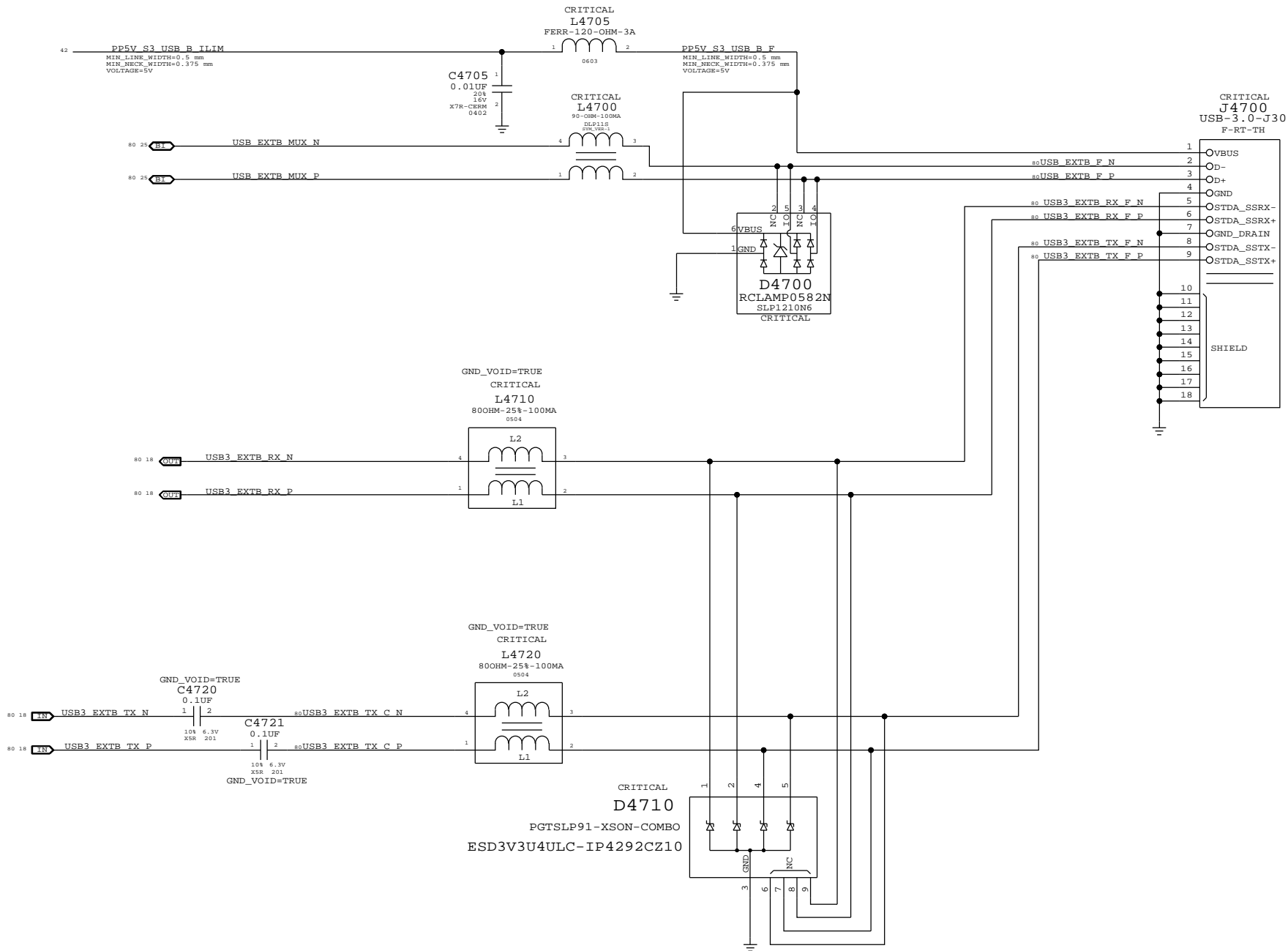
Mojo SMC Debug Mux




USB Port A (Front Port)



USB Port B (Back Port)



NOTE: Swapped pin4 and 5, pin6 and 7 for layout.

SYNC MASTER=J31 MLB		SYNC DATE=07/08/2013	
PAGE TITLE			
External B USB3 Connector			
 Apple Inc.		DRAWING NUMBER	SHEET
		051-9058	D
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		BRANCH	
		PAGE	47 OF 109
		SHEET	43 OF 86

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IR SUPPORT

41 7 =PP5V_S3_IR

1 C4801
0.1UF
10V
X7R-CERM
0402

VCC

U4800
CY7C63803-LQXC
QFN

12 P1.0/D+ P0.0 7
13 P1.1/D- P0.1 6
14 P1.2/VREG INT0/P0.2 5
15 P1.3/SSEL INT1/P0.3 4
16 P1.4/SCLK INT2/P0.4 3
17 P1.5/SMOSI TIO0/P0.5 2
18 P1.6/SMISO TIO1/P0.6 1

IR VREF FILTER

1 C4803
1UF
10V
X5S
402-1

CRITICAL OMIT

P/N 33800633

NC

24 THERML PAD VSS

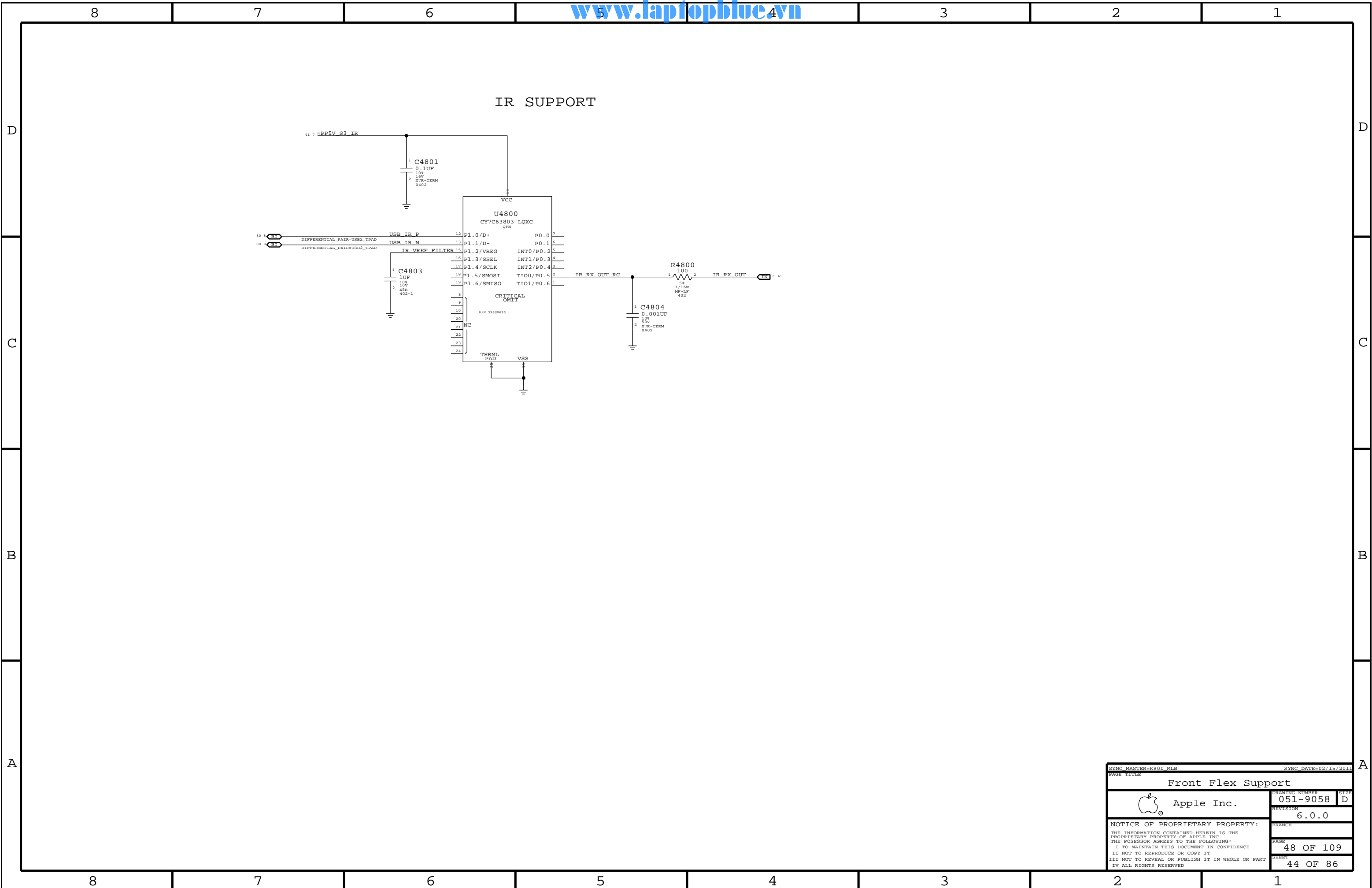
IR RX OUT RC

100
R4800
5%
1/16W
MF-LF
402

IR RX OUT

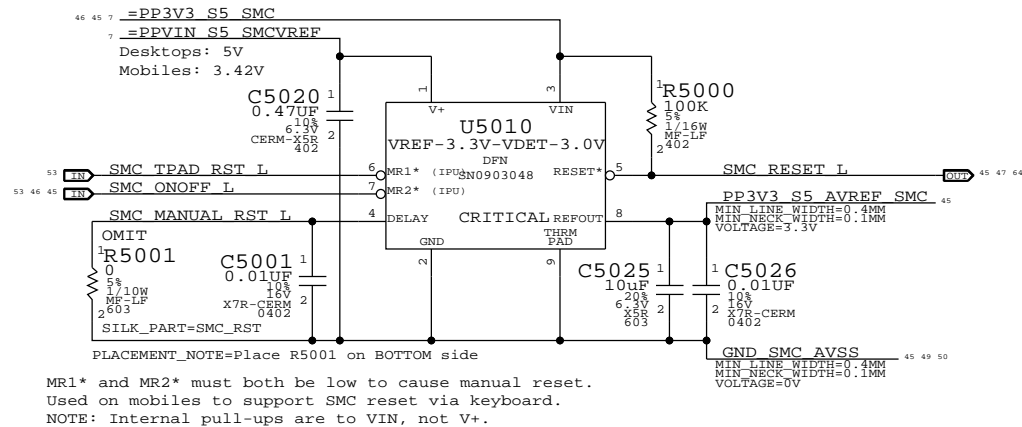
1 C4804
0.001UF
10V
X7R-CERM
0402

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2013	
PAGE TITLE			
Front Flex Support			
Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
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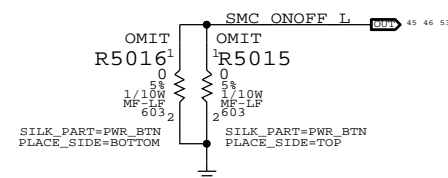
[illegible]

NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SMC Reset "Button", Supervisor & AVREF Supply

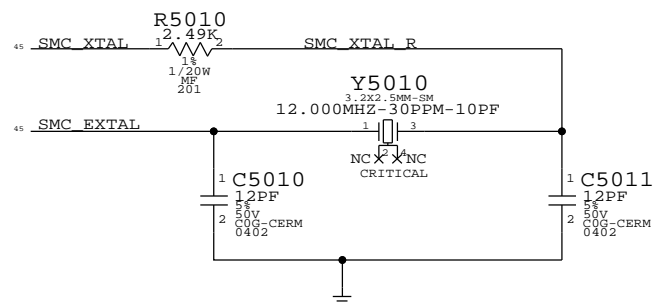


Debug Power "Buttons"



SMC Crystal Circuit

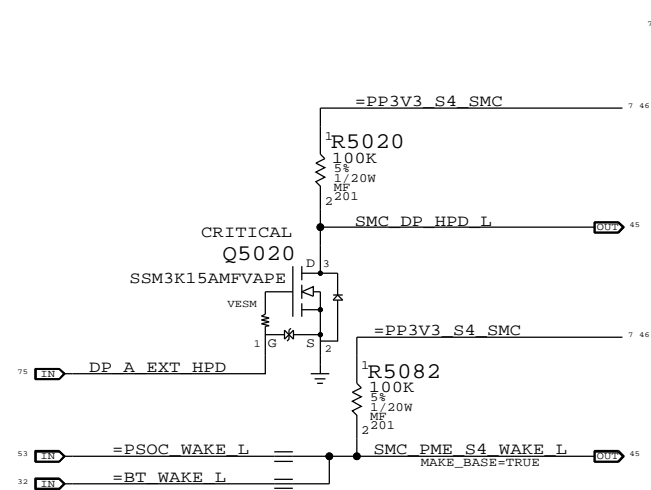
SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz



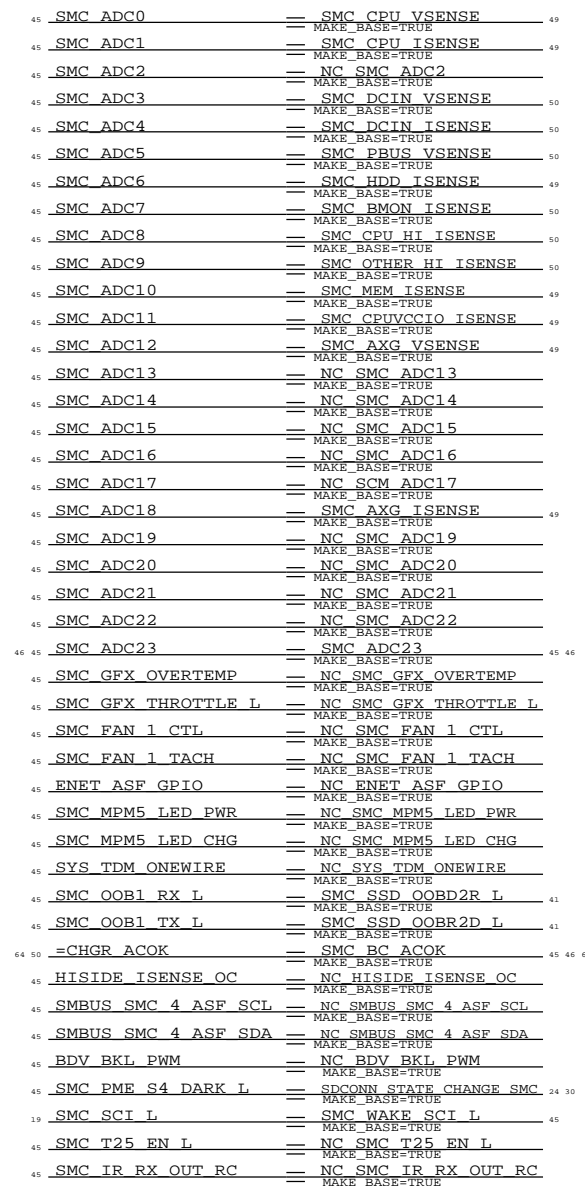
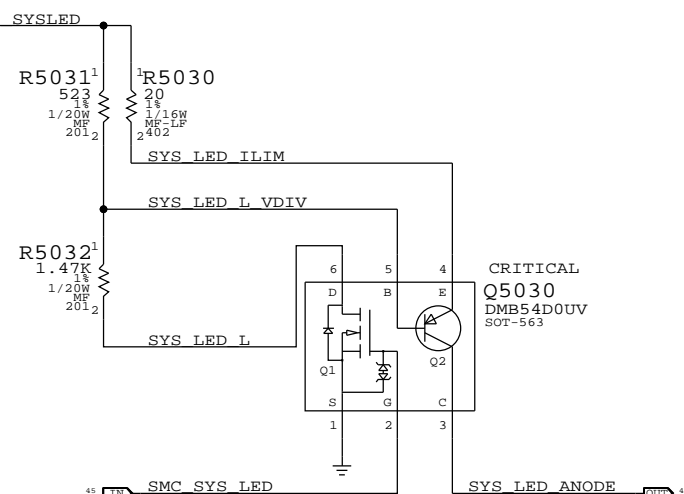
Note:
ADC10 and ADC11 are shared
with comparators on Stack Board.

Note:
Pull-up for SMC_PME_S4_DARK_L
are in page33 (R3315).

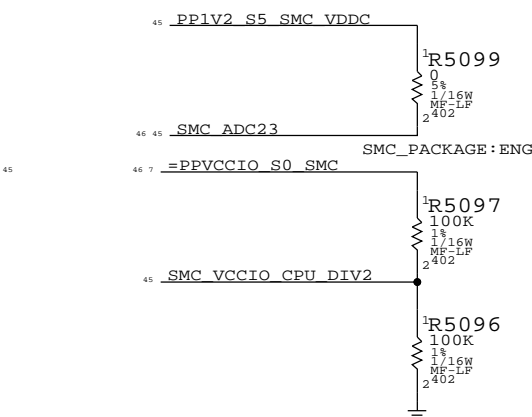
S4 HPD SMC Wake Source



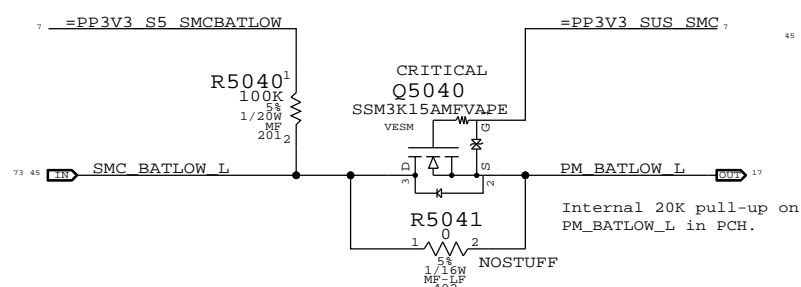
System (Sleep) LED Circuit



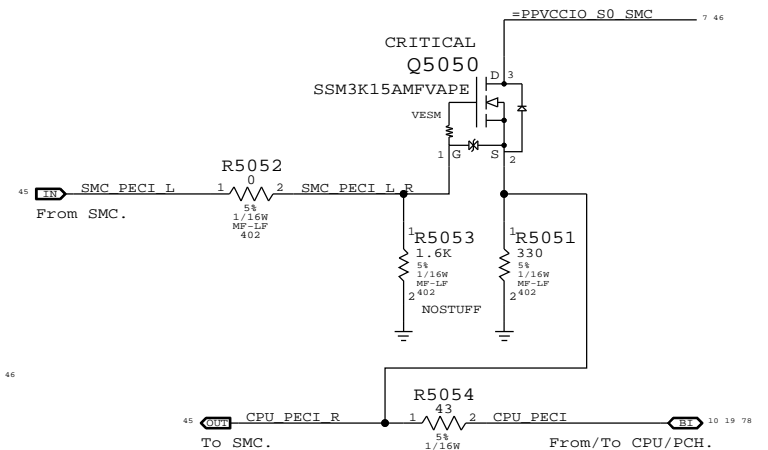
SCM12 Eng Pkg Support



BATLOW# Isolation

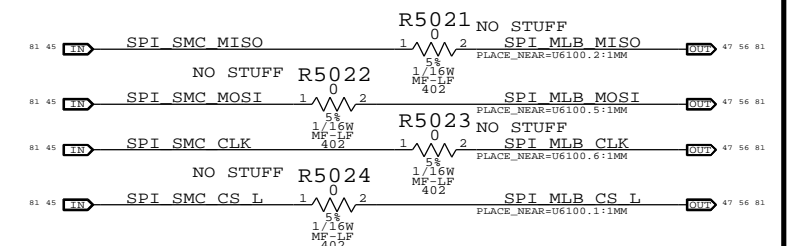


SMC12 PEFI Support

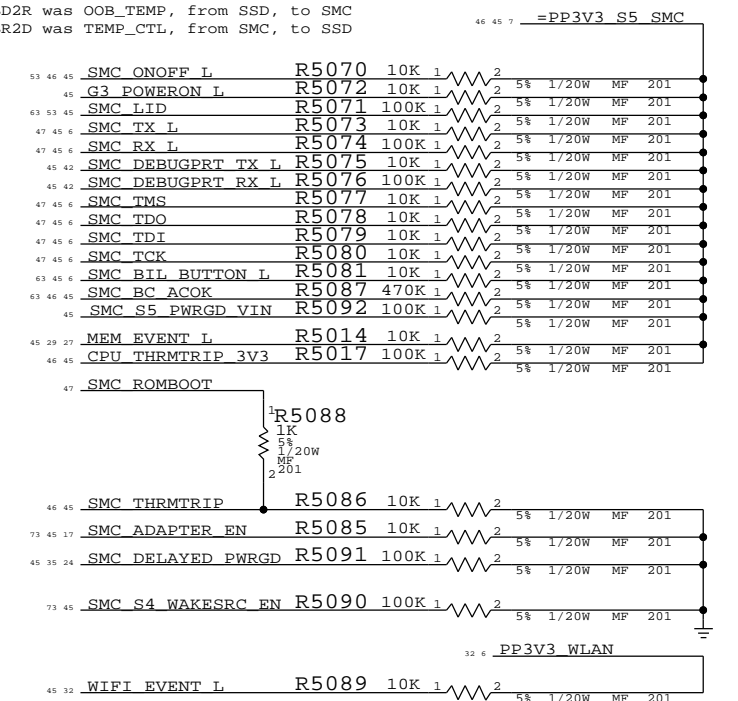



SMC12 SPI Support

Series resistors are no stuffed until the topology of 2 SPI Masters are verified.

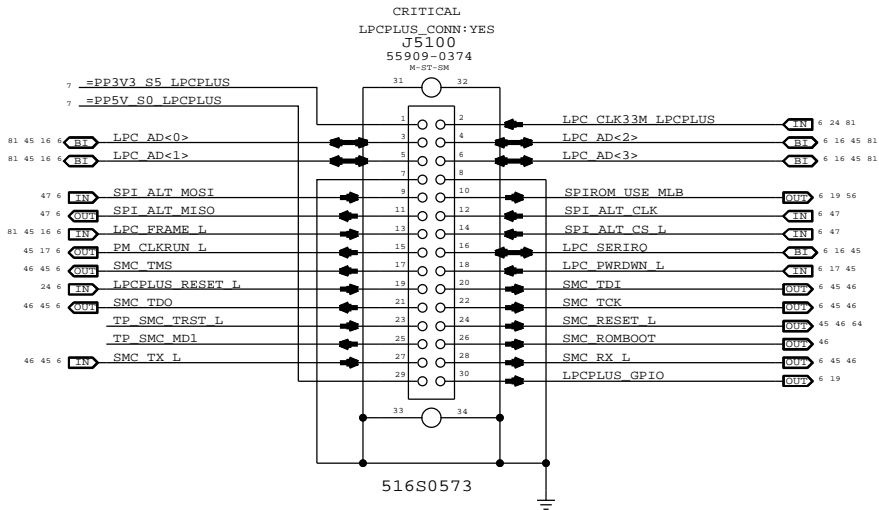


Notes:
OOBD2R was OOB_TEMP, from SSD, to SMC
OOBR2D was TEMP_CTL, from SMC, to SSD

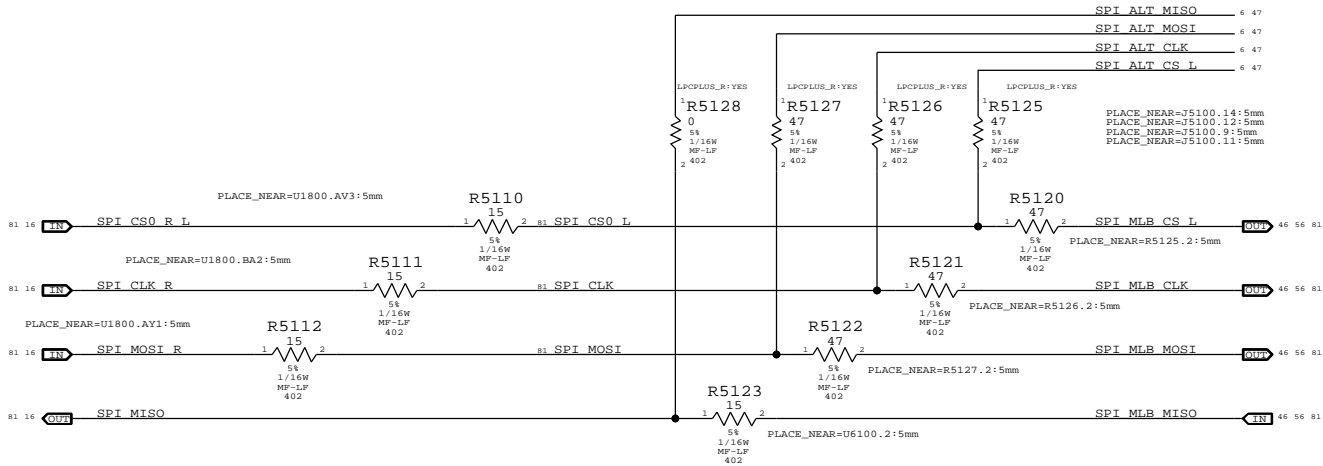


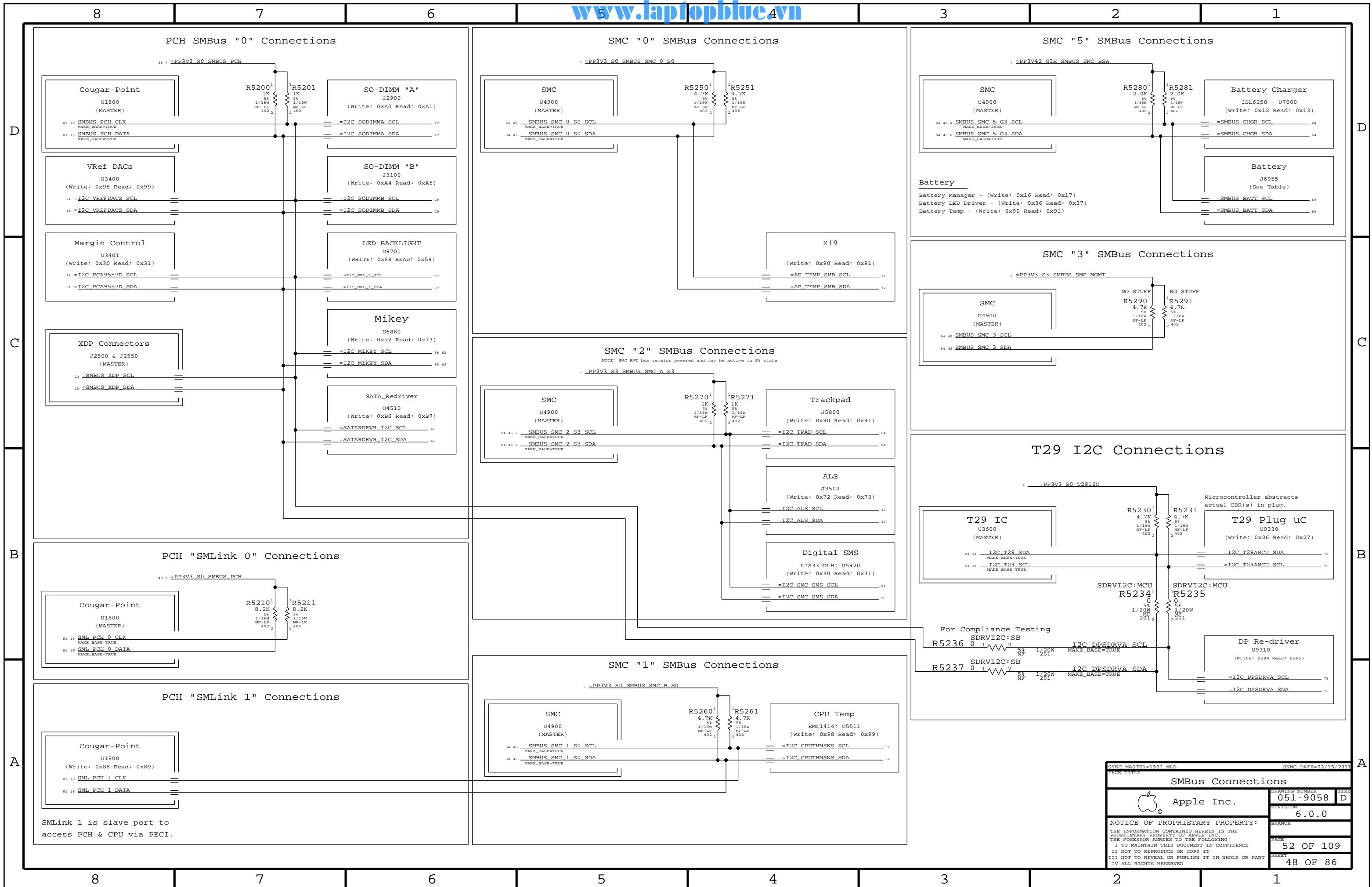
SYNC MASTER-YONAS J330		SYNC DATE=01/02/2012	
PAGE TITLE			
SMC Support			
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		SIZE	D
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LPC+SPI Connector



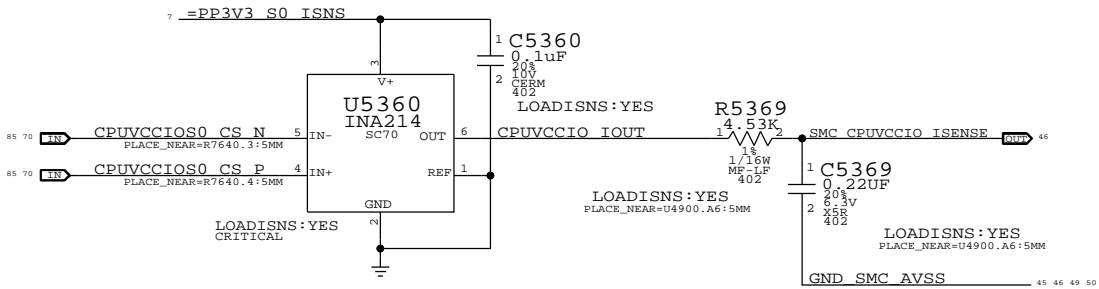
SPI Bus Series Termination





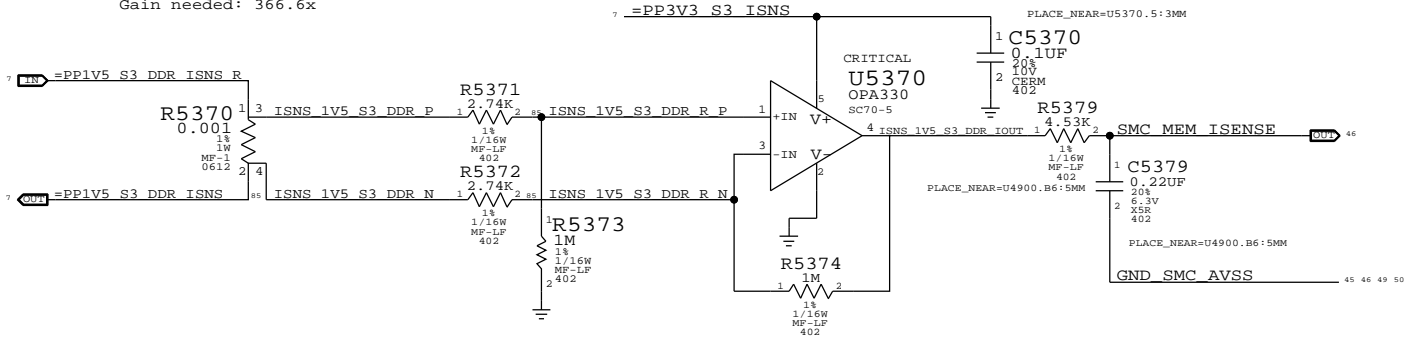
CPU VCCIO 1.05V Load Side Current Sense (IC1C)

Gain: 100x, EDP: 20.1 A
Rsense: 0.001 (R7640)
V across Rsense: 20.1 mV
Gain needed: 164.2x



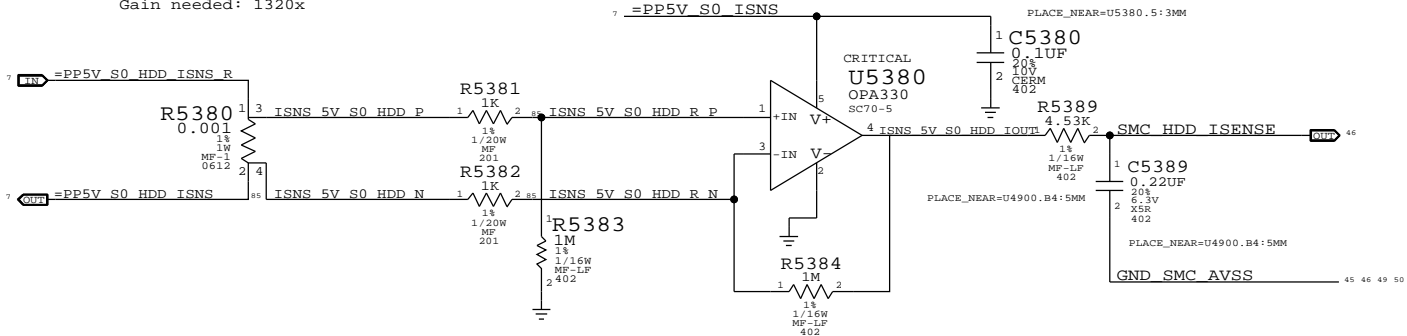
DDR 1.5V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
Gain needed: 366.6x

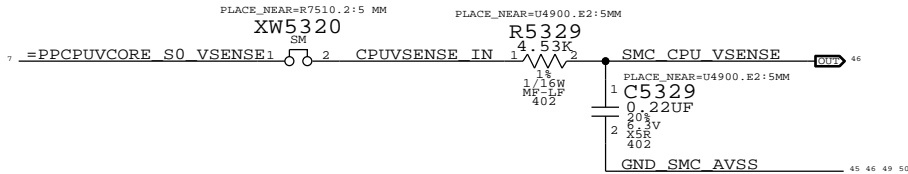


HDD Current Sense (IHDC)

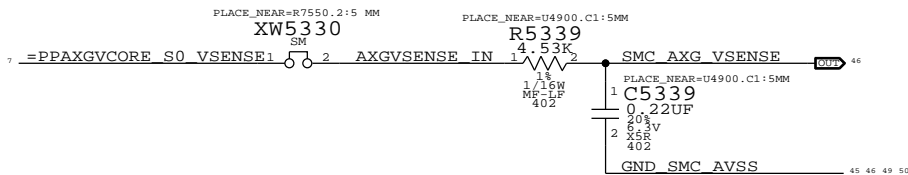
Gain: 1000x, EDP: 2.5 A (12.5 W)
Rsense: 0.001 (R5380)
V across Rsense: 2.5 mV
Gain needed: 1320x



CPU Core Voltage Sense (VC0C)

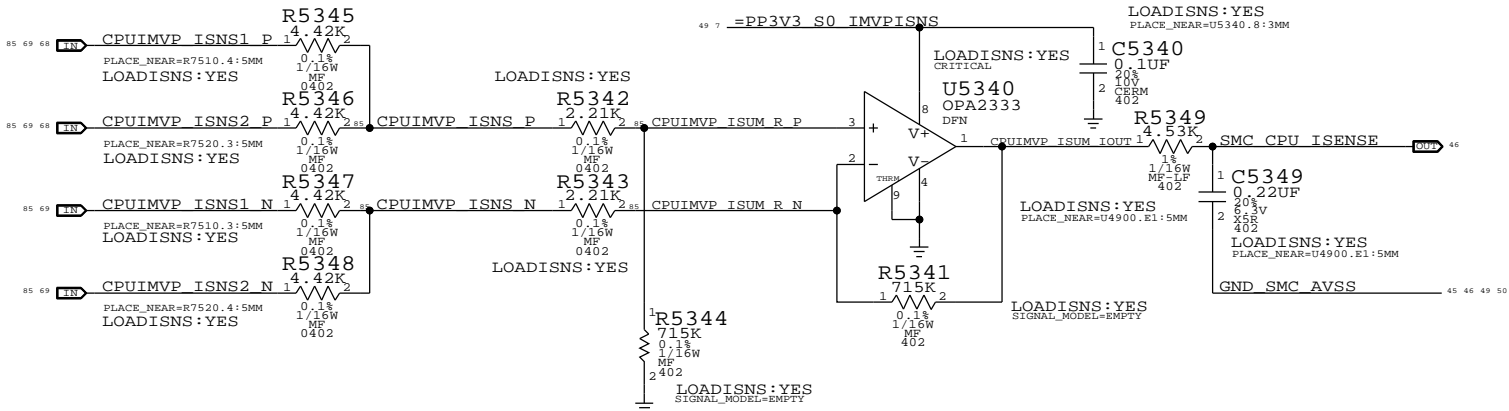


AXG Core Voltage Sense (VN0C)



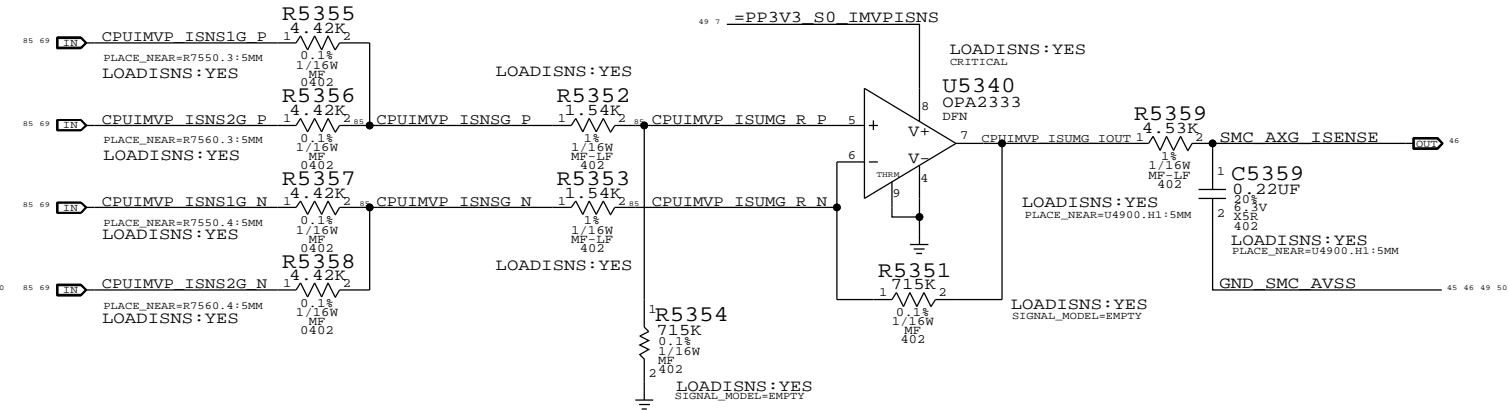
CPU Core Load Side Current Sense (IC0C)

Gain: 161.5x, EDP: 53 A
Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375
V across Rsense: 19.8 mV
Gain needed: 166.1x




AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375
V across Rsense: 17.25 mV
Gain needed: 191.3x

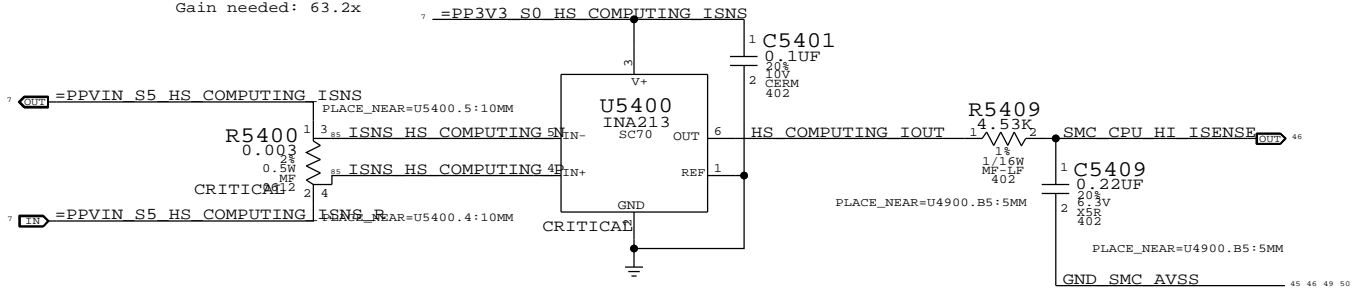


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	3	RES,MTL,FLIM,100K,1/16W,0402,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

SYNC MASTER=LINDA J30		SYNC DATE=09/28/2011	
PAGE TITLE			
Power Sensors: Load Side			
	DRAWING NUMBER		SIZE
	051-9058		D
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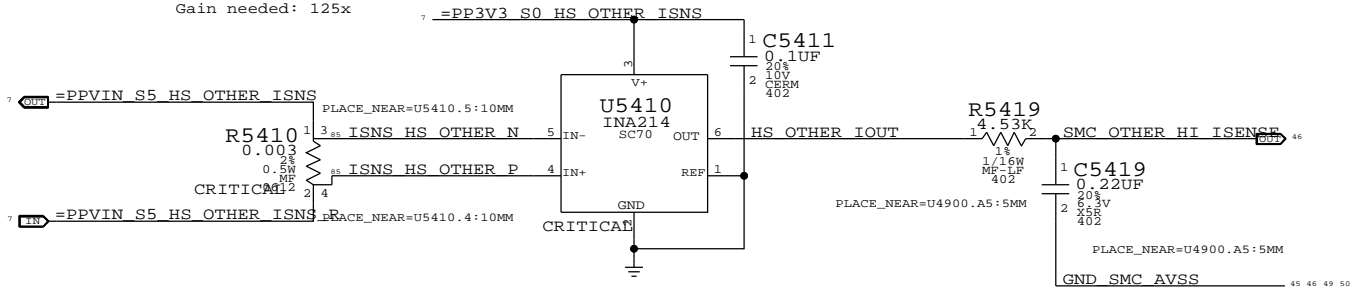
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
Rsense: 0.003 (R5400)
V across Rsense: 52.2 mV
Gain needed: 63.2x



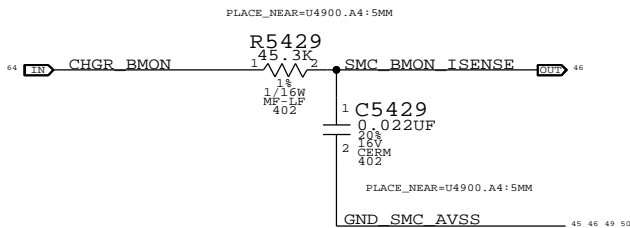
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
Rsense: 0.003 (R5410)
V across Rsense: 26.4 mV
Gain needed: 125x



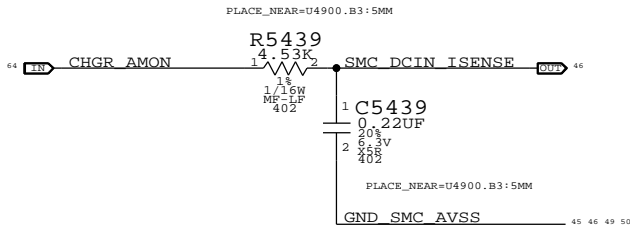
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x
Rsense: 0.010 (R7050)
Max Current Measured: 9.2 A

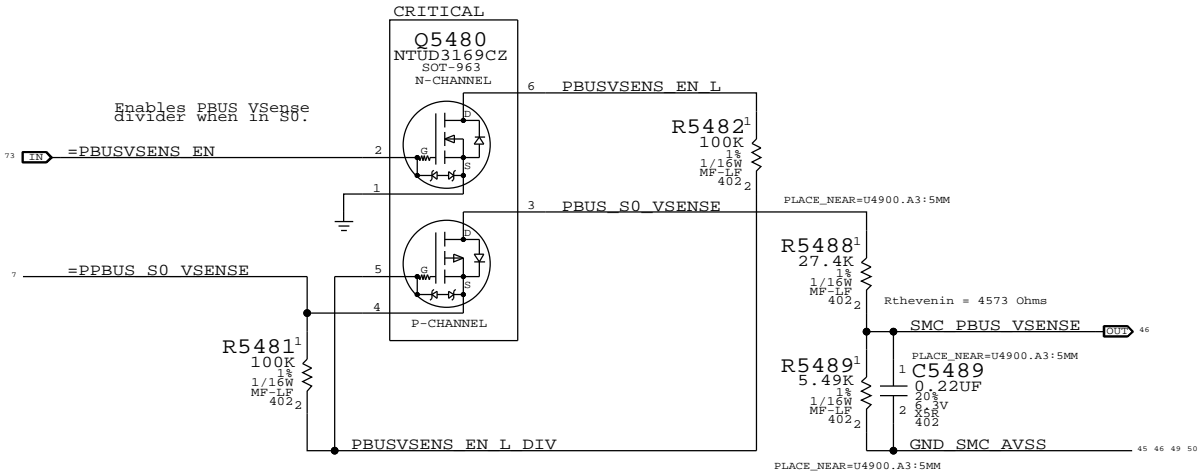


DC-In (AMON) Current Sense (ID0R)

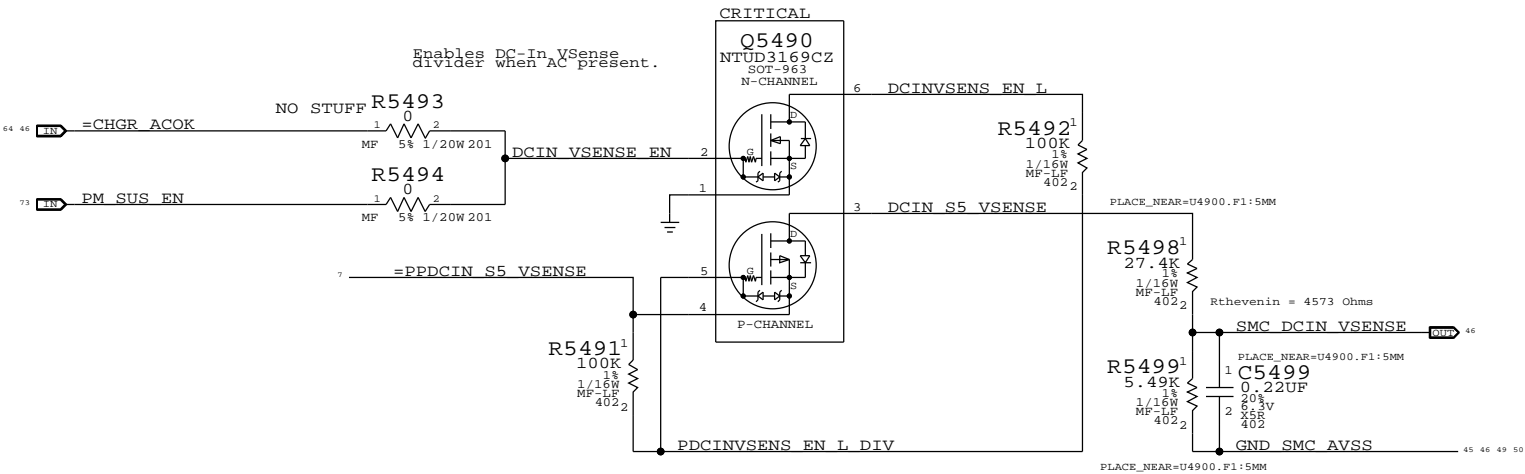
Charger Gain: 20x
Rsense: 0.020 (R7020)
Max Current Measured: 8.3 A



PBUS Voltage Sense & Enable (VP0R)

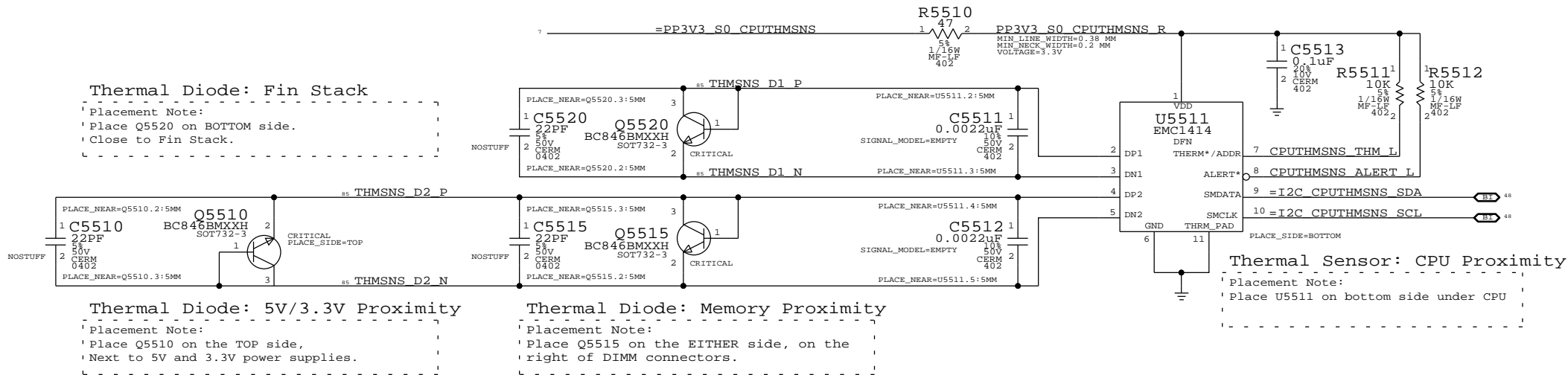


DC In Voltage Sense & Enable (VD0R)

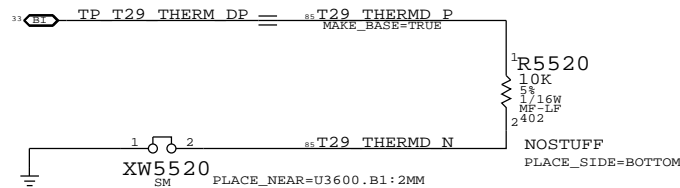


Thermal Sensor:
CPU Proximity, Fin Stack, Memory Proximity, 5V/3.3V Proximity

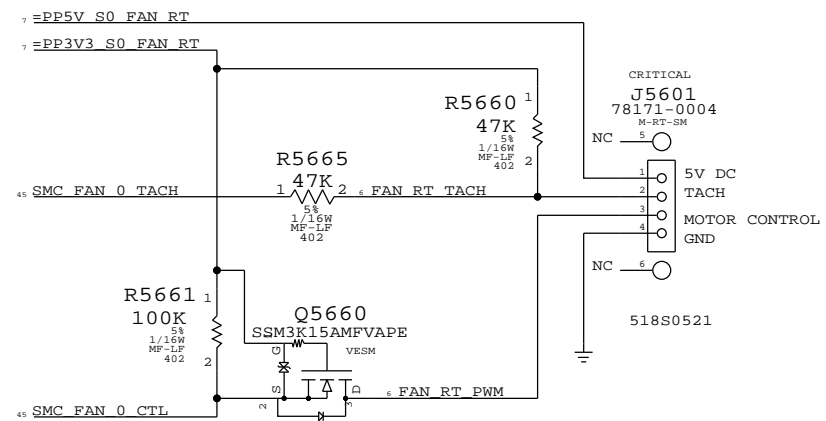
I2C Write: 0x98, I2C Read: 0x99




Thermal Sensor: T29 Die

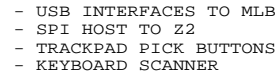


Note: Use GND pin B1 on U3600 for N leg.

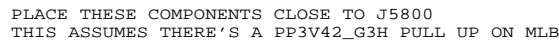


SYNC MASTER=K90I MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
Fan			
	Apple Inc.		DRAWING NUMBER 051-9058
			SIZE D
		REVISION 6.0.0	
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- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	100A	2.55 KOHM	0.0255 V	0.255E-6 W
		800A		0.204 V	16.32E-6 W
3V3 LDO	VDD	60mA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60mA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8mA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14mA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4mA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

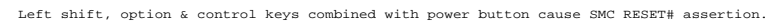
Keyboard Connector



SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

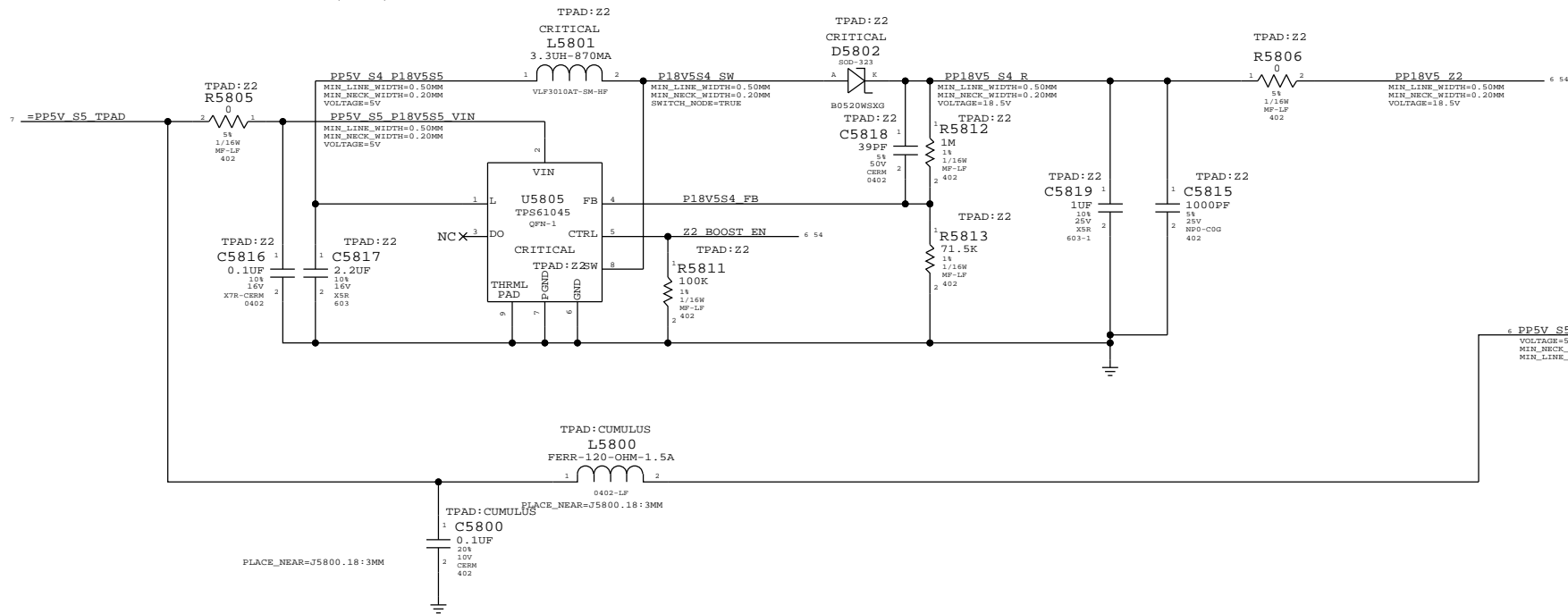
Left shift, option & control keys combined with power button cause SMC RESET# assertion.



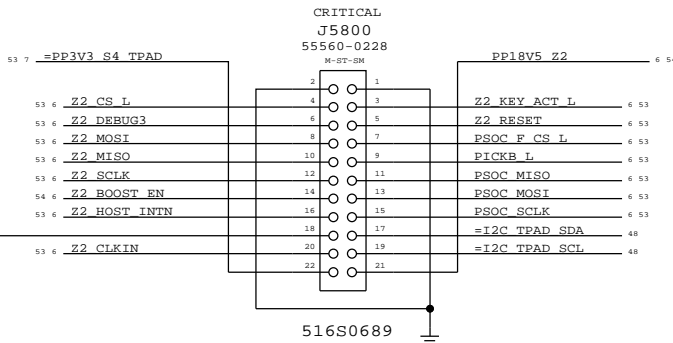
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:

- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED

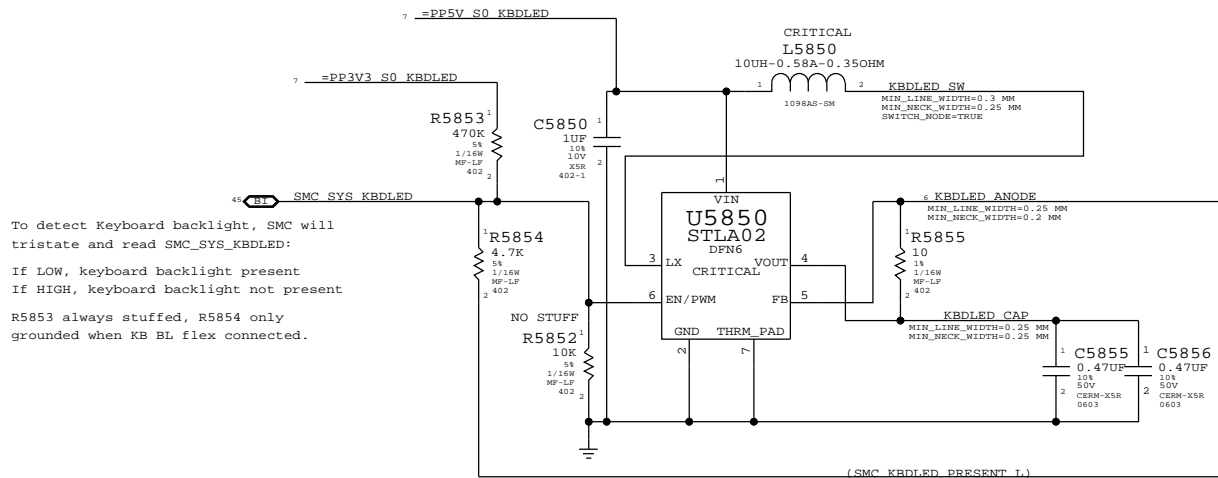


IPD Flex Connector

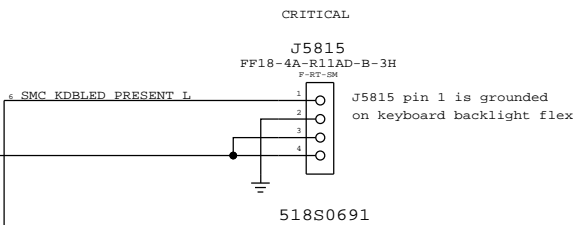


PIN 21 IS NC ON CUMULUS FLEX
PIN 18 IS NC ON Z2 FLEX


Keyboard Backlight Driver & Detection

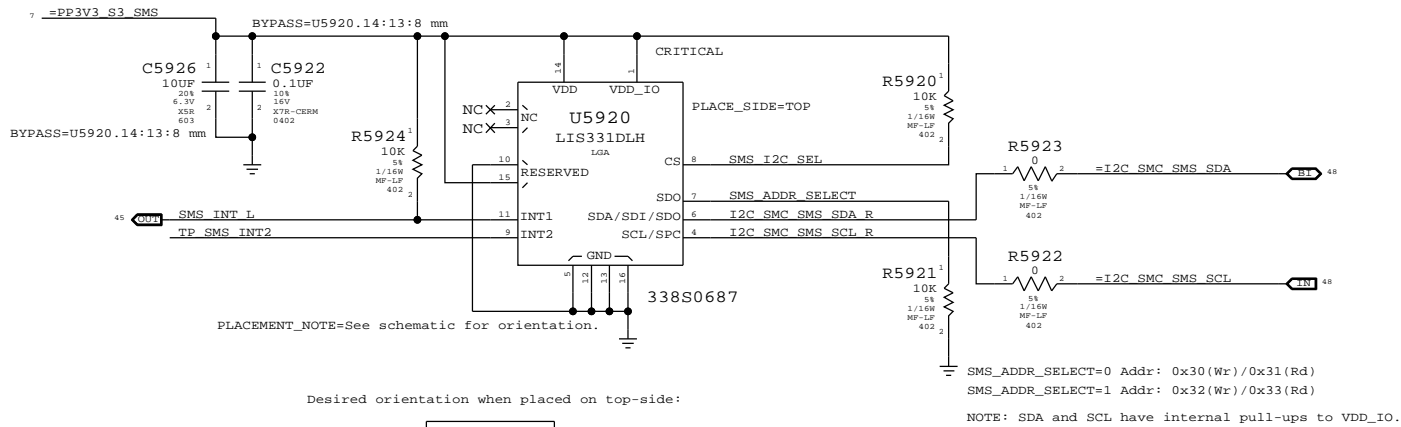


Keyboard Backlight Connector

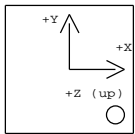


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:
If LOW, keyboard backlight present
If HIGH, keyboard backlight not present
R5853 always stuffed, R5854 only grounded when KB BL flex connected.

SYNC MASTER=JACK J30		SYNC DATE=09/28/2011	
PAGE TITLE			
WELLSPRING 2			
 Apple Inc.	DRAWING NUMBER	051-9058	SIZE
	REVISION	6.0.0	
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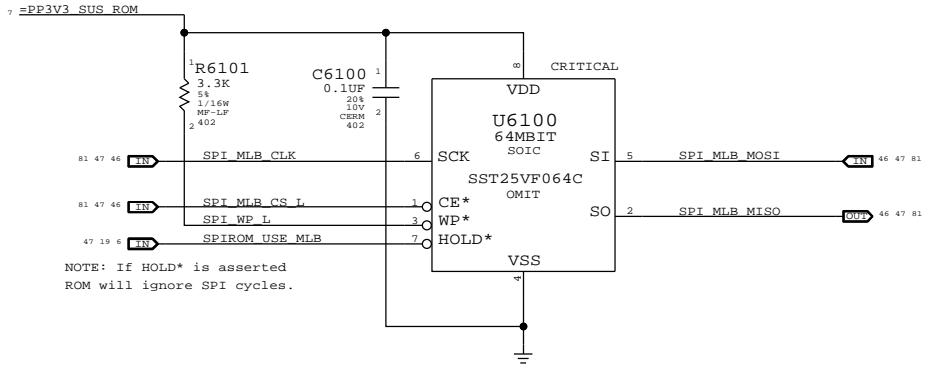


Desired orientation when placed on top-side:



Front of system

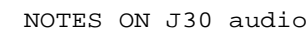
Circle indicates pin 1 location when placed in correct orientation





```
57 AUD DMIC CLK      — TP AUD DMIC CLK
                        — MAKE_BASE=TRUE

57 AUD GPIO 0       — TP AUD DMIC SDATA
                        — MAKE_BASE=TRUE
```

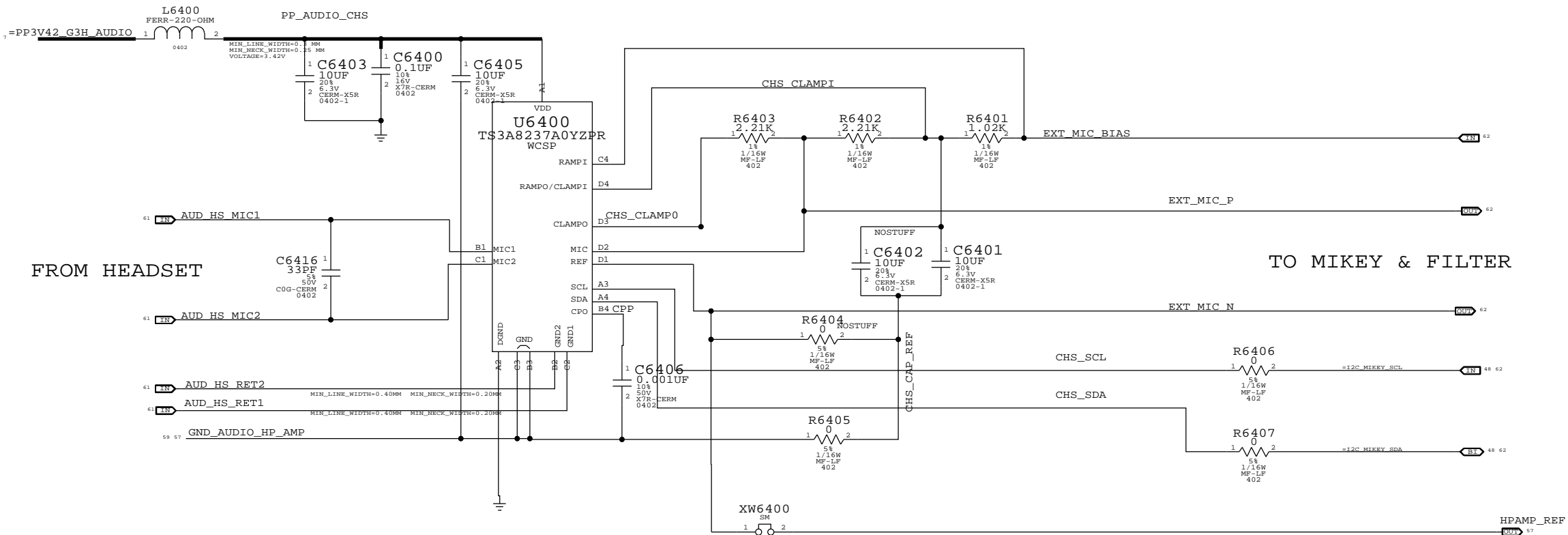
APPLE P/N 353S2281 as of July 2011



www.qdzbwx.com

SYNC MASTER-KAVITHA J30		SYNC DATE=07/25/2011	
PAGE TITLE			
AUDIO: CODEC/REGULATOR			
	Apple Inc.		DRAWING NUMBER 051-9058
			SIZE D
		REVISION 6.0.0	
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		SHEET	
		57 OF 86	

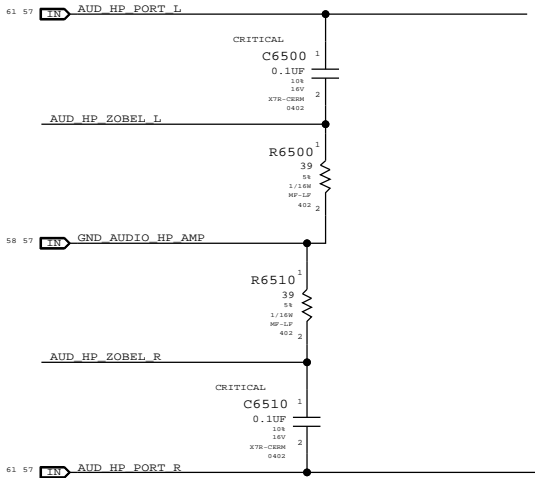
EXTERNAL (HEADSET) MIC INPUT CIRCUITRY APN:353S3066 as of July 2011



I2C ADDRESSES: CHS uses SMBus 0 connections

CHS	U6400	READ	0111	0111	0x77
CHS	U6400	WRITE	0111	0110	0x76

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

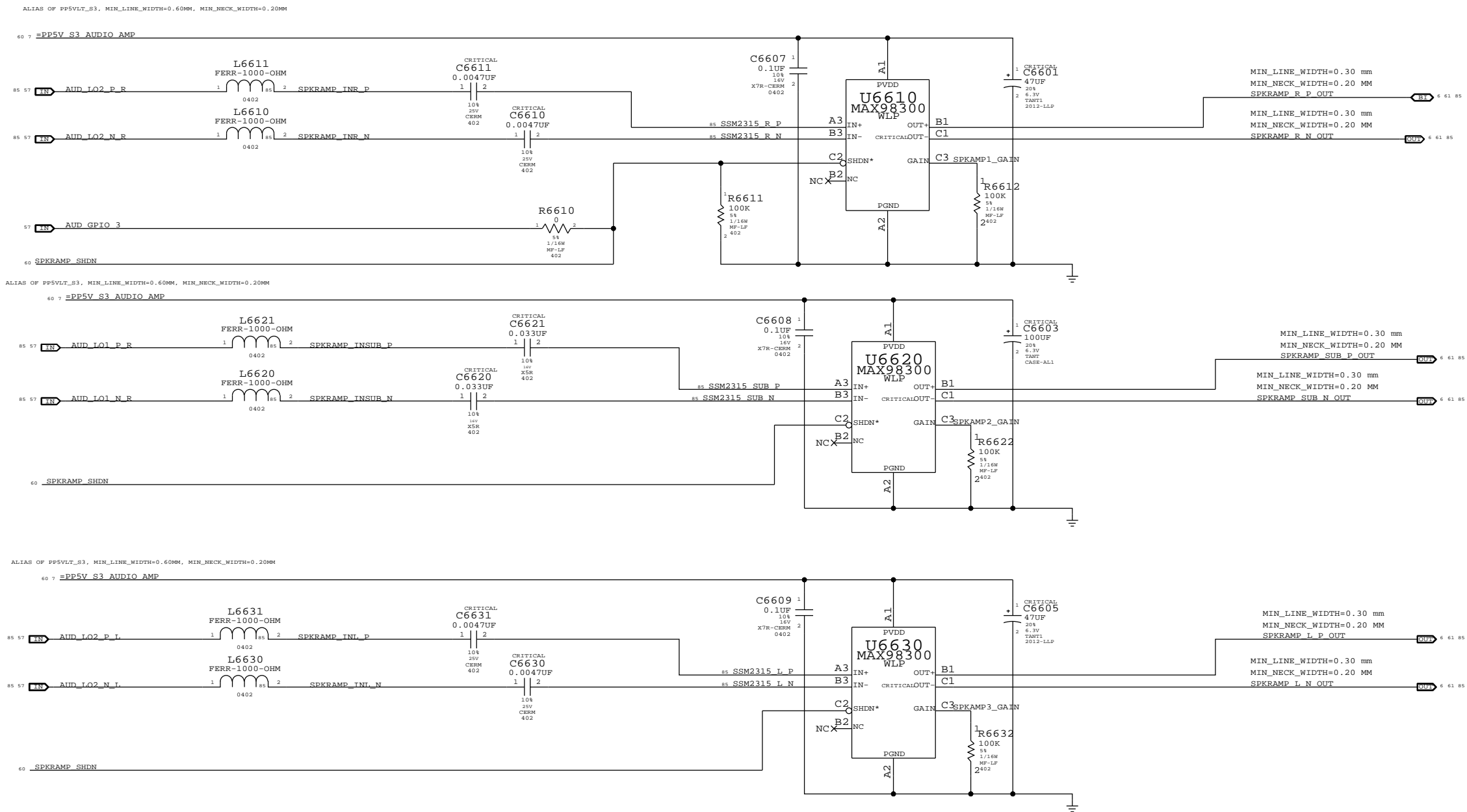


SATELLITE & SUB TWEETER AMPLIFIER

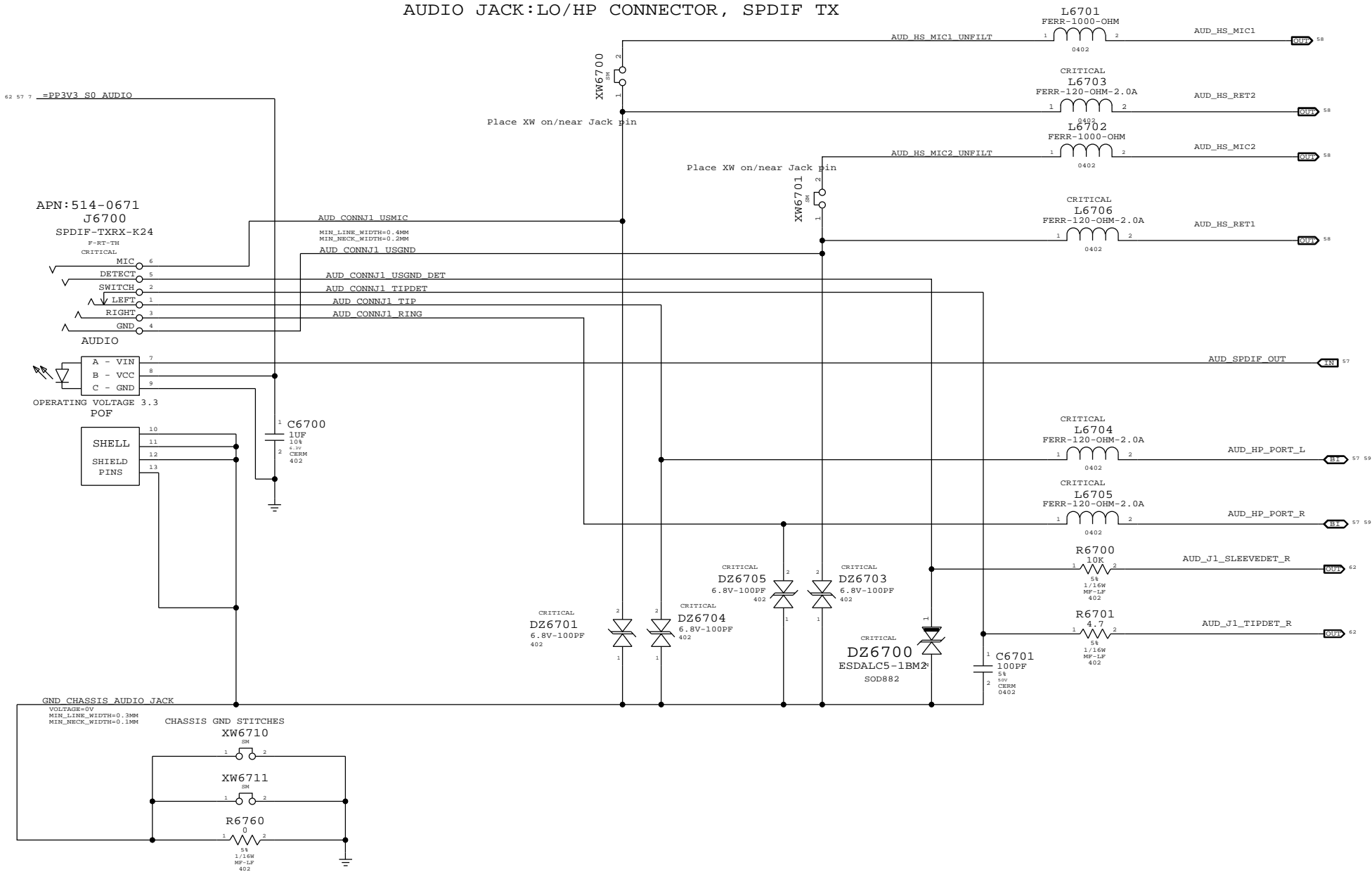
APN:353S2888 as of July 2011

SATELLITE	FC=1.2kHz typical
SUB	FC= 172 HZ typical
GAIN	3DB with Rin=28k typical

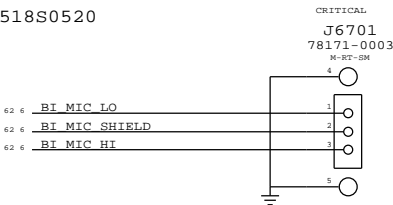
Gain Pin	Gain dB
Connect to VDD	12
Connect to VDD through 100k	9
Not connected	6
Connect to GND through 100k	3
Connect to GND	0



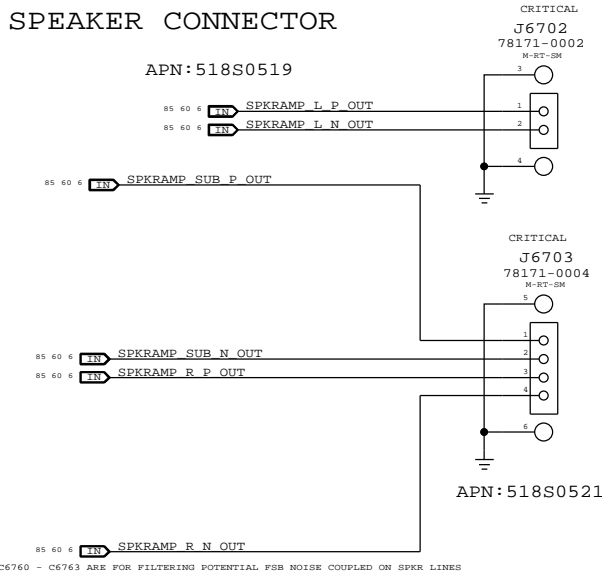
AUDIO JACK:LO/HP CONNECTOR, SPDIF TX




ANALOG MIC CONNECTOR
APN:518S0520



SPEAKER CONNECTOR



SYNC MASTER=DIRK J30		SYNC DATE=11/10/2011	
PAGE TITLE			
AUDIO: JACK			
 Apple Inc.		DRAWING NUMBER	051-9058
		SHEET	D
		REVISION	6.0.0
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CODEC OUTPUT SIGNAL PATHS

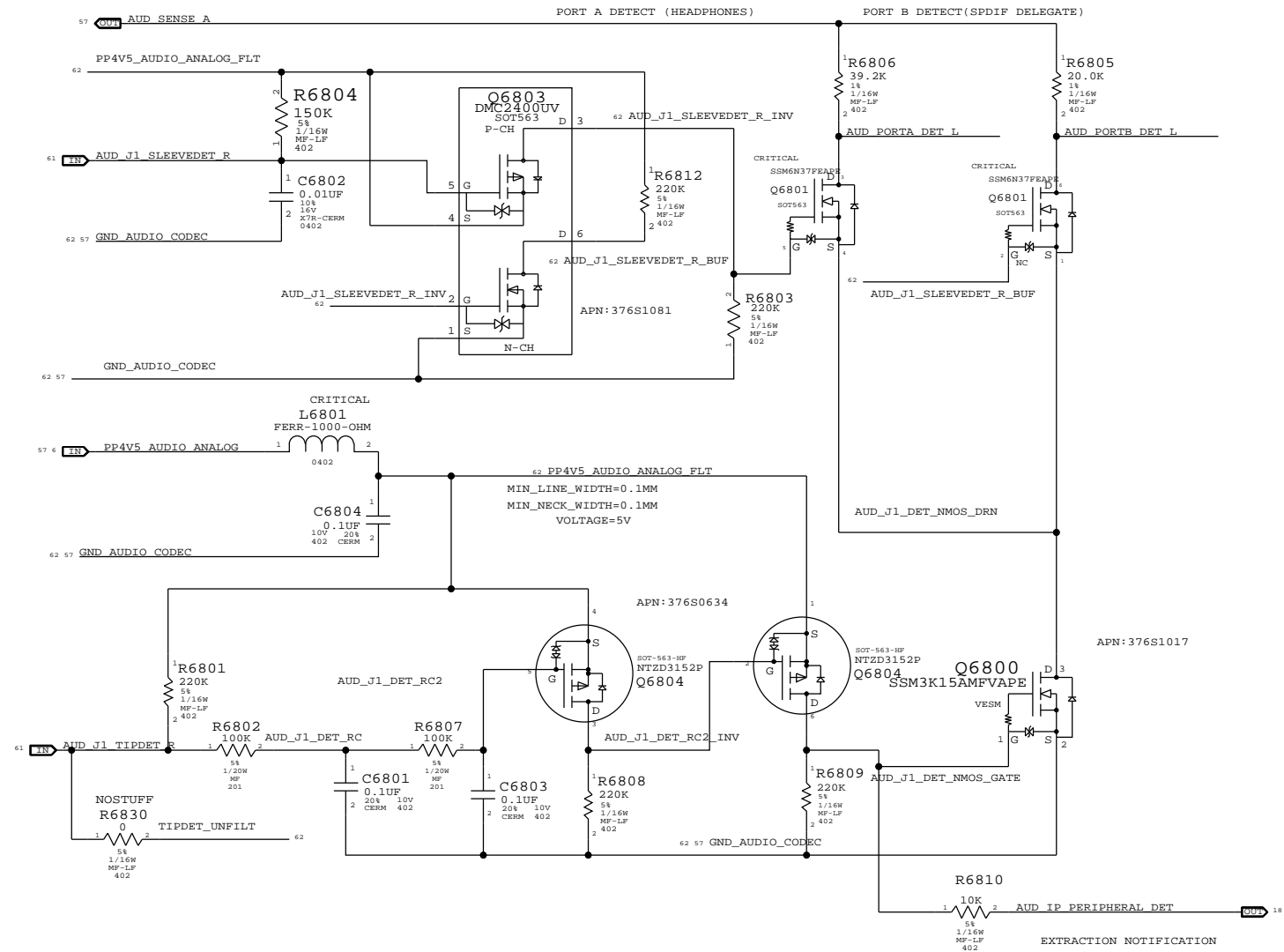
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

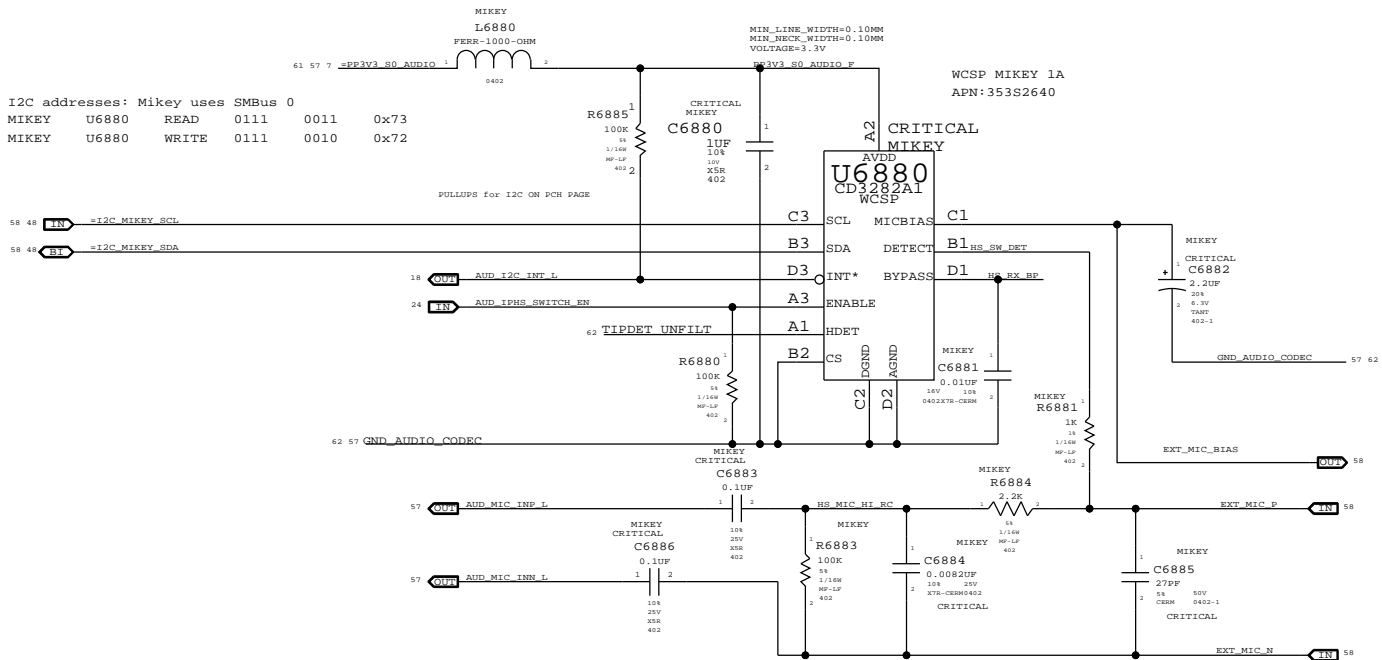
SOUTHBIDGE RESOURCES

FUNCTION	SYSTEM GPIO	SYSTEM INTERRUPT
AUD_IPMS_SWITCH_EN	PANTHER_POINT GPIO16	N/A
AUD_I2C_INT_L	N/A	PANTHER_POINT GPIO5/PIRQH
AUD_IP_PERIPHERAL_DET	N/A	PANTHER_POINT GPIO3/PIRQH

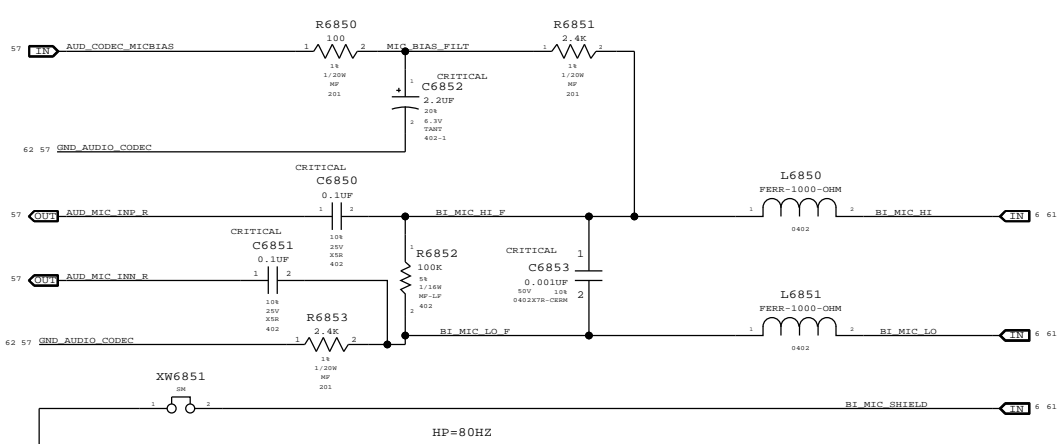



EXTRACTION NOTIFICATION

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ

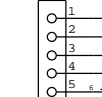


PORT B RIGHT(BUILT-IN MIC)

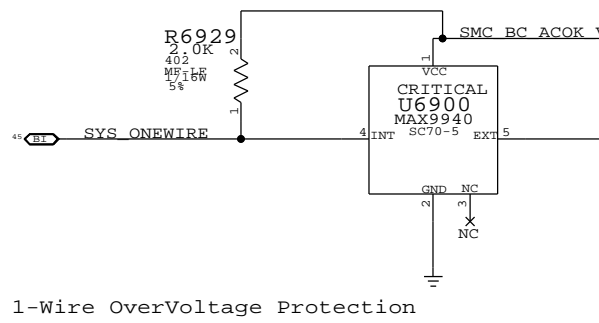


SYNC MASTER=DIRK J30		SYNC DATE=02/20/2012	
PAGE TITLE			
AUDIO:Apple Translators			
 Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	D
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MagSafe DC Power Jack

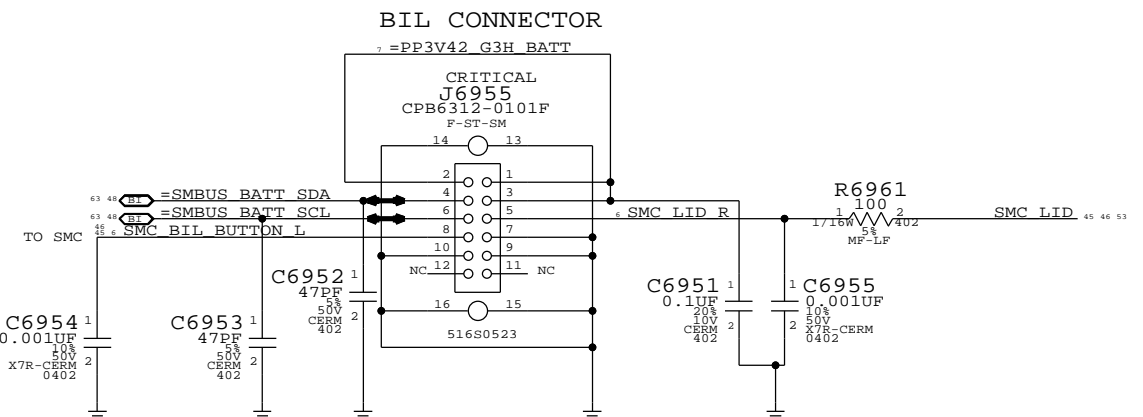
CRITICAL
J6900
78048-0573
M-RT-SM

518S0656

PP18V5 DCIN FUSE
MIN LINE WIDTH=0.25 mm
MIN NECK WIDTH=0.20 mm
VOLTAGE=18.5VC6905
0.01UF
20%
50V
CERM
0603CRITICAL
F6905
6AMP-24V
1206-1

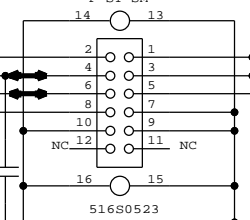
=PP18V5_DCIN_CONN 7 63

=PP3V42_G3H_ONEWIREPROT 7

C6908
0.1UF
20%
50V
CERM
402
PLACE_NEAR=U6901.5+1mmCRITICAL
U6901
TC7SZ08PEAPE S
SOT665

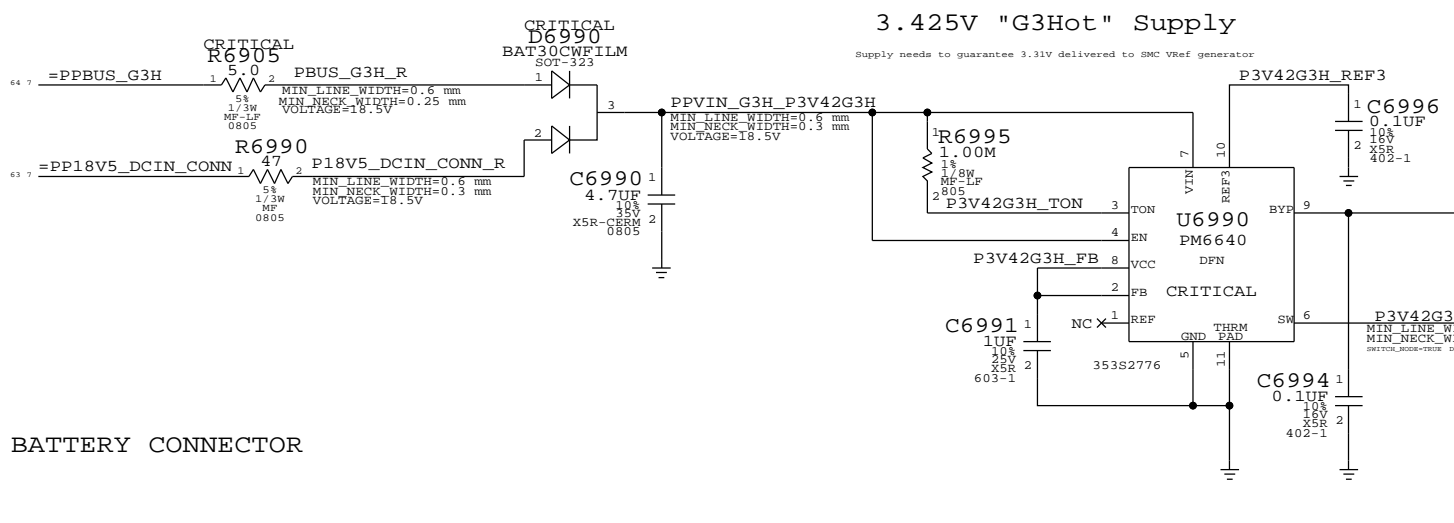
BIL CONNECTOR

=PP3V42_G3H_BATT 7

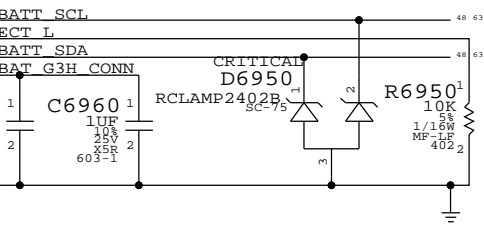
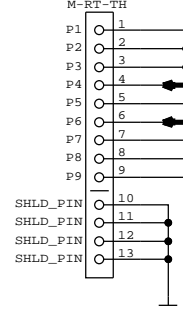
CRITICAL
J6955
CPB6312-0101F
F-ST-SM


3.425V "G3Hot" Supply

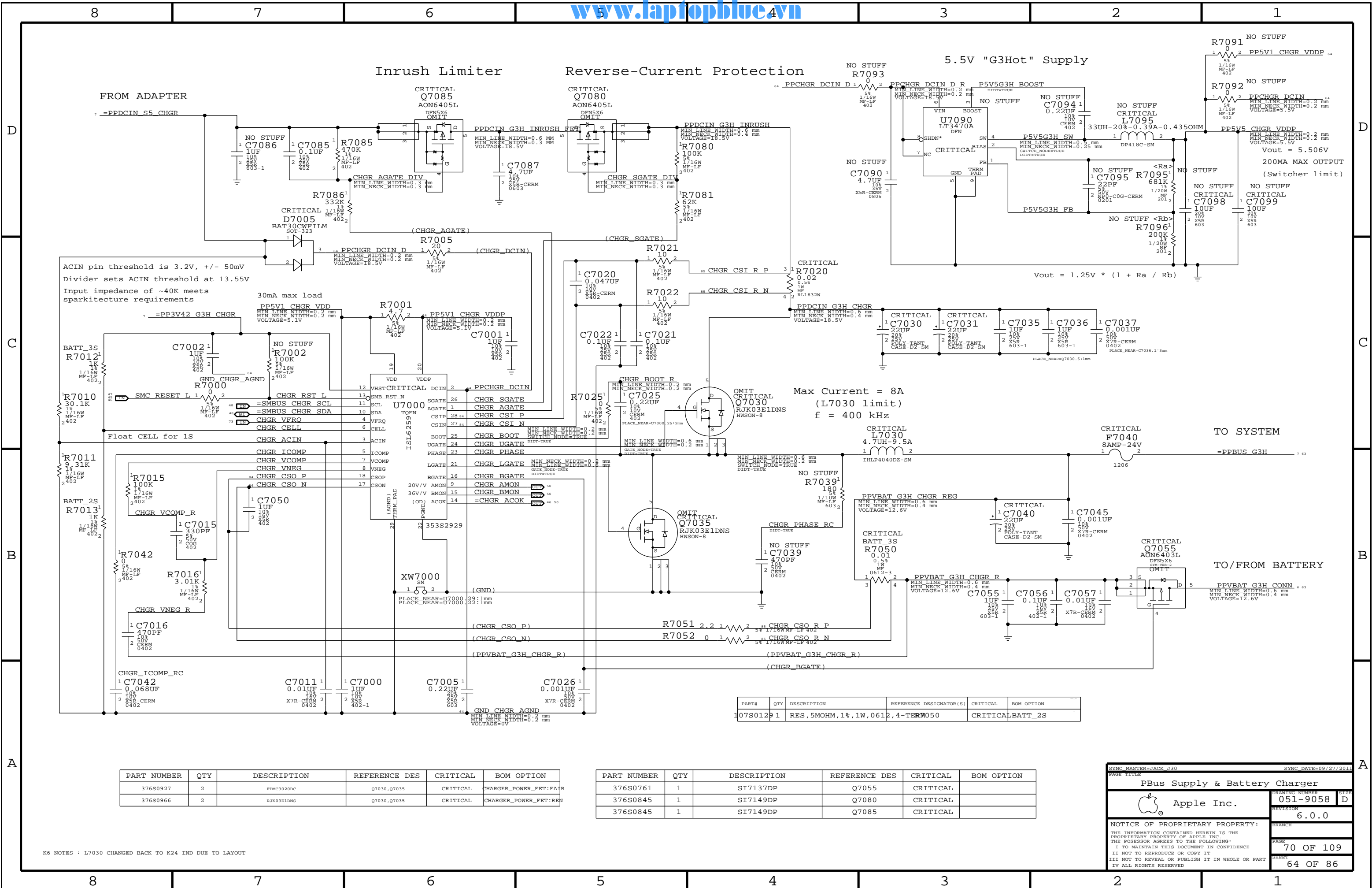
Supply needs to guarantee 3.31V delivered to SMC VRef generator



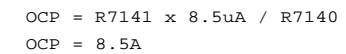
BATTERY CONNECTOR

518-0375
CRITICAL
J6950
BAT-K90-K91-K92
M-RT-TH

SYNC MASTER=JACK J30		SYNC DATE=07/29/2011	
PAGE TITLE			
DC-In & Battery Connectors			
 Apple Inc.		DRAWING NUMBER	051-9058
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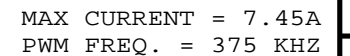



A |

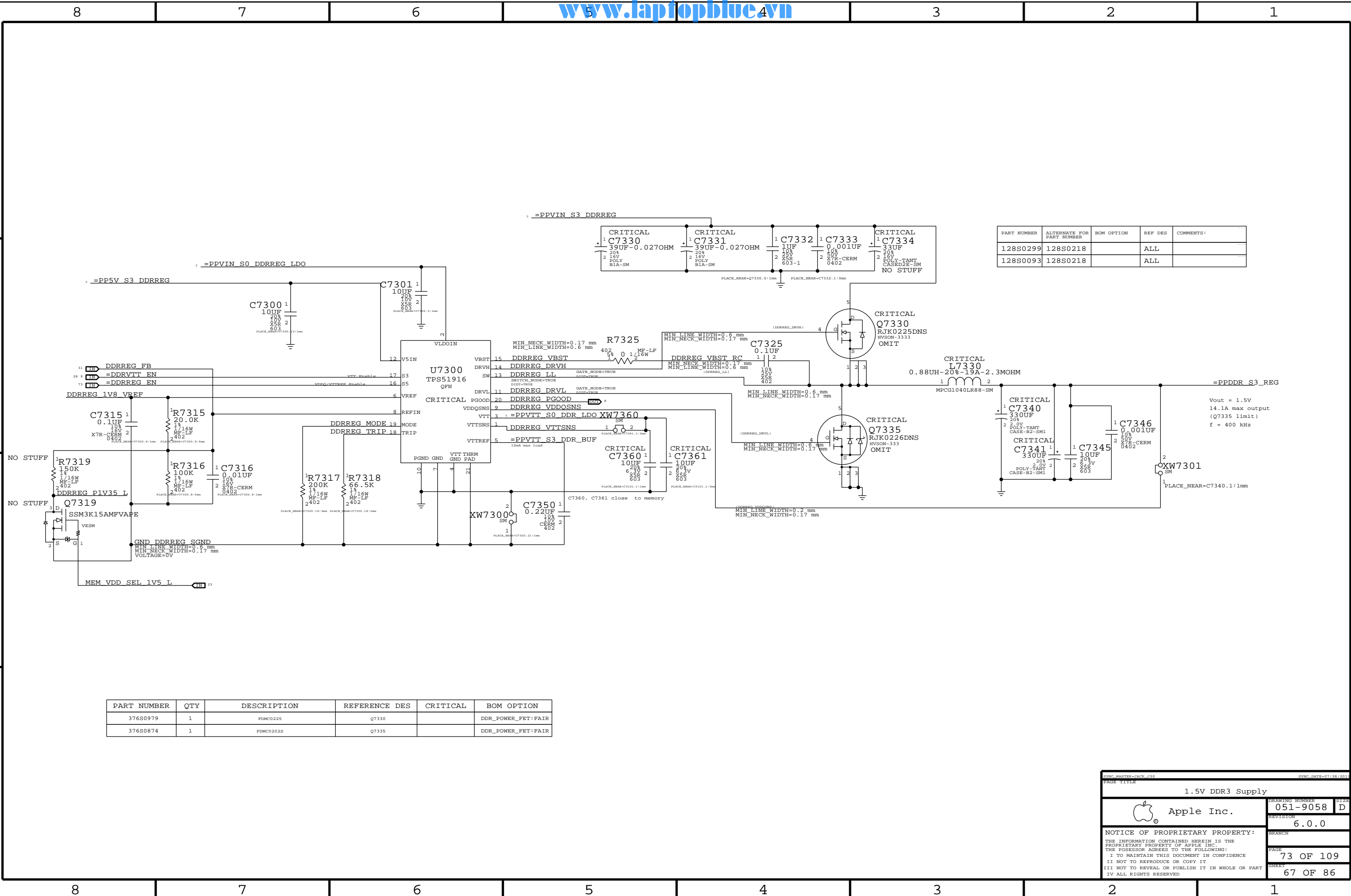


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1C	MSL95870A, PWM, 2BIT-VID, RMOT-S	ENSE, 20E7100	CRITICAL	

1

$$V_{OUT} = (2 * RC / RD) + 2$$


SYMC MASTER=JACK J30		SYMC DATE=08/27/2011	
PAGE TITLE			
5V/3.3V SUPPLY			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-9058	D
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		BRANCH	
		PAGE	
		SHEET	




PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0299	128S0218		ALL	
128S0093	128S0218		ALL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0979	1	FDMC0225	Q7330		DDR_POWER_FET:FAIR
376S0874	1	FDMC0202S	Q7335		DDR_POWER_FET:FAIR

SYMC PARTNERSHIP: 710

SYMC DATE: 07/28/2011

1.5V DDR3 Supply

 Apple Inc.

DRAWING NUMBER
051-9058

SIZE
D

REVISION
6.0.0

BRANCH

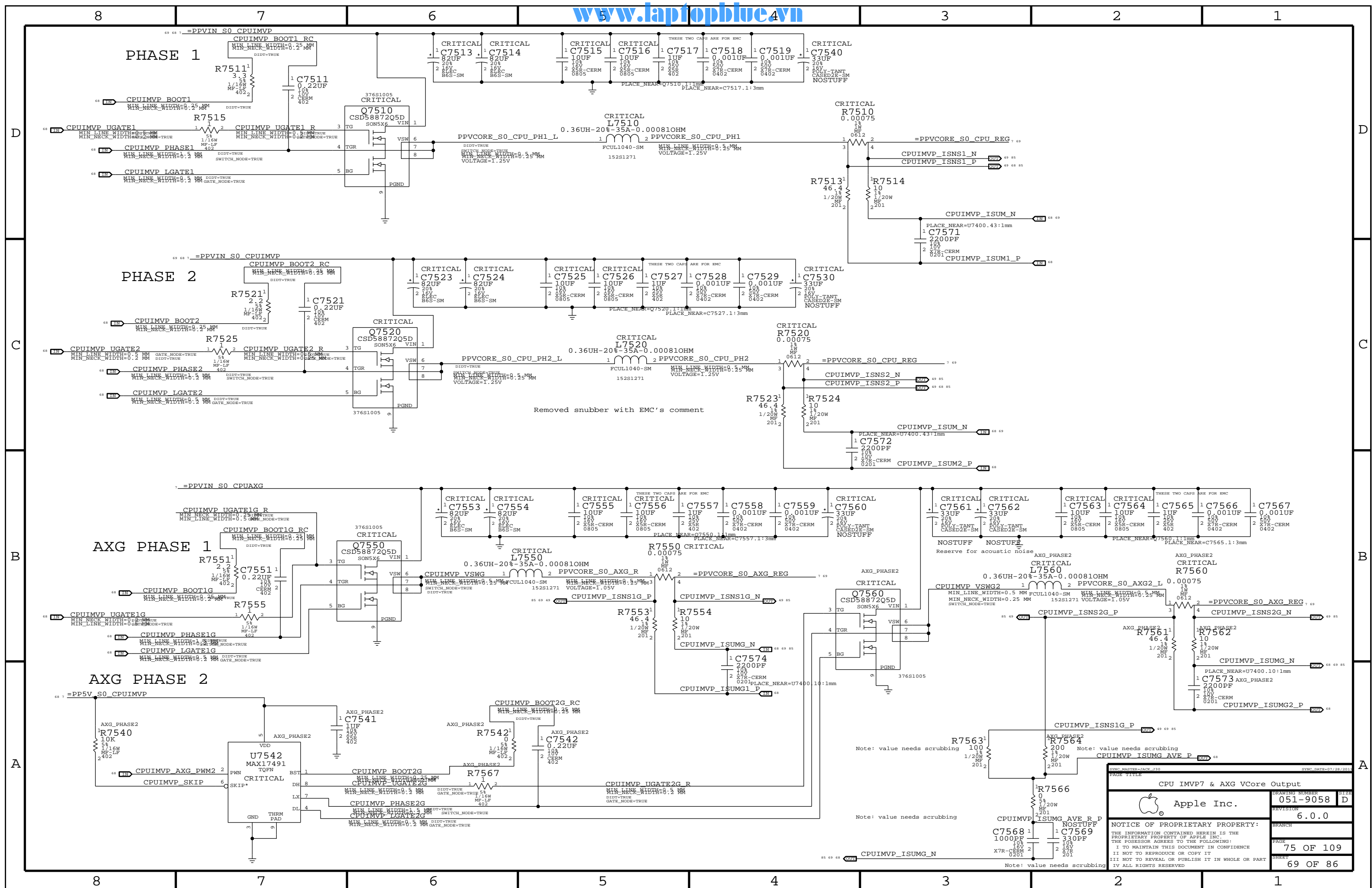
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73 OF 109

SHEET
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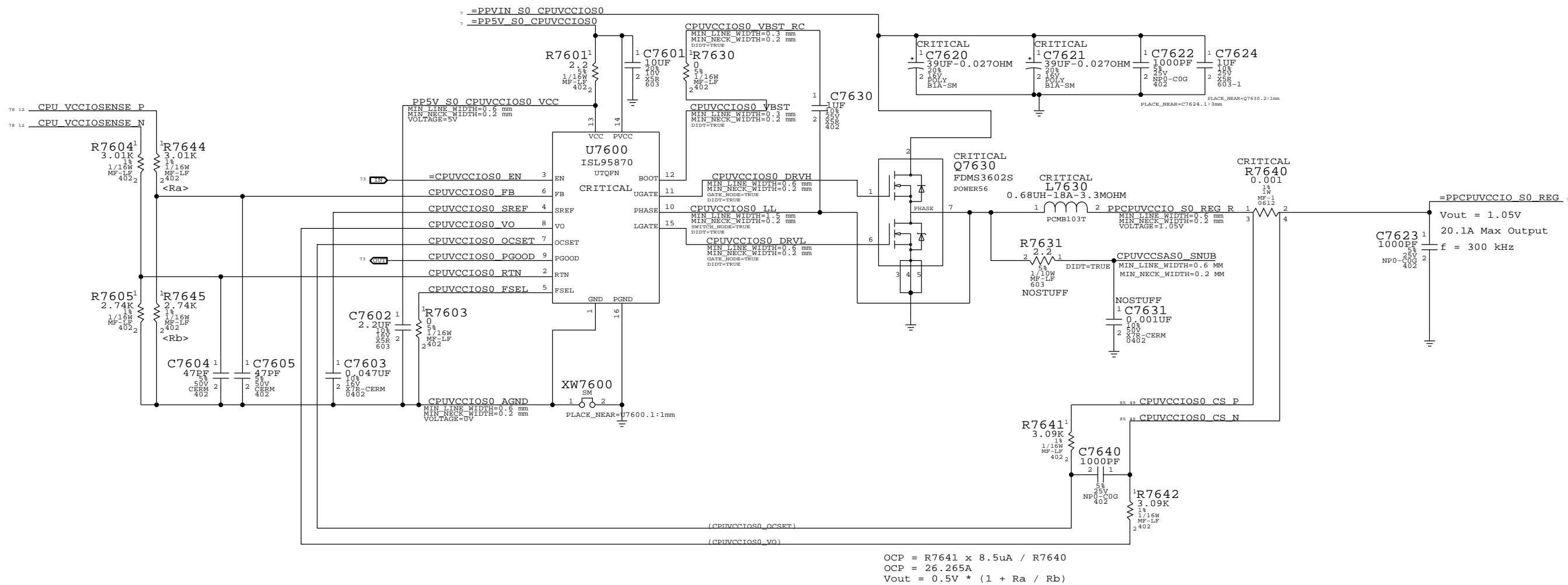
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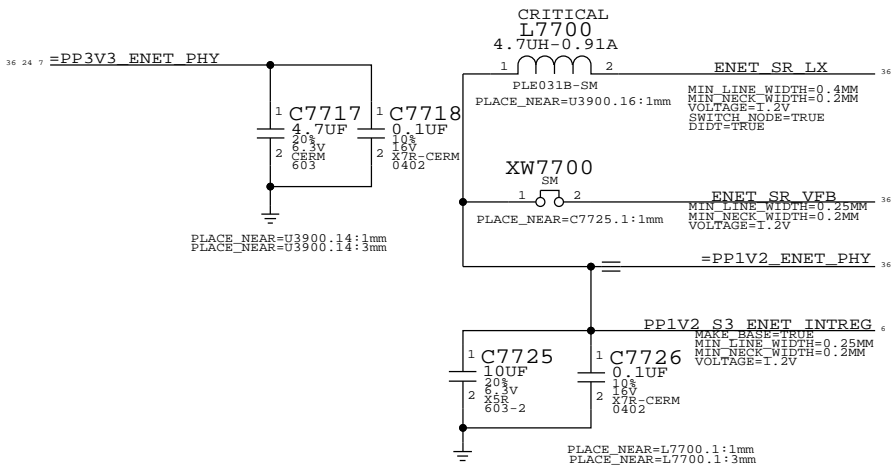
1



CPU VCCIO (1.05V S0) Regulator

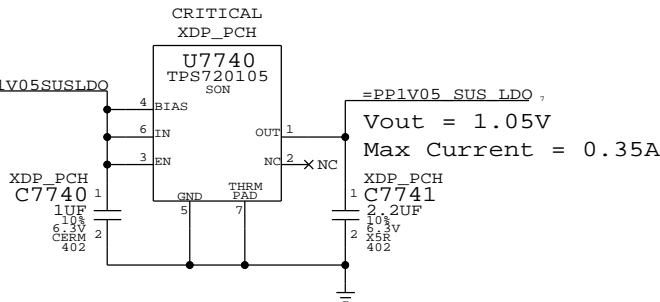


CAESAR IV 1.2V INT.VR CMPTS



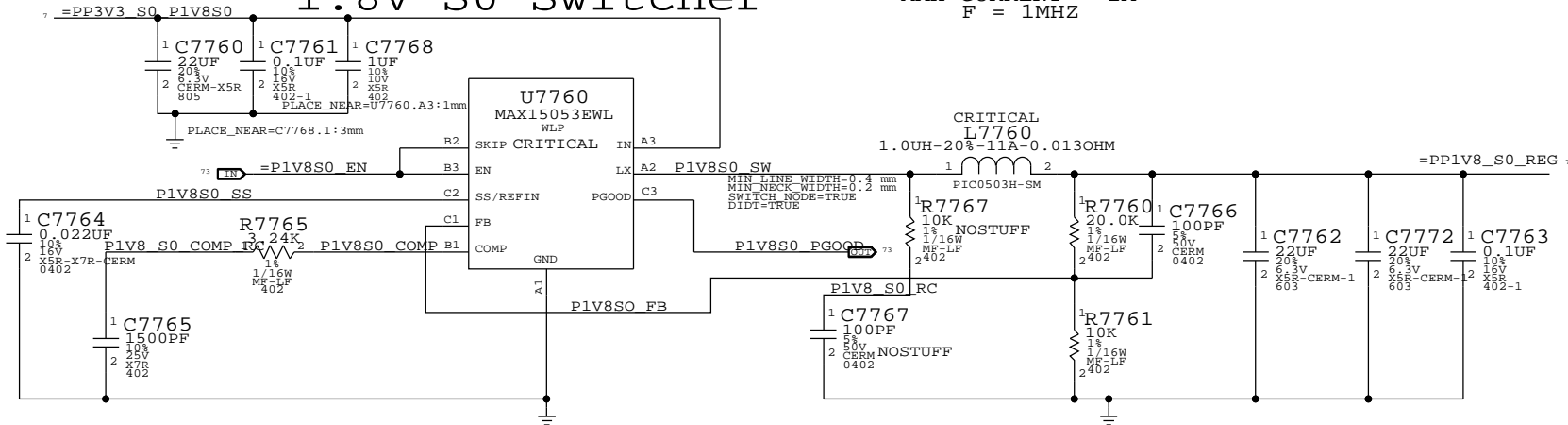
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



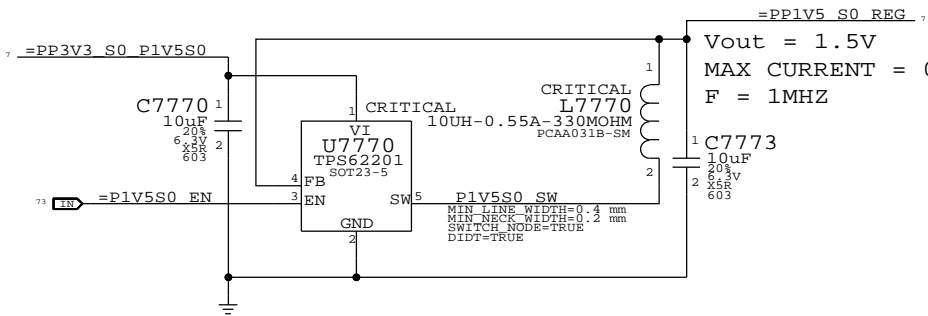
1.8V S0 Switcher

Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



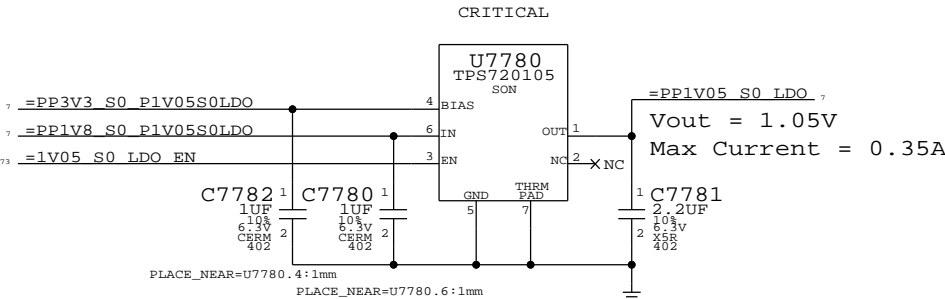
1.5V S0 Switcher


Vout = 1.5V
MAX CURRENT = 0.3A
F = 1MHZ

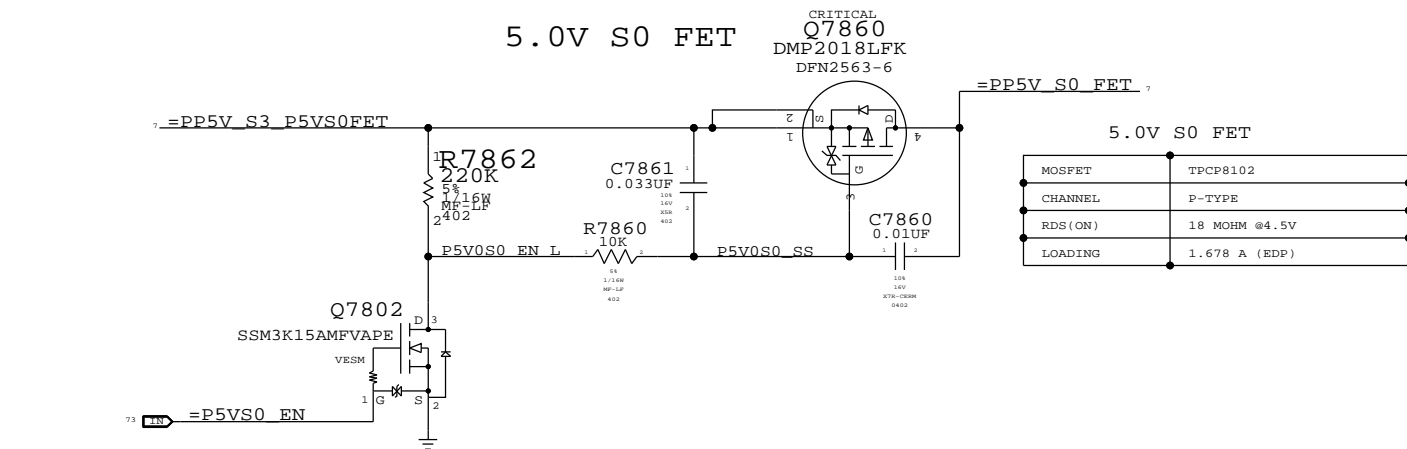
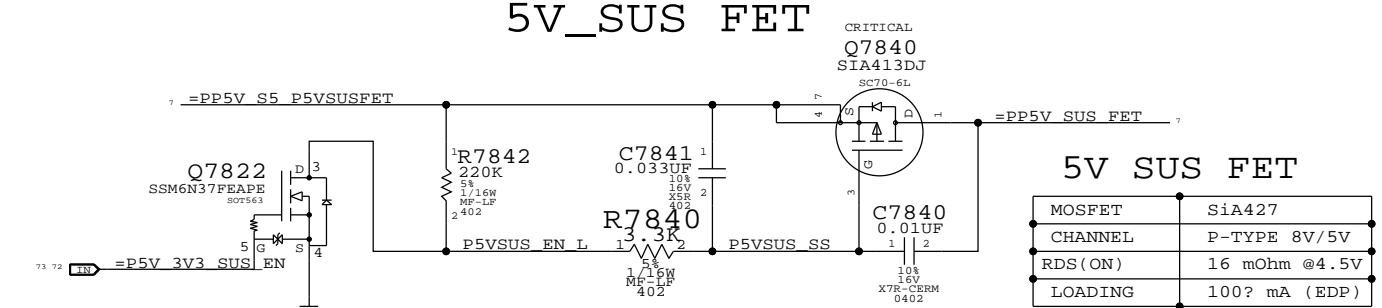
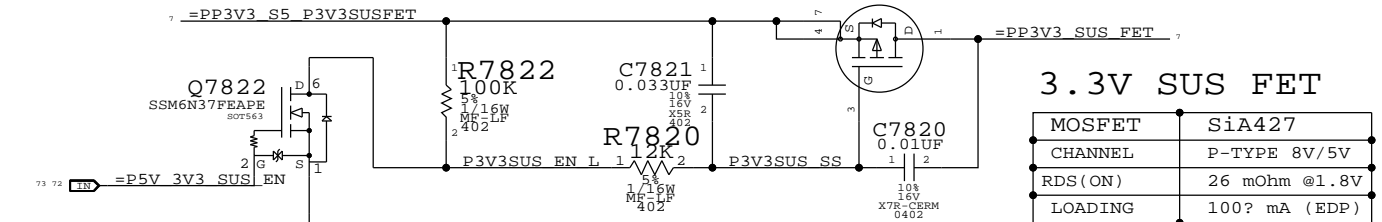
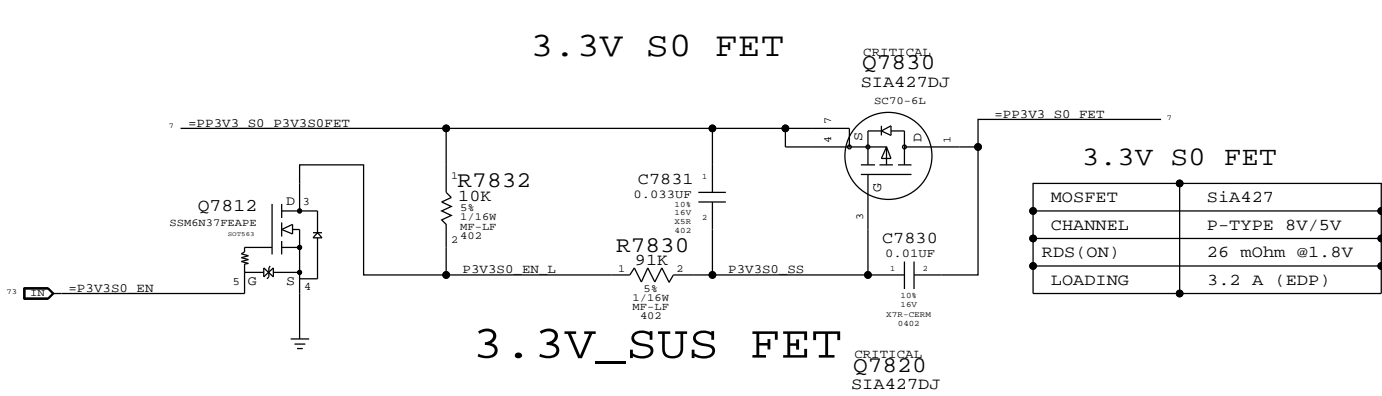
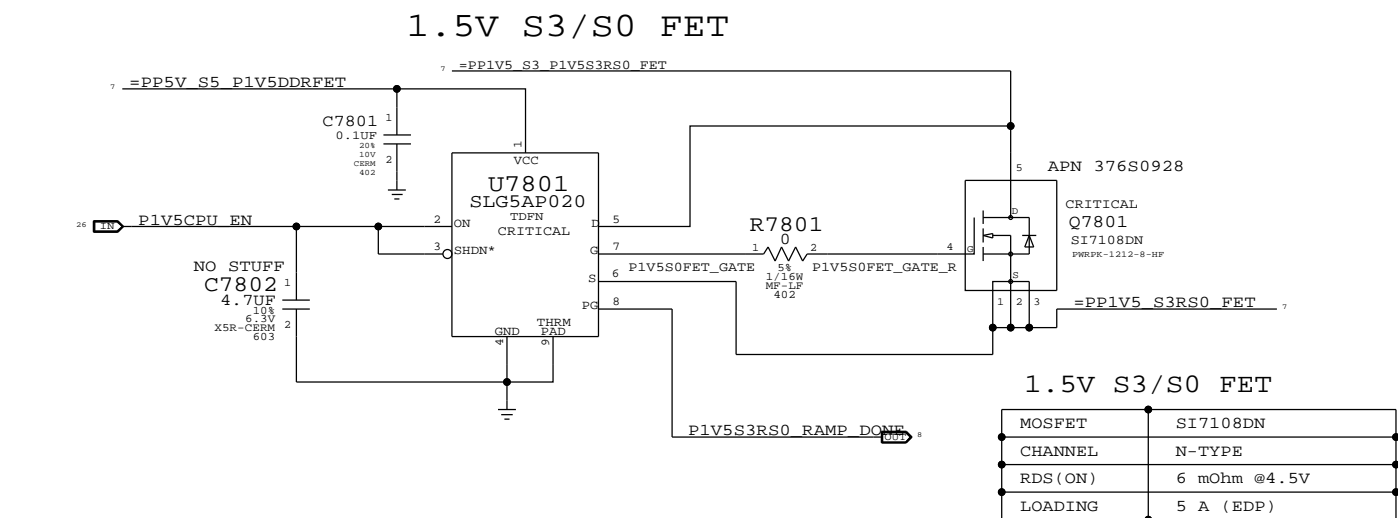
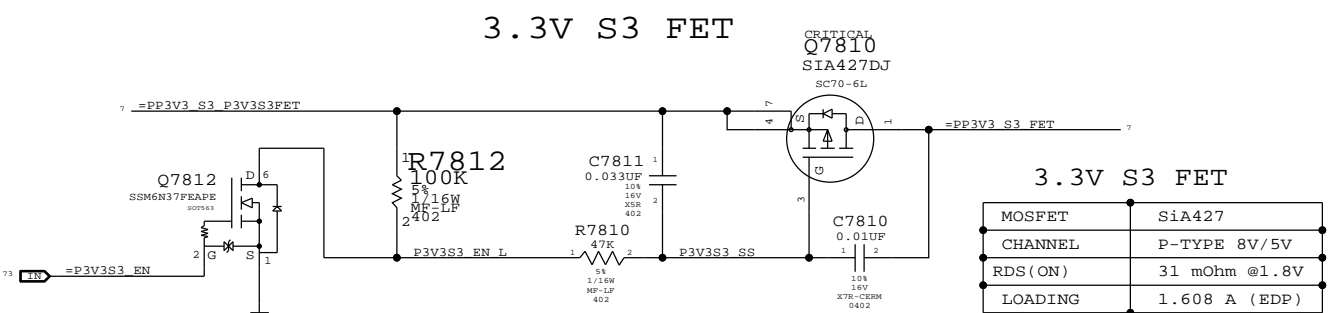
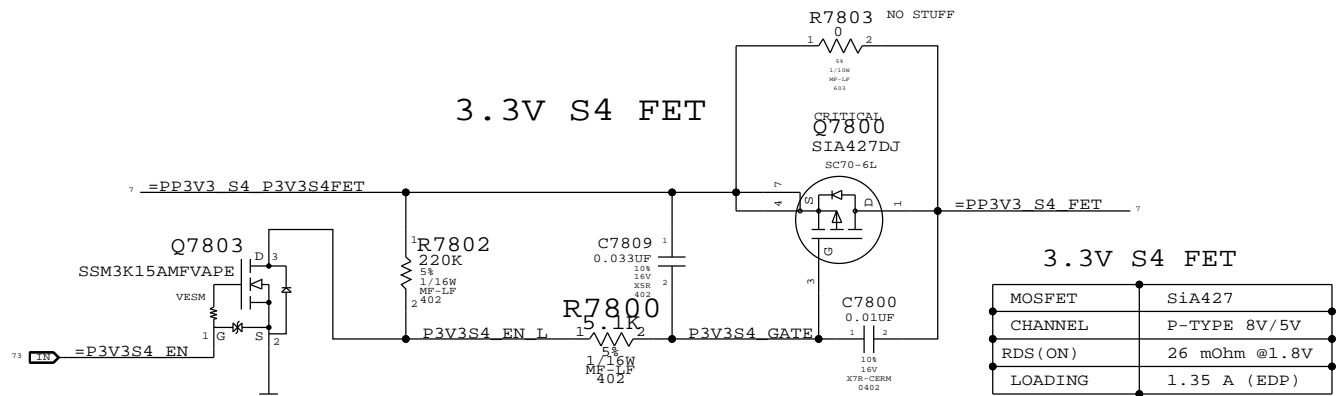


1.05V S0 LDO

Vout = 1.05V
Max Current = 0.35A



SYNC MASTER=JACK J30		SYNC DATE=07/28/2011	
PAGE TITLE			
Misc Power Supplies		DRAWING NUMBER	
 Apple Inc.		051-9058	
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S5 Rail Enables & PGOOD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

S0 Rail PGOOD (BJT Version)

S0 Rail PGOOD Circuitry

(ISL Version in development)

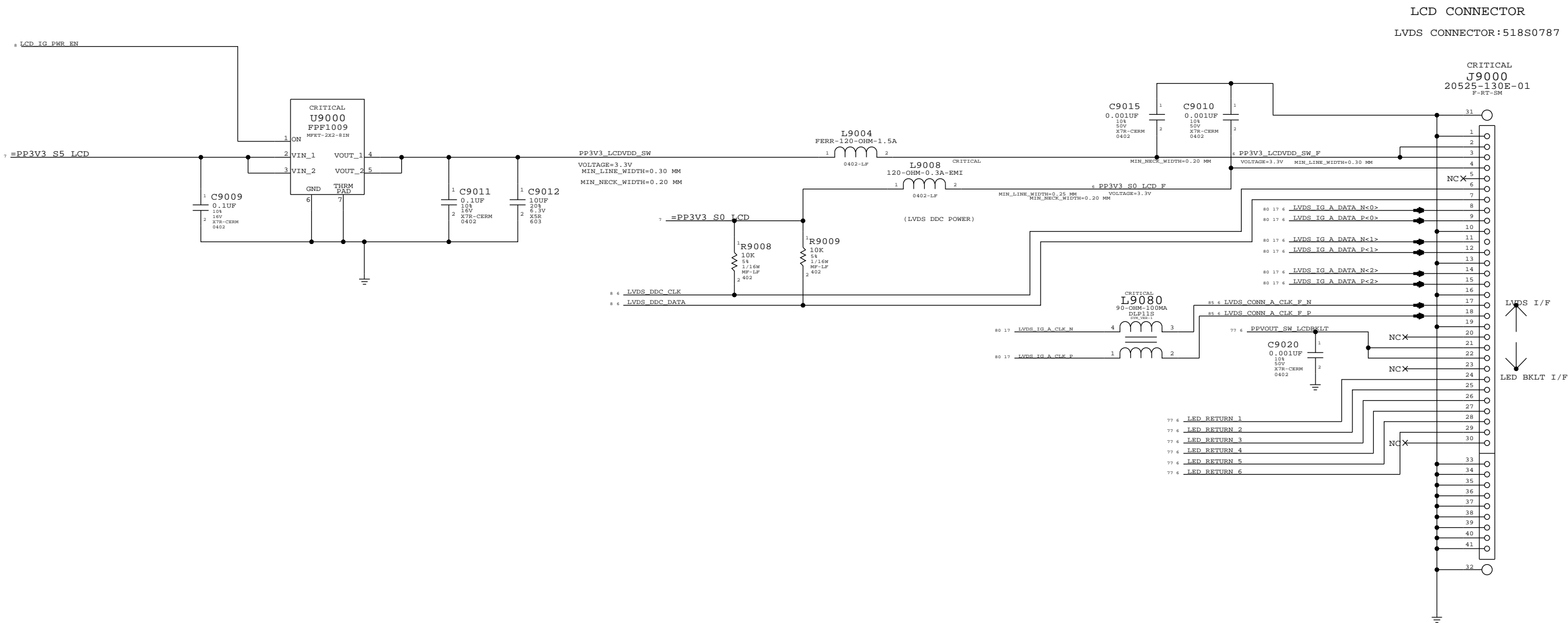
ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

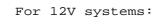
3.3V ENET FET

WLAN Enable Generation

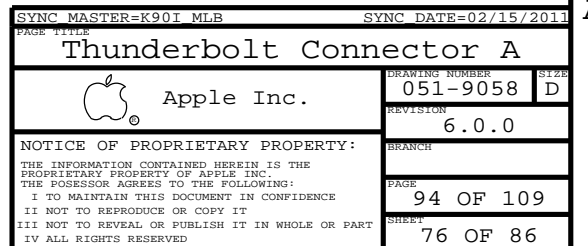
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.




7 =PP3V3 S4 TBTAPWRSW



	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)



10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=T31 ML#		SYNC DATE=07/08/2013	
PAGE TITLE			
LCD Backlight Driver			
 Apple Inc.		DRAWING NUMBER 051-9058	
		SIZE D	
		REVISION 6.0.0	
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	20 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SPF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_PCH_TX2TX	*	=3x_DIELECTRIC	?	PCIE_PCH_TX2TX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_PCH_TX2RX	*	=4x_DIELECTRIC	?	PCIE_PCH_TX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_PCH_RX2RX	*	=3x_DIELECTRIC	?	PCIE_PCH_RX2RX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_PCH_RX2TX	*	=4x_DIELECTRIC	?	PCIE_PCH_RX2TX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_PCH_2OTHER	*	=3x_DIELECTRIC	?	PCIE_PCH_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	*_PCH_TX	*	PCIE_PCH_TX2TX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_PCH_TX2RX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_PCH_RX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_PCH_RX2TX
PCIE_PCH_TX	*	*	PCIE_PCH_2OTHER
PCIE_PCH_RX	*	*	PCIE_PCH_2OTHER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DMI_S2N	PCIE_85D	PCIE_PCH_TX	DMI_S2N P<3:0>	9 17
DMI_S2N	PCIE_85D	PCIE_PCH_TX	DMI_S2N N<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE_PCH_RX	DMI_N2S P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE_PCH_RX	DMI_N2S N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE_PCH_RX	FDI_DATA P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE_PCH_RX	FDI_DATA N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	CPU_COMP	CPU_PECI	10 19 46
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM MEM PWRGD	10 17 26
	CPU_50S	CPU_ITP	XDP DBRESET L	10 23 24
	CPU_50S	CPU_ITP	XDP CPU PRDY L	10 23
	CPU_50S	CPU_ITP	XDP CPU PREQ L	10 23
	CPU_50S	CPU_AGTL	PM EXT TS L<0>	
	CPU_50S	CPU_AGTL	PM EXT TS L<1>	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP<2>	10
	CPU_50S	CPU_ITP	CPU CFG<11..0>	9 23
CPU_CATERER_L	CPU_50S	CPU_AGTL	CPU CATERER_L	10 45
	CPU_50S	CPU_AGTL	CPU VCCIO_SEL	8 12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L	10 45 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	10 19 23
PM_THERMTRIP_L	CPU_50S	CPU_8MIL	PM THERMTRIP L	10 19 46
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI CLK100M CPU P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI CLK100M CPU N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU CLK100M P	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU CLK100M N	10 16
ITPXDP_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP CLK100M P	16 23
ITPXDP_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP CLK100M N	16 23
XDP_CPU_CLK100M_P	CLK_PCIE_90D	CLK_PCIE	XDP CPU CLK100M_P	23
XDP_CPU_CLK100M_N	CLK_PCIE_90D	CLK_PCIE	XDP CPU CLK100M_N	23
EDP_COMP	CPU_27P4S	CPU_COMP	EDP COMP	9
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU PEG COMP	9
XDP_TDI	CPU_50S	CPU_ITP	XDP CPU TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP CPU TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP CPU TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP CPU TCK	10 23
XDP_TEST_L	CPU_50S	CPU_ITP	XDP CPU TEST_L	10 23
XDP_BFM_L	CPU_50S	CPU_ITP	XDP BFM L<3..0>	10 23
XDP_BFM_R_L	CPU_50S	CPU_ITP	CPU CFG<15..12>	9 23
(FSB_CPUURST_L)	CPU_50S	CPU_ITP	XDP CPUURST_L	23
CPU_VCCXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_P	12 68
CPU_VCCXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCIOSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCIOSENSE_N	12 70
CPU_VCCXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU AXG SENSE_P	12 68
CPU_VCCXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU AXG SENSE_N	12 68
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VDDO_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VDDO_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L	12 68
CPU_SVIDCLK	CPU_50S	CPU_COMP	CPU_VIDSClk	12 68
CPU_SVIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT	12 68

CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
CPU Constraints			
 Apple Inc.	DRAWING NUMBER	051-9058	SIZE D
	REVISION	6.0.0	
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL10	N	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL10	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	11 27
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	11 27
MEM_A_CMT	MEM_37S	MEM_CTRL	MEM A CKE<3..0>	11 27
MEM_A_CMT	MEM_37S	MEM_CTRL	MEM A CS L<3..0>	11 27
MEM_A_CMT	MEM_37S	MEM_CTRL	MEM A ODT<3..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	11 27
MEM_A_DQ_BVTE0	MEM_50S	MEM_DATA	MEM A DQ<7..0>	11 28
MEM_A_DQ_BVTE1	MEM_50S	MEM_DATA	MEM A DQ<15..8>	11 28
MEM_A_DQ_BVTE2	MEM_50S	MEM_DATA	MEM A DQ<23..16>	11 28
MEM_A_DQ_BVTE3	MEM_50S	MEM_DATA	MEM A DQ<31..24>	11 28
MEM_A_DQ_BVTE4	MEM_50S	MEM_DATA	MEM A DQ<39..32>	11 28
MEM_A_DQ_BVTE5	MEM_50S	MEM_DATA	MEM A DQ<47..40>	11 28
MEM_A_DQ_BVTE6	MEM_50S	MEM_DATA	MEM A DQ<55..48>	11 28
MEM_A_DQ_BVTE7	MEM_50S	MEM_DATA	MEM A DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	11 29
MEM_B_CMT	MEM_37S	MEM_CTRL	MEM B CKE<3..0>	11 29
MEM_B_CMT	MEM_37S	MEM_CTRL	MEM B CS L<3..0>	11 29
MEM_B_CMT	MEM_37S	MEM_CTRL	MEM B ODT<3..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	11 29
MEM_B_DQ_BVTE0	MEM_50S	MEM_DATA	MEM B DQ<7..0>	11 28
MEM_B_DQ_BVTE1	MEM_50S	MEM_DATA	MEM B DQ<15..8>	11 28
MEM_B_DQ_BVTE2	MEM_50S	MEM_DATA	MEM B DQ<23..16>	11 28
MEM_B_DQ_BVTE3	MEM_50S	MEM_DATA	MEM B DQ<31..24>	11 28
MEM_B_DQ_BVTE4	MEM_50S	MEM_DATA	MEM B DQ<39..32>	11 28
MEM_B_DQ_BVTE5	MEM_50S	MEM_DATA	MEM B DQ<47..40>	11 28
MEM_B_DQ_BVTE6	MEM_50S	MEM_DATA	MEM B DQ<55..48>	11 28
MEM_B_DQ_BVTE7	MEM_50S	MEM_DATA	MEM B DQ<63..56>	11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	11 28

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines per Huron River SFF DG rev1.0 (#438297).

DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.

DQ to DQS matching per byte lane should be within 0.127mm.

DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].

CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.

CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.

A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.

DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.

Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.

SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_PCH	*	=3x_DIELECTRIC	?	DP_PCH	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_PCH_TX	*	=3x_DIELECTRIC	?	DP_PCH_TX	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS_PCH_TX	*	=3x_DIELECTRIC	?	LVDS_PCH_TX	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_PCH_TX	*	=3x_DIELECTRIC	?	SATA_PCH_TX	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_PCH_RX	*	=3x_DIELECTRIC	?	SATA_PCH_RX	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?				

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_PCH_TX2TX	*	=4x_DIELECTRIC	?	SATA3_PCH_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_PCH_TX2RX	*	=5x_DIELECTRIC	?	SATA3_PCH_TX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_PCH_RX2RX	*	=4x_DIELECTRIC	?	SATA3_PCH_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_PCH_RX2TX	*	=5x_DIELECTRIC	?	SATA3_PCH_RX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_PCH_2OTHER	*	=4x_DIELECTRIC	?	SATA3_PCH_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	*_PCH_TX	*	SATA3_PCH_TX2TX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_PCH_TX2RX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_PCH_RX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_PCH_RX2TX
SATA3_PCH_TX	*	*	SATA3_PCH_2OTHER
SATA3_PCH_RX	*	*	SATA3_PCH_2OTHER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_PCH_TX2TX	*	=4x_DIELECTRIC	?	USB3_PCH_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX2RX	*	=5x_DIELECTRIC	?	USB3_PCH_TX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_PCH_RX2RX	*	=4x_DIELECTRIC	?	USB3_PCH_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX2TX	*	=5x_DIELECTRIC	?	USB3_PCH_RX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_PCH_2OTHER	*	=4x_DIELECTRIC	?	USB3_PCH_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	*_PCH_TX	*	USB3_PCH_TX2TX
USB3_PCH_TX	*_PCH_RX	*	USB3_PCH_TX2RX
USB3_PCH_RX	*_PCH_RX	*	USB3_PCH_RX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_PCH_RX2TX
USB3_PCH_TX	*	*	USB3_PCH_2OTHER
USB3_PCH_RX	*	*	USB3_PCH_2OTHER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
LVDS IG A CLK	LVDS_90D	LVDS_PCH_TX	LVDS IG A CLK P 17 74
LVDS IG A CLK	LVDS_90D	LVDS_PCH_TX	LVDS IG A CLK N 17 74
LVDS IG A DATA	LVDS_90D	LVDS_PCH_TX	LVDS IG A DATA P<2,.0> 6 17 74
LVDS IG A DATA	LVDS_90D	LVDS_PCH_TX	LVDS IG A DATA N<2,.0> 6 17 74
LVDS IG A DATA	LVDS_90D	LVDS_PCH_TX	LVDS IG A DATA P<3> 8 17
LVDS IG A DATA	LVDS_90D	LVDS_PCH_TX	LVDS IG A DATA N<3> 8 17
LVDS IG B DATA	LVDS_90D	LVDS_PCH_TX	LVDS IG B DATA P<3,.0> 8 17
LVDS IG B DATA	LVDS_90D	LVDS_PCH_TX	LVDS IG B DATA N<3,.0> 8 17
LVDS IG B CLK P	LVDS_90D	LVDS_PCH_TX	LVDS IG B CLK P 8 17
LVDS IG B CLK N	LVDS_90D	LVDS_PCH_TX	LVDS IG B CLK N 8 17
SATA HDD R2D	SATA_90D	SATA3_PCH_TX	SATA HDD R2D C P 16 41
SATA HDD R2D	SATA_90D	SATA3_PCH_TX	SATA HDD R2D C N 16 41
SATA HDD R2D_CONN	SATA_90D	SATA3_PCH_TX	SATA HDD R2D P 6 41
SATA HDD R2D_CONN	SATA_90D	SATA3_PCH_TX	SATA HDD R2D N 6 41
SATA HDD D2R	SATA_90D	SATA3_PCH_RX	SATA HDD D2R P 16 41
SATA HDD D2R	SATA_90D	SATA3_PCH_RX	SATA HDD D2R N 16 41
SATA HDD D2R_CONN	SATA_90D	SATA3_PCH_RX	SATA HDD D2R C P 6 41
SATA HDD D2R_CONN	SATA_90D	SATA3_PCH_RX	SATA HDD D2R C N 6 41
SATA ODD R2D	SATA_90D	SATA_PCH_TX	SATA ODD R2D C P 16 41
SATA ODD R2D	SATA_90D	SATA_PCH_TX	SATA ODD R2D C N 16 41
SATA ODD R2D	SATA_90D	SATA_PCH_TX	SATA ODD R2D P 6 41
SATA ODD R2D	SATA_90D	SATA_PCH_TX	SATA ODD R2D N 6 41
SATA ODD D2R	SATA_90D	SATA_PCH_RX	SATA ODD D2R P 16 41
SATA ODD D2R	SATA_90D	SATA_PCH_RX	SATA ODD D2R N 16 41
SATA HDD R2D_CONN	SATA_90D	SATA3_PCH_TX	SATA HDD R2D RC P 41
SATA HDD R2D_CONN	SATA_90D	SATA3_PCH_TX	SATA HDD R2D RC N 41
SATA HDD D2R_CONN	SATA_90D	SATA3_PCH_RX	SATA HDD D2R RC P 41
SATA HDD D2R_CONN	SATA_90D	SATA3_PCH_RX	SATA HDD D2R RC N 41
PCH SATA_ICOMP		SATA_ICOMP	PCH SATAICOMP 16
USB HUB1 UP	USB_85D	USB	USB HUB UP P 18 25
USB HUB1 UP	USB_85D	USB	USB HUB UP N 18 25
USB EXTA	USB_85D	USB	USB EXTA P 18 42
USB EXTA	USB_85D	USB	USB EXTA N 18 42
USB EXTB	USB_85D	USB	USB EXTB MUX P 25 43
USB EXTB	USB_85D	USB	USB EXTB MUX N 25 43
USB EXTA_MUXED_F_P	USB_85D	USB	USB EXTA_MUXED_F_P 42
USB EXTA_MUXED_F_N	USB_85D	USB	USB EXTA_MUXED_F_N 42
USB EXTB_F_P	USB_85D	USB	USB EXTB_F_P 43
USB EXTB_F_N	USB_85D	USB	USB EXTB_F_N 43
USB EXTA_MUXED_P	USB_85D	USB	USB EXTA_MUXED_P 42
USB EXTA_MUXED_N	USB_85D	USB	USB EXTA_MUXED_N 42
USB EXTD_XHCI_P	USB_85D	USB	USB EXTD_XHCI_P 8 18
USB EXTD_XHCI_N	USB_85D	USB	USB EXTD_XHCI_N 8 18
USB EXTB_EHCI_P	USB_85D	USB	USB EXTB_EHCI_P 18 25
USB EXTB_EHCI_N	USB_85D	USB	USB EXTB_EHCI_N 18 25
USB EXTB_XHCI_P	USB_85D	USB	USB EXTB_XHCI_P 18 25
USB EXTB_XHCI_N	USB_85D	USB	USB EXTB_XHCI_N 18 25
USB3 EXTA_RX_P	USB_85D	USB3_PCH_RX	USB3 EXTA_RX_P 18 42
USB3 EXTA_RX_N	USB_85D	USB3_PCH_RX	USB3 EXTA_RX_N 18 42
USB3 EXTA_TX_P	USB_85D	USB3_PCH_TX	USB3 EXTA_TX_P 18 42
USB3 EXTA_TX_N	USB_85D	USB3_PCH_TX	USB3 EXTA_TX_N 18 42
USB3 EXTB_RX_P	USB_85D	USB3_PCH_RX	USB3 EXTB_RX_P 18 43
USB3 EXTB_RX_N	USB_85D	USB3_PCH_RX	USB3 EXTB_RX_N 18 43
USB3 EXTB_TX_P	USB_85D	USB3_PCH_TX	USB3 EXTB_TX_P 18 43
USB3 EXTB_TX_N	USB_85D	USB3_PCH_TX	USB3 EXTB_TX_N 18 43
USB3 EXTA_RX_F_P	USB_85D	USB3_PCH_RX	USB3 EXTA_RX_F_P 42
USB3 EXTA_RX_F_N	USB_85D	USB3_PCH_RX	USB3 EXTA_RX_F_N 42
USB3 EXTA_TX_F_P	USB_85D	USB3_PCH_TX	USB3 EXTA_TX_F_P 42
USB3 EXTB_RX_F_P	USB_85D	USB3_PCH_RX	USB3 EXTB_RX_F_P 43
USB3 EXTB_TX_F_P	USB_85D	USB3_PCH_TX	USB3 EXTB_TX_F_P 43
USB3 EXTB_TX_F_N	USB_85D	USB3_PCH_TX	USB3 EXTB_TX_F_N 43
USB3 EXTA_TX_C_P	USB_85D	USB3_PCH_TX	USB3 EXTA_TX_C_P 42
USB3 EXTA_TX_C_N	USB_85D	USB3_PCH_TX	USB3 EXTA_TX_C_N 42
USB3 EXTB_TX_C_P	USB_85D	USB3_PCH_TX	USB3 EXTB_TX_C_P 43
USB3 EXTB_TX_C_N	USB_85D	USB3_PCH_TX	USB3 EXTB_TX_C_N 43
USB_SMC_P	USB_85D	USB	USB_SMC_P 8 45
USB_SMC_N	USB_85D	USB	USB_SMC_N 8 45
USB_EXTC_P	USB_85D	USB	USB_EXTC_P 8 18
USB_EXTC_N	USB_85D	USB	USB_EXTC_N 8 18
USB_CAMERA	USB_85D	USB	USB_CAMERA_P 18 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_N 18 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 6 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_N 6 32
USB_BT	USB_85D	USB	USB_BT_P 8 32
USB_BT	USB_85D	USB	USB_BT_N 8 32
USB_BT	USB_85D	USB	USB_BT_CONN_P 6 32
USB_BT	USB_85D	USB	USB_BT_CONN_N 6 32
USB_TP4D	USB_85D	USB	USB_TP4D_P 8 53
USB_TP4D	USB_85D	USB	USB_TP4D_N 8 53
USB_IR_P	USB_85D	USB	USB_IR_P 8 44
USB_IR_P	USB_85D	USB	USB_IR_N 8 44
PCH_USB_RBBIAS	PCH_USB_RBBIAS		PCH_USB_RBBIAS 18
PCH_CLK100M_PCH_P	CLK_PCH_90D	CLK_PCH	PCH_CLK100M_PCH_P 16
PCH_CLK100M_PCH_N	CLK_PCH_90D	CLK_PCH	PCH_CLK100M_PCH_N 16
PCH_CLK96M_DOT_P	CLK_PCH_80D	CLK_PCH	PCH_CLK96M_DOT_P 16
PCH_CLK96M_DOT_N	CLK_PCH_80D	CLK_PCH	PCH_CLK96M_DOT_N 16
PCH_CLK100M_SATA_P	CLK_PCH_90D	CLK_PCH	PCH_CLK100M_SATA_P 16
PCH_CLK100M_SATA_N	CLK_PCH_90D	CLK_PCH	PCH_CLK100M_SATA_N 16
PCH_CLK143M_REFCLK	CLK_PCH_50R	CLK_PCH	PCH_CLK143M_REFCLK 16
PCH_CLK33M_PCIIN	CLK_PCH_50R	CLK_PCH	PCH_CLK33M_PCIIN 16 24

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCI-Express Signal Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_T29_TX2TX	*	=3x_DIELECTRIC	?
PCIE_T29_TX2RX	*	=4x_DIELECTRIC	?
PCIE_T29_RX2RX	*	=3x_DIELECTRIC	?
PCIE_T29_RX2TX	*	=4x_DIELECTRIC	?
PCIE_T29_20THER	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_T29_TX2TX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_T29_TX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_T29_RX2RX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_T29_RX2TX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_T29_20THER	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_T29_TX	*_TX	*	PCIE_T29_TX2TX
PCIE_T29_TX	*_RX	*	PCIE_T29_TX2RX
PCIE_T29_RX	*_RX	*	PCIE_T29_RX2RX
PCIE_T29_RX	*_TX	*	PCIE_T29_RX2TX
PCIE_T29_TX	*	*	PCIE_T29_20THER
PCIE_T29_RX	*	*	PCIE_T29_20THER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE						
		PHYSICAL	SPACING					
	LPC_AD	LPC_50S	LPC	LPC AD<3...0>	6	16	45	47
	LPC_FRAME_L	LPC_50S	LPC	LPC FRAME L	6	16	45	47
	LPC_RESET_L	LPC_50S	LPC	LPC RESET L	24			
	LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC R	18	24		
	LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC	24	45		
	LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC CLK33M LPCPLUS	6	24	47	
	SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS PCH CLK	16	48		
	SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS PCH DATA	16	48		
	SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16	48		
	SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16	48		
	SMBUS_SMC_R_50_SCT	SMB_50S	SMB	SML_PCH_1_CLK	16	48		
	SMBUS_SMC_R_50_SDA	SMB_50S	SMB	SML_PCH_1_DATA	16	48		
	HDA_BIT_CLK	HDA_50S	HDA	HDA BIT CLK	16	57		
	HDA_BIT_CLK_R	HDA_50S	HDA	HDA BIT CLK R	16			
	HDA_SYNC	HDA_50S	HDA	HDA SYNC	16	57		
	HDA_SYNC_R	HDA_50S	HDA	HDA SYNC R	16			
	HDA_RST_L	HDA_50S	HDA	HDA RST R L	16			
	HDA_RST_L	HDA_50S	HDA	HDA RST L	16	57		
	HDA_SDIN0	HDA_50S	HDA	HDA SDIN0	16	57		
	HDA_SDI0_R	HDA_50S	HDA	AUD SDI R	57			
	HDA_SDOUT	HDA_50S	HDA	HDA SDOUT	16	57		
	HDA_SDOUT_R	HDA_50S	HDA	HDA SDOUT R	16	24		
	PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK				
	SPI_CLK	SPI_50S	SPI	SPI CLK R	16	47		
	SPI_CLK	SPI_50S	SPI	SPI CLK	47			
	SPI_MOSI	SPI_50S	SPI	SPI MOSI R	16	47		
	SPI_MOSI	SPI_50S	SPI	SPI MOSI	47			
	SPI_MISO	SPI_50S	SPI	SPI MISO	16	47		
	SPI_CS0_R_L	SPI_50S	SPI	SPI CS0 R L	16	47		
	SPI_CS0_L	SPI_50S	SPI	SPI CS0 L	47			
9281	SPI_MLB_CLK	SPI_50S	SPI	SPI MLB CLK	46	47	56	
9282	SPI_MLB_CS_L	SPI_50S	SPI	SPI MLB CS L	46	47	56	
9283	SPI_MLB_MOSI	SPI_50S	SPI	SPI MLB MOSI	46	47	56	
9284	SPI_MLB_MISO	SPI_50S	SPI	SPI MLB MISO	46	47	56	
9285	SPI_SMC_MISO	SPI_50S	SPI	SPI SMC MISO	45	46		
9286	SPI_SMC_MOSI	SPI_50S	SPI	SPI SMC MOSI	45	46		
9287	SPI_SMC_CLK	SPI_50S	SPI	SPI SMC CLK	45	46		
9288	SPI_SMC_CS_L	SPI_50S	SPI	SPI SMC CS L	45	46		
	PCIE_ENET_R2D_P	PCIE_85D	PCIE_PCH_TX	PCIE ENET R2D P	36			
	PCIE_ENET_R2D_N	PCIE_85D	PCIE_PCH_TX	PCIE ENET R2D N	36			
	PCIE_ENET_R2D_C_P	PCIE_85D	PCIE_PCH_TX	PCIE ENET R2D C P	16	36		
	PCIE_ENET_R2D_C_N	PCIE_85D	PCIE_PCH_TX	PCIE ENET R2D C N	16	36		
	PCIE_ENET_D2R_P	PCIE_85D	PCIE_PCH_RX	PCIE ENET D2R P	16	36		
	PCIE_ENET_D2R_N	PCIE_85D	PCIE_PCH_RX	PCIE ENET D2R N	16	36		
	PCIE_ENET_D2R_C_P	PCIE_85D	PCIE_PCH_RX	PCIE ENET D2R C P	36			
	PCIE_ENET_D2R_C_N	PCIE_85D	PCIE_PCH_RX	PCIE ENET D2R C N	36			
	PCIE_AP_R2D_P	PCIE_85D	PCIE_PCH_TX	PCIE AP R2D P	6	32		
	PCIE_AP_R2D_N	PCIE_85D	PCIE_PCH_TX	PCIE AP R2D N	6	32		
	PCIE_AP_R2D_C_P	PCIE_85D	PCIE_PCH_TX	PCIE AP R2D C P	16	32		
	PCIE_AP_R2D_C_N	PCIE_85D	PCIE_PCH_TX	PCIE AP R2D C N	16	32		
	PCIE_AP_D2R_P	PCIE_85D	PCIE_PCH_RX	PCIE AP D2R P	16	32		
	PCIE_AP_D2R_N	PCIE_85D	PCIE_PCH_RX	PCIE AP D2R N	16	32		
	PCIE_FW_R2D_P	PCIE_85D	PCIE_PCH_TX	PCIE FW R2D P	38			
	PCIE_FW_R2D_N	PCIE_85D	PCIE_PCH_TX	PCIE FW R2D N	38			
	PCIE_FW_R2D_C_P	PCIE_85D	PCIE_PCH_TX	PCIE FW R2D C P	16	38		
	PCIE_FW_R2D_C_N	PCIE_85D	PCIE_PCH_TX	PCIE FW R2D C N	16	38		
	PCIE_FW_D2R_P	PCIE_85D	PCIE_PCH_RX	PCIE FW D2R P	16	38		
	PCIE_FW_D2R_N	PCIE_85D	PCIE_PCH_RX	PCIE FW D2R N	16	38		
	PCIE_FW_D2R_C_P	PCIE_85D	PCIE_PCH_RX	PCIE FW D2R C P	38			
	PCIE_FW_D2R_C_N	PCIE_85D	PCIE_PCH_RX	PCIE FW D2R C N	38			
	PCIE_AP_D2R_PI_P	PCIE_85D	PCIE_PCH_RX	PCIE AP D2R PI P	6	32		
	PCIE_AP_D2R_PI_N	PCIE_85D	PCIE_PCH_RX	PCIE AP D2R PI N	6	32		
	PCIE_AP_R2D_PI_P	PCIE_85D	PCIE_PCH_RX	PCIE AP R2D PI P				
	PCIE_AP_R2D_PI_N	PCIE_85D	PCIE_PCH_RX	PCIE AP R2D PI N				
	PEG_CLK100M_P	CLK_PCIE_80D	CLK_PCIE	PEG CLK100M P	8	16		
	PEG_CLK100M_N	CLK_PCIE_80D	CLK_PCIE	PEG CLK100M N	8	16		
	PCIE_CLK100M_ENET_P	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M ENET P	16	36		
	PCIE_CLK100M_ENET_N	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M ENET N	16	36		
	PCIE_CLK100M_AP_P	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M AP P	16	32		
	PCIE_CLK100M_AP_N	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M AP N	16	32		
	PCIE_CLK100M_FW_P	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M FW P	16	38		
	PCIE_CLK100M_FW_N	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M FW N	16	38		
	PCIE_CLK100M_EXCARD_P	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M EXCARD P	8	16		
	PCIE_CLK100M_EXCARD_N	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M EXCARD N	8	16		
9289	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<1>	6			
9290	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<2>	6			
9291	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<5>	6			
9292	CPU_27E4S	CPU_COMP		TP_PCH_VSS_NCTF<7>				
9293	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<9>	6	81		
9294	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<9>	6	81		
9295	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<11>	6			
9296	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<12>	6			
9297	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<15>	6			
9298	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<17>	6			
9299	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<19>	6			
9300	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<21>	6			
9301	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<22>	6			
9302	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<25>	6			
9303	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<27>	6			
9304	CPU_27E4S	CPU_COMP		PCH_VSS_NCTF<29>	6			

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE				
	PHYSICAL	SPACING				
R689	DP_EXT_A_ML	DP_85D	DP_PCH_TX	DP_EXT_A_ML_C P<3..0>	8	75
R690	DP_EXT_A_ML	DP_85D	DP_PCH_TX	DP_EXT_A_ML_C N<3..0>	8	75
R691	DP_EXT_A_ML	DP_85D	DP_PCH_TX	DP_EXT_A_ML_P<3..0>	75	
R692	DP_EXT_A_ML	DP_85D	DP_PCH_TX	DP_EXT_A_ML_N<3..0>	75	
R693	DP_EXT_A_AUXCH	DP_85D	DP_PCH	DP_EXT_A_AUXCH_C P	8	75
R694	DP_EXT_A_AUXCH	DP_85D	DP_PCH	DP_EXT_A_AUXCH_C N	8	75
R695	DP_EXT_A_AUXCH	DP_85D	DP_PCH	DP_EXT_A_AUXCH_P	75	
R696	DP_EXT_A_AUXCH	DP_85D	DP_PCH	DP_EXT_A_AUXCH_N	75	
R697	PCIE_T29_R2D_P	PCIE_85D	PCIE_T29_RX	PCIE_T29_R2D_C P<3..0>	8	33
R698	PCIE_T29_R2D_P	PCIE_85D	PCIE_T29_RX	PCIE_T29_R2D_C N<3..0>	8	33
R699	PCIE_T29_R2D_P	PCIE_85D	PCIE_T29_RX	PCIE_T29_R2D_P<3..0>	33	
R700	PCIE_T29_R2D_P	PCIE_85D	PCIE_T29_RX	PCIE_T29_R2D_N<3..0>	33	
R701	PCIE_T29_D2R_P	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R_P<3..0>	8	33
R702	PCIE_T29_D2R_P	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R_N<3..0>	8	33
R703	PCIE_T29_D2R_P	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R_C P<3..0>	33	
R704	PCIE_T29_D2R_P	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R_C N<3..0>	33	
R705	PCIE_CLK100M_T29_P	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_T29_P	16	33
R706	PCIE_CLK100M_T29_N	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_T29_N	16	33

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
E249	SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 24
E250	SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	16 24
E248		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	16
E251		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	24 36
E252		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
E253	SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	24 33
E249		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	33


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A

SYNCH MASTER#K901 MLB		SYNCH DATE=02/15/2013	
PAGE TITLE			
Ethernet/FW Constraints			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-9058		D
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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 IC Net Properties

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
DP_85D	DP_85D	DP_ECH_TX	DP T29SNK0 ML C P<3..0> 8 33
DP_85D	DP_85D	DP_ECH_TX	DP T29SNK0 ML C N<3..0> 8 33
DP_T29SNK0_ML	DP_85D	DP_ECH_TX	DP T29SNK0 ML P<3..0> 33
DP_T29SNK0_ML	DP_85D	DP_ECH_TX	DP T29SNK0 ML N<3..0> 33
DP_85D	DP_85D	DP_ECH	DP T29SNK0 AUXCH C P 8 33
DP_85D	DP_85D	DP_ECH	DP T29SNK0 AUXCH C N 8 33
DP_T29SNK0_AUXCH	DP_85D	DP_ECH	DP T29SNK0 AUXCH P 33
DP_T29SNK0_AUXCH	DP_85D	DP_ECH	DP T29SNK0 AUXCH N 33
DP_85D	DP_85D	DP_ECH_TX	DP T29SNK1 ML C P<3..0> 8 33
DP_85D	DP_85D	DP_ECH_TX	DP T29SNK1 ML C N<3..0> 8 33
DP_T29SNK1_ML	DP_85D	DP_ECH_TX	DP T29SNK1 ML P<3..0> 33
DP_T29SNK1_ML	DP_85D	DP_ECH_TX	DP T29SNK1 ML N<3..0> 33
DP_85D	DP_85D	DP_ECH	DP T29SNK1 AUXCH C P 8 33
DP_85D	DP_85D	DP_ECH	DP T29SNK1 AUXCH C N 8 33
DP_T29SNK1_AUXCH	DP_85D	DP_ECH	DP T29SNK1 AUXCH P 33
DP_T29SNK1_AUXCH	DP_85D	DP_ECH	DP T29SNK1 AUXCH N 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC ML C P<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC ML C N<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C P
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C N
DP_85D	T29_I2C_55S	T29_I2C	I2C T29_SCL 33 48
DP_85D	T29_I2C_55S	T29_I2C	I2C T29_SDA 33 48
DP_85D	T29_SPI_CLK	T29_SPI	T29_SPI_CLK 33
DP_85D	T29_SPI_MOSI	T29_SPI	T29_SPI_MOSI 33
DP_85D	T29_SPI_MISO	T29_SPI	T29_SPI_MISO 33
DP_85D	T29_SPI_CS_L	T29_SPI	T29_SPI_CS_L 33
DP_85D	T29DP_80D	T29DP	T29_R2D C P<3..0> 8 33 75
DP_85D	T29DP_80D	T29DP	T29_R2D C N<3..0> 8 33 75
DP_85D	T29DP_100D	T29DP	T29_D2R P<3..0> 8 33 75
DP_85D	T29DP_100D	T29DP	T29_D2R N<3..0> 8 33 75

Only used on hosts supporting T29 video-in

T29/DP Net Properties

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
DP_85D	T29DP_80D	T29DP	T29_R2D P<0> 75
DP_85D	T29DP_80D	T29DP	T29_R2D N<0> 75
DP_85D	T29DP_80D	T29DP	T29_R2D P<1> 75
DP_85D	T29DP_80D	T29DP	T29_R2D N<1> 75
DP_85D	T29DP_80D	T29DP	T29_R2D C F P<1..0> 75
DP_85D	T29DP_80D	T29DP	T29_R2D C F N<1..0> 75
DP_85D	T29DP_100D	T29DP	T29_D2R C P<0> 75 76
DP_85D	T29DP_100D	T29DP	T29_D2R C N<0> 75 76
DP_85D	T29DP_100D	T29DP	T29_D2R C P<1> 75 76
DP_85D	T29DP_100D	T29DP	T29_D2R C N<1> 75 76
DP_85D	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P 76
DP_85D	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N 76
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0> 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0> 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0> 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0> 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2> 75 83
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2> 75 83
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2> 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2> 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N 75
DP_85D	T29DP_80D	T29DP	T29DPA_ML_P<3..0> 75 76
DP_85D	T29DP_80D	T29DP	T29DPA_ML_N<3..0> 75 76
DP_85D	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0> 75 76
DP_85D	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0> 75 76
DP_85D	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P 75 76
DP_85D	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N 75 76
DP_85D	T29DP_80D	T29DP	T29_R2D P<2>
DP_85D	T29DP_80D	T29DP	T29_R2D N<2>
DP_85D	T29DP_80D	T29DP	T29_R2D P<3>
DP_85D	T29DP_80D	T29DP	T29_R2D N<3>
DP_85D	T29DP_80D	T29DP	T29_R2D C F P<3..2>
DP_85D	T29DP_80D	T29DP	T29_R2D C F N<3..2>
DP_85D	T29DP_100D	T29DP	T29_D2R C P<2>
DP_85D	T29DP_100D	T29DP	T29_D2R C N<2>
DP_85D	T29DP_100D	T29DP	T29_D2R C P<3>
DP_85D	T29DP_100D	T29DP	T29_D2R C N<3>
DP_85D	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P
DP_85D	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2> 83
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2> 83
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P
DP_85D	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N
DP_85D	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P
DP_85D	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N
DP_85D	T29DP_80D	T29DP	T29DPB_ML_P<3..0>
DP_85D	T29DP_80D	T29DP	T29DPB_ML_N<3..0>
DP_85D	T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>
DP_85D	T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>
DP_85D	T29DP_80D	T29DP	DP_B_EXT_AUXCH_P
DP_85D	T29DP_80D	T29DP	DP_B_EXT_AUXCH_N



Only used on dual-port hosts.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
□	SMBUS_SMC_4_S3_SCL	SMB_5.0S	SMB	SMBUS_SMC_2_S3_SCL	5 45 68
	SMBUS_SMC_4_S3_SDA	SMB_5.0S	SMB	SMBUS_SMC_2_S3_SDA	6 45 68
□	SMBUS_SMC_8_S0_SCL	SMB_5.0S	SMB	SMBUS_SMC_1_S0_SCL	45 68
	SMBUS_SMC_8_S0_SDA	SMB_5.0S	SMB	SMBUS_SMC_1_S0_SDA	45 68
□	SMBUS_SMC_8_S0_SCL	SMB_5.0S	SMB	SMBUS_SMC_0_S0_SCL	45 68
	SMBUS_SMC_8_S0_SDA	SMB_5.0S	SMB	SMBUS_SMC_0_S0_SDA	45 68
□	SMBUS_SMC_16_S0_SCL	SMB_5.0S	SMB	SMBUS_SMC_5_G3_SCL	6 45 68
	SMBUS_SMC_16_S0_SDA	SMB_5.0S	SMB	SMBUS_SMC_5_G3_SDA	6 45 68
□	SMBUS_SMC_32_S0_SCL	SMB_5.0S	SMB	SMBUS_SMC_3_SCL	45 68
	SMBUS_SMC_32_S0_SDA	SMB_5.0S	SMB	SMBUS_SMC_3_SDA	45 68

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE	
		PHYSICAL	SPACING
	CHGR CSI	1T01_DIFFPAIR	CHGR CSI P
		1T01_DIFFPAIR	CHGR CSI N
	CHGR CSO	1T01_DIFFPAIR	CHGR CSO P
		1T01_DIFFPAIR	CHGR CSO N

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	LVS*	*	GND_P2004

8	7	6	5	4	3	2	1
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K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYFF, BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.3 MM	5

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	NCA	NCA_0.1MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SR	TOP_BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SR	*	Y	0.080 MM	0.080 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SS	TOP, BOTTOM	Y	0.165 MM	0.165 MM			
40_OHM_SS	ISL10	N	0.126 MM	0.126 MM	-STANDARD	-STANDARD	-STANDARD
40_OHM_SS	ISL3, ISL4, ISL9	Y	0.126 MM	0.126 MM	-STANDARD	-STANDARD	-STANDARD
40_OHM_SS	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1_5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2_5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SS	TOP_BOTTOM	Y	0.190 MM	0.1 MM			
37_OHM_SS	ISL10	N	0.145 MM	0.1 MM	-STANDARD	-STANDARD	-STANDARD
37_OHM_SS	ISL3,ISL4,ISL9	Y	0.145 MM	0.1 MM	-STANDARD	-STANDARD	-STANDARD
37_OHM_SS	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P_4_OHM_SE	TOP_BOTTOM	Y	0.310 MM	0.2 MM			
27P_4_OHM_SE	*	Y	0.235 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFPAIR PRIMARY GAP	DIFFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OBM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OBM_DIFF	ISL3, ISL4, ISL9	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
72_OBM_DIFF	ISL10	N	0.140MM	0.140 MM		0.190 MM	0.190 MM
72_OBM_DIFF	TOP, BOTTOM	Y		0.175 MM	0.200 MM	0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	+STANDARD	+STANDARD	+STANDARD	+STANDARD	+STANDARD
85_OHM_DIFF	ISL3, ISL4	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL9, ISL10	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.190 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF
85_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.111 MM	0.111 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF
90_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.085 MM	0.085 MM	0.200 MM	0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_NGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_NGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_NGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_NGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
48_OHM_SE	*	Y	0.090 MM	0.090 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
80_OHM_DIFF	ISL3, ISL4	Y	0.115 MM	0.115 MM	0.180 MM	0.180 MM	0.180 MM
80_OHM_DIFF	ISL9, ISL10	Y	0.115 MM	0.115 MM	0.180 MM	0.180 MM	0.180 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM	0.190 MM	0.190 MM	0.190 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DEFAULT	*	0.1 MM	?	*	*	BGA	BGA_P10H
STANDARD	*	=DEFAULT	?	MEM_CLK	*	BGA	BGA_P20H
BGA_P10H	*	=DEFAULT	?	CLK_P0TE	*	BGA	BGA_P20H
BGA_P20H	*	=DEFAULT	?	CLK_SLOW	*	BGA	BGA_P20H

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P100M
MEM_CLK	*	BGA	BGA_P200M
CLK_PCIE	*	BGA	BGA_P200M
CLK_SLOW	*	BGA	BGA_P200M

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
6X_DIELECTRIC	*	0.420 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
6X_DIELECTRIC	*	0.420 MM	?
7X_DIELECTRIC	*	0.490 MM	?

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	-STANDARD	-STANDARD	-STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF
85_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.


PYCHAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF
90_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	<100_OHM_DIFF	<100_OHM_DIFF	<100_OHM_DIFF	<100_OHM_DIFF	<100_OHM_DIFF	<100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

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