



Compal Confidential

IFTxx Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M
(With nVIDIA MXM/B)

2006-11-01

REV: 0.1

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				IFTXX M/B LA-3541P Schematic	
				Date: Wednesday, November 01, 2006	Sheet 1 of 52
				Rev 0.1	

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Model Name : IFTXX
File Name : LA-3541P

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Fan Control
page 4

Intel Merom Processor
uPGA-478 Package
page 4,5,6

Thermal Sensor
ADM1032
page 4

Clock Generator
ICS9LPRS365
page 16

CRT & TV-out
page 19

FSB
667/800MHz
H_A#(3..35) H_D#(0..63)

LCD Conn.
page 18

Video Processor
page 18

LVDS
SDVO

Intel Crestline
uFCBGA-1299
page 7,8,9,10,11,12,13

Memory BUS(DDR2)
Dual Channel
1.8V DDR2 533/667

200pin DDR2-SO-DIMM X2
BANK 0, 1, 2, 3
page 14,15

MXM II VGA/B
page 17

PCI-Express

DMI
X4 mode

USB conn x2
TO M/B
page 33

USB conn x2
TO I/O/B
page 37

Bluetooth
Conn
page 33

CMOS Camera
page 42

Finger Print
Conn
page 42

PCI-Express

Intel ICH8-M
BGA-676
page 20,21,22,23

3.3V 48MHz

USB

3.3V 24.576MHz/48MHz

HD Audio

3.3V ATA-100

IDE

S-ATA port 0

New Card
Socket
page 33

MINI Card x3
WLAN,
3G/TV-Tuner
Robson
page 32

LAN(GbE)
BCM5787M/5906
page 30

IDSEL:AD20
(PIRQC#,PIRQD#,
GNT#2, REQ#2)

CardBus
ENE CB1410
page 26

Card Reader
R5C833
page 28

RJ45
page 31

PCMCIA
Socket
page 26

1394
Conn.
page 28

3 in 1
socket
page 29

CDROM
Conn.
page 24

MDC 1.5
Conn
page 42

HDA Codec
ALC268
page 38

Audio AMP
page 39

S-ATA HDD
Conn.
page 24

LPC BUS

ENE KB925
page 34

SUPER I/O
LPC47N217
page 41

TPM
page 29

Touch Pad
page 36

Int. KBD
page 35

G-Sensor
page 25

BIOS
page 36

SCREW
page 40

RTC CKT.
page 21

Power On/Off CKT.
page 37

DC/DC Interface CKT.
page 43

Power Circuit DC/DC
page 44,45,47,48
49,50,51

CHARGER
page 46

Switch/B Conn.
page 35

I/O Conn.
FRONT LCD /B,
LID SW
page 37

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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				IFTXX M/B LA-3541P Schematic	
				Date: Wednesday, November 01, 2006	Sheet 2 of 52

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+Cardreader	AD22	0	G,H

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	NVIDIA NB8X	

EC SM Bus2 address

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

ID1	ID0	TEST
0(R744)	0(R745)	A-TEST
0(R744)	1(R742)	B-TEST
1(R741)	0(R745)	C-TEST

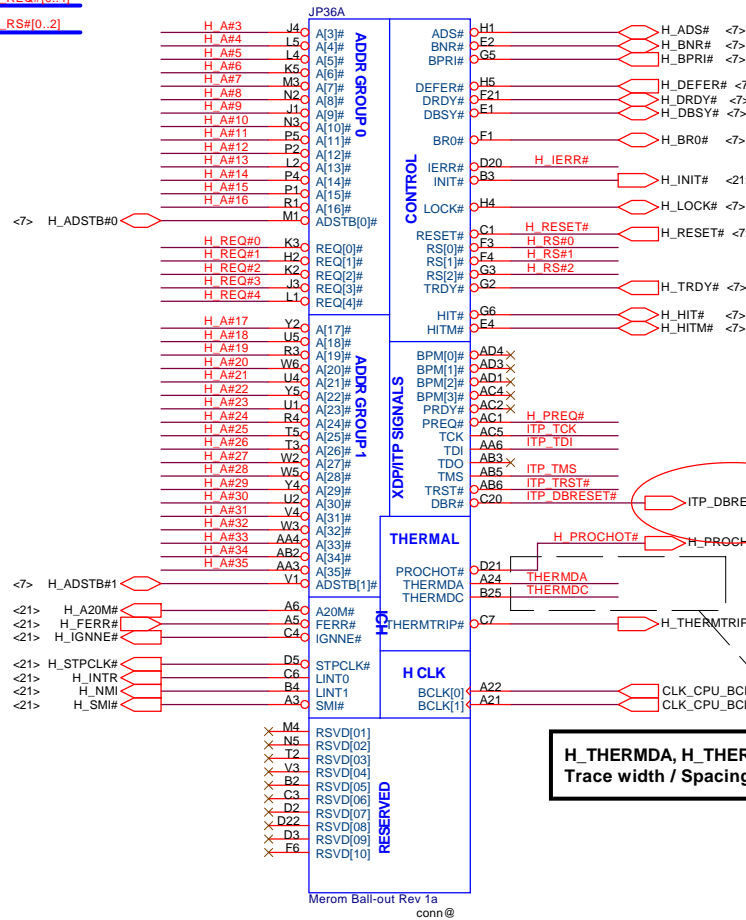
PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

ICH8M SM Bus address

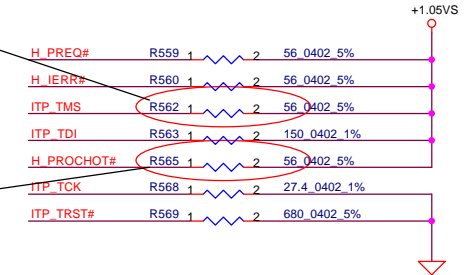
Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

<7> H_A# [3..35] H_A# [3..35]
<7> H_REQ# [0..4] H_REQ# [0..4]
<7> H_RS# [0..2] H_RS# [0..2]

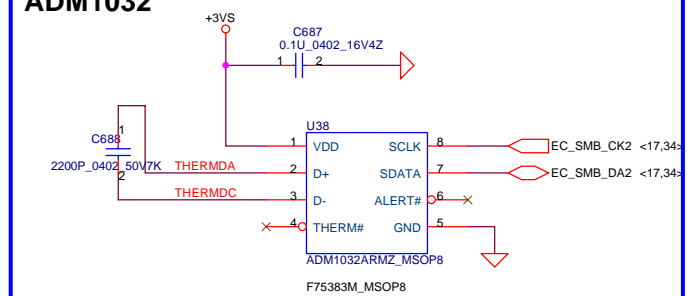


Checklist recommend 39 Ohm

CRB pull 75 Ohm



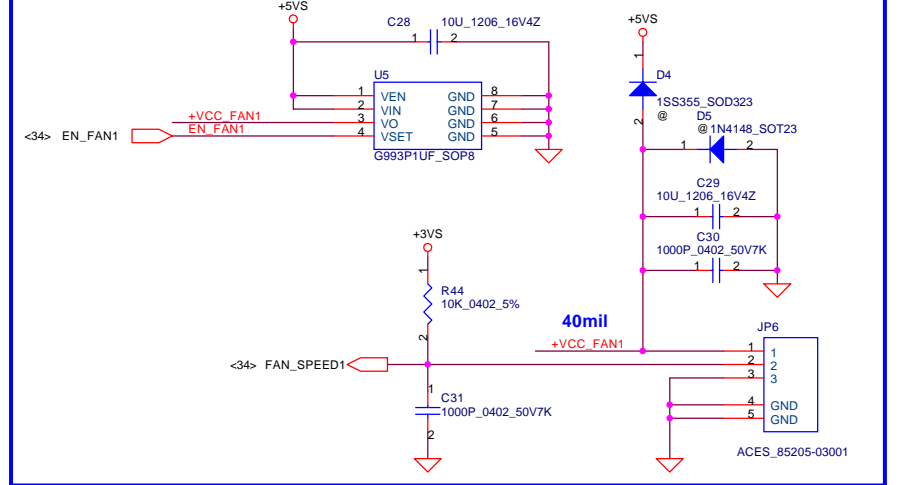
ADM1032



Connect SB SYS_RESET# or just left NC

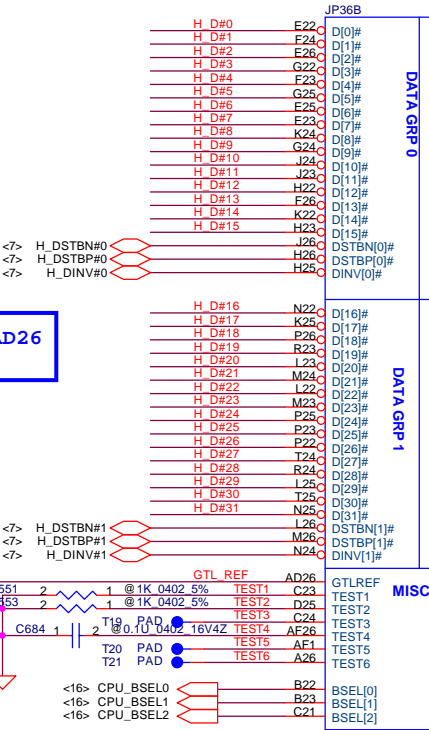
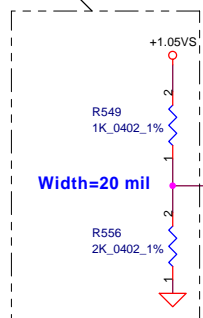
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

FAN1 Conn



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				IFTXX M/B LA-3541P Schematic	
				Date: Wednesday, November 01, 2006	Sheet 4 of 52

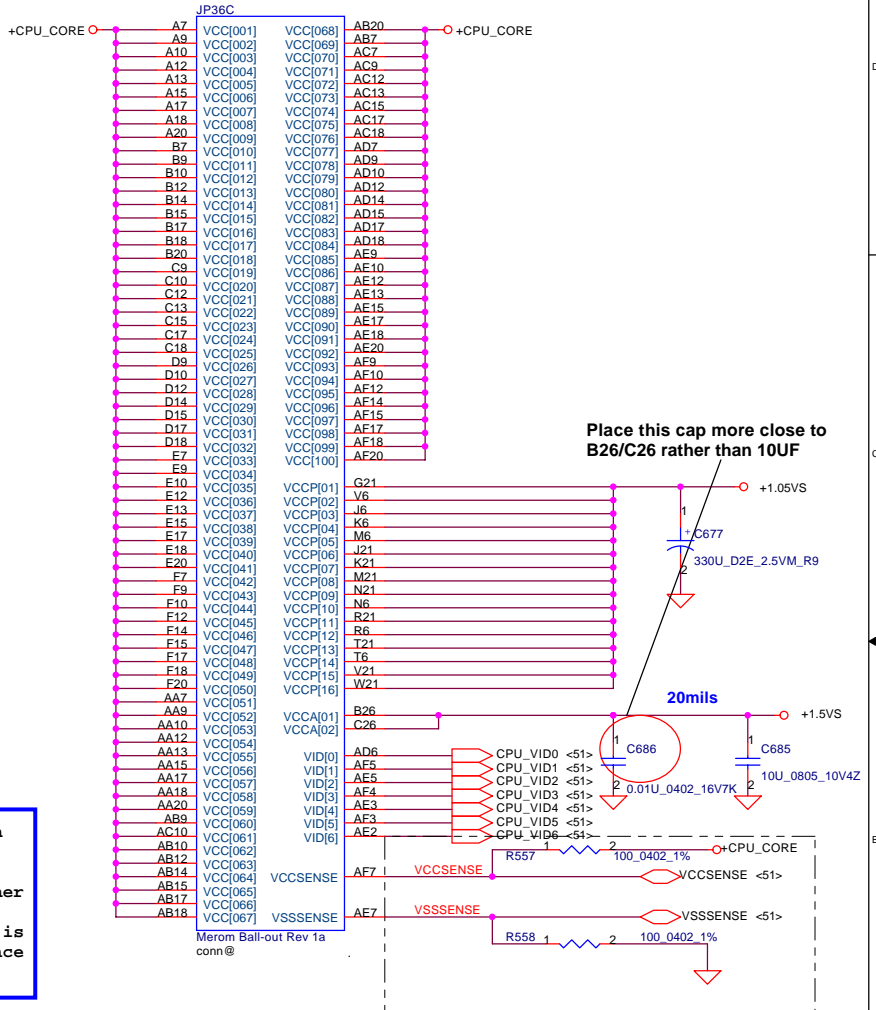
Close to CPU pin AD26
within 500mils.



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

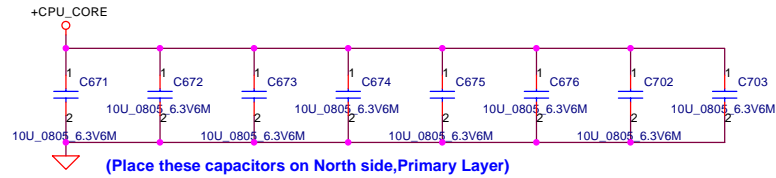
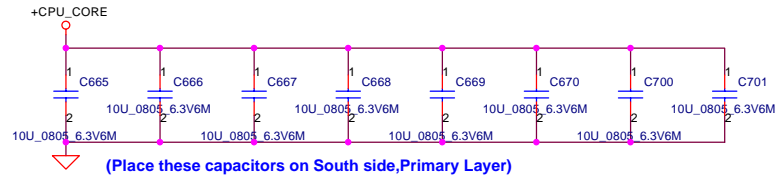
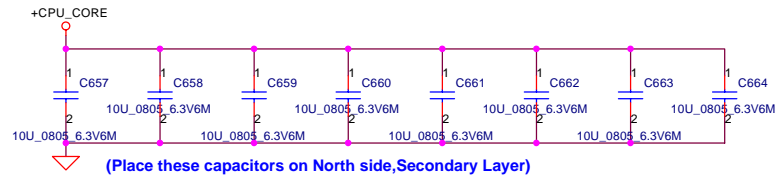
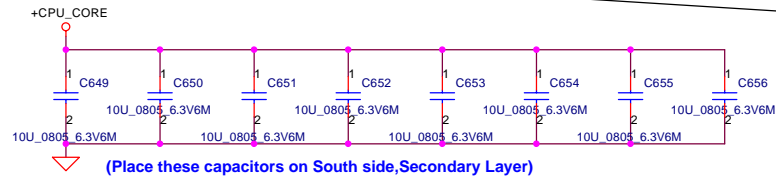
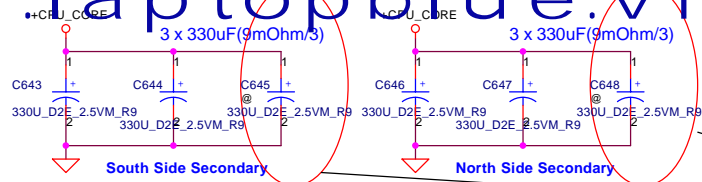
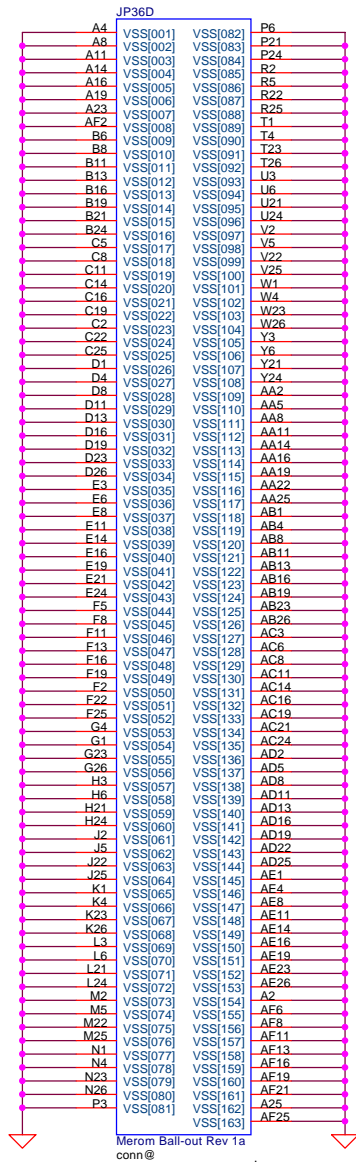
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within
0.5" of CPU pin. Trace
should be at least 25
mils away from any other
toggling signal.
COMP[0,2] trace width is
18 mils. COMP[1,3] trace
width is 4 mils.

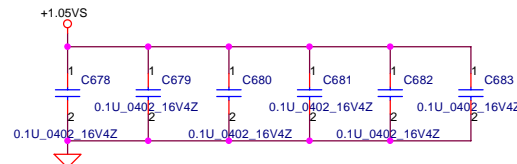


Length match within 25 mils.
The trace width/space/other is
20/7/25.

Close to CPU pin
within 500mils.



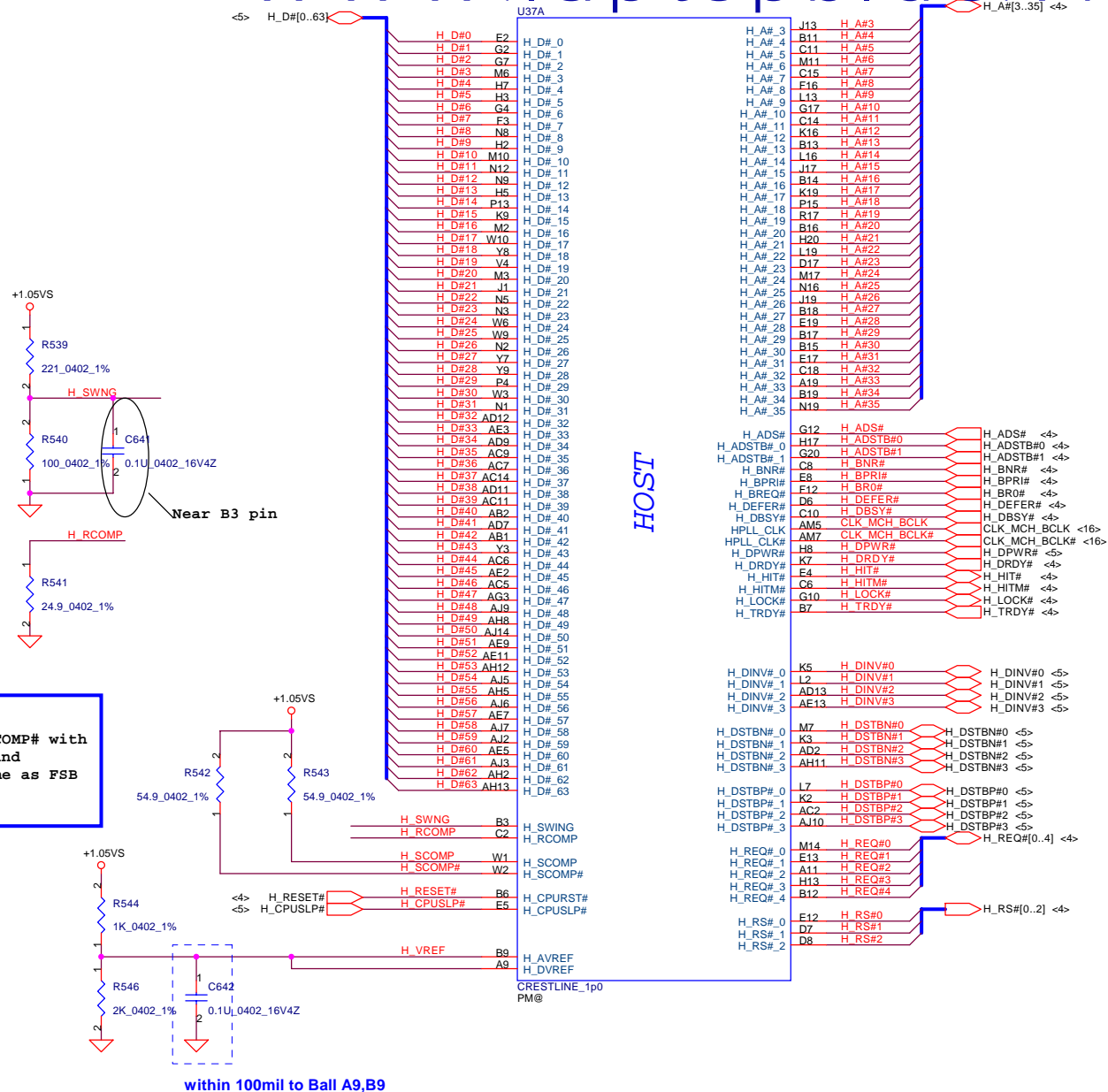
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



CRB no stuff. Reserved!

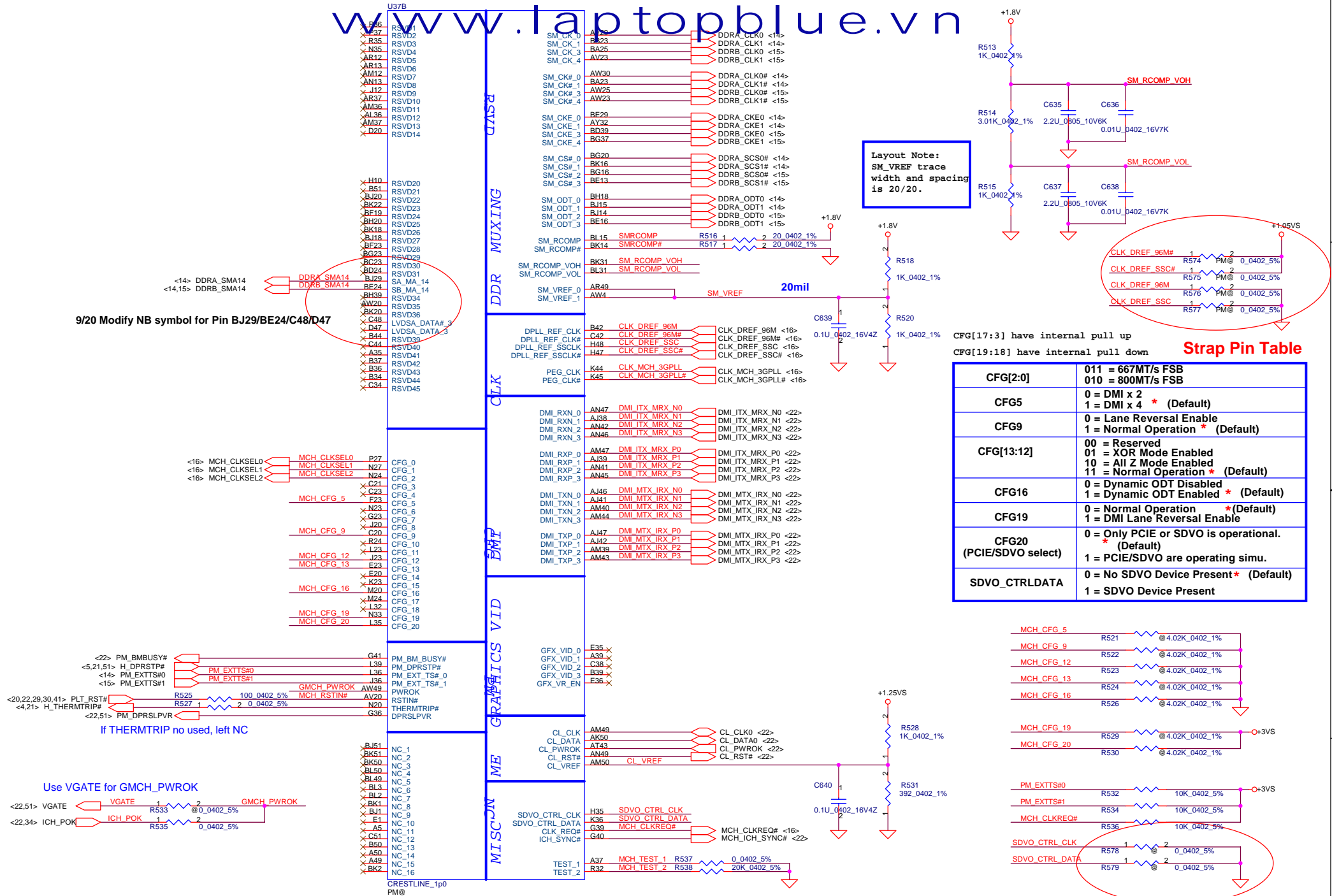
9/25 10U checked. OK for use!

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				B	IFTXX M/B LA-3541P Schematic	0
				Date:	Wednesday, November 01, 2006	Sheet 6 of 52



Layout Note:
H_SCOMP / H_SCOMP#
trace width and spacing is 10/20

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Size B	Document Number	IFTXX M/B LA-3541P Schematic		Rev	0
Date:	Wednesday, November 01, 2006	Sheet	7	of	52



<14> DDRA_SDQ[0..63] DDRA_SDQ[0..63]
<14> DDRA_SDM[0..7] DDRA_SDM[0..7]
<14> DDRA_SMA[0..13] DDRA_SMA[0..13]

<15> DDRB_SDQ[0..63] DDRB_SDQ[0..63]
<15> DDRB_SDM[0..7] DDRB_SDM[0..7]
<15> DDRB_SMA[0..13] DDRB_SMA[0..13]

U37D

DDRA_SDQ0	AR43	SA_DQ_0
DDRA_SDQ1	AW44	SA_DQ_1
DDRA_SDQ2	BA45	SA_DQ_2
DDRA_SDQ3	AY46	SA_DQ_3
DDRA_SDQ4	AR41	SA_DQ_4
DDRA_SDQ5	AR45	SA_DQ_5
DDRA_SDQ6	AT42	SA_DQ_6
DDRA_SDQ7	AW47	SA_DQ_7
DDRA_SDQ8	BB48	SA_DQ_8
DDRA_SDQ9	BF48	SA_DQ_9
DDRA_SDQ10	BG47	SA_DQ_10
DDRA_SDQ11	BA45	SA_DQ_11
DDRA_SDQ12	BB47	SA_DQ_12
DDRA_SDQ13	BG50	SA_DQ_13
DDRA_SDQ14	BH49	SA_DQ_14
DDRA_SDQ15	BE45	SA_DQ_15
DDRA_SDQ16	AW44	SA_DQ_16
DDRA_SDQ17	BE44	SA_DQ_17
DDRA_SDQ18	BG42	SA_DQ_18
DDRA_SDQ19	BE40	SA_DQ_19
DDRA_SDQ20	BF44	SA_DQ_20
DDRA_SDQ21	BH45	SA_DQ_21
DDRA_SDQ22	BG40	SA_DQ_22
DDRA_SDQ23	BE40	SA_DQ_23
DDRA_SDQ24	AR40	SA_DQ_24
DDRA_SDQ25	AW40	SA_DQ_25
DDRA_SDQ26	AT39	SA_DQ_26
DDRA_SDQ27	AW36	SA_DQ_27
DDRA_SDQ28	AW41	SA_DQ_28
DDRA_SDQ29	AY41	SA_DQ_29
DDRA_SDQ30	AV38	SA_DQ_30
DDRA_SDQ31	AT38	SA_DQ_31
DDRA_SDQ32	AV13	SA_DQ_32
DDRA_SDQ33	AT13	SA_DQ_33
DDRA_SDQ34	AW11	SA_DQ_34
DDRA_SDQ35	AY11	SA_DQ_35
DDRA_SDQ36	AU15	SA_DQ_36
DDRA_SDQ37	AT11	SA_DQ_37
DDRA_SDQ38	BA13	SA_DQ_38
DDRA_SDQ39	BA11	SA_DQ_39
DDRA_SDQ40	BE10	SA_DQ_40
DDRA_SDQ41	BD10	SA_DQ_41
DDRA_SDQ42	BD8	SA_DQ_42
DDRA_SDQ43	AY9	SA_DQ_43
DDRA_SDQ44	BG10	SA_DQ_44
DDRA_SDQ45	AW9	SA_DQ_45
DDRA_SDQ46	BD7	SA_DQ_46
DDRA_SDQ47	BB9	SA_DQ_47
DDRA_SDQ48	BB5	SA_DQ_48
DDRA_SDQ49	AY7	SA_DQ_49
DDRA_SDQ50	AT5	SA_DQ_50
DDRA_SDQ51	AT7	SA_DQ_51
DDRA_SDQ52	AY6	SA_DQ_52
DDRA_SDQ53	BB7	SA_DQ_53
DDRA_SDQ54	AR5	SA_DQ_54
DDRA_SDQ55	AR8	SA_DQ_55
DDRA_SDQ56	AR9	SA_DQ_56
DDRA_SDQ57	AN3	SA_DQ_57
DDRA_SDQ58	AN8	SA_DQ_58
DDRA_SDQ59	AN10	SA_DQ_59
DDRA_SDQ60	AT9	SA_DQ_60
DDRA_SDQ61	AN9	SA_DQ_61
DDRA_SDQ62	AM9	SA_DQ_62
DDRA_SDQ63	AN11	SA_DQ_63

CRESTLINE_1p0
PM@

DDR SYSTEM MEMORY A

SA_BS_0	BB19	DDRA_SBS0 <14>
SA_BS_1	BK19	DDRA_SBS1 <14>
SA_BS_2	BF29	DDRA_SBS2 <14>
SA_CAS#	BL17	DDRA_SCAS# <14>
SA_DM_0	AT45	DDRA_SDM0
SA_DM_1	BD44	DDRA_SDM1
SA_DM_2	BD42	DDRA_SDM2
SA_DM_3	AW38	DDRA_SDM3
SA_DM_4	AW13	DDRA_SDM4
SA_DM_5	BG8	DDRA_SDM5
SA_DM_6	AV5	DDRA_SDM6
SA_DM_7	AN6	DDRA_SDM7
SA_DQS_0	AT46	DDRA_SDQS0
SA_DQS_1	BE48	DDRA_SDQS1
SA_DQS_2	BB43	DDRA_SDQS2
SA_DQS_3	BC37	DDRA_SDQS3
SA_DQS_4	BB16	DDRA_SDQS4
SA_DQS_5	BH6	DDRA_SDQS5
SA_DQS_6	BB2	DDRA_SDQS6
SA_DQS_7	AP3	DDRA_SDQS7
SA_DQS#_0	AT47	DDRA_SDQS#0
SA_DQS#_1	BD47	DDRA_SDQS#1
SA_DQS#_2	BC41	DDRA_SDQS#2
SA_DQS#_3	BA37	DDRA_SDQS#3
SA_DQS#_4	BA16	DDRA_SDQS#4
SA_DQS#_5	BH7	DDRA_SDQS#5
SA_DQS#_6	BC1	DDRA_SDQS#6
SA_DQS#_7	AP2	DDRA_SDQS#7
SA_MA_0	BJ19	DDRA_SMA0
SA_MA_1	BD20	DDRA_SMA1
SA_MA_2	BK27	DDRA_SMA2
SA_MA_3	BH28	DDRA_SMA3
SA_MA_4	BL24	DDRA_SMA4
SA_MA_5	BK28	DDRA_SMA5
SA_MA_6	BJ27	DDRA_SMA6
SA_MA_7	BJ25	DDRA_SMA7
SA_MA_8	BL28	DDRA_SMA8
SA_MA_9	BA28	DDRA_SMA9
SA_MA_10	BC19	DDRA_SMA10
SA_MA_11	BE28	DDRA_SMA11
SA_MA_12	BG30	DDRA_SMA12
SA_MA_13	BJ16	DDRA_SMA13
SA_RAS#	BE18	DDRA_SRAS# <14>
SA_RCVEN#	AY20	DDRA_SRCVEN# <14>
SA_WE#	BA19	DDRA_SWE# <14>

PAD T18

DDRA_SWE# <14>

U37E

DDRB_SDQ0	AP49	SB_DQ_0
DDRB_SDQ1	AR51	SB_DQ_1
DDRB_SDQ2	AW50	SB_DQ_2
DDRB_SDQ3	AW51	SB_DQ_3
DDRB_SDQ4	AN51	SB_DQ_4
DDRB_SDQ5	AN50	SB_DQ_5
DDRB_SDQ6	AV50	SB_DQ_6
DDRB_SDQ7	AV49	SB_DQ_7
DDRB_SDQ8	BA50	SB_DQ_8
DDRB_SDQ9	BB50	SB_DQ_9
DDRB_SDQ10	BA49	SB_DQ_10
DDRB_SDQ11	BE50	SB_DQ_11
DDRB_SDQ12	BA51	SB_DQ_12
DDRB_SDQ13	AY49	SB_DQ_13
DDRB_SDQ14	BF50	SB_DQ_14
DDRB_SDQ15	BF49	SB_DQ_15
DDRB_SDQ16	BJ50	SB_DQ_16
DDRB_SDQ17	BJ44	SB_DQ_17
DDRB_SDQ18	BJ43	SB_DQ_18
DDRB_SDQ19	BL43	SB_DQ_19
DDRB_SDQ20	BK47	SB_DQ_20
DDRB_SDQ21	BK49	SB_DQ_21
DDRB_SDQ22	BK43	SB_DQ_22
DDRB_SDQ23	BK42	SB_DQ_23
DDRB_SDQ24	BJ41	SB_DQ_24
DDRB_SDQ25	BJ41	SB_DQ_25
DDRB_SDQ26	BJ37	SB_DQ_26
DDRB_SDQ27	BJ36	SB_DQ_27
DDRB_SDQ28	BK41	SB_DQ_28
DDRB_SDQ29	BJ40	SB_DQ_29
DDRB_SDQ30	BL36	SB_DQ_30
DDRB_SDQ31	BK37	SB_DQ_31
DDRB_SDQ32	BK13	SB_DQ_32
DDRB_SDQ33	BE11	SB_DQ_33
DDRB_SDQ34	BK11	SB_DQ_34
DDRB_SDQ35	BC11	SB_DQ_35
DDRB_SDQ36	BC13	SB_DQ_36
DDRB_SDQ37	BE12	SB_DQ_37
DDRB_SDQ38	BC12	SB_DQ_38
DDRB_SDQ39	BG12	SB_DQ_39
DDRB_SDQ40	BJ10	SB_DQ_40
DDRB_SDQ41	BL9	SB_DQ_41
DDRB_SDQ42	BK5	SB_DQ_42
DDRB_SDQ43	BL5	SB_DQ_43
DDRB_SDQ44	BK9	SB_DQ_44
DDRB_SDQ45	BK10	SB_DQ_45
DDRB_SDQ46	BJ8	SB_DQ_46
DDRB_SDQ47	BL6	SB_DQ_47
DDRB_SDQ48	BE4	SB_DQ_48
DDRB_SDQ49	BH5	SB_DQ_49
DDRB_SDQ50	BG1	SB_DQ_50
DDRB_SDQ51	BG2	SB_DQ_51
DDRB_SDQ52	BK3	SB_DQ_52
DDRB_SDQ53	BE4	SB_DQ_53
DDRB_SDQ54	BD3	SB_DQ_54
DDRB_SDQ55	BJ2	SB_DQ_55
DDRB_SDQ56	BG3	SB_DQ_56
DDRB_SDQ57	BB3	SB_DQ_57
DDRB_SDQ58	AR1	SB_DQ_58
DDRB_SDQ59	AT3	SB_DQ_59
DDRB_SDQ60	AY2	SB_DQ_60
DDRB_SDQ61	AY3	SB_DQ_61
DDRB_SDQ62	AU2	SB_DQ_62
DDRB_SDQ63	AT2	SB_DQ_63

DDR SYSTEM MEMORY B

SB_BS_0	AY17	DDRB_SBS0 <15>
SB_BS_1	BG18	DDRB_SBS1 <15>
SB_BS_2	BG36	DDRB_SBS2 <15>
SB_CAS#	BE17	DDRB_SCAS# <15>
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SB_DM_1	BD49	DDRB_SDM1
SB_DM_2	BK45	DDRB_SDM2
SB_DM_3	BL39	DDRB_SDM3
SB_DM_4	BH12	DDRB_SDM4
SB_DM_5	BJ7	DDRB_SDM5
SB_DM_6	BE3	DDRB_SDM6
SB_DM_7	AW2	DDRB_SDM7
SB_DQS_0	AT50	DDRB_SDQS0
SB_DQS_1	BD50	DDRB_SDQS1
SB_DQS_2	BK46	DDRB_SDQS2
SB_DQS_3	BK39	DDRB_SDQS3
SB_DQS_4	BL12	DDRB_SDQS4
SB_DQS_5	BL7	DDRB_SDQS5
SB_DQS_6	BE2	DDRB_SDQS6
SB_DQS_7	AV2	DDRB_SDQS7
SB_DQS#_0	AU50	DDRB_SDQS#0
SB_DQS#_1	BC50	DDRB_SDQS#1
SB_DQS#_2	BL45	DDRB_SDQS#2
SB_DQS#_3	BK38	DDRB_SDQS#3
SB_DQS#_4	BK12	DDRB_SDQS#4
SB_DQS#_5	BK7	DDRB_SDQS#5
SB_DQS#_6	BE2	DDRB_SDQS#6
SB_DQS#_7	AV3	DDRB_SDQS#7
SB_MA_0	BC18	DDRB_SMA0
SB_MA_1	BG28	DDRB_SMA1
SB_MA_2	BG25	DDRB_SMA2
SB_MA_3	AW17	DDRB_SMA3
SB_MA_4	BE25	DDRB_SMA4
SB_MA_5	BE25	DDRB_SMA5
SB_MA_6	BA29	DDRB_SMA6
SB_MA_7	BC28	DDRB_SMA7
SB_MA_8	AY28	DDRB_SMA8
SB_MA_9	BD37	DDRB_SMA9
SB_MA_10	BG17	DDRB_SMA10
SB_MA_11	BE37	DDRB_SMA11
SB_MA_12	BA39	DDRB_SMA12
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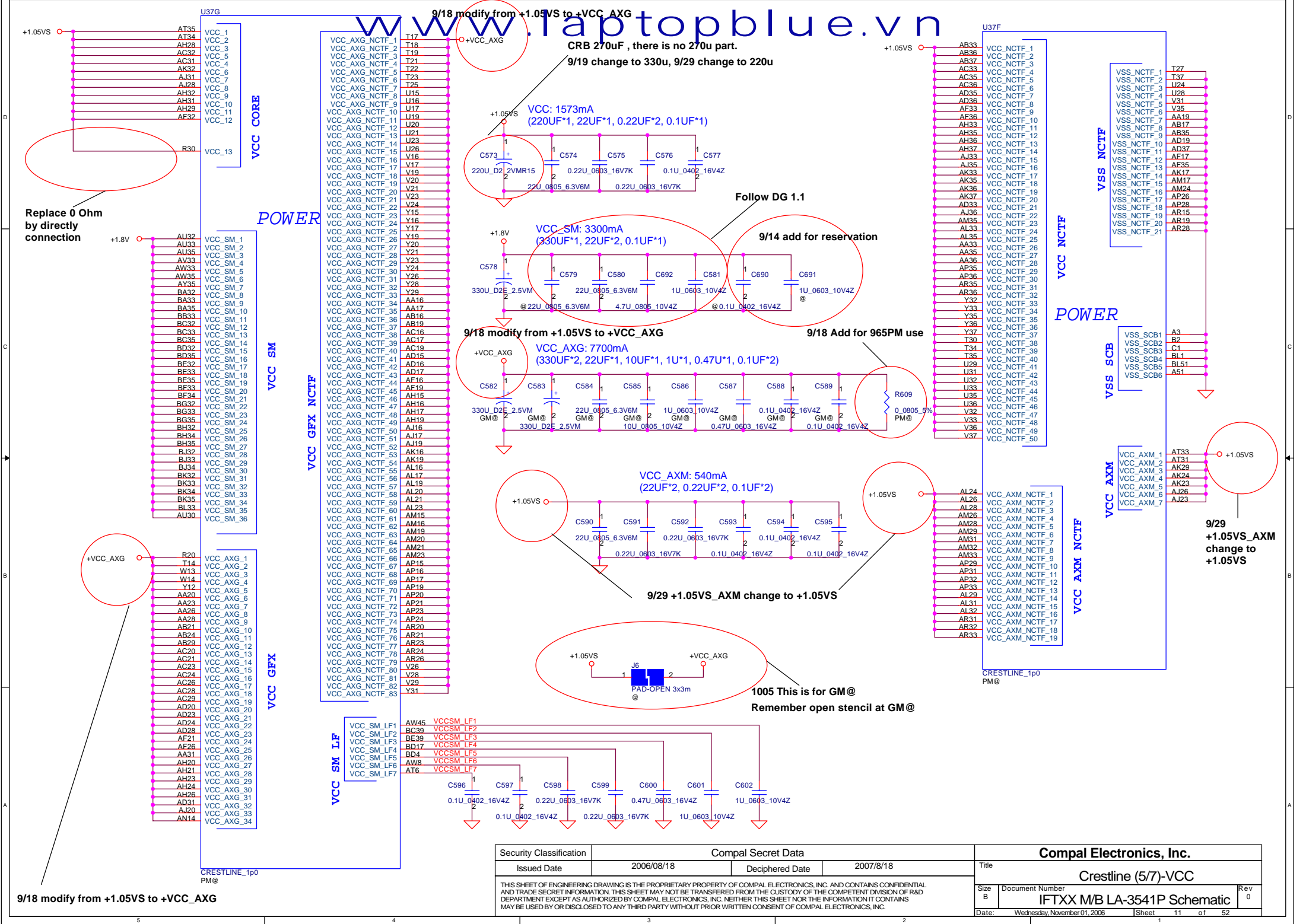
PAD T17

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Issued Date		2006/08/18		Deciphered Date		2007/8/18		Title			
								Crestline (3/7)-DDRII			
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							IFTXX M/B LA-3541P Schematic				
						Date:		Wednesday, November 01, 2006		Sheet 9 of 52	



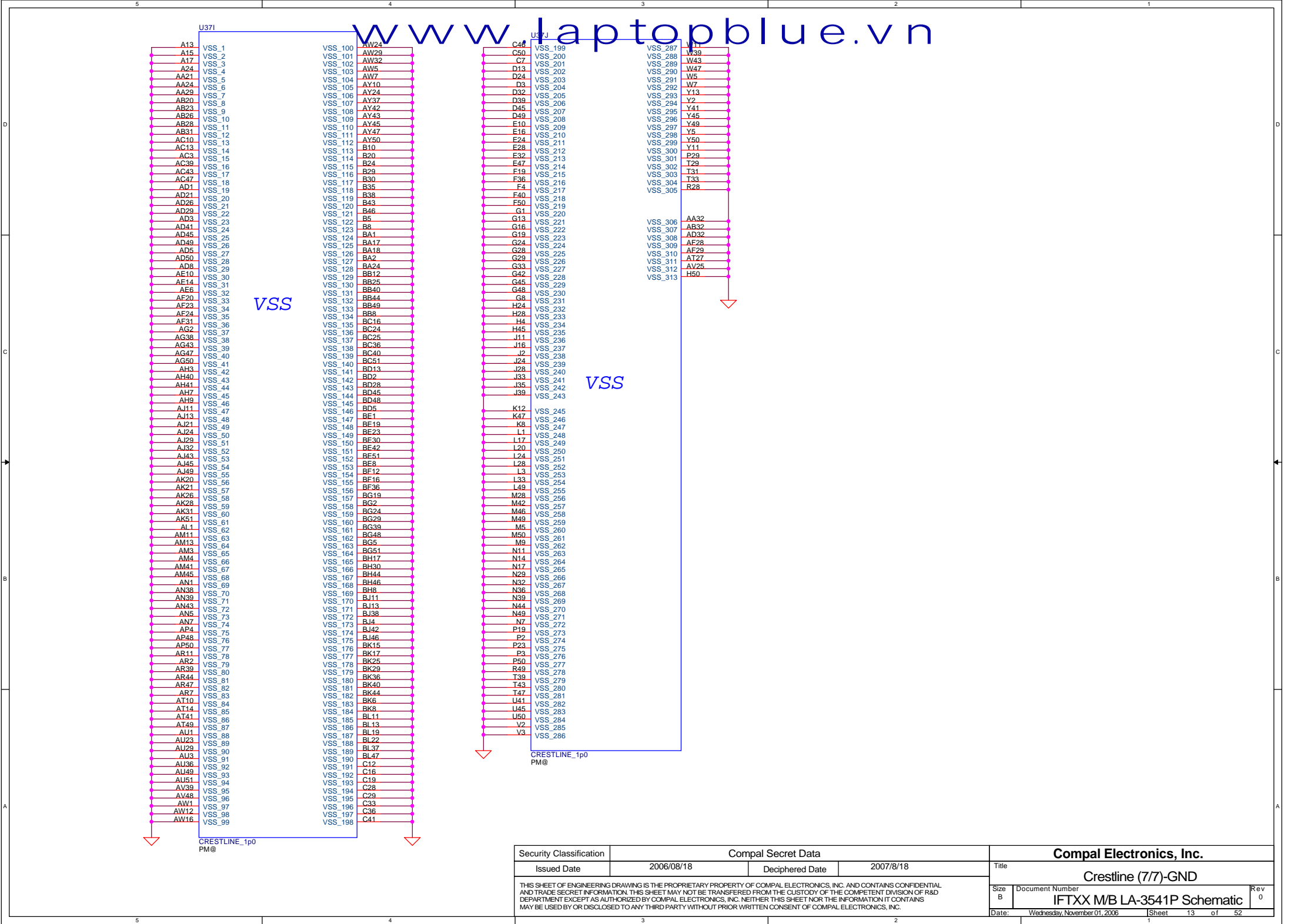
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Size B	Document Number IFTXX M/B LA-3541P Schematic Date: Wednesday, November 01, 2006
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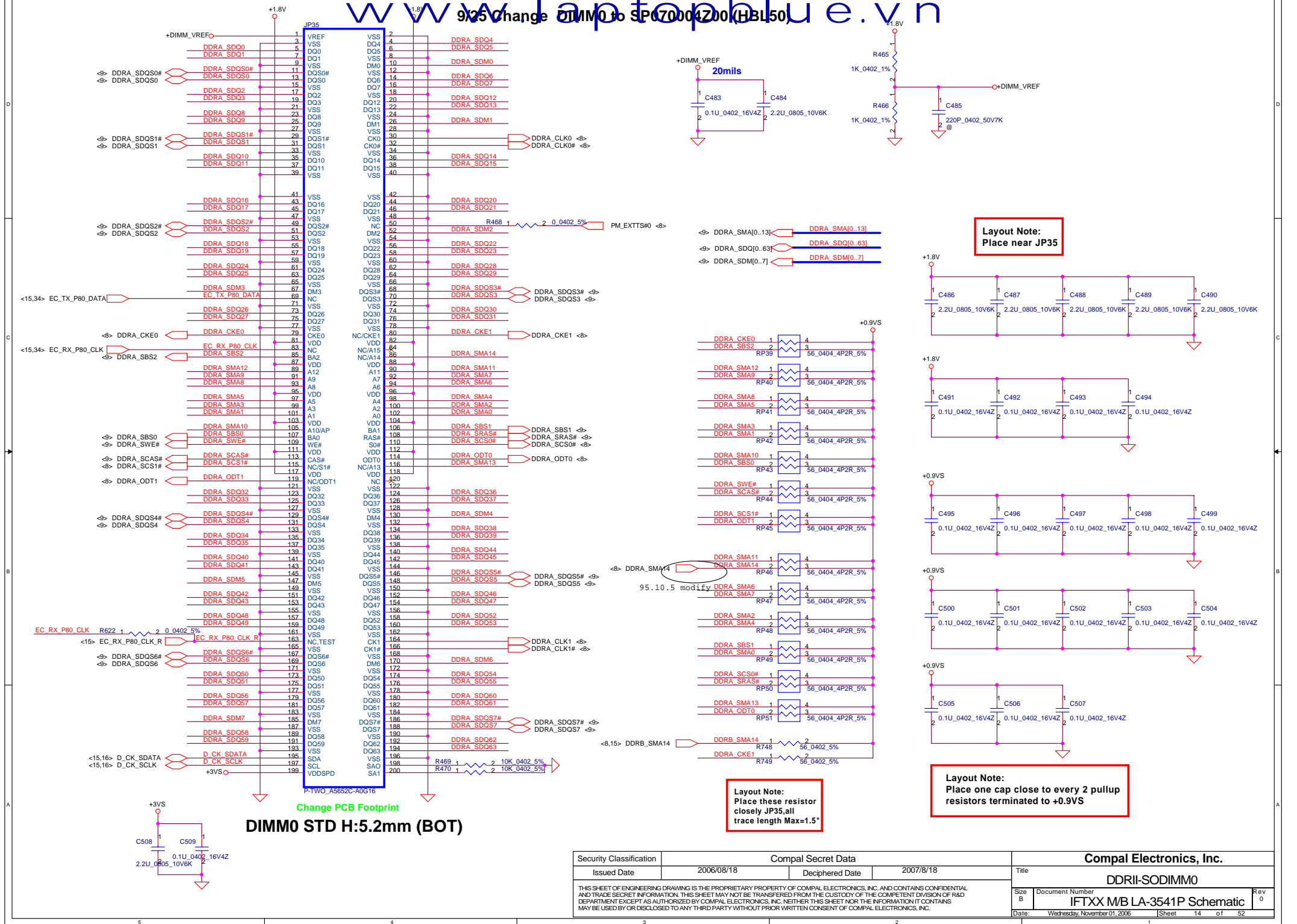
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	Rev			
B	IFTXX M/B LA-3541P Schematic	0			
Date:	Wednesday, November 01, 2006	Sheet	11	of	52

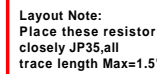
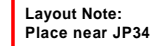
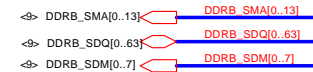
Close to VCC_HV (pin C40/B40)

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				IFTXX M/B LA-3541P Schematic			
				Date: Wednesday, November 01, 2006	Sheet 12 of 52		



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Crestline (7/7)-GND	
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				IFTXX M/B LA-3541P Schematic	
				Date:	Wednesday, November 01, 2006
				Sheet	13 of 52

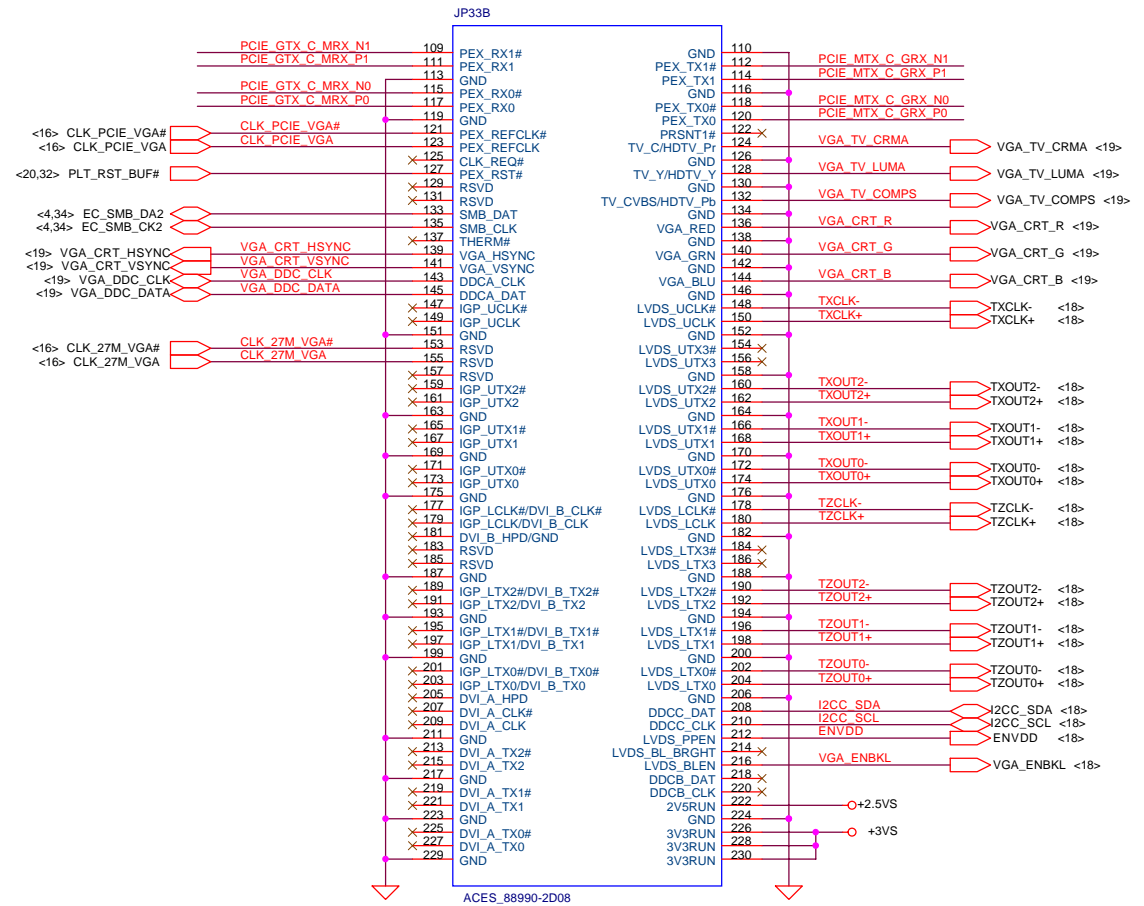
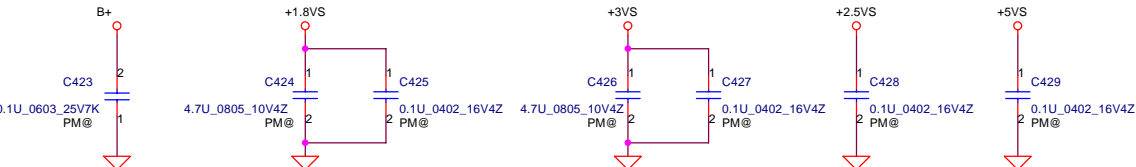




Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

DIMM1 STD H:9.2mm (BOT)

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				Date: Wednesday, November 01, 2006		Sheet 15 of 52



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				Cust	IFTXX MB LA-3541P Schematic	0	
				Date:	Wednesday, November 01, 2006	Sheet	17 of 52

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Issued Date		2006/08/18	Deciphered Date	2007/8/18		Title		
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				Size B	Document Number		Rev 0	
				IFTXX M/B LA-3541P Schematic				
Date:		Wednesday, November 01, 2006		Sheet 18 of 52				

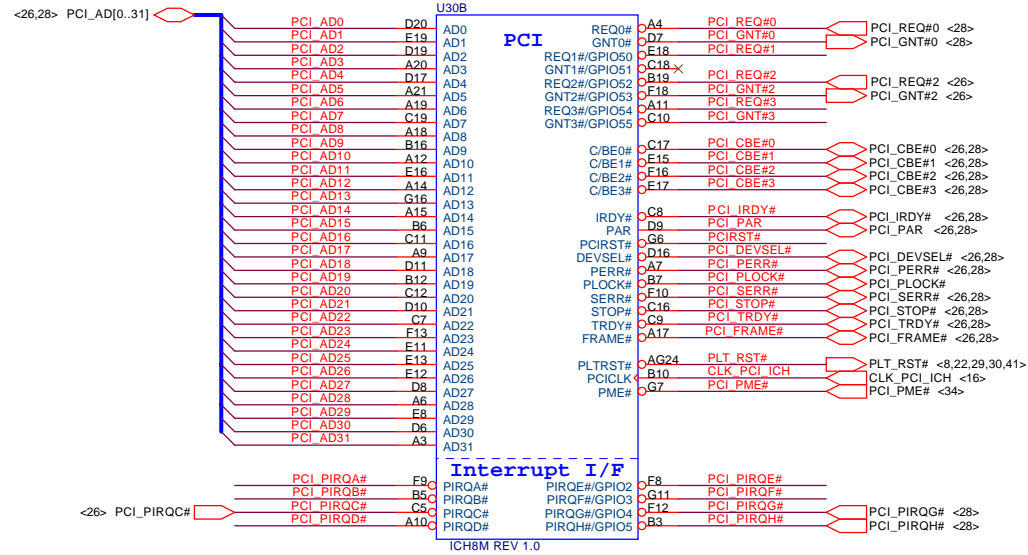
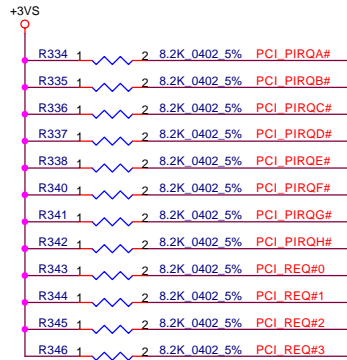
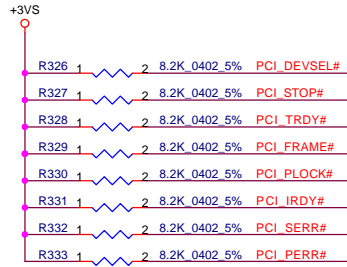


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				Size B	Document Number		Rev 0	
				IFTXX M/B LA-3541P Schematic				
Date:				Wednesday, November 01, 2006		Sheet 19 of 52		

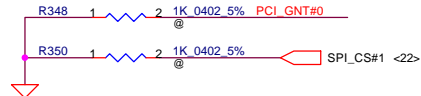
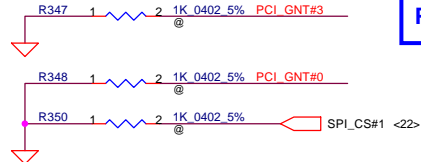
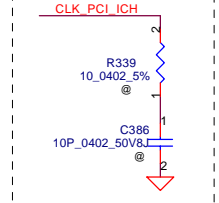
10/17 : Change P/N from SA000010G00 to SA00001JU10

10/17 : FootPrint : SA000010G00

BOM : SA00001JU10

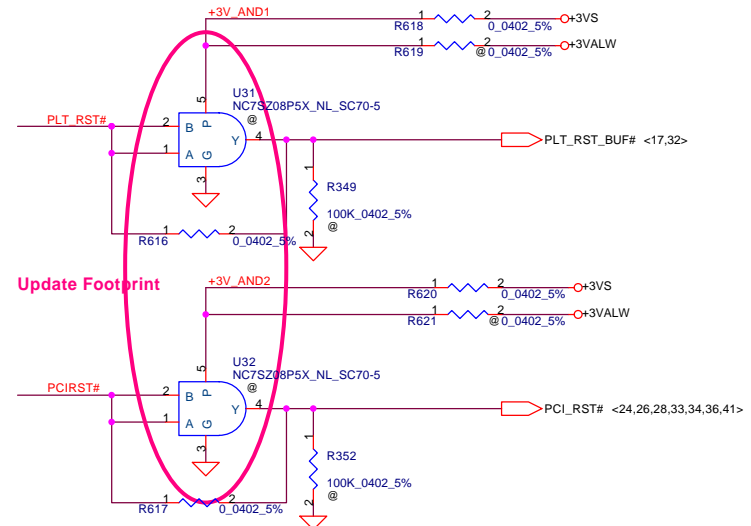


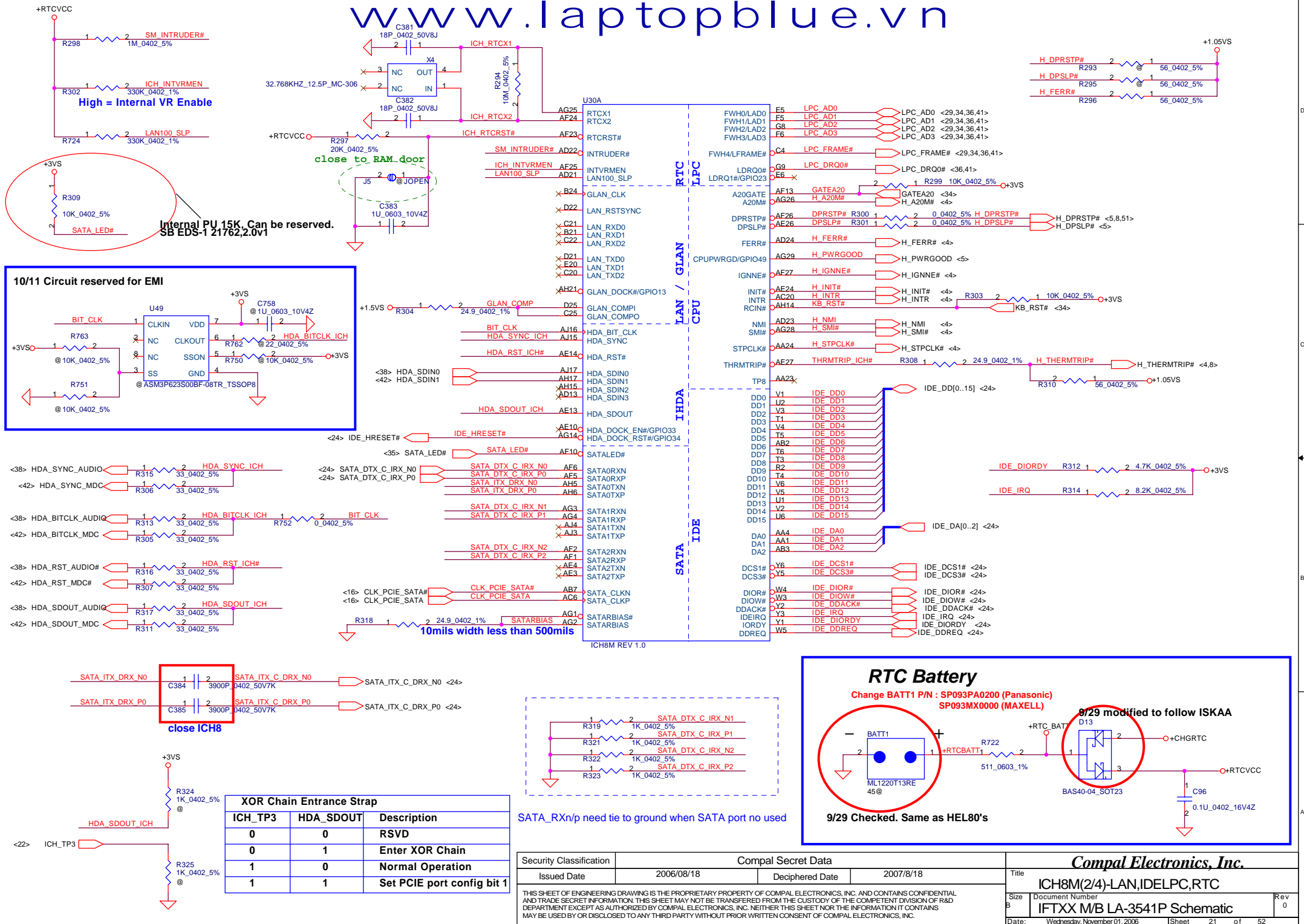
Place closely pin B10

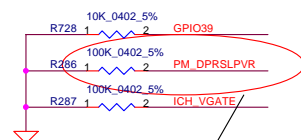
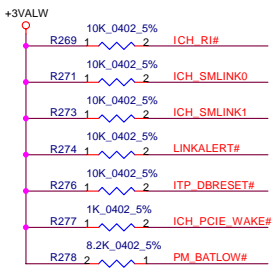
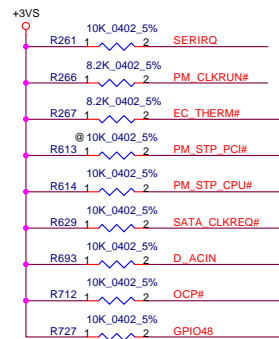


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

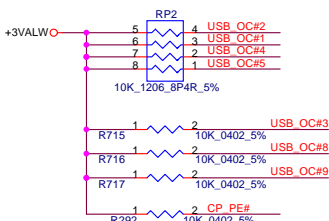
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



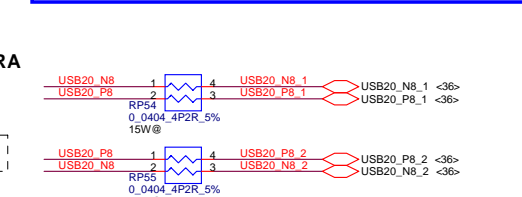
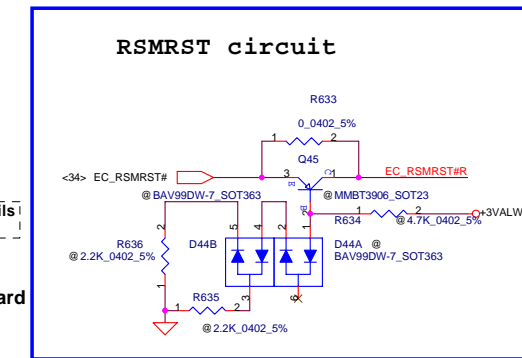
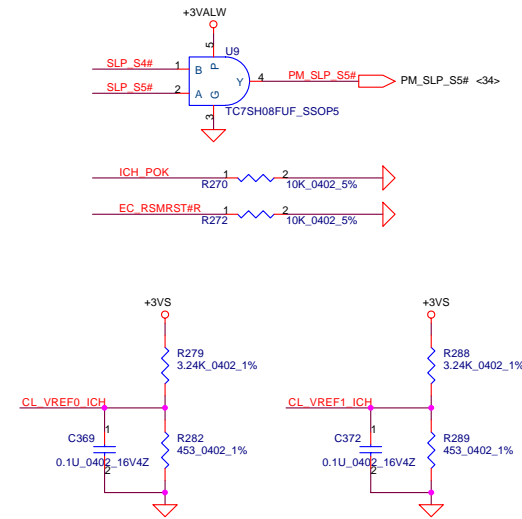
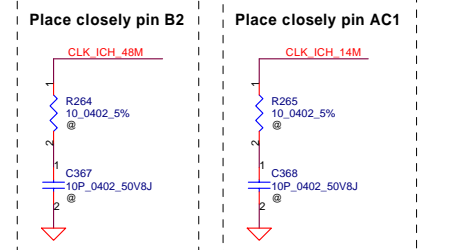
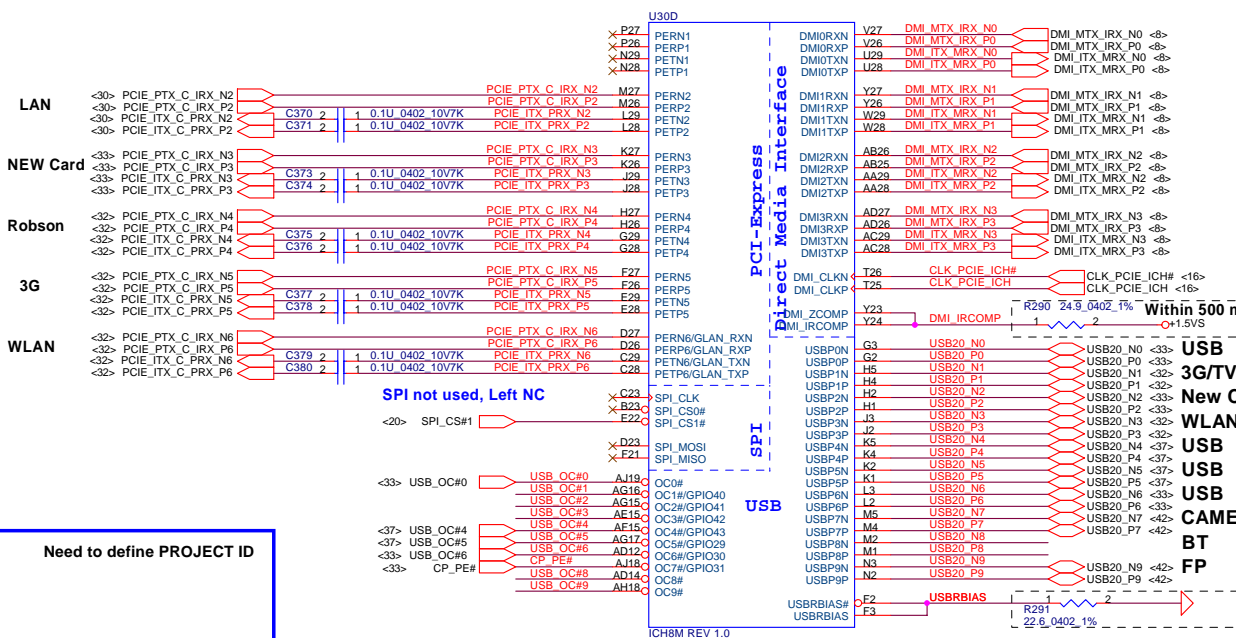
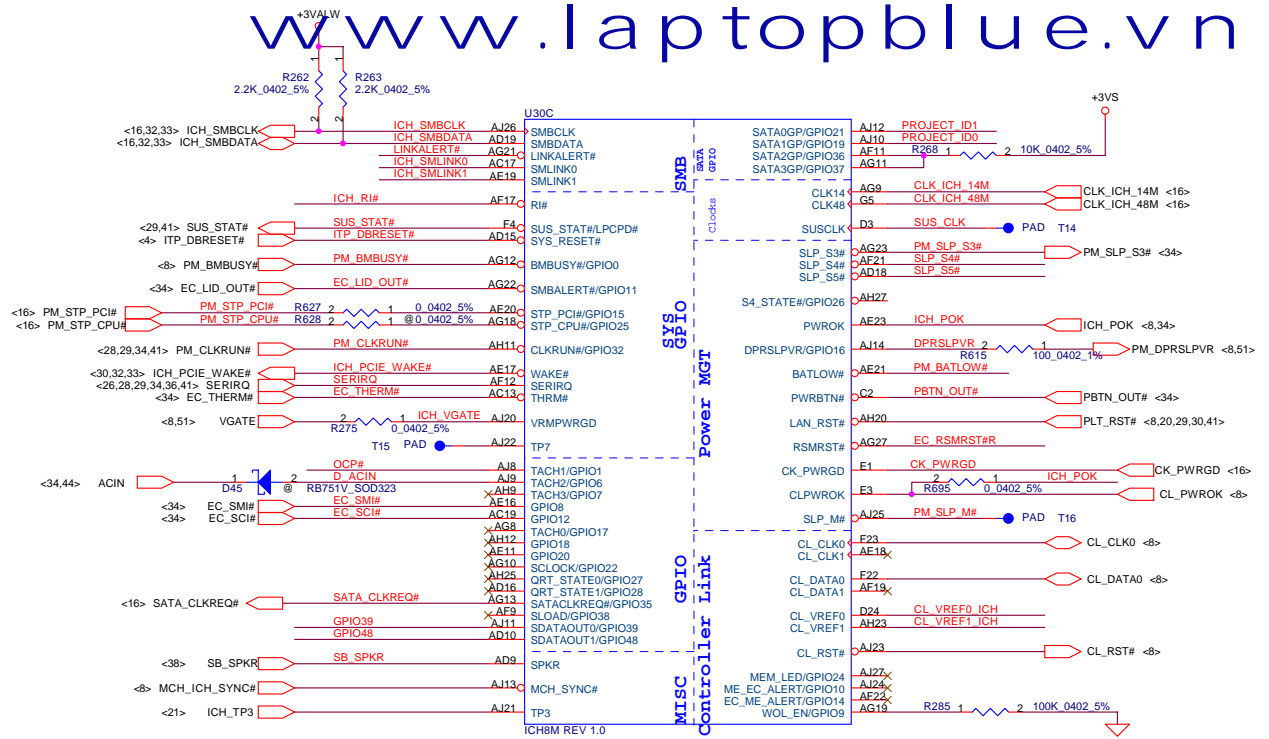
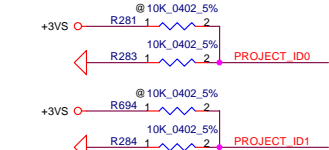




Not in CRB,Keep!



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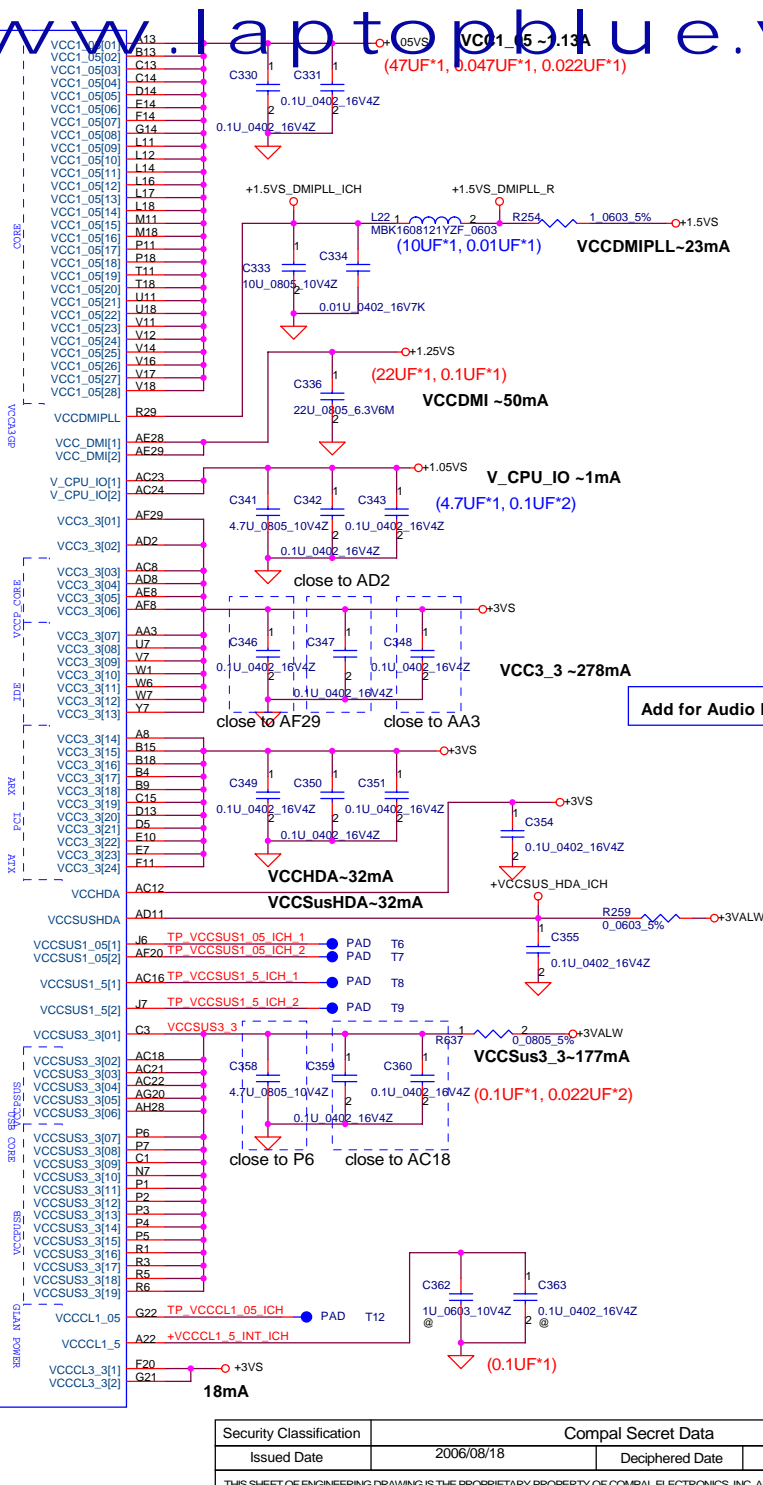
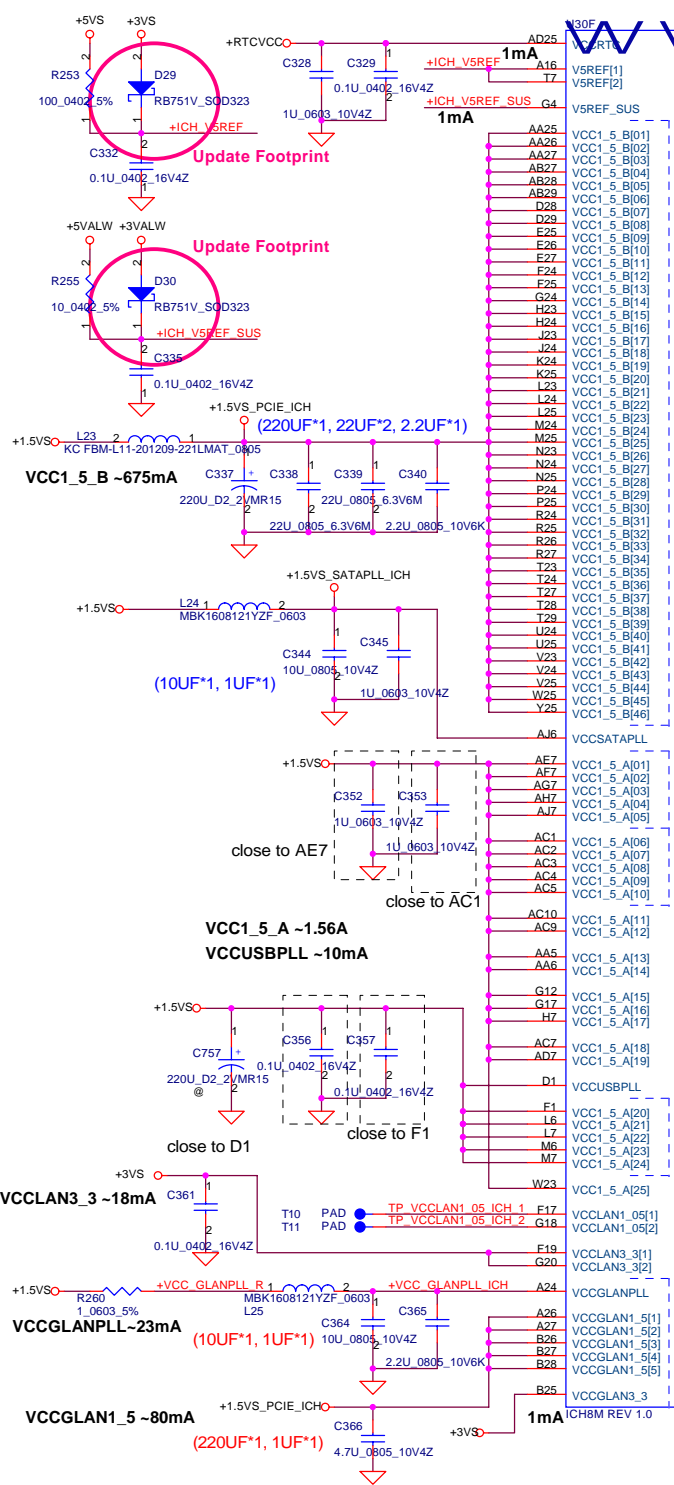
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Title	ICH8M(3/4)-USB,GPIO,PCIE
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Size	Document Number
Custom	IFTXX M/B LA-3541P Schematic

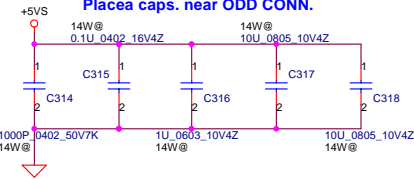
Date:	Wednesday, November 01, 2006	Sheet	22	of	52
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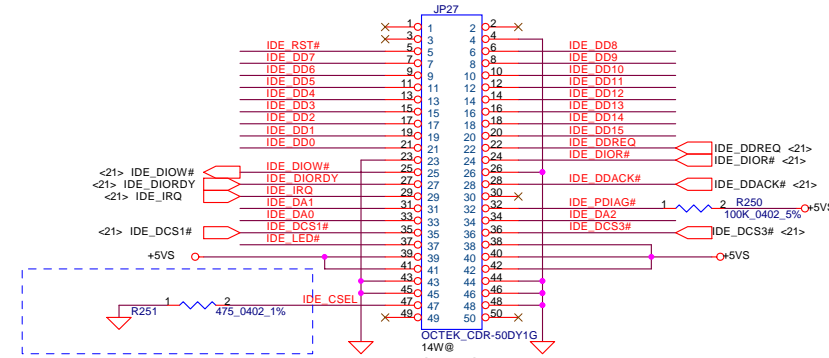
U30E			
A23	VSS0[001]	VSS0[099]	K7
A5	VSS0[002]	VSS0[100]	L1
A2	VSS0[003]	VSS0[101]	L13
AA7	VSS0[004]	VSS0[102]	L15
A25	VSS0[005]	VSS0[103]	L26
AB1	VSS0[006]	VSS0[104]	L27
AB24	VSS0[007]	VSS0[105]	L4
AC11	VSS0[008]	VSS0[106]	L5
AC14	VSS0[009]	VSS0[107]	M12
AC25	VSS0[010]	VSS0[108]	M13
AC26	VSS0[011]	VSS0[109]	M14
AC27	VSS0[012]	VSS0[110]	M15
AD17	VSS0[013]	VSS0[111]	M17
AD20	VSS0[014]	VSS0[112]	M23
AD28	VSS0[015]	VSS0[113]	M28
AD29	VSS0[016]	VSS0[114]	M29
AD3	VSS0[017]	VSS0[115]	M3
AD4	VSS0[018]	VSS0[116]	M3
AD6	VSS0[019]	VSS0[117]	N1
AE1	VSS0[020]	VSS0[118]	N11
AE12	VSS0[021]	VSS0[119]	N12
AE2	VSS0[022]	VSS0[120]	N13
AE22	VSS0[023]	VSS0[121]	N14
AD1	VSS0[024]	VSS0[122]	N15
AE25	VSS0[025]	VSS0[123]	N16
AE5	VSS0[026]	VSS0[124]	N17
AE6	VSS0[027]	VSS0[125]	N18
AE9	VSS0[028]	VSS0[126]	N26
AF14	VSS0[029]	VSS0[127]	N27
AF16	VSS0[030]	VSS0[128]	N4
AF18	VSS0[031]	VSS0[129]	N5
AF3	VSS0[032]	VSS0[130]	N6
AF4	VSS0[033]	VSS0[131]	P12
AG5	VSS0[034]	VSS0[132]	P13
AG6	VSS0[035]	VSS0[133]	P14
AH10	VSS0[036]	VSS0[134]	P15
AH13	VSS0[037]	VSS0[135]	P16
AH16	VSS0[038]	VSS0[136]	P17
AH19	VSS0[039]	VSS0[137]	P23
AH2	VSS0[040]	VSS0[138]	P28
AF28	VSS0[041]	VSS0[139]	P29
AH22	VSS0[042]	VSS0[140]	R11
AH24	VSS0[043]	VSS0[141]	R12
AH26	VSS0[044]	VSS0[142]	R13
AH3	VSS0[045]	VSS0[143]	R14
AH4	VSS0[046]	VSS0[144]	R15
AH8	VSS0[047]	VSS0[145]	R16
AJ5	VSS0[048]	VSS0[146]	R17
B11	VSS0[049]	VSS0[147]	R18
B14	VSS0[050]	VSS0[148]	R28
B17	VSS0[051]	VSS0[149]	R4
B2	VSS0[052]	VSS0[150]	T12
B20	VSS0[053]	VSS0[151]	T13
B22	VSS0[054]	VSS0[152]	T14
B8	VSS0[055]	VSS0[153]	T15
C24	VSS0[056]	VSS0[154]	T16
C26	VSS0[057]	VSS0[155]	T17
C27	VSS0[058]	VSS0[156]	T2
C6	VSS0[059]	VSS0[157]	U12
D12	VSS0[060]	VSS0[158]	U13
D15	VSS0[061]	VSS0[159]	U14
D18	VSS0[062]	VSS0[160]	U15
D2	VSS0[063]	VSS0[161]	U16
D4	VSS0[064]	VSS0[162]	U17
E21	VSS0[065]	VSS0[163]	U23
E24	VSS0[066]	VSS0[164]	U26
E4	VSS0[067]	VSS0[165]	U27
E9	VSS0[068]	VSS0[166]	U3
F15	VSS0[069]	VSS0[167]	U6
F28	VSS0[070]	VSS0[168]	V13
F29	VSS0[071]	VSS0[169]	V15
F7	VSS0[072]	VSS0[170]	V28
G1	VSS0[073]	VSS0[171]	V29
G2	VSS0[074]	VSS0[172]	W2
G10	VSS0[075]	VSS0[173]	W26
G13	VSS0[076]	VSS0[174]	W27
G19	VSS0[077]	VSS0[175]	Y28
G19	VSS0[078]	VSS0[176]	Y29
G23	VSS0[079]	VSS0[177]	Y4
G25	VSS0[080]	VSS0[178]	AB4
G26	VSS0[081]	VSS0[179]	AB23
G27	VSS0[082]	VSS0[180]	AB5
H25	VSS0[083]	VSS0[181]	AB6
H28	VSS0[084]	VSS0[182]	AD5
H29	VSS0[085]	VSS0[183]	U4
H3	VSS0[086]	VSS0[184]	W24
H6	VSS0[087]		
J1	VSS0[088]	VSS_NCTF[01]	A1
J25	VSS0[089]	VSS_NCTF[02]	A2
J27	VSS0[090]	VSS_NCTF[03]	A28
J4	VSS0[091]	VSS_NCTF[04]	A29
J5	VSS0[092]	VSS_NCTF[05]	AH1
K23	VSS0[093]	VSS_NCTF[06]	AH29
K29	VSS0[094]	VSS_NCTF[07]	A11
K29	VSS0[095]	VSS_NCTF[08]	A12
K3	VSS0[096]	VSS_NCTF[09]	A18
K6	VSS0[097]	VSS_NCTF[10]	A29
VSS0[098]	VSS_NCTF[11]	B1	</

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title			
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				Size	Document Number	Rev	
				Custom	ICL50/ICK70 M/B LA-3551P Schematic	0	
				Date:	Wednesday, November 01, 2006	Sheet	23 of 52

Place caps. near ODD CONN.

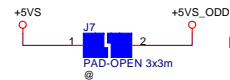


<21> IDE_DD[0..15] IDE DD[0..15]
<21> IDE_DA[0..2] IDE DA[0..2]



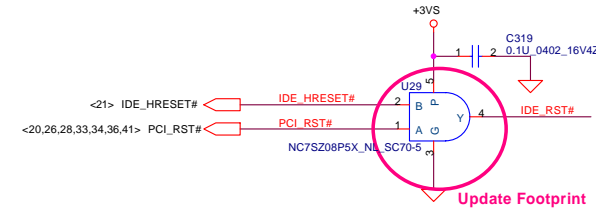
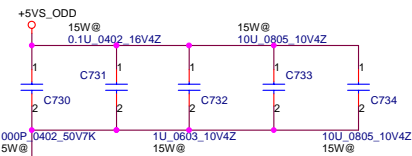
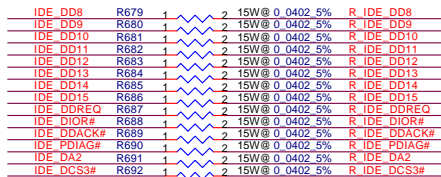
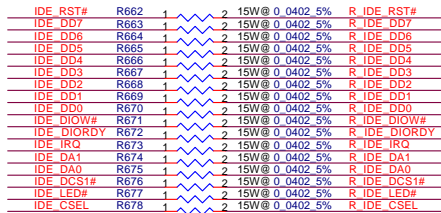
IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

(NEW)

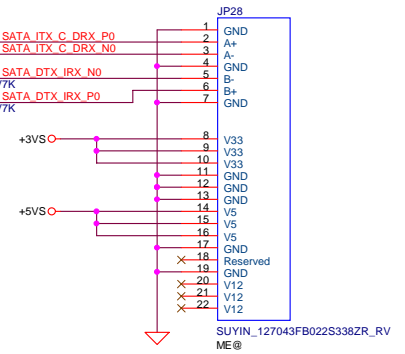
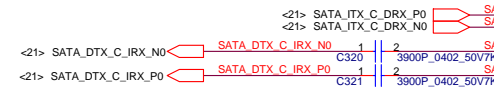
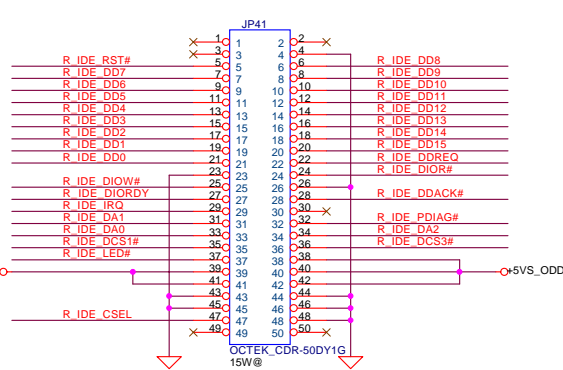
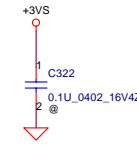
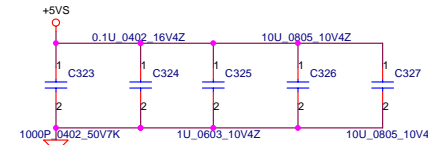


Remember Short at 15W@

15W ODD Conn.



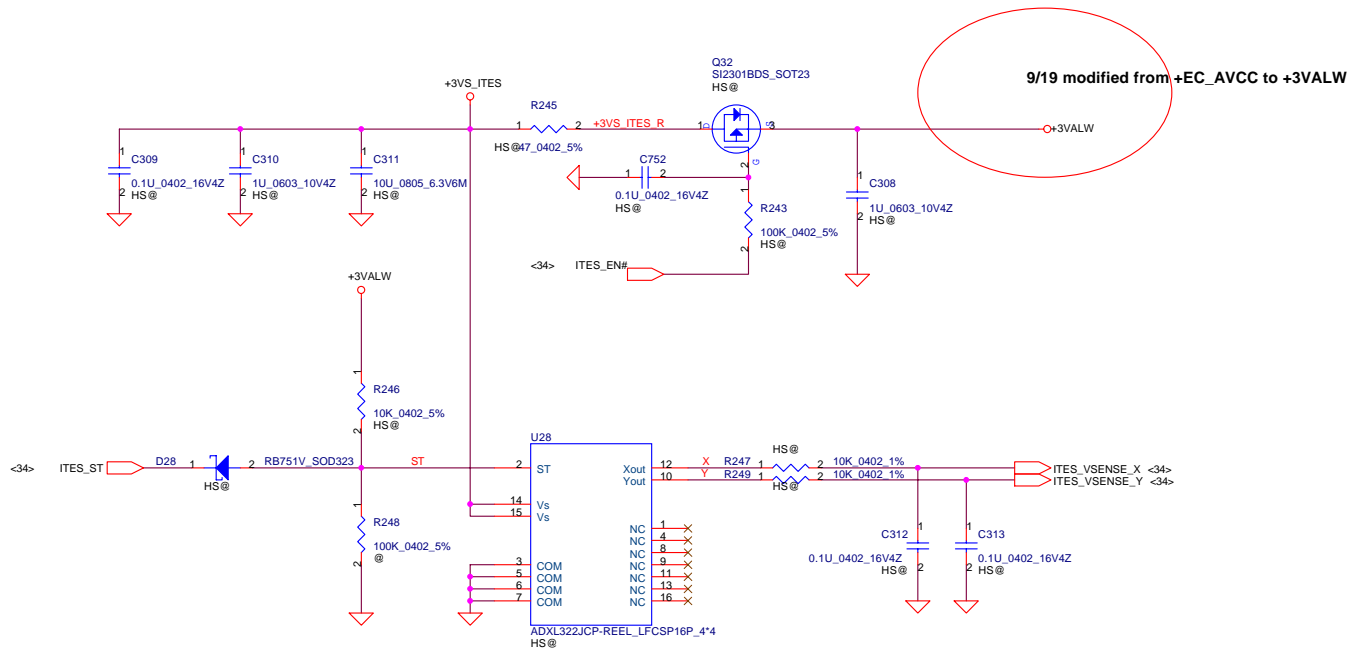
SATA HDD Conn.



(NEW)
Change Library

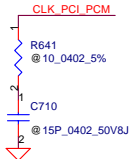
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	IFTXX M/B LA-3541P Schematic		Rev 0	
Date:	Wednesday, November 01, 2006	Sheet	24	of 52	

Note : BOM structure HS@ is for Heng shan IFT10/11 this model

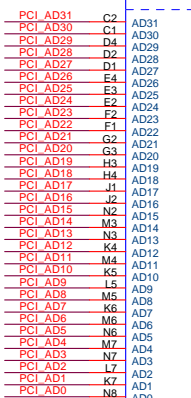
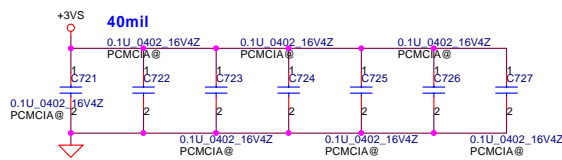
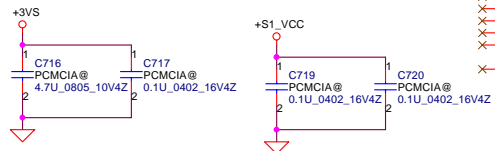
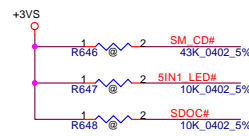
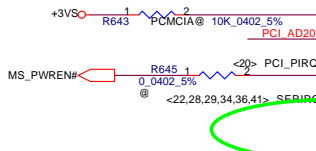


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				LA-3541P	
				Date: Wednesday, November 01, 2006	Rev 0.1
				Sheet 25 of 52	

<20,28> PCI_AD[0..31] \rightarrow PCI_AD[0..31]
<20,28> PCI_CBE#[0..3] \rightarrow PCI_CBE#[0..3]

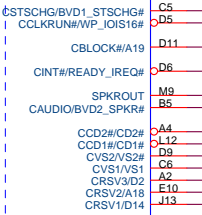
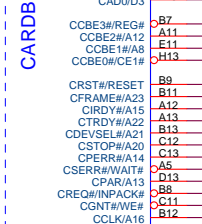


<20,24,28,33,34,36,41> PCI_RST# \rightarrow PCI_RST#
<20,28> PCI_FRAME# \rightarrow PCI_FRAME#
<20,28> PCI_IRDY# \rightarrow PCI_IRDY#
<20,28> PCI_TRDY# \rightarrow PCI_TRDY#
<20,28> PCI_DEVSEL# \rightarrow PCI_DEVSEL#
<20,28> PCI_STOP# \rightarrow PCI_STOP#
<20,28> PCI_PERR# \rightarrow PCI_PERR#
<20,28> PCI_SERR# \rightarrow PCI_SERR#
<20,28> PCI_PAR# \rightarrow PCI_PAR#
<20> PCI_REQ#2 \rightarrow PCI_REQ#2
<20> PCI_GNT#2 \rightarrow PCI_GNT#2
<16> CLK_PCI_PCM \rightarrow CLK_PCI_PCM

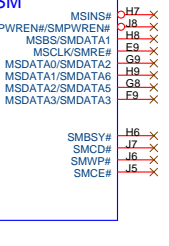


PCI Interface

CARDBUS

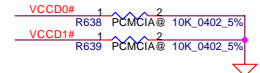
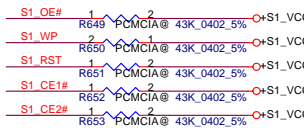
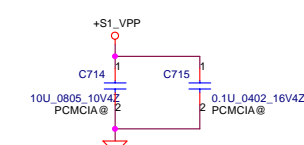
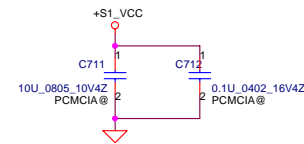
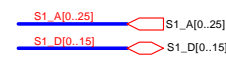
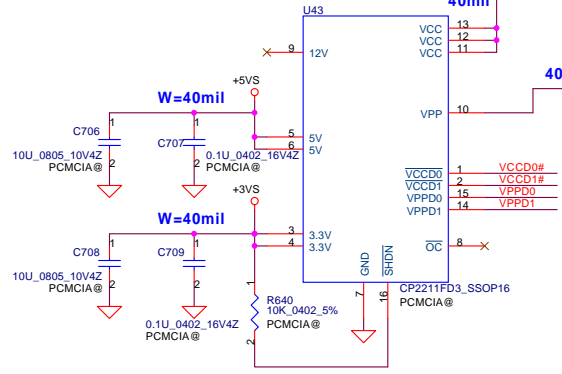


SD/MMC/MS/SM

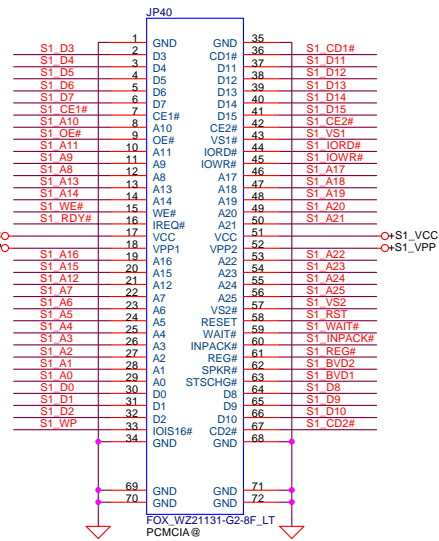


10/17 : FootPrint : SA007140B10
BOM : SA014100310

CB1410 P/N: SA014100310



PCMCIA Socket



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		Custom		IFTXX LA-3541P		0.1		Sheet		26 of 52	

D

C

B

A

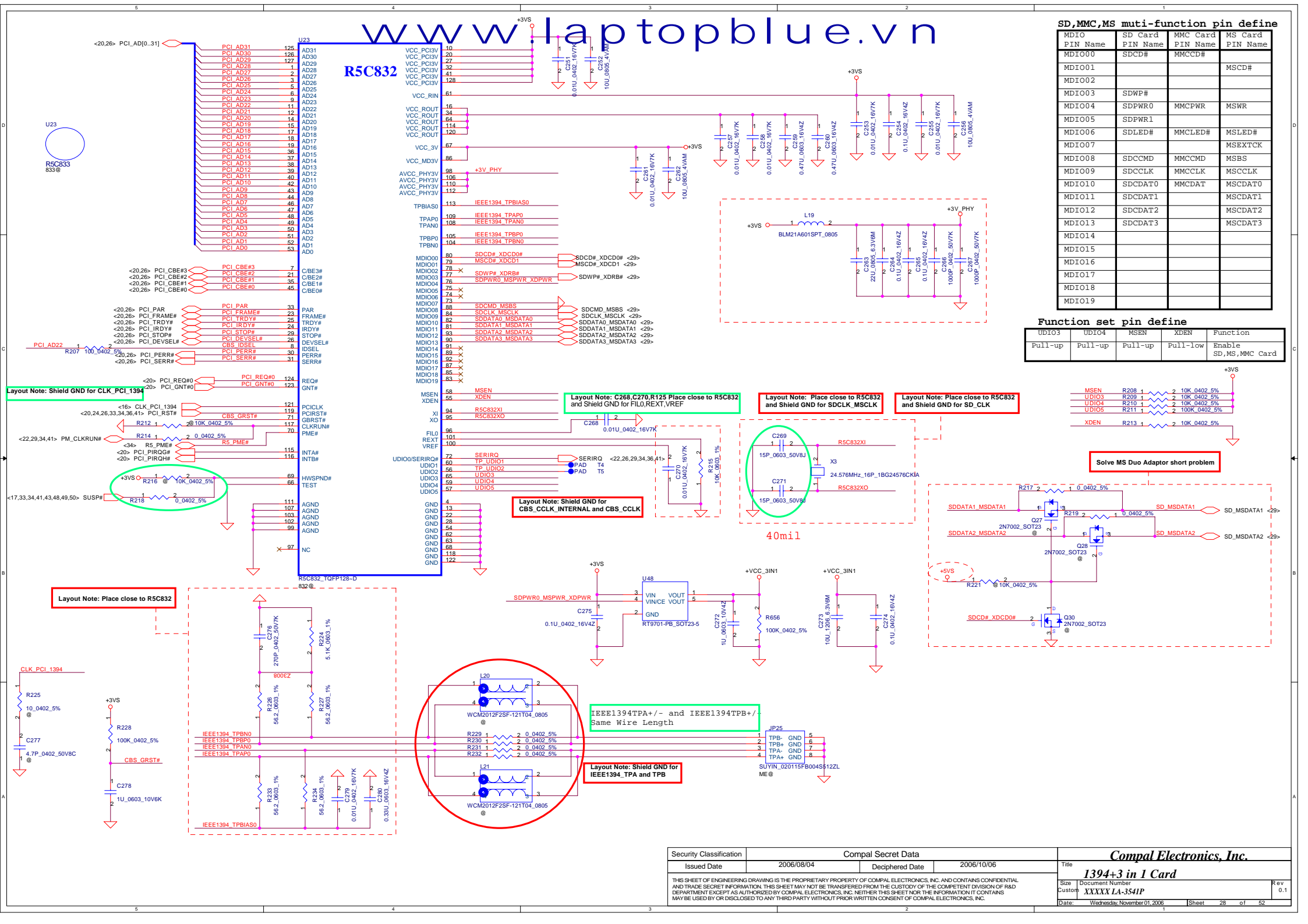
D

C

B

A

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, November 01, 2006		Sheet 27 of 52

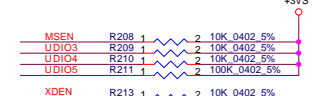


SD,MMC,MS multi-function pin define

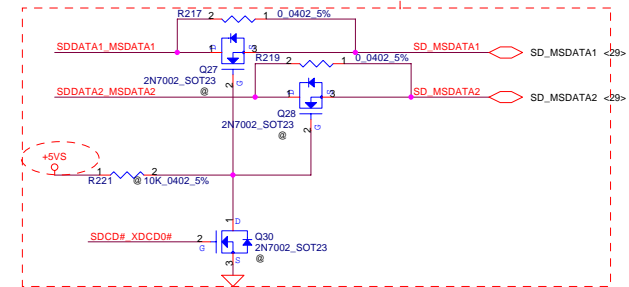
MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
MDIO0	SDCD#	MMCCD#	
MDIO01			MSCD#
MDIO02			
MDIO03	SDWP#		
MDIO04	SDPWR0	MMCPWR	MSWR
MDIO05	SDPWR1		
MDIO06	SDLED#	MMCLED#	MSLED#
MDIO07			MSEXTCK
MDIO08	SDCCMD	MMCCMD	MSBS
MDIO09	SDCLK	MMCLK	MSCCLK
MDIO10	SDCDAT0	MMCDAT	MSCDAT0
MDIO11	SDCDAT1		MSCDAT1
MDIO12	SDCDAT2		MSCDAT2
MDIO13	SDCDAT3		MSCDAT3
MDIO14			
MDIO15			
MDIO16			
MDIO17			
MDIO18			
MDIO19			

Function set pin define

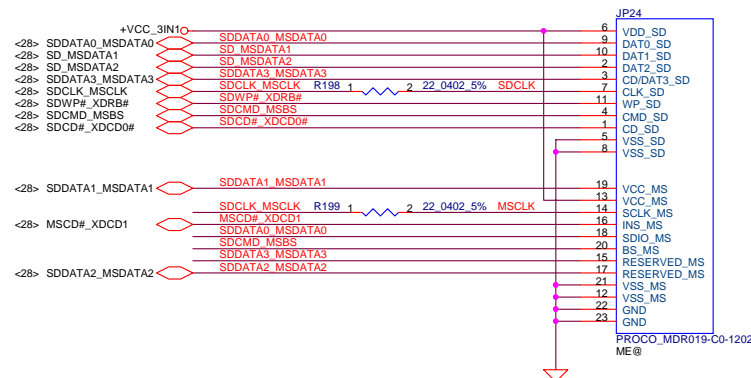
UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-low	Enable SD, MS, MMC Card



Solve MS Duo Adaptor short problem

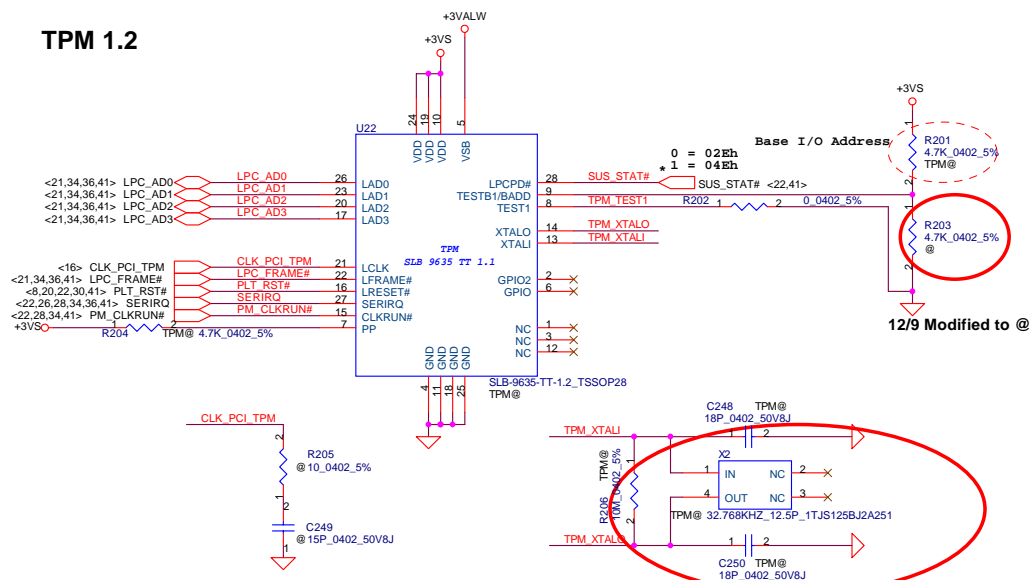


3 in 1 Card Reader

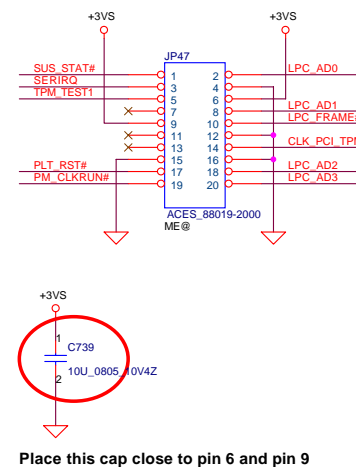


For A30

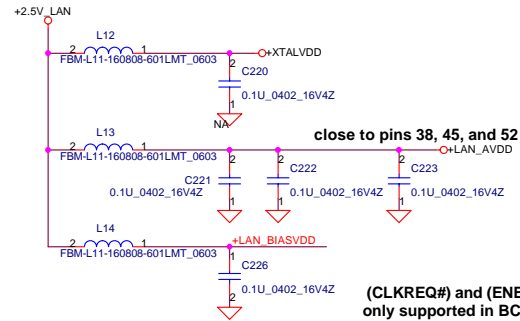
TPM 1.2



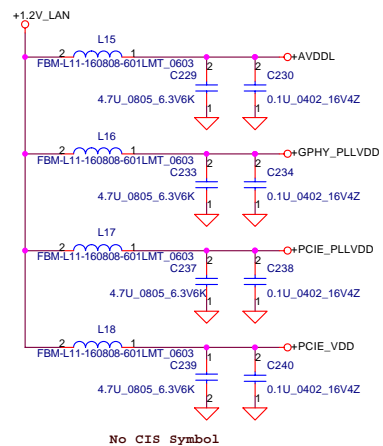
TPM Conn. For C38



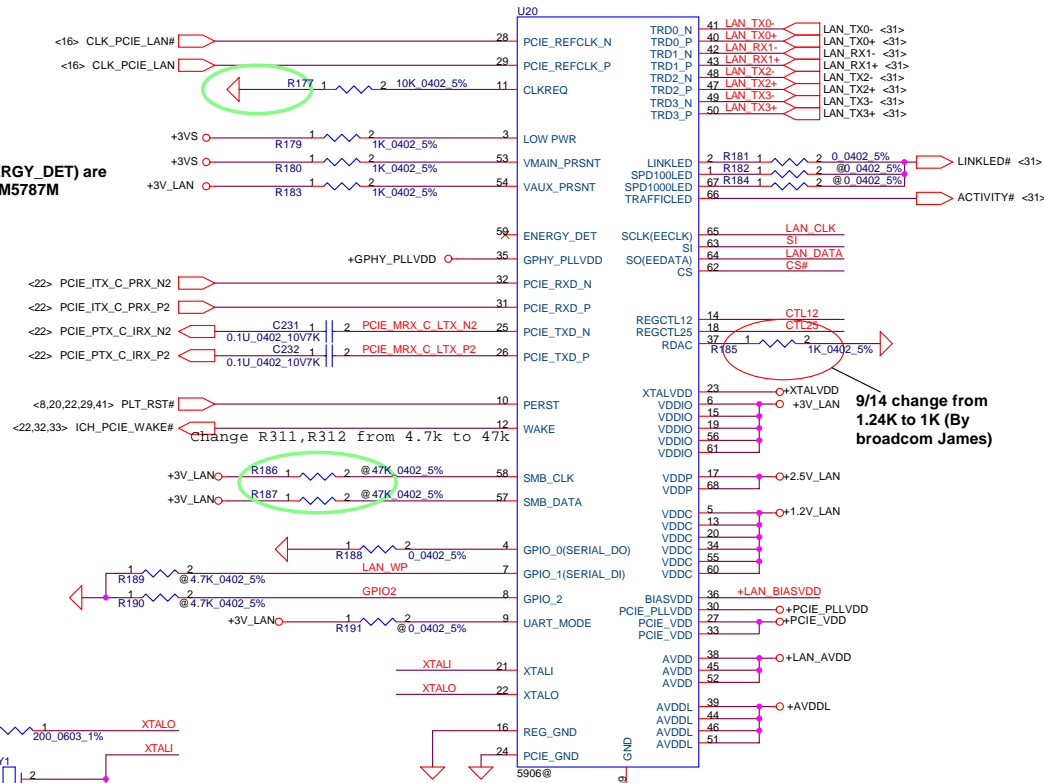
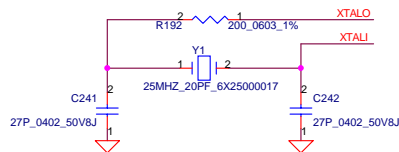
Layout Notice : Filter place as close chip as possible.



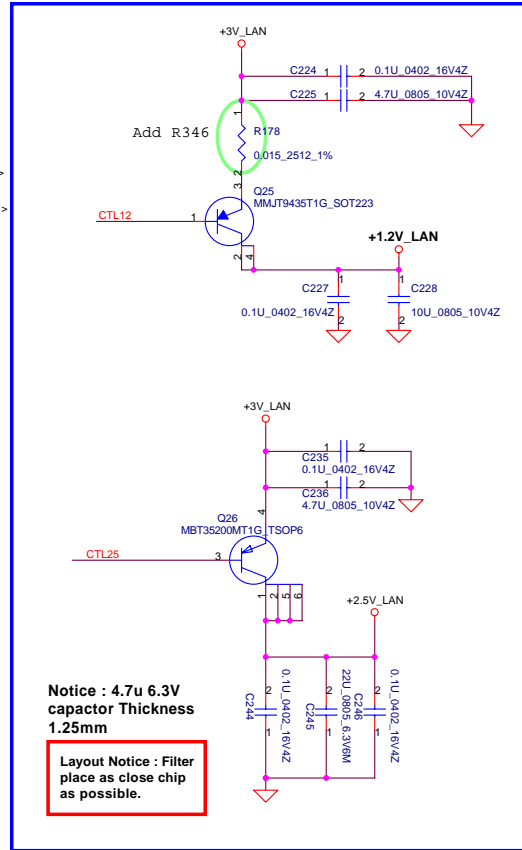
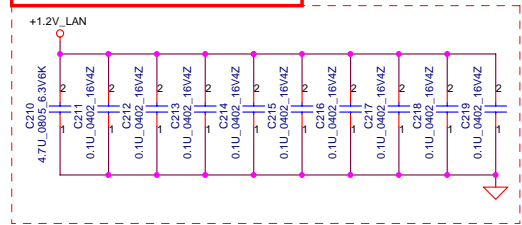
(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M



No CIS Symbol

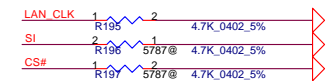
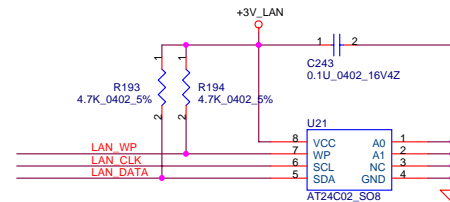


9/14 change from
1.24K to 1K (By
broadcom James)



**Notice : 4.7u 6.3V
capacitor Thickness
1.25mm**

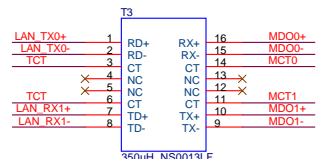
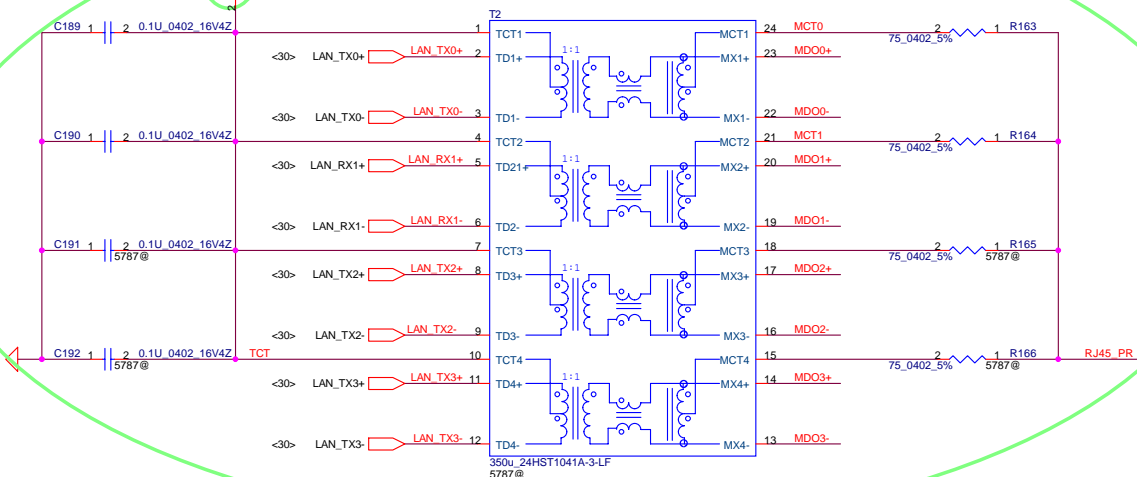
**Layout Notice : Filter
place as close chip
as possible.**



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				Customer	XXXXX LA-3541P	0.1	
Date: Wednesday, November 01, 2006				Sheet	30	of 52	

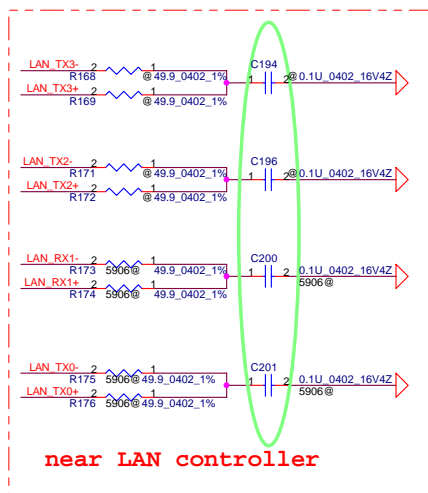
Change L1 from SD013000080 to SM010005500

Change T2 from SP050002130 to SP050002140



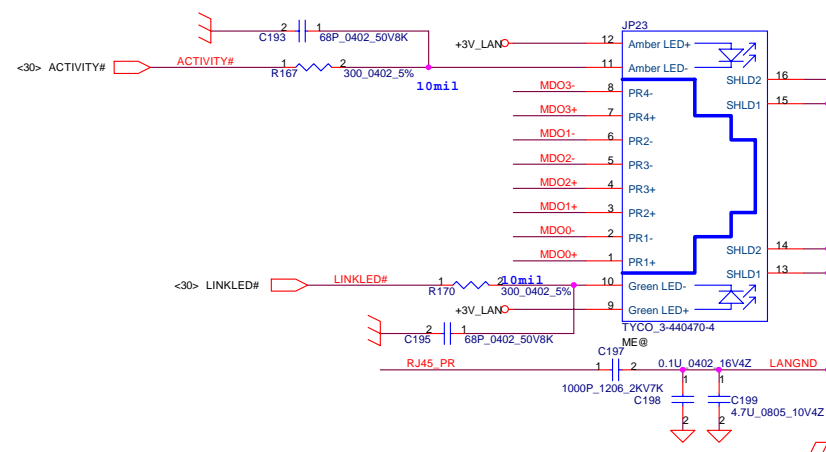
Change T1 from SP050001210 to SP050001210

Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



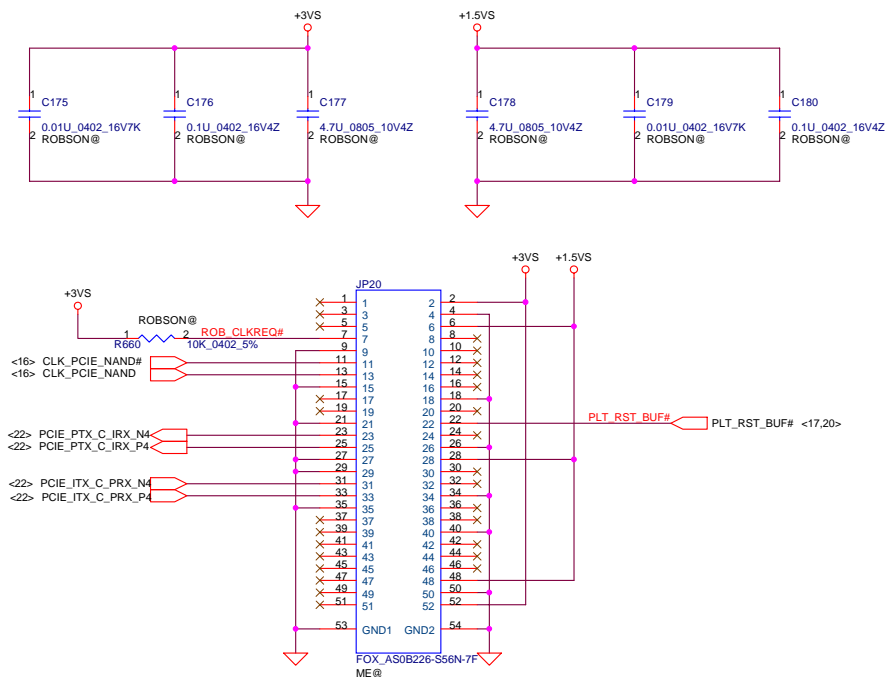
near LAN controller

Lan Conn.

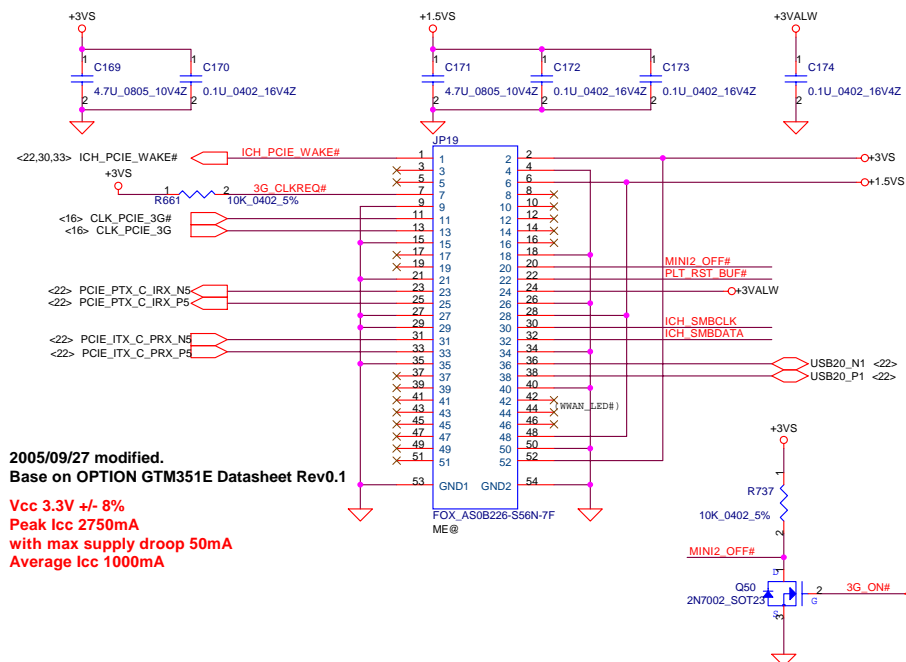


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Size		Document Number		Rev	
Custom		XXXXX LA-3541P		0.1	
Date:		Wednesday, November 01, 2006		Sheet 31 of 52	

NAND mini Card(Robson support) www.laptopblue.vn Mini-Express Card for 3G Or TV Tuner



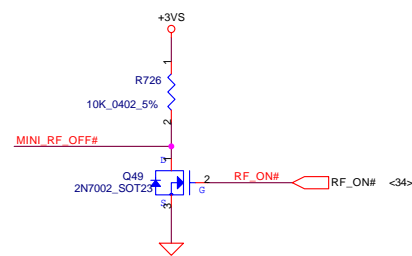
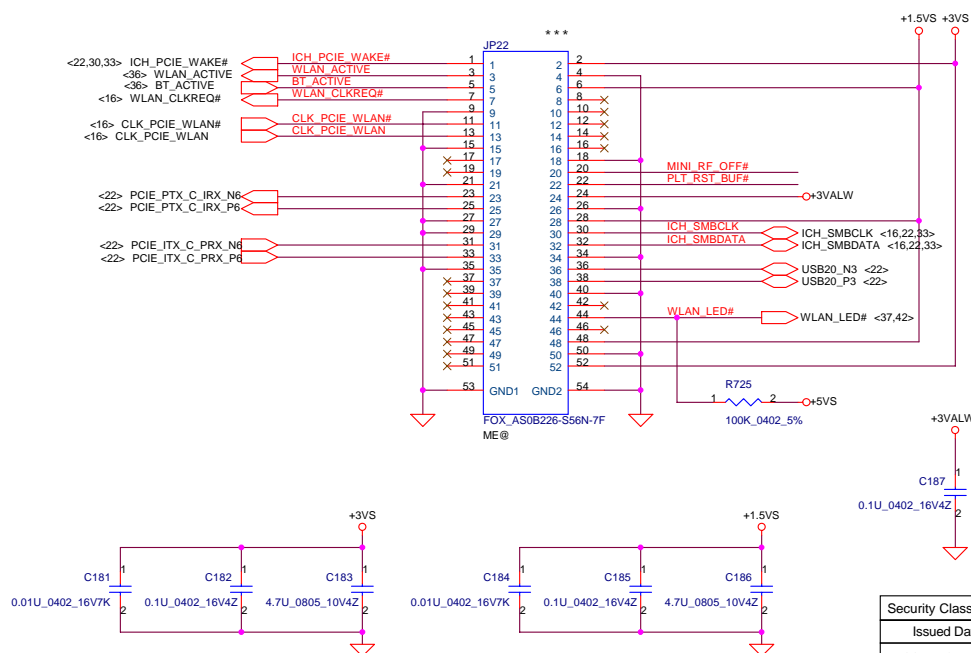
Mini-Express Card for 3G Or TV Tuner



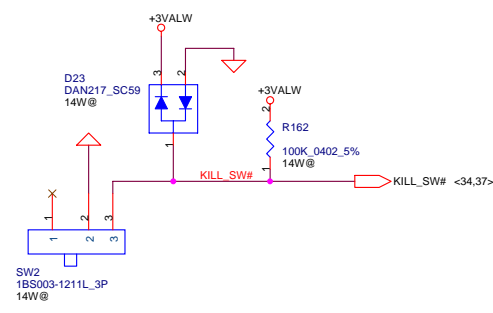
2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

Mini-Express Card for WLAN



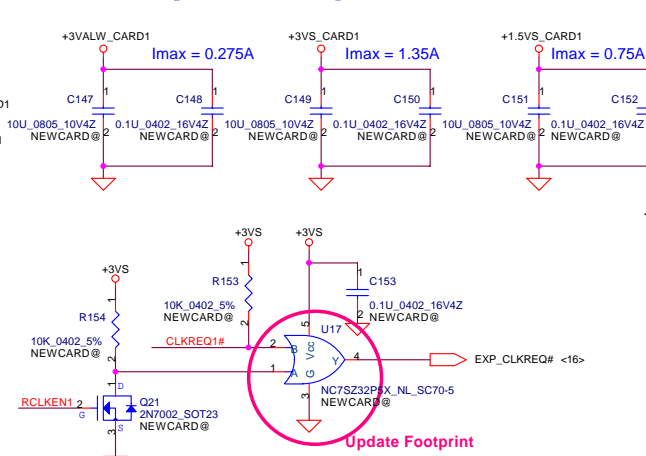
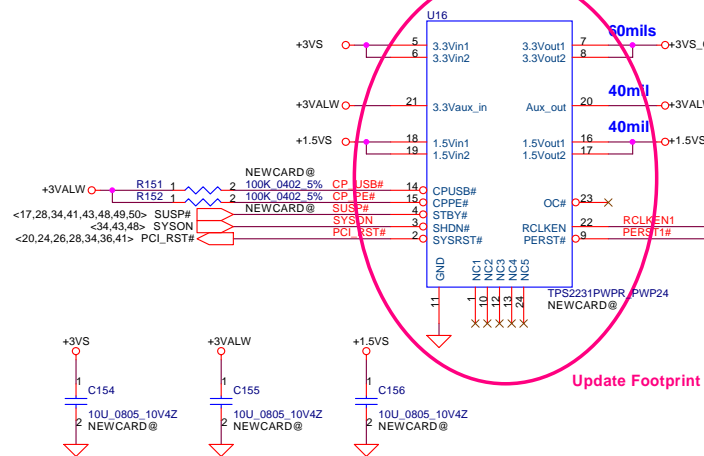
Kill SWITCH



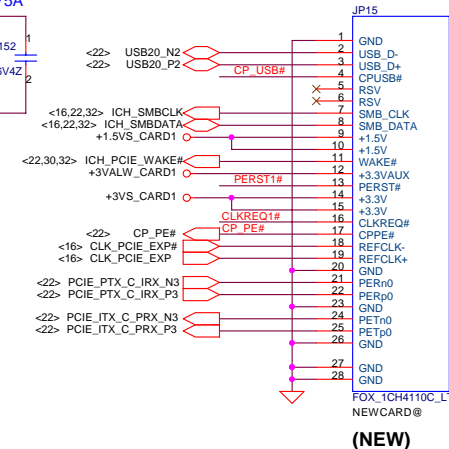
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Issued Date		2006/08/05		Deciphered Date		2007/08/05		Title					
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						Size	Document Number			LA- 3541P		Rev	0.1
						Date:	Wednesday, November 01, 2006		Sheet	32	of	52	

New Card Power Switch

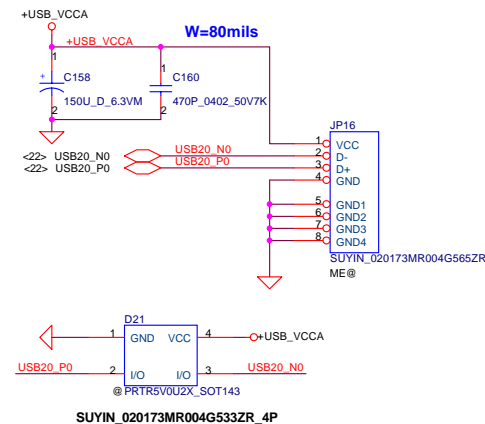
www.laptopblue.vn



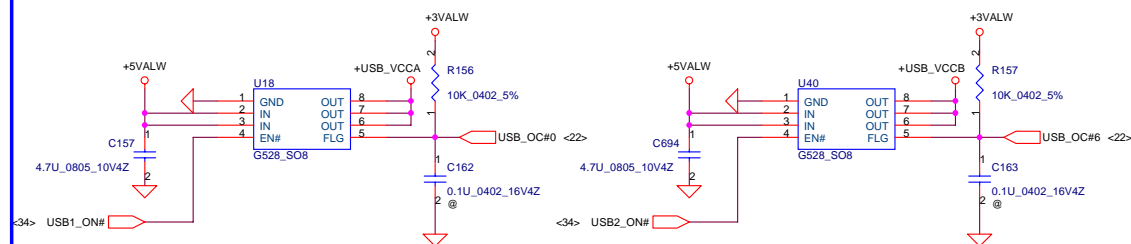
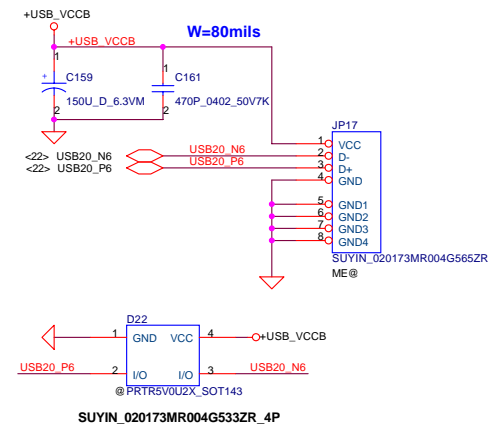
New Card Socket (Left/TOP)



USB CONN. 1

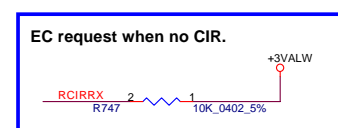


USB CONN. 2



9/17 modified this block

Security Classification		Compal Secret Data		Title	
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				IFITXX M/B LA-3541P Schematic	
				Date:	Wednesday, November 01, 2006
				Sheet	33 of 52



KB925 should use Data code 06361 which has fixed bonding issue
KB925 pin 139 is used for XCI KO. Pin 140 NC

10/17 : FootPrint : SA009100120
BOM : SA000001H700

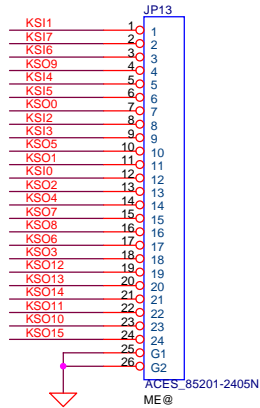
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Issued Date	2006/08/04	Deciphered Date	2006/10/06
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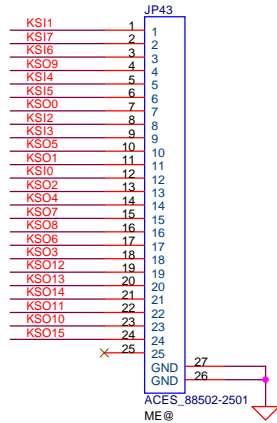
ENE-KB925

Document Number	Rev
IEL10 LA-3451P	0.1

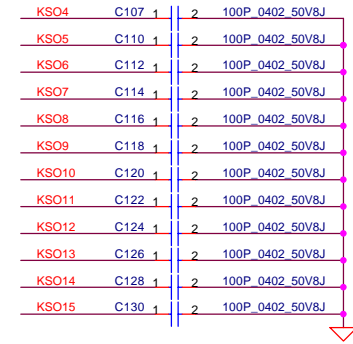
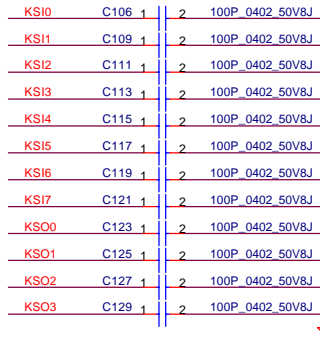
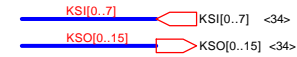
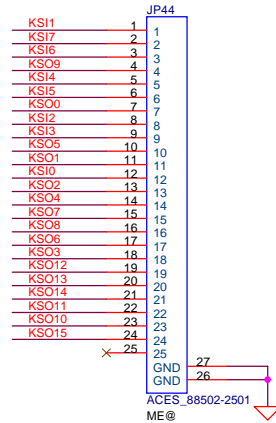
For IFT10



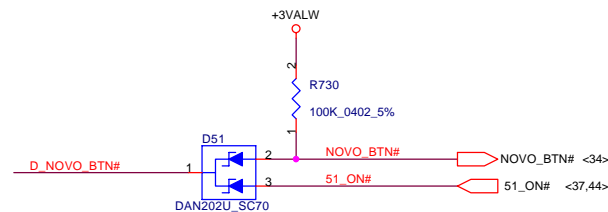
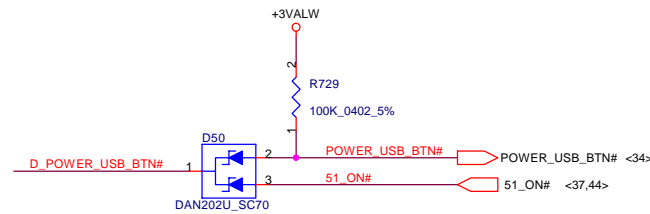
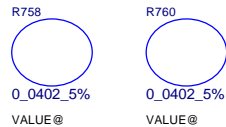
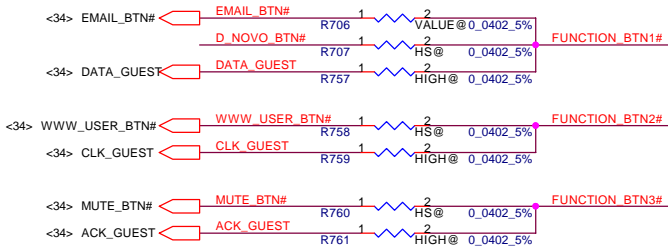
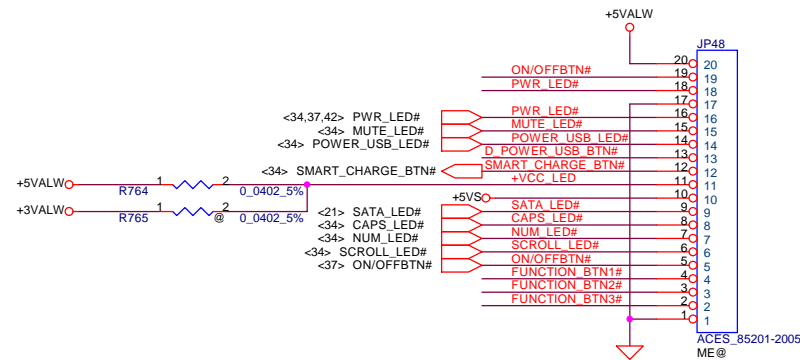
For IFL90



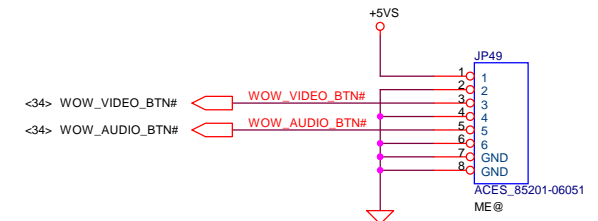
For IFT00



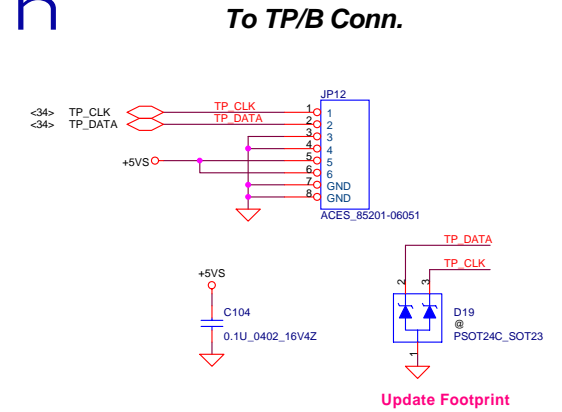
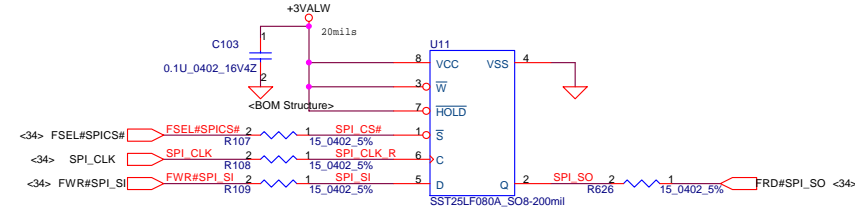
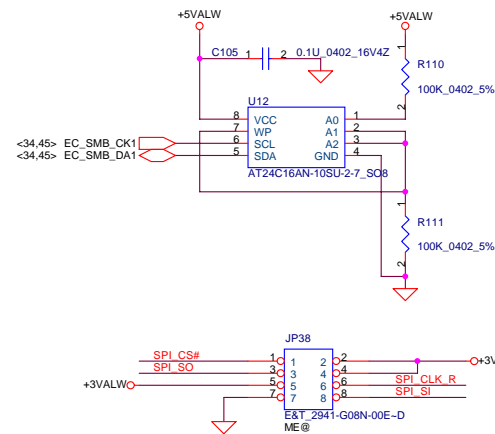
Switch Board Conn.



Video Switch Board Conn.

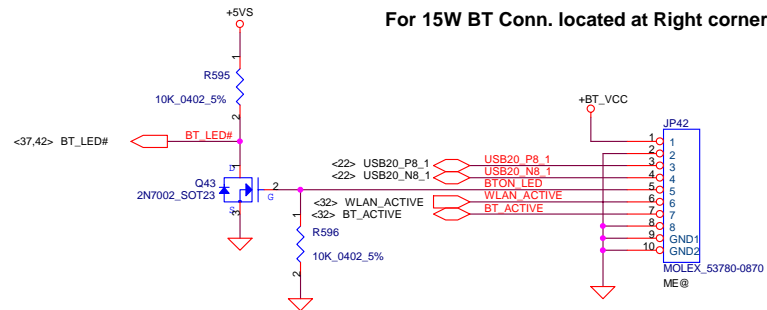


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Size	Document Number	IFTXX M/B LA-3541P Schematic		Rev	0
Date:	Wednesday, November 01, 2006	Sheet	35	of	52

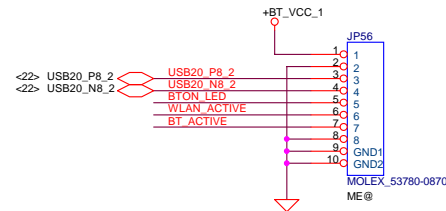


Bluetooth Conn.

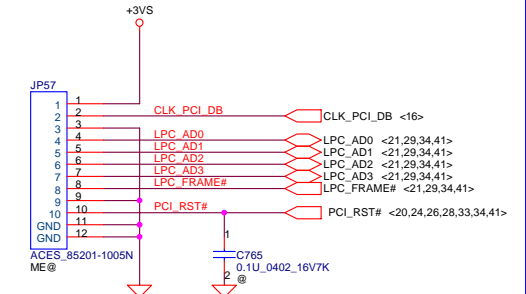
Need to check BT pin definition again!
9/20 modified this block



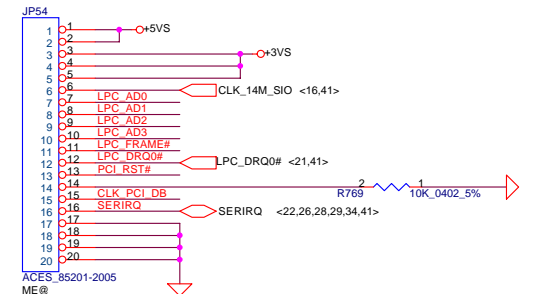
For 14W BT Conn. located at Left corner



FOR LPC DEBUG PORT



FOR LPC SIO DEBUG PORT

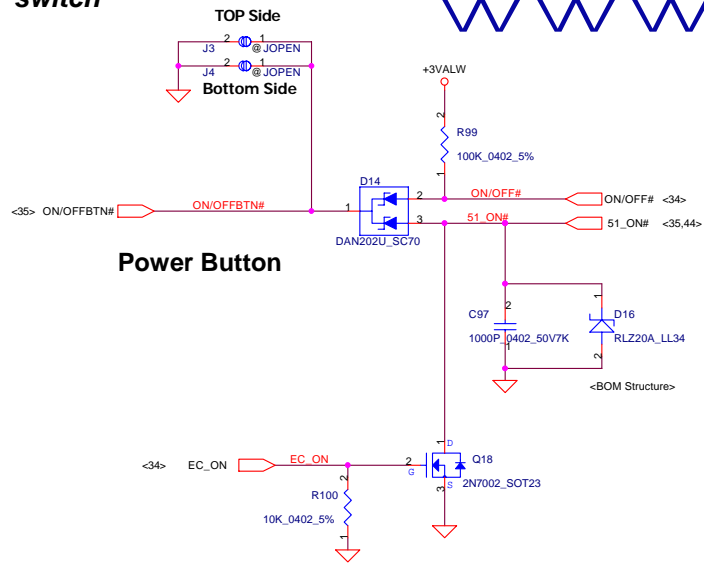


9/29 follow HEL80's

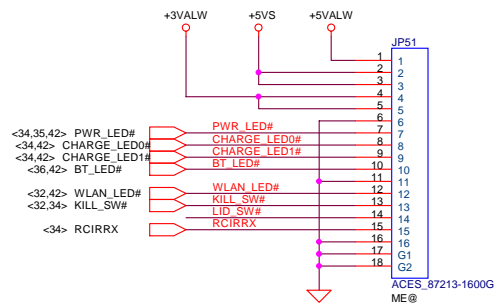
9/29 follow HEL80's

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				Deciphered Date				BIOS, I/O Port & K/B Connector			
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								Document Number			
								IFTXX M/B LA-3541P Schematic			
								Rev			
								0			
								Date: Wednesday, November 01, 2006			
								Sheet 36 of 52			

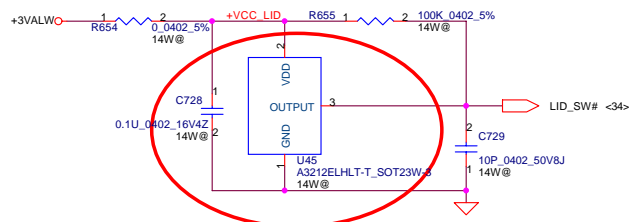
ON/OFF switch



Front LED Board

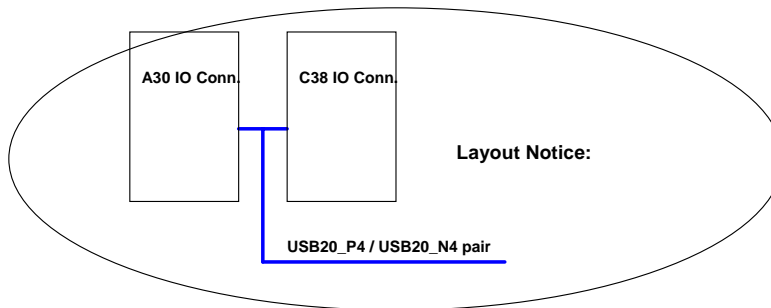


Lid Switch

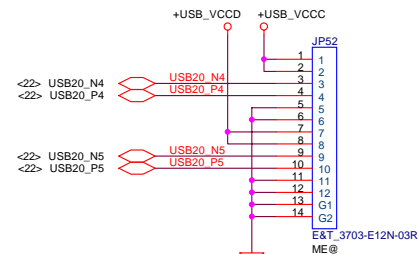


12/9 Change to SA032120010

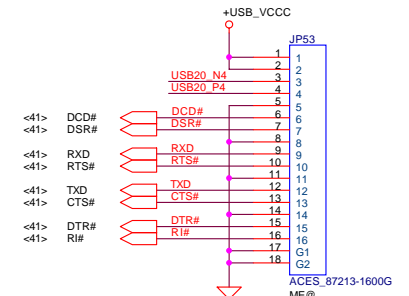
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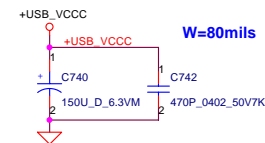
For A30 IO Conn.



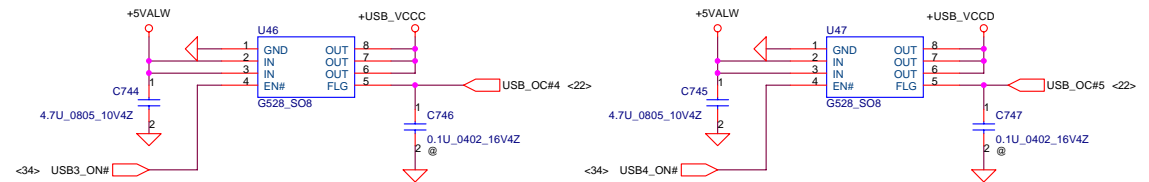
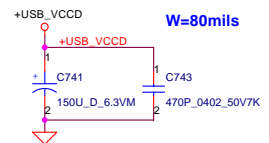
For C38 IO Conn.



To USB CONN. 3

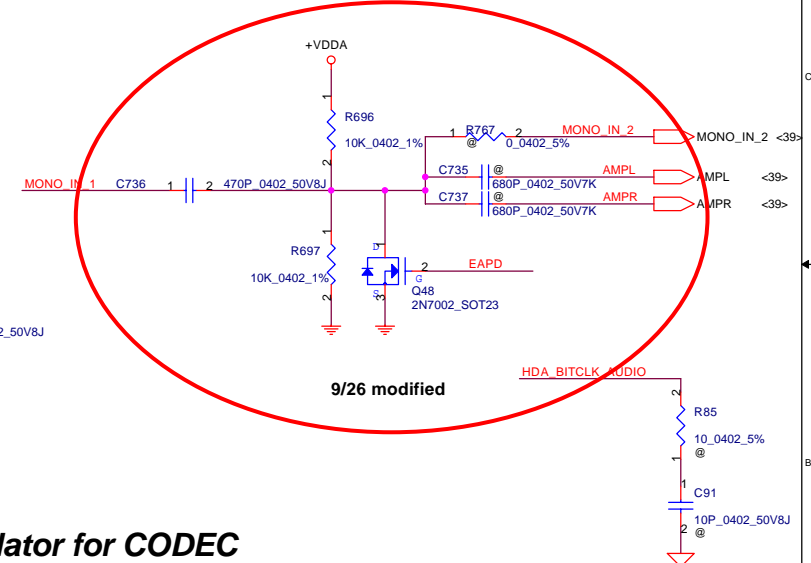
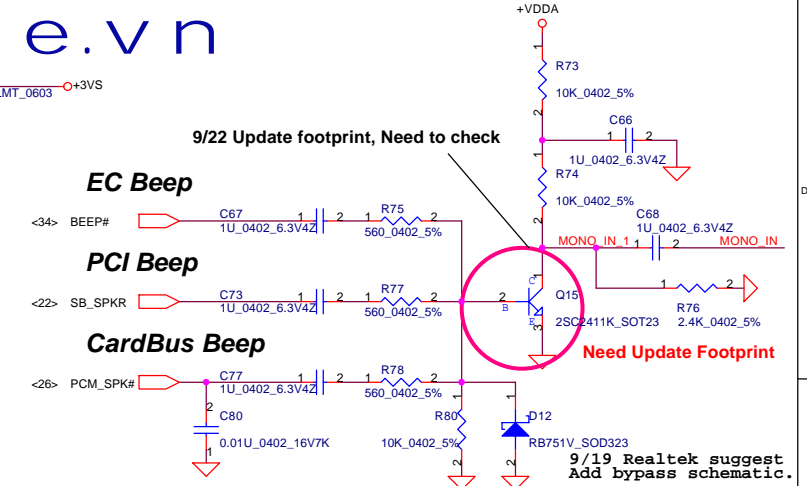
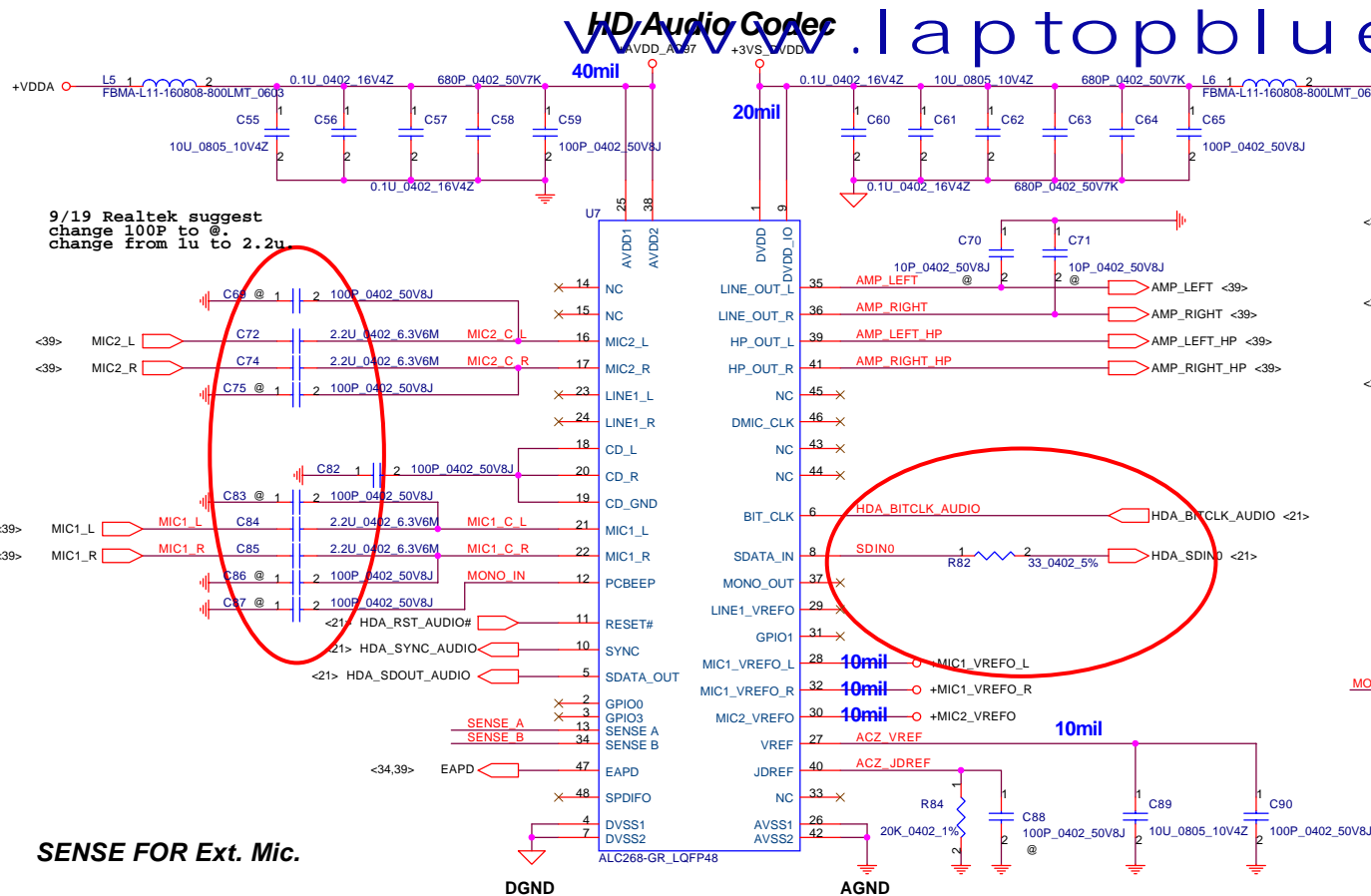


To USB CONN. 4



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Size B	Document Number	IFTXX MB LA-3541P Schematic		Rev 0	
Date:	Wednesday, November 01, 2006	Sheet	37	of	52

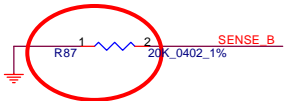
HD Audio Codec



SENSE FOR Ext. Mic.



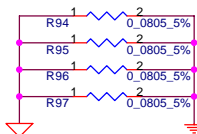
SENSE FOR Solo Int. Mic.



SENSE FOR HP

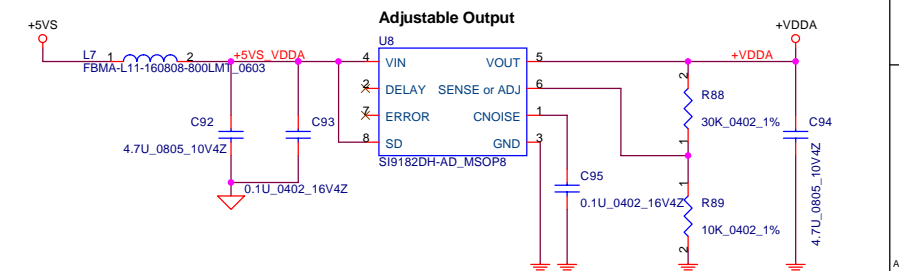


Moat Bridge



Sense Pin	Impedance	Codec Signals	Funnnction
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
	5.1K	PORT-D (PIN 35, 36)	LINE Out
SENSE B	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE Out

Regulator for CODEC







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				Custom	LA-3541P	0.1	
				Date:	Wednesday, November 01, 2006	Sheet 38 of 52	

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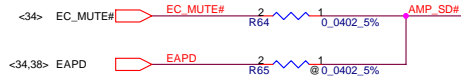
$$f_o = 1 / (2 * 3.14 * R * C) = 106 \text{ Hz}$$

$$R = 1.5 \text{ K} / C = 1 \mu\text{F}$$

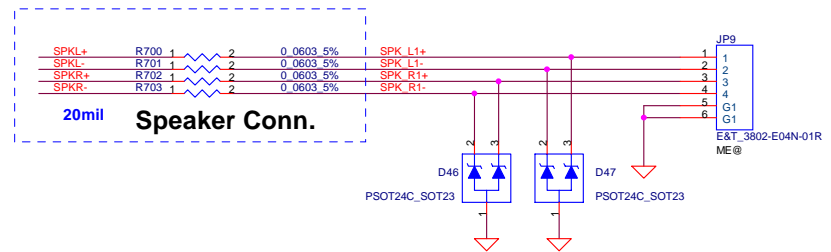
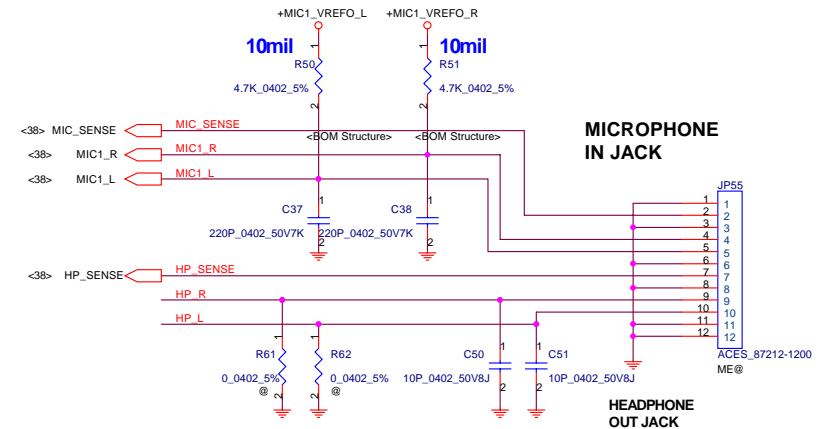
<38> AMP_RIGHT_HP   1 2
C43 4.7U₁

<38> AMP_LEFT_HP   1 2
C44 4.7U₁

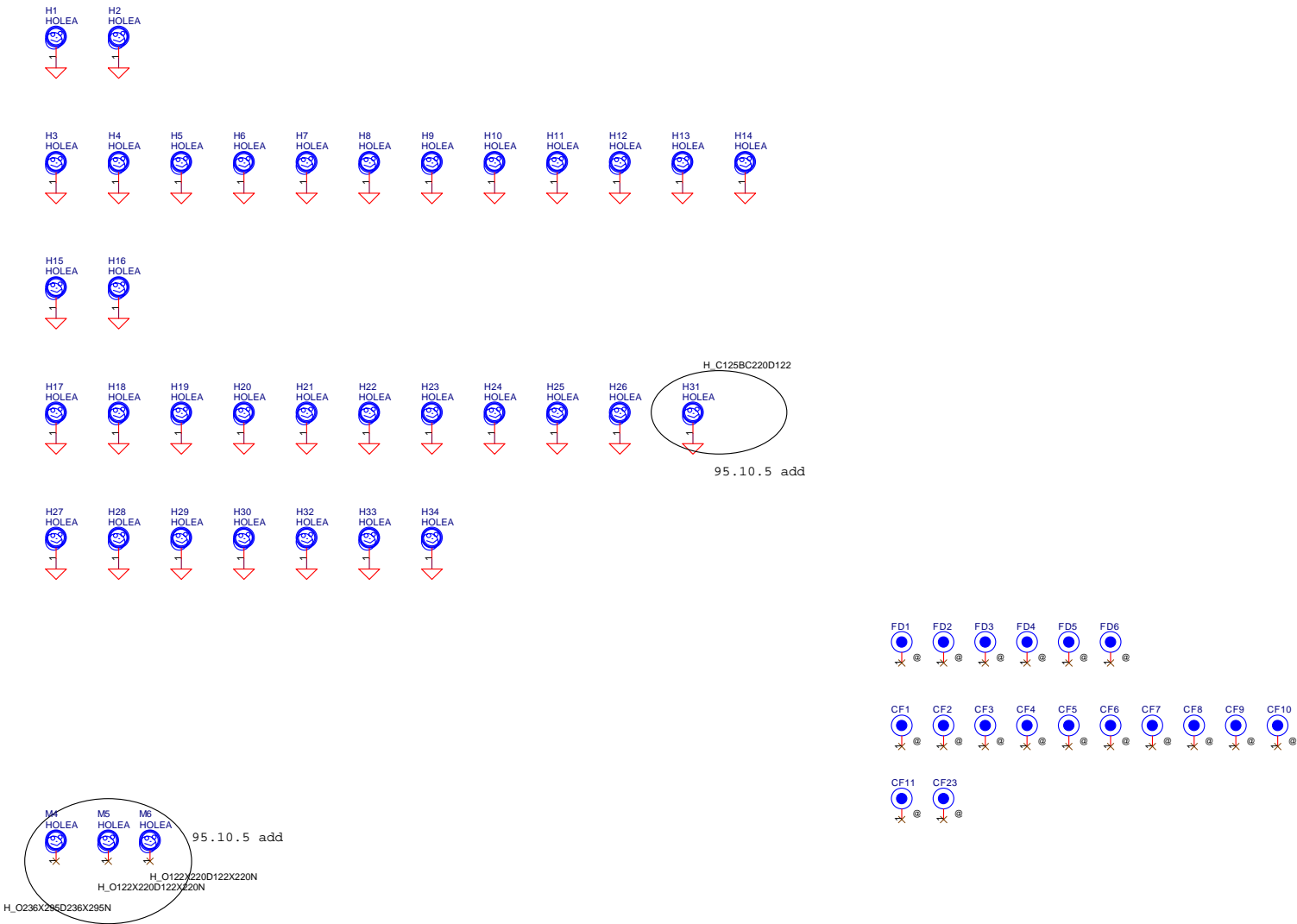
IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)



The schematic diagram illustrates the microphone input circuit for the ACES_88231-02001. It features two channels, MIC2_L and MIC2_R, each connected to a microphone (MIC L1 and MIC R1) via a 4.7K 0402 5% resistor (R70 and R71) and a 220P 0402 50V7K capacitor (C52). The input signal is derived from MIC2_VREFO and MIC2_VREFO. The output of the MIC2_L channel is labeled <3B> and the output of the MIC2_R channel is labeled <3B>.



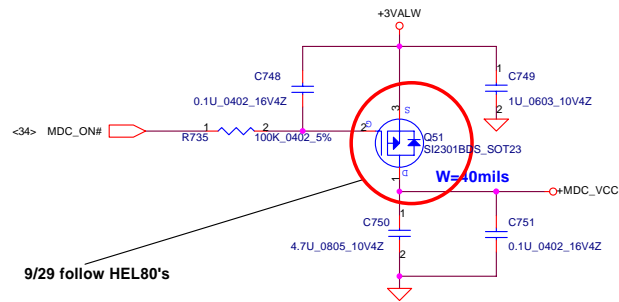
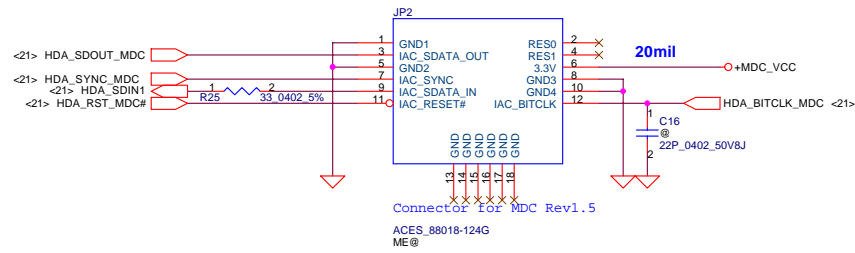
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Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title	AMP/VR/Audio Jack/MIC	
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				Custom	LA-3541P	0.1
				Date:	Wednesday, November 01, 2006	Sheet 39 of 52



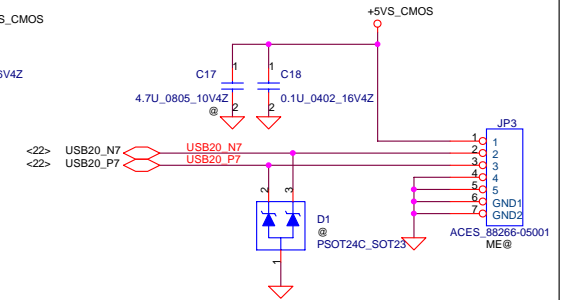
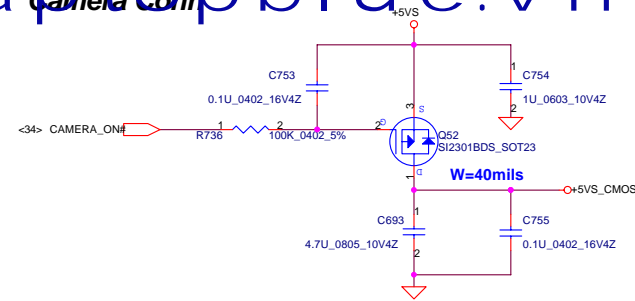
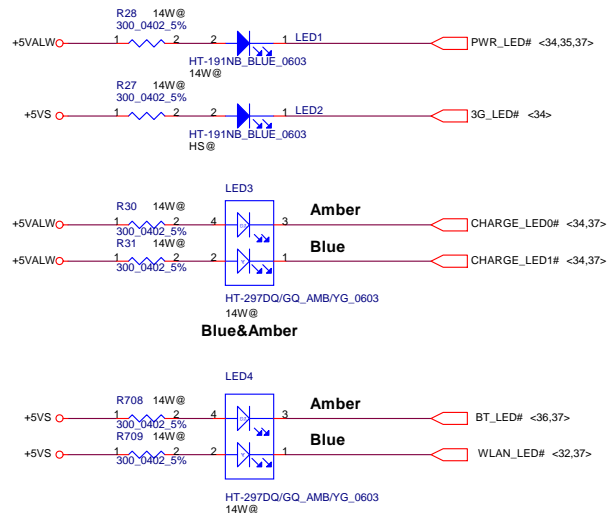
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					FAN & Screw Hole
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B					0
Date:		Wednesday, November 01, 2006	Sheet	40	of 52



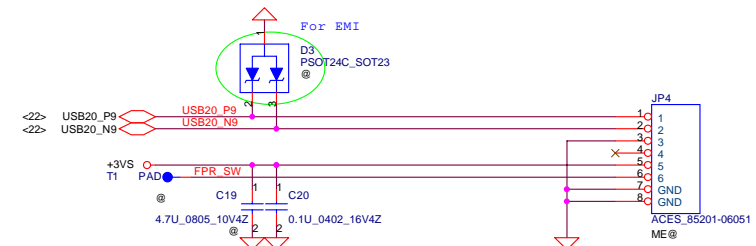
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LED

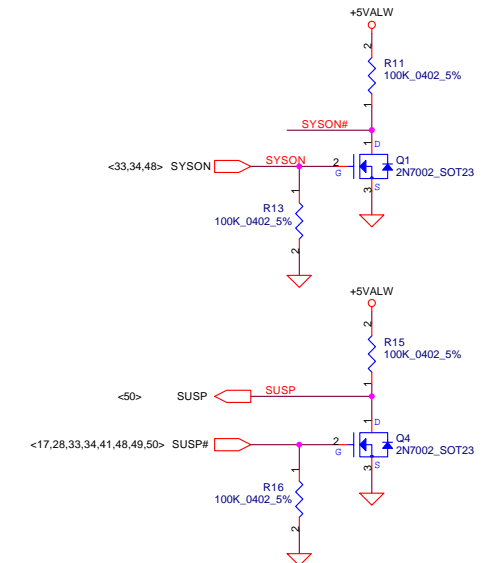
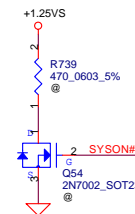
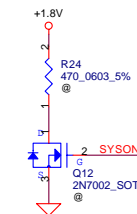
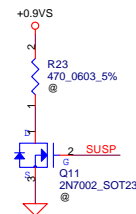
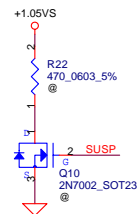
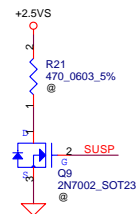
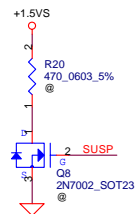
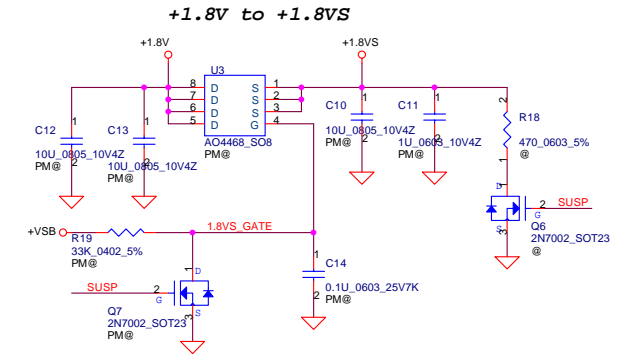
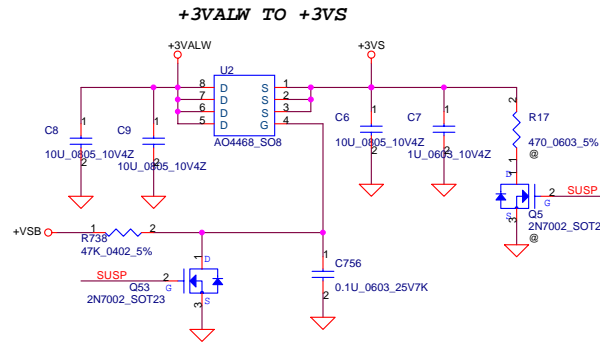
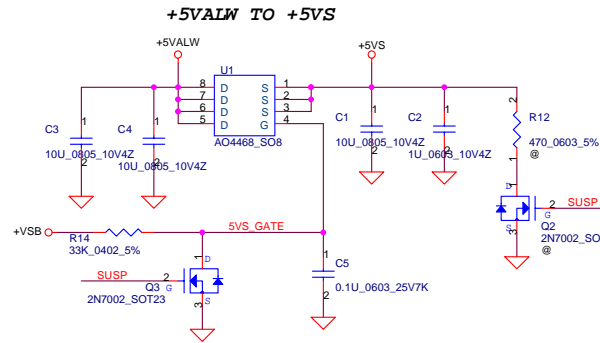


Finger Print board



Need to check pin definition

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				B	IFTXX M/B LA-3541P Schematic
				Date:	Rev 0
				Wednesday, November 01, 2006	Sheet 42 of 52



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				Size B		Document Number		IFTXX M/B LA-3541P Schematic		Rev 0	
				Date:		Wednesday, November 01, 2006		Sheet 43 of 52			