MODEL NAME : *QBL00*

PCB NO : *QC:LA-7851P, DAA00003200*
DC:LA-7852P, DAA00003300

BOM P/N : *TBD*

Dell/Compal Confidential

Schematic Document

Phantom(Chief River)

Ivy Bridge(BGA1224) + Panther Point

DISCRETE VGA N13P-GS(optimus)

2011-08-02

Rev: 0.1 (X00)

@ : Nopop Component
CONN@ : Connector Component
DP1.2@ : DP output from DGPU
DP1.1A@ : DP output from iGPU
GV@ : GPU N13-GV
GS@ : GPU N13-GS
GVH@ :GV+Hynix VRAM
GVS@ : GV+Samsung VRAM
GSH@ : GS+Hynix VRAM
GSS@ : GS+Samsung VRAM
GVHA@ : GV+Hynix VRAM A-die
GVHM@ : GV+Hynix VRAM M-die
GVSC@ : GV+Samsung VRAM C-die
GVSD@ : GV+Samsung VRAM D-die
SB@ : Sandy bridge CPU
TPM@ : With TPM

GV+Hyn M 1G R1

UV4 H5GQ2H24MFR-T2C_BGA 170P~D GVHM@
UV5 H5GQ2H24MFR-T2C_BGA 170P~D GVHM@
UV6 H5GQ2H24MFR-T2C_BGA 170P~D GVHM@
UV7 H5GQ2H24MFR-T2C_BGA 170P~D GVHM@

GV+SAM C 1G R1

UV4 K4G20325FC-HC04_FBGA170P~D GVSC@
UV5 K4G20325FC-HC04_FBGA170P~D GVSC@
UV6 K4G20325FC-HC04_FBGA170P~D GVSC@
UV7 K4G20325FC-HC04_FBGA170P~D GVSC@

GV+SAM D 1G R1

UV7 K4G20325FC-HC04_FBGA170P~D GVSD@
UV4 K4G20325FC-HC04_FBGA170P~D GVSD@
UV5 K4G20325FC-HC04_FBGA170P~D GVSD@
UV6 K4G20325FC-HC04_FBGA170P~D GVSD@

GS+SAM D 2G R1

UV4 K4G20325FC-HC04_FBGA170P~D GSSD@
UV5 K4G20325FC-HC04_FBGA170P~D GSSD@
UV6 K4G20325FC-HC04_FBGA170P~D GSSD@
UV7 K4G20325FC-HC04_FBGA170P~D GSSD@
UV8 K4G20325FC-HC04_FBGA170P~D GSSD@
UV9 K4G20325FC-HC04_FBGA170P~D GSSD@
UV10 K4G20325FC-HC04_FBGA170P~D GSSD@
UV11 K4G20325FC-HC04_FBGA170P~D GSSD@

GS+Hyn M 2G R1

UV4 H5GQ2H24MFR-T2C_BGA 170P~D GSHM@
UV5 H5GQ2H24MFR-T2C_BGA 170P~D GSHM@
UV6 H5GQ2H24MFR-T2C_BGA 170P~D GSHM@
UV7 H5GQ2H24MFR-T2C_BGA 170P~D GSHM@
UV8 H5GQ2H24MFR-T2C_BGA 170P~D GSHM@
UV9 H5GQ2H24MFR-T2C_BGA 170P~D GSHM@
UV10 H5GQ2H24MFR-T2C_BGA 170P~D GSHM@
UV11 H5GQ2H24MFR-T2C_BGA 170P~D GSHM@

GS+SAM D 2G R3

UV8 K4G20325FC-HC04_FBGA170P~D GSSDR3@
UV4 K4G20325FC-HC04_FBGA170P~D GSSDR3@
UV9 K4G20325FC-HC04_FBGA170P~D GSSDR3@
UV7 K4G20325FC-HC04_FBGA170P~D GSSDR3@
UV10 K4G20325FC-HC04_FBGA170P~D GSSDR3@
UV5 K4G20325FC-HC04_FBGA170P~D GSSDR3@
UV11 K4G20325FC-HC04_FBGA170P~D GSSDR3@
UV6 K4G20325FC-HC04_FBGA170P~D GSSDR3@

GS+HYN M 2G R3

UV8 K4G20325FC-HC04_FBGA170P~D GSHMR3@
UV4 K4G20325FC-HC04_FBGA170P~D GSHMR3@
UV9 K4G20325FC-HC04_FBGA170P~D GSHMR3@
UV7 K4G20325FC-HC04_FBGA170P~D GSHMR3@
UV10 K4G20325FC-HC04_FBGA170P~D GSHMR3@
UV6 K4G20325FC-HC04_FBGA170P~D GSHMR3@
UV11 K4G20325FC-HC04_FBGA170P~D GSHMR3@
UV5 K4G20325FC-HC04_FBGA170P~D GSHMR3@

GV+Hyn M 1G R3

UV6 H5GQ2H24MFR-T2C_BGA 170P~D GVHMR3@
UV4 H5GQ2H24MFR-T2C_BGA 170P~D GVHMR3@
UV5 H5GQ2H24MFR-T2C_BGA 170P~D GVHMR3@
UV7 H5GQ2H24MFR-T2C_BGA 170P~D GVHMR3@

GV+SAM C 1G R3

UV7 K4G20325FC-HC04_FBGA170P~D GVSCR3@
UV4 K4G20325FC-HC04_FBGA170P~D GVSCR3@
UV5 K4G20325FC-HC04_FBGA170P~D GVSCR3@
UV6 K4G20325FC-HC04_FBGA170P~D GVSCR3@

GV+SAM D 1G R3

UV7 K4G20325FC-HC04_FBGA170P~D GVSDR3@
UV4 K4G20325FC-HC04_FBGA170P~D GVSDR3@
UV5 K4G20325FC-HC04_FBGA170P~D GVSDR3@
UV6 K4G20325FC-HC04_FBGA170P~D GVSDR3@

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Issued Date	2011/08/25	Deciphered Date	2011/08/25

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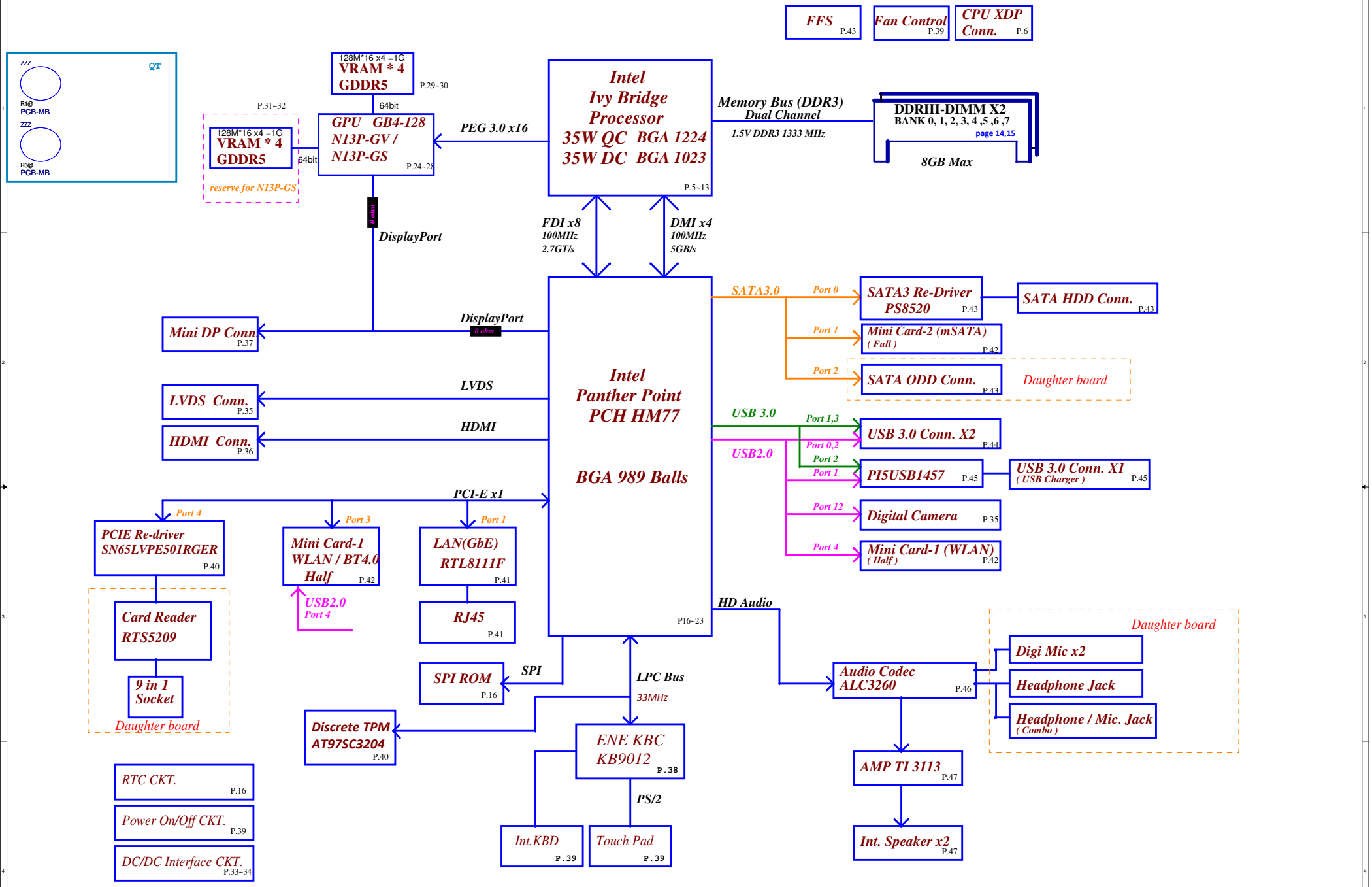
Title: *Cover Page*

Size: | Document Number: *LA-7851P* | Rev: 0.1

Date: Monday, March 26, 2012 | Sheet 1 of 65



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Issued Date	2011/08/25	Deciphered Date	2012/07/25
Title			
Size C	Document Number		Rev 0.1
Date: Monday, March 26, 2012	Sheet 2 of 66		

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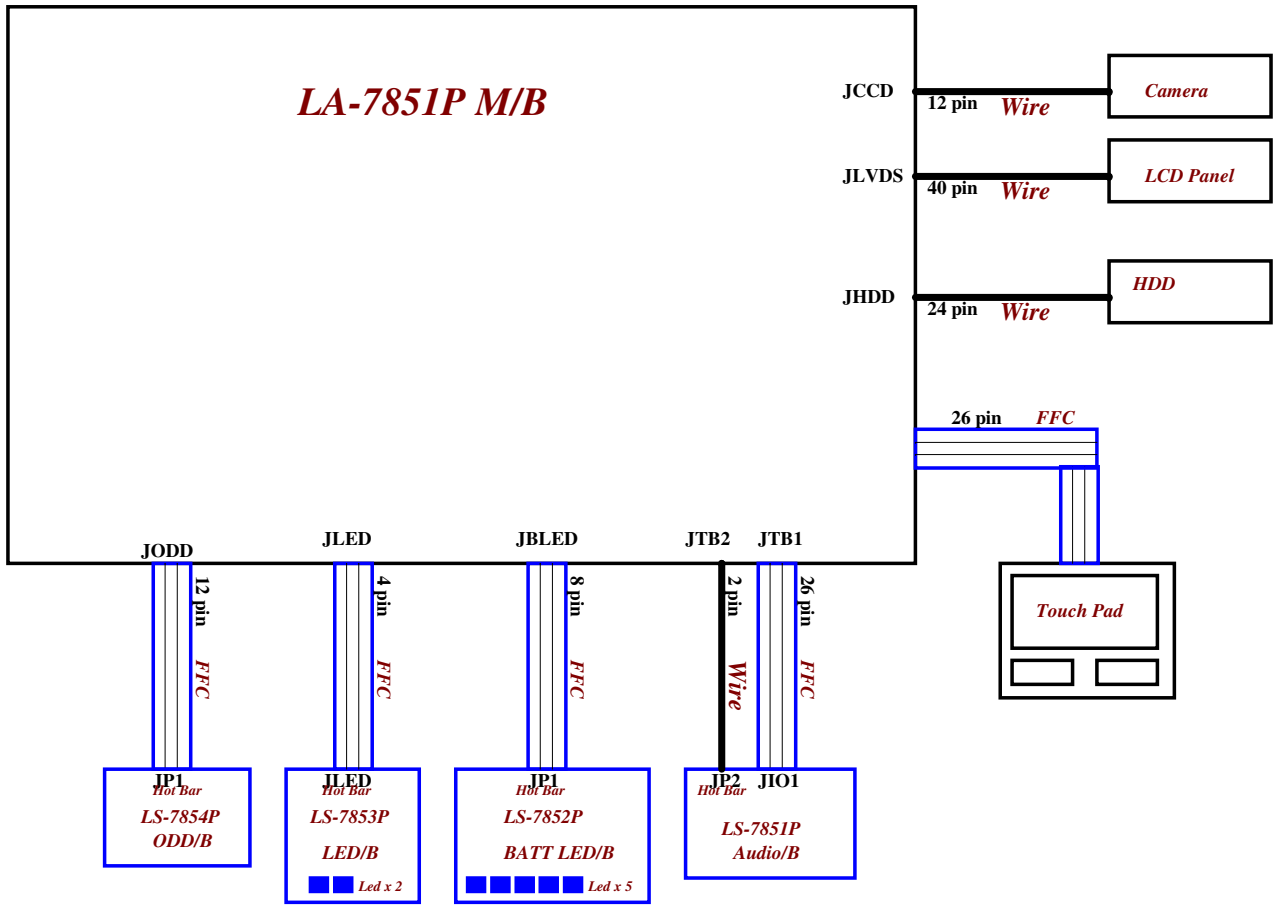
Project Code : QBL00
File Name : LA-7851P



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	None
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

SATA	DESTINATION
SATA0	HDD
SATA1	SSD
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

	USB PORT#	DESTINATION
PCH	0	USB Conn 1
	1	USB Conn 3 (Power share)
	2	USB Conn 2
	3	None
	4	JMINI1 (WLAN)
	5	None
	6	None
	7	None
	8	None
	9	None
	10	None
	11	None
	12	CAMERA
	13	None

USB3	DESTINATION
1	USB Conn 1
2	USB Conn 3 (Power share)
3	USB Conn 2
4	None

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	None	CLKOUTFLEX0	CLK_PCI_TPM
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	LAN_25M
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

: means Digital Ground

: means Analog Ground

Compal Electronics, Inc.

Title: Notes List

Size | Document Number: LA-7851P | Rev: 0.1

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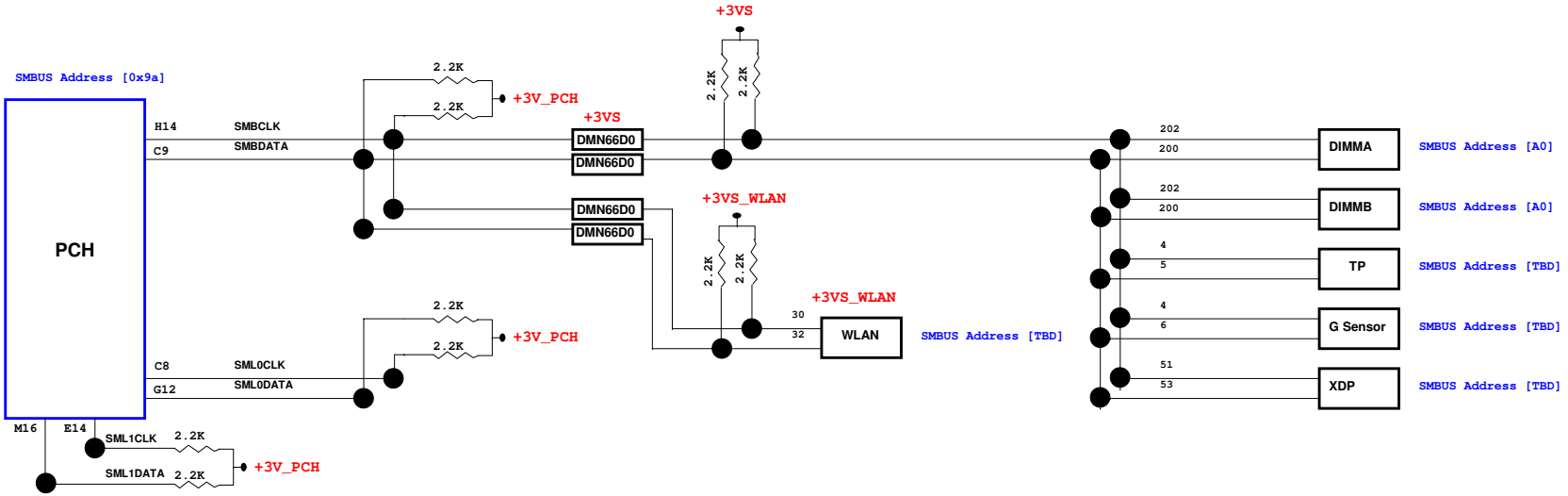

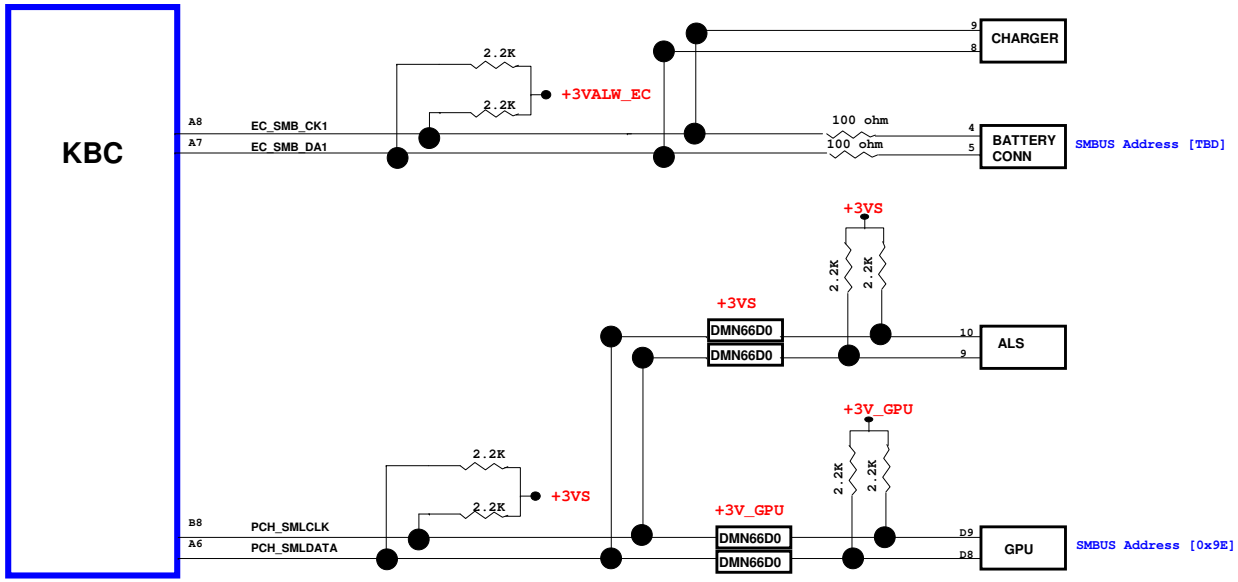

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/15

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Title: SMBus Block Diagram

Size	Document Number	Rev
Custom		0.1

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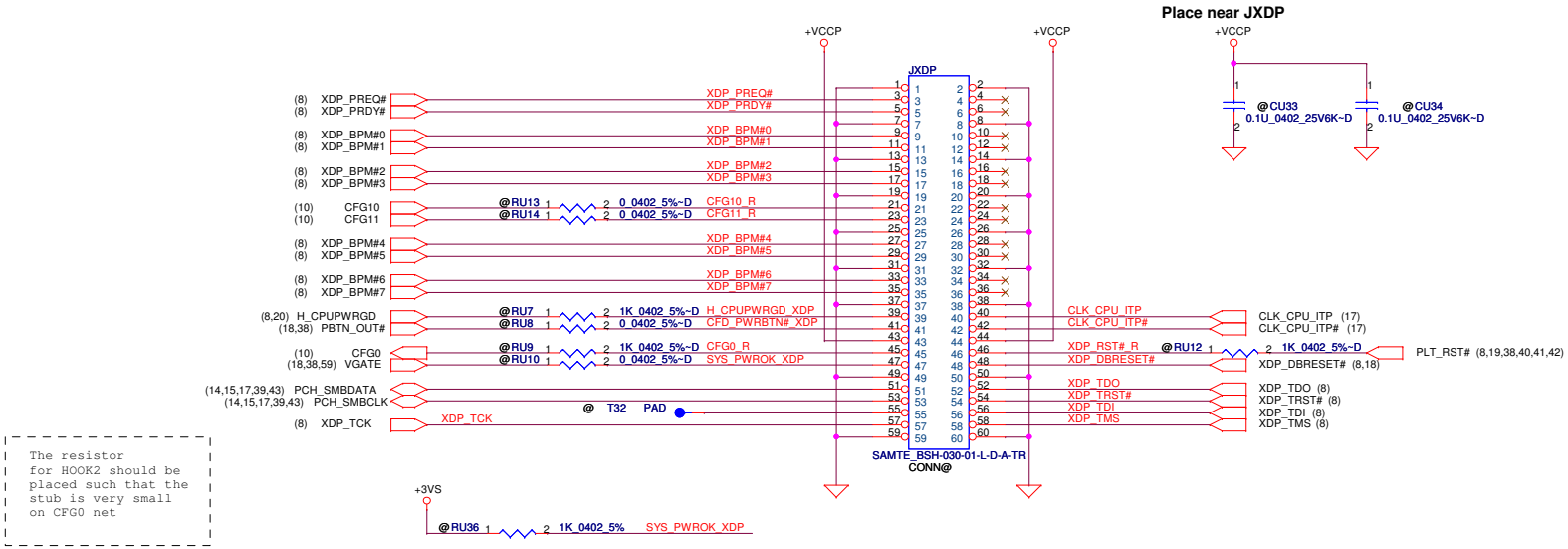
XDP CONN



The resistor for HOOK2 should be placed such that the stub is very small on CFG0 net

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

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ST

UU1

E0@

AV80638011307O3 QC02 E0 2.1G

QT

UU1

QCR1@

S IC AV80638011307O4 SR0MR E1 2.1G BGA 1224

UU1

QCR3@

S IC AV80638011307O4 SR0MR E1 2.1G BGA 1224 A31 !

PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with -
max length = 500 mils
- typical impedance = 14.5 mohms

+VCCP

RU1 1 2 24.9 0402 1%

PEG_COMP

UU1A

DMI

(18) DMI_CRX_PTX_N0 N10 DMI_RX#[0]
(18) DMI_CRX_PTX_N1 R10 DMI_RX#[1]
(18) DMI_CRX_PTX_N2 R8 DMI_RX#[2]
(18) DMI_CRX_PTX_N3 U10 DMI_RX#[3]

(18) DMI_CRX_PTX_P0 N8 DMI_RX[0]
(18) DMI_CRX_PTX_P1 T9 DMI_RX[1]
(18) DMI_CRX_PTX_P2 R6 DMI_RX[2]
(18) DMI_CRX_PTX_P3 U8 DMI_RX[3]

(18) DMI_CTX_PRX_N0 N4 DMI_TX#[0]
(18) DMI_CTX_PRX_N1 R4 DMI_TX#[1]
(18) DMI_CTX_PRX_N2 P1 DMI_TX#[2]
(18) DMI_CTX_PRX_N3 U6 DMI_TX#[3]

(18) DMI_CTX_PRX_P0 N2 DMI_TX[0]
(18) DMI_CTX_PRX_P1 R2 DMI_TX[1]
(18) DMI_CTX_PRX_P2 P3 DMI_TX[2]
(18) DMI_CTX_PRX_P3 T5 DMI_TX[3]

INTEL(R) FDI

(18) FDI_CTX_PRX_N0 V7 FDI0_TX#[0]
(18) FDI_CTX_PRX_N1 W8 FDI0_TX#[1]
(18) FDI_CTX_PRX_N2 AA8 FDI0_TX#[2]
(18) FDI_CTX_PRX_N3 AC10 FDI0_TX#[3]
(18) FDI_CTX_PRX_N4 U4 FDI1_TX#[0]
(18) FDI_CTX_PRX_N5 W2 FDI1_TX#[1]
(18) FDI_CTX_PRX_N6 V1 FDI1_TX#[2]
(18) FDI_CTX_PRX_N7 Y5 FDI1_TX#[3]

(18) FDI_CTX_PRX_P0 W6 FDI0_TX[0]
(18) FDI_CTX_PRX_P1 W10 FDI0_TX[1]
(18) FDI_CTX_PRX_P2 Y9 FDI0_TX[2]
(18) FDI_CTX_PRX_P3 AA10 FDI0_TX[3]
(18) FDI_CTX_PRX_P4 U2 FDI1_TX[0]
(18) FDI_CTX_PRX_P5 W4 FDI1_TX[1]
(18) FDI_CTX_PRX_P6 V3 FDI1_TX[2]
(18) FDI_CTX_PRX_P7 AA6 FDI1_TX[3]

(18) FDI_FSYNC0 AC8 FDI0_FSYNC
(18) FDI_FSYNC1 AA2 FDI1_FSYNC

(18) FDI_INT AD9 FDI_INT

(18) FDI_LSYNC0 AB7 FDI0_LSYNC
(18) FDI_LSYNC1 AB3 FDI1_LSYNC

+VCCP

RU2 1 2 24.9 0402 1%

EDP_COMP

DP

AC2 eDP_COMPIO
AB1 eDP_ICOMPO
AE8 eDP_HPD#

AE4 eDP_AUX
AE2 eDP_AUX#

AG4 eDP_TX[0]
AF3 eDP_TX[1]
AF7 eDP_TX[2]
AG8 eDP_TX[3]

AG2 eDP_TX#[0]
AF1 eDP_TX#[1]
AE6 eDP_TX#[2]
AG6 eDP_TX#[3]

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI G2
PEG_ICOMPO H1
PEG_RCOMPO F3

PEG_RX#[0] F23 PEG_GTX_C_HRX_N15
PEG_RX#[1] H23 PEG_GTX_C_HRX_N14
PEG_RX#[2] H21 PEG_GTX_C_HRX_N13
PEG_RX#[3] H19 PEG_GTX_C_HRX_N12
PEG_RX#[4] J20 PEG_GTX_C_HRX_N11
PEG_RX#[5] G18 PEG_GTX_C_HRX_N10
PEG_RX#[6] K17 PEG_GTX_C_HRX_N9
PEG_RX#[7] F15 PEG_GTX_C_HRX_N8
PEG_RX#[8] H15 PEG_GTX_C_HRX_N7
PEG_RX#[9] H13 PEG_GTX_C_HRX_N6
PEG_RX#[10] H11 PEG_GTX_C_HRX_N5
PEG_RX#[11] J12 PEG_GTX_C_HRX_N4
PEG_RX#[12] E8 PEG_GTX_C_HRX_N3
PEG_RX#[13] G10 PEG_GTX_C_HRX_N2
PEG_RX#[14] J8 PEG_GTX_C_HRX_N1
PEG_RX#[15] F7 PEG_GTX_C_HRX_N0

PEG_RX[0] G22 PEG_GTX_C_HRX_P15
PEG_RX[1] K23 PEG_GTX_C_HRX_P14
PEG_RX[2] K21 PEG_GTX_C_HRX_P13
PEG_RX[3] F19 PEG_GTX_C_HRX_P12
PEG_RX[4] K19 PEG_GTX_C_HRX_P11
PEG_RX[5] H17 PEG_GTX_C_HRX_P10
PEG_RX[6] K15 PEG_GTX_C_HRX_P9
PEG_RX[7] G14 PEG_GTX_C_HRX_P8
PEG_RX[8] J16 PEG_GTX_C_HRX_P7
PEG_RX[9] K13 PEG_GTX_C_HRX_P6
PEG_RX[10] F11 PEG_GTX_C_HRX_P5
PEG_RX[11] K11 PEG_GTX_C_HRX_P4
PEG_RX[12] F9 PEG_GTX_C_HRX_P3
PEG_RX[13] H9 PEG_GTX_C_HRX_P2
PEG_RX[14] H7 PEG_GTX_C_HRX_P1
PEG_RX[15] G6 PEG_GTX_C_HRX_P0

PEG_TX#[0] A22 PEG_HTX_GRX_N15 CU1 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N15
PEG_TX#[1] B23 PEG_HTX_GRX_N14 CU2 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N14
PEG_TX#[2] C18 PEG_HTX_GRX_N13 CU3 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N13
PEG_TX#[3] D21 PEG_HTX_GRX_N12 CU4 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N12
PEG_TX#[4] B19 PEG_HTX_GRX_N11 CU5 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N11
PEG_TX#[5] E20 PEG_HTX_GRX_N10 CU6 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N10
PEG_TX#[6] A14 PEG_HTX_GRX_N9 CU7 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N9
PEG_TX#[7] D17 PEG_HTX_GRX_N8 CU8 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N8
PEG_TX#[8] B15 PEG_HTX_GRX_N7 CU9 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N7
PEG_TX#[9] E16 PEG_HTX_GRX_N6 CU10 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N6
PEG_TX#[10] D13 PEG_HTX_GRX_N5 CU11 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N5
PEG_TX#[11] A10 PEG_HTX_GRX_N4 CU12 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N4
PEG_TX#[12] B11 PEG_HTX_GRX_N3 CU13 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N3
PEG_TX#[13] D9 PEG_HTX_GRX_N2 CU14 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N2
PEG_TX#[14] B7 PEG_HTX_GRX_N1 CU15 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N1
PEG_TX#[15] E12 PEG_HTX_GRX_N0 CU16 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_N0

PEG_TX[0] C22 PEG_HTX_GRX_P15 CU17 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P15
PEG_TX[1] D23 PEG_HTX_GRX_P14 CU18 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P14
PEG_TX[2] A18 PEG_HTX_GRX_P13 CU19 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P13
PEG_TX[3] B21 PEG_HTX_GRX_P12 CU20 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P12
PEG_TX[4] D19 PEG_HTX_GRX_P11 CU21 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P11
PEG_TX[5] F21 PEG_HTX_GRX_P10 CU22 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P10
PEG_TX[6] C14 PEG_HTX_GRX_P9 CU23 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P9
PEG_TX[7] B17 PEG_HTX_GRX_P8 CU24 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P8
PEG_TX[8] D15 PEG_HTX_GRX_P7 CU25 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P7
PEG_TX[9] F17 PEG_HTX_GRX_P6 CU26 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P6
PEG_TX[10] B13 PEG_HTX_GRX_P5 CU27 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P5
PEG_TX[11] C10 PEG_HTX_GRX_P4 CU28 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P4
PEG_TX[12] D11 PEG_HTX_GRX_P3 CU29 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P3
PEG_TX[13] B9 PEG_HTX_GRX_P2 CU30 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P2
PEG_TX[14] D7 PEG_HTX_GRX_P1 CU31 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P1
PEG_TX[15] F13 PEG_HTX_GRX_P0 CU32 1 2 0.22U_0402_16V7K-D PEG_HTX_C_GRX_P0

PEG_GTX_C_HRX_N[0..15] PEG_GTX_C_HRX_N[0..15] (24)
PEG_GTX_C_HRX_P[0..15] PEG_GTX_C_HRX_P[0..15] (24)
PEG_HTX_C_GRX_N[0..15] PEG_HTX_C_GRX_N[0..15] (24)
PEG_HTX_C_GRX_P[0..15] PEG_HTX_C_GRX_P[0..15] (24)

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

AV80638011080O3_BGA1224~D

E1@

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Title: PROCESSOR(1/7) DMI,FDI,PEG

Size: Custom | Document Number | Rev: 0.1

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This pin is for compability with future platforms. A pull up resistor to VCCIO is required if connected to the DF_TVS strap on the PCH.

PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present

Processor Pullups

place RU32,RU30 near CPU

If motherboard only supports external graphics or if it supports Processor Graphics but without eDP

S3 circuit:- DRAM_RST# to memory should be high during S3

SM_DRAMPWROK

Buffered reset to CPU

DDR3 Compensation Signals

PU/PD for JTAG signals

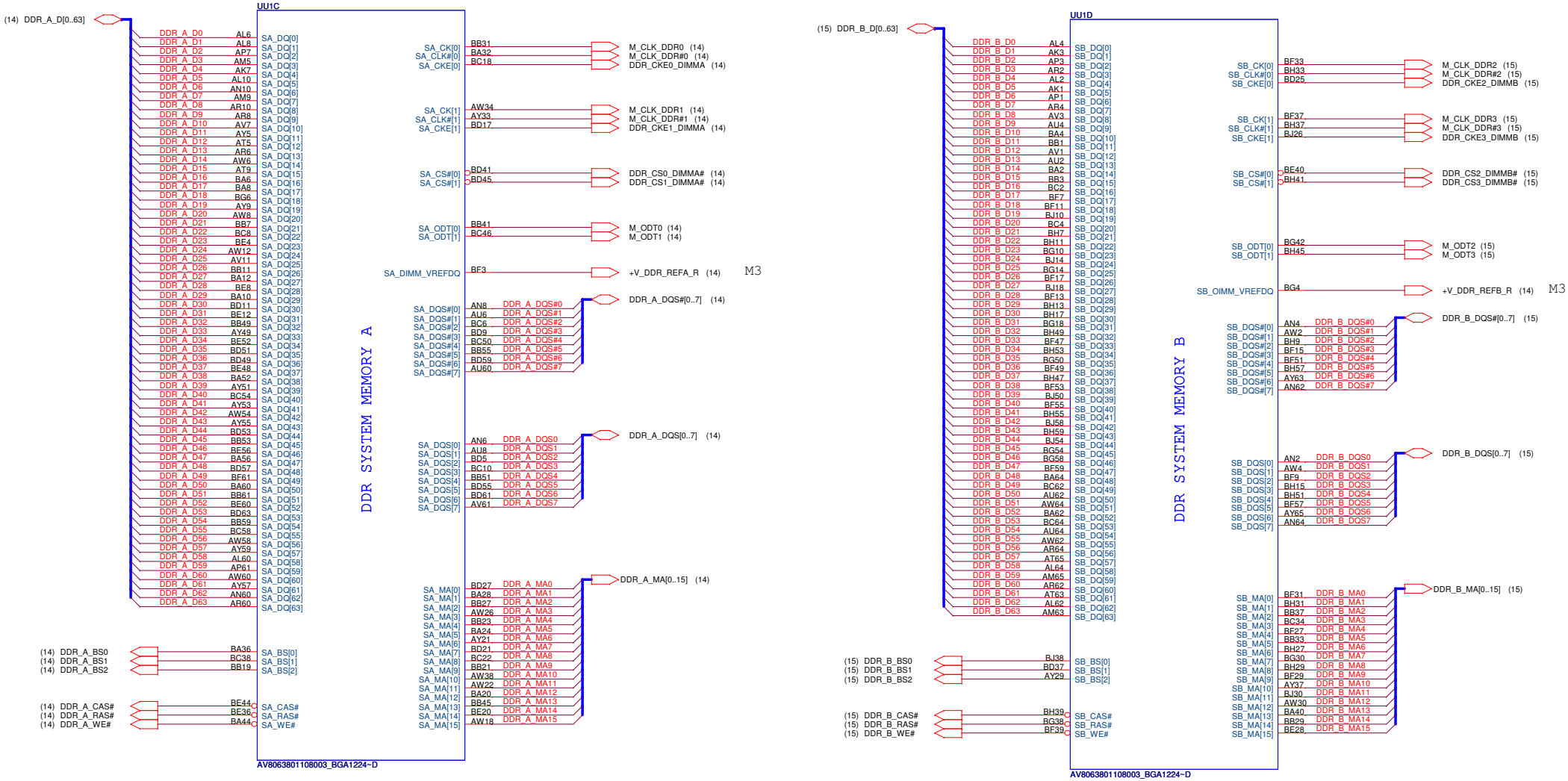
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number | Rev: 0.1

Date: Monday, March 26, 2012 | Sheet 8 of 66



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom		0.1

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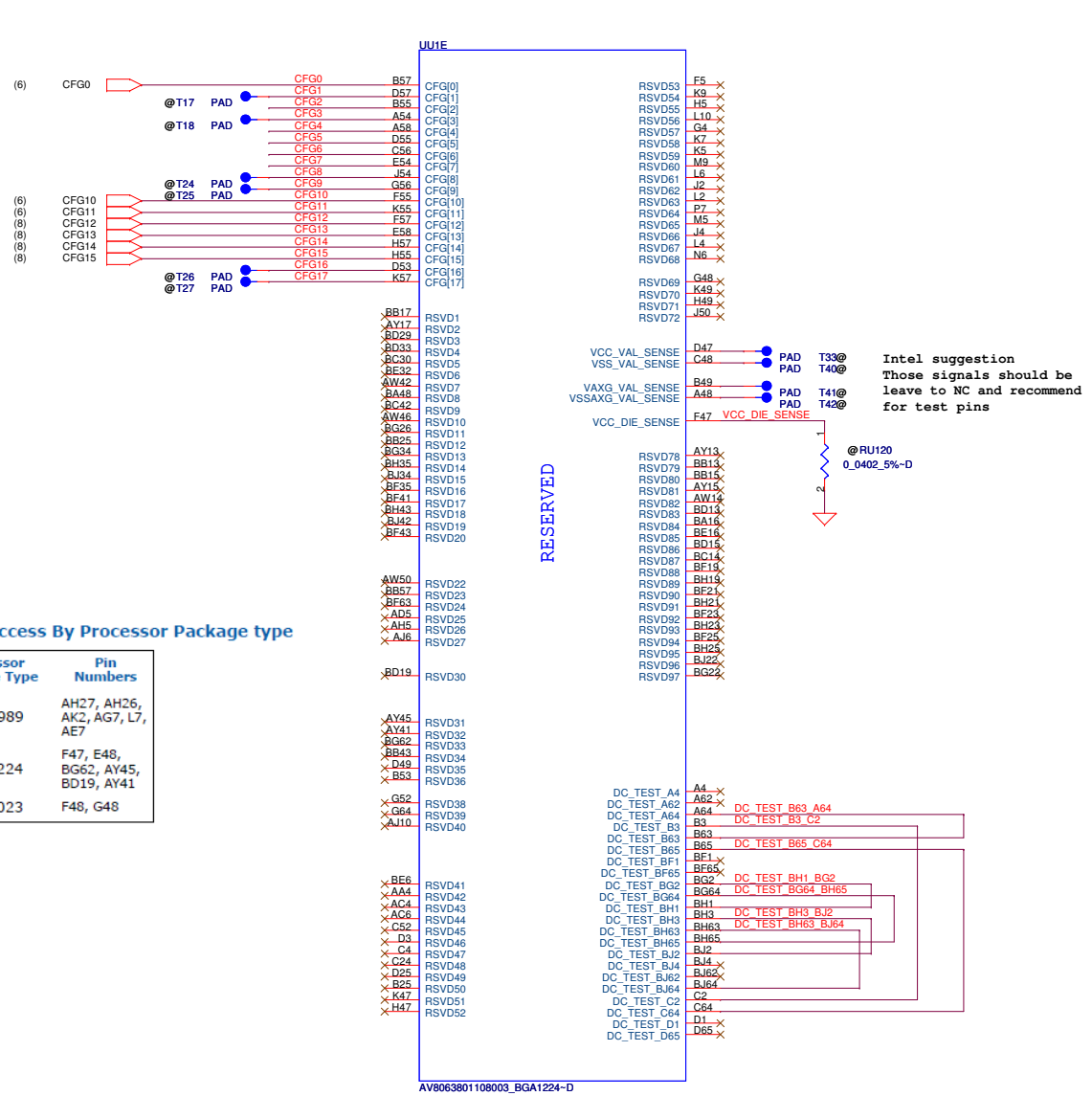
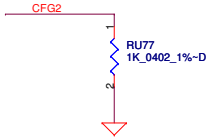
CFG Straps for Processor



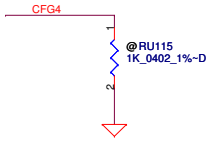
Intel suggestion
Those signals should be leave to NC and recommend for test pins

Debug Access By Processor Package type

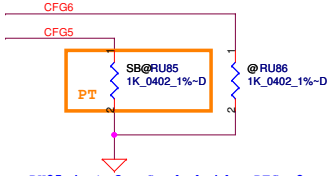
Processor Package Type	Pin Numbers
rPGA 989	AH27, AH26, AK2, AG7, L7, AE7
BGA1224	F47, E48, BG62, AY45, BD19, AY41
BGA1023	F48, G48



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

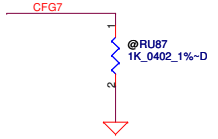


Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



RU85 just for Sandy bridge PEG x8

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled PT 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number | Rev: 0.1

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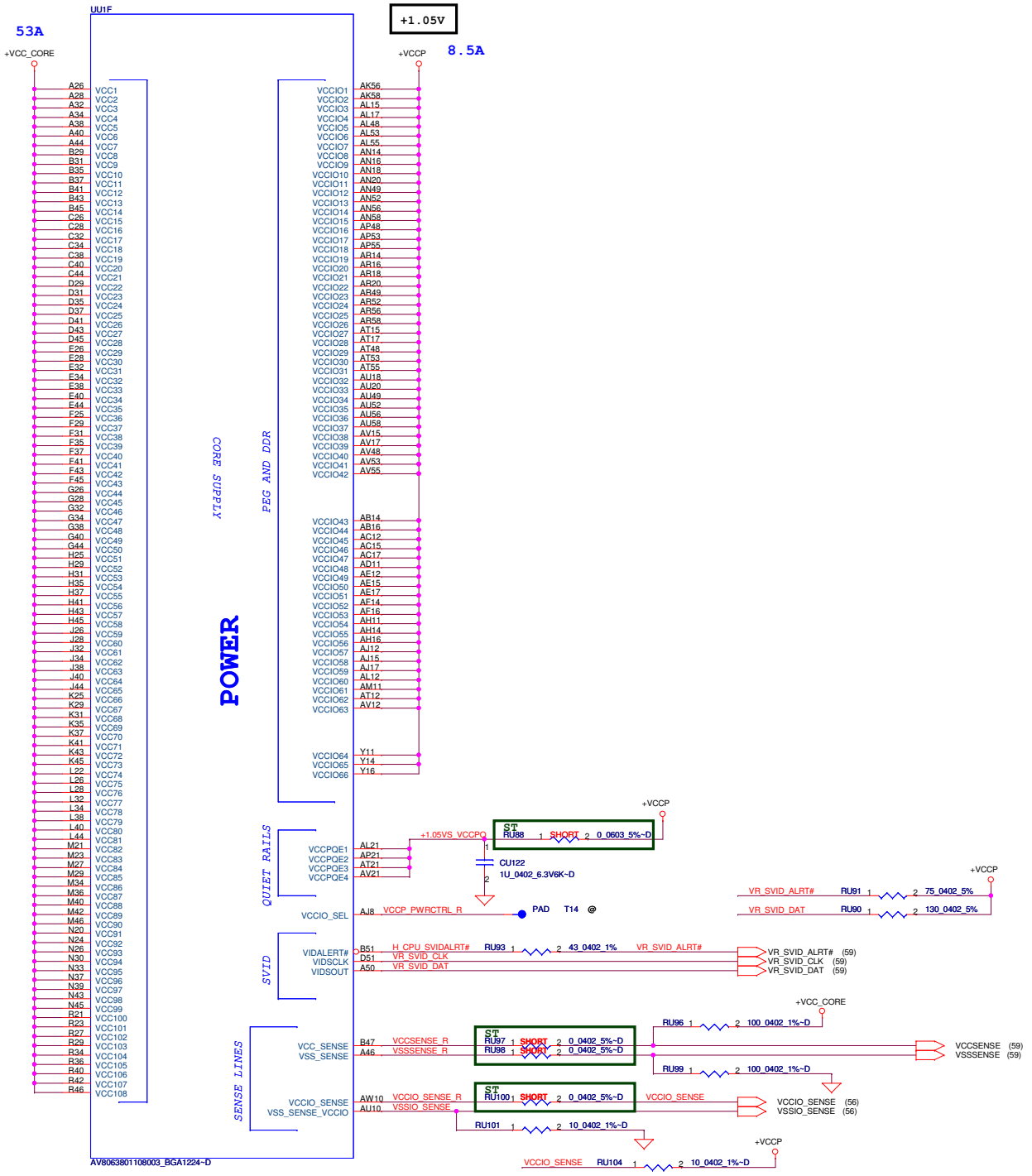


Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: **PROCESSOR(5/7) PWR,BYPASS**

Size	Document Number	Rev
Custom		0.1

Date: Monday, March 26, 2012 | Sheet 11 of 66

+V_SM_VREF should have 20 mil trace width

33A

UU1G

+VCC_GFXCORE_AXG

AA60 AA62 AA64 AB56 AB58 AB61 AB63 AB65 AD56 AD58 AD61 AD63 AD65 AE60 AE62 AE64 AF56 AF58 AG60 AG62 AG64 AH56 AH58 AH61 AH63 AH65 L48 L52 L56 M48 M53 M55 M59 M61 M63 M65 N49 N52 N56 N58 N60 N62 N64 R48 R53 R55 R60 R62 R64 T56 T58 T61 T63 T65 V56 V58 V61 V63 V65 W60 W62 W64 Y56 Y58

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54 VAXG55 VAXG56 VAXG57 VAXG58 VAXG59 VAXG60 VAXG61 VAXG62 VAXG63 VAXG64

GRAPHICS

DDR3 - 1.5V RAILS

POWER

SENSE SENSES

1.8V RAIL

QUIET RAILS

SENSE LINES

SA RAIL

SM_VREF — BJ44

VDDQ1 AL27 VDDQ2 AL29 VDDQ3 AL34 VDDQ4 AL36 VDDQ5 AL40 VDDQ6 AL42 VDDQ7 AL46 VDDQ8 AN24 VDDQ9 AN26 VDDQ10 AN30 VDDQ11 AN33 VDDQ12 AN37 VDDQ13 AN39 VDDQ14 AN43 VDDQ15 AN45 VDDQ16 AP27 VDDQ17 AP29 VDDQ18 AP34 VDDQ19 AP36 VDDQ20 AP40 VDDQ21 AP42 VDDQ22 AP46 VDDQ23 AR24 VDDQ24 AR26 VDDQ25 AR30 VDDQ26 AR33 VDDQ27 AR37 VDDQ28 AR39 VDDQ29 AR43 VDDQ30 AR45 VDDQ31 AT27 VDDQ32 AT29 VDDQ33 AT34 VDDQ34 AT36 VDDQ35 AT40 VDDQ36 AT42 VDDQ37 AT46 VDDQ38 AU24 VDDQ39 AU26 VDDQ40 AU30 VDDQ41 AU33 VDDQ42 AU37 VDDQ43 AU39 VDDQ44 AU43 VDDQ45 AU45 VDDQ46 AV27 VDDQ47 AV29 VDDQ48 AV34 VDDQ49 AV36 VDDQ50 AV40 VDDQ51 AV42 VDDQ52 AV46 VDDQ53 AY23 VDDQ54 AY27 VDDQ55 AY31 VDDQ56 AY35 VDDQ57 AY39 VDDQ58 AY43 VDDQ59 AY47 VDDQ60 BB35 VDDQ61 BD23 VDDQ62 BD31 VDDQ63 BD39 VDDQ64 BD43 VDDQ65 BD47 VDDQ66 BG32 VDDQ67 BG40 VDDQ68 BJ28 VDDQ69 BJ36

VCCDQ1 AL23 VCCDQ2 AP23 VCCDQ3 AT23 VCCDQ4 AV23

VDDQ_SENSE AY19 VSS_SENSE_VDDQ AW20

VCCSA_SENSE K3

VCCSA_VID[0] AE10 VCCSA_VID[1] AG10

VCCSA1 L14 VCCSA2 L18 VCCSA3 M11 VCCSA4 M12 VCCSA5 M15 VCCSA6 M17 VCCSA7 N14 VCCSA8 N16 VCCSA9 N18 VCCSA10 T11 VCCSA11 T14 VCCSA12 T16 VCCSA13 U12 VCCSA14 U15 VCCSA15 U17 VCCSA16 W12 VCCSA17 W15 VCCSA18 W17

VAXG_SENSE F49 VSSAXG_SENSE E50

VCCPLL1 AK61 VCCPLL2 AK63 VCCPLL3 AK65

AV8063801108003_BGA1224-D

+V_DDR_REFA

+SM_VREF

RU83 1K_0402_1%~D

RU117 0_0402_5%~D

QU4 AP2302GN-HF_SOT23-3-D

RU84 1K_0402_1%~D

CU154 0.1U_0402_25V6K~D

RUN_ON_CPU1.5VS3

+0.75VS

RU118 SHORT 0_0402_5%~D

+1.5V_CPU_VDDQ

5A

CU168 330U_D2_2V_Y

CU169 CU170 CU171 CU172 CU173 CU174 CU175 CU176 10U_0603_6.3V6M~D

CU177 CU178 CU179 CU191 0.1U_0402_10V7K~D

CU192 CU193 CU194 CU195 CU196 CU197 CU198 CU199 CU200 CU201 1U_0402_6.3V6K~D

+1.5V

+VCC_GFXCORE_AXG

RU103 100_0402_1%~D

RU108 SHORT 0_0402_5%~D

RU109 SHORT 0_0402_5%~D

RU112 100_0402_1%~D

(59) VCC_AXG_SENSE

(59) VSS_AXG_SENSE

+1.8VS

1.2A

RU111 SHORT 0_0805_5%~D

+1.8VS_VCCPLL_B

CU207 10U_0603_6.3V6M~D

CU205 1U_0402_6.3V6K~D

CU206 1U_0402_6.3V6K~D

+VCCSA

6A

CU215 330U_D2_2V_Y

CU211 CU212 CU213 CU214 10U_0603_6.3V6M~D

CU216 CU217 CU218 CU219 CU220 1U_0402_6.3V6K~D

CU208 1U_0402_6.3V6K~D

(8,38,57) CPU1.5V_S3_GATE

+1.5V_CPU_VDDQ Source

+3VALW

+VSBP

+1.5V

6720mA

QU6 AO4728L_SO8~D

RU107 100K_0402_5%~D

RU105 100K_0402_5%~D

RUN_ON_CPU1.5VS3

RUN_ON_CPU1.5VS3#

QU5B 2N7002DW-7-F_SOT363-6

QU5A 2N7002DW-7-F_SOT363-6

RU110 330K_0402_1%

CU204 0.1U_0603_50V_X7R

(8,34)

VCCSA_SEL Voltage Selection Table

VID[0] Pin AE10	VID[1] Pin AG10	VCCSA Vout
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

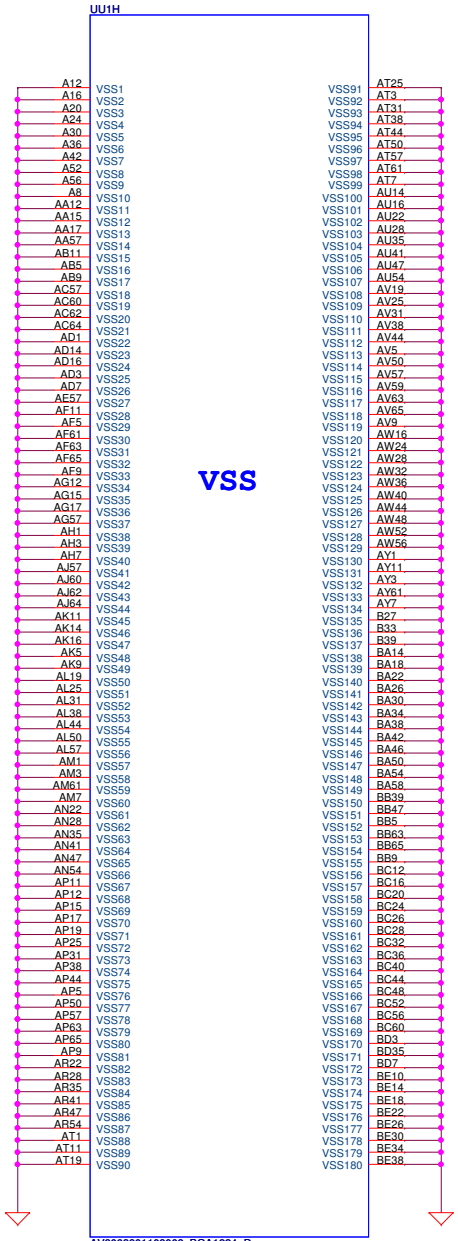
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

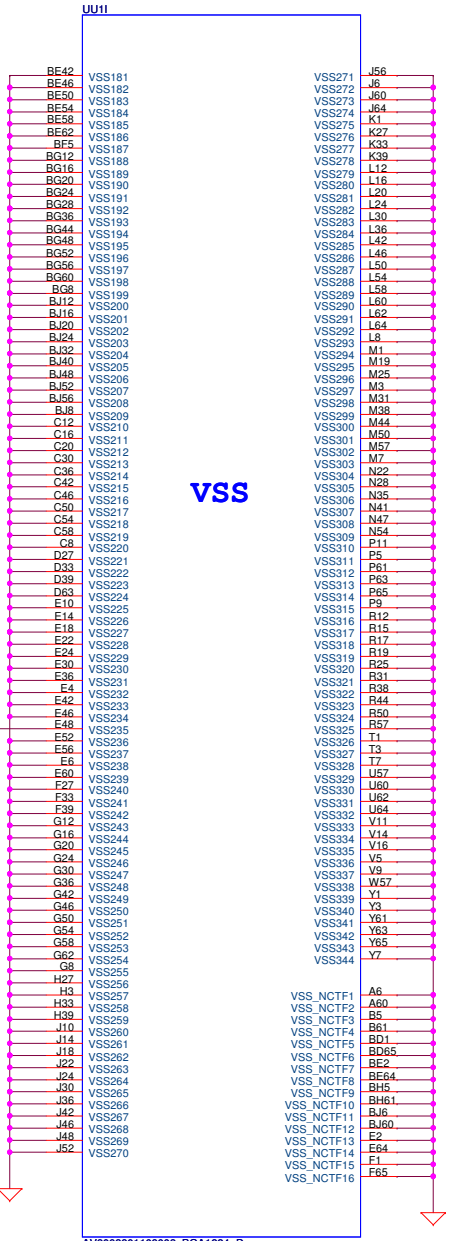
Compal Electronics, Inc.

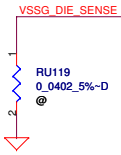
Title: PROCESSOR(6/7) PWR

Size: Custom | Document Number | Rev: 0.1

Date: Monday, March 26, 2012 | Sheet 12 of 66







Debug Access By Processor Package type

Processor Package Type	Pin Numbers
rPGA 989	AH27, AH26, AK2, AG7, L7, AE7
BGA1224	F47, E48, BG62, AY45, BD19, AY41
BGA1023	F48, G48

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom		0.1

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(9) DDR_A_DQS#[0..7]
(9) DDR_A_DQS[0..7]
(9) DDR_A_D[0..63]
(9) DDR_A_MA[0..15]

All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

Layout Note:
Place near JDIMM1.199

M1

+1.5V
RD2 1K_0402_1%~D
+V_DDR_REFA
RD3 1K_0402_1%~D
@CD1 2.2U_0603_6.3V6K~D
CD2 0.1U_0402_16V7K~D

M3

@RD6 0_0402_5%~D
+V_DDR_REFA
QD1 BSS138-G_SOT23-3
+V_DDR_REFA_R (9)
@RD17 1K_0402_1%~D
(9,17) DRAMRST_CNTRL_PCH
@RD7 0_0402_5%~D
(15) +V_DDR_REFB
QD2 BSS138-G_SOT23-3
+V_DDR_REFB_R (9)
@RD18 1K_0402_1%~D

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

JDIMM1
BELLW_80011-1021
CONN@

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: DDRIII DIMMA

Size | Document Number: LA-7851P | Rev: 0.1

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8/15 update for SSI

M1

(9) DDR_B_DQS#[0..7]
(9) DDR_B_DQS[0..7]
(9) DDR_B_D[0..63]
(9) DDR_B_MA[0..15]

+1.5V
RD11 1K_0402_1%~D
+V_DDR_REFB
RD12 1K_0402_1%~D
@CD23 2.2U_0603_6.3V6K~D
CD24 0.1U_0402_16V7K~D

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMMB

All VREF traces should have 10 mil trace width

+1.5V
CD25 1U_0402_6.3V6K~D
CD26 1U_0402_6.3V6K~D
CD27 1U_0402_6.3V6K~D
CD28 1U_0402_6.3V6K~D
CD30 10U_0603_6.3V6M~D
CD31 10U_0603_6.3V6M~D
CD32 10U_0603_6.3V6M~D
CD33 10U_0603_6.3V6M~D
CD34 10U_0603_6.3V6M~D
CD35 10U_0603_6.3V6M~D

Layout Note:
Place near JDIMMB.203,204

+0.75VS
CD39 1U_0402_6.3V6K~D
CD40 1U_0402_6.3V6K~D
CD41 1U_0402_6.3V6K~D
CD42 1U_0402_6.3V6K~D

Layout Note:
Place near JDIMMB.199

+3VS
CD43 0.1U_0402_16V7K~D
CD44 2.2U_0603_6.3V6K~D

JDIMM2

(14) +V_DDR_REFB
RD16 10K_0402_5%~D
RD15 10K_0402_5%~D
BELLW_80001-2021
CONN@

RD13 1K_0402_1%~D
RD14 1K_0402_1%~D
@CD37 2.2U_0603_6.3V6K~D
CD38 0.1U_0402_16V7K~D

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **DDRIII DIMMB**

Size	Document Number	Rev
	LA-7851P	0.1

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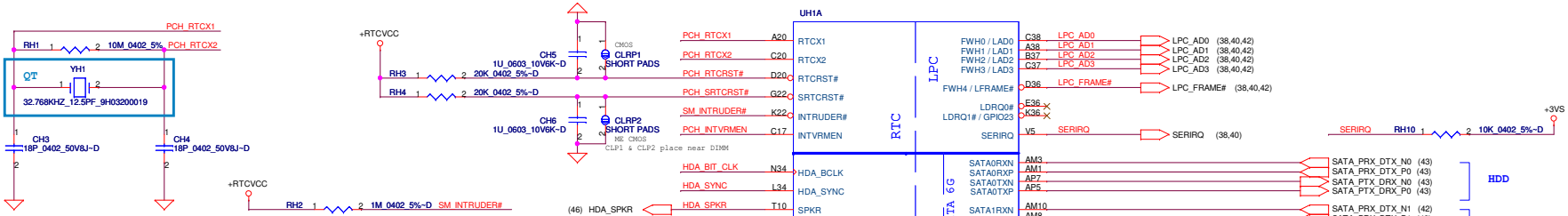
RTC CRYSTAL



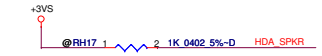
UH1 QT
OCR1@
S IC BD82HM77 SLJ8C C1 BGA 989P PCH
UH1
OCR3@
S IC BD82HM77 SLJ8C C1 BGA 989P PCH A31!

PCH Strap PIN

INTVRMEN Integrated 1.05V VRM Enable/Disable

* H : Integrated VRM enable
L : Integrated VRM disable

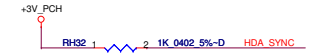
SPKR No Reboot



*LOW=Default
HIGH=No Reboot

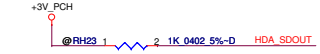
If the signal is sampled high, this indicate that the system is strapped to the "No Reboot" mode

HDA_SYNC On-Die PLL Voltage Regulator Voltage Select



This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

HDA_SDO
Flash Descriptor Security Override/Intel ME Debug Mode



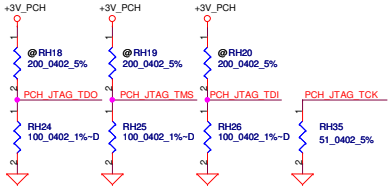
*Low = Disabled
High = Enabled

ME debug mode , this signal has a weak internal PD

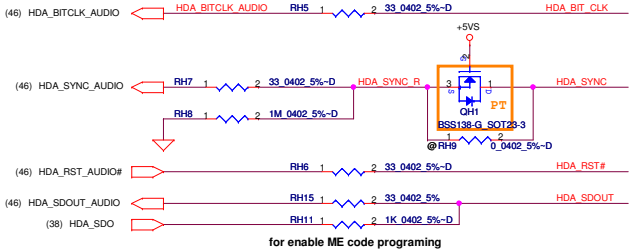
L=>security measures defined in the Flash Descriptor will be in effect (default)

H=>Flash Descriptor Security will be overridden

JTAG

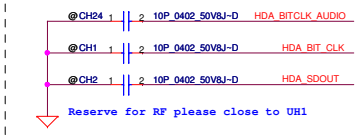


HD Audio



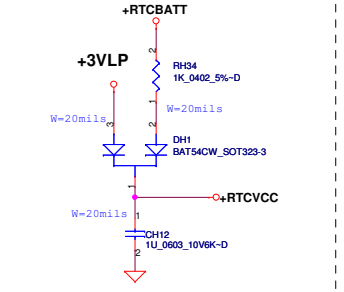
for enable ME code programing

Reserve for EMI

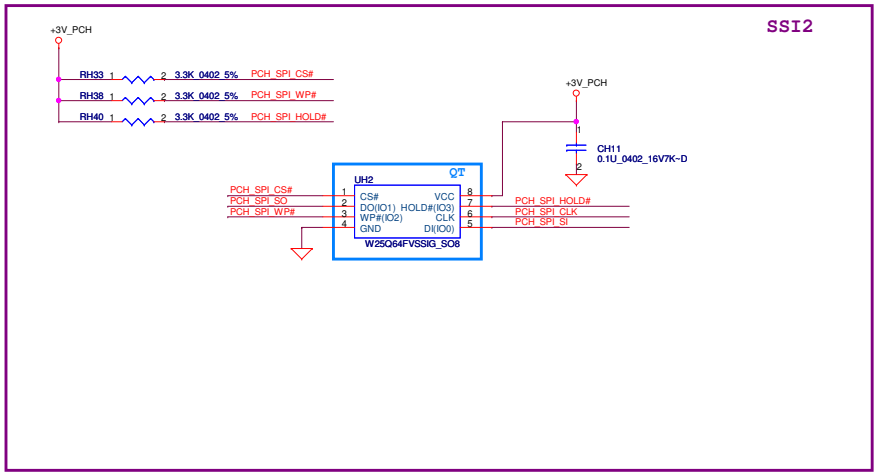


Reserve for RF please close to UH1

RTC Battery



SPI ROM FOR ME (8MByte)



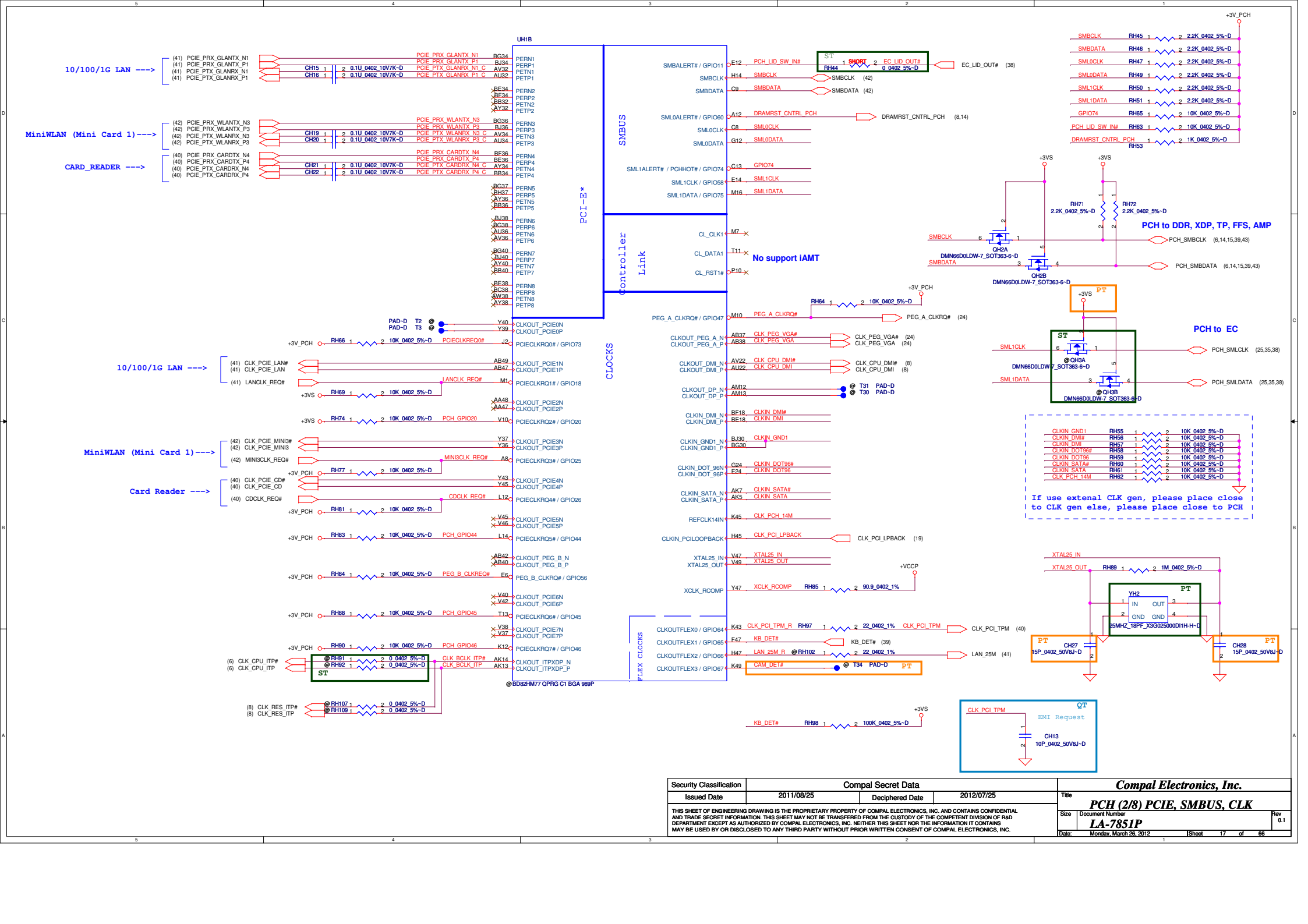
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC

Size	Document Number	Rev
	LA-7851P	0.1

Date: Monday, March 26, 2012 Sheet 16 of 66


10/100/1G LAN ---> (41) PCIE_PRX_GLANTX_N1 (41) PCIE_PRX_GLANTX_P1 (41) PCIE_PTX_GLANRX_N1 (41) PCIE_PTX_GLANRX_P1
CH15 0.1U_0402_10V7K-D CH16 0.1U_0402_10V7K-D
MiniWLAN (Mini Card 1)---> (42) PCIE_PRX_WLANTX_N3 (42) PCIE_PRX_WLANTX_P3 (42) PCIE_PTX_WLANRX_N3 (42) PCIE_PTX_WLANRX_P3
CH19 0.1U_0402_10V7K-D CH20 0.1U_0402_10V7K-D
CARD_READER ---> (40) PCIE_PRX_CARDTX_N4 (40) PCIE_PRX_CARDTX_P4 (40) PCIE_PTX_CARDRX_N4 (40) PCIE_PTX_CARDRX_P4
CH21 0.1U_0402_10V7K-D CH22 0.1U_0402_10V7K-D
UH1B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
@BD82HM77 QPRG C1 BGA 989P
SMBALERT# / GPIO11 SMBCLK SMBDATA
SML0ALERT# / GPIO60 SML0CLK SML0DATA
SML1ALERT# / PCHHOT# / GPIO74 SML1CLK / GPIO58 SML1DATA / GPIO75
CL_CLK1 CL_DATA1 CL_RST1#
No support iAMT
PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N CLKOUT_PEG_A_P
CLKOUT_DMI_N CLKOUT_DMI_P
CLKOUT_DP_N CLKOUT_DP_P
CLKIN_DMI_N CLKIN_DMI_P
CLKIN_GND1_N CLKIN_GND1_P
CLKIN_DOT_96N CLKIN_DOT_96P
CLKIN_SATA_N CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0 / GPIO64 CLKOUTFLEX1 / GPIO65 CLKOUTFLEX2 / GPIO66 CLKOUTFLEX3 / GPIO67
PCH_LID_SW_IN# EC_LID_OUT# EC_LID_OUT (38)
SMBCLK (42) SMBDATA (42)
DRAMRST_CNTRL_PCH (8,14)
GPIO74 SML1CLK SML1DATA
PCH to DDR, XDP, TP, FFS, AMP
PCH_SMBCLK (6,14,15,39,43) PCH_SMBDATA (6,14,15,39,43)
PCH to EC
PCH_SMLCLK (25,35,38) PCH_SMLDATA (25,35,38)
If use extenal CLK gen, please place close to CLK gen else, please place close to PCH
CLK_PCI_LPBACK (19)
CLK_PCI_TPM (40)
LAN_25M (41)
KB_DET (39)
CLK_CPU_ITP# CLK_CPU_ITP
CLK_RES_ITP# CLK_RES_ITP
10/100/1G LAN ---> (41) CLK_PCIE_LAN# (41) CLK_PCIE_LAN (41) LANCLK_REQ#
MiniWLAN (Mini Card 1)---> (42) CLK_PCIE_MINI3# (42) CLK_PCIE_MINI3 (42) MINI3CLK_REQ#
Card Reader ---> (40) CLK_PCIE_CD# (40) CLK_PCIE_CD (40) CDCLK_REQ#
PCIECLKRQ0# / GPIO73
PCIECLKRQ1# / GPIO18
PCIECLKRQ2# / GPIO20
PCIECLKRQ3# / GPIO25
PCIECLKRQ4# / GPIO26
PCIECLKRQ5# / GPIO44
PEG_B_CLKRQ# / GPIO56
PCIECLKRQ6# / GPIO45
PCIECLKRQ7# / GPIO46
Security Classification Compal Secret Data
Issued Date 2011/08/25 Deciphered Date 2012/07/25
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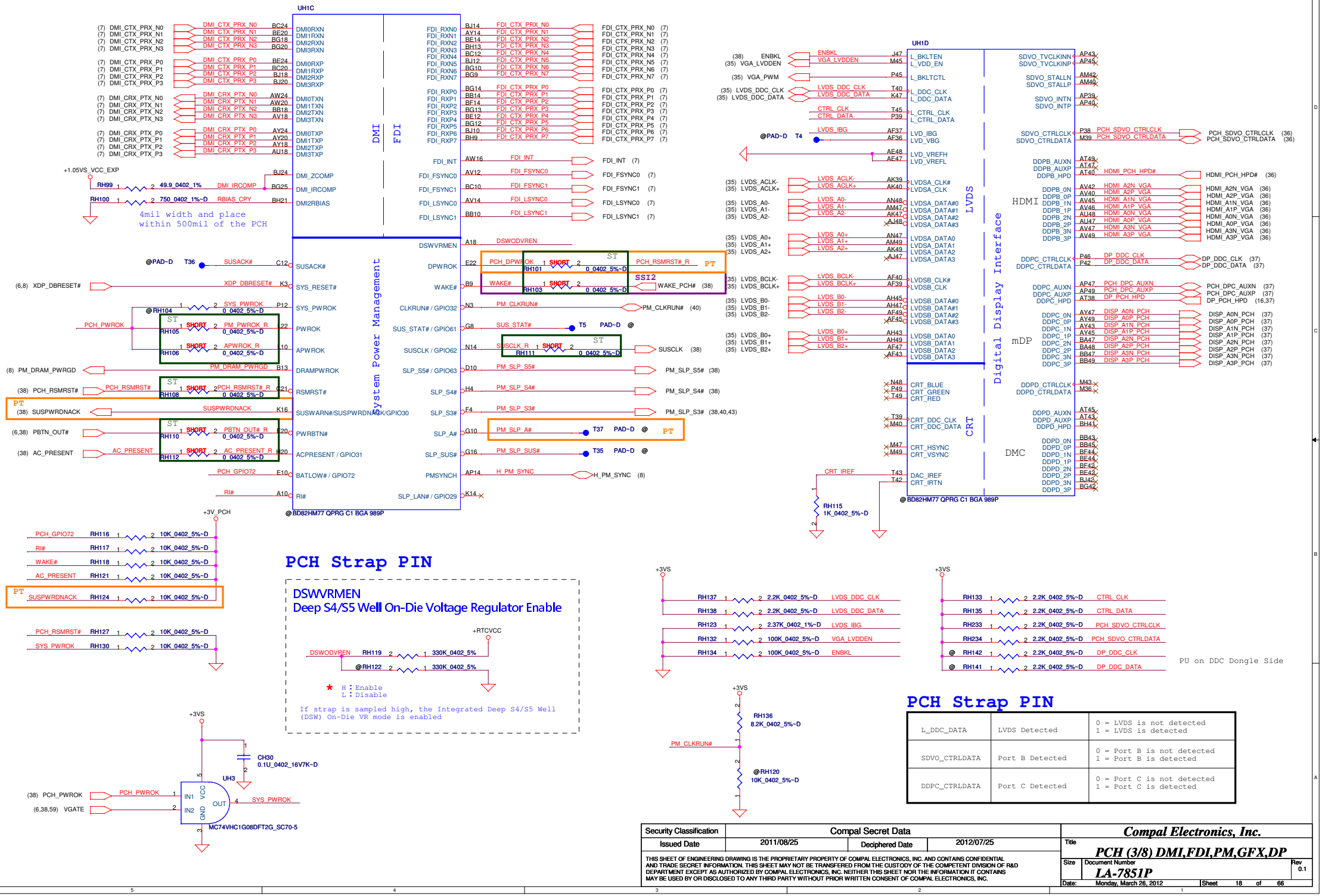
Compal Electronics, Inc.
Title PCH (2/8) PCIE, SMBUS, CLK
Size Document Number LA-7851P Rev 0.1
Date: Monday, March 26, 2012 Sheet 17 of 66


UH1C
DMI
FDI
System Power Management
@PAD~D T36
SUSACK#
SUSACK#
SYS_RESET#
SYS_PWROK
PWROK
APWROK
DRAMPWROK
RSMRST#
SUSWARN#/SUSPWRDNACK/GPIO30
PWRBTN#
ACPRESENT / GPIO31
BATLOW# / GPIO72
RI#
SLP_LAN# / GPIO29
DSWVRMEN
DPWROK
WAKE#
CLKRUN# / GPIO32
SUS_STAT# / GPIO61
SUSCLK / GPIO62
SLP_S5# / GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
DMI_ZCOMP
DMI_IRCOMP
DMI2RBIAS
4mil width and place within 500mil of the PCH
@BD82HM77 QPRG C1 BGA 989P
UH1D
LVDS
Digital Display Interface
HDMI
mDP
CRT
DMC
@BD82HM77 QPRG C1 BGA 989P
PCH Strap PIN
DSWVRMEN
Deep S4/S5 Well On-Die Voltage Regulator Enable
If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled
H : Enable
L : Disable
PU on DDC Dongle Side
PCH Strap PIN
L_DDC_DATA | LVDS Detected | 0 = LVDS is not detected 1 = LVDS is detected
SDVO_CTRLDATA | Port B Detected | 0 = Port B is not detected 1 = Port B is detected
DDPC_CTRLDATA | Port C Detected | 0 = Port C is not detected 1 = Port C is detected
UH3
MC74VHC1G08DFT2G_SC70-5
Security Classification | Compal Secret Data
Issued Date | 2011/08/25 | Deciphered Date | 2012/07/25
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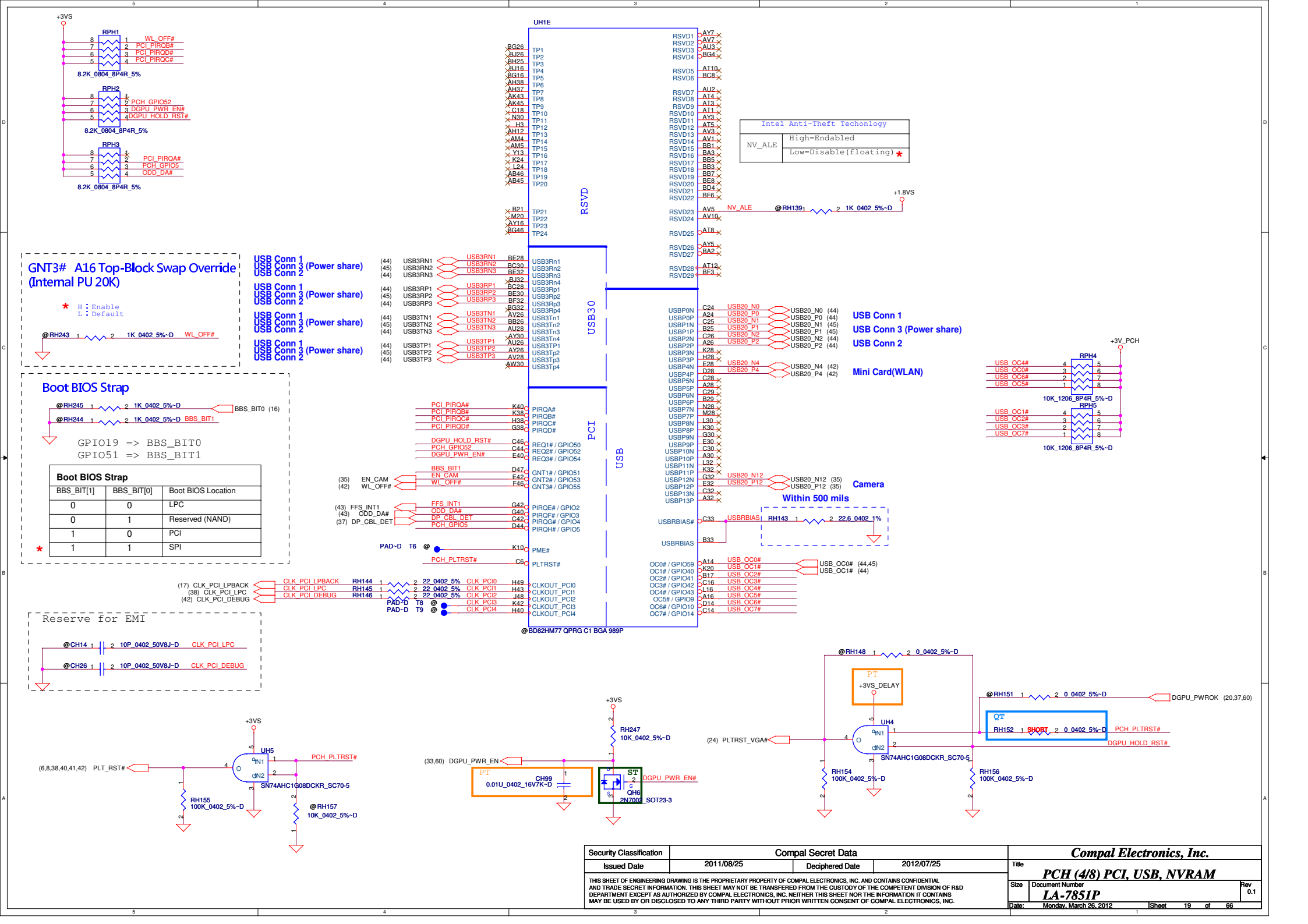
Compal Electronics, Inc.
Title: PCH (3/8) DMI,FDI,PM,GFX,DP
Size | Document Number: LA-7851P | Rev: 0.1
Date: Monday, March 26, 2012 | Sheet 18 of 66
Compal Electronics, Inc



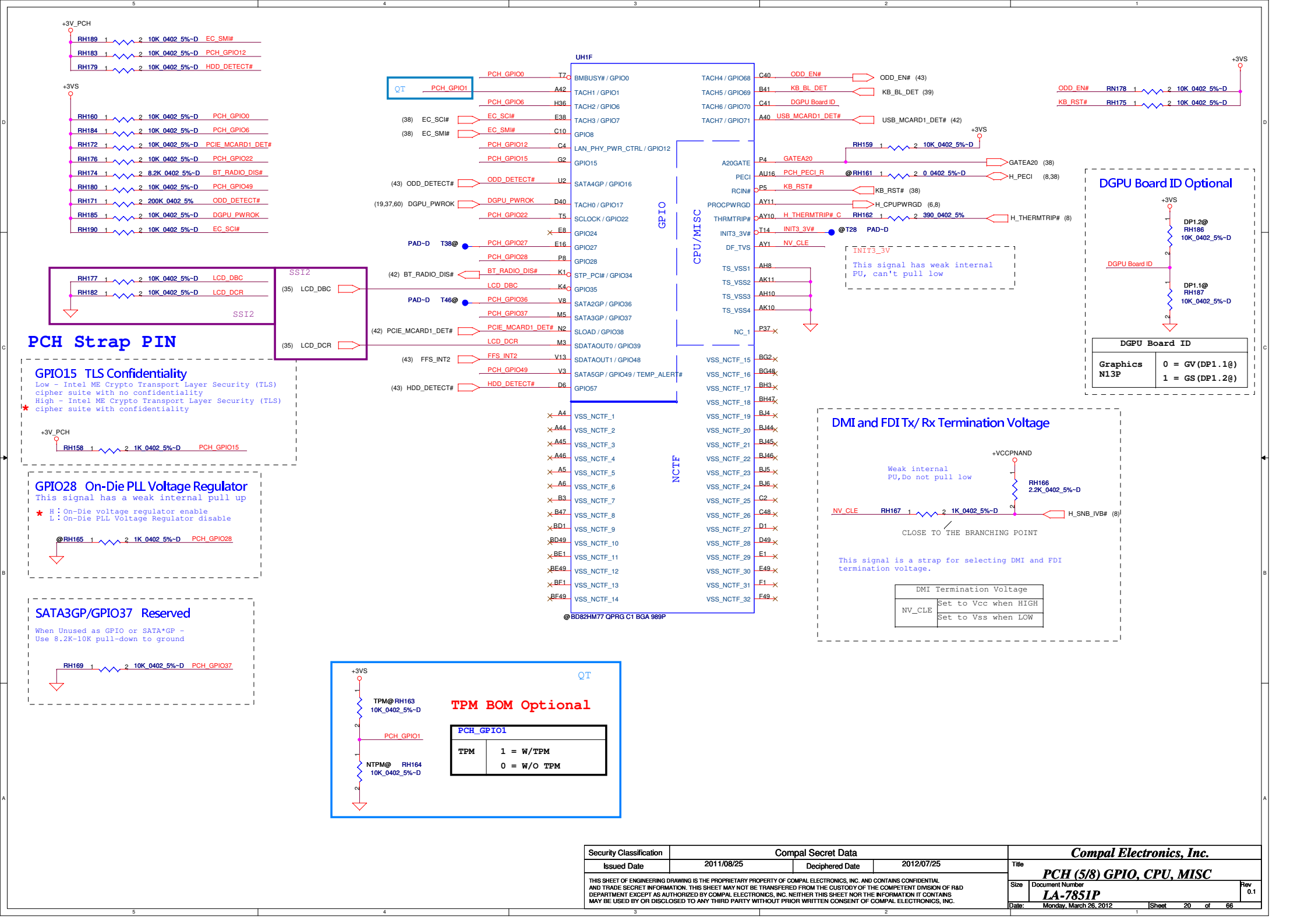
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (4/8) PCI, USB, NVRAM

Size	Document Number	Rev
	LA-7851P	0.1

Date: Monday, March 26, 2012 Sheet 19 of 66



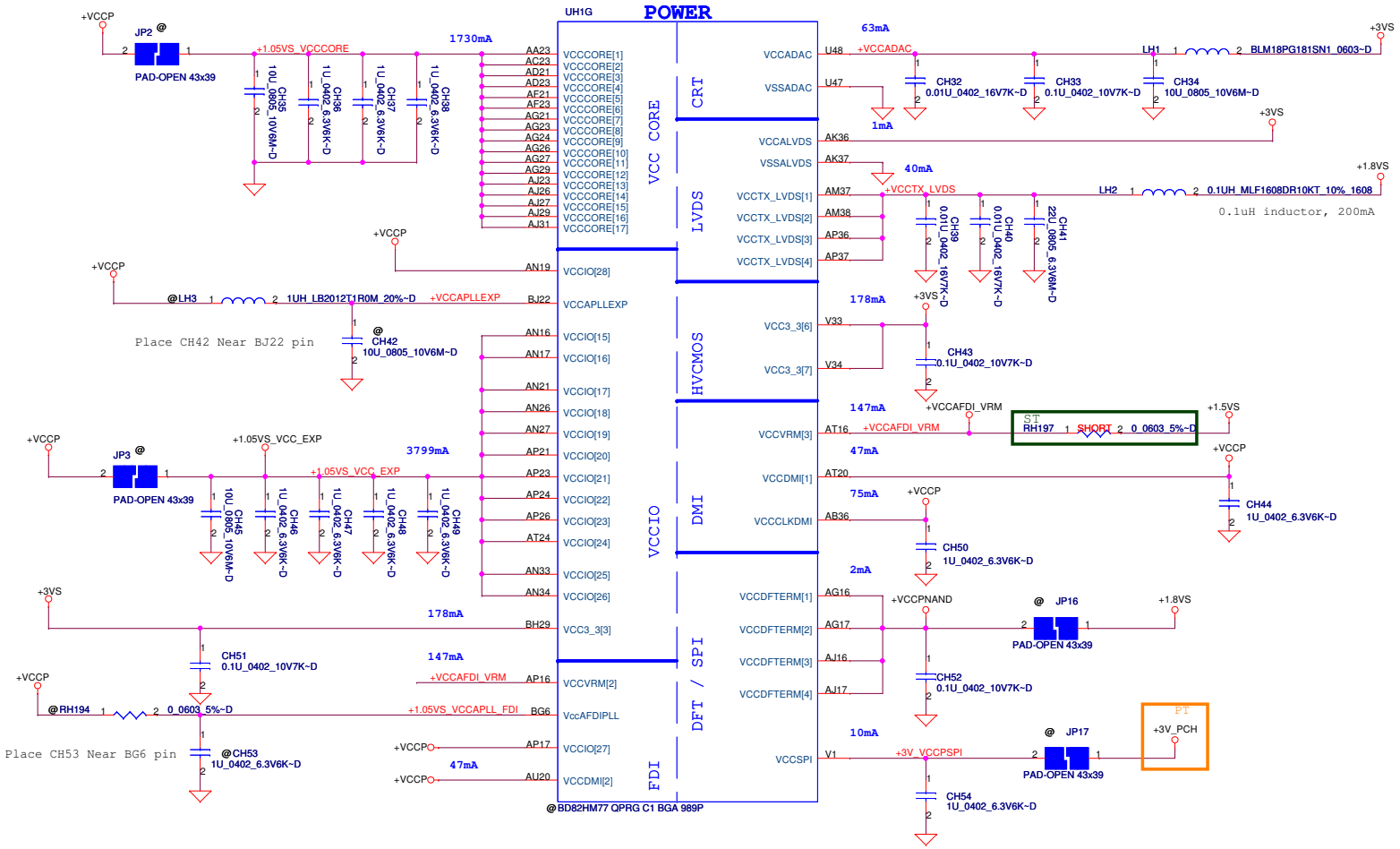
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size	Document Number	Rev
	LA-7851P	0.1

Date: Monday, March 26, 2012 Sheet 20 of 66



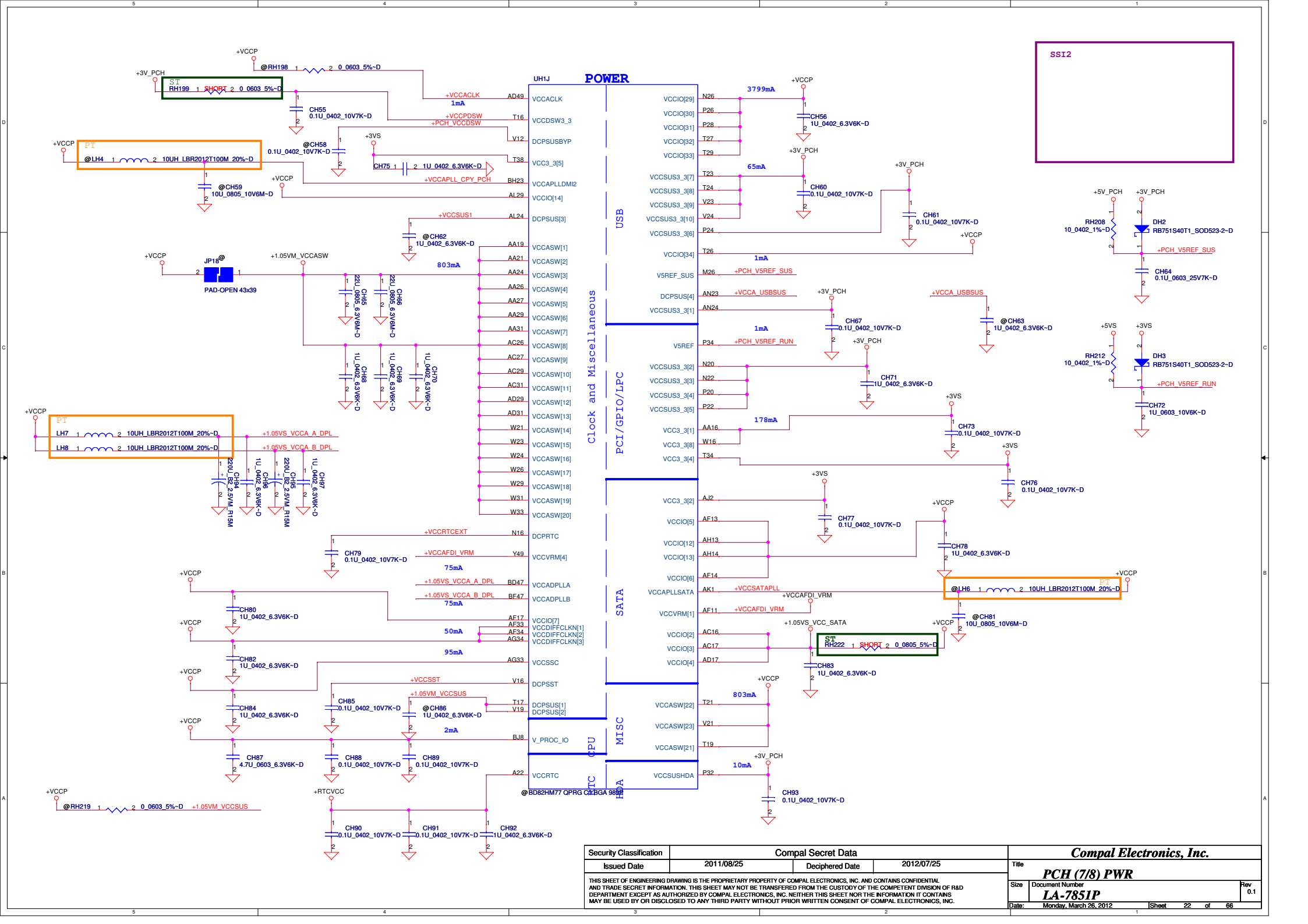
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.0075
VccADPLLB	1.05	0.0075
VccCore	1.05	1.73
VccDMI	1.05	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccpNAND	1.8	0.19
VccRTC	3.3	NA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.147
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.050
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size | Document Number: LA-7851P | Rev: 0.1

Date: Monday, March 26, 2012 | Sheet 21 of 66



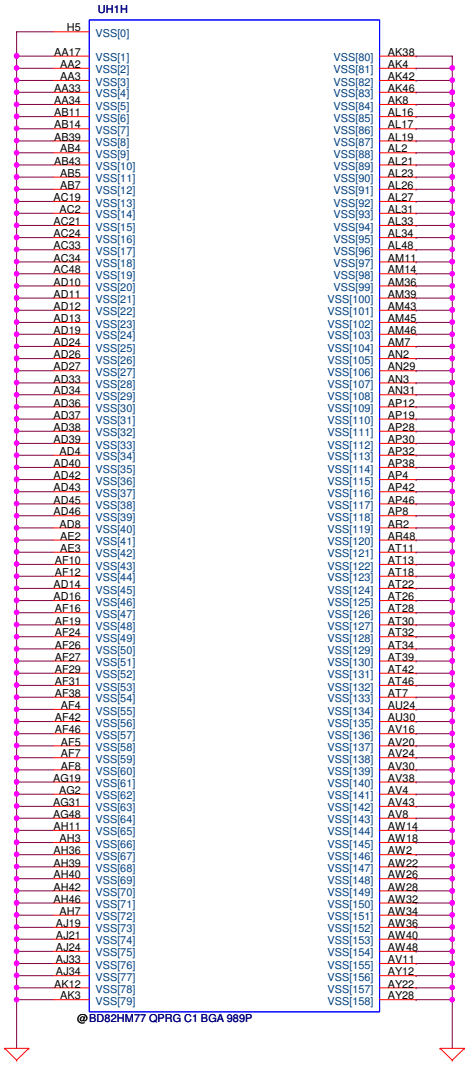
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

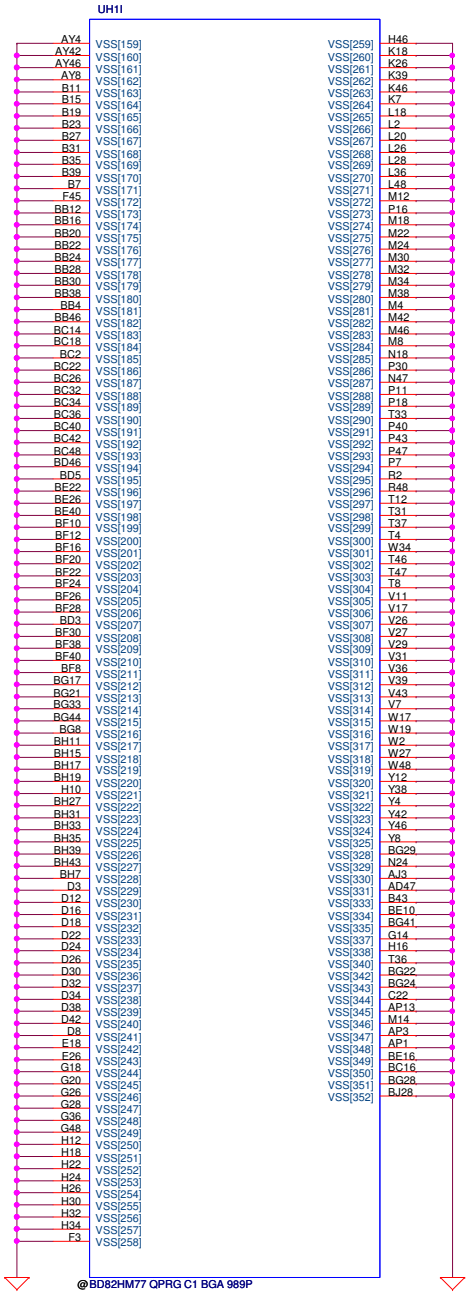
Compal Electronics, Inc.

Title: PCH (7/8) PWR

Size: | Document Number: LA-7851P | Rev: 0.1

Date: Monday, March 26, 2012 | Sheet 22 of 66





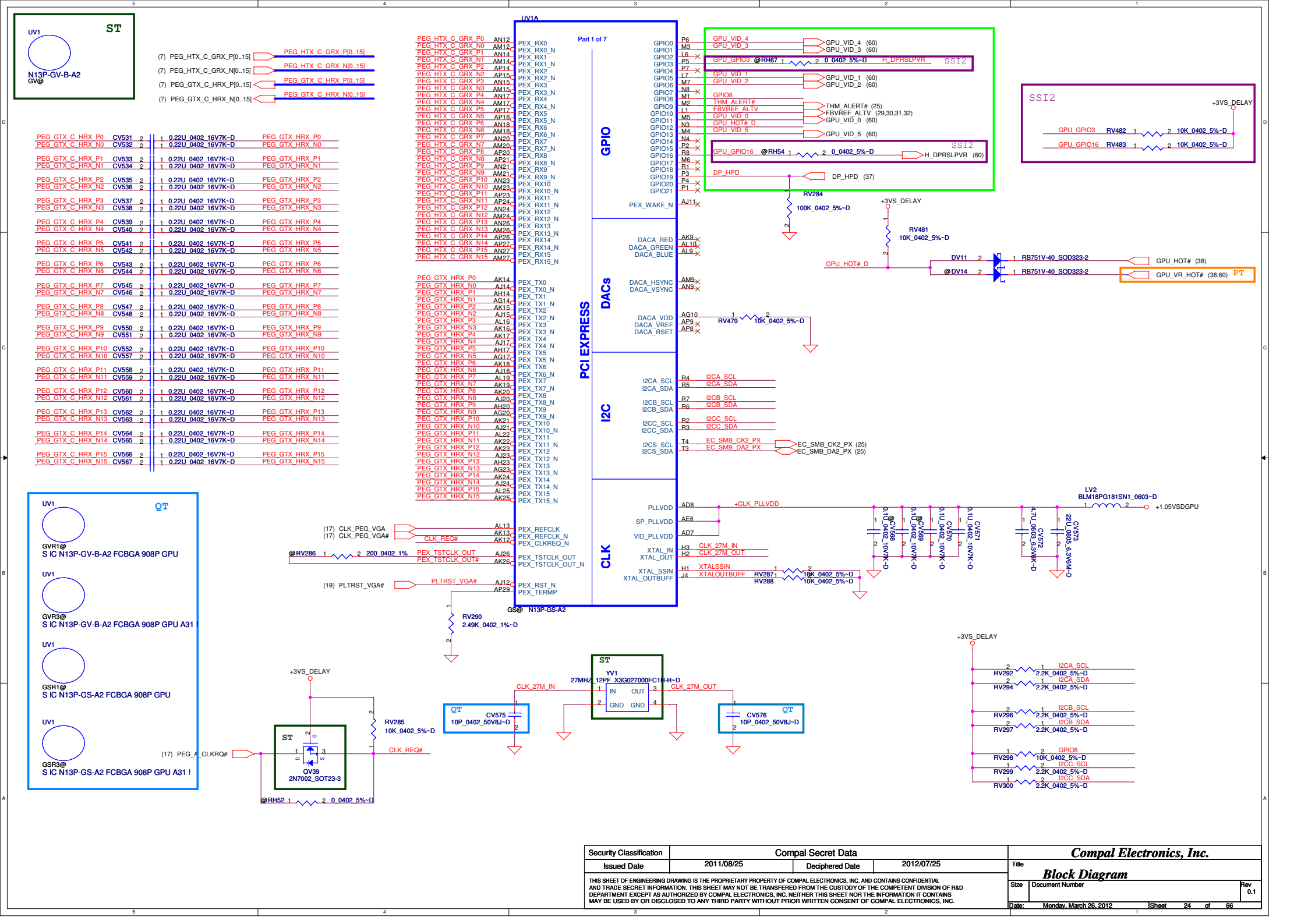
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size	Document Number	Rev
	LA-7851P	0.1

Date: Monday, March 26, 2012 Sheet 23 of 66



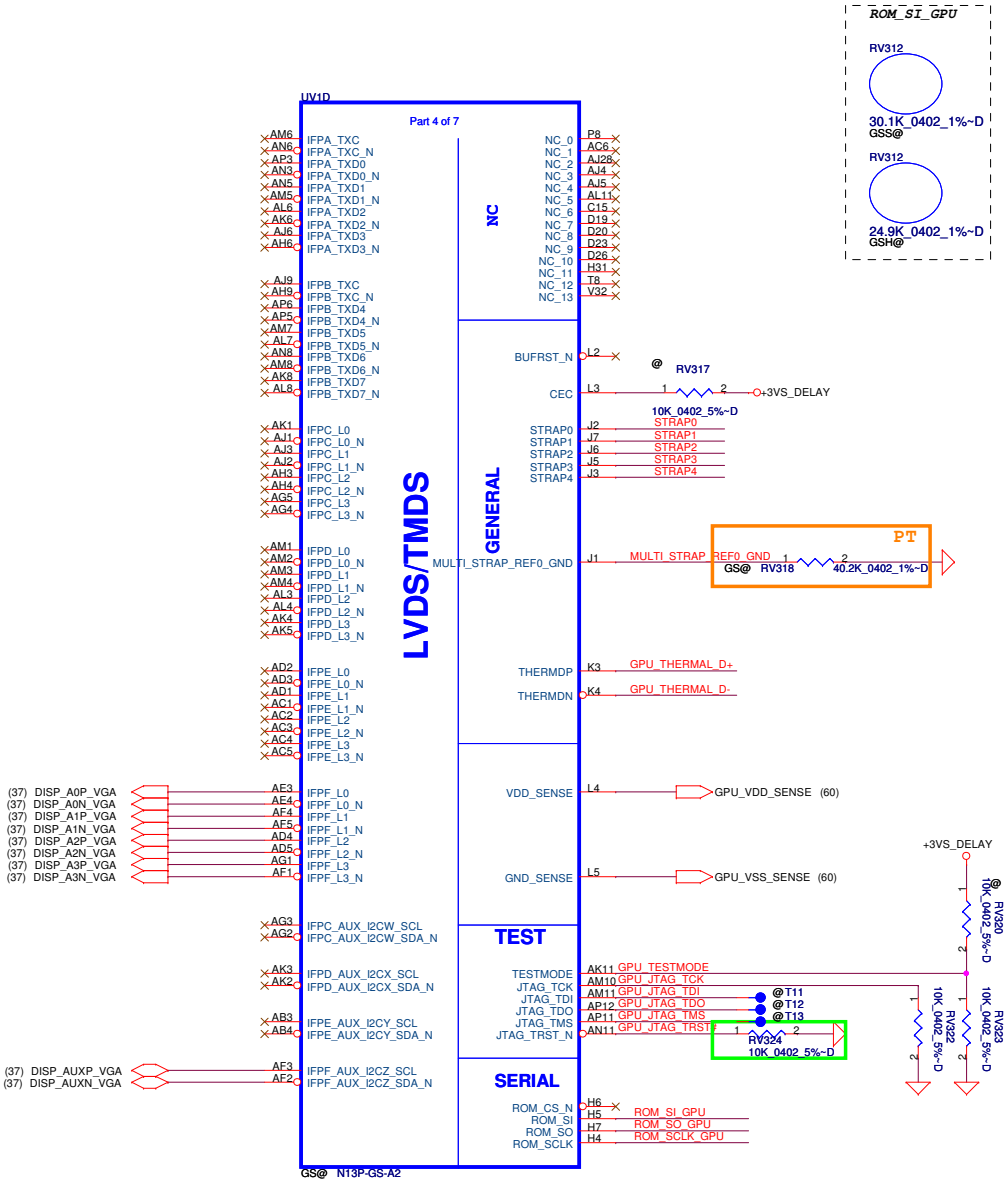
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

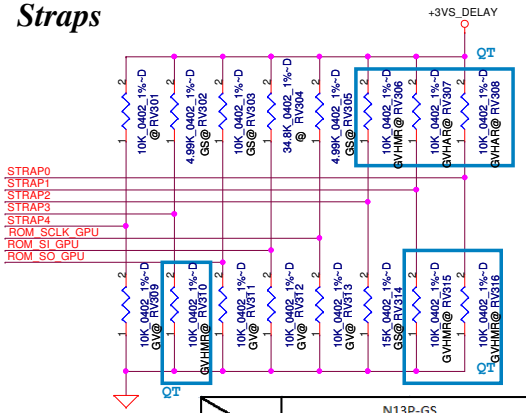
Title: **Block Diagram**

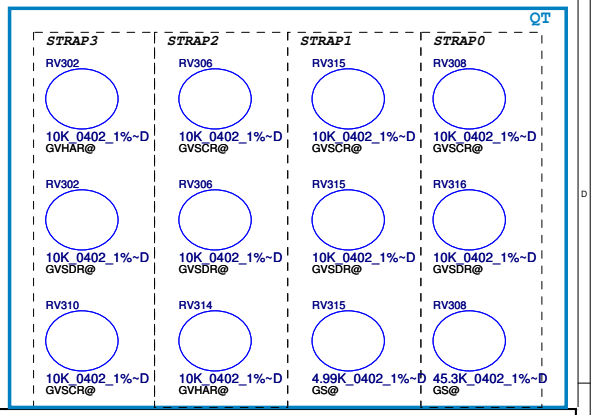
Size	Document Number	Rev
		0.1

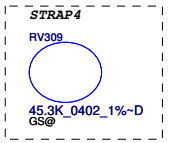
Date: Monday, March 26, 2012 Sheet 24 of 66



Straps

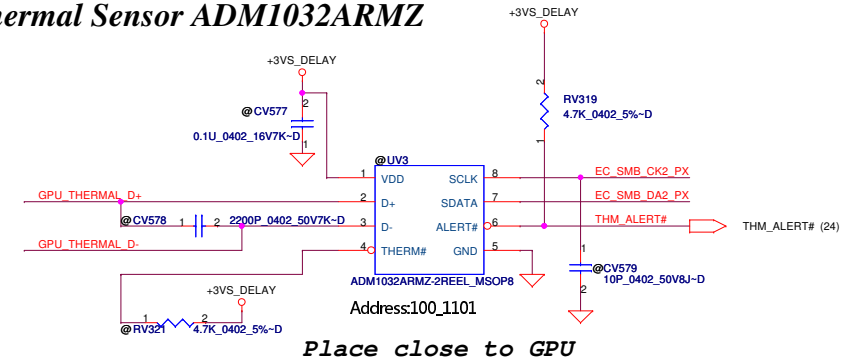




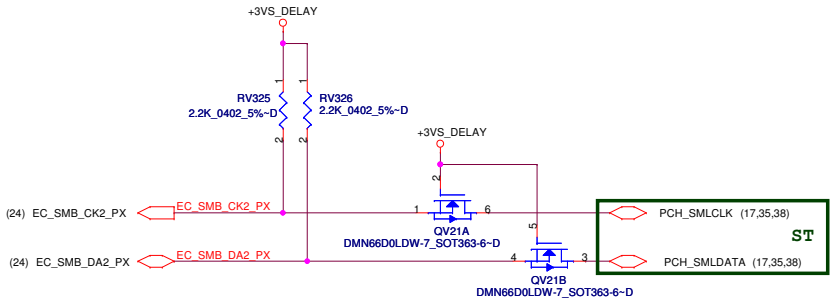


	N13P-GS		N13P-GV			
	DID: 0x0FD2		DID: 0x1140			
STRAPs	Hynix	Samsung	Hynix (H5GQ2H24MFR-T2C)	Hynix (H5GQ2H24AFR-T2C)	Samsung (K4G20325FC-HC04)	Samsung (K4G20325FD-FC04)
	128Mx16	128Mx16	128Mx16	128Mx16	128Mx16	128Mx16
ROM_SCLK	PU 5K <- (RV305)		PD 10K <- (RV313)			
ROM_SI	PD 25K <- (RV312)	PD 30K <- (RV312)	PD 10K <- (RV312)			
ROM_SO	PU 10K <- (RV303)		PD 10K <- (RV311)			
STRAP0	PU 45.3K <- (RV308)		PD 10K <- (RV316)	PU 10K <- (RV308)	PU 10K <- (RV308)	PD 10K <- (RV316)
STRAP1	PD 4.99K <- (RV315)		PD 10K <- (RV315)	PU 10K <- (RV307)	PD 10K <- (RV315)	PD 10K <- (RV315)
STRAP2	PD 15K <- (RV314)		PU 10K <- (RV306)	PD 10K <- (RV314)	PU 10K <- (RV306)	PU 10K <- (RV306)
STRAP3	PU 5K <- (RV302)		PD 10K <- (RV310)	PU 10K <- (RV302)	PD 10K <- (RV310)	PU 10K <- (RV302)
STRAP4	PD 45K <- (RV309)		PD 10K <- (RV309)			

VGA Thermal Sensor ADM1032ARMZ



Place close to GPU



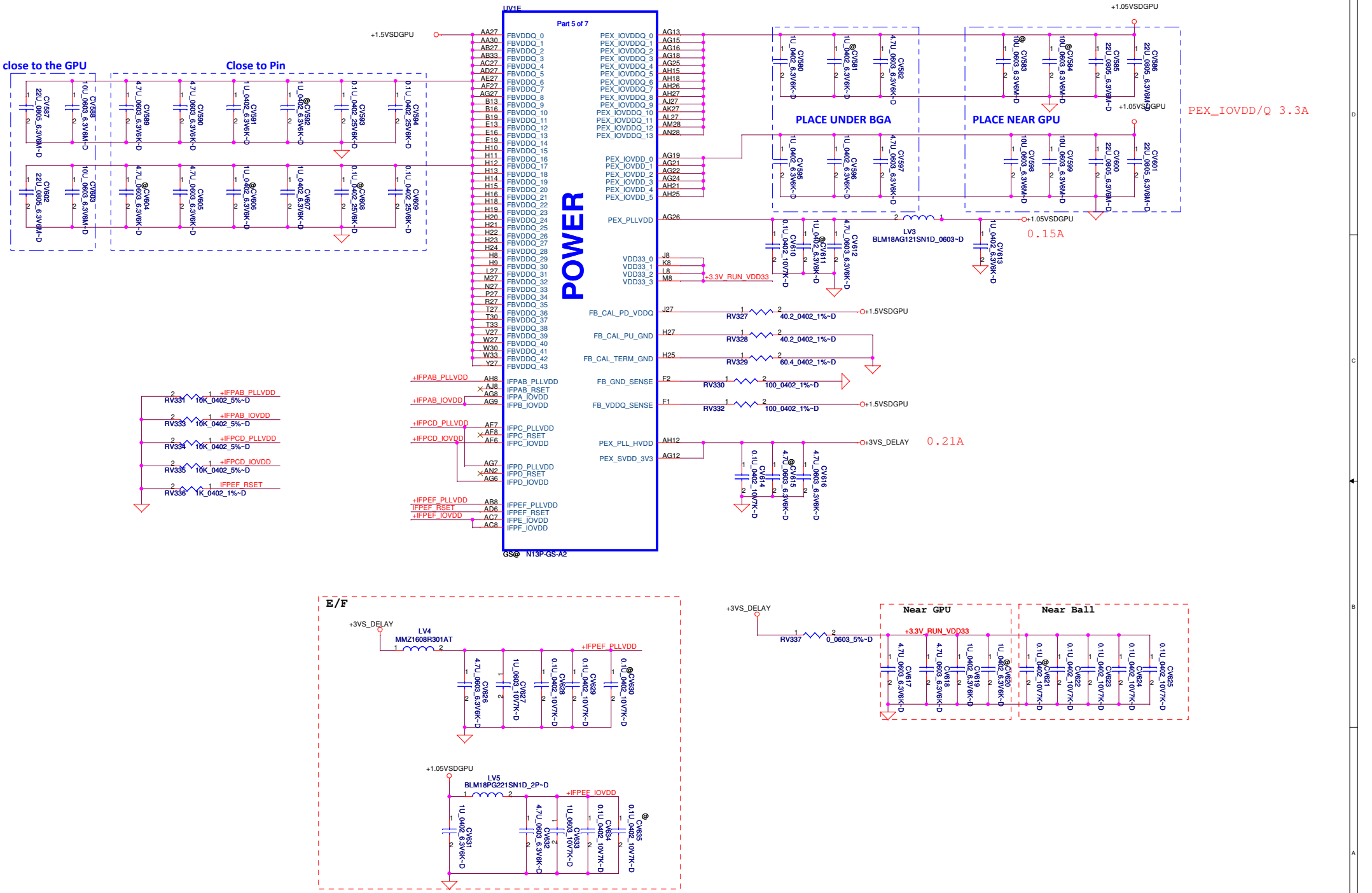
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

Date: Monday, March 26, 2012 Sheet 25 of 66



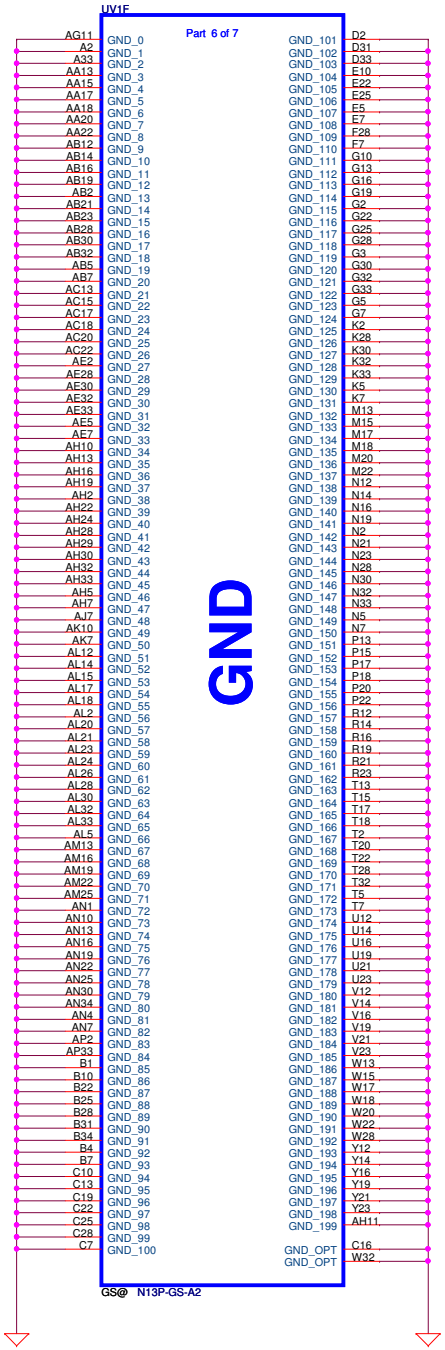
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

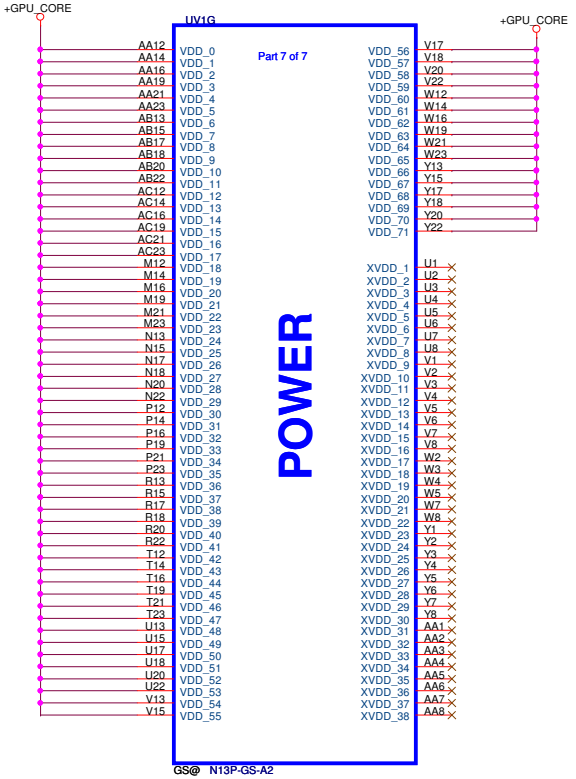
Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

Date: Monday, March 26, 2012 Sheet 26 of 66





Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

Date: Monday, March 26, 2012 Sheet 27 of 66

GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD21	WE#
CMD0	CMD16	CS#
CMD8	CMD24	ABI#
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD2	CMD18	A2_BA0
CMD1	CMD17	A3_BA3
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD7	CMD23	A6_A11
CMD6	CMD22	A7_A8
CMD9	CMD25	A12_FRU
CMD14	CMD30	CKE#
CMD13	CMD29	RESET#

CHANNEL-B NOT TO USE, NEED TO BE DISABLED

(29) FBA_D[0..31] — FBA_D[0..31]
(30) FBA_D[32..63] — FBA_D[32..63]
(29,30) FBA_CMD[0..31] — FBA_CMD[0..31]
(30) FBA_DBI[4..7] — FBA_DBI[4..7]
(29) FBA_DBI[0..3] — FBA_DBI[0..3]
(30) FBA_EDC[4..7] — FBA_EDC[4..7]
(29) FBA_EDC[0..3] — FBA_EDC[0..3]

(31) FBB_D[0..31] — FBB_D[0..31]
(32) FBB_D[32..63] — FBB_D[32..63]
(31,32) FBB_CMD[0..31] — FBB_CMD[0..31]
(32) FBB_DBI[4..7] — FBB_DBI[4..7]
(31) FBB_DBI[0..3] — FBB_DBI[0..3]
(32) FBB_EDC[4..7] — FBB_EDC[4..7]
(31) FBB_EDC[0..3] — FBB_EDC[0..3]

UV1B — MEMORY INTERFACE A — Part 2 of 7

+1.5VSDGPU
RV338 10K_0402_5%-D — CKE_H — FBA_CMD30
RV339 10K_0402_5%-D — CKE_L — FBA_CMD14
RV340 10K_0402_5%-D — RST_H* — FBA_CMD29
RV341 10K_0402_5%-D — RST_L* — FBA_CMD13

FBA_D0 L28, FBA_D1 M29, FBA_D2 L29, FBA_D3 M28, FBA_D4 N31, FBA_D5 P29, FBA_D6 R29, FBA_D7 P28, FBA_D8 J28, FBA_D9 H29, FBA_D10 J29, FBA_D11 H28, FBA_D12 G29, FBA_D13 E31, FBA_D14 E32, FBA_D15 F30, FBA_D16 C34, FBA_D17 D32, FBA_D18 B33, FBA_D19 C33, FBA_D20 F33, FBA_D21 F32, FBA_D22 H33, FBA_D23 H32, FBA_D24 P34, FBA_D25 P32, FBA_D26 P31, FBA_D27 P33, FBA_D28 L31, FBA_D29 L34, FBA_D30 L32, FBA_D31 L33, FBA_D32 AG28, FBA_D33 AF29, FBA_D34 AG29, FBA_D35 AF28, FBA_D36 AD30, FBA_D37 AD29, FBA_D38 AC29, FBA_D39 AD28, FBA_D40 AJ29, FBA_D41 AK29, FBA_D42 AJ30, FBA_D43 AK28, FBA_D44 AM29, FBA_D45 AM31, FBA_D46 AN29, FBA_D47 AM30, FBA_D48 AN31, FBA_D49 AN32, FBA_D50 AP30, FBA_D51 AP32, FBA_D52 AM33, FBA_D53 AL31, FBA_D54 AK33, FBA_D55 AK32, FBA_D56 AD34, FBA_D57 AD32, FBA_D58 AC30, FBA_D59 AD33, FBA_D60 AF31, FBA_D61 AG34, FBA_D62 AG32, FBA_D63 AG33

FBA_CMD0 U30, FBA_CMD1 T31, FBA_CMD2 U29, FBA_CMD3 R34, FBA_CMD4 R33, FBA_CMD5 U32, FBA_CMD6 U33, FBA_CMD7 U28, FBA_CMD8 V28, FBA_CMD9 V29, FBA_CMD10 V30, FBA_CMD11 U34, FBA_CMD12 U31, FBA_CMD13 V34, FBA_CMD14 V33, FBA_CMD15 Y32, FBA_CMD16 AA31, FBA_CMD17 AA29, FBA_CMD18 AA28, FBA_CMD19 AC34, FBA_CMD20 AC33, FBA_CMD21 AA32, FBA_CMD22 AA33, FBA_CMD23 Y28, FBA_CMD24 Y29, FBA_CMD25 W31, FBA_CMD26 Y30, FBA_CMD27 AA34, FBA_CMD28 Y31, FBA_CMD29 Y34, FBA_CMD30 Y33, FBA_CMD31 V31

FBA_DQM0 P30, FBA_DQM1 F31, FBA_DQM2 F34, FBA_DQM3 M32, FBA_DQM4 AD31, FBA_DQM5 AL29, FBA_DQM6 AM32, FBA_DQM7 AF34

FBA_DBI0 P30, FBA_DBI1 F31, FBA_DBI2 F34, FBA_DBI3 M32, FBA_DBI4 AD31, FBA_DBI5 AL29, FBA_DBI6 AM32, FBA_DBI7 AF34

FBA_DQS_RN0 M30, FBA_DQS_RN1 H30, FBA_DQS_RN2 E34, FBA_DQS_RN3 M34, FBA_DQS_RN4 AF30, FBA_DQS_RN5 AK31, FBA_DQS_RN6 AM34, FBA_DQS_RN7 AF32

FBA_DQS_WP0 M31, FBA_DQS_WP1 G31, FBA_DQS_WP2 E33, FBA_DQS_WP3 M33, FBA_DQS_WP4 AE31, FBA_DQS_WP5 AK30, FBA_DQS_WP6 AN33, FBA_DQS_WP7 AF33

FBA_EDC0 M31, FBA_EDC1 G31, FBA_EDC2 E33, FBA_EDC3 M33, FBA_EDC4 AE31, FBA_EDC5 AK30, FBA_EDC6 AN33, FBA_EDC7 AF33

FBA_CMD_RFU0 R32, FBA_CMD_RFU1 AC32

FBA_CLK0 R30 — CLKA0 (29)
FBA_CLK0_N R31 — CLKA0# (29)
FBA_CLK1 AB31 — CLKA1 (30)
FBA_CLK1_N AC31 — CLKA1# (30)

FBA_WCK01 K31, FBA_WCK01_N L30, FBA_WCK23 H34, FBA_WCK23_N J34, FBA_WCK45 AG30, FBA_WCK45_N AG31, FBA_WCK67 AJ34, FBA_WCK67_N AK34

FBA_WCK01 (29), FBA_WCK01# (29), FBA_WCK23 (29), FBA_WCK23# (29), FBA_WCK45 (30), FBA_WCK45# (30), FBA_WCK67 (30), FBA_WCK67# (30)

NC FBA_WCKB01 J30, FBA_WCKB01_N J31, FBA_WCKB23 J32, FBA_WCKB23_N J33, FBA_WCKB45 AH31, FBA_WCKB45_N AJ31, FBA_WCKB67 AJ32, FBA_WCKB67_N AJ33

THE FBA_ECKBxx ARE USED ON GK107. ON GF108 AND GF117

+FBA_PLL_AVDD U27
+FB_VREF H26
FB_VREF
FB_DLL_AVDD K27
FB_CLAMP E1
FBA_DEBUG0 R28
FBA_DEBUG1 AC28

+FBA_PLL_AVDD — CV637 1U_0402_10V7K-D
+1.5VSDGPU — RV344 60.4_0402_1%-D — RV345 60.4_0402_1%-D

GS@ N13P-GS-A2

UV1C — MEMORY INTERFACE B — Part 3 of 7

FBB_D0 G9, FBB_D1 E9, FBB_D2 G8, FBB_D3 F9, FBB_D4 F11, FBB_D5 G11, FBB_D6 F12, FBB_D7 G12, FBB_D8 G6, FBB_D9 F5, FBB_D10 E6, FBB_D11 F6, FBB_D12 F4, FBB_D13 G4, FBB_D14 E2, FBB_D15 F3, FBB_D16 C2, FBB_D17 D4, FBB_D18 D3, FBB_D19 C1, FBB_D20 B3, FBB_D21 C4, FBB_D22 B5, FBB_D23 C5, FBB_D24 A11, FBB_D25 C11, FBB_D26 D11, FBB_D27 B11, FBB_D28 D8, FBB_D29 A8, FBB_D30 C8, FBB_D31 B8, FBB_D32 F24, FBB_D33 G23, FBB_D34 E24, FBB_D35 G24, FBB_D36 D21, FBB_D37 E21, FBB_D38 G21, FBB_D39 F21, FBB_D40 G27, FBB_D41 D27, FBB_D42 G26, FBB_D43 E27, FBB_D44 E29, FBB_D45 F29, FBB_D46 E30, FBB_D47 D30, FBB_D48 A32, FBB_D49 C31, FBB_D50 C32, FBB_D51 B32, FBB_D52 D29, FBB_D53 A29, FBB_D54 C29, FBB_D55 B29, FBB_D56 B21, FBB_D57 C23, FBB_D58 A21, FBB_D59 C21, FBB_D60 B24, FBB_D61 C24, FBB_D62 B26, FBB_D63 C26

FBB_CMD0 D13, FBB_CMD1 E14, FBB_CMD2 F14, FBB_CMD3 A12, FBB_CMD4 B12, FBB_CMD5 C14, FBB_CMD6 B14, FBB_CMD7 G15, FBB_CMD8 F15, FBB_CMD9 E15, FBB_CMD10 D15, FBB_CMD11 A14, FBB_CMD12 D14, FBB_CMD13 A15, FBB_CMD14 B15, FBB_CMD15 C17, FBB_CMD16 D18, FBB_CMD17 E18, FBB_CMD18 F18, FBB_CMD19 A20, FBB_CMD20 B20, FBB_CMD21 C18, FBB_CMD22 B18, FBB_CMD23 G18, FBB_CMD24 G17, FBB_CMD25 F17, FBB_CMD26 D16, FBB_CMD27 A18, FBB_CMD28 D17, FBB_CMD29 A17, FBB_CMD30 B17, FBB_CMD31 E17

FBB_DQM0 E11, FBB_DQM1 E3, FBB_DQM2 A3, FBB_DQM3 C9, FBB_DQM4 F23, FBB_DQM5 F27, FBB_DQM6 C30, FBB_DQM7 A24

FBB_DBI0 E11, FBB_DBI1 E3, FBB_DBI2 A3, FBB_DBI3 C9, FBB_DBI4 F23, FBB_DBI5 F27, FBB_DBI6 C30, FBB_DBI7 A24

FBB_DQS_RN0 D9, FBB_DQS_RN1 E4, FBB_DQS_RN2 B2, FBB_DQS_RN3 A9, FBB_DQS_RN4 D22, FBB_DQS_RN5 D28, FBB_DQS_RN6 A30, FBB_DQS_RN7 B23

FBB_DQS_WP0 D10, FBB_DQS_WP1 D5, FBB_DQS_WP2 C3, FBB_DQS_WP3 B9, FBB_DQS_WP4 E23, FBB_DQS_WP5 E28, FBB_DQS_WP6 B30, FBB_DQS_WP7 A23

FBB_EDC0 D10, FBB_EDC1 D5, FBB_EDC2 C3, FBB_EDC3 B9, FBB_EDC4 E23, FBB_EDC5 E28, FBB_EDC6 B30, FBB_EDC7 A23

FBB_CMD_RFU0 C12, FBB_CMD_RFU1 C20

FBB_CLK0 D12 — CLKB0 (31)
FBB_CLK0_N E12 — CLKB0# (31)
FBB_CLK1 E20 — CLKB1 (32)
FBB_CLK1_N F20 — CLKB1# (32)

FBB_WCK01 F8, FBB_WCK01_N E8, FBB_WCK23 A5, FBB_WCK23_N A6, FBB_WCK45 D24, FBB_WCK45_N D25, FBB_WCK67 B27, FBB_WCK67_N C27

FBB_WCK01 (31), FBB_WCK01# (31), FBB_WCK23 (31), FBB_WCK23# (31), FBB_WCK45 (32), FBB_WCK45# (32), FBB_WCK67 (32), FBB_WCK67# (32)

FBB_WCKB01 D6, FBB_WCKB01_N D7, FBB_WCKB23 C6, FBB_WCKB23_N B6, FBB_WCKB45 B22, FBB_WCKB45_N F26, FBB_WCKB67 E26, FBB_WCKB67_N A26

THE FBA_ECKBxx ARE USED ON GK107. NC ON GF108 AND GF117

+FBA_PLL_AVDD H17
FBB_PLL_AVDD
FBB_DEBUG0 G14
FBB_DEBUG1 G20

+FBA_PLL_AVDD — CV639 0.1U_0402_10V7K-D
+1.5VSDGPU — RV346 60.4_0402_1%-D — RV347 60.4_0402_1%-D

GS@ N13P-GS-A2

+1.5VSDGPU
RV409 10K_0402_5%-D — CKE_H — FBB_CMD30
RV410 10K_0402_5%-D — CKE_L — FBB_CMD14
RV414 10K_0402_5%-D — RST_H* — FBB_CMD29
RV418 10K_0402_5%-D — RST_L* — FBB_CMD13

for Test/Debug

+1.5VSDGPU
RV342 1.1K_0402_1%-D — RV343 1.1K_0402_1%-D — 16mil — +FB_VREF
CV638 0.01U_0402_16V7K-D

+1.05VSDGPU

NEED FIND 30R BEAD
LV6 BLM18PG300SN1D_2P_D
+FBA_PLL_AVDD
CV642 1U_0402_6.3V6K-D
CV639 22U_0805_6.3V6M-D
CV640 1U_0402_6.3V6K-D
CV641 0.1U_0402_10V7K-D

Security Classification	Compal Secret Data		
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Title: **Block Diagram**

Size	Document Number	Rev
		0.1

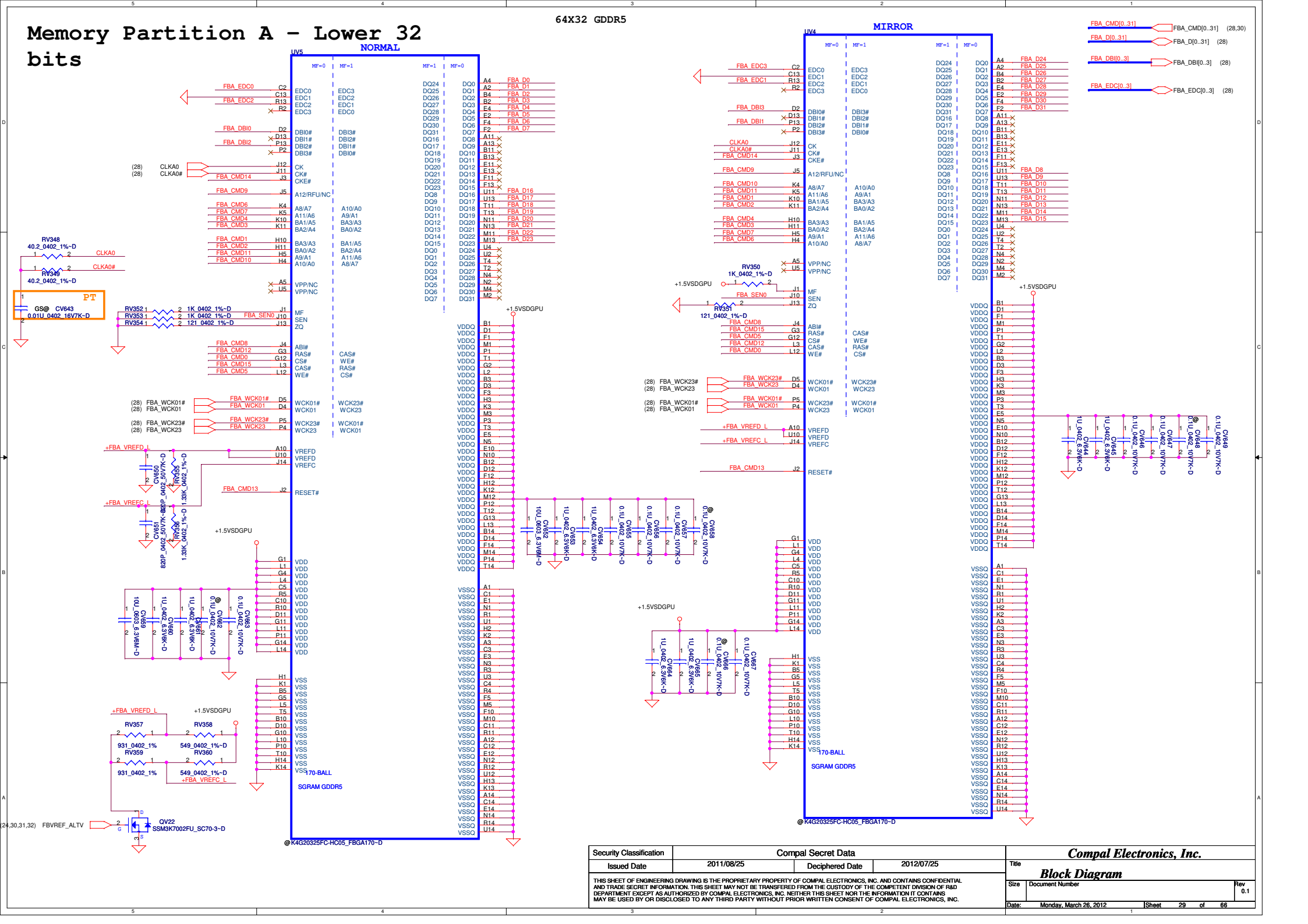
Date: Monday, March 26, 2012 — Sheet 28 of 66

Memory Partition A – Lower 32 bits

64X32 GDDR5

NORMAL

MIRROR



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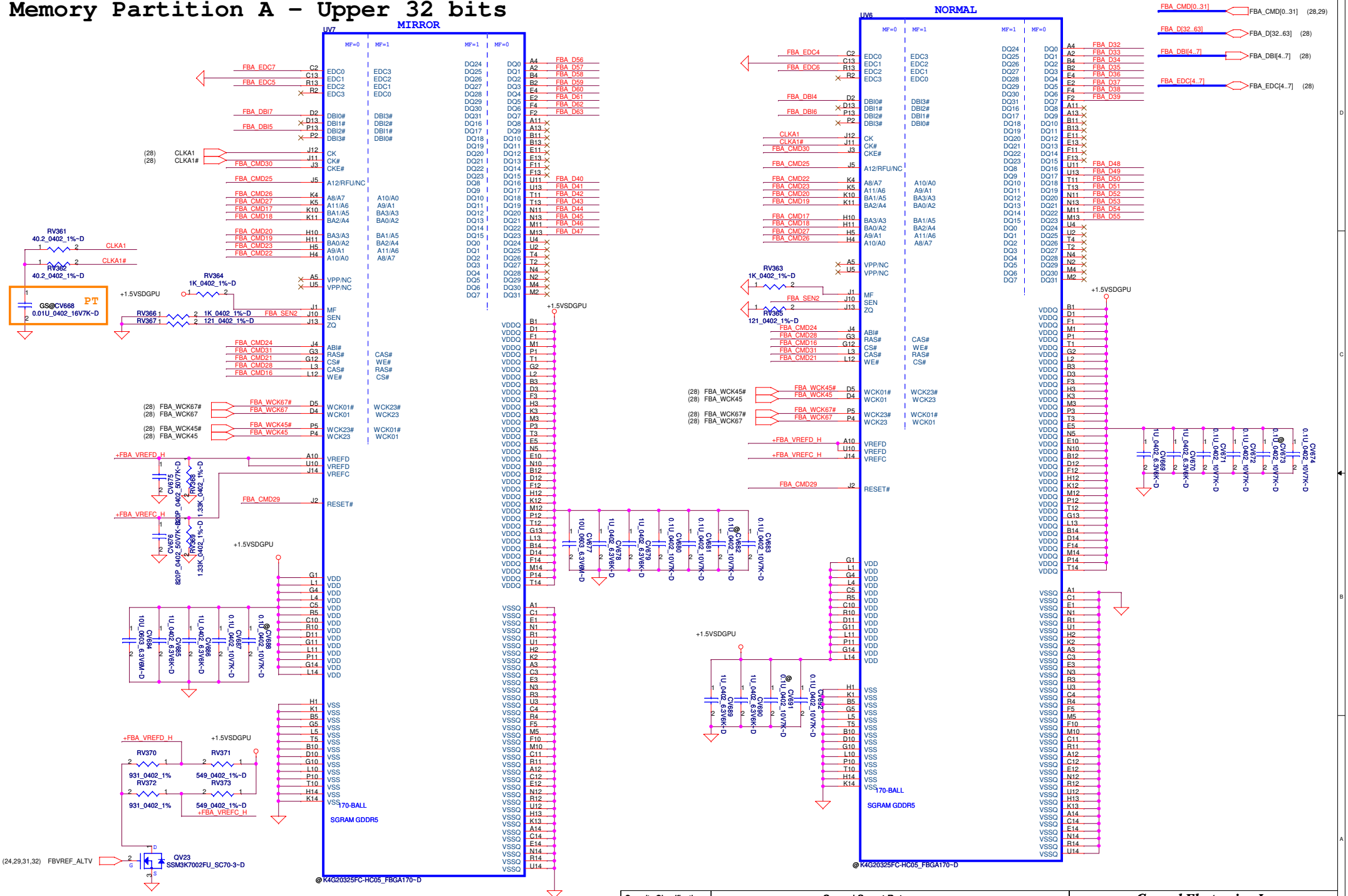
Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

Date: Monday, March 26, 2012 | Sheet 29 of 66

Memory Partition A – Upper 32 bits



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Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

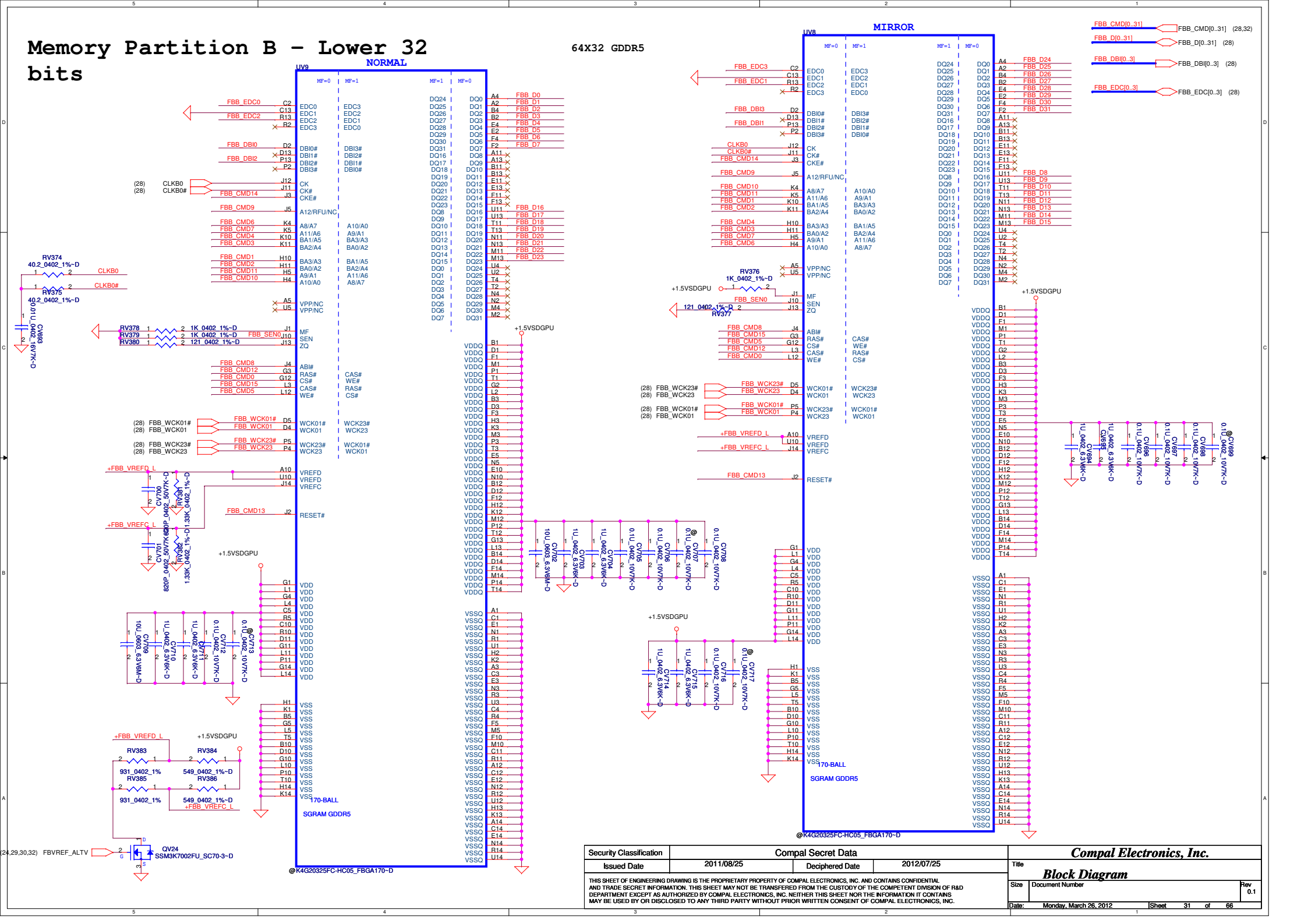
Date: Monday, March 26, 2012 | Sheet 30 of 66

Memory Partition B – Lower 32 bits

64X32 GDDR5

NORMAL

MIRROR



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Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

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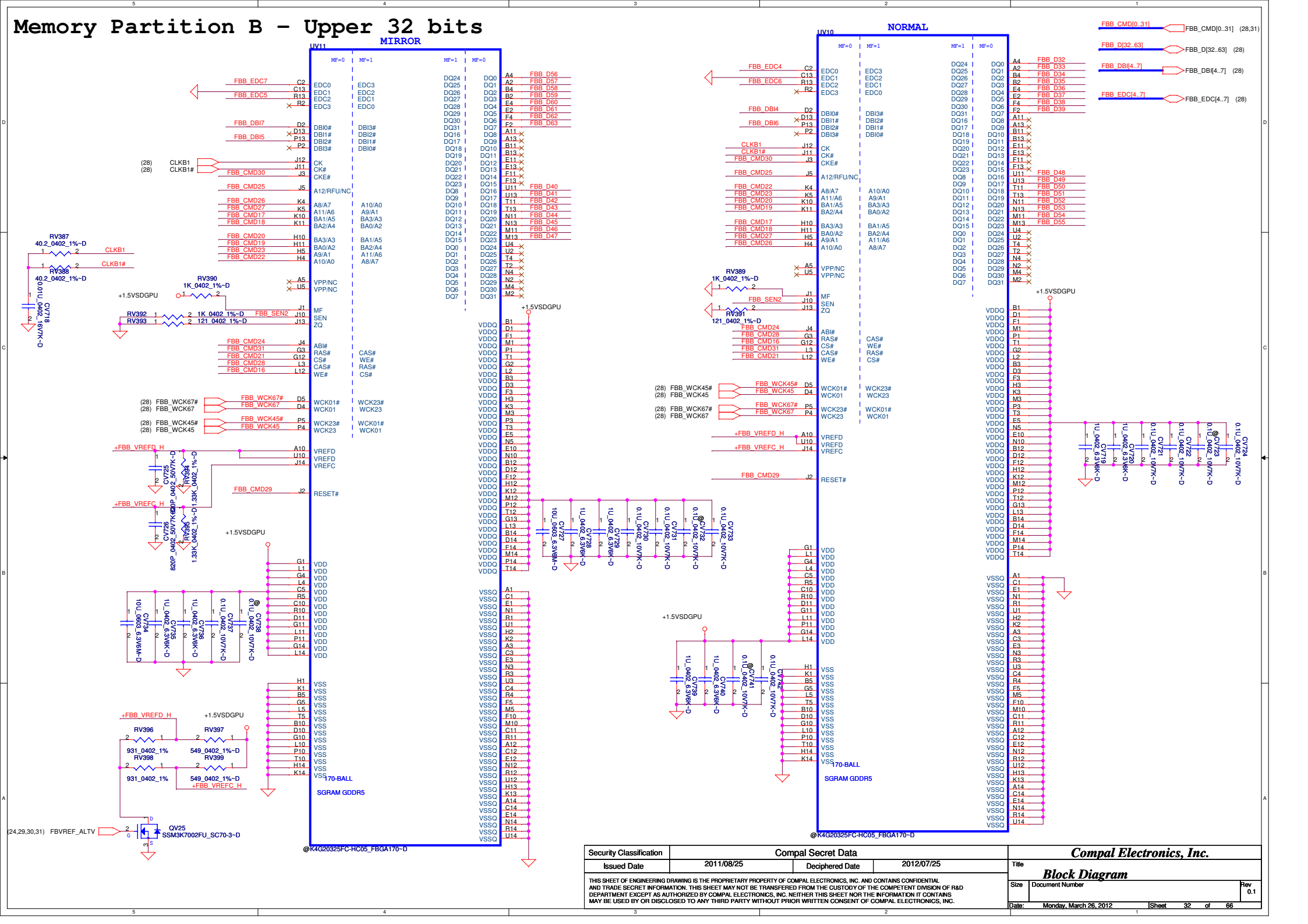
Memory Partition B – Upper 32 bits



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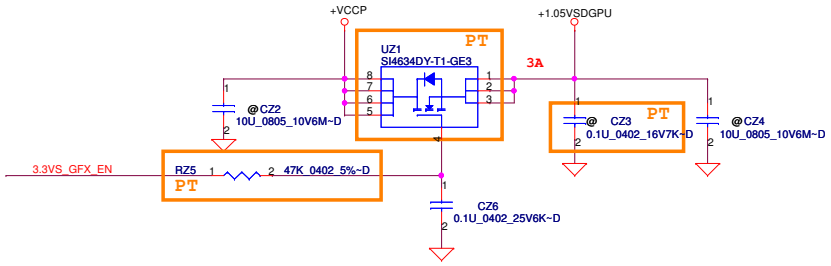
Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

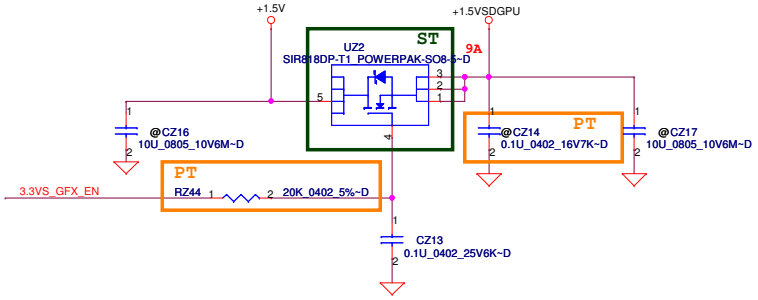
Date: Monday, March 26, 2012 Sheet 32 of 66

+1.05VS to +1.05VSDGPU

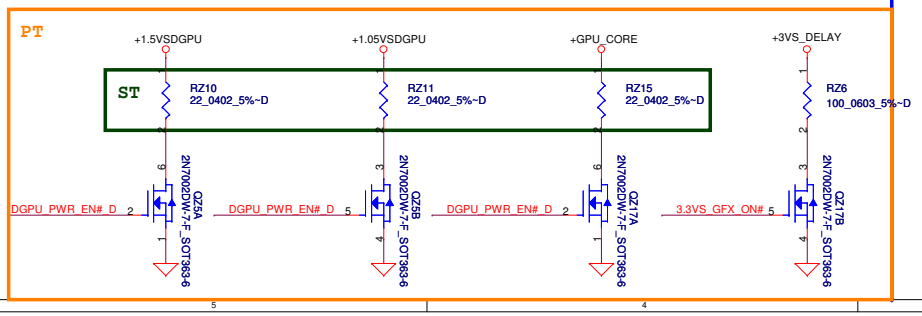


PT

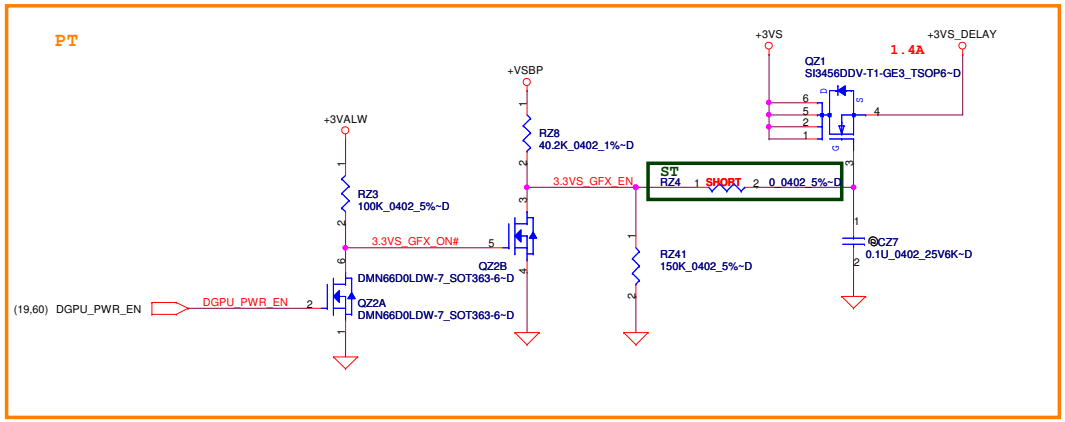
+1.5V to +1.5VSDGPU



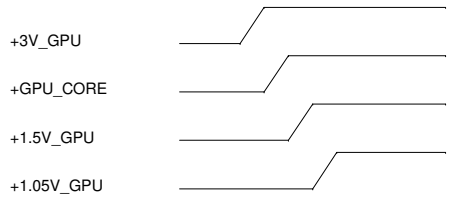
Discharge



+3VS to +3VS_DELAY

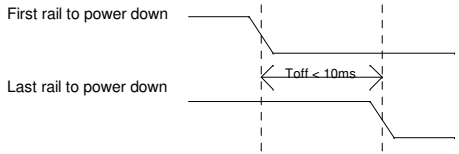


GPU Power Up Power Rail Sequence

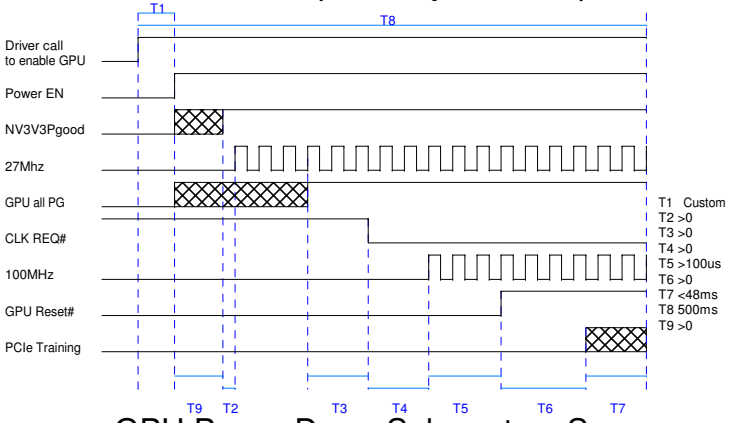


The ramp time for any rail must be more than 40us.

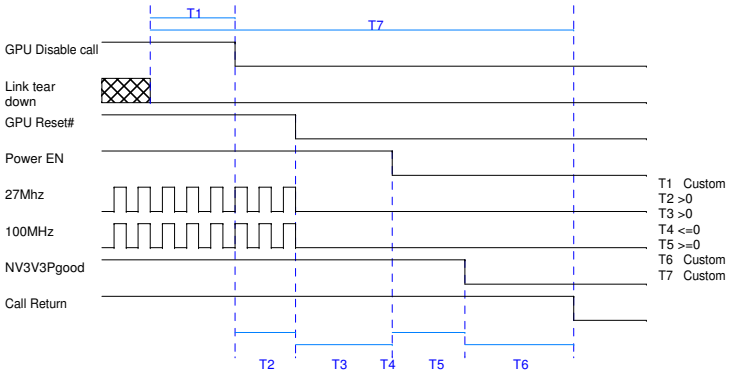
GPU Power Down Sequence



GPU Power Up Sub-system Sequence



GPU Power Down Sub-system Sequence



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Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

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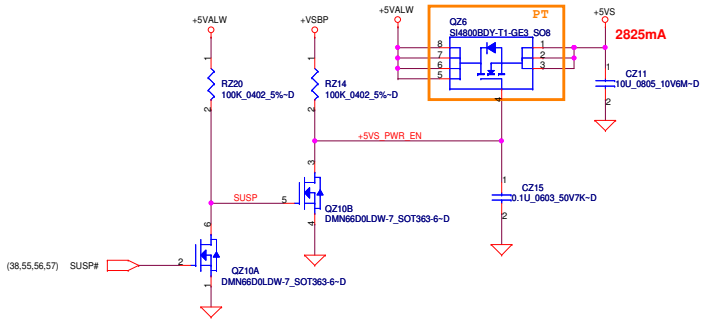
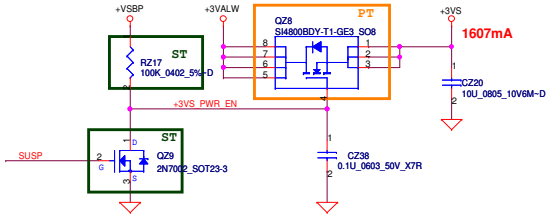
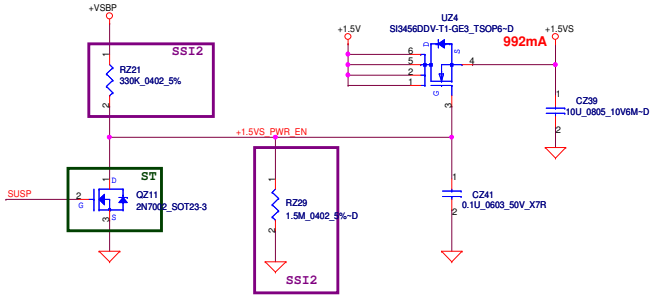
+5VALW to +5VS



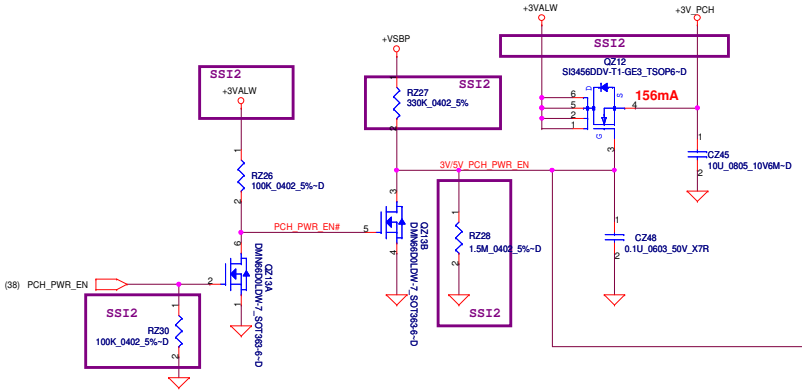
+3VALW to +3VS



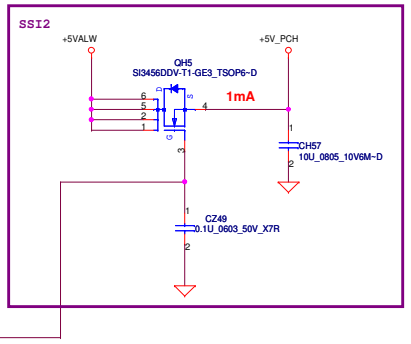
+1.5V To +1.5VS



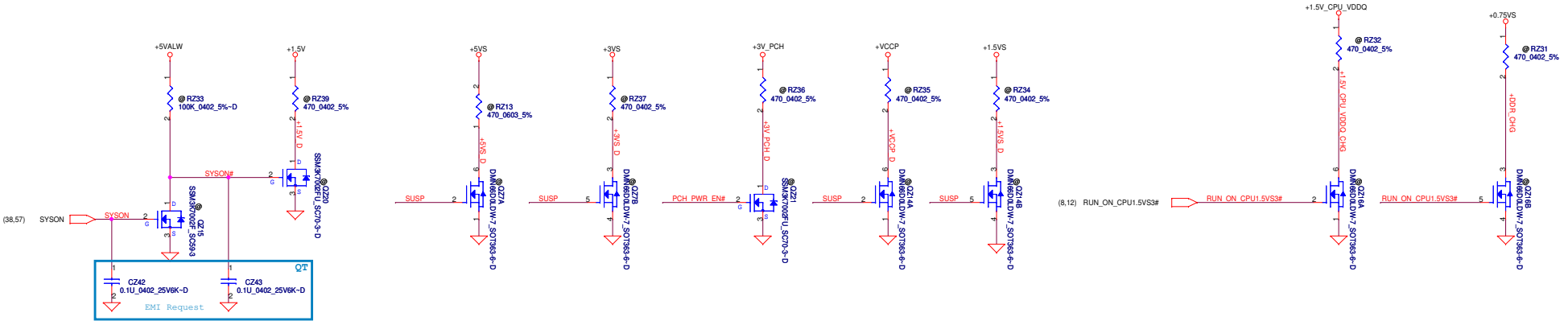
+3VALW to +3V_PCH



+5VALW to +5V_PCH



Discharge



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **DC/DC Interface**

Size	Document Number	Rev
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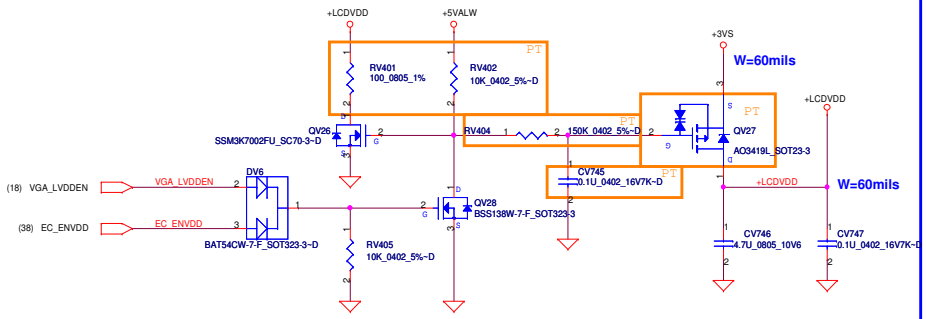
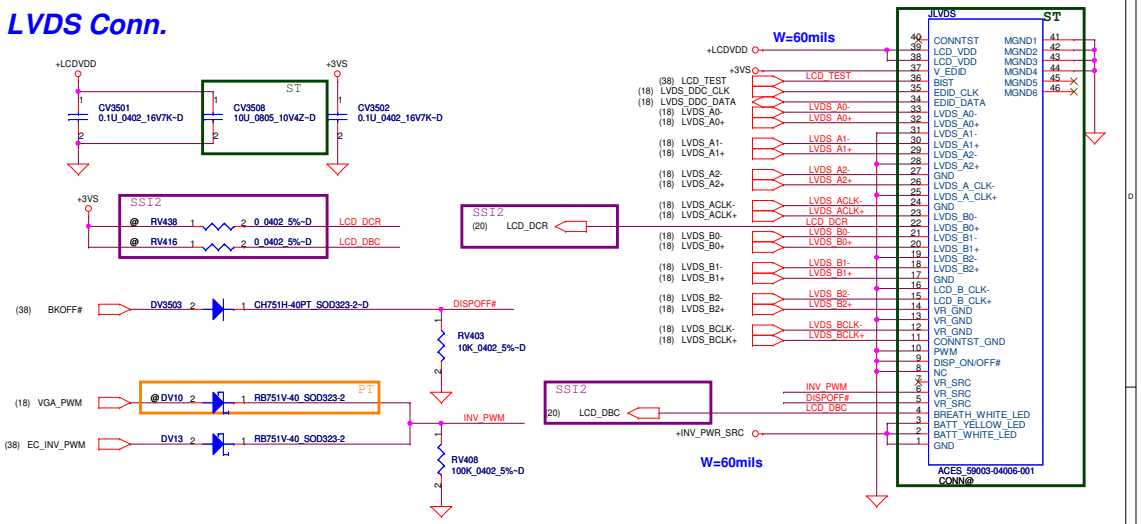
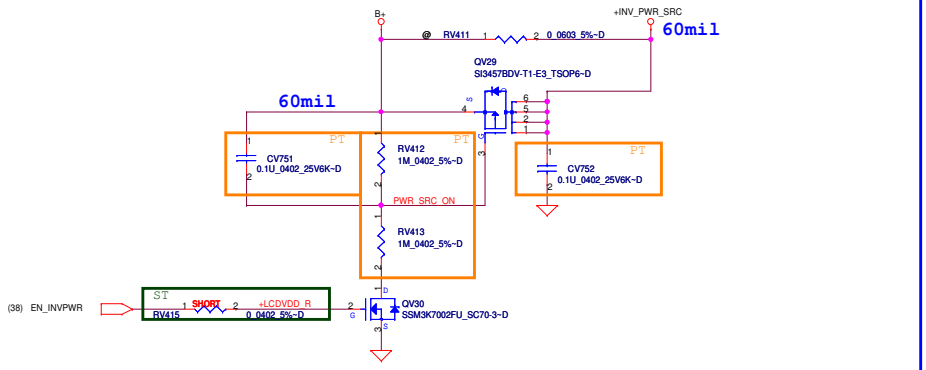
LCD PWR CTRL



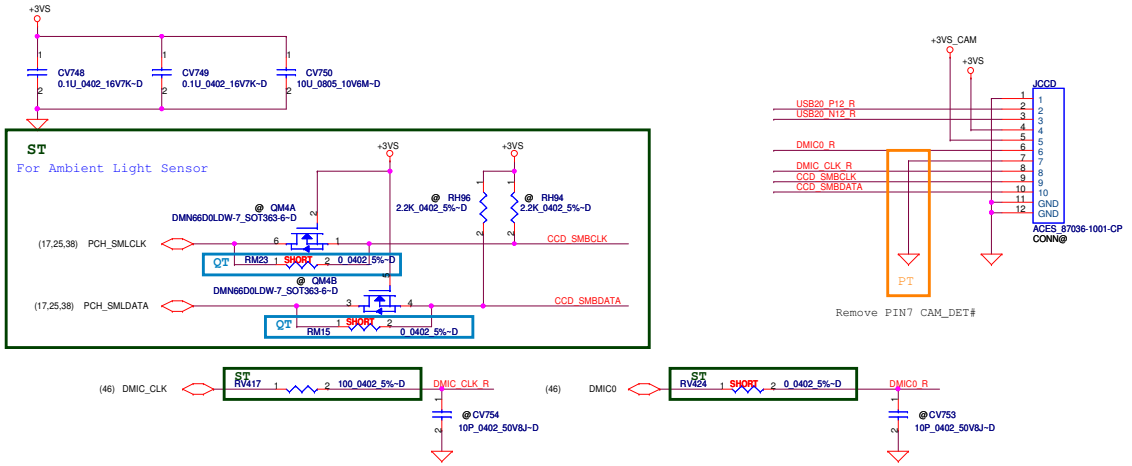
LVDS Conn.



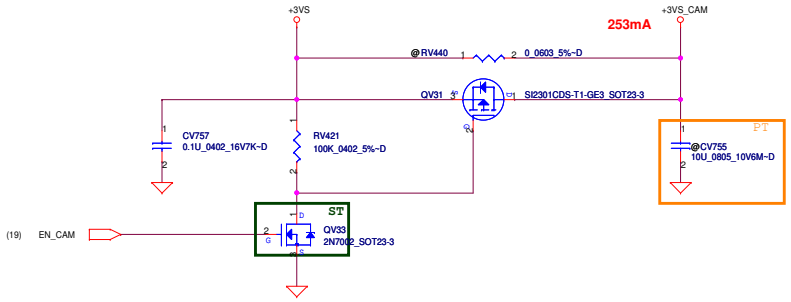
LCD backlight PWR CTRL



CCD Conn.

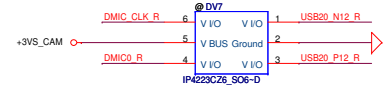


Wedcam PWR CTRL

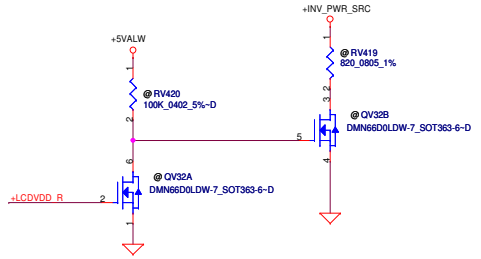


(19) USB20_P12
(19) USB20_N12
@LV11 DLW21SN900SQ2L_0805_4P~D
USB20_P12
USB20_N12
USB20_P12_R
USB20_N12_R
RI27 0_0402_5%~D
RI26 0_0402_5%~D

** Reserved for EMI/ESD/RF need to close to JCCD*



* Reserved for LCD sequence tuning



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **LVDS /camera conn.**

Size	Document Number	Rev
	LA-7851P	0.1

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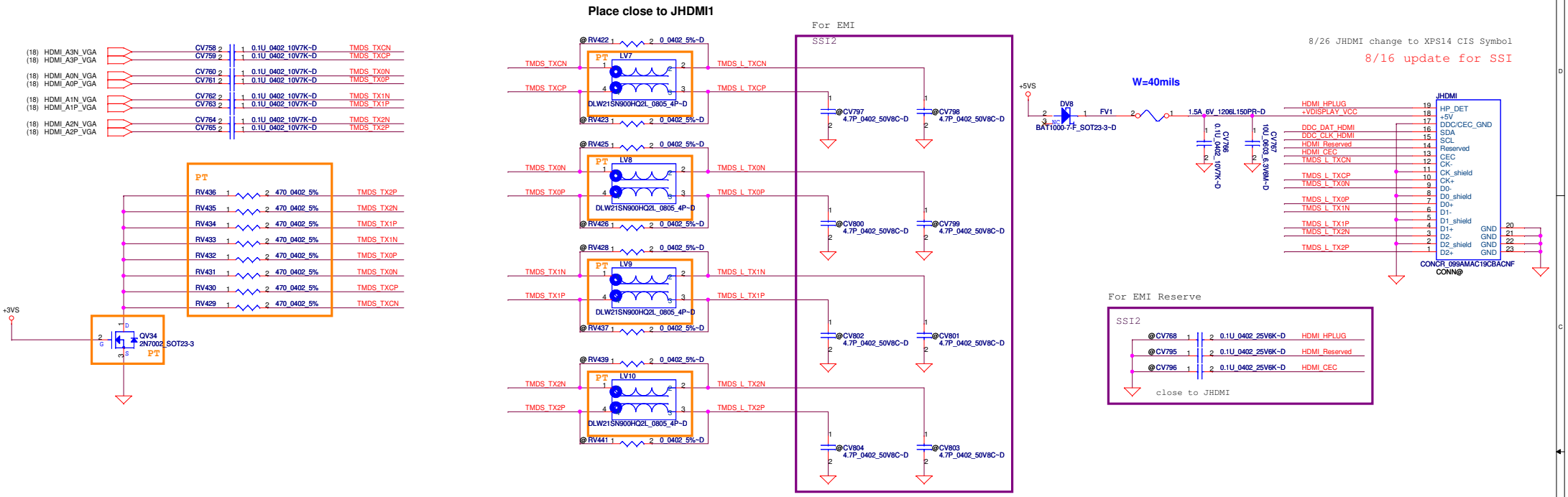
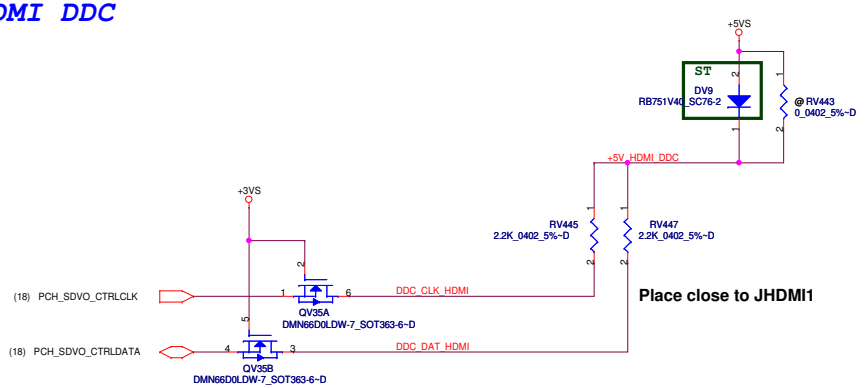
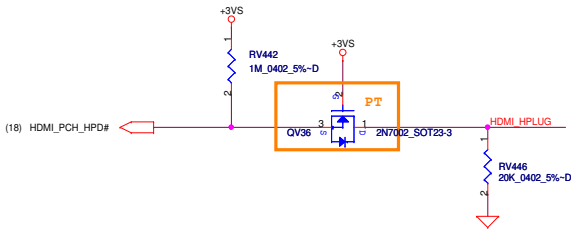
HDMI Cost Reduce type



HDMI DDC



HDMI HPD



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: HDMI

Size: Custom | Document Number: LA-7851P | Rev: 0.1

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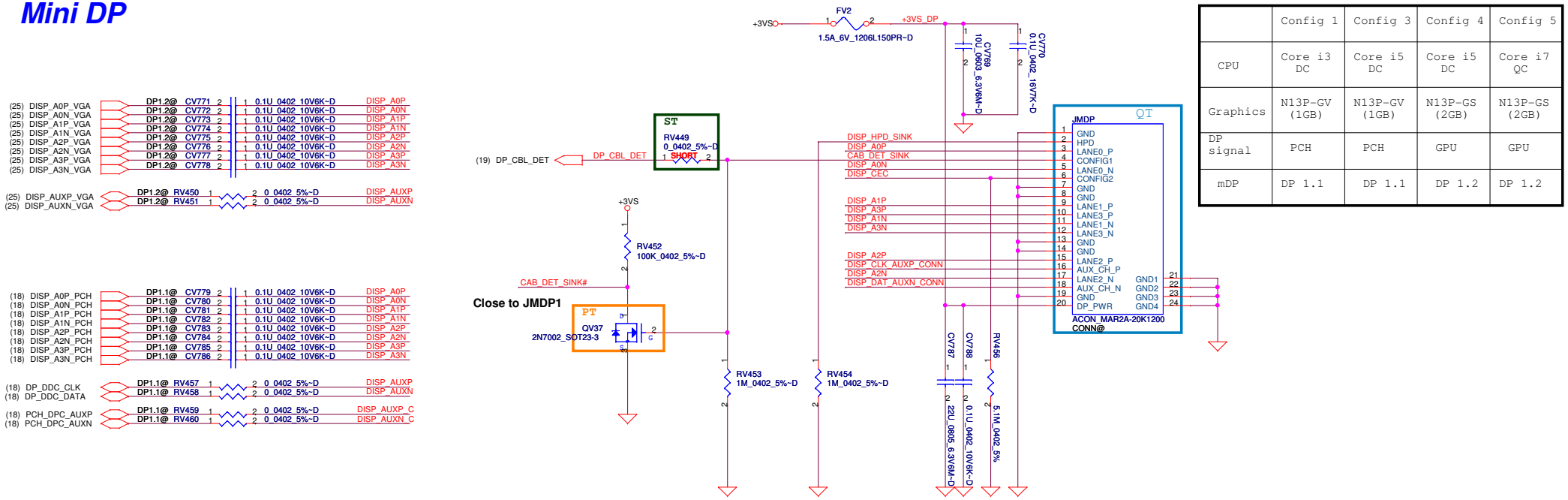
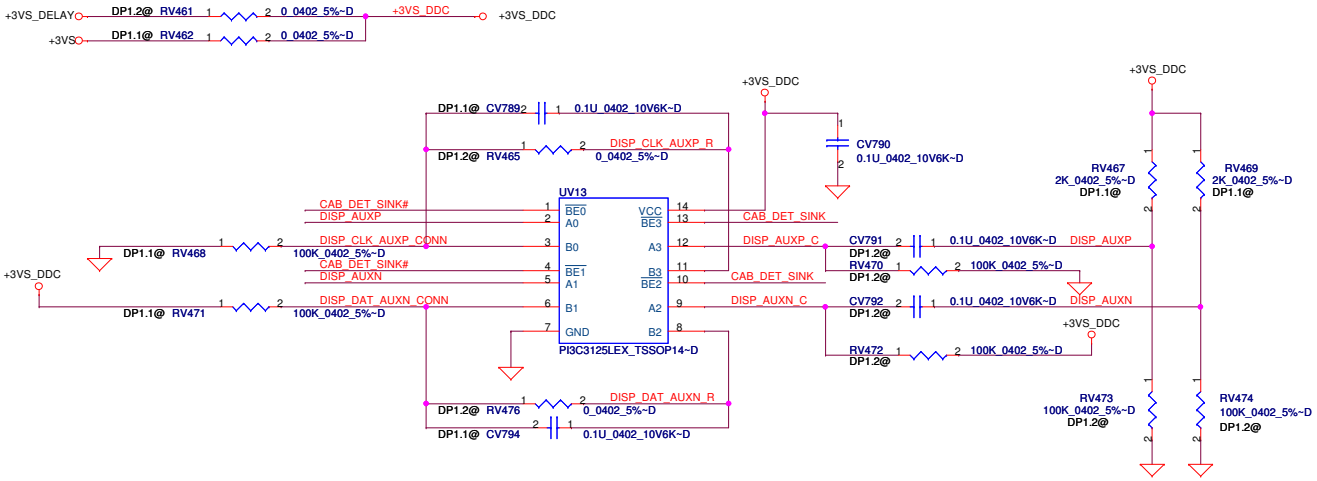
Mini DP



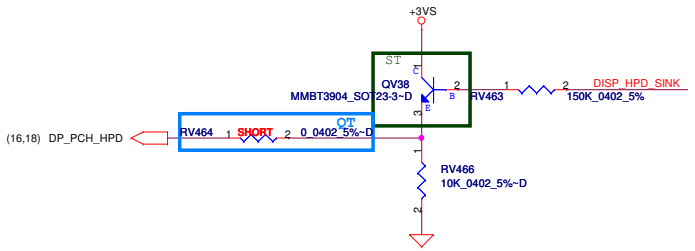
	Config 1	Config 3	Config 4	Config 5
CPU	Core i3 DC	Core i5 DC	Core i5 DC	Core i7 QC
Graphics	N13P-GV (1GB)	N13P-GV (1GB)	N13P-GS (2GB)	N13P-GS (2GB)
DP signal	PCH	PCH	GPU	GPU
mDP	DP 1.1	DP 1.1	DP 1.2	DP 1.2

DDC Dongle SW for DP

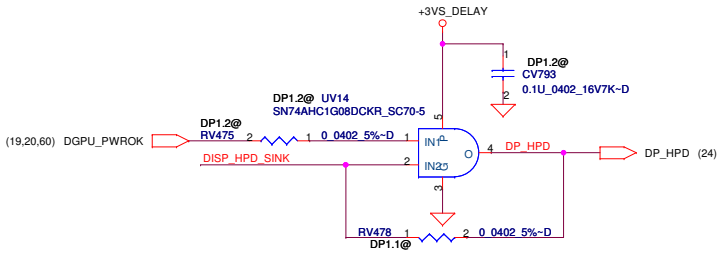


DP1.1A@ --> DP output from iGPU
DP1.2@ --> DP output from dGPU

DP HPD to PCH (iGPU)



DP HPD for DGPU output (Optimus)



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title: Mini DP			
Size: Custom	Document Number: LA-7851P		Rev: 0.1
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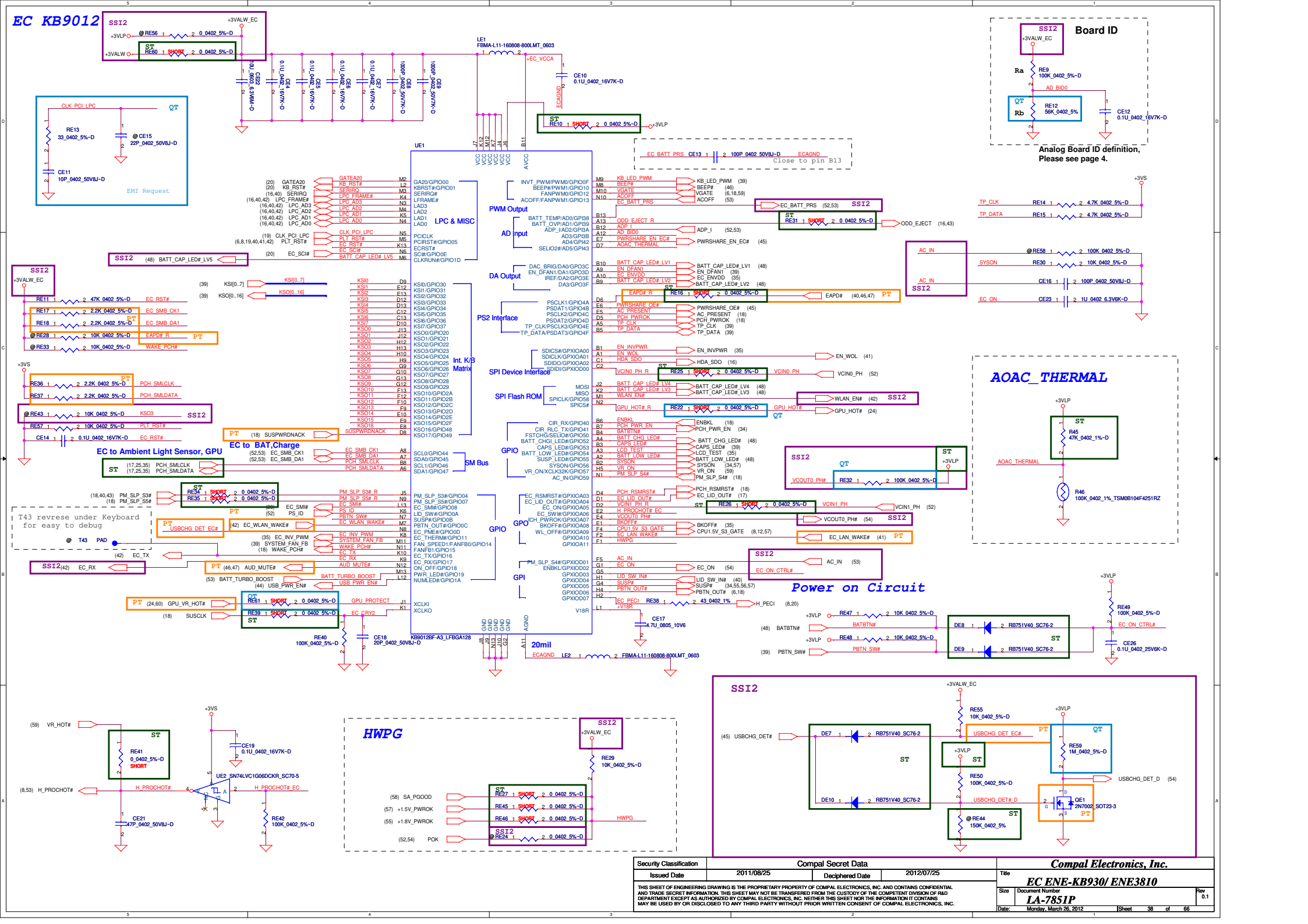
EC KB9012



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Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Compal Electronics, Inc.

Title: EC ENE-KB930/ ENE3810

Size	Document Number	Rev
	LA-7851P	0.1

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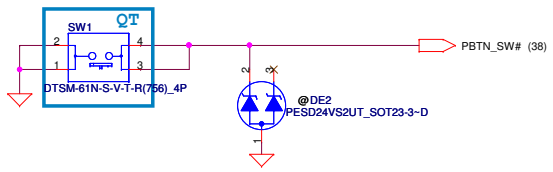
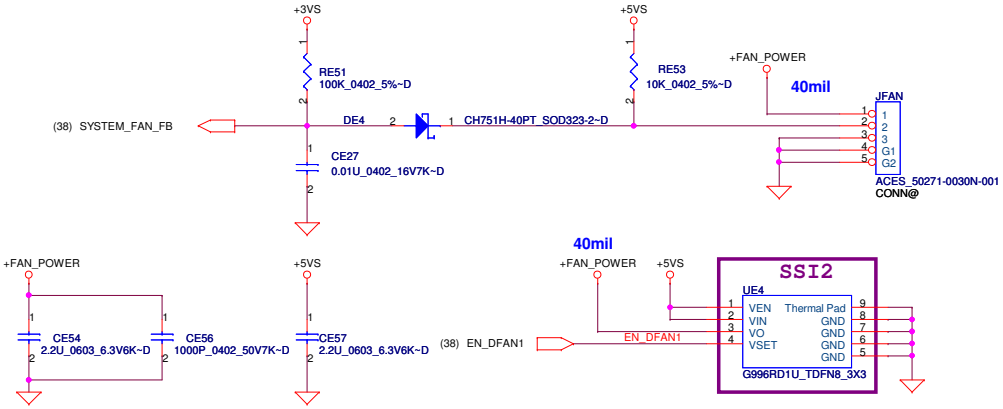
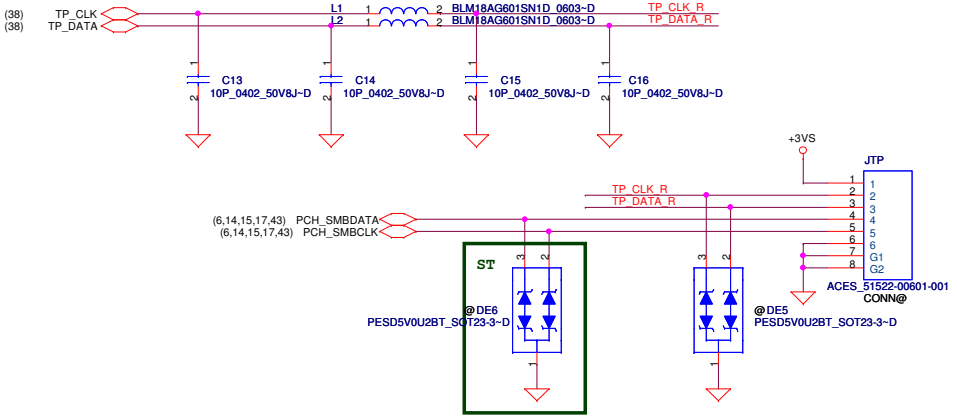
Power on Button



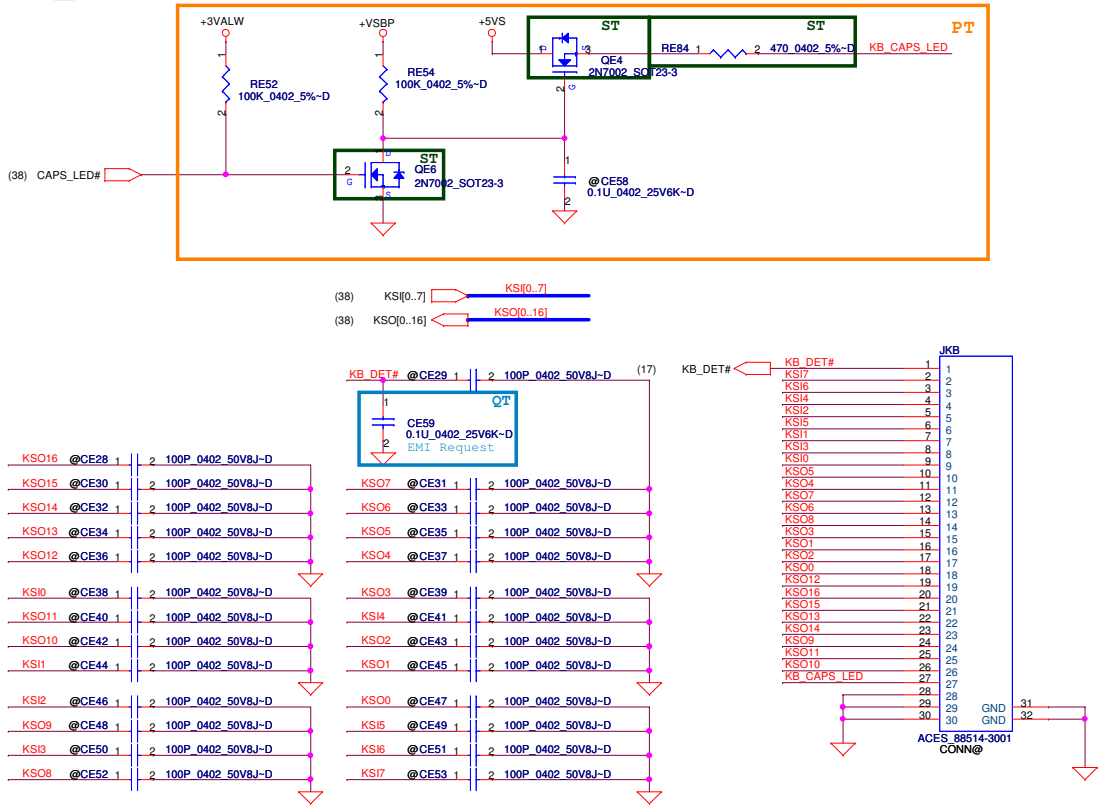
FAN Control



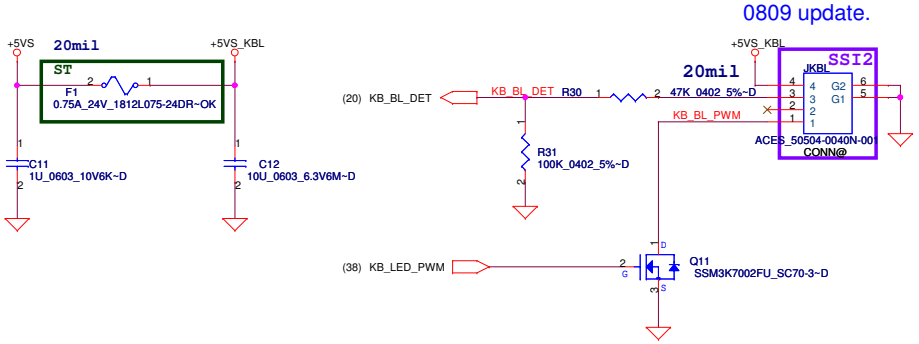
Touch pad



INT_KBD CONN



Keyboard back light



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **SW/TP/SCREW**

Size	Document Number	Rev
Custom	LA-7851P	0.1

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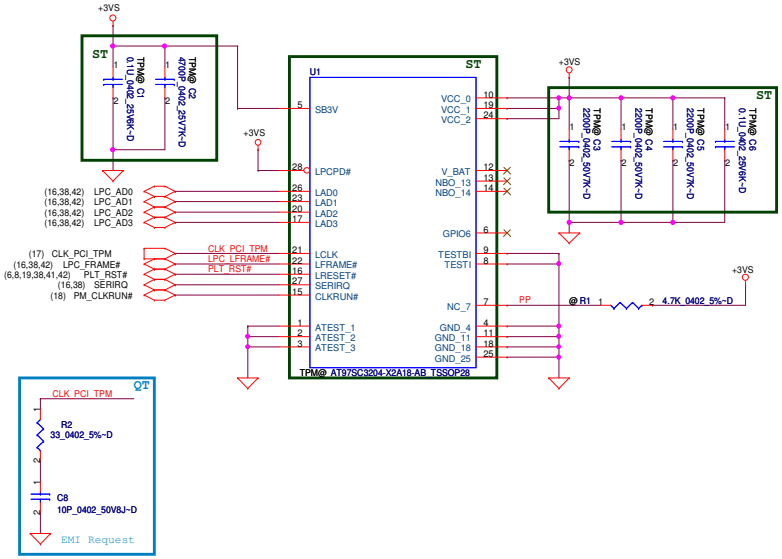
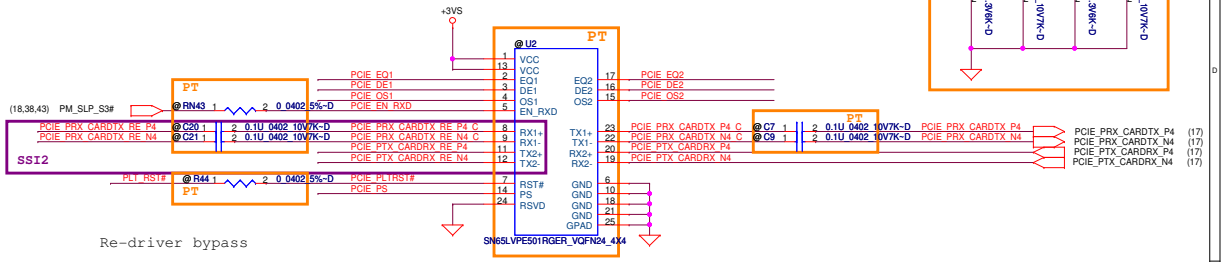
ATMEL TPM



PCIe Re-driver for Cardreader



Signal Control Pin Setting

EN_RXD	DEVICE FUNCTION
0	Set input termination to Z_{OC_RX} and disable Rx. Detect
1	Perform Rx.Detect (default, internally pulled to Vcc)

RST	DEVICE FUNCTION
0	Device in quiescent state and inputs set to Hi-Z
1	Device not in shut_down mode (default, internally pulled to Vcc)

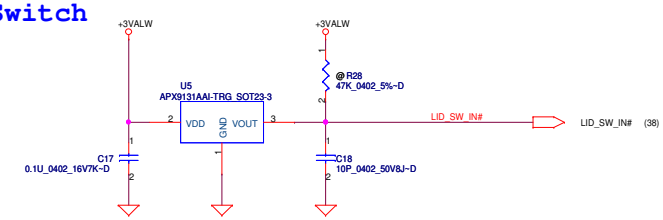
PS	DEVICE FUNCTION
0	Auto-low power mode disabled (default, internally pulled to GND)
1	Auto-low power mode enabled

OSx	*TRANSITION* BIT AMPLITUDE (TYP. mVpp)
NC	1000
0	875
1	1100

DEx[1]	OSx[1] = NC	OSx[1] = 0	OSx[1] = 1
NC	–3.7 dB	–2.5 dB	–4.6 dB
0	–6.4 dB	–5.5 dB	–6.6 dB
1	–9.4 dB	–9.5 dB	–8.7 dB

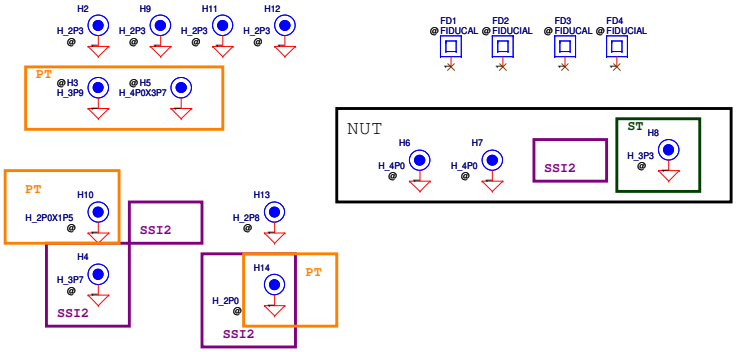
EQx[1]	EQUALIZATION dB (At Gen II Speed)
NC	0
0	7
1	15

Lid Switch

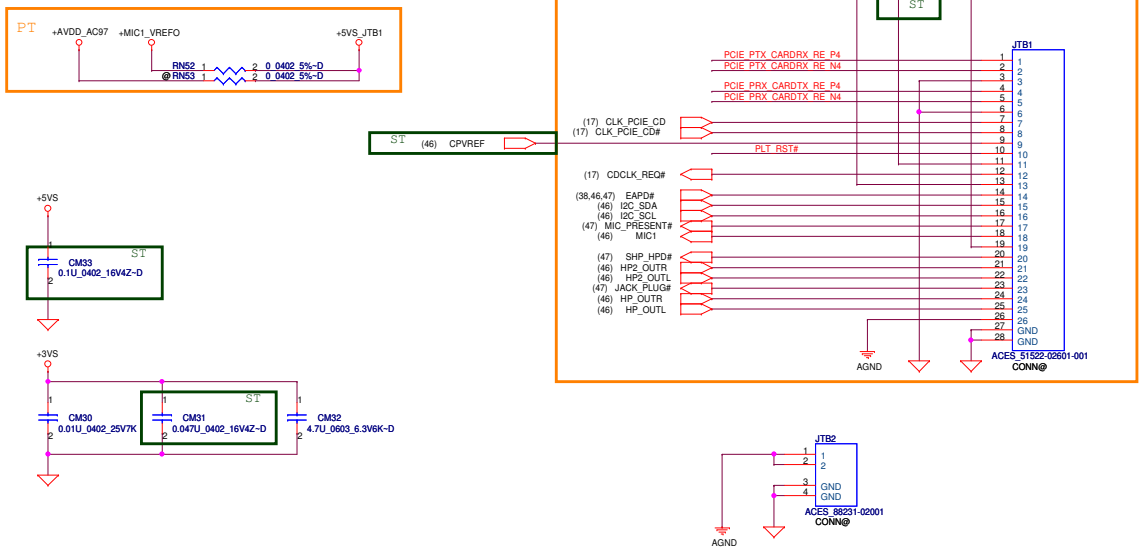


0825
ME request change LID SW PN to SA00003B900

Screw Hole



M/B to D/B conn.



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **CONN & LID**

Size	Document Number	Rev
	LA-7851P	0.1

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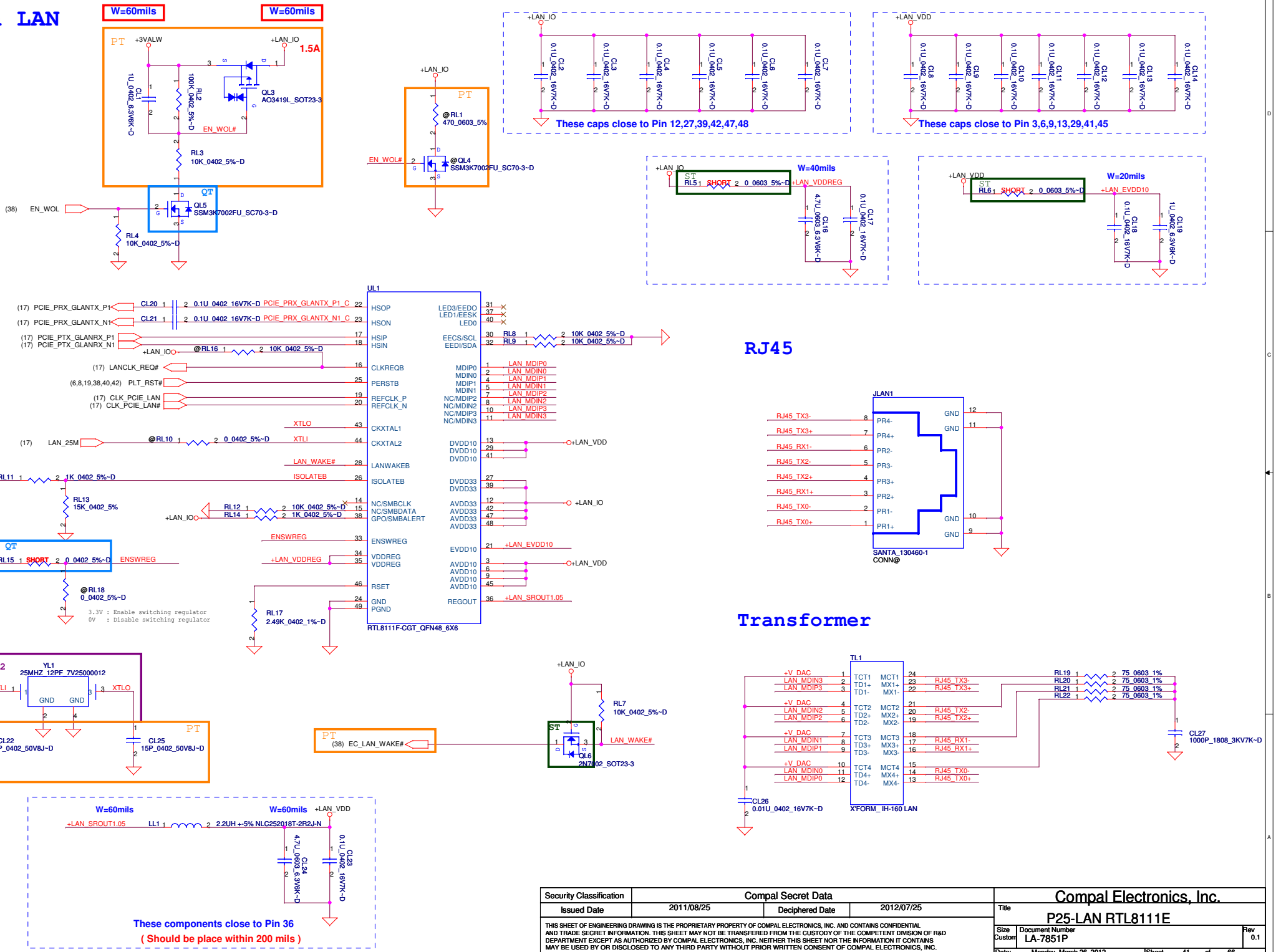
Giga LAN



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

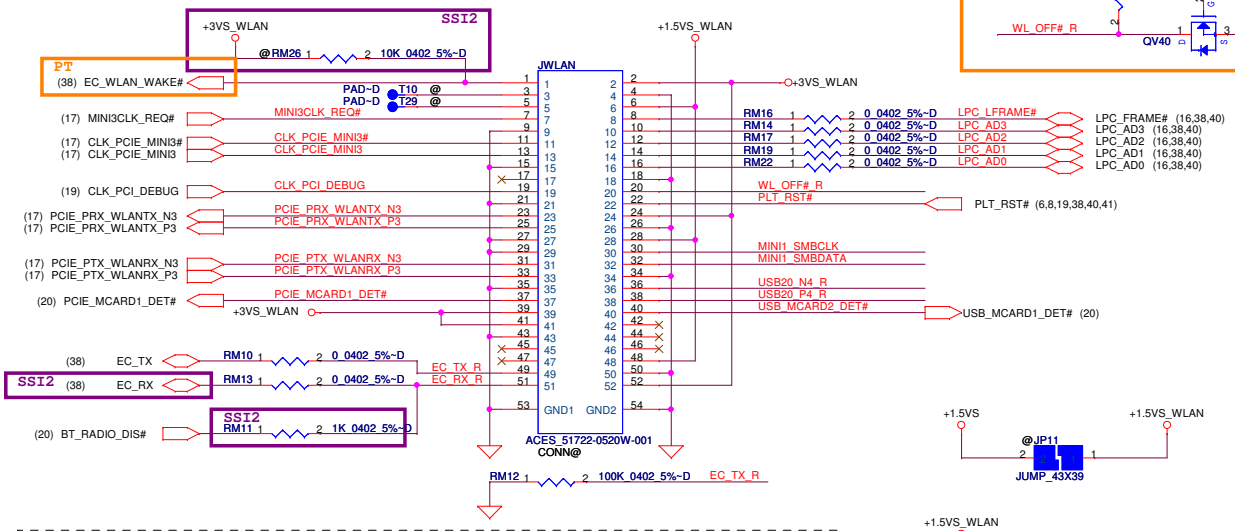
Compal Electronics, Inc.

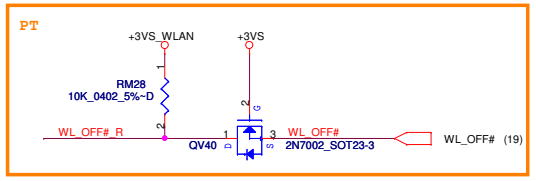
Title: P25-LAN RTL8111E

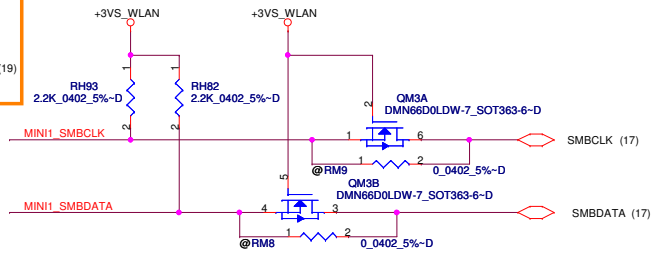
Size	Document Number	Rev
Custom	LA-7851P	0.1

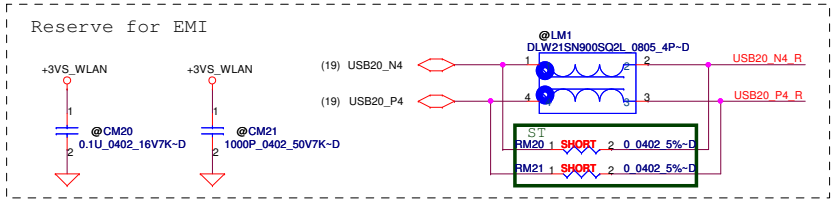
Date: Monday, March 26, 2012 Sheet 41 of 66

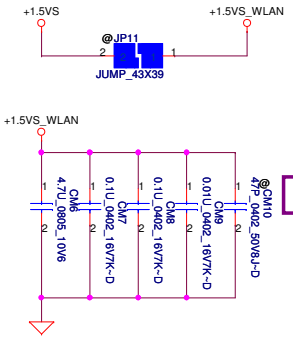
WLAN / BT4.0 PCIE Mini Card



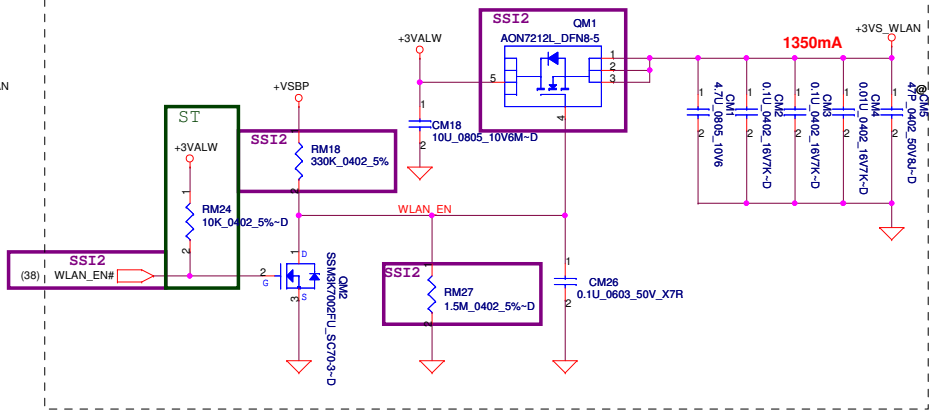






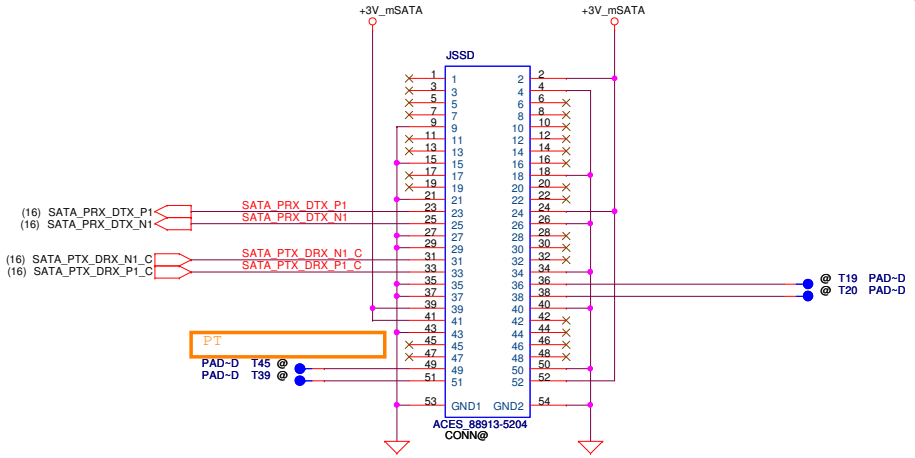


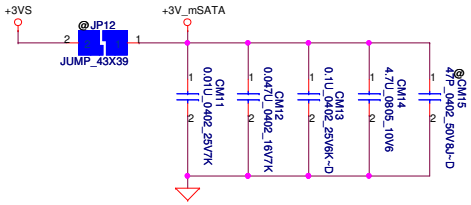
WLAN power control for AOAC



Pin#	Assignment	Description	Pin#	Assignment	Description
1	N/A	N/A	27	GND	Return Current Path
2	+3.3V	3.3V source	28	N/A	N/A
3	N/A	N/A	29	GND	Return Current Path
4	GND	Return Current Path	30	N/A	N/A
5	N/A	N/A	31	-A (port 1)	SATA Differential RX- based on SSD
6	N/A	N/A	32	N/A	N/A
7	N/A	N/A	33	+A (port 1)	SATA Differential RX+ based on SSD
8	N/A	N/A	34	GND	Return Current Path
9	GND	Return Current Path	35	GND	Return Current Path
10	N/A	N/A	36	Reserved	No Connect
11	N/A	N/A	37	GND	Return Current Path
12	N/A	N/A	38	Reserved	No Connect
13	N/A	N/A	39	+3.3V	3.3V Source
14	N/A	N/A	40	GND	Return Current Path
15	GND	Return Current Path	41	+3.3V	3.3V Source
16	N/A	N/A	42	N/A	N/A
17	N/A	N/A	43	N/A	N/A
18	GND	Return Current Path	44	N/A	N/A
19	N/A	N/A	45	Reserved	N/A
20	N/A	N/A	46	N/A	N/A
21	GND	Return Current Path	47	Reserved	N/A
22	N/A	N/A	48	N/A	N/A
23	+B(port 1)	SATA Differential	49	DA/DSS	Device Activity / Disable Staggered Spin-up
24	+3.3V	3.3V Source	50	GND	Return Current Path
25	-B(port 1)	SATA Differential	51	Presence Detection	Shall be pulled to GND by device
26	GND	Return Current Path	52	+3.3V	3.3V Source

mSATA SSD

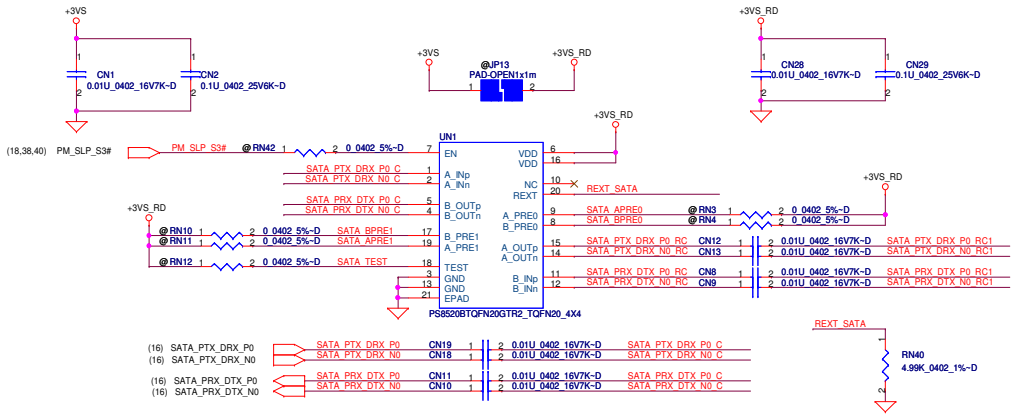




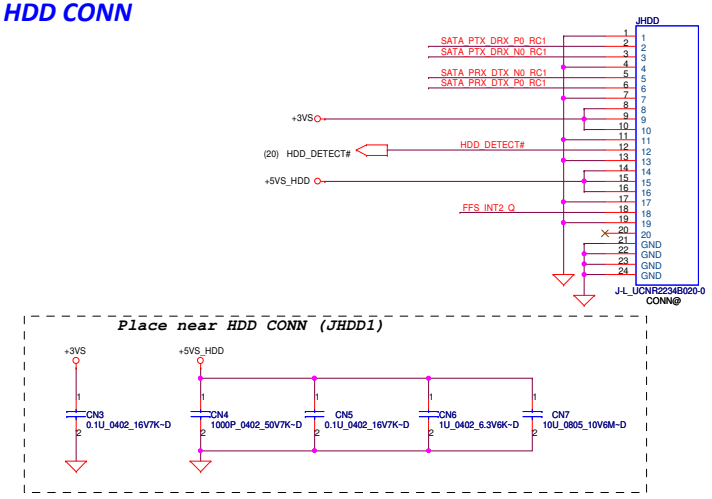
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.	
Title	WLAN/WWAN/SIM/BT
Size: Custom	Document Number: LA-7851P
Rev	0.1
Date: Monday, March 26, 2012	Sheet 42 of 66

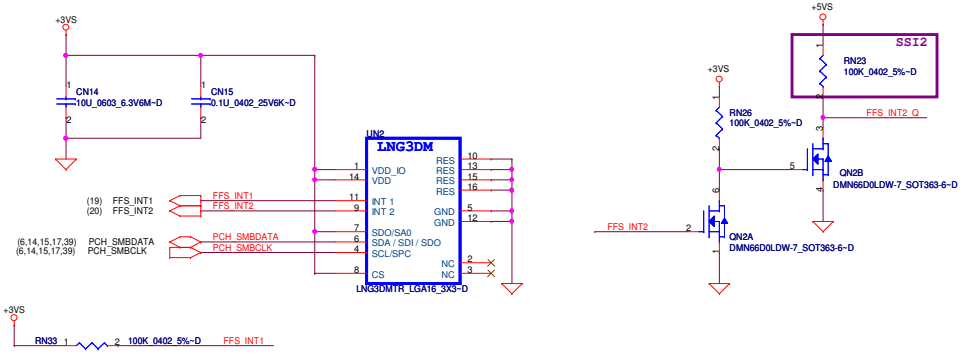
SATA III Re-driver for HDD



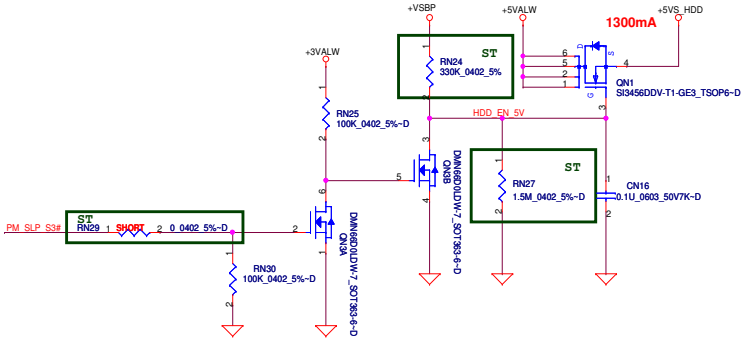
HDD CONN



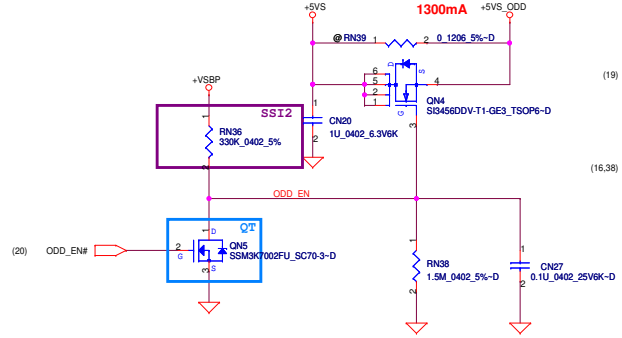
Free Fall Sensor



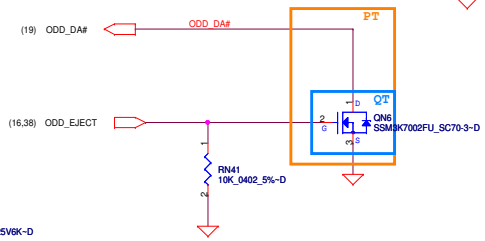
HDD power control for AOAC



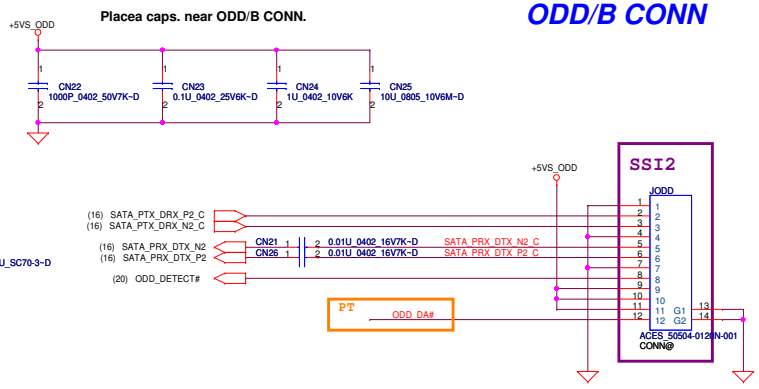
ODD power control



ODD Ejection



ODD/B CONN



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

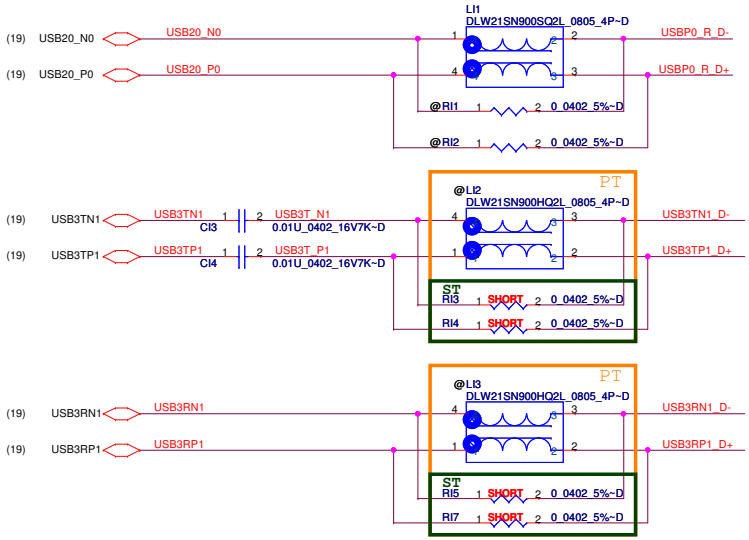
Compal Electronics, Inc.

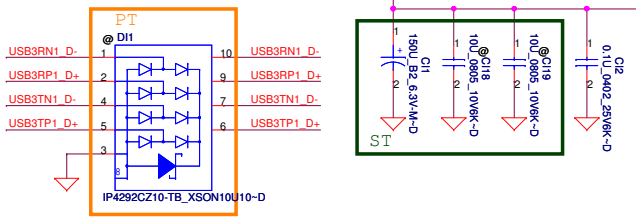
Title: DC/DC INTERFACE

Size	Document Number	Rev
Custom	LA-7851P	0.1

Date: Monday, March 25, 2012 | Sheet 43 of 66

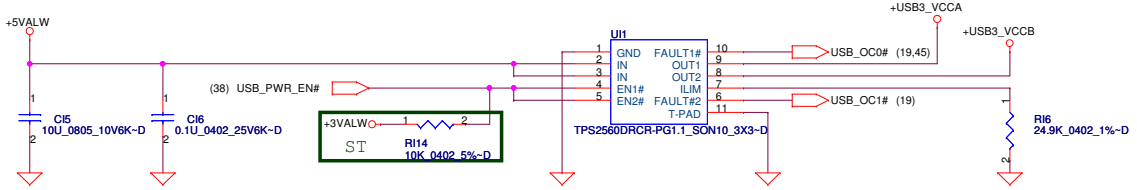
USB3.0 / USB2.0



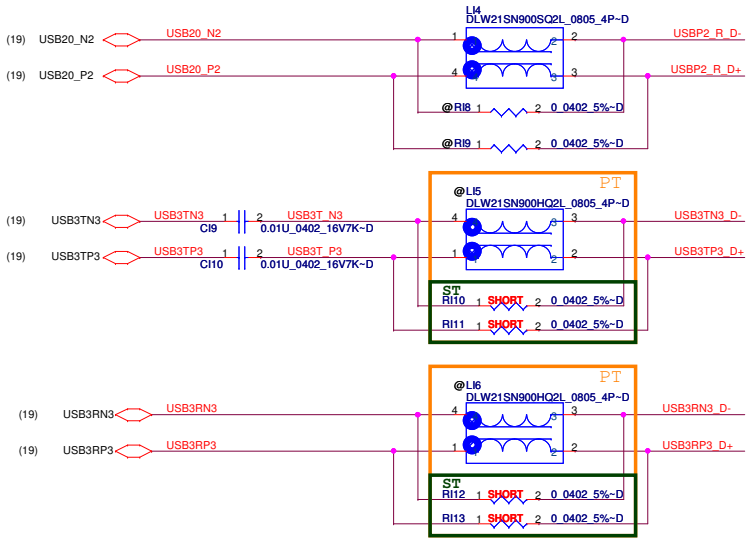


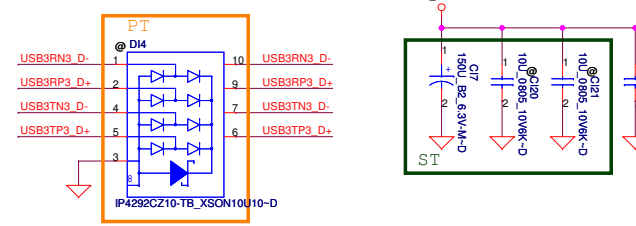
Place close to JUSB1

2.5A / Channel



USB3.0 / USB2.0





Place close to JUSB2

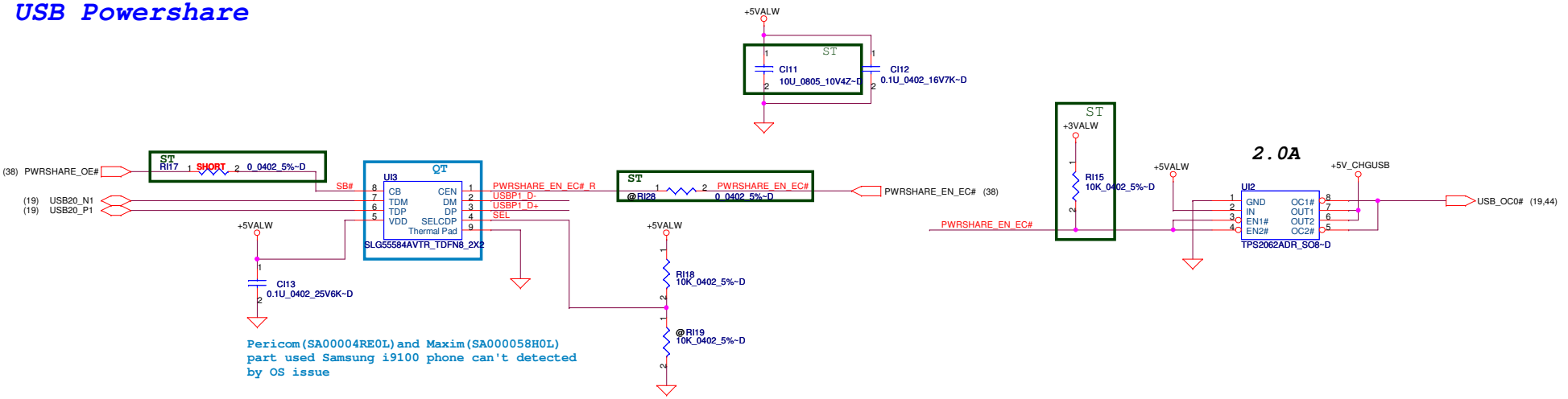
Compal Electronics, Inc.

Title: USB conn.

Size | Document Number: LA-7851P | Rev: 0.1

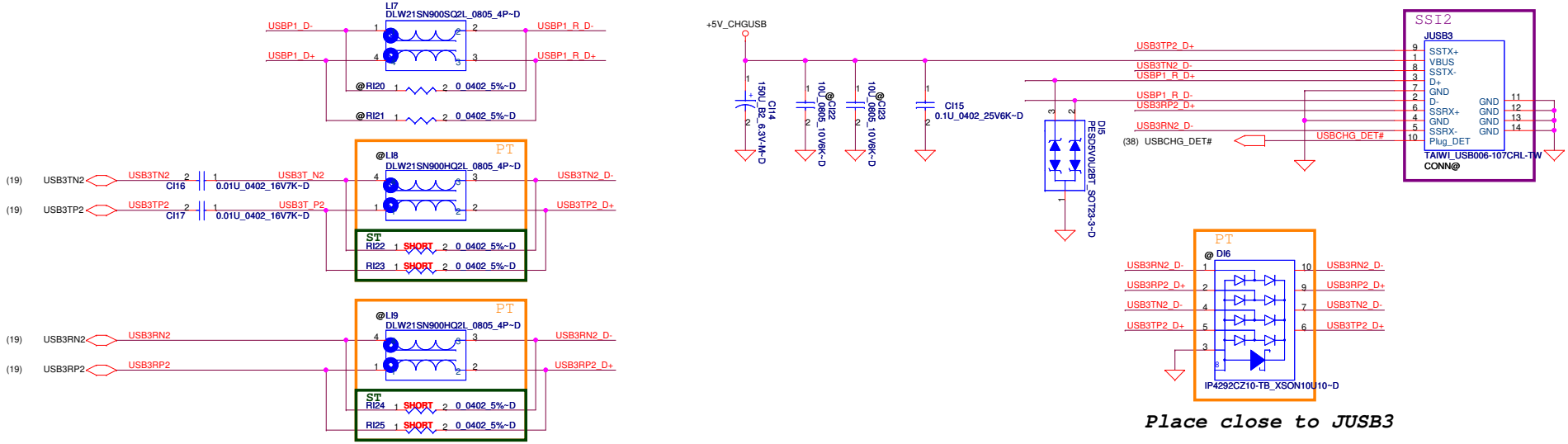
Date: Monday, March 26, 2012 | Sheet 44 of 66

USB Powershare



Pericom(SA00004RE0L)and Maxim(SA000058H0L)
part used Samsung i9100 phone can't detected
by OS issue

USB3.0 / USB2.0



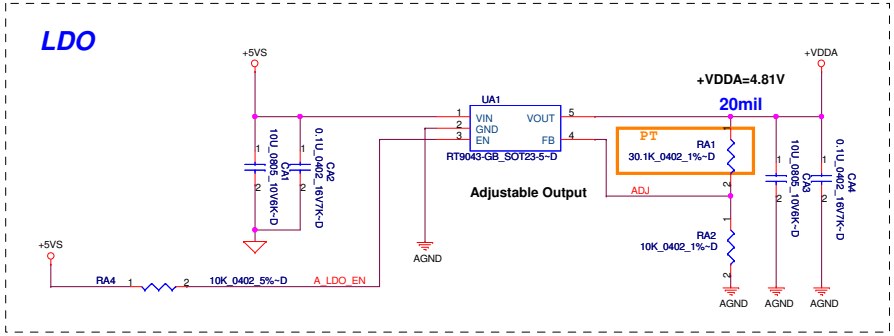
Place close to JUSB3

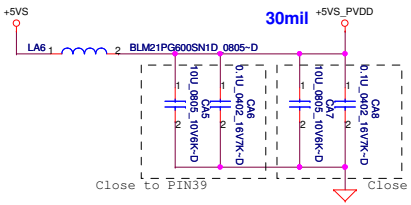
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

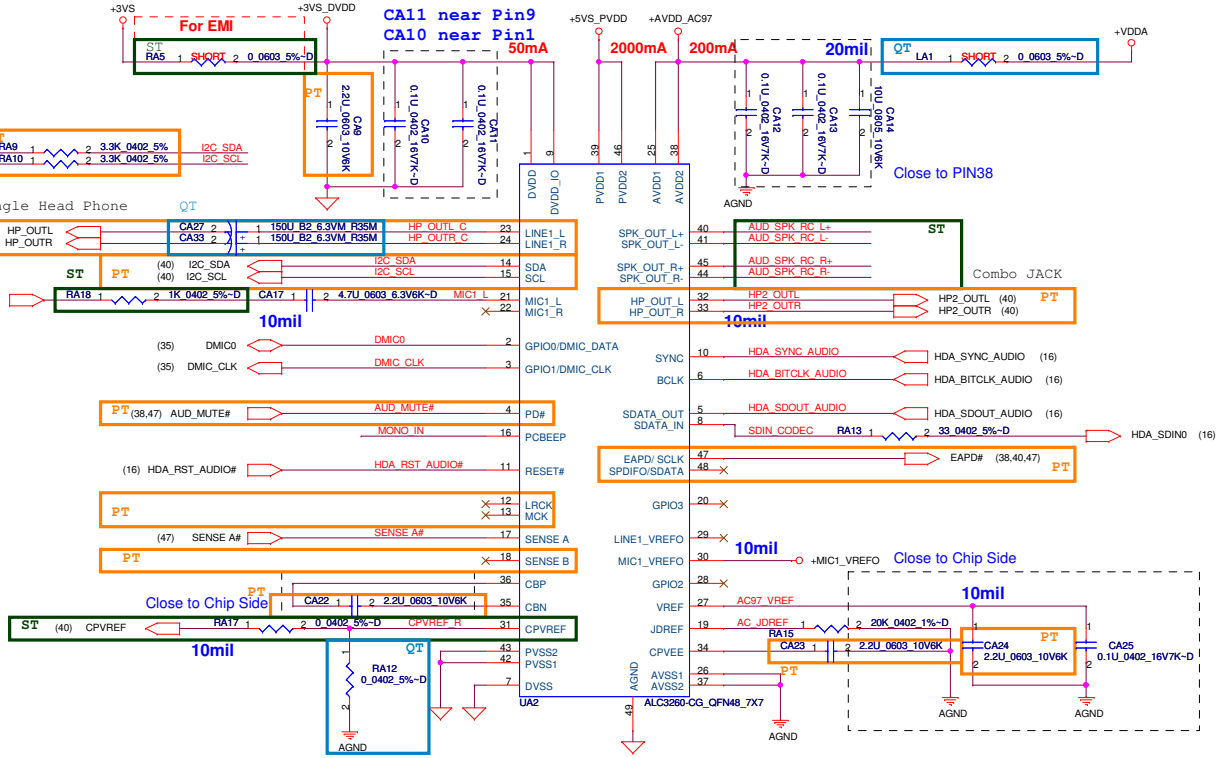
Compal Electronics, Inc.			
Title: USB conn.			
Size	Document Number: LA-7851P		Rev: 0.1
Date: Monday, March 26, 2012		Sheet 45 of 66	

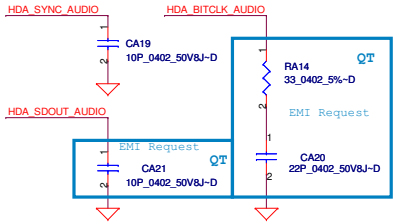
HD Audio Codec

LDO

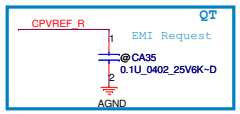






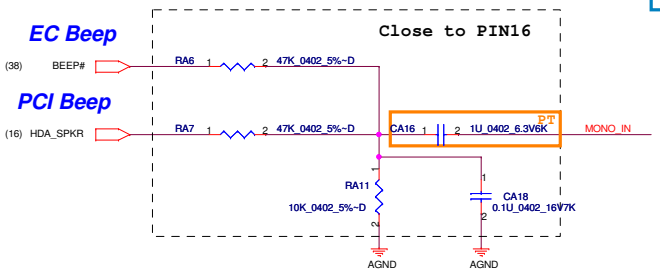


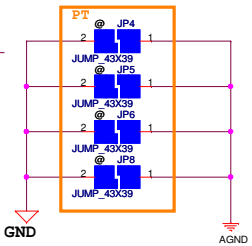
Beep sound

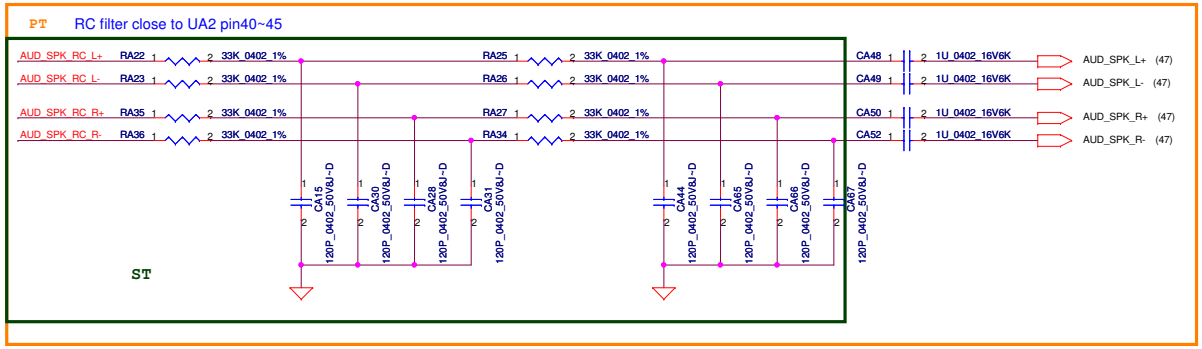


EC Beep

PCI Beep







Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **HD Audio ALC275/Audio Jack**

Size: Custom | Document Number | Rev

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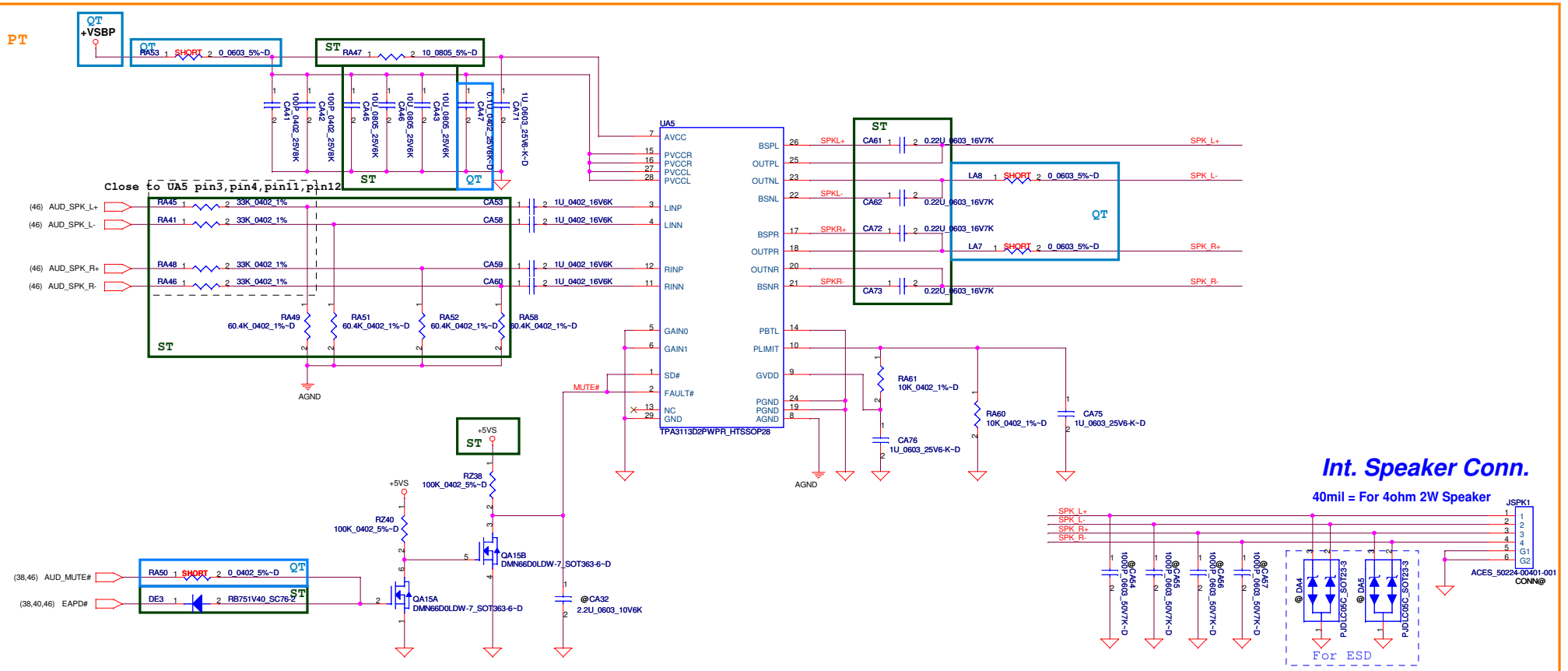
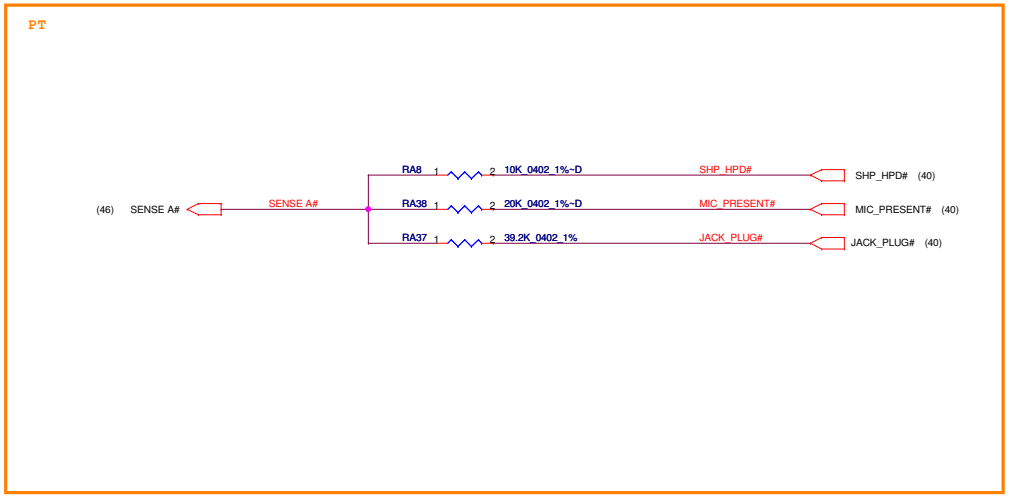
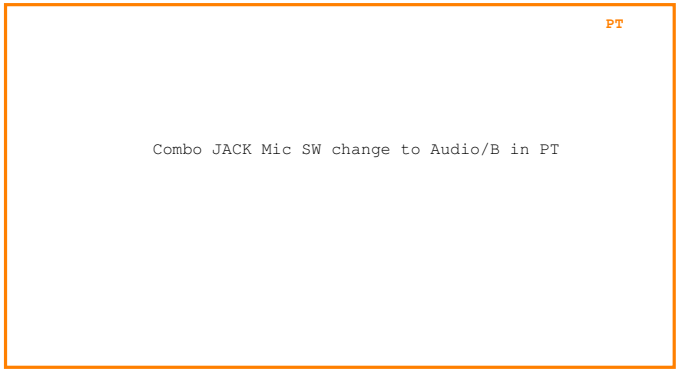
Audio AMP



SENSE PIN



Combo JACK Mic SW



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/21

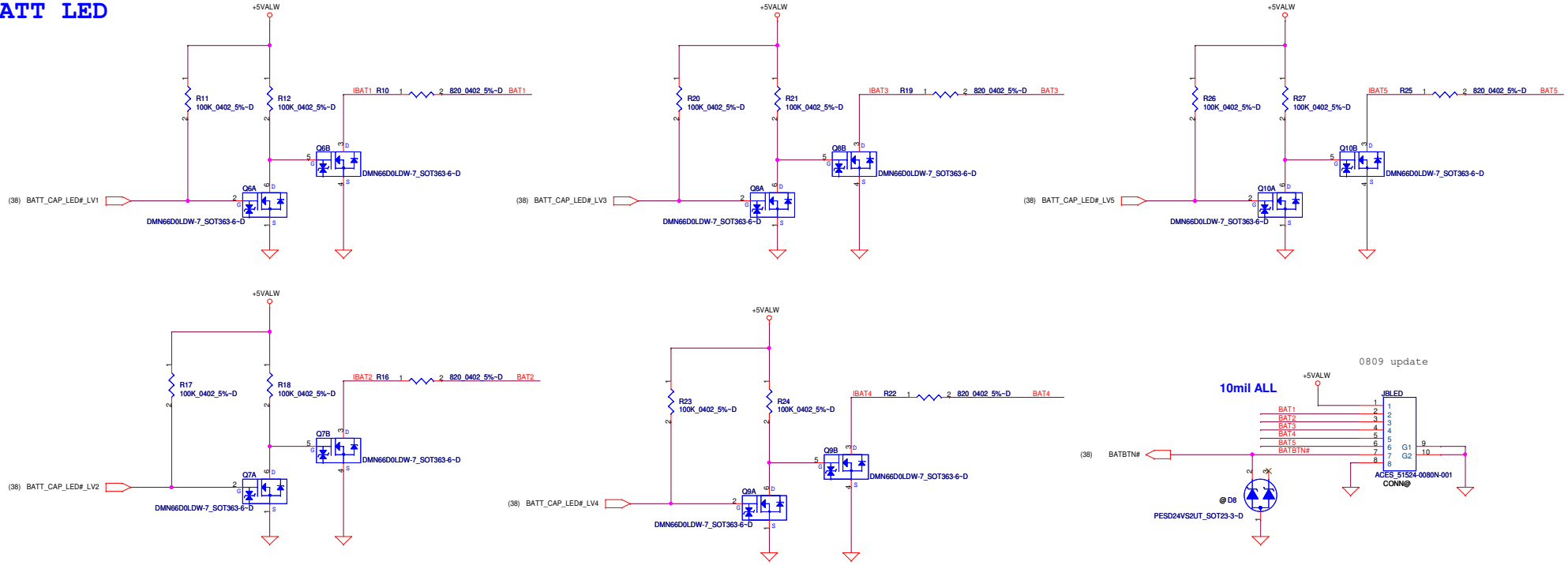
Compal Electronics, Inc.

Title: Speaker/Audio Jack

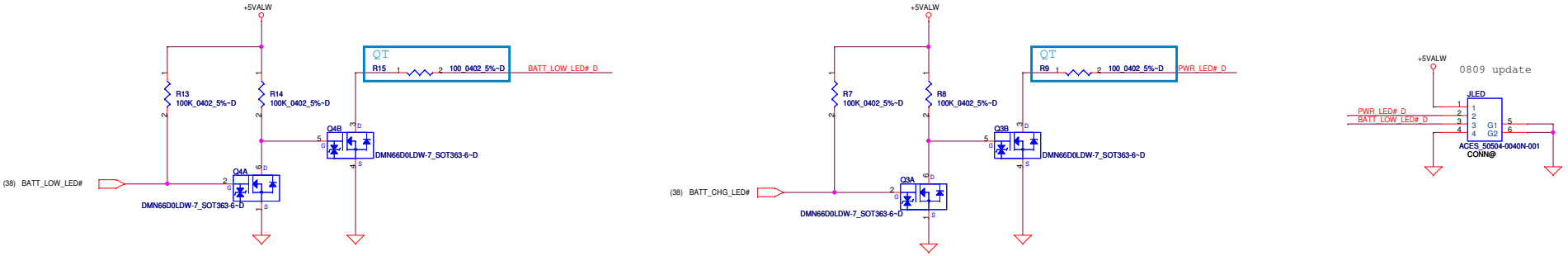
Size	Document Number	Rev
Custom	LA-7851P	0.1

Date: Monday, March 26, 2012 Sheet 47 of 66

BATT LED



Charge LED



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: Speaker/Audio Jack

Size	Document Number	Rev
C	LA-7841P	0.1

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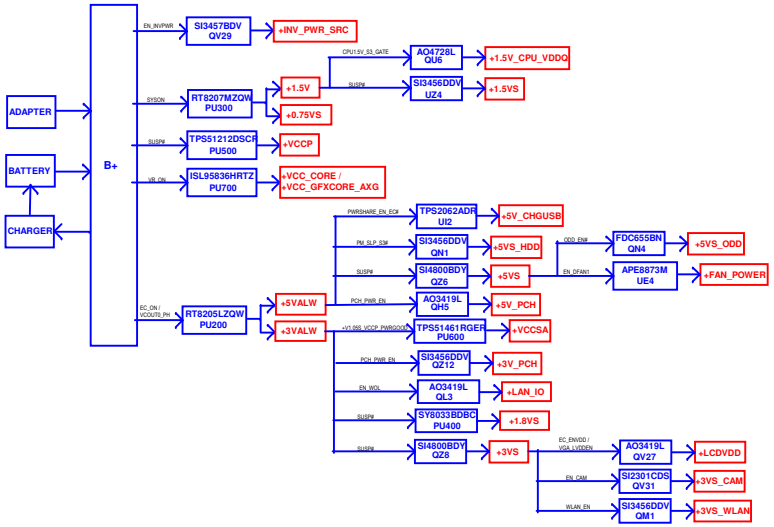
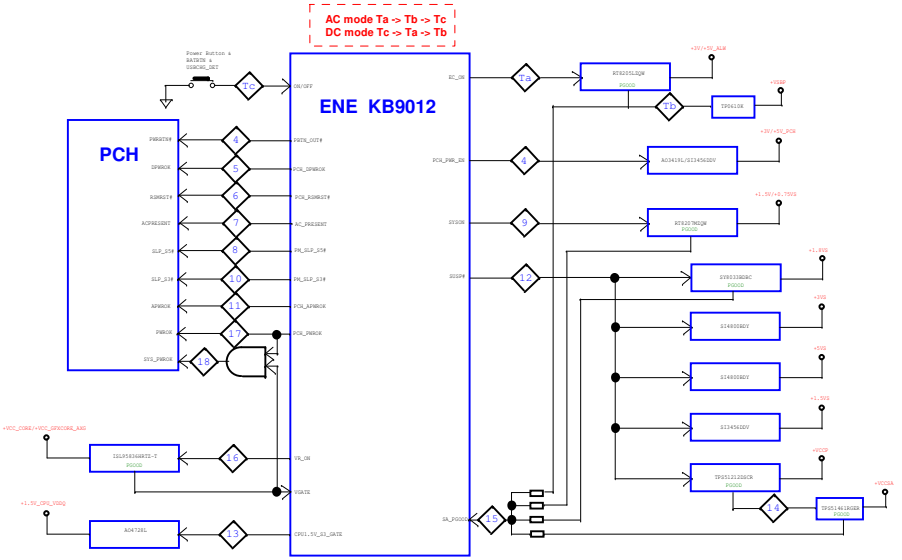
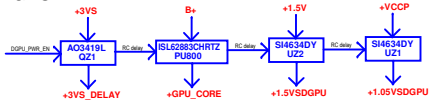
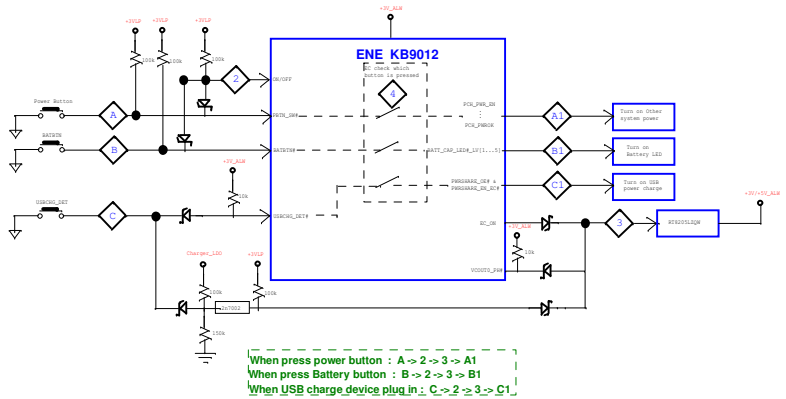




GPU





Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: Power Sequence

Size | Document Number | Rev 0.1

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EE change note for QBL00 Main Board

Item	Page	Title	Date	Issue Description	Solution Description	Rev.	BOM	Layout	Note
1	41	Transformer 1000P CAP	2011/8/29	PN upload BOM error	Change PN form SE120102K8L to SE120102K3L	0.1	V		BOM Change
2	46	Codec +5VS Bead	2011/8/29	PN upload BOM error	Change PN form SM010017800 to SM01001788L	0.1	V		BOM Change
3	47	Combo JACK Mic SW chip change to MB	2011/8/29		Add UA4	0.2		V	
4	40	IO Board pin define	2011/8/29		Modify JTB1 pin define for MB add Combo JACK SW cheip	0.2		V	
5	51-62	Update Power circuit	2011/8/29		Update Power circuit for QC & DC type	0.2		V	
6	38	EC_KB9012	2011/8/30	AC_STATUS	Modify DE7, DE10 and add AC_STATUS PD	0.2		V	
7	42	MINI CARD connector	2011/8/30	For AOAC function	Add DM1, RM24 and reserve RM25(PLT_RST#)	0.2		V	
8	42	EC_WLAN_WAKE	2011/8/30	For WLAN wake up function	Reserve RM26 PU +3V_WLAN	0.2		V	
9	39	JKBL CONN	2011/8/30	JKBL pin define reserve	JKBL pin define reserve (Pin1 PWM)	0.2		V	
10	47	Audio AMP 10uF CAP	2011/8/31	PJM suggestion change PN	Change PN form SE00000QKL0 to SE00000QK0L	0.1	V		BOM Change
11	39	FAN Control IC	2011/9/1	CIS symbol PN error	Change UE4 PN from SA000035G00 to SA00002W800	0.2		V	
12	47	AMP IC package	2011/9/1	Change package type	Change UA4 from BGA to QFN type	0.2		V	
13	47	AMP SPKR Bead	2011/9/1		Change PN from SM01000BP00 to SM01000BP0L	0.1	V		
14	38	EC_KB9012	2011/9/2	ODD_EJECT netname	Change GPI39 netname from ODD_EJECT to ODD_EJECT_R	0.2		V	
15	38	Power on Circuit	2011/9/2	USBCHG_DET# pin	Add QE1 on USBCHG_DET# signal	0.2		V	
16	43	Change JODD CONN	2011/9/4		Change PN from SP01000E400 to SP01001BF10	0.2		V	
17	38	Update EC GPIO table Rev.10	2011/9/4		Remove PCH_DPWROK(Pin D8) and Change pin name from PCIE_WAKE#(Pin29) to WAKE_PCH# Change pin name from EC_EAPD# to AMP_MUTE# Change pin name from AC_STATUS to AC_IN Change pin name from ACIN to EC_ON_CTRL1 Change pin name from ON/OFF# to EC_ON_CTRL2#	0.2		V	
18	38	EC_KB9012	2011/9/6	Reserve +3VLP	Reserve RE56	0.2		V	
19	38	Power on Circuit	2011/9/6	USBCHG_DET# pin	Remove AC_IN pin and change to control VL signal	0.2		V	
20	51-62	Update Power circuit	2011/9/6		Update Power circuit for QC & DC type	0.2		V	
21	35, 42	DC to DC Interface & WLAN power	2011/9/7	De-rating VGS issue	Add Z28, RZ29, RM27	0.2		V	
22	38	EC_KB9012	2011/9/7	Board ID Rb setting	Change RE12 to 8.2K	0.2	V		BOM Change
23	24, 59	NV P8I Function	2011/9/8		Add GPU_GPIO3, GPU_GPIO16 PU 10K and reserve 0 ohm to GPU CORE H_DPRSLPVR	0.2		V	
24	12	CPU VCCDQ power	2011/9/8	Intel suggestion	Add RU89	0.2		V	
25	38, 41	EN_WOL#	2011/9/9	Correct netname	Change Netname from EN_WOL to EN_WOL#	0.2		V	
26	38, 42	WLAN_EN#	2011/9/9	Correct netname	Change Netname from WLAN_EN to WLAN_EN#	0.2		V	
27	47	Combo Jack Mic SW circuit	2011/9/9	vendor suggestion	Change JACK_PLUG PU from +5VS to +3VS and add 10uF to GND ADDR_SEL add RA55 to GND Add RA56, RA57 reserve for I2C_SCL, I2C_SDA and add RA21, RA22 PU 10K for I2C_SCL_JACK_SW, I2C_SDA_JACK_SW	0.2		V	
28	43	Free Fall Sensor Pin11	2011/9/9	HDD pin 11 to be PU via internal PU	Mount RN23	0.2	V		BOM Change
29	16	2M SPI ROM	2011/9/9		Delete 2M SPI ROM circuit	0.2		V	
30	37, 44, 45	CONN Change	2011/9/14	CONN Change	Change JMDP PN to SP011109061 Change JUSB1, JUSB2 to SP011109062 Change JUSB3 to SP011109063	0.2		V	
31	38	EC_KB9012	2011/9/14	KSO3 PD	Reserve RE43 for SSI rework item	0.2		V	
32	47	AMP	2011/9/14	AMP issue	Reserve RA12, RA29 for SSI rework item	0.2		V	
33	18, 38	PCH_DPWROK	2011/9/14		Add PCH_DPWROK for detect the ME request global reset	0.2		V	
34	24~32	GPU BOM Config	2011/9/14		Add GPU BOM Config	0.2	V		BOM Change
35	51~62	Update Power circuit	2011/9/19		Update Power circuit for DC type	0.2		V	
36	46	Layout footprint issue	2011/9/20	footprint issue	Change LA1 to SM01000BX0L	0.2		V	
37	40	PCIE Re-driver	2011/9/20	Redrive TX/RX swap	Swap U2 pin8/pin9 to pin11/pin12	0.2		V	
38	41	Update Power circuit	2011/9/21		Update power circuit for DC & QC type	0.2			
39	63	Add power on timing page	2011/9/21		Add page 63 power on timing	0.2			
40	38	Power on Sequence	2011/9/21	POK power sequence timing	Reserve RE24, mount PR910	0.2		V	
41	42	Debug card active	2011/9/21	EC_RX debug	Change RM11 to 1K	0.2	V		BOM Change
42	40	Screw	2011/9/21		Delete H16, H17	0.2		V	
43	40	Screw	2011/9/22		Add H14 and change H3, H4, H5 footprint	0.2		V	
44	51~62	Update Power circuit	2011/9/22		Update power circuit for DC & QC type	0.2		V	
45	20, 35	LCD DBC and CE behaviro	2011/9/24		Change RH177, RH182 PD and reserve RV416, RV438 for LCD DBC, CE behaviro	0.2		V	
46	22,34	Back drive issue	2011/9/26	3V/5V PCH back drive issue	Delete JP4, add RZ230, CZ49 and change QH5 PN to SB53456003L, CH57 PN to SE064106M1L	0.2		V	
47	51~62	Update Power circuit	2011/9/26		Update power circuit for DC & QC type	0.2		V	
48	38	Update EC GPIO table Rev.11	2011/9/26	Update EC_GPIO table Rev.11	Change pin name from EC_ON_CTRL2 to EC_ON_CTRL# Change pin name from EC_ON_CTRL1 to AC_IN Change pin name from BATT_TEMP to EC_BATT_PRS Change pin name from EC_GPIO1D to BATT_CAP_LED#_LV5 Change pin name from BATT_CAP_LED#_LV5 to EC_RX Remove PCH_DPWROK pin Add GPU_PROTECT pin	0.2		V	
49	47	AMP and Combo JACK SW	2011/9/26	AMP issue	Remove AMP circuit and reserve Combo JACK bypass circuit	0.2		V	
50	8	Back drive issue	2011/9/27	3V/5V PCH back drive issue	Change PM_DRAM_PWRGD PU to +3V_PCH	0.2		V	
51	46,47	Audio FAE review	2011/9/28		Change CA17 to 4.7U, resserve RA43, RA44 for I2C_LRCK, I2C_MCK, reserve RA29 for EAPD Add RA12 PD and reserve RA39, QE5 for JACK_PLUG, change RA53 to 47K and reserve CA27 for SHP_HPD	0.2		V	
52	42	WLAN power control for AOAC	2011/9/28	WLAN_EN can't control the 3VS_W	Change QM1 PN to SB00000NR00 and RM18 to 330K, RM27 to 2M	0.2		V	
53	42	MINI CARD connector	2011/9/28	For AOAC function	Remove RM24, DM1, RM25	0.2		V	
54	36	EMI	2011/9/28	EMI solution for HDMI issue	Reserve CV768, CV795, CV796, CV797, CV798, CV799, CV800, CV801, CV802, CV803, CV804	0.2		V	
55	38	ERP lot6 implementation	2011/9/28		Change EC 3VALW power rail to 3VALW_EC	0.2		V	
56	16, 17, 24, 41	Crystal change design for package size	2011/9/28		Change YH1, YH2, YV1, YL1 footprint	0.2		V	

Item	Page	Title	Date	Issue Description	Solution Description	Cause Category	Note	Rev.	BOM	Layout
1	18	SSI2 Power on issue	2011/10/23	PCH_DPWORK BOM error	Add RH101	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
2	37	Change Part PN	2011/10/23		Change QV37 PN to SB000006A00	Others				V
3	18, 38	SUSPWRDNACK signal	2011/10/23		SUSPWRDNACK signal from EC to PCH for ME reset function	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
4	35	MIC issue	2011/10/23	MIC record has background noise	Change JCCD pin7 to GND, remove CAM_DET pin and remove RH95, reserve CV755	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
5	38	Modify netname	2011/10/23	Modify netname	USBCHG_DET_EC#, GPU_VR_HOT#, EAPD#	Others		0.3		V
6	10	Sandy Bridge CPU PEG*8	2011/10/24	Sandy CPU MB GPU can't detect	Add RU85 for Sandy bridge sku	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
7	47	Amp circuit	2011/10/24	AMP	Add TI AMP 3113 circuit	Design issue--Improper circuit design	不適當的線路設計	0.3		V
8	47	Combo Jack SW	2011/10/24	Combo Jack SW no function	Change JACK_PLUG to SENSE A#, SHP_HPD to SENSE B#	Design issue--Improper circuit design	不適當的線路設計	0.3		V
9	40,43	PCIE Re-driver IC reserve bypass circuit	2011/10/25		Add RN44~RN51 for PCIE re-driver	Cost down		0.3		V
10	40,47	Combo Jack Ssw	2011/10/25		Change Combo Jack SW circuit to Audio/B and modify JTB pin define	Others		0.3		V
11	33	GPU power on sequence	2011/10/25	3V_DELAY Power SW circuit	Change QZ1 from P-MOS to N-MOS	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
12	33	dGPU timing tuning	2011/10/25	dGPU timing tuning	Change CH99 from 0.1u to 0.01u, delete RZ2, QZ3, RZ7, RZ9, QZ4, DZ1, RZ12 and reserve CZ3,	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
13	18	Intel workshop add SLP_A# test point	2011/11/25		Add SLP_A# test point	Design issue--Check list coverage inadequate		0.3		V
14	46	Sourcer suggestion to change part	2011/10/30		Change UA16 footprint to 0402 and PN to SE000000K80	Cost down		0.3		V
15	46~47	Reltek review schematic suggestion	2011/10/30		HP1 & HP2 Jack exchange port, change RA22,RA23,RA25,RA26,RA35,RA36,RA27,RA34 to 137K1%, change CA15,CA30,CA28,CA31,CA44,CA65,CA66,CA67 to 30PF, change RA45,RA41,RA48,RA46 to 56K 1%, reserve RA49,RA51,RA52,RA58,CA32, change RA8 to	Vendor design issue	基于零件設計問題，要求設計變更	0.3		V
16	40	Reserve PCIE re-driver circuit	2011/10/30		Reserve U2,C20,C21,C22,C23,C24,C25,R441	Cost down		0.3	V	
17	37	Change Part PN	2011/11/1		Change QV38 PN SB3904008L to SB000006A00	Others		0.3	V	
18	52~64	Update power schematic	2011/11/1		Update power schematic	Others		0.3		V
19	39	Change Part PN	2011/11/1		Change SW1 PN SN100002M00 to SN100002M10	Others		0.3	V	
20	8	Change Part PN	2011/11/1		Change UU3 PN SA00003Y000 to SA00003Y00L for buyer suggestion	Others		0.3	V	
21	34,47,8, 16,14	Change Part PN for non-HF part	2011/11/1		Change UZ1, UZ2 PN to SB00000DA10, change QD1, QD2, QH1, QU3 PN to SB501380050 Change UZ6,UZ8 PN to SB548000320, change QE1, QV34, QV36, QV37, QV39 PN to SB000008J00, change CA9, CA22, CA23, CA24 PN to SE000003H00, change LH4, LH6, LH7, LH8 PN to SHI00008S0L	Others		0.3		V
22	38		2011/11/1	S3 Back drive issue	Change RE36,RE37 PU to +3VALW_EC for S3 back drive	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
23	21		2011/11/2	S3 Back drive issue	Change QH3 PU to +3V_PCH	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
24	40	JTB1 Pin define	2011/11/4		Modify JTB1 pin define for add AGND pin	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
25	38	Change PU reistor	2011/11/4		Change RE17,RE18,RE36,RE37 to 2.2K for EC checklist	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
26	39		2011/11/4	CAP_LED always on issue	Add RE84, delete RE53 and reserve CE58,CE50	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
27	42		2011/11/4		Add RM28, QV40 for AOAC WLAN_Radio_On/Off# implementation	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
28	38		2011/11/4		Change RE12 to 18K for EC Board ID	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
29	35		2011/11/6	Panel screen flash or brightness no	Reserve DV10	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
30	35		2011/11/6		Reserve CV755 for +3V_CAM	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
31	41		2011/11/6		Reserve RL1 & QL4	Cost down		0.3	V	
32	8	Update CIS symbol	2011/11/6		Update UU2 CIS symbol	Others		0.3		V
33	38		2011/11/7		Reserve RE16 and change to AUDIO control to AMP	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
34	35	LVDS Timing Tuning	2011/11/7		Change RV401 to 22 ohm, RV412,RV413 to 1M and CV751 to 0.1u and change CV752 to 0402	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
35	16		2011/11/7		Add RH95 for divide ODD_EJECT signal control by PCH & EC	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
36	17,41		2011/11/8		Mount RH102, RL10, reserve YL1, CL22, CL25 for use PCH 25M to LAN chip	Cost down		0.3	V	
37	17		2011/11/8		Change CH27, CH28, CL22, CL25 to 15P and CV575, CV576 change to 10P for vendor	Others		0.3	V	V
38	44		2011/11/10		Reserve CI1, CI7 and add CI18,CI19,CI20,CI21 for JUSB1,JUSB2, reserve CI22, CI23 for JUSB3	Cost down		0.3		V
39	33	dGPU timing tuning	2011/11/10		RZ8 change to 40.2K, RZ41 change to 150K, mount RZ6, RZ10, RZ11, RZ15, QZ15, QZ17 and change to 22 ohm, RZ5 change to 47K, RZ44 change to 20K	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
40	39		2011/11/10	CAP_LED always on issue	Add RE52,QE6,QE7,RE84 delete CE59	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
41	40	ME NUT	2011/11/10		Change H3, H5 footprint	ME/SA request design change	其他設計單位要求的設計變更	0.3		V
42	19		2011/11/10	Back drive issue	Change UH4 power rail to +3V_DELAY	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
43	40		2011/11/11		JTB1 pin define change	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
44	35		2011/11/11		Change RV401 to 100 ohm 0805 package	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
45	37		2011/11/13	Mdp Dongle issue	Change JMDP to footprint	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
46	16,38	ODD_Ejection	2011/11/14		Reserve RH95 and mount RE31 for EC control ODD EJECT, change QN5 to singal package	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
47	25	GPU DID strap pin	2011/11/14		Change RV302, RV306, RV307, RV308, RV309, RV311, RV312, RV313, RC314, RV315, RV316 to 10K.	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
48	40		2011/11/14		Modify JTB1 pin define	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
49	39		2011/11/14	CAP_LED always on issue	Delete QE7 and reserve CE58	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
50	38		2011/11/14	INT SPKR PO noise issue	Mount RE16 for EAPD# control	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
51	46	FAE suggestion	2011/11/14	Audio Precision fail	Change RA1 to 30.1K for adjusted LDO output voltage to 4.8V	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
52	46,47		2011/11/15		Add CA27 & CA33 for DB change to MB, delete QE5	Others		0.3		V
53	52~64	Update power schematic	2011/11/15		Update power circuit for DC & QC type	Others		0.3		V
54	35, 41		2011/11/15		Update QV27, QL3 CIS symbol	Library Update	CIS資料庫更新	0.3		V
55	41		2011/11/16		Change RL3 to 10K and delete CL15 for modify LAN_IO ppwer design	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
56	52		2011/11/16		Change EC_BATT_PRS PU to 3VALW_EC	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3		V
57	42,38,41		2011/11/16		Change EC_WLAN_WAKE netname to EC_WLAN_WAKE# and EC_LAN_WAKE netname to EC_LAN_WAKE#	Others		0.3		V
58	35	LVDS Timing Tuning	2011/11/16		Change RV402 to 10K, RV404 to 150K, CV475 to 0.1uF	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	
59	36		2011/11/16		Change LV7~LV10 PN from SM070001E0L to SM070002S0L	Others		0.3	V	
60	1		2011/11/17		Change UV4~UV7 PN to SA00005B70L for D-die	Others		0.3	V	
61	42		2011/11/17		Delete T22, T23 test point	Others		0.3		V
62	44,45		2011/11/17		Reserve LI2, LI3, LI5, LI6, LI8, LI9 and mount RU3, RI4, RI5, RI7, RI10, RI11, RI12, RI13, reserve DI1, DI4, DI6, DI2, DI3	Cost down		0.3	V	
63	33	dGPU timing tuning	2011/11/17		Change RZ6 to 100 ohm 0603 package for NVIDA suggestion	Vendor design issue	基于零件設計問題，要求設計變更	0.3		V
64	46		2011/11/17		Change CA16 to 0402 package,Delete RA43, RA44, RA28, RA29, RA42	Vendor design issue	基于零件設計問題，要求設計變更	0.3		V
65	43		2011/11/17		Delete RN15~RN22 HDD re-driver bypass circuit	Others		0.3		V
66	36	HDMI EA 7-2 item	2011/11/18		Change RV429~RV436 to 470 ohm	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的範疇	0.3	V	

Security Classification	Compal Secret Data		
Issued Date	2011/08/29	Deciphered Date	2012/07/25

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Title: **Block Diagram**

Size	Document Number	Rev
		0.1

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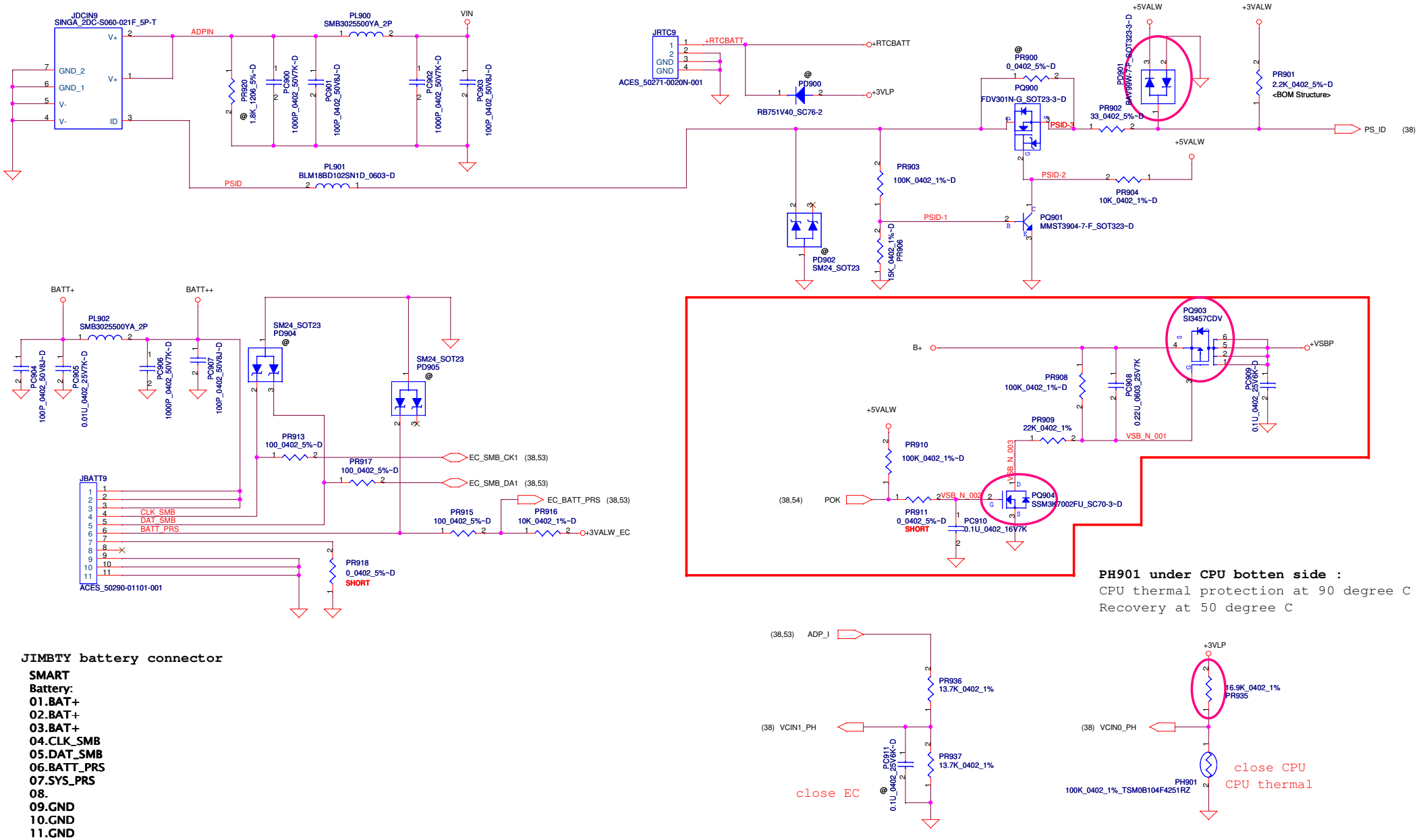

PH901 under CPU botten side :

CPU thermal protection at 90 degree C

Recovery at 50 degree C

JIMBTY battery connector

SMART
Battery:
01.BAT+
02.BAT+
03.BAT+
04.CLK_SMB
05.DAT_SMB
06.BATT_PRS
07.SYS_PRS
08.
09.GND
10.GND
11.GND

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Title: PWR-DCIN / BATT CONN / OTP

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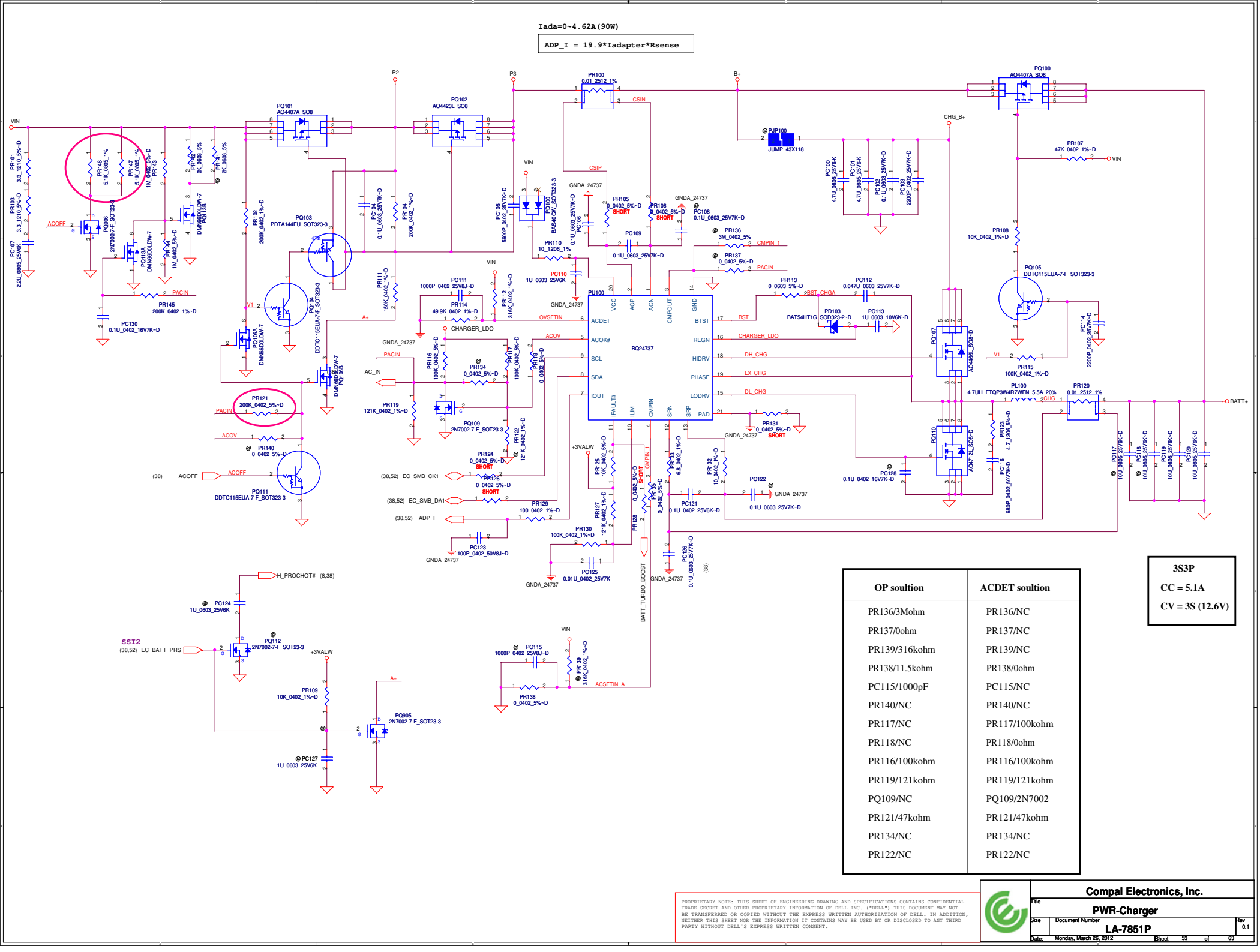

OP soultion	ACDET soultion
PR136/3Mohm	PR136/NC
PR137/0ohm	PR137/NC
PR139/316kohm	PR139/NC
PR138/11.5kohm	PR138/0ohm
PC115/1000pF	PC115/NC
PR140/NC	PR140/NC
PR117/NC	PR117/100kohm
PR118/NC	PR118/0ohm
PR116/100kohm	PR116/100kohm
PR119/121kohm	PR119/121kohm
PQ109/NC	PQ109/2N7002
PR121/47kohm	PR121/47kohm
PR134/NC	PR134/NC
PR122/NC	PR122/NC

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Title: PWR-Charger

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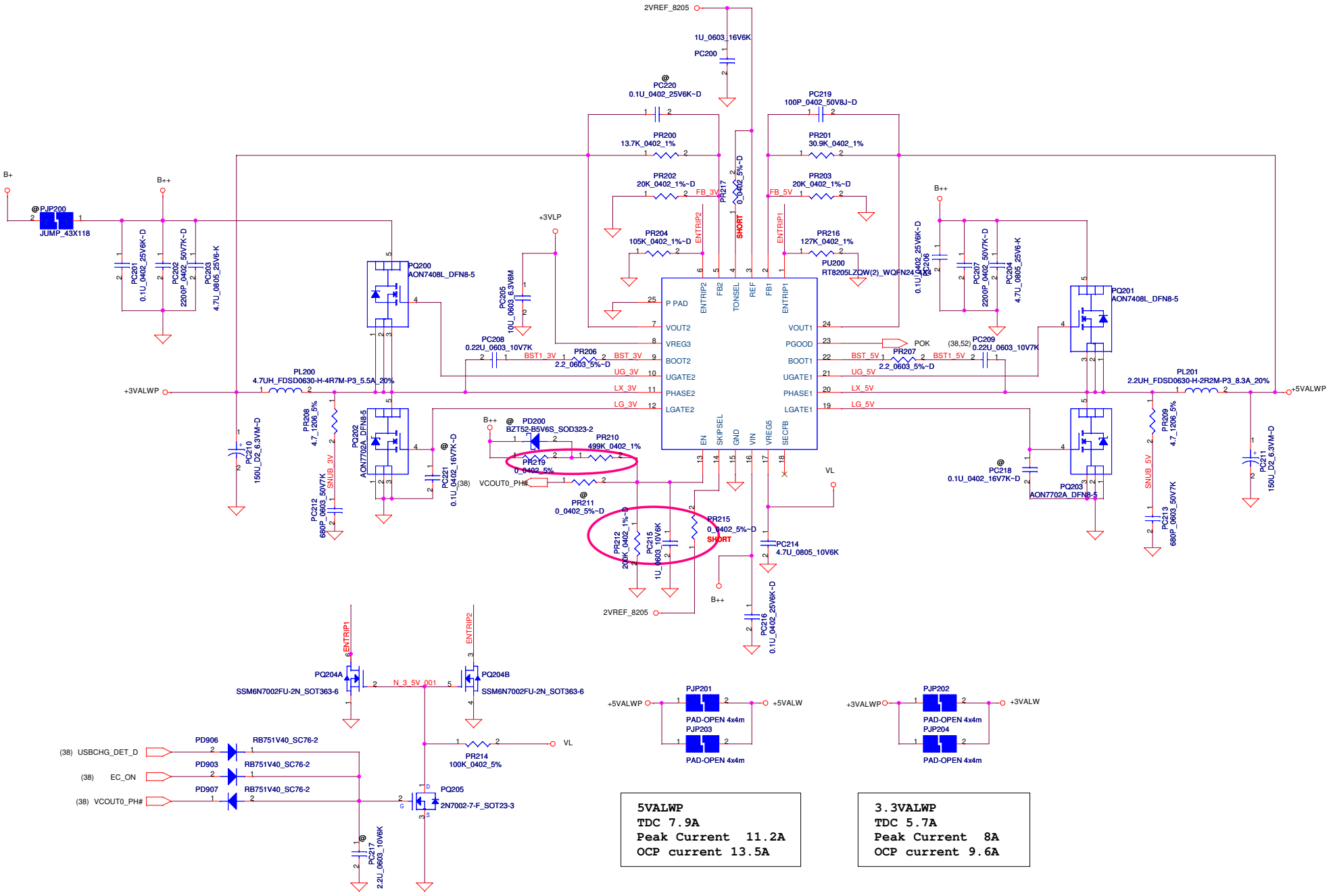

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Title	PWR-3VALWP/5VALWP
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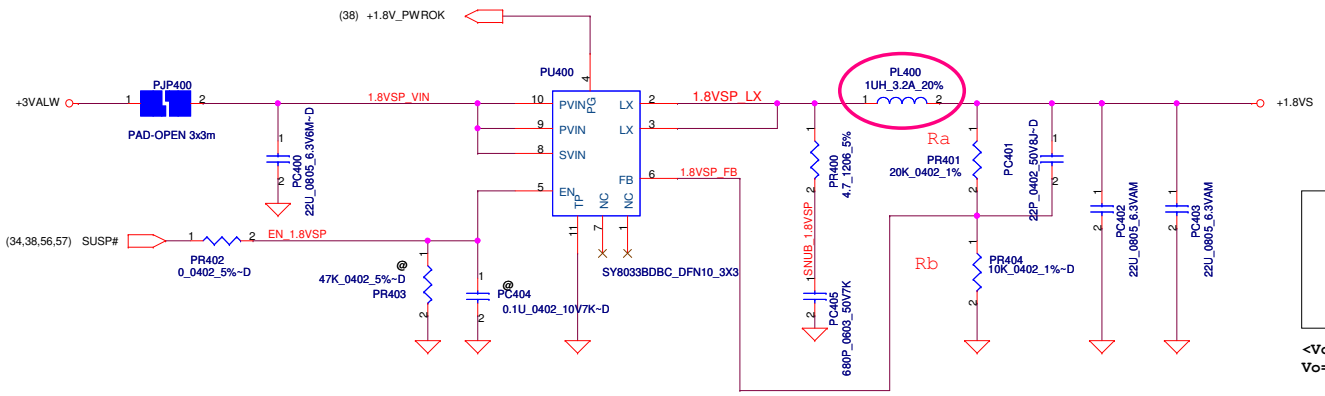

+1.8VSP
TDC 1.3A
Peak Current 1.9A
OCP current 2.3A

<Vo=1.8V> VFB=0.6V
Vo=VFB*(1+Ra/Rb)=0.6*(1+20K/10K)=1.8V

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Title: PWR-1.8VSP

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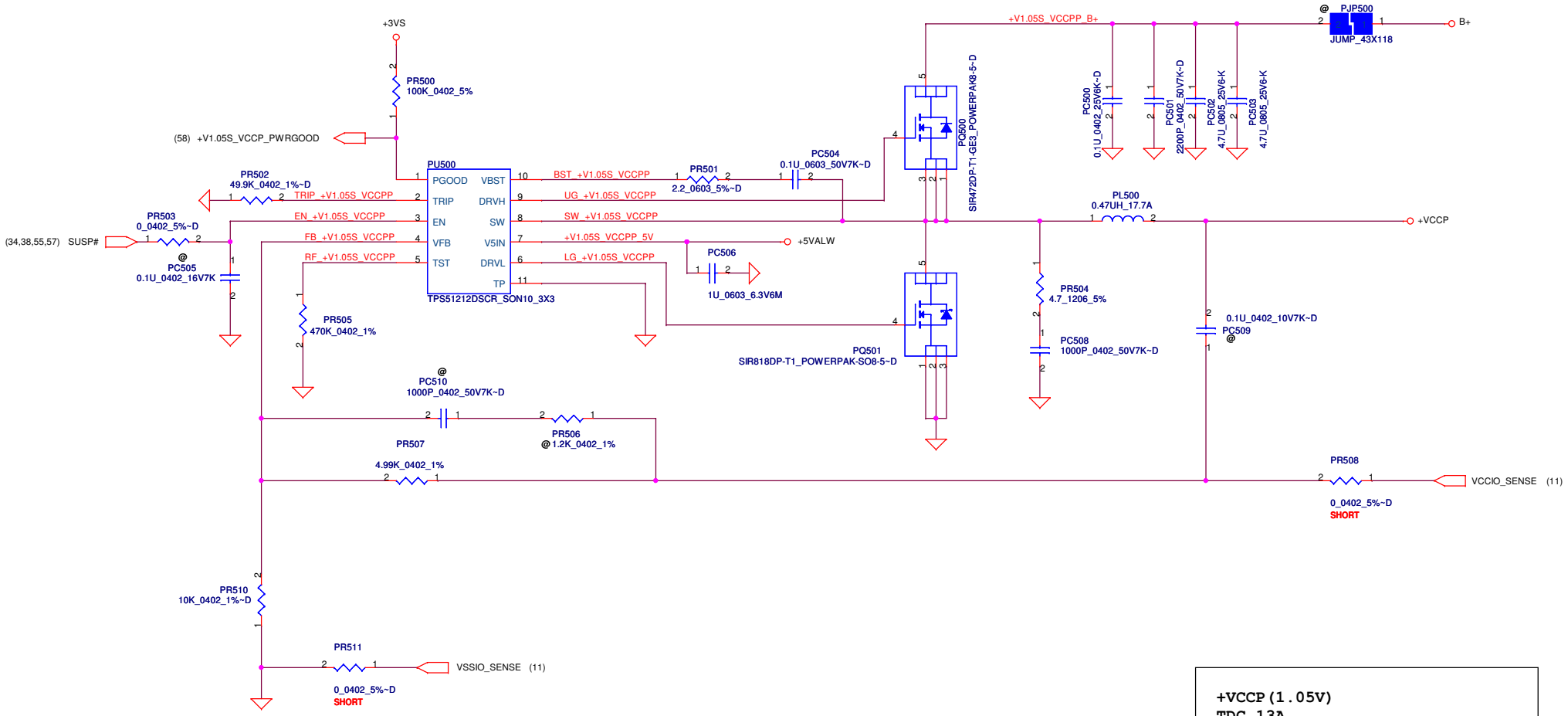

+VCCP(1.05V)
TDC 13A
Peak Current 19A
OCP current 22.8A

	TYP	MAX
H/S Rds(on)	10mohm ,	14.5mohm
L/S Rds(on)	:3mohm ,	3.6mohm

Compal Electronics, Inc.

Title: PWR-V1.05S_VCCPP

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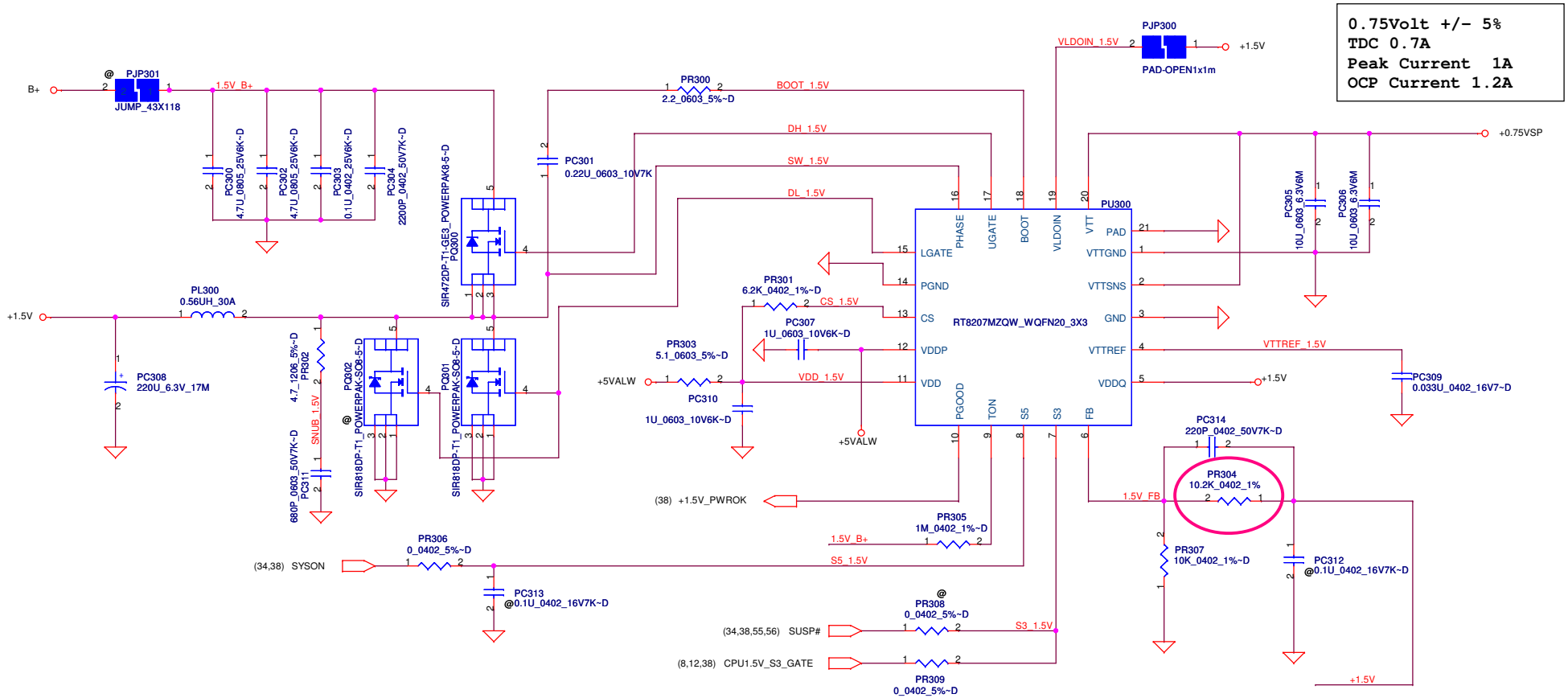

1.5VP
TDC 14 A
Peak Current 20 A
OCP current 24A

	TYP	MAX
H/S Rds(on)	:10mohm ,	14.5mohm
L/S Rds(on)	:3mohm ,	3.6mohm

Compal Electronics, Inc.

Title: PWR-1.5VP/0.75VSP

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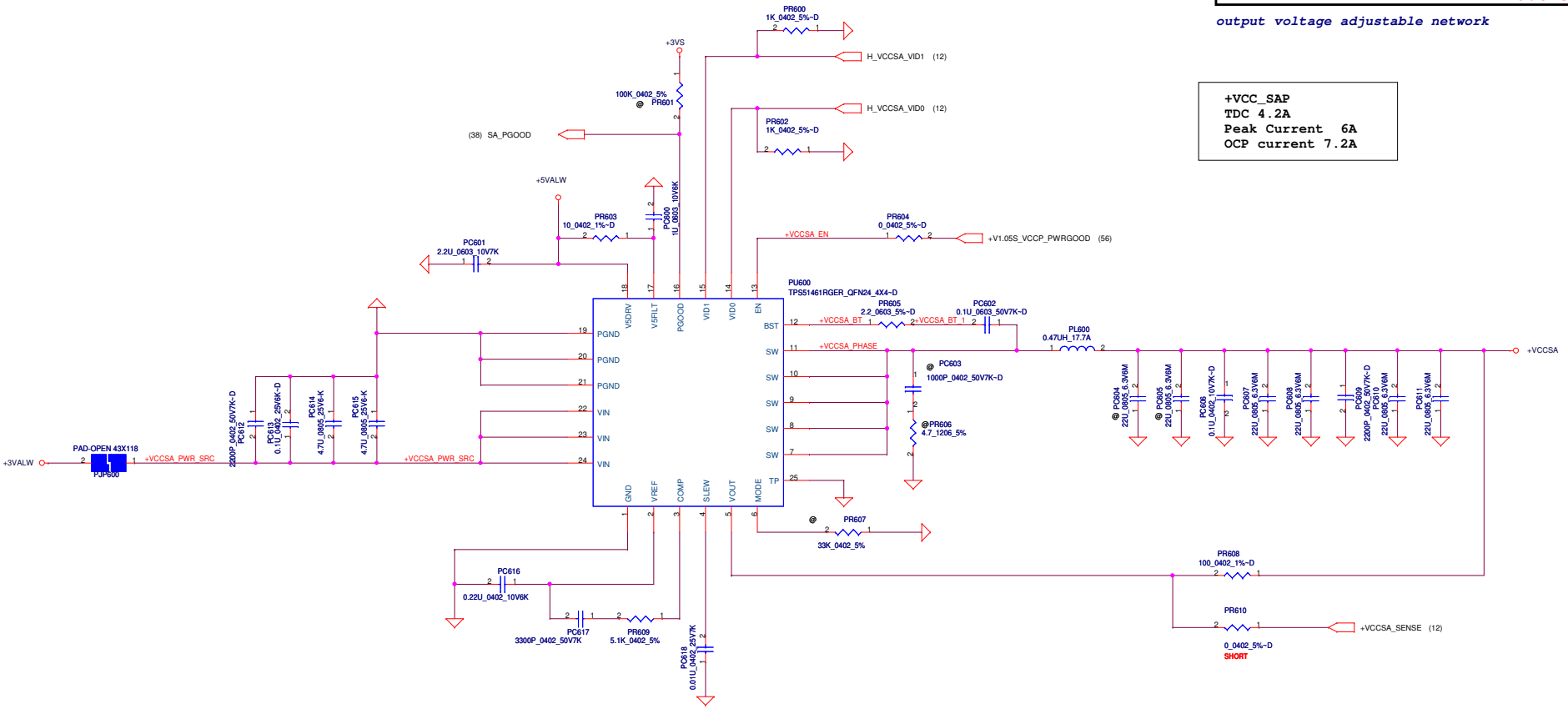
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



Compal Electronics, Inc.

Title: PWR-VCC_SAP

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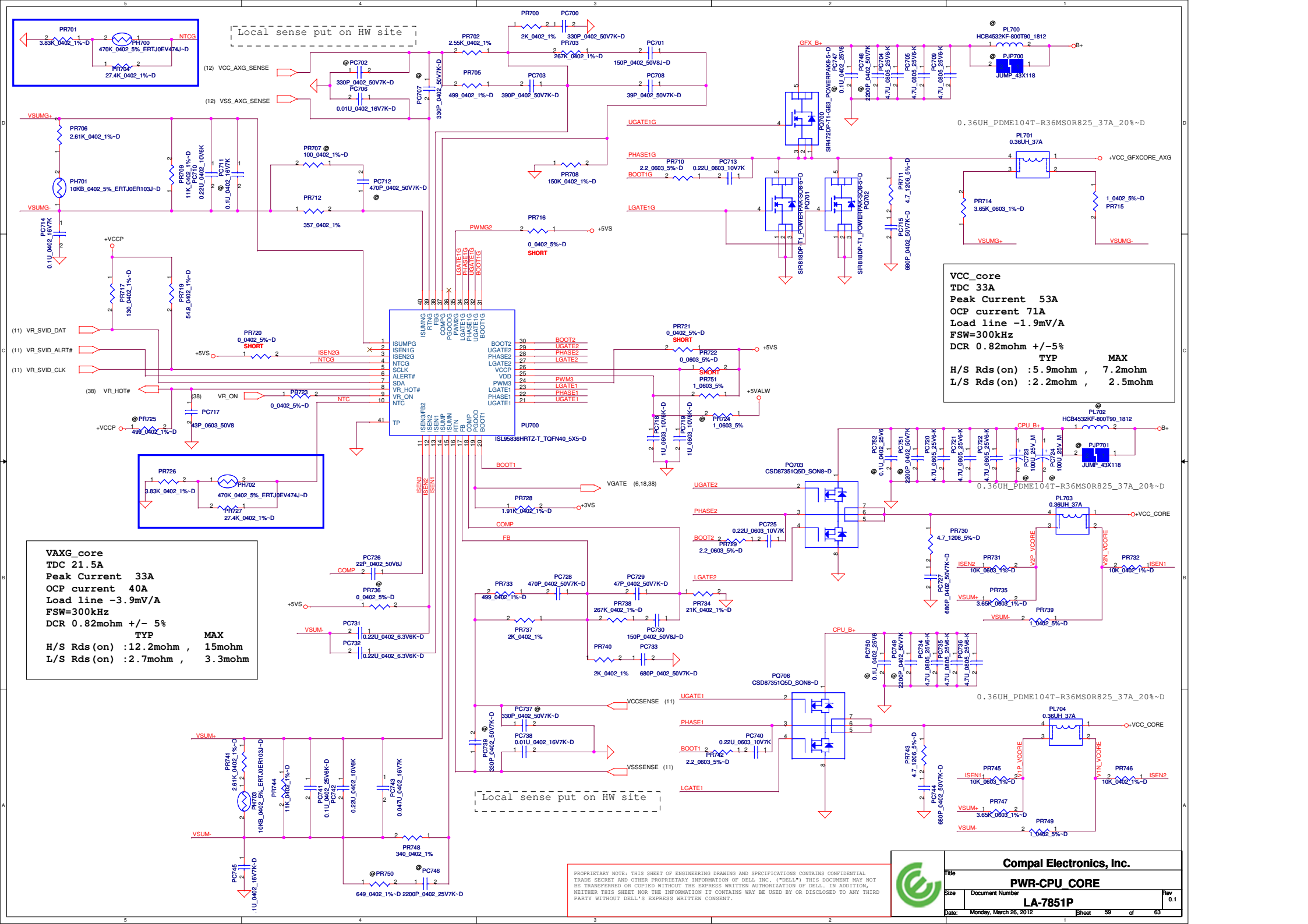
Local sense put on HW site
Local sense put on HW site
VAXG_core
TDC 21.5A
Peak Current 33A
OCP current 40A
Load line -3.9mV/A
FSW=300kHz
DCR 0.82mohm +/- 5%
TYP MAX
H/S Rds(on) :12.2mohm , 15mohm
L/S Rds(on) :2.7mohm , 3.3mohm
VCC_core
TDC 33A
Peak Current 53A
OCP current 71A
Load line -1.9mV/A
FSW=300kHz
DCR 0.82mohm +/-5%
TYP MAX
H/S Rds(on) :5.9mohm , 7.2mohm
L/S Rds(on) :2.2mohm , 2.5mohm
PU700
ISL95836HRTZ-T_TQFN40_5X5~D
0.36UH_PDME104T-R36MS0R825_37A_20%~D
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Compal Electronics, Inc.
Title
PWR-CPU_CORE
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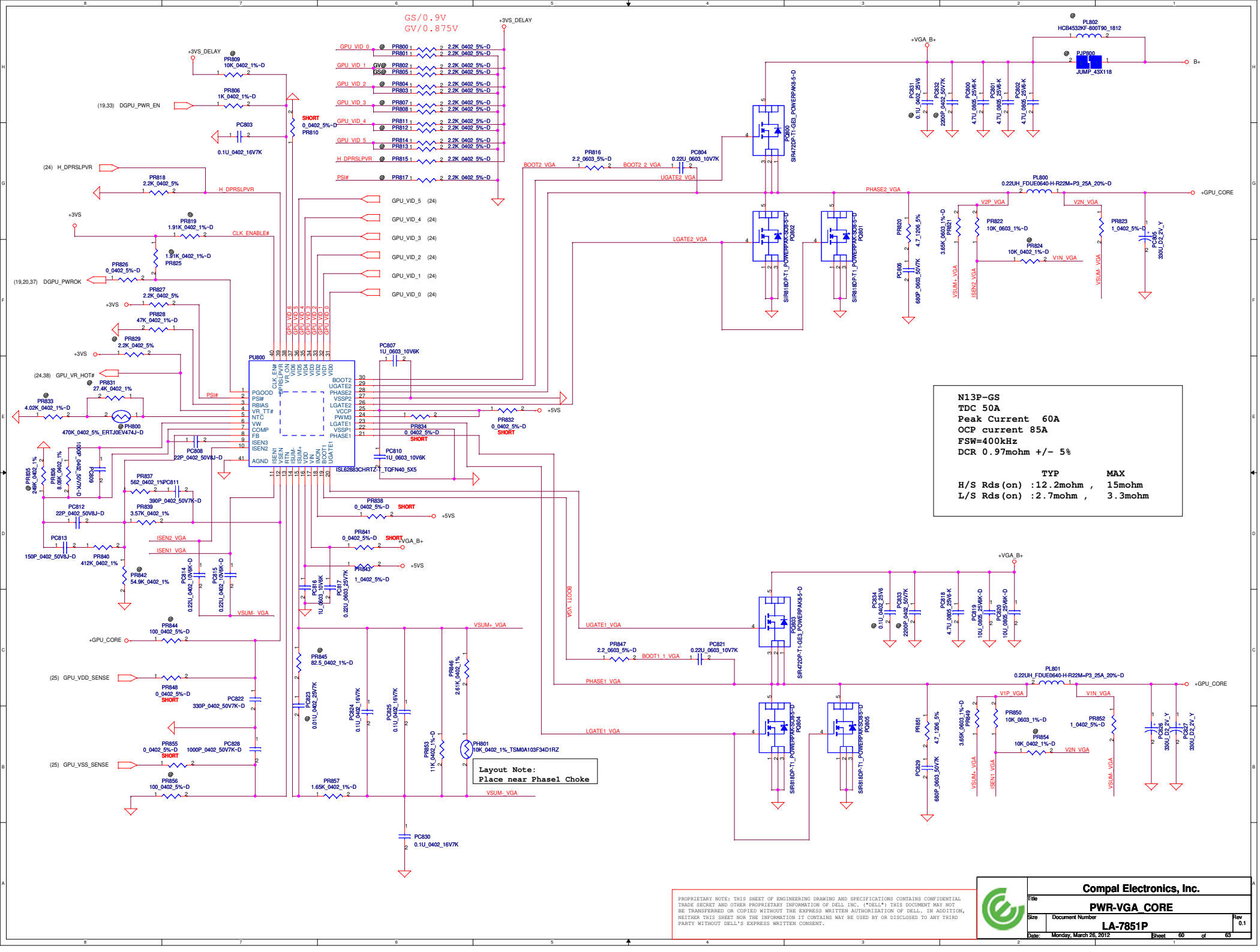

Compal Electronics, Inc.

Title: PWR-VGA_CORE

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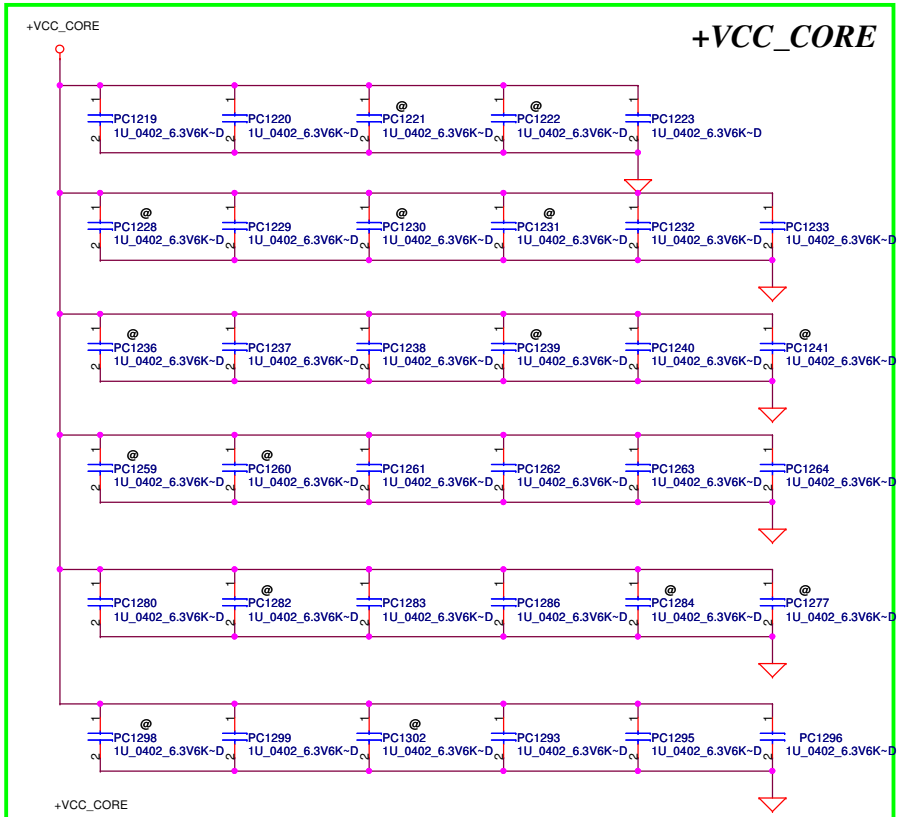
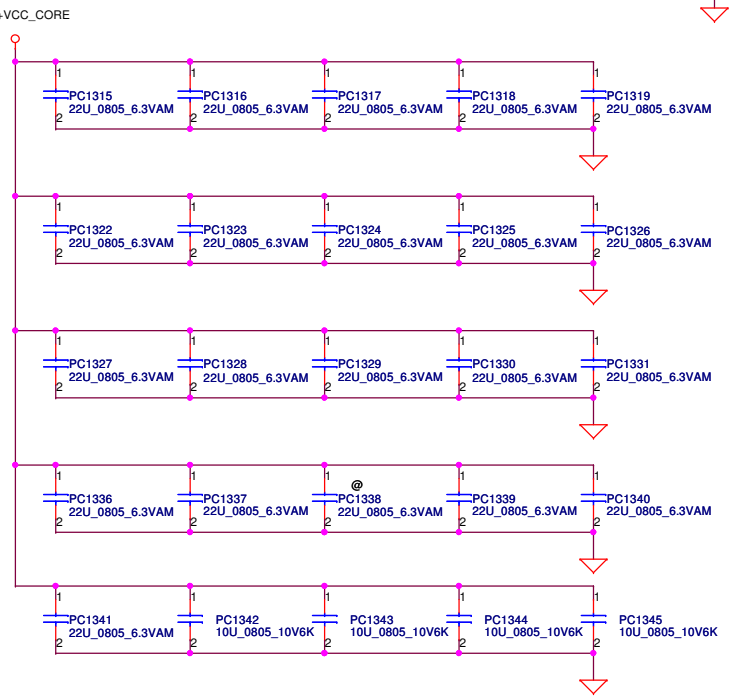
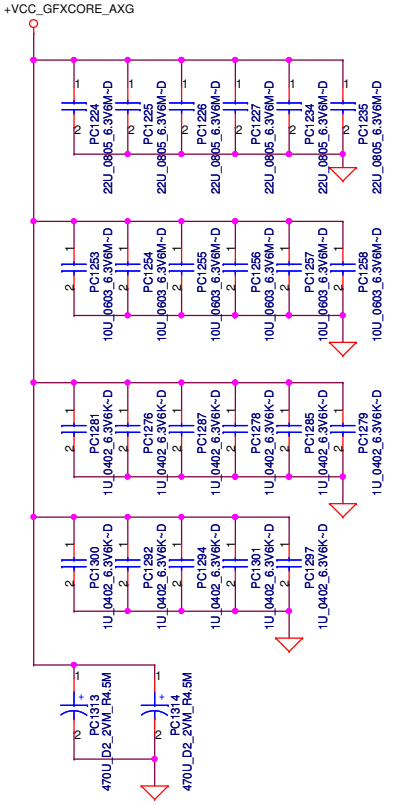
+VCC_CORE





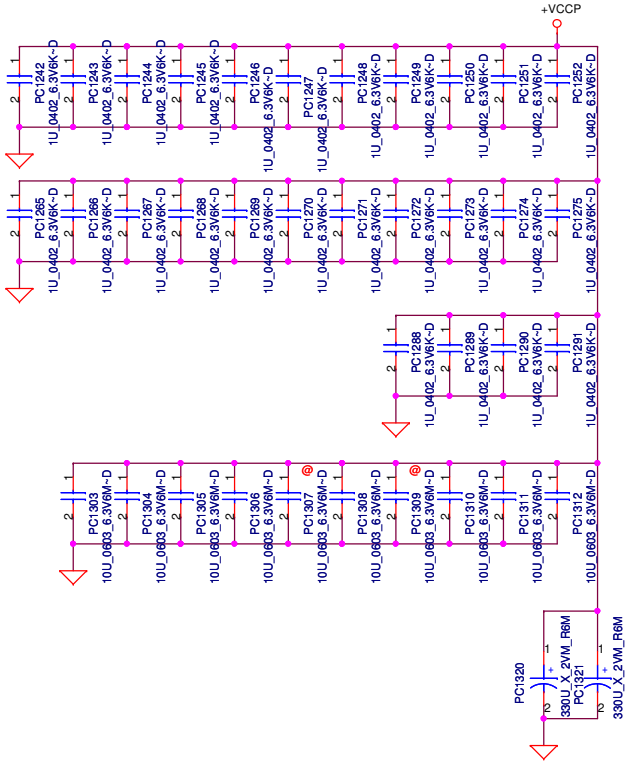
+VCC_GFXCORE_AXG

Design guilde:
iGfx_Cout
1.22uF*6 (SE000000I10)
2.10uF*8 (SE000005T8L)
3.1uF*9 (SE000000K8L)
4.470uF 4.5m *2 (SGA00004200)

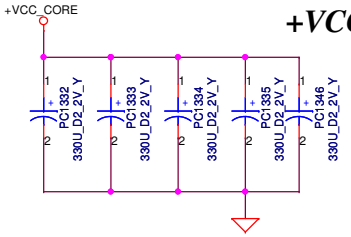


+VCCP

Design guilde:
+1.05V_RUN_VTT
1.1uF*26 (SE000000K8L)
2.10uF*10 (SE000005T8L)
3.330uF 6m *2 (SGA00001Q80)



+VCC_CORE



Design guilde: Vcore_Cout
1.1uF*20 (SE00000888L),reserve 8pcs is not stuff
2.22uF*20 (SE000008L80)
3.470uF 4.5m *4 (SGA00004X80)
4.10uF*4 (SE000004880)

Red @ is for 20% Cap reduces

Compal Electronics, Inc.		
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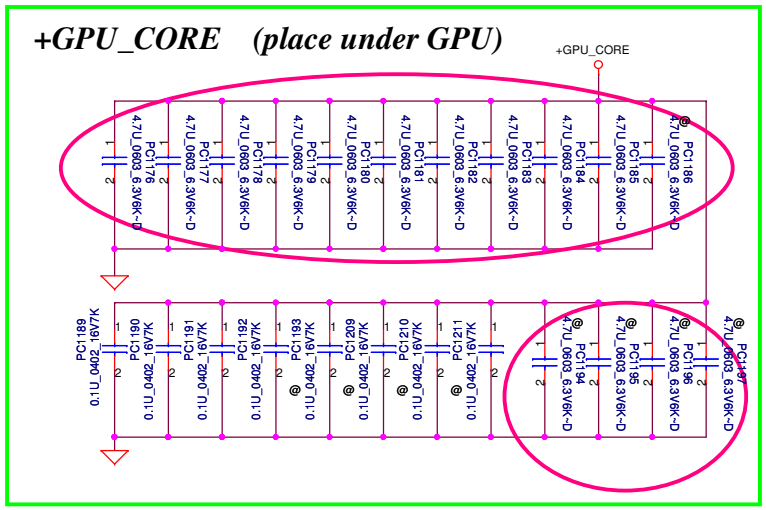

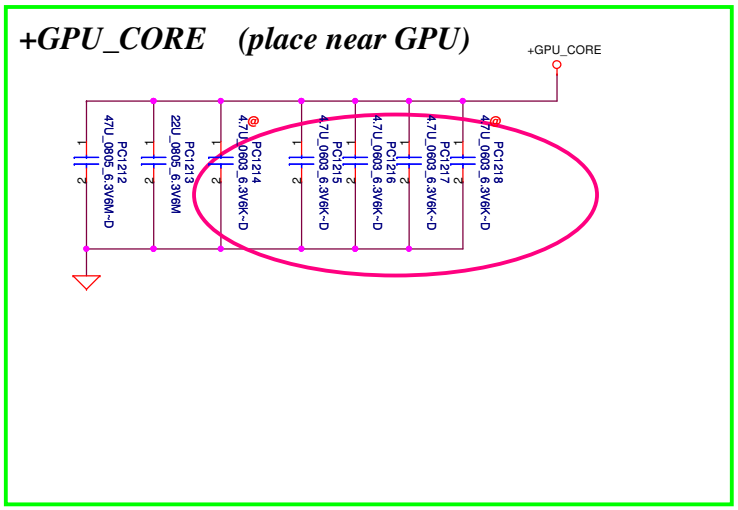

Red @ is for 20% Cap reduces

Design guilde: +GPU_CORE_Cout
Under GPU
1.4.7uF*10 (SE00000G30L),.reserve 5pcs is not stuff
2.0.1uF*4 (SE076104K80)),.reserve 4pcs is not stuff
Near GPU
1.47uF*1 (SE000001120)
2.22uF*1 (SE00000PL0L)
3.4.7uF*5 (SE00000G30L
4.reserve D-case cap is not stuff

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Title	GPU DECOUPLING	
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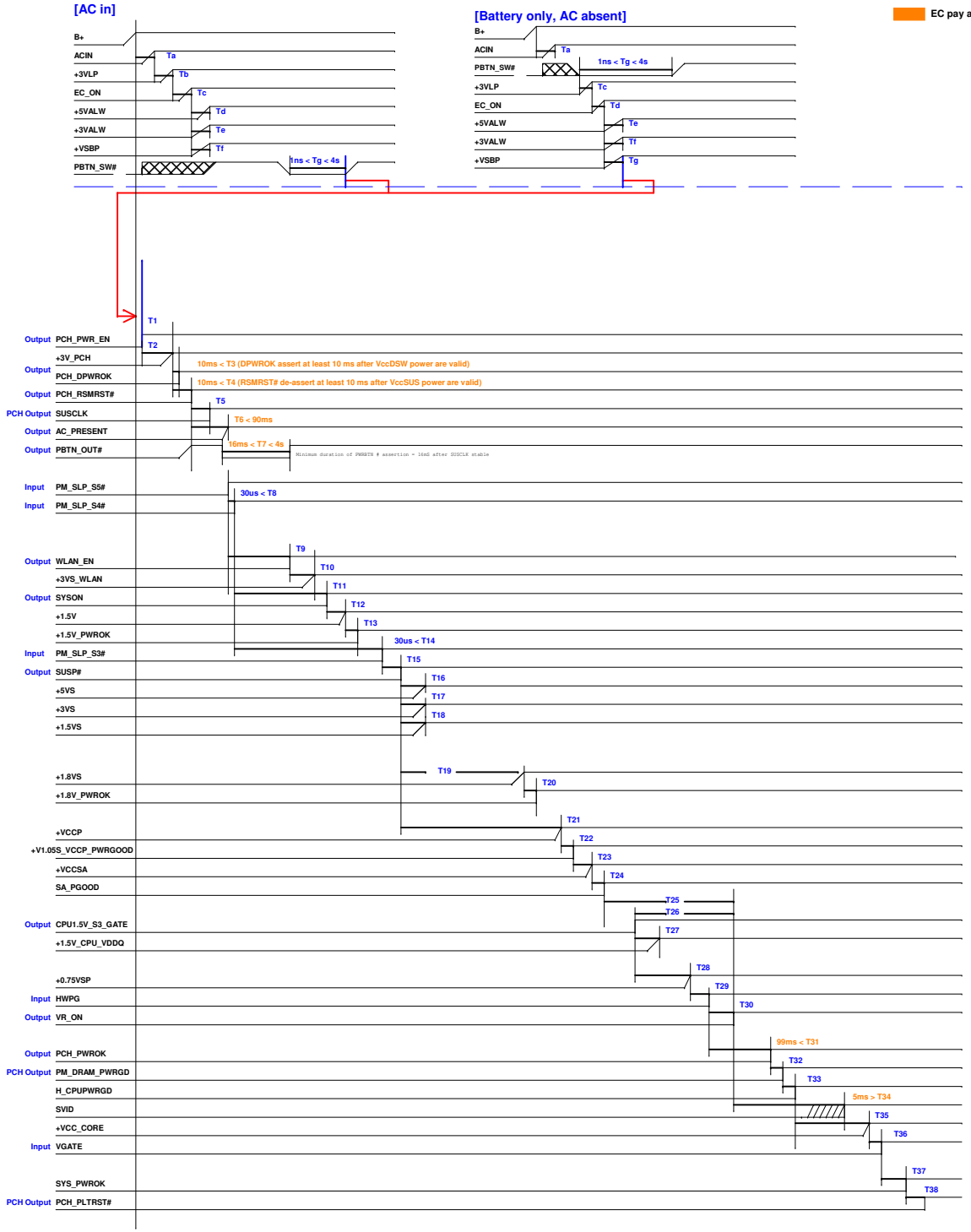
Discrete Power On Sequence



[AC in]

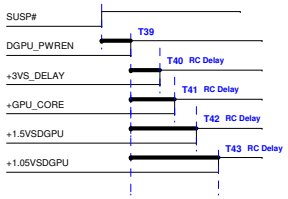
ITEM	Measure Point			Time
Ta	B+	To	ACIN	
Tb	ACIN	To	+3VLP	
Tc	+3VLP	To	EC_ON	
Td	EC_ON	To	+5VALW	
Te	EC_ON	To	+3VALW	
Tf	EC_ON	To	+VSBP	
Tg	PBTN_SW#		Low pluse width	N/A

[Battery only, AC absent]

ITEM	Measure Point			Time
Ta	B+	To	ACIN	
Tb	PBTN_SW#		Low pluse width	N/A
Tc	PBTN_SW#	To	+3VLP	
Td	+3VLP	To	EC_ON	
Te	EC_ON	To	+5VALW	
Tf	EC_ON	To	+3VALW	
Tg	EC_ON	To	+VSBP	

ITEM	Measure Point			Time
T1	PBTN_SW#	To	PCH_PWR_EN	
T2	PCH_PWR_EN	To	+3V_PCH	
T3	+3V_PCH	To	PCH_DPWROK	
T4	+3V_PCH	To	PCH_RSMRST#	
T5	PCH_RSMRST#	To	SUSCLK	
T6	PCH_RSMRST#	To	AC_PRESENT	
T7	PBTN_OUT#	To	Low pluse width	
T8	PM_SLP_S5#	To	PM_SLP_S4#	
T9	PM_SLP_S5#	To	WLAN_EN	
T10	WLAN_EN	To	+3VS_WLAN	
T11	PM_SLP_S4#	To	SYSON	
T12	SYSON	To	+1.5V	
T13	+1.5V	To	+1.5V_PWROK	
T14	PM_SLP_S4#	To	PM_SLP_S3#	
T15	PM_SLP_S3#	To	SUSP#	
T16	SUSP#	To	+5VS	
T17	SUSP#	To	+3VS	
T18	SUSP#	To	+1.5VS	
T19	SUSP#	To	+1.8VS	
T20	+1.8VS	To	+1.8V_PWROK	
T21	SUSP#	To	+VCCP	
T22	+VCCP	To	+V1.05S_VCCP_PWRGOOD	
T23	+V1.05S_VCCP_PWRGOOD	To	+VCCSA	
T24	+VCCSA	To	SA_PGOOD	
T25	SA_PGOOD	To	VR_ON	
T26	CPU1.5V_S3_GATE	To	VR_ON	
T27	CPU1.5V_S3_GATE	To	+1.5V_CPU_VDDQ	
T28	CPU1.5V_S3_GATE	To	+0.75VSP	
T29	+0.75VSP	To	HWPG	
T30	HWPG	To	VR_ON	
T31	HWPG	To	PCH_PWROK	
T32	PCH_PWROK	To	PM_DRAM_PWRGD	
T33	PM_DRAM_PWRGD	To	H_CPUPWRGD	
T34	VR_ON	To	SVID	
T35	H_CPUPWRGD	To	+VCC_CORE	
T36	+VCC_CORE	To	VGATE	
T37	VGATE	To	SYS_PWROK	
T38	SYS_PWROK	To	PCH_PLTRST#	
T39	DGPU_PWREN	To	+3VS_DELAY	
T40	DGPU_PWREN	To	+GPU_CORE	
T41	DGPU_PWREN	To	+1.5VSDGPU	
T42	DGPU_PWREN	To	+1.05VSDGPU	
T43	DGPU_PWREN	To	+1.05VSDGPU	

GPU power on sequence



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: Power Sequence

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X02

	Compal Electronics, Inc.	
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EE change note for QBL00 Main Board

Item	Page	Title	Date	Issue Description	Solution Description	Cause Category	Note	Rev.	BOM	Layout
1	46, 47, 38, 17, 24, 39	PT SMT MEMO change part	2011/12/21		Change RA22, RA23, RA35, RA36, RA25, RA26, RA27, RA34 PN to SD034330280(33K) Change CA15, CA30, CA28, CA31, CA44, CA65, CA66, CA67 PN to SE071121J8L(120P) Change RA45, RA41, RA48, RA46 PN to SD034150380(150k) Change YH2 PN to SJ10000EF00(25MHz) Change YV1 PN to SJ10000970L(27MHz) Change RE84 PN to SD02847008L(470 ohm) Change R45 PN to SD03447028L(47K) Change CA43, CA45, CA46 PN to SE00000QK0L(10U_0805)	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.4	V	
2	47	Change to X7R part	2011/12/21		Change CA61, CA62, CA72, CA73 to X7R part	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.4	V	
3	17	Reserve CLK_CPU_ITP signal	2011/12/21		Reserve RH91, RH92 for CLK_CPU_ITP	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.4	V	
4	12		2011/12/21		Delete JP7	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.4		V
5	40		2011/12/21		Change JTB1 PIN11 to +RTCVCC	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.4		V
6	42, 44, 45		2011/12/22	USB port and MiniCard will flash of light when AC plug in	Add USB_PWR_EN# PU 10K(RI14) to +3VALW Add PWRSHARE_EN_EC#PU 10K(RI15) to +3VALW Add WLAN_EN# PU 10K(RM24) to +3VALW	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.4		V
7	43	Derating	2011/12/23		Change RN24 to 330K and add RN27 1.5M	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
8	38	Board ID Table for AD channel	2011/12/23		Change RE12 to 33K	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題		V	
9	46		2011/12/28	AUD_SPK Netname duplicate	Modify netname to AUD_SPK_RC_L+/AUD_SPK_RC_L-	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
10	47		2011/12/28		Change RA47 package to 0805	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
11	47		2011/12/30	For S5 power saving in AC mode	Change RZ38 PU to +5VS	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
12	38		2011/12/30	3V/5V_ALW on in DC mode	Change RE50 PU to +3VLP and reserve RE44	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
13	7~13	Modify CPU PN	2012/1/2		LA7851 QC sku Change UU1 PN to SA00005JZ0L for LA7852 DC sku	Others			V	
14	24~28	Modify GPU PN	2012/1/2		Change UV1 PN to SA00005180L for GS, change UV1 PN to SA0000569 0L for GV	Others			V	
15	16~23	Modify PCH PN	2012/1/2		Change UH1 PN to SA00005AG1L	Others			V	
16	40	Modify TPM PN and add BOM optional	2012/1/2		Change U1 PN to SA00004WQ10 and add TPM@ in value for BOM optional C1~C6 add TPM@ in value for BOM optional	Others			V	
17	35		2012/1/4	Ambient light sensor abnormal	Change RV417 to 100 ohm for DMIC_CLK signal	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題		V	
18	47		2012/1/4	Audio Precision SPRK Fail	Change LA7, LA8 to 0 ohm	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
19	45	Cost down	2012/1/4		Reserve CI14(150uF) and add CI22(10uF), CI23(10uF)	Cost down				V
20	8, 11, 12, 17, 18, 21, 22, 26, 33, 35, 37, 38, 40, 41, 42, 43, 44, 45, 46 , 47	Change 0 ohm footprint to shortpad	2012/1/4		Change RU31, RU34, RU75, RU62, RU88, RU97, RU98, RU100, RU108, RU109, RU111, RU118, RU94, RH44, RH105, RH106, RH108, RH110, RH112, RH101, RH103, RH111, RH197, RH222, RH199, RV337, RZ4, RV415, RV424, RI27, RI26, RV449, RE60, RE34, RE35, RE61, RE39, RE41, RE27, RE45, RE46, RE10, RE31, RE16, RE25, RE22, RE26, RN44, RN45, RN46, RN48, RN49, RN50, RN51, RL5, RL6, RM10, RM13, RM20, RM21, RN29, RI3, RI4, RI5, RI7, RI10, RI11, RI12, RI13, RI17, RI22, RI23, RI24, RI25, RA5, RA50 to shortpad	Cost down				V
21	40, 46		2012/1/5	Audio Precision Headphone out c	Modify JTB1 Pin9 to UA2 Pin31 (CPVREF)	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
22	45	For buyer suggestion change to PI5USB1457	2012/1/9		Change UI3 PN to SA00004RE0L and reserve RI28 for PWRSHARE_EN_EC# signal from EC	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
23	46	For Audio precision EA	2012/1/9		Change CA27, CA33 PN to SGA00004D00	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題		V	
24	35	Change LVDS CONN Footprint	2012/1/10		Change JLVDS PN&Footprint to SP01001BT00&ACES_50003-04006-001_40P	Others				V
25	46	Audio Vendor review suggestion	2012/1/10		Add RA17 and reserve RA12 to AGND for CPVREF signal Change LA1 to 0 ohm Add RA18 for MIC1 signal	Others				V
26	47				Change RA41, RA45, RA46, RA48 to 33K, RA49, RA51, RA52, RA58 to 60.4K Change RA50 to 0 ohm	Others			V	
27	17, 25, 35, 38		2012/1/11	Battery can't Charge	Change Ambient Light Sensor, GPU SMBus to PCH_SMLCLK/PCH_SMLDATA Reserve QH3 for EC to PCH SMBus Change QV21, QM4 from EC_SMB_CK1/EC_SMB_DA1 to PCH_SMLCLK/PCH_SMLDATA	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
28	25	Nvdia vendor strap pin suggestion	2012/1/11		Change RV303 to 10K, RV302 to 4.99K and RV309, RV310 value add GV@, Add RV309 45.3K for GS@	Vendor design issue		V		
29	52~64	Update power circuit	2012/1/11		Update power circuit	Others				V
30	47	For breakdown	2012/1/11		Add LA9	Others				V
31	52~64	Update power circuit	2012/1/12		Update power circuit	Others				V
32	25, 12	Layout placement	2012/1/12		Change RV337 to 0_0603, delete RU94	Others				V
33	34	Follow XPS14 design	2012/1/12		Changee RZ17 to 100K	Others				V
34	38, 42	For QT reserve it	2012/1/12		Change RE61, RE22, RM10, RM13 to 0_0402	Others				V
35	35	Cost down	2012/1/12		Reserve QM4, RH96, RH94 and mount RM23, RM15	Others		V		
36	33		2012/1/13	GPU 1.5VSDGPU voltage drop	Change UZ2 PN to SB000008J0L	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
37	38		2012/1/13	USB Charge can't wake up system	Change RE32 PU to +3VLP	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
38	39	EMI reust reserve for ESD	2012/1/13		Reserve DE6	ME/SA request design change				V
39	40		2012/1/13		Change HS footprint to H_3P5	ME/SA request design change				V
40	52~64	Update power circuit	2012/1/13		Update power circuit	Others				V
41	46	Layout placement	2012/1/13		Change CA27, CA33 footprint to C_B2	Others				V
42	39	Cost down	2012/1/13		Change SW1 PN to SN100005100	ME/SA request design change		V		
43	25	Nvdia vendor strap pin suggestion	2012/1/13		Change RV315 to 4.99K	Vendor design issue		V		
44	33	HF part	2012/1/13		Change RZ10, RZ11, RZ15 PN to SD028220A8L	Others		V		
45	52~64	Update power circuit	2012/1/16		Update power circuit	Others		V		
46	19, 34, 35, 39, 41, 36 47, 48	接水登錄機	2012/1/18		Change QE4, QE6, QH6, QL6, QV33, QZ9, QZ11 PN to SB00000M700 Change DE7, DE8, DE9, DE10, DE3 PN to SCS00002G00 Change DV9 PN to SCS00002G00	Others		V		
47	44, 45		2012/1/18	Can't detect the [Gauntlet2 USB3.0 HDD BOX] on USB port	Mount CI1, CI7, CI14 and reserve CI18, CI19, CI20, CI21, CI22, CI23	Others		V		
48	52~64	Update power circuit	2012/1/19		Update power circuit	Others		V		
49	49	Tune system LED brightness	2012/1/30		Change R9 to 220 ohm	ME/SA request design change		V		
50	37, 24, 39	HF part	2012/1/30		Change QV38 PN to SB339040310 Change QV24 PN to SB000008J00 Change F1 PN to SP040003200	Others		V		
51	52~64	Update power circuit	2012/2/1		Update power circuit	Others		V		
52	35, 40, 45	Change Y5V CAP PN	2012/2/6		Change CI11, CV3508 PN to SE064106M8L Change CM33 PN to SE076104K8L Change CM31 PN to SE076473K8L	Others		V		
53	14	Change CAP PN	2012/7/1		Change CD7 PN to SGA00005H0L	Others		V		

EE change note for QBL00 Main Board

Item	Page	Title	Date	Issue Description	Solution Description	Cause Category	Note	Rev.	BOM	Layout
1	47	ST build MEMO change	2012/2/23	CA47 footprint not match with BOM	Change CA47 footprint to 0402 in LA7851 MB	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	V
2	24			CV575, CV576 PN is not match Value	Change CV575, CV576 PN to SE071100J8L	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	V
3	12, 19, 41	0 ohm shortpad	2012/2/23		Change RU118, RH152, RL15 footprint to shortpad	Others		1.00		V
4	38	Board ID Table for AD channel	2012/3/2		Change RE12 to 56K	Others		1.00	V	
5	20	TPM board ID for BOM optional	2012/3/2		Add RH164 (1K) PD for WO TPM and RH163 PU for W/TPM	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	V
6	7	R1 & R3 BOM control for CPU PN	2012/3/5		Add UU1 BOM symbol QCR1@ & QCR3@ for LA7851 Add UU1 BOM symbol IVBR1@, IVBR3@, SNBR1@ and SNBR3@ for LA7852	Others		1.00	V	
7	16	Change SPI ROM PN R1 & R3 BOM control for PCH PN	2012/3/5		Change UH2 PN to SA000039A2L Add UH1 BOM symbol R1@ & R3@ for PCH PN	Others		1.00	V	
8	1	VRAM X76 BOM control for HYN1G & HYN2	2012/3/5		Add UV4, UV5, UV6, UV7, UV8, UV9, UV10, UV11 BOM symbol HYN2G@ for VRAM X76	Others		1.00	V	
9	45	Change Powershare IC to SILEGO	2012/3/5	Used Samsung i9100 phone can't detected by OS issue	Change UI3 PN to SA00004VH00	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	
10	14	Change 330U CAP	2012/3/5		Change CD7 PN to SGA19331D0L(ESR=15)	Others		1.00	V	
11	24	R1 & R3 BOM control for GPU GV & GS PN	2012/3/5		Add UV1 BOM symbol GVR1@, GVR3@, GSR1@ and GSR3@ for GPU	Others		1.00	V	
12	25	GPU strap pin setting	2012/3/5		GVHA@	Vendor design issue		1.00	V	
13	2	R1 & R3 BOM control for PCB-MB	2012/3/5		Add ZZZ BOM symbol for PCB-MB	Others		1.00	V	
14	52~62	Update power circuit	2012/3/5		Update Power circuit	Others		1.00	V	V
15	47	Change AMP chip power rail	2012/3/5	S5 power consumption in DC mode	Change UA5 power rail from B+ to +VSBP	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00		V
16	37	0 ohm shortpad	2012/3/6		Change RV464 footprint to shortpad	Others		1.00		V
17	52	Update power circuit	2012/3/7	PD901 Layout footprint error	Change PD901 footprint to RHU002N06_SOT323-3(same to XPS14)	Others		1.00		V
18	52~62	Update power circuit	2012/3/12		Change 1.8V choke	Others		1.00	V	
19	19, 38, 17 40	EMI Request	2012/3/13	EMI_ Fails at 99MHz @-1.19dB it is harmonic ofPCI clo	Mount CH14, RE13, CE11 and add CE15 for CLK_PCI_LPC signal Mount R2, C8, CH13 for CLK_PCI_TPM signal	Others		1.00	V	V
20	39, 34, 46	EMI Request	2012/3/13		Add CE59 for KB_DET# signal Add CZ42 for SYSON signal and add CZ43 for SYSON# signal Mount CA20, RA14 and change to 33 ohm CA20 for HDA_BITCLK_AUDIO signal Mount CA21 for HDA_SDOUT_AUDIO signal Add CA35 for CPVREF_R signal	Others		1.00	V	V
21	35, 46, 47	0 ohm shortpad	2012/3/13		Change RM15, RM23 footprint to shortpad Change LA1 footprint to shortpad Change RA50, RA53, LA7, LA8 footprint to shortpad	Others		1.00	V	V
22	52~62	Update power circuit	2012/3/14		Update Power circuit	Others		1.00	V	V
23	38	0 ohm shortpad	2012/3/14		Change RE51, RE22 footprint to shortpad	Others		1.00	V	V
24	37	Update JMDP footprint	2012/3/14		Change JMDP footprint	ME/SA request design change	其他設計單位要求的設計變更	1.00	V	V
25	14	Change 330U CAP	2012/3/15		Change CD7 PN to SGA00002281(ESR=15) and footprint to C_SX	Others		1.00	V	V
26	46		2012/3/16	DTM issue (Ti switch 在inbox driver 下，combo Jack 信	Mount RA12 and reverse CA35	ME/SA request design change	其他設計單位要求的設計變更	1.00	V	
27	16	Sourcer request to remove TXC 32.768K crystal in BOM	2012/3/19		Change YH1 PN to SJ10000BM00	Others		1.00	V	
28	48		2012/3/19	System LED Brigtness	Change R15 to 100 ohm	ME/SA request design change	其他設計單位要求的設計變更	1.00	V	
29	48		2012/3/21	Fine tune system LED Brigtness	Change R9 to 100 ohm	ME/SA request design change	其他設計單位要求的設計變更	1.00	V	
30	39		2012/3/22		Change SW1 PN to SN100002M10	ME/SA request design change	其他設計單位要求的設計變更	1.00	V	
31	38, 40		2012/3/22	PCI clock EA fail for EMI soulation	Change C8, CE11 to 10P for CLK_PCI_TPM	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	
32	38		2012/3/22	OTP fail for PQ205 2nd source	Change RE59 to 1M and RE32 to 100K	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	
33	46	Change FSOV back to 300mV	2012/3/23		Change CA27, CA33 to 150uF	Others		1.00	V	
34	19, 38		2012/3/23	PCI clock EA fail for EMI soulation	Reserve CH14, CE15	Others		1.00	V	
35	41, 43, 52	SB0000009610 turned to EL	2012/3/26		Change QL5, QN5, QN6, PQ904 PN to SB00000960L	Others		1.00	V	

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/29	Deciphered Date	2012/07/25
Title	Block Diagram		
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