
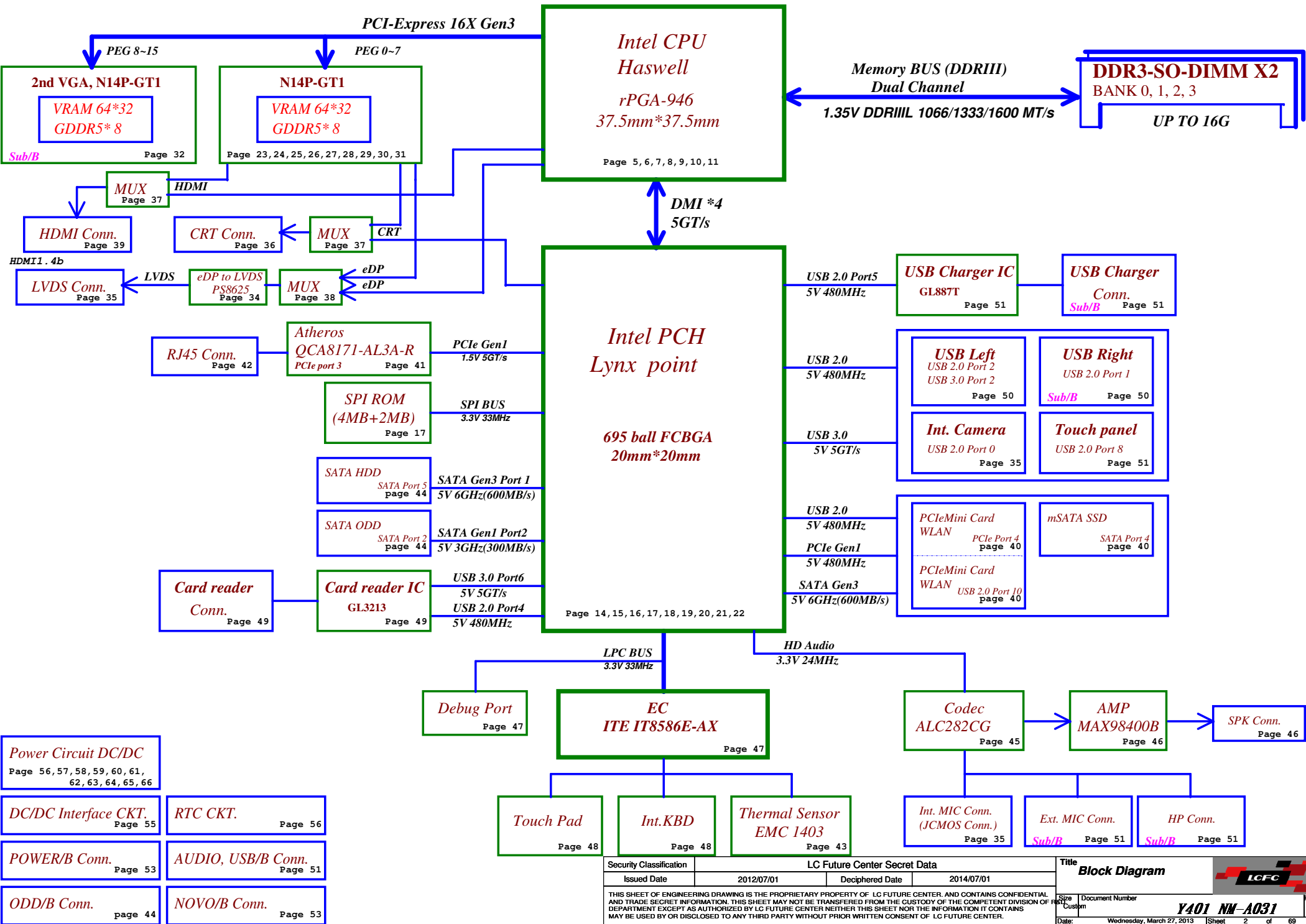


VIQY0 (Y410)

NM_A031 Rev1.0 Schematic

***Intel Haswell Processor with DDRIII + Lynx point PCH
nVIDIA N14P GT + 2nd VGA N14P GT
2013-03-19 Rev1.0***

Security Classification	LC Future Center Secret Data			Title Cover Page		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Size Custom		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Document Number Y410 NM-A031		Rev 1.0
Date: Wednesday, March 27, 2013				Sheet 1 of 69		



Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
EHCI1	XHCI	0	Camera
		1	USB Port (Right Side)
		2	USB Port (Left Side)
		3	
	4	4	Card Reader
		5	USB Port (Right Side)
		6	
7			
EHCI2		8	
		9	
		10	Mini Card(WLAN)
		11	
		12	
		13	

BOM Structure Table

BOM Structure	BTO Item
GT@	NV GT750M
GT1@	NV GT755M
CMOS@	CMOS Camera part
SURGE@	QCA8171 LAN surge part
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
@	Unpop
DS3@	Deep S3 support part
daul@	Support daul channel panel function
887T@	GENESYS 887T USB charger solution
887@	GENESYS 887 USB charger solution
TI@	TI USB charger solution
EDP@	Support EDP panel function
SLI@	For SLI function part
47W@	For 47W CPU part
37W@	For 37W CPU part

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
SMB_CLK_S3 SMB_DATA_S3	PCH +3VS	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIe PORT LIST

Port	Device
1	
2	
3	
4	LAN
5	WLAN
6	
7	
8	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

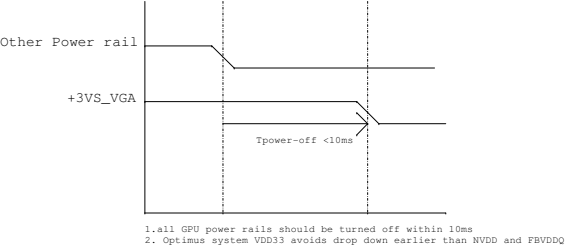
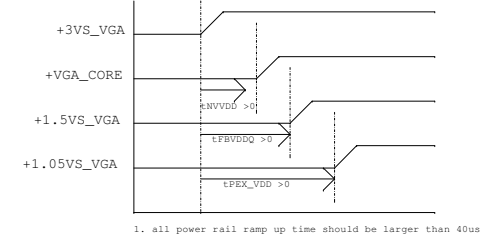


Security Classification	LC Future Center Secret Data		Title	Notes List	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FUTURE CENTER DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Rev	1.0
				Date:	Wednesday, March 27, 2013
				Sheet	3 of 69

Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N14Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	IN	-	FB_CLAMP_MON
GPIO1	OUT	-	NA
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	NA
GPIO6	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO7	OUT	-	NA
GPIO8	OUT	-	OVERT#
GPIO9	OUT	-	VGA_ALERT#
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	NVVD PWM_VID
GPIO12	IN	-	AC Power Detect Input (10K pull High)
GPIO13	OUT	-	DPRSLPVR_VGA
GPIO14	OUT	-	NA
GPIO15	IN	-	NA
GPIO16	OUT	-	NA
GPIO17	IN	-	VGA_EDP_HPD
GPIO18	IN	-	DGPU_HDMI_HPD
GPIO19	IN	-	NA



Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Device ID		setting		I2C Slave addresses ID	
N14P-GT (28nm)	0x0FCD	SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E	
			1	0x9C	

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N14P-GT 28nm	PU 10K	PD 15K	PU 45K	PD 5K	PD 25K	PU 5K	PD 45K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU		N14P-GT	N14P-GT1	
FB Memory (GDDR5)		ROM_SI	ROM_SI	
Samsung 3000MHz	K4G20325FD-FC03			
	64Mx32		PD 30K	
Hynix 3000MHz	H5GQ2H24AFR-R0C			
	64Mx32		PD 25K	
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24AFR-T2C			
	64Mx32	PD 25K		

Security Classification

LC Future Center Secret Data

Issued Date

2012/07/01

Deciphered Date

2014/07/01

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title

VGA Notes List

Size

Custom

Document Number

Y401 NW-A031

Date

Wednesday, March 27, 2013

Sheet

4

of

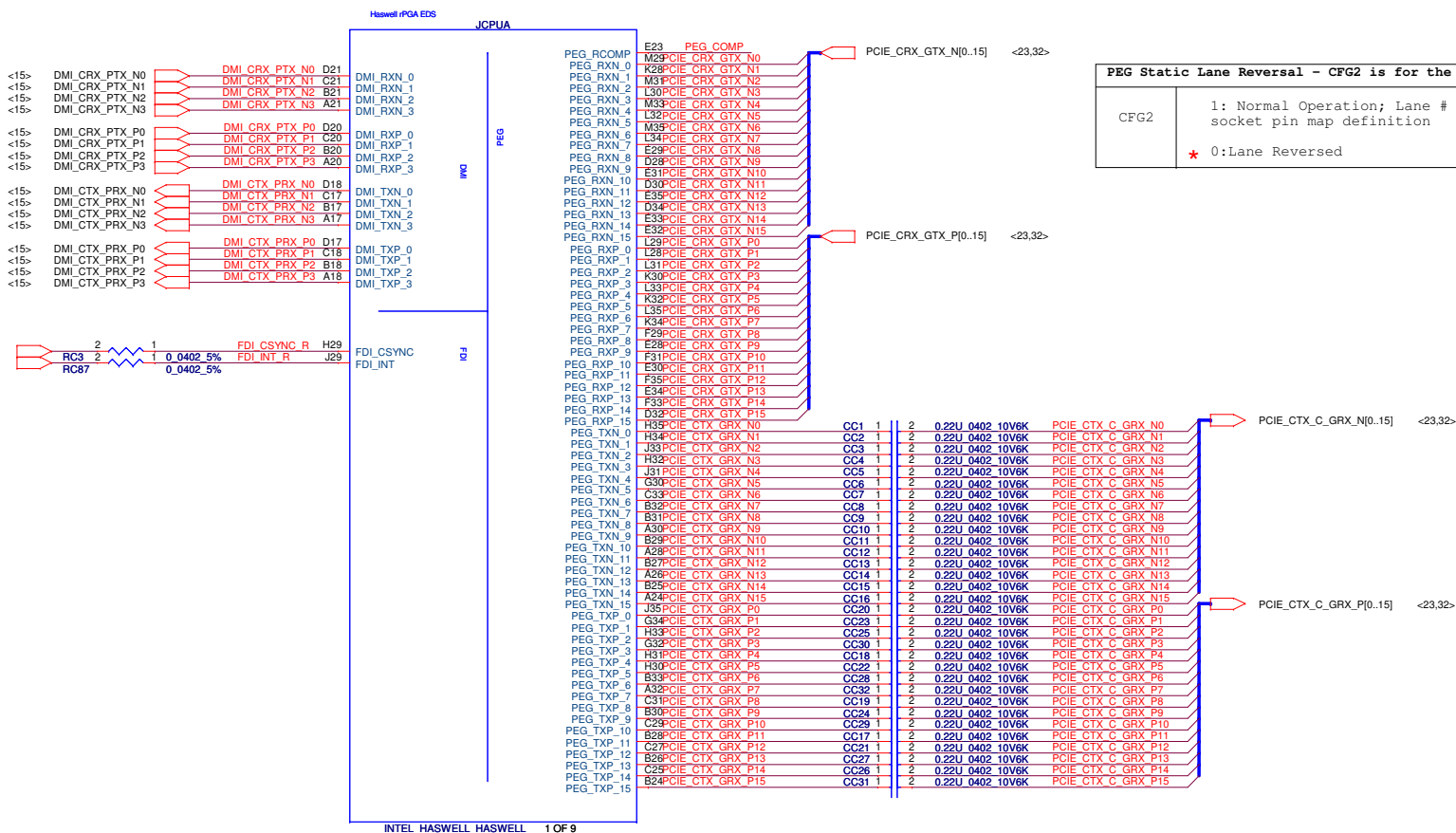
69

Rev


1.0

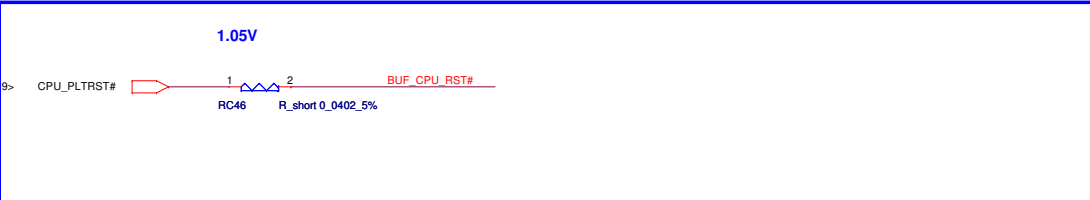
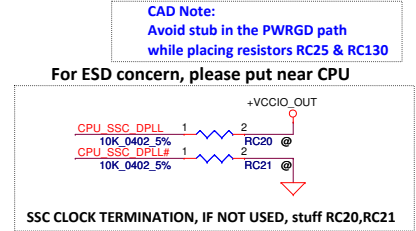
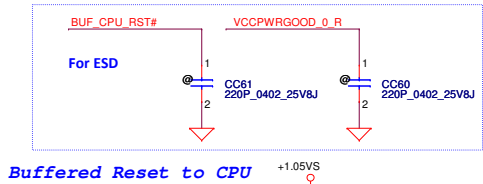
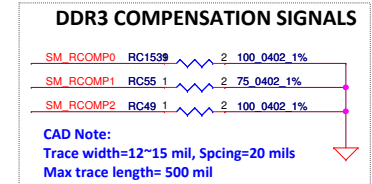
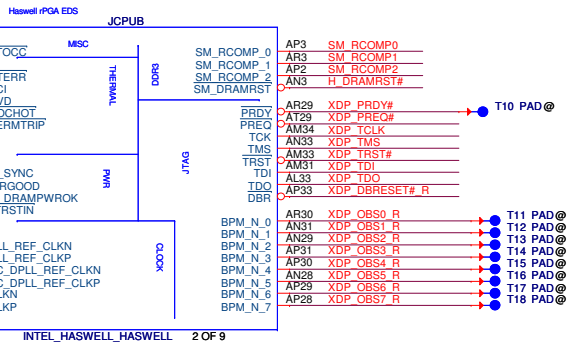
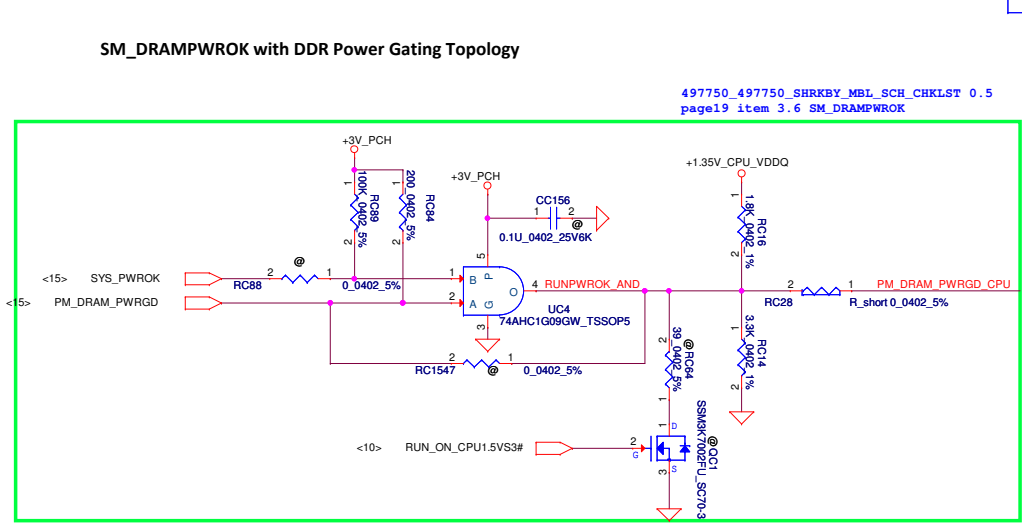
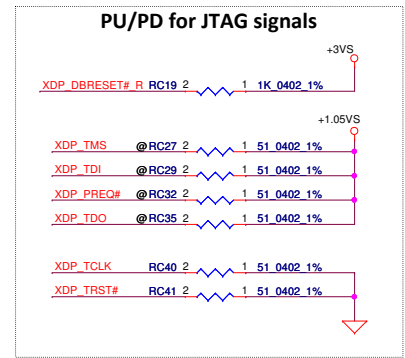
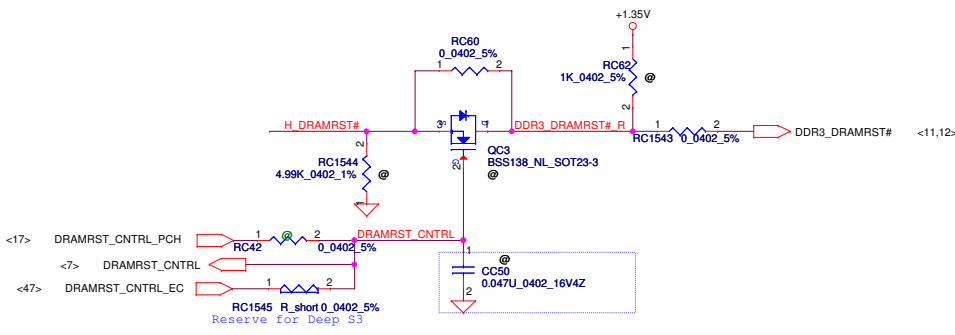


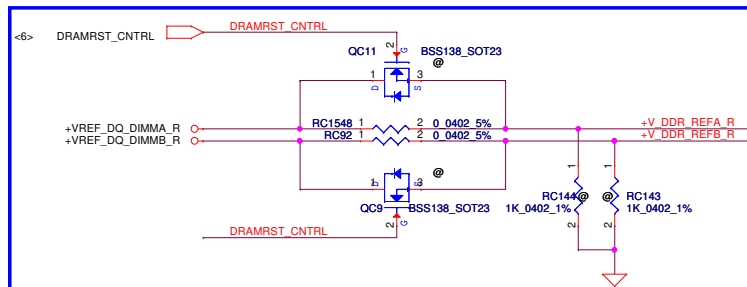
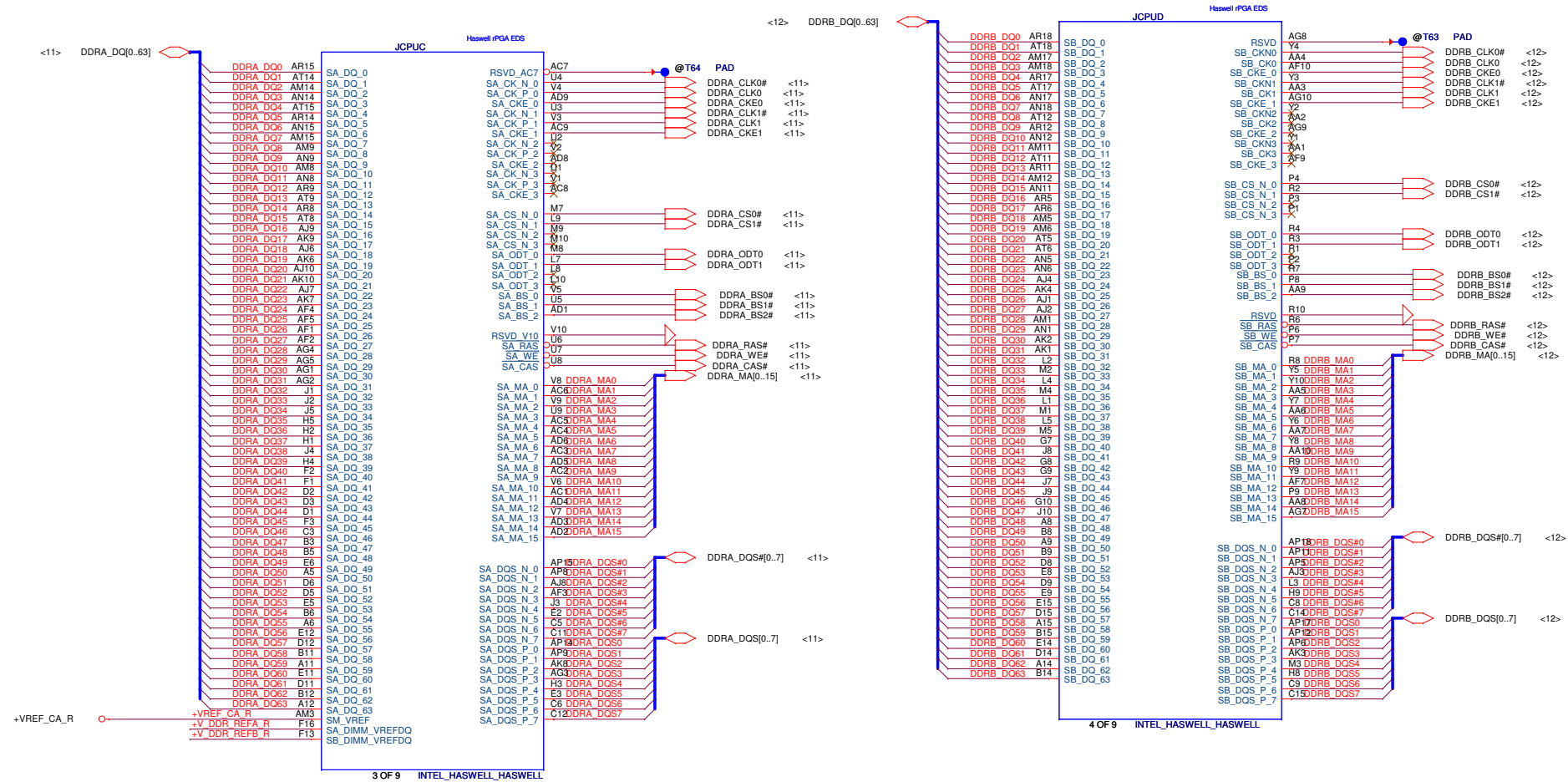
CAD Note:
Trace width=12 mils ,Spacing=15mils
Max length= 400 mils.



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	* 0: Lane Reversed

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	CPU (1/7) DMI, FDI, PEG		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					Size Custom	Document Number Y401 NW-A031
					Date: Wednesday, March 27, 2013	Sheet 5 of 69
					Rev 1.0	



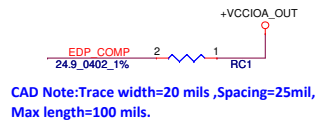


6/8: Add M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

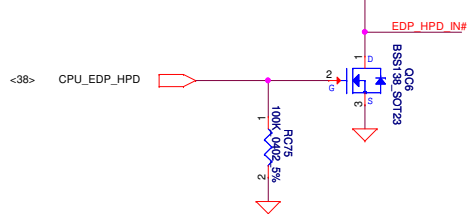
CFG STRAPS for CPU

check CLK item

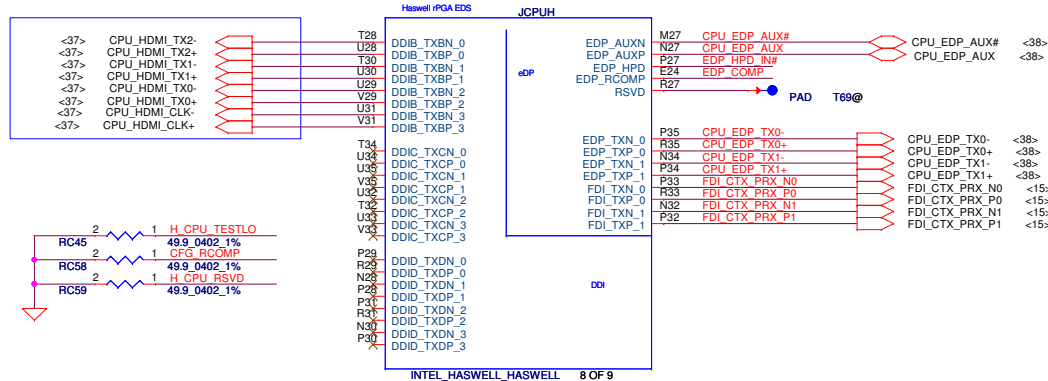
COMPENSATION PU FOR eDP



HPD INVERSION FOR EDP



20120829 VAI
Add net for add HDMI MUX



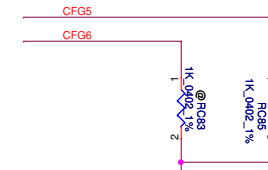
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	<p>★ 1: (Default) Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>
------	---



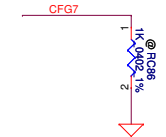
Display Port Presence Strap

CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>
------	---



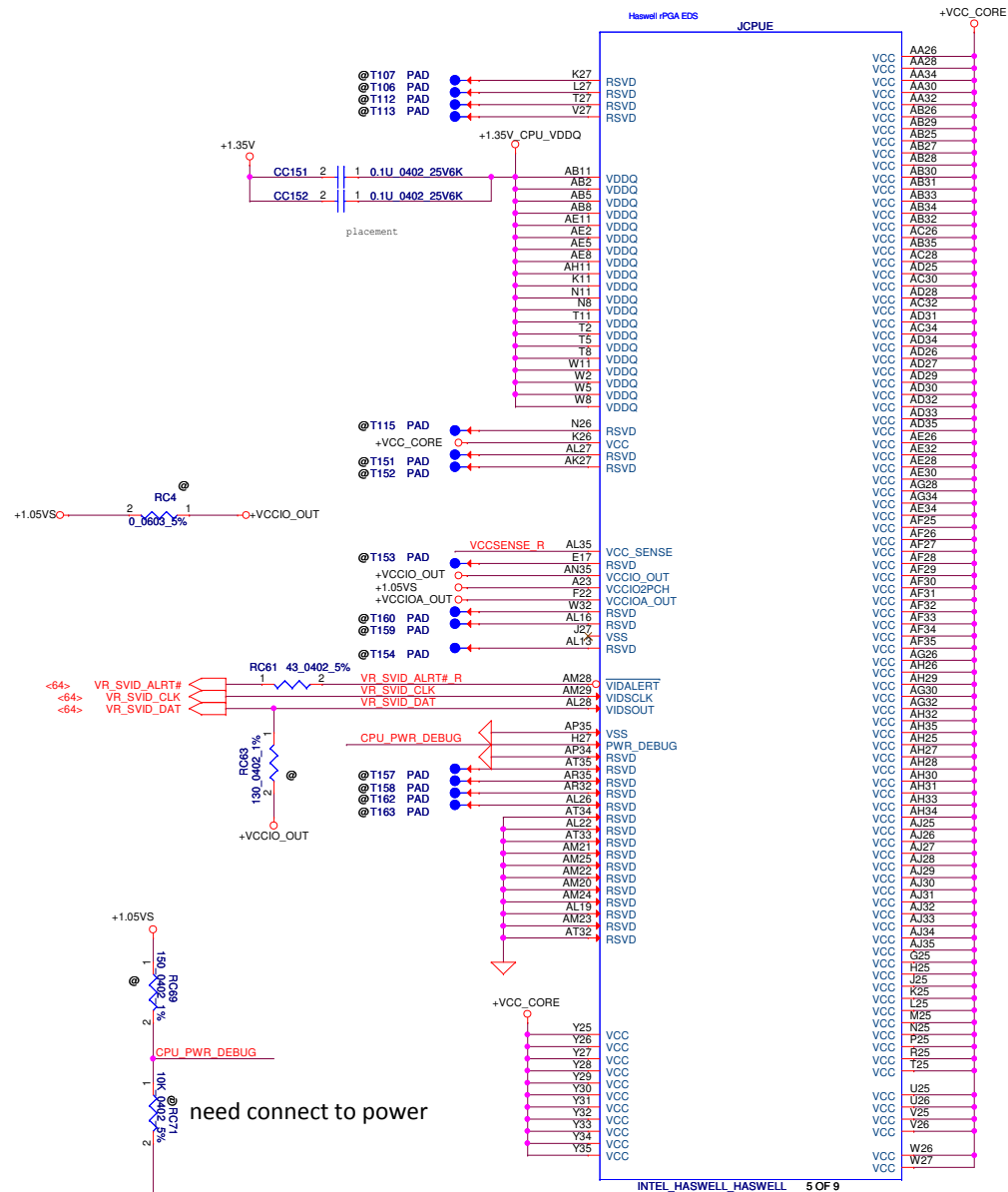
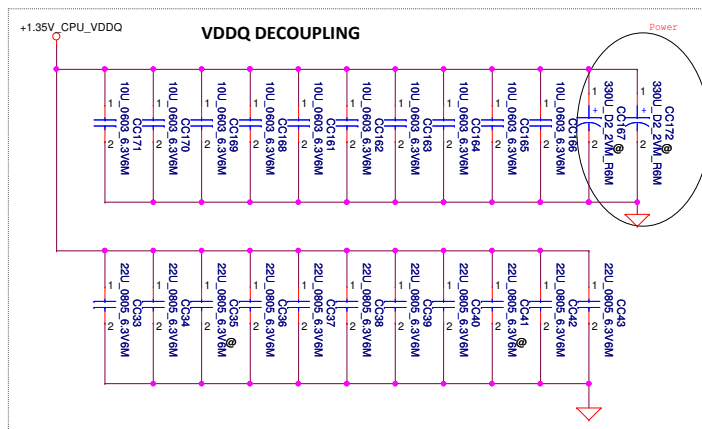
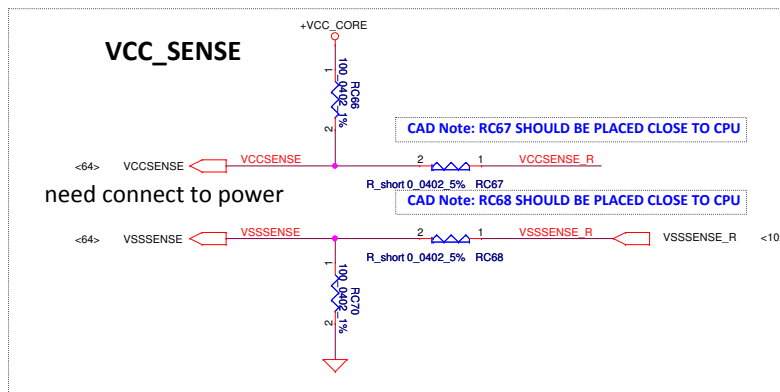
PCIe Port Bifurcation Straps

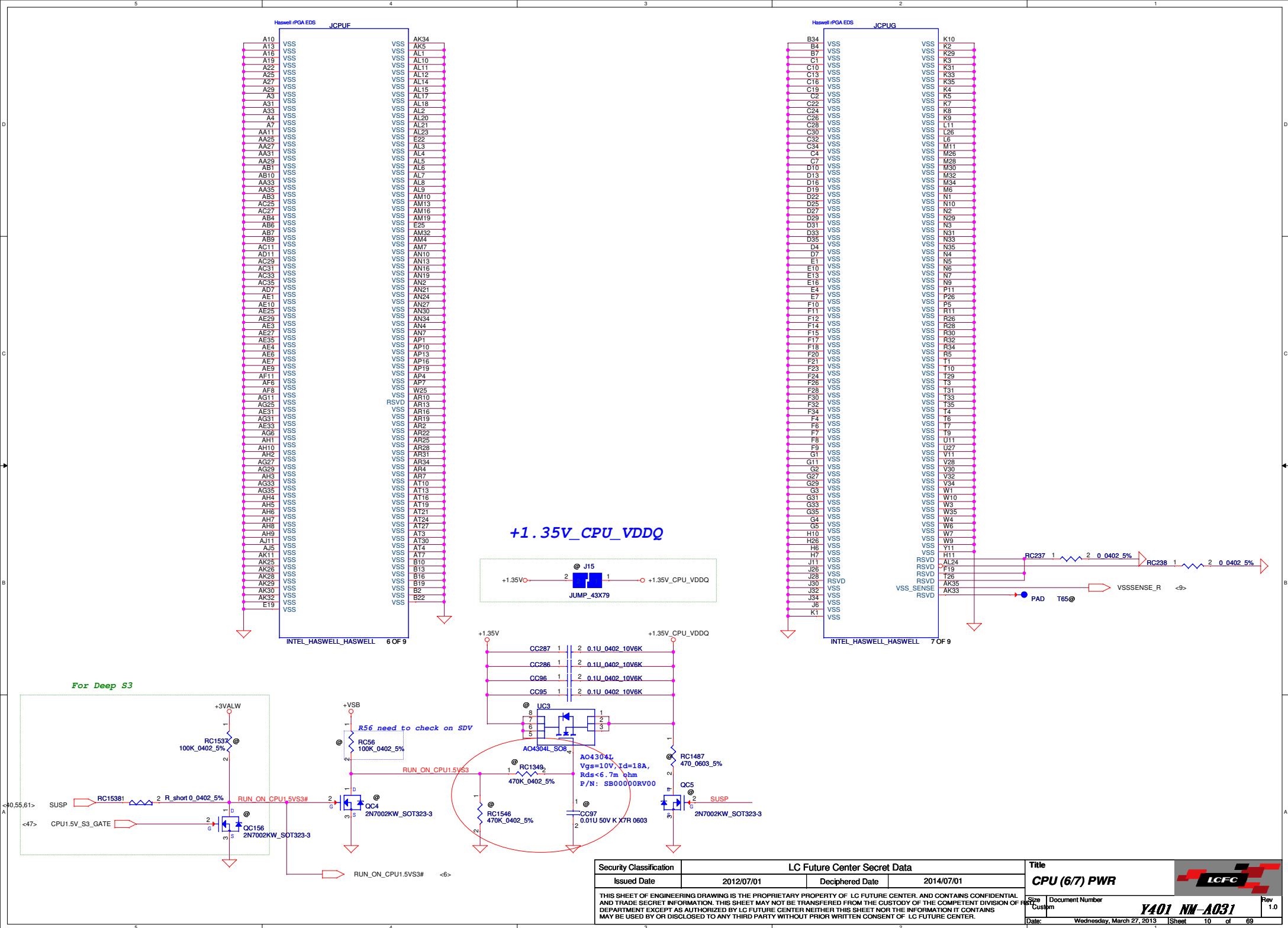
CFG[6:5]	<p>11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>★ 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>
----------	---



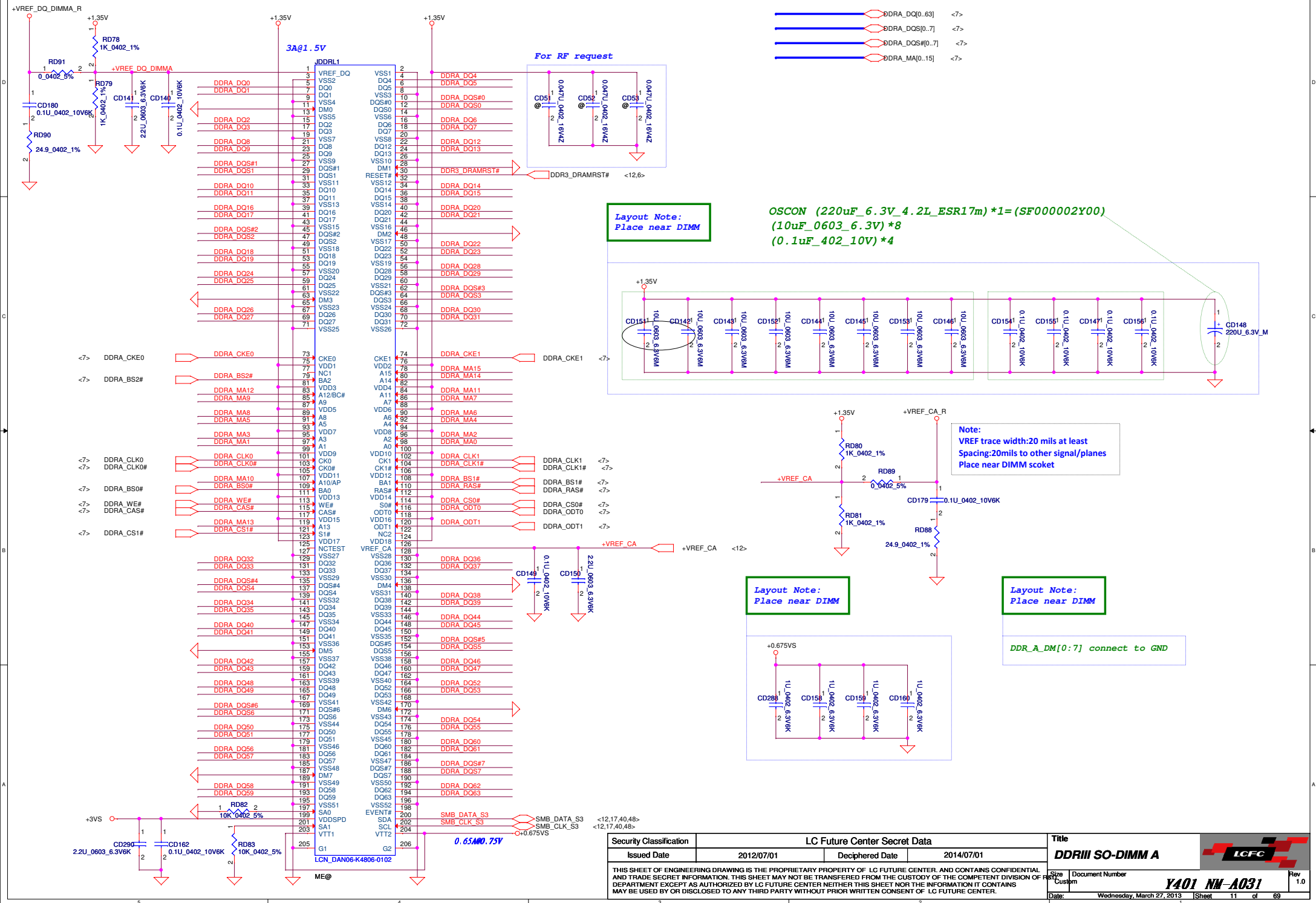
PEG DEFER TRAINING

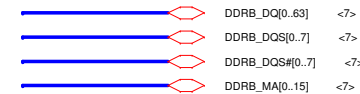
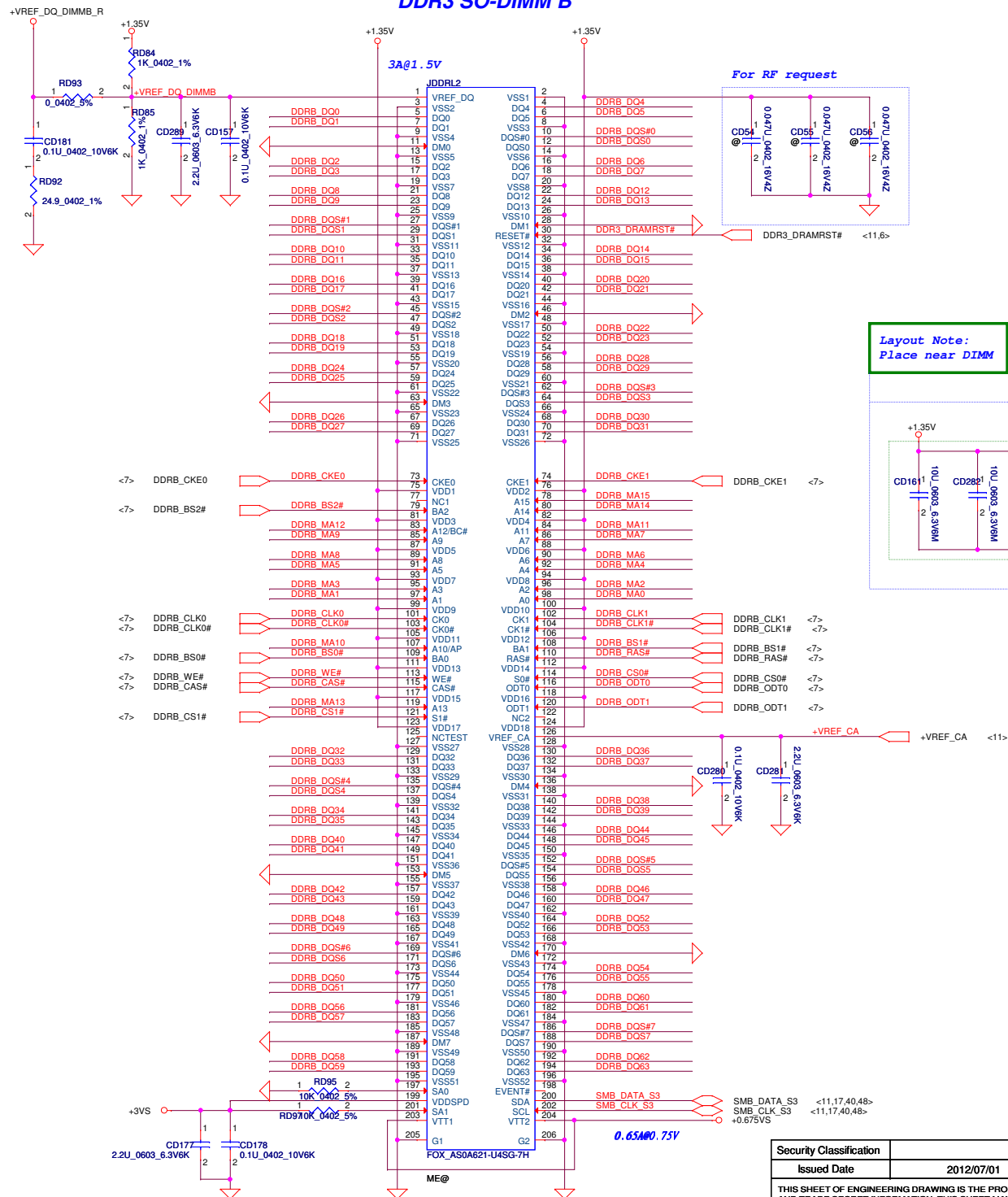
CFG7	<p>★ 1: (Default) PEG Train immediately following xRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>
------	---





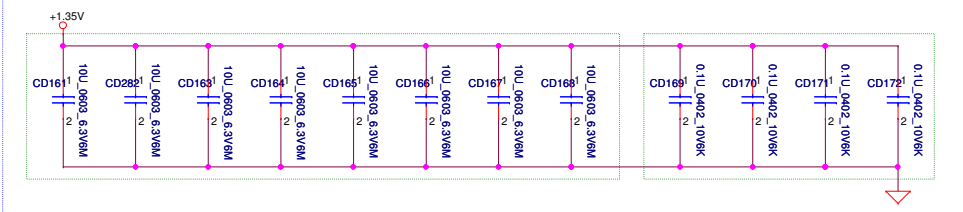
DDR3 SO-DIMM A



DDR3 SO-DIMM B

Layout Note:
Place near DIMM

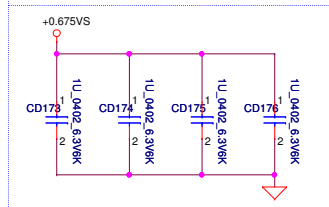
```
(10uF_0603_6.3V) *8  
(0.1uF_402_10V) *4
```



Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

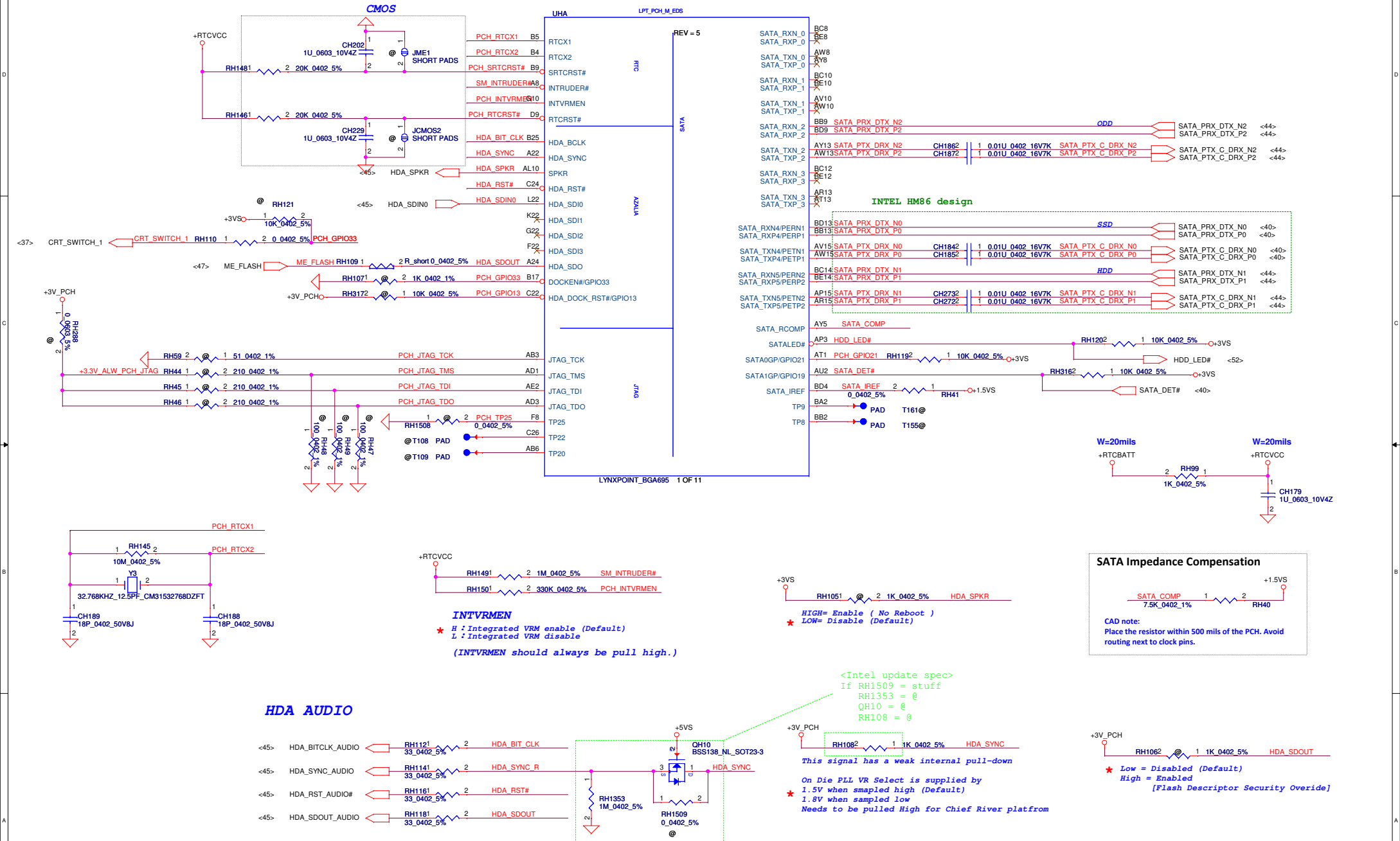
DDR_B_DM[0:7] connect to GND




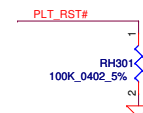
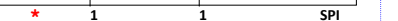
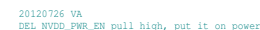
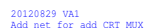
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>			


Title			
DDRIII SO-DIMM B			
Size Custom	Document Number	Y401 NM-A031	Rev 1.0
Date:	Wednesday, March 27 2013	13:47	12 - 1 - 20

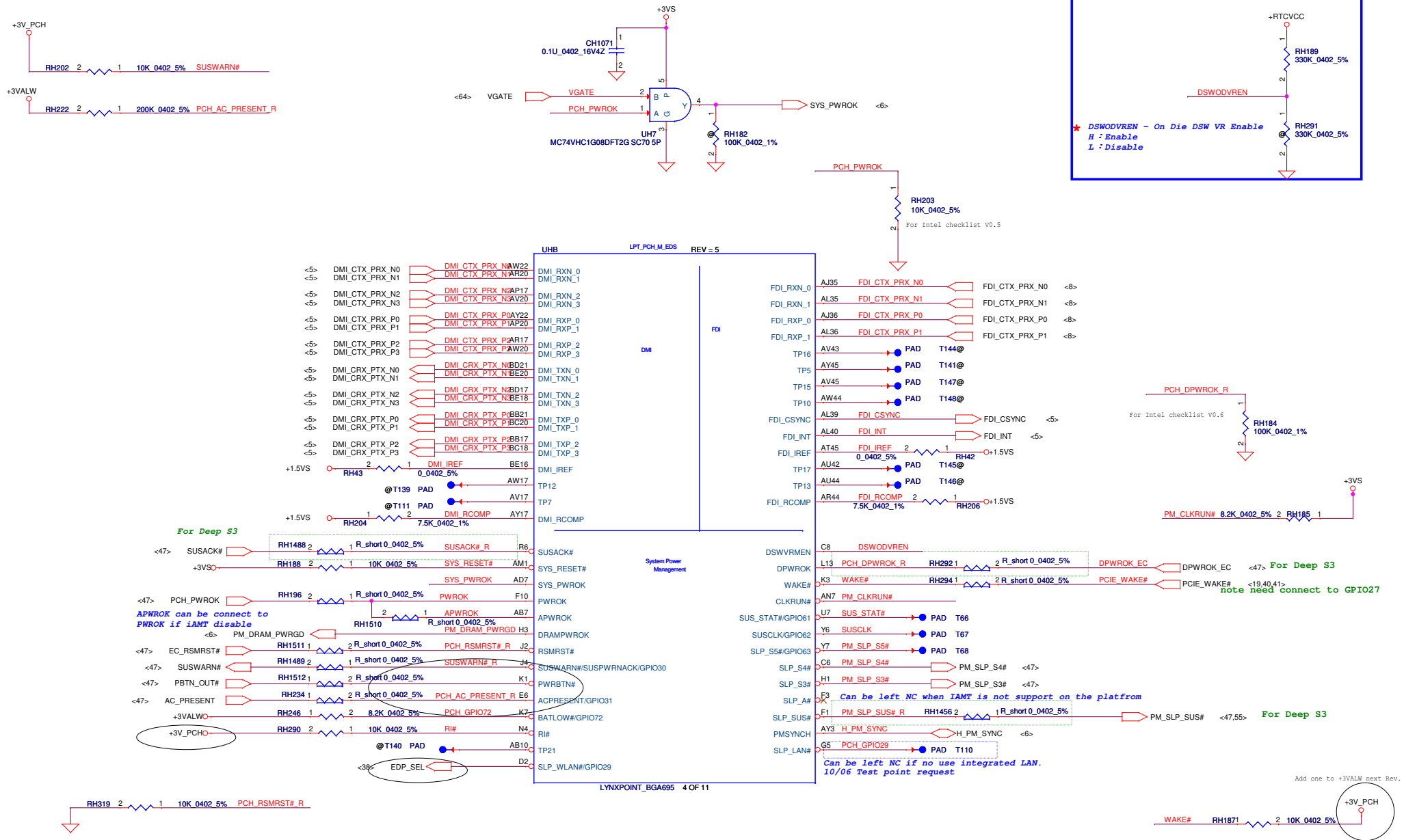
Place JUMPER under RAM door



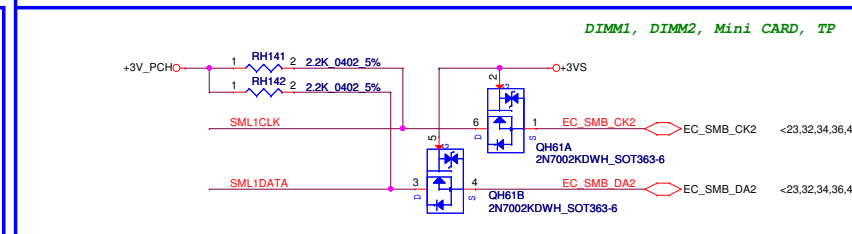
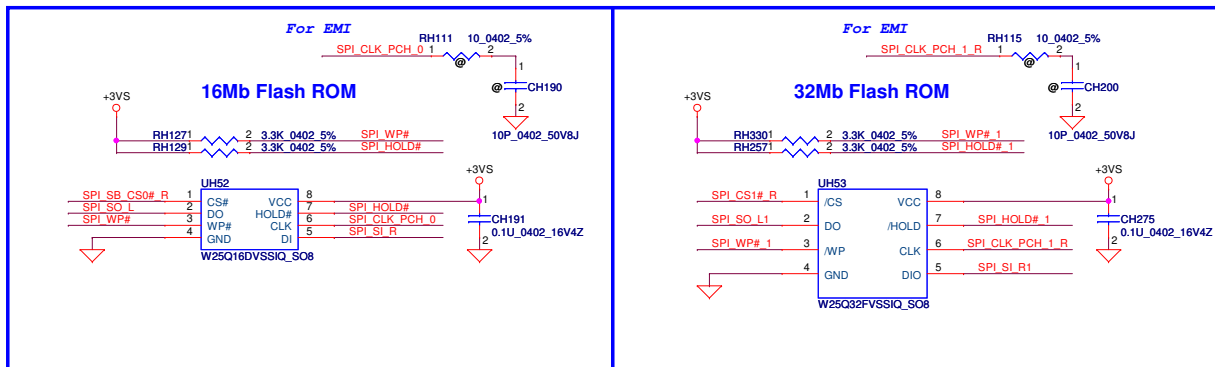
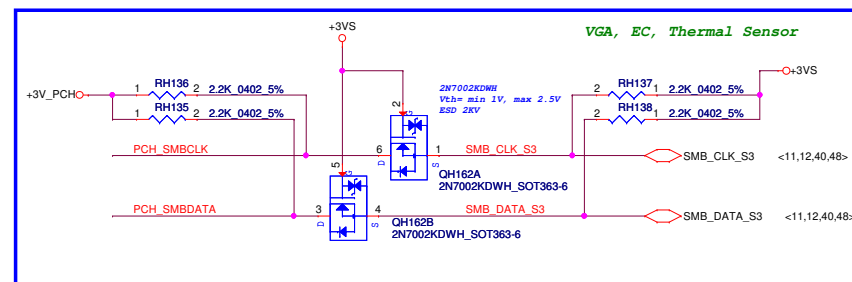
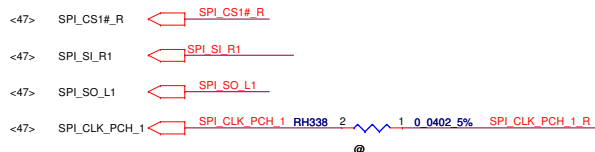
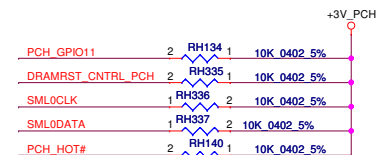
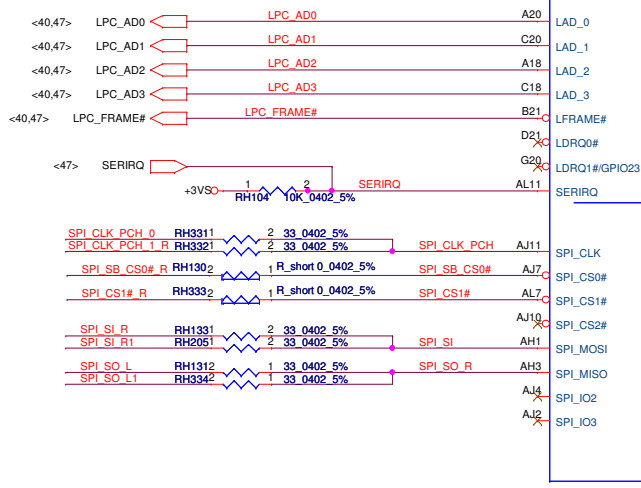
Security Classification		LC Future Center Secret Data		Title						
Issued Date		2012/07/01		Deciphered Date			2014/07/01		PCH (1/9) SATA,HDA,SPI, LPC	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FUTURE CENTER EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.							Size Custom	Document Number	Y401 NW-A031	Rev 1.0
Date:		Wednesday, March 27, 2013		Sheet		13		of 69		

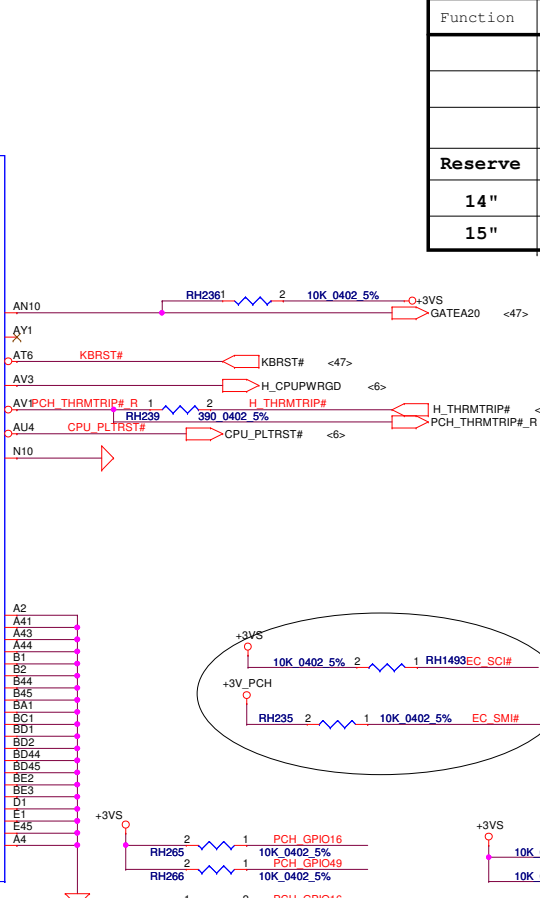


Title		PCH (2/9) PCIE, SMBUS, CLK			
Size	Document Number	Y401 NM-A031		Rev	1.0
Custom					
Date:	Wednesday, March 27, 2013	Time:	14:44	69	



EC and Mini card debug port





6b)

<23.32>

<16> PCH_GPIO67

PCH_GPIO38

PCH_GPIO67

PCH_GPIO70

+3V5

RH711 RH708 RH704

10K_0402_5% 10K_0402_5% 10K_0402_5%

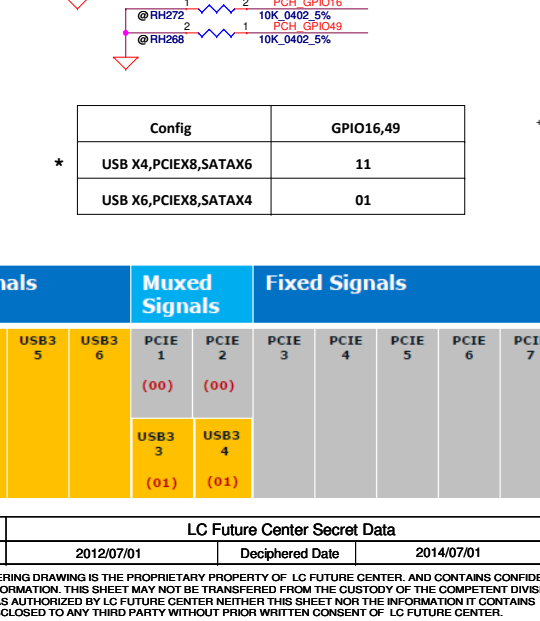
1 2 2


1 1 1


1 1 1



1 1 1


10K_0402_5% 10K_0402_5% 10K_0402_5%

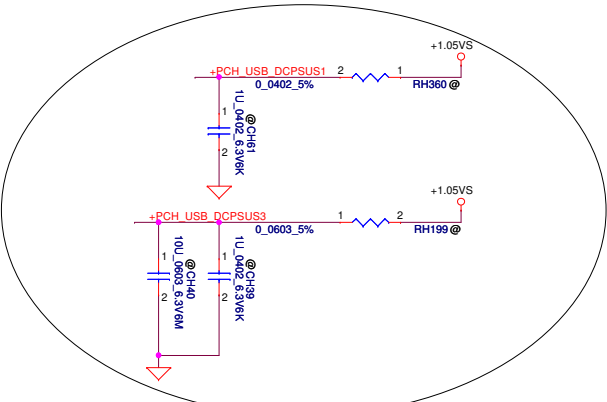



0402 5% 2  1 RH255 PCH_GPIO68

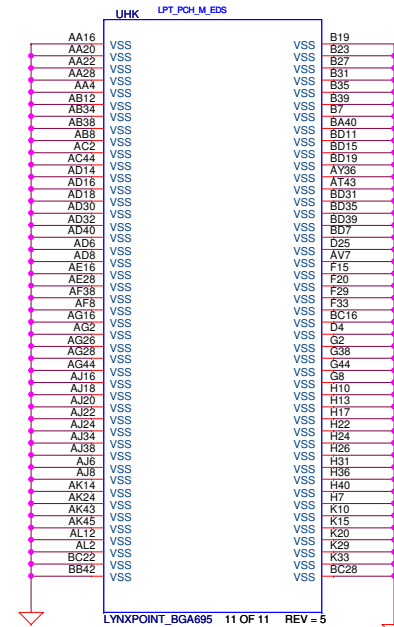
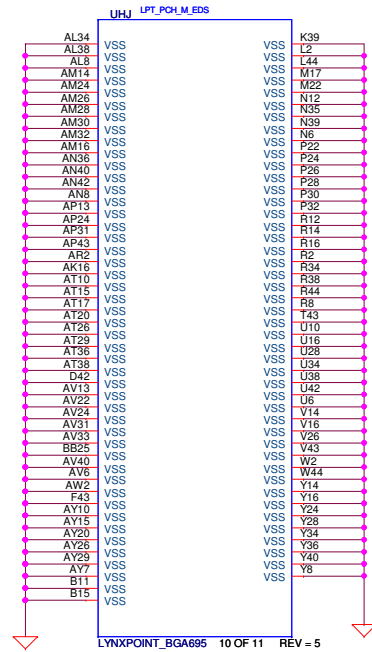
0402 5% 2  1 RH226 KBRST#

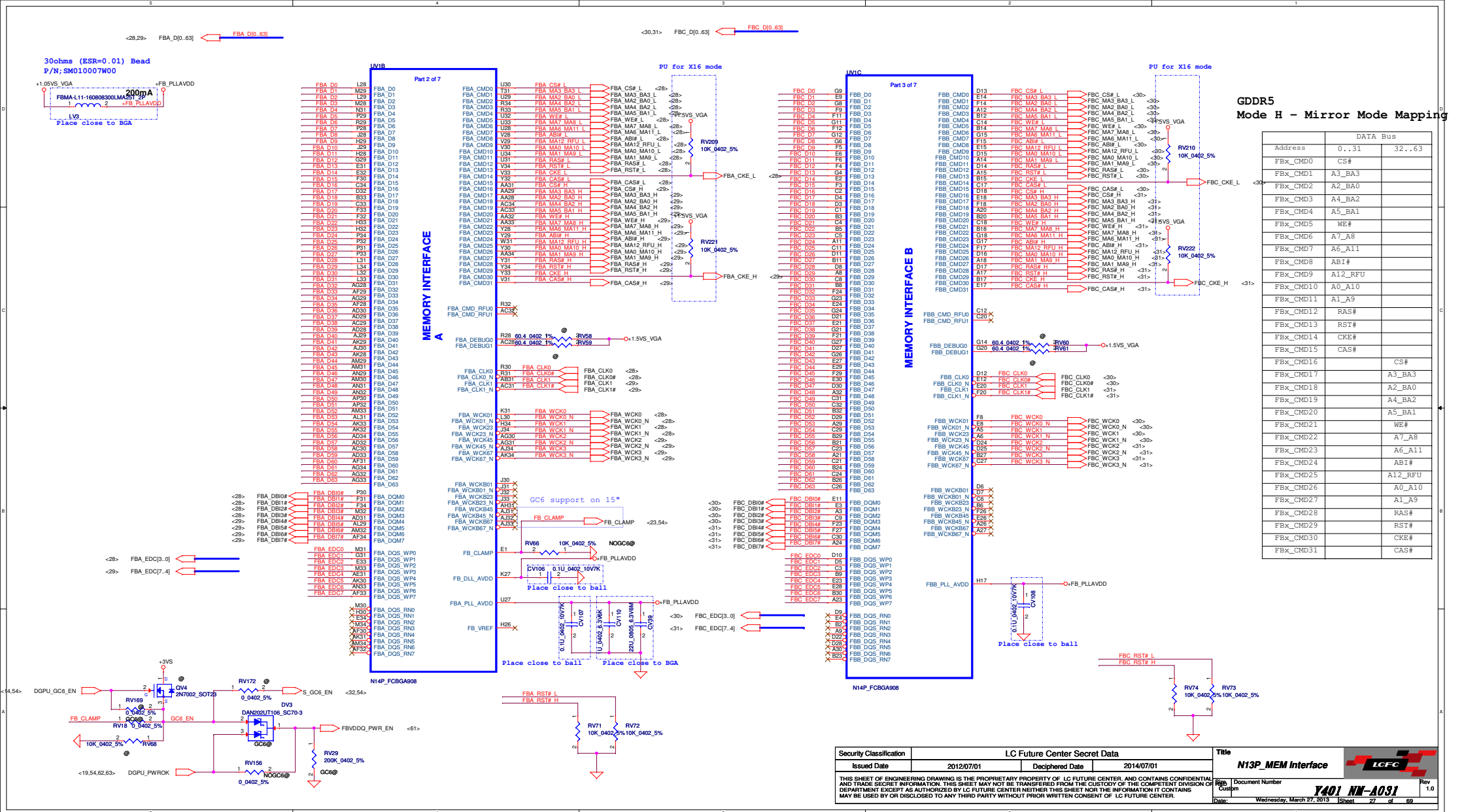
3VS

10K 0402 5% 2  1 RH1517 S_DGPU_PWR_EN

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	PCH (6/9) GPIO, CPU, MISC		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom	Document Number Y401 NW-A031	Rev 1.0
Date:				Wednesday, March 27, 2013	Sheet 19 of 69	

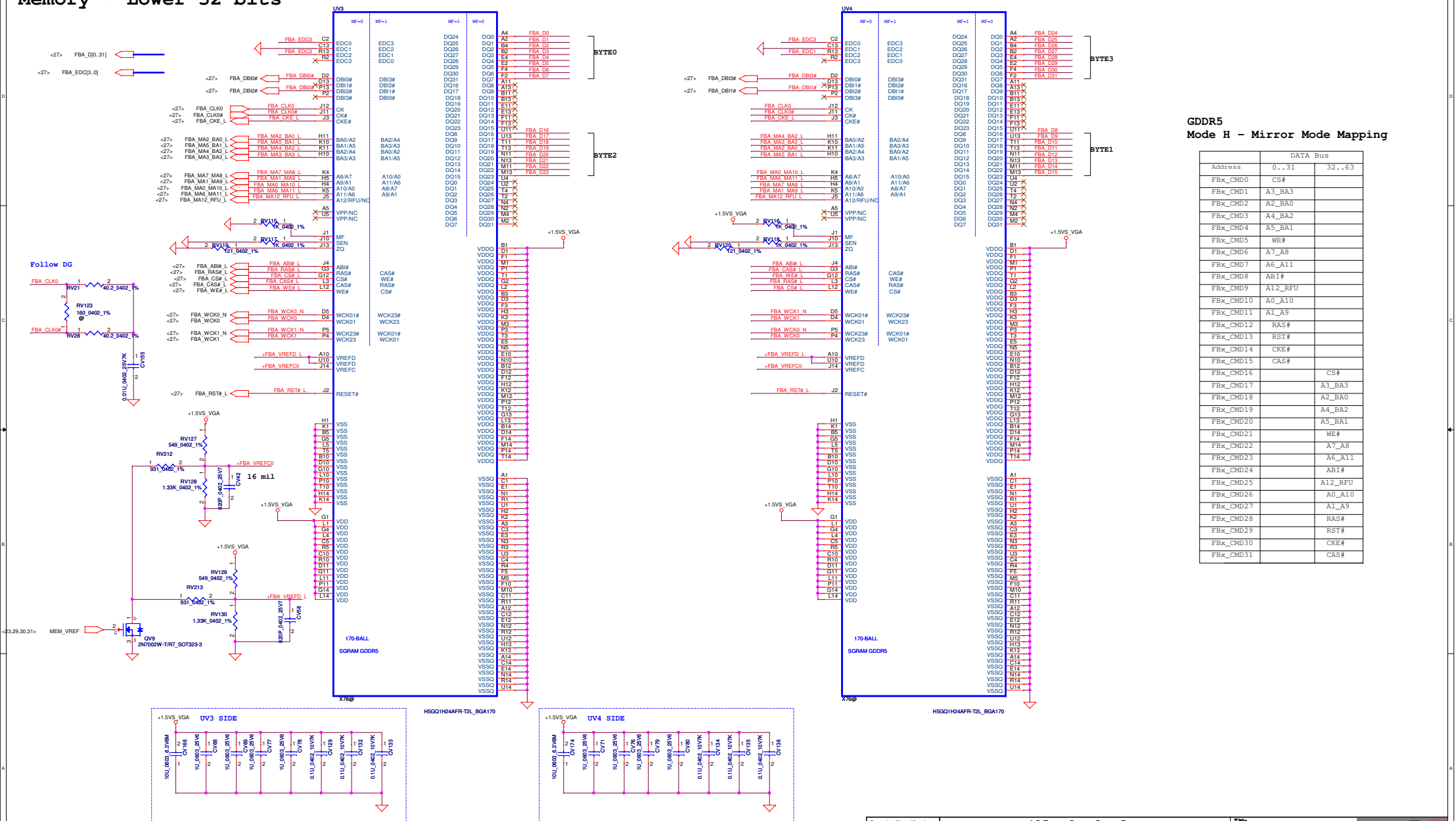


Security Classification	LC Future Center Secret Data			Title		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	PCH (7/9) PWR		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FST DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom	Document Number Y401 NW-A031	Rev 1.0
				Date:	Wednesday, March 27, 2013	Sheet 20 of 69






Memory - Lower 32 bits

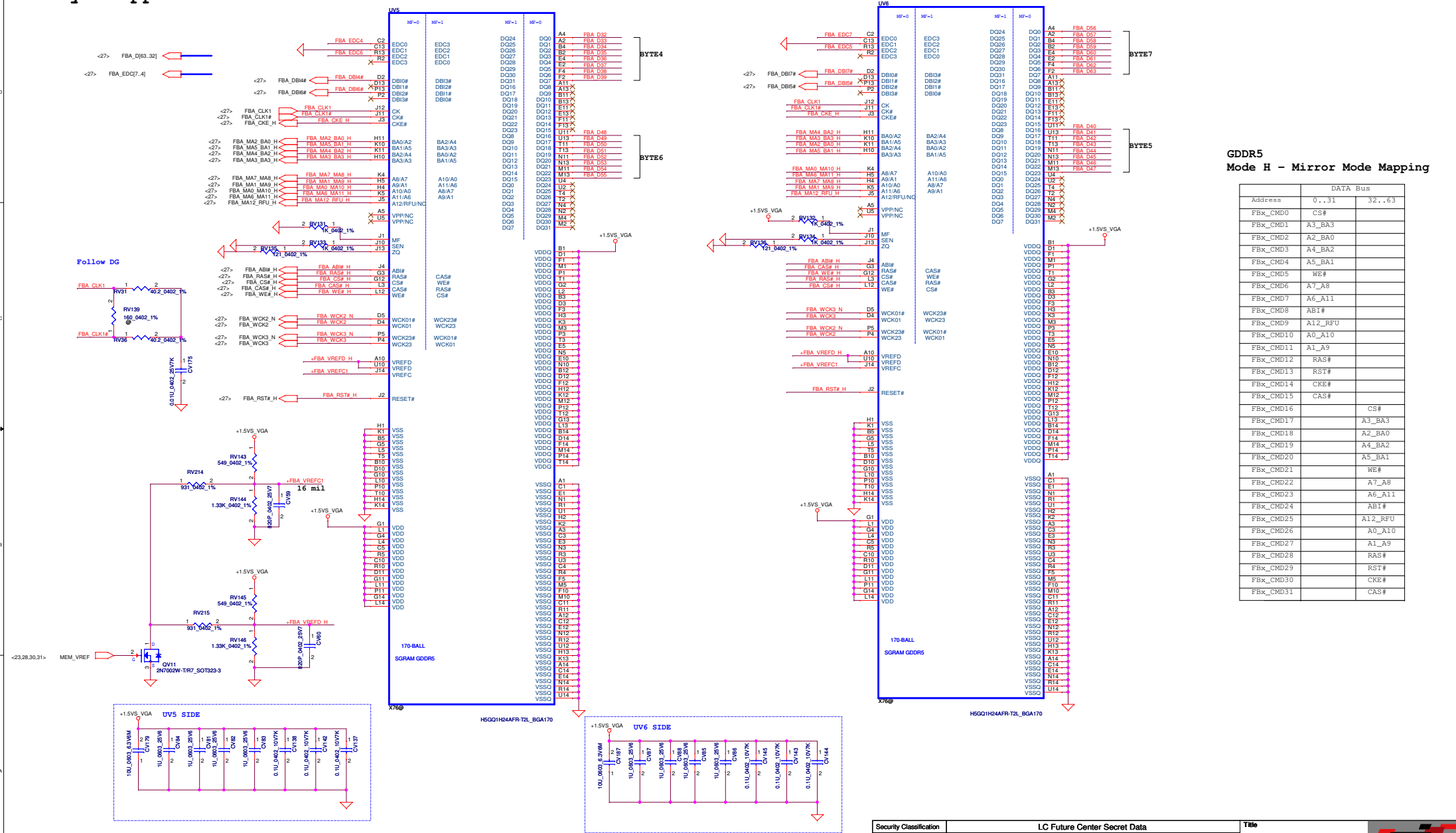


GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FbxCMD0	CS#	
FbxCMD1	A3_BA3	
FbxCMD2	A2_BA0	
FbxCMD3	A4_BA2	
FbxCMD4	A5_BA1	
FbxCMD5	WE#	
FbxCMD6	A7_A8	
FbxCMD7	A6_A11	
FbxCMD8	AB1#	
FbxCMD9	A12_RFU	
FbxCMD10	A0_A10	
FbxCMD11	A1_A9	
FbxCMD12	RAS#	
FbxCMD13	RST#	
FbxCMD14	CKE#	
FbxCMD15	CAS#	
FbxCMD16		CS#
FbxCMD17		A3_BA3
FbxCMD18		A2_BA0
FbxCMD19		A4_BA2
FbxCMD20		A5_BA1
FbxCMD21		WE#
FbxCMD22		A7_A8
FbxCMD23		A6_A11
FbxCMD24		AB1#
FbxCMD25		A12_RFU
FbxCMD26		A0_A10
FbxCMD27		A1_A9
FbxCMD28		RAS#
FbxCMD29		RST#
FbxCMD30		CKE#
FbxCMD31		CAS#


Security Classification	LC Future Center Secret Data			Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	N13P_GDDR5_A Lower	
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF P&D DEPARTMENT OF THE ARMY WITHOUT BEING AUTHORIZED BY LC FUTURE CENTER. THE INFORMATION CONTAINED HEREIN MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom	Rev 1.0
				Drawing Number 7401 NW-A031	
				Date Wednesday, March 27, 2013	Sheet 28 of 69

Memory - Upper 32 bits

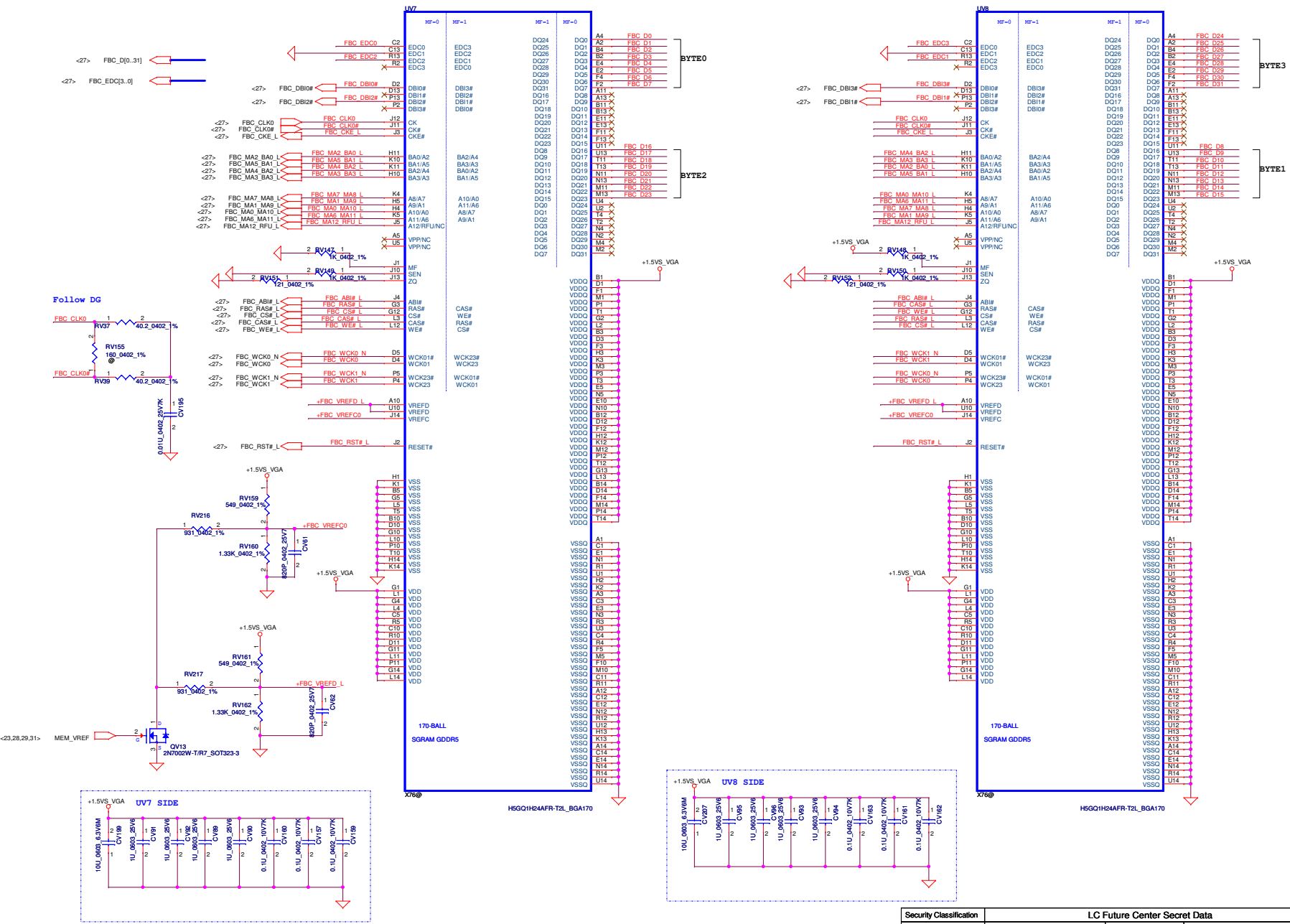


GDDR5
Mode H - Mirror Mode Mapping

DATA Bus		
Address	0...31	32...63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	AB1#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		AB1#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification			LC Future Center Secret Data			Title			
Issued Date		2012/07/01		Deciphered Date		2014/07/01		N13P_GDDR5_A Upper	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D TO ANY OTHER DEPARTMENT OR AUTHORIZED BY LC FUTURE CENTER. THE INFORMATION CONTAINED HEREIN IS UNCLASSIFIED AND MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.								Document Number Y401 NM-A031	
								Revision 1.0	

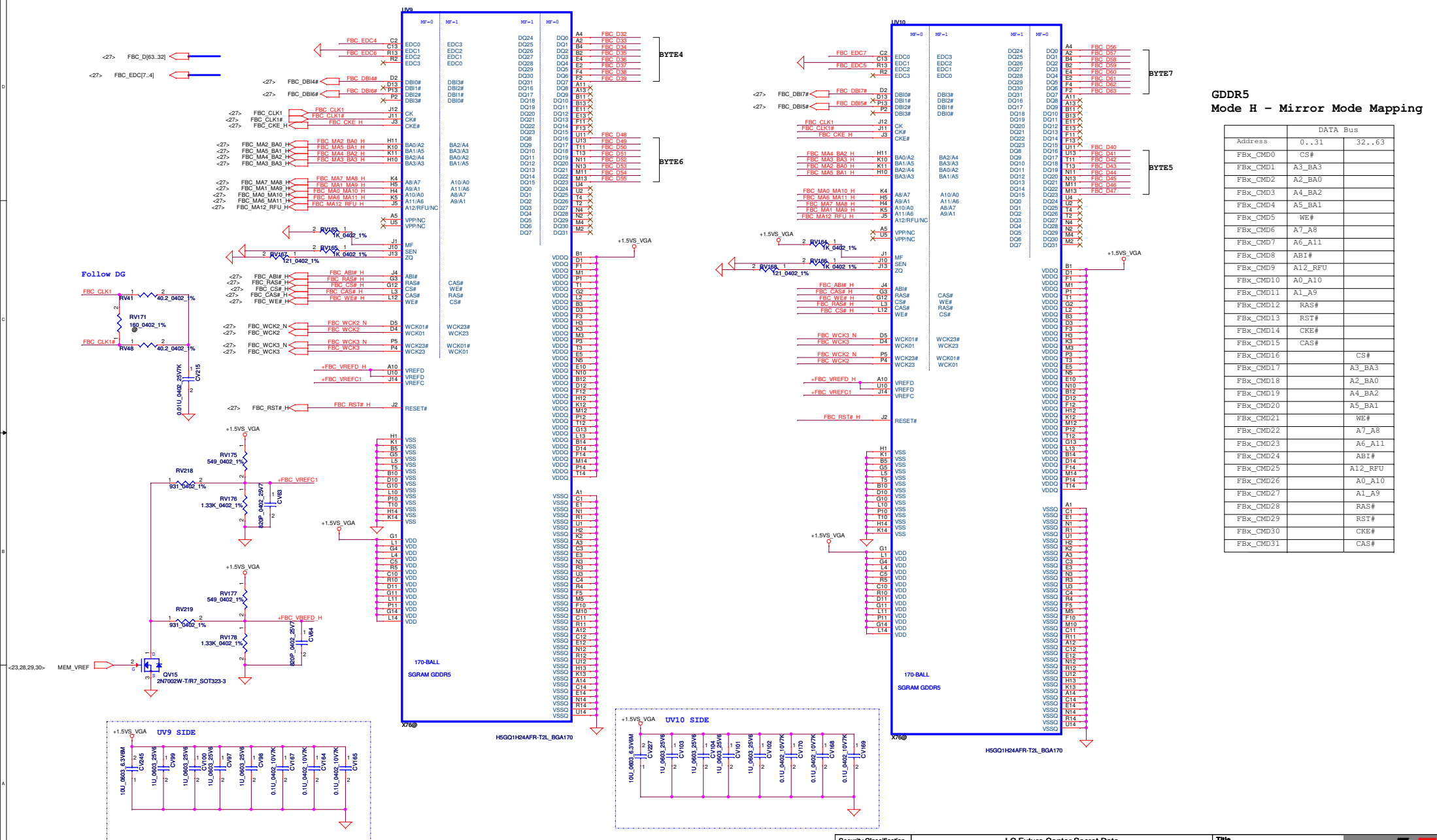
Memory Partition C - Lower 32 bits



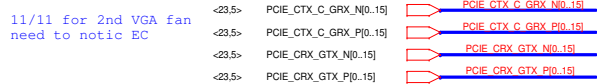
GDDR5 Mode H - Mirror Mode Mapping


DATA Bus	
Address	0..31 32..63
FBX_CMD0	CS#
FBX_CMD1	A3_BA3
FBX_CMD2	A2_BA0
FBX_CMD3	A4_BA2
FBX_CMD4	A5_BA1
FBX_CMD5	WE#
FBX_CMD6	A7_A8
FBX_CMD7	A6_A11
FBX_CMD8	AB1#
FBX_CMD9	A12_RFU
FBX_CMD10	A0_A10
FBX_CMD11	A1_A9
FBX_CMD12	RAS#
FBX_CMD13	RST#
FBX_CMD14	CKE#
FBX_CMD15	CAS#
FBX_CMD16	
FBX_CMD17	A3_BA3
FBX_CMD18	A2_BA0
FBX_CMD19	A4_BA2
FBX_CMD20	A5_BA1
FBX_CMD21	WE#
FBX_CMD22	A7_A8
FBX_CMD23	A6_A11
FBX_CMD24	AB1#
FBX_CMD25	A12_RFU
FBX_CMD26	A0_A10
FBX_CMD27	A1_A9
FBX_CMD28	RAS#
FBX_CMD29	RST#
FBX_CMD30	CKE#
FBX_CMD31	CAS#

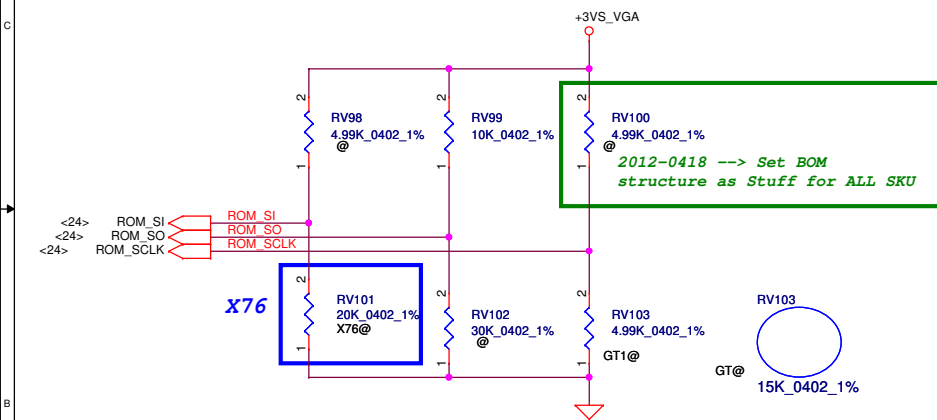
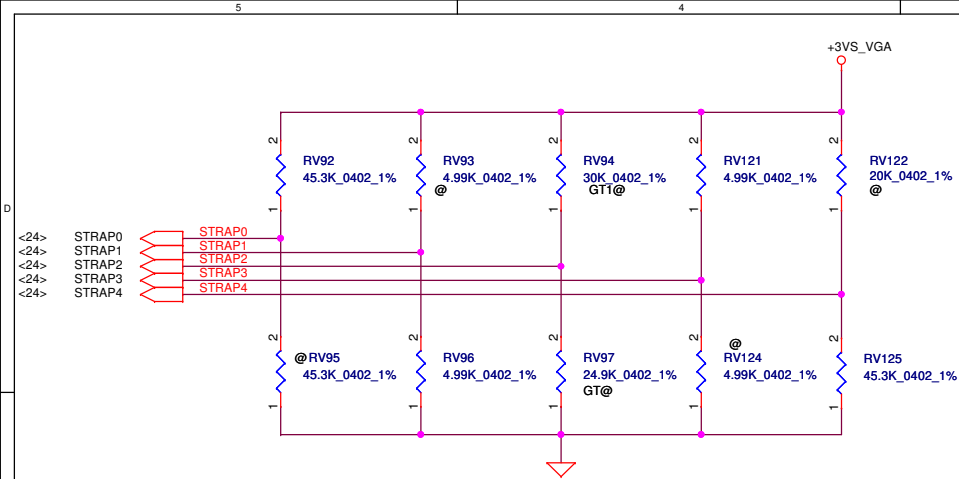
Memory Partition C - Upper 32 bits



	DATA Bus	
Address	0..31	32..63
FBX_CMD0	CS#	
FBX_CMD1	A3_BA3	
FBX_CMD2	A2_BA0	
FBX_CMD3	A4_BA2	
FBX_CMD4	A5_BA1	
FBX_CMD5	WE#	
FBX_CMD6	A7_A8	
FBX_CMD7	A6_A11	
FBX_CMD8	ABI#	
FBX_CMD9	A12_RFU	
FBX_CMD10	A0_A10	
FBX_CMD11	A1_A9	
FBX_CMD12	RAS#	
FBX_CMD13	RST#	
FBX_CMD14	CKE#	
FBX_CMD15	CAS#	
FBX_CMD16		CS#
FBX_CMD17		A3_BA3
FBX_CMD18		A2_BA0
FBX_CMD19		A4_BA2
FBX_CMD20		A5_BA1
FBX_CMD21		WE#
FBX_CMD22		A7_A8
FBX_CMD23		A6_A11
FBX_CMD24		ABI#
FBX_CMD25		A12_RFU
FBX_CMD26		A0_A10
FBX_CMD27		A1_A9
FBX_CMD28		RAS#
FBX_CMD29		RST#
FBX_CMD30		CKE#
FBX_CMD31		CAS#



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	VGA MXM	
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>					
				<p>Size Document Number</p> <p>Custm Y401 NW-A031</p> <p>Rev 1.0</p>	
				<p>Date: Wednesday, March 27, 2013 Sheet 32 of 69</p>	



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0000	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

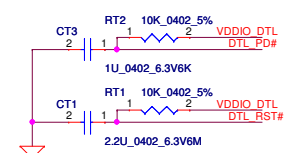
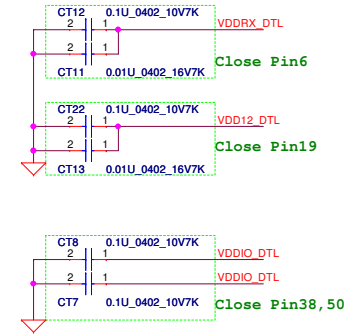
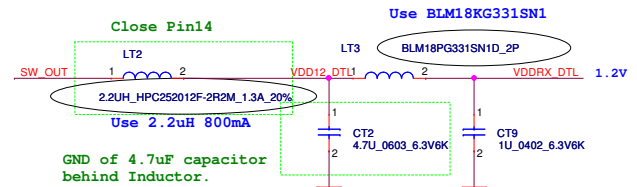
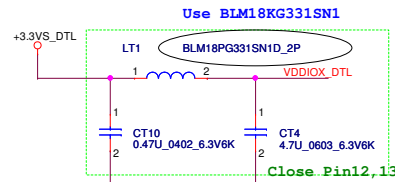
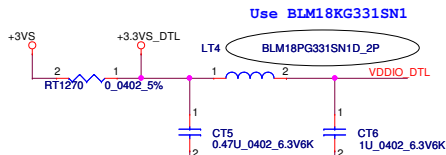
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

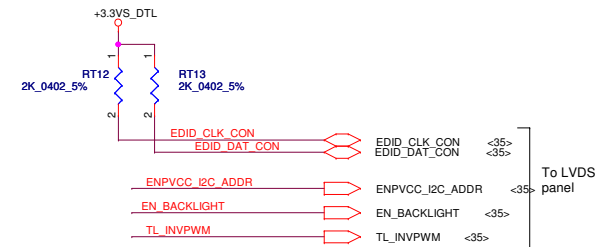
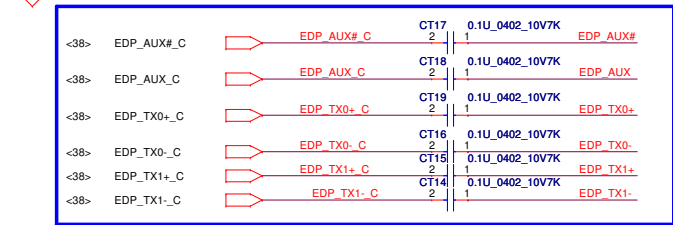
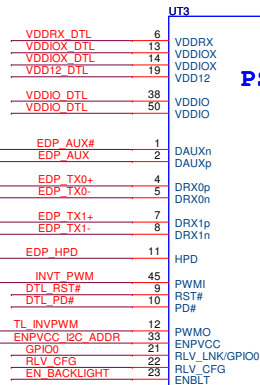
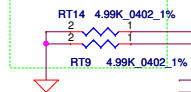
X76											
GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	Samsung	K4G20325FD-FC04 2G 64Mx32	PD 30K	PU 10K	PD15K (ALL SKU)	PU 45K	PD 5K	PD 25K	PU 5K	PD 45K	
		K4G20325FD-FC03 2G 64Mx32	PD 30K								
	Hynix										
		H5GQ2H24AFR-R0C 2G 64Mx32	PD 25K								
		H5GQ2H24AFR-T2C 2G 64Mx32	PD 25K								

VRAM	X76	VRAM P/N
Samsung	X7600412001 (2G 64Mx32)	SA00005B71J
Hynix	X7600412002 (2G 64Mx32)	SA00004GD2J

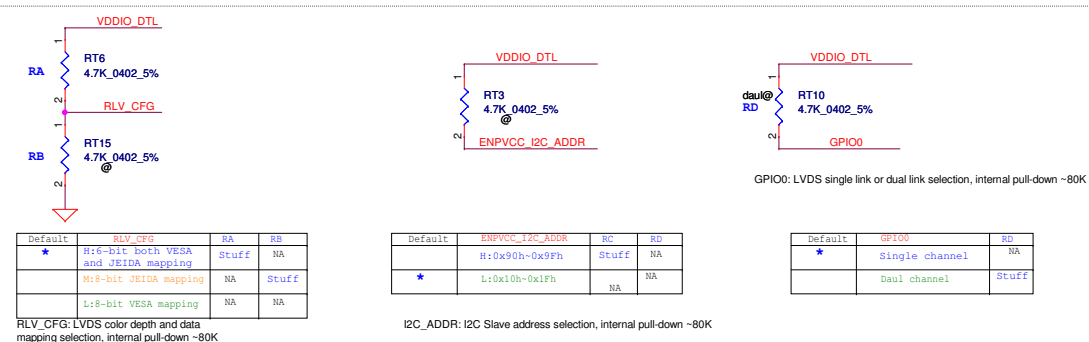
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	N13P_MISC
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom
				Document Number Y401 NM-A031
				Date: Wednesday, March 27, 2013
				Sheet 33 of 69



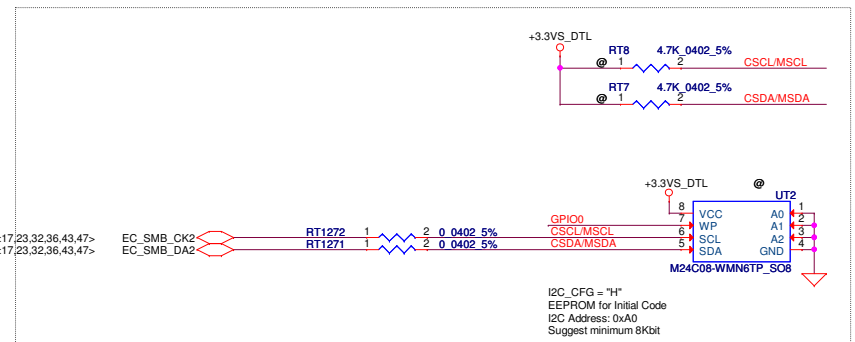
No: LVDS output swing control
4.99K for default swing, change the value for swing adjust

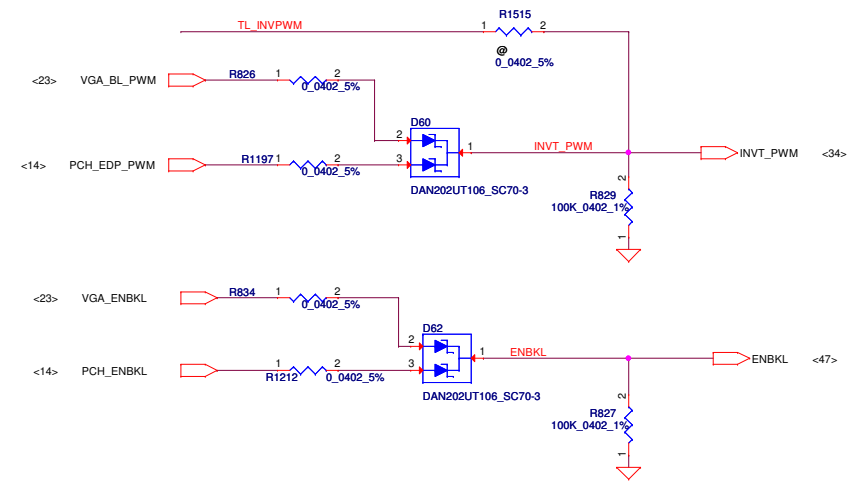
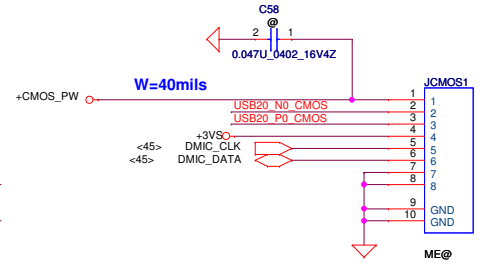
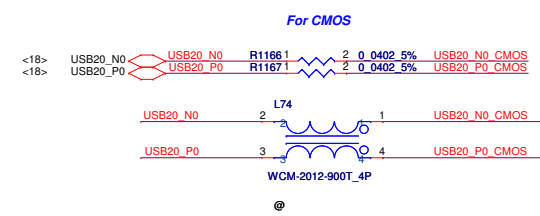
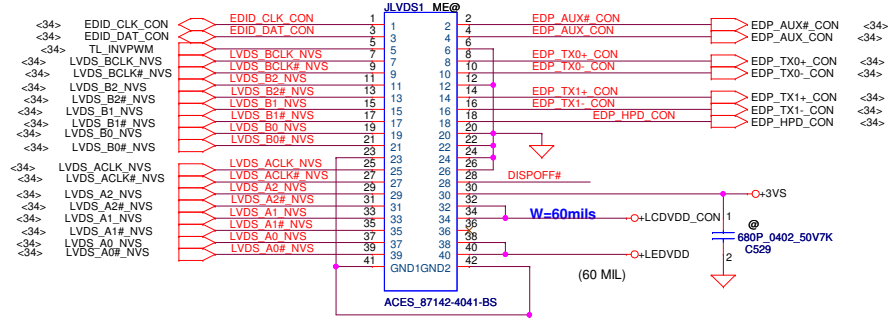
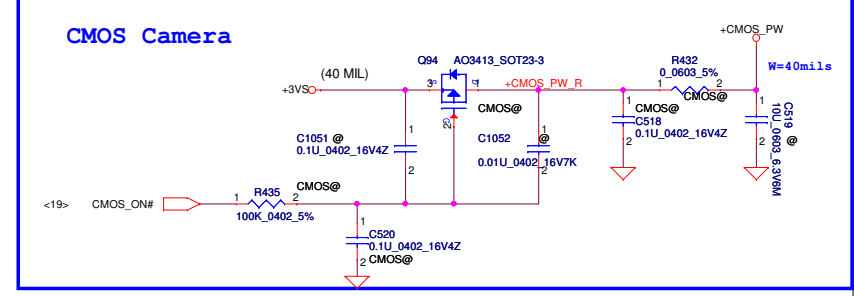
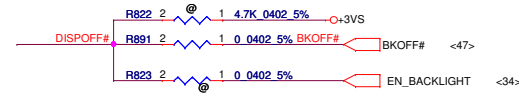
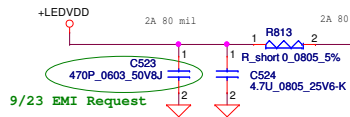


Power On Configuration

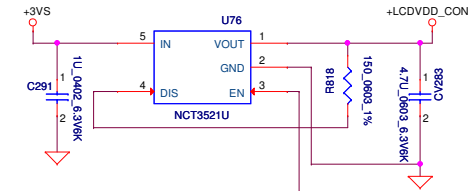


Initial Code EEPROM

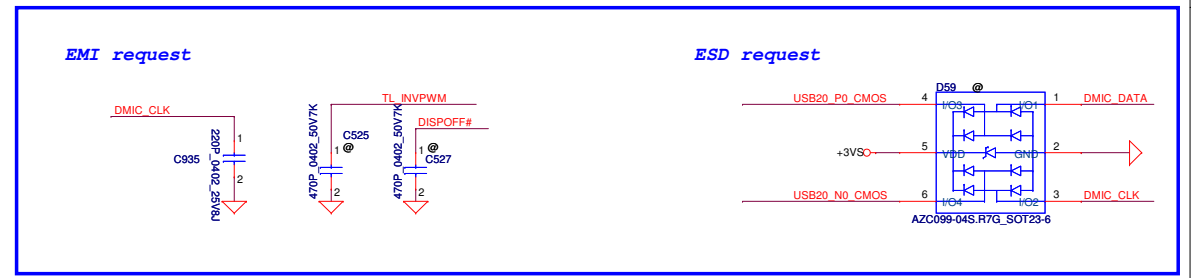
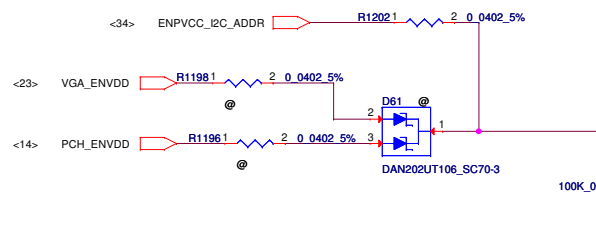





LCDVDD

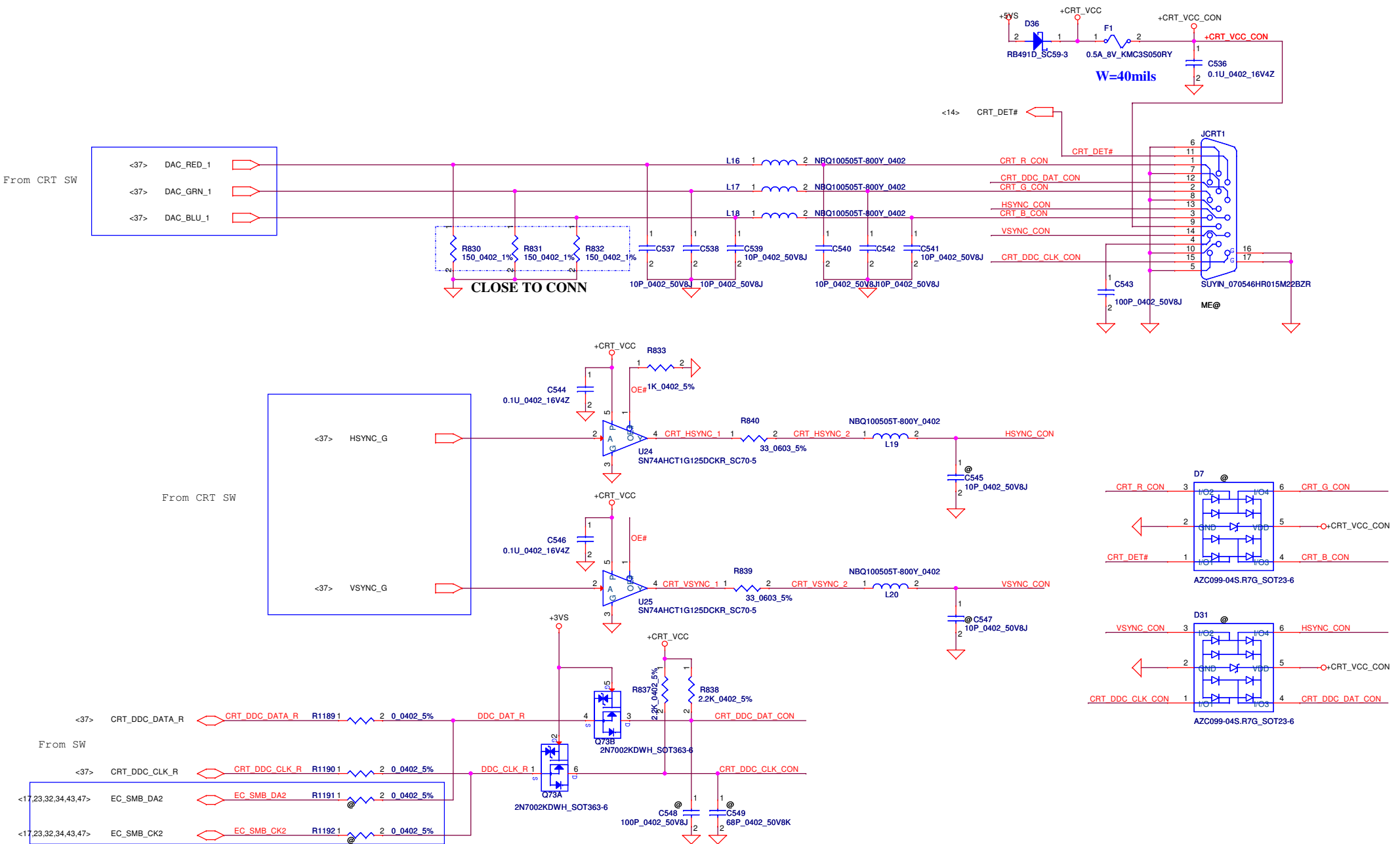



LCDVDD



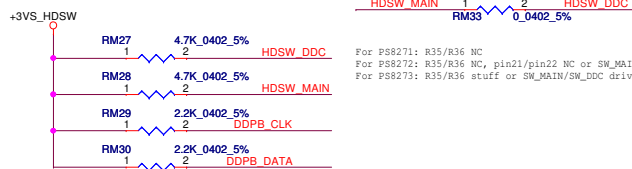
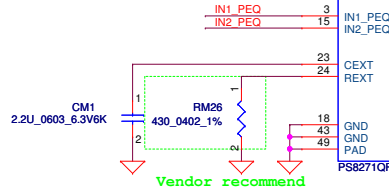
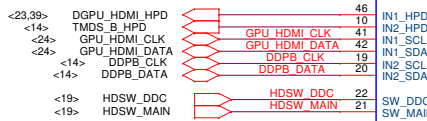
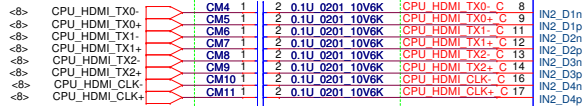
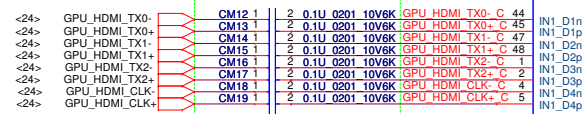
Security Classification		LC Future Center Secret Data		Title			
Issued Date	2012/07/01	Deciphered Date	2014/07/01	LVDS/ CMOS/ USB-ReDriver			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FUTURE CENTER TO ANY OTHER DIVISION OR TO ANY OTHER PERSON WITHOUT THE WRITTEN CONSENT OF THE COMPETENT DIVISION OF FUTURE CENTER. DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size	Document Number	Rev	
				Custom	Y401 NM-A031	1.0	
				Date:	Wednesday, March 27, 2013	Sheet	35

CRT Connector



Security Classification		LC Future Center Secret Data		Title							
Issued Date		2012/07/01		Deciphered Date			2014/07/01				
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.							Size		Document Number		Rev 1.0
							Custom		Y401 NM-A031		
							Date:		Wednesday, March 27, 2013		

From 0402 footprint change to 0201

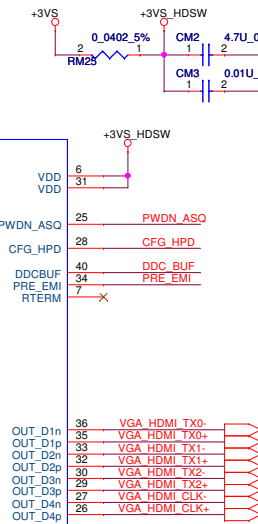


For P88271: R35/R36 NC
For P88272: R35/R36 NC, pin21/pin22 NC or SW_MAIN/SW_DDC driven to LOW
For P88273: R35/R36 stuff or SW_MAIN/SW_DDC driven to HIGH

SW	Input	Output
SW_DDC	IN1---GPU IN2---CPU	L=IN1 H=IN2
SW_MAIN	IN1---GPU IN2---CPU	L=IN1 H=IN2

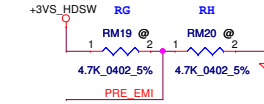
Channel A --> GPU

Channel B --> PCH



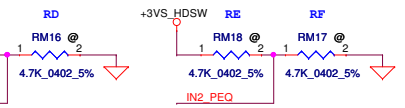
SEL	DDC_BUF	RA	RB
H: Active DDC buffer enable, setting 1	Stuff	NA	NA
M: Active DDC buffer enable, setting 2	NA	NA	Stuff
L: No DDC active buffer, passive DDC level shifting	NA	NA	NA

DDCBUF DDC_BUF_EN = L: No DDC active buffer, passive DDC level shifting



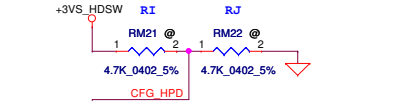
SEL	PRE_EMI	RG	RH
H: Pre-emphasis added, no EMI control	Stuff	NA	NA
M: No pre-emphasis, EMI control selected	NA	Stuff	NA
L: No pre-emphasis, no EMI control	NA	NA	NA

PRE_EMI: TMDS output drive pre-emphasis and EMI setting. Internal pull-down ~500k ohm



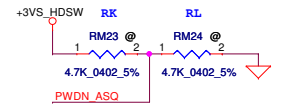
SEL	IN1_PEQ/IN2_PEQ	RC	RD	RE	RF
H: High level receiving equalization selection	Stuff	NA	Stuff	NA	NA
M: Low level receiving equalization selection	NA	Stuff	NA	NA	Stuff
L: Middle level receiving equalization selection	NA	NA	NA	NA	NA

IN1_PEQ/IN2_PEQ: Rx Equalization Setting for port1/port2. Internal pull-down ~500k ohm



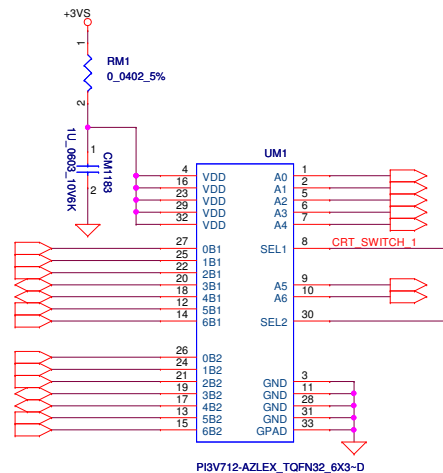
SEL	CFG_HPD	RI	RJ
H: IN1_HPD=OUT_HPD when SW_DDC=L / IN2_HPD=OUT_HPD when SW_DDC=H	Stuff	NA	NA
M: IN1_HPD=OUT_HPD when SW_DDC=L or SW_MAIN=L / IN2_HPD=OUT_HPD when SW_DDC=H or SW_MAIN=H	NA	Stuff	NA
L: IN1_HPD=OUT_HPD when SW_MAIN=L / IN2_HPD=OUT_HPD when SW_MAIN=H	NA	NA	NA

CFG_HPD: HPD switching configuration. Internal pull-down ~500k



SEL	PWDN_ASQ	RS	RH
H: power down	Stuff	NA	NA
L: Normal operation	NA	NA	NA

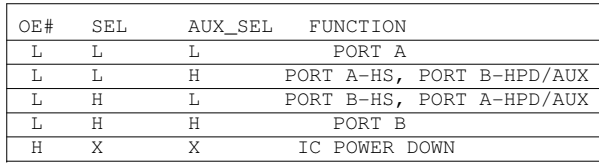
PWDN_ASQ: Power down control. Internal pull-down ~500k



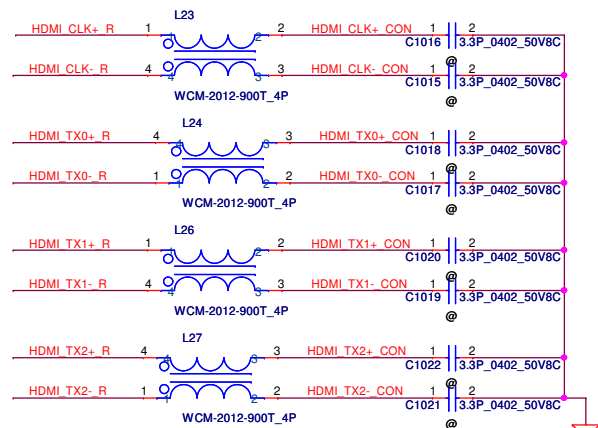
DAC_RED_1 <36>
DAC_ORN_1 <36>
DAC_BLU_1 <36>
CRT_DDC_CLK_R <36>
CRT_DDC_DATA_R <36>

For reserved CRT SW

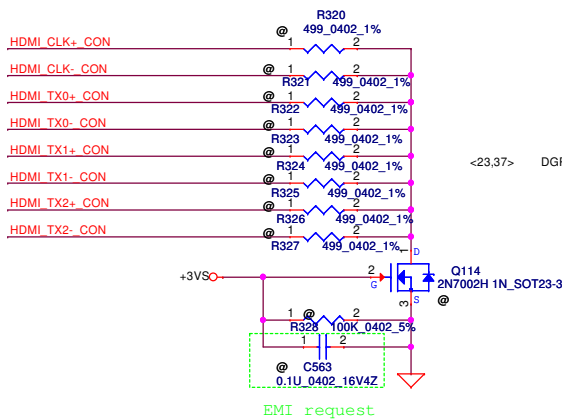
Input SELx	Input/Output An	Function
L	nB1--GPU	An=nB1
H	nB2---PCH	An=nB2



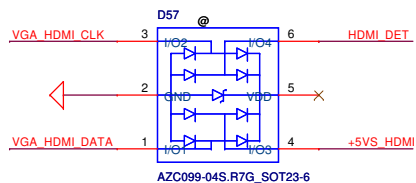
Title eDP SW			
Size Custom	Document Number Y401 NM-A031	Rev 1.0	
Date: Wednesday, March 27, 2013	Sheet 38	of 69	



<37> HDMI_CONN_HPDI
20120829 VA1
Change net name for add HDMI_MUX



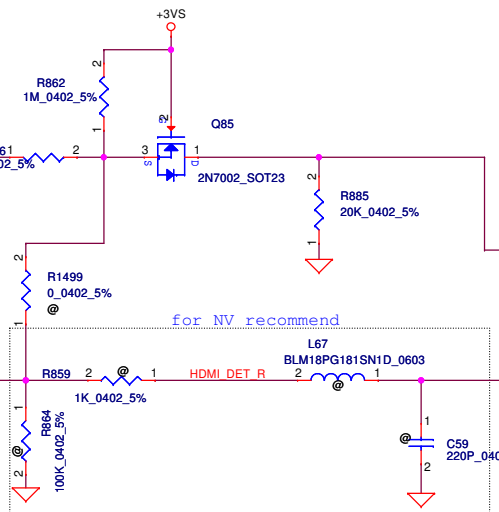
EMI request



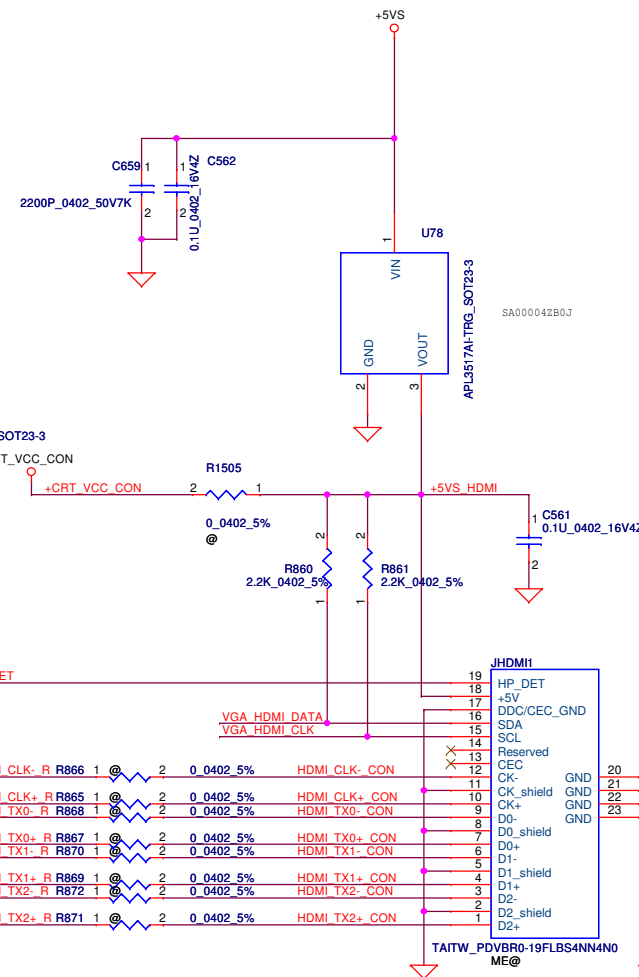
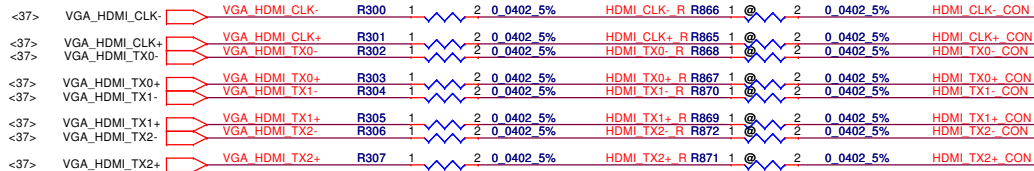
46@

HDMI+HDCP

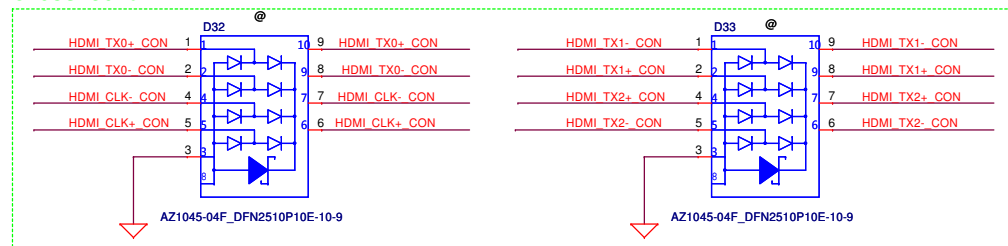
<37> VGA_HDMI_CLK
<37> VGA_HDMI_DATA




for NV recommend



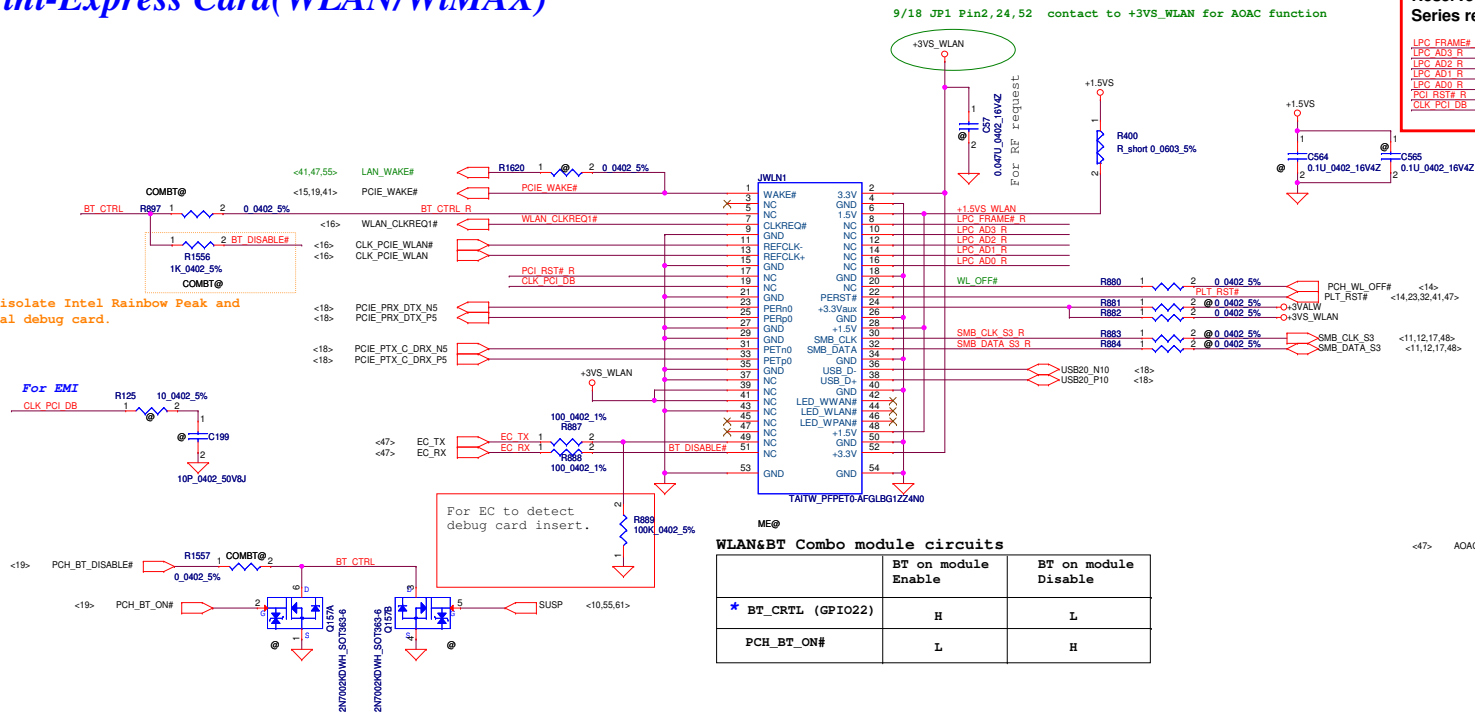
Close to JHDMI1



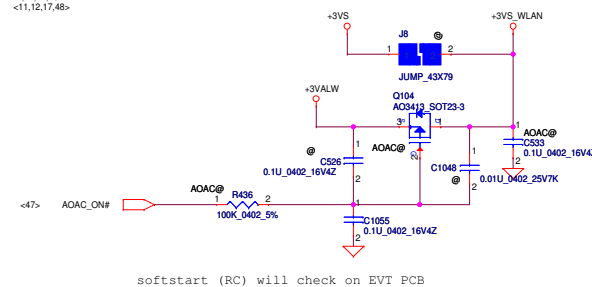
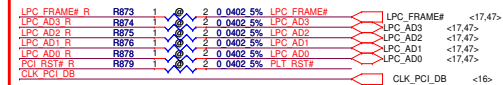
Security Classification		LC Future Center Secret Data		Title									
Issued Date		2012/07/01		Deciphered Date			2014/07/01		HDMI_CONN				
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.							Size Custom		Document Number		Y401 NM-A031		Rev 1.0
Date:						Wednesday, March 27, 2013		Sheet		39		of 69	

Mini-Express Card(WLAN/WiMAX)

For isolate Intel Rainbow Peak and Compal debug card.

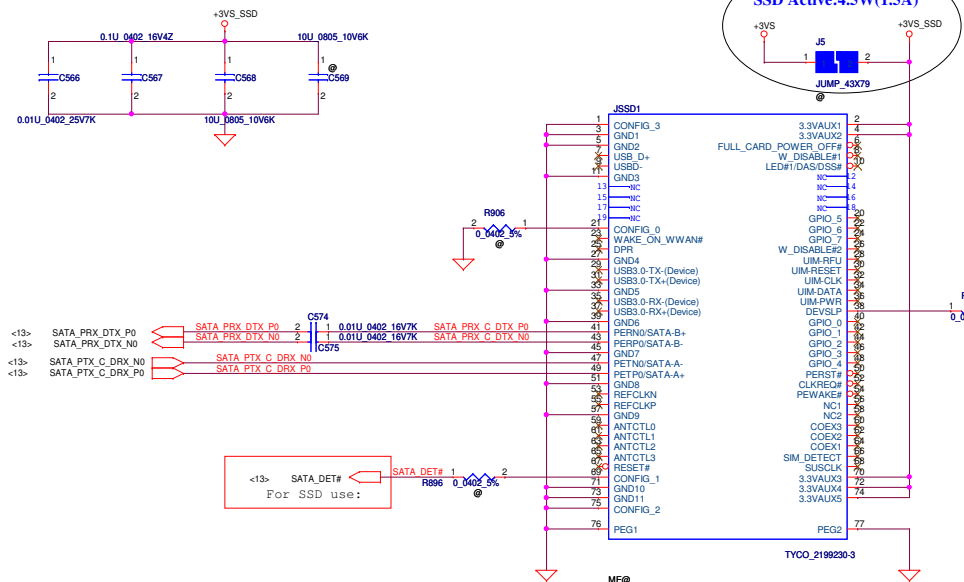


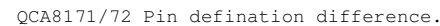
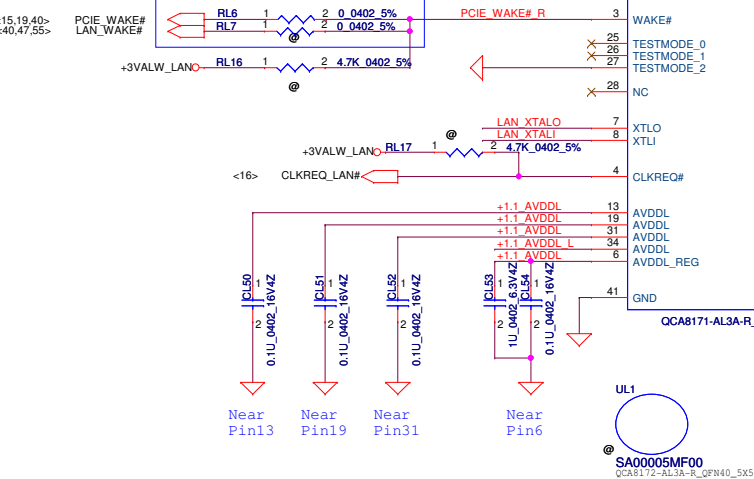
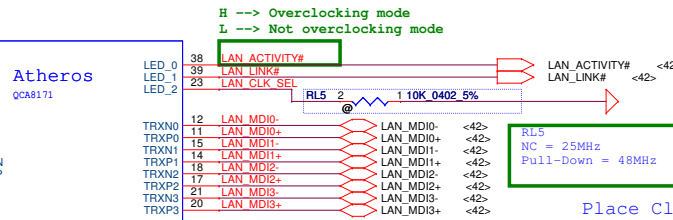
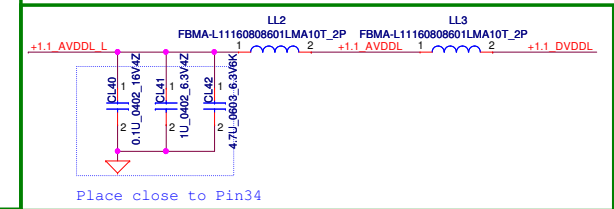
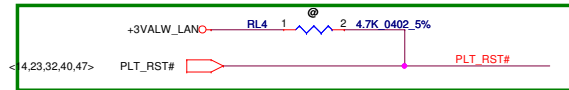
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.




9/18 Increase for Intel AOAC function

NGFF(SSD)

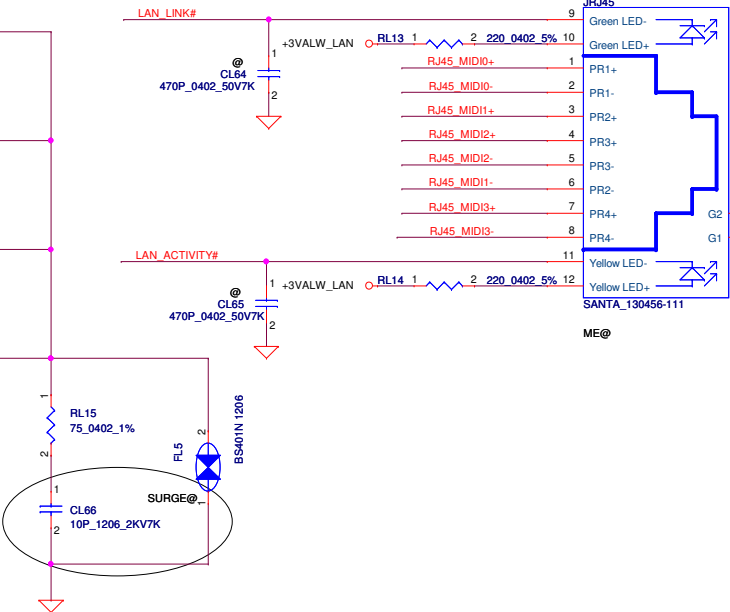
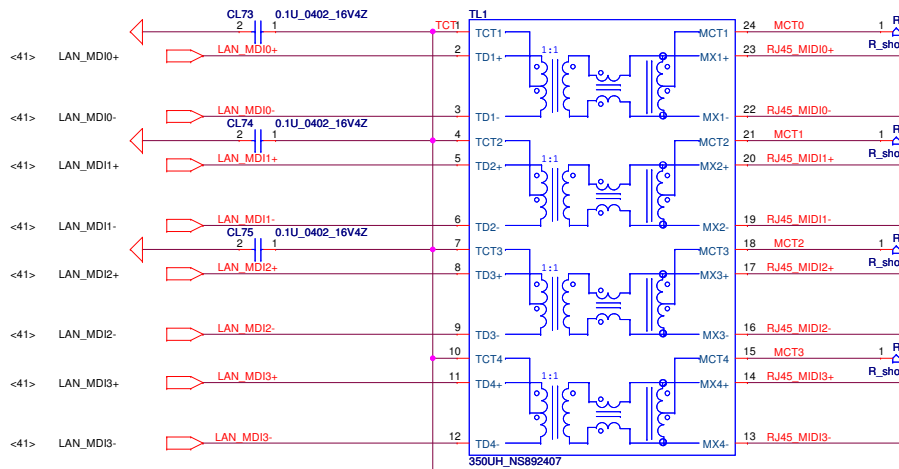




Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OR DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>			

Title	LAN_QCA8171		
Size Custom	Document Number	Y401 NW-A031	
Date	Wednesday, March 27, 2019 11:58 AM		

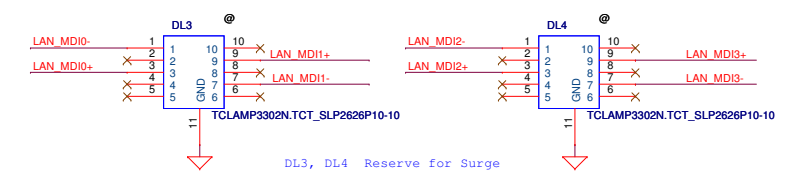
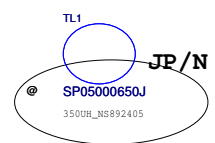
<41> LAN_LINK#
 <41> LAN_ACTIVITY#



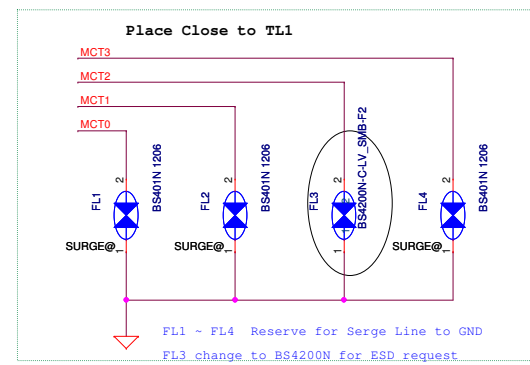
placement

CL69 reserved for EMI,
place close to TL1

Place CL33 close to TL1




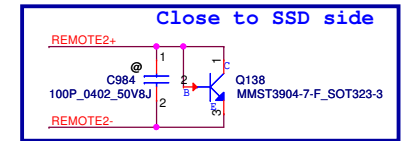
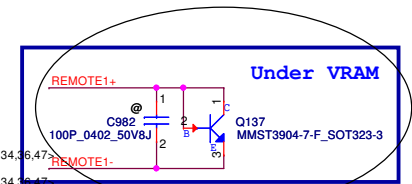
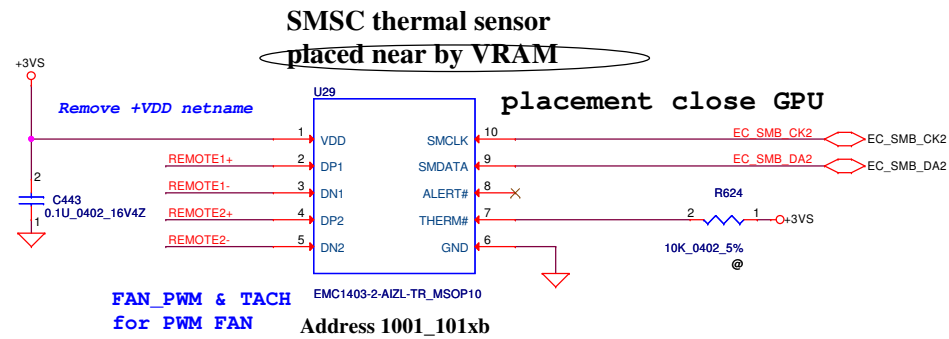
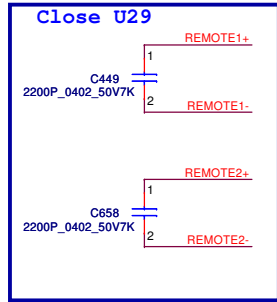
DL3, DL4 Reserve for Surge



Place Close to TL1

FL1 ~ FL4 Reserve for Surge Line to GND
 FL3 change to BS4200N for ESD request

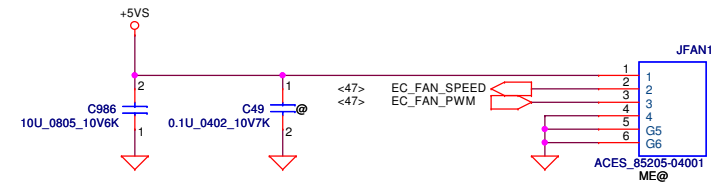
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	LAN Transformer		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.						
Size	Document Number		Y401 NM-A031		Rev	1.0
Date	Wednesday, March 27, 2013		Sheet	42	of	69





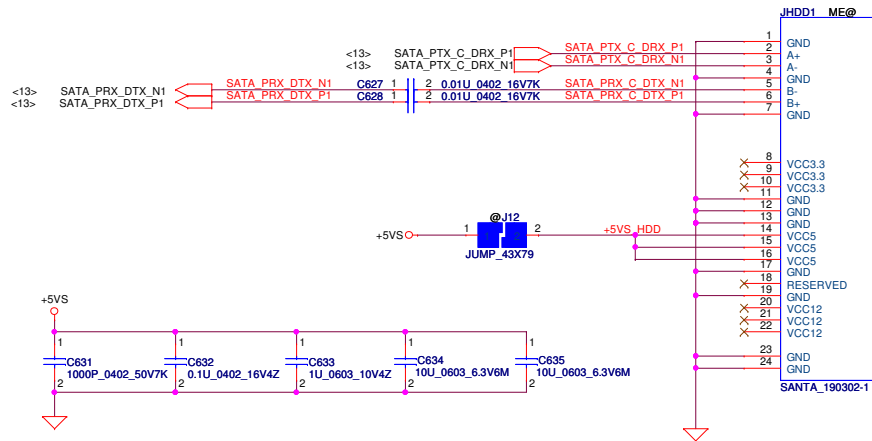
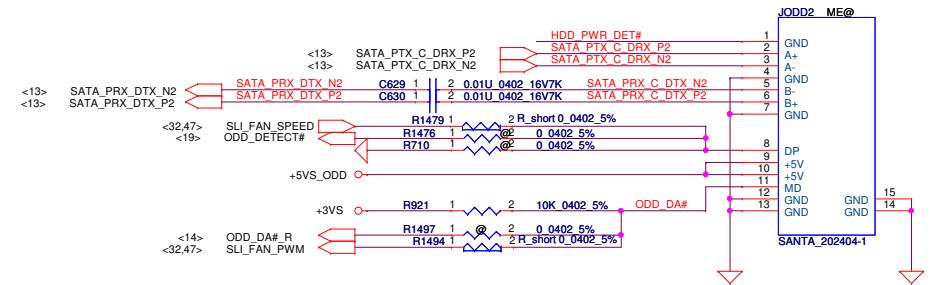
internal pull up 1.2K to 1.5V
 R for initial thermal
 shutdown temp

REMOTE2+/-:
 Trace width/space:10/10 mil
 Trace length:<8"

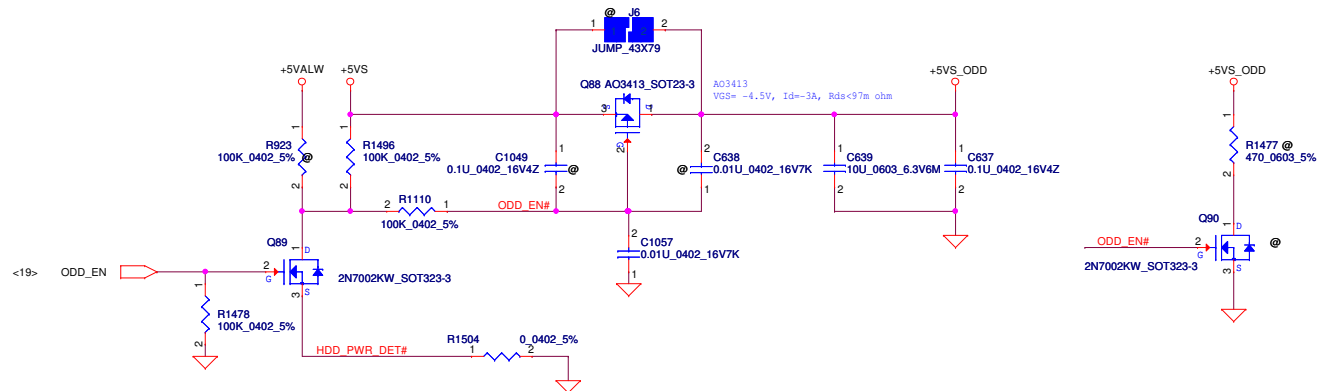
FAN1 Conn




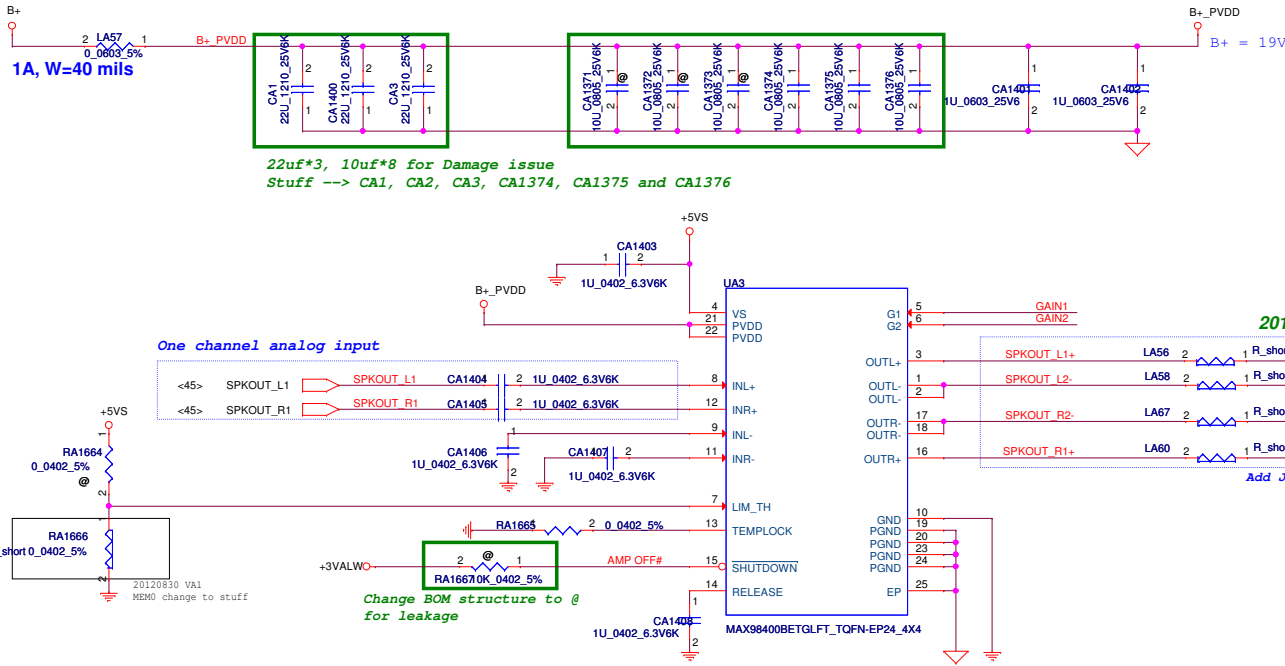
Security Classification		LC Future Center Secret Data				Title					
Issued Date		2012/07/01		Deciphered Date		2014/07/01				VGA Thermal sensor/FAN CONN	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.											
Size		Document Number		Date		Wednesday, March 27, 2013		Sheet 43 of 69			
Custom								Y401 NM-A031			

SATA HDD Conn.**SATA ODD Conn.**

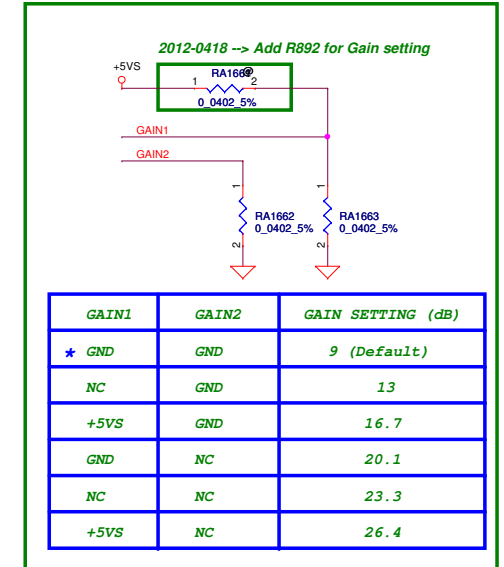
ODD Power Control



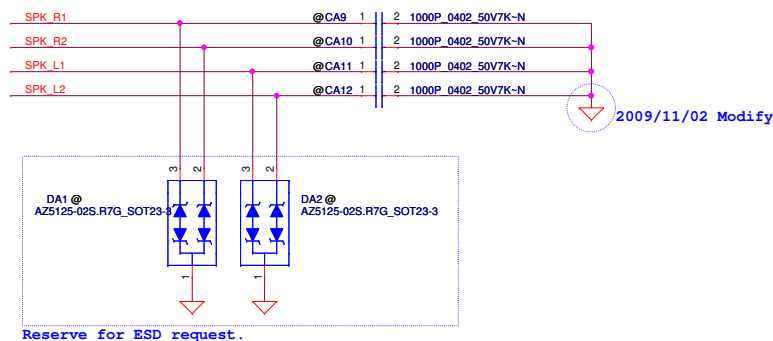
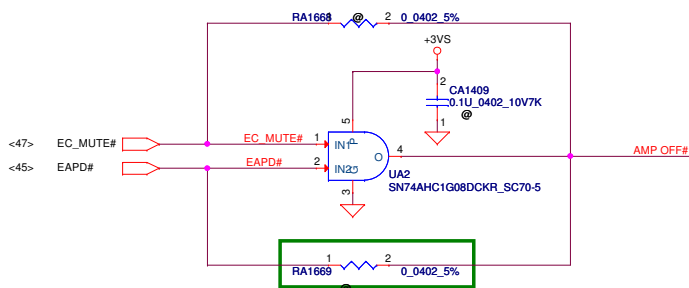
Security Classification		LC Future Center Secret Data		Title			
Issued Date	2012/07/01	Deciphered Date	2014/07/01	HDD/ODD CONN			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size	Document Number	Rev	
				Custom	Y401 NW-A031	1.0	
				Date:	Wednesday, March 27, 2013	Sheet	44 of 69



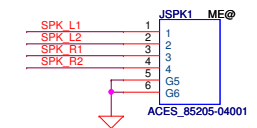
GAIN SETTING



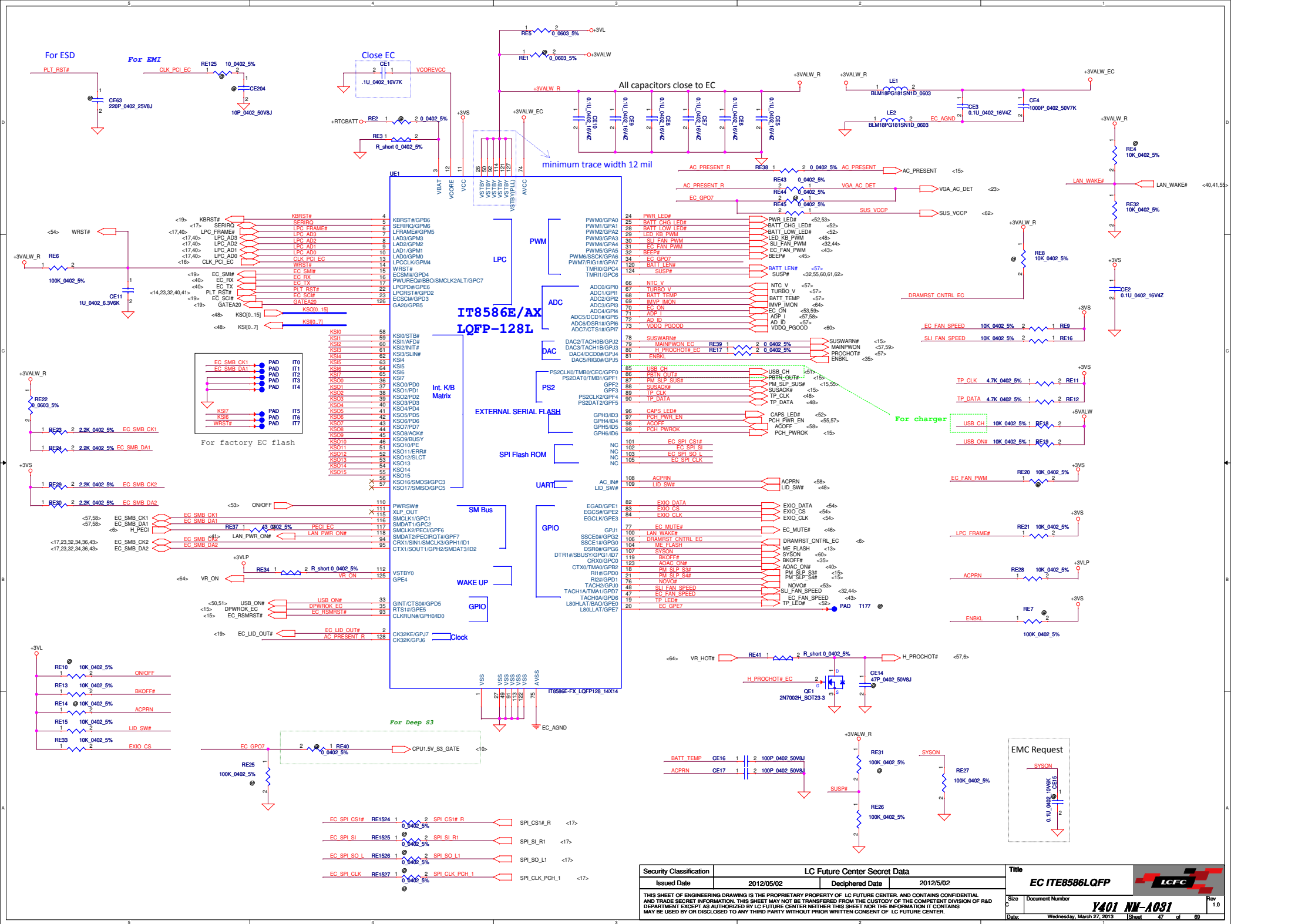
2012-0418 --> Set R890 BOM structure as Stuff



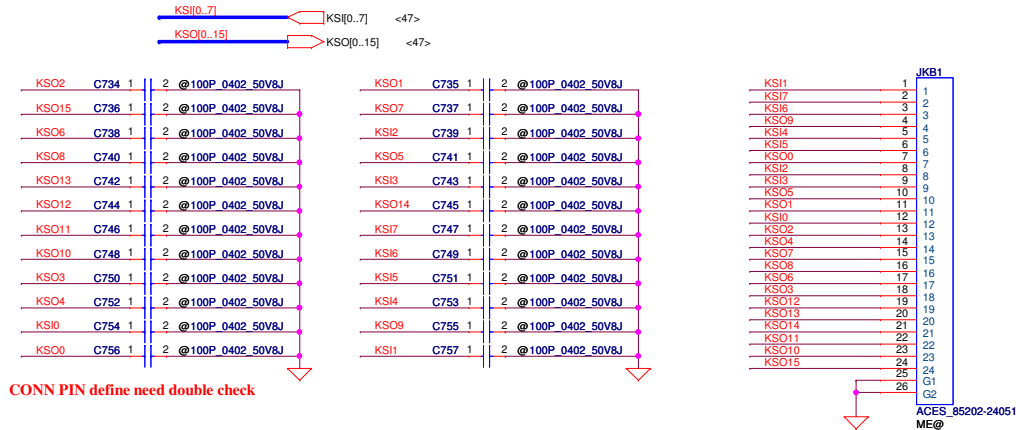
Speaker Conn.



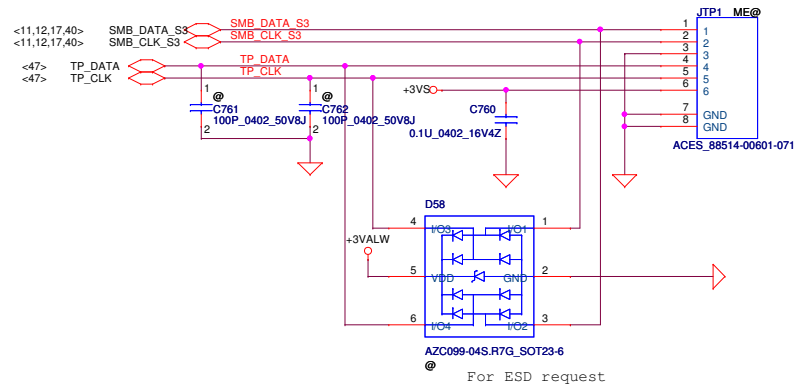
Speaker 2.5W



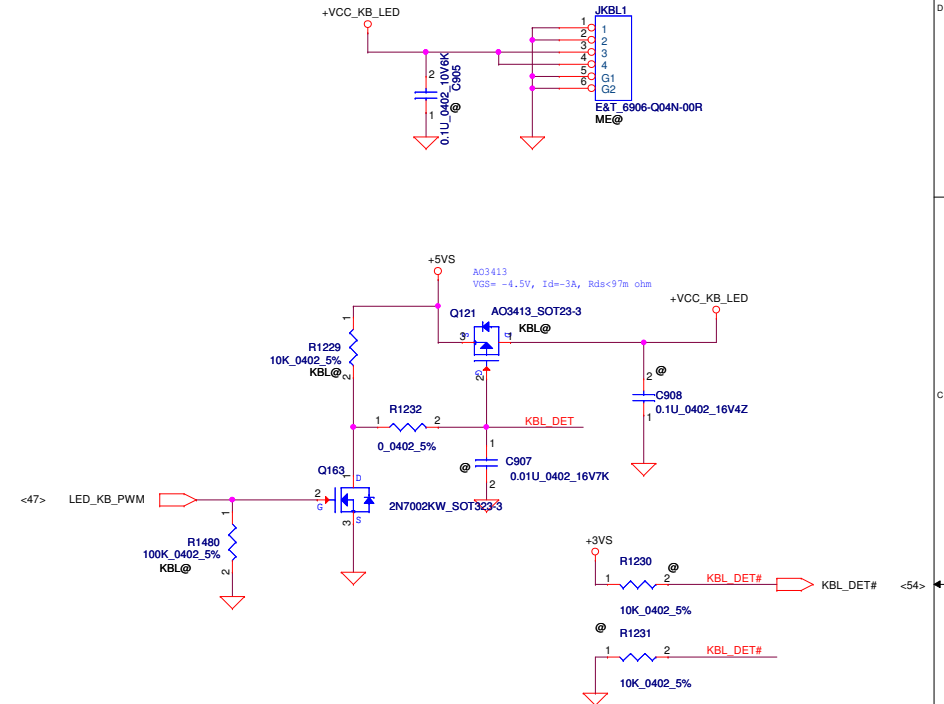
14" INT_KBD Conn.



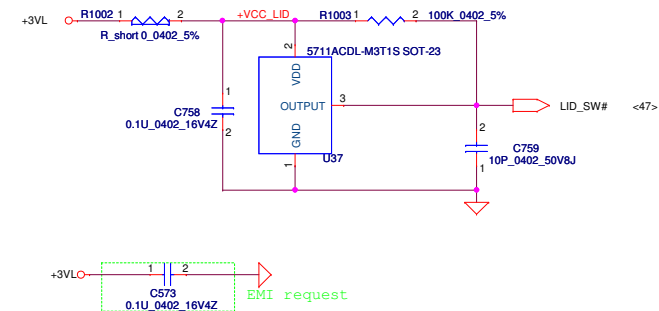
To TP/B Conn.




KB Lighting CONN.4pin

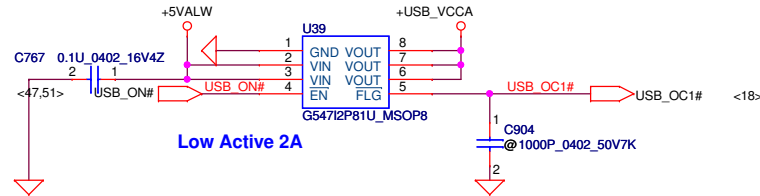


Lid Switch

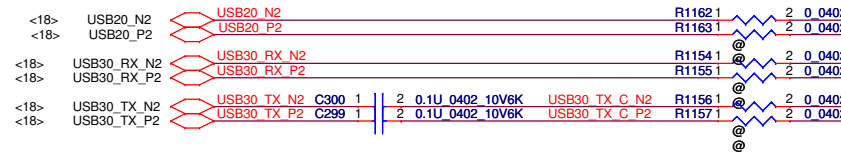
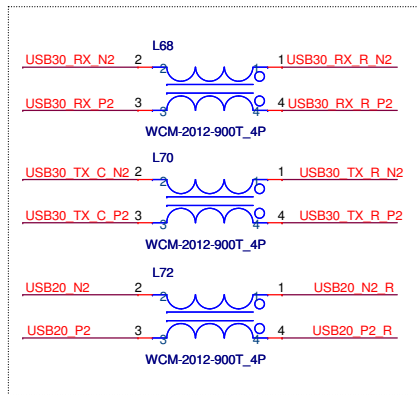


Security Classification		LC Future Center Secret Data		Title			
Issued Date		2012/07/01		Deciphered Date			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FUTURE CENTER. DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.							
Size		Document Number		Y401 NW-A031		Rev 1.0	
Custom		Date:		Wednesday, March 27, 2013		Sheet 48 of 69	

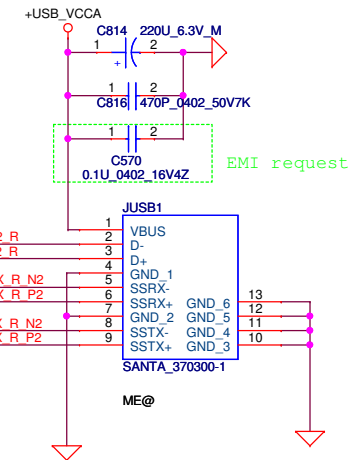
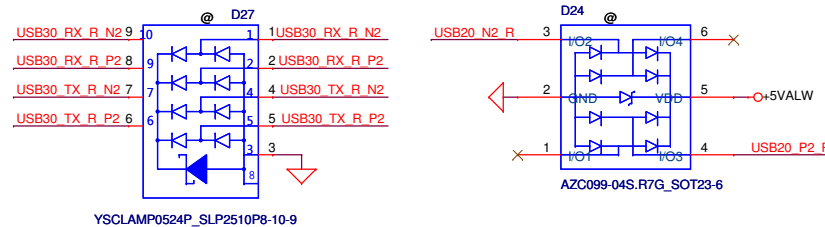
LEFT SIDE USB3.0 PORT X1




For EMI request
USB2.0 choke --> SM070001S0J
USB3.0 Choke --> SM070001S0J

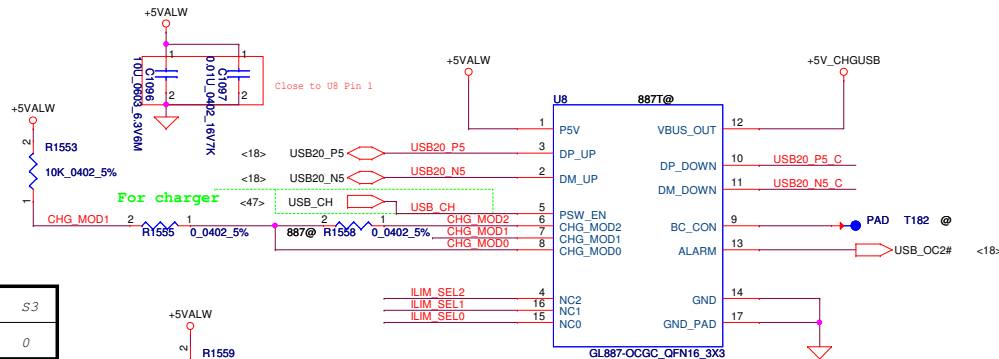


For ESD request



Security Classification		LC Future Center Secret Data		Title					
Issued Date	2012/07/01	Deciphered Date	2014/07/01	USB 3.0 PORT (LEFT)					
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.						Size	Document Number	Y401 NW-A031	Rev 1.0
						Custom			
						Date:	Wednesday, March 27, 2013	Sheet 50 of 69	

Sleep & Charge **Right side USB Charger Port (USB_Port5, near JMIC1)**



Genesys GL887

CHG_MOD2	CHG_MOD1	CHG_MOD0	Charge Mode
0	0	0	Charge Disable
0	1	0	CDP mode
0	1	1	DCP mode
1	0	0	Apple 1A mode
1	0	1	Apple 2A mode
1	1	0	Auto mode (DCP and Apple 1A)
1	1	1	Auto mode (DCP and Apple 2A)

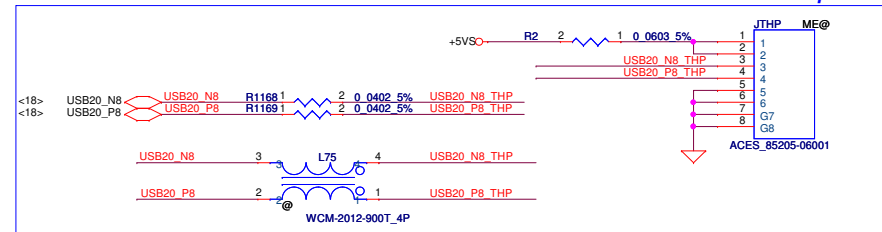
Genesys GL887T

CHG_MOD2	CHG_MOD1	CHG_MOD0	Charge Mode
0	0	0	Power down mode
0	0	1	Auto 2A mode without wake up function
X	1	0	BC1.2 SDP mode
0	1	1	Auto 2A mode with wake up function
1	0	0	BC1.2 DCP mode
1	0	1	Apple 2A mode
1	1	1	BC1.2 CDP mode with Smart CDP

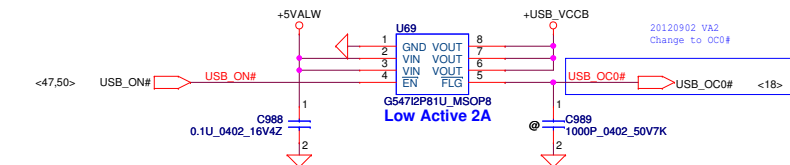
TI TPS2543

CHG_MOD2	CHG_MOD1	CHG_MOD0	ILIM_SEL2	MODE
0	0	0	X	DCH OUT held low /Data lines disconnected
1	1	1	1	CDP Data connected and Load detect active
1	1	1	0	SDP2 Data connected
1	1	0	X	SDP1 Data connected
0	1	0	X	SDP1 Data connected
1	0	0	X	DCP_Short Stay in DCP BC1.2 Charging mode
1	0	1	X	DCP_Divider Stay in DCP Divider1 Charging mode
0	1	1	X	DCP_Auto Data disconnected and Load detect active
0	0	1	X	DCP_Auto Data disconnected and Load detect active

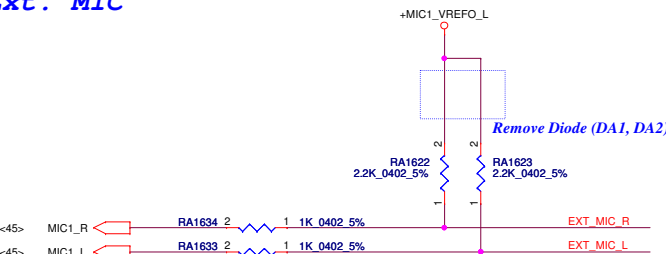
Touch panel



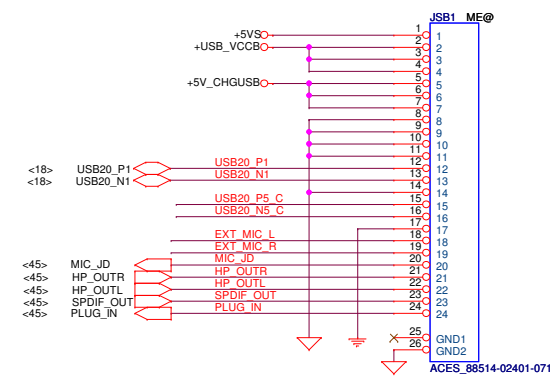
USB Power (USB20_P9)



Ext. MIC



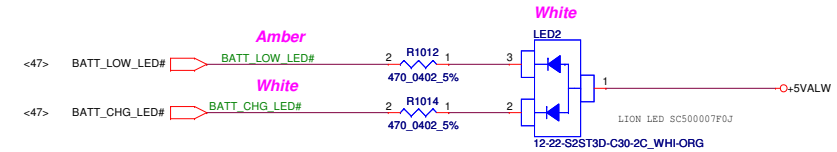
AUDIO/B Conn.



need change to 鍍錫材料
COMPAL : SP010015W1J
Footprint : 88514-0240N-071

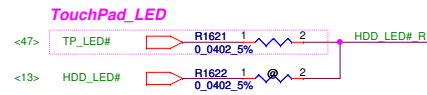
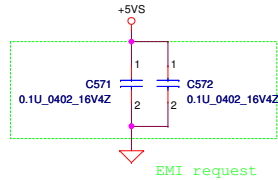
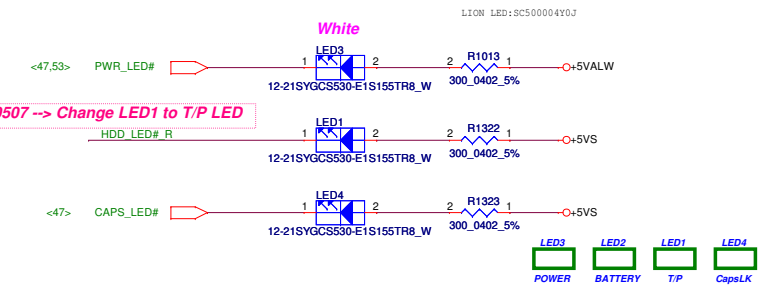
Security Classification	LC Future Center Secret Data		Title	Rev	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	AUDIO-B CONN/ USB CHARGER	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FUTURE CENTER DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size	Document Number
				Custom	Y401 NW-A031
				Date:	Wednesday, March 27, 2013
				Sheet	51 of 69

BATT CHARGE/LOW LED



2012-0507 --> Add MOS solution on LED3, 2 to avoid the light blinked.

PWR LED HDD LED CapsLK LED



BlueTooth DC

Screw Hole

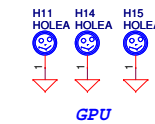
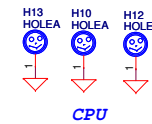
CPU and GPU: H_3P8X 6

MIN PCIE: H_3P3 X 1

C: H_3P8X 3

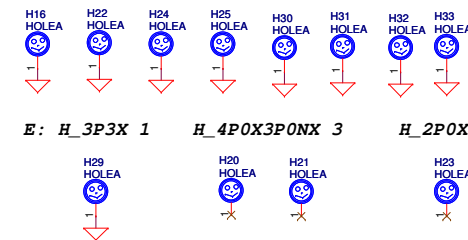
B: H_3P8X 3

E: H_3P3X 1




ME: H_8P0 X 8; H_3P3X 1; H_4P0X3P0N X 2; H_2P0X 1

A: H_2P8X 8

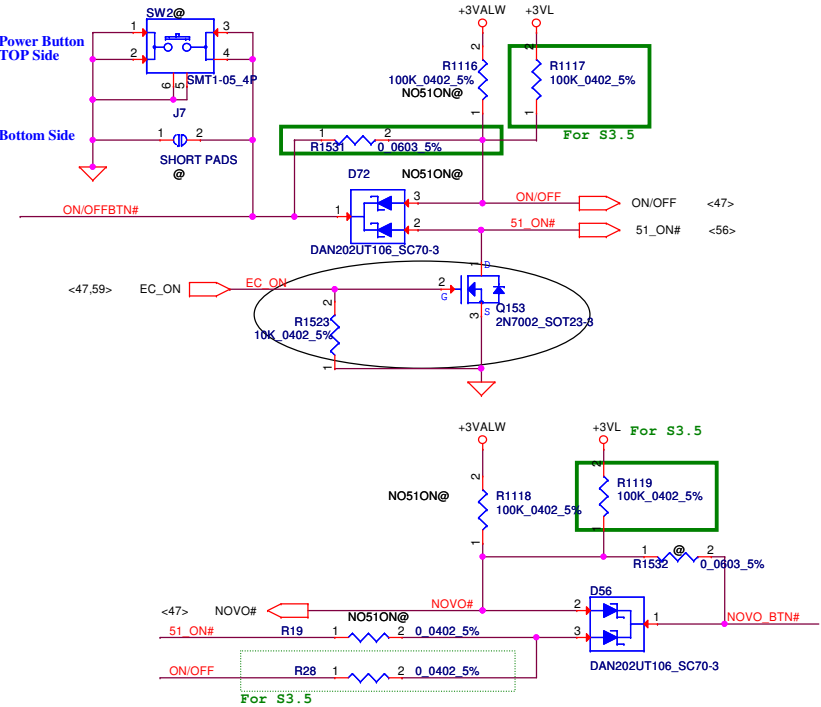


PCB Federal Mark PAD

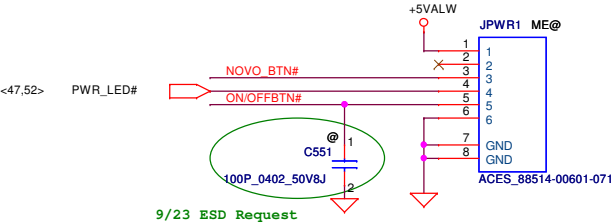


Security Classification		LC Future Center Secret Data		Title		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	LED		
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>						Rev
Size		Document Number		Y401 NM-A031		1.0
Custom						
Date:		Wednesday, March 27, 2013		Sheet		52 of 69

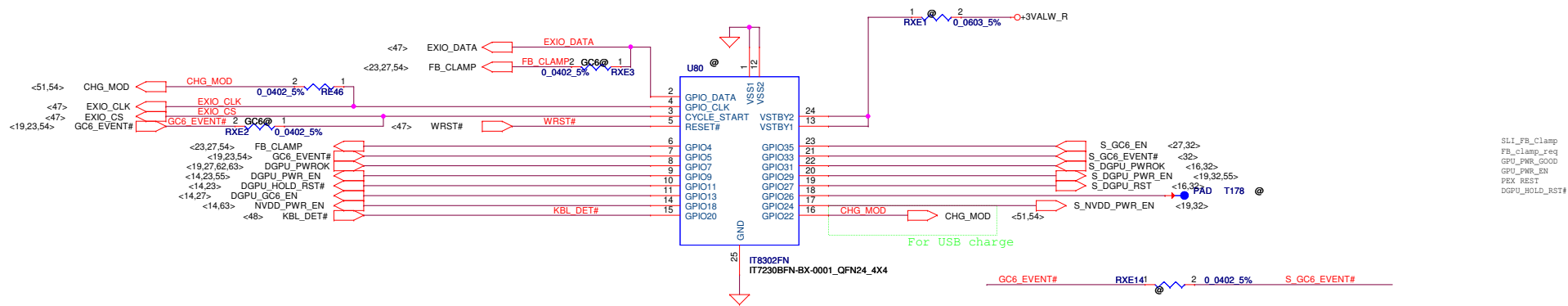
ON/OFF switch



Power Button/B link
to Function/B Conn. 10pin



EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	EX IO	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size	Document Number
				Custom	Y501 NM-A031
				Date:	Wednesday, March 27, 2013
				Sheet	54 of 69
				Rev	1.0

AP4800BGM
 $VGS=10V$, $ID=9A$, $R_{ds}=18m\ \Omega$
 $VGS=-25V$

+5VALW

U46

C836
 100u_0805_10V6K

C837
 100u_0603_6.3V6M

AP4800BGM-HF

C838
 1U_0603_10V4Z

or EMI apply

R1475
 470_0603_5%

+5V_GATE R

R1088
 82K_0402_5%

+5V_GATE

R1484
 820K_0402_5%

R1085
 150K_0402_5%

+VSB

C842
 0.01U_0402_25V7K

R1475
 470_0603_5%

Q99
 2N7002KW_SOT323-3

SUSP

[illegible]


For B phase test, 通知power 修改57頁 (反向)

+3VS to +3VS_SLI

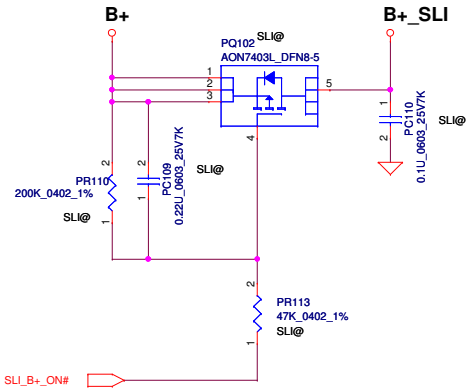
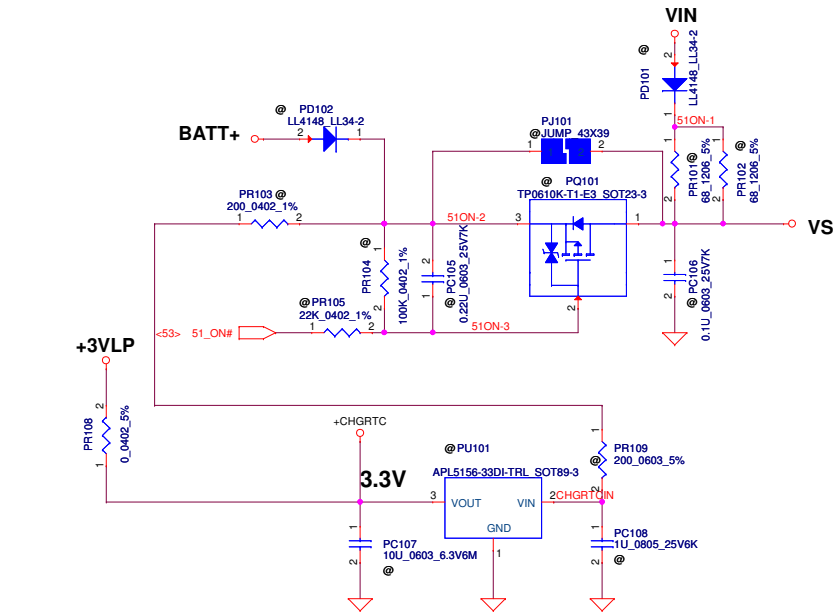
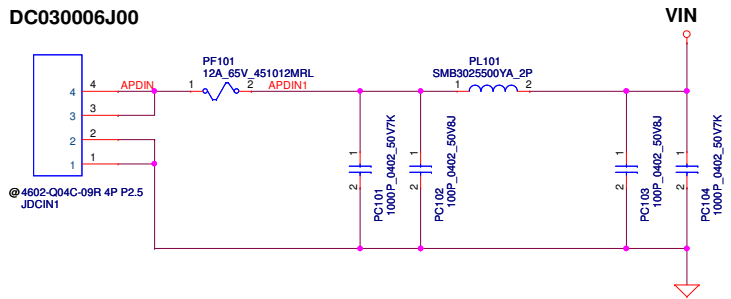
2012-0419 --> modify +3VS_SLI BOM structure to "SLI@"

The diagram shows the power rail modification for the SLI interface. Key components and connections include:

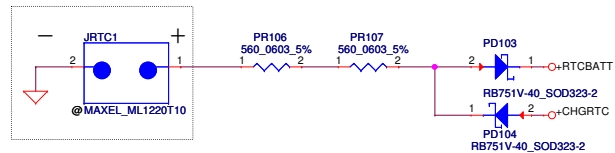
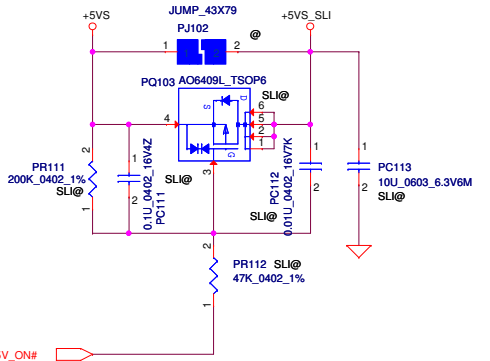
- Power Rails:** +3VS, +3VS_SLI, +5VALW, S_DGPU_PWR_EN#.
- Resistors:**
 - R1502 (47K_0402_5%) connected to +5VALW.
 - R1503 (100K_0402_5%) and R_short_0_0402_5% connected to S_DGPU_PWR_EN#.
 - R1501 (100K_0402_5%) connected to ground.
 - R1513 (10K_0402_5%) connected to +3VS.
- Capacitors:**
 - C1062 (0.1uF_0402_16V4Z) connected to +3VS.
 - C1063 (0.01uF_0402_25V7K) connected to +3VS_SLI.
 - C1012 (0.1uF_0402_10V7K) connected to +3VS.
- MOSFETs:**
 - Q150 (2N7002KW_SOT323-3) controlled by S_DGPU_PWR_EN#.
 - Q147 (AO3413_SOT23) connected to +3VS.
 - Q151 (2N7002KW_SOT323-3) controlled by S_DGPU_PWR_EN#.

Security Classification		LC Future Center Secret Data		Title			
Issued Date		2012/07/01		Deciphered Date			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.							
Size		Document Number		Y401		Rev	
Custom		A031		1.0			
Date:		Wednesday, March 27, 2013		Sheet		55 of 69	

DC030006J00

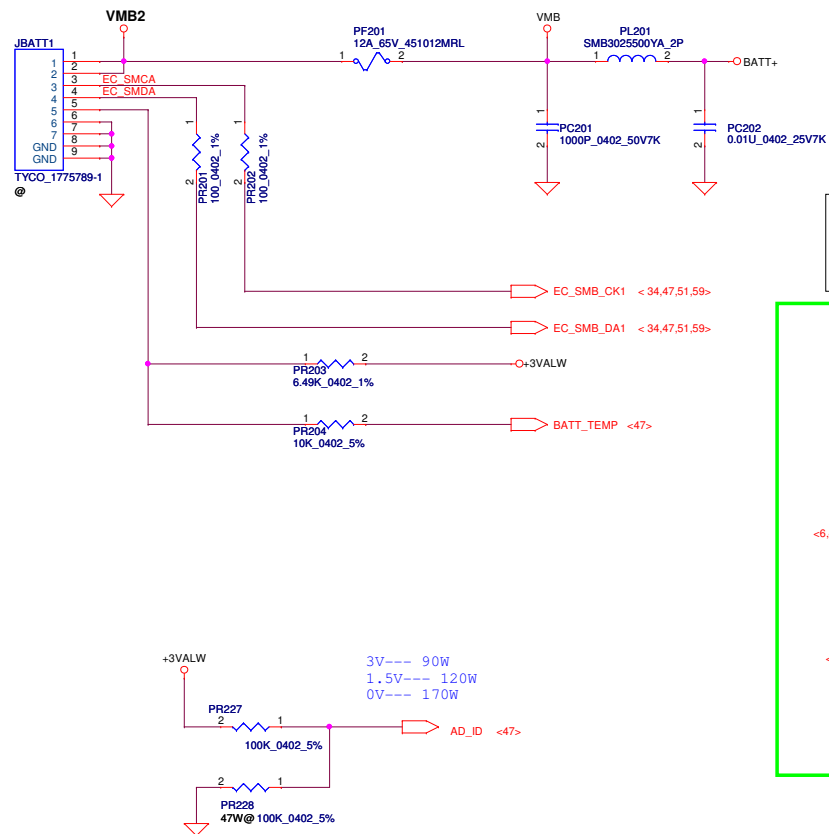


+5VS to +5VS_SLI



RTC Battery

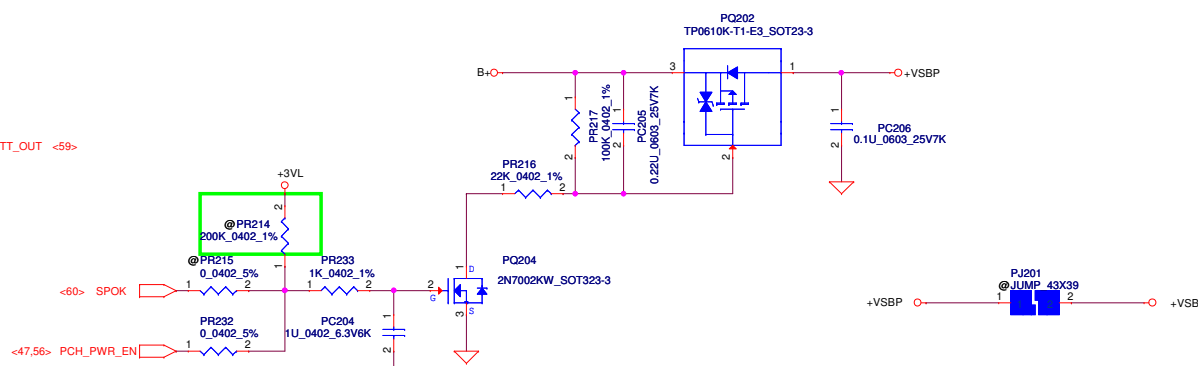
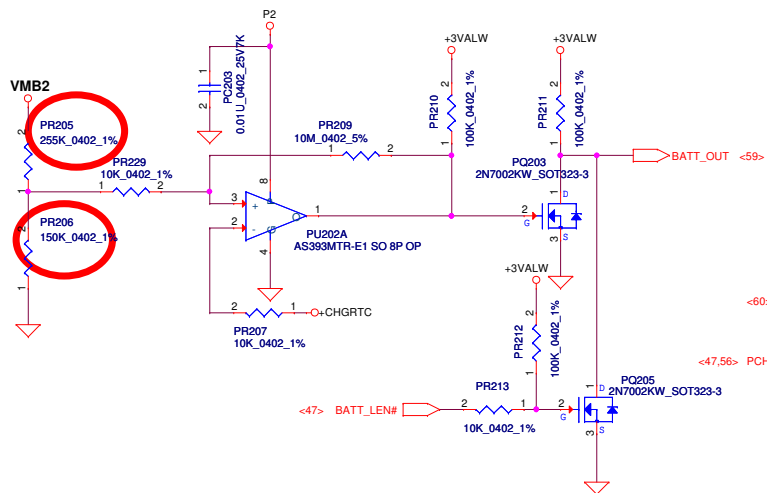
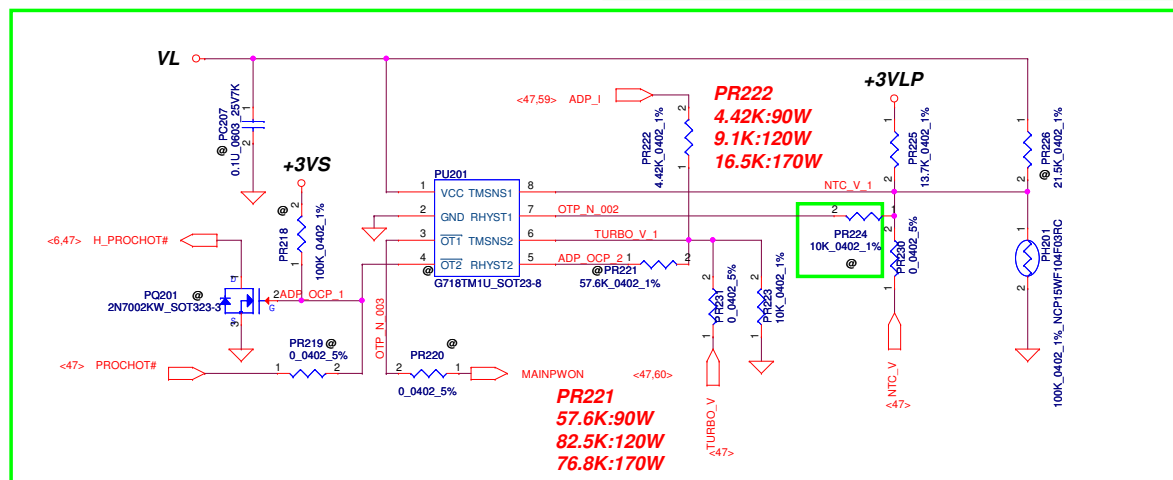
Security Classification	LC Future Center Secret Data		Title	Vin Detector	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Size	Custom
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FRO DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Date:	Wednesday, March 27, 2013	Sheet	56	of	69
Rev	1.0	Y410 NM-A031			



PH1 under CPU bottom side :
CPU thermal protection at 92+/-3 degree C
Recovery at 56 +3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

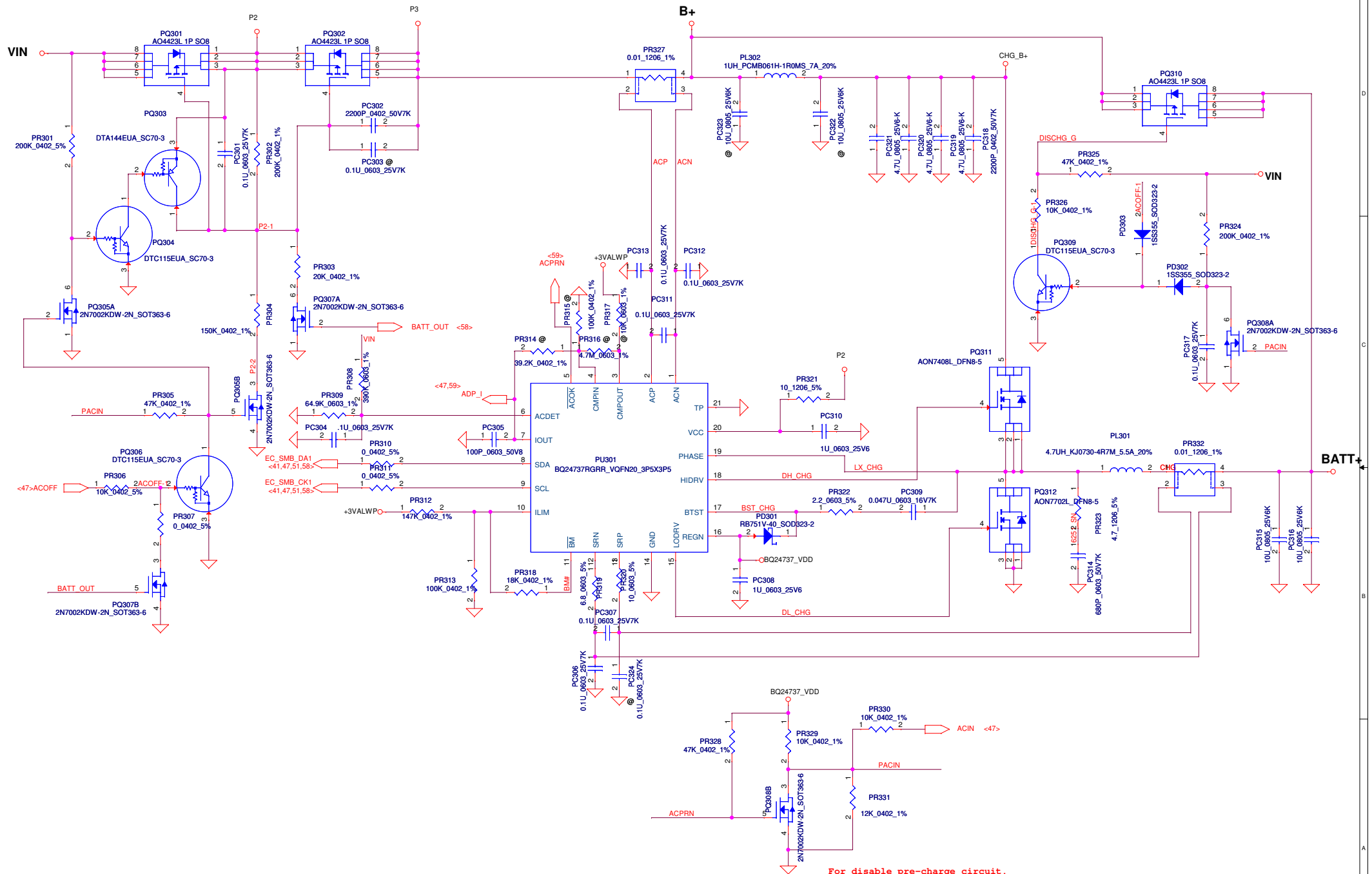
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212



Security Classification	LC Future Center Secret Data		Title
Issued Date	2012/07/01	Deciphered Date	2014/07/01
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FRO DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			

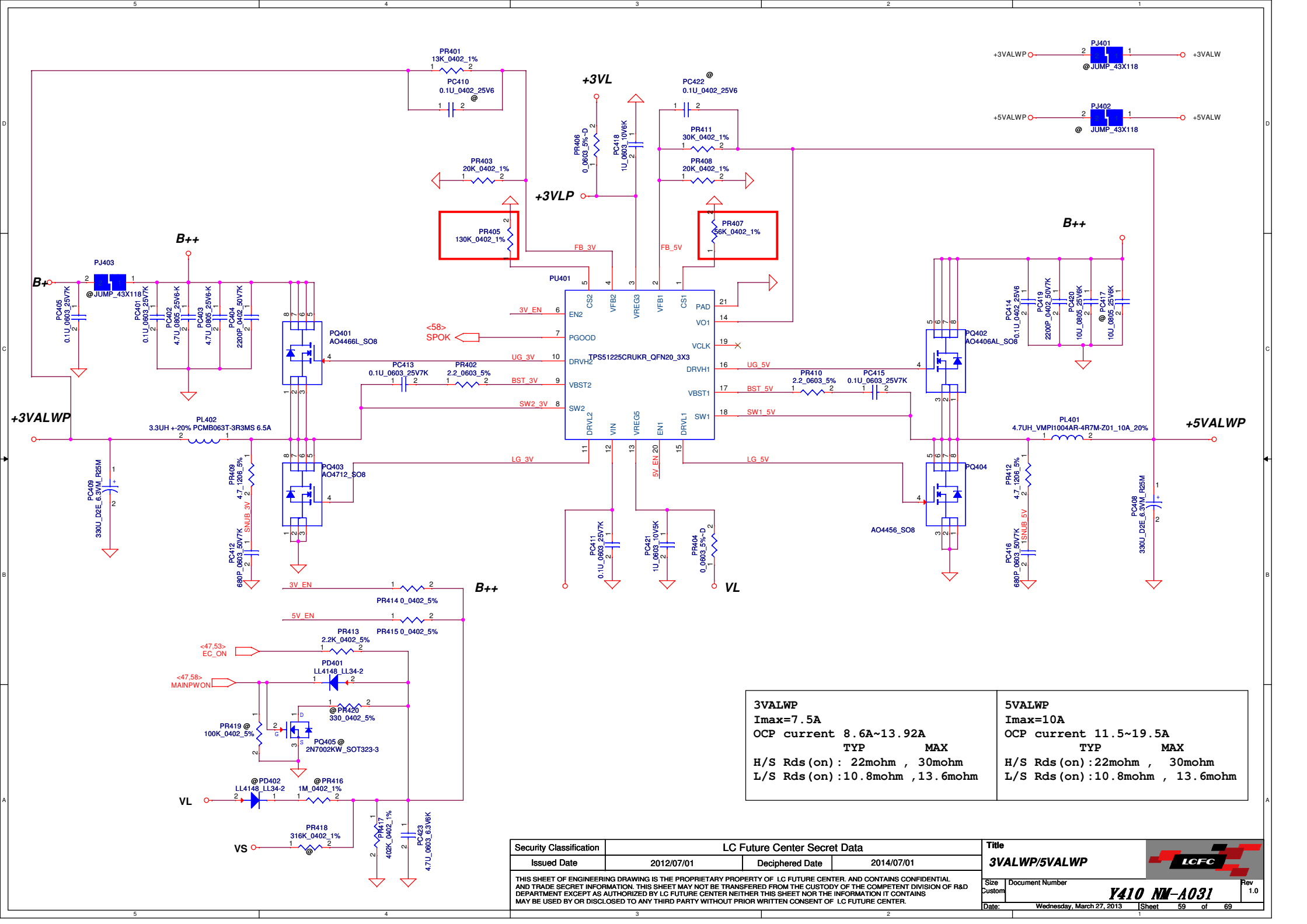
Size	Document Number	Rev
Custom	Y410 NM-A031	1.0
Date:	Wednesday, March 27, 2013	Sheet 57 of 69

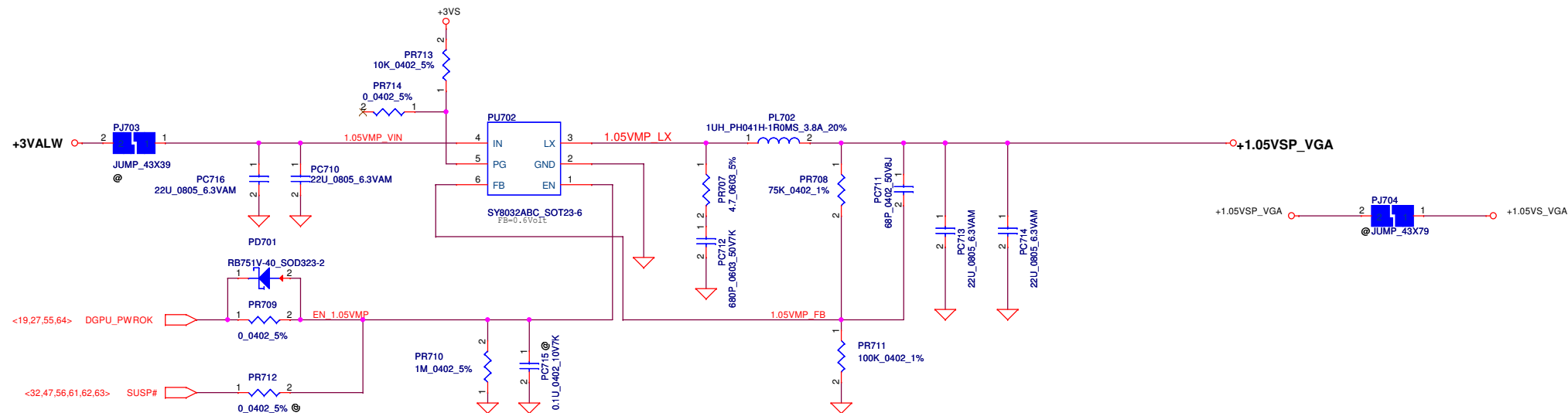
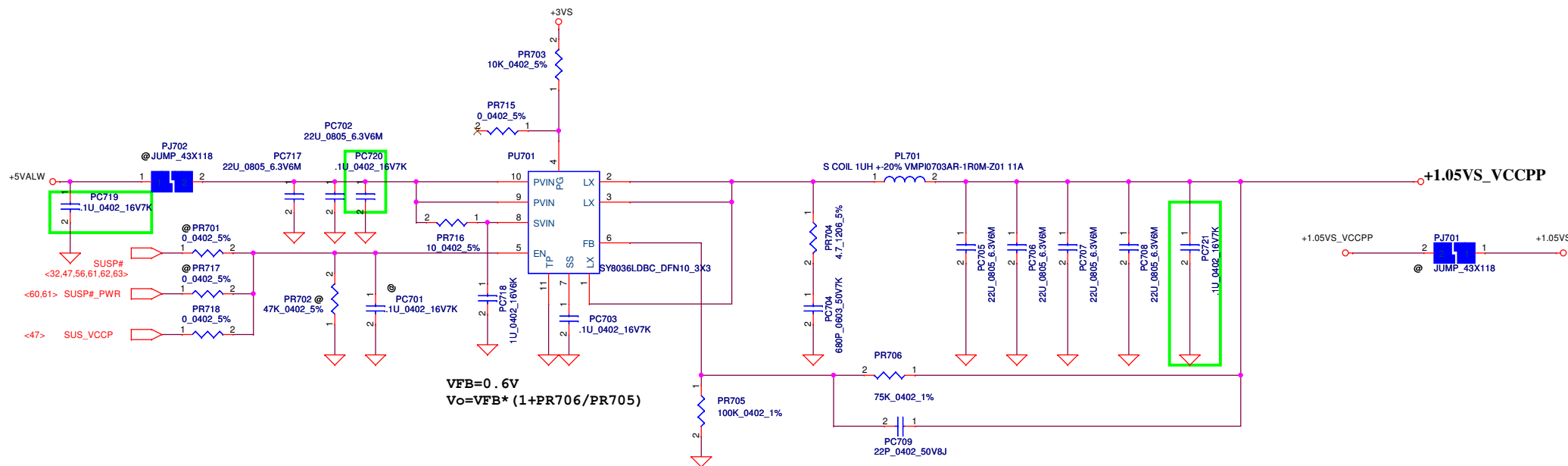
Charge Option() bit[8]=1



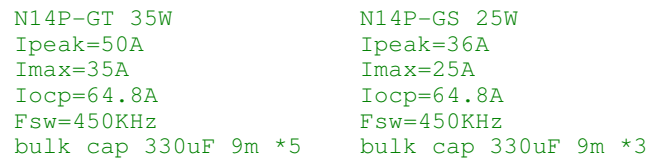
For disable pre-charge circuit.


Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		CHARGER	
2012/07/01		2014/07/01		Size	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.		Document Number		Rev	
		Y410 NM-A031		1.0	
Date:		Wednesday, March 27, 2013		Sheet	
		58		of	
		69			

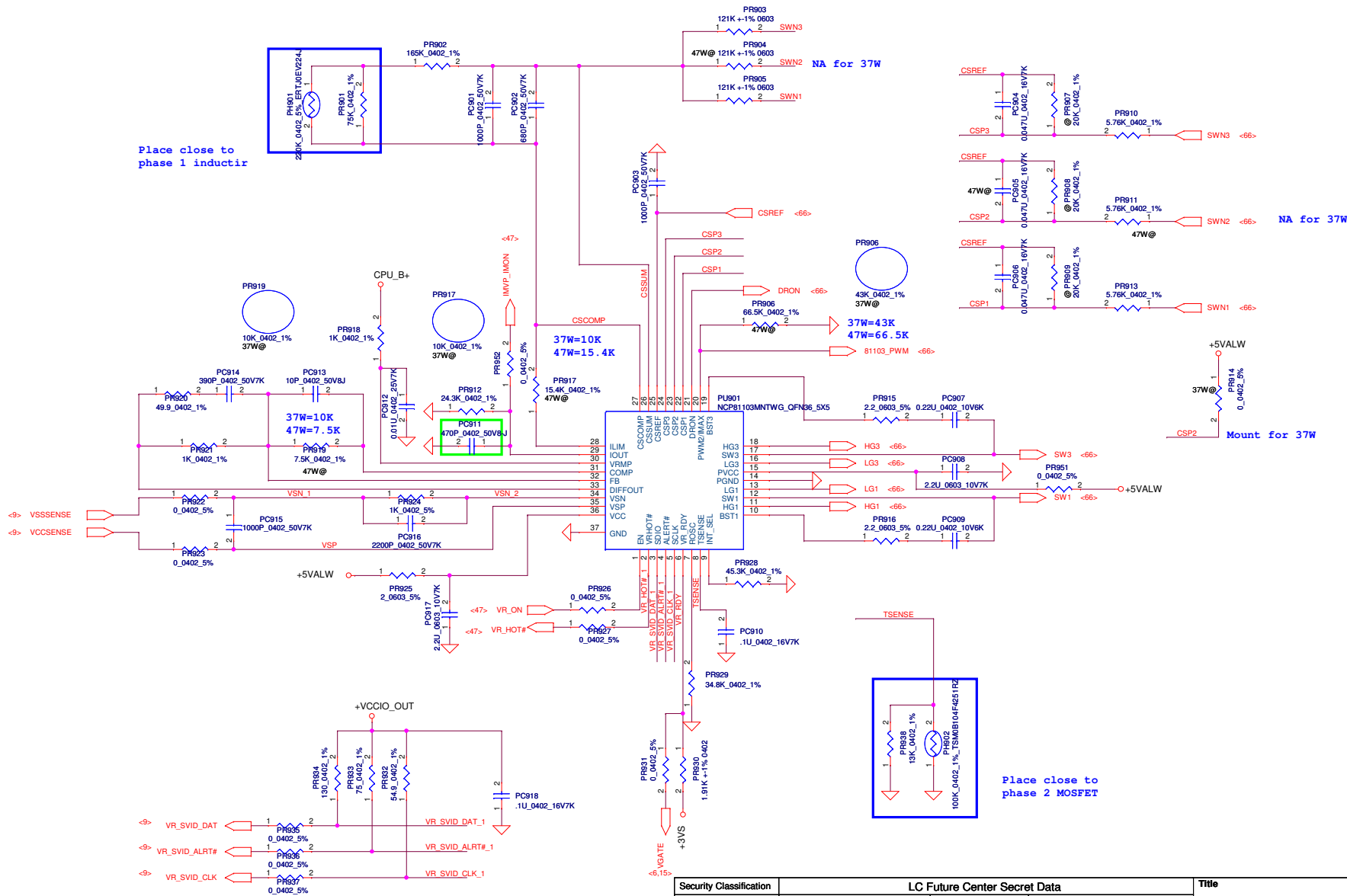




GB4-128 package

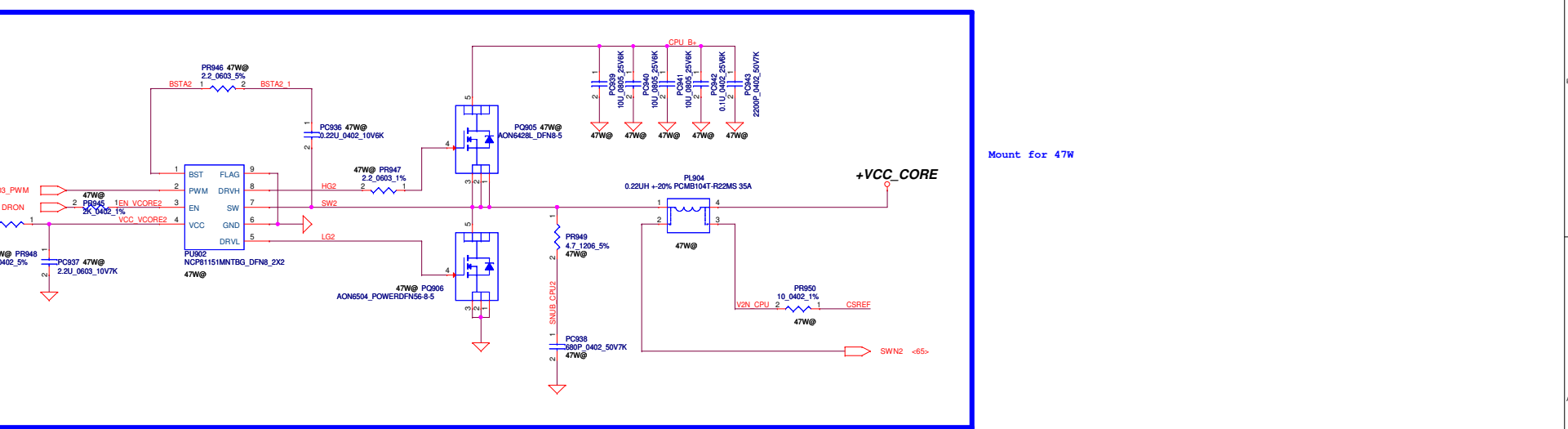
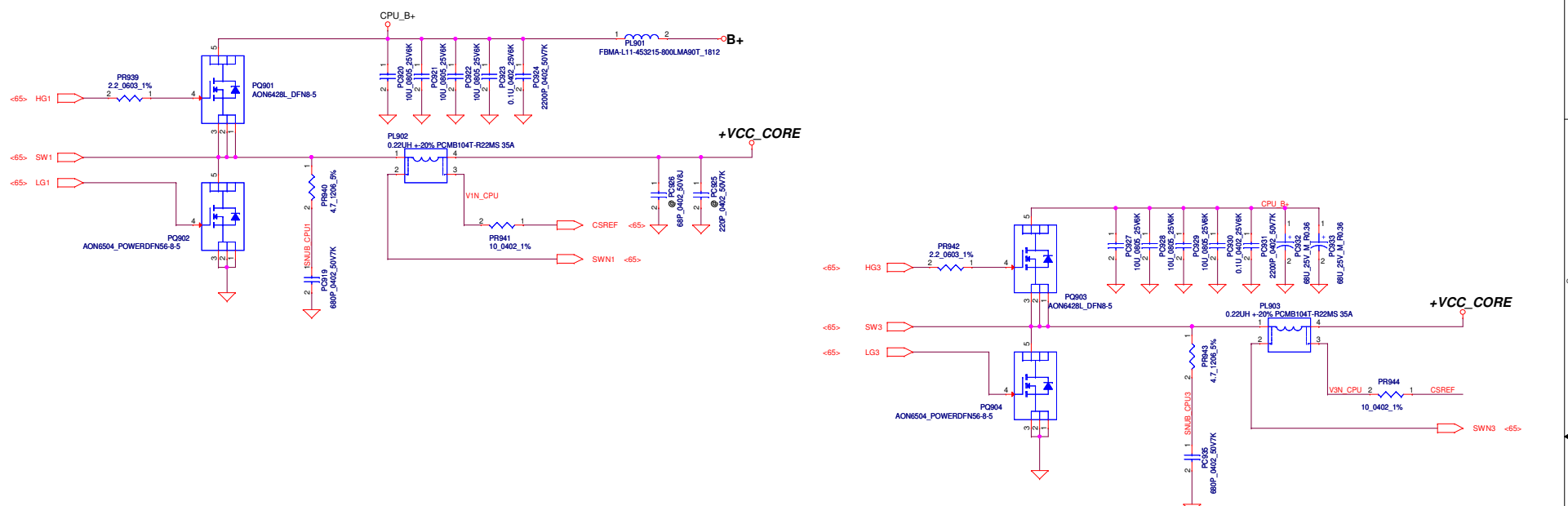


Security Classification		LC Future Center Secret Data		Title		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	VGA_CORE		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom	Document Number Y410 NW-A031	
				Date:	Wednesday, March 27, 2013	Sheet 63 of 69 Rev 1.0



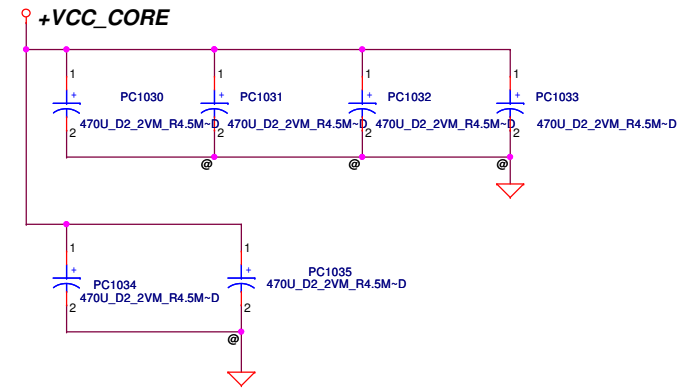
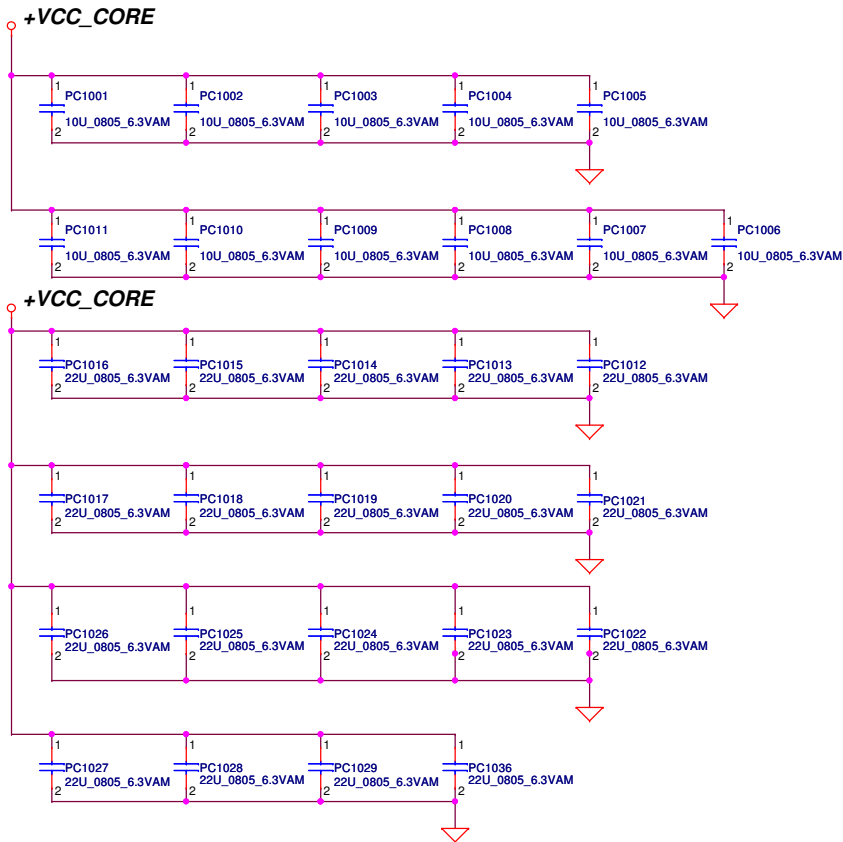
5 4 3 2 1

0 C B A

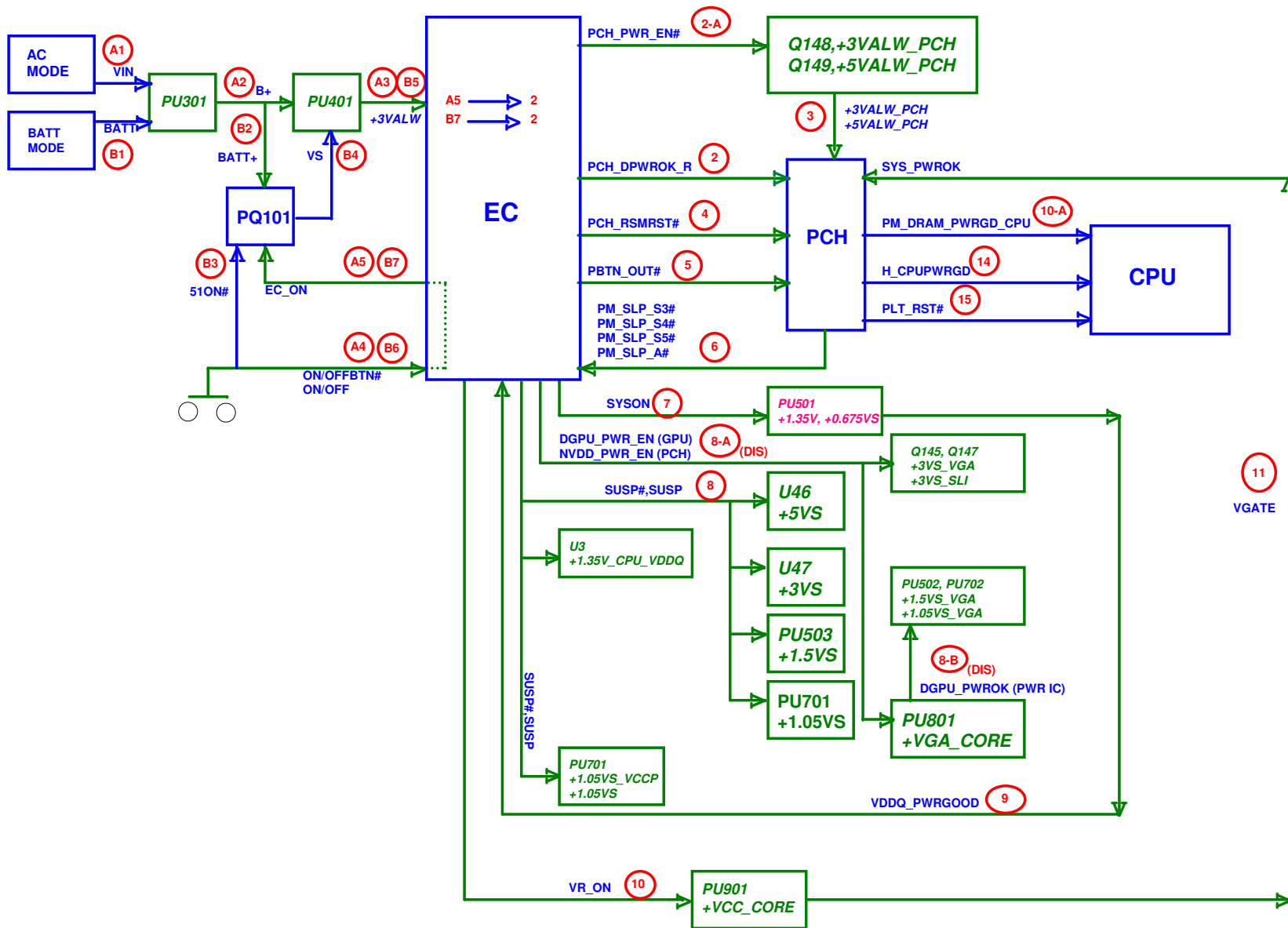


Mount for 47W

Based on PDDG rev 0.7 Table 5-1.




Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	PROCESSOR DECOUPLING	
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>					
Size	Custom	Document Number			Rev
				Y410 NM-A031	0.1
Date:	Wednesday, March 20, 2013		Sheet	66	of 69



HW PIR (Product Improve Record)

QIQY5 LA-8691P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2012/03/09

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01)	03/14	10	R64	Change R64 BOM structure from "@" to "DS3@"
				For Deep S3 Function

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	HW-PIR		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FORT DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom		
				Document Number		Rev
				Date: Wednesday, March 27, 2013		1.0
				Sheet 68 of 70		

Item	Reason for change	PG#	Modify List	Date	Phase
1		51		201109/27	B test
2				201109/27	B test
3		51		201109/27	B test
4		53		201109/27	B test
5		56		201109/27	B test
6		56		201109/27	B test
7		57		201109/27	B test
8		55/58		201109/27	B test
9		59		201109/27	B test
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/06/30	Deciphered Date	2012/12/31	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PIR (PWR)		
				Size	Document Number	Rev
				Custom	Y490-LA8691P	1.0
Date:				Wednesday, March 27, 2013	Sheet 69 of 70	