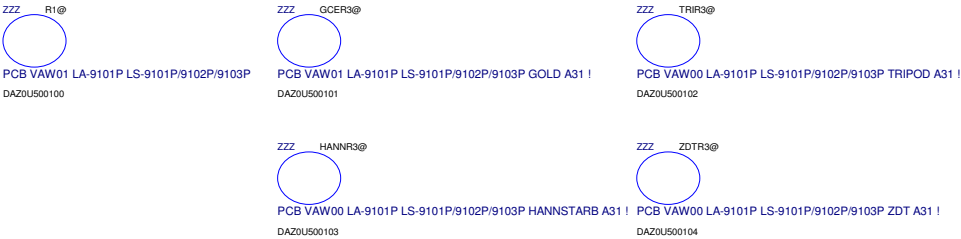


MODEL NAME : VAW01
PROJECT CODE : ANRVAW0100
PCB NO : LA-9101P (Mars Pro)

DA60000UT00 LA-9101P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B



Dell / Compal Confidential

Schematic Document

Intel Chief River
Ivy Bridge (BGA) + Panther Point
OAK 15" UMA/DIS AMD Mars Pro

2012-08-22
Rev: 0.4

46@ : for 46 level
@ : Nopop Component
CONN@ : Connector Component
KB9012@ : ENE KB9012 Implemented
UMA@ : Only for UMA
EMC@ : EMI/ESD parts

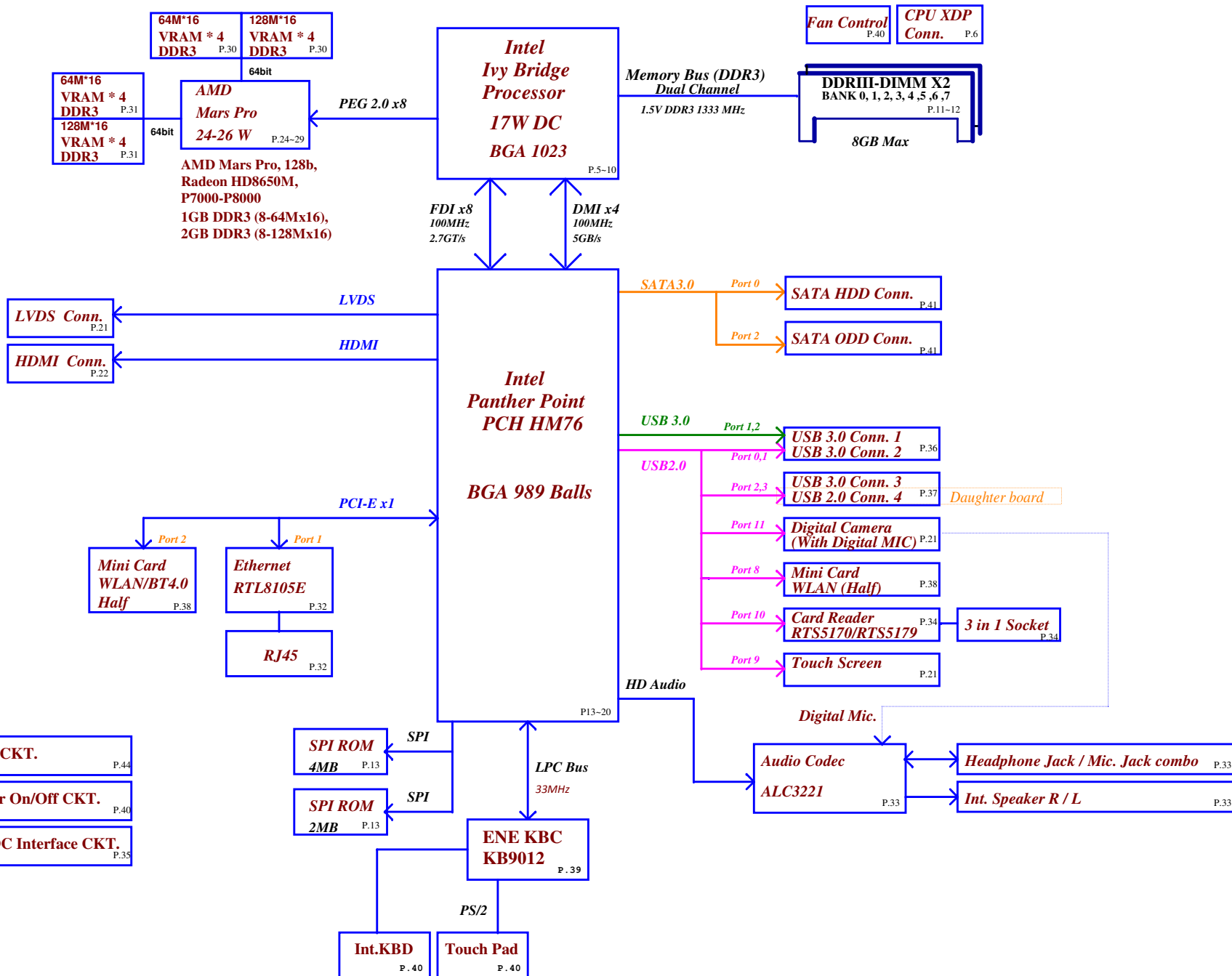
GCLK@ : Green CLK implemented
GCLKUMA@ : Green CLK for UMA
GCLKDIS@ : Green CLK for DIS
XTAL@ : X'tal implemented
XTALDIS@ : X'tal with DIS implemented

R1@ : R1 P/N
R3@ : R3 P/N

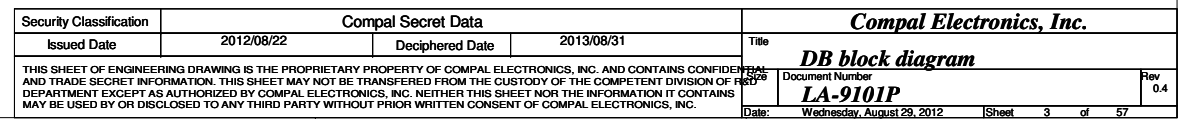
i3R1@ : CPU i3-3217 1.8G
i3VOSR1@ : CPU i3-2365 1.4G
i5R1@ : CPU i5-3317 1.7G
i7R1@ : CPU i7-3517 1.9G
CEL1R1@ : CPU Celeron 887 1.5G
PENR1@ : CPU Pentium 997 1.6G

DIS@ : Only for Discrete
TH@/THR1@ : Thames-XT
MS@/MSR1@ : Mars Pro
X76@ :
SPI-ROM & VRAM Group

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Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title	Cover Page
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				Date	Wednesday, August 28, 2012
				Sheet	1 of 57
				Rev	0.4



Project Code : VAW01
File Name : LA-9101P



Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

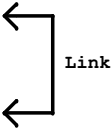
ID	PCB Revision
0	0.1
1	0.1
2	0.2
3	0.2
4	0.3
5	0.4
6	1.0
7	1.0
UMA	THM
MARS	

Project ID Table

ID	Project Revision
0	
1	
2	
3	
4	
5	UMA
6	DIS THAMES
7	DIS MARS PRO

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	



CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100 LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

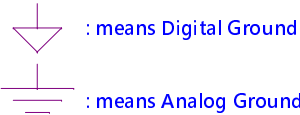
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

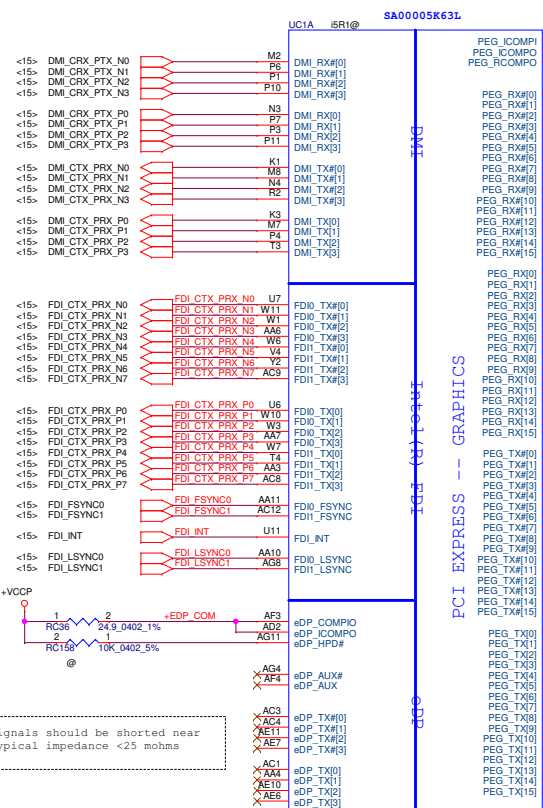
SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

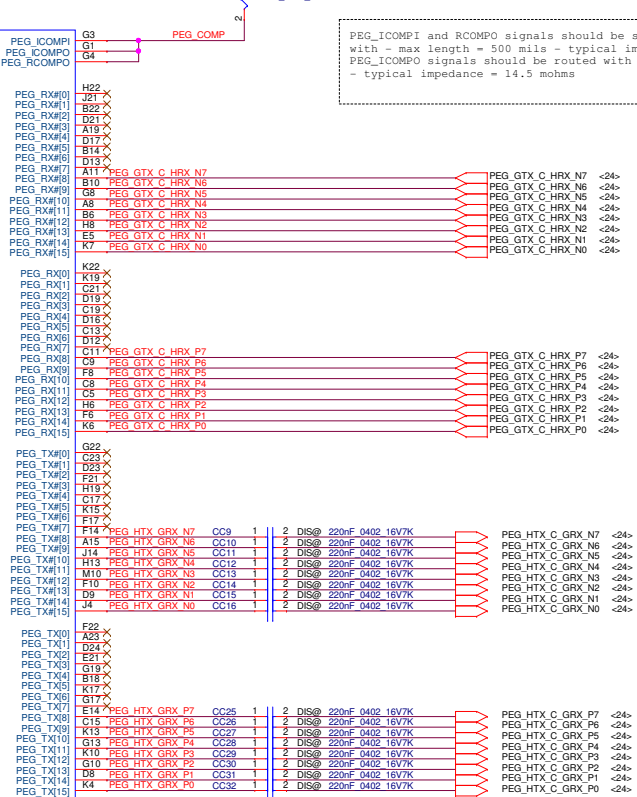
PCH	USB PORT#	DESTINATION
	0	USB conn.2
	1	USB conn.1
	2	USB conn.3
	3	USB conn.4 (DB)
	4	NC
	5	NC
	6	NC
	7	NC
	8	MINI CARD (WLAN)
	9	Touch Screen
	10	Card Reader
	11	Camera
	12	NC
	13	NC

Symbol Note :

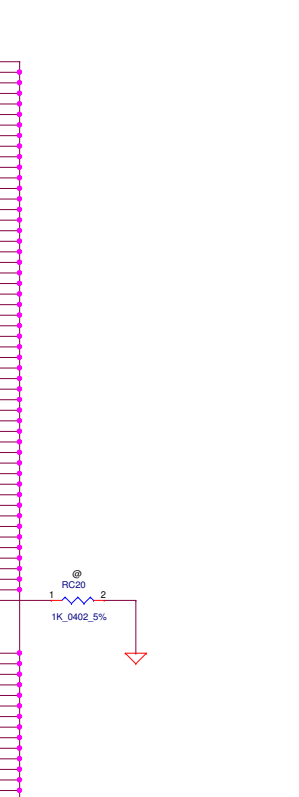
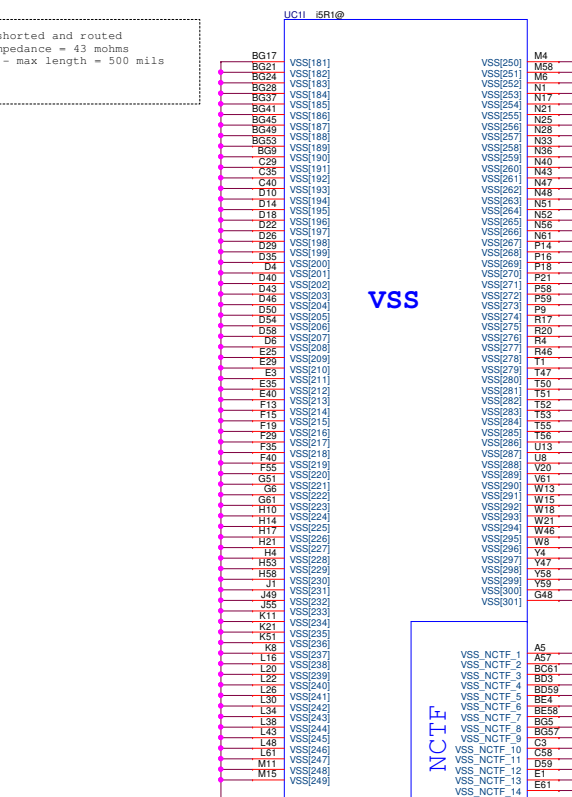




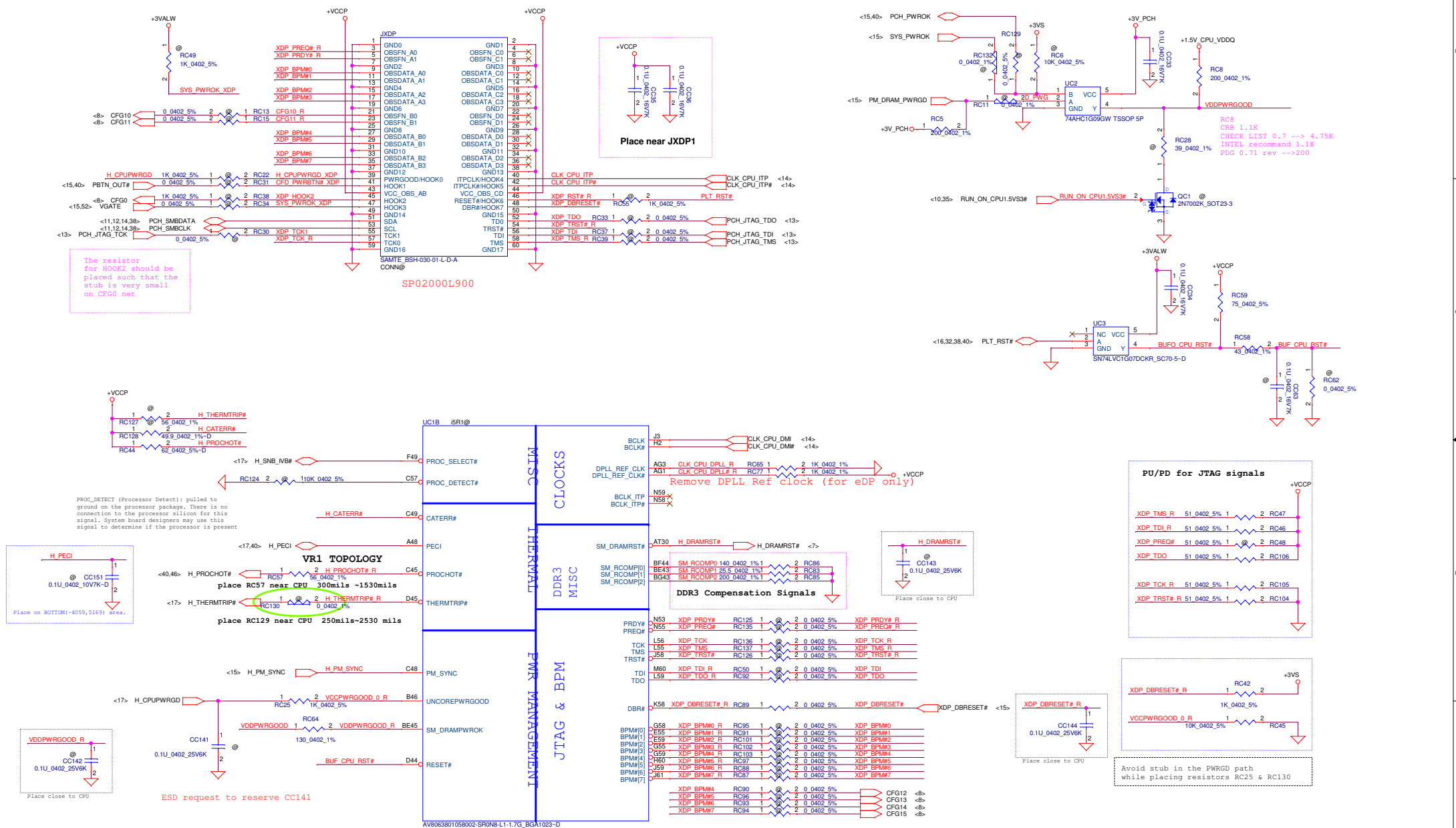
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

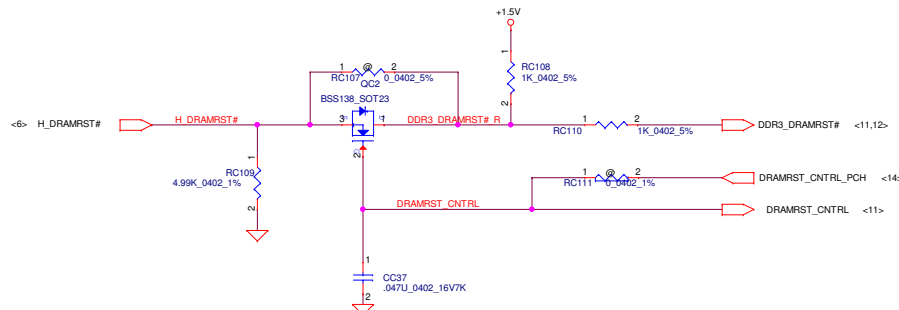
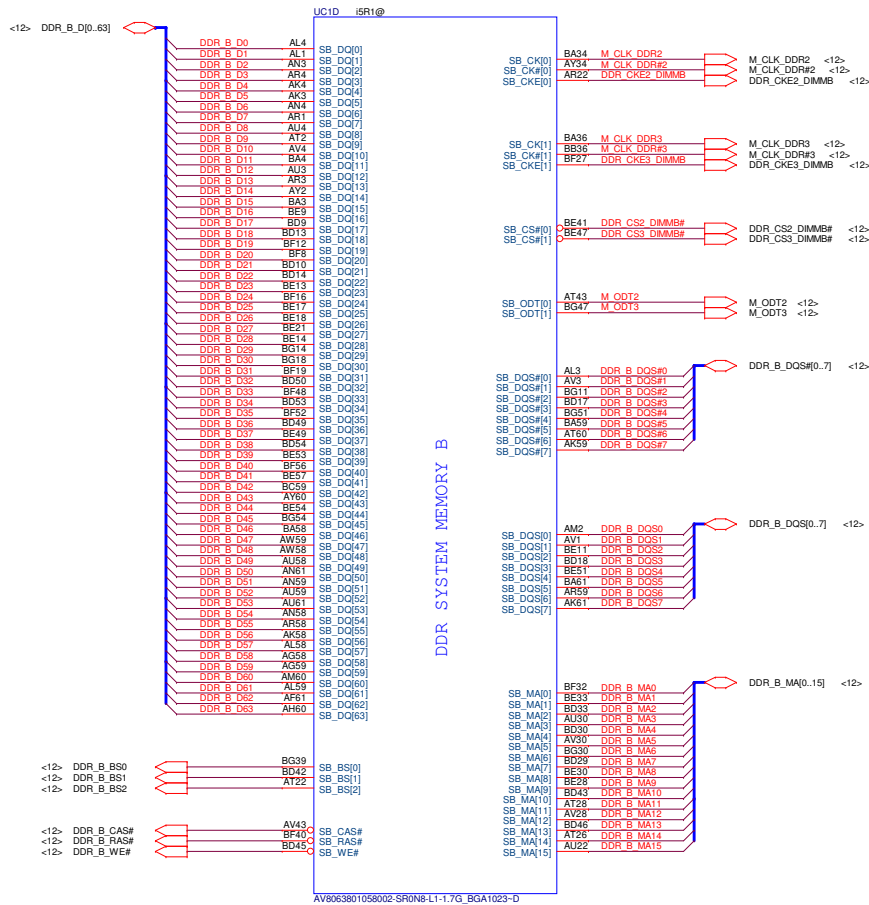
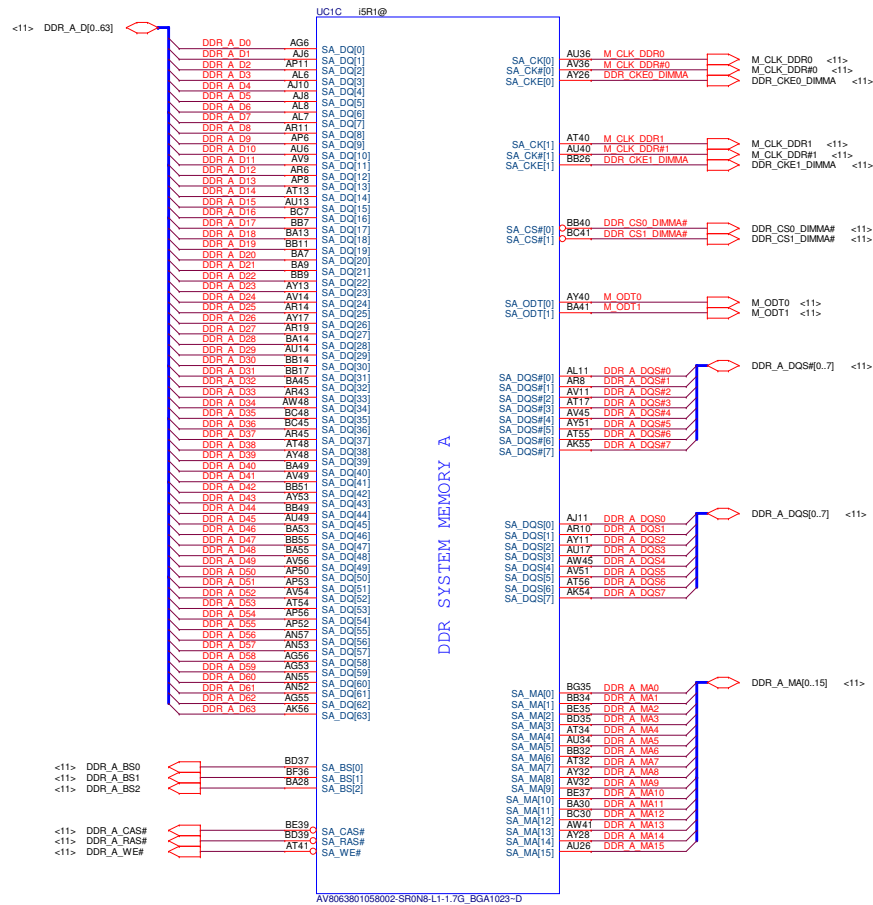


PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

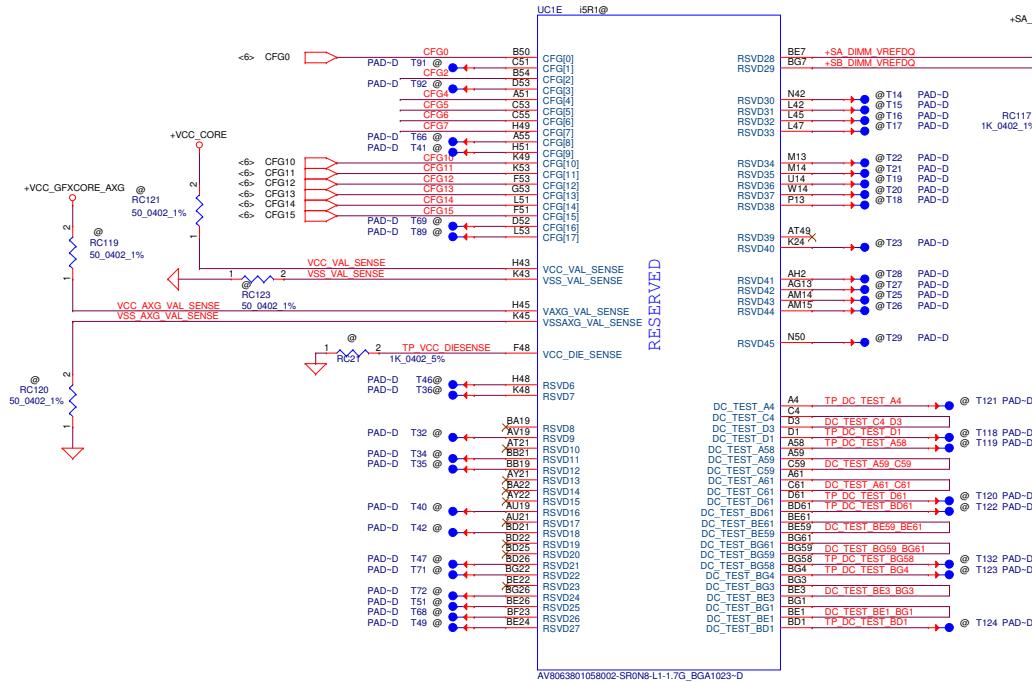


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Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title	PROCESSOR(1/6) DMI,FDI,PEG	
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				LA-9101P	0.4	
Date:				Wednesday, August 29, 2012	Sheet	5 of 57





CFG Straps for Processor



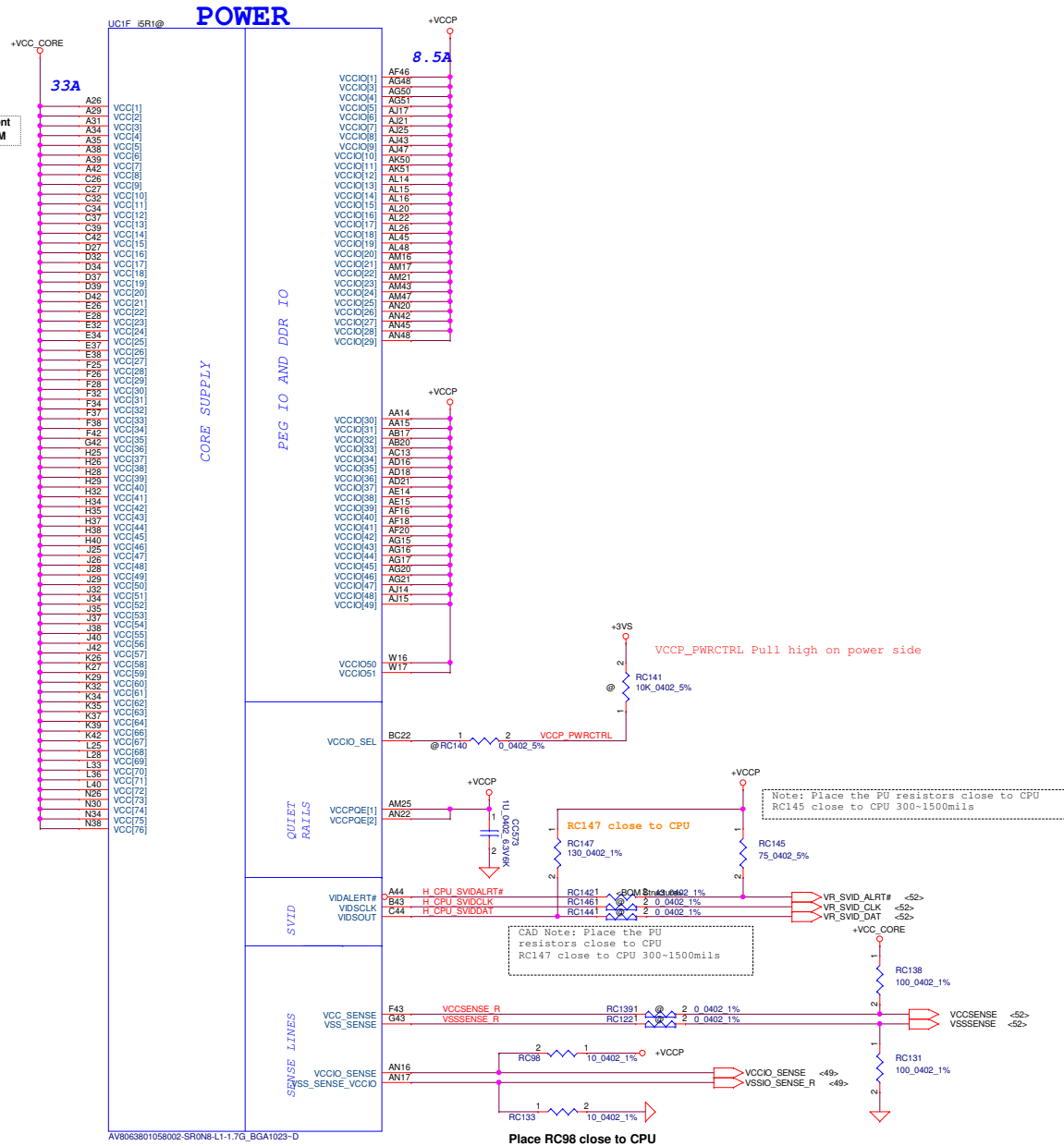
CFG2	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled * 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

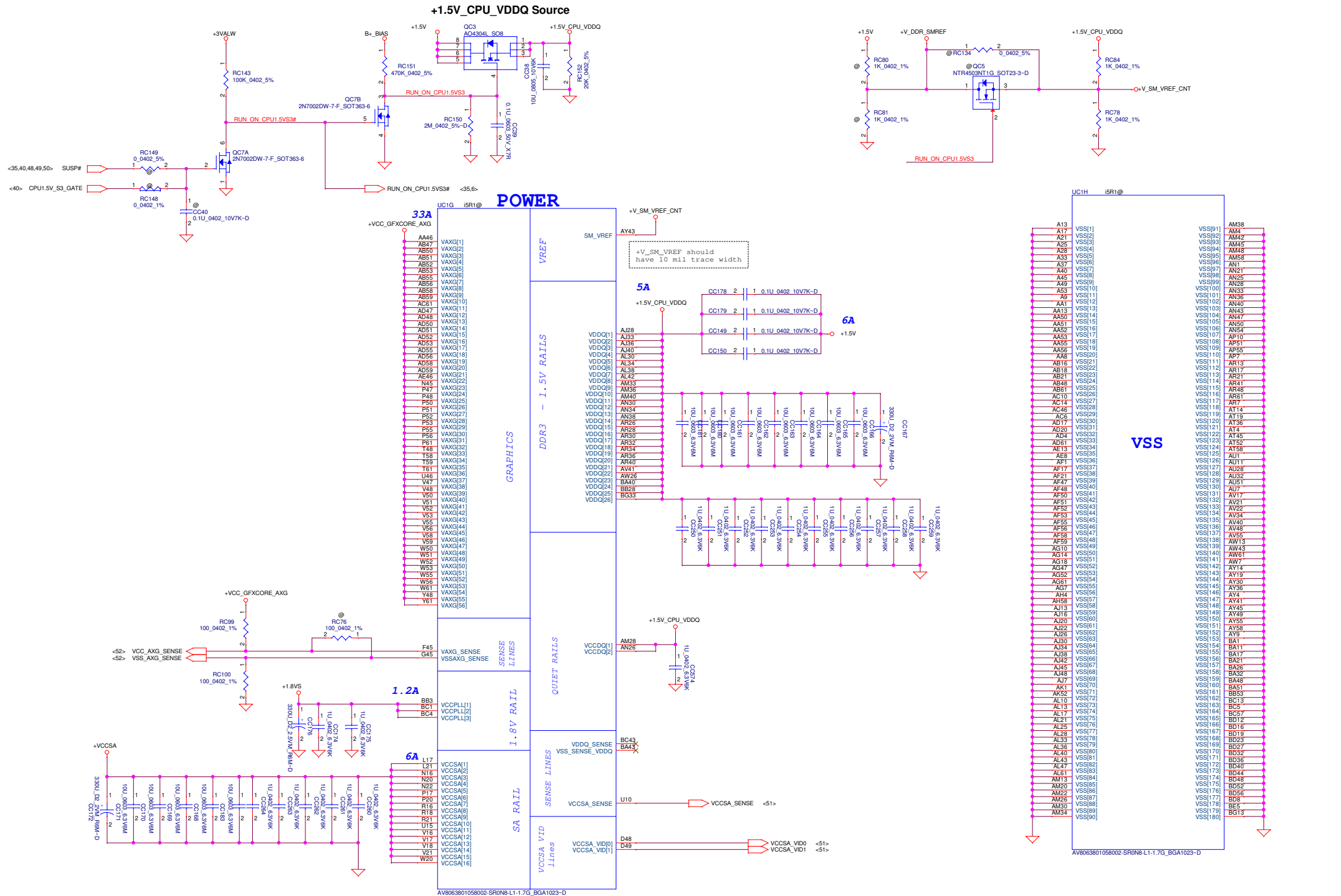
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

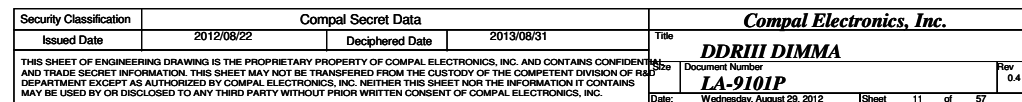
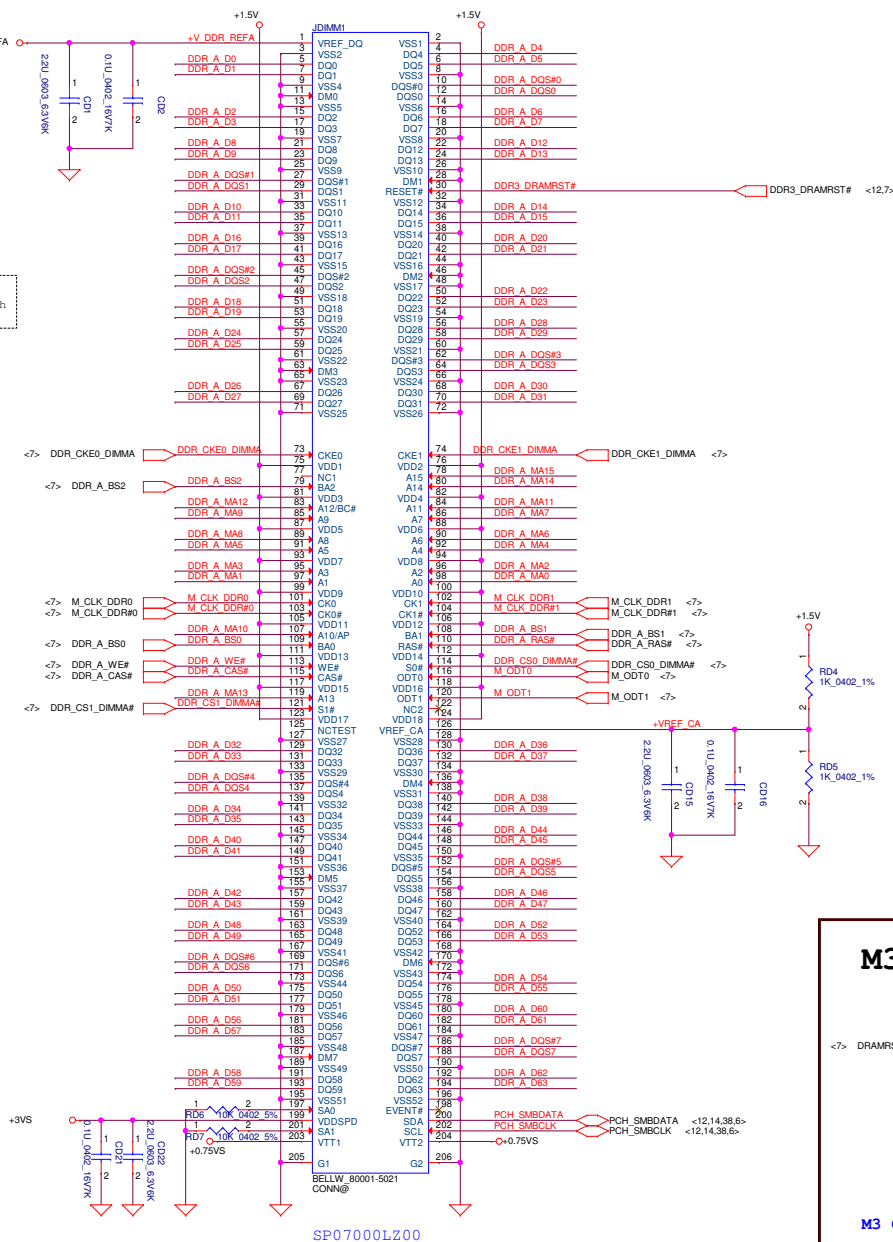
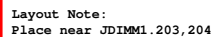
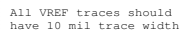
ULV 17W , Max Current
in Turbo Mode or HFM

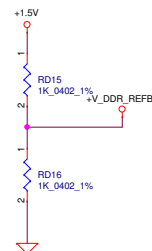


Iccmax current changed for PBDG Rev0.7

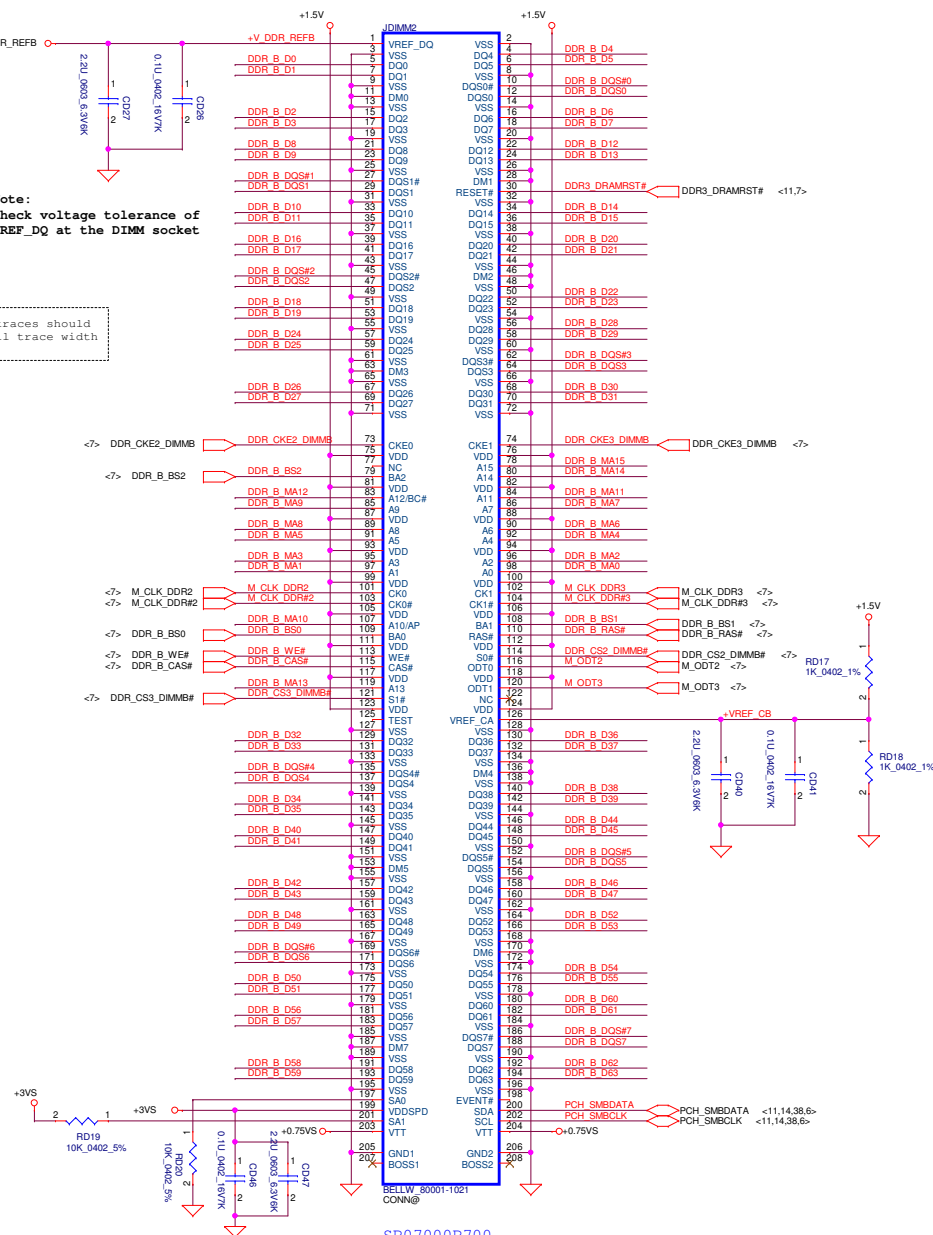
CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0-1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *
★ Description		
5A to Mem controller (+1.5V_CPU_VDDQ)		
5-6A to 2 DIMMs/channel		
2-5A to +1.5V_RUN & +0.75V_DDR_VTT		



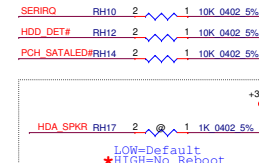
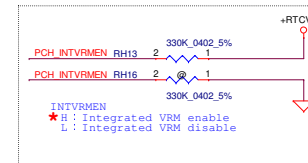
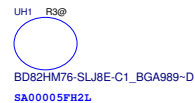
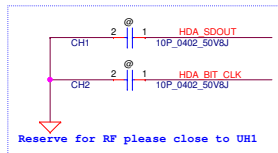
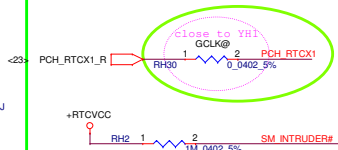
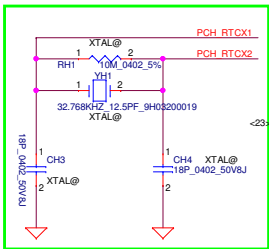




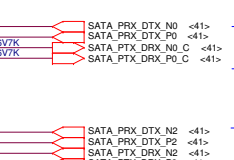
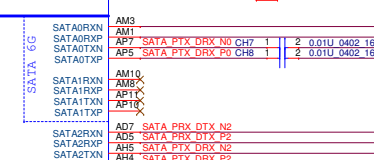
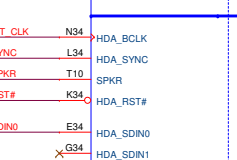
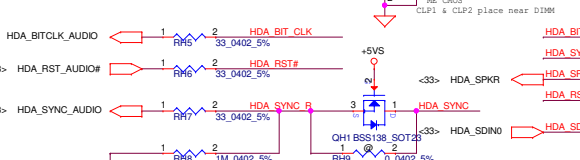
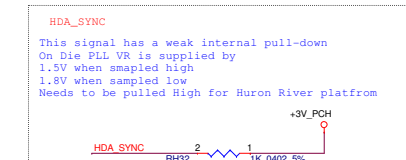
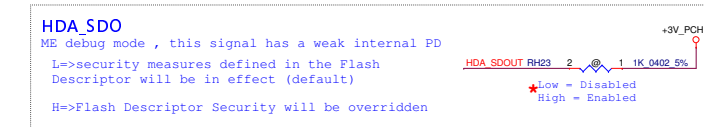
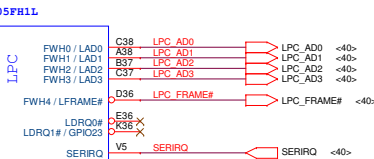
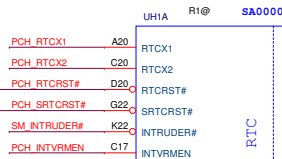
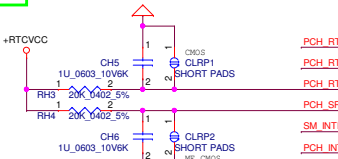
All VREF traces should have 10 mil trace width



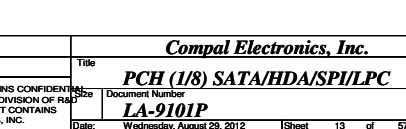
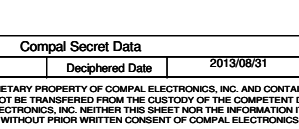
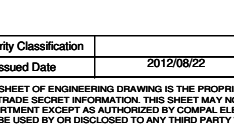
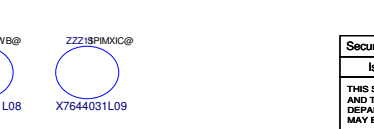
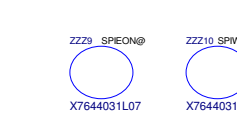
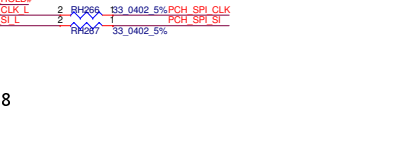
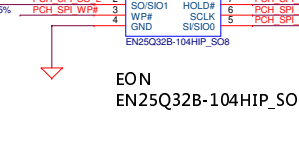
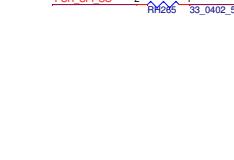
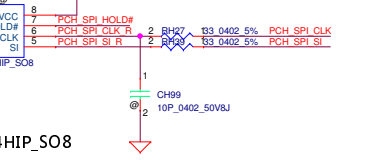
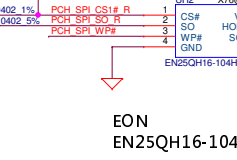
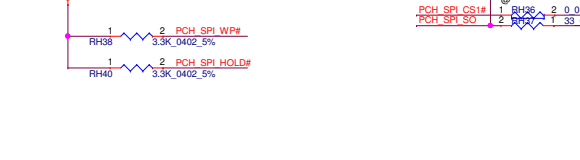
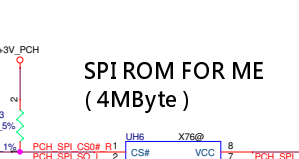
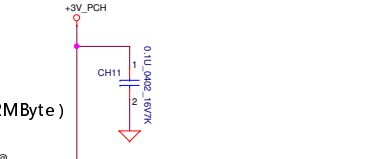
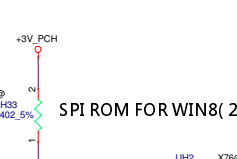
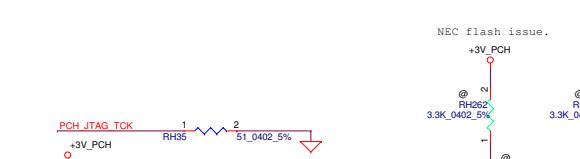
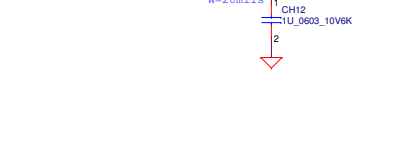
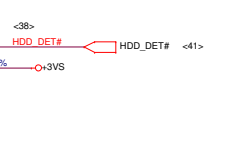
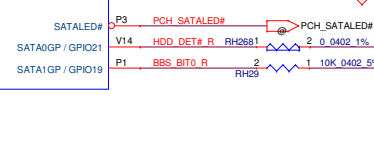
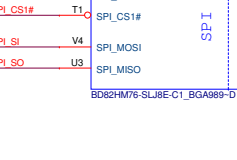
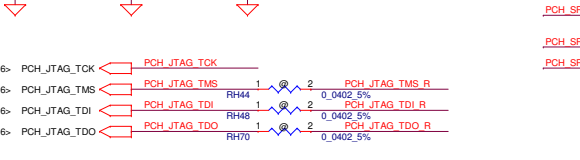
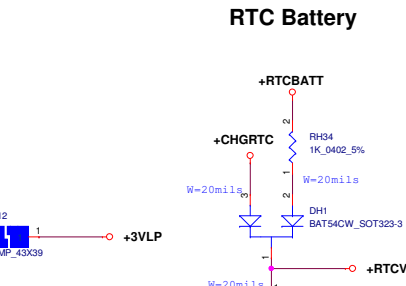
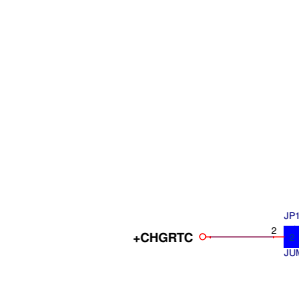
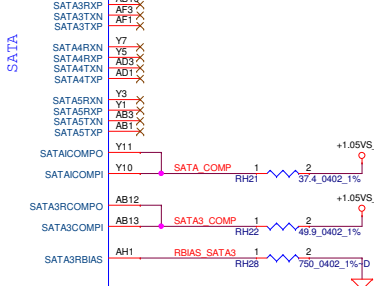
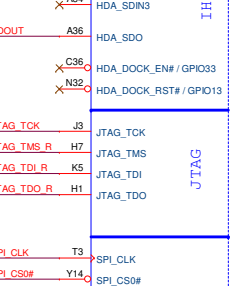
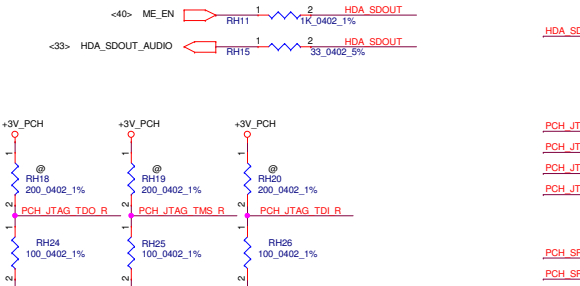
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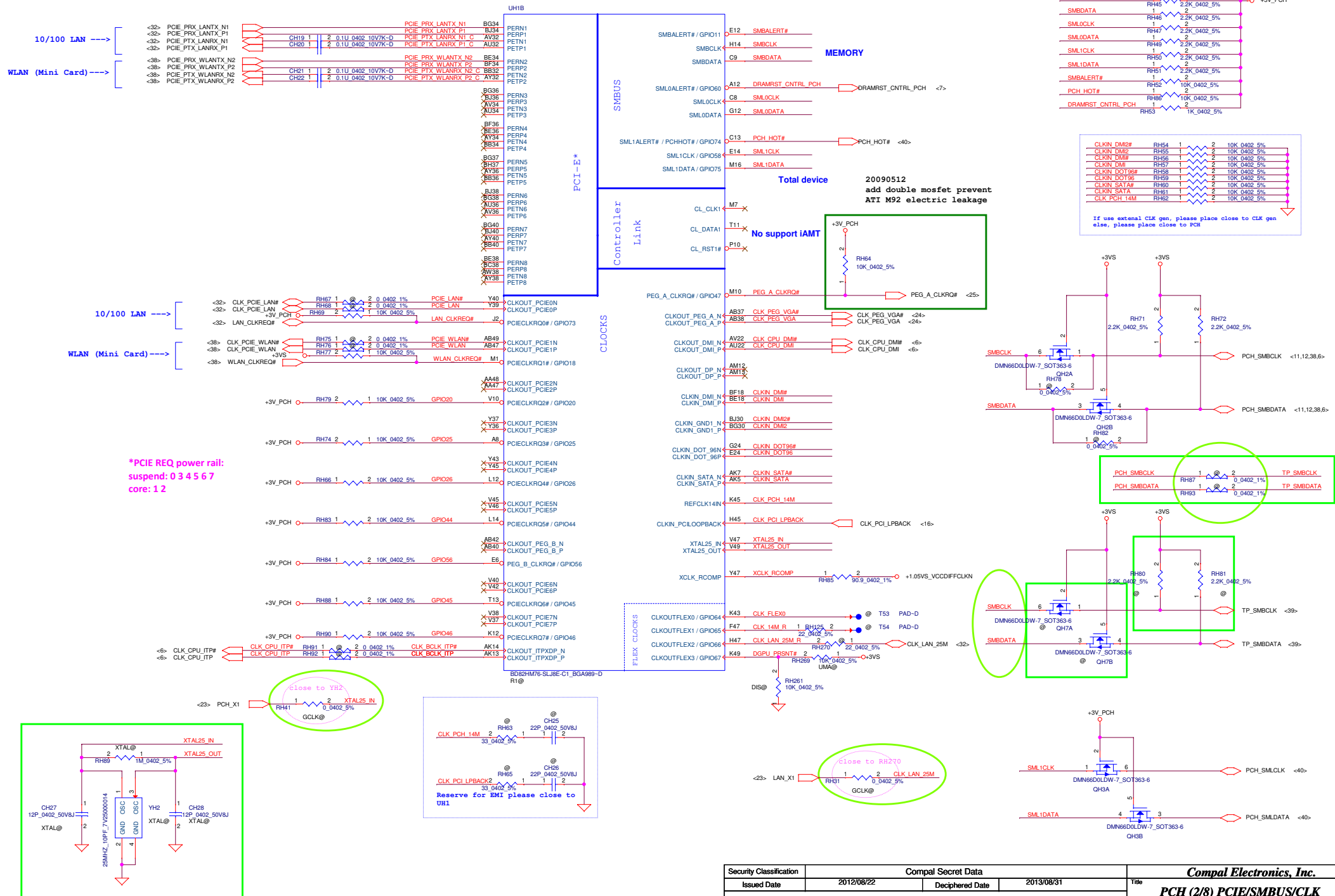
keep away hot spot

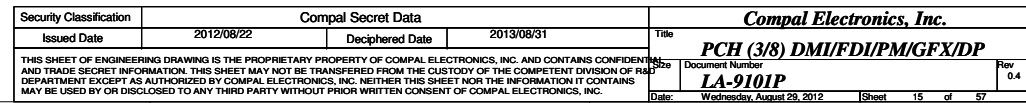


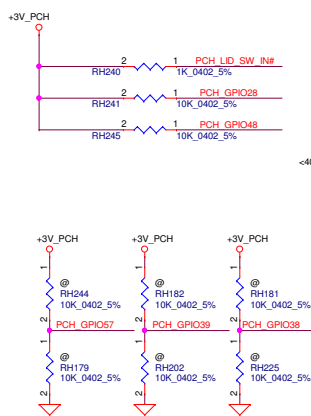
RTC Battery



Security Classification		Compal Secret Data		Title	
Issued Date	2012/08/22	Deciphered Date	2013/08/31	PCH (I/8) SATA/HDA/SPI/LPC	
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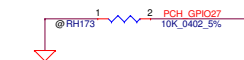
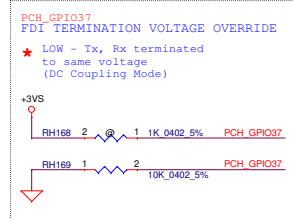
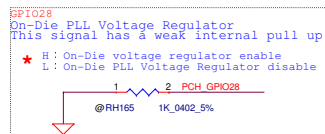




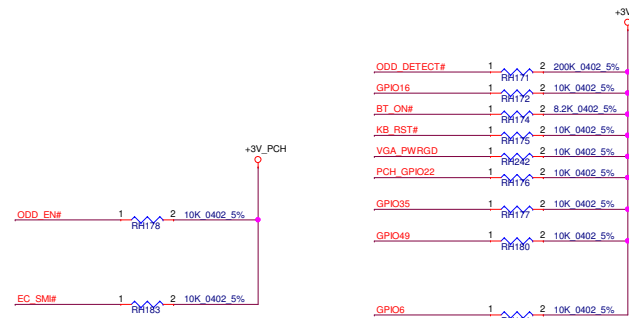
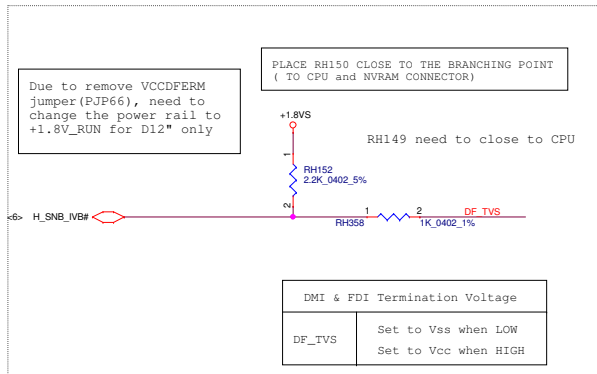
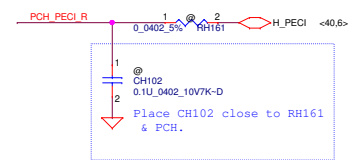
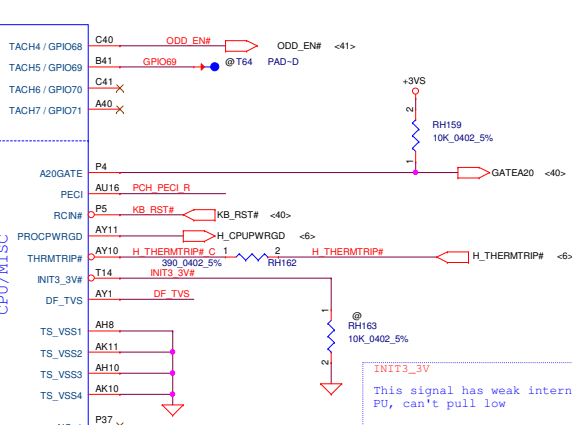
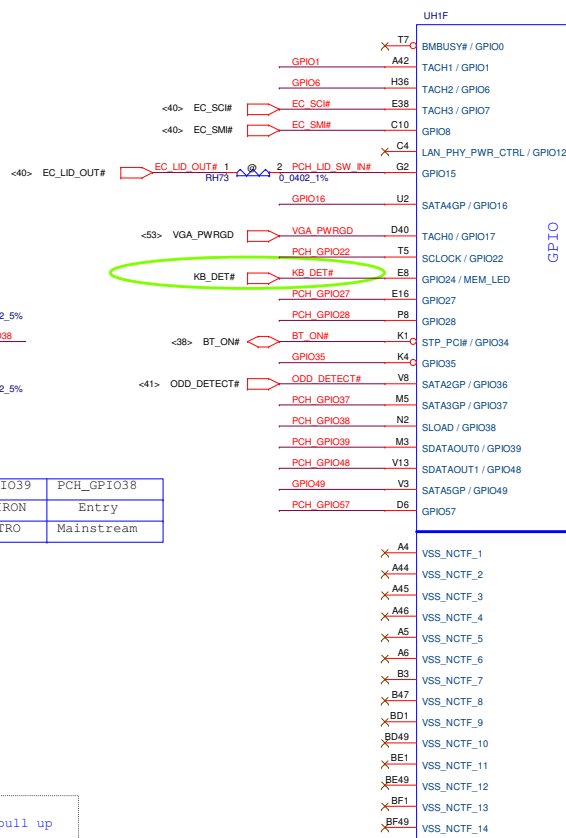


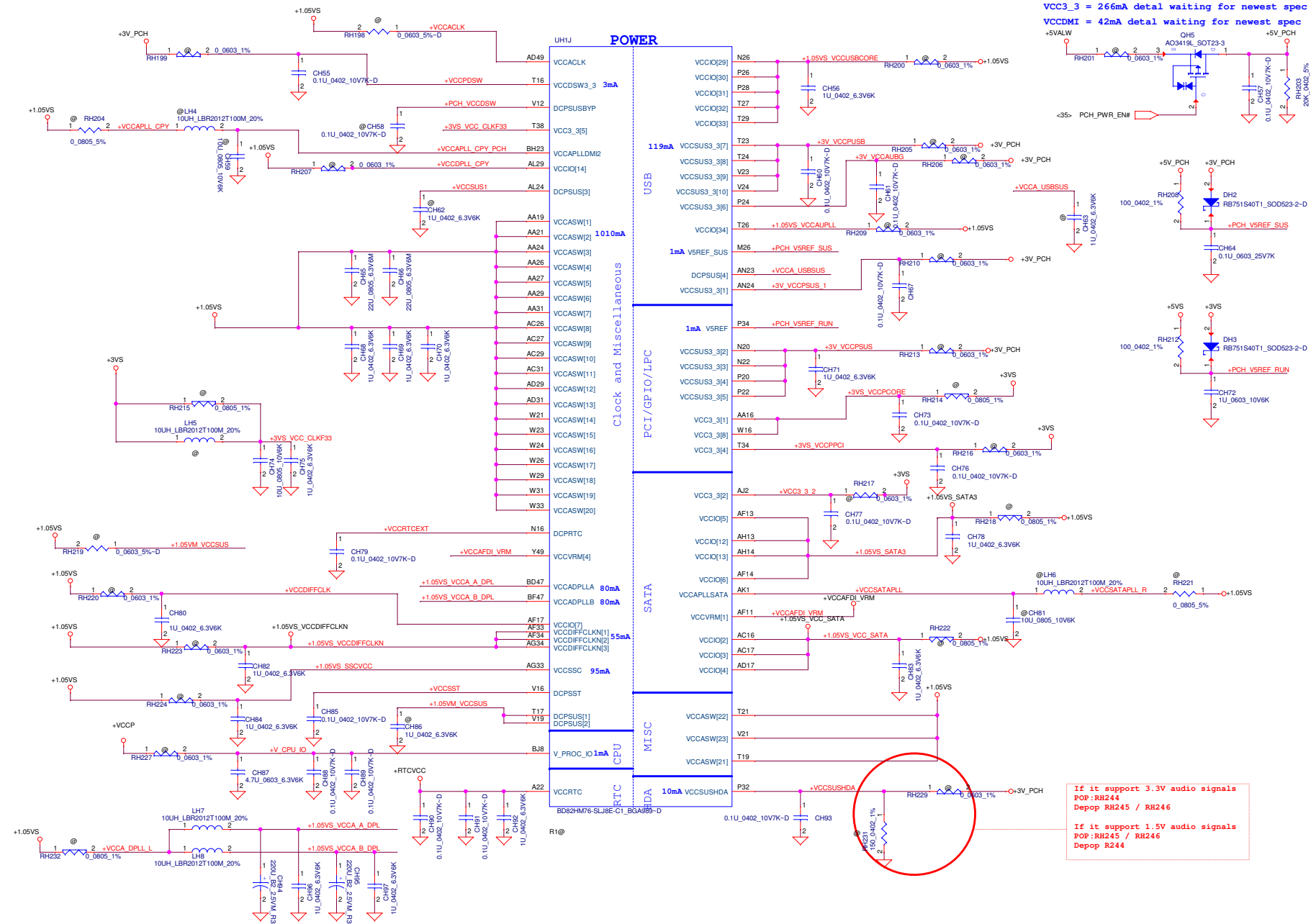
System ID

	PCH_GPIO57	PCH_GPIO39	PCH_GPIO38
LOW	VAW00 15''	INSPIRON	Entry
HIGH	VAW10 17''	VOSTRO	Mainstream



PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16
Please refer to Huron River Debug Board DG 0.5

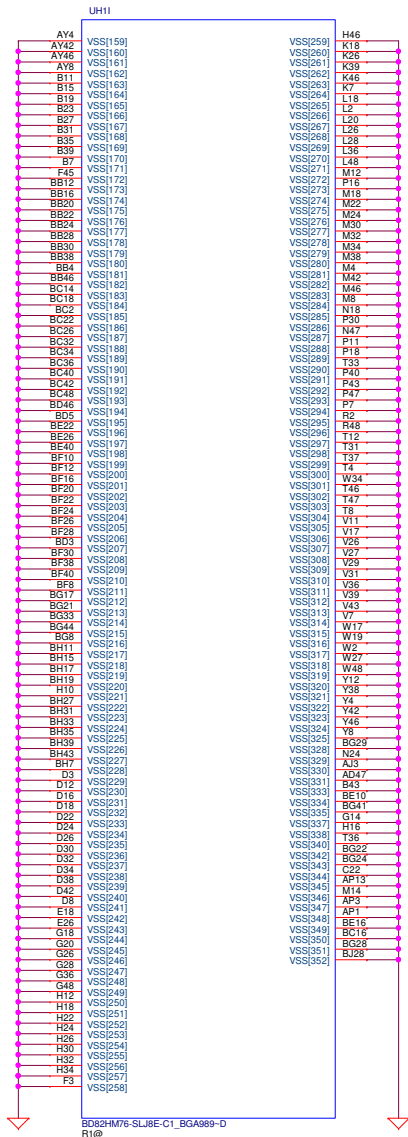




VCC3_3 = 266mA detail waiting for newest spec
VCCDMI = 42mA detail waiting for newest spec

If it support 3.3V audio signals
POP: RH244 / RH246
Depop RH244 / RH246

If it support 1.5V audio signals
POP: RH245 / RH246
Depop R244



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LCD_PWR_CTRL

The schematic diagram for the LCD_PWR_CTRL circuit shows the following components and connections:

- Inputs:**
 - <15> PCH_ENVDD (pin 2)
 - <40> EC_ENVDD (pin 3)
 - +LCDVDD (pin 1)
 - +5VALW (pin 2)
 - +3V3 (pin 3)
- Outputs:**
 - +LCDVDD (pin 1)
 - +LCDVDD (pin 1)
- Components:**
 - MOSFETs: DV7, QV3 (2N7002B), QV4 (AO3419L), OV5 (BSS138)
 - Resistors: RV14 (100_0402_1%), RV15 (47K_0402_5%), RV17 (56K_0402_5%), RV18 (10K_0402_5%)
 - Capacitors: CV19 (0.1u_0402_16VTK), CV20 (4.7u_0805_10V4Z), CV21 (0.1u_0402_16VTK)
- Design Parameters:**
 - Width: W=60mils

The schematic diagram illustrates the LCD backlight power control circuit. It features two MOSFETs, QV6 (Si3457CDV-T1-E3, TSOP6-D) and QV7 (2N7002BKW_SOT323-D), which are used to switch the power to the LCD backlight. The circuit includes several resistors (RV25, RV26, RV27, RV28, RV31, RV32, RV33, RV34, RV35, RV36, RV37, RV38, RV39, RV40, RV41, RV42, RV43, RV44, RV45, RV46, RV47, RV48, RV49, RV50, RV51, RV52, RV53, RV54, RV55, RV56, RV57, RV58, RV59, RV60, RV61, RV62, RV63, RV64, RV65, RV66, RV67, RV68, RV69, RV70, RV71, RV72, RV73, RV74, RV75, RV76, RV77, RV78, RV79, RV80, RV81, RV82, RV83, RV84, RV85, RV86, RV87, RV88, RV89, RV90, RV91, RV92, RV93, RV94, RV95, RV96, RV97, RV98, RV99, RV100) and capacitors (CV25, CV26, CV27, CV28, CV29, CV30, CV31, CV32, CV33, CV34, CV35, CV36, CV37, CV38, CV39, CV40, CV41, CV42, CV43, CV44, CV45, CV46, CV47, CV48, CV49, CV50, CV51, CV52, CV53, CV54, CV55, CV56, CV57, CV58, CV59, CV60, CV61, CV62, CV63, CV64, CV65, CV66, CV67, CV68, CV69, CV70, CV71, CV72, CV73, CV74, CV75, CV76, CV77, CV78, CV79, CV80, CV81, CV82, CV83, CV84, CV85, CV86, CV87, CV88, CV89, CV90, CV91, CV92, CV93, CV94, CV95, CV96, CV97, CV98, CV99, CV100) for timing and filtering. The circuit is powered by a +LCDVDD source and a +INV_PWR_SRC source. The output of the circuit is connected to the LCD backlight. The schematic is labeled with dimensions 60mil and 60mil.

*** Reserved for EMI/ESD/RF
need to close to JLVDS**

5P_0402_50V8C CV27
1 2 LVDS_BCLK-
5P_0402_50V8C CV28
1 2 LVDS_BCLK+
RV229 1 2
0_0402_1%
RV230 1 2
100K_0402_5%
CV30 1 2
680P_0402_50V7K

VGA_PWM
RV_PWM
RV229
0_0402_1%
RV230
100K_0402_5%
CV30
680P_0402_50V7K

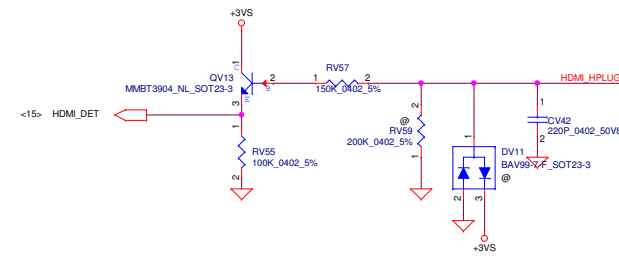
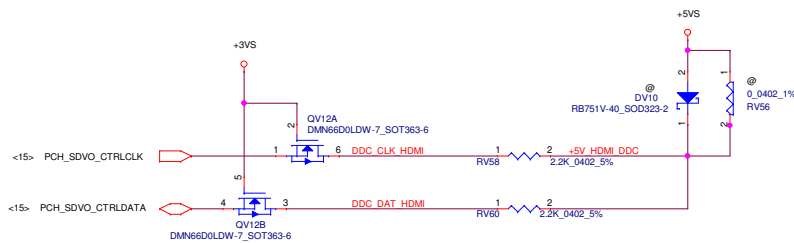
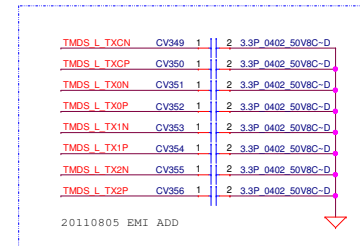
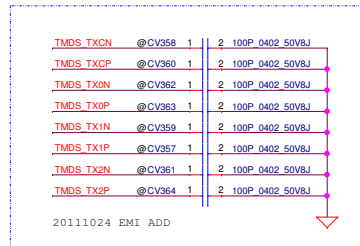
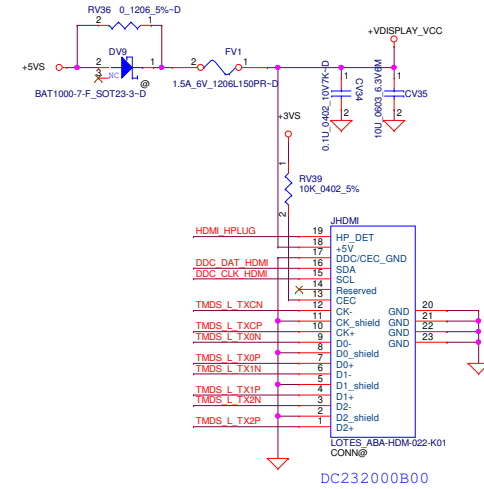
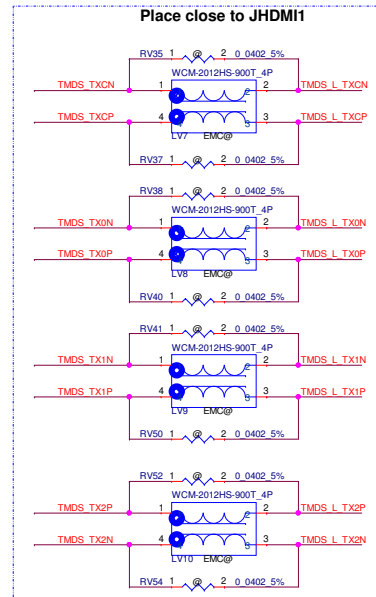
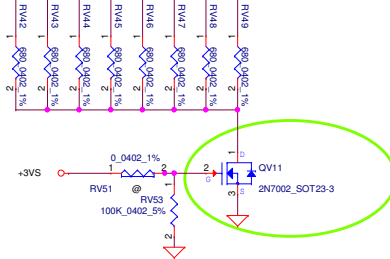
*** Reserved for EMI/ESD/RF
need to close to JLVDS**

MIC_CLK_R 6
V I/O V I/O
+5VSD 5
V BUS Ground 2
MIC_DATA 4
V I/O V I/O
P4223C26_S06-D
1 2 3
USB20_CAM P11_R
USB20_CAM N11_R

[illegible]

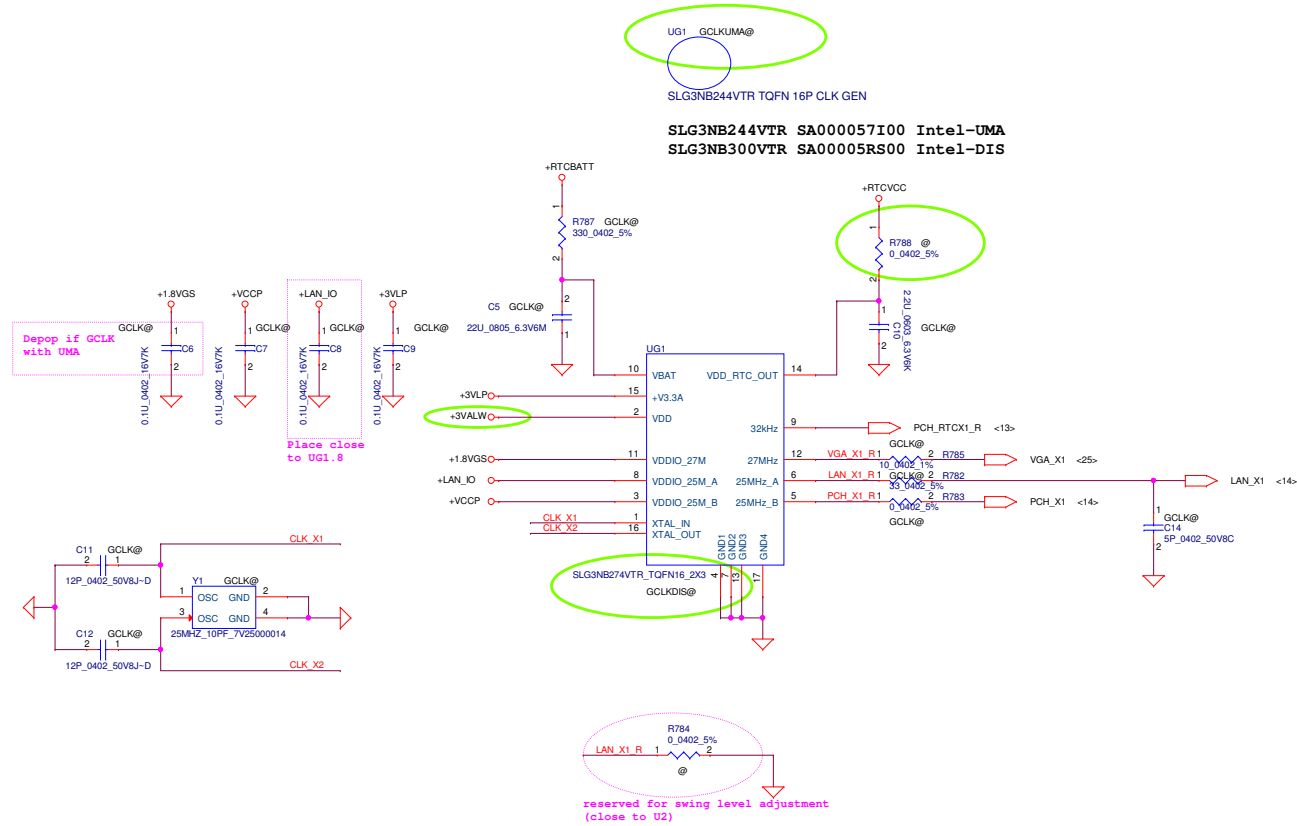
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Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title	LVDS/webcam	
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<15> HDMI_A3N_VGA CV32 2 1 0.1U 0402 10V7K-D TMD5 TXCN
 <15> HDMI_A3P_VGA CV33 2 1 0.1U 0402 10V7K-D TMD5 TXCP
 <15> HDMI_A0N_VGA CV36 2 1 0.1U 0402 10V7K-D TMD5 TX0N
 <15> HDMI_A0P_VGA CV37 2 1 0.1U 0402 10V7K-D TMD5 TX0P
 <15> HDMI_A1N_VGA CV38 2 1 0.1U 0402 10V7K-D TMD5 TX1N
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 <15> HDMI_A2N_VGA CV40 2 1 0.1U 0402 10V7K-D TMD5 TX2N
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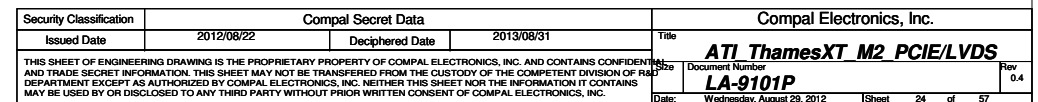
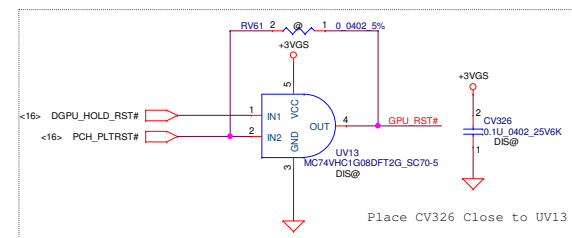


Part Number	Description
46@	ROYALTY HDMI W/LOGO
8000000023M	HDMI W/Logo:8000000023M

Security Classification	2012/08/22	Deciphered Date	2013/08/31	Title	HDMI
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Document Number	LA-9101P
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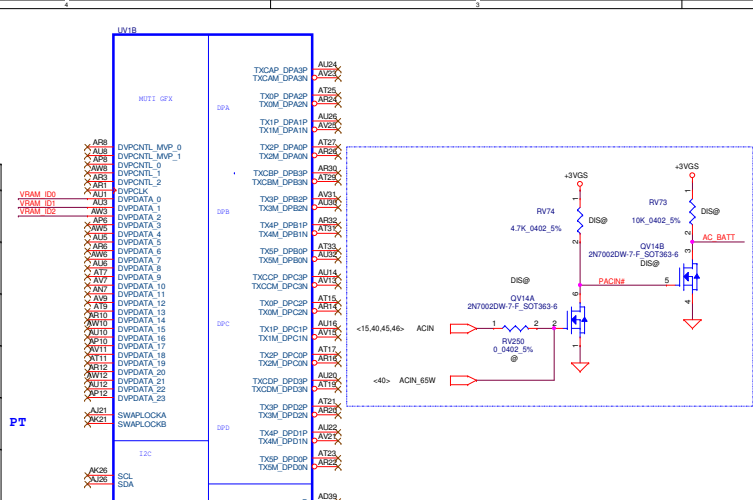


UVIG			
LVDS CONTROL	VARY BL DIGION	AK27 AJ27	
		AK35 AJ38	
	TXCLK_UP_DPFP3 TXCLK_UN_DPFP3N	AJ38 AK37	
	TXOUT_U0P_DPFP2 TXOUT_U0N_DPFP2N	AJ38 AK37	
	TXOUT_U1P_DPFP1 TXOUT_U1N_DPFP1N	AH35 AJ38	
	TXOUT_U2P_DPFP0 TXOUT_U2N_DPFP0N	AG38 AH37	
	TXOUT_U3P TXOUT_U3N	AF35 AG36	
	LVTDNP		AP34 AF37
		TXCLK_LP_DPFP3 TXCLK_LN_DPFP3N	AW37 AU35
TXOUT_LP_DPFP2 TXOUT_LN_DPFP2N		AR37 AU39	
TXOUT_L1P_DPFP1 TXOUT_L1N_DPFP1N		AP35 AR35	
TXOUT_LP_DPFP0 TXOUT_LN_DPFP0N		AN36 AP37	
TXOUT_L3P TXOUT_L3N			

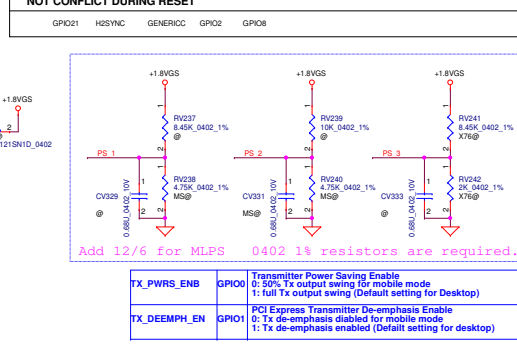
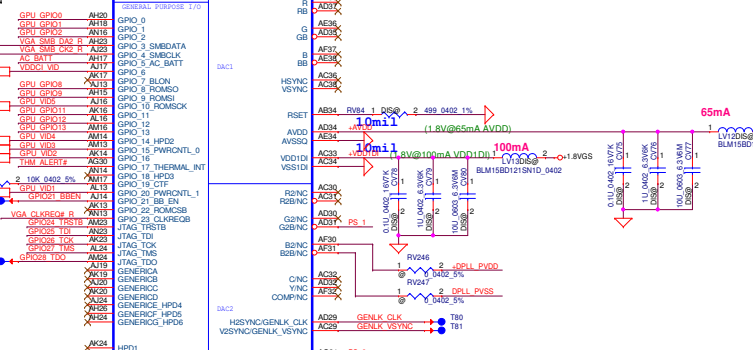
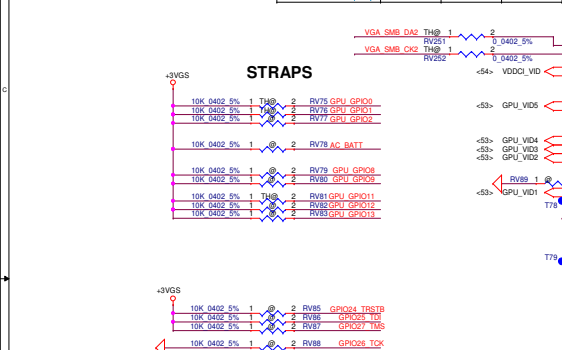


ZZ28 Sam1GR1@	ZZ24 Sam1GR3@
X7644031L01	X7644031L10
ZZ25 Micron1GR1@	ZZ23 Micron1GR3@
X7644031L02	X7644031L11
ZZ27 Sam2GR1@	ZZ22 Sam2GR3@
X7644031L05	X7644031L12
ZZ26 Hyn2GR1@	ZZ21 Hyn2GR3@
X7644031L06	X7644031L13

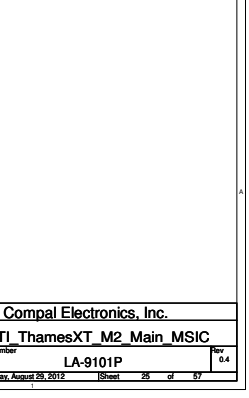
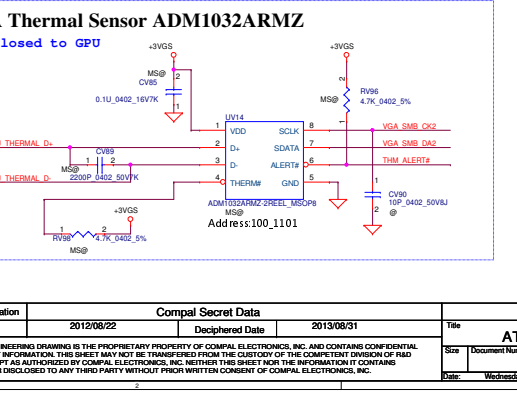
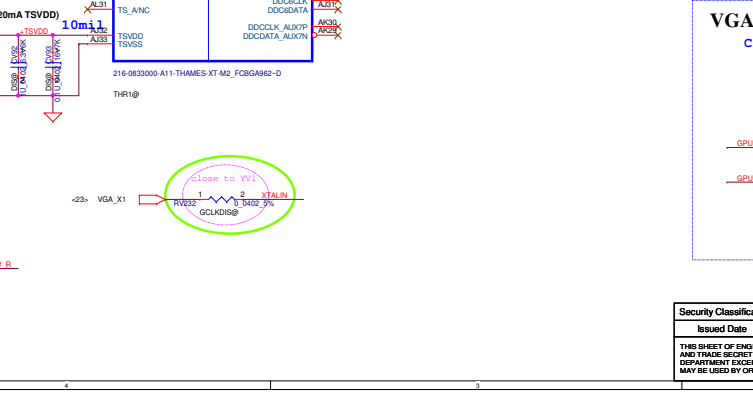
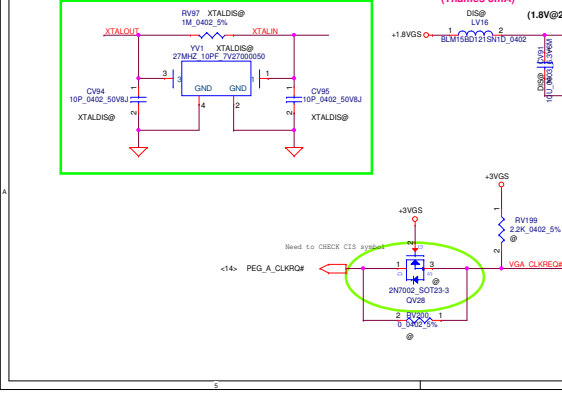
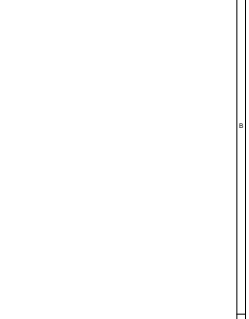
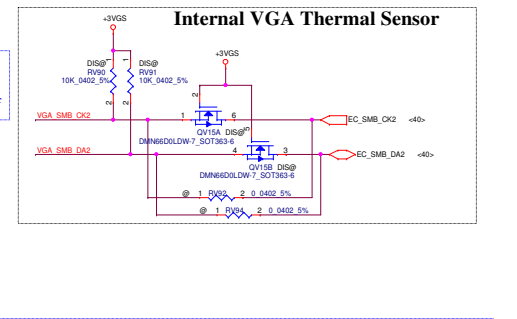
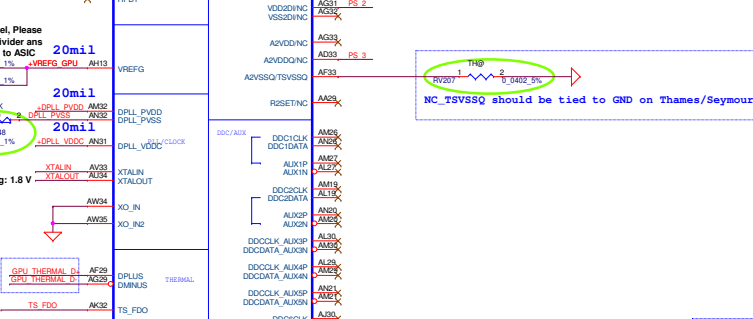
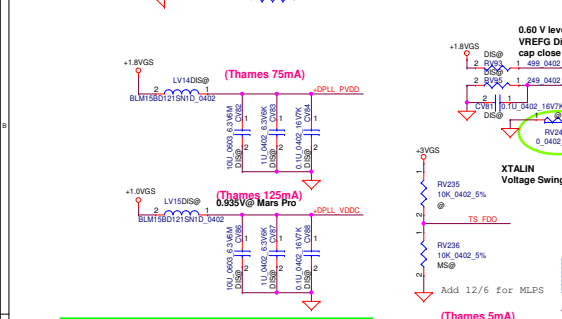
Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
SA00004GSL1(R1)	RV68	RV69	RV72
SA00004GSL1(R3)	0	1	0
Hynix 1GB SA00004Y21L(R1)	RV67	RV70	RV72
SA00004Y21L(R3)	1	0	1
Samsung 2GB SA00005SH0L(R1)	RV68	RV69	RV71
SA00005SH0L(R3)	0	1	1
Hynix 2GB SA00003Y02L(R1)	RV67	RV70	RV71
SA00003Y02L(R3)	1	0	1
Micron 2GB SA00005XB0L(R1)			
SA00005XB0L(R3)			



CONFIGURATION STRAPS			ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET		RECOMMENDED SETTINGS	
STRAPS	PN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS	RECOMMENDED SETTINGS		
TX_PWRS_ENB	GPI00	PCI FULL TX OUTPUT SWING	0: 50% swing 1: Pull swing	X		
TX_DEEMPH_EN	GPI01	PCI TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X		
RSVD	GPI02	Advertises PCIe speed when compliance test	0: 2.5GT/s 1: 5GT/s	0		
RSVD	GPI08	RESERVED		0		
BIF_VGA_DIS	GPI09	VGA ENABLED		0		
RSVD	GPI021	RESERVED		0		
BIOS_ROM_EN	GPI0_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X		
ROMDCFG(2:0)	GPI0(3:1:1)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX		
VP_DEVICE_STRAP_BNA	V2SYNC	IGNORE VIP DEVICE STRAPS		0		
RSVD	HSYNCR			0		
RSVD	GENERICC			0		
ALD[1]	HSYNCR	Audio[1] Audio[0]	0: 0 No audio function 1: 1 Audio for DisplayPort and HDMI if dongle is detected 1: 0 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI	11		
ALD[0]	VSYNCR					
AMD RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET						
GPI021	HSYNCR	GENERICC	GPI02	GPI08		



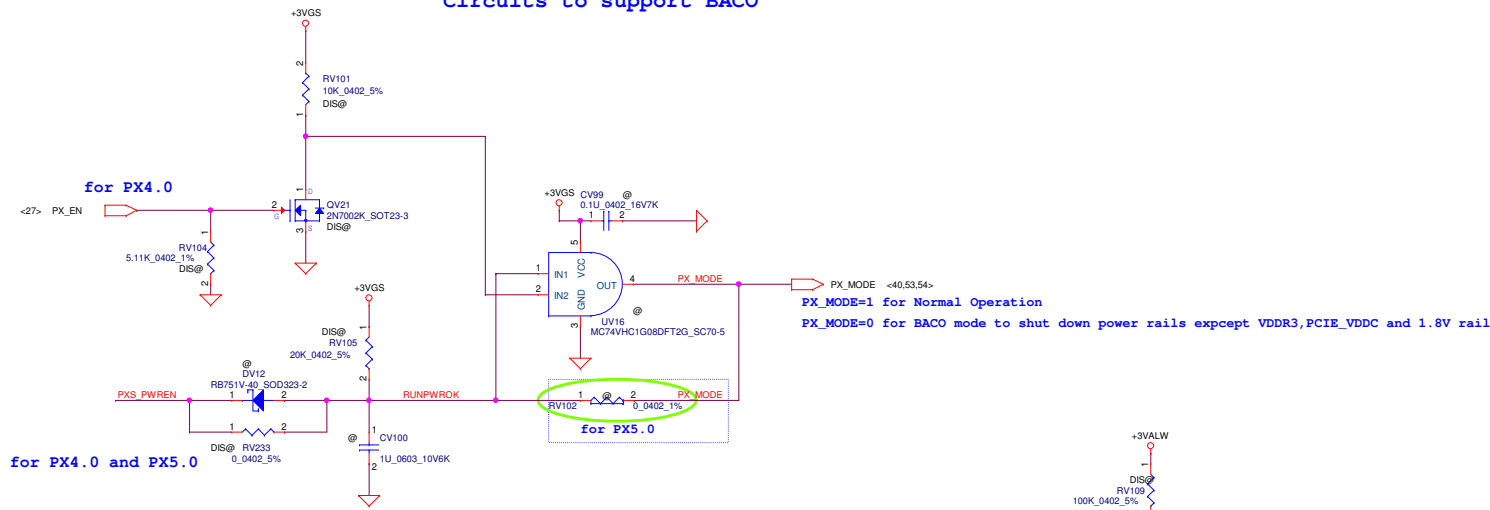
Mars Pro MLPs	RV241	RV242	Bits [3:1]
Hynix	NC	4.75k	000
Samsung	8.45k	2k	001
Micron	4.75k	NC	111



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Issued Date	2012/08/22	Deciphered Date	2013/08/31	ATI	ThamesXT M2 Main_MSIC	
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55mA@1.0V, in BACO mode

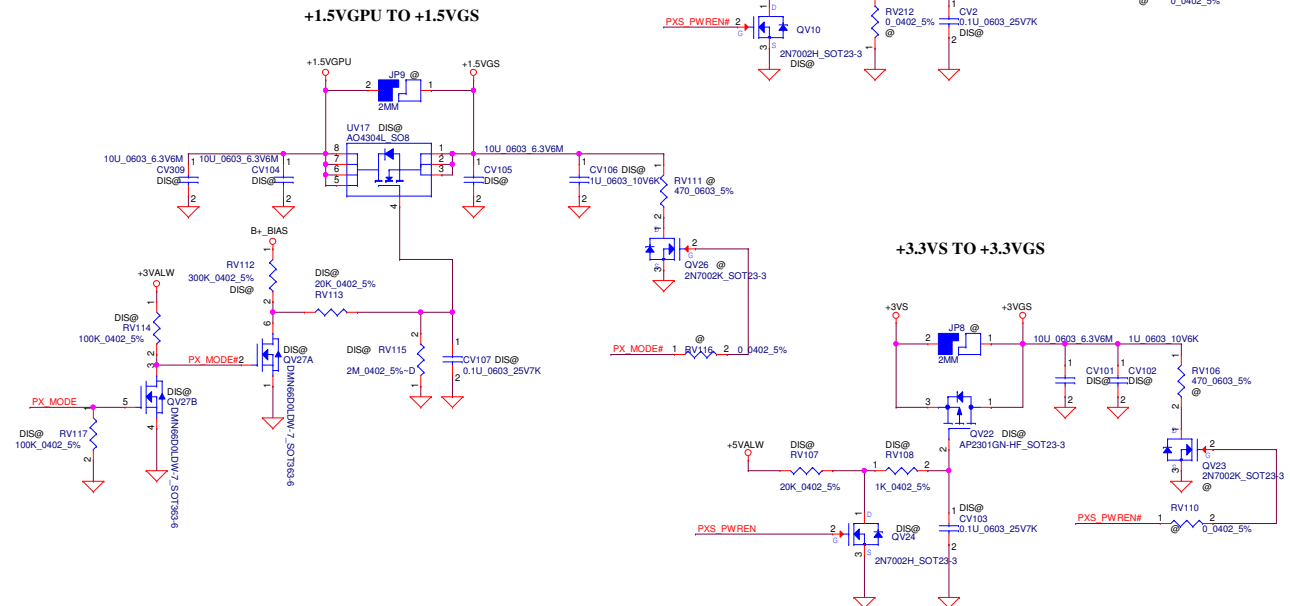
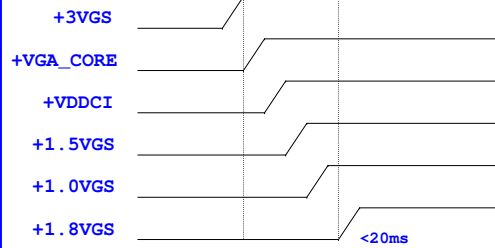
Circuits to support BACO

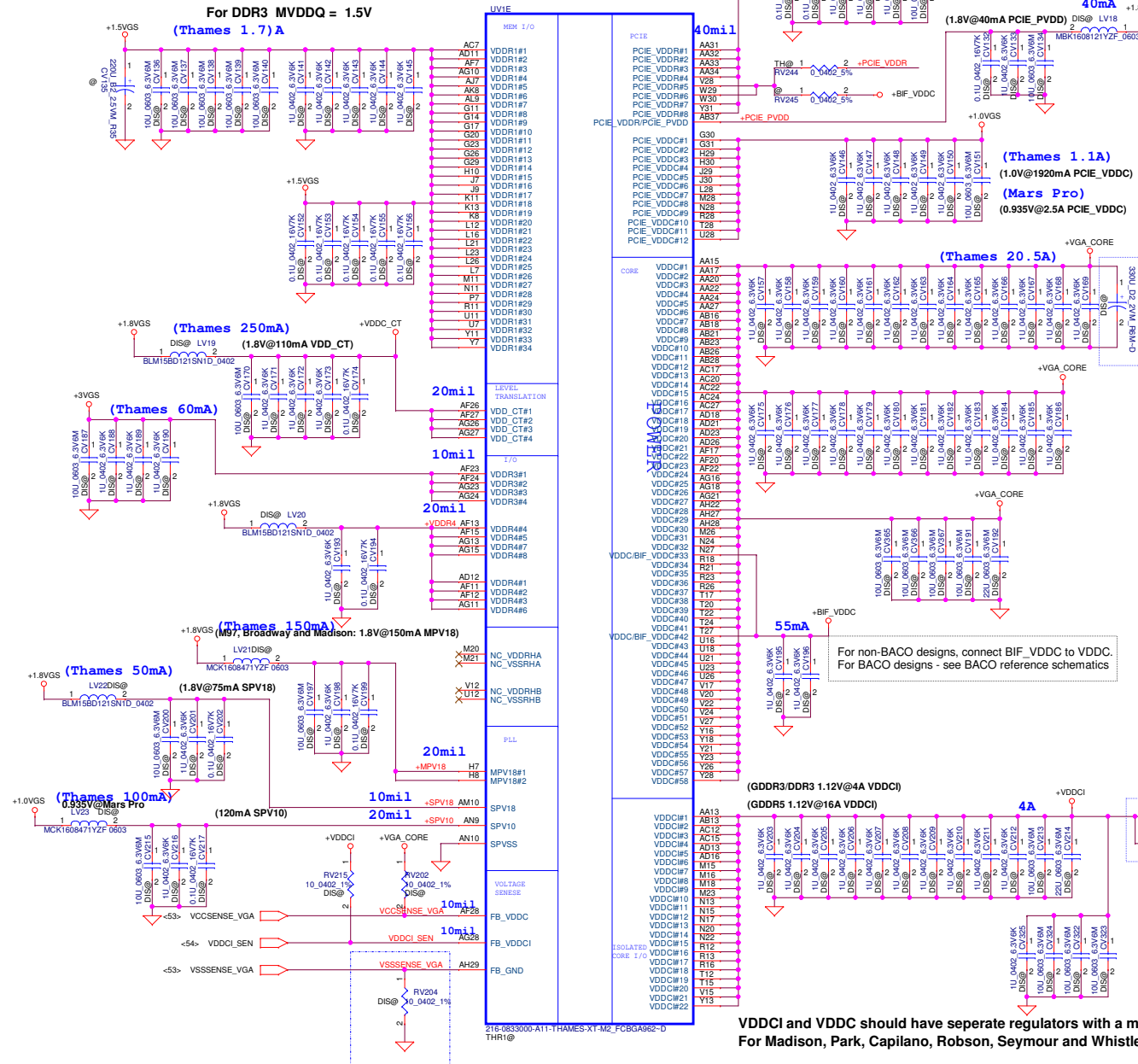


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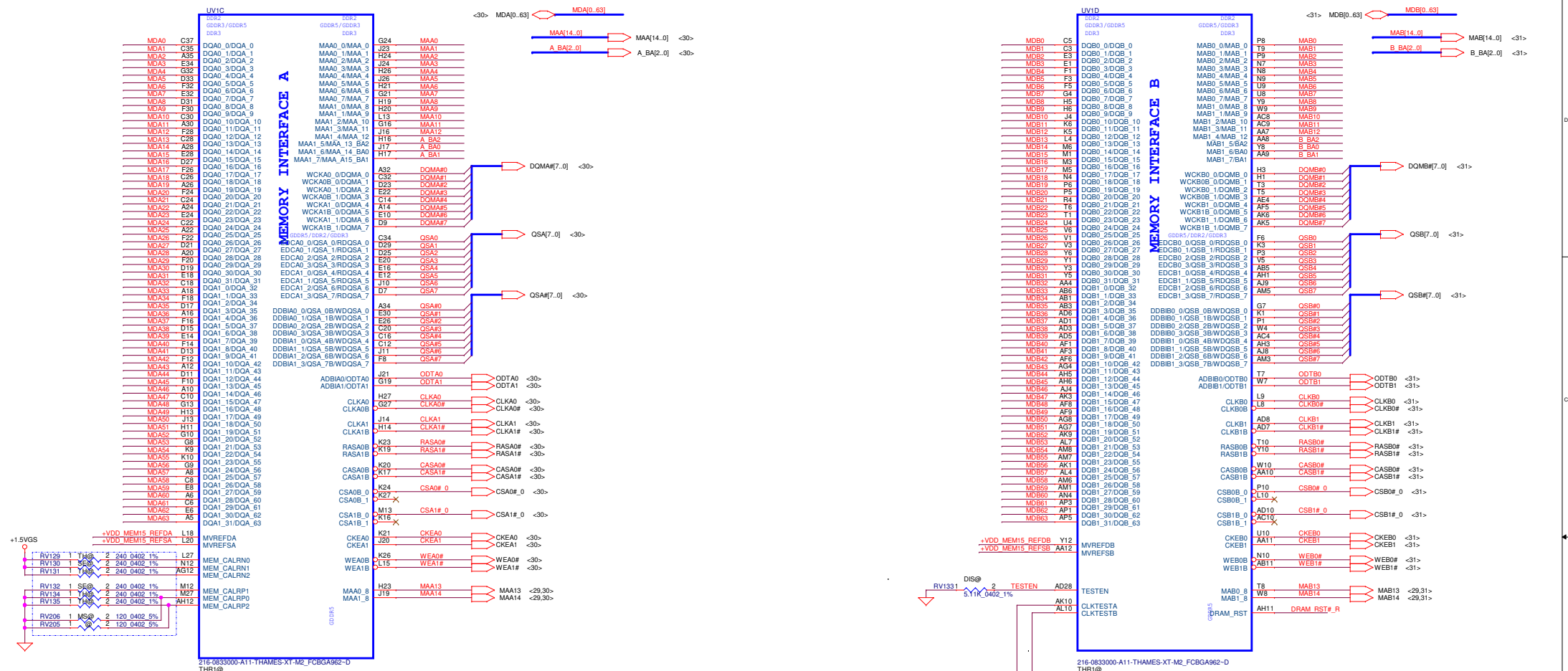
PX4.0 +VGA_CORE, VDDCI, +1.5VGS ON
 PX4.0 +3VGS, +1.0VGS, +1.8VGS OFF
 PX5.0 +3VGS, +VGA_CORE, VDDCI, +1.5VGS, +1.0VGS, +1.8VGS OFF

Power Sequence of Thames and Mars Pro





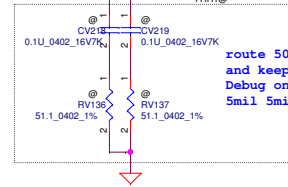
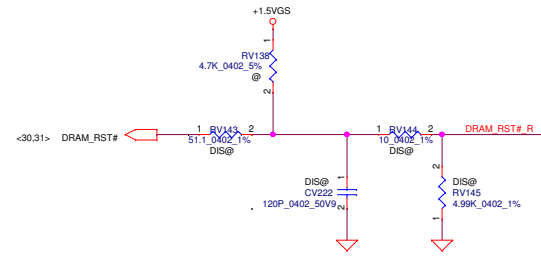
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Issued Date	2012/08/22	Deciphered Date	2013/08/31	Rev	04
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Co-lay Thames/Seymour/Mars Pro

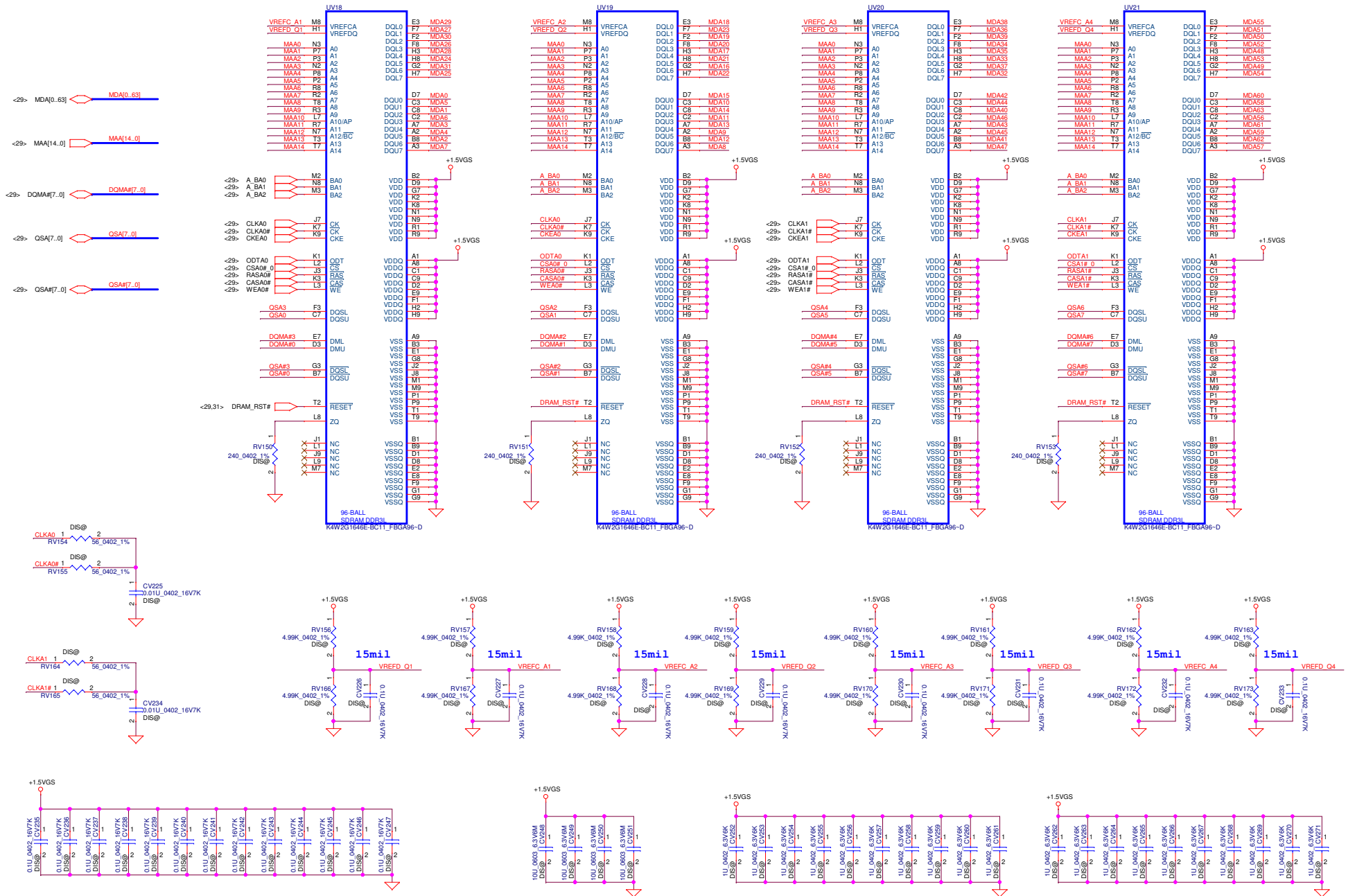
	Thames M2	Seymour M2	Mars Pro
RV129	TH@	@	@
RV130	@	SE@	@
RV131	TH@	@	@
RV132	@	SE@	@
RV134	TH@	@	@
RV135	TH@	@	@
RV206	@	@	MS@
RV205	@	@	@

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and I Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



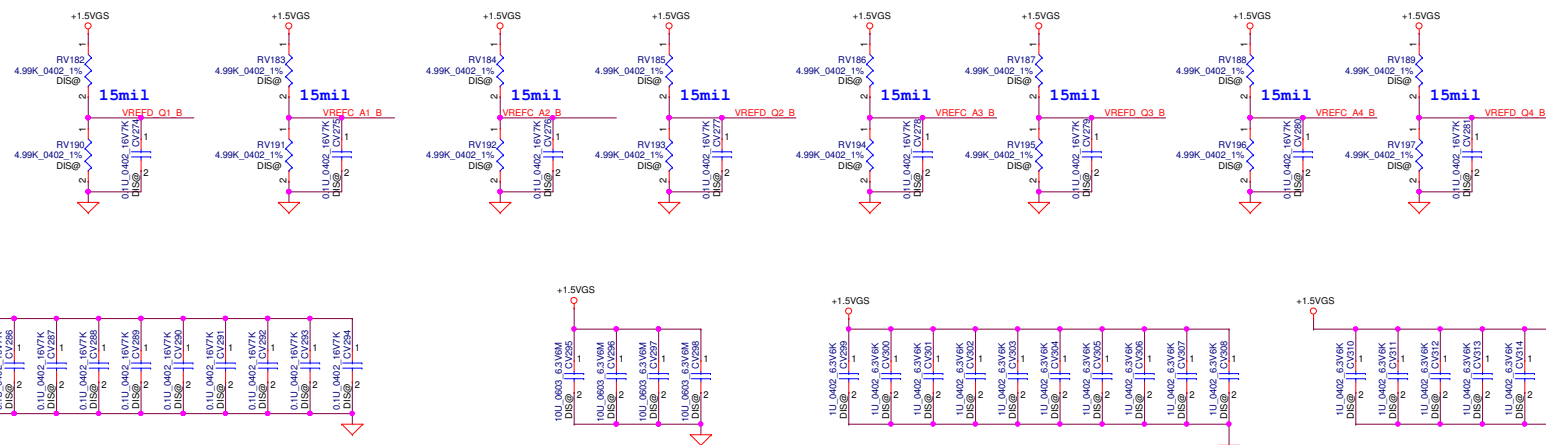
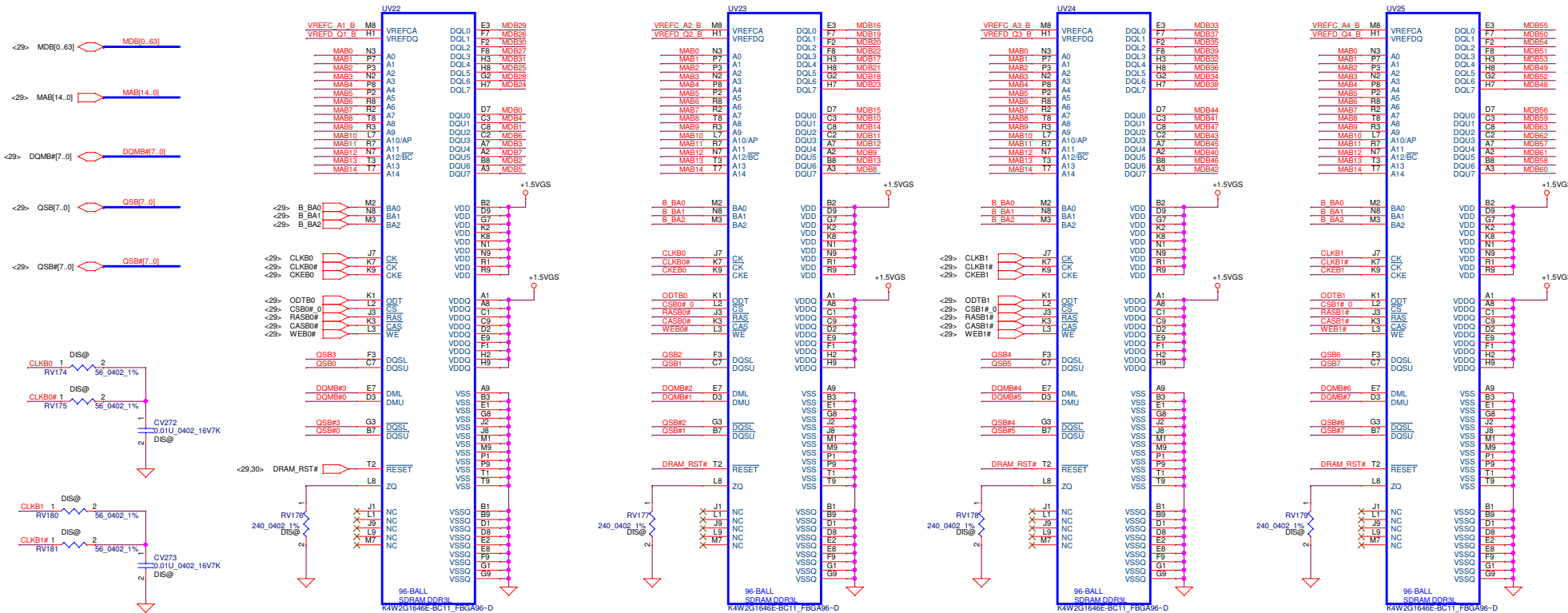
route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DNI
5mil 5mil

CHANNEL A: 256MB/512MB DDR3

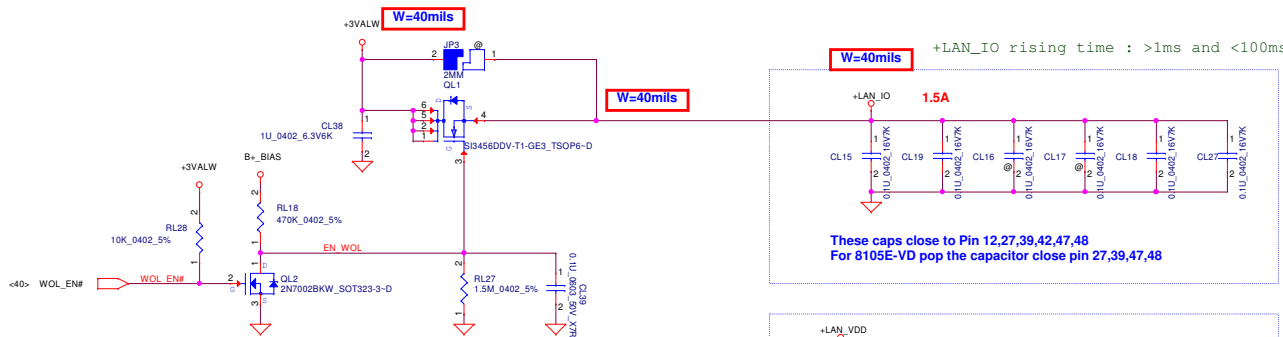


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					Size	Document Number	Rev
					LA-9101P		0.4
Date:		Wednesday, August 29, 2012	Sheet	30	of	57	

CHANNEL B: 256MB/512MB DDR3

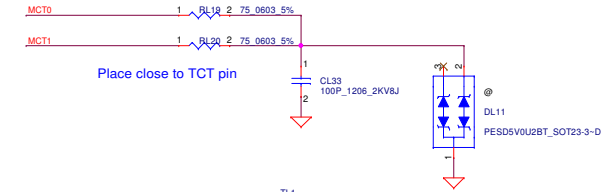
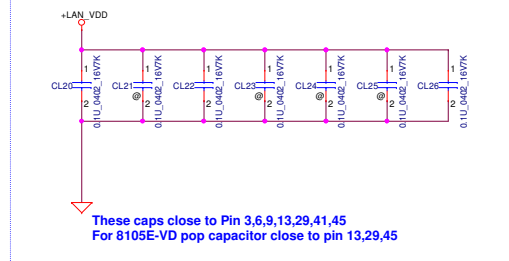


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				LA-9101P	
				Date:	Wednesday, August 22, 2012
				Sheet	31 of 57

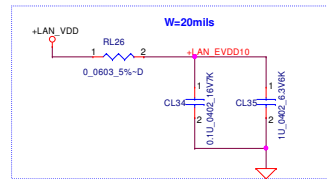
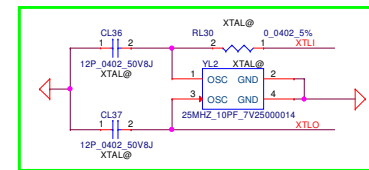
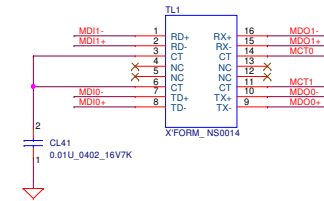


These caps close to Pin 12,27,39,42,47,48

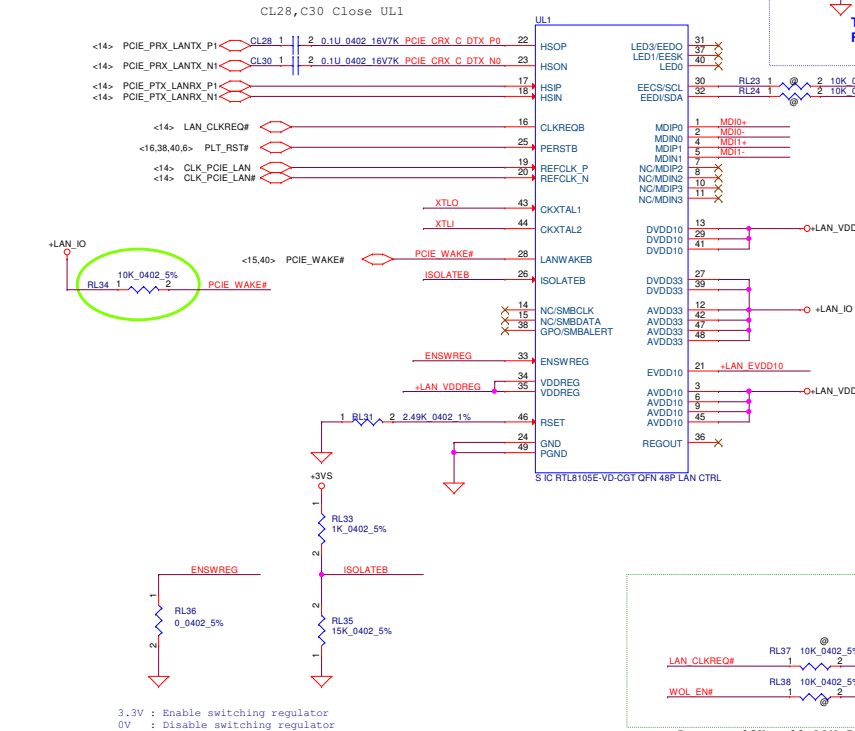
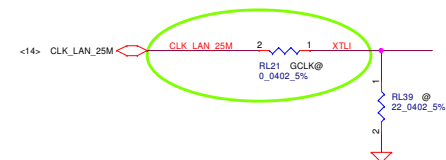
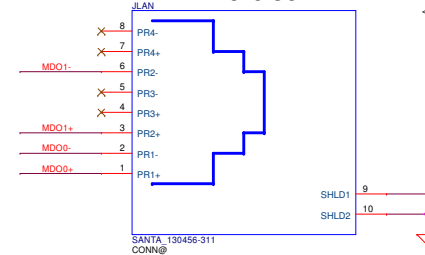
For 8105E-VD pop the capacitor close pin 27,39,47,48



DL11 as close as possible to C27 and C32

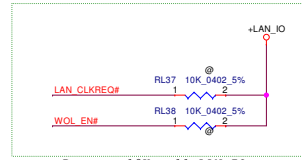


RJ45 Conn.



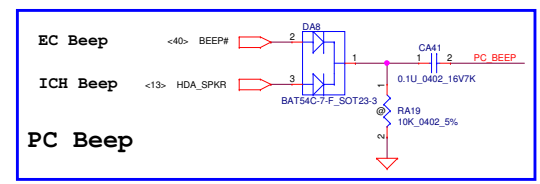
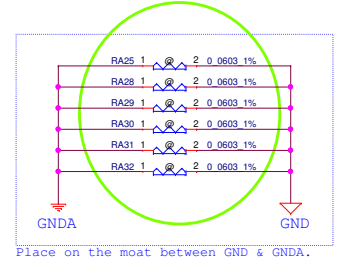
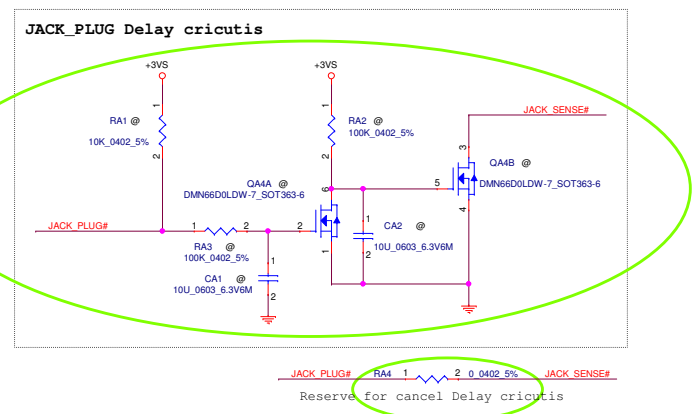
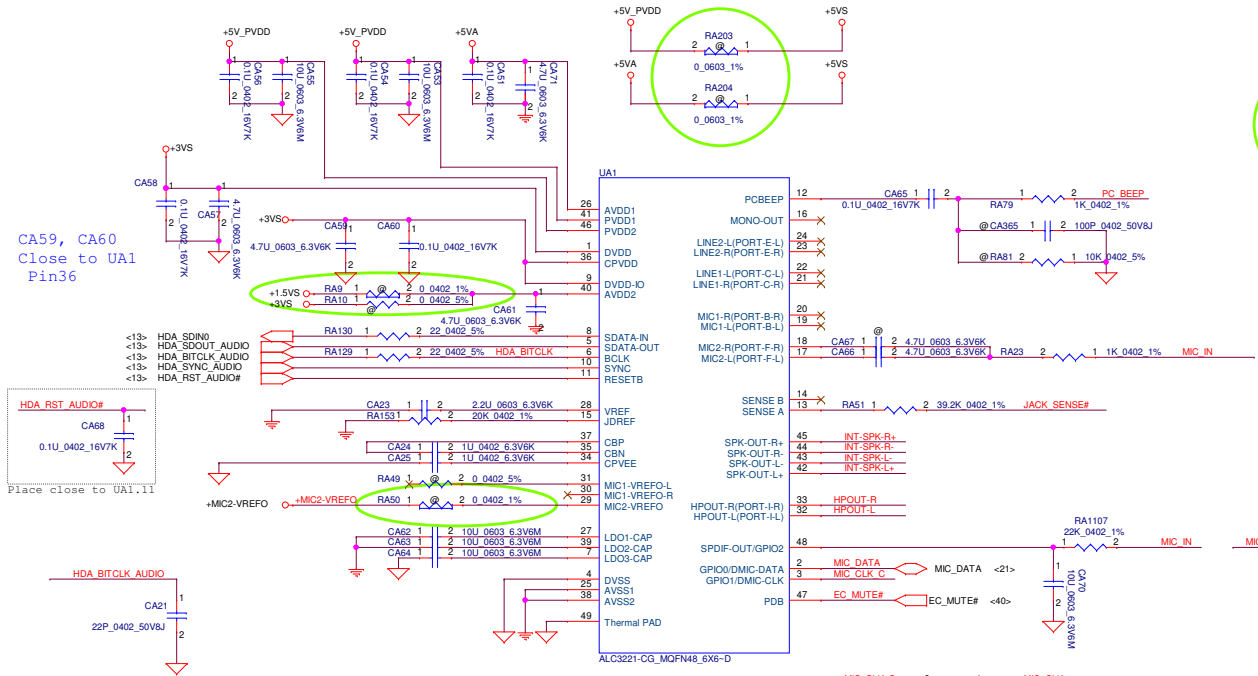
3.3V : Enable switching regulator
0V : Disable switching regulator

10/100 : 100@ (LDO mode used)

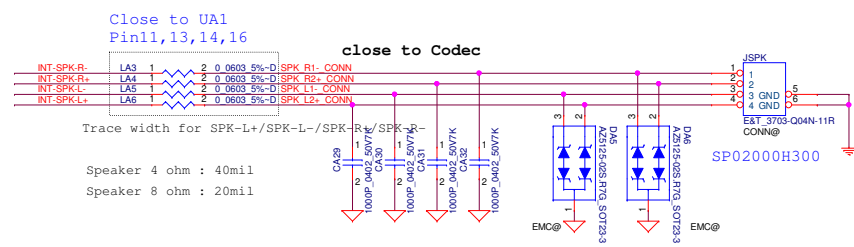
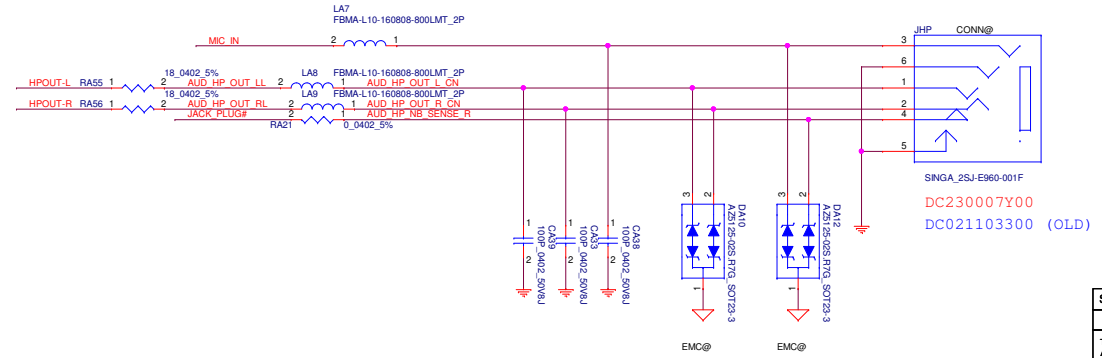


Reserve 10K pull LAN_IO

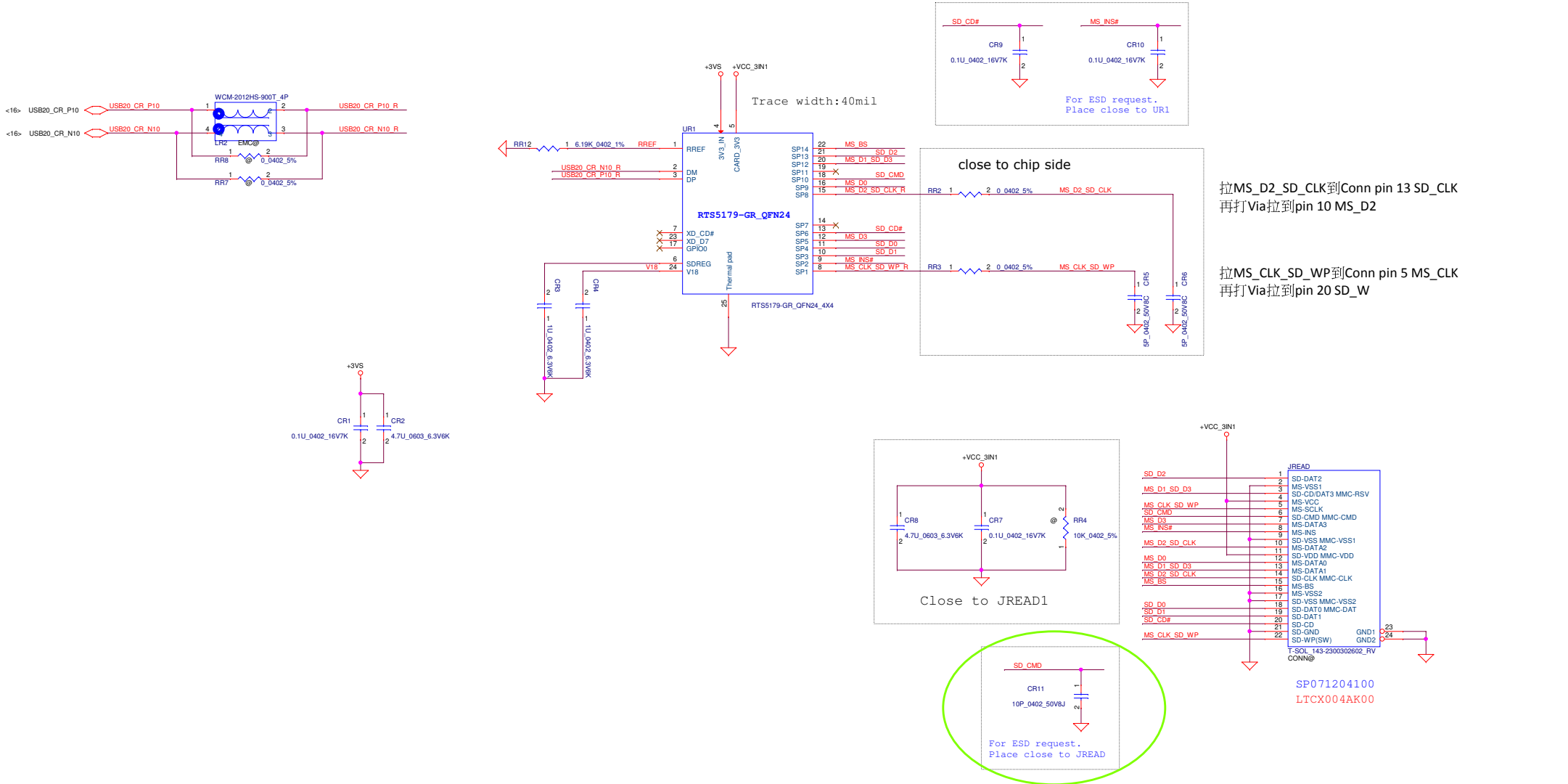
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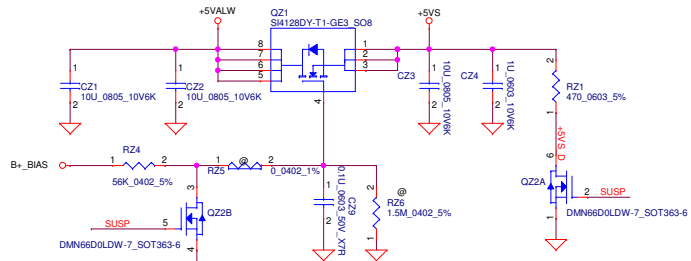
iPhone type Combo Jack



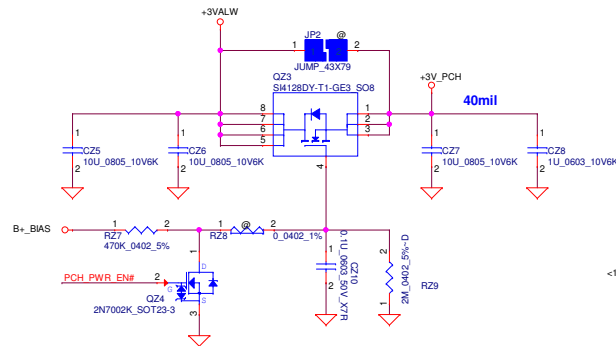
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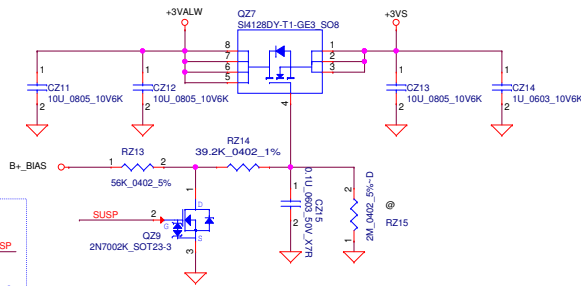
+5VALW to +5VS



+3VALW to +3V_PCH

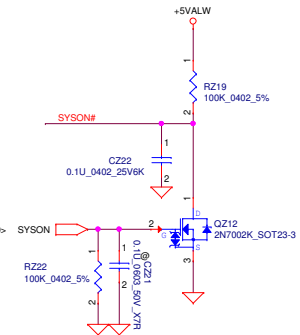
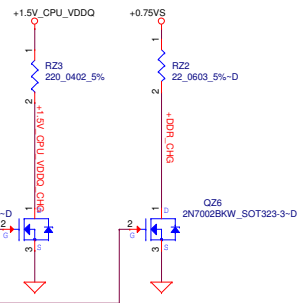
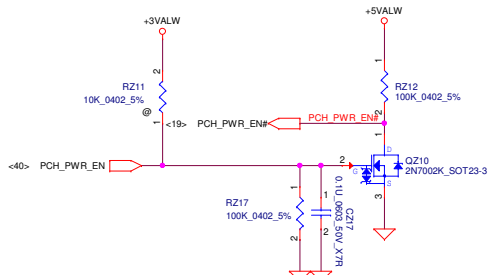
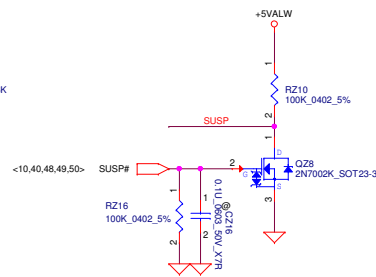
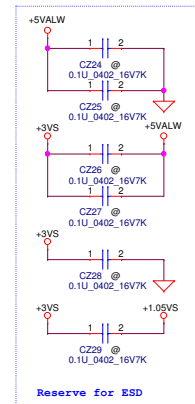
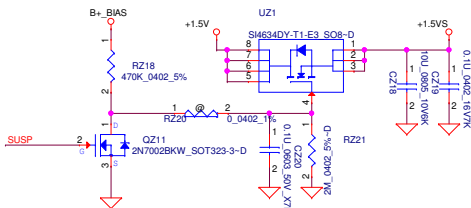


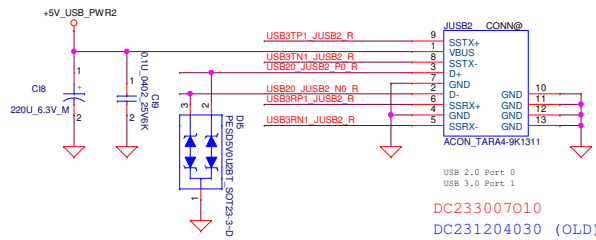
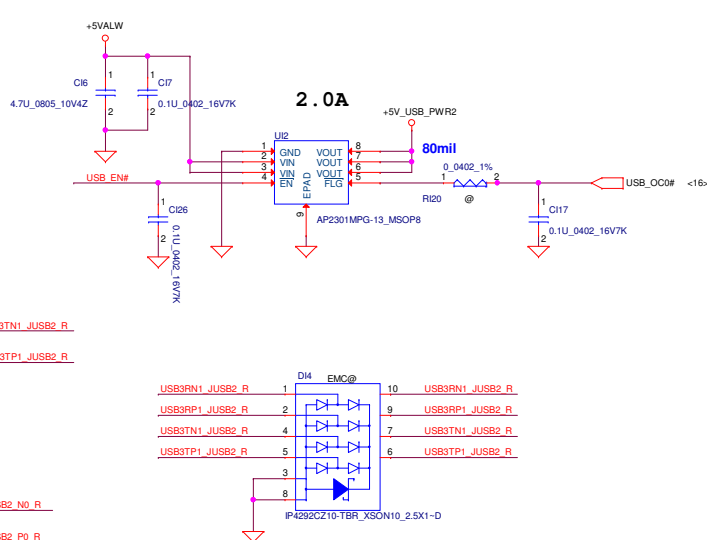
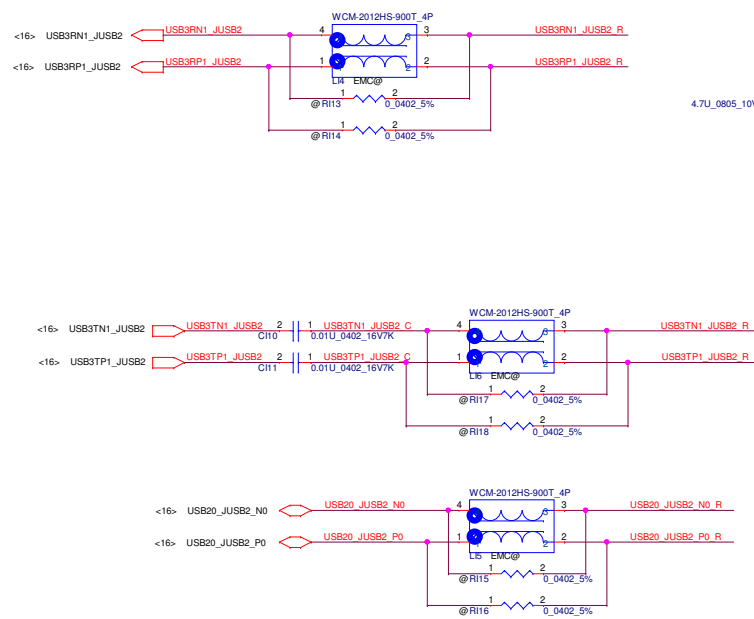
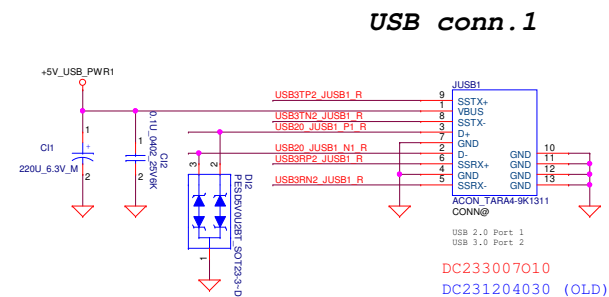
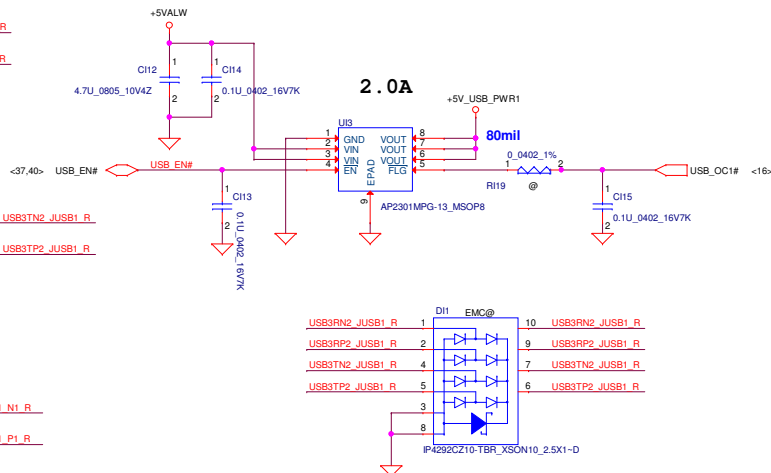
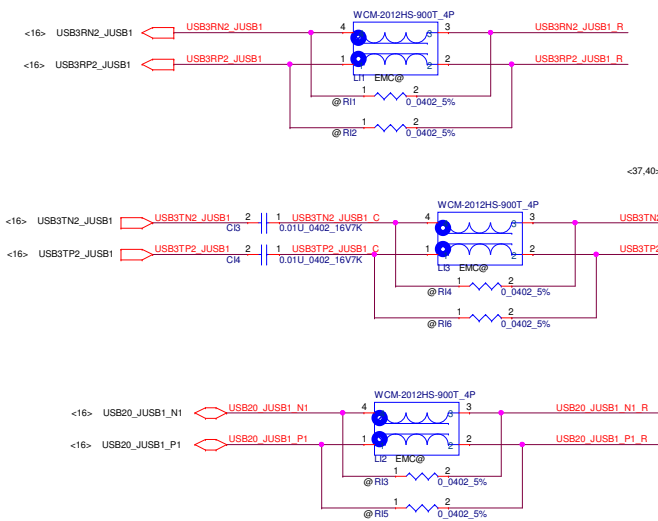
+3VALW to +3VS



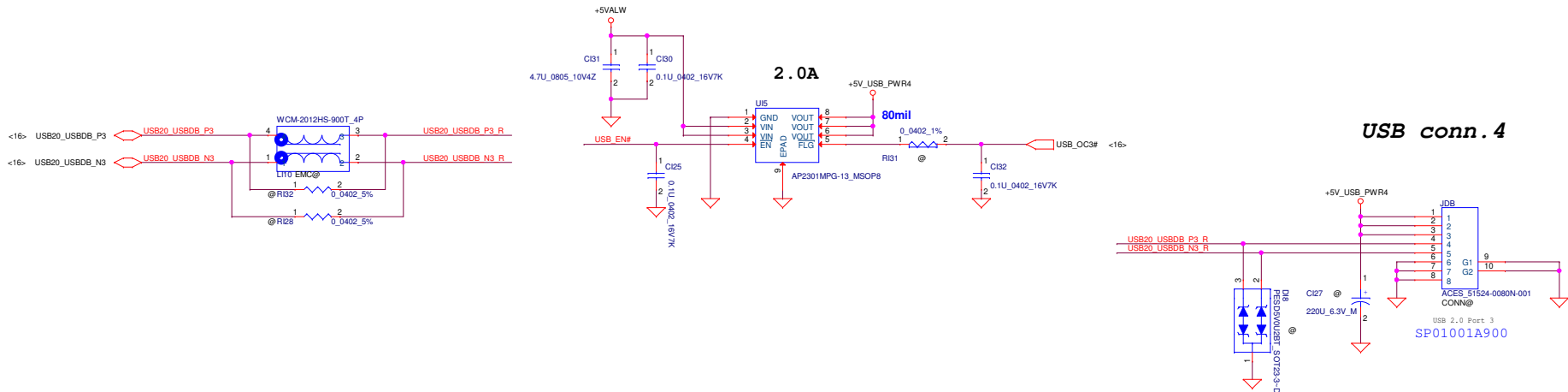
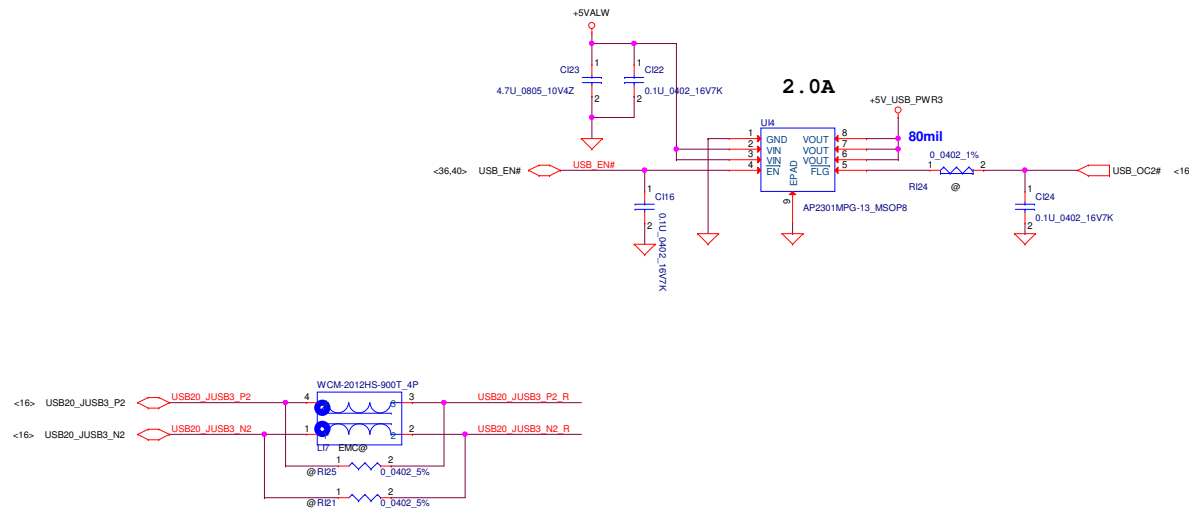
Reserve for ESD
CZ23 2 1
0.1U_0402_16V7K
Please close to Q29

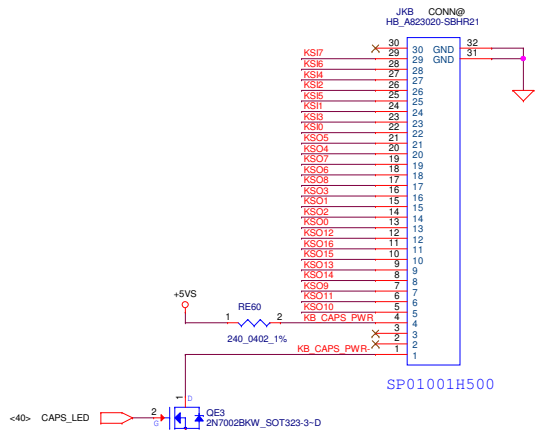
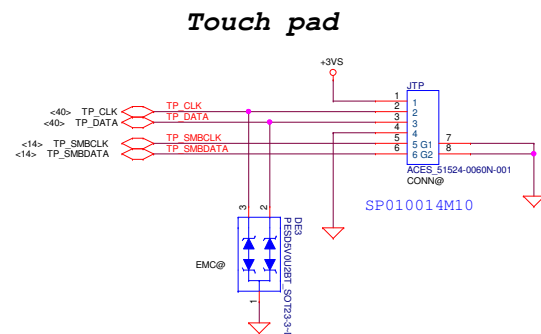
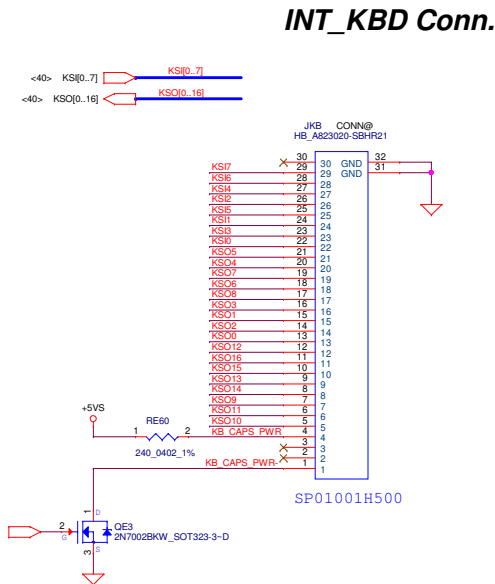
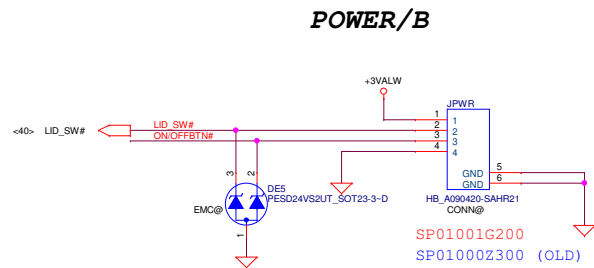
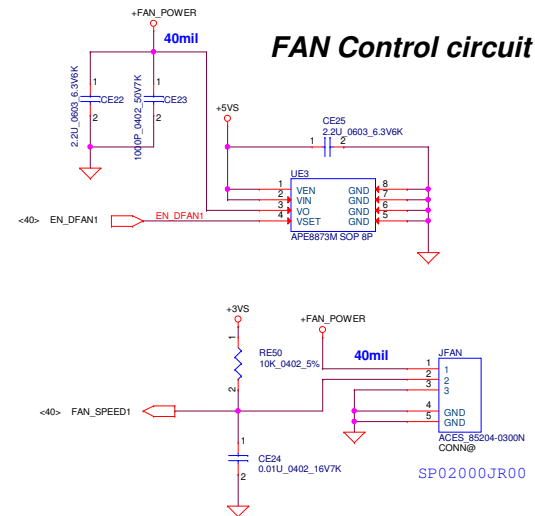
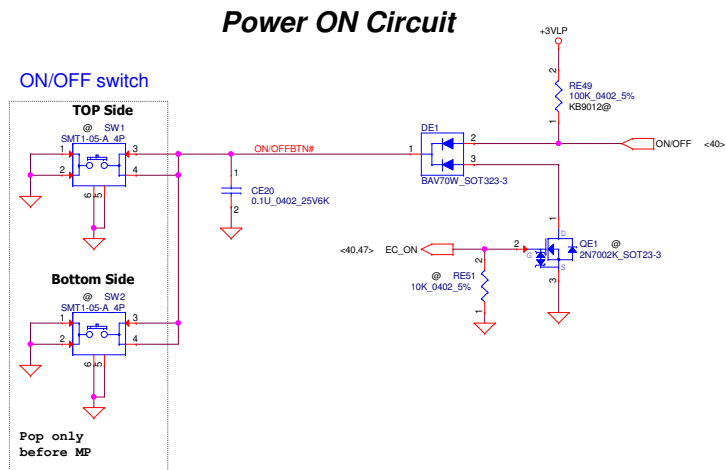
+1.5V To +1.5VS



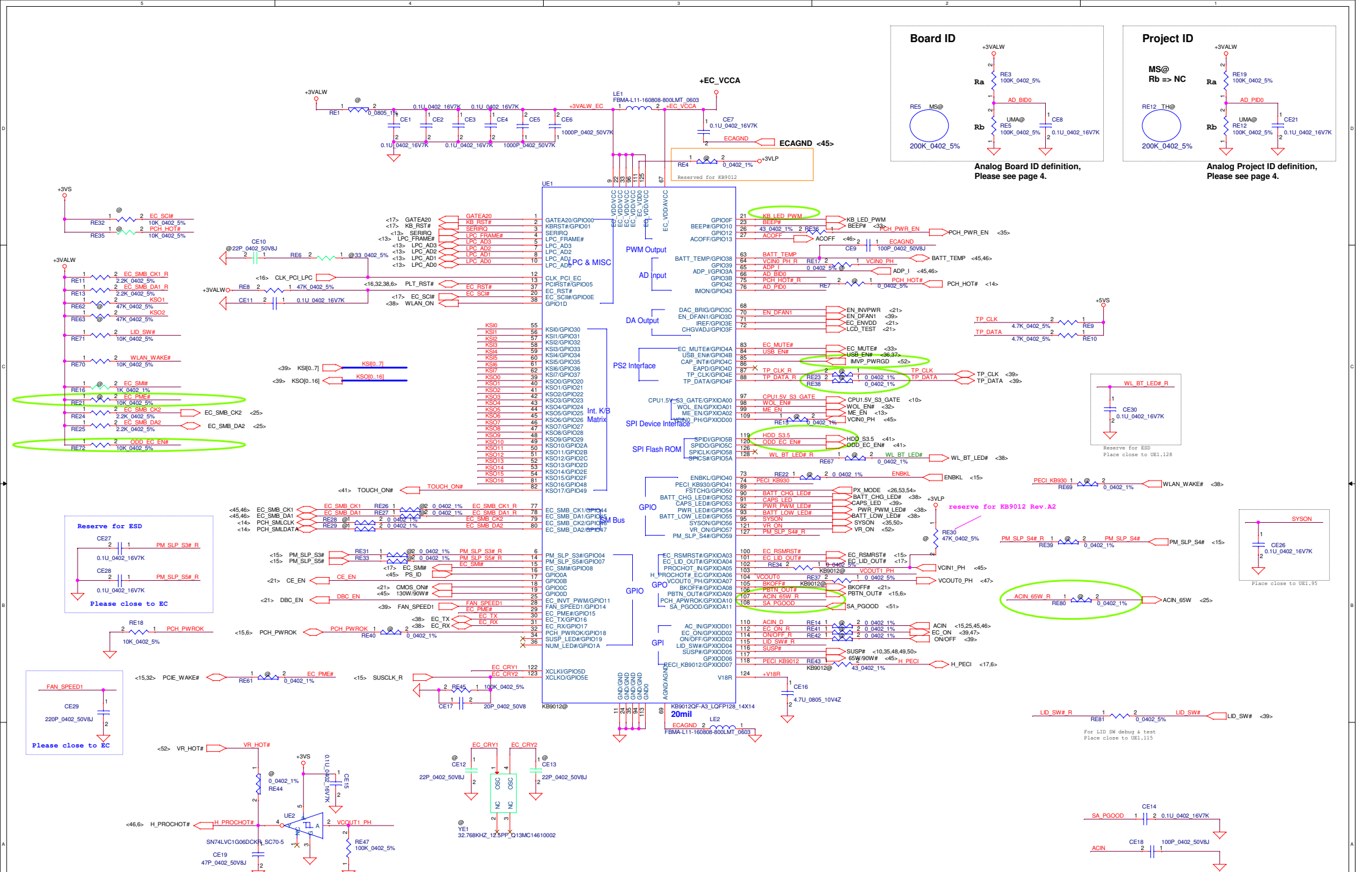


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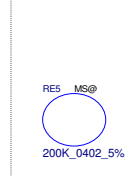




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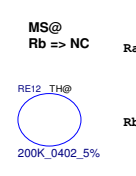


Board ID



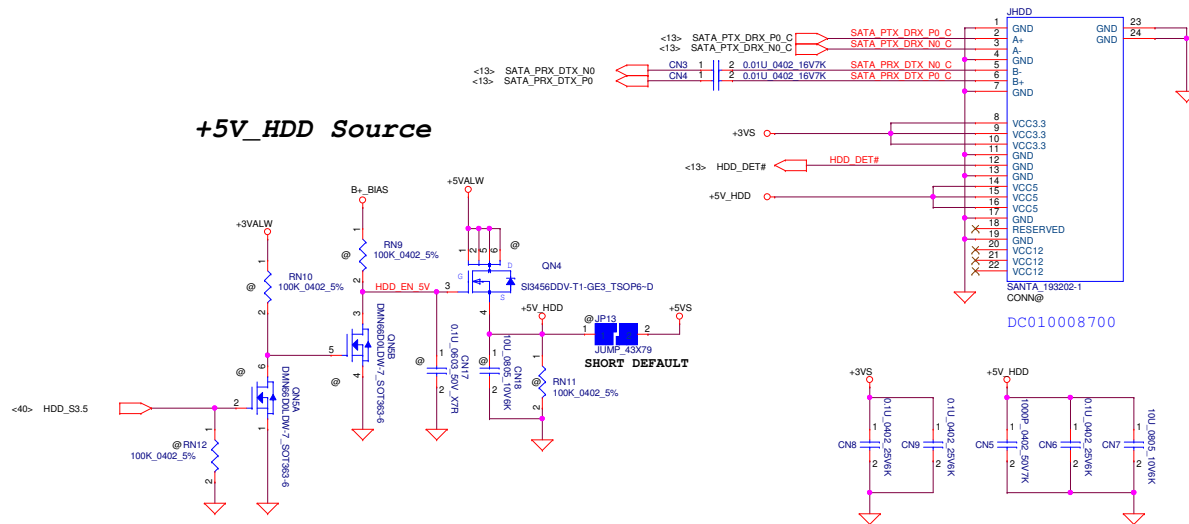
Analog Board ID definition, Please see page 4.

Project ID

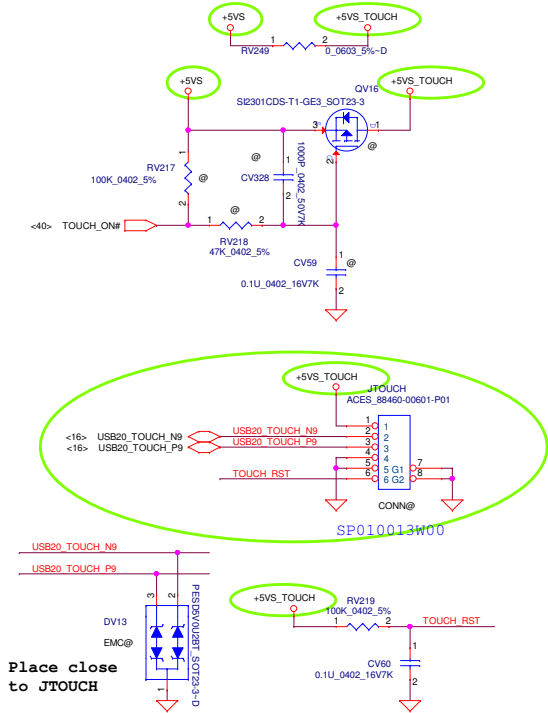


Analog Project ID definition, Please see page 4.

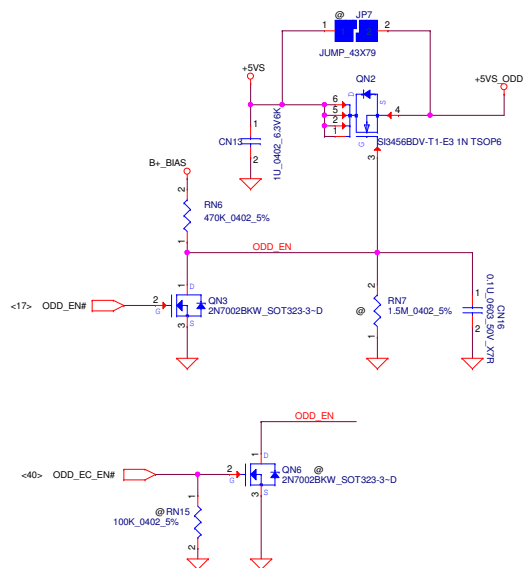
SATA HDD Conn.



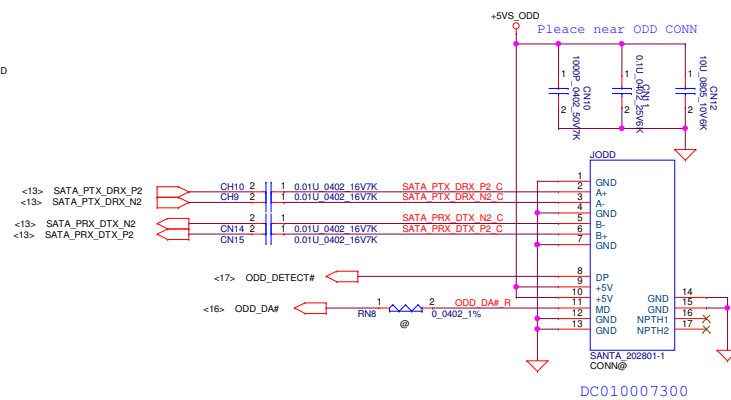
*** Touch Screen Panel**



ODD Power Control

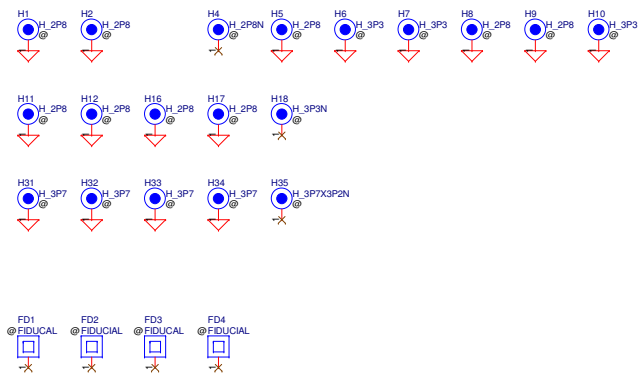


SATA ODD Conn.



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				Documnet Number	LA-9101P
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Screw Hole




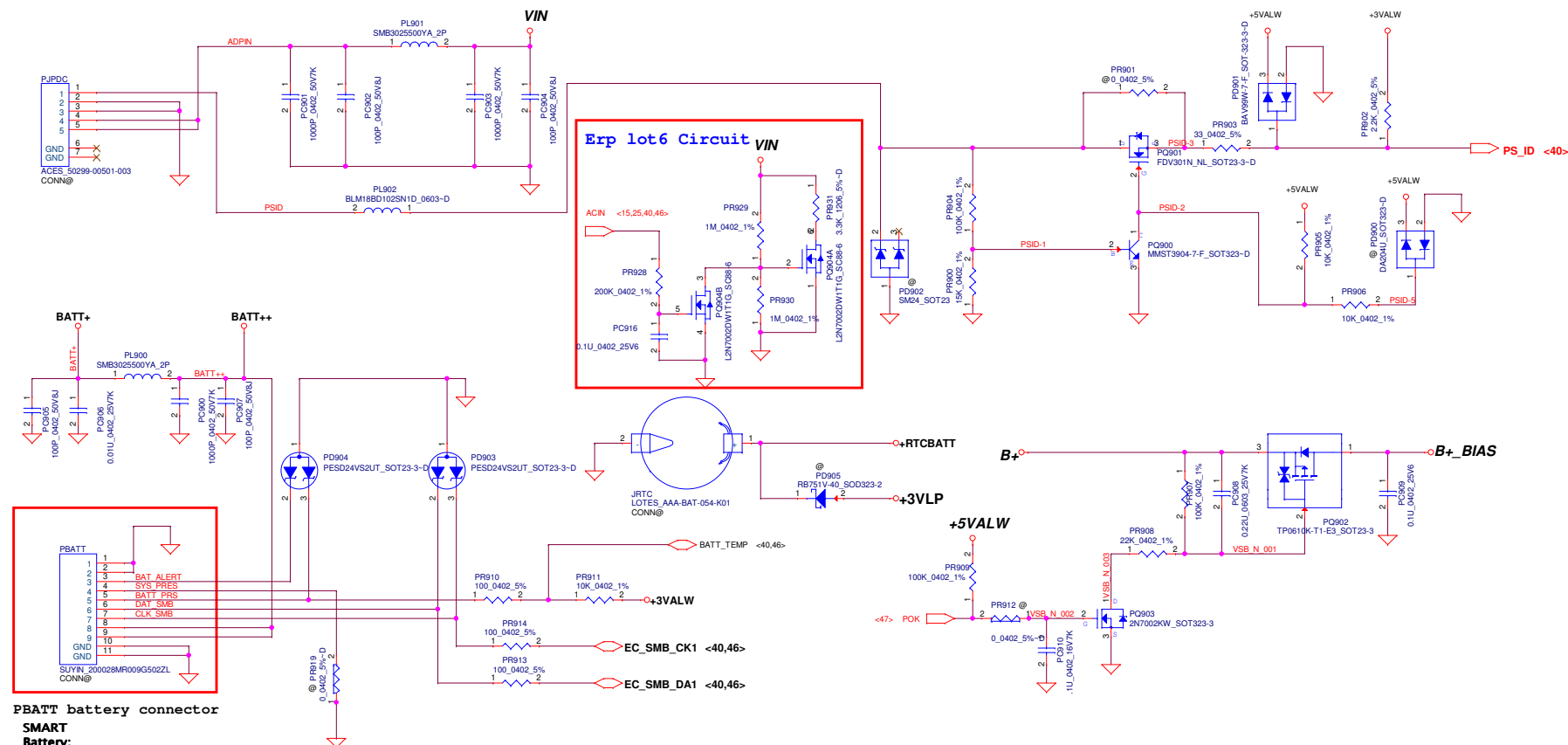
Version Change List (P. I. R. List)

Page 1

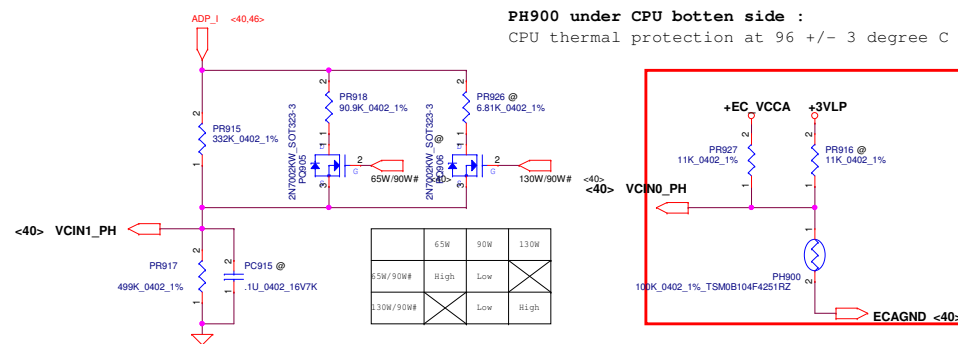
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2	40	Keyboard	2012/05/03	SED	Keyboard pin define change.	Follow new SPEC.SWAP JKB pin define.	0.2
3	16, 21, 34, 36, 37, 38	USB	2012/05/04	Function team	Change USB port assignment for function team request	USB port change detail please reference Page.16 description.	0.2
4	26	VGA	2012/05/05	HW	Delete reserve BACO circuit	Delete UV15,QV16,QV17,QV18,QV19,QV20,RV99,RV100,RV249,CV96,CV98	0.2
5	42	DC/DC	2012/05/07	HW	Design change	UN-POP R211, POP R217	0.2
6	33	Audio codec	2012/05/09	ESD	ESD team ask solution	Add RA29,RA30,RA31,RA32 and place on the moat between GND & GNDA	0.2
7	6, 17	PCH	2012/05/09	ESD	ESD team ask reserve solution	Add CC151,CH102 for reserve	0.2
8	32	LAN	2012/05/10	HW	Remove China Go-rural for DELL request	Remove DL7,DL8,DL9	0.2
9	16, 38	USB	2012/05/10	HW	Remove JUSB3 USB3.0	Delete LI8,LI9,DI6 and change JUSB3 to USB2.0 type	0.2
10	32	Crystal	2012/05/15	HW	Crystal vendor suggestion	Change CL36,CL37 from 33p/0402 to 12p/0402	0.2
11	21, 39	LVDS	2012/05/17	SED	Add FHD Panel CE_ENABLE, DBC_ENABLE function from SED request	Add CE_EN, DBC_EN control pin to EC	0.2
12	21	LVDS	2012/05/22	SED	Follow SED team request disable CE_EN function	Change RV62 to DE-POP and RV100 to POP for disable CE_EN function	0.2
13	33	Audio codec	2012/05/23	CODEC	Follow CODEC vendor suggestion	Add AUDIO JACK PLUG delay circuit, Spearate NET JACK_PLUG to -> JACK_SENSE# & "> JACK_PLUG#	0.2
14	16, 21	Touch Screen	2012/05/29	HW	Add touch screen function	Add RV217, RV218, RV219, RV249, CV59, CV60, CV328, DV13, QV16, JTOUCH	0.2
15	39	Board ID	2012/05/30	HW	Board ID change for PT	Change RE5 from 8.2k_0402(SD028820180) to 33k_0402(SD028330280)	0.2
16	21, 39	Touch Screen	2012/05/30	HW	Add touch screen function power control	Add NET "TOUCH_ON#" from JTOUCH to UE1.82(KB9012) for TOUCH SCREEN PANEL power control	0.2
17	33	Audio codec	2012/05/30	HW	Follow RealTek suggestion remove, delete reserve MUTE circuit	Delete D1,QA1,QA2,QA3,RA24,RA26,RA60,RA62,RA68,RA109,CA72,CA73	0.2
18	15, 16, 39, 41	ESD	2012/05/30	ESD	ESD ask CAP for reserve	Reserve 0.1u/0402 CH104,CZ23,CH105,CE27,CE28	0.2
19	14	Green CLK	2012/05/30	HW	For Green CLK test	Change RH31,RH41,RV232 0ohm form "GCLK#" to "g" for break the clock signal to device	0.2
20	10, 26, 41	DC/DC	2012/05/31	HW	Change "+1.5V_CPU_VDDQ", "+1.5VS", "+1.5VGS" derating	Change RC150 330K/0402 to 2M/0402, RC151 100K/0402 to 470K/0402, RZ18 100K/0402 to 470K/0402, RV115 0/0402 to 2M/0402	0.2
21	41	DC/DC	2012/05/31	HW	For power sequence trunning	Change RZ15 to DE-POP	0.2
22	06, 15, 16, 39, 41	ESD	2012/05/31	ESD	Follow ESD team request	Change 0.1u/0402 from "g" to POP	0.2
23	32	Green CLK	2012/06/15	HW	Change for Green CLK bom control	Change RL21,RL30 from "g" to "GCLK#"	0.2
24	41	DC/DC	2012/06/15	HW	For WLAN card power sequence issue	Change RZ4,RZ13 from 470K/0402 56K/0402	0.2
25	35, 41	Schematic page modify	2012/06/18	HW	Schematic page modify for easily maintain.	Swap Page. 35 & Page 41.	0.2
26	41	ODD	2012/06/18	HW	Change component location for easily maintain.	Move RH42,RH43 from Page.13 to Page.41.	0.2
27	39	FAN	2012/06/29	HW	Fan speed noise issue	Reserve 220p/0402 CE24	0.3
28	6	CPU	2012/06/29	ESD	System boot-up shot down issue.	Change CC151 from POP to "g"	0.3
29	21, 35, 39, 40, 41	Circuit adjust	2012/07/01	HW	Circuit & page adjust for OAK 15" & OAK 17"	1. Swap P.35 & P.41and move touch screen circuit from P.21 to P.41. 2. Swap P.39 & P.40 page no	0.3
30	40	LID SW	2012/07/01	HW	LID SW need a trace for debug and switch.	Add RE81 for LID SW.	0.3
31	25	GPU	2012/07/01	HW	Follow AMD request, MarsPro will used MPLs.	Change RV75,RV76,RV81 from "DIS#" to "TH#"	0.3
32	29	GPU	2012/07/01	HW	Follow AMD request, MEM_CALRP2 is not need for Mars ASIC now.	Change RV205 from "MS#" to "g"	0.3
33	38	MINI card	2012/07/03	HW	Power Control for Mini card didn't need	Change R17 to "g"	0.3
34	6	XDP	2012/07/06	HW	S3 return hang issue	Change RC89 from "g" to POP	0.3
35	23	GREEN CLK	2012/07/09	HW	Follow Green CLK FAE suggestion	1. Change UG1.2(+3VLP) & UG1.8(+3VALN) connect to +LAN_IO 2. Add R787 connect from +RTCBATT to C5.2 & UG1.10 3. Change C14 from 0.1u to 5p/0402 4. Change C8 connect from +3V_ALW to +LAN_IO 5. Add R788 0ohm/0402 from +RTCVCC to UG1 for GCLK & DH1 select	0.3
36	35	MOAT	2012/07/09	ESD	For ESD request reserve CAP.	Reserve those CAP for ESD MOAT.	0.3
37	18	LVDS	2012/07/10	HW	Change RES and reserve CAP for LVDS issue	Change RH185 from 0ohm-short to 0ohm/0805, and reserve CH106 1U/0402	0.3
38	41	Connector	2012/07/10	ME	For ME request	Change JBTB1 footprint from SP02000G800 (OLD) to SP02000MJ00	0.3
39	13	PCH	2012/07/11	ESD	Follow ESD team request	Add RH44,RH48,RH70 & NET PCH_JTAG_TMS_R, PCH_JTAG_TDI_R, PCH_JTAG_IDO_R for break signal trace	0.3
40	40	PCH	2012/07/11	ESD	Follow ESD team request	1. Change NET NAME "N59110727" to "WL_BT_LED#_R" 2. Reserve 0.1u/0402 on "WL_BT_LED#_R" for ESD	0.3
41	21	LVDS	2012/07/11	HW	Reserve for CE function for LVDS connector	Change CE_EN_R from dummy to JLVDS.18	0.3

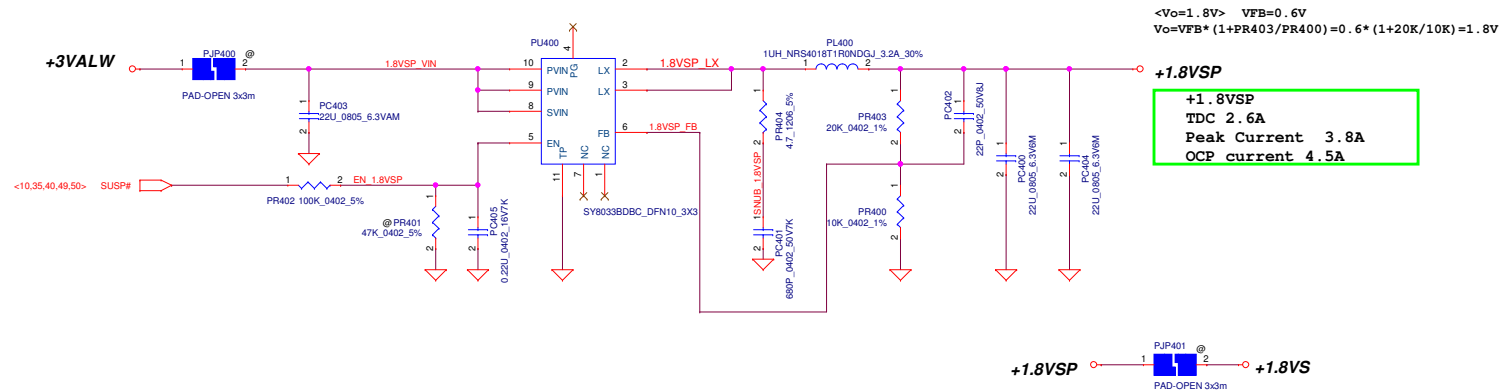
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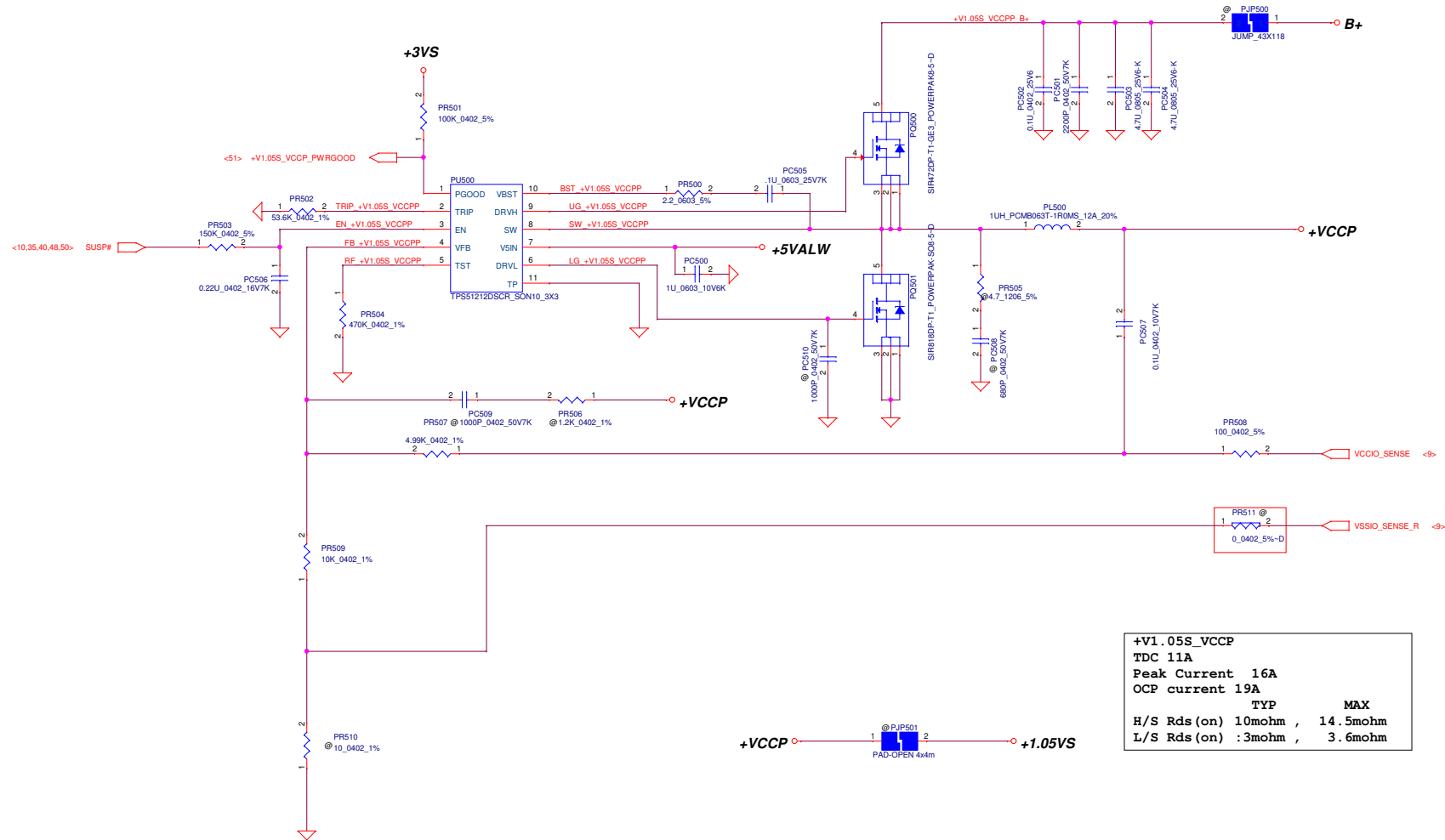
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P900 under CPU bottom side :
CPU thermal protection at 96 +/- 3 degree C



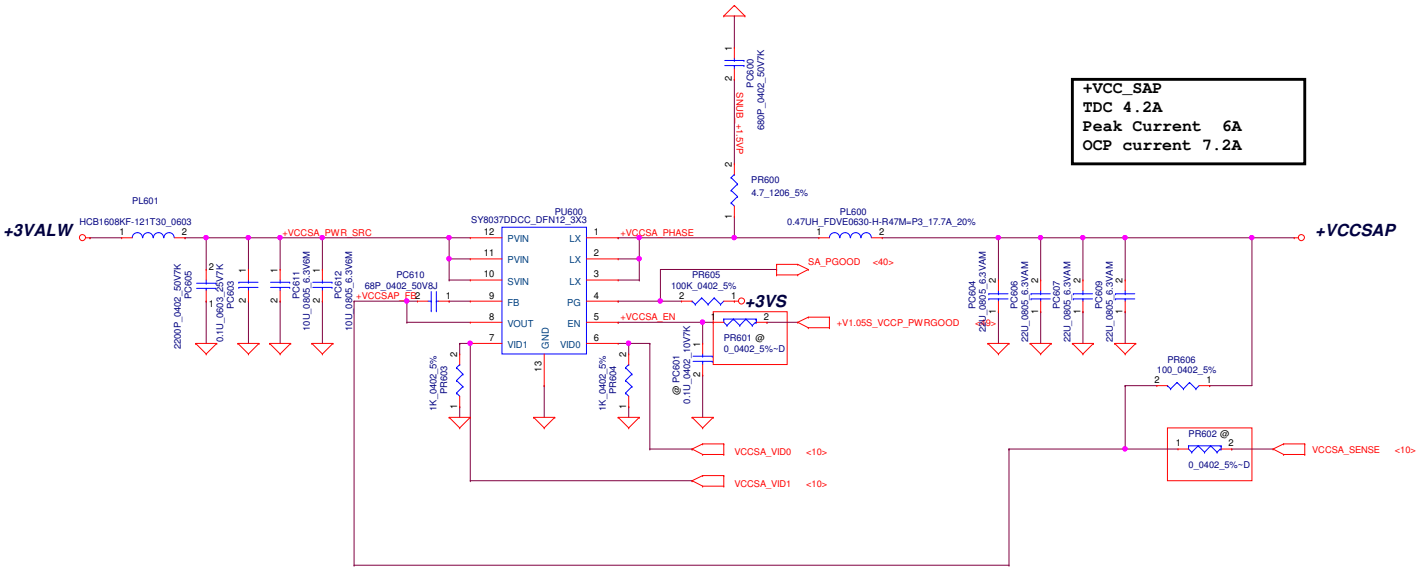




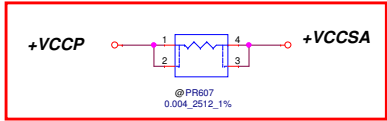
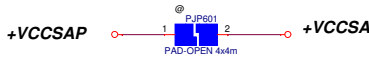
+V1.05S_VCCP	
TDC 11A	
Peak Current 16A	
OCP current 19A	
	TYP
H/S Rds (on)	10mohm , 14.5mohm
L/S Rds (on)	: 3mohm , 3.6mohm

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

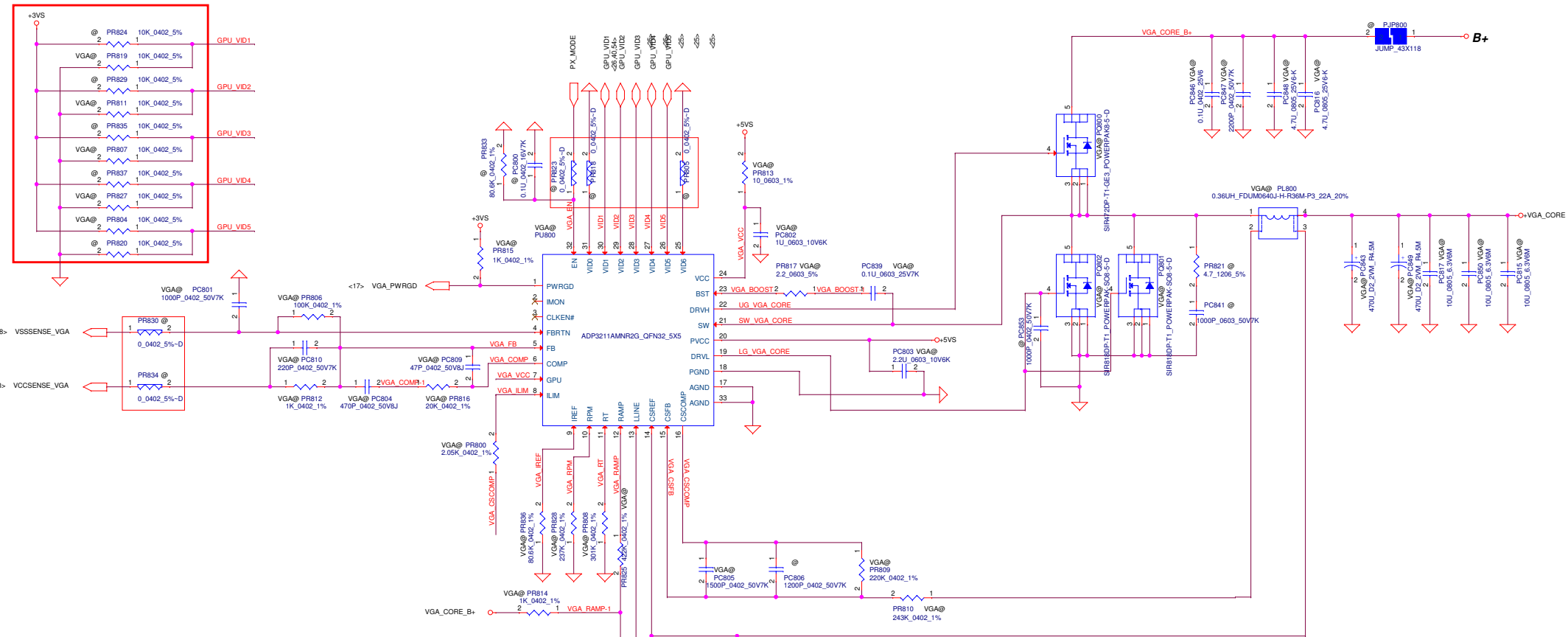
output voltage adjustable network



The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.



reserve for Pentium and Celeron only



Mars Pro

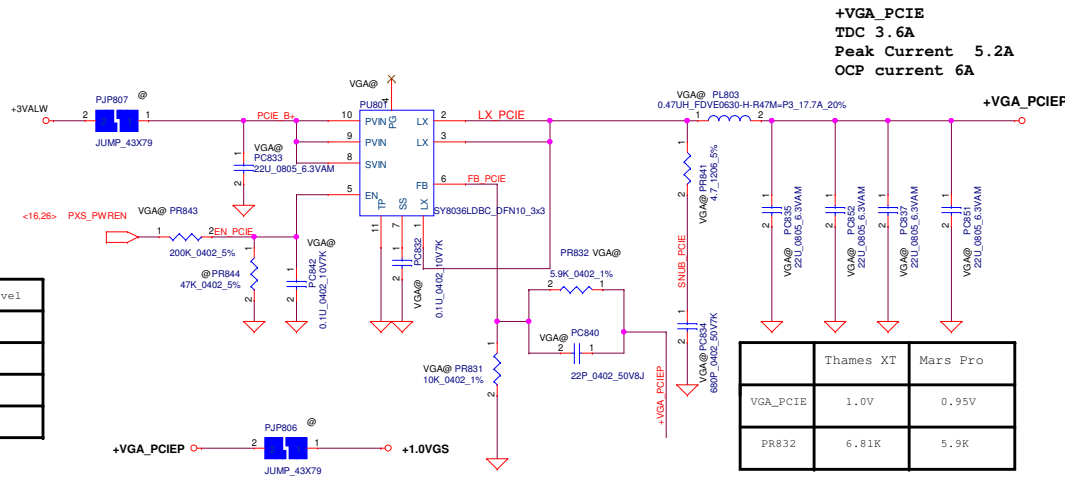
GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V

+VGA_CORE
TDC 22A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.1mohm +/-5%
Loadline = 1.5mohm

Thames XT

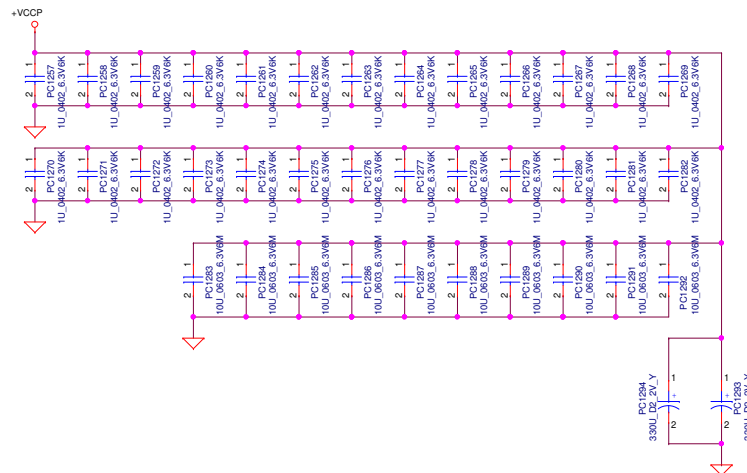
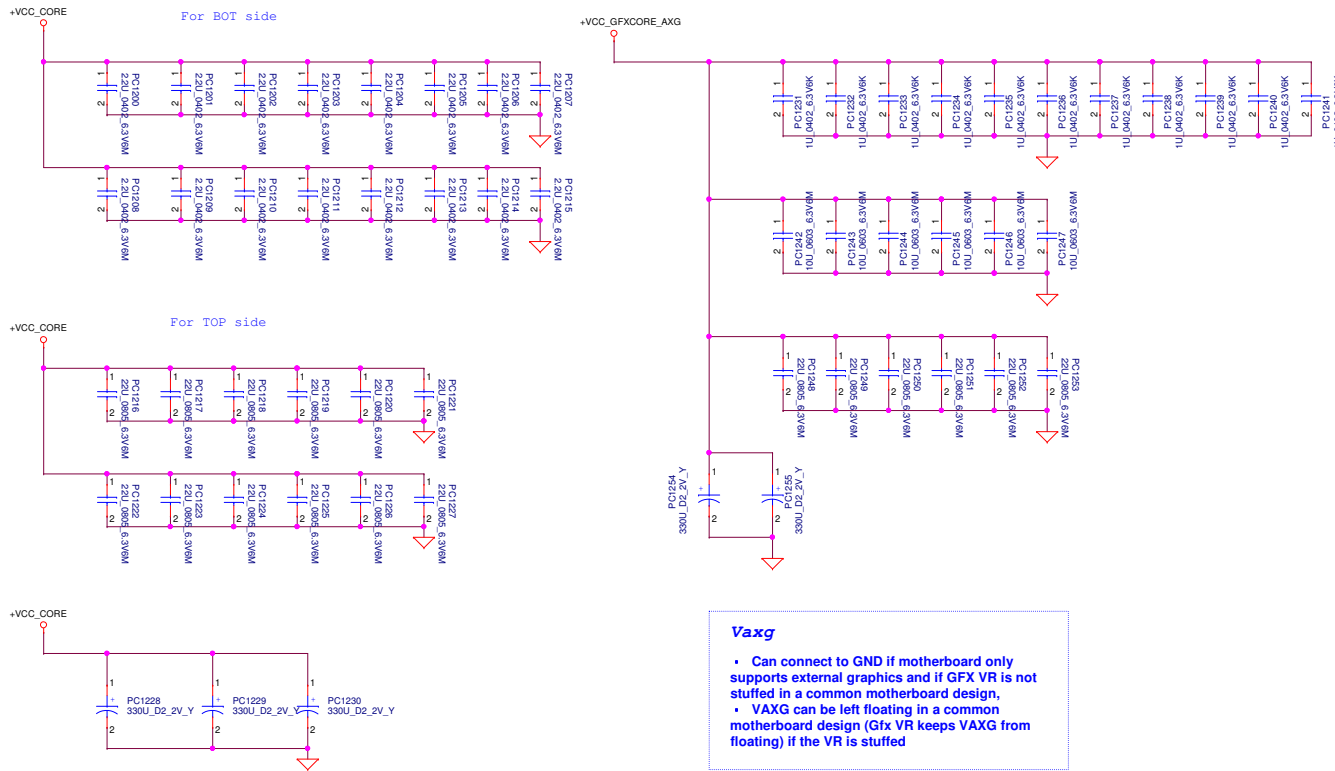
GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
1	0	0	1	0	1.05V
1	0	1	0	0	1V
1	0	1	1	0	0.95V
1	1	0	0	0	0.9V

+VGA_CORE
TDC 20A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.1mohm +/-5%

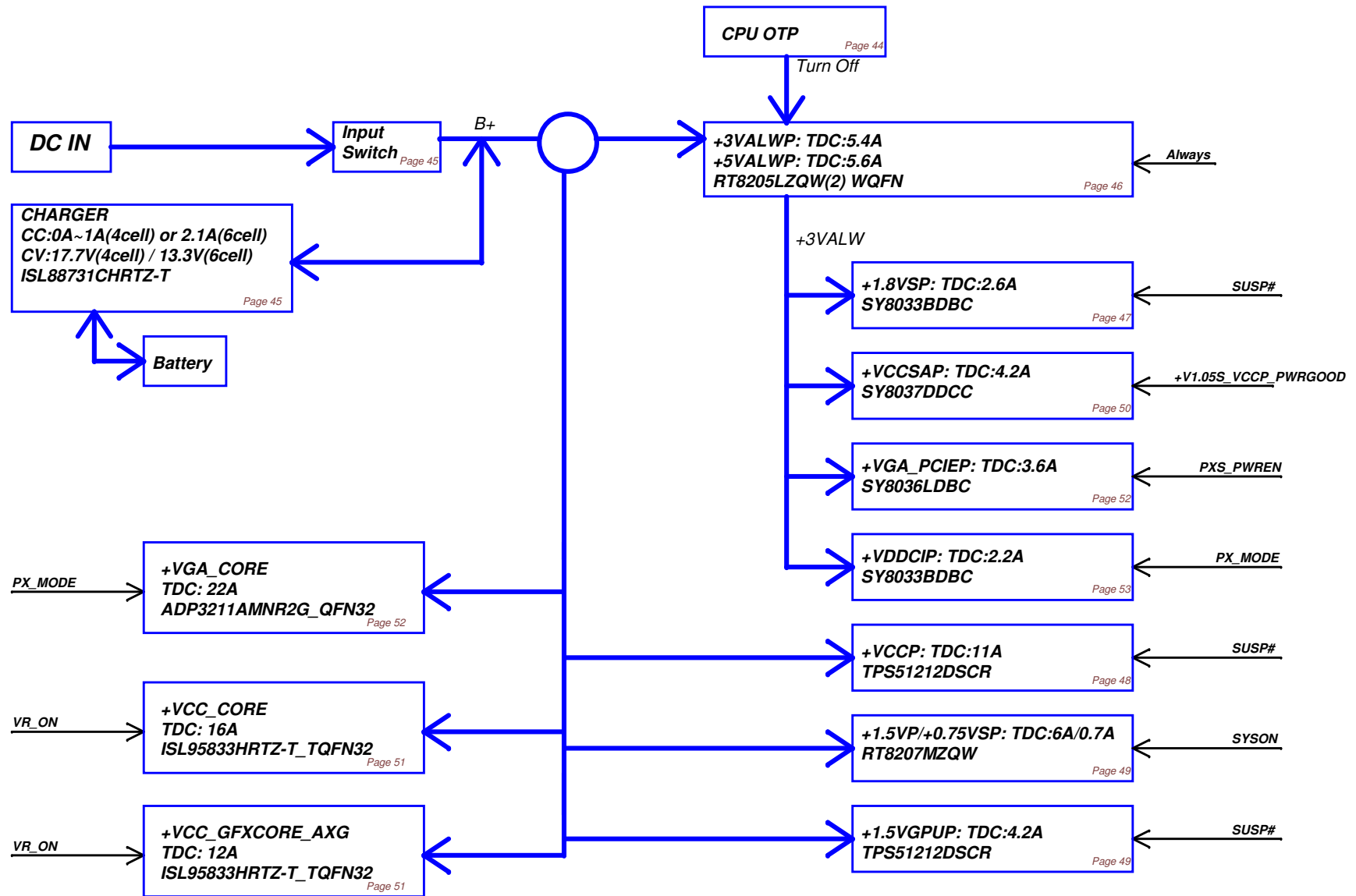


+VGA_PCIE
TDC 3.6A
Peak Current 5.2A
OCP current 6A

	Thames XT	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K



Power block



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