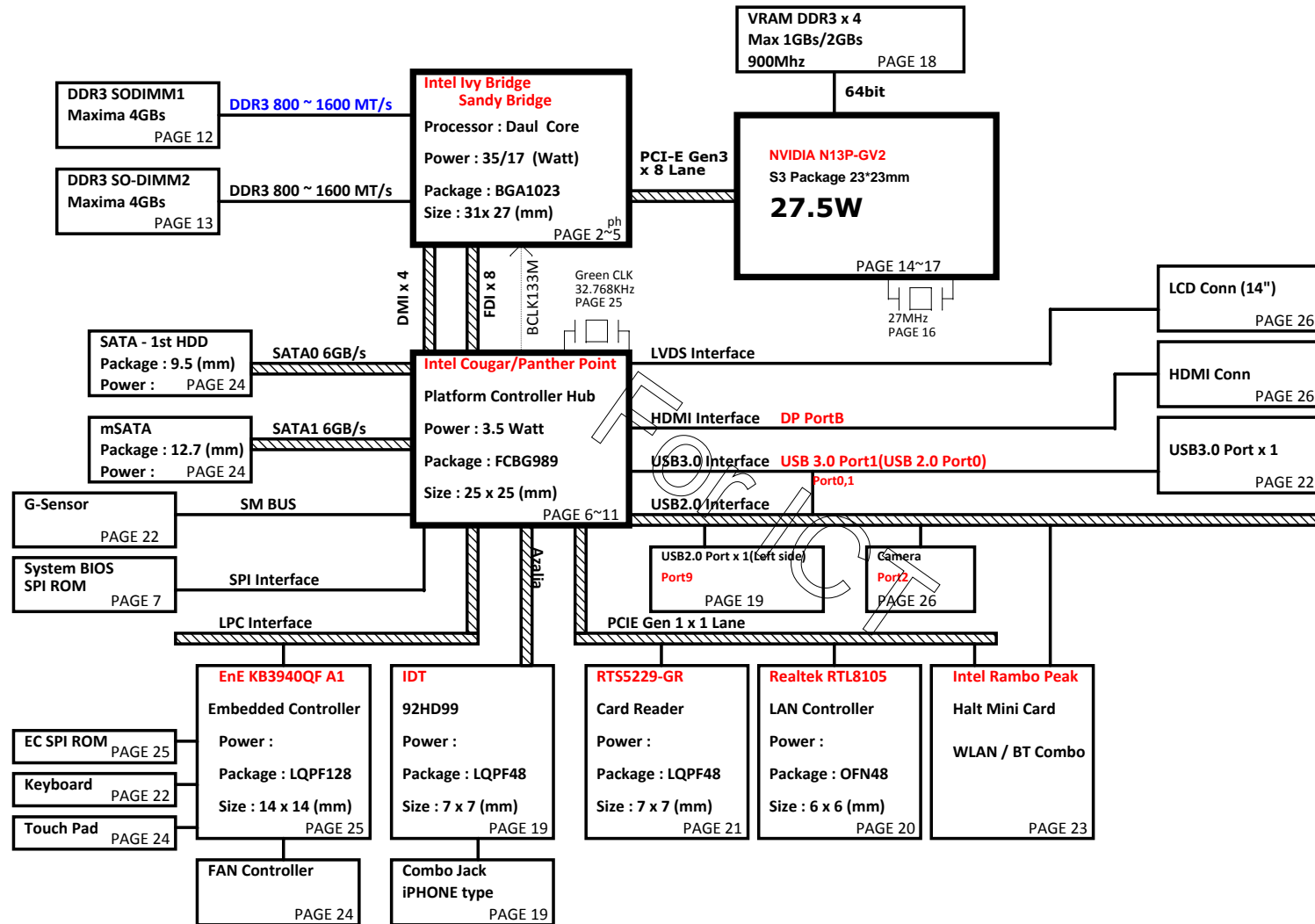


# Volks DIS/UMA (14"/15.6") Ultra/Slim Intel Chief River Platform Block Diagram



## PCB 6L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : BOT

## Power Source

**BQ24738**  
System Charge Power (+BATCHG)

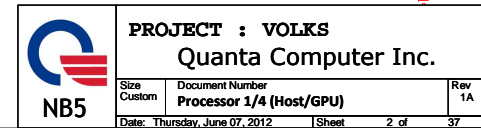
**Ricktek RT8223P**  
System Power (+3VPCU/+5VPCU/  
+3VS5/+5VS5)

**NCP6132/NCP5911/RT8240P/  
TP551462RGER**  
Processor Power (+VCC\_CORE/  
+1.05\_VTT/+VCCSA)

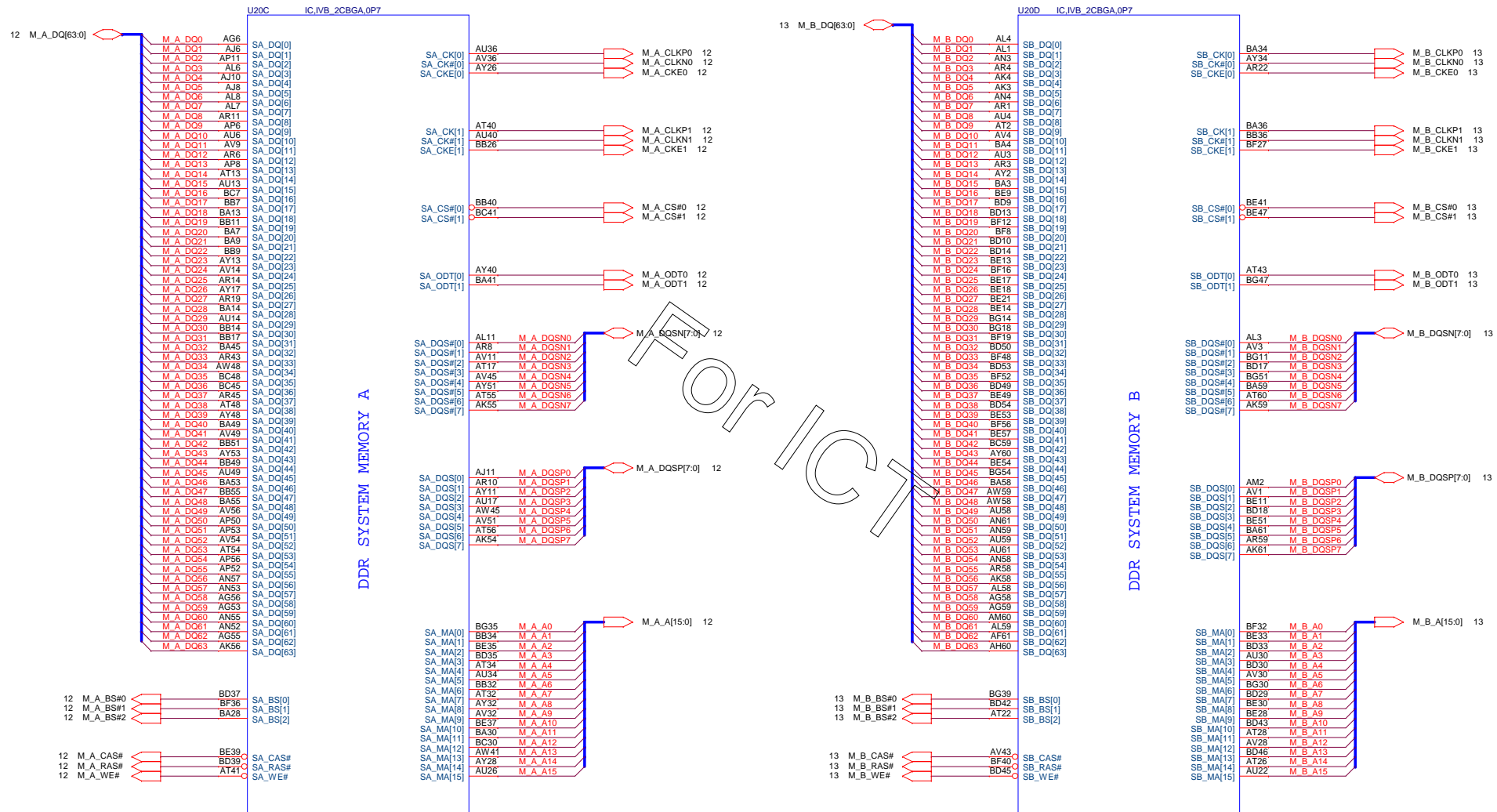
**SLG55448V**  
System Discharge Power  
(+1.5V/+3V/+5V)

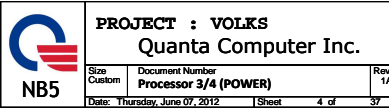
**Richtek RT8207**  
System Memory Power (+1.5VSUS/  
+0.75V\_DDR\_VTT)

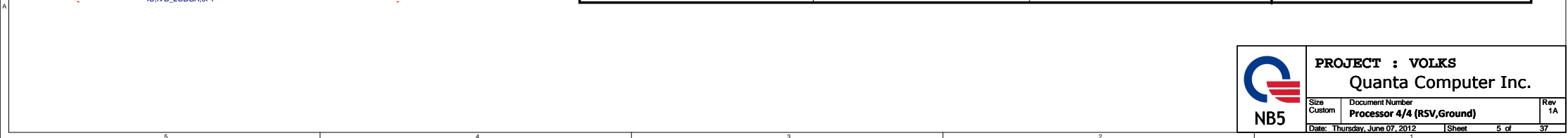
**NCP3218G**  
GPU core power(+VGACORE)



## Ivy Bridge Processor (DDR3)





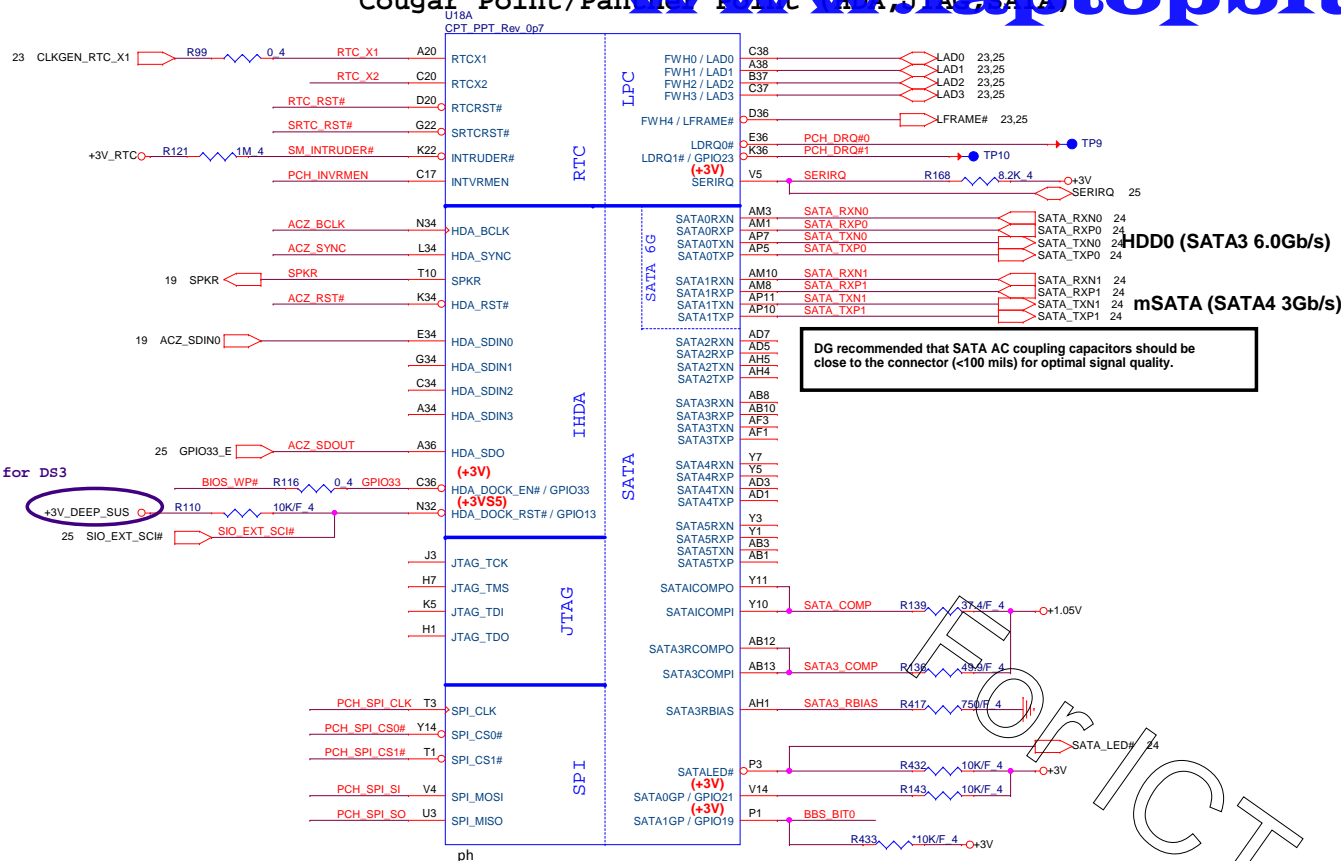






### System PWR\_OK(CLG)

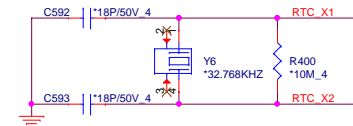




PCH Strap Table

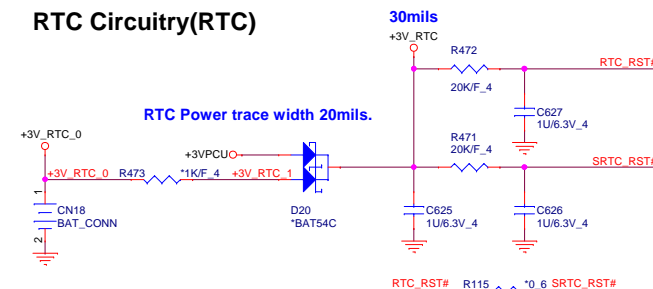
Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>0</td><td>1</td><td>SPI</td></tr><tr><td>1</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	0	1	SPI	1	0	LPC	
GNT1#	GNT0#	Boot Location											
0	1	SPI											
1	0	LPC											
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										

## RTC Clock 32.768KHz

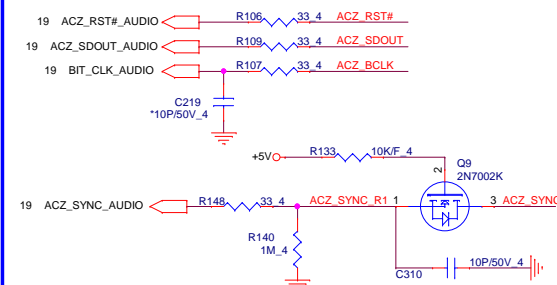


no stuff if use green Clock

## RTC Circuitry(RTC)

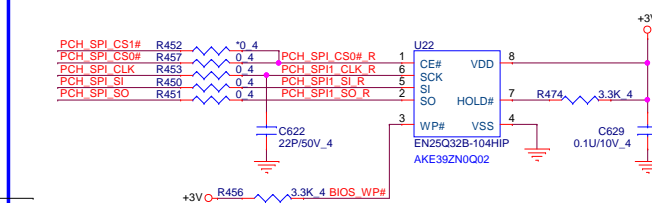


## HDA Bus(CLG)



Vender	Size	P/N
EON	4MB	AKE392N0Q02 (EN25Q32B-104HIP)
MX	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023

## PCH SPI ROM(CLG)



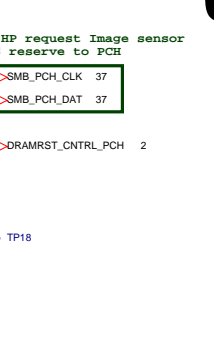
+3V	6,8,9,10,12,13,14,16,19,20,21,22,23,24,25,26,30,32,34,36
+5V	10,19,21,22,23,24,26,36
+1.8V	4,10,31
+1.05V	2,4,6,8,10,21,23,30,33,34
+3VSS	6,10,23,28,30,33,36
+3VPCU	21,22,23,24,25,26,27,28
+3V_RTC	6,10,23



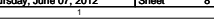
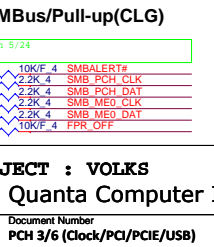
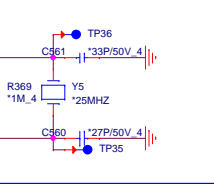
PROJECT : VOLKS  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (HDA/RTC/SATA/SPI)	1A
Date: Thursday, June 07, 2012	Sheet	7 of 37

Cougar Point M/Panther Point (PCI-E,SMBUS,CLK)



NUMBER OF SUBJECTS







for DS3

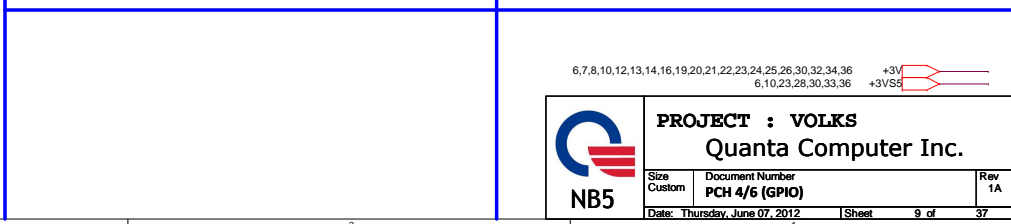
8 BOARD\_ID0  
8 BOARD\_ID1  
8 BOARD\_ID2  
8 BOARD\_ID3

R147 \*10K/F 4 BOARD\_ID0 R144 \*10K/F 4  
R166 \*10K/F 4 BOARD\_ID1 R167 \*10K/F 4  
R138 \*10K/F 4 BOARD\_ID2 R158 \*10K/F 4  
R355 \*10K/F 4 BOARD\_ID3 R356 \*10K/F 4  
R78 \*10K/F 4 BOARD\_ID4 R79 \*10K/F 4  
R84 \*10K/F 4 BOARD\_ID5 R85 \*10K/F 4  
R423 \*10K/F 4 DGPU PRSNT R422 \*10K/F 4

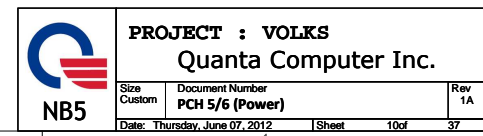
Rb Ra

+3V\_DEEP\_SLEEP  
+3V\_DEEP\_SLEEP  
+3V\_DEEP\_SLEEP  
+3V

	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

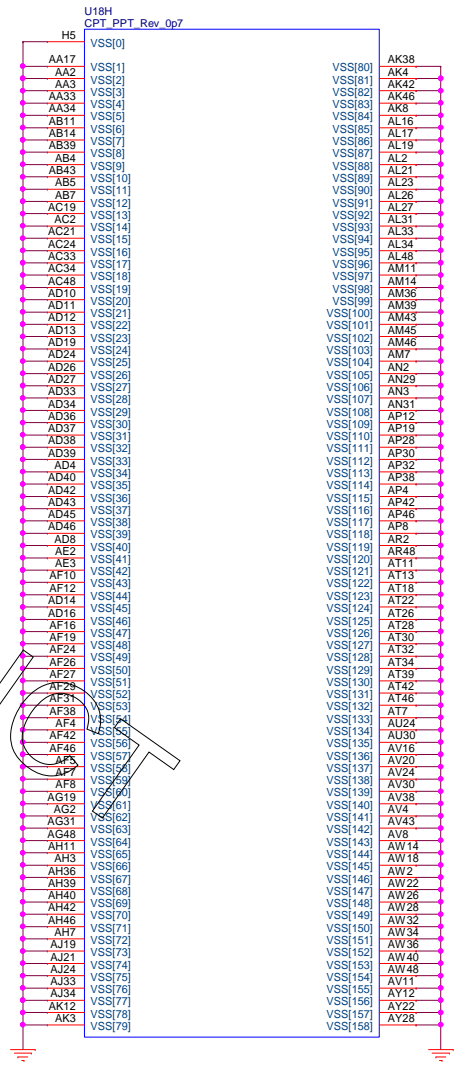
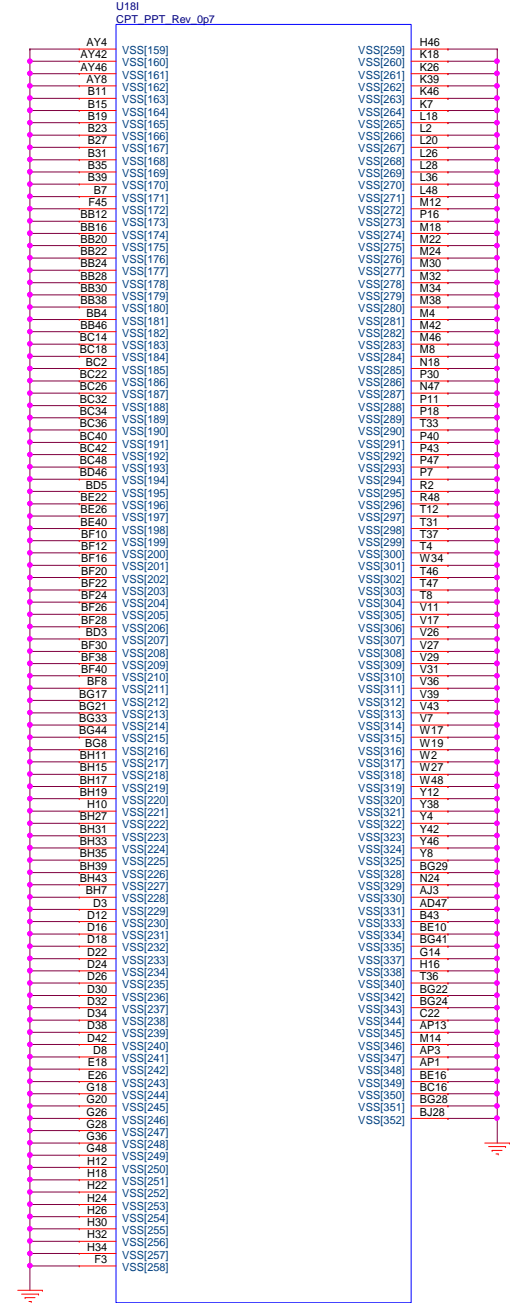


Cougar Point/Panther Point (POWER)

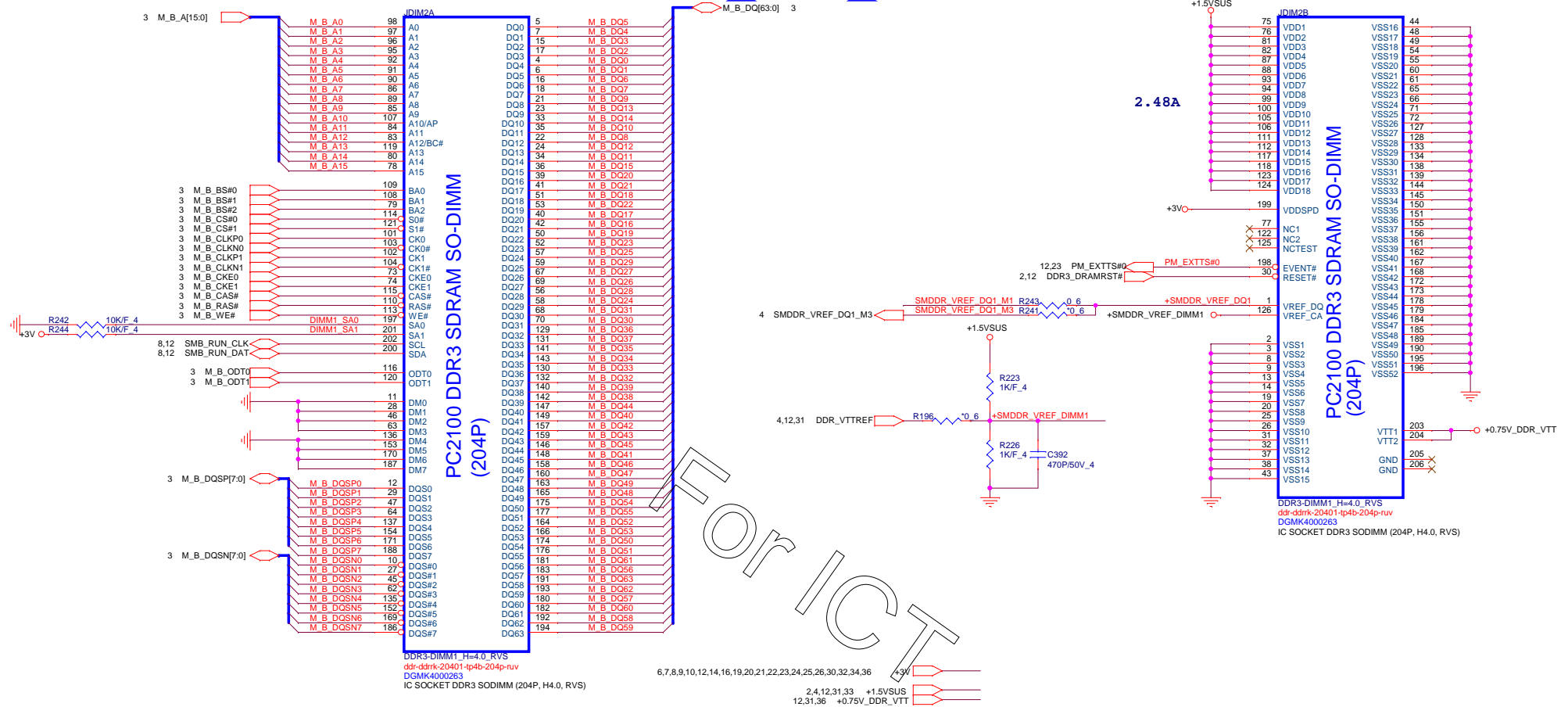


Cougar Point/Panther Point (GND)

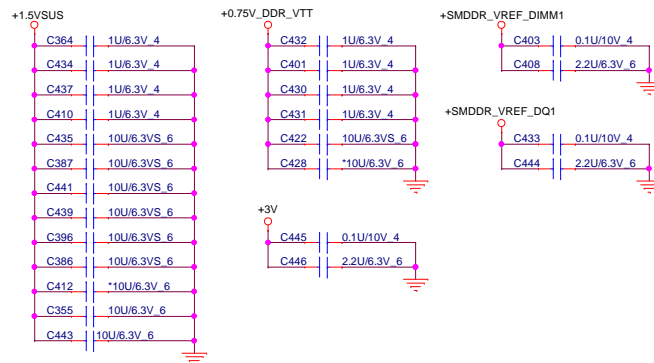
Cougar Point/Panther Point (GND)



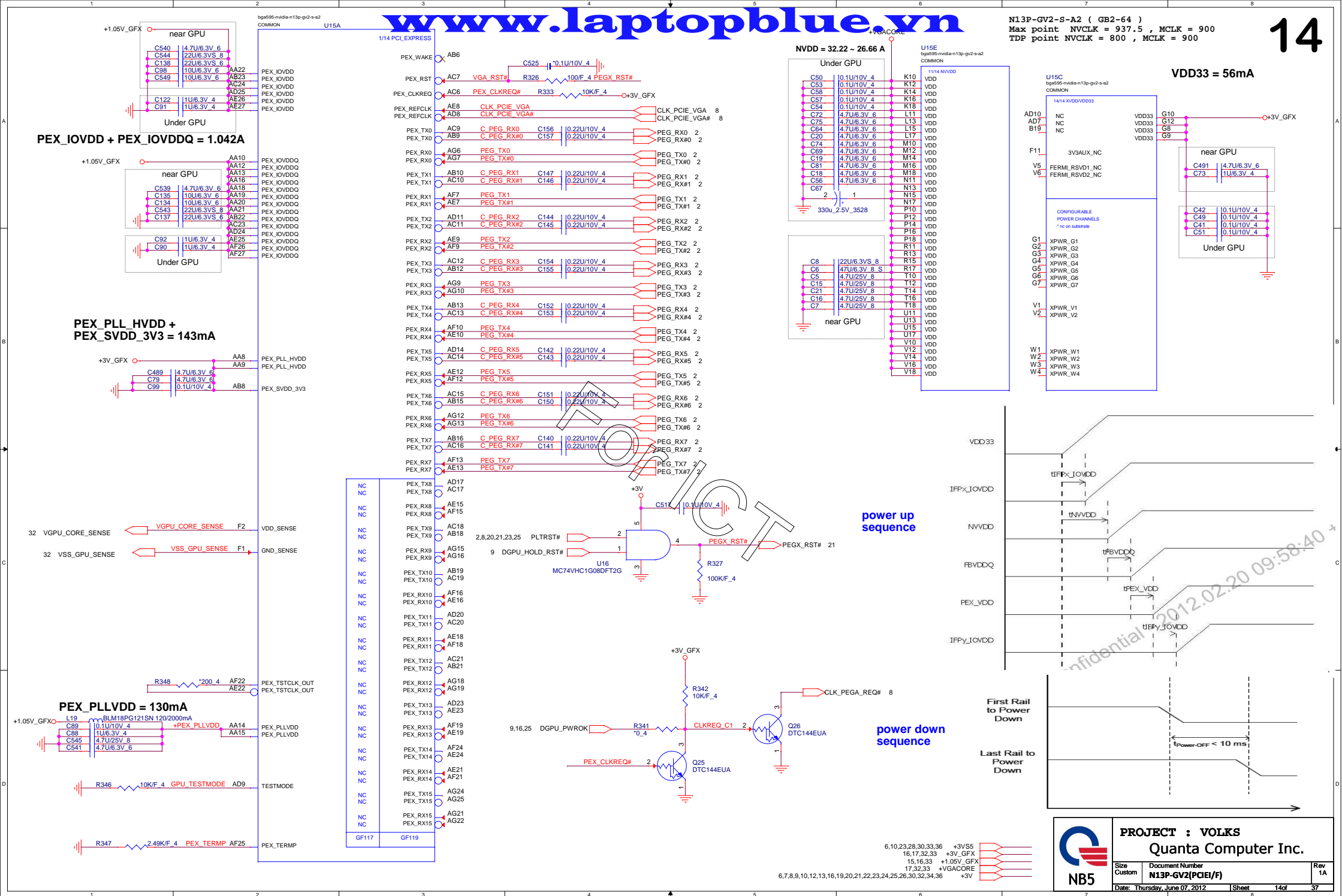


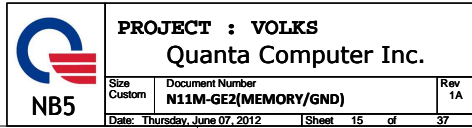


## Place these Caps near So-Dimm1.

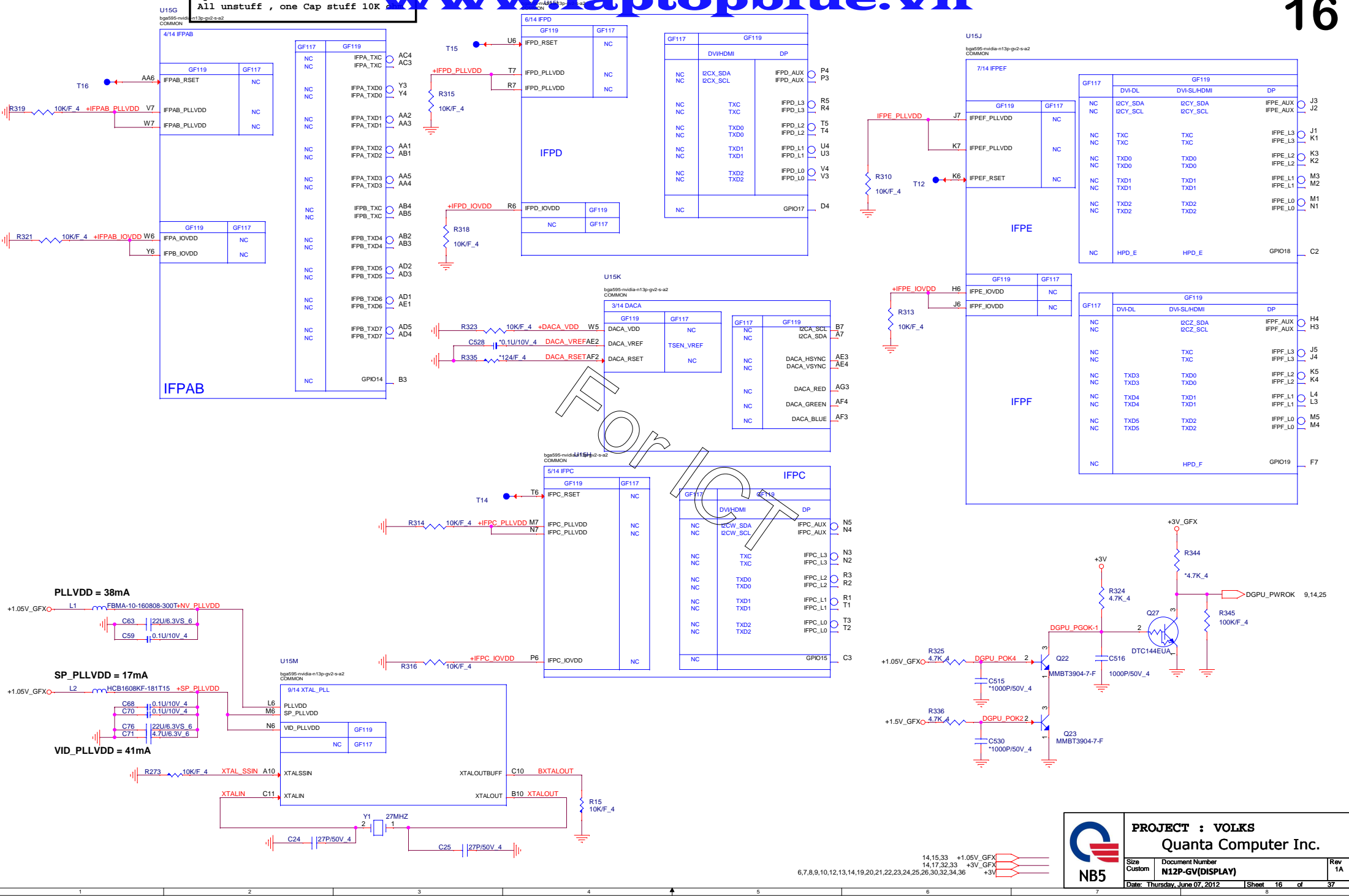


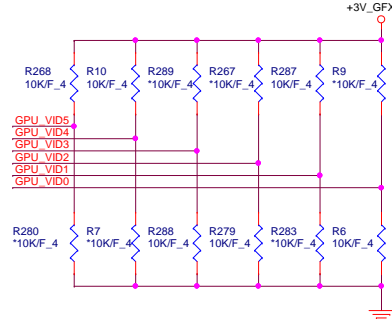




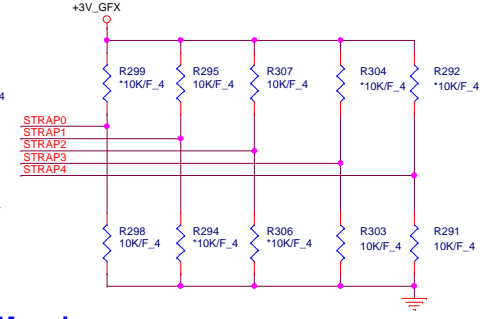
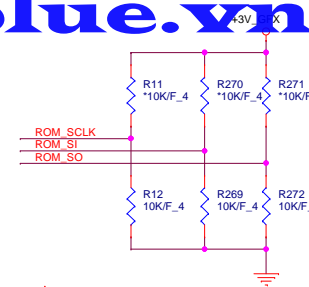
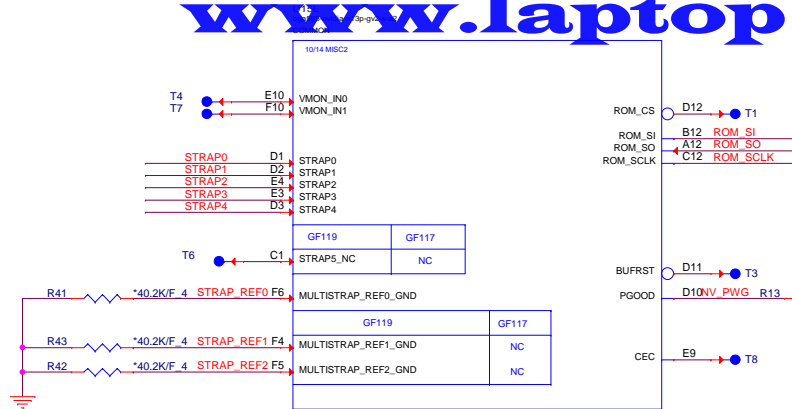


Optimus:  
All unstuff , one Cap stuff 10K





N13P-GV2 NVDD HW BOOT Voltage = 0.875V  
VID = 0110010



## Binary Strap Mode Mapping

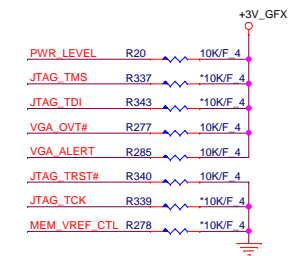
Strap Pin name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10Kohm	Pull-down to GND
ROM_SI	SUB_VENDOR	10Kohm	Pull-up to 3V3 if VBIOS ROM Exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10Kohm	Pull-down to GND ( no dispaly )
STRAP0	RAMCFG[0]	10Kohm	USER defined
STRAP1	RAMCFG[1]	10Kohm	USER defined
STRAP2	RAMCFG[2]	10Kohm	USER defined
STRAP3	RAMCFG[3]	10Kohm	USER defined
STRAP4	PCIE_MAX_SPEED	10Kohm	Pull-down to GND

## VRAM Configuration Table

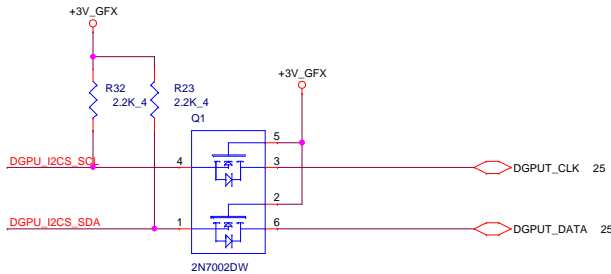
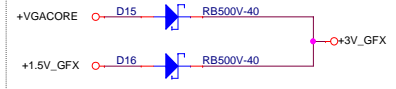
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QBCON P/N	HP P/N
0011 0101 1100 0101	(MP) DDR3 256Mx16x4, 64bit, 2Gb,900MHz DDR3 256Mx16x4, 64bit, 2Gb,900MHz DDR3 128Mx16x4, 64bit, 1Gb,900MHz DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Reserved Hynix Micron Hynix Samsung	H5TQ4G63MFR-11C MT41K256M16HA-107G:E H5TQ2G63DFR-11C K4W2G1646C-HC11	AKD5PGWTW00 AKD5PGSTL01 AKD5MGWTW12 AKD5MGWT513	AKD5PGWTW01 AKD5PGSTL02 AKD5MGWTW13 AKD5MGWT508
0001 0100 1011	(OOC) DDR3 256Mx16x4, 64bit, 2Gb,900MHz DDR3 256Mx16x4, 64bit, 2Gb,900MHz DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Samsung Hynix Samsung	K4W4G1646B-HC11 H5TQ4G63AFR-11C K4W2G1646E-BC11	AKD5MGWT518 applying AKD5MGGT521	AKD5MGWT517 applying AKD5MGGT522

## GB2-64 and GB4-128 GPIO Description

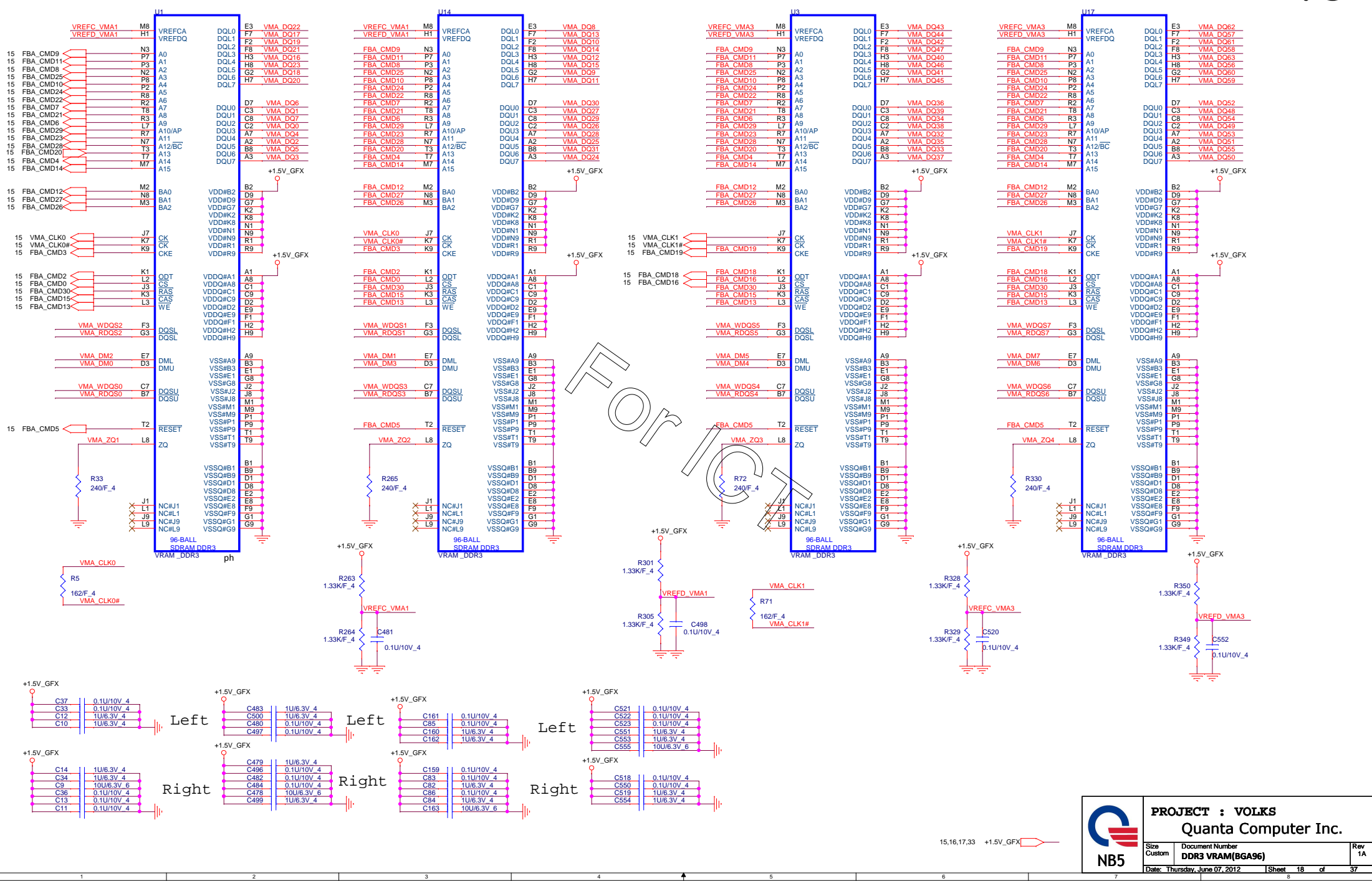
GPIO pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	GPU_VID4	O	GPU Core VDD VID4	Strap to boot NVDD
GPIO1	GPU_VID3	O	GPU Core VDD VID3	Strap to boot NVDD
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding	LCD_VCC: 100K pull-down PSI: 10K pull-up or pull-down; stuff as needed to disable phase shedding by default
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 K pull-down
GPIO5	GPU_VID1	O	GPU Core VDD VID1	Strap to boot NVDD
GPIO6	GPU_VID2	O	GPU Core VDD VID2	Strap to boot NVDD
GPIO7	3DIVISION	O	3D Vision Left/Right signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	GPU_VID0	O	GPU Core VDD VID0	Strap to boot NVDD
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	GPU_VID5	O	GPU Core VDD VID5	Strap to boot NVDD
GPIO14	HPD_AB	I	Hot Plug Detect for IFPA	See Figure 76
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 76
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID	PSI: 10K pull-up or pull-down; stuff as needed to disable phase shedding by default MEM_VDD_CTL: Strap to boot FBVDD/Q
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 76
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 76
GPIO19	HPD_F	I	Hot Plug Detect for IFPF	See Figure 76
GPIO20	Reserved			
GPIO21	Reserved			



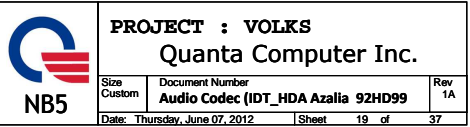
for meet Power down sequence.  
Nvidia request for optimus

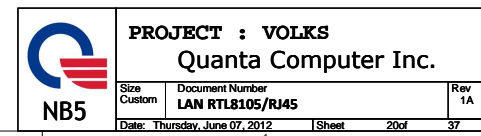


14,16,32,33 +3V\_GFX

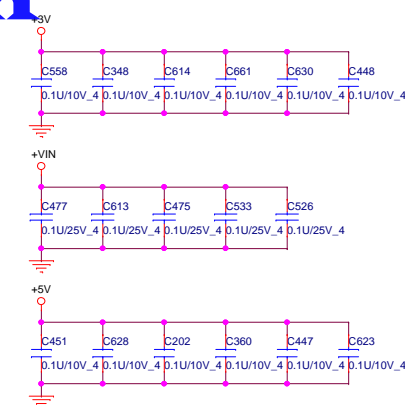
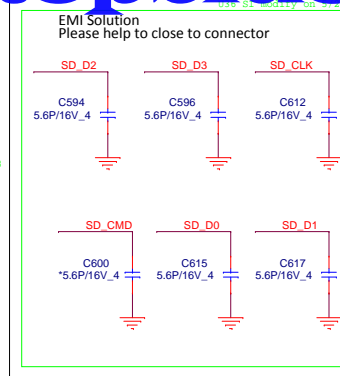




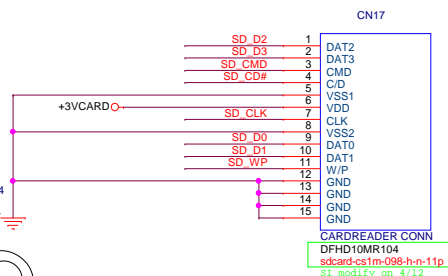




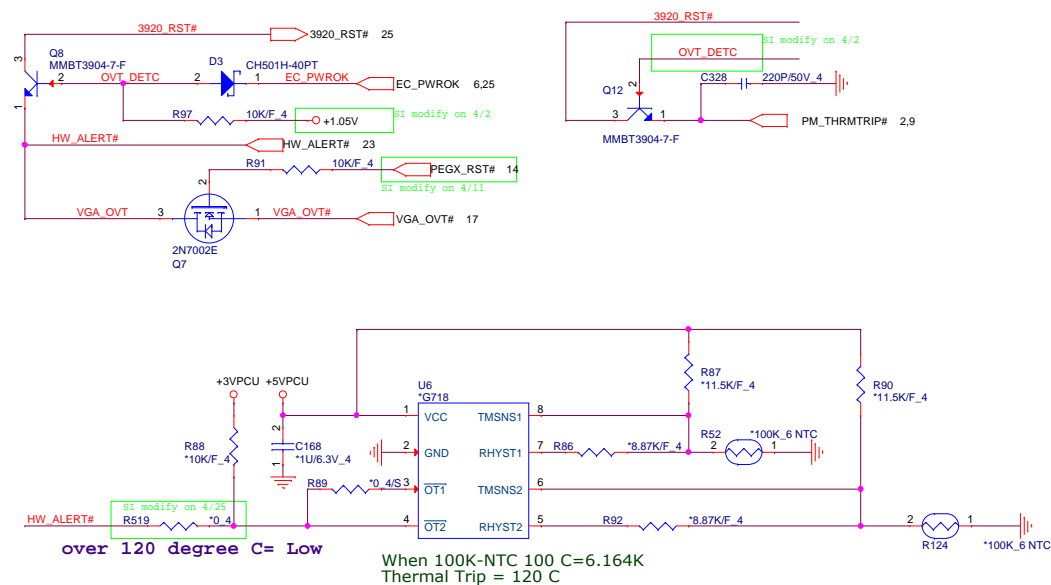
## SD / MMC



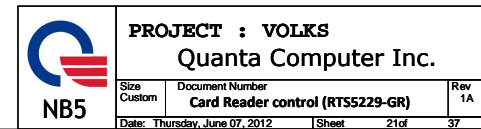
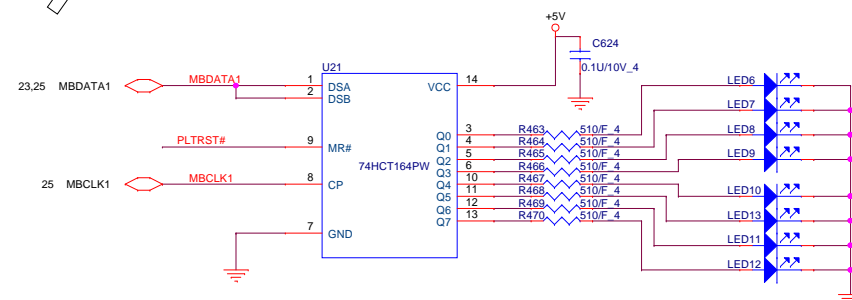
Close to chip pin

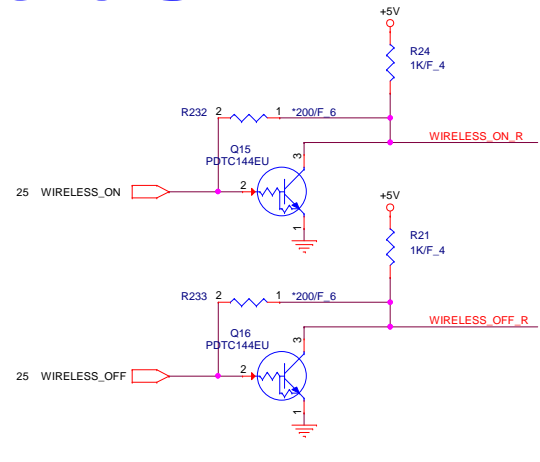
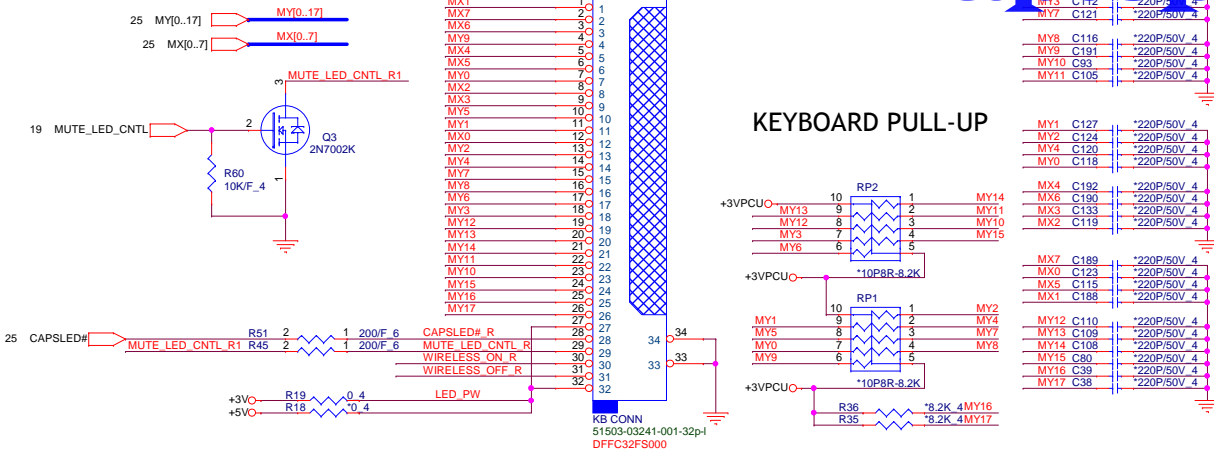


## Thermal HW protect

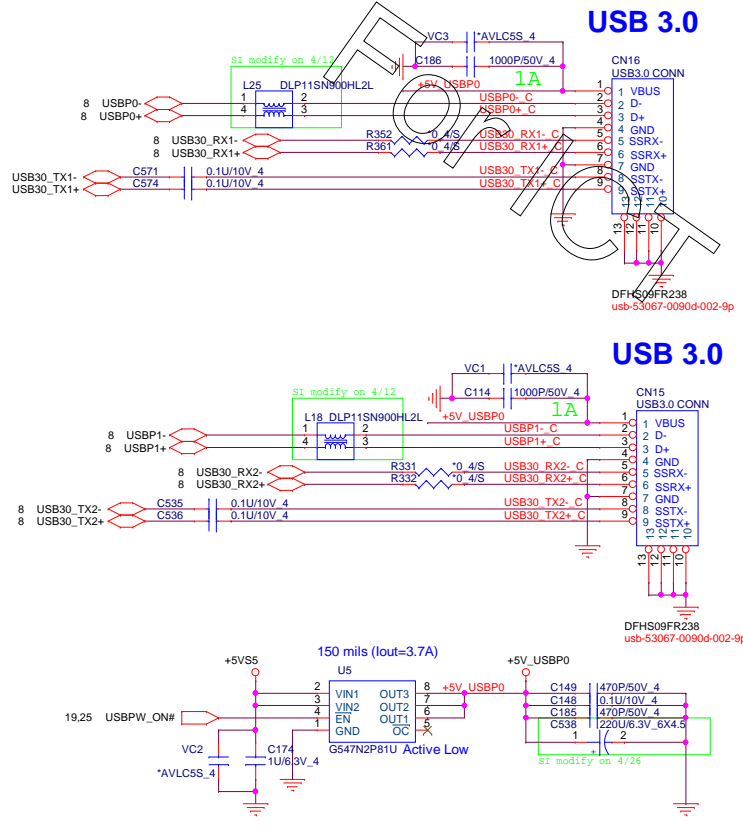
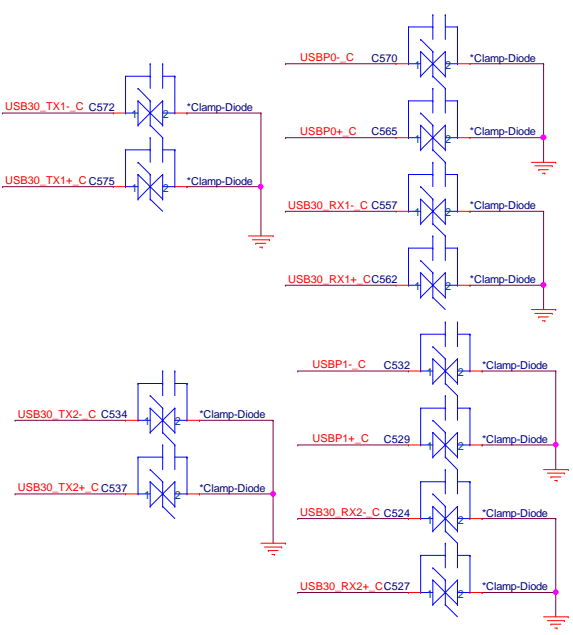


80 port

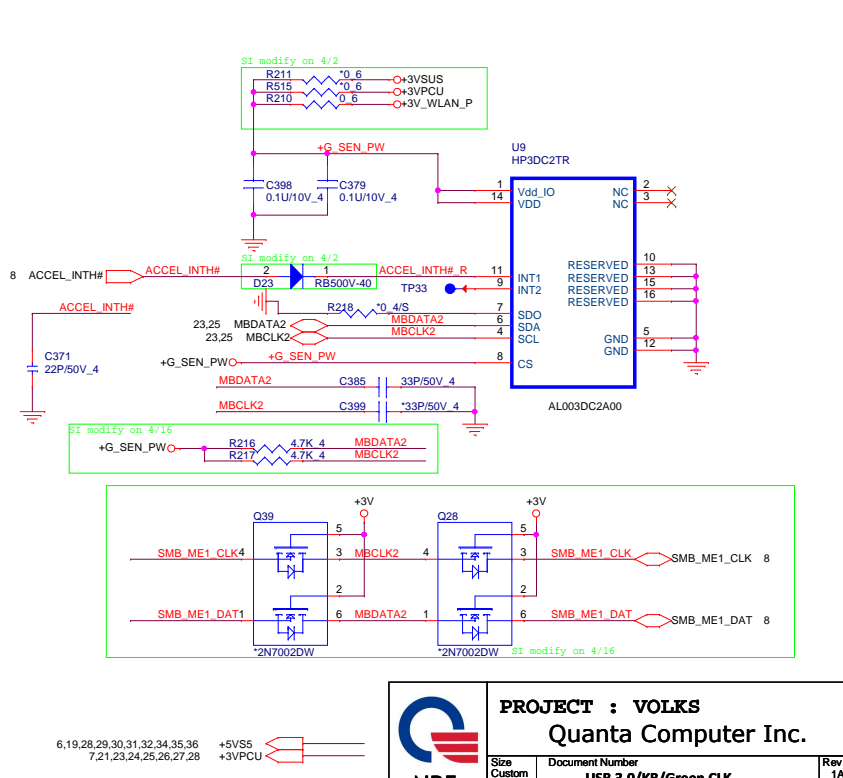




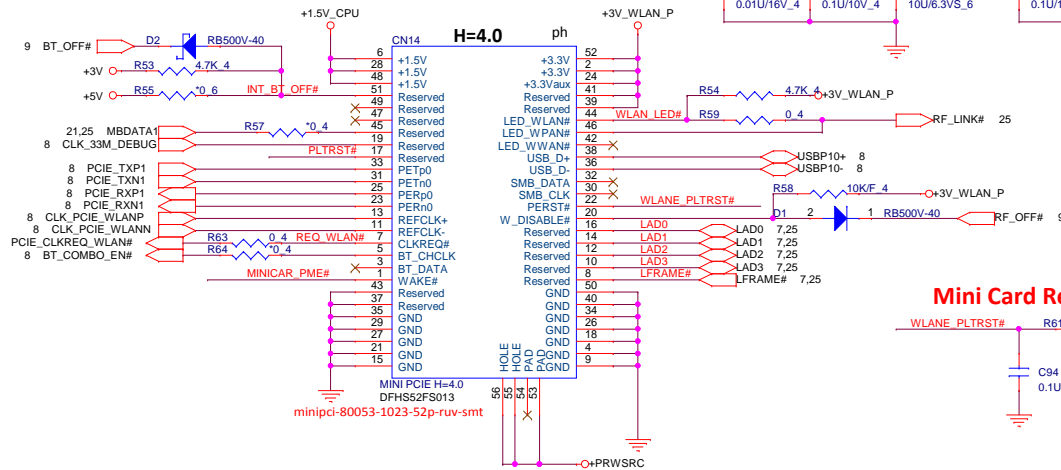
USB 2.0/3.0 Combo



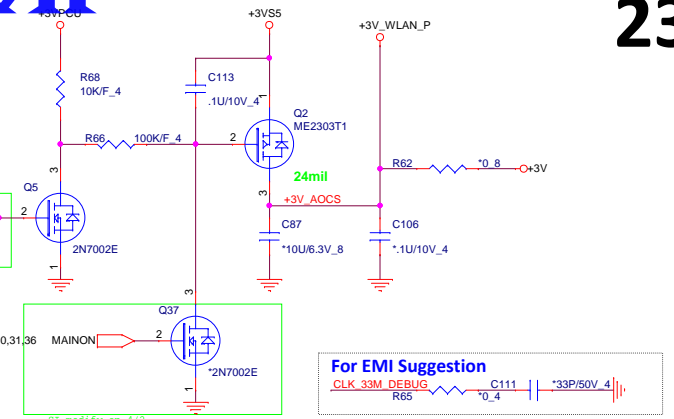
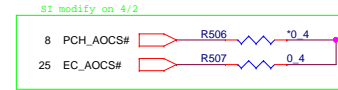
Accelerometer Sensor



Mini Card  
WLAN/BT(Optional)

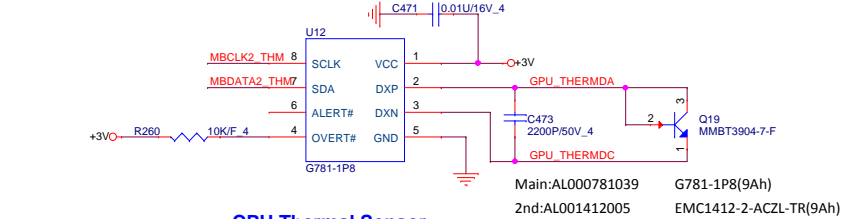


Mini Card Reset

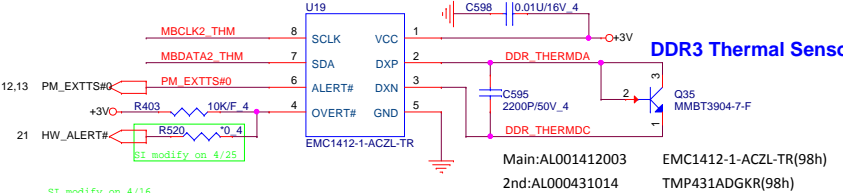


Local Thermal Sensor

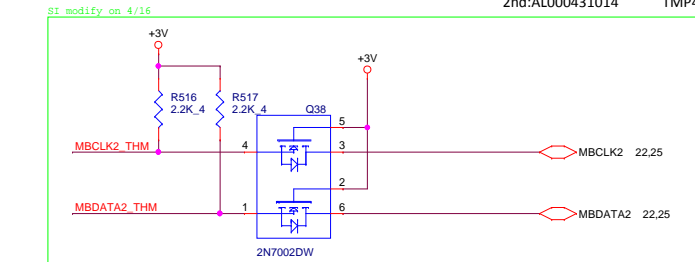
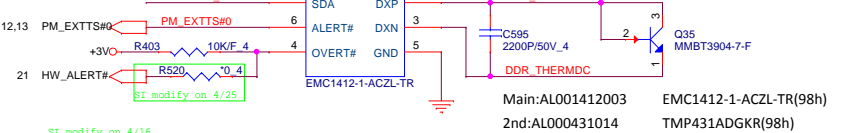
GPU Thermal Sensor



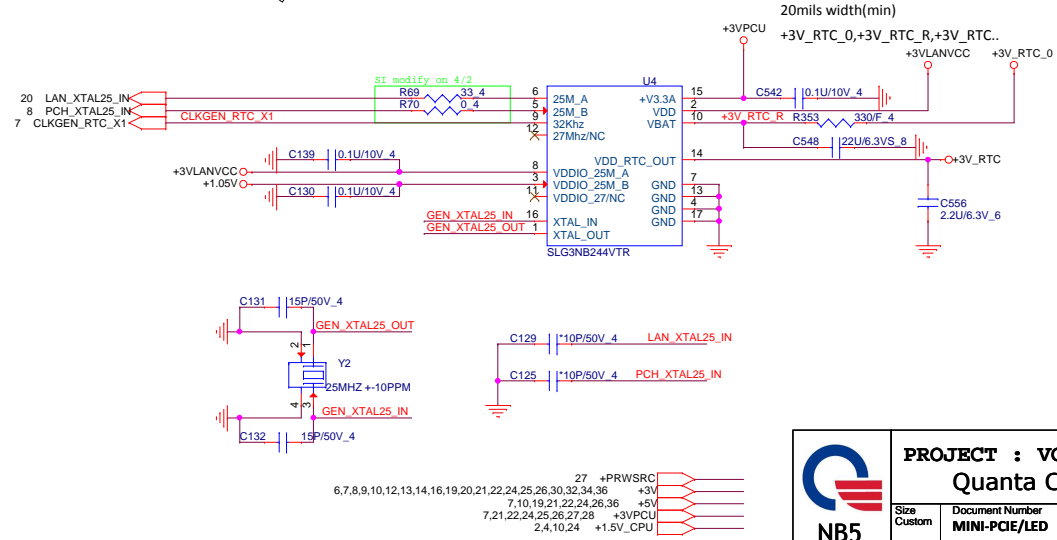
CPU Thermal Sensor



DDR3 Thermal Sensor



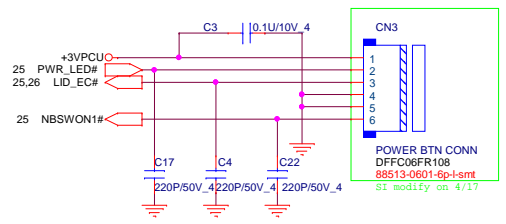
Green CLK Circuitry



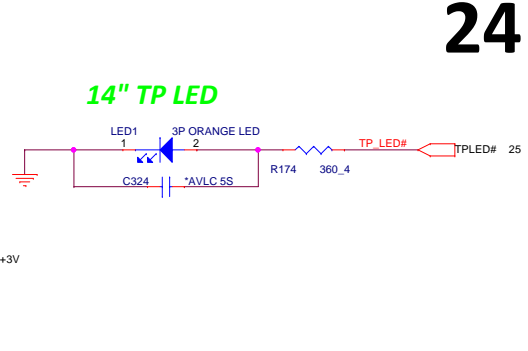
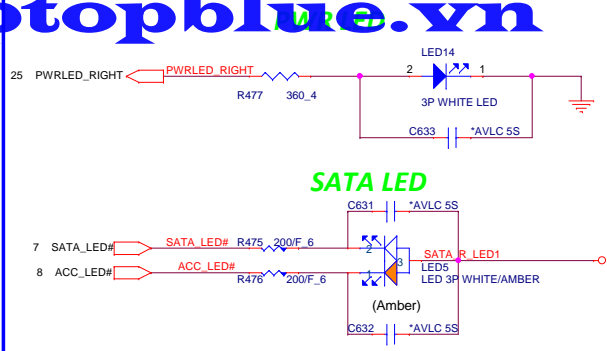
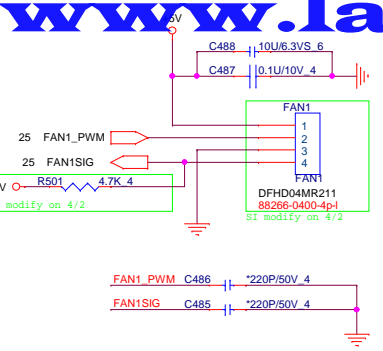


# Power Button Connector

Pin1 : +3VPCU(LIDSWITCH PWR)  
Pin2 : POWER LED  
Pin3 : LIDSWITCH  
Pin4 : GND  
Pin5 : GND  
Pin6 : POWERON#

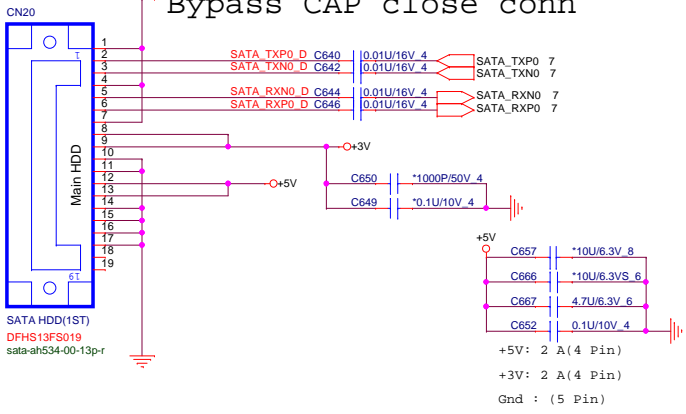


# FAN

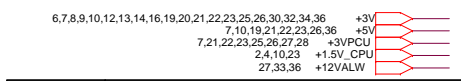
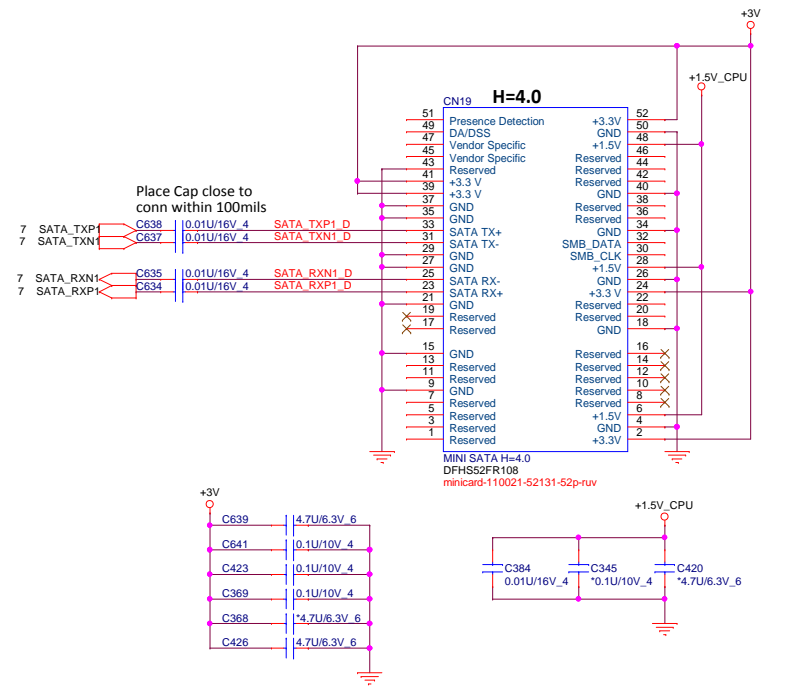


# SATA HDD Connector(Cable type)

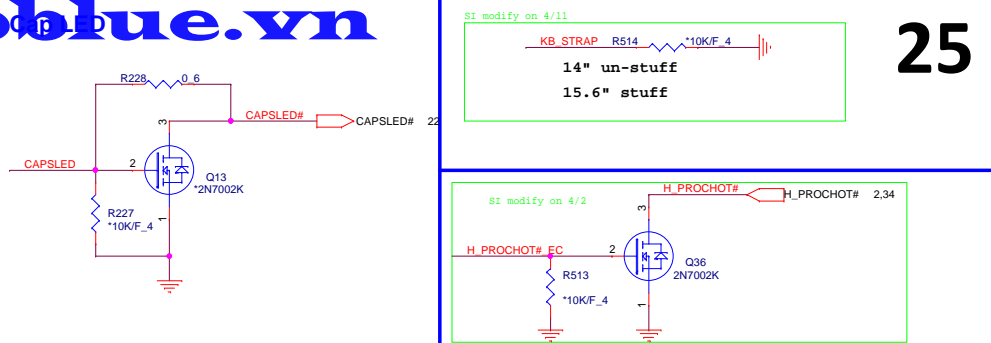
Bypass CAP close conn



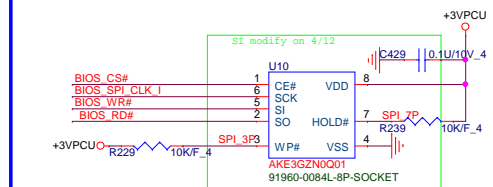
# Mini PCI-E Card 2- Full size mSATA



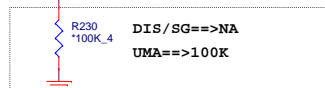
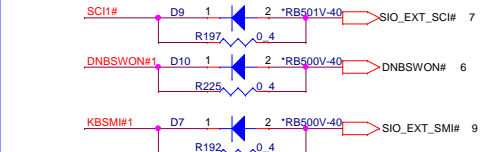
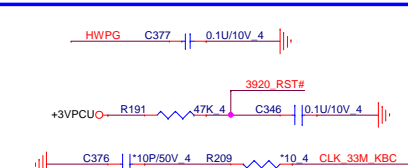
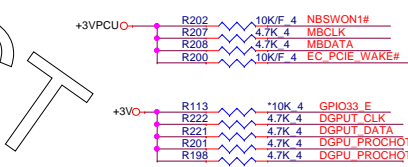
NB5	PROJECT : VOLKS		
	Quanta Computer Inc.		
	Size Custom	Document Number	Rev 1A
	SATA HDD/ODD/MSATA CONN		
Date: Thursday, June 07, 2012		Sheet	24 of 37

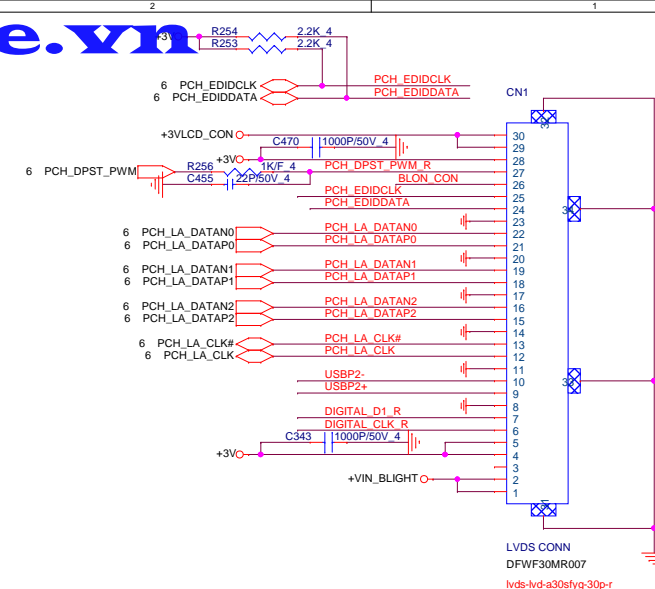
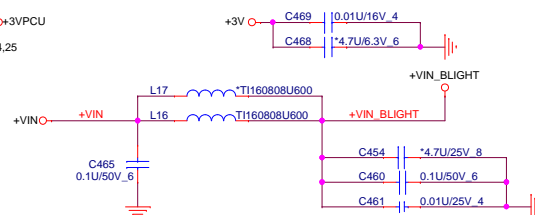
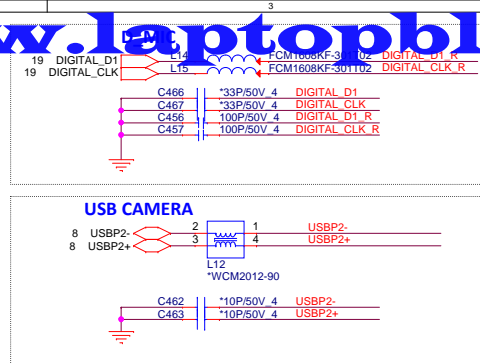


## Adapter select for EC



MBCLK2	C381	*10P/50V 4
MBDATA2	C380	*10P/50V 4
MBCLK	C373	*10P/50V 4
MBDATA	C375	*10P/50V 4
DGPWT_CLK	C389	*10P/50V 4
DGPWT_DATA	C388	*10P/50V 4

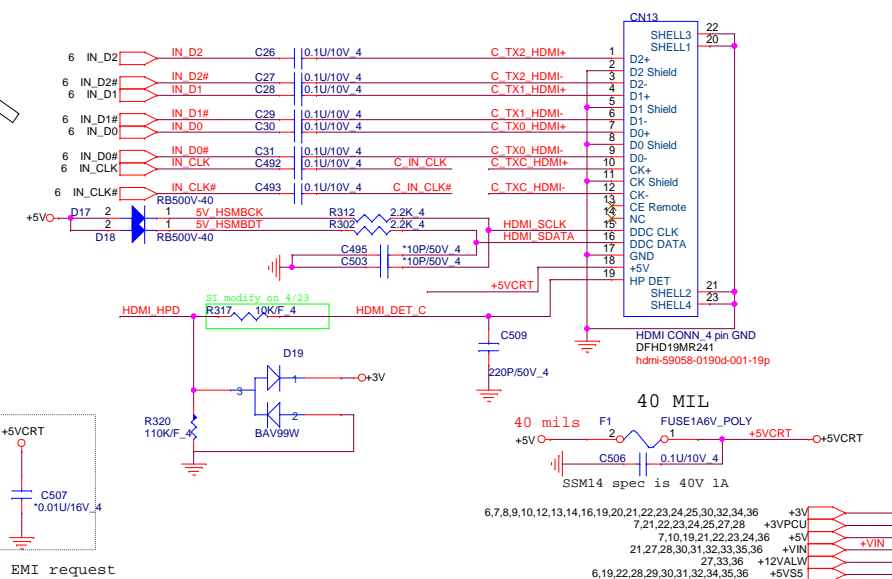
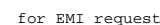
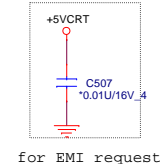
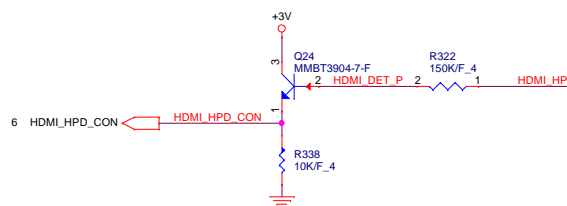
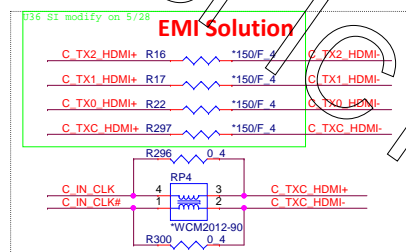
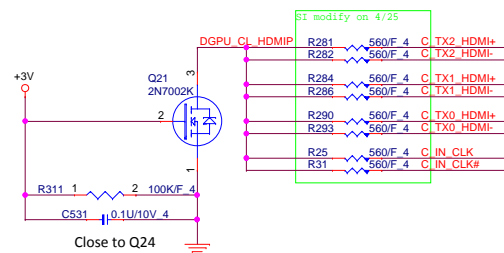


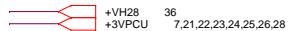
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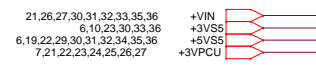
### HDMI SMBus Isolation

**HDMI SMBus Isolation**

The diagram illustrates the connection for the HDMI SMBus Isolation circuit. The MOSFET (2N7002DW) is connected to the HDMI SCL and SDA lines. The gate is connected to +3V through a 2.2K resistor (R308). The drain is connected to the HDMI SCL line (pin 4) through a 2.2K resistor (R309). The source is connected to ground. The MOSFET is controlled by SDVO\_CLK (pin 6) and SDVO\_DATA (pin 6). The HDMI SCL line (pin 4) is connected to the MOSFET drain. The HDMI SDA line (pin 6) is connected to the MOSFET source. The MOSFET is labeled 2N7002DW. The circuit is labeled "Close to HDMI connector".







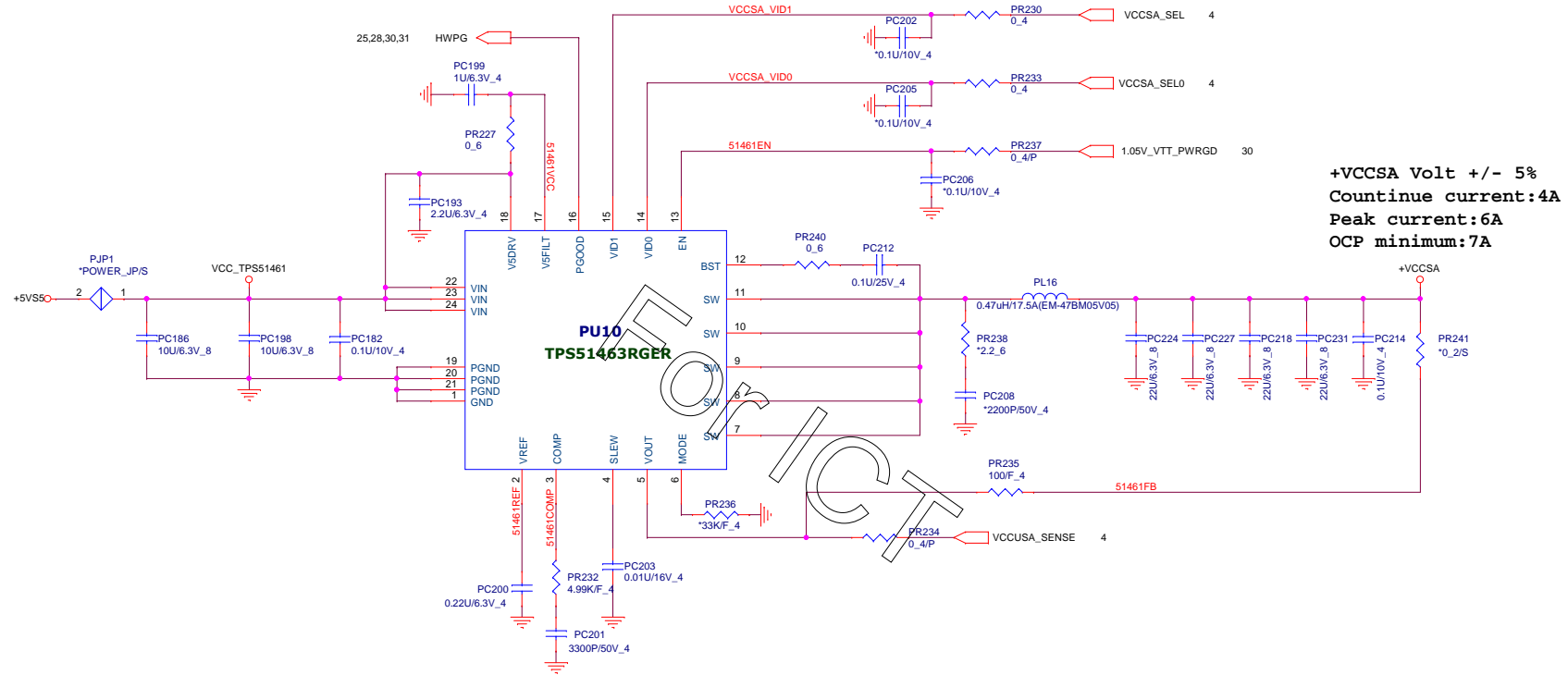


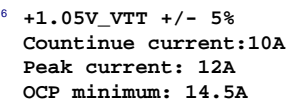
**TPS51462RGER/AL051462000**  
For CPU SV system agent  
voltage slew rate of 0.5 -10 mV/ $\mu$ s

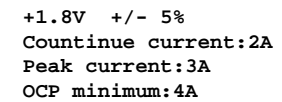
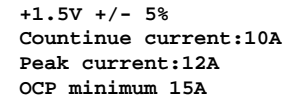
SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V


**TPS51463RGER/AL051463000**  
For CPU ULV system agent  
voltage slew rate of 0.5 -10 mV/ $\mu$ s

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

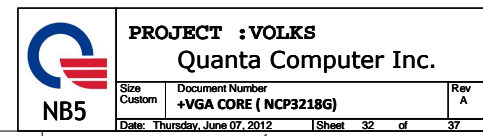




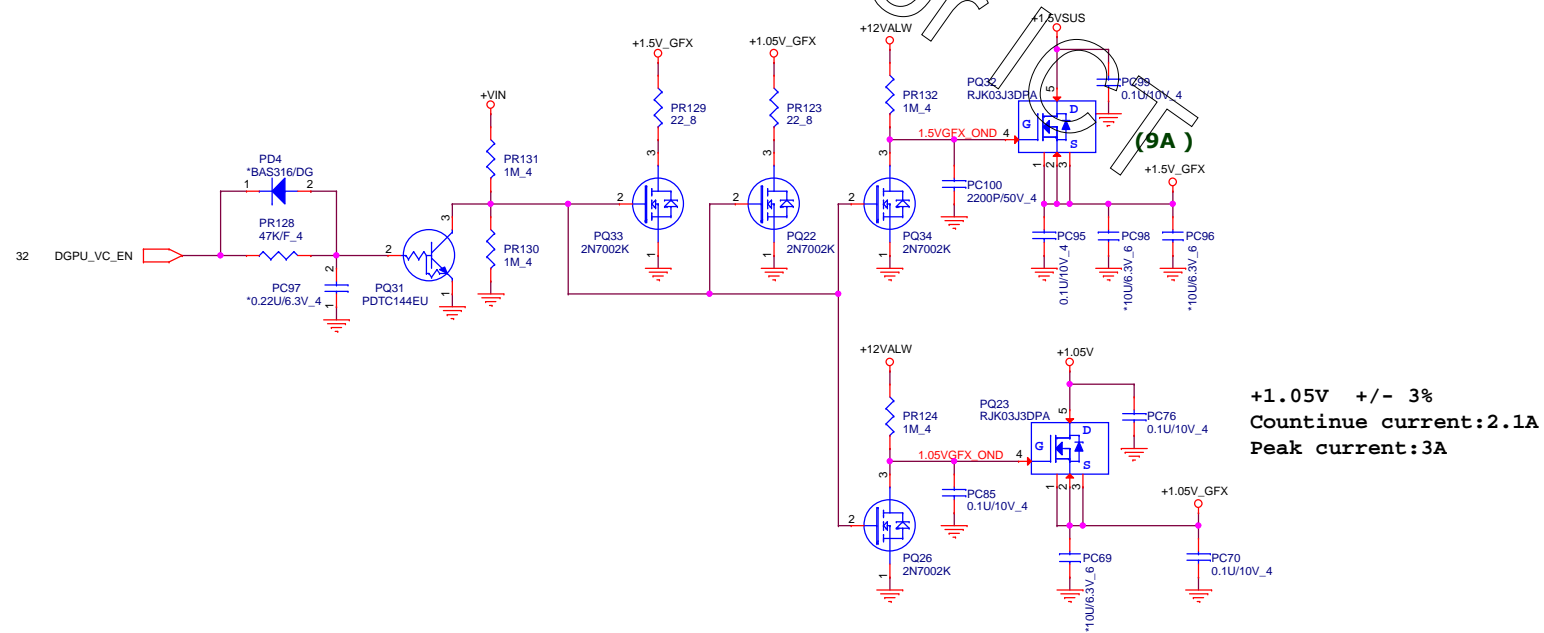
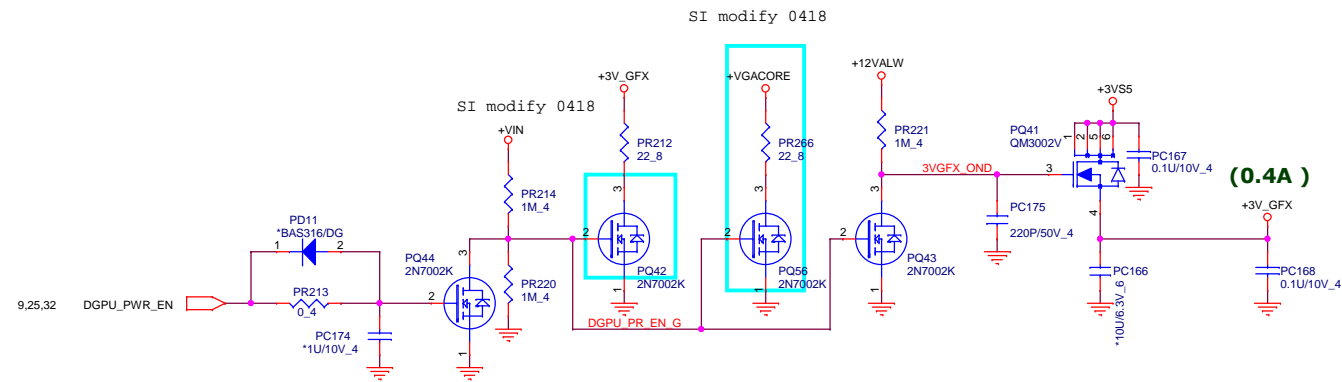


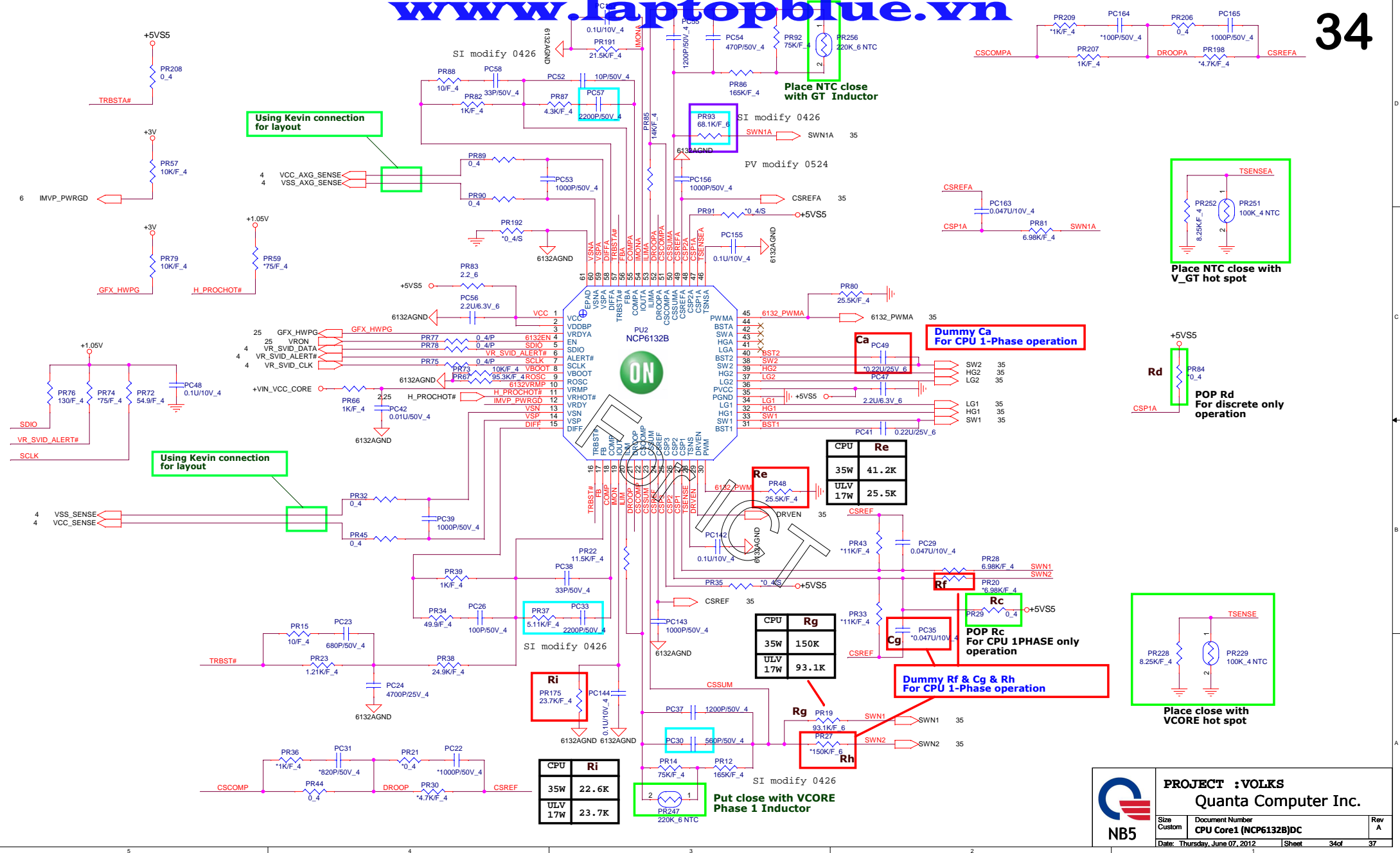
 <b>NB5</b>	<b>PROJECT :VOLKS</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>DDR3 (RT8207)</b>	Rev A
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Countinue current: 45A  
Peak current: 50A  
OCP minimum 56A



2,4,12,13,31	+1.5VSUS	
6,10,23,28,30,36	+3VS5	
14,16,17,32	+3V_GFX	
15,16,17,18	+1.5V_GFX	
14,15,16	+1.05V_GFX	
27,36	+12VALW	
2,4,6,7,8,10,21,23,30,34	+1.05V	

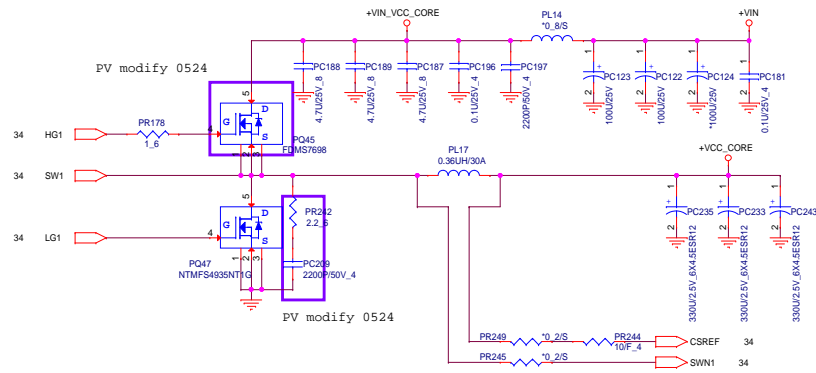




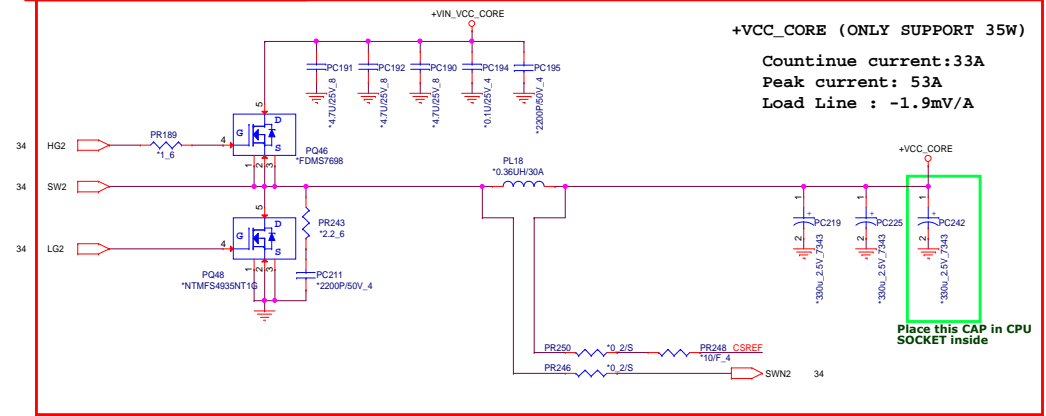
**PROJECT :VOLKS**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>CPU Core1 (NCP6132B)DC</b>	Rev A
Date: Thursday, June 07, 2012		Sheet 34 of 37





Dummy This Schematic  
For CPU 1-Phase operation



+VCC\_CORE (ONLY SUPPORT 35W)

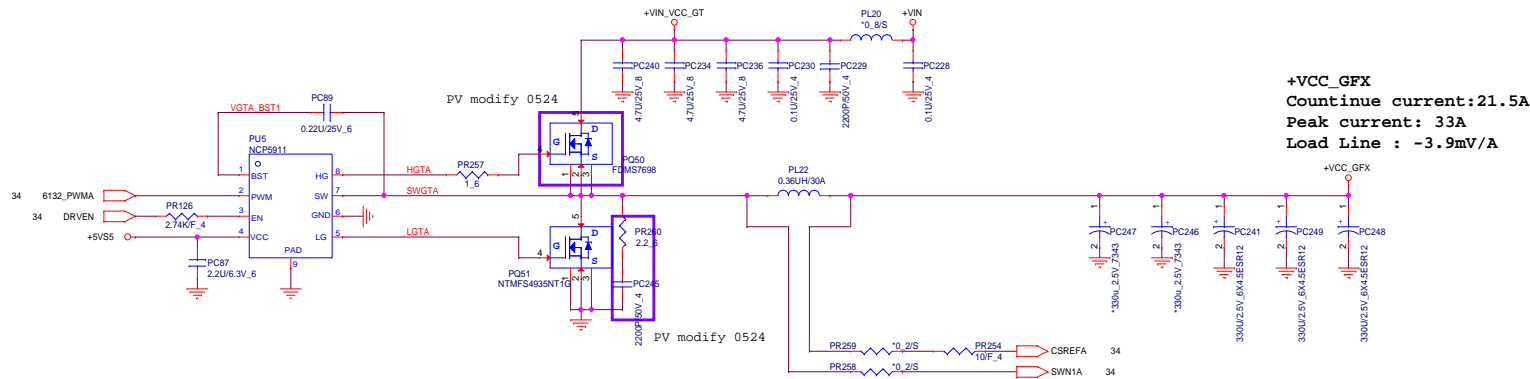
Countinue current:33A  
Peak current: 53A  
Load Line : -1.9mV/A

+VCC\_CORE (ONLY SUPPORT 35W)

Countinue current:32A  
Peak current: 53A  
Load Line : -1.9mV/A

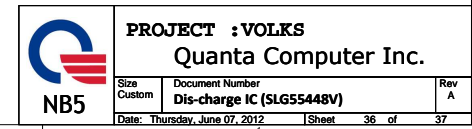
+VCC\_CORE (ULV 17W)

Countinue current:16A  
Peak current: 33A  
Load Line : -2.9mV/A

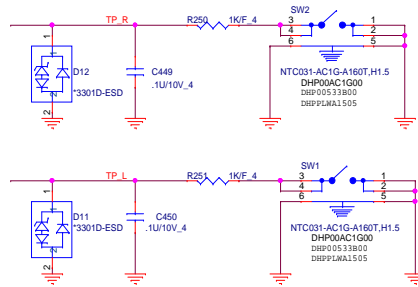
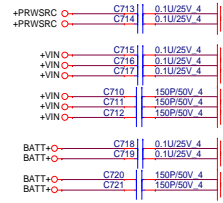
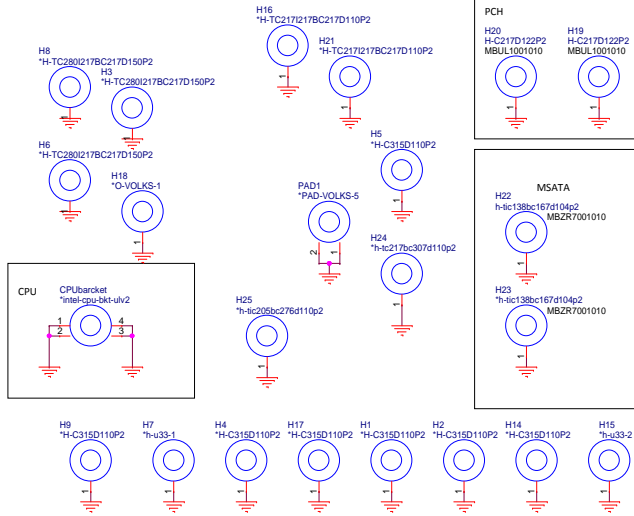


+VCC\_GFX

Countinue current:21.5A  
Peak current: 33A  
Load Line : -3.9mV/A



# 14" Hole



## Touch Pad Connector

