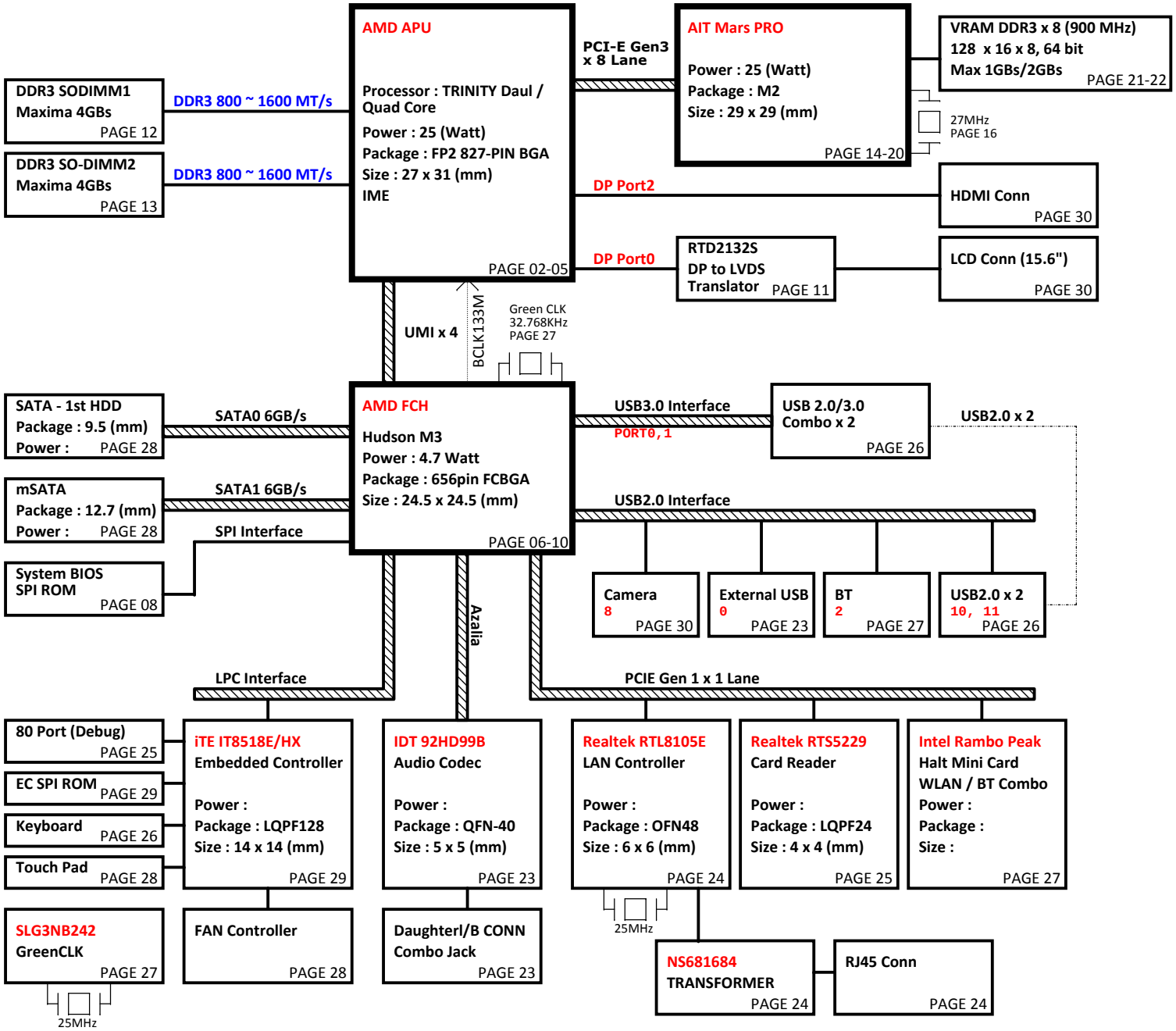
Volks_AMD Comal DIS/UMA (14") Ultra/Slim

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24728
System Charge Power (+BATCHG)

G5934RZ1U
System Discharge Power (+1.5V/+3V/+5V)
(+3VSUSV/+3VLANVCC/+1.1V)

Ricktek RT8223PZ
System Power (+3VPCU/+5VPCU/ +3VS5/+5VS5)

ISL6277/RT8228AZ/AP3407A/ISL6208BCRZ
Processor Power (+VCC_CORE/ +1.2V/+2.5V/+VDDNB_CORE)

Richtek RT8207L
System Memory Power (+1.5VSUS/ +0.75V_DDR_VTT)

Richtek RT8228AZ
PCH Power (+1.1VS5)

RT8152E/G5193/G5193R41U/NB650
DGPU Power (+VGA_CORE/+1.0V_VGA/+3V_VGA/ +1.5V_VGA/+1.8V_VGA/+VDDCI)

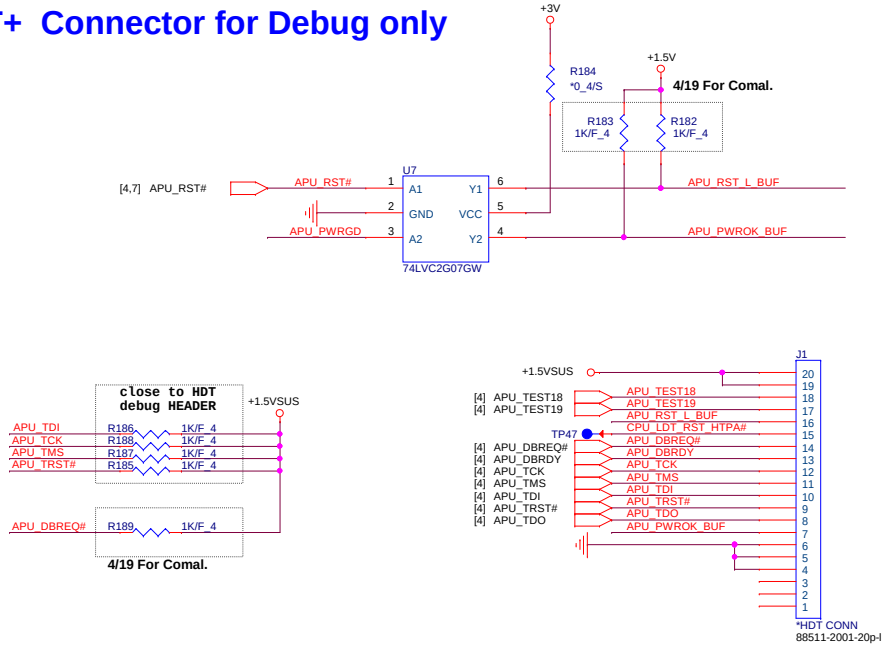
NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
A3	Block Diagram	1A

Date: Thursday, September 20, 2012 | Sheet 1 of 42

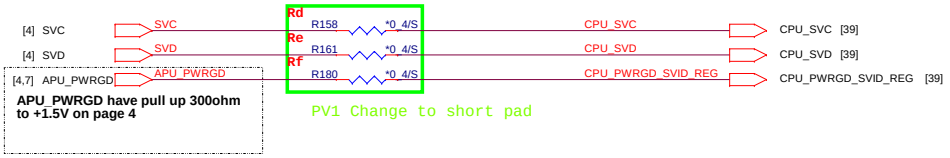
HDT+ Connector for Debug only



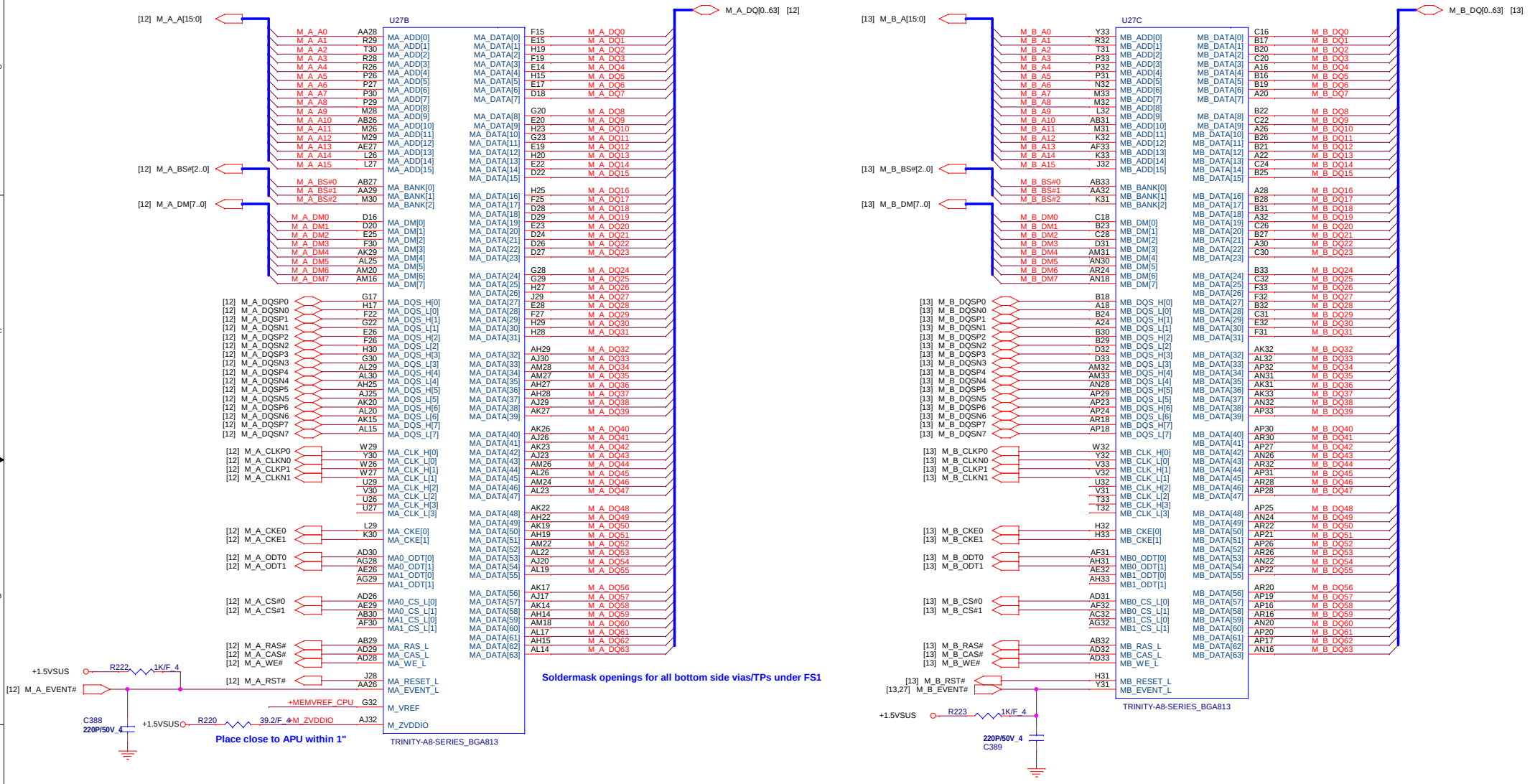
VID Override Circuit

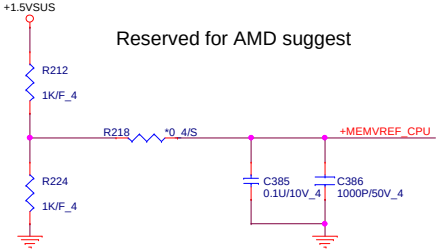
	BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

Note:
To override VID,Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.



NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size: Custom	Document Number: Llano PCIE/UMI/GPP	Rev: 1A
Date: Thursday, September 20, 2012	Sheet 2 of 42	





NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size: Custom	Document Number: Llano DDR3 MEM I/F	Rev: 1A
Date: Thursday, September 20, 2012	Sheet 3 of 42	

Place caps within 500 < 200 mil
route PCIE as 85ohm +/- 10%

DP0 output to
eDP to LVDS converter

Display port power 1.5V min 1.2v max : 1.65v

4/19 HDMI change to DP2 for Comal.

DP2 output to
HDMI connector

note --HDMI P&N can not swap

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

PV1 add for HW thermal protect

LVDS

HDMI

To AMD HDT

7/8 For Comal.

TEST35 PU FOR INTERNAL
TEST35 PD FOR CUSTOMER

DMAACTIVE_L controls
entry and exit from the
sleep and power states

SI

Thermal

THERMTRIP# shutdown temperature 125度C

4/19 For Comal,
close to APU.

PV1 change GPU thermal protect

PV1 add for HW thermal protect

ADD VGA TEMP_ FAIL function is active Hi

over 120 degree C= Low

When 100K-NTC 100 C=6.164K
Thermal Trip = 120 C

TRINITY-A8-SERIES_BGA813

PROJECT :	VOLKS_Comal 14"
Quanta Computer Inc.	
NB5	
Size	Document Number: Llano Display/Misc
Rev	1A
Date: Thursday, September 20, 2012	Sheet 4 of 42

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

EMI suggestion

+VCC_CORE

C361 470P/50V_4 | C333 *470P/50V_4 | C360 *470P/50V_4

U27E

+VCC_CORE

36A
Maximum IDDspike 50A

C338 22U/6.3VS_8 | C339 22U/6.3VS_8 | C348 22U/6.3VS_8 | C363 22U/6.3VS_8 | C317 22U/6.3VS_8 | C749 22U/6.3VS_8 | C347 22U/6.3VS_8 | C319 22U/6.3VS_8

C334 22U/6.3VS_8 | C335 22U/6.3VS_8 | C311 22U/6.3VS_8 | C288 *22U/6.3VS_8 | C318 *22U/6.3VS_8 | C735 *22U/6.3VS_8 | C325 *22U/6.3VS_8

C321 0.22U/10V_4 | C354 0.22U/10V_4 | C336 180P/50V_4 | C341 180P/50V_4 | C362 180P/50V_4 | C364 0.01U/25V_4 | C349 0.01U/25V_4 | C352 0.01U/25V_4

+VDDNB_CORE

C762 22U/6.3VS_8 | C788 22U/6.3VS_8 | C763 22U/6.3VS_8 | C764 22U/6.3VS_8

C294 0.22U/10V_4 | C295 0.22U/10V_4 | C293 180P/50V_4 | C291 180P/50V_4 | C292 180P/50V_4

+VDDNB_CAP

C300 22U/6.3VS_8 | C297 22U/6.3VS_8 | C298 22U/6.3VS_8 | C299 22U/6.3VS_8 | C289 180P/50V_4

+VDDP_CAP

C301 22U/6.3VS_8 | C302 *22U/6.3VS_8

+VDDNB_CORE

+VDDNB_CORE

25A
Maximum IDDNBspike 33A

DECOUPLING between PROCESSOR and DIMMs
Across VDDIO and VSS split

+1.5VSUS

C420 4.7U/6.3V_6 | C511 4.7U/6.3V_6 | C368 4.7U/6.3V_6 | C426 4.7U/6.3V_6 | C377 0.22U/10V_4 | C378 0.22U/10V_4 | C800 0.22U/10V_4 | C802 0.22U/10V_4

+VDDNB_CAP

VDDNB_CAP
VDDNB_CAP

If the VSS plane is cut to create a VDDIO plane,
ceramic capacitors are connected across
the VDDIO and VSS plane split as follows

+1.5VSUS

2.8A Up to DDR3-1333 @ 1.50V VDDIO

C455 0.22U/10V_4 | C425 0.22U/10V_4 | C458 0.22U/10V_4 | C438 0.22U/10V_4 | C479 0.22U/10V_4 | C365 0.22U/10V_4

C432 180P/50V_4 | C429 180P/50V_4 | C481 180P/50V_4 | C452 180P/50V_4 | C373 180P/50V_4

C366 22U/6.3VS_8 | C367 22U/6.3VS_8 | C414 4.7U/6.3V_6 | C421 4.7U/6.3V_6 | C415 4.7U/6.3V_6 | C369 4.7U/6.3V_6

+1.2V_VDDP

VDDP = 5A

+1.2V | R427 *0_8/S | +1.2V_VDDP

C770 22U/6.3VS_8 | C772 0.22U/10V_4 | C771 0.22U/10V_4 | C769 22U/6.3VS_8

C774 180P/50V_4 | C773 180P/50V_4 | C768 *22U/6.3VS_8

+VDDP_CAP

TP43

VDDR = 3.3A (Up to DDR3-1333 @ 1.5V)

+1.2V

+1.2V_VDDR_B

R429 *0_8/S

C780 0.22U/10V_4 | C778 0.22U/10V_4 | C777 1000P/50V_4 | C779 180P/50V_4 | C776 180P/50V_4

TRINITY-A8-SERIES_BGA813

VDDA= 0.75A

+2.5V | L21 PBY160808T-221Y-N(220,2A) | +2.5V_VDDA

C353 4.7U/6.3V_6 | C350 0.22U/10V_4 | C351 3300P/50V_4

U27F

TRINITY-A8-SERIES_BGA813

PROJECT :	VOLKS_Comal 14"
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Llano POWER/GND
Rev: 1A	
Date: Thursday, September 20, 2012	Sheet 5 of 42

+3VS5 NC,no install by default
R146 *2.2K_4 FCH_TEST0
R153 *2.2K_4 FCH_TEST1
R151 *2.2K_4 FCH_TEST2

+3V
R176 2.2K_4 SMB_RUN_CLK
R177 2.2K_4 SMB_RUN_DAT
to DDR3 SMBUS
+3VS5
R148 *1K/F_4 SYS_RST#
SYS_RST# internal 10K pull up

+3VS5
R134 10K/F_4 SCL3
R135 10K/F_4 SDA3
R130 10K/F_4 SCL2
R133 10K/F_4 SDA2
R142 2.2K_4 SCL1
R141 2.2K_4 SDA1
R143 *4.7K_4 FCH_THERMTRIP#
C273 *0.01U/25V_4
R375 10K/F_4 DNBSWON#

GEVENT0# internal pull Hi 8.2K to +3V
GEVENT1# internal pull Hi 8.2K to +3V
GEVENT23# internal pull Hi 8.2K to +3V
GEVENT5# internal pull Hi 8.2K to +3VS5
PCIE_WAKE# no need to pull
Hi resistor from check list
CLK_REQ2# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V
CLK_REQ4# internal pull Hi 8.2K to +3V
This pin is used to power down VGA DAC regulators when CRT no connected
GEVENT16# internal pull Hi 8.2K to +3VS5
GEVENT15# internal pull Hi 8.2K to +3VS5

4/19 For Comal.
For Zero ODD

HD audio interface is +3V_S5 voltage

To Azalia

ACZ_SDOUT_R R411 33_4 ACZ_SDOUT_AUDIO [23]
ACZ_SYNC_R R412 33_4 ACZ_SYNC_AUDIO [23]
ACZ_BCLK_R R414 33_4 BIT_CLK_AUDIO [23]
ACZ_RST#_R R425 33_4 ACZ_RST#_AUDIO [23]
ACZ_SDIN0 ACZ_SDIN0 [23]
C275 *33P/50V_4
C280 33P/50V_4

Pure UMA can remove
CLK_REQ# already internal pull up 8.2K
[37] VGA_REQ 1 D21 2 CLKREQ1# *RB501V-40
R440 10K/F_4
[36,37,38] DGPU_PWROK 2 Q20 *MMBT3904-7-F 3 1

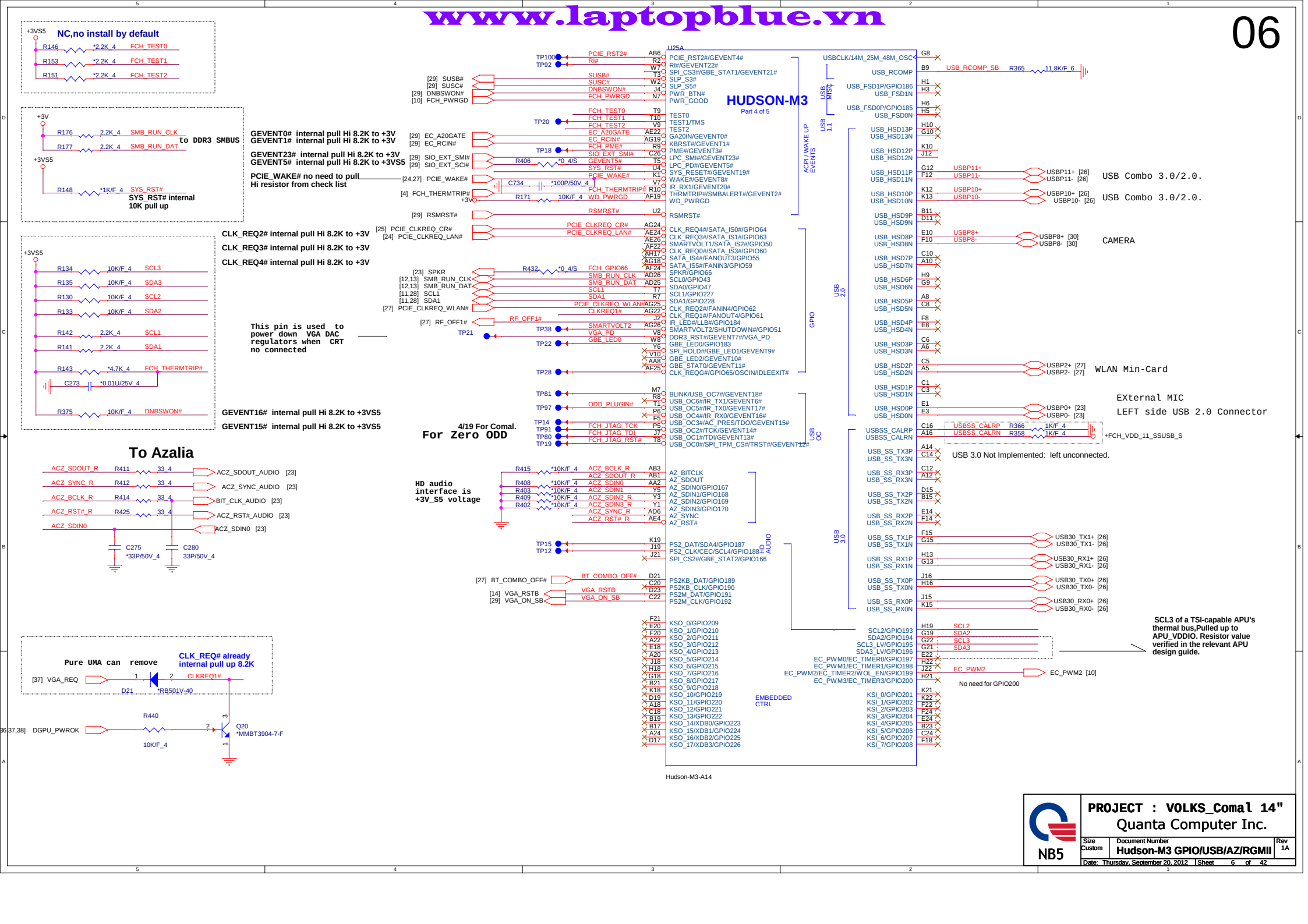
HUDSON-M3

Part 4 of 5

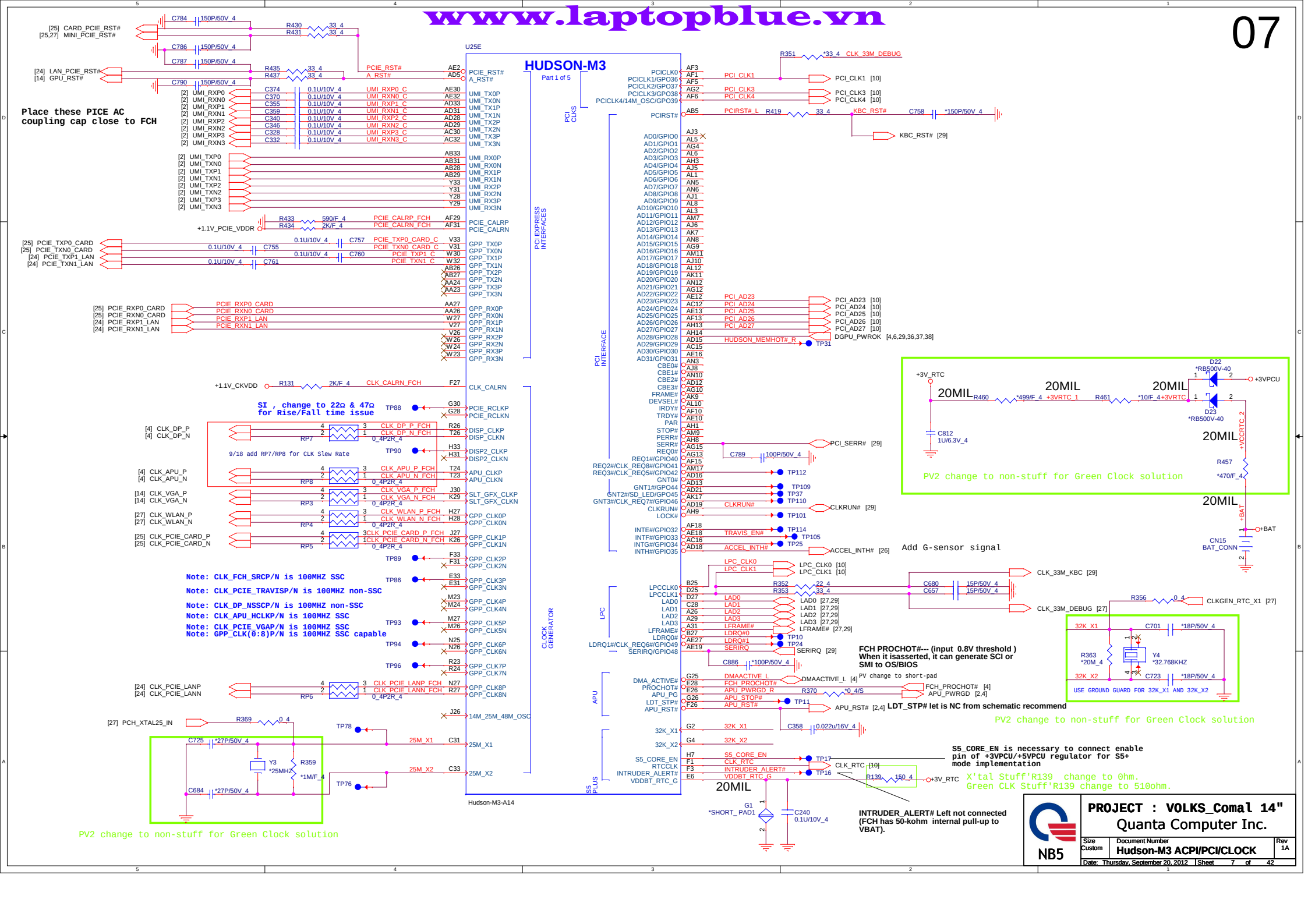
PCIE_RST2#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/XDB0/GPIO223
KSO_15/XDB1/GPIO224
KSO_16/XDB2/GPIO225
KSO_17/XDB3/GPIO226
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USBSS_CALRP
USBSS_CALRN
USB_SS_TX3P
USB_SS_TX3N
USB_SS_RX3P
USB_SS_RX3N
USB_SS_TX2P
USB_SS_TX2N
USB_SS_RX2P
USB_SS_RX2N
USB_SS_TX1P
USB_SS_TX1N
USB_SS_RX1P
USB_SS_RX1N
USB_SS_TX0P
USB_SS_TX0N
USB_SS_RX0P
USB_SS_RX0N
SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208

USB Combo 3.0/2.0.
USB Combo 3.0/2.0.
CAMERA
WLAN Min-Card
EXternal MIC
LEFT side USB 2.0 Connector
USB 3.0 Not Implemented: left unconnected.
No need for GPIO200
SCL3 of a TSI-capable APU's thermal bus,Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.

Hudson-M3-A14



NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size Custom	Document Number Hudson-M3 GPIO/USB/AZ/RGMII	Rev 1A
Date: Thursday, September 20, 2012	Sheet 6 of 42	



NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.		
	Size: Custom	Document Number: Hudson-M3 ACPI/PCI/CLOCK	Rev: 1A
	Date: Thursday, September 20, 2012	Sheet 7 of 42	

U25D

HUDSON-M3

Part 5 of 5

GROUND

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64

VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73 VSS_74 VSS_75 VSS_76 VSS_77 VSS_78 VSS_79 VSS_80 VSS_81 VSS_82 VSS_83 VSS_84 VSS_85 VSS_86 VSS_87 VSS_88 VSS_89 VSS_90 VSS_91 VSS_92 VSS_93 VSS_94 VSS_95 VSS_96 VSS_97 VSS_98 VSS_99 VSS_100 VSS_101 VSS_102 VSS_103 VSS_104 VSS_105 VSS_106 VSS_107 VSS_108 VSS_109 VSS_110 VSS_111 VSS_112 VSS_113 VSS_114 VSS_115 VSS_116 VSS_117 VSS_118 VSS_119 VSS_120 VSS_121 VSS_122 VSS_123 VSS_124 VSS_125 VSS_126 VSS_127 VSS_128

A3 A33 B7 B13 D9 D13 E5 E12 E16 E29 F7 F9 F11 F13 F16 F17 F19 F23 F25 F29 G6 G16 G32 H12 H15 H29 J6 J9 J10 J13 J28 J32 K7 K16 K27 K28 L6 L12 L13 L15 L16 L21 M13 M16 M21 M25 N6 N11 N13 N23 N24 P12 P18 P20 P21 P31 P33 R4 R11 R25 R28 T11 T16 T18

T25 T27 U6 U14 U17 U20 U21 U30 U32 V11 V16 V18 W4 W6 W25 W28 Y14 Y16 Y18 AA6 AA12 AA13 AA14 AA16 AA17 AA25 AA28 AA30 AA32 AB25 AC6 AC18 AC28 AD27 AE6 AE15 AE21 AE28 AF8 AF12 AF16 AF33 AG30 AG32 AH5 AH11 AH18 AH19 AH21 AH23 AH25 AH27 AJ18 AJ28 AJ29 AK21 AK25 AL18 AM21 AM25 AN1 AN18 AN28 AN33

N8 VSSAN_HWM

K25 VSSXL

H25 VSSPL_SYS

T21 VSSPL_DAC
L28 VSSAN_DAC
K33 VSSANQ_DAC
N28 VSSIO_DAC

R6 EFUSE

Hudson-M3-A14

PLACE SATA AC COUPLING
CAPS CLOSE TO HUDSON-M2/M3

SATA HDD

MINISATA

[28] SATA_TXP0 SATA_TXP0 AK19 SATA_TX0P
[28] SATA_TXN0 SATA_TXN0 AM19 SATA_TX0N
[28] SATA_RXN0 AL20 SATA_RX0N
[28] SATA_RXP0 AN20 SATA_RX0P
[28] SATA_TXP1 SATA_TXP1 AN22 SATA_TX1P
[28] SATA_TXN1 SATA_TXN1 AL22 SATA_TX1N
[28] SATA_RXN1 AH20 SATA_RX1N
[28] SATA_RXP1 AJ20 SATA_RX1P
AJ22 SATA_TX2P
AH22 SATA_TX2N
AM23 SATA_RX2N
AK23 SATA_RX2P
AH24 SATA_TX3P
AJ24 SATA_TX3N
AN24 SATA_RX3N
AL24 SATA_RX3P
AL26 SATA_TX4P
AN26 SATA_TX4N
AJ26 SATA_RX4N
AH26 SATA_RX4P
AN29 SATA_TX5P
AL28 SATA_TX5N
AK27 SATA_RX5N
AM27 SATA_RX5P

[28] SATA_LED# R170 *0_4/S SB_SATA_LED#

PV , change
to short pad

PLACE SATA_CAL RES VERY
CLOSE TO BALL OF
HUDSON-M2/M3

+1.1V_AVDD_SATA R163 1K/F_4 SATA_CALRP AF28 SATA_CALRP
R159 931/F_4 SATA_CALRN AF27 SATA_CALRN

4/19 For Comal.

+3V R178 *220/F_6 SB_SATA_LED# AD22 SATA_ACT#/GPIO67

AF21 SATA_X1

Integrated Clock Mode:
Leave unconnected.

AG21 SATA_X2

GPIO52 internal pull Hi 8.2K to +3V
GPIO53 internal pull Hi 8.2K to +3V
GPIO54 internal pull Hi 8.2K to +3V
GPIO56 internal pull Hi 8.2K to +3V
GPIO57 internal pull Hi 8.2K to +3V
GPIO58 internal pull Hi 8.2K to +3V

[27] RF_OFF# RF_OFF# AH16 FANOUT0/GPIO52
TP99 BT_OFF# AM15 FANOUT1/GPIO53
TP39 BT_COMBO_EN# AJ16 FANOUT2/GPIO54

[28] ACC_LED# AK15 FANIN0/GPIO56
AN16 FANIN1/GPIO57
AL16 FANIN2/GPIO58

[30] LCD_BK LCD_BK

TEMPIN0 K6 TEMPIN0/GPIO171
TEMPIN1 K5 TEMPIN1/GPIO172
TEMPIN2 K3 TEMPIN2/GPIO173
TEMPIN3 M6 TEMPIN3/TALERT#/GPIO174

R136 10K/F_4 R137 10K/F_4 R378 10K/F_4 R138 10K/F_4

TEMP(0 - 3)
Temp Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

U25D

HUDSON-M3

Part 2 of 5

SERIAL ATA

SD CARD

SD_CLK/SCLK_2/GPIO73 AL14
SD_CMD/SLOAD_2/GPIO74 AN14
SD_CD#/GPIO75 AJ12
SD_WP/GPIO76 AH12
SD_DATA0/SDATI_2/GPIO77 AK13
SD_DATA1/SDATO_2/GPIO78 AM13
SD_DATA2/GPIO79 AH15
SD_DATA3/GPIO80 AJ14

GBE LAN

GBE_COL AC4
GBE_CRS AD3
GBE_MDCK AD9
GBE_MDIO W10
GBE_RXCLK AB8
GBE_RXD3 AH7
GBE_RXD2 AF7
GBE_RXD1 AE7
GBE_RXD0 AD7
GBE_RXCTL/RXDV AG8
GBE_RXERR AD1
GBE_TXCLK AB7
GBE_TXD3 AF9
GBE_TXD2 AG6
GBE_TXD1 AE8
GBE_TXD0 AD8
GBE_TXCTL/TXEN AB9
GBE_PHY_PD AC2
GBE_PHY_RST# AA7
GBE_PHY_INTR W9 GBE_PHY_INTR R147 10K/F_4 +3VS5

+3VS5
R444 10K/F_4
SPI_CS0# *0_4/S R445 EC_BIOS_CS# [29]
SPI_CLK *0_4/S R443 EC_BIOS_SPI_CLK_I [29]
SPI_SO *0_4/S R442 EC_BIOS_WR# [29]
SPI_SI *0_4/S R446 EC_BIOS_RD# [29]

SPI ROM

SPI_DI/GPIO164 V6 SPI_SI TP104
SPI_DO/GPIO163 V5 SPI_SO TP103
SPI_CLK/GPIO162 V3 SPI_CLK TP107
SPI_CS1#/GPIO165 T6 SPI_CS0# TP108
ROM_RST#/SPI_WP#/GPIO161 V1 FCH_SPI_WP TP98

VGA DAC

VGA_RED L30
VGA_GREEN L32
VGA_BLUE M29
VGA_HSYNC/GPO68 M28
VGA_VSYNC/GPO69 N30
VGA_DDC_SDA/GPO70 M33
VGA_DDC_SCL/GPO71 N32
VGA_DAC_RSET K31 TP87

VGA MAINLINK

AUX_VGA_CH_P V28
AUX_VGA_CH_N V29
AUXCAL U28 TP95
ML_VGA_L0P T31
ML_VGA_L0N T33
ML_VGA_L1P T29
ML_VGA_L1N T28
ML_VGA_L2P R32
ML_VGA_L2N R30
ML_VGA_L3P P29
ML_VGA_L3N P28
ML_VGA_HPD/GPO229 C29 TP13

HW MONITOR

VIN0/GPIO175 N2 SIDE_PORT_ID0
VIN1/GPIO176 M3 SIDE_PORT_ID1
VIN2/SDATI_1/GPIO177 L2 SIDE_PORT_ID2
VIN3/SDATO_1/GPIO178 N4 BOARD_ID0
VIN4/SLOAD_1/GPIO179 P1 BOARD_ID1
VIN5/SCLK_1/GPIO180 P3 BOARD_ID2
VIN6/GBE_STAT3/GPIO181 M1 BOARD_ID3
VIN7/GBE_LED3/GPIO182 M5 BOARD_ID4

NC1 AG16
NC2 AH10
NC3 A28
NC4 G27
NC5 L4

VIN (0 - 7)
Voltage Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

Hudson-M3-A14

+3VS5
R395 *10K/F_4 BOARD_ID0 R396 10K/F_4
R398 *10K/F_4 BOARD_ID1 R399 10K/F_4
R400 *10K/F_4 BOARD_ID2 R401 10K/F_4
R386 *10K/F_4 BOARD_ID3 R387 10K/F_4
R390 *10K/F_4 BOARD_ID4 R391 10K/F_4
R392 10K/F_4 SIDE_PORT_ID0 R393 *10K/F_4
R384 10K/F_4 SIDE_PORT_ID1 R385 *10K/F_4
R379 *10K/F_4 SIDE_PORT_ID2 R380 10K/F_4

Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 SATA/HWM/SPI	1A

Date: Thursday, September 20, 2012 Sheet 8 of 42

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

HUDSON-M3

U25C — Part 3 of 5

VDDQ--3.3V I/O power — 102mA

+3.3V_VDDIO → R166 *0_8/S (PV1 Change to short pad) → +3V

C308 0.1U/10V_4, C314 22U/6.3VS_8, C316 0.1U/10V_4, C310 0.1U/10V_4, C309 0.1U/10V_4

AB17 VDDIO_33_PCIGP_1
AB18 VDDIO_33_PCIGP_2
AE9 VDDIO_33_PCIGP_3
AD10 VDDIO_33_PCIGP_4
AG7 VDDIO_33_PCIGP_5
AC13 VDDIO_33_PCIGP_6
AB12 VDDIO_33_PCIGP_7
AB13 VDDIO_33_PCIGP_8
AB14 VDDIO_33_PCIGP_9
AB16 VDDIO_33_PCIGP_10

PCI/GPIO I/O

VDDCR-- S/B CORE power — 1007mA for M3, 902mA for M2

T14 VDDCR_11_1
T17 VDDCR_11_2
T20 VDDCR_11_3
U16 VDDCR_11_4
U18 VDDCR_11_5
V14 VDDCR_11_6
V17 VDDCR_11_7
V20 VDDCR_11_8
Y17 VDDCR_11_9

CORE S0

TRACE WIDTH >=100mil → +1.1V

C284 0.1U/10V_4, C271 0.1U/10V_4, C286 1U/6.3V_4, C278 1U/6.3V_4, C272 10U/6.3V_6

VDDPDL_3.3V — 47mA

+3V → L22 PBY160808T-221Y-N(220,2A) → TRACE WIDTH >=15mil

C344 2.2U/6.3V_4, C356 *0.1U/10V_4

H24 VDDPL_33_SYS
V22 VDDPL_33_DAC
U22 VDDPL_33_ML
T22 VDDAN_33_DAC
L18 VDDPL_33_SSUSB_S
D7 VDDPL_33_USB_S
AH29 VDDPL_33_PCIE
AG28 VDDPL_33_SATA

+FCH_VDDPL_33_SSUSB_S → 11mA
+FCH_VDDPL_33_PCIE → 11mA
+FCH_VDDPL_33_SATA → 12mA

*0_4/S R145 (PV1 Change to short pad)

VDDAN_CLK-- Internal clock Generator I/O power — 340mA

H26 VDDAN_11_CLK_1
J25 VDDAN_11_CLK_2
K24 VDDAN_11_CLK_3
L22 VDDAN_11_CLK_4
M22 VDDAN_11_CLK_5
N21 VDDAN_11_CLK_6
N22 VDDAN_11_CLK_7
P22 VDDAN_11_CLK_8

CLKGEN I/O

+1.1V_CKVDD

TRACE WIDTH >=30mil → +1.1V

C260 1U/6.3V_4, C269 1U/6.3V_4, C249 0.1U/10V_4, C254 0.1U/10V_4, C241 22U/6.3VS_8

L16 BLM18PG181SN1D(180,1.5A)_6

L23 PBY160808T-221Y-N(220,2A) → TRACE WIDTH >=15mil

C357 2.2U/6.3V_4, C345 *0.1U/10V_4

VDDAN_11_ML -- UMI 1.1V analog power

+LDO_CAP M31 → C753 *2.2U/6.3V_4

LDO_CAP
V21 VDDPL_11_DAC
Y22 VDDAN_11_ML_1
V23 VDDAN_11_ML_2
V24 VDDAN_11_ML_3
V25 VDDAN_11_ML_4

MAIN LINK EXPRESS

*0_4/S R152 (PV1 Change to short pad)

VDDAN_11_PCIE --PCIE/UMI analog power — 1088mA

+1.1V_PCIE_VDDR

AB24 VDDAN_11_PCIE_1
Y21 VDDAN_11_PCIE_2
AE25 VDDAN_11_PCIE_3
AD24 VDDAN_11_PCIE_4
AB23 VDDAN_11_PCIE_5
AA22 VDDAN_11_PCIE_6
AF26 VDDAN_11_PCIE_7
AG27 VDDAN_11_PCIE_8

TRACE WIDTH >=100mil → L19 BLM18PG181SN1D(180,1.5A)_6 → +1.1V

C303 0.1U/10V_4, C296 0.1U/10V_4, C331 1U/6.3V_4, C307 1U/6.3V_4, C281 22U/6.3VS_8

VDDPL_11_SYS_S : System Clock Gen PLLs analog power

+1.1VS5 → L18 PBY160808T-221Y-N(220,2A) → +VDDPL_1.1V

C257 2.2U/6.3V_4, C247 0.1U/10V_4

VDDPL_33_USB_S : USB PHY PLL analog power

+3V → L13 PBY160808T-221Y-N(220,2A) → +VDDPL_3.3V

C228 2.2U/6.3V_4, C239 0.1U/10V_4

+3V_AVDD_USB → L47 PBY160808T-221Y-N(220,2A) → +FCH_VDDPL_33_SUSB_S

C722 2.2U/6.3V_4, C728 1U/6.3V_4

AB10 VDDIO_33_GBE_S
AB11 VDDCR_11_GBE_S_1
AA11 VDDCR_11_GBE_S_2
AA9 VDDIO_GBE_S_1
AA10 VDDIO_GBE_S_2

GBE LAN SERIAL ATA

VDDAN_11_SATA--SATA PHY analog/IO power — 1337mA

+1.1V_AVDD_SATA

AA21 VDDAN_11_SATA_1
Y20 VDDAN_11_SATA_4
AB21 VDDAN_11_SATA_2
AB22 VDDAN_11_SATA_3
AC22 VDDAN_11_SATA_5
AC21 VDDAN_11_SATA_6
AA20 VDDAN_11_SATA_7
AA18 VDDAN_11_SATA_8
AB20 VDDAN_11_SATA_9
AC19 VDDAN_11_SATA_10

TRACE WIDTH >=50mil → L20 BLM18PG181SN1D(180,1.5A)_6 → +1.1V

C312 1U/6.3V_4, C304 1U/6.3V_4, C323 0.1U/10V_4, C324 0.1U/10V_4, C322 22U/6.3VS_8

if support USB 3.0 wake up should be change pull hi to S5 power

VDDAN_33_USB_S : USB PHY I/O analog power — 470mA

+3V_AVDD_USB → L44 PBY160808T-221Y-N(220,2A) → +3VS5

TRACE WIDTH >=50mil

C253 0.1U/10V_4, C243 10U/6.3V_6, C711 10U/6.3V_6, C255 1U/6.3V_4, C262 1U/6.3V_4

G7 VDDAN_33_USB_S_1
H8 VDDAN_33_USB_S_2
J8 VDDAN_33_USB_S_3
K8 VDDAN_33_USB_S_4
K9 VDDAN_33_USB_S_5
M9 VDDAN_33_USB_S_6
M10 VDDAN_33_USB_S_7
N9 VDDAN_33_USB_S_8
N10 VDDAN_33_USB_S_9
M12 VDDAN_33_USB_S_10
N12 VDDAN_33_USB_S_11
M11 VDDAN_33_USB_S_12

USB

VDDIO_33_S-- 3.3v S5 I/O power — 59mA

N18 VDDIO_33_S_1
L19 VDDIO_33_S_2
M18 VDDIO_33_S_3
V12 VDDIO_33_S_4
V13 VDDIO_33_S_5
Y12 VDDIO_33_S_6
Y13 VDDIO_33_S_7
W11 VDDIO_33_S_8

3.3V_S5 I/O

TRACE WIDTH >=20mil → +3VS5

C306 *0.1U/10V_4, C244 2.2U/6.3V_4, C258 1U/6.3V_4, C287 1U/6.3V_4, C250 1U/6.3V_4, C285 1U/6.3V_4

if support USB 3.0 wake up should be change pull hi to S5 power

VDDAN_11_USB_S : USB PHY PLL analog power — 140mA

+1.1VS5 → L46 PBY160808T-221Y-N(220,2A) → +FCH_VDDAN_11_USB_S

C277 0.1U/10V_4, C721 2.2U/6.3V_4, C276 0.1U/10V_4

TRACE WIDTH >=20mil

U12 VDDAN_11_USB_S_1
U13 VDDAN_11_USB_S_2

VDDXL_33_S-- 25MHZ XTAL IO power — 5mA

G24 VDDXL_33_S

+VDDXL_3.3V

VDDCR_1.1_S-- 1.1V S5 Core power — 187mA

N20 VDDCR_11_S_1
M20 VDDCR_11_S_2

+VDDCR_1.1V → TRACE WIDTH >=15mil → +1.1VS5

C231 *0.1U/10V_4, C236 2.2U/6.3V_4

L14 PBY160808T-221Y-N(220,2A) → +3VS5

VDDCR_11_USB_S : USB PHY core power — 42mA

+1.1VS5 → L45 PBY160808T-221Y-N(220,2A) → +FCH_VDDCR_11_USB_S

TRACE WIDTH >=15mil

C268 0.1U/10V_4, C270 0.1U/10V_4, C727 10U/6.3V_6

T12 VDDCR_11_USB_S_1
T13 VDDCR_11_USB_S_2

M3 chipset need to stuff for support USB3.0

SI , AMD SR tool review

VDDPL_11_SYS_S -- 70mA

J24 VDDPL_11_SYS_S

+VDDPL_1.1V

C259 1U/6.3V_4, C265 2.2U/6.3V_4

VDDAN_33_HWM_S -- 12mA

M8 VDDAN_33_HWM_S

+3VS5

C261 0.1U/10V_4, C232 2.2U/6.3V_4

VDDIO_AZ_S -- 26mA

AA4 VDDIO_AZ_S

Trace width >=20 mil → +3V

C330 2.2U/6.3V_4

VDDAN_11_SSUSB_S : USB3.0 PHY PLL analog power — 282mA

+1.1VS5 → L10 PBY160808T-221Y-N(220,2A) → +FCH_VDD_11_SSUSB_S

+FCH_VDDAN_11_SSUSB_S_R

P16 VDDAN_11_SSUSB_S_1
M14 VDDAN_11_SSUSB_S_2
N14 VDDAN_11_SSUSB_S_3
P13 VDDAN_11_SSUSB_S_4
P14 VDDAN_11_SSUSB_S_5

VDDCR_11_SSUSB_S : USB3.0 PHY core power — 424mA

+FCH_VDDCR_11_SSUSB_S

N16 VDDCR_11_SSUSB_S_1
N17 VDDCR_11_SSUSB_S_2
P17 VDDCR_11_SSUSB_S_3
M17 VDDCR_11_SSUSB_S_4

USB SS

C219 1U/6.3V_4, C226 0.1U/10V_4, C221 0.1U/10V_4, C218 1U/6.3V_4, C242 10U/6.3V_6, C252 1U/6.3V_4, C266 0.1U/10V_4, C264 0.1U/10V_4

POWER

Hudson-M3-A14

M3 chipset need to stuff for support USB3.0

if support Modem wake up should be change pull hi to S5 power

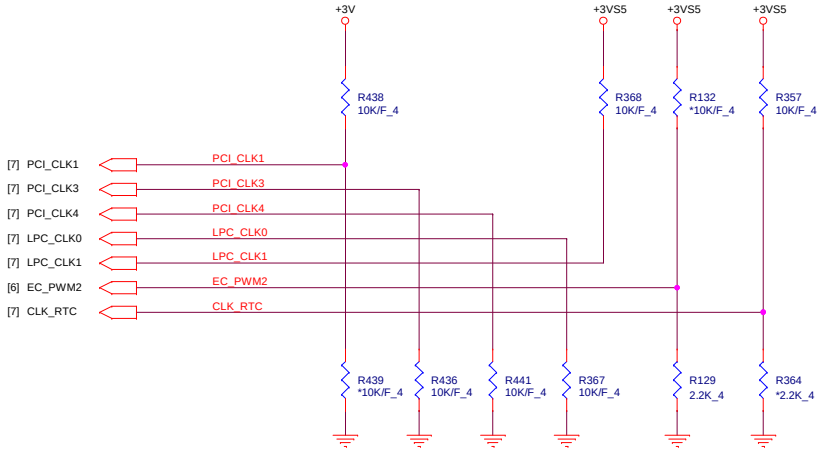
+3VS5 → L17 PBY160808T-221Y-N(220,2A) → +FCH_VDDPL_33_SSUSB_S

C246 2.2U/6.3V_6, C248 0.1U/10V_4

PROJECT :	VOLKS_Comal 14"
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Hudson-M3 POWER/GND
Rev: 1A	
Date: Thursday, September 20, 2012	Sheet 9 of 42

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

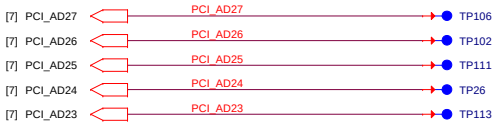


REQUIRED STRAPS

	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

DEBUG STRAPS

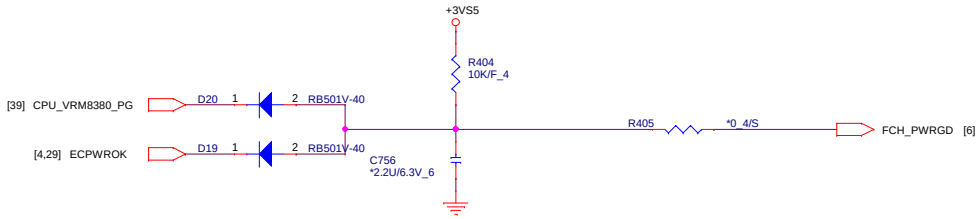
FCH has 15K Internal Pull Up for PCI_AD[27:23]



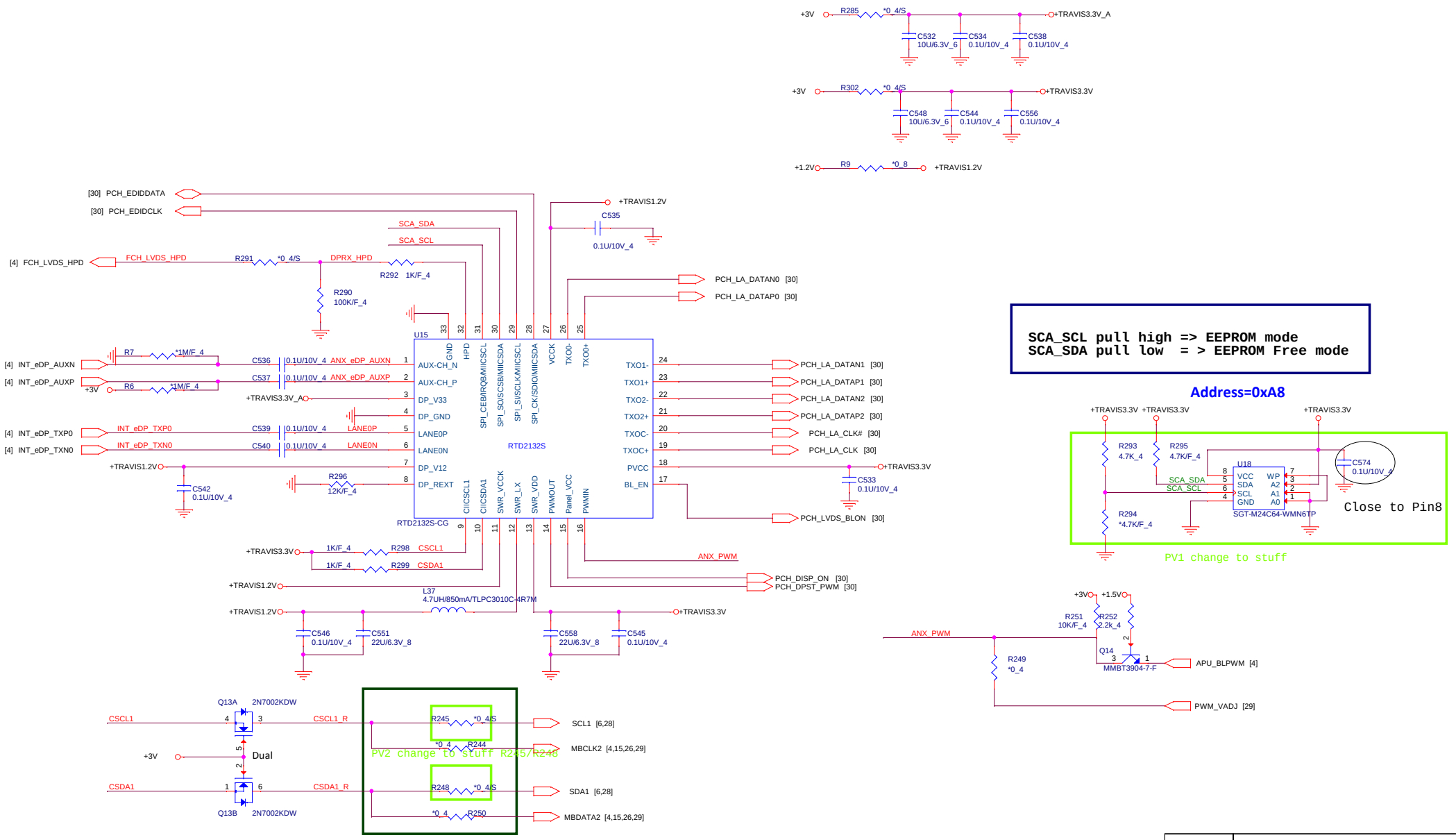
remove reserve pull low resistor
reserve test point only.

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD

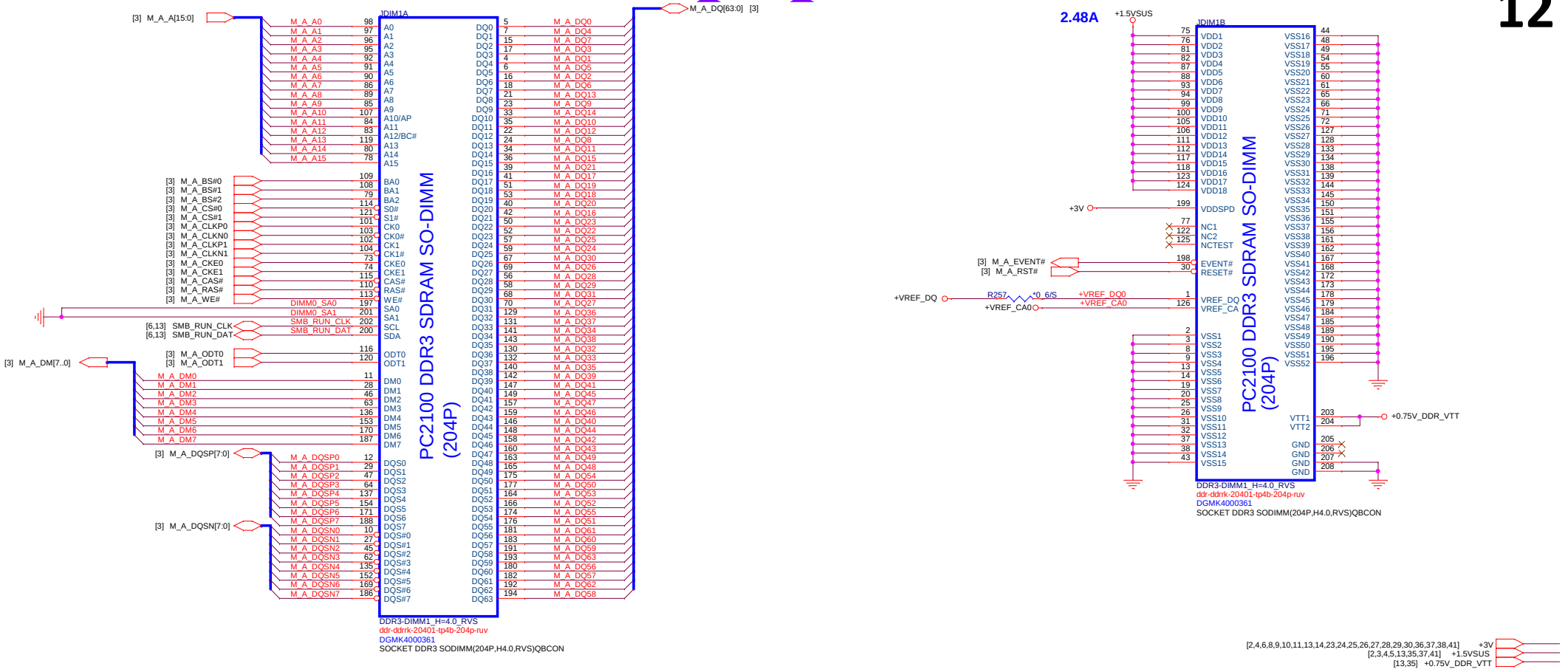


NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.		
	Size: Custom	Document Number: Hudson-M3 STRAP/PWRGD	Rev: 1A
	Date: Thursday, September 20, 2012	Sheet 10 of 42	

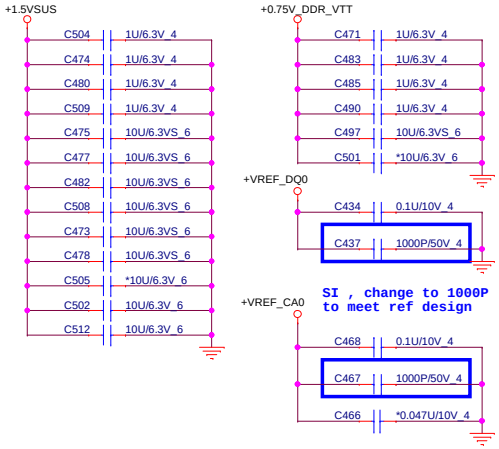


EE PROM R3054,R3056
EC OPTION R3055,R3057

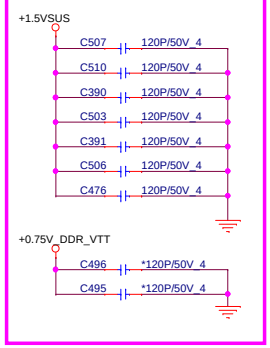
NB5	**PROJECT : VOLKS_Comal 14"** Quanta Computer Inc.	
Size Custom	Document Number **RTD2132S**	Rev 1A
Date: Thursday, September 20, 2012	Sheet 11 of 42	



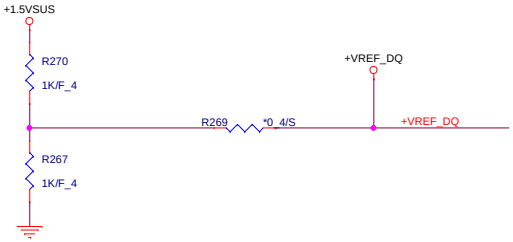
Place these Caps near So-Dimm0.



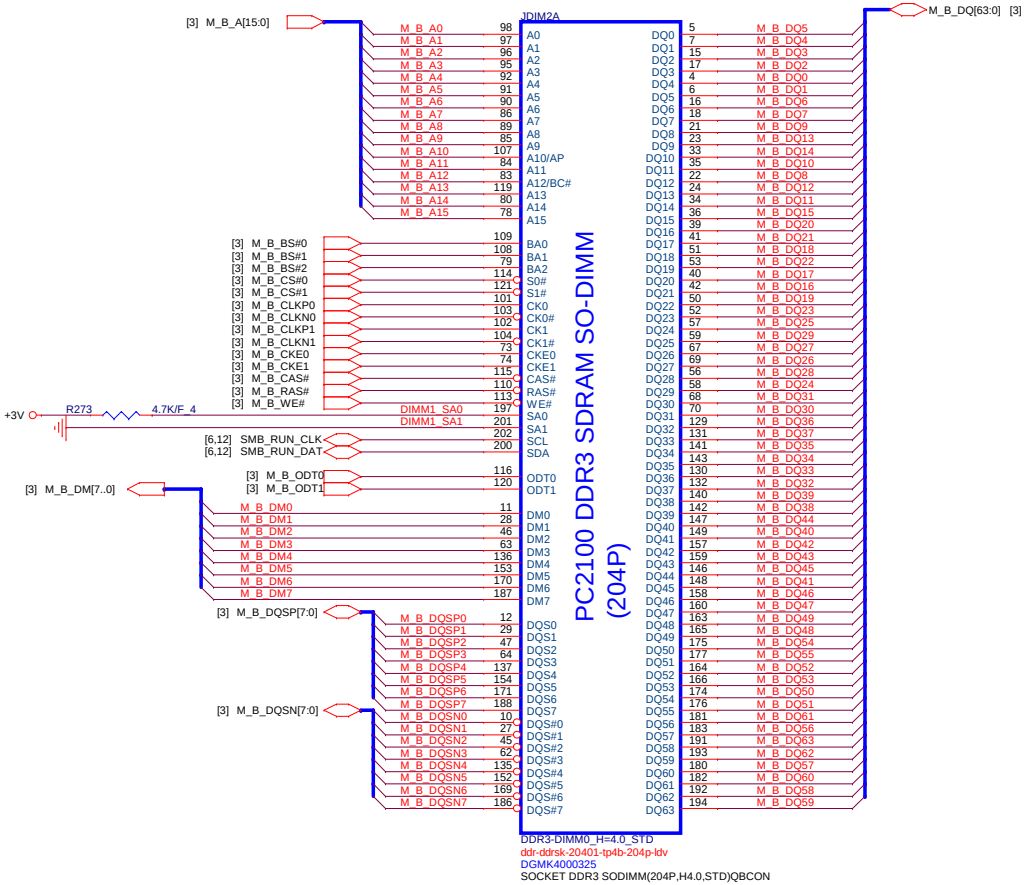
For EMI RESERVE

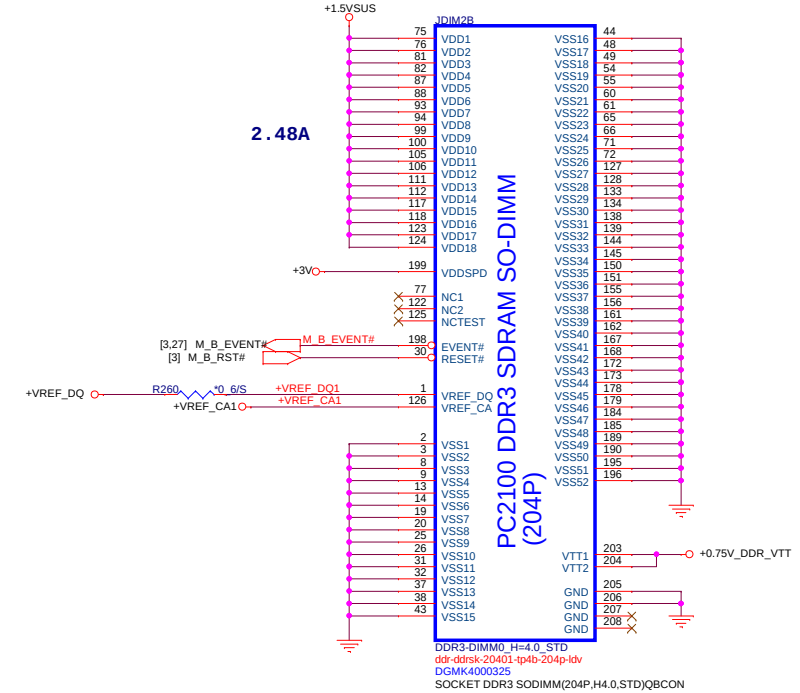


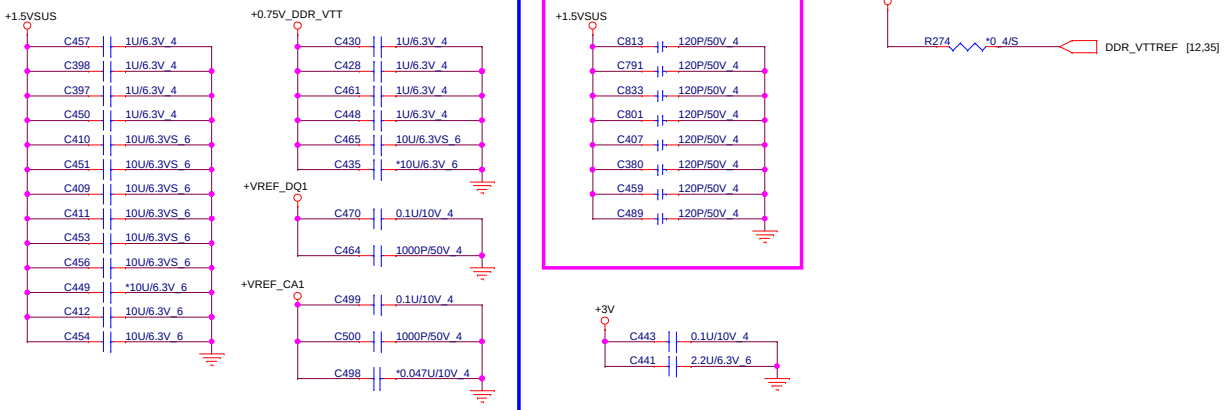
Reserved for AMD suggest



NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size: Custom	Document Number: System Memory 1/2 (5.2H)	Rev: 1A
Date: Thursday, September 20, 2012	Sheet: 12of	42







NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size: Custom	Document Number: System Memory 2/2 (9.2H)	Rev: 1A
Date: Thursday, September 20, 2012	Sheet 13of 42	

FOR Mars support Gne3: AC cap nees use 0.22u
FOR Thems: AC cap need use 0.1u for Gen2

U21A

PART 1 OF 9

[2] PEG_TXP0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	C_PEG_RXP0	C202	*0.22U/10V_4
[2] PEG_TXN0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	C_PEG_RXN0	C203	*0.22U/10V_4
[2] PEG_TXP1	Y35	PCIE_RX1P	PCIE_TX1P	W33	C_PEG_RXP1	C190	*0.22U/10V_4
[2] PEG_TXN1	W36	PCIE_RX1N	PCIE_TX1N	W32	C_PEG_RXN1	C191	*0.22U/10V_4
[2] PEG_TXP2	W38	PCIE_RX2P	PCIE_TX2P	U33	C_PEG_RXP2	C200	*0.22U/10V_4
[2] PEG_TXN2	V37	PCIE_RX2N	PCIE_TX2N	U32	C_PEG_RXN2	C201	*0.22U/10V_4
[2] PEG_TXP3	V35	PCIE_RX3P	PCIE_TX3P	U30	C_PEG_RXP3	C187	*0.22U/10V_4
[2] PEG_TXN3	U36	PCIE_RX3N	PCIE_TX3N	U29	C_PEG_RXN3	C186	*0.22U/10V_4
[2] PEG_TXP4	U38	PCIE_RX4P	PCIE_TX4P	T33	C_PEG_RXP4	C204	*0.22U/10V_4
[2] PEG_TXN4	T37	PCIE_RX4N	PCIE_TX4N	T32	C_PEG_RXN4	C197	*0.22U/10V_4
[2] PEG_TXP5	T35	PCIE_RX5P	PCIE_TX5P	T30	C_PEG_RXP5	C188	*0.22U/10V_4
[2] PEG_TXN5	R36	PCIE_RX5N	PCIE_TX5N	T29	C_PEG_RXN5	C189	*0.22U/10V_4
[2] PEG_TXP6	R38	PCIE_RX6P	PCIE_TX6P	P33	C_PEG_RXP6	C199	*0.22U/10V_4
[2] PEG_TXN6	P37	PCIE_RX6N	PCIE_TX6N	P32	C_PEG_RXN6	C198	*0.22U/10V_4
[2] PEG_TXP7	P35	PCIE_RX7P	PCIE_TX7P	P30	C_PEG_RXP7	C195	*0.22U/10V_4
[2] PEG_TXN7	N36	PCIE_RX7N	PCIE_TX7N	P29	C_PEG_RXN7	C194	*0.22U/10V_4

	N38	PCIE_RX8P	PCIE_TX8P	N33			
	M37	PCIE_RX8N	PCIE_TX8N	N32			
	M35	PCIE_RX9P	PCIE_TX9P	N30			
	L36	PCIE_RX9N	PCIE_TX9N	N29			
	L38	PCIE_RX10P	PCIE_TX10P	L33			
	K37	PCIE_RX10N	PCIE_TX10N	L32			
	K35	PCIE_RX11P	PCIE_TX11P	L30			
	J36	PCIE_RX11N	PCIE_TX11N	L29			
	J38	PCIE_RX12P	PCIE_TX12P	K33			
	H37	PCIE_RX12N	PCIE_TX12N	K32			
	H35	PCIE_RX13P	PCIE_TX13P	J33			
	G36	PCIE_RX13N	PCIE_TX13N	J32			
	G38	PCIE_RX14P	PCIE_TX14P	K30			
	F37	PCIE_RX14N	PCIE_TX14N	K29			
	F35	PCIE_RX15P	PCIE_TX15P	H33			
	E37	PCIE_RX15N	PCIE_TX15N	H32			

PCI EXPRESS INTERFACE

For Mars NC pin :
N38,M37,M35,L36,L38,K37,K35,J36,J38
H37,H35,G36,G38,F37,F35,E37

FOR Mars NC pin :
N33,N32,N30,N29,L33,L32,L30,L29,K33,K32
J33,J32,K30,K29,H33,H32

CLOCK

[7] CLK_VGA_P	CLK_VGA_P	AB35	PCIE_REFCLKP
[7] CLK_VGA_N	CLK_VGA_N	AA36	PCIE_REFCLKN

Install for Mars/ Chelsea

R69 Ra *1K/F_4

	AH16	TEST_PG
PEGX_RST#	AA30	PERSTB

CALIBRATION

PCIE_CALR_TX	Y30	PCIE_CALRP
PCIE_CALR_RX	Y29	PCIE_CALRN

*MARS_M2_PRO

Mars/ Chelsea Only : Stuff Ra
Do not install For Thames

R373 Ra *1.69K/F_4 +1.0V_VGA

Install for Thames ONLY: Stuff Rb
Do not install for Chelsea

R371 Rb *1.27K/F_4

R372 Rc *1K/F_4 +1.0V_VGA

Install 2k for Thames
Install 1k for Mars

	Chelsea/MARS	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K

+3V

C748 *0.1U/10V_4

*TC7SH08FU U24

[7] GPU_RST#

[6] VGA_RSTB

R383 *330_4 DGPU_HIN_RST#

PEGX_RST#

R374 *100K_4

[16,18,19,37] +1.0V_VGA +1.0V_VGA

NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Mars_PCIE_Interface	1A

Date: Thursday, September 20, 2012 Sheet 14 of 42

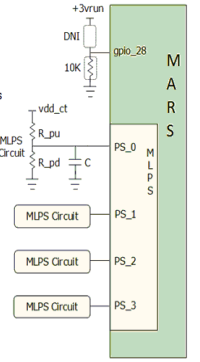
MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix- D (VEGA)	64Mx16 *8, 900Mhz	H5TQ1G63DFR-11C
0001	Micron- G die	64Mx16 *8, 900Mhz	MT41J64M16JT-107G:G
0010	Samsung- G die	64Mx16 *8, 900Mhz	K4W1G1646G-BC11
0011	Hynix- B (VEGA)	128Mx16 *8, 900Mhz	H5TQ2G63BFR-11C
0100	Micron- D die	128Mx16 *8, 900Mhz	MT41J128M16HA-107G:D
0101	Samsung- C die	128Mx16 *8, 900Mhz	K4W2G1646C-HC11
0110	Reserve		
0111	Reserve		
1000	Reserve		
1001	Hynix- D (VEGA)	128Mx16 *8, 900Mhz	H5TQ2G63DFR-11C
1010			
1011			
1100			
1101			
1110			
1111			

GPIO30 GPIO12 GPIO16 GPIO20 GPIO15 Thames XT

PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	PWRCNTL0	V-CORE
0	0	0	0	0	1.0V
0	0	0	0	1	0.9V
0	0	0	1	0	0.875V
0	0	0	1	1	0.85V
0	0	1	0	0	0.8V
0	0	1	0	1	0.75V

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance



Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

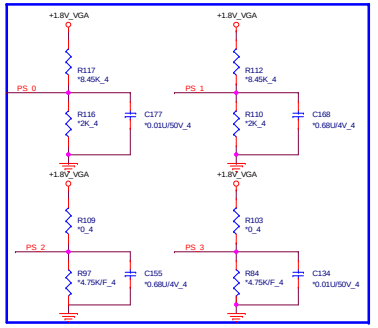
Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

BIT5 => BIT0

PS0 => 11001
PS1 => 00001
PS2 => 00000
PS3 => 11000



Memory ID

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

Mars / Chelsea : AVSSN must be short to gnd

GPIO29, 30 are NC on Thems/ whistler/ Seymour

Thames INSTALL Ra,Rb.

Do not install for Mars/ Chelsea
PS_0 should be tied to GND on Thames

PS_1,PS_2, PS_3 are NC on Thames
Do not install for Thames

Thermal Solution(Close to GPU)

Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Reserve for Power Play

For Mars: Stuff Ra only=> VDDC 1.1V
For Thems: Stuff Ra, Rb=> VDDC 1.0V

For Mars:NC pin
AL30, AM30, AL29, AM29, AN21, AM21, AK30, AK29

PV, change to 0ohm
PV, change to 0ohm
PV, change to DNI

[14,16,18,19,37] +1.0V_VGA
[16,18,19,38] +1.8V_VGA
[17,18] +3V_DELAY

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.
NB5
Size: Custom | Document Number: Mars_Main & GND | Rev: 1A
Date: Thursday, September 20, 2012 | Sheet 15 of 42

Fo Mars/ Chelsea
Change La, Lb
Bead to 0 ohm
For Thems: La,Lb:
CX8PG471000/BLM18PG471SN1D/1A_6

Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

La
+1.8V_DPLL_PVDD
Display Phase Lock Loop Power
DPLL_PVDD : 1.8V @ 75mA
+1.8V_VGA L9 *0_6
C173 *10U/6.3V_8
C175 *1U/6.3V_4
C174 *0.1U/10V_4

Lb
+1.0V_DPLL_VDDC
DPLL_VDDC : 0.935V @ 140mA
+1.0V_VGA L8 *0_6
1.0V(125mA DPLL_VDDC)
C165 *10U/6.3V_8
C171 *1U/6.3V_4
C166 *0.1U/10V_4
DPLL_PVSS

+1.8V_MPLL_PVDD
MPLL_PVDD : 1.8V @ 150mA
*BLM18PG471SN1D/1A_6
+1.8V_VGA L38
C577 *10U/6.3V_8
C575 *1U/6.3V_4
C576 *0.1U/10V_4

+1.8V_SPLL_PVDD
SPLL_PVDD : 1.8V @ 75mA
+1.0V_VGA L2 *HCB1608KF-121T30(120,3000MA)
C61 *10U/6.3V_8
C64 *1U/6.3V_4
C58 *0.1U/10V_4

+1.0V_SPLL_VDDC
SPLL_VDDC : 0.935V @ 150mA
+1.0V_VGA L1 *BLM18PG471SN1D/1A_6
1.0V(125mA DPLL_VDDC)
C56 *10U/6.3V_8
C54 *1U/6.3V_4
C57 *0.1U/10V_4
SPLL_PVSS

+1.8V_DPLL_PVDD
R115 Ra *0_4
R114 Rb *0_4
reserve Ra, Rb for future ASIC

U21I
PART 9 OF 9
AM32 DPLL_PVDD
AN31 DPLL_VDDC
AN32 DPLL_PVSS
H7 MPLL_PVDD
H8 MPLL_PVDD
AM10 SPLL_PVDD
AN9 SPLL_VDDC
AN10 SPLL_PVSS
AF30 NC_XTAL_PVDD
AF31 NC_XTAL_PVSS
PLLSXTAL
*MARS_M2_PRO

XTALIN AV33 EVGA-XTALI
XTALOUT AU34 EVGA-XTALO
R348 *10M_6
Y2 *27MHZ
*22P/50V_4 C652
*22P/50V_4 C653
XO_IN AW34 R349 Ra *0_4 EVGA-XTALI
For Mars: Stuff Ra only
XO_IN2 AW35
CLKTESTA AK10 CLKTESTA
CLKTESTB AL10 CLKTESTB

Debug only,
for clock observation,
if not needed, DNI
C62 *0.1U/10V_4
C69 *0.1U/10V_4
R39 *51.1/F_4
R45 *51.1/F_4

route 50ohms
single-ended/
100ohms diff and keep short

For Mars only : AG22 NC

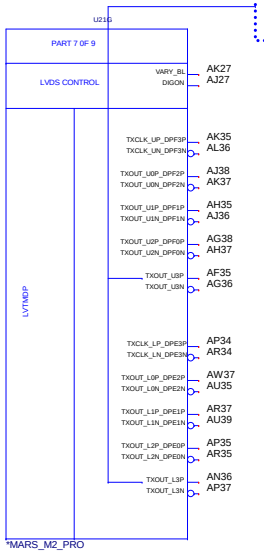
U21F
PART 6 OF 9
AB39 E39 F34 F39 G33 G34 H31 H34 H39 J31 J34 K31 K34 K39 L31 L34 M34 M39 N31 N34 P31 P34 P39 R34 T31 T34 T39 U31 U34 V34 V39 W31 W34 Y34 Y39 PCIE_VSS
F15 F17 F19 F21 F23 F25 F27 F29 F31 F33 F7 F9 G2 G6 H9 J2 J27 J6 J8 K14 K7 L11 L17 L2 L22 L24 L6 M17 M22 M24 N16 N18 N2 N21 N23 N26 N8 R15 R17 R2 R20 R22 R24 R27 R6 T11 T13 T16 T18 T21 T23 T26 U15 U17 U2 U20 U22 U24 U27 U6 V11 V16 V18 V21 V23 V26 W2 W6 Y15 Y17 Y20 Y22 Y24 Y27 GND
A3 A37 AA16 AA18 AA2 AA21 AA23 AA26 AA28 AA6 AB12 AB15 AB17 AB20 AB22 AB24 AB27 AC11 AC13 AC16 AC18 AC2 AC21 AC23 AC26 AC28 AC6 AD15 AD17 AD20 AD22 AD24 AD27 AD9 AE2 AE6 AF10 AF16 AF18 AF21 AG17 AG2 AG20 AG22 AG6 AG9 AH21 AJ10 AJ11 AJ2 AJ28 AJ6 AK11 AK31 AK7 AL11 AL14 AL17 AL2 AL20 AL23 AL26 AL32 AL6 AL8 AM11 AM31 AM9 AN11 AN2 AN30 AN6 AN8 AP11 AP7 AP9 AR5 B11 B13 B15 B17 B19 B21 B23 B25 B27 B29 B31 B33 B7 B9 C1 C39 E35 E5 F11 F13 GND
VSS_MECH A39 AW1 AW39
*MARS_M2_PRO

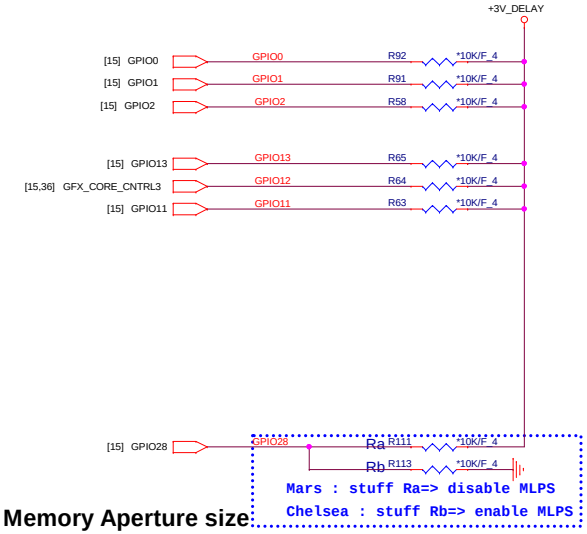
[14,18,19,37] +1.0V_VGA → +1.0V_VGA
[15,18,19,38] +1.8V_VGA → +1.8V_VGA

NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.
Size: Custom | Document Number: Mars_XTAL & GND | Rev: 1A
Date: Thursday, September 20, 2012 | Sheet 16 of 42

Fo Mars only: AF35, AG36: NC pin
Fo Mars only: AN36, AP37: NC pin





Mars : stuff Ra=> disable MLPS
Chelsea : stuff Rb=> enable MLPS

CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

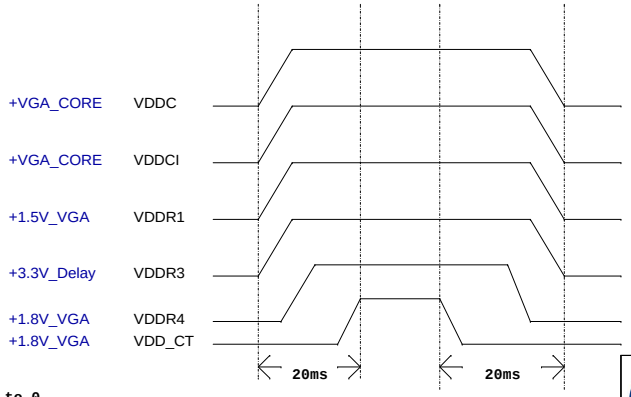
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled, It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence

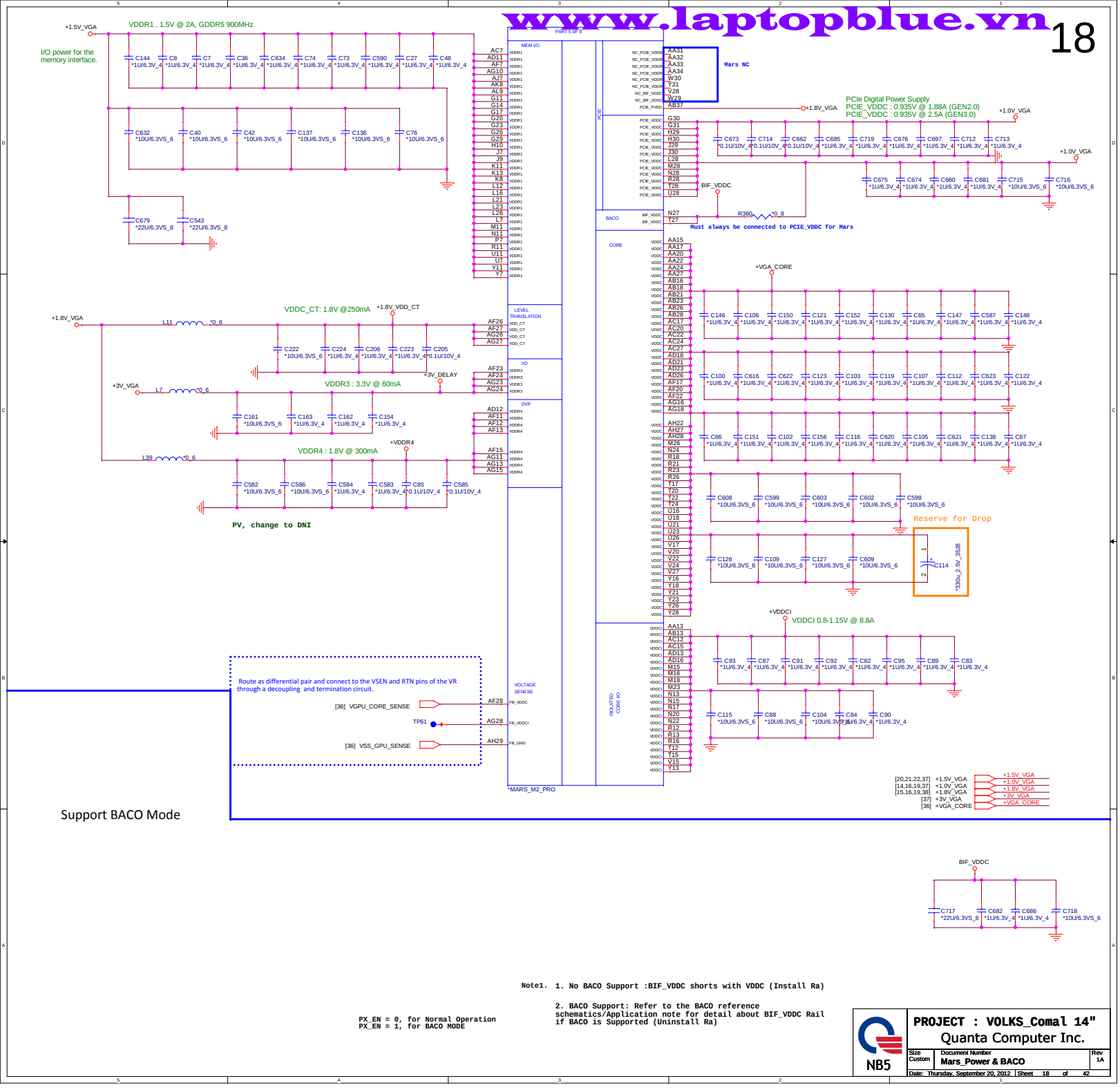


NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Mars_LVDS / STRAP	1A

Date: Thursday, September 20, 2012 Sheet 17 of 42



Support BACO Mode

Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

NB5

PROJECT : VOLKS_Comal 14"

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Mars_Power & BACO	1A

Date: Thursday, September 20, 2012 | Sheet 18 of 42

For Thames a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

U21H

PART 8 0F 9

DP_VDDR

DP_VDDC

DP GND

CALIBRATION

*MARS_M2_PRO

+1.0V_VGA

DPAB_VDD10

0.5A

L41 *0_6

C644 *0.1U/10V_4

C645 *1U/6.3V_4

C642 *10U/6.3VS_6

DP_VDDC AP31
DP_VDDC AP32
DP_VDDC AN33
DP_VDDC AP33

DP_VDDC AP13
DP_VDDC AT13
DP_VDDC AP14
DP_VDDC AP15

For Mars NC

DP_VDDC AL33
DP_VDDC AM33
DP_VDDC AK33
DP_VDDC AK34

+1.0V_VGA

0.5A

DPEF_VDD10

L42 *0_6

C659 *0.1U/10V_4

C658 *1U/6.3V_4

C677 *10U/6.3VS_6

AN24 DP_VDDR
AP24 DP_VDDR
AP25 DP_VDDR
AP26 DP_VDDR
AU28 DP_VDDR
AV29 DP_VDDR

For Mars NC

AP20 DP_VDDR
AP21 DP_VDDR
AP22 DP_VDDR
AP23 DP_VDDR
AU18 DP_VDDR
AV19 DP_VDDR

+1.8V_VGA

L43 *0_6

0.5A

DPEF_VDD18

C678 *10U/6.3VS_6

C664 *1U/6.3V_4

C663 *0.1U/10V_4

AH34 DP_VDDR
AJ34 DP_VDDR
AF34 DP_VDDR
AG34 DP_VDDR
AM37 DP_VDDR
AL38 DP_VDDR

DP_VSSR AN27
DP_VSSR AP27
DP_VSSR AP28
DP_VSSR AW24
DP_VSSR AW26
DP_VSSR AN29
DP_VSSR AP29
DP_VSSR AP30
DP_VSSR AW30
DP_VSSR AW32
DP_VSSR AN17
DP_VSSR AP16
DP_VSSR AP17
DP_VSSR AW14
DP_VSSR AW16
DP_VSSR AN19
DP_VSSR AP18
DP_VSSR AP19
DP_VSSR AW20
DP_VSSR AW22
DP_VSSR AN34
DP_VSSR AP39
DP_VSSR AR39
DP_VSSR AU37
DP_VSSR AF39
DP_VSSR AH39
DP_VSSR AK39
DP_VSSR AL34
DP_VSSR AV27
DP_VSSR AR28
DP_VSSR AV17
DP_VSSR AR18
DP_VSSR AN38
DP_VSSR AM35

For Mars :Ra ,Rb : no stuff

For Thems/ Chelsea :
Ra , Rb : stuff 150R

Ra

R108 *150/F_4 AW28 DPAB_CALR

Rb

R341 *150/F_4 AW18 DPCD_CALR

R362 *150/F_4 AM39 DPEF_CALR

[14,16,18,37] +1.0V_VGA
[15,16,18,38] +1.8V_VGA

+1.0V_VGA
+1.8V_VGA

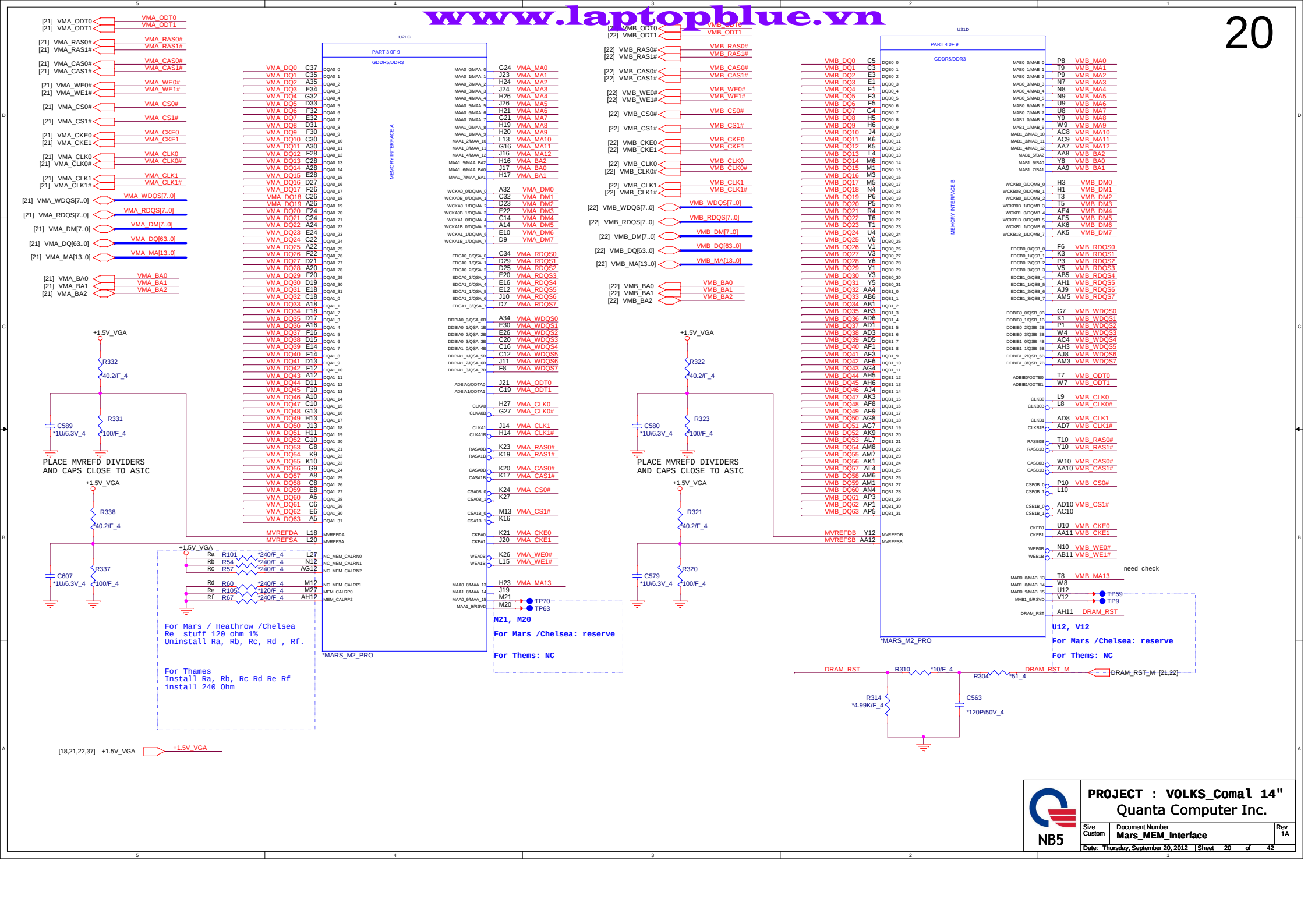
NB5

PROJECT : VOLKS_Comal 14"

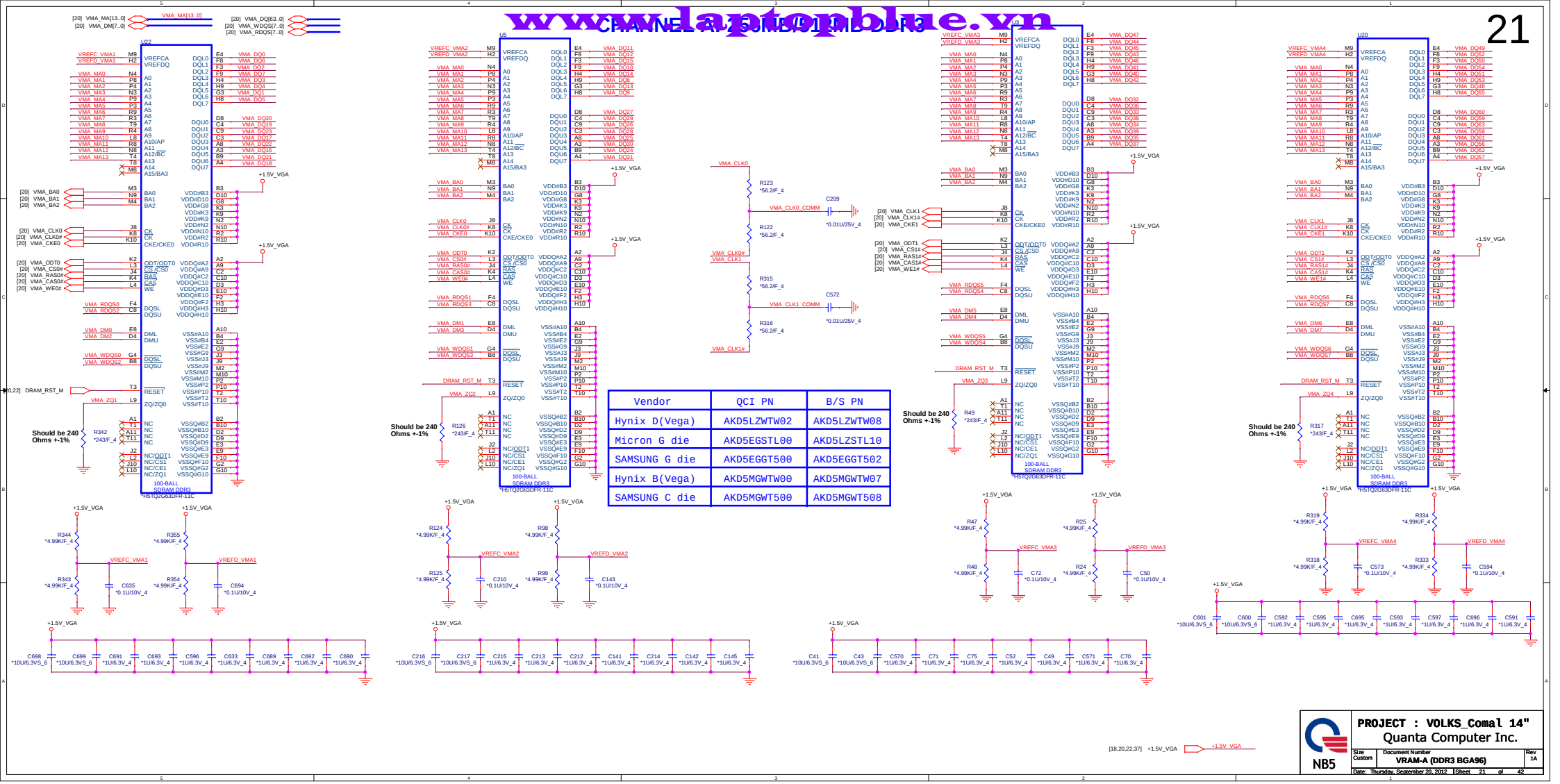
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Mars_DP Powers	1A

Date: Thursday, September 20, 2012 Sheet 19 of 42



NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
	Size: Custom — Document Number: Mars_MEM_Interface	Rev: 1A
	Date: Thursday, September 20, 2012 — Sheet 20 of 42	



Vendor	QCI PN	B/S PN
Hynix D(Vega)	AKD5LZWTW02	AKD5LZWTW08
Micron G die	AKD5EGSTL00	AKD5LZSTL10
SAMSUNG G die	AKD5EGGT500	AKD5EGGT502
Hynix B(Vega)	AKD5MGWTW00	AKD5MGWTW07
SAMSUNG C die	AKD5MGWT500	AKD5MGWT508

[18,20,22,37] +1.5V_VGA

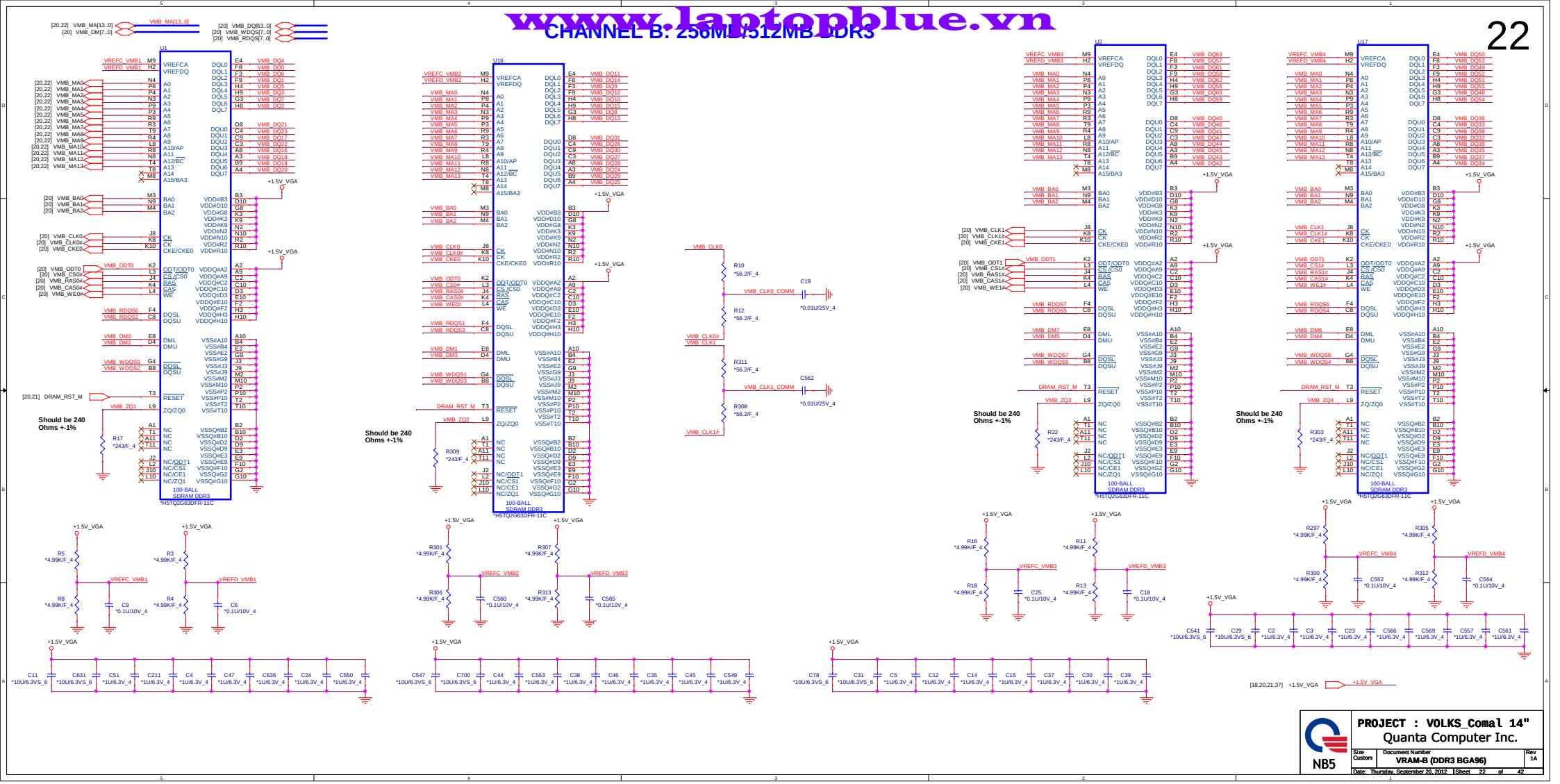
NB5

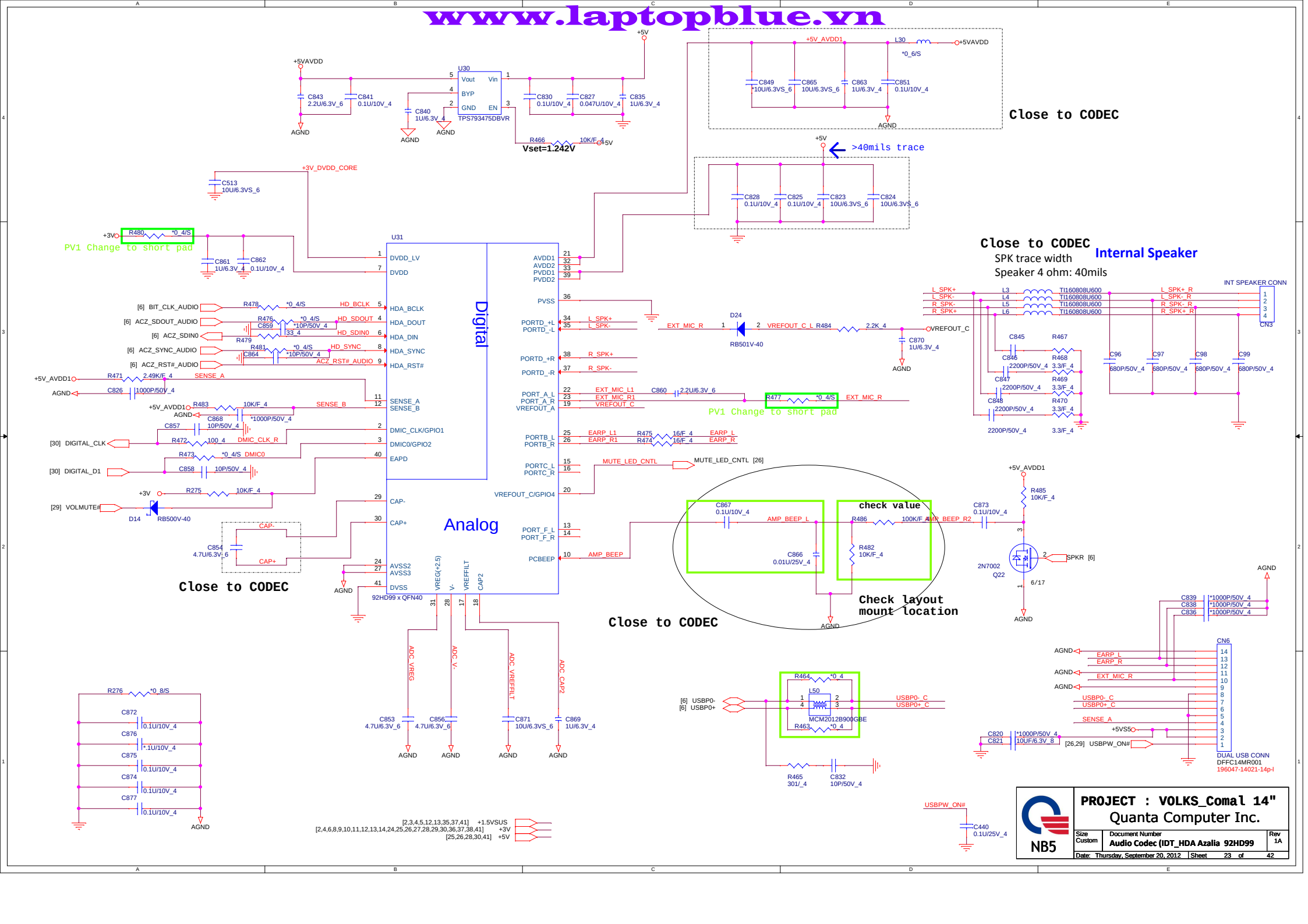
PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-A (DDR3 BGA96)	1A

Date: Thursday, September 20, 2012 | Sheet 21 of 42

CHANNEL B: 256MB/512MB DDR3





For EMI 0 ~ 22 ohm

LAN_XTAL1 R335 *10_4 XTAL1

Y1 *25MHz

XTAL2

C604 *33P/50V_4

C605 *33P/50V_4

PV2 change to non-stuff for Green Clock solution

Green Clk [27] LAN_XTAL25_IN R336 510/F_4 XTAL2

PV2 change to stuff for Green Clock solution

Change to 0603 size for EMI request

75_6 R20 C33 0.01U/100V_0603

75_6 R21 C34 0.01U/100V_0603

C555 10P/3KV_1808

U19 NS681684

LAN_MX0+ LAN_MX0- LAN_MCT1 LAN_MX1+ LAN_MX1- LAN_MCT0

TD+ TD- CT RD+ RD- CT

TX+ CMT TX- RX- CT RX+

MDI0+ V_DAC2 MDI0- MDI1- V_DAC1 MDI1+

C53 0.01U/25V_4

+3V_LAN +3VLANVCC

C613 *10U/6.3V_8 C625 0.1U/10V_4 C614 0.1U/10V_4 C611 0.1U/10V_4 C610 0.1U/10V_4

GND VIA x 9 Pcs

+1.05V_LAN

R52 2.49K/F_4 LANRSET

+3V_LAN

LAN_TX# LAN_GPIOS R340 1K/F_4 +3V_LAN LAN_GLINK100#

U4 RTL8105E

GND AVDD33 AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 AVDD33 DVDD10(NC) LED0 DVDD33 GPIO/SMBALERT LED1/EESK XTAL2 XTAL1

MDI0+ MDI0- MDI1+ MDI1-

MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 AVDD10(NC) MDIP2(NC) MDIN2(NC) AVDD10(NC) MDIP3(NC) MDIN3(NC) AVDD33(NC)

REGOUT VDDREG VDDREG ENSWREG EEDI LED3/EEDO EECS DVDD10 LANWAKEB DVDD33 ISOLATEB PERSTB

LAN_GLINK10# TP1

LAN_ECS_SCL TP2

+1.05V_LAN

PCIE_WAKE# PCIE_WAKE# [6,27]

+3V_LAN

ISOLATEB

PLTRST# LAN_PCIE_RST# [7]

DVDD10 SMBCLK(NC) SMBDATA(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_N EVDD10 HSOP HSON GND

+1.05V_LAN

LAN_CLKRQ EVDD10

[6] PCIE_CLKREQ_LAN# PCIE_CLKREQ_LAN# R102 *0_4/S

[7] PCIE_TXP1_LAN [7] PCIE_TXN1_LAN PCIE_TXP1_LAN PCIE_TXN1_LAN

[7] CLK_PCIE_LANP [7] CLK_PCIE_LANN CLK_PCIE_LANP CLK_PCIE_LANN

PCIE_RXN1_LAN_L C159 0.1U/10V_4 PCIE_RXN1_LAN [7]

PCIE_RXP1_LAN_L C158 0.1U/10V_4 PCIE_RXP1_LAN [7]

+3V

R100 1K/F_4

ISOLATEB

R86 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

+1.05V_LAN

C624 0.1U/10V_4 C627 0.1U/10V_4 C628 0.1U/10V_4 C612 *10U/6.3V_8

EVDD10

C626 1U/6.3V_4 C619 0.1U/10V_4

+3VLANVCC R19 62_4 C26 1000P/50V_4

2P Amber LED(Side-View) LED3

LAN_YLED (Amber) LAN_TX#

朝前

+3VLANVCC R1 62_4

2P WHITE LED(Side-View) LED2

LAN_GLED (White) LAN_GLINK100#

C1 1000P/50V_4

朝前

RJ45

CN8 RJ45_CONN

LAN_MX1- LAN_MX1+ LAN_MX0- LAN_MX0+

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+

GND2 GND1 GND3 GND4

R23 *0_6/S

R2 *0_6/S

C10 68P/50V_4

NB5

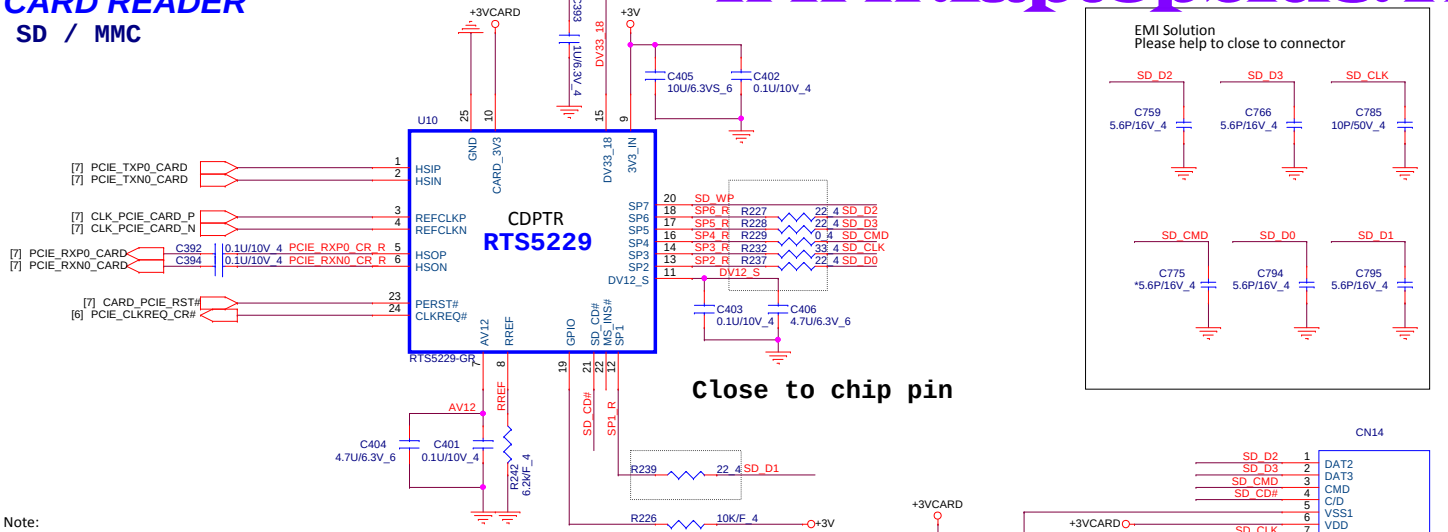
PROJECT : VOLKS_Comal 14"

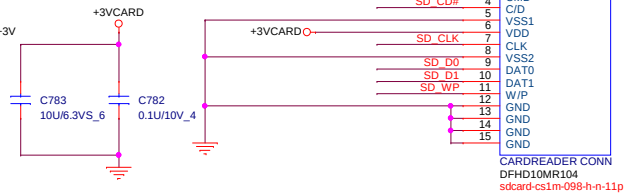
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN RTL8105/RJ45	1A

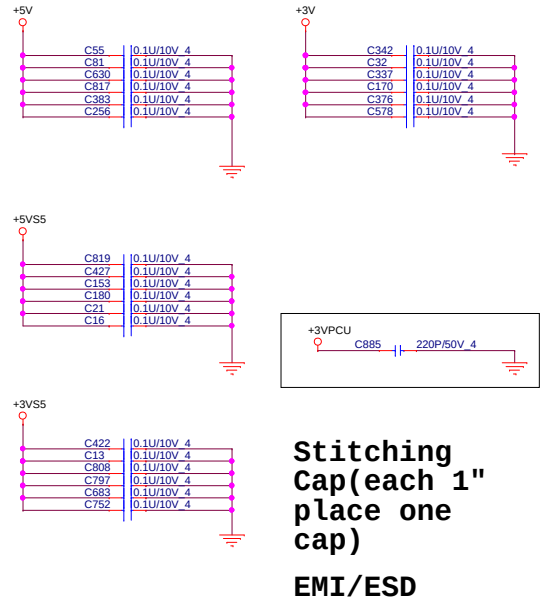
Date: Thursday, September 20, 2012 Sheet 24of 42

CARD READER
SD / MMC



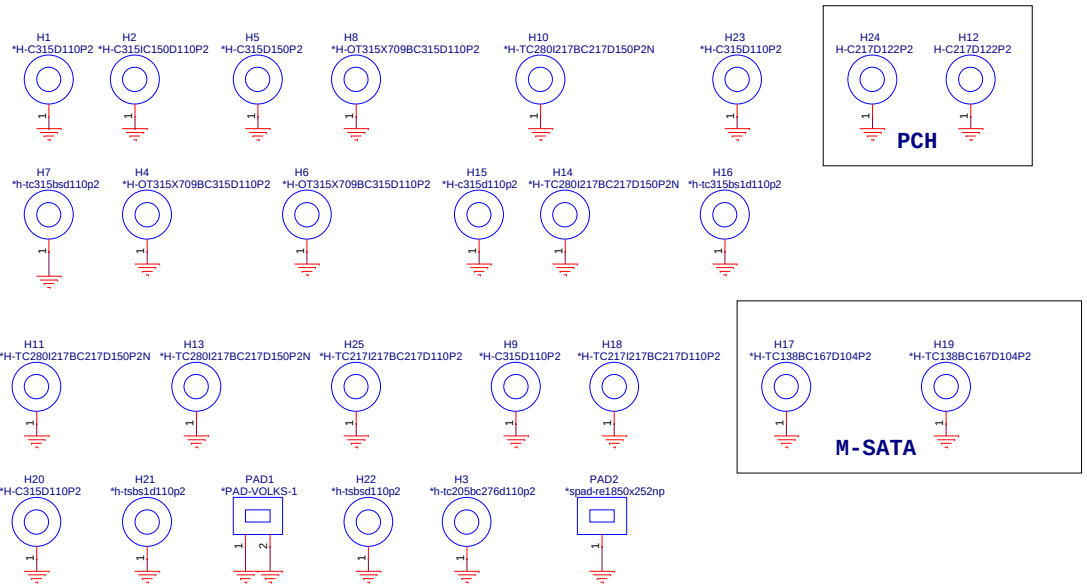


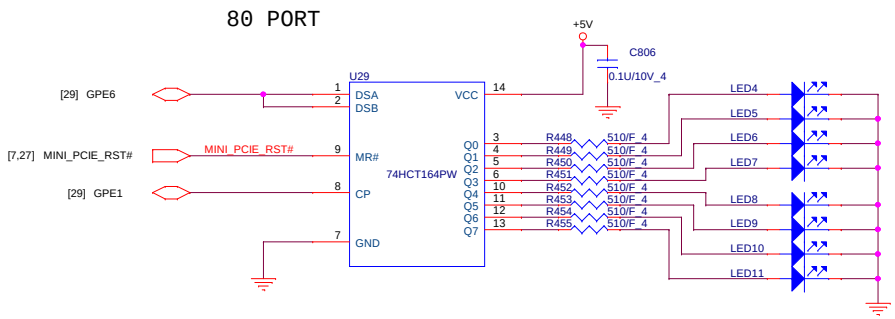
Note:
1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4



Stitching Cap(each 1" place one cap)

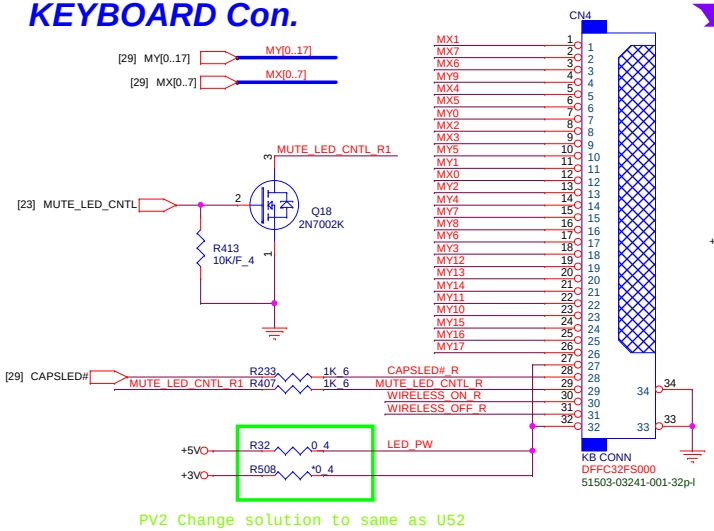
EMI/ESD



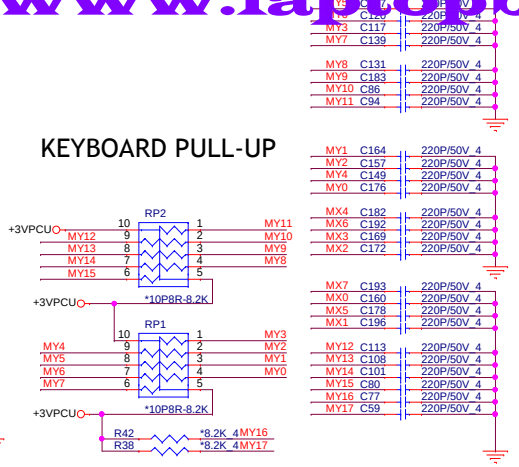


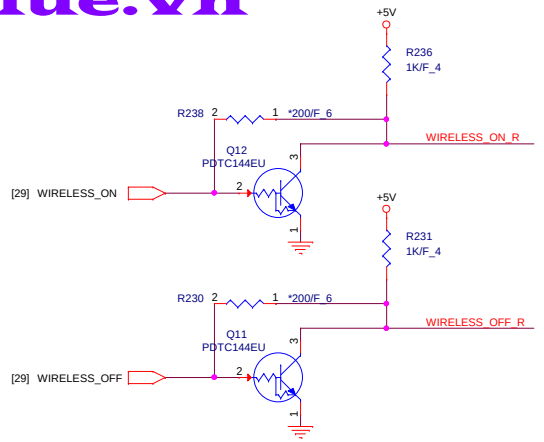
NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size: Custom	Document Number: Card Reader control (RTS5229-GR)	Rev: 1A
Date: Thursday, September 20, 2012	Sheet: 25of	42

KEYBOARD Con.

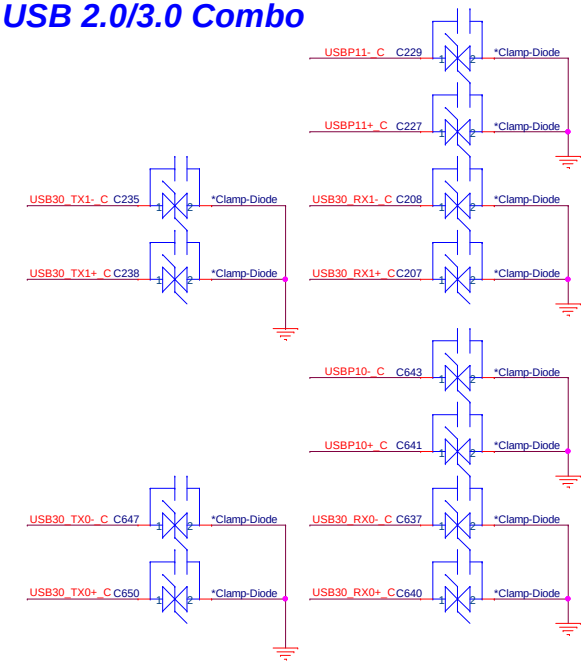


KEYBOARD PULL-UP

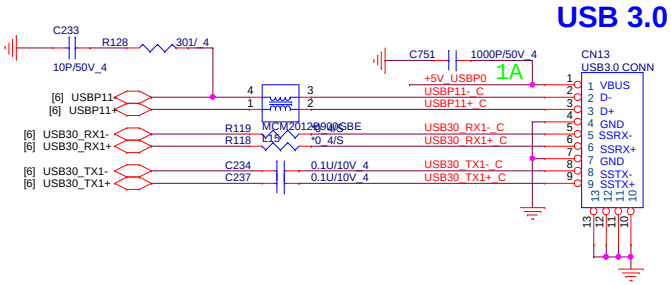




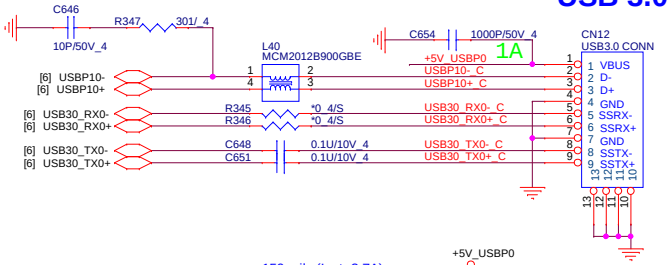
USB 2.0/3.0 Combo

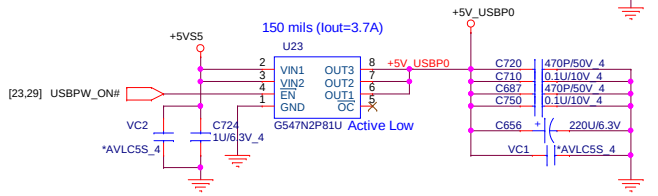


USB 3.0

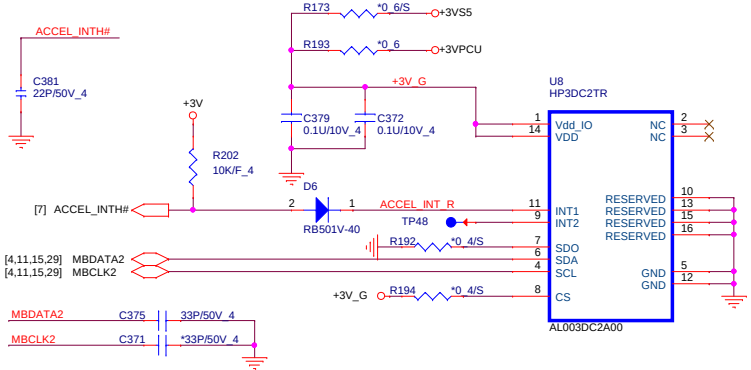


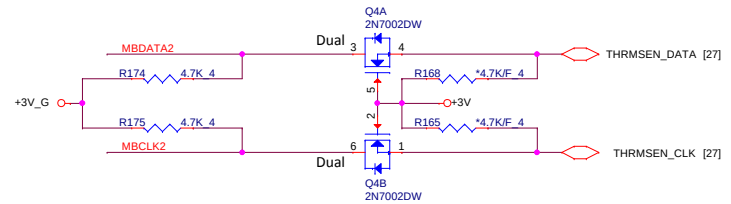
USB 3.0





Accelerometer Sensor





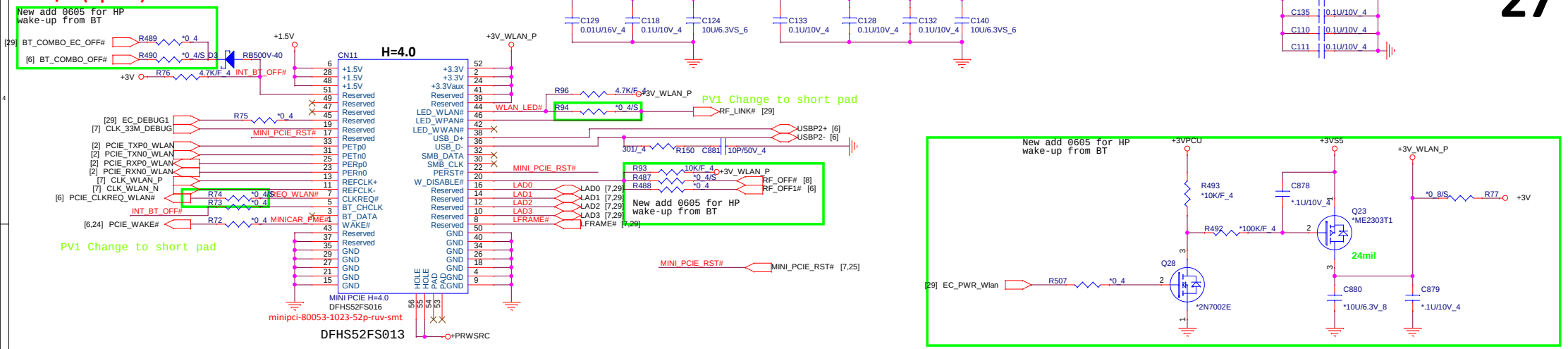
[23,25,32,33,34,35,36,38,39,40,41] +5VS5
[4,7,25,27,28,29,30,31,32] +3VPCU

NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

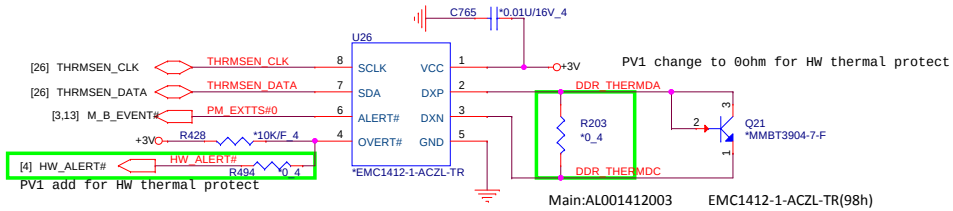
Size	Document Number	Rev
Custom	USB 3.0/KB/Green CLK	1A
Date: Thursday, September 20, 2012	Sheet 26of	42

Mini Card WLAN/BT(Option)



Local Thermal Sensor

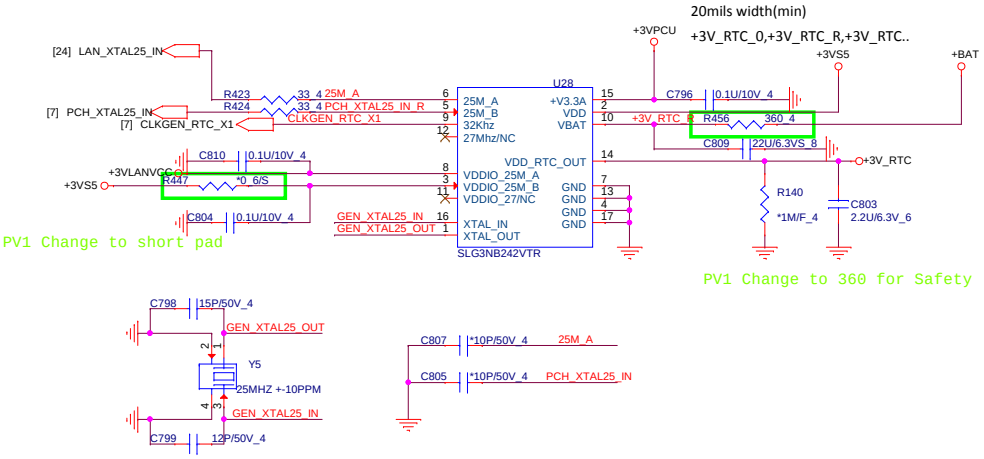
DDR3 Thermal Sensor



Main:AL001412003 EMC1412-1-ACZL-TR(98h)

2nd:AL000431014 TMP431ADGKR(98h)

Green CLK Circuitry



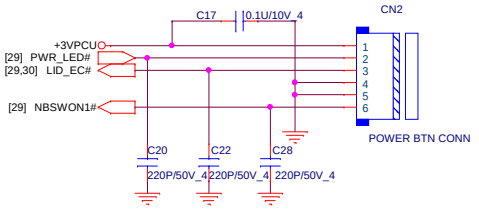
[6,8,9,10,25,26,29,32,34,36,37,41] +3VS5
[2,4,6,8,9,10,11,12,13,14,23,24,25,26,28,29,30,36,37,38,41] +3V
[23,25,26,28,30,41] +5V
[4,7,25,26,28,29,30,31,32] +3VPCU
[2,4,11,28,39,41] +1.5V

PROJECT : VOLKS_Comal 14"		
Quanta Computer Inc.		
Size: Custom	Document Number: MINI-PCIE/LED	Rev: 1A
Date: Thursday, September 20, 2012	Sheet: 27of 42	

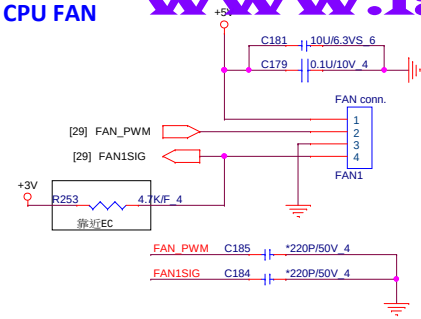
NB5

Power Botton Connector

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

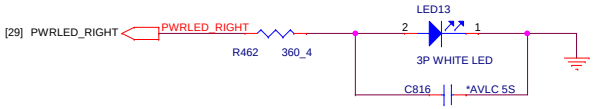


CPU FAN

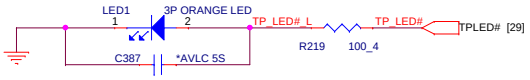


LED Status

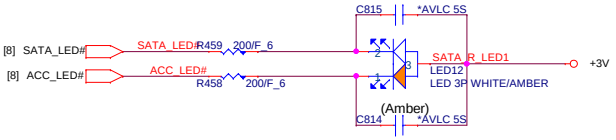
PWR LED



14 "TP LED

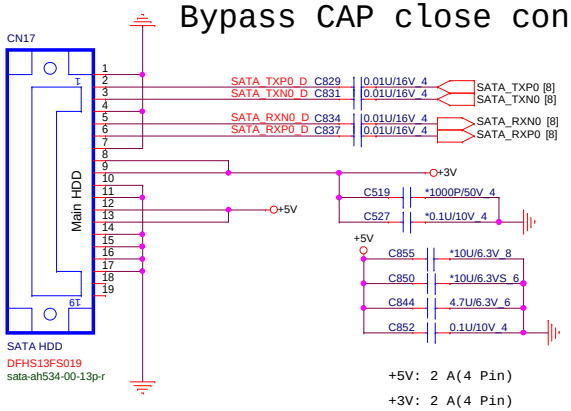


SATA LED

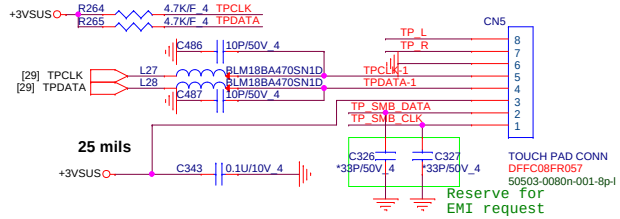


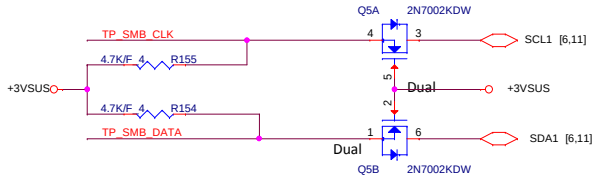
SATA HDD Connector(Cable type)

Bypass CAP close conn

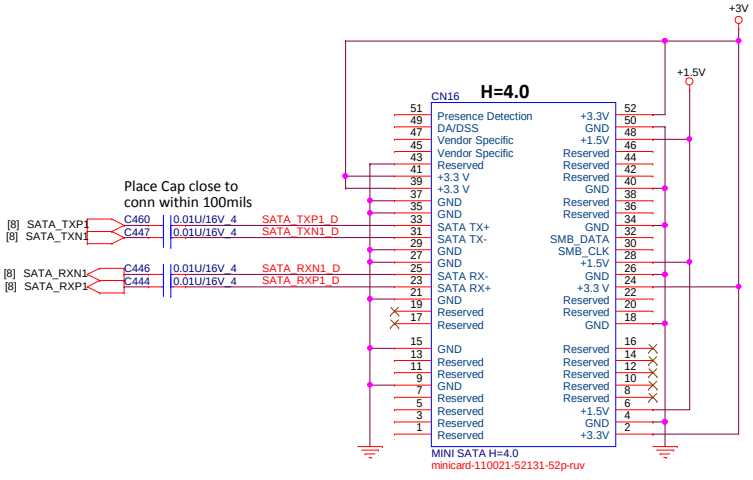


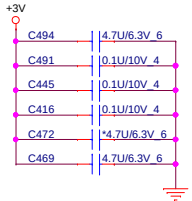
+5V: 2 A(4 Pin)
+3V: 2 A(4 Pin)
Gnd : (5 Pin)

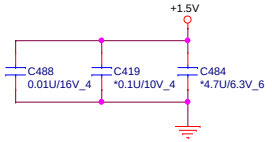




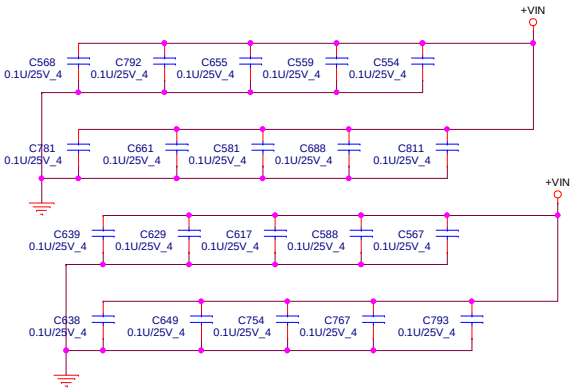
Mini PCI-E Card 2- Full size
mSATA



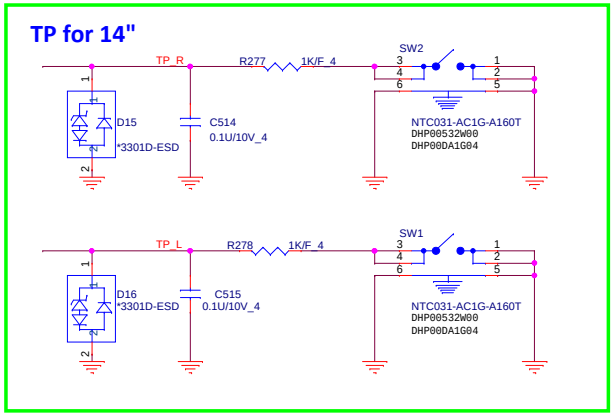




+VIN Cap



TP for 14"



[2,4,6,8,9,10,11,12,13,14,23,24,25,26,27,29,30,36,37,38,41] +3V
[23,25,26,30,41] +5V
[4,7,25,26,27,29,30,31,32] +3VPCU
[2,4,11,27,39,41] +1.5V
[31,37,41] +12VALW

NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size: Custom	Document Number: SATA HDD/ODD/MSATA CONN	Rev: 1A
Date: Thursday, September 20, 2012	Sheet: 28of	42

ITE pin 100 , 104 , 106 default can not pull up to +3VPCU it will cause chip into test mode

+3VPCU CAP close to EC pin

CAPS LED

CAPSLED# [26]

Q10 2N7002K

+3VPCU_AC L29 FCM1608KF-121T04

+3VPCU_EC L24 FCM1608KF-121T04

500mA

Change to RB500 as Current loss

SCI1# D12 RB501V-40 SIO_EXT_SCI# [6]

DNBSWON1# D13 RB501V-40 DNBSWON# [6]

KBSMI#1 D10 RB501V-40 SIO_EXT_SMI# [6]

For +VIN noise

Vender	Size	P/N
PME	4M	AKE39ZN0500
GGD	4M	AKE39GN0Q00
AMC	4M	AKE39F-0800
Socket		DFHS08FS023

4M SPI EC ROM

U13 A25LQ32AM-F/Q AKE39F-0800 SOIC8-8-1_27

128K byte SPI EC ROM

U12 *DFHS08FS023 SOIC8-6-1_27

ICT need TP2675 size test point

TP place on top lay for ICT request

IT8518E/HX

LPC: LAD0–LAD3, LFRAME#, LPCRST#/WUI4/GPD2, LPCCLK, LPCPD#/WUI6/GPE6, GA20/GPB5, SERIRQ, ECSMI#/GPD4, ECSCI#/GPD3, WRST#, KBRST#/GPB6, PWUREQ#/BBO/GPC7

GPIO: EGCLK/WUI27/GPE3, EGCS#/WUI26/GPE2, EGAD/WUI25/GPE1, KSO16/SMOSI/GPC3, KSO17/SMISO/GPC5, L80HLAT/BAO/WUI24/GPE0, L80LLAT/WUI7/GPE7, SBUSY/GPG1/ID7, HMOSIGPH6/ID6, HMISO/GPH5/ID5, HSCK/GPH4/ID4, HSCE#/WUI19/GPH3/ID3, CTX1/WUI18/GPH2/SMDAT3/ID2, CRX1/WUI17/GPH1/SMCLK3/ID1, CLKRUN#/WUI16/GPH0/ID0

GPC0 TMA0/GPB2

PS/2: PS2DAT0/TMB1/GPF1, PS2CLK0/TMB0/GPF0, PS2DAT2/WUI21/GPF5, PS2CLK2/WUI20/GPF4

SM_BUS: SMCLK2/WUI22/GPF6/PECI, SMDAT2/WUI23/GPF7, SMCLK0/GPB3, SMDAT0/GPB4, SMCLK1/GPC1, SMDAT1/GPC2

UART: DAC4/DCD0#/GPJ4, DSR0#/GPG6, GINT/CTS0#/GPD5, PS2DAT1/RTS0#/GPF3, DAC5/RIG0#/GPJ5, PS2CLK1/DTR0#/GPF2, RXD/SIN0/GPB0, TXD/SOUT0/GPB1

PWM: PWM0/GPA0, PWM1/GPA1, PWM2/GPA2, PWM3/GPA3, PWM4/GPA4, PWM5/GPA5, PWM6/SSCK/GPA6, PWM7/GPA7, TACH0/GPD6, TACH1/TMA1/GPD7, TMR0/WUI2/GPC4, TMR1/WUI3/GPC6

FLASH: GPG0 FSCK, FMISO FMOSI FSCE# SSCE0#/GPG2

KBMX: KSO0/PD0 … KSO17/ERR#, KSO12/SLCT, KSO13, KSO14, KSO15, KSI0/STB#, KSI1/AFD#, KSI2/INIT#, KSI3/SLIN#, KSI4, KSI5, KSI6, KSI7

WAKE UP: PWRSW/GPE4, RI1#/WUI0/GPD0, RI2#/WUI1/GPD1, WUI5/GPE5, RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7

A/D D/A: ADC0/GPI0, ADC1/GPI1, ADC2/GPI2, ADC3/GPI3, ADC4/WUI28/GPI4, ADC5/WUI29/GPI5, ADC6/WUI30/GPI6, ADC7/WUI31/GPI7

CLOCK: CK32K, CK32KE

DAC0/GPJ0, DAC1/GPJ1, DAC2/GPJ2, DAC3/GPJ3

TPLED# [28], VRON [33,39], GPE1 [25], EC_PWR_Wlan [27], BT_COMBO_EC_OFF# [27], SUSON [35,41], CAPSLED#_OUT, PWRLED_RIGHT [28], EC_BIOS_WR# [8], EC_BIOS_RD# [8], EC_BIOS_SPI_CLK_I [8], EC_BIOS_CS# [8], MAINON [34,35,41], RF_LINK# [27], CLKRUN# [7]

For GPU thermal

for Battery charge/discharge

for CPU themal

GPUT_CLK [15], GPUT_DATA [15], MBCLK [31], MBDATA [31], MBCLK2 [4,11,15,26], MBDATA2 [4,11,15,26]

WIRELESS_OFF [26], WIRELESS_ON [26], AC_LED_ON# [31], MBATLED0# [31], FAN_PWM [28], LAN_POWER [41], VOLMUTE# [23], PWM_VADJ [11]

FAN1SIG [28], S5_ON [32,34]

SUSC# [6], ECPWROK [4,10]

from power button

NBSWON1# [28], LID_EC# [28,30], ACIN [31,41], SUSB# [6]

VGA_ON_SB [6], DGPU_PWROK [4,6,7,36,37,38], SYS_I [31], AD_AIR [31], TEMP_MBAT [31]

BATSHIP [31], PCI_SERR# [7], ODD_PD, DNBSWON1#, TP54

AJ085180F04 IT8518E/HX

IT8518_AGND

PWR_LED

0424 Fix PWR_LED

Q15 MMBT3904-7-F

Adapter select

Hi ==> DIS/SG
Low ==>UMA

Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

PV1 Change to short pad

NB5

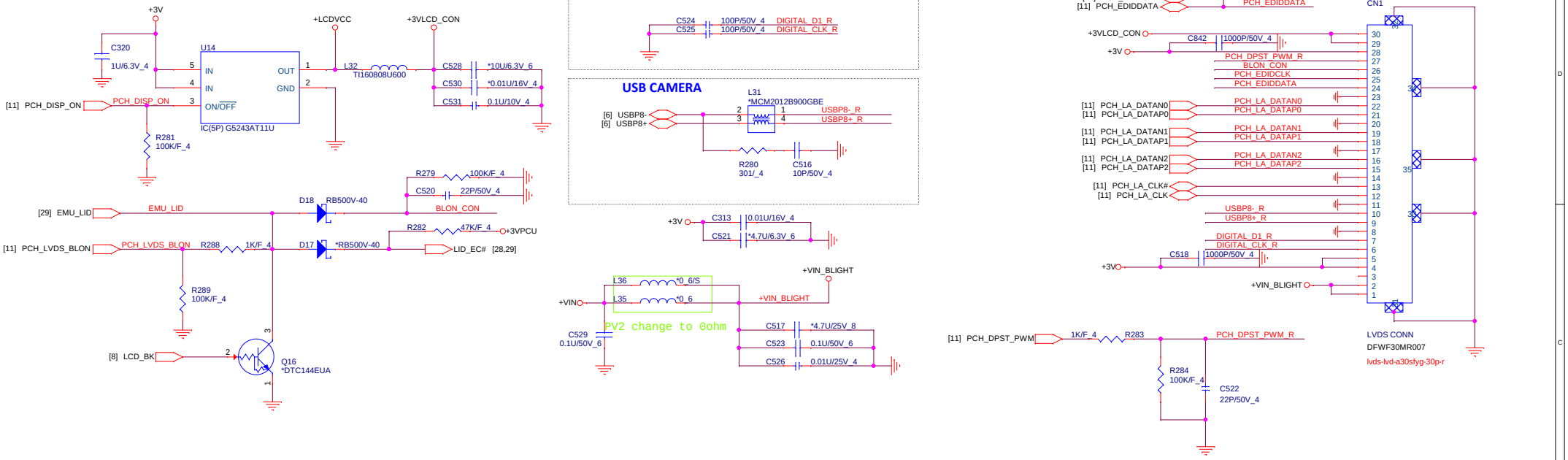
PROJECT : VOLKS_Comal 14"

Quanta Computer Inc.

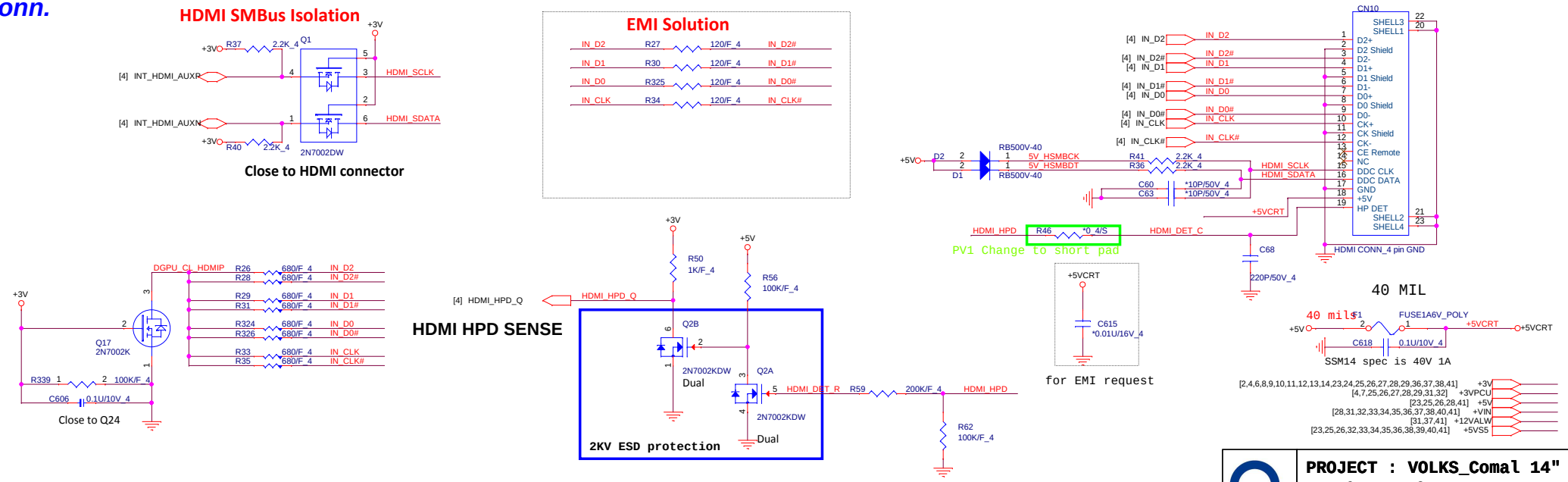
Size: Custom | Document Number: EC (KB3926)/ROM | Rev: 1A

Date: Thursday, September 20, 2012 | Sheet 29 of 42

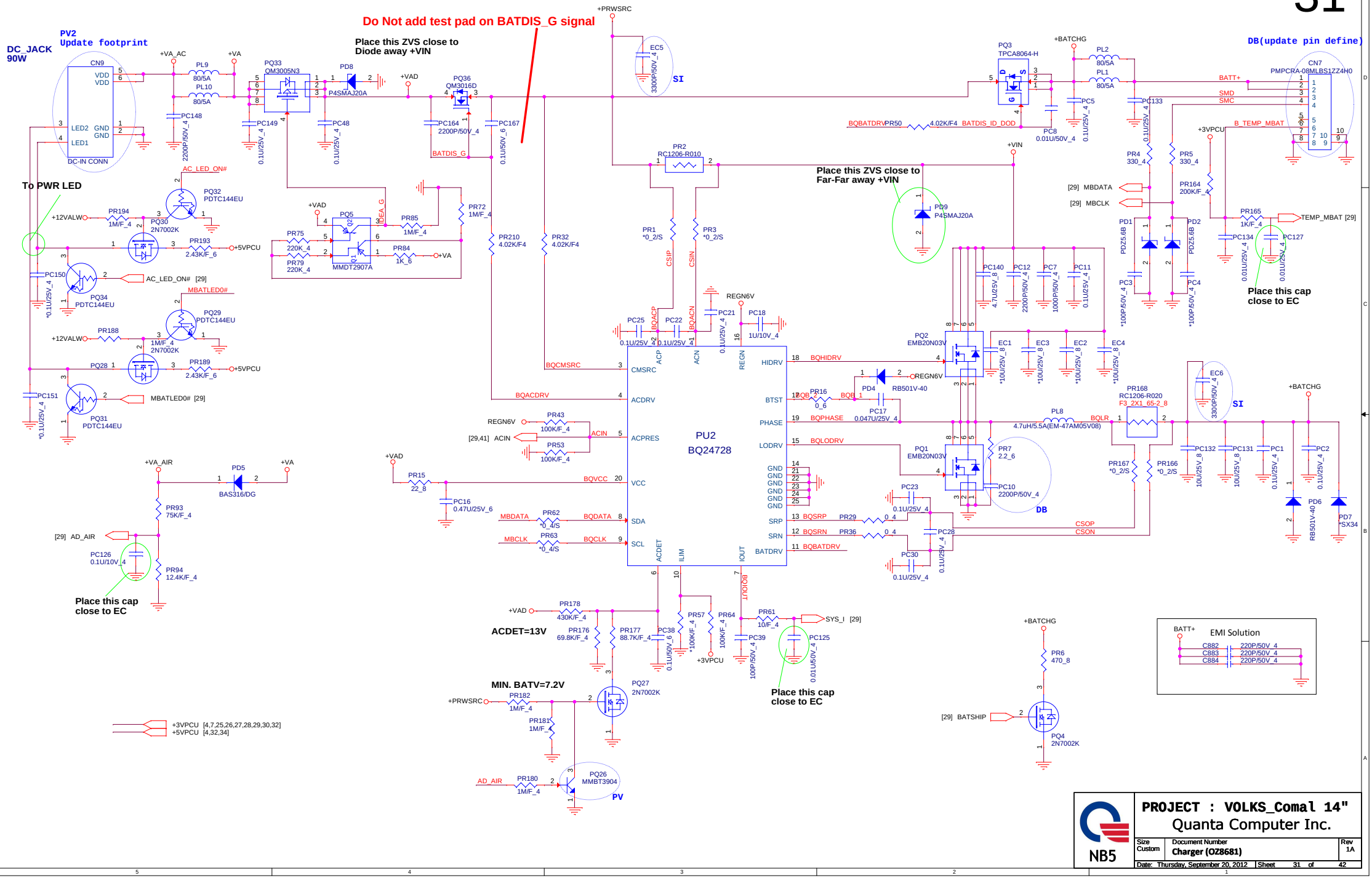
LVDS Conn.



HDMI Conn.

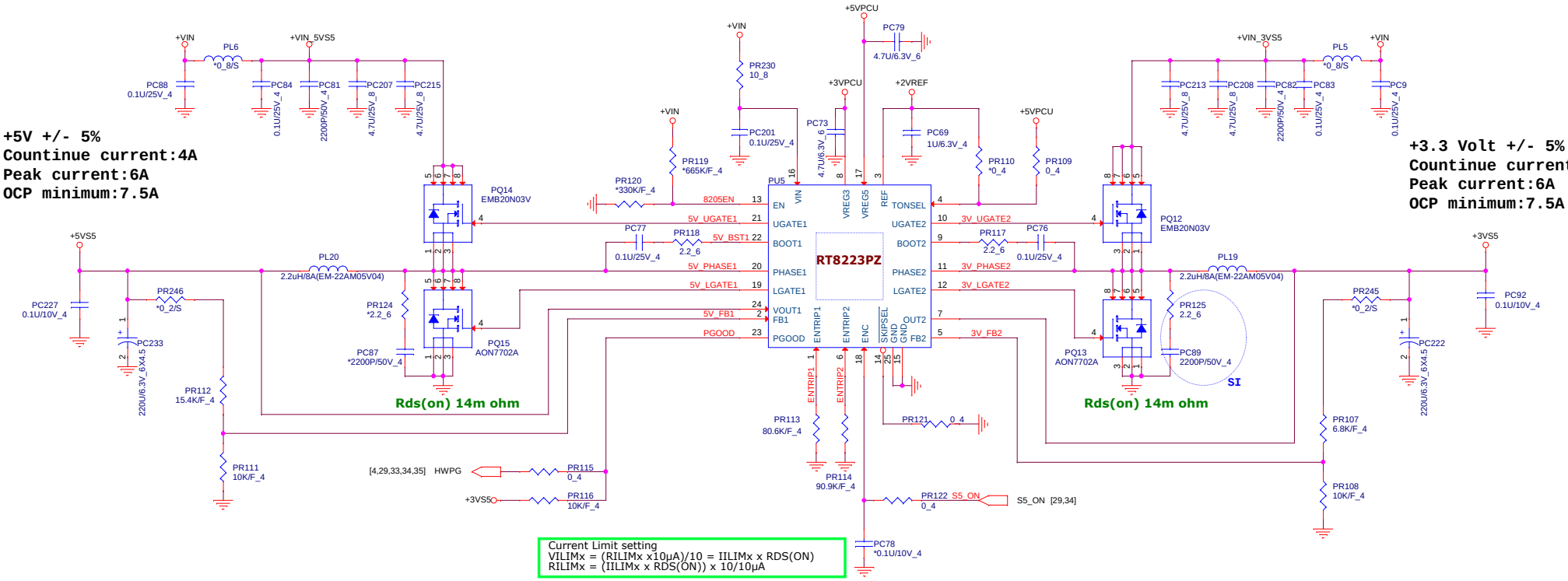


NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.		
	Size: Custom	Document Number: LCD Connector (LVDS)	Rev: 1A
	Date: Thursday, September 20, 2012	Sheet: 30of	42



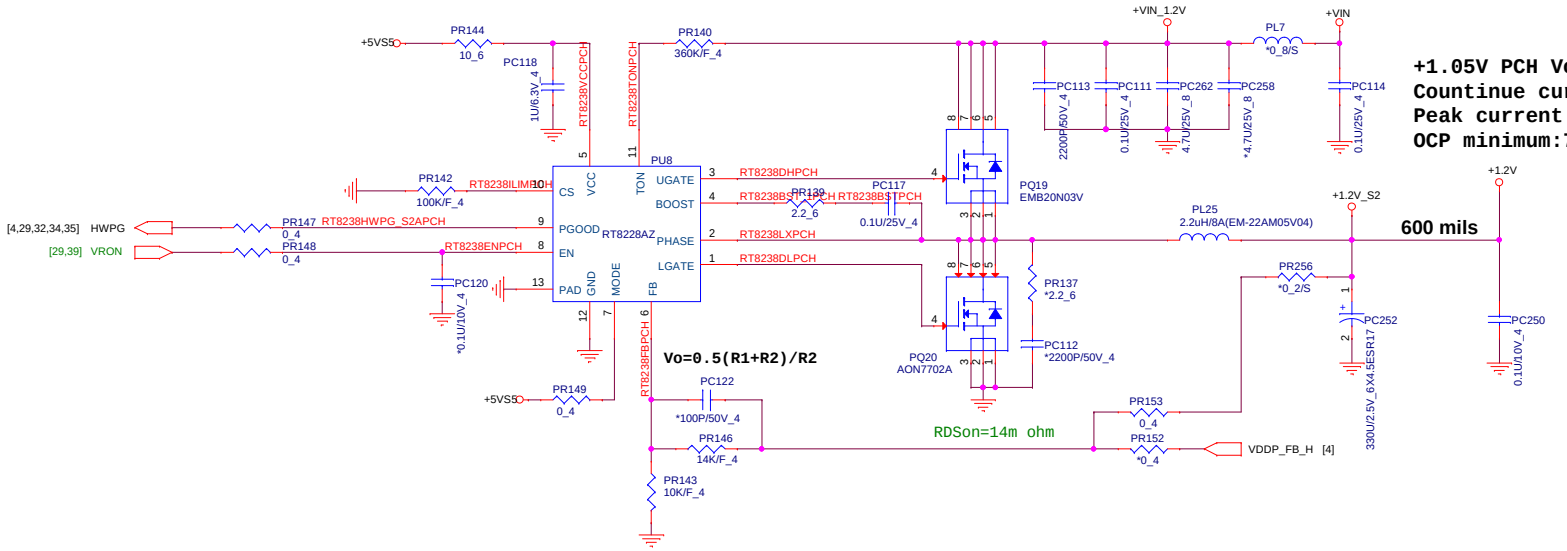
+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

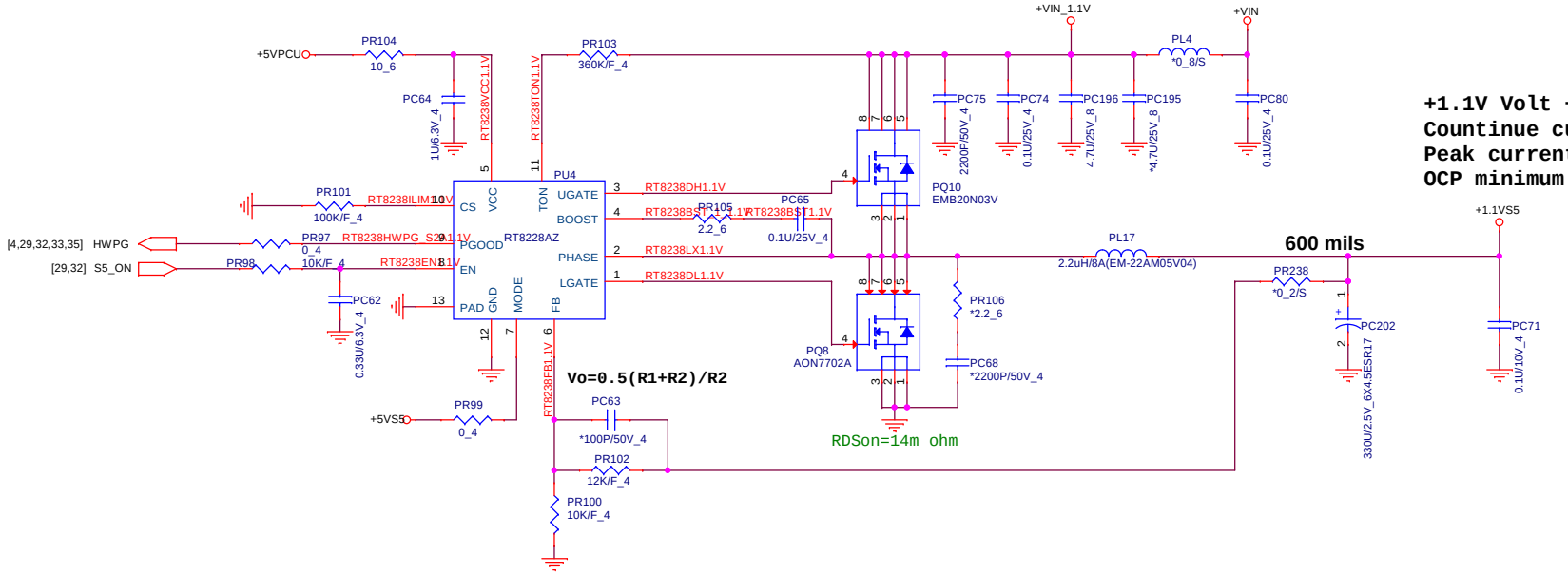


Size: Custom	Document Number: 3/5VS5 (RT8223P)	Rev: 1A
Date: Thursday, September 20, 2012	Sheet 32 of 42	

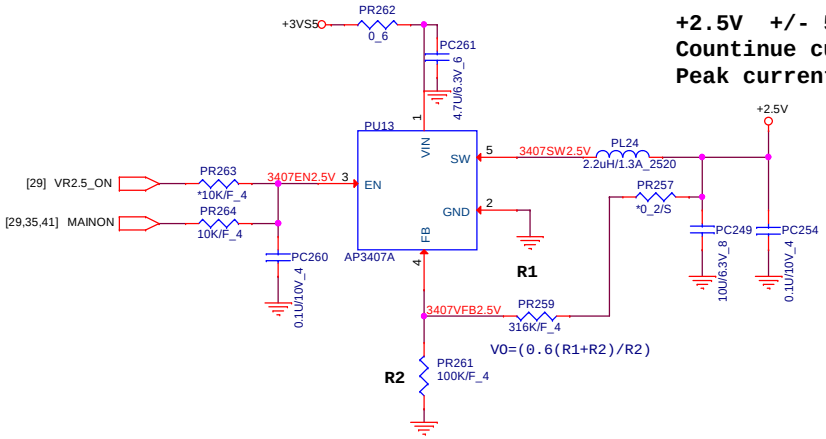
PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.
NB5



NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
	Size: Custom — Document Number: +1.2V (RT8228)	Rev: 1A
	Date: Thursday, September 20, 2012 — Sheet 33 of 42	

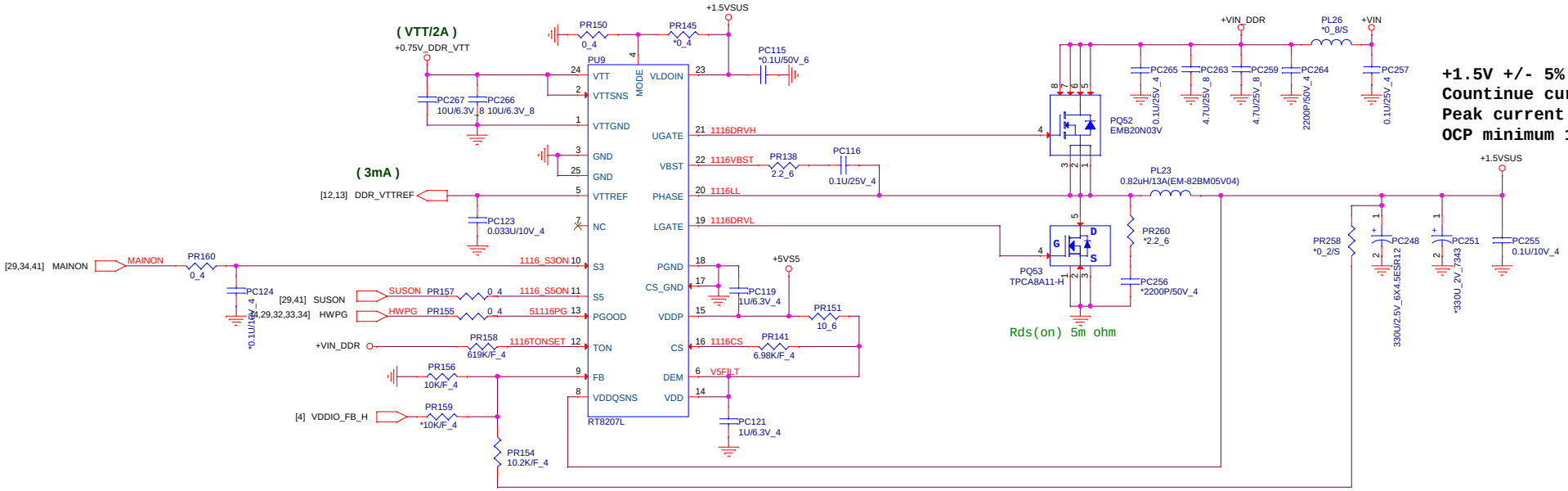


+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 6.5A
OCP minimum:7.5A



+2.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A

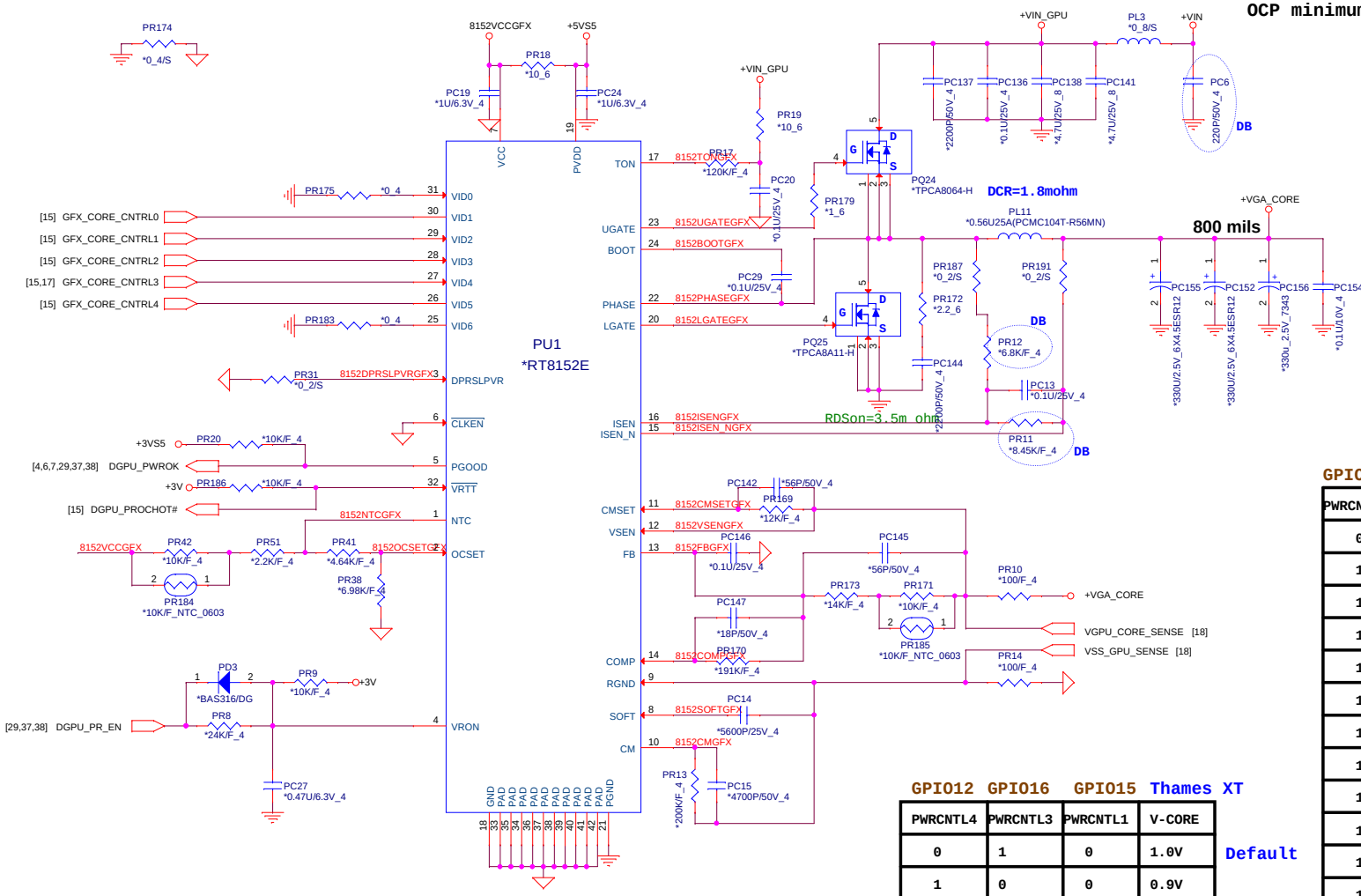
NB5	**PROJECT : VOLKS_Comal 14"** Quanta Computer Inc.	
Size: Custom	Document Number: **+1.1VS5 (RT8228)/2.5V**	Rev: 1A
Date: Thursday, September 20, 2012	Sheet 34 of 42	



NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 (RT8207)	Rev: 1A
Date: Thursday, September 20, 2012	Sheet 35 of 42	

VGA Core

+VGA_UMA +/- 5%
Countinue current:18A
Peak current:22A
OCP minimum 25A



GPIO12 GPIO16 GPIO15 Thames XT

PWRCNTL4	PWRCNTL3	PWRCNTL1	V-CORE	
0	1	0	1.0V	Default
1	0	0	0.9V	
1	0	1	0.875V	

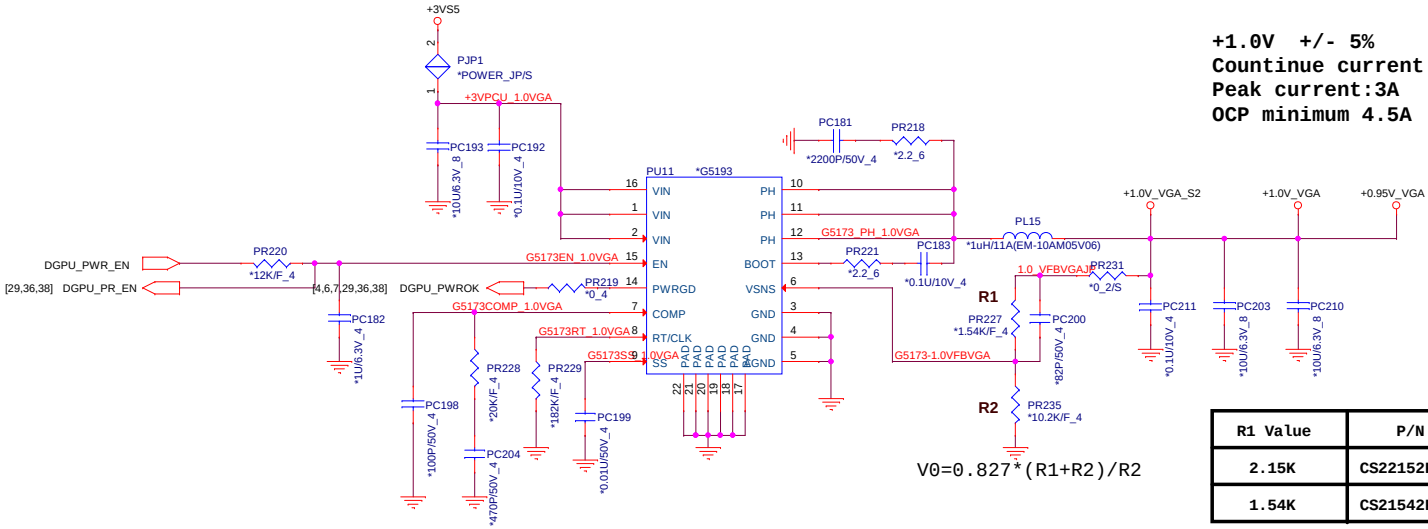
GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	Default
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	
1	1	1	0	1	0.775V	PV

NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE NCP3218G)	1A
Date: Thursday, September 20, 2012	Sheet 36 of 42	



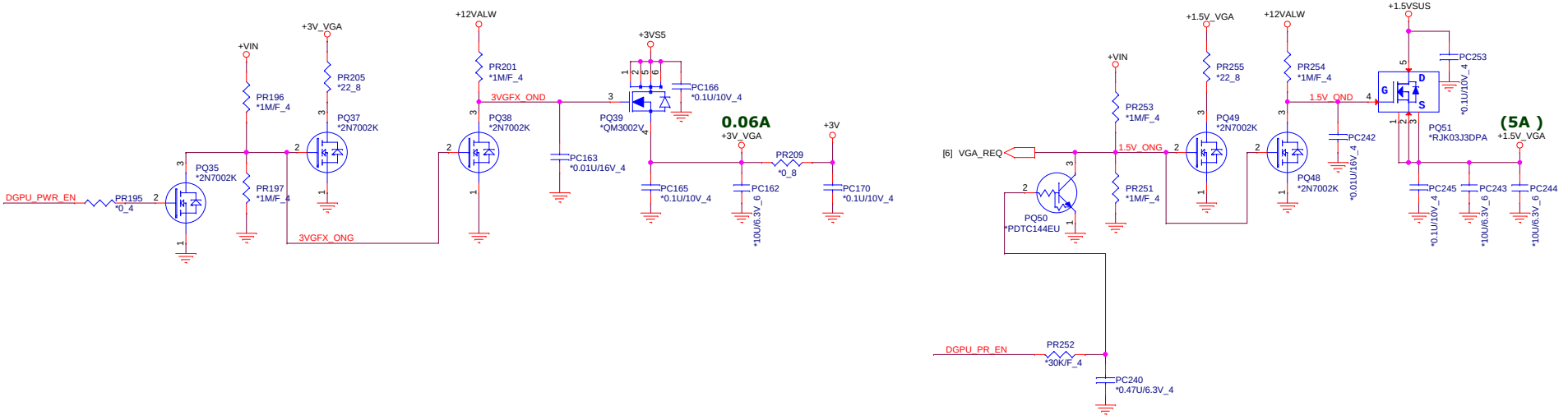
+1.0V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

V0=0.827*(R1+R2)/R2

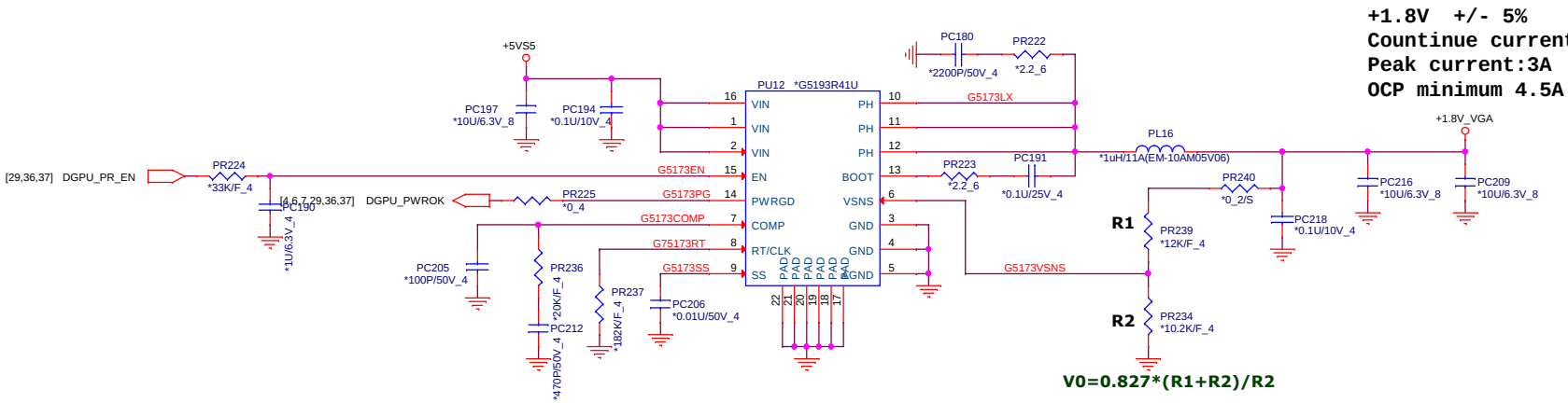
R1 Value	P/N	1.0V_VGA
2.15K	CS22152FB07	1.0V
1.54K	CS21542FB02	0.95V

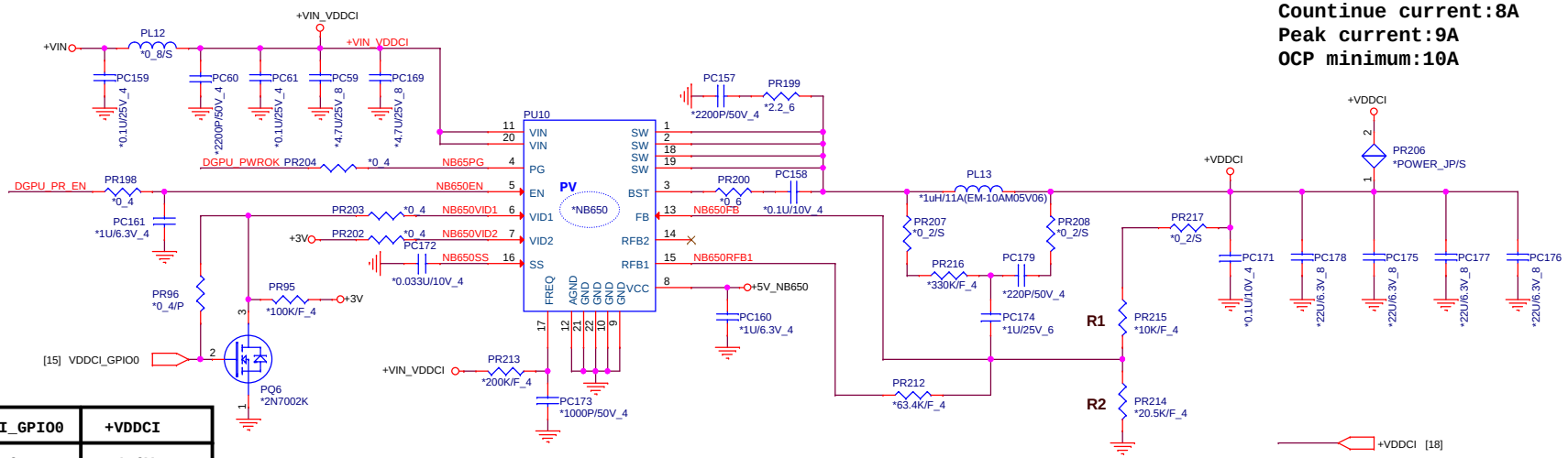
+3V [2,4,6,8,9,10,11,12,13,14,23,24,25,26,27,28,29,30,36,38,41]
+VIN [28,30,31,32,33,34,35,36,38,40,41]

+3VS5 [6,8,9,10,25,26,27,29,32,34,36,41]
+5VS5 [23,25,26,32,33,34,35,36,38,39,40,41]
+3V_VGA [18]
+12VALW [31,41]
+1.5VSUS [2,3,4,5,12,13,35,41]
+1.5V_VGA [18,20,21,22]
+1.8V_VGA [15,16,18,19,38]
+3V_DELAY [15,17,18]
+VGA_CORE [18,36]



NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size: Custom	Document Number: +VGA POWER	Rev: 1A
Date: Thursday, September 20, 2012	Sheet 37 of 42	





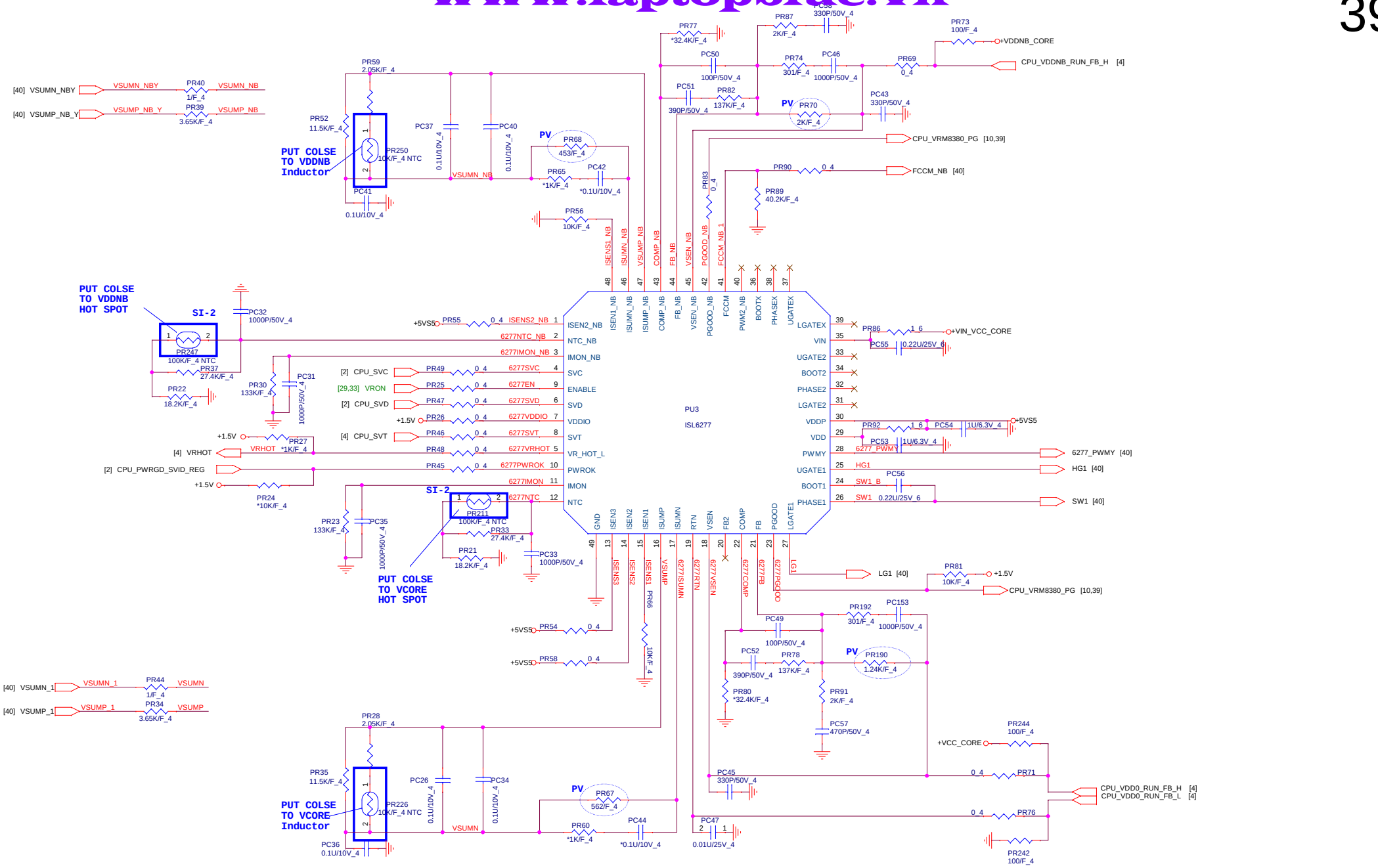
VDDCI_GPIO1	VDDCI_GPIO0	+VDDCI
X	0	1.0V
X	1	0.9V
X	X	X
X	X	X

NB5

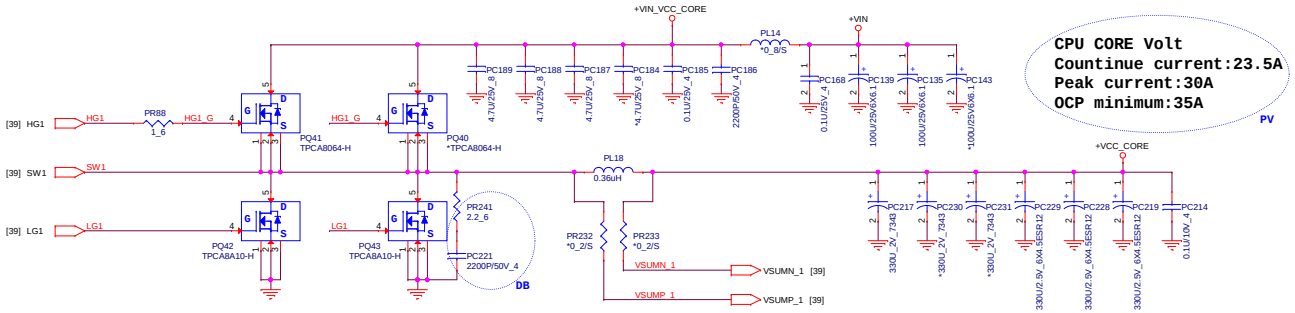
PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

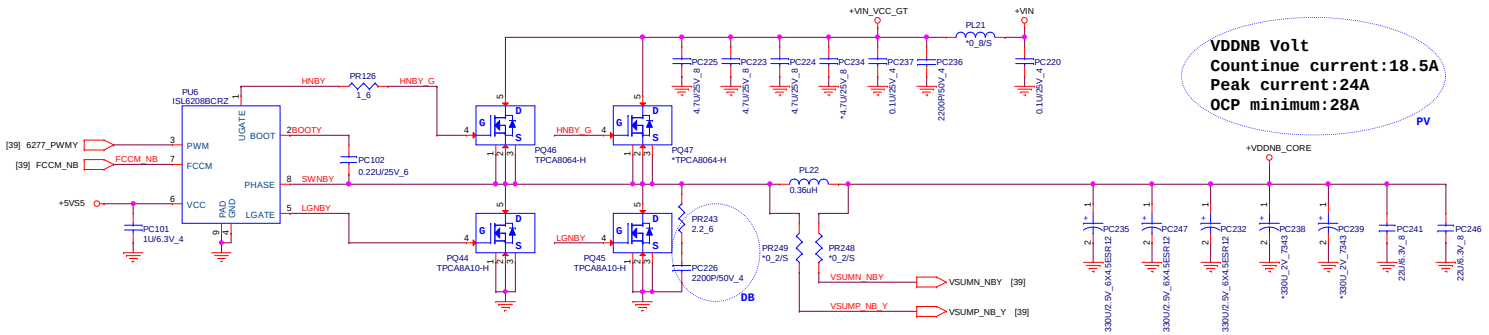
Size	Document Number	Rev
Custom	+1.8V_VGA (G5193)	1A

Date: Thursday, September 20, 2012 | Sheet 38 of 42



PROJECT : VOLKS_Comal 14"	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: ISL6277; Rev: 1A
Date: Thursday, September 20, 2012	Sheet 39 of 42



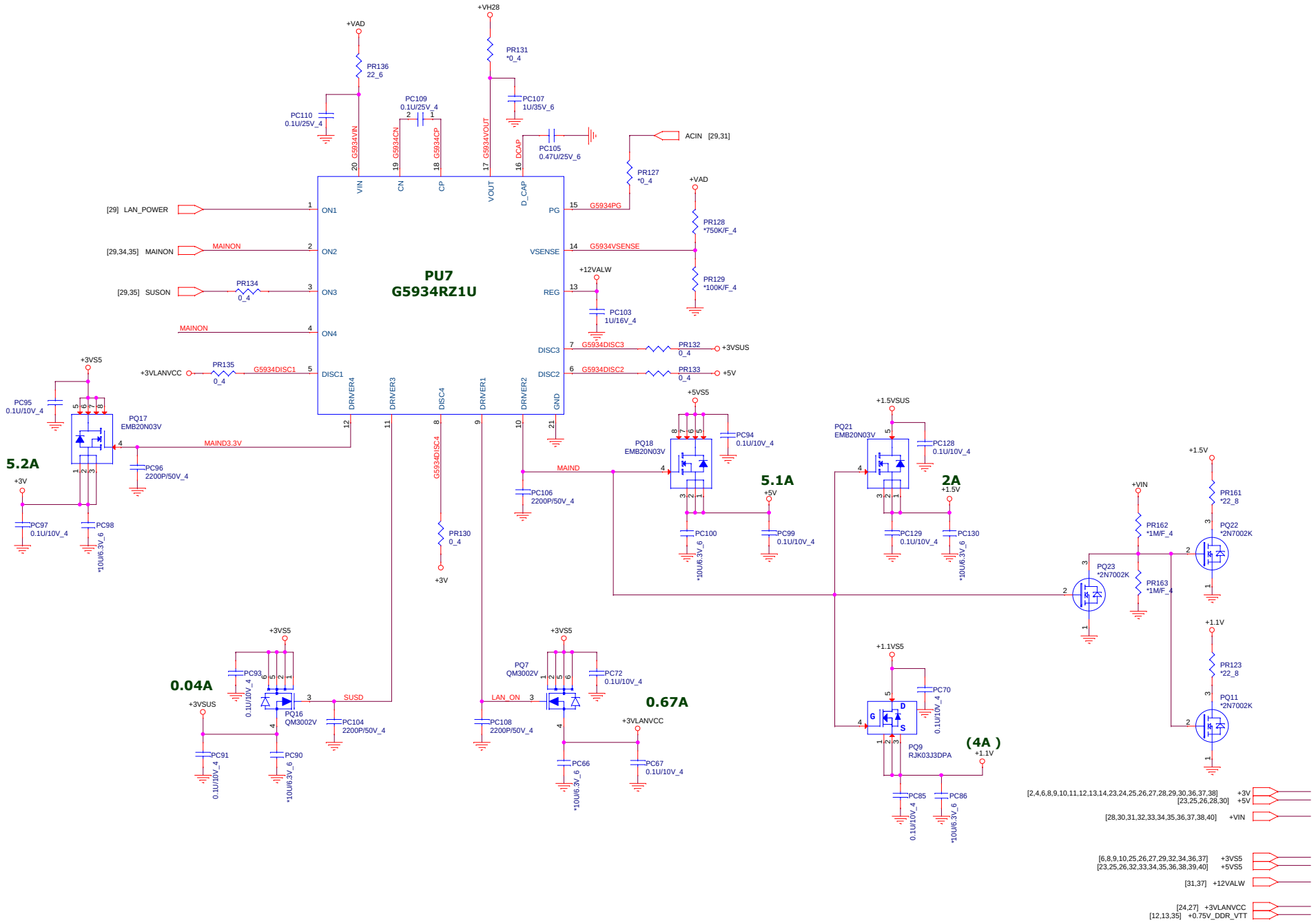


NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ISL6208	1A

Date: Thursday, September 20, 2012 | Sheet 40 of 42



NB5

PROJECT : VOLKS_Comal 14"

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448V)	1A

Date: Thursday, September 20, 2012 | Sheet 41 of 42

NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
C	History	1A

Date: Thursday, September 20, 2012 | Sheet 42 of 42