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REV

ECN

DESCRIPTION OF REVISION

CK APPD

DATE

2012-05-09

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, MLB, KEPLER, 2PHASE, D2

FSB, 5/9/2012

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01/13/2012

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9589	1	SCHEM,MLB, KEPLER_2PHASE,D2	SCM	CRITICAL	
820-3332	1	PCBP,MLB, KEPLER_2PHASE,D2	PCB	CRITICAL	

TITLE-MLB

ARMOREV-ARMOREV

SAFT_PRODUCTNAME Rev. 6 11:00:02 2012

SCHEM, MLB, KEPLER, 2PHASE, D2

Apple Inc.

051-9589

4.18.0

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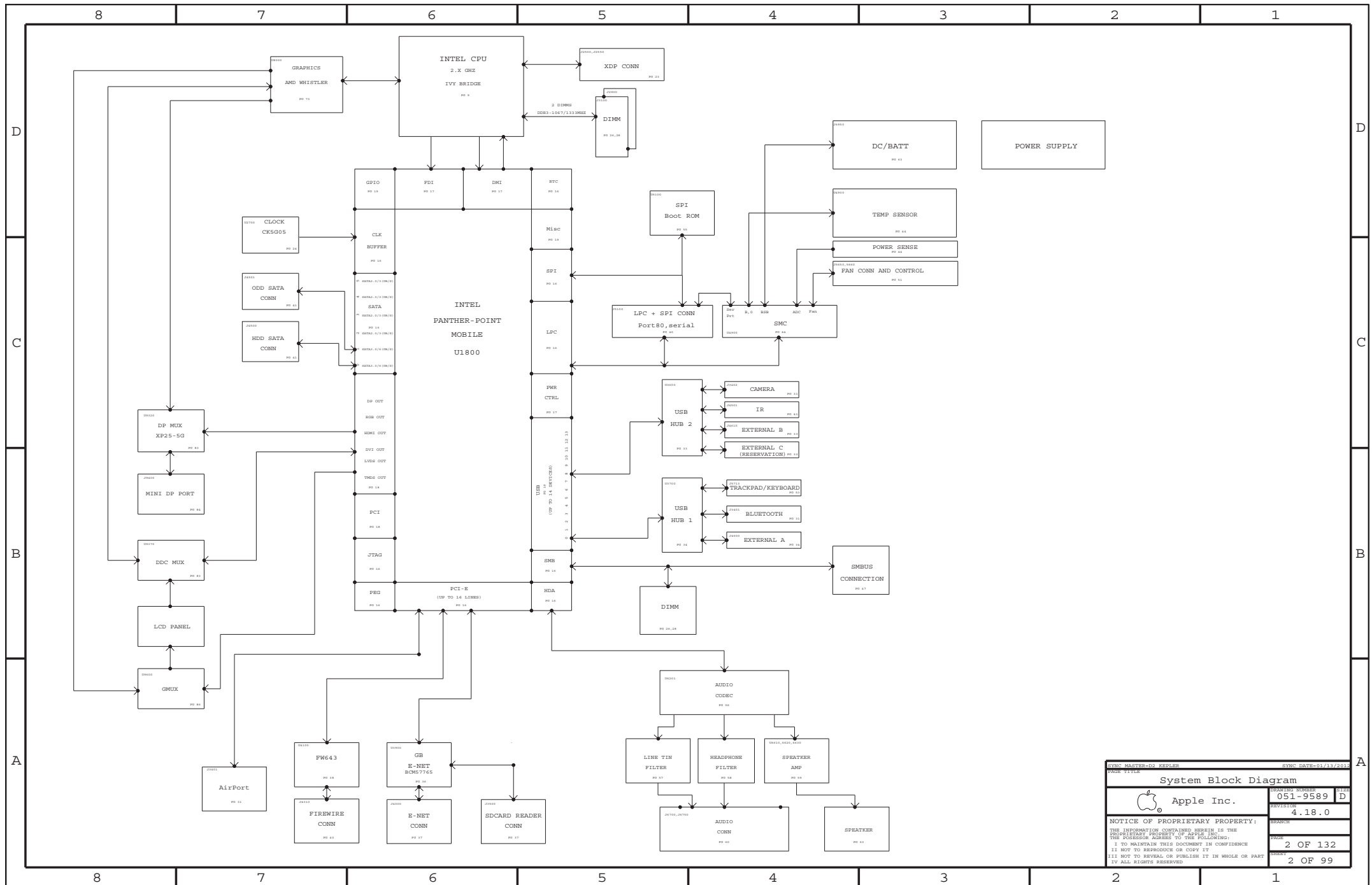
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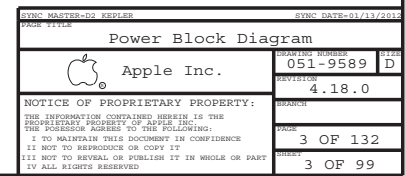
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SYSTEM MASTER-D3 REPLAC		SYNCH DATE: 01/11/2013	
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System Block Diagram			
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REVISION		4.18.0	
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A large empty rectangular area with a grid of 8 columns and 4 rows. The columns are labeled 1 through 8 from right to left at the top. The rows are labeled A through D from bottom to top on the left. The area is mostly empty, with a small table in the bottom right corner.

BPMC MASTER-D2 REDLINE		SYMC DATE-01/19/2012	
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 Apple Inc.		DRAWING NUMBER	051-9589
		REVISION	4.18.0
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BOM Variants (continued from CSA 5)

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3382	PCBA, 2.3G, 8G_ELP, VRAM_HYN, MLB_KEPLER, D2, DY41	BASE_BOM_CPU_IVY2_3GHZ, FR_3G_HYNIX_A_DIE, EEEE: DY41, DEVEL_BOM_RAM_3G_ELPIDA_1600
639-3383	PCBA, 2.3G, 8G_ELP, VRAM_SAM, MLB_KEPLER, D2, DY42	BASE_BOM_CPU_IVY2_3GHZ, FR_3G_SAMSUNG, EEEE: DY42, DEVEL_BOM_RAM_3G_ELPIDA_1600
639-3445	PCBA, 2.3G, 16G_ELP, VRAM_HYN, MLB_KEPLER, D2, DYJ5	BASE_BOM_CPU_IVY2_3GHZ, FR_3G_HYNIX_A_DIE, EEEE: DYJ5, DEVEL_BOM_RAM_4G_ELPIDA_1600
639-3446	PCBA, 2.3G, 16G_ELP, VRAM_SAM, MLB_KEPLER, D2, DYJ6	BASE_BOM_CPU_IVY2_3GHZ, FR_3G_SAMSUNG, EEEE: DYJ6, DEVEL_BOM_RAM_4G_ELPIDA_1600
639-2818	PCBA, 2.6G, 8G_ELP, VRAM_HYN, MLB_KEPLER, D2, DRF0	BASE_BOM_CPU_IVY2_6GHZ, FR_3G_HYNIX_A_DIE, EEEE: DRF0, DEVEL_BOM_RAM_3G_ELPIDA_1600
639-2820	PCBA, 2.6G, 8G_ELP, VRAM_SAM, MLB_KEPLER, D2, DRDP	BASE_BOM_CPU_IVY2_6GHZ, FR_3G_SAMSUNG, EEEE: DRDP, DEVEL_BOM_RAM_3G_ELPIDA_1600
639-2823	PCBA, 2.6G, 16G_ELP, VRAM_HYN, MLB_KEPLER, D2, DRDT	BASE_BOM_CPU_IVY2_6GHZ, FR_3G_HYNIX_A_DIE, EEEE: DRDT, DEVEL_BOM_RAM_4G_ELPIDA_1600
639-2819	PCBA, 2.6G, 16G_ELP, VRAM_SAM, MLB_KEPLER, D2, DRDQ	BASE_BOM_CPU_IVY2_6GHZ, FR_3G_SAMSUNG, EEEE: DRDQ, DEVEL_BOM_RAM_4G_ELPIDA_1600
639-3632	PCBA, 2.7G, 8G_ELP, VRAM_HYN, MLB_KEPLER, D2, FOJD	BASE_BOM_CPU_IVY2_7GHZ, FR_3G_HYNIX_A_DIE, EEEE: FOJD, DEVEL_BOM_RAM_3G_ELPIDA_1600
639-3633	PCBA, 2.7G, 8G_ELP, VRAM_SAM, MLB_KEPLER, D2, FOJ3	BASE_BOM_CPU_IVY2_7GHZ, FR_3G_SAMSUNG, EEEE: FOJ3, DEVEL_BOM_RAM_3G_ELPIDA_1600
639-3630	PCBA, 2.7G, 16G_ELP, VRAM_HYN, MLB_KEPLER, D2, FOJ4	BASE_BOM_CPU_IVY2_7GHZ, FR_3G_HYNIX_A_DIE, EEEE: FOJ4, DEVEL_BOM_RAM_4G_ELPIDA_1600
639-3631	PCBA, 2.7G, 16G_ELP, VRAM_SAM, MLB_KEPLER, D2, FOJC	BASE_BOM_CPU_IVY2_7GHZ, FR_3G_SAMSUNG, EEEE: FOJC, DEVEL_BOM_RAM_4G_ELPIDA_1600

Bar Code Labels / EEEE #'s (continued from CSA 5)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL_MLB/110_MBA	[EEEE: DY41]	CRITICAL	EEEE: DY41
825-7563	1	LABEL_MLB/110_MBA	[EEEE: DY42]	CRITICAL	EEEE: DY42
825-7563	1	LABEL_MLB/110_MBA	[EEEE: DYJ5]	CRITICAL	EEEE: DYJ5
825-7563	1	LABEL_MLB/110_MBA	[EEEE: DYJ6]	CRITICAL	EEEE: DYJ6
825-7563	1	LABEL_MLB/110_MBA	[EEEE: DRF0]	CRITICAL	EEEE: DRF0
825-7563	1	LABEL_MLB/110_MBA	[EEEE: DRDP]	CRITICAL	EEEE: DRDP
825-7563	1	LABEL_MLB/110_MBA	[EEEE: DRDT]	CRITICAL	EEEE: DRDT
825-7563	1	LABEL_MLB/110_MBA	[EEEE: DRDQ]	CRITICAL	EEEE: DRDQ
825-7563	1	LABEL_MLB/110_MBA	[EEEE: FOJD]	CRITICAL	EEEE: FOJD
825-7563	1	LABEL_MLB/110_MBA	[EEEE: FOJ3]	CRITICAL	EEEE: FOJ3
825-7563	1	LABEL_MLB/110_MBA	[EEEE: FOJ4]	CRITICAL	EEEE: FOJ4
825-7563	1	LABEL_MLB/110_MBA	[EEEE: FOJC]	CRITICAL	EEEE: FOJC

Elipda DQ'd
Keeping for PRQ

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BOM Variants

Apple Inc.

051-9589

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NO_TEST NC NO_TESTS

TRUE	NC_SMC_FAN_3_TACH
TRUE	NC_SMC_FAN_3_CTL
TRUE	NC_SMC_FAN_2_TACH
TRUE	NC_SMC_FAN_2_CTL
TRUE	NC_FW2_TPRP
TRUE	NC_FW2_TPRN
TRUE	NC_FW2_TPRIAS
TRUE	NC_FW2_TPRP
TRUE	NC_FW2_TPRN

```

7F00H    NC FWD TERN
7F01H    NC FWD TEAP
7F02H    NC ESTARLDO EN
7F03H    NC ALS GAIN
7F04H    NC USB HUB FRTPMR2
7F05H    NC USB HUB FRTPMR3
7F06H    NC USB HUB FRTPMR4
7F07H    NC USB HUB OCS2
7F08H    NC USB HUB OCS3
7F09H    NC USB HUB OCS4
7F0AH    NC SMC KOEC1
7F0BH    NC SMC_ODD_DETECT

```

7F012E	NC_SMC_S1B_LED
7F012F	NC_SMC_HIB_L
7F0130	NC_SMBUS_SMC_4_ASF_SDA
7F0131	NC_SMBUS_SMC_4_ASF_SCL
7F0132	NC_SMC_T25_EN_L
7F0133	NC_SMC_T25_ISENSE
7F0134	NC_I2S0_R1V1V25_CENDDR

TRUE	NC ISNS P155R1V35 CPUDDN
TRUE	NC ISNS LCDBKLT
TRUE	NC ISNS LCDBKLTN
TRUE	NC ISNS LCD PANELP
TRUE	NC ISNS LCD PANELN
TRUE	NC ISNS AIRPORTP

```
DMI_CBC == TRUE NC_HDMI_C
== MAKE_BASE-TRUE

C_HPD == TRUE NC_DP_IG_C_H
== MAKE_BASE-TRUE
C_CTRL_CLK == TRUE NC_DP_IG_C
```

```
C CTRL DATA      == TRUE          NC DP IG C M
C MLP<3..0>      == MAKE_BASE-TRUE   NC DP IG C M
                  == TRUE            NC DP IG C M
C MLP<3..0>      == MAKE_BASE-TRUE   NC DP IG C M
                  == TRUE            NC DP IG C M
C AUXP           == MAKE_BASE-TRUE   NC DP IG C A
                  == TRUE            NC DP IG C A
C AUXN           == MAKE_BASE-TRUE   NC DP IG C A
                  == TRUE            NC DP IG C A
D HPD            == TRUE             NC DP IG D H
```

D CTRL DATA	=====	NAKE BASE-TRUE	NC DP IG D C
D MLP<3..0>	=====	NAKE BASE-TRUE	NC DP IG D M
D MLN<3..0>	=====	NAKE BASE-TRUE	NC DP IG D M
D AUXP	=====	NAKE BASE-TRUE	NC DP IG D A
D AUXN	=====	NAKE BASE-TRUE	NC DP IG D A
	=====	NAKE BASE-TRUE	

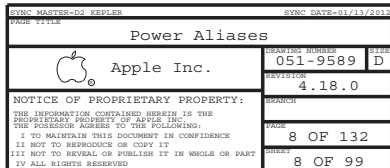
TVCLKINN	TRUE	NC	SDVO	T
TVCLKINP	MAKE BASE=TRUE	NC	SDVO	T
STALIN	TRUE	NC	SDVO	S
STALLP	MAKE BASE=TRUE	NC	SDVO	S
INTN	TRUE	NC	SDVO	I
CAESAR	MAKE BASE=TRUE	MC	CMAC	

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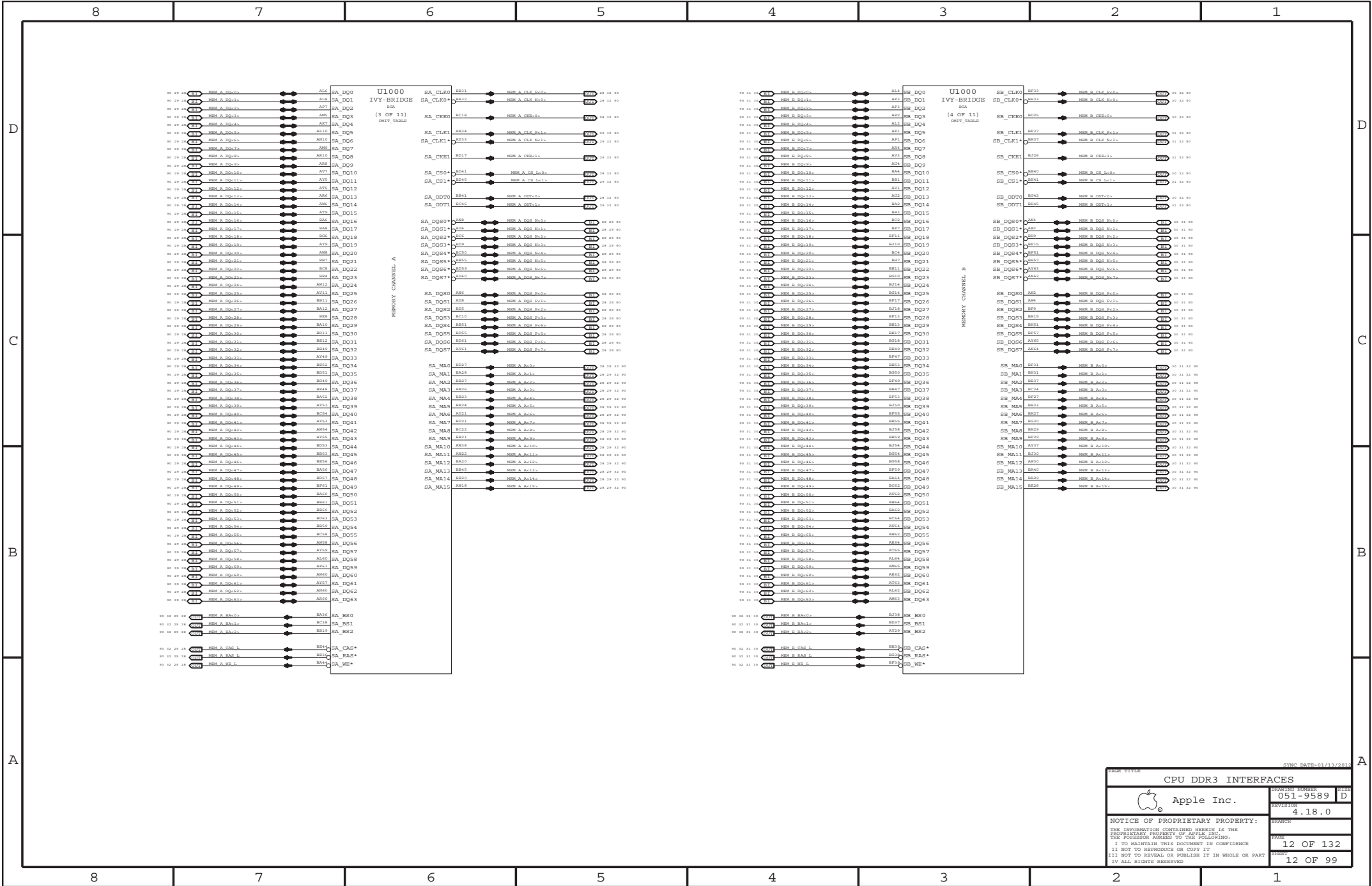
===== MAKE_BASE=TRUE
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PU GSTATE<0>      ===== MAKE_BASE=TRUE  NC GPU GS
PU GSTATE<1>      ===== TRUE      NC GPU GS
PU MIOA D<9..0>   ===== MAKE_BASE=TRUE  NC GPU MI
PU MIOA DE         ===== MAKE_BASE=TRUE  NC GPU MI
===== MAKE_BASE=TRUE

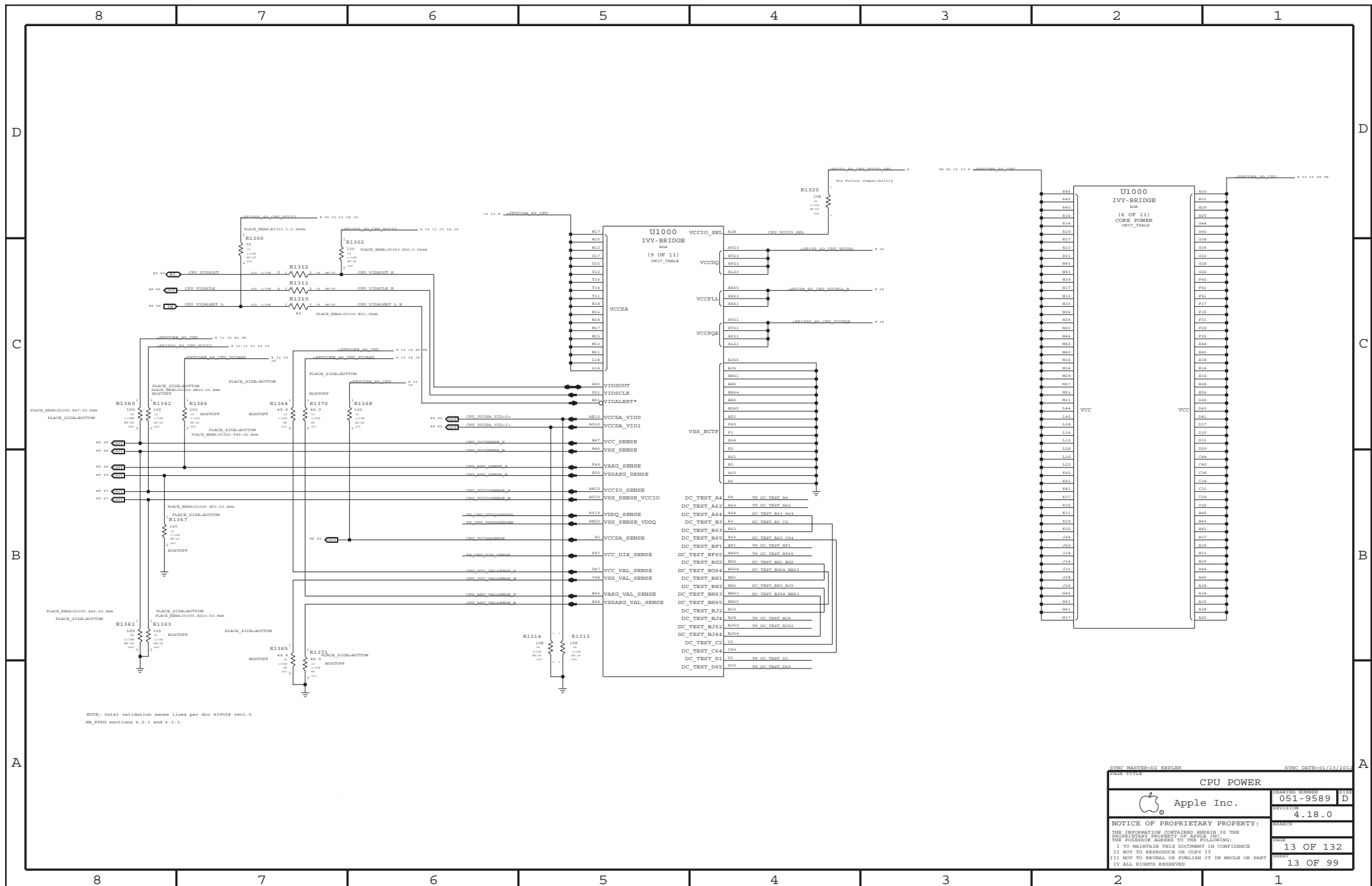
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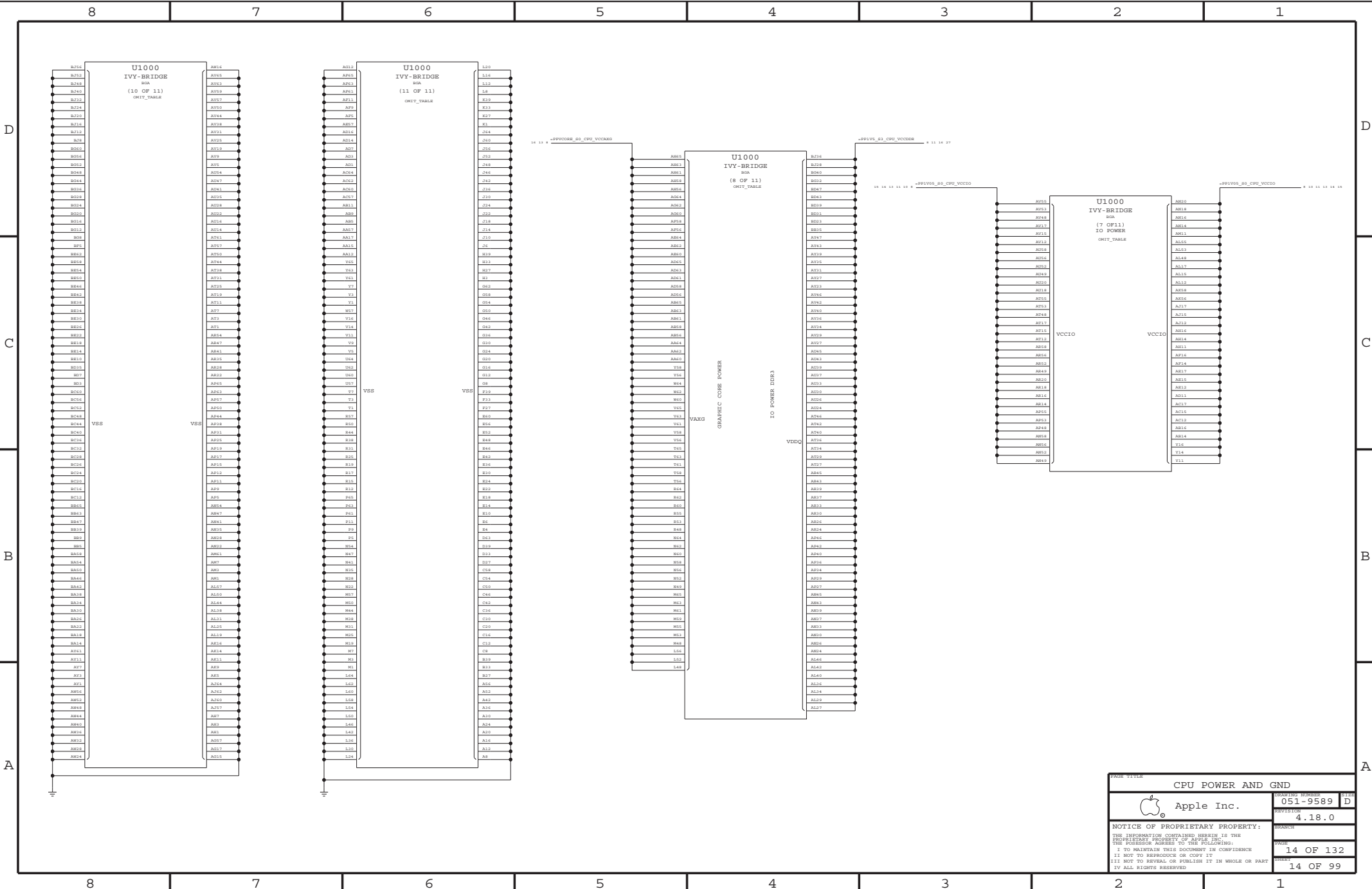
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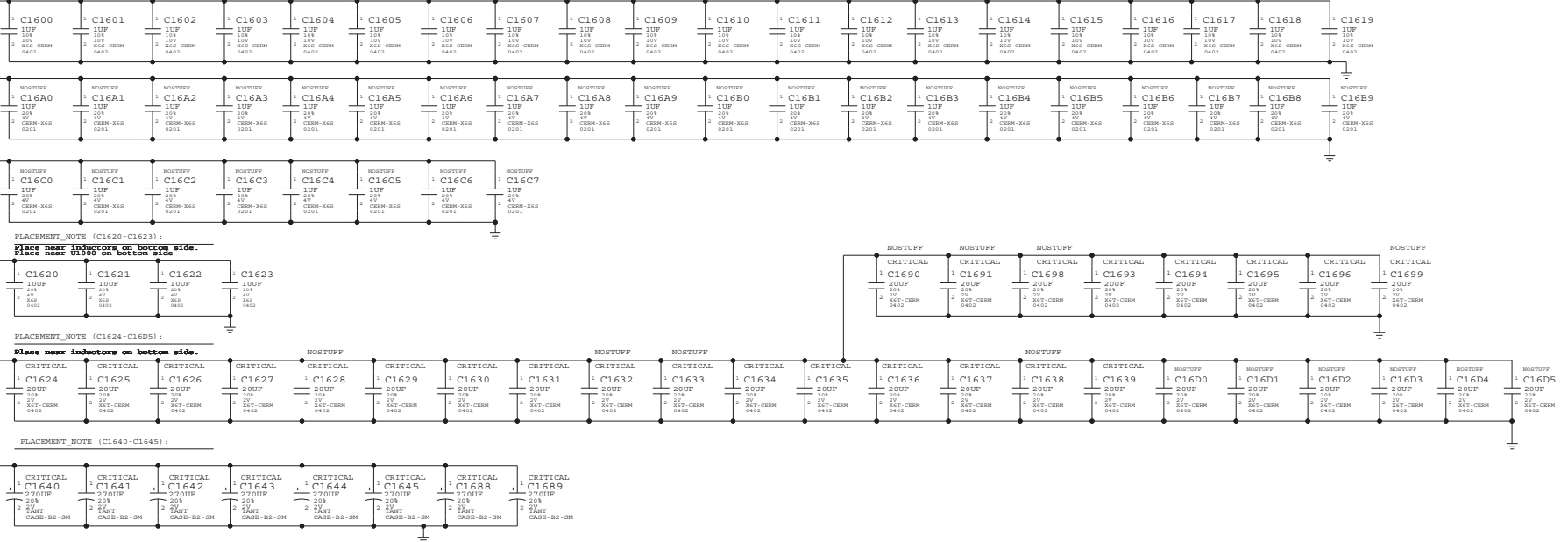


CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 8x 270uF 6mOhm, 0x 470uF 4mOhm, 16x 22uF 0402, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0402 (NOSTUFF)

PLACEMENT_NOTE (C1600-C1671):

Place on bottom side of U1000

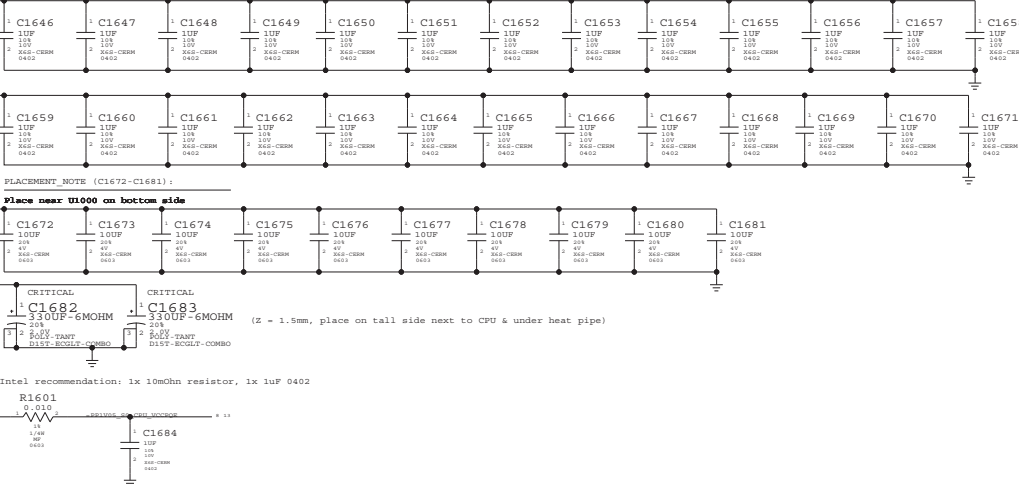


CPU VCCIO/VCCPQ DECOUPLING

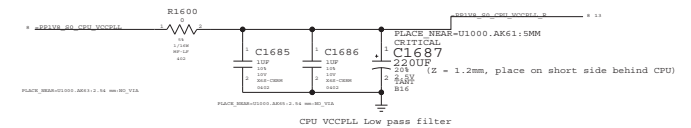
Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):

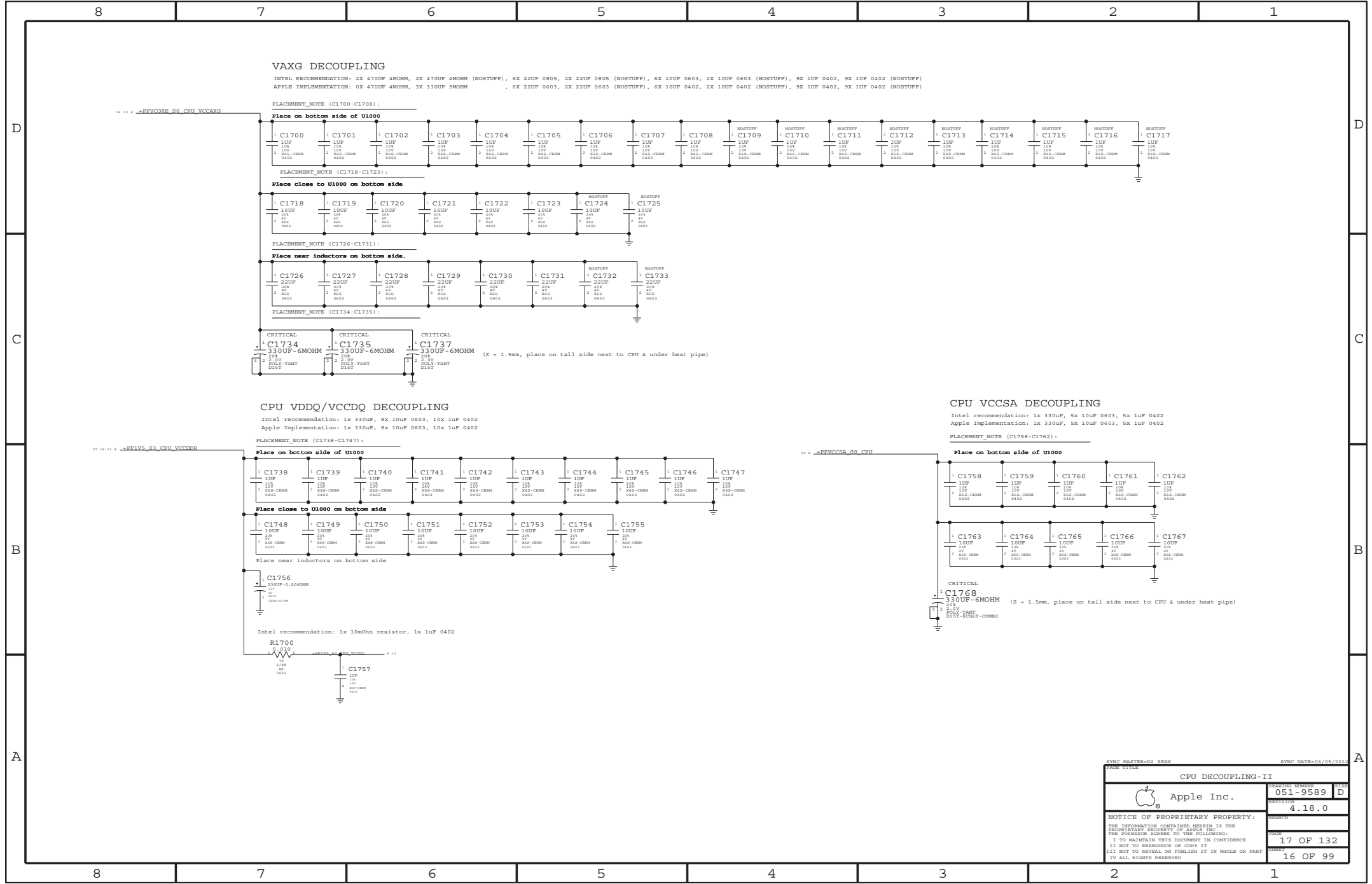
Place on bottom side of U1000

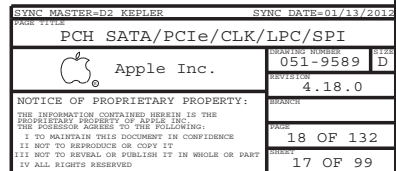


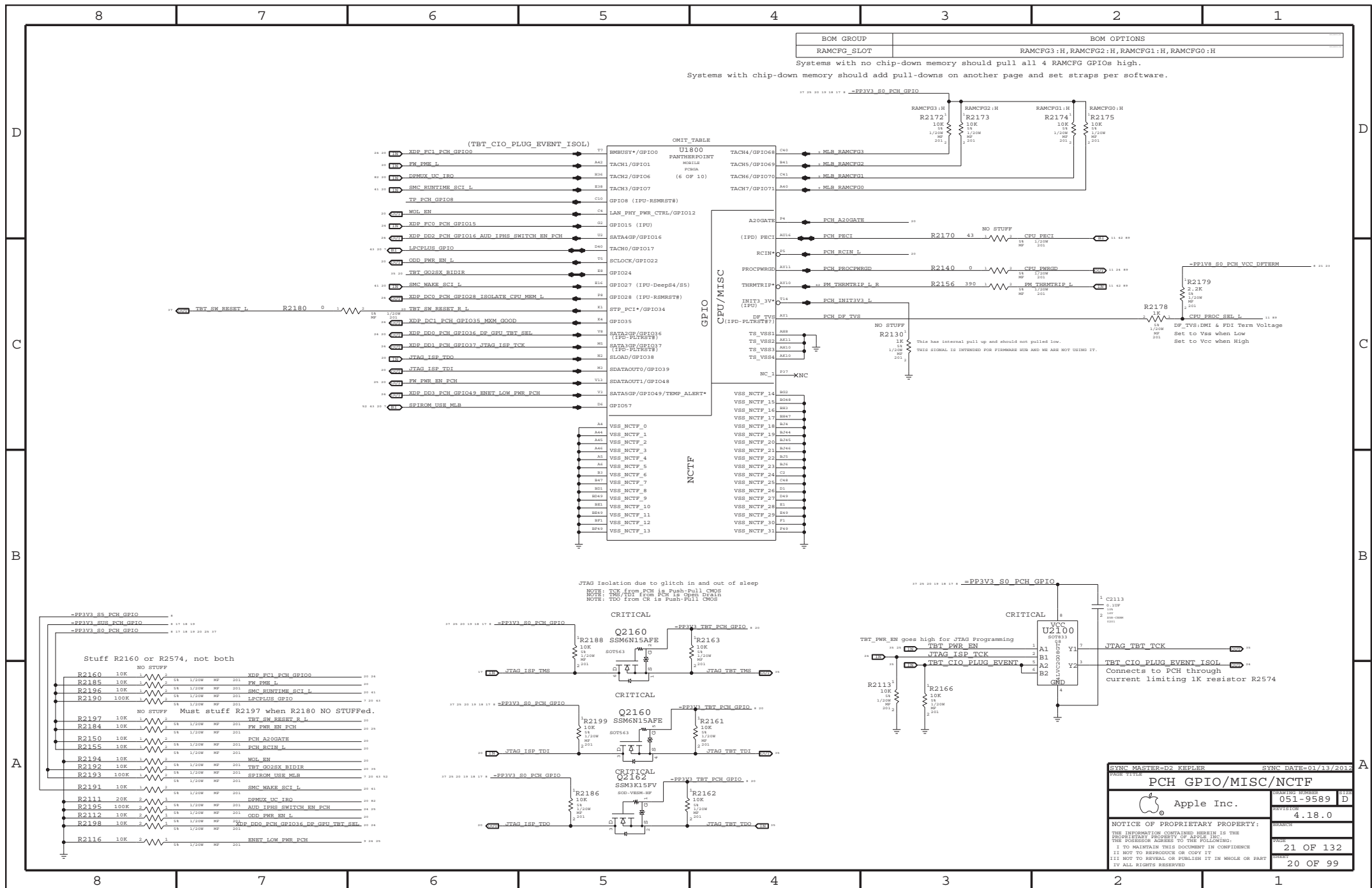
CPU VCCPLL DECOUPLING



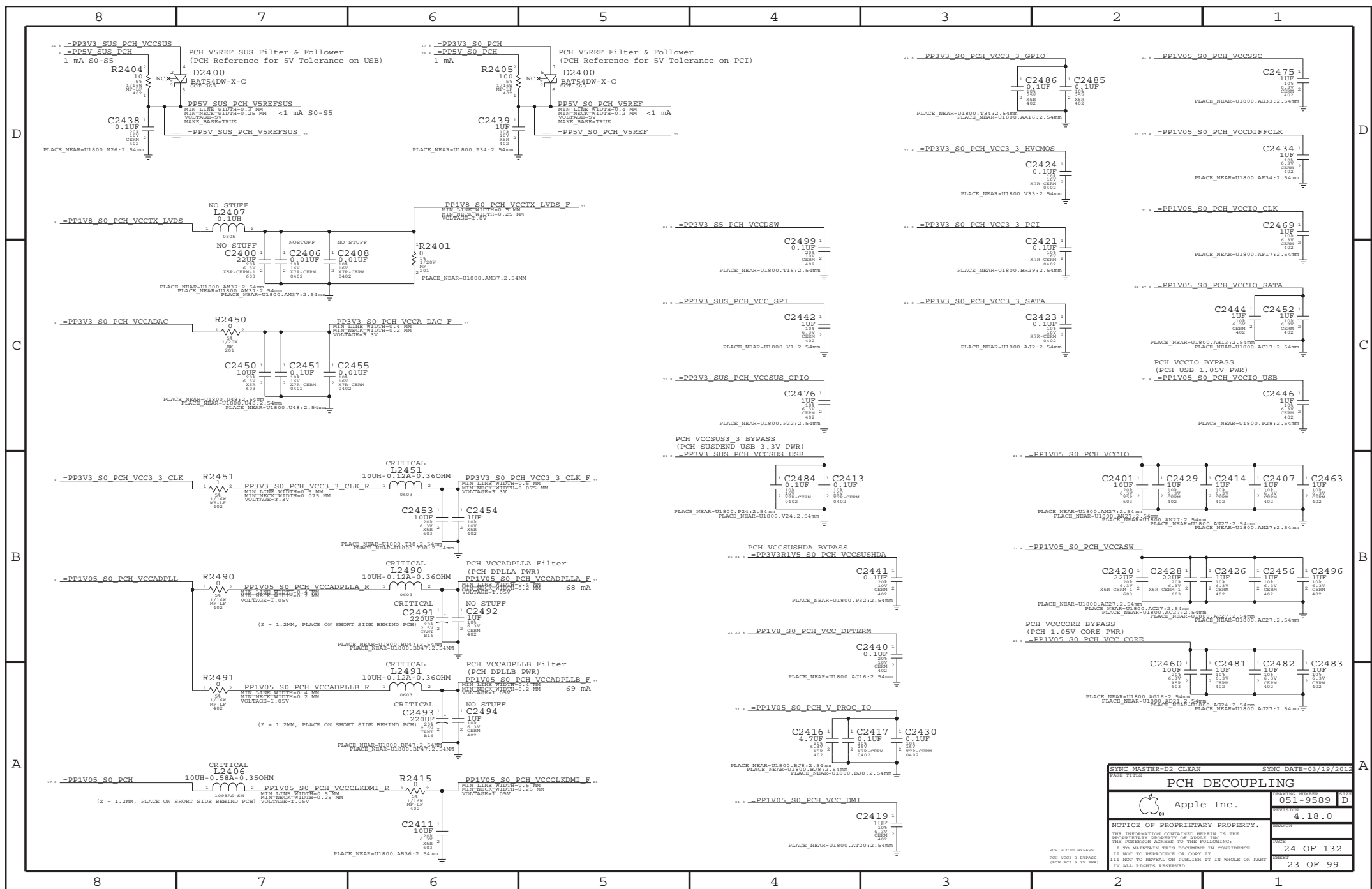
SYNCH MASTER-D2 REAN		SYNCH DATE-01/05/2013	
PAGE TITLE		CPU DECOUPLING-1	
Apple Inc.		DESIGN NUMBER	051-9589 D
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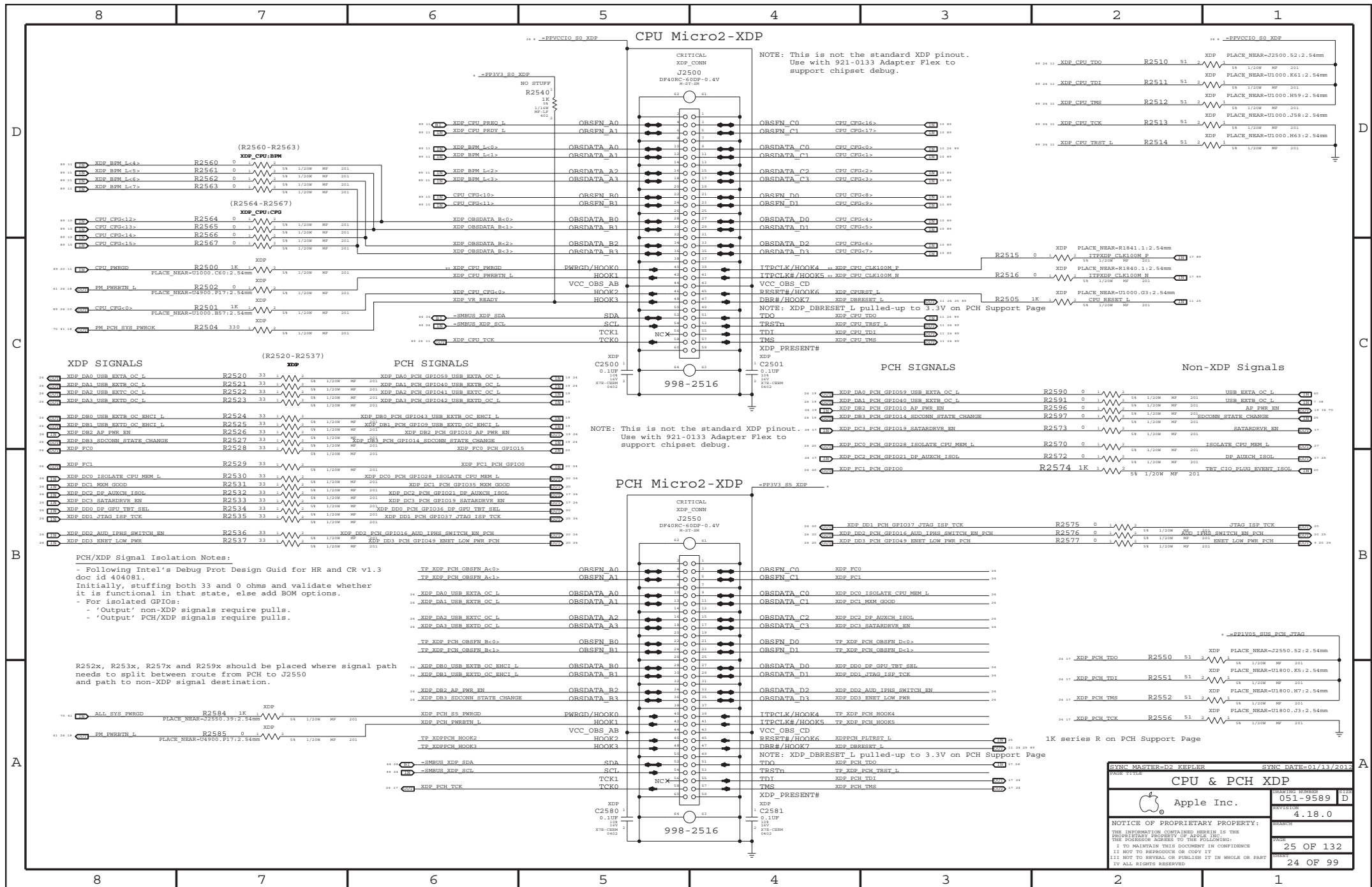




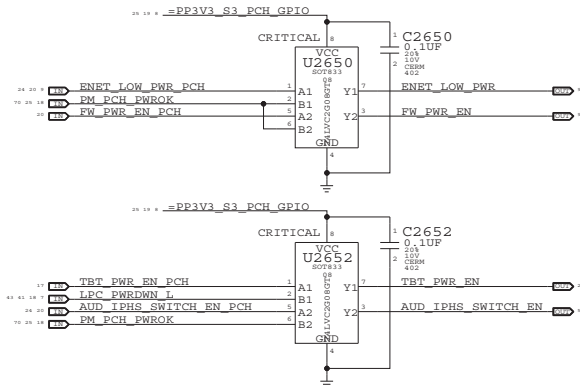


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			OMIT TABLE			OMIT TABLE			
			H5 VSS U1800			AY4 VSS U1800			
			AA17 VSS PANTHERPOINT			AY42 VSS PANTHERPOINT			
			AA2 VSS MOBILE			AY46 VSS MOBILE			
			AA3 VSS PCBGA			AY8 VSS PCBGA			
			AA13 VSS (9 OF 10)			B11 VSS (10 OF 10)			
			AA34 VSS VSS			B15 VSS VSS			
			AB11 VSS			B19 VSS			
			AB14 VSS			B23 VSS			
			AB39 VSS			B27 VSS			
			AB4 VSS			B31 VSS			
			AB43 VSS			B35 VSS			
			AB5 VSS			B39 VSS			
			AB7 VSS			B7 VSS			
			AC19 VSS			F45 VSS			
			AC2 VSS			BB12 VSS			
			AC21 VSS			BB16 VSS			
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			AD8 VSS			BE40 VSS			
			AE2 VSS			BF10 VSS			
			AE3 VSS			BF12 VSS			
			AP10 VSS			BF16 VSS			
			AP12 VSS			BF20 VSS			
			AD14 VSS			BF22 VSS			
			AD16 VSS			BF24 VSS			
			AP16 VSS			BF26 VSS			
			AP19 VSS			BF28 VSS			
			AP24 VSS			BD3 VSS			
			AP26 VSS			BF30 VSS			
			AF27 VSS			BF38 VSS			
			AP29 VSS			BF40 VSS			
			AP31 VSS			BF8 VSS			
			AP38 VSS			BG17 VSS			
			AP4 VSS			BG21 VSS			
			AF42 VSS			BG23 VSS			
			AP46 VSS			BG44 VSS			
			AP5 VSS			BG8 VSS			
			AF7 VSS			BH11 VSS			
			AF8 VSS			BH15 VSS			
			AG19 VSS			BH17 VSS			
			AG2 VSS			BH19 VSS			
			AG11 VSS			H10 VSS			
			AG48 VSS			BH27 VSS			
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			AK71 VSS			H34 VSS			
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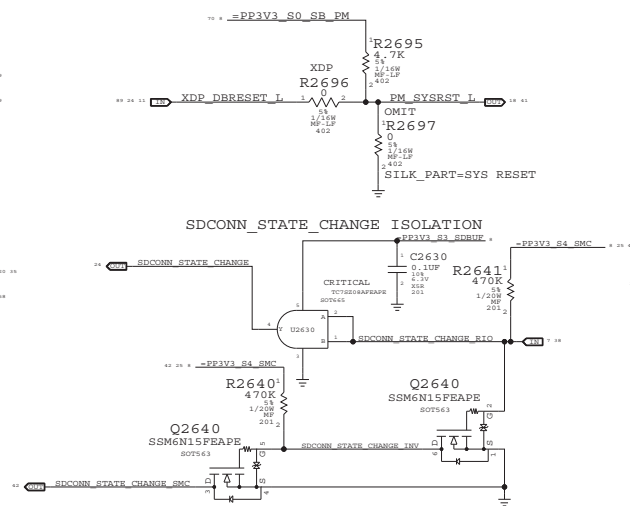




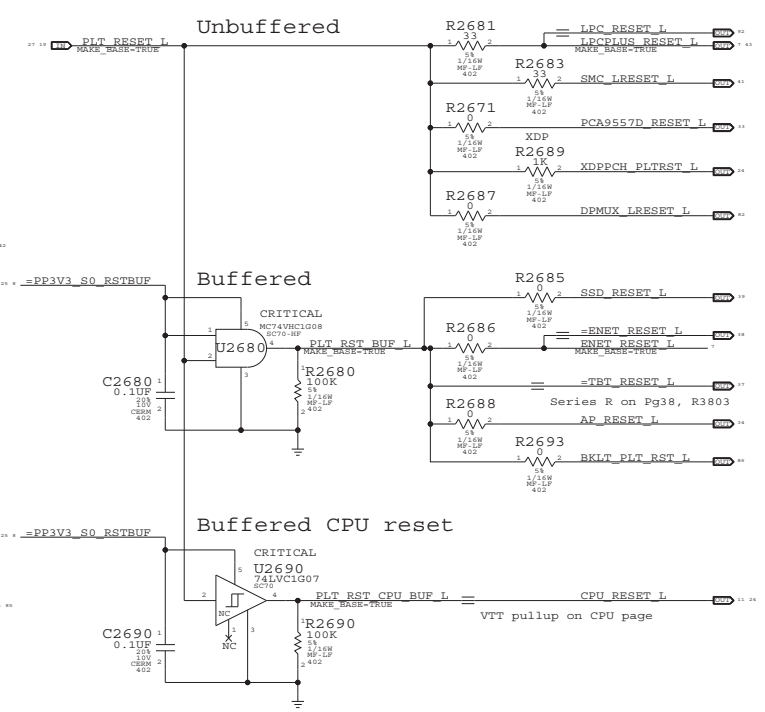
GPIO Glitch Prevention



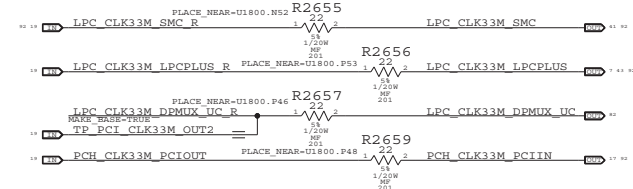
PCH Reset Button



Platform Reset Connections



LPC 33MHz Clock Series Termination

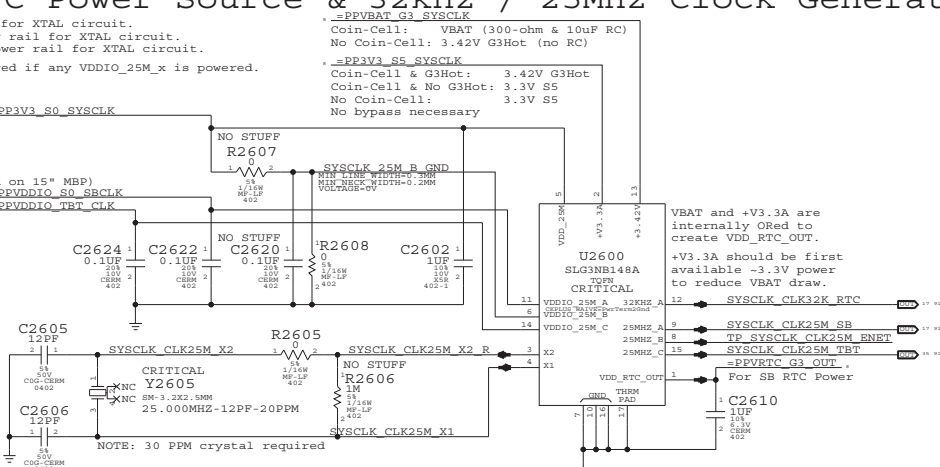


System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.
NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

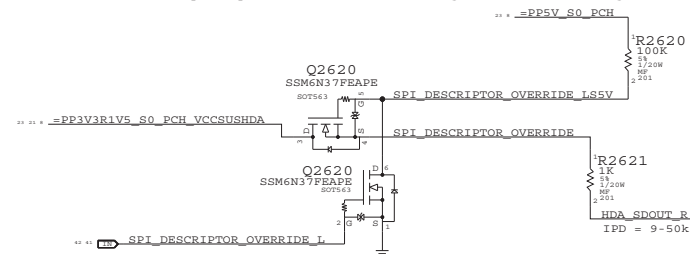
GreenClk 25MHz Power = PP3V3_S0_SYSCLK

Ethernet XTAL Power (Unused on 15" MBP) = PPVDDIO_S0_SBCLK
SB XTAL Power = PPVDDIO_TBT_CLK



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC MASTER=D2 KEPI-ER		SYNC DATE=01/13/2012	
PAGE TITLE		Chipset Support	
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USB MUX FOR LS/FS INTERNAL DEVICES

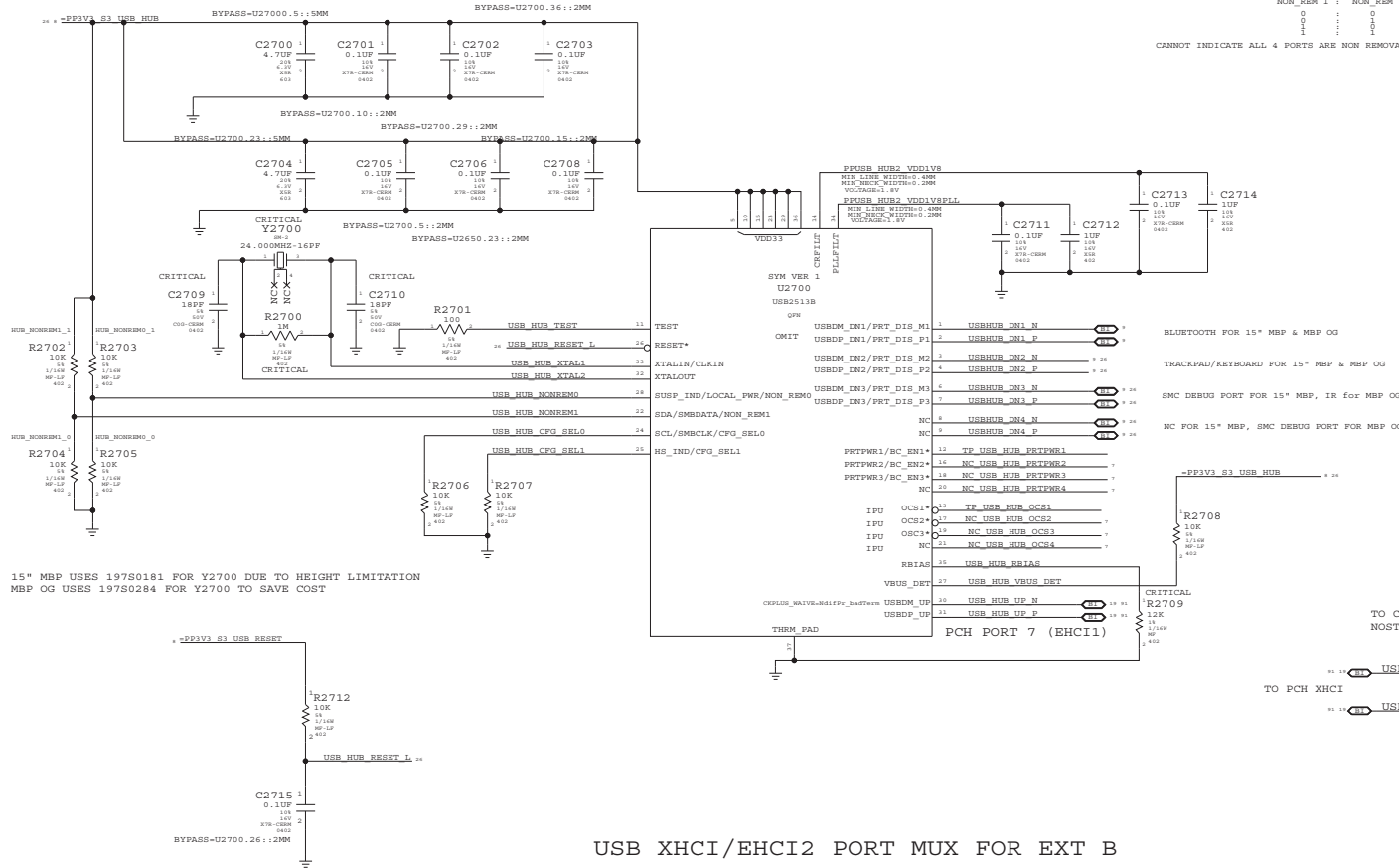
BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

NON_REM 1 : NON_REM 0 STRAP PIN CFG
 0 1 0 1
 1 0 1 0
 1 1 1 1
 1 0 0 0
 CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STAPPPING, PROGRAM NON_REMOVABLE_DEVICE_REGISTER_09H

BOM TABLE

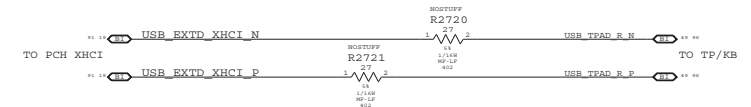
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
31680824	1	USB MUX 2514B	U2700	CRITICAL	USBHUB2514B
31680923	1	USB MUX 2513B	U2700	CRITICAL	USBHUB2513B
31680983	1	USB MUX 2512B	U2700	CRITICAL	USBHUB2512B

15" MBP ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
 MBP OG ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B

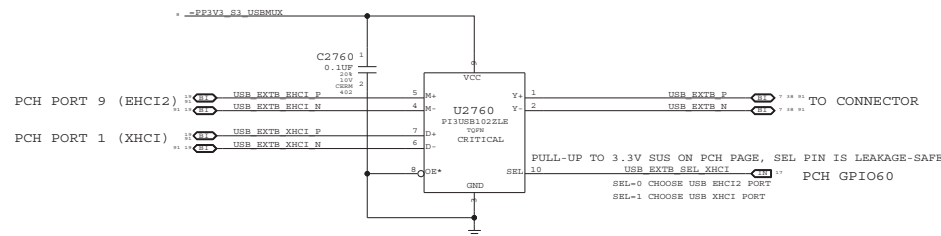


15" MBP USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
 MBP OG USES 197S0284 FOR Y2700 TO SAVE COST

TO CONNECT TP/KB TO PCH XHCI
 NOSTUFF R5701 & R5702, STUFF R2720 & R2721



USB XHCI/EHCI2 PORT MUX FOR EXT B



SYNC MASTER=D2 KEPI-ER	SYNC DATE=01/13/2012
PAGE TITLE	USB HUB & MUX
Apple Inc.	051-9589
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.

WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

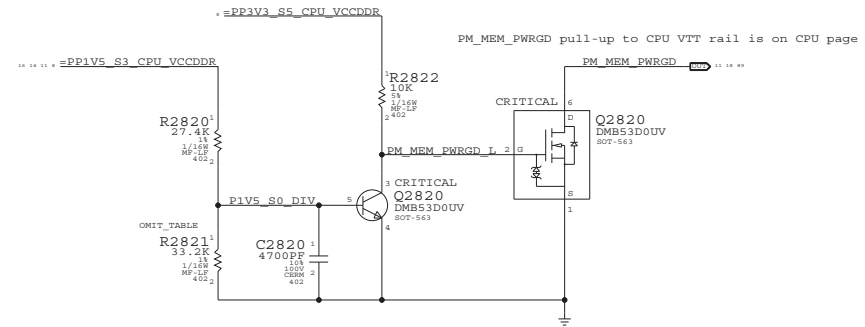
$$P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L$$

$$MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L$$

$$MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L$$

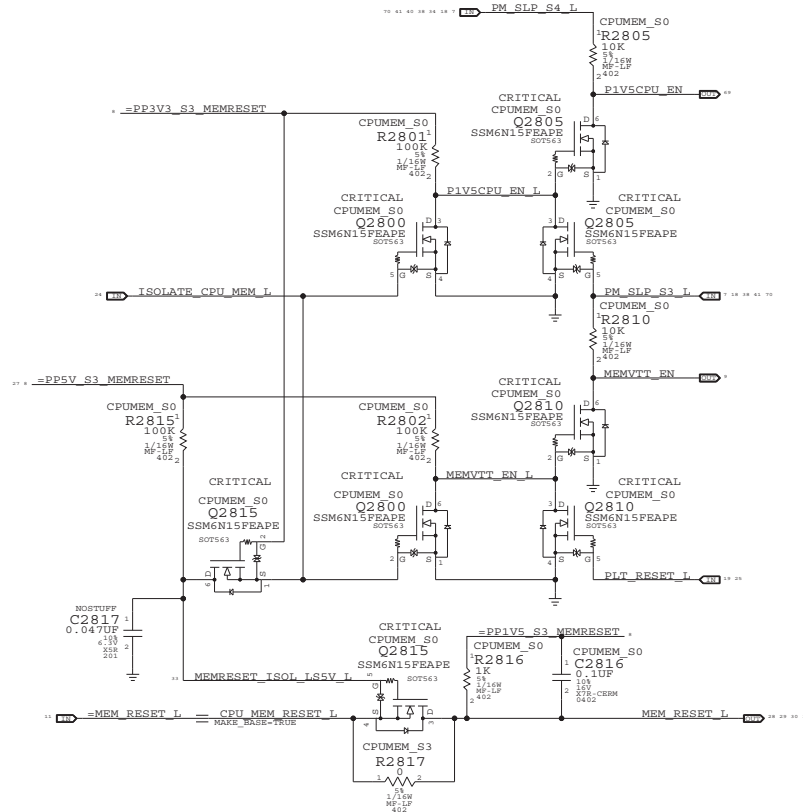
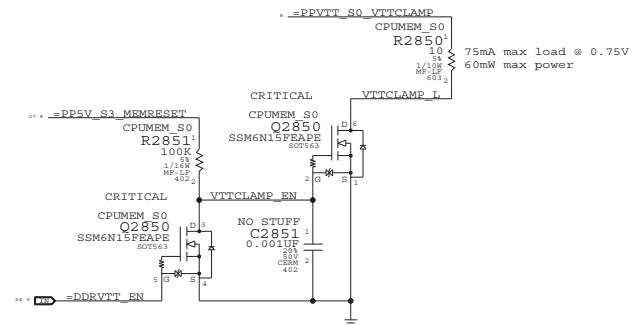
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11480165	1	PMU, MFL, P10M, 1.2V/0.45, 10, 10, 1, 1000, 000, 00	R2821		PPDDR:1V5
11480376	1	PMU, MFL, P10M, 1.2V/0.45, 10, 10, 1, 1000, 000, 00	R2821		PPDDR:1V35

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3

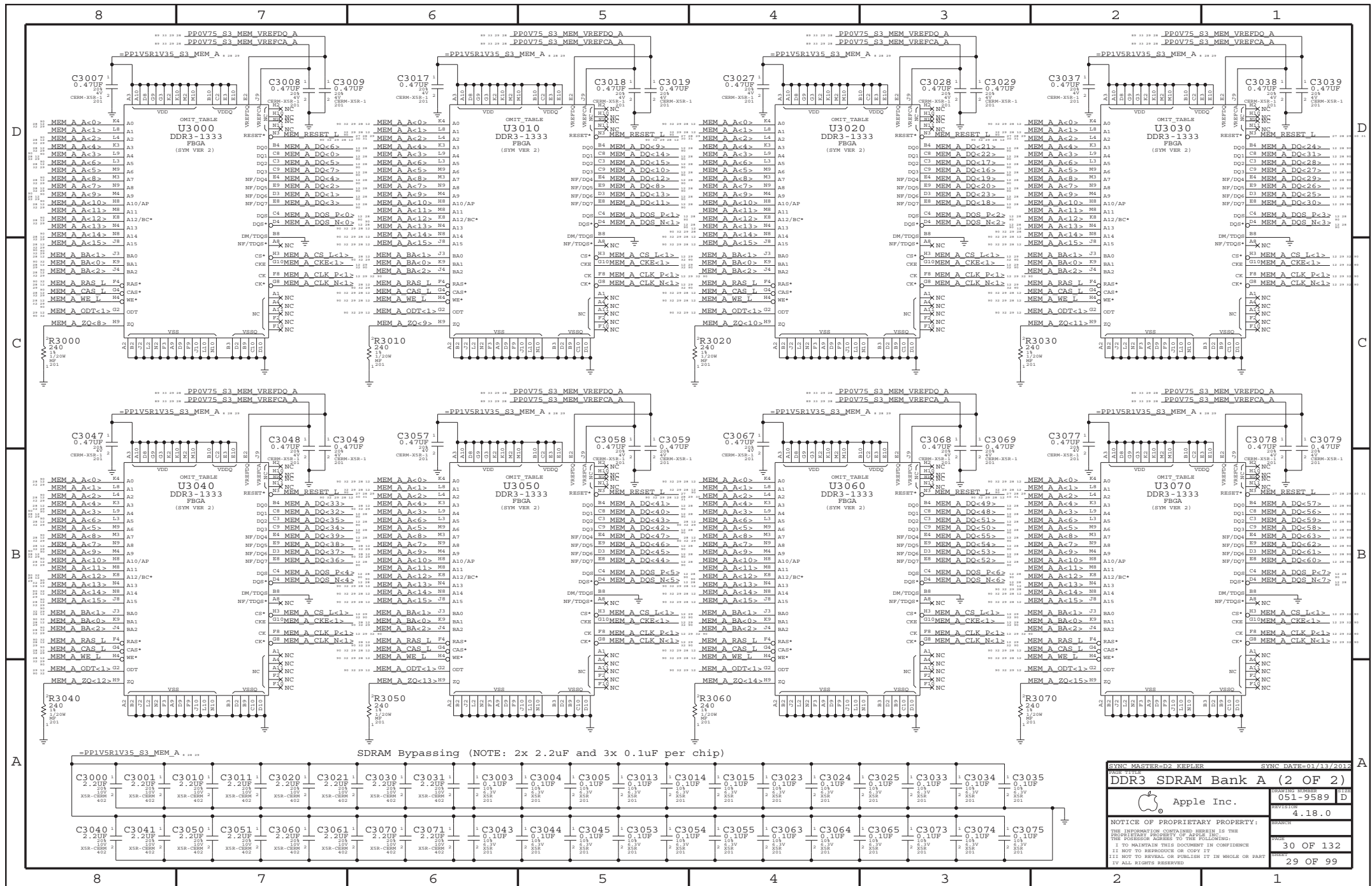


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
S3	1	1	1	1	1	1	1	1
S0	0	0	1	1	1	1	0	1
S3	0	0	0	1	1	1	0	0
S0	0	0	1	1	1	1	0	1
S3	0	1	1	1	1	1	1	1
S0	1	1	1	1	1	1	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE		CPU Memory S3 Support	
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DDR3 SDRAM Bank A (2 OF 2)

Apple Inc.

051-9589 D

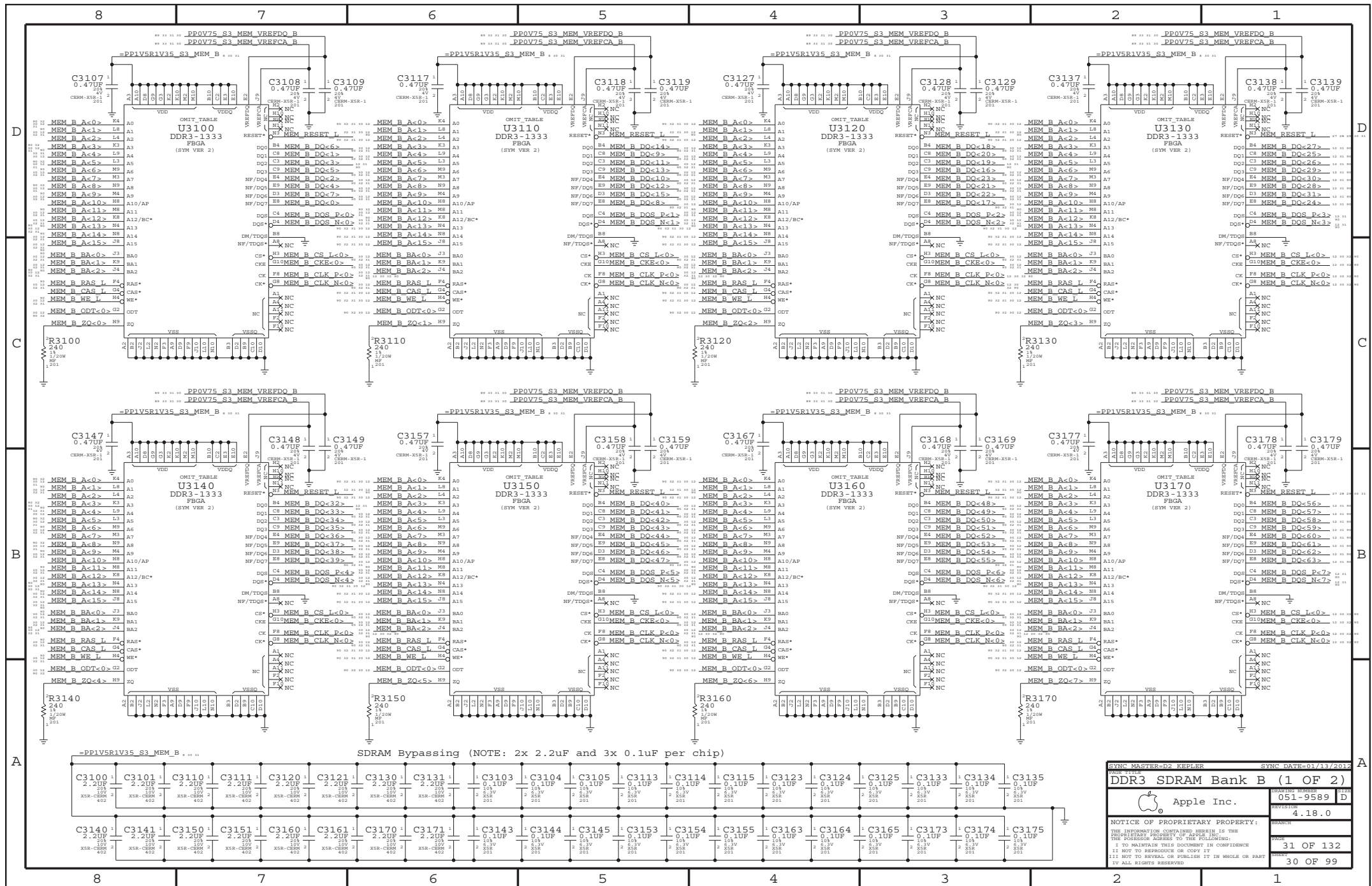
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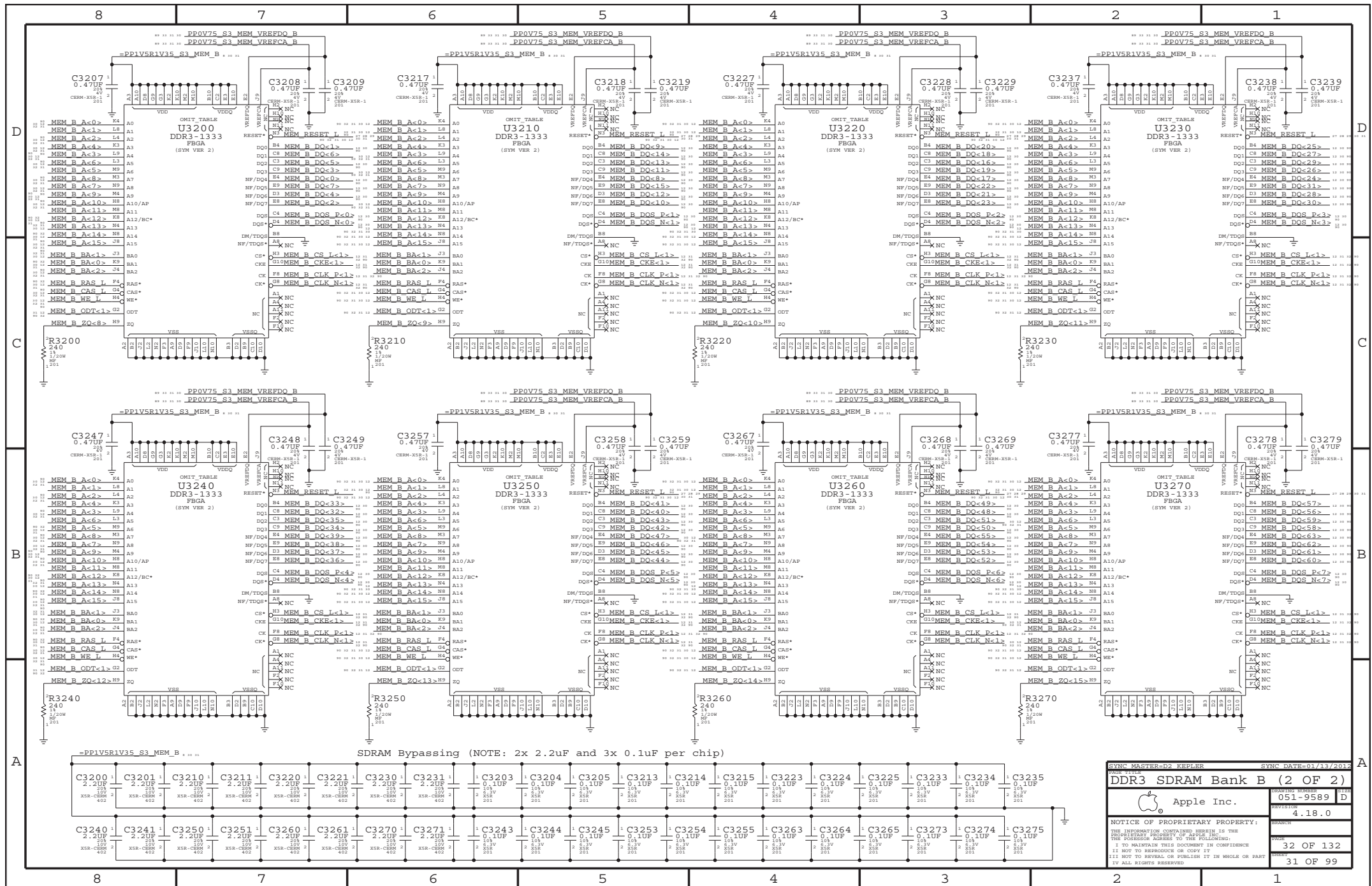
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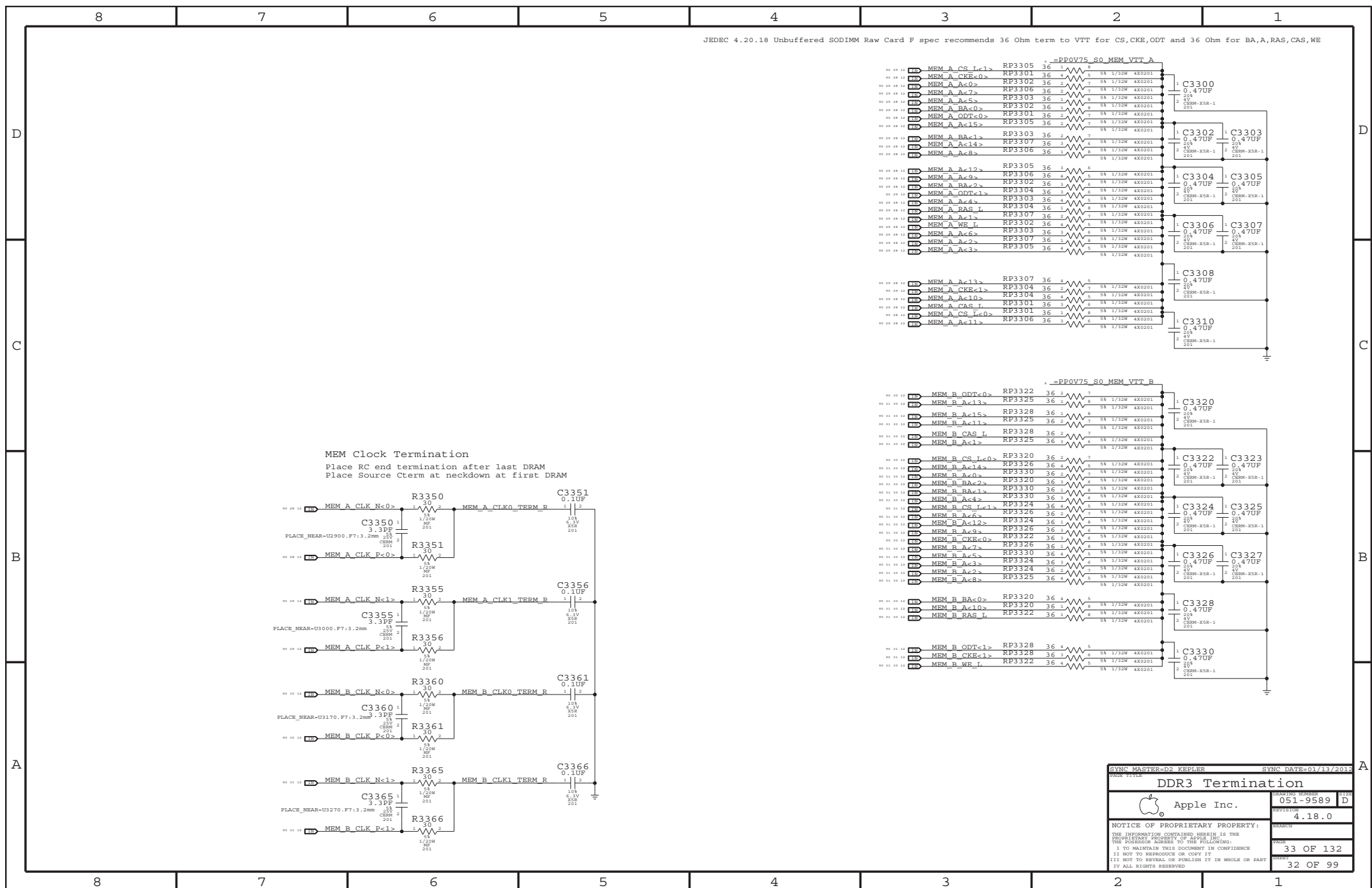
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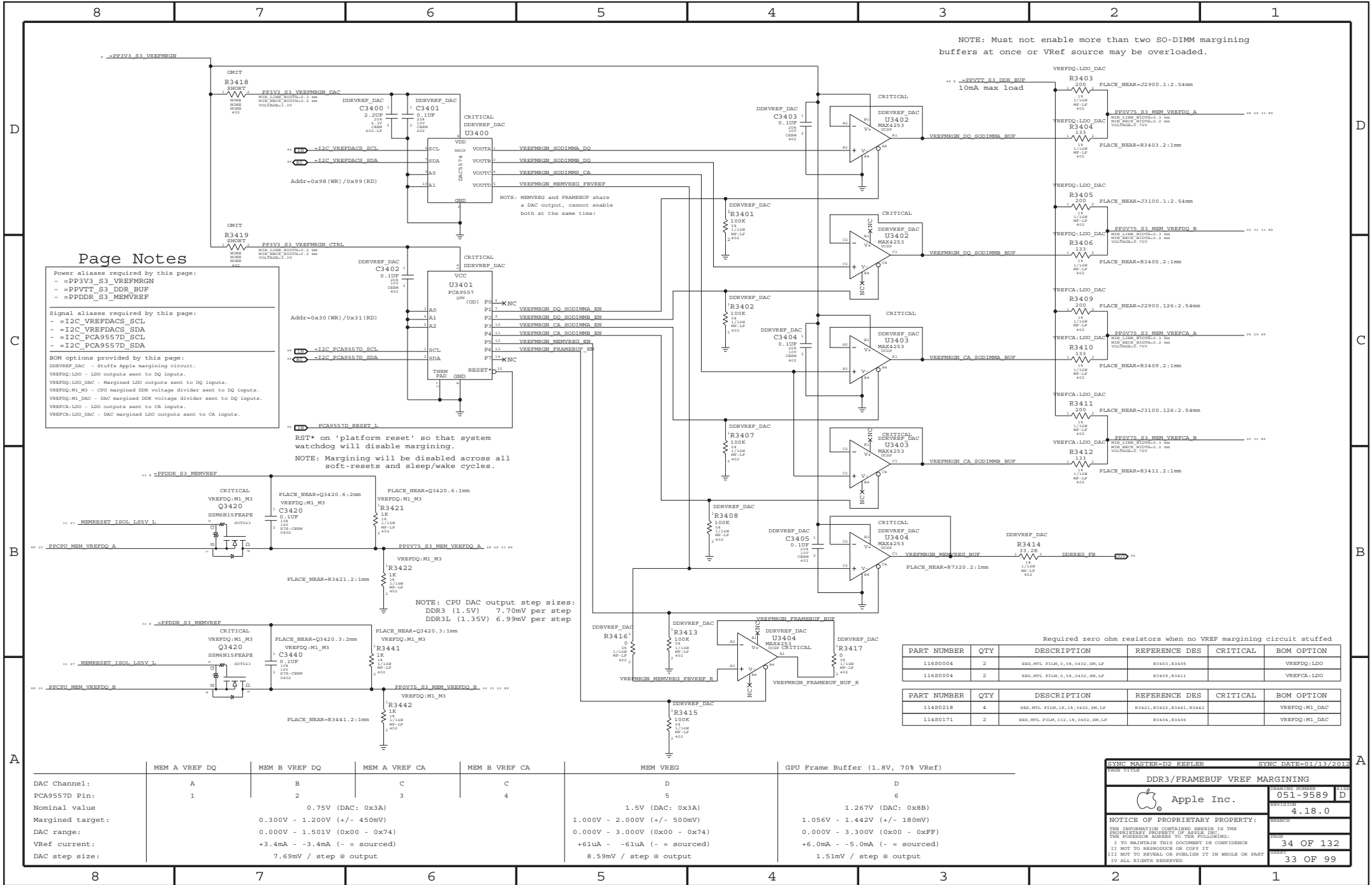
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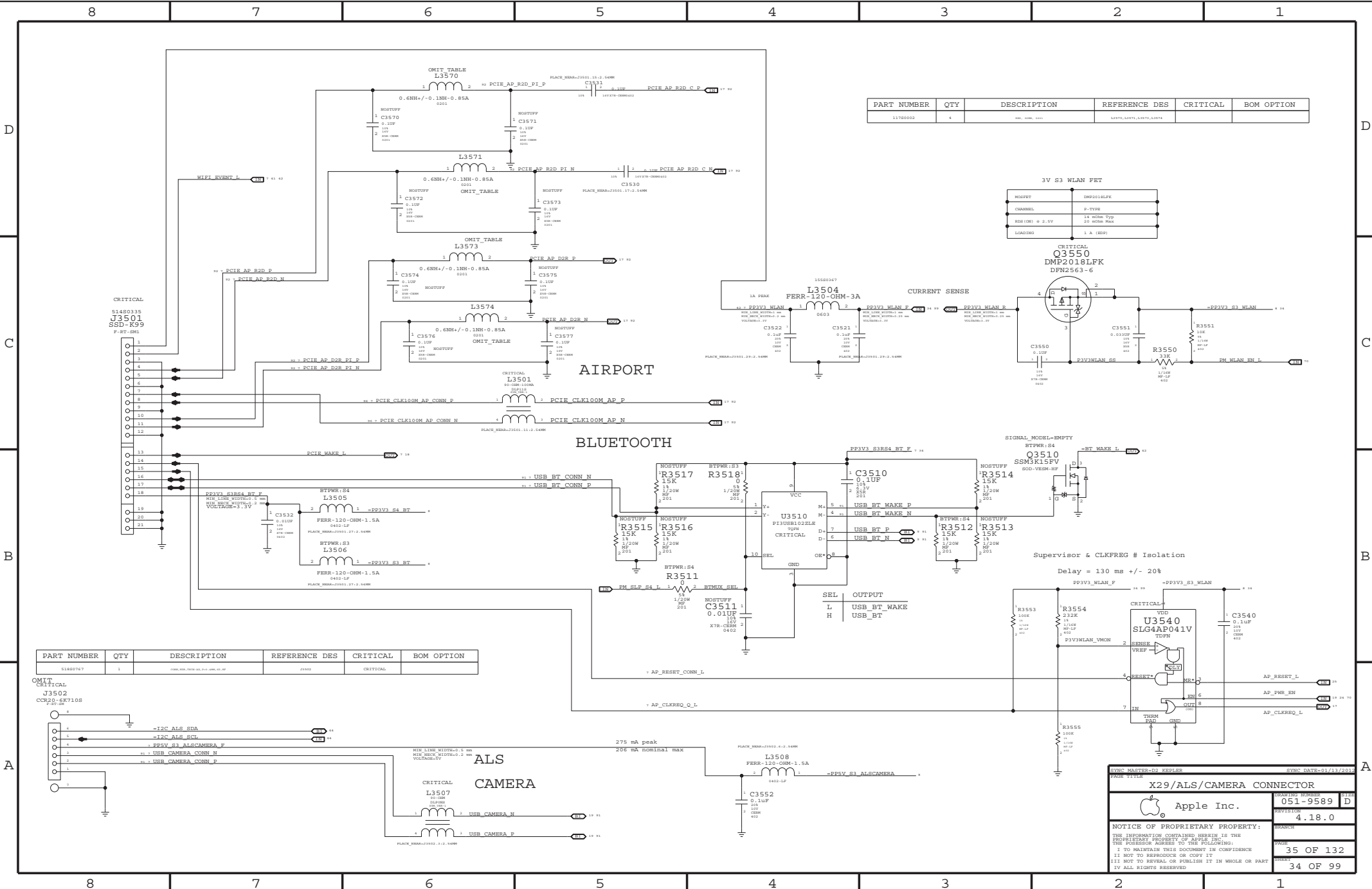
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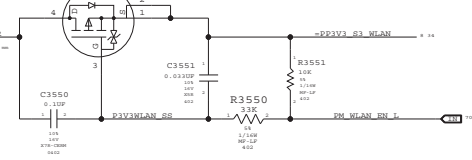




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12780002	4	0.6NH +/- 0.1NH - 0.85A	PCIE AP R2D C.P		

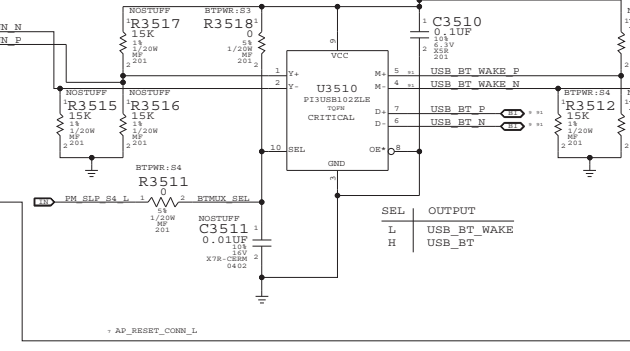
3V S3 WLAN FET	
MODE/SET	DMP2018LFK
CHANNEL	P-TYPE
DSM (DSM) @ 2.5V	14 MOSFET
LOAD/DSM	1 A (DSM)

CRITICAL
Q3550
DMP2018LFK
DFW2563-6



AIRPORT

BLUETOOTH

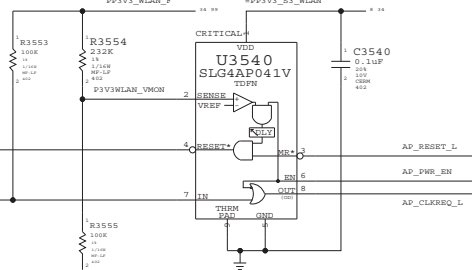


SIGNAL_MODEL=EMPTY
BTWPR: S4

CRITICAL
Q3510
SSM3K15FV
SOD-VESM-HEF



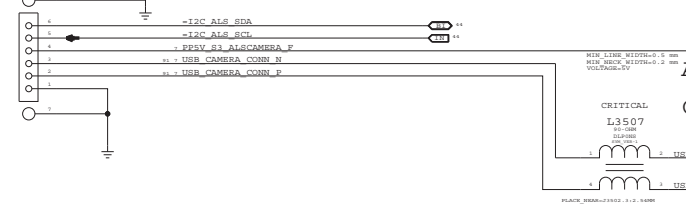
Supervisor & CLKFREG # Isolation
Delay = 130 ms +/- 20%



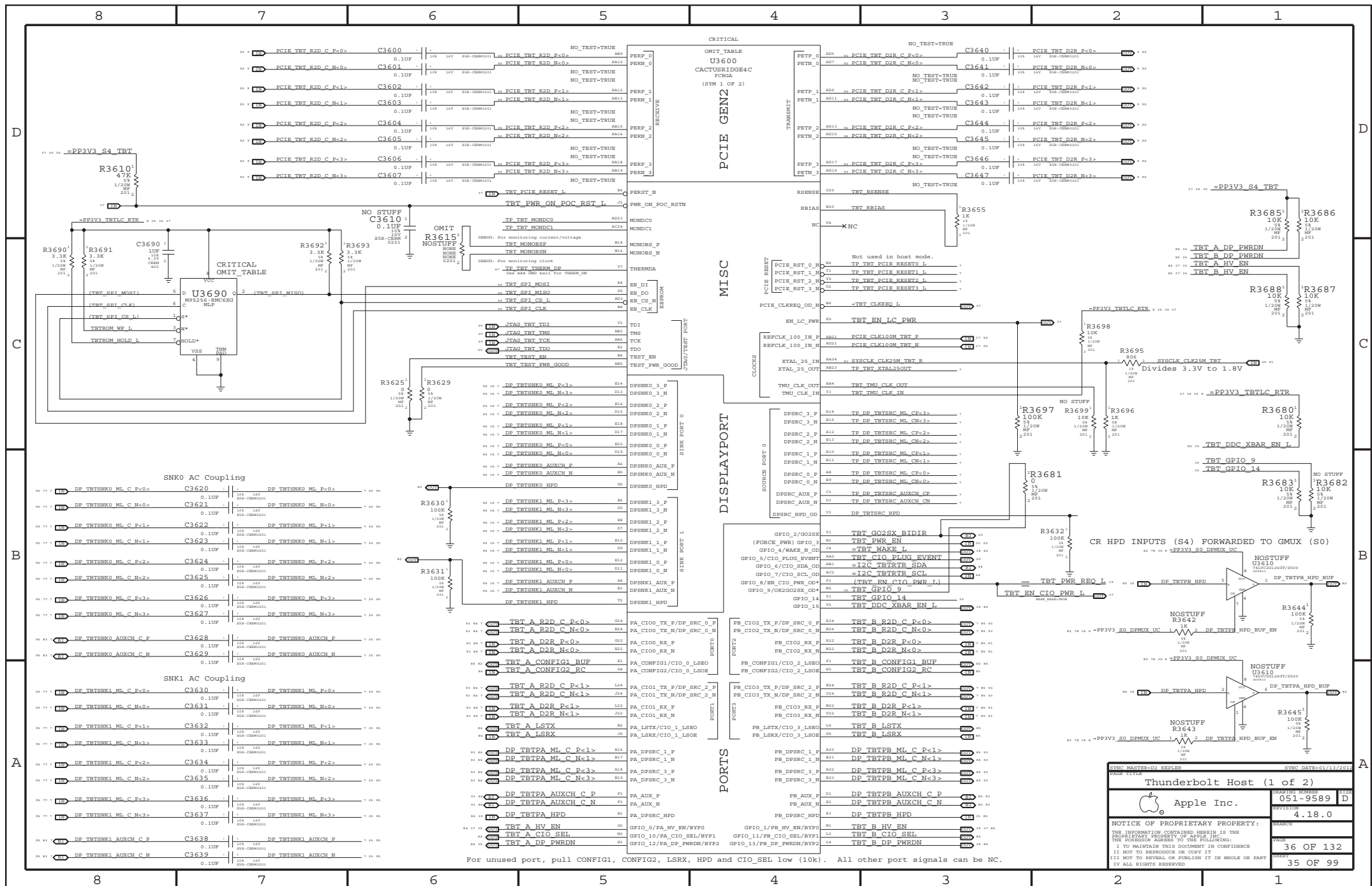
SYNC MASTER=DS REPLIER		SYNC DATE=01/11/2013	
PAGE TITLE			
X29/ALS/CAMERA CONNECTOR			
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
51850335	1	0.6NH +/- 0.1NH - 0.85A	PCIE AP R2D C.P		

CRITICAL
J3502
C3502-6K710S
F=0.5



ALS
CAMERA




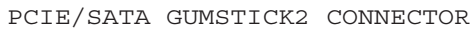

```
Power alaises required by this page:
-- FPPVIN_SM_TBSTST      (8-13V Boost Input)
-- FPP15V_TST_REG        (15V Boost Output)
-- FPPV3_TST_P3V3TSTFET  (3.3V FET Input)
-- FPPV3_TSTLC_FET       (3.3V FET Output)
-- FPPV3_BO_TSTWMCNTL     (1.05V FET Input)
-- FPPV05_TSTLC_FET       (1.05V FET Output)


Signal alaises required by this page:
-- TST_CLKREQ_L
-- TST_RESET_L

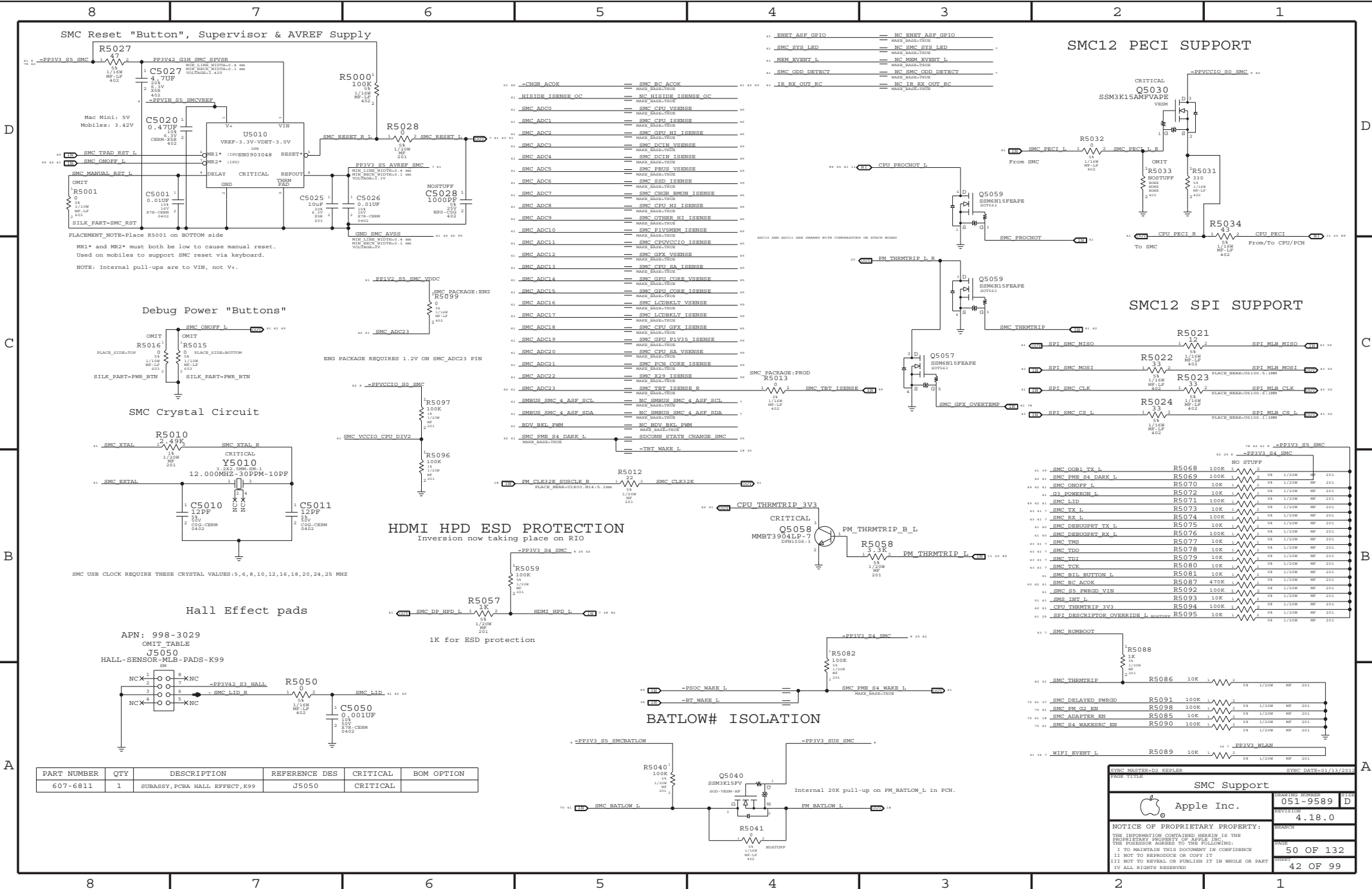
BCM options provided by this page:
TSTBST:Y - Stuffs 15v boost circuitry.
```



SYNC MASTER=D3 REPLER PAGE TITLE		SYNC DATE=01/11/2018	
<h1>Thunderbolt Power Supply</h1>			
	<h2>Apple Inc.</h2>		DRAWING NUMBER 051-9589
			REVISION 4.18.0
			BRAND Apple
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NTSC MASTER-D2 EPISODE		SYNCH DATE=51/13/2011	
PAGE TITLE			
 Apple Inc.		DRAWING NUMBER	TYPE
		051-9589	D
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		4.18.0	
		SCALE	
		45 OF 132	
		SHEET	
		39 OF 99	



SMC Reset "Button", Supervisor & AVREF Supply

SMC12 PECEI SUPPORT

Debug Power "Buttons"

SMC Crystal Circuit

HDMI HPD ESD PROTECTION

Hall Effect pads

BATLOW# ISOLATION

SMC12 SPI SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5050	CRITICAL	

SYMC MASTER-DS REPLIER
PAGE TITLE
SYMC DATE=01/11/2013

SMC Support

Apple Inc.

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REVISION
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PAGE
50 OF 132

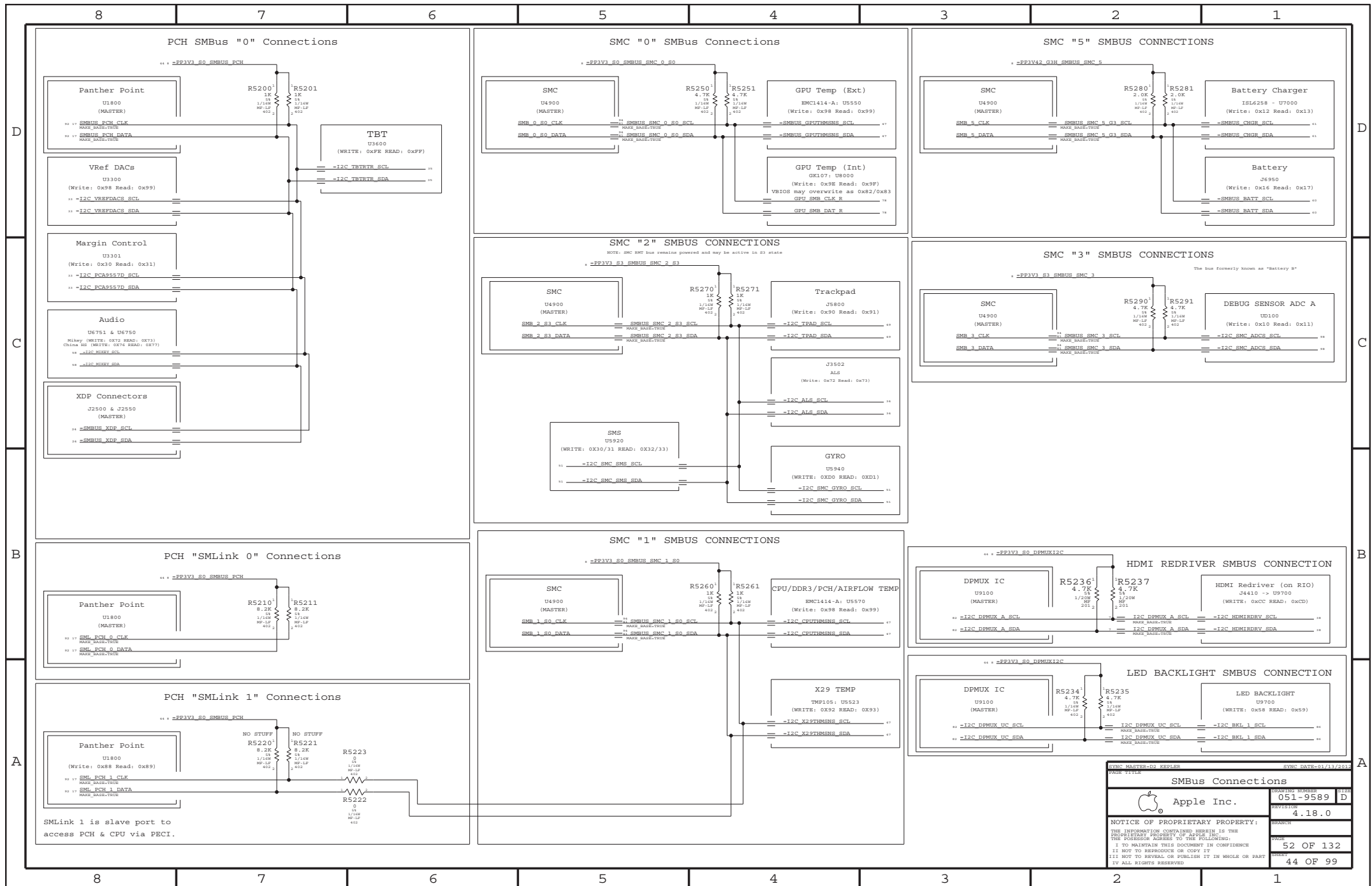
SHEET
42 OF 99


D

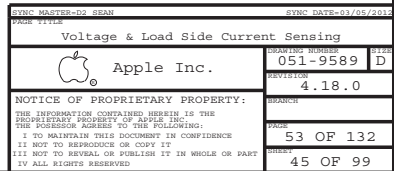


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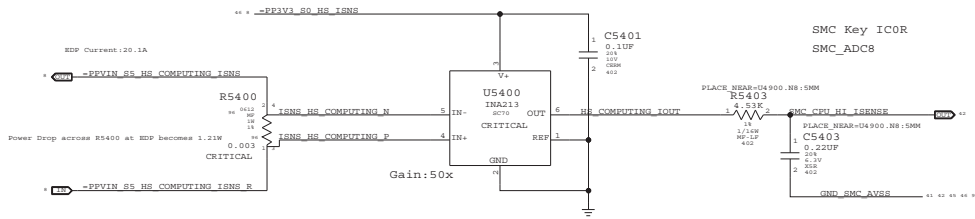
D



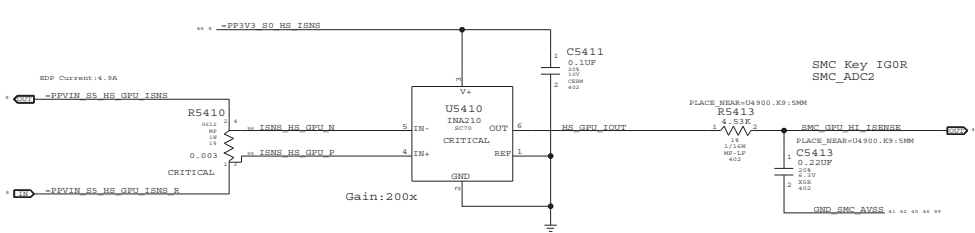
SYNCH MASTER-DS KEPLER		SYNCH DATE=01/11/2013	
PAGE TITLE			
SMBus Connections			
	Apple Inc.	REVISION NUMBER	051-9589 D
		REVISION	4.18.0
		SEARCH	
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		44 OF 99	



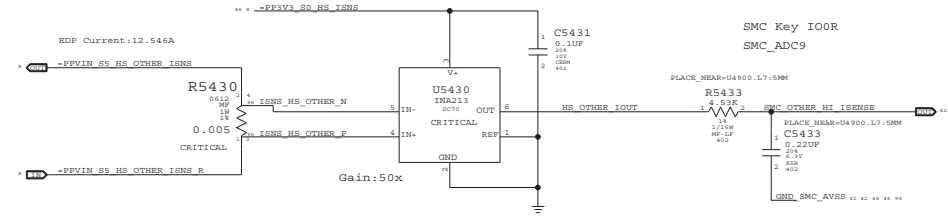
COMPUTING High Side Current Sense / Filter



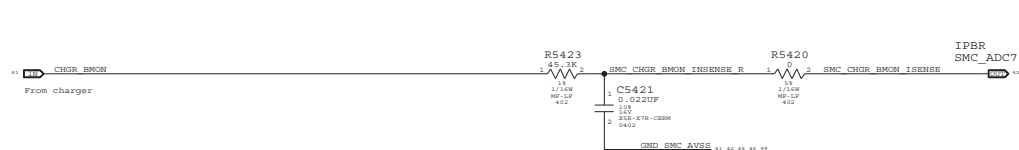
GRAPHICS High Side Current Sense / Filter



OTHER High Side Current Sense / Filter



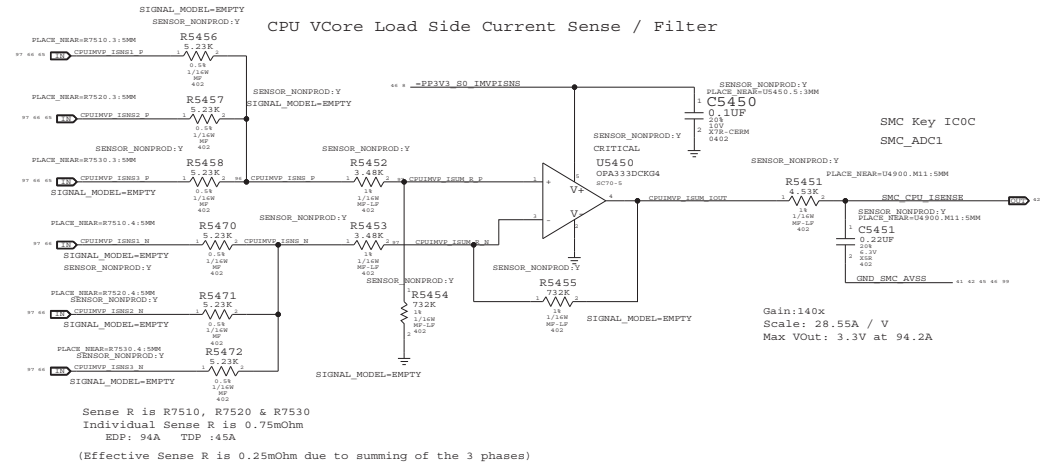
CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



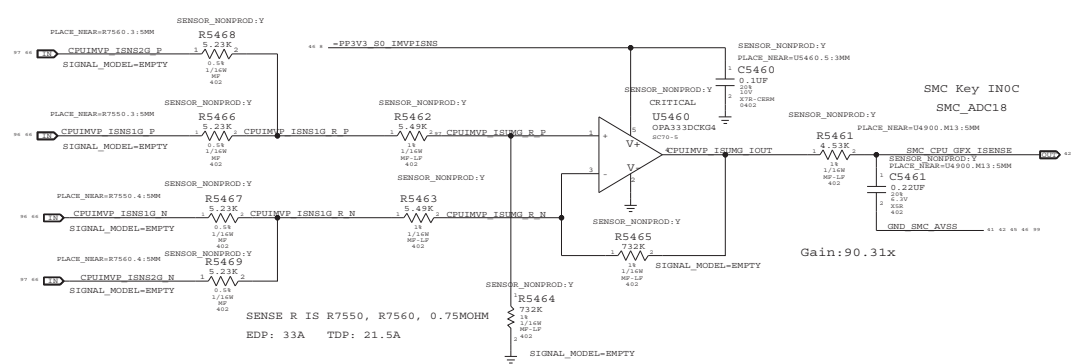
DC-IN (AMON) Current Sense Filter



CPU VCore Load Side Current Sense / Filter

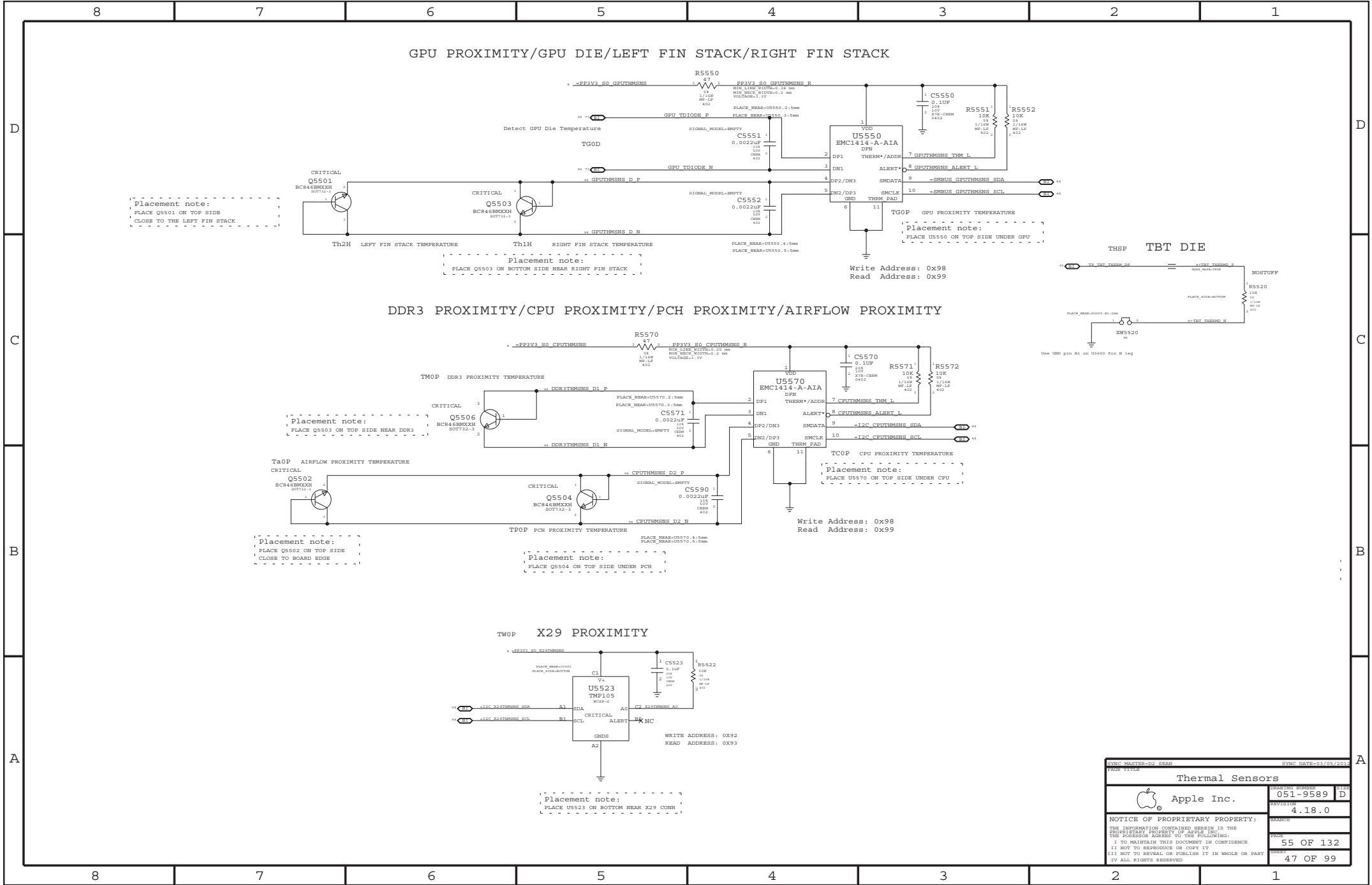



GFX/IG VCore Load Side Current Sense / Filter

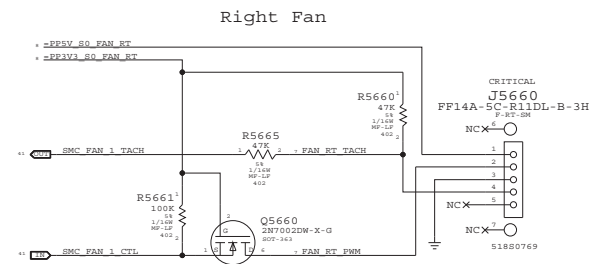



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11420114	2	SMC KEY IC0C, CPUIMPV1, 0.002 Ohm, 1/10W, NP-LP, 402	CH0451, CH0451		SENSOR_NONPROD-Y

SYMC MASTER-03 REAN		SYMC DATE: 01/05/2013	
PAGE TITLE		High Side and CPU/AXG Current Sensing	
Apple Inc.		501-9589	
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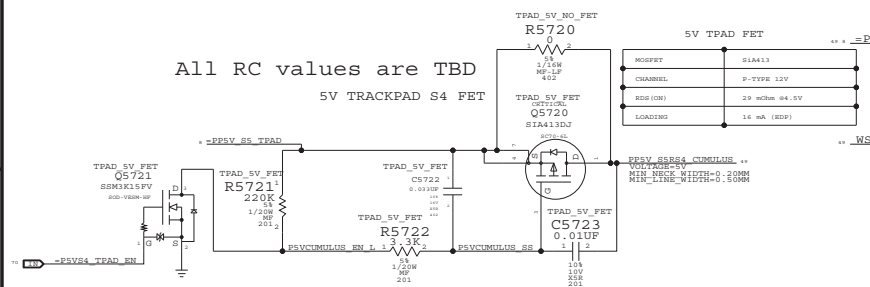
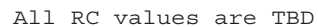
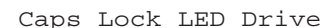
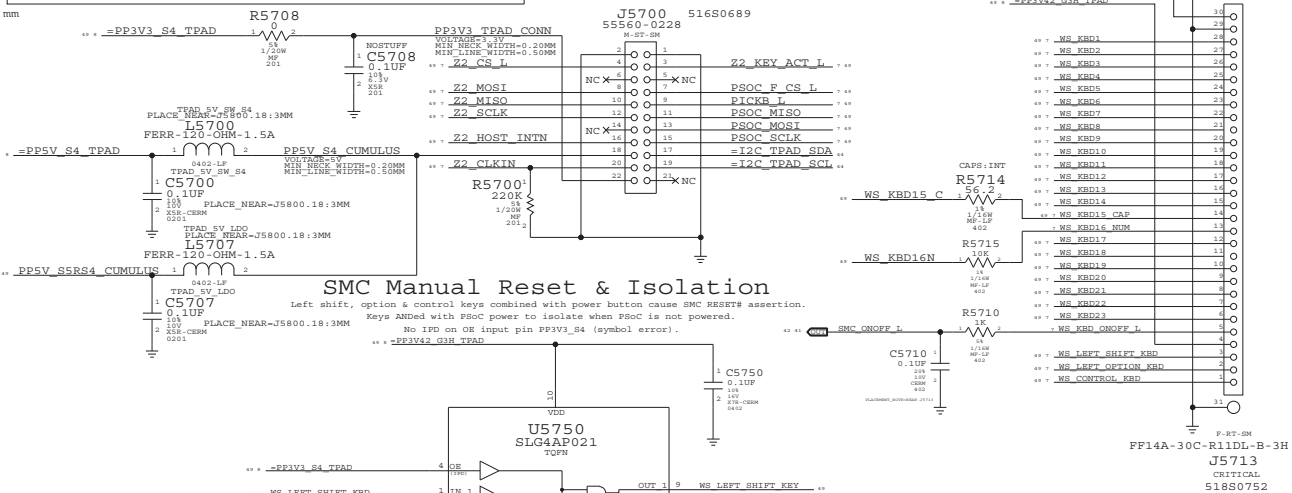
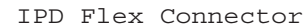
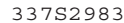


SYNCH MASTER=D3 REAN		SYNCH DATE=01/05/2013	
PAGE TITLE			
Thermal Sensors			
 Apple Inc.		DRAWING NUMBER	PAGE
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BIOG MASTER-10 KEYER		BIOG DATE-01/13/2012	
NAME TITLE			
Fan Connectors			
 Apple Inc.		SECRET NUMBER	CLASS
		051-9589	D
		DIVISION	
		4.18.0	
		BRANCH	
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PAGE		56 OF 132	
		48 OF 99	

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



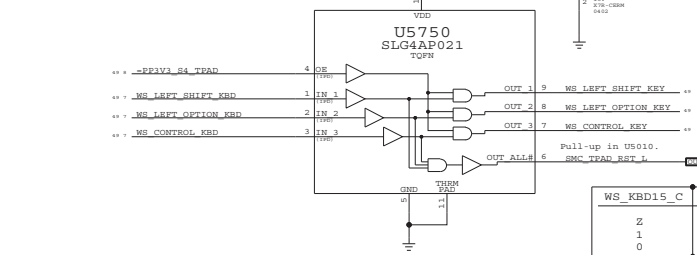
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE WHEN THE LID IS CLOSED	BOM
LID OPN => SMC_LID_LC ~ 3.42V	TPAD_
LID CLOSE => SMC_LID_LC < 0.50V	TPAD_

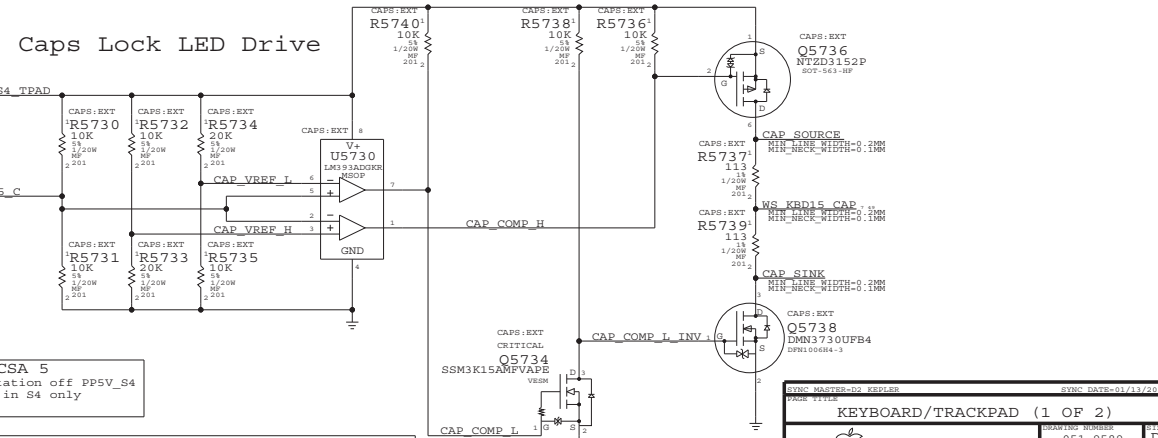
BOM Options available to CSA 5


TPAD_5V:SW_S4	Original implementation off PP5V_S4
TPAD_5V:LDO_S4	PP5V_S5 LDO power in S4 only
TPAD_5V:LDO_S5	PP5V_S5 LDO power

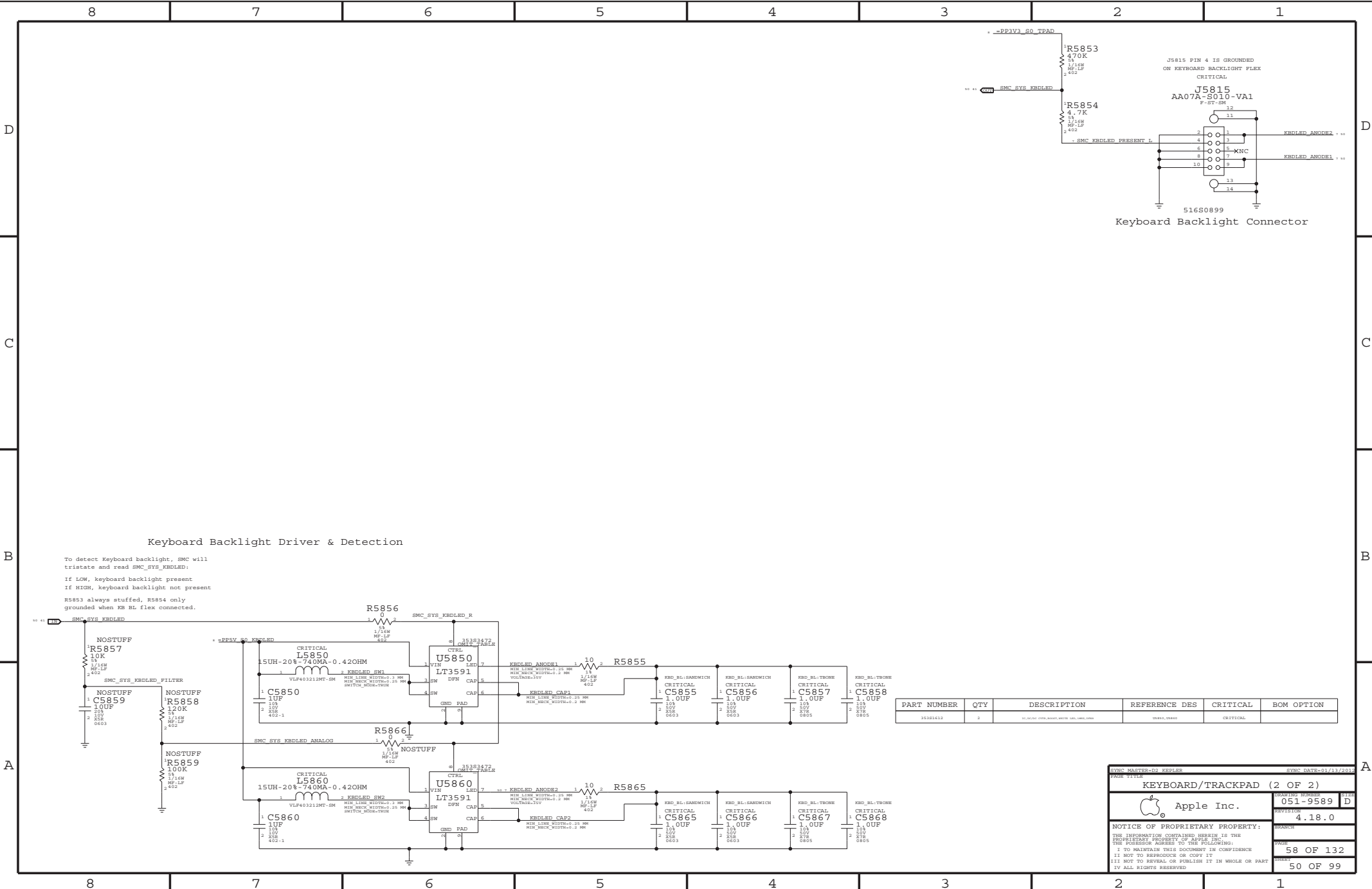
BOM GROUP	BOM OPTIONS
TPAD_5V:SW_S4	TPAD_5V_SW_S4
TPAD_5V:LDO_S4	TPAD_5V_FET,TPAD_5V_LDO
TPAD_5V:LDO_S5	TPAD_5V_NO_FET,TPAD_5V_LDO



WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink



TMC MASTER-D 820000		SYNCH DATE=01/19/2011																									
PAGE TITLE																											
KEYBOARD/TRACKPAD (1 OF 2)																											
		Apple Inc.																									
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ORIGIN NUMBER	051-9589	STATUS	D																								
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TYPE	57 OF 132																										
PRINT	49 OF 99																										



Keyboard Backlight Driver & Detection

To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBLED. If LOW, keyboard backlight present. If HIGH, keyboard backlight not present. R5853 always stuffed, R5854 only grounded when KB BL flex connected.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
35181612	2	10-10-100 0000 00000 00000 00000 00000	00000 00000	CRITICAL	

SYMC MASTER-03 KBLED

SYMC DATE=01/11/2013

KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

051-9589

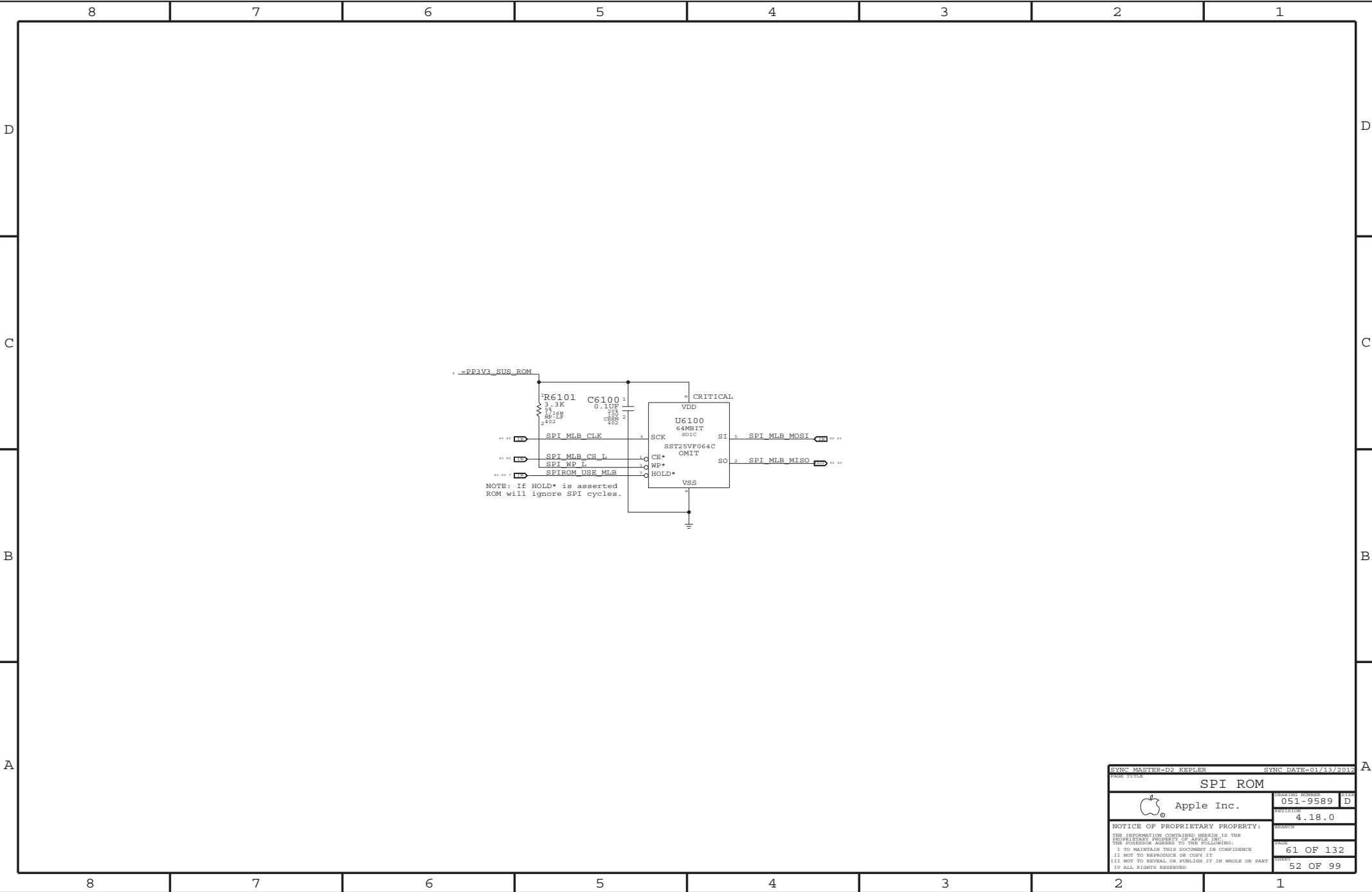
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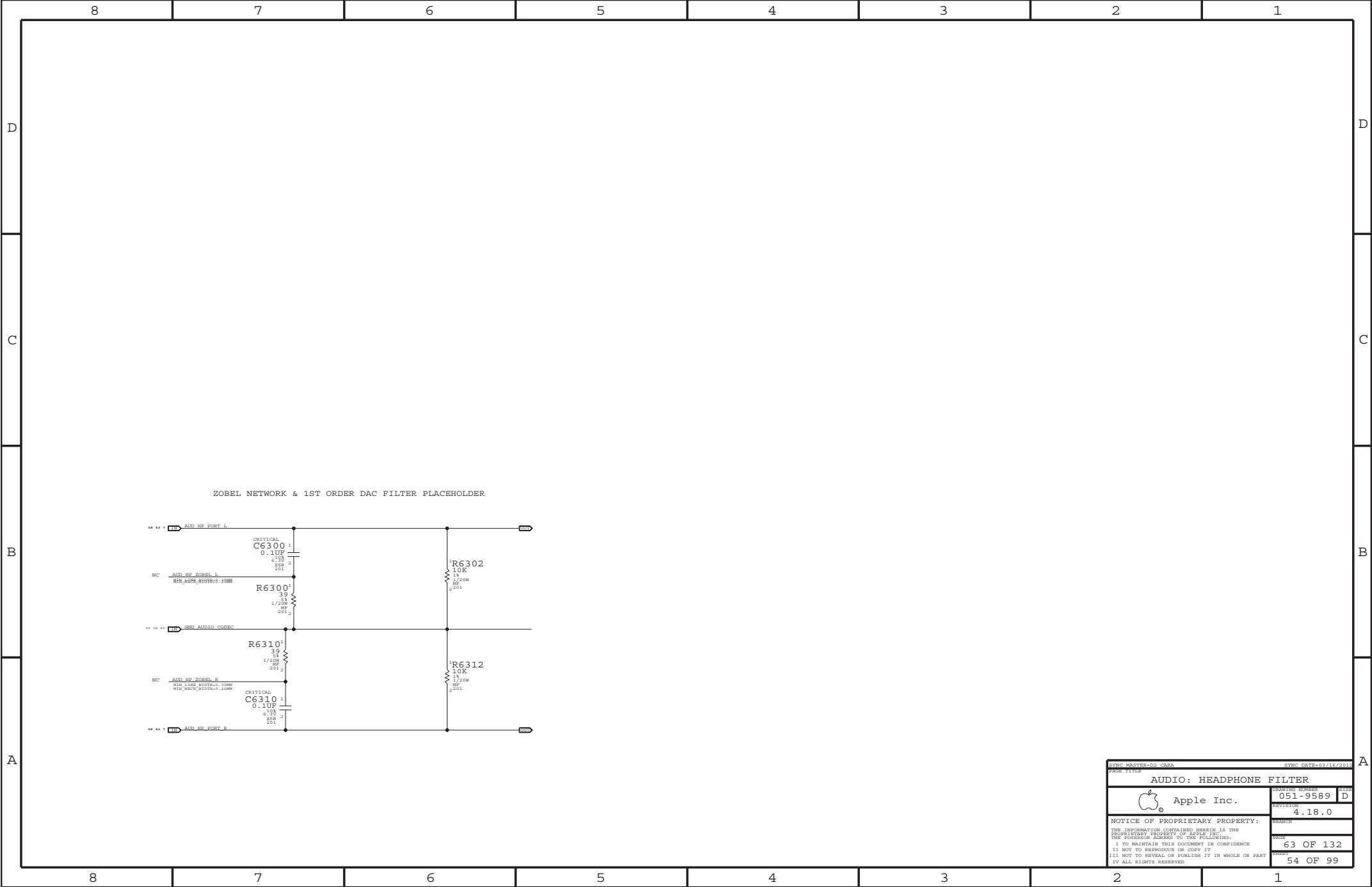
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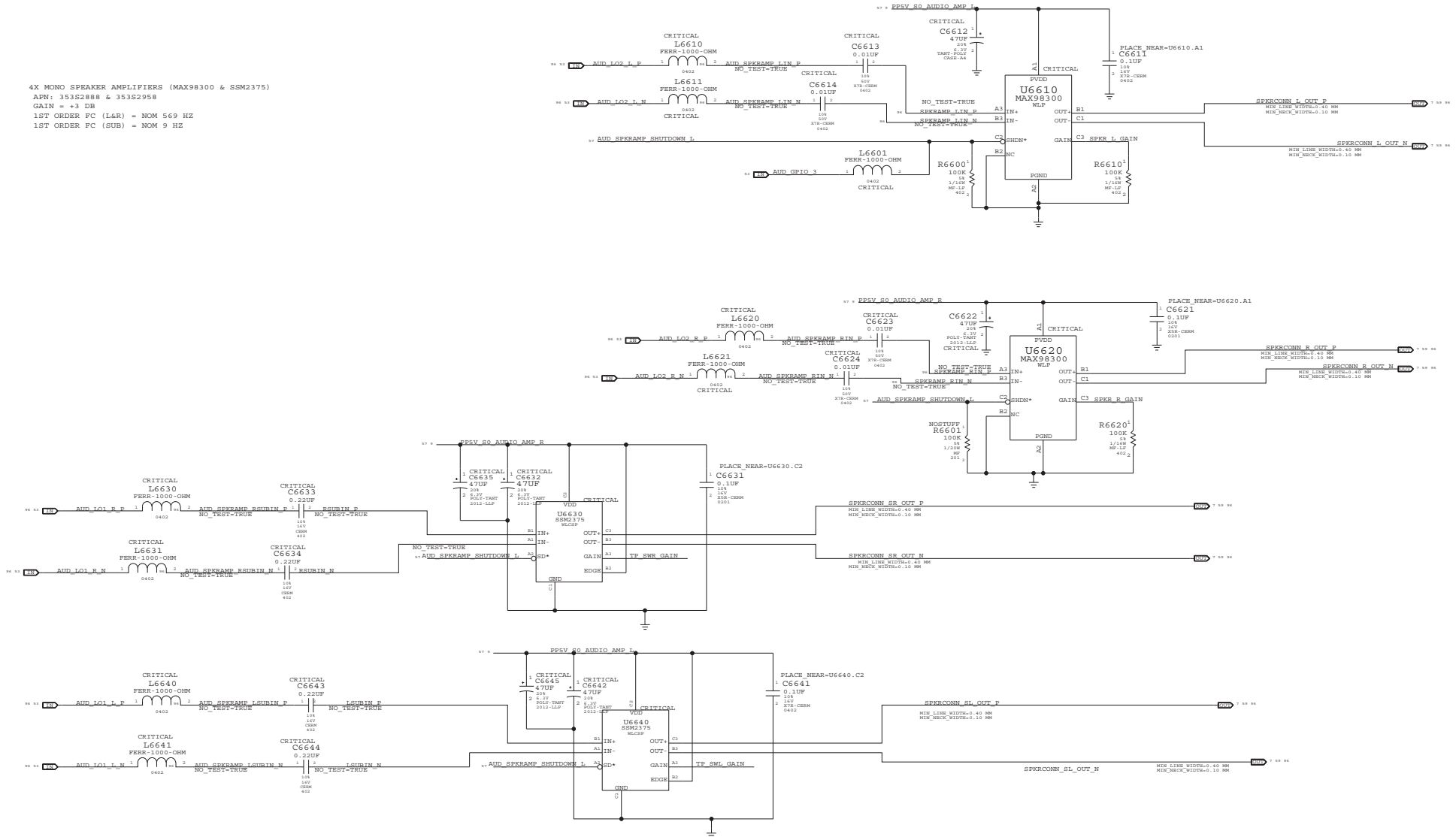





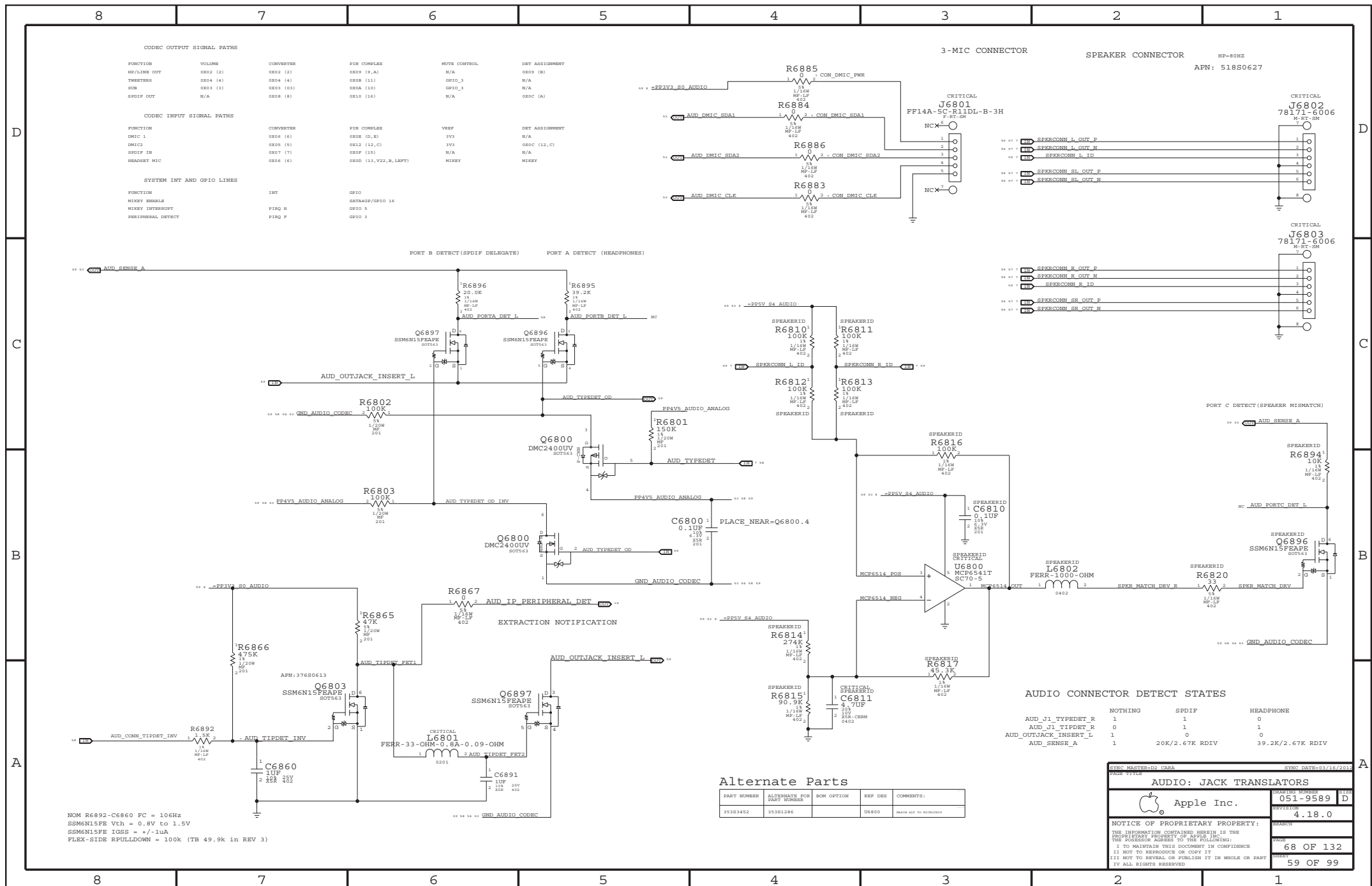
SYMC MASTER-D3 CABA		SYMC DATE:01/16/2013	
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AUDIO: HEADPHONE FILTER			
 Apple Inc.		DESIGNING NUMBER	051-9589
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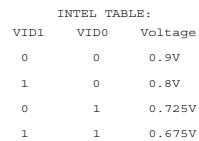
[illegible]

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ




SYNC MASTER-D3 CABA		SYNC DATE=01/16/2013	
PAGE TITLE			
AUDIO: SPEAKER AMP			
 Apple Inc.		SEARCH NUMBER	051-9589
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		SHEET	57 OF 99

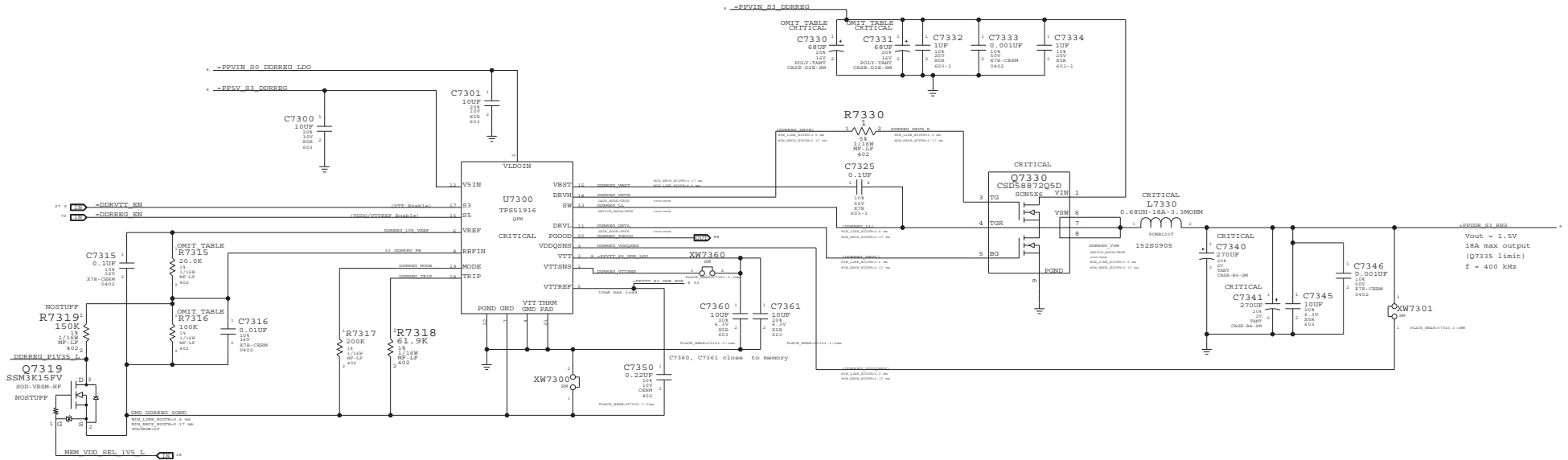




```
fb = (R7151+R712)/R7152 = 1.349 and Vref = 0.5;
VID1=1, VIDO=1;
Vout<1,1> = Vref x fb;
VID1=0, VIDO=1;
Vout<0,1> = Vref x (1+R7147 / (R7148 + R7149 )) x fb
VID1=1, VIDO=0;
Vout<1,0> = Vref x (1+ (R7147 + R7148) / R7149 )) x fb
VID1=0, VIDO=0;
Vout<0,0> = Vref x (1+ (R7147 / (R7148 + R7149 // R7150 )) x fb
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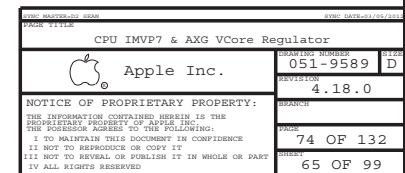
AT&T MASTER-D2 KEYPL		SYNCH DATE-01/13/201	
PAGE TITLE			
System Agent Supply			
	Apple Inc.		
	051-9589	D	
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PAGE		71 OF 132	
		62 OF 99	

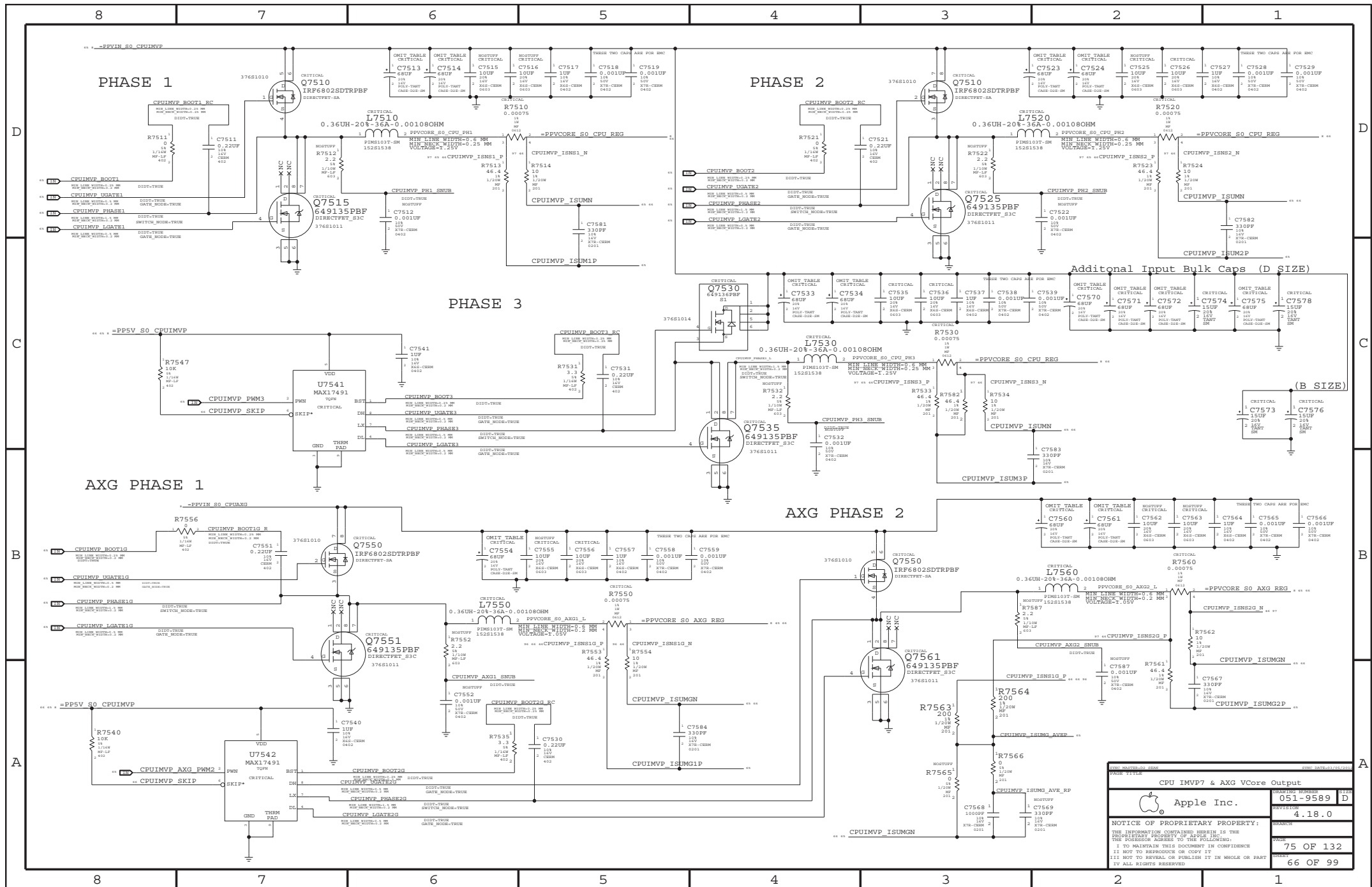
DDR3 (1V5R1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11480343	1	REG. PWR. 1.5V/1.5V, 1.5V, 1.5V, 1.5V, 1.5V, 1.5V	R7315		PPDDR:1V5
11480342	1	REG. PWR. 1.5V/1.5V, 1.5V, 1.5V, 1.5V, 1.5V, 1.5V	R7315		PPDDR:1V35
11480411	1	REG. PWR. 1.5V/1.5V, 1.5V, 1.5V, 1.5V, 1.5V, 1.5V	R7316		PPDDR:1V5
11480389	1	REG. PWR. 1.5V/1.5V, 1.5V, 1.5V, 1.5V, 1.5V, 1.5V	R7316		PPDDR:1V35

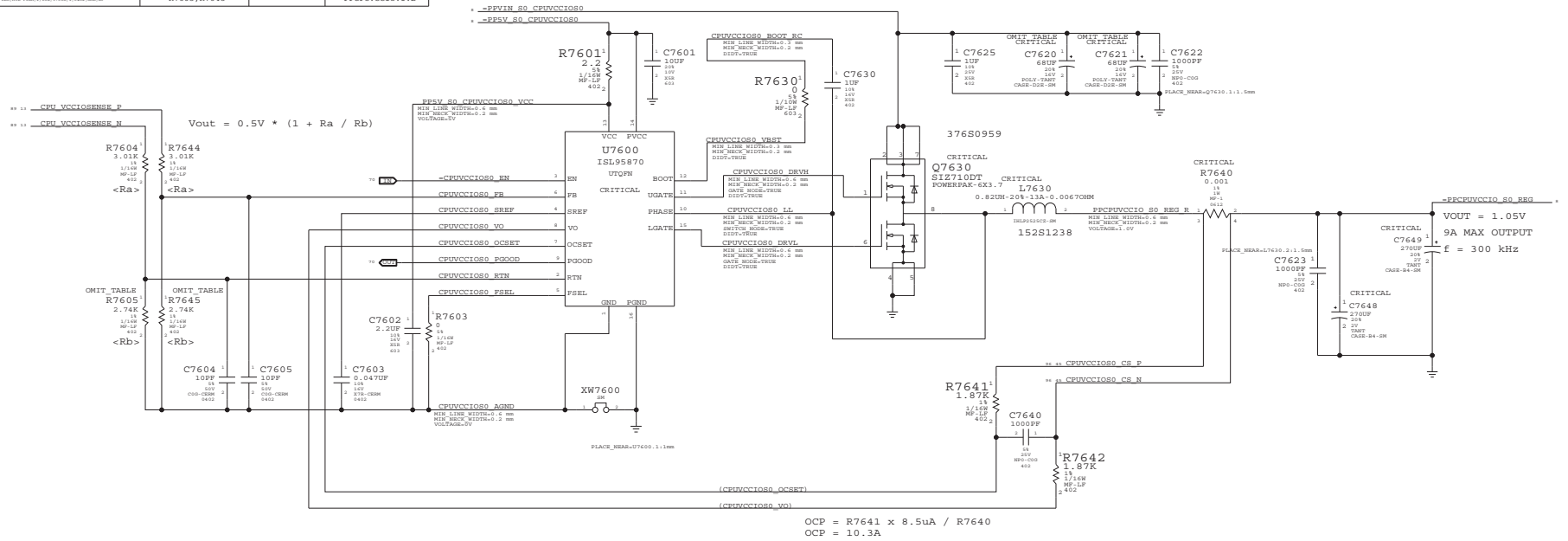
1V5R1V35V DDR3 SUPPLY	
Apple Inc.	051-9589 D
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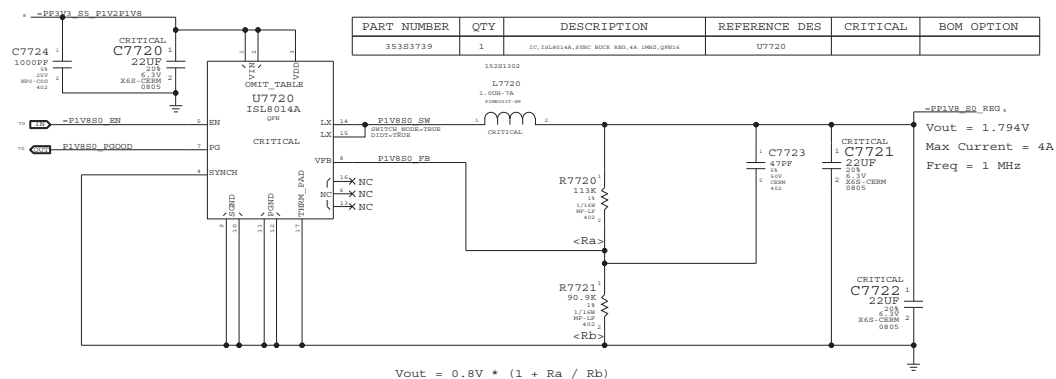
CPU VCCIO (1V0R1V05 S0) REGULATOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0260	2	RES, 0705, 010A, 1/10W, 2.74K, 1, 0.400, 0805, LF	R7605, R7645		PPCPUVCCIO:SNB
114S0264	2	RES, 0705, 010A, 1/10W, 3.01K, 1, 0.400, 0805, LF	R7605, R7645		PPCPUVCCIO:IVB



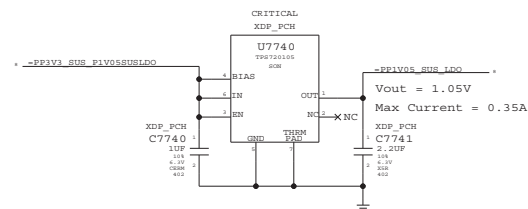
CPU VCCIO (1V0R1V05 S0) POWER SUPPLY	
Apple Inc.	051-9589 D
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1.8V S0 Regulator

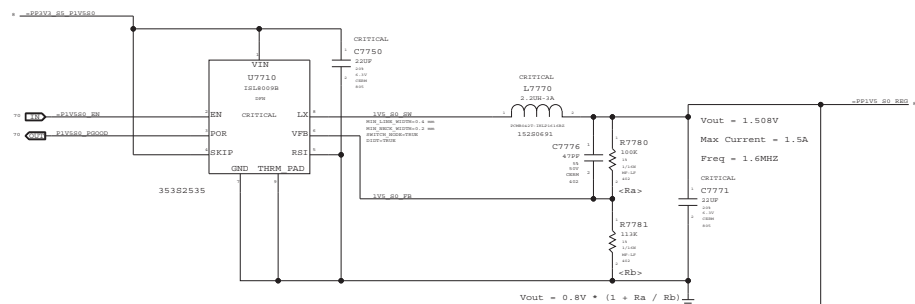


1.05V SUS LDO

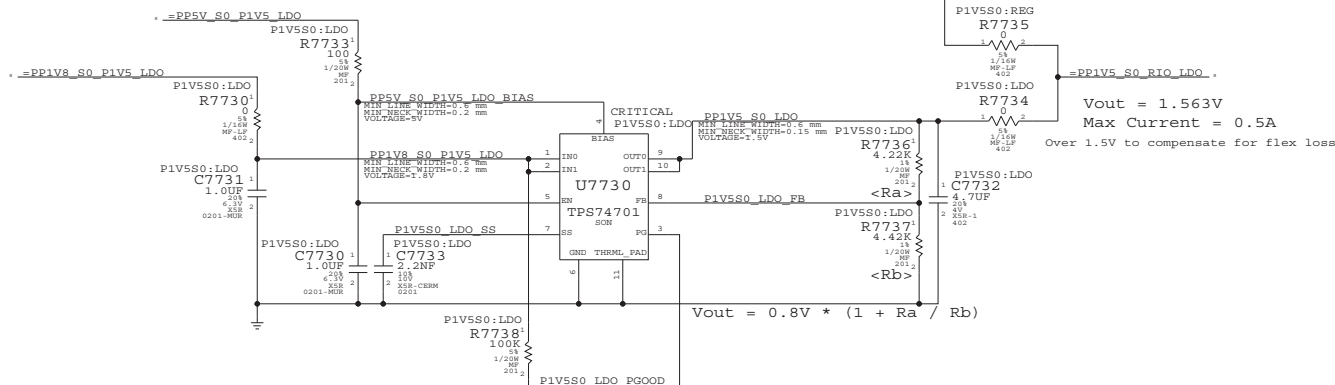
Panther Point-M requires JTAG pull-ups to be powered at 1.05V in Sus. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.




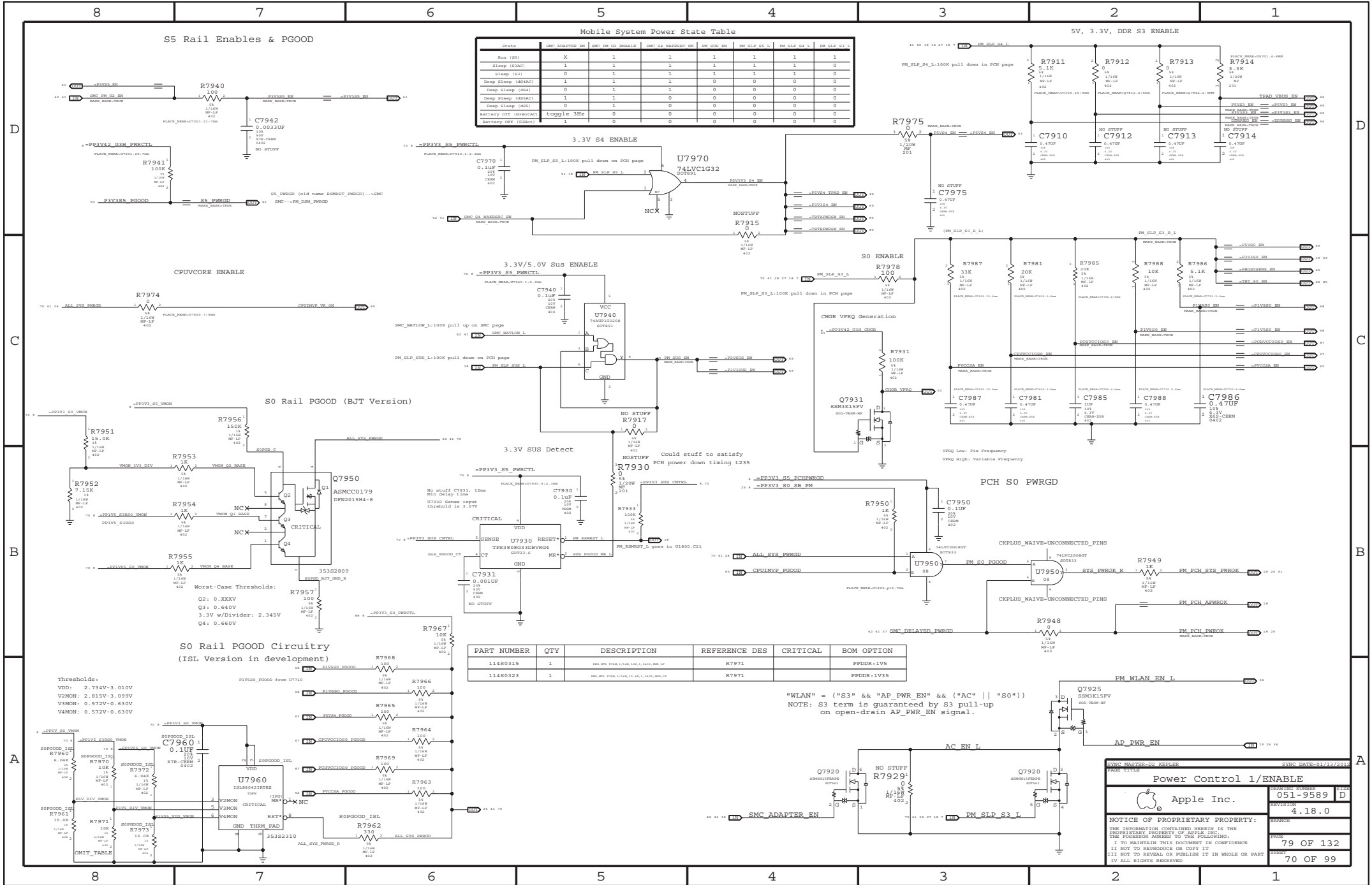
1.5V S0 Regulator

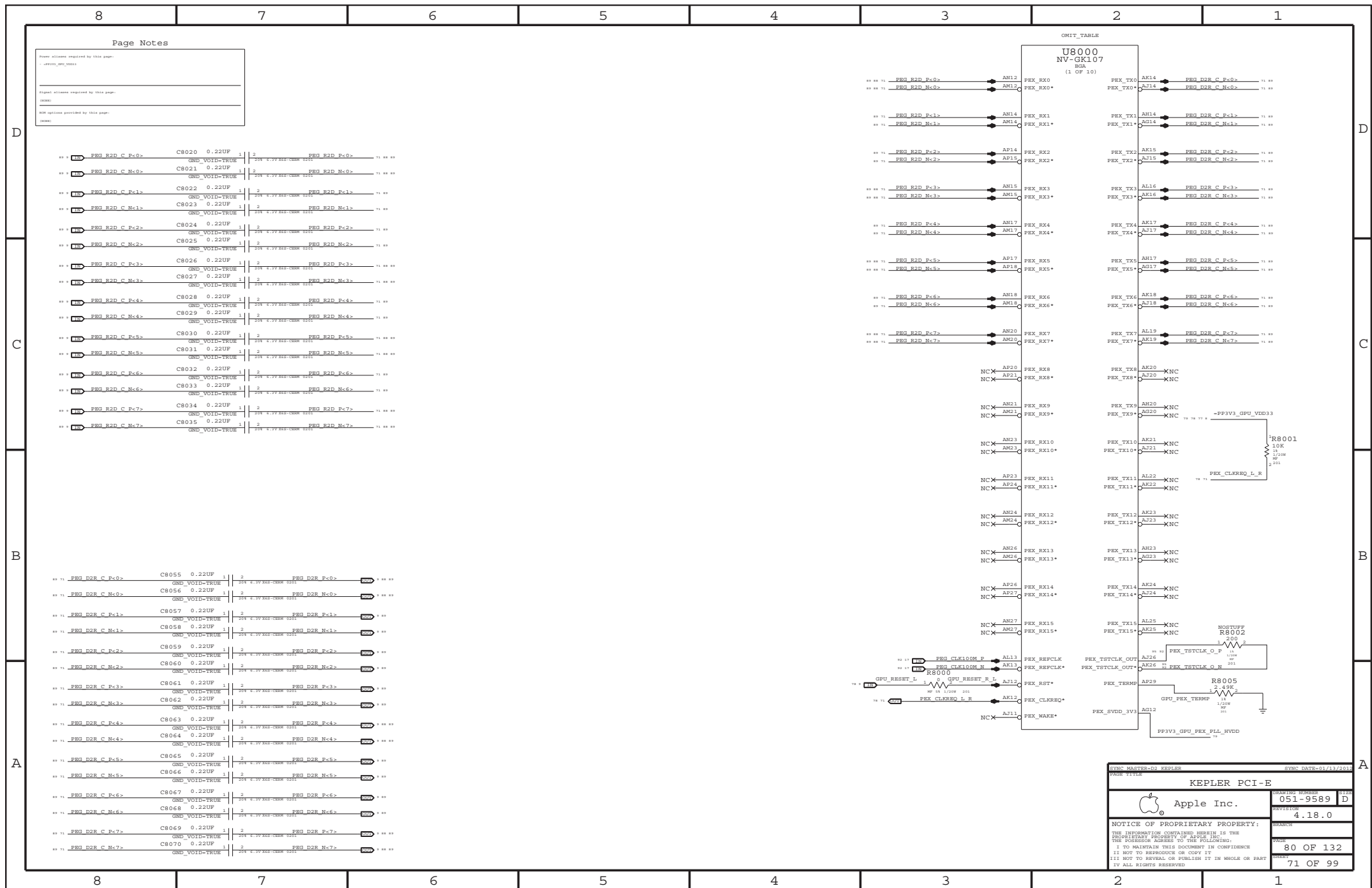


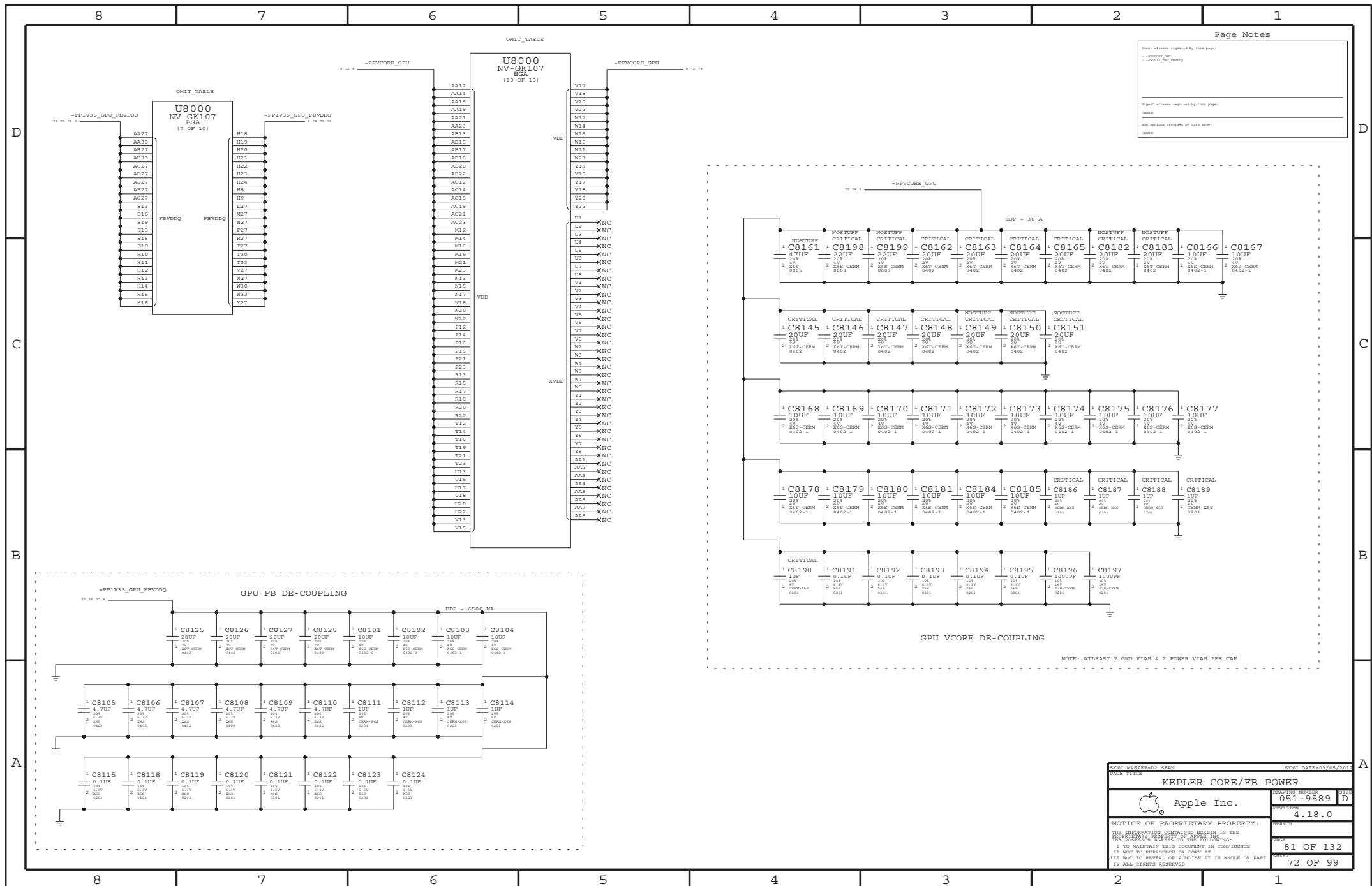
1.5V S0 LDO (RIO)

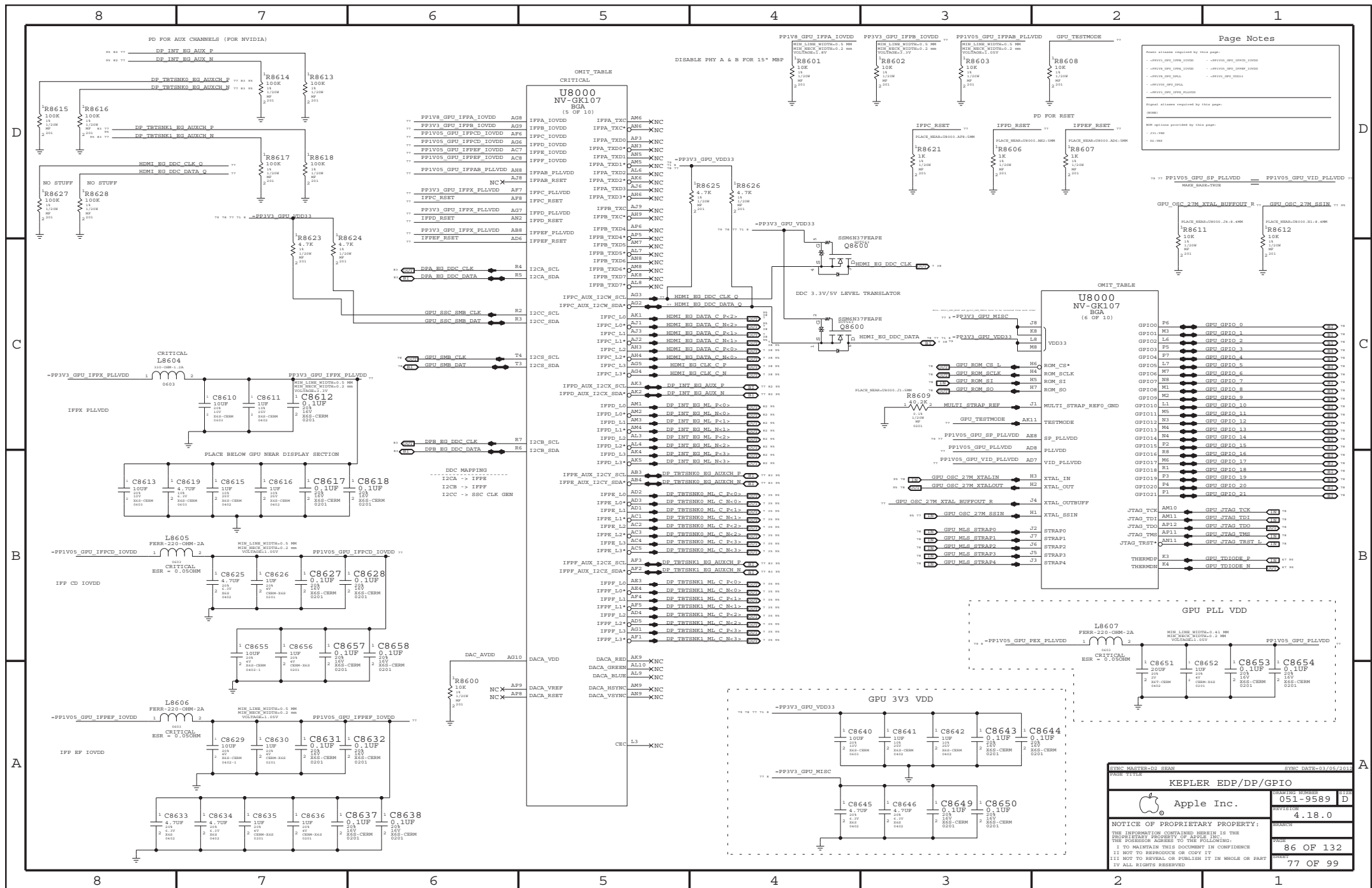


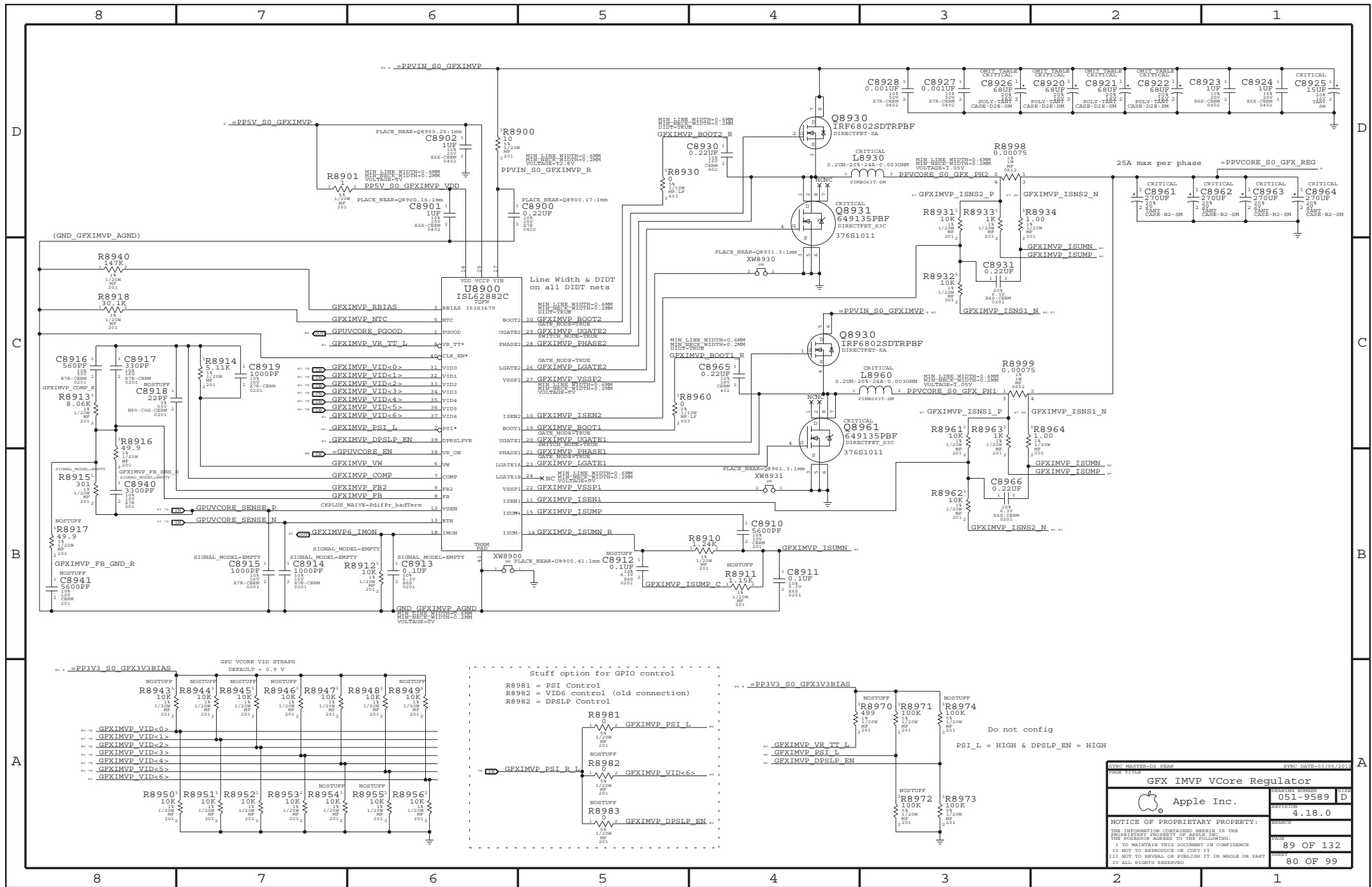
RUN: MASTER-02 REVER		SYN: DATE-01/11/20	
DATE TITLE			
Misc Power Supplies			
	Apple Inc.		DRAWING NUMBER 051-9589
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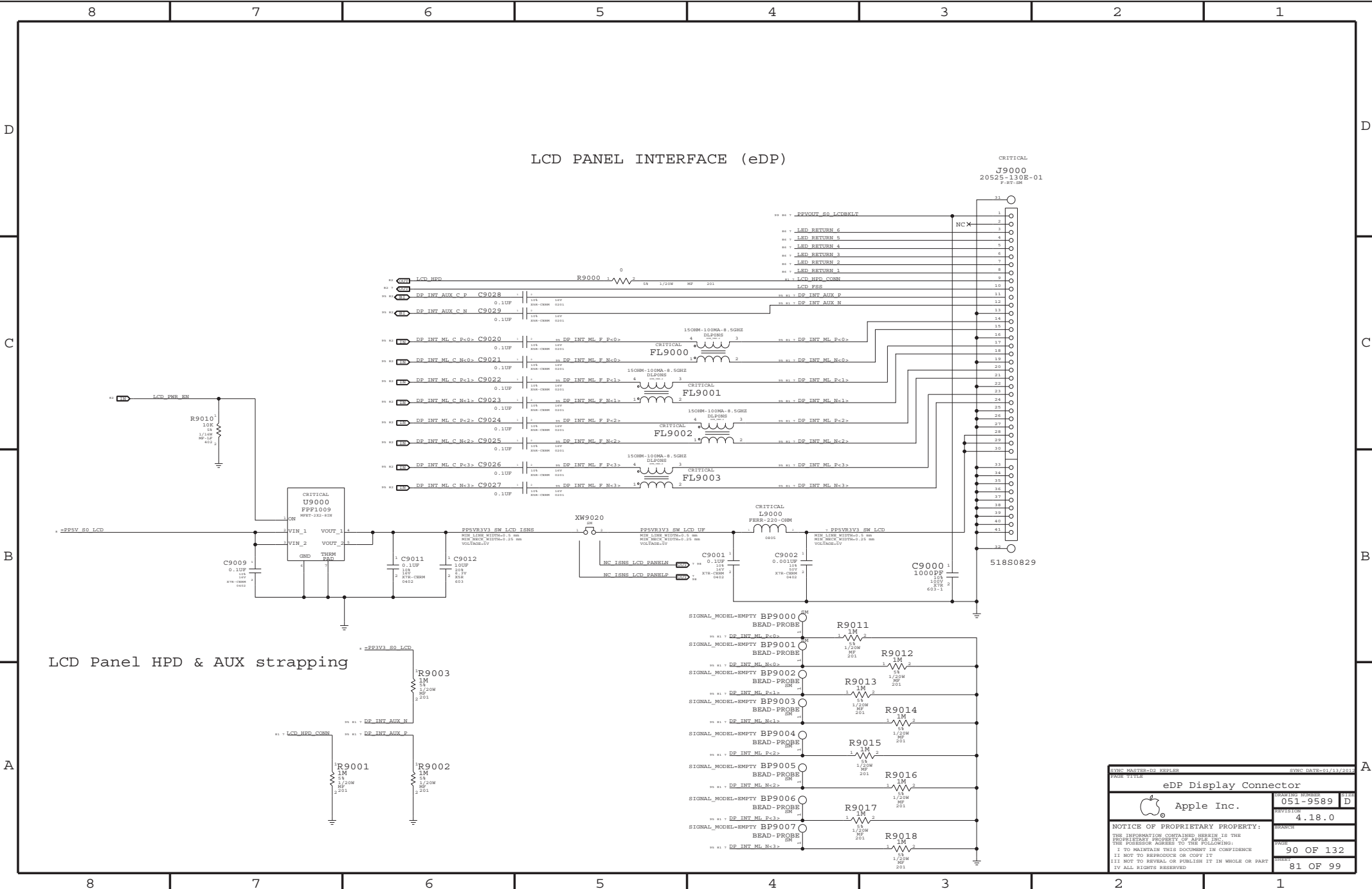









SYNCHRONOUS DESIGN		SYNCHRONOUS DATE: 01/05/2013	
PAGE TITLE		GFX IMVP VCore Regulator	
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PAGE		89 OF 132	
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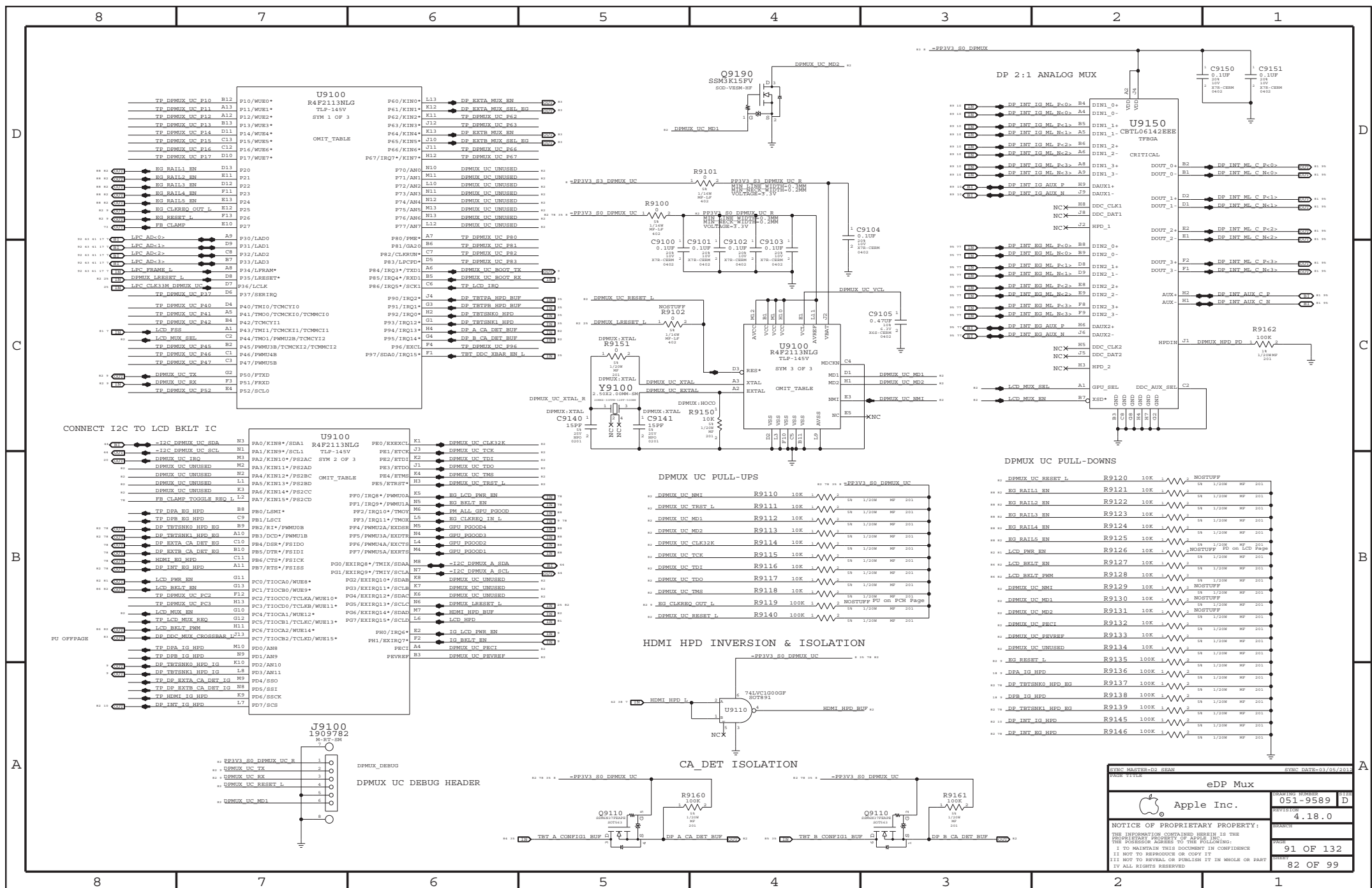


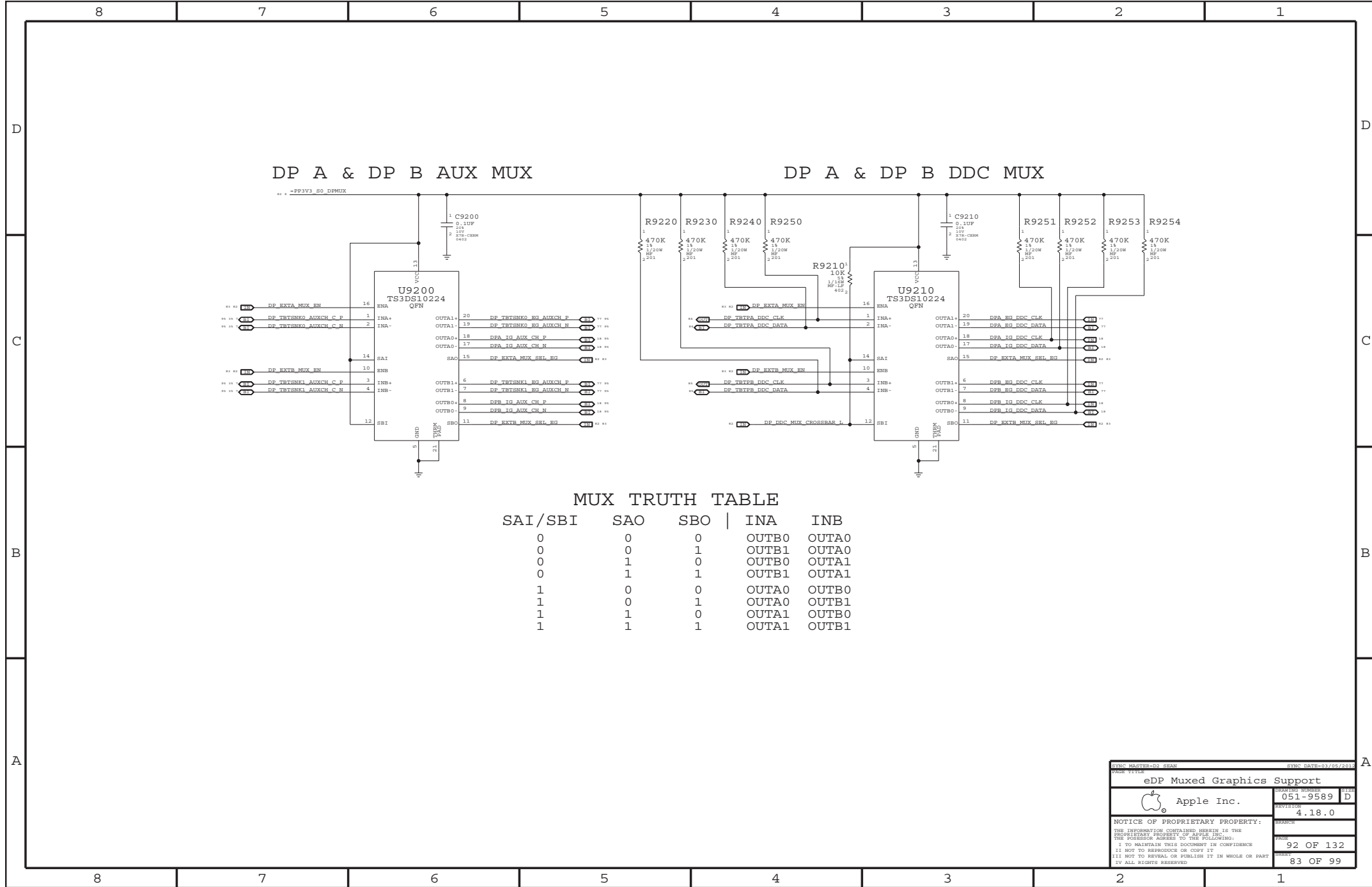
LCD PANEL INTERFACE (eDP)

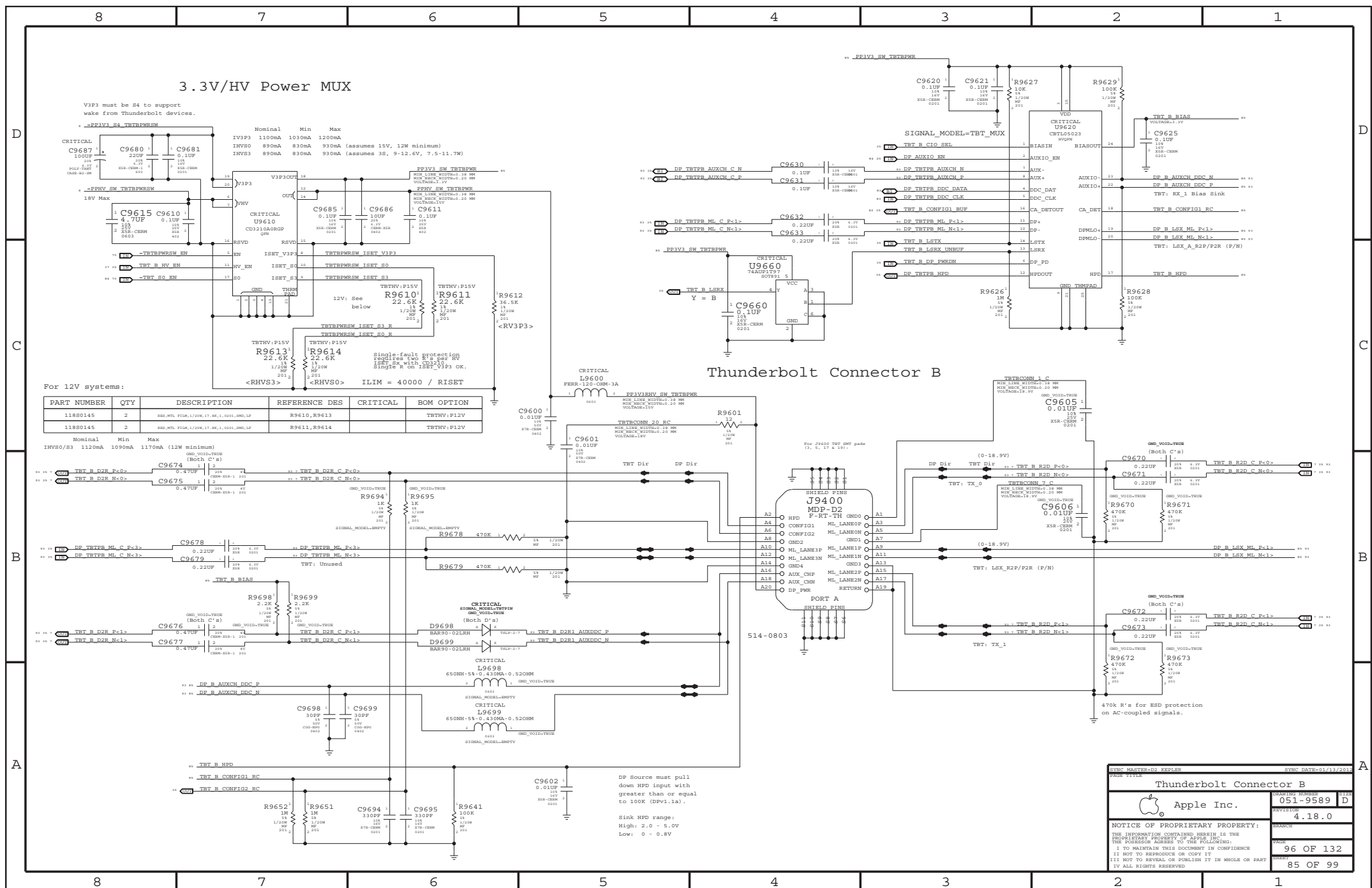
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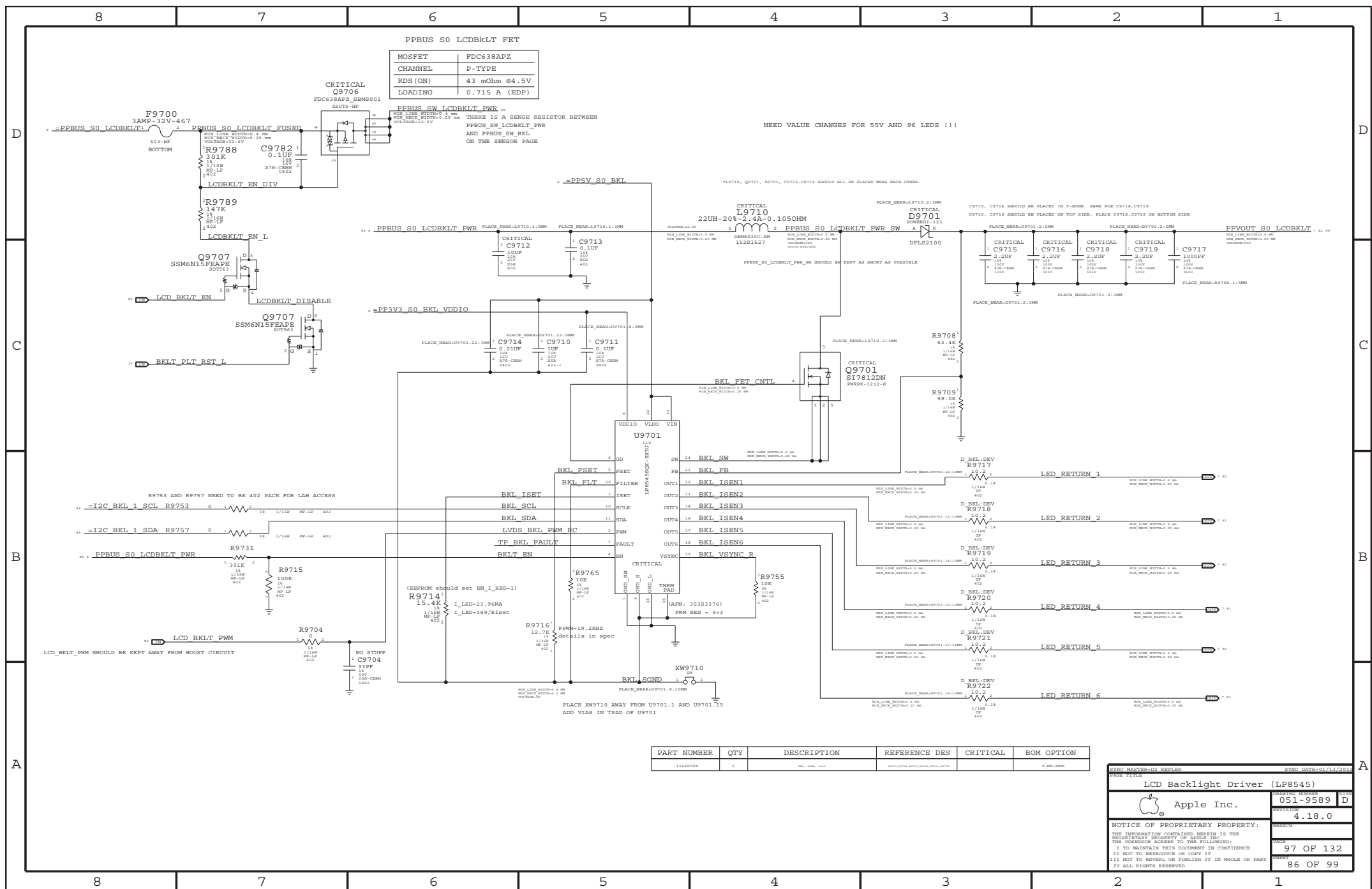
LCD Panel HPD & AUX strapping

SYNC MASTER-02 KEYL88		SYNC DATE=01/13/2011	
PAGE TITLE		eDP Display Connector	
 Apple Inc.		DESIGNING NUMBER	051-9589 D
		REVISION	4.18.0
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		PRINT	81 OF 99

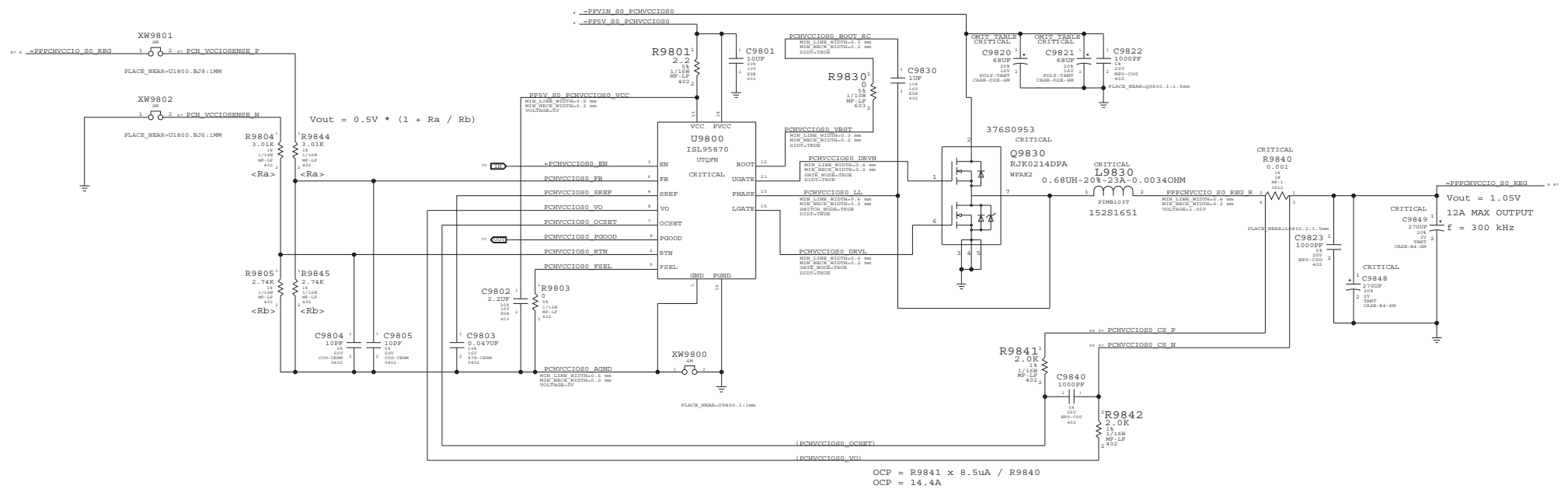




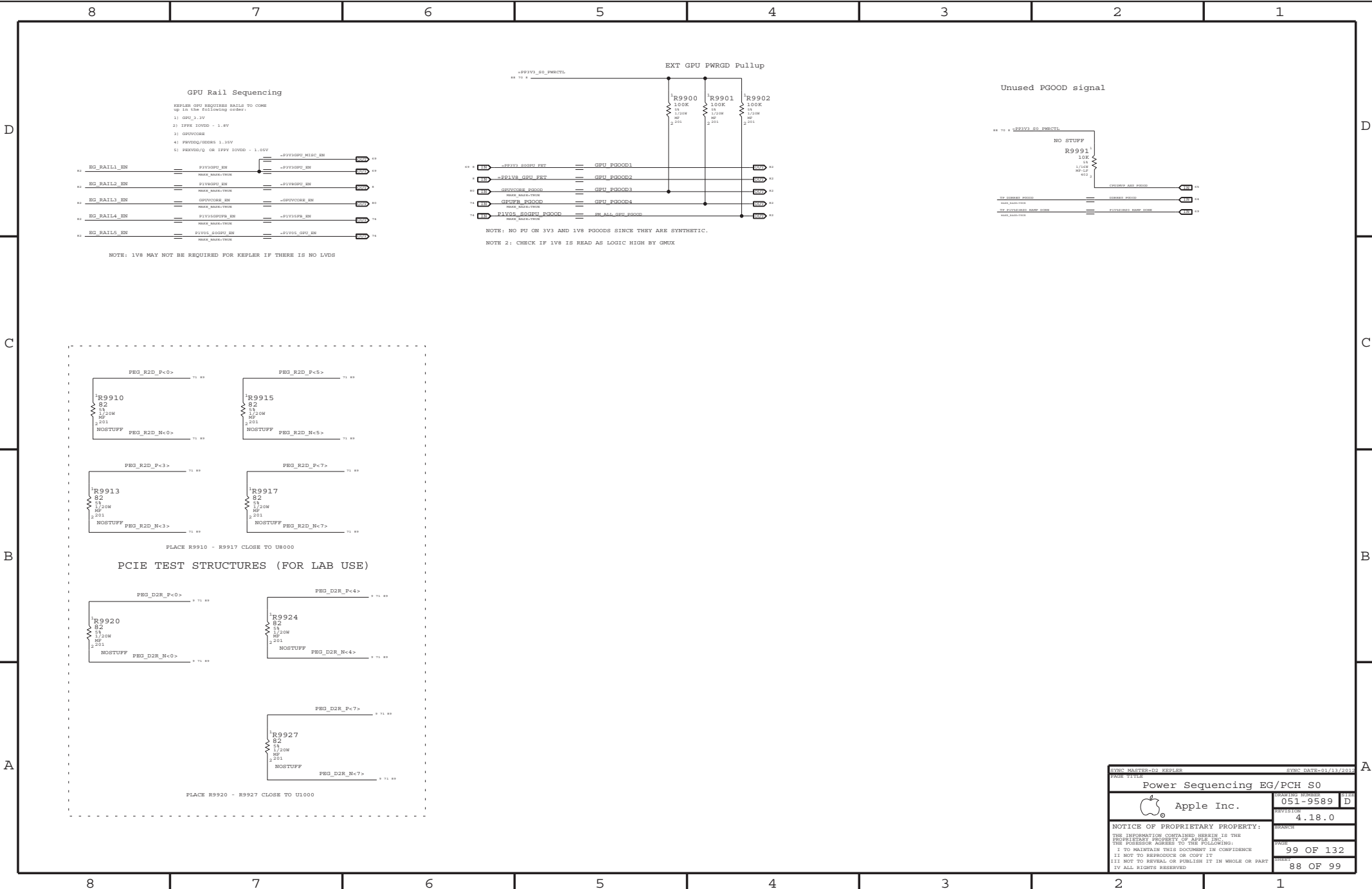




PCH VCCIO (1.05V S0) REGULATOR



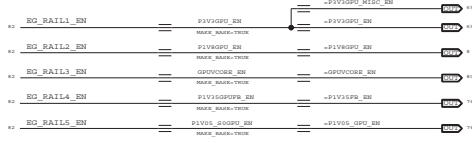
PCH VCCIO (1.05V) POWER SUPPLY	
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GPU Rail Sequencing

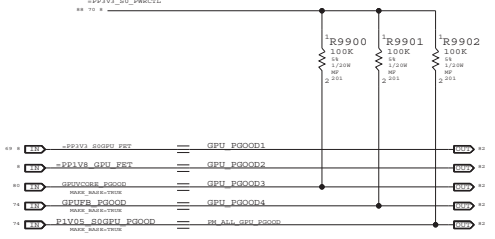
KEPLER GPU REQUIRES RAILS TO COME
up in the following order:

- 1) GPU_3.3V
- 2) IFEX IOVDD - 1.8V
- 3) GPUVCORE
- 4) PEVDDQ/GDDQS 1.35V
- 5) PEVDDQ/Q OR IFPP IOVDD - 1.05V



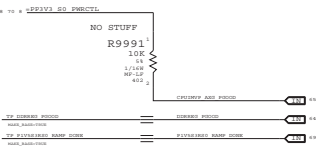
NOTE: 1V8 MAY NOT BE REQUIRED FOR KEPLER IF THERE IS NO LVDS

EXT GPU PWRGD Pullup

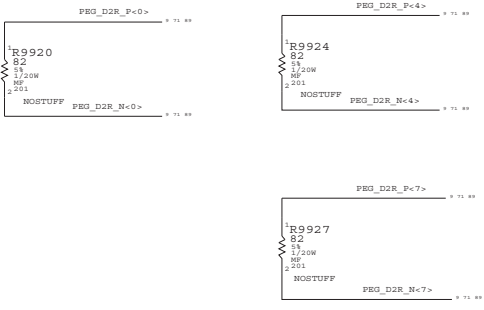


NOTE: NO PU ON 3V3 AND 1V8 PGOODS SINCE THEY ARE SYNTHETIC.
NOTE 2: CHECK IF 1V8 IS READ AS LOGIC HIGH BY GMIUX

Unused PGOOD signal



PCIE TEST STRUCTURES (FOR LAB USE)



PLACE R9920 - R9927 CLOSE TO U1000

SYNCH MASTERS-D3 KEPLER		SYNCH DATE: 01/11/2013	
PAGE TITLE		Power Sequencing EG/PCH S0	
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	<table><tr><th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER?</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr><tr><td>CPU_S05</td><td>*</td><td>=S0_OHM_SE</td><td>=S0_OHM_SE</td><td>=S0_OHM_SE</td><td>=S0_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr><tr><td>CPU_S55</td><td>*</td><td>=S5_OHM_SE</td><td>=S5_OHM_SE</td><td>=S5_OHM_SE</td><td>=S5_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr><tr><td>CPU_27F45</td><td>*</td><td>=27F4_OHM_SE</td><td>=27F4_OHM_SE</td><td>=27F4_OHM_SE</td><td>=27F4_OHM_SE</td><td>7 MIL</td><td>7 MIL</td></tr></table>									PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	CPU_S05	*	=S0_OHM_SE	=S0_OHM_SE	=S0_OHM_SE	=S0_OHM_SE	=STANDARD	=STANDARD	CPU_S55	*	=S5_OHM_SE	=S5_OHM_SE	=S5_OHM_SE	=S5_OHM_SE	=STANDARD	=STANDARD	CPU_27F45	*	=27F4_OHM_SE	=27F4_OHM_SE	=27F4_OHM_SE	=27F4_OHM_SE	7 MIL	7 MIL																																																																																																																																																																																																																																																																																																																																													
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NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.																																																																																																																																																																																																																																																																																																																																																																																						
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Most CPU signals with impedance requirements are 50-ohm single-ended. Some signals require 27.4-ohm single-ended impedance. SOURCE: IVB PLATFORM DG , Tables 205-207																																																																																																																																																																																																																																																																																																																																																																																						
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	<table><tr><th rowspan="2">ELECTRICAL_CONSTRAINT_SET</th><th colspan="2">NET TYPE</th><th rowspan="2"></th><th rowspan="2"></th></tr><tr><th>PHYSICAL</th><th>SPACING</th></tr><tr><td>DMI_S0N</td><td>DMI_S0N</td><td>DMI_S0N</td><td>DMI_S0N_P<3:0></td><td>10 18</td></tr><tr><td>DMI_S0N</td><td>DMI_S0N</td><td>DMI_S0N</td><td>DMI_S0N_N<3:0></td><td>10 18</td></tr><tr><td>DMI_S0S</td><td>DMI_S0S</td><td>DMI_S0S</td><td>DMI_S0S_P<3:0></td><td>10 18</td></tr><tr><td>DMI_S0S</td><td>DMI_S0S</td><td>DMI_S0S</td><td>DMI_S0S_N<3:0></td><td>10 18</td></tr><tr><td>FDI_DATA</td><td>FDI_DATA</td><td>FDI_DATA</td><td>FDI_DATA_P<7:0></td><td>9 10</td></tr><tr><td>FDI_DATA</td><td>FDI_DATA</td><td>FDI_DATA</td><td>FDI_DATA_N<7:0></td><td>9 10</td></tr><tr><td>FDI_SYNC</td><td>FDI_SYNC</td><td>FDI_SYNC</td><td>FDI_SYNC<1..0></td><td>9 10</td></tr><tr><td>FDI_SYNC</td><td>FDI_SYNC</td><td>FDI_SYNC</td><td>FDI_SYNC<1..0></td><td>9 10</td></tr><tr><td>FDI_INT</td><td>FDI_INT</td><td>FDI_INT</td><td>FDI_INT</td><td>10 18</td></tr><tr><td>DMI_CLK100M</td><td>DMI_CLK100M</td><td>DMI_CLK100M</td><td>DMI_CLK100M_CPU_P</td><td>11 17</td></tr><tr><td>DMI_CLK100M</td><td>DMI_CLK100M</td><td>DMI_CLK100M</td><td>DMI_CLK100M_CPU_N</td><td>11 17</td></tr><tr><td>DP_INT_IG_ML_P<3:0></td><td>DP_INT_IG_ML_P<3:0></td><td>DP_INT_IG_ML_P<3:0></td><td>DP_INT_IG_ML_P<3:0></td><td>10 82</td></tr><tr><td>DP_INT_IG_ML_N<3:0></td><td>DP_INT_IG_ML_N<3:0></td><td>DP_INT_IG_ML_N<3:0></td><td>DP_INT_IG_ML_N<3:0></td><td>10 82</td></tr><tr><td>DP_INT_IG_AUX_P</td><td>DP_INT_IG_AUX_P</td><td>DP_INT_IG_AUX_P</td><td>DP_INT_IG_AUX_P</td><td>10 82</td></tr><tr><td>DP_INT_IG_AUX_N</td><td>DP_INT_IG_AUX_N</td><td>DP_INT_IG_AUX_N</td><td>DP_INT_IG_AUX_N</td><td>10 82</td></tr><tr><td>CPU_RDP_COMP</td><td>CPU_RDP_COMP</td><td>CPU_RDP_COMP</td><td>CPU_RDP_COMP</td><td>10</td></tr><tr><td>CPU_P00_COMP</td><td>CPU_P00_COMP</td><td>CPU_P00_COMP</td><td>CPU_P00_COMP</td><td>10</td></tr><tr><td>CPU_CPS<17..0></td><td>CPU_CPS<17..0></td><td>CPU_CPS<17..0></td><td>CPU_CPS<17..0></td><td>10 24</td></tr><tr><td>ITPCPU_CLK100M_P</td><td>ITPCPU_CLK100M_P</td><td>ITPCPU_CLK100M_P</td><td>ITPCPU_CLK100M_P</td><td>10 24</td></tr><tr><td>ITPCPU_CLK100M_N</td><td>ITPCPU_CLK100M_N</td><td>ITPCPU_CLK100M_N</td><td>ITPCPU_CLK100M_N</td><td>10 24</td></tr><tr><td>ITXPDP_CLK100M_P</td><td>ITXPDP_CLK100M_P</td><td>ITXPDP_CLK100M_P</td><td>ITXPDP_CLK100M_P</td><td>10 24</td></tr><tr><td>ITXPDP_CLK100M_N</td><td>ITXPDP_CLK100M_N</td><td>ITXPDP_CLK100M_N</td><td>ITXPDP_CLK100M_N</td><td>10 24</td></tr><tr><td>DPLL_RFP_CLKP</td><td>DPLL_RFP_CLKP</td><td>DPLL_RFP_CLKP</td><td>DPLL_RFP_CLKP</td><td>11</td></tr><tr><td>DPLL_RFP_CLKN</td><td>DPLL_RFP_CLKN</td><td>DPLL_RFP_CLKN</td><td>DPLL_RFP_CLKN</td><td>11</td></tr><tr><td>XDP_CPU_TDI</td><td>XDP_CPU_TDI</td><td>XDP_CPU_TDI</td><td>XDP_CPU_TDI</td><td>10 24</td></tr><tr><td>XDP_CPU_TDO</td><td>XDP_CPU_TDO</td><td>XDP_CPU_TDO</td><td>XDP_CPU_TDO</td><td>10 24</td></tr><tr><td>XDP_CPU_TMS</td><td>XDP_CPU_TMS</td><td>XDP_CPU_TMS</td><td>XDP_CPU_TMS</td><td>10 24</td></tr><tr><td>XDP_CPU_TCK</td><td>XDP_CPU_TCK</td><td>XDP_CPU_TCK</td><td>XDP_CPU_TCK</td><td>10 24</td></tr><tr><td>XDP_CPU_TRST_I</td><td>XDP_CPU_TRST_I</td><td>XDP_CPU_TRST_I</td><td>XDP_CPU_TRST_I</td><td>10 24</td></tr><tr><td>XDP_BPM_I<7..3></td><td>XDP_BPM_I<7..3></td><td>XDP_BPM_I<7..3></td><td>XDP_BPM_I<7..3></td><td>10 24</td></tr><tr><td>XDP_BPM_I<7..3></td><td>XDP_BPM_I<7..3></td><td>XDP_BPM_I<7..3></td><td>XDP_BPM_I<7..3></td><td>10 24</td></tr><tr><td>XDP_DMMGMT_I</td><td>XDP_DMMGMT_I</td><td>XDP_DMMGMT_I</td><td>XDP_DMMGMT_I</td><td>10 24 25</td></tr><tr><td>XDP_CPU_PWDY_I</td><td>XDP_CPU_PWDY_I</td><td>XDP_CPU_PWDY_I</td><td>XDP_CPU_PWDY_I</td><td>10 24</td></tr><tr><td>XDP_CPU_PWDY_N</td><td>XDP_CPU_PWDY_N</td><td>XDP_CPU_PWDY_N</td><td>XDP_CPU_PWDY_N</td><td>10 24</td></tr><tr><td>CPU_CATERR_I</td><td>CPU_CATERR_I</td><td>CPU_CATERR_I</td><td>CPU_CATERR_I</td><td>10 81</td></tr><tr><td>CPU_PROC_SEL_I</td><td>CPU_PROC_SEL_I</td><td>CPU_PROC_SEL_I</td><td>CPU_PROC_SEL_I</td><td>10 82</td></tr><tr><td>CPU_PECI</td><td>CPU_PECI</td><td>CPU_PECI</td><td>CPU_PECI</td><td>10 82 83</td></tr><tr><td>CPU_PROCHOT_I</td><td>CPU_PROCHOT_I</td><td>CPU_PROCHOT_I</td><td>CPU_PROCHOT_I</td><td>10 81 82 83</td></tr><tr><td>XDP_CPU_PMSG0</td><td>XDP_CPU_PMSG0</td><td>XDP_CPU_PMSG0</td><td>XDP_CPU_PMSG0</td><td>10</td></tr><tr><td>PM_THRSTCTIP_I</td><td>PM_THRSTCTIP_I</td><td>PM_THRSTCTIP_I</td><td>PM_THRSTCTIP_I</td><td>10 82</td></tr><tr><td>PM_SYNC</td><td>PM_SYNC</td><td>PM_SYNC</td><td>PM_SYNC</td><td>10 82</td></tr><tr><td>PM_MEM_PMSG0</td><td>PM_MEM_PMSG0</td><td>PM_MEM_PMSG0</td><td>PM_MEM_PMSG0</td><td>10 27</td></tr><tr><td>CPU_PMSG0</td><td>CPU_PMSG0</td><td>CPU_PMSG0</td><td>CPU_PMSG0</td><td>10 24</td></tr><tr><td>CPU_ARM_ACMP<2..0></td><td>CPU_ARM_ACMP<2..0></td><td>CPU_ARM_ACMP<2..0></td><td>CPU_ARM_ACMP<2..0></td><td>11</td></tr><tr><td>CPU_VID0P</td><td>CPU_VID0P</td><td>CPU_VID0P</td><td>CPU_VID0P</td><td>10 85</td></tr><tr><td>CPU_VIDREV_I</td><td>CPU_VIDREV_I</td><td>CPU_VIDREV_I</td><td>CPU_VIDREV_I</td><td>10 85</td></tr><tr><td>CPU_VID0A_VID<1..0></td><td>CPU_VID0A_VID<1..0></td><td>CPU_VID0A_VID<1..0></td><td>CPU_VID0A_VID<1..0></td><td>10 85</td></tr><tr><td>CPU_VCCSENSE_P</td><td>CPU_VCCSENSE_P</td><td>CPU_VCCSENSE_P</td><td>CPU_VCCSENSE_P</td><td>10 85</td></tr><tr><td>CPU_VCCSENSE_N</td><td>CPU_VCCSENSE_N</td><td>CPU_VCCSENSE_N</td><td>CPU_VCCSENSE_N</td><td>10 85</td></tr><tr><td>CPU_VCCSENSE_P</td><td>CPU_VCCSENSE_P</td><td>CPU_VCCSENSE_P</td><td>CPU_VCCSENSE_P</td><td>10 87</td></tr><tr><td>CPU_VCCSENSE_N</td><td>CPU_VCCSENSE_N</td><td>CPU_VCCSENSE_N</td><td>CPU_VCCSENSE_N</td><td>10 87</td></tr><tr><td>CPU_A0X_SENSOR_P</td><td>CPU_A0X_SENSOR_P</td><td>CPU_A0X_SENSOR_P</td><td>CPU_A0X_SENSOR_P</td><td>10 85</td></tr><tr><td>CPU_A0X_SENSOR_N</td><td>CPU_A0X_SENSOR_N</td><td>CPU_A0X_SENSOR_N</td><td>CPU_A0X_SENSOR_N</td><td>10 85</td></tr><tr><td>CPU_A0X_VAISENSE_P</td><td>CPU_A0X_VAISENSE_P</td><td>CPU_A0X_VAISENSE_P</td><td>CPU_A0X_VAISENSE_P</td><td>10</td></tr><tr><td>CPU_A0X_VAISENSE_N</td><td>CPU_A0X_VAISENSE_N</td><td>CPU_A0X_VAISENSE_N</td><td>CPU_A0X_VAISENSE_N</td><td>10</td></tr><tr><td>CPU_VCCSENSE</td><td>CPU_VCCSENSE</td><td>CPU_VCCSENSE</td><td>CPU_VCCSENSE</td><td>10 82</td></tr><tr><td>EP0CPU_MEM_VREFDQ_A</td><td>EP0CPU_MEM_VREFDQ_A</td><td>EP0CPU_MEM_VREFDQ_A</td><td>EP0CPU_MEM_VREFDQ_A</td><td>10 23</td></tr><tr><td>EP0CPU_MEM_VREFDQ_B</td><td>EP0CPU_MEM_VREFDQ_B</td><td>EP0CPU_MEM_VREFDQ_B</td><td>EP0CPU_MEM_VREFDQ_B</td><td>10 23</td></tr><tr><td>EP0V75_53_MEM_VREFDQ_A</td><td>EP0V75_53_MEM_VREFDQ_A</td><td>EP0V75_53_MEM_VREFDQ_A</td><td>EP0V75_53_MEM_VREFDQ_A</td><td>10 23 23</td></tr><tr><td>EP0V75_53_MEM_VREFDQ_B</td><td>EP0V75_53_MEM_VREFDQ_B</td><td>EP0V75_53_MEM_VREFDQ_B</td><td>EP0V75_53_MEM_VREFDQ_B</td><td>10 23 23</td></tr><tr><td>EP0V75_53_MEM_VREFDQ_A</td><td>EP0V75_53_MEM_VREFDQ_A</td><td>EP0V75_53_MEM_VREFDQ_A</td><td>EP0V75_53_MEM_VREFDQ_A</td><td>10 23 23</td></tr><tr><td>EP0V75_53_MEM_VREFDQ_B</td><td>EP0V75_53_MEM_VREFDQ_B</td><td>EP0V75_53_MEM_VREFDQ_B</td><td>EP0V75_53_MEM_VREFDQ_B</td><td>10 23 23</td></tr><tr><td>XDP_CLK_1TP</td><td>CLK_PCIE_S0D</td><td>CLK_PCIE_S0D</td><td>XDP_CPU_CLK100M_P</td><td>24</td></tr><tr><td>XDP_CLK_2TP</td><td>CLK_PCIE_S0D</td><td>CLK_PCIE_S0D</td><td>XDP_CPU_CLK100M_N</td><td>24</td></tr><tr><td>PEG_R0D_P<7..0></td><td>PEG_R0D</td><td>PEG_R0D</td><td>PEG_R0D_P<7..0></td><td>10 84</td></tr><tr><td>PEG_R0D_N<7..0></td><td>PEG_R0D</td><td>PEG_R0D</td><td>PEG_R0D_N<7..0></td><td>10 84</td></tr><tr><td>PEG_R2D_C_P<7..0></td><td>PEG_R0D</td><td>PEG_R0D</td><td>PEG_R2D_C_P<7..0></td><td>10 71</td></tr><tr><td>PEG_R2D_C_N<7..0></td><td>PEG_R0D</td><td>PEG_R0D</td><td>PEG_R2D_C_N<7..0></td><td>10 71</td></tr><tr><td>PEG_D2R_P<7..0></td><td>PEG_R0D</td><td>PEG_R0D</td><td>PEG_D2R_P<7..0></td><td>10 71 88</td></tr><tr><td>PEG_D2R_N<7..0></td><td>PEG_R0D</td><td>PEG_R0D</td><td>PEG_D2R_N<7..0></td><td>10 71 88</td></tr><tr><td>PEG_D2R_C_P<7..0></td><td>PEG_R0D</td><td>PEG_R0D</td><td>PEG_D2R_C_P<7..0></td><td>10</td></tr><tr><td>PEG_D2R_C_N<7..0></td><td>PEG_R0D</td><td>PEG_R0D</td><td>PEG_D2R_C_N<7..0></td><td>10</td></tr></table>									ELECTRICAL_CONSTRAINT_SET	NET TYPE				PHYSICAL	SPACING	DMI_S0N	DMI_S0N	DMI_S0N	DMI_S0N_P<3:0>	10 18	DMI_S0N	DMI_S0N	DMI_S0N	DMI_S0N_N<3:0>	10 18	DMI_S0S	DMI_S0S	DMI_S0S	DMI_S0S_P<3:0>	10 18	DMI_S0S	DMI_S0S	DMI_S0S	DMI_S0S_N<3:0>	10 18	FDI_DATA	FDI_DATA	FDI_DATA	FDI_DATA_P<7:0>	9 10	FDI_DATA	FDI_DATA	FDI_DATA	FDI_DATA_N<7:0>	9 10	FDI_SYNC	FDI_SYNC	FDI_SYNC	FDI_SYNC<1..0>	9 10	FDI_SYNC	FDI_SYNC	FDI_SYNC	FDI_SYNC<1..0>	9 10	FDI_INT	FDI_INT	FDI_INT	FDI_INT	10 18	DMI_CLK100M	DMI_CLK100M	DMI_CLK100M	DMI_CLK100M_CPU_P	11 17	DMI_CLK100M	DMI_CLK100M	DMI_CLK100M	DMI_CLK100M_CPU_N	11 17	DP_INT_IG_ML_P<3:0>	DP_INT_IG_ML_P<3:0>	DP_INT_IG_ML_P<3:0>	DP_INT_IG_ML_P<3:0>	10 82	DP_INT_IG_ML_N<3:0>	DP_INT_IG_ML_N<3:0>	DP_INT_IG_ML_N<3:0>	DP_INT_IG_ML_N<3:0>	10 82	DP_INT_IG_AUX_P	DP_INT_IG_AUX_P	DP_INT_IG_AUX_P	DP_INT_IG_AUX_P	10 82	DP_INT_IG_AUX_N	DP_INT_IG_AUX_N	DP_INT_IG_AUX_N	DP_INT_IG_AUX_N	10 82	CPU_RDP_COMP	CPU_RDP_COMP	CPU_RDP_COMP	CPU_RDP_COMP	10	CPU_P00_COMP	CPU_P00_COMP	CPU_P00_COMP	CPU_P00_COMP	10	CPU_CPS<17..0>	CPU_CPS<17..0>	CPU_CPS<17..0>	CPU_CPS<17..0>	10 24	ITPCPU_CLK100M_P	ITPCPU_CLK100M_P	ITPCPU_CLK100M_P	ITPCPU_CLK100M_P	10 24	ITPCPU_CLK100M_N	ITPCPU_CLK100M_N	ITPCPU_CLK100M_N	ITPCPU_CLK100M_N	10 24	ITXPDP_CLK100M_P	ITXPDP_CLK100M_P	ITXPDP_CLK100M_P	ITXPDP_CLK100M_P	10 24	ITXPDP_CLK100M_N	ITXPDP_CLK100M_N	ITXPDP_CLK100M_N	ITXPDP_CLK100M_N	10 24	DPLL_RFP_CLKP	DPLL_RFP_CLKP	DPLL_RFP_CLKP	DPLL_RFP_CLKP	11	DPLL_RFP_CLKN	DPLL_RFP_CLKN	DPLL_RFP_CLKN	DPLL_RFP_CLKN	11	XDP_CPU_TDI	XDP_CPU_TDI	XDP_CPU_TDI	XDP_CPU_TDI	10 24	XDP_CPU_TDO	XDP_CPU_TDO	XDP_CPU_TDO	XDP_CPU_TDO	10 24	XDP_CPU_TMS	XDP_CPU_TMS	XDP_CPU_TMS	XDP_CPU_TMS	10 24	XDP_CPU_TCK	XDP_CPU_TCK	XDP_CPU_TCK	XDP_CPU_TCK	10 24	XDP_CPU_TRST_I	XDP_CPU_TRST_I	XDP_CPU_TRST_I	XDP_CPU_TRST_I	10 24	XDP_BPM_I<7..3>	XDP_BPM_I<7..3>	XDP_BPM_I<7..3>	XDP_BPM_I<7..3>	10 24	XDP_BPM_I<7..3>	XDP_BPM_I<7..3>	XDP_BPM_I<7..3>	XDP_BPM_I<7..3>	10 24	XDP_DMMGMT_I	XDP_DMMGMT_I	XDP_DMMGMT_I	XDP_DMMGMT_I	10 24 25	XDP_CPU_PWDY_I	XDP_CPU_PWDY_I	XDP_CPU_PWDY_I	XDP_CPU_PWDY_I	10 24	XDP_CPU_PWDY_N	XDP_CPU_PWDY_N	XDP_CPU_PWDY_N	XDP_CPU_PWDY_N	10 24	CPU_CATERR_I	CPU_CATERR_I	CPU_CATERR_I	CPU_CATERR_I	10 81	CPU_PROC_SEL_I	CPU_PROC_SEL_I	CPU_PROC_SEL_I	CPU_PROC_SEL_I	10 82	CPU_PECI	CPU_PECI	CPU_PECI	CPU_PECI	10 82 83	CPU_PROCHOT_I	CPU_PROCHOT_I	CPU_PROCHOT_I	CPU_PROCHOT_I	10 81 82 83	XDP_CPU_PMSG0	XDP_CPU_PMSG0	XDP_CPU_PMSG0	XDP_CPU_PMSG0	10	PM_THRSTCTIP_I	PM_THRSTCTIP_I	PM_THRSTCTIP_I	PM_THRSTCTIP_I	10 82	PM_SYNC	PM_SYNC	PM_SYNC	PM_SYNC	10 82	PM_MEM_PMSG0	PM_MEM_PMSG0	PM_MEM_PMSG0	PM_MEM_PMSG0	10 27	CPU_PMSG0	CPU_PMSG0	CPU_PMSG0	CPU_PMSG0	10 24	CPU_ARM_ACMP<2..0>	CPU_ARM_ACMP<2..0>	CPU_ARM_ACMP<2..0>	CPU_ARM_ACMP<2..0>	11	CPU_VID0P	CPU_VID0P	CPU_VID0P	CPU_VID0P	10 85	CPU_VIDREV_I	CPU_VIDREV_I	CPU_VIDREV_I	CPU_VIDREV_I	10 85	CPU_VID0A_VID<1..0>	CPU_VID0A_VID<1..0>	CPU_VID0A_VID<1..0>	CPU_VID0A_VID<1..0>	10 85	CPU_VCCSENSE_P	CPU_VCCSENSE_P	CPU_VCCSENSE_P	CPU_VCCSENSE_P	10 85	CPU_VCCSENSE_N	CPU_VCCSENSE_N	CPU_VCCSENSE_N	CPU_VCCSENSE_N	10 85	CPU_VCCSENSE_P	CPU_VCCSENSE_P	CPU_VCCSENSE_P	CPU_VCCSENSE_P	10 87	CPU_VCCSENSE_N	CPU_VCCSENSE_N	CPU_VCCSENSE_N	CPU_VCCSENSE_N	10 87	CPU_A0X_SENSOR_P	CPU_A0X_SENSOR_P	CPU_A0X_SENSOR_P	CPU_A0X_SENSOR_P	10 85	CPU_A0X_SENSOR_N	CPU_A0X_SENSOR_N	CPU_A0X_SENSOR_N	CPU_A0X_SENSOR_N	10 85	CPU_A0X_VAISENSE_P	CPU_A0X_VAISENSE_P	CPU_A0X_VAISENSE_P	CPU_A0X_VAISENSE_P	10	CPU_A0X_VAISENSE_N	CPU_A0X_VAISENSE_N	CPU_A0X_VAISENSE_N	CPU_A0X_VAISENSE_N	10	CPU_VCCSENSE	CPU_VCCSENSE	CPU_VCCSENSE	CPU_VCCSENSE	10 82	EP0CPU_MEM_VREFDQ_A	EP0CPU_MEM_VREFDQ_A	EP0CPU_MEM_VREFDQ_A	EP0CPU_MEM_VREFDQ_A	10 23	EP0CPU_MEM_VREFDQ_B	EP0CPU_MEM_VREFDQ_B	EP0CPU_MEM_VREFDQ_B	EP0CPU_MEM_VREFDQ_B	10 23	EP0V75_53_MEM_VREFDQ_A	EP0V75_53_MEM_VREFDQ_A	EP0V75_53_MEM_VREFDQ_A	EP0V75_53_MEM_VREFDQ_A	10 23 23	EP0V75_53_MEM_VREFDQ_B	EP0V75_53_MEM_VREFDQ_B	EP0V75_53_MEM_VREFDQ_B	EP0V75_53_MEM_VREFDQ_B	10 23 23	EP0V75_53_MEM_VREFDQ_A	EP0V75_53_MEM_VREFDQ_A	EP0V75_53_MEM_VREFDQ_A	EP0V75_53_MEM_VREFDQ_A	10 23 23	EP0V75_53_MEM_VREFDQ_B	EP0V75_53_MEM_VREFDQ_B	EP0V75_53_MEM_VREFDQ_B	EP0V75_53_MEM_VREFDQ_B	10 23 23	XDP_CLK_1TP	CLK_PCIE_S0D	CLK_PCIE_S0D	XDP_CPU_CLK100M_P	24	XDP_CLK_2TP	CLK_PCIE_S0D	CLK_PCIE_S0D	XDP_CPU_CLK100M_N	24	PEG_R0D_P<7..0>	PEG_R0D	PEG_R0D	PEG_R0D_P<7..0>	10 84	PEG_R0D_N<7..0>	PEG_R0D	PEG_R0D	PEG_R0D_N<7..0>	10 84	PEG_R2D_C_P<7..0>	PEG_R0D	PEG_R0D	PEG_R2D_C_P<7..0>	10 71	PEG_R2D_C_N<7..0>	PEG_R0D	PEG_R0D	PEG_R2D_C_N<7..0>	10 71	PEG_D2R_P<7..0>	PEG_R0D	PEG_R0D	PEG_D2R_P<7..0>	10 71 88	PEG_D2R_N<7..0>	PEG_R0D	PEG_R0D	PEG_D2R_N<7..0>	10 71 88	PEG_D2R_C_P<7..0>	PEG_R0D	PEG_R0D	PEG_D2R_C_P<7..0>	10	PEG_D2R_C_N<7..0>	PEG_R0D	PEG_R0D
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XDP_BPM_I<7..3>	XDP_BPM_I<7..3>	XDP_BPM_I<7..3>	XDP_BPM_I<7..3>	10 24																																																																																																																																																																																																																																																																																																																																																																																		
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XDP_DMMGMT_I	XDP_DMMGMT_I	XDP_DMMGMT_I	XDP_DMMGMT_I	10 24 25																																																																																																																																																																																																																																																																																																																																																																																		
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM BECK WIDTH	MAXIMUM BECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR BECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20OTHER	*	25 MILS	?
MEM_DQBL2BL	*	16 MILS	?
MEM_DQCH2CH	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_*	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_*	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	*	*	MEM_20OTHER

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.

A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.

DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.

Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Chief River SFF Platform DG, Rev 0.7 (#460452), Section 2.6.3

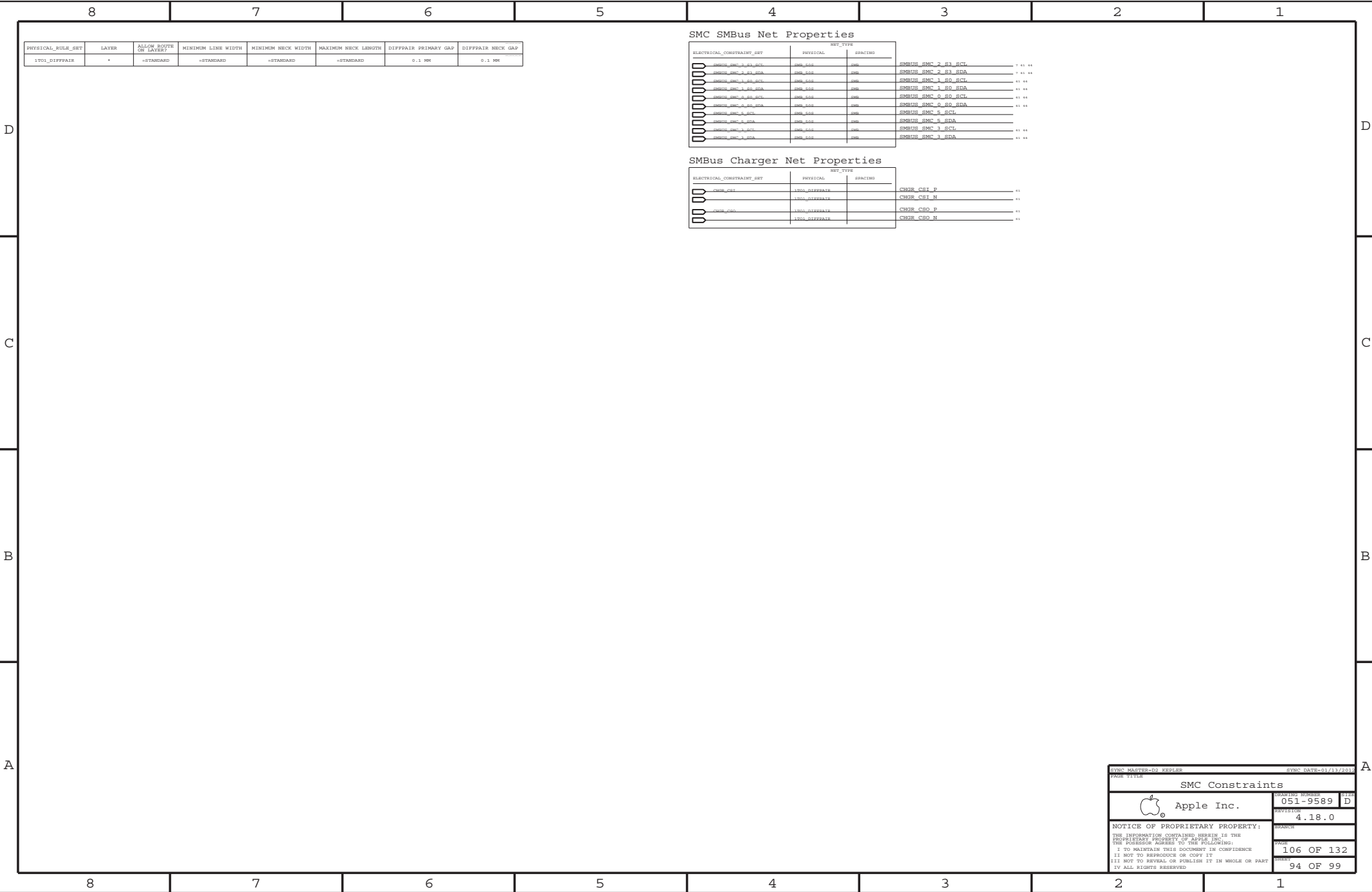
Memory Net Properties

ELECTRICAL_CONSTRAINT_SET		NET TYPE		
		PHYSICAL	SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK P<5..0>	12 00 00 00
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK N<5..0>	12 00 00 00
MEM_A_CKE1	MEM_17S	MEM_CTRL	MEM_A_CKE<3..0>	12 00 00 00
MEM_A_CKE1	MEM_17S	MEM_CTRL	MEM_A_CS L<3..2>	12 00 00 00
MEM_A_CKE1	MEM_17S	MEM_CTRL	MEM_A_CS L<4>	12 00 00 00
MEM_A_CKE1	MEM_17S	MEM_CTRL	MEM_A_CS L<5>	12 00 00 00
MEM_A_CKE1	MEM_17S	MEM_CTRL	MEM_A_ODT<3..2>	12 00 00 00
MEM_A_CKE1	MEM_17S	MEM_CTRL	MEM_A_ODT<1>	12 00 00 00
MEM_A_CKE1	MEM_17S	MEM_CTRL	MEM_A_ODT<0>	12 00 00 00
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	12 00 00 00
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	12 00 00 00
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS L	12 00 00 00
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS L	12 00 00 00
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WR L	12 00 00 00
MEM_A_DQ_BVTE0	MEM_50S	MEM_A_DQ_BVTE0	MEM_A_DQ<7..0>	12 00 00 00
MEM_A_DQ_BVTE1	MEM_50S	MEM_A_DQ_BVTE1	MEM_A_DQ<15..8>	12 00 00 00
MEM_A_DQ_BVTE2	MEM_50S	MEM_A_DQ_BVTE2	MEM_A_DQ<23..16>	12 00 00 00
MEM_A_DQ_BVTE3	MEM_50S	MEM_A_DQ_BVTE3	MEM_A_DQ<31..24>	12 00 00 00
MEM_A_DQ_BVTE4	MEM_50S	MEM_A_DQ_BVTE4	MEM_A_DQ<39..32>	12 00 00 00
MEM_A_DQ_BVTE5	MEM_50S	MEM_A_DQ_BVTE5	MEM_A_DQ<47..40>	12 00 00 00
MEM_A_DQ_BVTE6	MEM_50S	MEM_A_DQ_BVTE6	MEM_A_DQ<55..48>	12 00 00 00
MEM_A_DQ_BVTE7	MEM_50S	MEM_A_DQ_BVTE7	MEM_A_DQ<63..56>	12 00 00 00
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS P<0>	12 00 00 00
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS N<0>	12 00 00 00
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS P<1>	12 00 00 00
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS N<1>	12 00 00 00
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS P<2>	12 00 00 00
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS N<2>	12 00 00 00
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS P<3>	12 00 00 00
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS N<3>	12 00 00 00
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS P<4>	12 00 00 00
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS N<4>	12 00 00 00
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS P<5>	12 00 00 00
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS N<5>	12 00 00 00
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS P<6>	12 00 00 00
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS N<6>	12 00 00 00
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS P<7>	12 00 00 00
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS N<7>	12 00 00 00
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK P<5..0>	12 00 00 00
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK N<5..0>	12 00 00 00
MEM_B_CKE1	MEM_17S	MEM_CTRL	MEM_B_CKE<3..2>	12 00 00 00
MEM_B_CKE1	MEM_17S	MEM_CTRL	MEM_B_CKE<1>	12 00 00 00
MEM_B_CKE1	MEM_17S	MEM_CTRL	MEM_B_CKE<0>	12 00 00 00
MEM_B_CKE1	MEM_17S	MEM_CTRL	MEM_B_CS L<3..0>	12 00 00 00
MEM_B_CKE1	MEM_17S	MEM_CTRL	MEM_B_ODT<3..1>	12 00 00 00
MEM_B_CKE1	MEM_17S	MEM_CTRL	MEM_B_ODT<0>	12 00 00 00
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..7>	12 00 00 00
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<6>	12 00 00 00
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<5..0>	12 00 00 00
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	12 00 00 00
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS L	12 00 00 00
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS L	12 00 00 00
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WR L	12 00 00 00
MEM_B_DQ_BVTE0	MEM_50S	MEM_B_DQ_BVTE0	MEM_B_DQ<7..0>	12 00 00 00
MEM_B_DQ_BVTE1	MEM_50S	MEM_B_DQ_BVTE1	MEM_B_DQ<15..8>	12 00 00 00
MEM_B_DQ_BVTE2	MEM_50S	MEM_B_DQ_BVTE2	MEM_B_DQ<23..16>	12 00 00 00
MEM_B_DQ_BVTE3	MEM_50S	MEM_B_DQ_BVTE3	MEM_B_DQ<31..24>	12 00 00 00
MEM_B_DQ_BVTE4	MEM_50S	MEM_B_DQ_BVTE4	MEM_B_DQ<39..32>	12 00 00 00
MEM_B_DQ_BVTE5	MEM_50S	MEM_B_DQ_BVTE5	MEM_B_DQ<47..40>	12 00 00 00
MEM_B_DQ_BVTE6	MEM_50S	MEM_B_DQ_BVTE6	MEM_B_DQ<55..48>	12 00 00 00
MEM_B_DQ_BVTE7	MEM_50S	MEM_B_DQ_BVTE7	MEM_B_DQ<63..56>	12 00 00 00
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS P<0>	12 00 00 00
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS N<0>	12 00 00 00
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS P<1>	12 00 00 00
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS N<1>	12 00 00 00
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS P<2>	12 00 00 00
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS N<2>	12 00 00 00
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS P<3>	12 00 00 00
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS N<3>	12 00 00 00
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS P<4>	12 00 00 00
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS N<4>	12 00 00 00
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS P<5>	12 00 00 00
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS N<5>	12 00 00 00
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS P<6>	12 00 00 00
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS N<6>	12 00 00 00
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS P<7>	12 00 00 00
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS N<7>	12 00 00 00

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PAGE TITLE					
Memory Constraints					
Apple Inc.		REVISION	D		
		DATE	4.18.0		
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Digital Video Signal Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_DP_90D	*	=+90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_90D	*	=+90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_DISPLAYPORT	TOP,BOTTOM	=+11_SPACING	?	PCH_DISPLAYPORT	TOP,BOTTOM	=+11_SPACING	?
LVDS	TOP,BOTTOM	=+11_SPACING	?	LVDS	TOP,BOTTOM	=+11_SPACING	?
SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193							
SATA Interface Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=+90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_375E	*	=+37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_505E	*	=+50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=+51_SPACING	?	SATA	TOP,BOTTOM	=+51_SPACING	?
SATA_10CMP	*	15 MIL	?				
SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193							
USB 2.0 Interface Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_81A5	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=+85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=+11_SPACING	?	USB	TOP,BOTTOM	=+11_SPACING	?
USB_81A5	*	15 MIL	?				
SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193							
USB 3.0 INTERFACE CONSTRAINTS							
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	TOP,BOTTOM	=+11_SPACING	?	USB3	TOP,BOTTOM	=+11_SPACING	?
SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+							
System Clock Signal Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2X_DIELECTRIC	?				
CLK_25M	*	=5X_DIELECTRIC	?				
NOTE: 25MHz system clocks very sensitive to noise.							
PCH Net Properties							
ELECTRICAL_CONSTRAINT_SET				NET_TYPE			
				PHYSICAL SPACING			
LVDS_IG_A_CLK_P	LVDS_90D	LVDS	LVDS_IG_A_CLK_P	10	10	10	10
LVDS_IG_A_CLK_N	LVDS_90D	LVDS	LVDS_IG_A_CLK_N	10	10	10	10
LVDS_IG_A_DATA_P<2..0>	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<2..0>	10	10	10	10
LVDS_IG_A_DATA_N<2..0>	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<2..0>	10	10	10	10
LVDS_IG_A_DATA_P<3>	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<3>	10	10	10	10
LVDS_IG_A_DATA_N<3>	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<3>	10	10	10	10
LVDS_IG_B_DATA_P<2..0>	LVDS_90D	LVDS	LVDS_IG_B_DATA_P<2..0>	10	10	10	10
LVDS_IG_B_DATA_N<2..0>	LVDS_90D	LVDS	LVDS_IG_B_DATA_N<2..0>	10	10	10	10
SATA_HDD_R2D_C_P	SATA_90D	SATA	SATA_HDD_R2D_C_P	17	17	17	17
SATA_HDD_R2D_C_N	SATA_90D	SATA	SATA_HDD_R2D_C_N	17	17	17	17
SATA_HDD_R2D_P	SATA_90D	SATA	SATA_HDD_R2D_P	17	17	17	17
SATA_HDD_R2D_N	SATA_90D	SATA	SATA_HDD_R2D_N	17	17	17	17
SATA_SSD_R2D_MUX_OUT_P	SATA_90D	SATA	SATA_SSD_R2D_MUX_OUT_P	19	19	19	19
SATA_SSD_R2D_MUX_OUT_N	SATA_90D	SATA	SATA_SSD_R2D_MUX_OUT_N	19	19	19	19
SATA_SSD_R2D_MUX_IN_P	SATA_90D	SATA	SATA_SSD_R2D_MUX_IN_P	19	19	19	19
SATA_SSD_R2D_MUX_IN_N	SATA_90D	SATA	SATA_SSD_R2D_MUX_IN_N	19	19	19	19
SATA_SSD_R2D_P	SATA_90D	SATA	SATA_SSD_R2D_P	19	19	19	19
SATA_SSD_R2D_N	SATA_90D	SATA	SATA_SSD_R2D_N	19	19	19	19
SATA_HDD_R2D_IF_P	SATA_90D	SATA	SATA_HDD_R2D_IF_P	19	19	19	19
SATA_HDD_R2D_IF_N	SATA_90D	SATA	SATA_HDD_R2D_IF_N	19	19	19	19
SATA_ODD_R2D_C_P	SATA_90D	SATA	SATA_ODD_R2D_C_P	17	17	17	17
SATA_ODD_R2D_C_N	SATA_90D	SATA	SATA_ODD_R2D_C_N	17	17	17	17
SATA_ODD_R2D_P	SATA_90D	SATA	SATA_ODD_R2D_P	17	17	17	17
SATA_ODD_R2D_N	SATA_90D	SATA	SATA_ODD_R2D_N	17	17	17	17
SATA_ODD_R2D_MUX_OUT_P	SATA_90D	SATA	SATA_ODD_R2D_MUX_OUT_P	19	19	19	19
SATA_ODD_R2D_MUX_OUT_N	SATA_90D	SATA	SATA_ODD_R2D_MUX_OUT_N	19	19	19	19
PCH_SATA1COMP	SATA_10CMP	SATA_10CMP	PCH_SATA1COMP	17	17	17	17
PCH_SATA1COMP	SATA_10CMP	SATA_10CMP	PCH_SATA1COMP	17	17	17	17
USB_EXTB_XHCI_P	USB_85D	USB	USB_EXTB_XHCI_P	19	19	19	19
USB_EXTB_XHCI_N	USB_85D	USB	USB_EXTB_XHCI_N	19	19	19	19
USB_EXTB_XHCI_P	USB_85D	USB	USB_EXTB_XHCI_P	19	19	19	19
USB_EXTB_XHCI_N	USB_85D	USB	USB_EXTB_XHCI_N	19	19	19	19
USB_HUB_UP_P	USB_85D	USB	USB_HUB_UP_P	19	19	19	19
USB_HUB_UP_N	USB_85D	USB	USB_HUB_UP_N	19	19	19	19
USB_EXT_A_P	USB_85D	USB	USB_EXT_A_P	19	19	19	19
USB_EXT_A_N	USB_85D	USB	USB_EXT_A_N	19	19	19	19
USB_EXT_B_P	USB_85D	USB	USB_EXT_B_P	19	19	19	19
USB_EXT_B_N	USB_85D	USB	USB_EXT_B_N	19	19	19	19
USB_EXT_C_P	USB_85D	USB	USB_EXT_C_P	19	19	19	19
USB_EXT_C_N	USB_85D	USB	USB_EXT_C_N	19	19	19	19
USB_CAMERA_CONN_P	USB_85D	USB	USB_CAMERA_CONN_P	19	19	19	19
USB_CAMERA_CONN_N	USB_85D	USB	USB_CAMERA_CONN_N	19	19	19	19
USB_BT_P	USB_85D	USB	USB_BT_P	19	19	19	19
USB_BT_N	USB_85D	USB	USB_BT_N	19	19	19	19
USB_BT_CONN_P	USB_85D	USB	USB_BT_CONN_P	19	19	19	19
USB_BT_CONN_N	USB_85D	USB	USB_BT_CONN_N	19	19	19	19
USB_BT_WAKE_P	USB_85D	USB	USB_BT_WAKE_P	19	19	19	19
USB_BT_WAKE_N	USB_85D	USB	USB_BT_WAKE_N	19	19	19	19
USB_TPAD_P	USB_85D	USB	USB_TPAD_P	19	19	19	19
USB_TPAD_N	USB_85D	USB	USB_TPAD_N	19	19	19	19
USB_I2C_P	USB_85D	USB	USB_I2C_P	19	19	19	19
USB_I2C_N	USB_85D	USB	USB_I2C_N	19	19	19	19
PCH_USB_81A5	PCH_USB_81A5	PCH_USB_81A5	PCH_USB_81A5	19	19	19	19
PCH_USB_81A5	PCH_USB_81A5	PCH_USB_81A5	PCH_USB_81A5	19	19	19	19
USB_EXTD_XHCI_P	USB_85D	USB	USB_EXTD_XHCI_P	19	19	19	19
USB_EXTD_XHCI_N	USB_85D	USB	USB_EXTD_XHCI_N	19	19	19	19
USB_EXT_A_MUXED_P	USB_85D	USB	USB_EXT_A_MUXED_P	19	19	19	19
USB_EXT_A_MUXED_N	USB_85D	USB	USB_EXT_A_MUXED_N	19	19	19	19
USB_CAMERA_P	USB_85D	USB	USB_CAMERA_P	19	19	19	19
USB_CAMERA_N	USB_85D	USB	USB_CAMERA_N	19	19	19	19
USB_I2T1_P	USB_85D	USB	USB_I2T1_P	19	19	19	19
USB_I2T1_N	USB_85D	USB	USB_I2T1_N	19	19	19	19
USB3_EXTX_TX_P	USB3_85D	USB3	USB3_EXTX_TX_P	19	19	19	19
USB3_EXTX_TX_N	USB3_85D	USB3	USB3_EXTX_TX_N	19	19	19	19
USB3_EXTX_RX_P	USB3_85D	USB3	USB3_EXTX_RX_P	19	19	19	19
USB3_EXTX_RX_N	USB3_85D	USB3	USB3_EXTX_RX_N	19	19	19	19
USB3_EXTX_TX_P	USB3_85D	USB3	USB3_EXTX_TX_P	19	19	19	19
USB3_EXTX_TX_N	USB3_85D	USB3	USB3_EXTX_TX_N	19	19	19	19
USB3_EXTX_RX_P	USB3_85D	USB3	USB3_EXTX_RX_P	19	19	19	19
USB3_EXTX_RX_N	USB3_85D	USB3	USB3_EXTX_RX_N	19	19	19	19
USB3_EXTX_TX_P	USB3_85D	USB3	USB3_EXTX_TX_P	19	19	19	19
USB3_EXTX_TX_N	USB3_85D	USB3	USB3_EXTX_TX_N	19	19	19	19
USB3_EXTX_RX_P	USB3_85D	USB3	USB3_EXTX_RX_P	19	19	19	19
USB3_EXTX_RX_N	USB3_85D	USB3	USB3_EXTX_RX_N	19	19	19	19
USB3_EXTX_TX_P	USB3_85D	USB3	USB3_EXTX_TX_P	19	19	19	19
USB3_EXTX_TX_N	USB3_85D	USB3	USB3_EXTX_TX_N	19	19	19	19
USB3_EXTX_RX_P	USB3_85D	USB3	USB3_EXTX_RX_P	19	19	19	19
USB3_EXTX_RX_N	USB3_85D	USB3	USB3_EXTX_RX_N	19	19	19	19
Clock Net Properties							
ELECTRICAL_CONSTRAINT_SET				NET_TYPE			
				PHYSICAL SPACING			
SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	19	19	19	19
SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	19	19	19	19
SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	19	19	19	19
SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT	19	19	19	19
SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT	19	19	19	19
SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT	19	19	19	19
SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+							
PCH Constraints 1							
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D	LPC Bus Constraints											
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP				
	LPC_SSS	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD				
C	CLC_LPC_SSS	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD				
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT								
	LPC	*	6 MIL	7								
B	CLC_LPC	*	8 MIL	7								
	SMBus Interface Constraints											
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP				
A	SMB_SSS	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD				
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT								
	SMB	*	=2x_DIELECTRIC	7								
	HD Audio Interface Constraints											
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP				
	HDA_SSS	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD				
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT								
	HDA	*	=2x_DIELECTRIC	7								
	SIO Signal Constraints											
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH					MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	CLC_SIO_SSS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD				
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT								
	CLC_SIO	*	8 MIL	7								
	SPI Interface Constraints											
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH					MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	SPI_SSS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD				
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT								
	SPI	*	8 MIL	7								
PCH Net Properties												
ELECTRICAL_CONSTRAINT_SET			NET_TYPE									
			PHYSICAL	SPACING								
1	LPC_AD3	LPC_SSS	LPC	LPC	LPC_AD3_0x	7	17	41	42	43		
2	LPC_FRAME_I	LPC_SSS	LPC	LPC	LPC_FRAME_I	7	17	41	42	43		
3	LPC_RESET_I	LPC_SSS	LPC	LPC	LPC_RESET_I	7	17	41	42	43		
4	LPC_CLK33M_RMC_R	CLC_LPC_SSS	CLC_LPC	CLC	LPC_CLK33M_RMC_R	17	44					
5	LPC_CLK33M_RMC	CLC_LPC_SSS	CLC_LPC	CLC	LPC_CLK33M_RMC	17	44					
6	LPC_CLK33M_LPCDIO0	CLC_LPC_SSS	CLC_LPC	CLC	LPC_CLK33M_LPCDIO0	17	44					
7	SMBUS_FCH_CLK	SMB_SSS	SMB	SMB	SMBUS_FCH_CLK	17	44					
8	SMBUS_FCH_DATA	SMB_SSS	SMB	SMB	SMBUS_FCH_DATA	17	44					
9	SMB_FCH_0_CLK	SMB_SSS	SMB	SMB	SMB_FCH_0_CLK	17	44					
10	SMB_FCH_0_DATA	SMB_SSS	SMB	SMB	SMB_FCH_0_DATA	17	44					
11	SMB_FCH_1_CLK	SMB_SSS	SMB	SMB	SMB_FCH_1_CLK	17	44					
12	SMB_FCH_1_DATA	SMB_SSS	SMB	SMB	SMB_FCH_1_DATA	17	44					
13	HDA_BIT_CLK	HDA_SSS	HDA	HDA	HDA_BIT_CLK	17	44					
14	HDA_BIT_CLK_R	HDA_SSS	HDA	HDA	HDA_BIT_CLK_R	17	44					
15	HDA_SYNC	HDA_SSS	HDA	HDA	HDA_SYNC	17	44					
16	HDA_SYNC_R	HDA_SSS	HDA	HDA	HDA_SYNC_R	17	44					
17	HDA_RST_I	HDA_SSS	HDA	HDA	HDA_RST_I	17	44					
18	HDA_RST_I	HDA_SSS	HDA	HDA	HDA_RST_I	17	44					
19	HDA_RST0	HDA_SSS	HDA	HDA	HDA_RST0	17	44					
20	AUD_SDI_R	HDA_SSS	HDA	HDA	AUD_SDI_R	17	44					
21	HDA_SDO0T	HDA_SSS	HDA	HDA	HDA_SDO0T	17	44					
22	HDA_SDO0T_R	HDA_SSS	HDA	HDA	HDA_SDO0T_R	17	44					
23	SPI_CLK	SPI_SSS	SPI	SPI	SPI_CLK_R	17	44					
24	SPI_CLK	SPI_SSS	SPI	SPI	SPI_CLK	17	44					
25	SPI_M0ST	SPI_SSS	SPI	SPI	SPI_M0ST_R	17	44					
26	SPI_M0ST	SPI_SSS	SPI	SPI	SPI_M0ST	17	44					
27	SPI_MISO	SPI_SSS	SPI	SPI	SPI_MISO	17	44					
28	SPI_CSD_I	SPI_SSS	SPI	SPI	SPI_CSD_I	17	44					
29	SPI_CSD_I	SPI_SSS	SPI	SPI	SPI_CSD_I	17	44					
30	PCI0_ENET_R2D_P	PCI0_SSS	PCI0	PCI0	PCI0_ENET_R2D_P	17	44					
31	PCI0_ENET_R2D_N	PCI0_SSS	PCI0	PCI0	PCI0_ENET_R2D_N	17	44					
32	PCI0_ENET_R2D_C_P	PCI0_SSS	PCI0	PCI0	PCI0_ENET_R2D_C_P	17	44					
33	PCI0_ENET_R2D_C_N	PCI0_SSS	PCI0	PCI0	PCI0_ENET_R2D_C_N	17	44					
34	PCI0_ENET_D2R_P	PCI0_SSS	PCI0	PCI0	PCI0_ENET_D2R_P	17	44					
35	PCI0_ENET_D2R_N	PCI0_SSS	PCI0	PCI0	PCI0_ENET_D2R_N	17	44					
36	PCI0_ENET_D2R_C_P	PCI0_SSS	PCI0	PCI0	PCI0_ENET_D2R_C_P	17	44					
37	PCI0_ENET_D2R_C_N	PCI0_SSS	PCI0	PCI0	PCI0_ENET_D2R_C_N	17	44					
38	PCI0_AP_R2D_P	PCI0_SSS	PCI0	PCI0	PCI0_AP_R2D_P	17	44					
39	PCI0_AP_R2D_N	PCI0_SSS	PCI0	PCI0	PCI0_AP_R2D_N	17	44					
40	PCI0_AP_R2D_C_P	PCI0_SSS	PCI0	PCI0	PCI0_AP_R2D_C_P	17	44					
41	PCI0_AP_R2D_C_N	PCI0_SSS	PCI0	PCI0	PCI0_AP_R2D_C_N	17	44					
42	PCI0_AP_D2R_P	PCI0_SSS	PCI0	PCI0	PCI0_AP_D2R_P	17	44					
43	PCI0_AP_D2R_N	PCI0_SSS	PCI0	PCI0	PCI0_AP_D2R_N	17	44					
44	PCI0_AP_D2R_P1_P	PCI0_SSS	PCI0	PCI0	PCI0_AP_D2R_P1_P	17	44					
45	PCI0_AP_D2R_P1_N	PCI0_SSS	PCI0	PCI0	PCI0_AP_D2R_P1_N	17	44					
46	PCI0_AP_R2D_P1_P	PCI0_SSS	PCI0	PCI0	PCI0_AP_R2D_P1_P	17	44					
47	PCI0_AP_R2D_P1_N	PCI0_SSS	PCI0	PCI0	PCI0_AP_R2D_P1_N	17	44					
48	PCI0_TPT_D2R	PCI0_SSS	PCI0	PCI0	PCI0_SSD_D2R_MUX_OUT_P	17	44					
49	PCI0_TPT_D2R	PCI0_SSS	PCI0	PCI0	PCI0_SSD_D2R_MUX_OUT_N	17	44					
50	PCI0_TPT_R2D	PCI0_SSS	PCI0	PCI0	PCI0_SSD_R2D_C_P<1..0>	17	44					
51	PCI0_TPT_R2D	PCI0_SSS	PCI0	PCI0	PCI0_SSD_R2D_C_N<1..0>	17	44					
52	PCI0_TPT_D2R	PCI0_SSS	PCI0	PCI0	PCI0_SSD_D2R_P<1..0>	17	44					
53	PCI0_TPT_D2R	PCI0_SSS	PCI0	PCI0	PCI0_SSD_R2D_N<1..0>	17	44					
54	PCI0_TPT_R2D	PCI0_SSS	PCI0	PCI0	PCI0_SSD_R2D_MUX_IN_P	17	44					
55	PCI0_TPT_R2D	PCI0_SSS	PCI0	PCI0	PCI0_SSD_R2D_MUX_IN_N	17	44					
56	PCI0_TPT_D2R	PCI0_SSS	PCI0	PCI0	PCI0_SSD_D2R_C_P<1>	17	44					
57	PCI0_TPT_R2D	PCI0_SSS	PCI0	PCI0	PCI0_SSD_D2R_C_N<1>	17	44					
58	PCI0_TPT_R2D	PCI0_SSS	PCI0	PCI0	PCI0_SSD_R2D_P<1>	17	44					
59	PCI0_TPT_R2D	PCI0_SSS	PCI0	PCI0	PCI0_SSD_R2D_N<1>	17	44					
60	PCI0_CLK100M	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_PCH_P	17	44					
61	PCI0_CLK100M	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_PCH_N	17	44					
62	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
63	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
64	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
65	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
66	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
67	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
68	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
69	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
70	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
71	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
72	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
73	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
74	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
75	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
76	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
77	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
78	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
79	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
80	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
81	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
82	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
83	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
84	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
85	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
86	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
87	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
88	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
89	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
90	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
91	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
92	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
93	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
94	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
95	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
96	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
97	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
98	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_P	17	44					
99	PCI0_CLK100M_TBT_N	CLC_PCI0_SSS	CLC_PCI0	CLC	PCI0_CLK100M_TBT_N	17	44					
100	PCI0_CLK100M_TBT_P	CLC_PCI0_SSS	CLC_PCI0	CLC								



PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1Y01_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMCUS_SMC_2_S3_SCT	SMC_SCS	SMC	SMBUS_SMC_2_S3_SCT	17 41 44
SMCUS_SMC_2_S3_SDA	SMC_SCS	SMC	SMBUS_SMC_2_S3_SDA	17 41 44
SMCUS_SMC_3_S0_SCT	SMC_SCS	SMC	SMBUS_SMC_3_S0_SCT	41 44
SMCUS_SMC_3_S0_SDA	SMC_SCS	SMC	SMBUS_SMC_3_S0_SDA	41 44
SMCUS_SMC_0_S0_SCT	SMC_SCS	SMC	SMBUS_SMC_0_S0_SCT	41 44
SMCUS_SMC_0_S0_SDA	SMC_SCS	SMC	SMBUS_SMC_0_S0_SDA	41 44
SMCUS_SMC_5_SCT	SMC_SCS	SMC	SMBUS_SMC_5_SCT	
SMCUS_SMC_5_SDA	SMC_SCS	SMC	SMBUS_SMC_5_SDA	
SMCUS_SMC_3_SCT	SMC_SCS	SMC	SMBUS_SMC_3_SCT	41 44
SMCUS_SMC_3_SDA	SMC_SCS	SMC	SMBUS_SMC_3_SDA	41 44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CHGR_CSI	1Y01_DIFFPAIR		CHGR_CSI_P	41
CHGR_CSI	1Y01_DIFFPAIR		CHGR_CSI_N	41
CHGR_CSO	1Y01_DIFFPAIR		CHGR_CSO_P	41
CHGR_CSO	1Y01_DIFFPAIR		CHGR_CSO_N	41

SYMC MASTER-03 REPLIER

SYMC DATE=01/11/2013

PAGE TITLE

SMC Constraints

Apple Inc.

051-9589

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4.18.0

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SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

