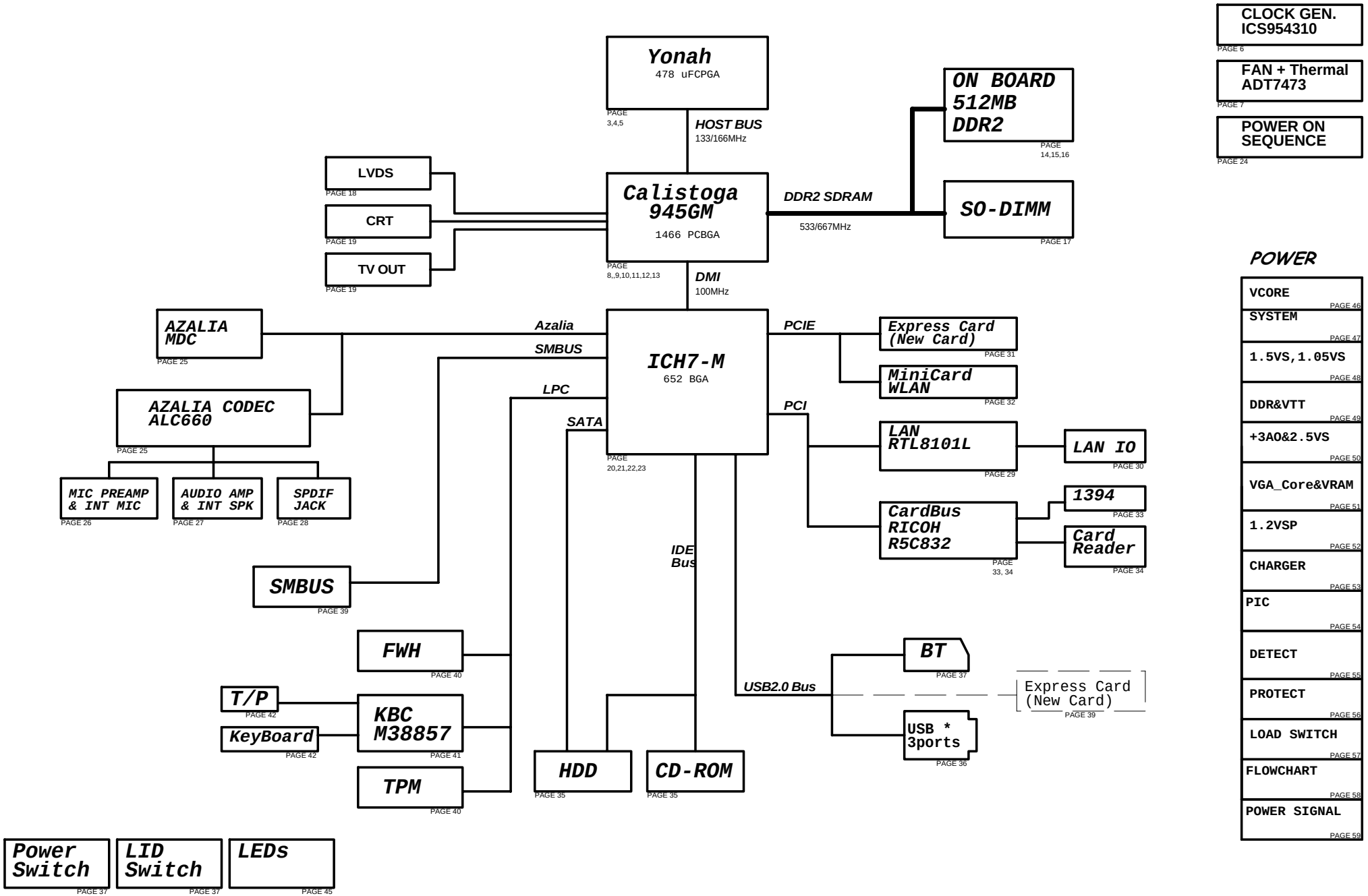
W6F: YONAH/CALISTOGA-GM BLOCK DIAGRAM

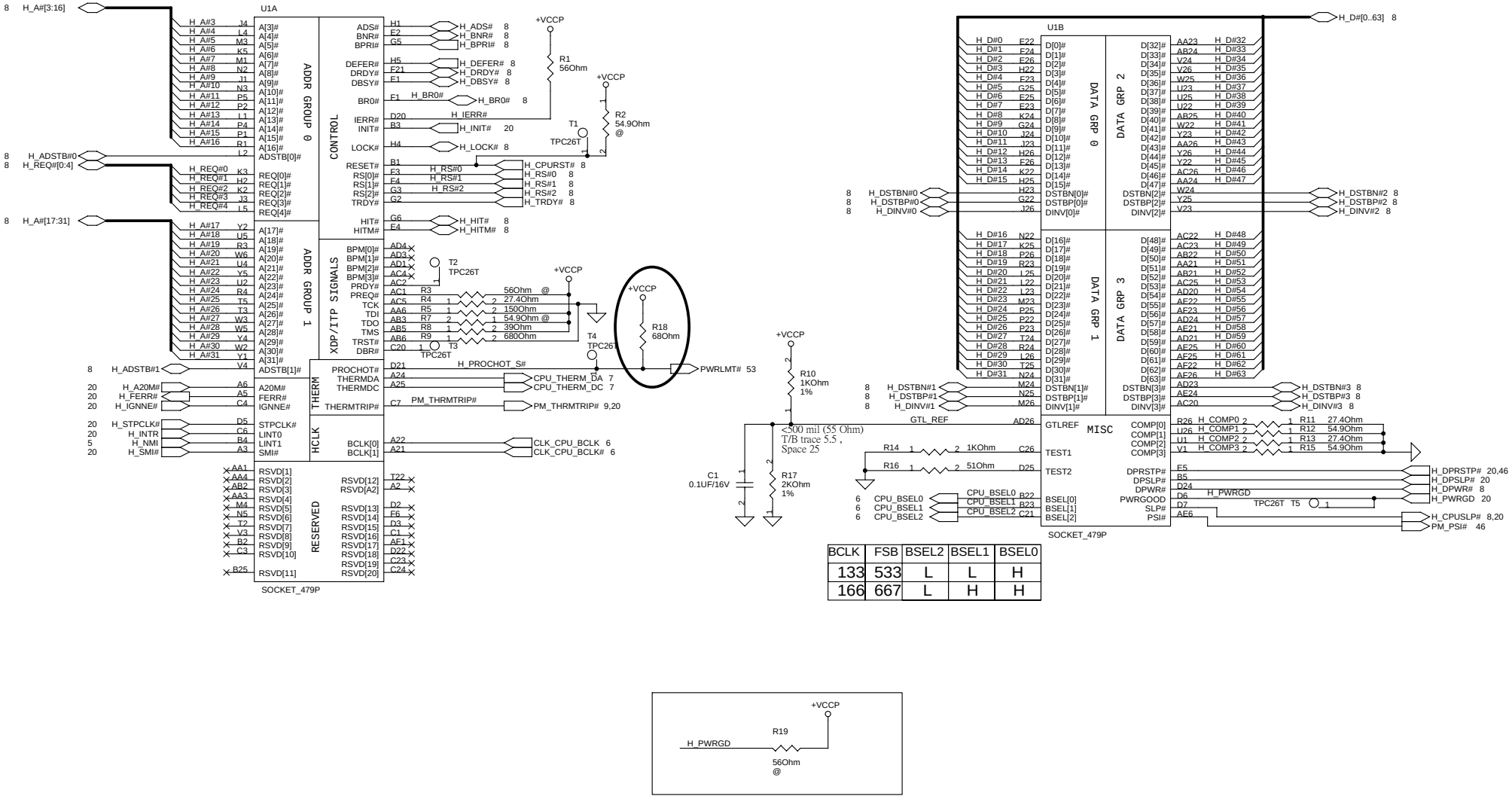


PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: BLOCK DIAGRAM	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 1 OF 60		LIBRARY DATE :	

PAGE	Content
	W6F PAGE REF.
1	Block Diagram
2	Page Reference
3	YONAH CPU (1)
4	YONAH CPU (2)
5	DEBUG PORT
6	CLOCK GENERATOR
7	Fan & Thermal Sensor
8	Calistoga - HOST (1)
9	Calistoga - DMI, DISPLAY (2)
10	Calistoga -DDR BUS (3)
11	Calistoga - POWER(4)
12	Calistoga - GROUND (5)
13	Calistoga - STRAPPING (6)
14	ON BOARD DDR2 (1)
15	ON BOARD DDR2 (2)
16	ON BOARD TERMINATION
17	DDR2 SO-DIMM
18	LVDS & INVERTER
19	CRT & TV OUT
20	ICH7M - LPC, IDE (1)
21	ICH7M - DMI, USB, PCIE (2)
22	ICH7M - SM BUS, GPIO(3)
23	ICH7M - POWER, GND (4)
24	RESET CIRCUIT
25	AZALIA CODEC - ALC660
26	MIC PRE-AMP & INT MIC
27	AUDIO AMP & INT SPK
28	SPDIF & AUDIO BOARD CONN
29	10/100 Mbps LAN - RTL8101L
30	LAN IO & MDC
31	EXPRESS CARD
32	MINI CARD - GOLAN
33	RICOH R5C832 -1394 (1)
34	RICOH R5C832 - PCI, 4IN1 CARD (2)
35	HDD & CDROM CONN
36	USB 2.0 CONN * 3
37	BLUETOOTH & EXT. BOARD
38	N/A
39	SM BUS & RTC CONN
40	TPM 1.2 & FWH
41	KEYBOARD CONTROLLER (M3885)
42	INTERNAL KEYBOARD & TOUCH PAD
43	DISCHARGE & POWER RAIL
44	DC IN JACK & BAT CONN
45	LEDs
46	POWER - VCORE
47	POWER - SYSTEM
48	POWER - I/O, +1.5VS, +1.05VS
49	POWER - DDR2, VTT
50	POWER - +3VA, +2.5VS
51	POWER - VGA CORE & VRAM (N/A)
52	POWER - +1.2VSP (N/A)
53	POWER - CHARGER
54	POWER - PIC
55	POWER - POWER DETECT
56	POWER - POWER PROTECT
57	POWER - LOAD SWITCH

PAGE	
58	POWER - FLOW CHART
59	POWER - SIGNAL
60	REVISION HISTORY

P/N: 12G04600479A

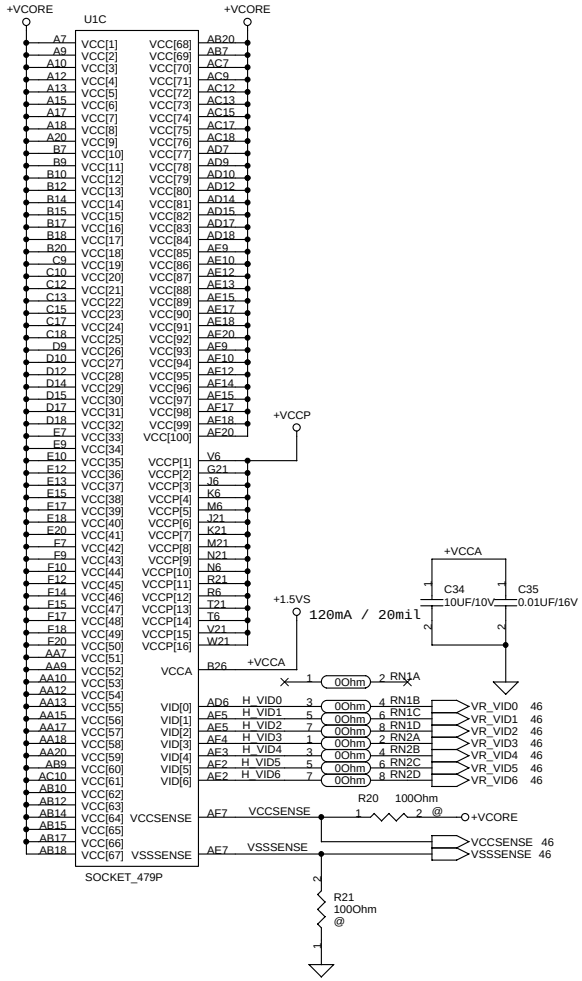


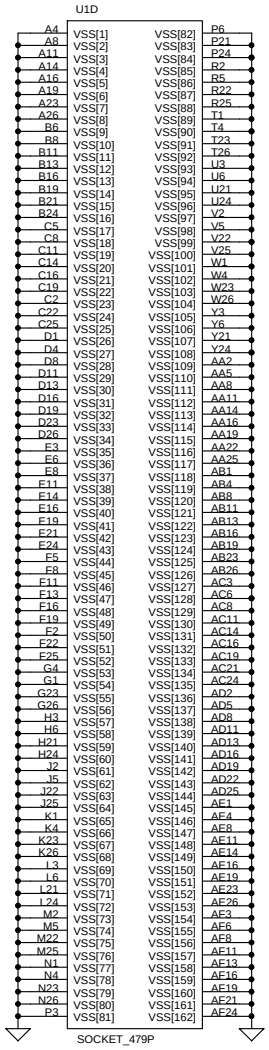
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

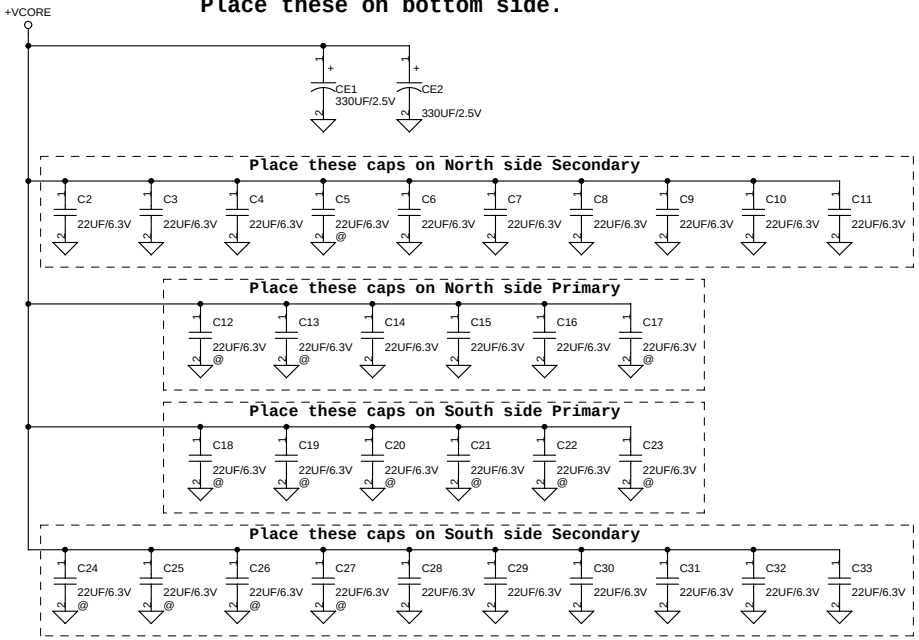
PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	SHEET 3 OF 60	DESCRIPTION: YONAH CPU (1)	SCHEMATIC FILE NAME : <Doc> LIBRARY DATE :	DESIGN ENGINEER : George Chen

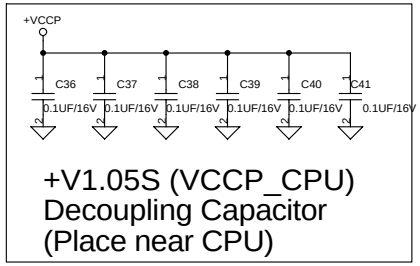
YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

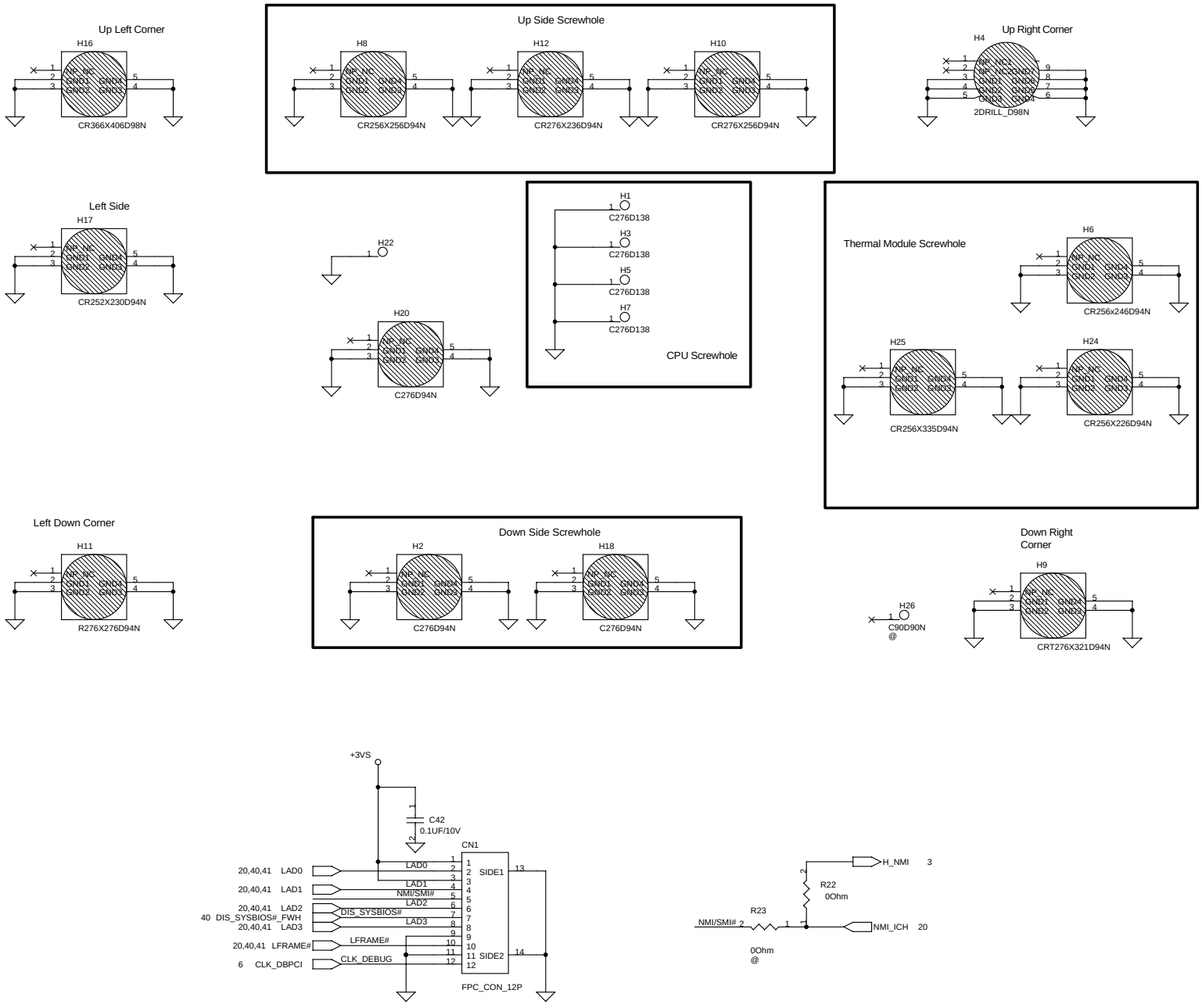




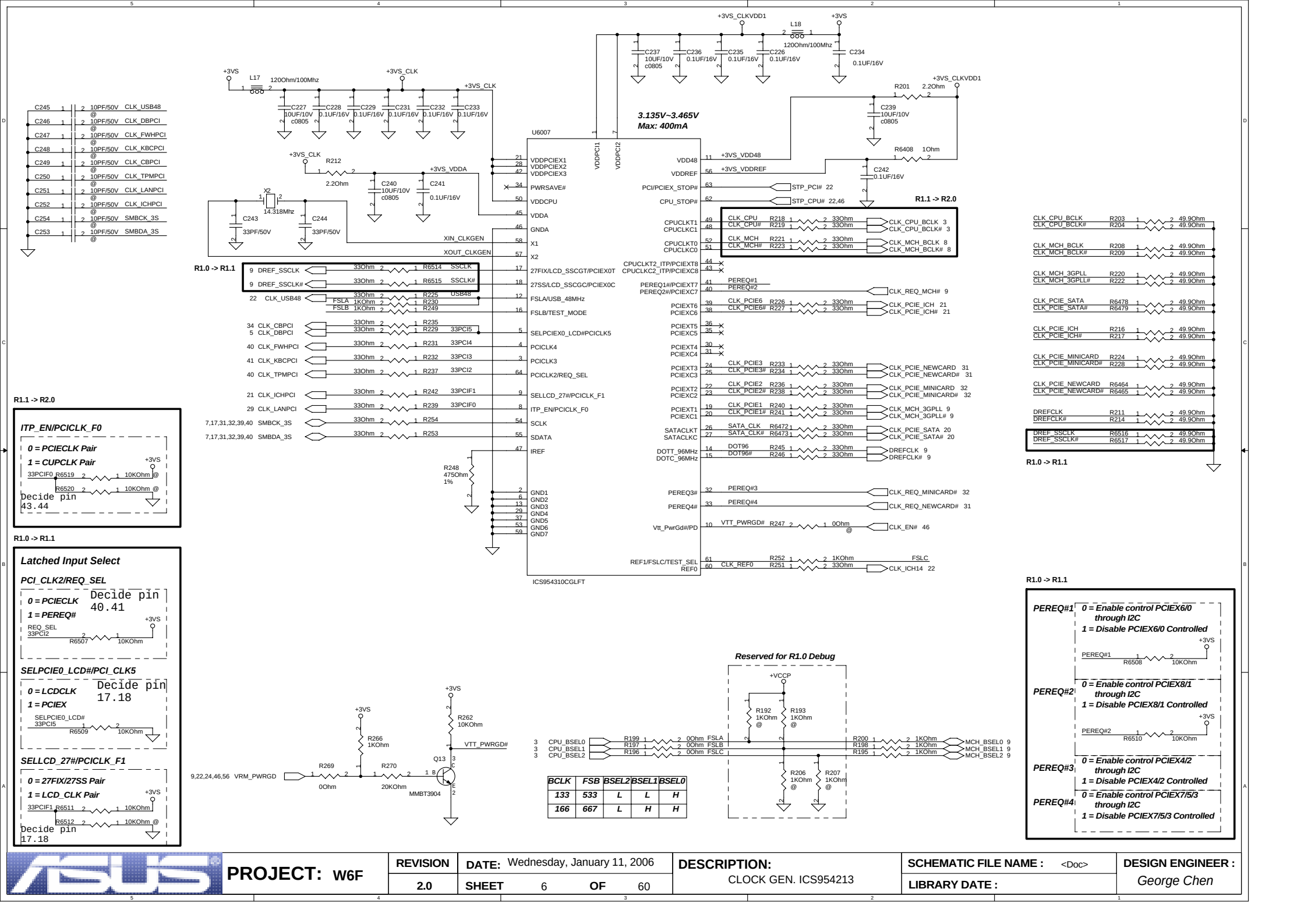




PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: YONAH CPU (2)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 4 OF 60		LIBRARY DATE :	

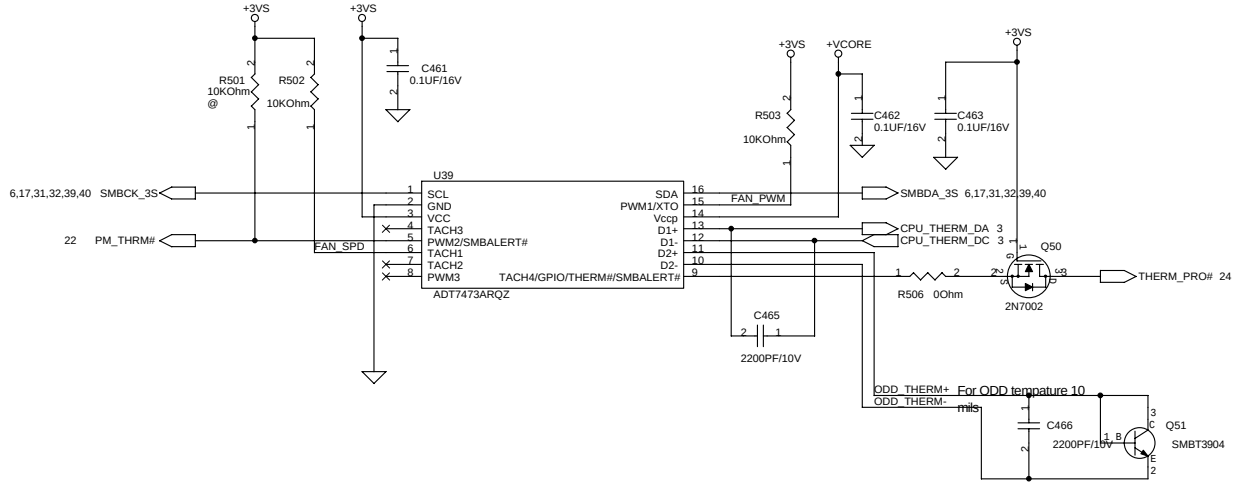


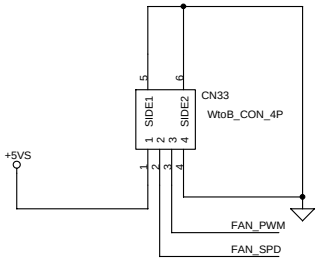
PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** DEBUG PORT	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** *George Chen*
		SHEET 5 **OF** 60		**LIBRARY DATE :**	



PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006 SHEET 6 OF 60	DESCRIPTION: CLOCK GEN. ICS954213	SCHEMATIC FILE NAME : <Doc> LIBRARY DATE :	DESIGN ENGINEER : George Chen

FAN

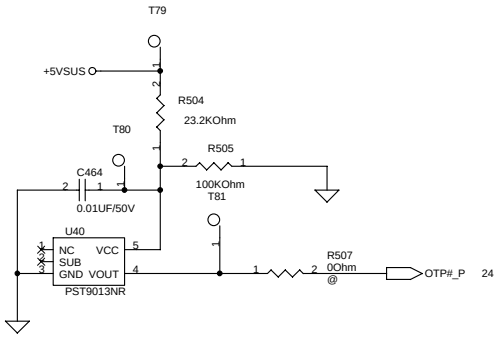




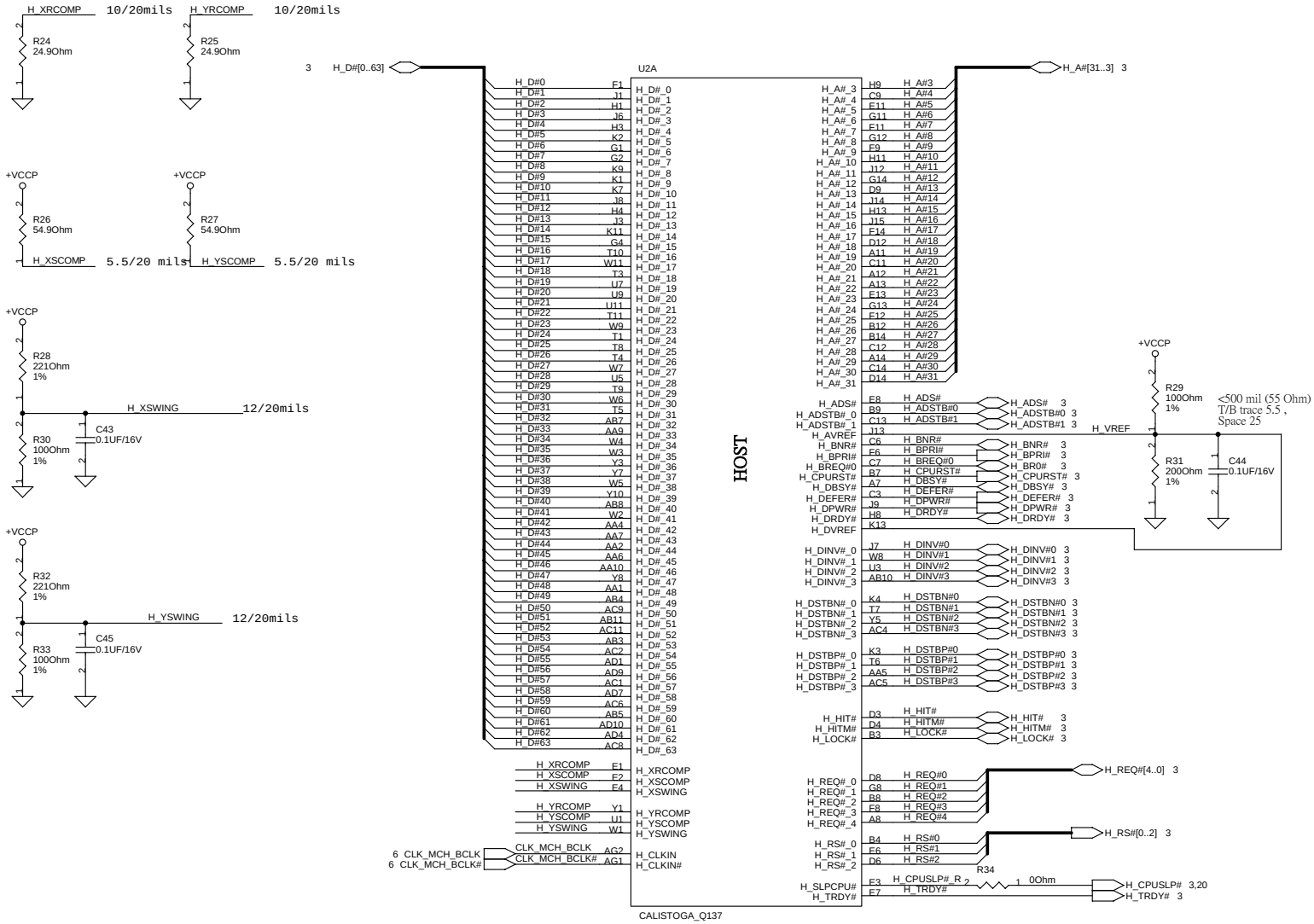
95 DEGREE C
THERMAL PROTECTION
PLACE UNDER CPU

R173==> 23.3k==>95 degree c

R173==> 33.2k==>80 degree c

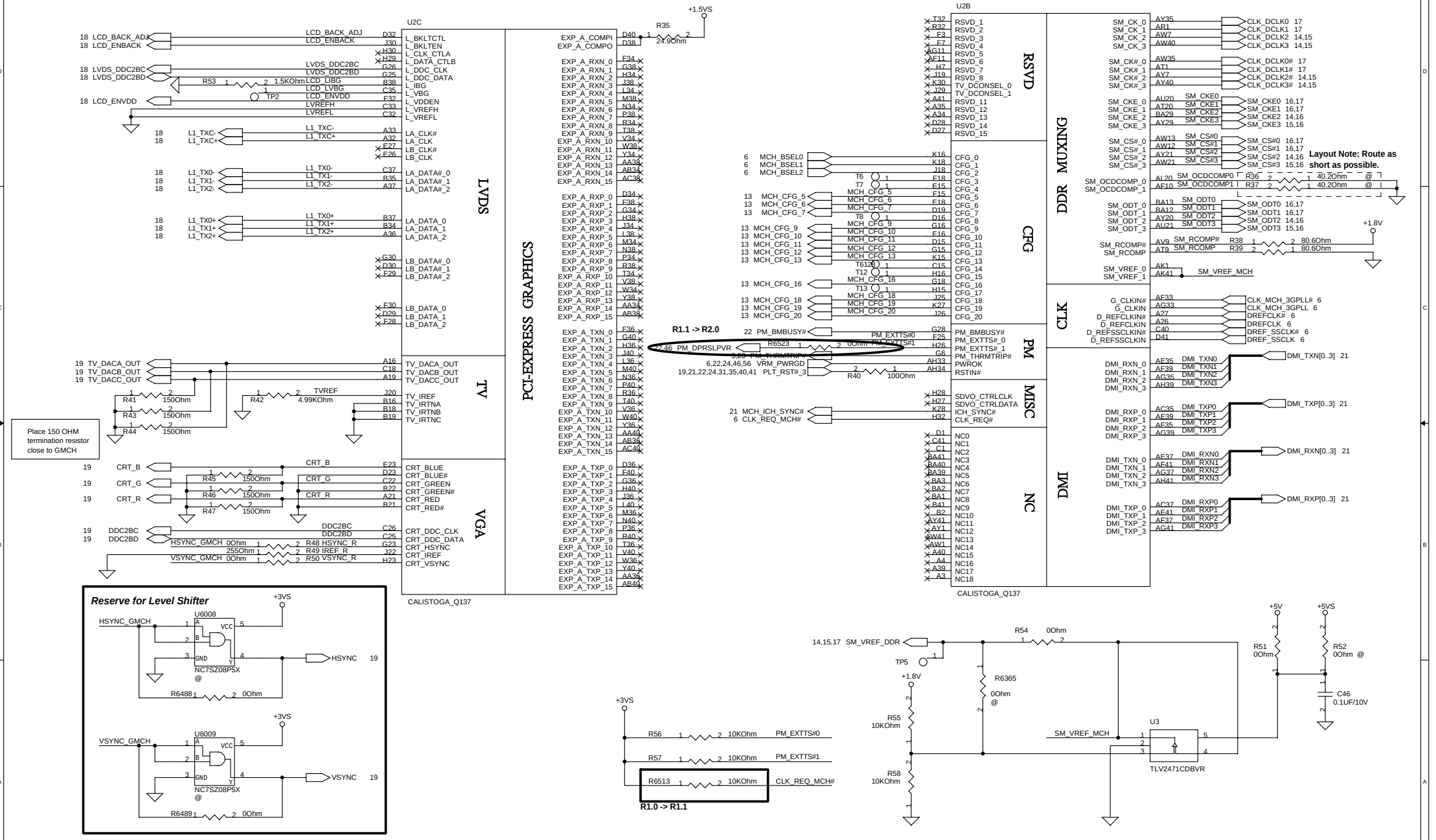


PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006 **SHEET** 7 **OF** 60	**DESCRIPTION:** FAN & THERMAL SENSOR	**SCHEMATIC FILE NAME :** <Doc> **LIBRARY DATE :**	**DESIGN ENGINEER :** *George Chen*

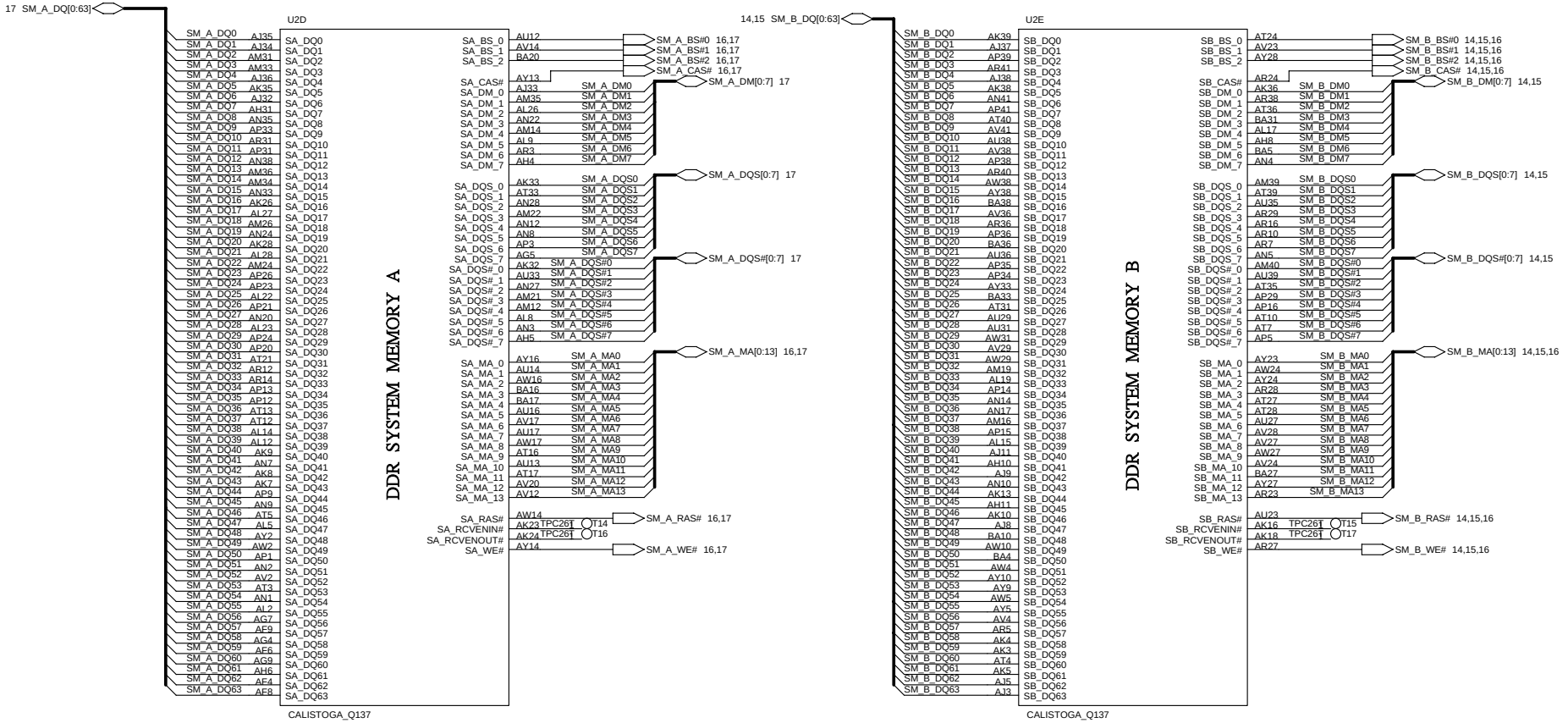


PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** Calistoga - HOST(1)	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** *George Chen*
		SHEET 8 **OF** 60		**LIBRARY DATE :**	

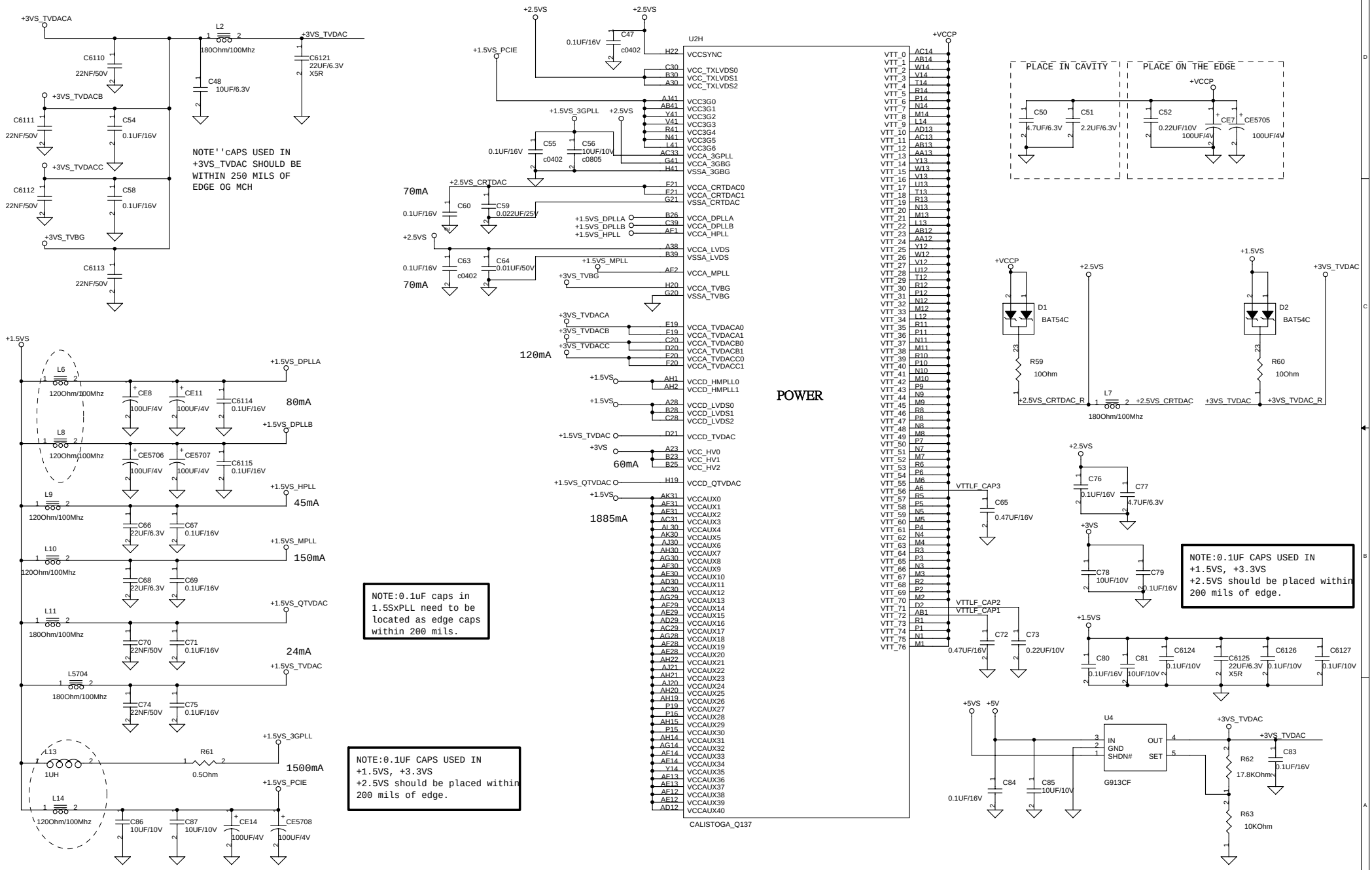
1.4A



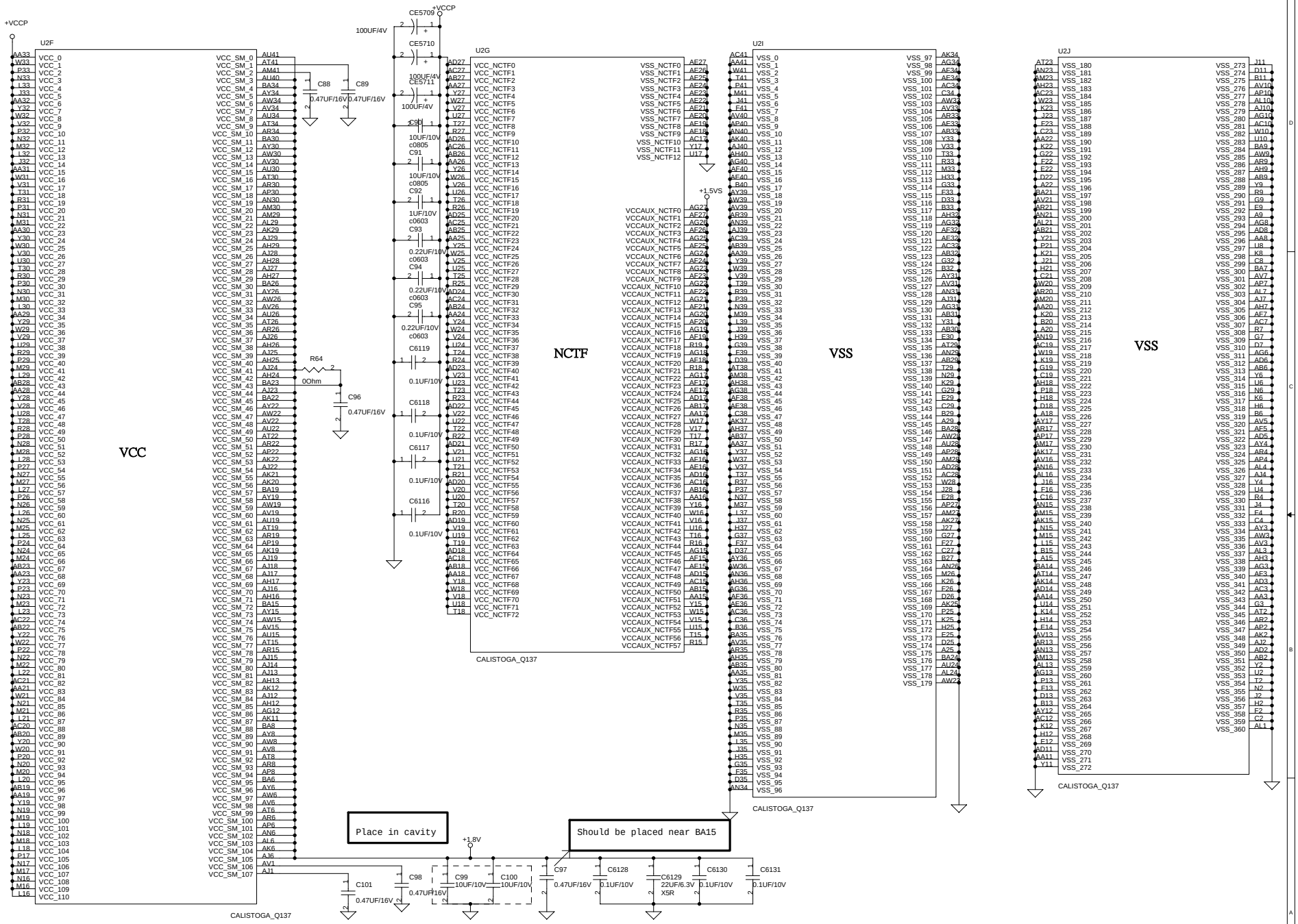
PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: Calistoga - DMI, DISPLAY(2)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 9 OF 60		LIBRARY DATE :	



PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** Calistoga - DDR BUS(3)	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** *George Chen*
		SHEET 10 **OF** 60		**LIBRARY DATE :**	



PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** Calistoga - POWER(4)	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** *George Chen*
		SHEET 11 **OF** 60		**LIBRARY DATE :**	

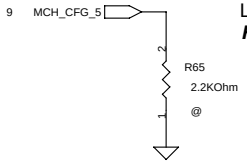


ASUS	**PROJECT:** W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006 **SHEET** 12 **OF** 60	**DESCRIPTION:** Calistoga - GND(5)	**SCHEMATIC FILE NAME :** <Doc> **LIBRARY DATE :**	**DESIGN ENGINEER :** *George Chen*

CFG5 : DMI STRAP

LOW = DMI X 2

HIGH = DMI X 4 (Default)

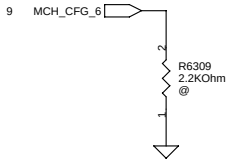


CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

CFG6 : DDR

LOW = MOBY DICK

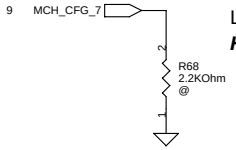
HIGH = CALISTGA

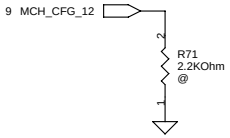


CFG7 : CPU STRAP

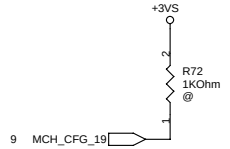
LOW = Mobile Prescott

HIGH = Dothan CPU (Default)





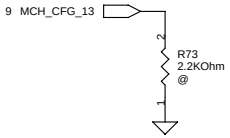
XOR/ALL-Z

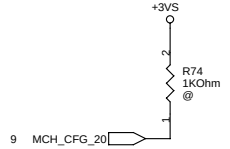


CFG19 : DMI LANE REVERSAL

LOW = NORMAL

HIGH = LANES REVERSED





CFG20 : PCIE BACKWARDIN INTERPOERABILITY MODE

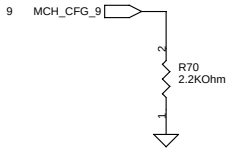
LOW = DEFAULT

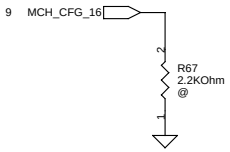
HIGH = SDVO AND PCIE *1 ARE OPEATING SIMULTANEOUSLY VIA THE PRG PORT

CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE

HIGH = NORMAL OPERATION (Default)





CFG16 : FSB DYNAMIC ODT

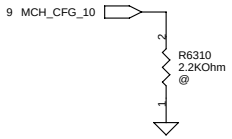
LOW = Dynamic ODT Disabled

HIGH = Dynamic ODT Enabled (Default)

CFG10 : HOST PLL VCC SELECT

LOW = REVERSE LANE

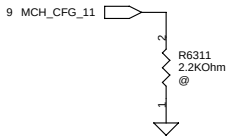
HIGH = MOBILITY



CFG11 : FSB 4X CLK ENABLE

LOW = REVERSE LANE

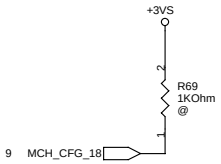
HIGH = CALISTOGA



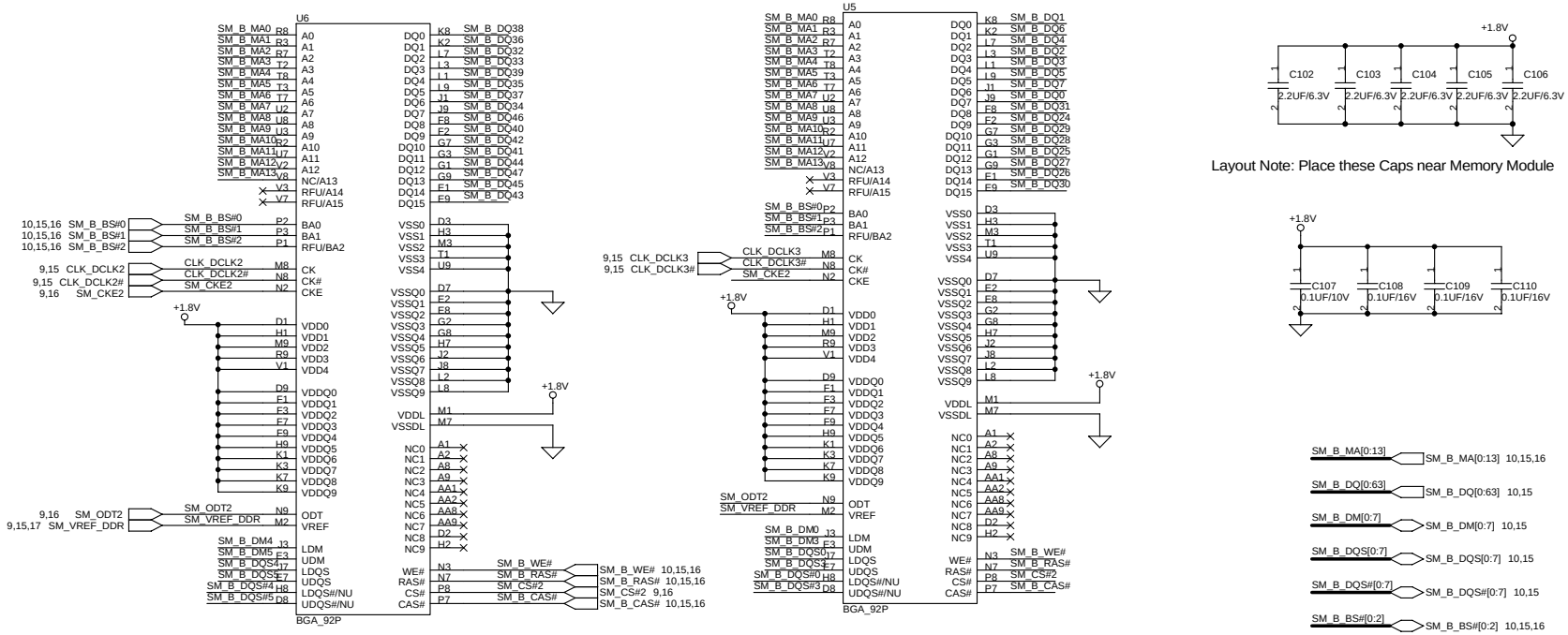
CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)

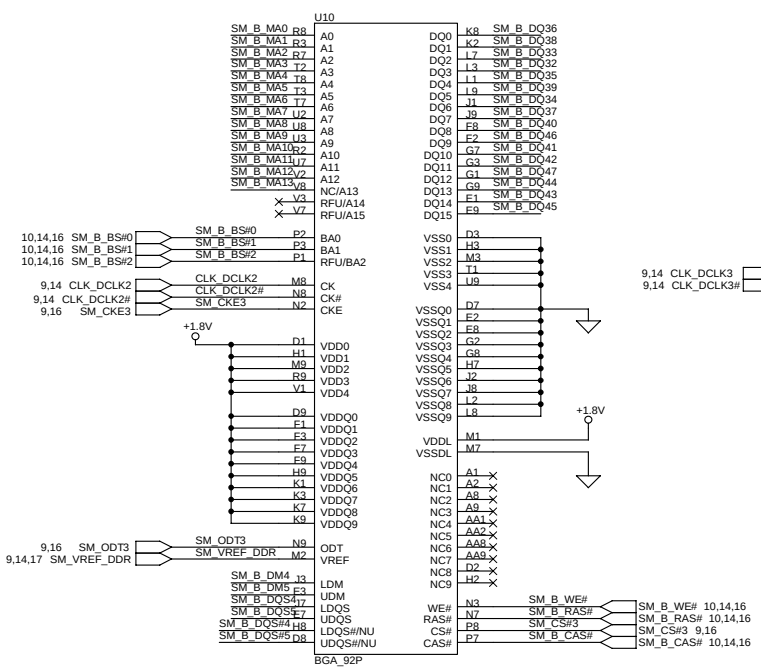
HIGH = 1.5V

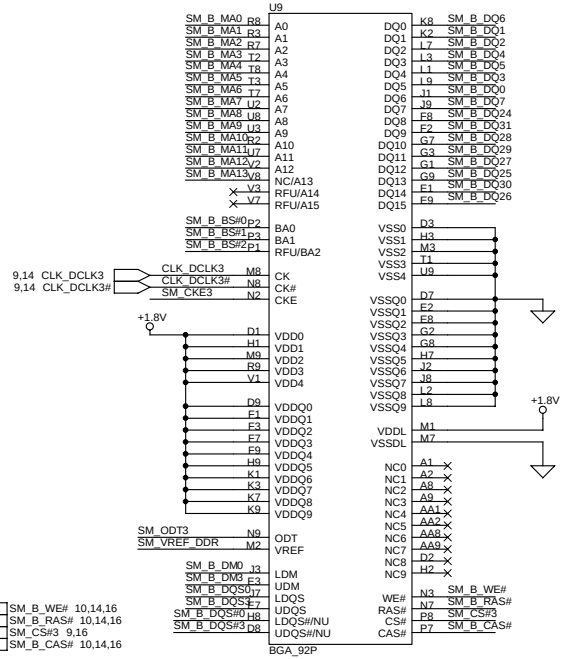


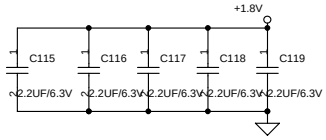
PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006 **SHEET** 13 **OF** 60	**DESCRIPTION:** Calistoga - Strapping(6)	**SCHEMATIC FILE NAME :** <Doc> **LIBRARY DATE :**	**DESIGN ENGINEER :** *George Chen*



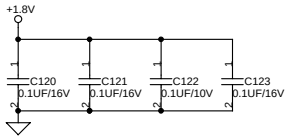
PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** ON BOARD DDR2(1)	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** George Chen
		SHEET 14 **OF** 60		**LIBRARY DATE :**	

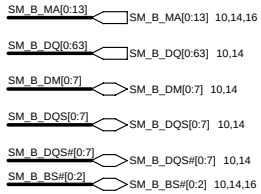


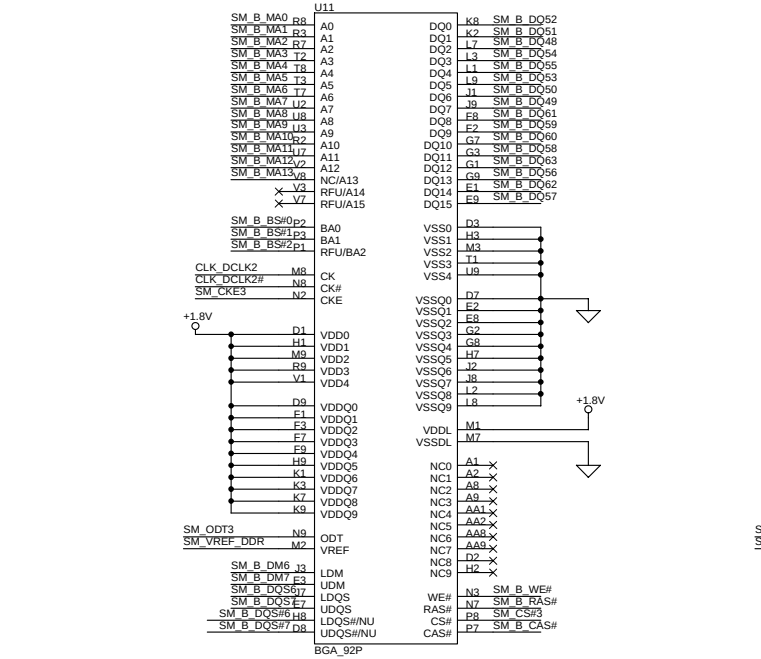


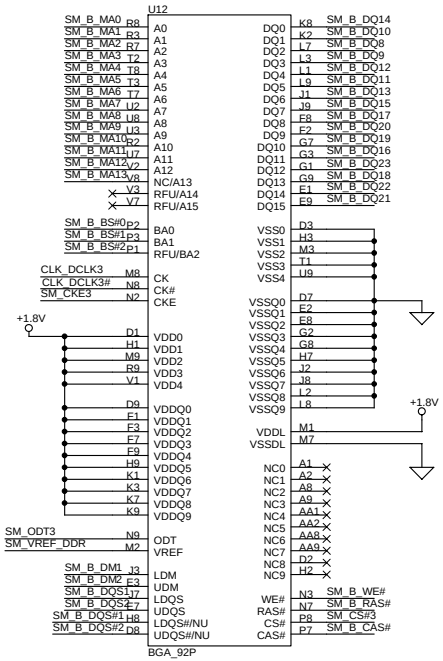


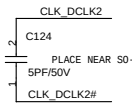
Layout Note: Place these Caps near Memory Module

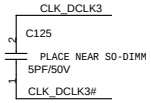


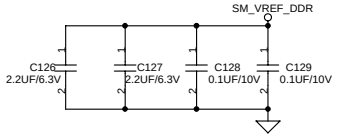




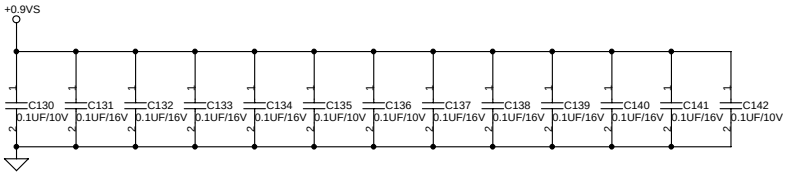




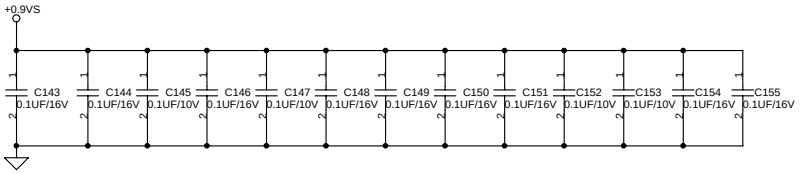


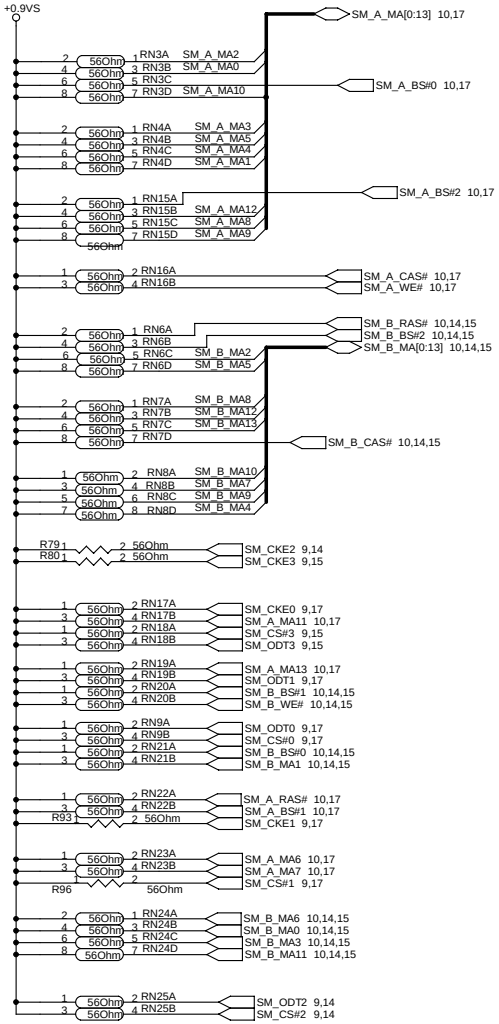


PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** ON BOARD DDR2(2)	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** George Chen
		SHEET 15 **OF** 60		**LIBRARY DATE :**	

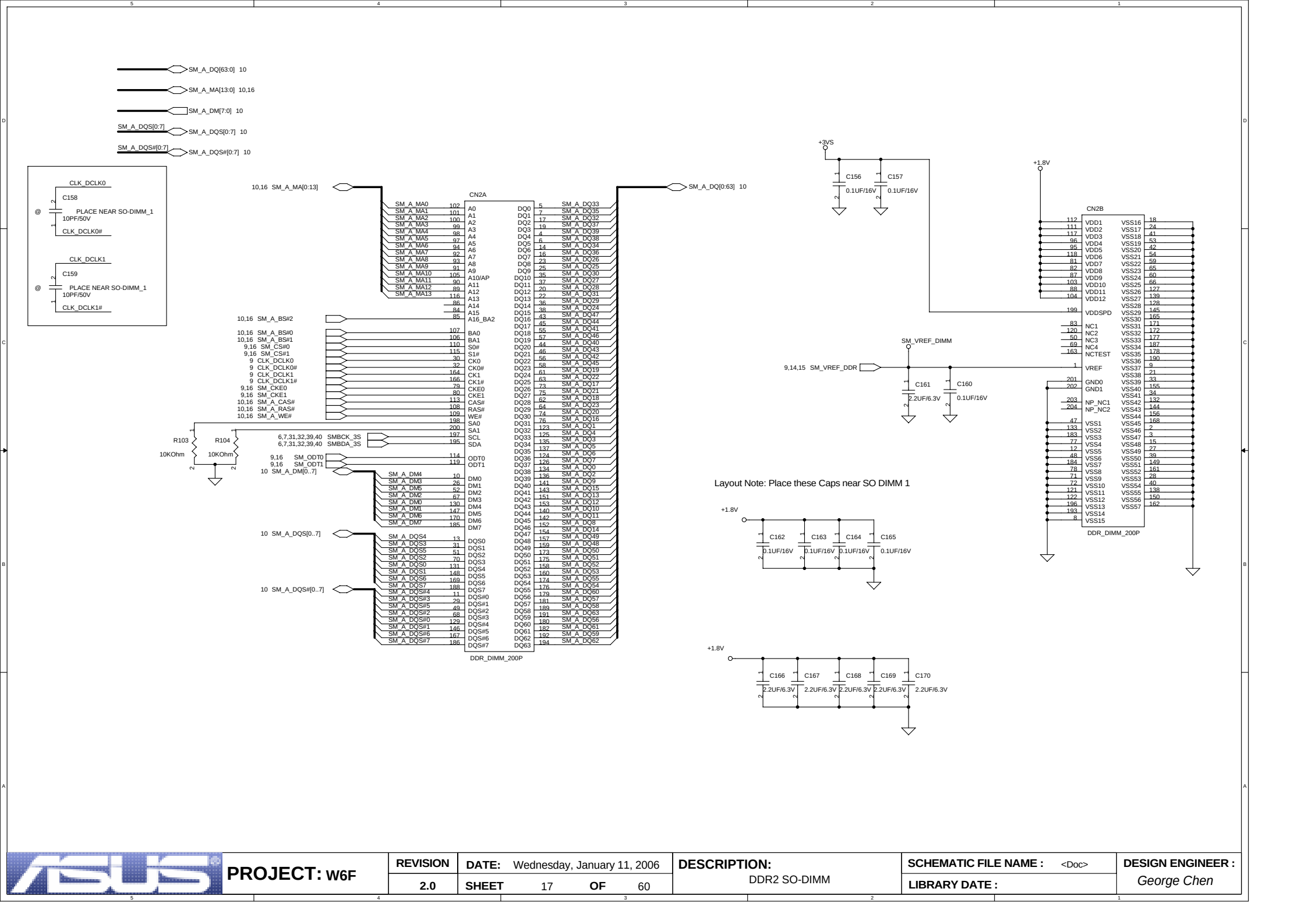


Layout Note: Place one cap close to every 2 pullup resitors terminated to +0.9VS

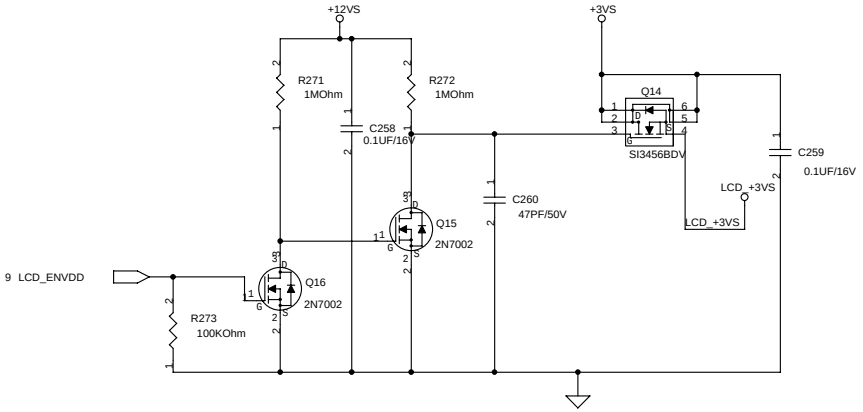


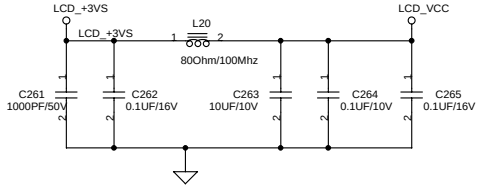


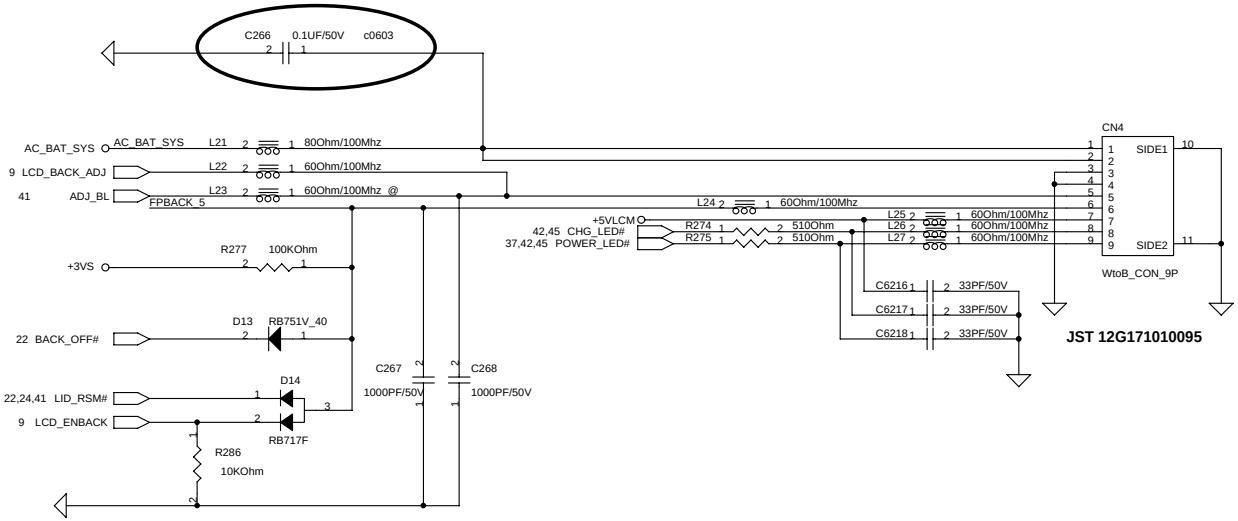
PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** ON BOARD DDR2 TERMINATION	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** *George Chen*
		SHEET 16 **OF** 60		**LIBRARY DATE :**	

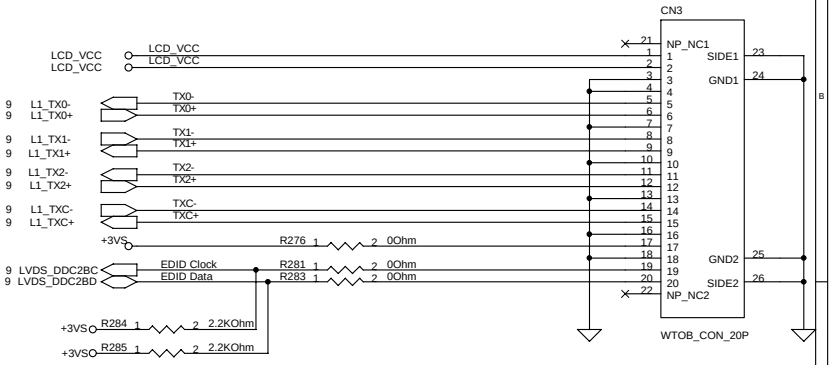


PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: DDR2 SO-DIMM	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 17 OF 60		LIBRARY DATE :	



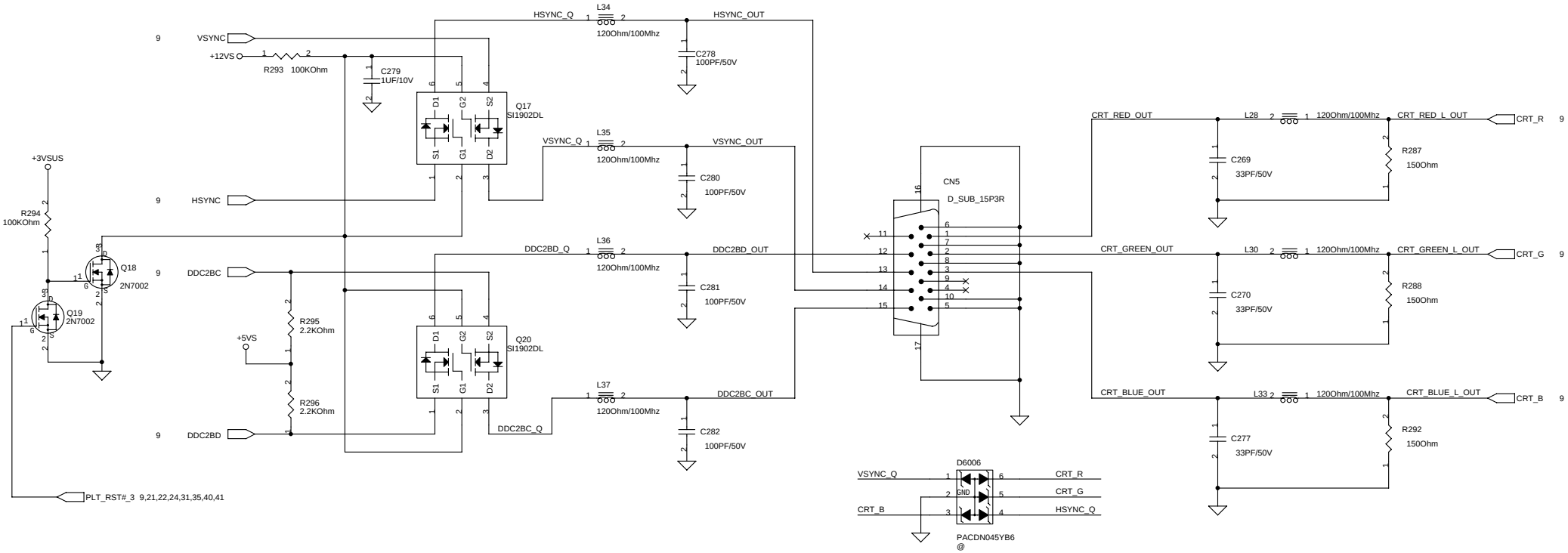




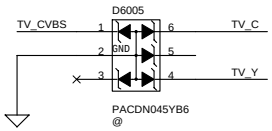


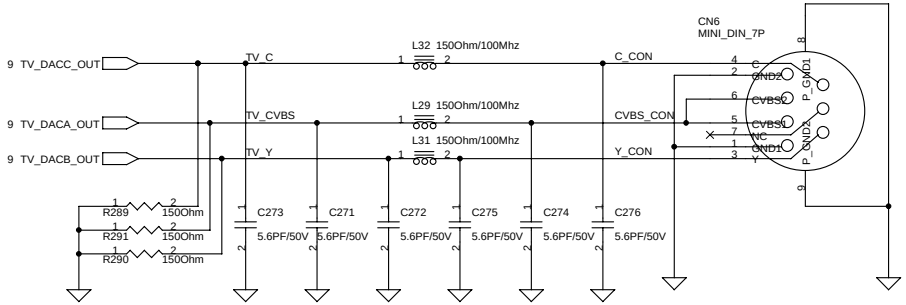
PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** LVDS & INVERTER	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** *George Chen*
		SHEET 18 **OF** 60		**LIBRARY DATE :**	

CRT Connector



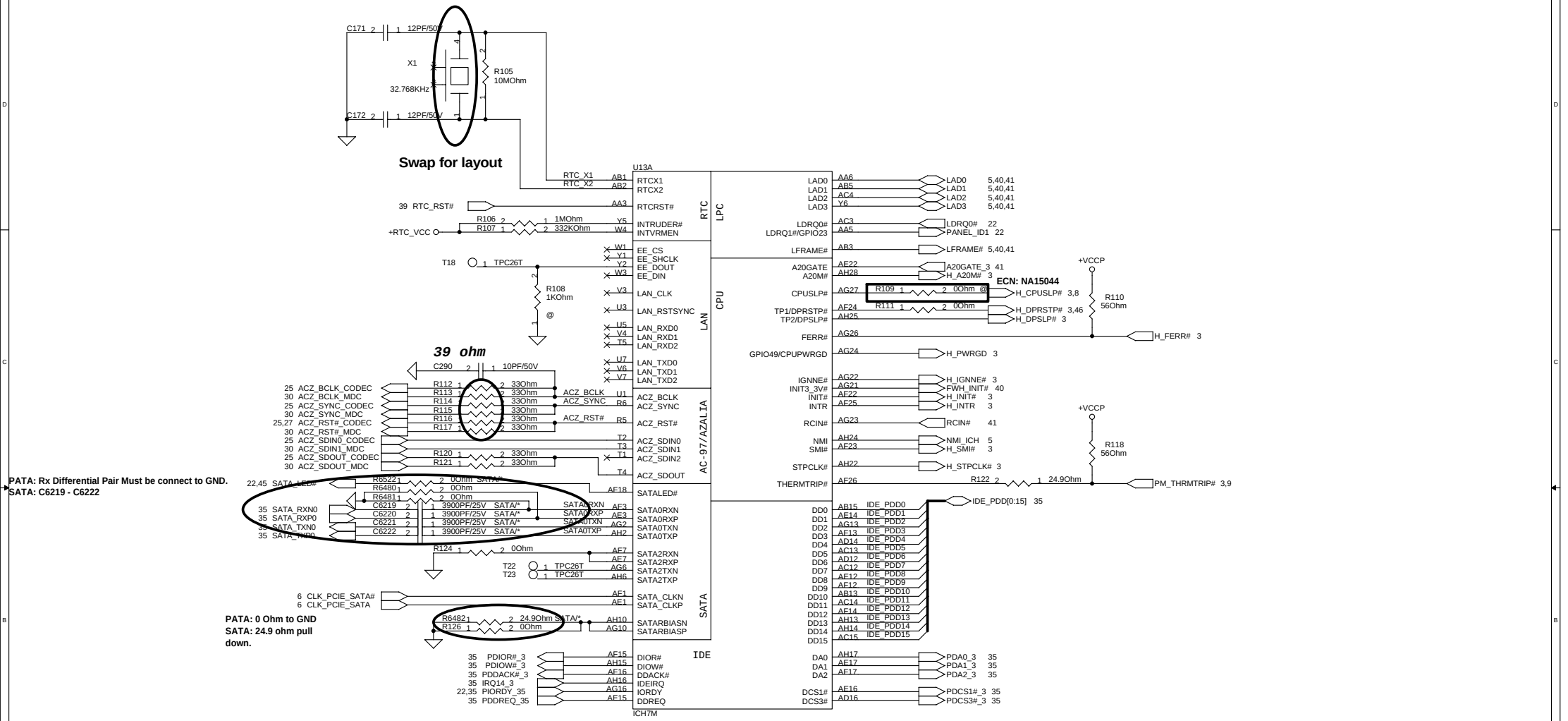
TV OUT



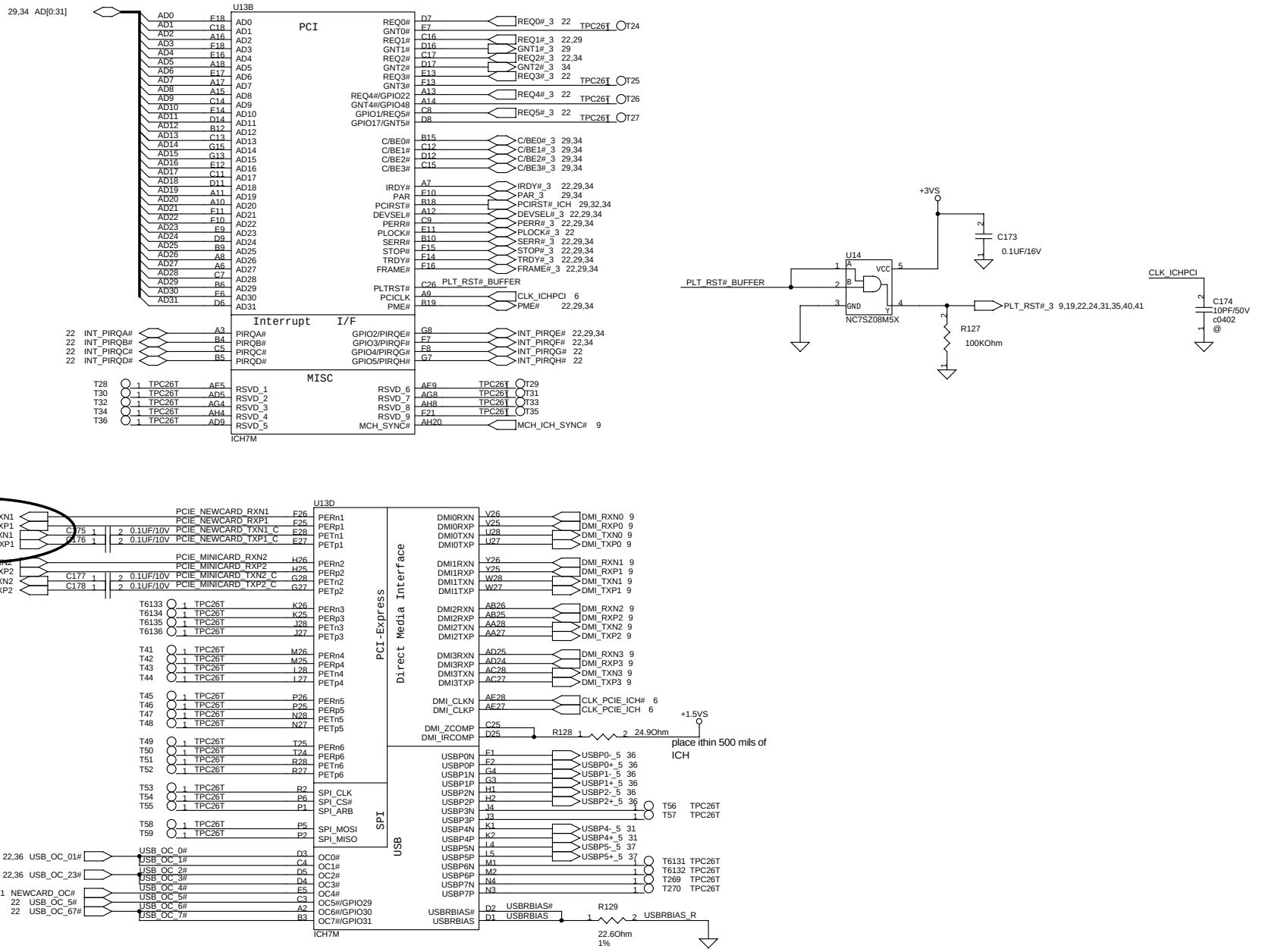


PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: CRT & TV OUT	SCHEMATIC FILE NAME : <Doc>
		SHEET 19 OF 60		LIBRARY DATE :

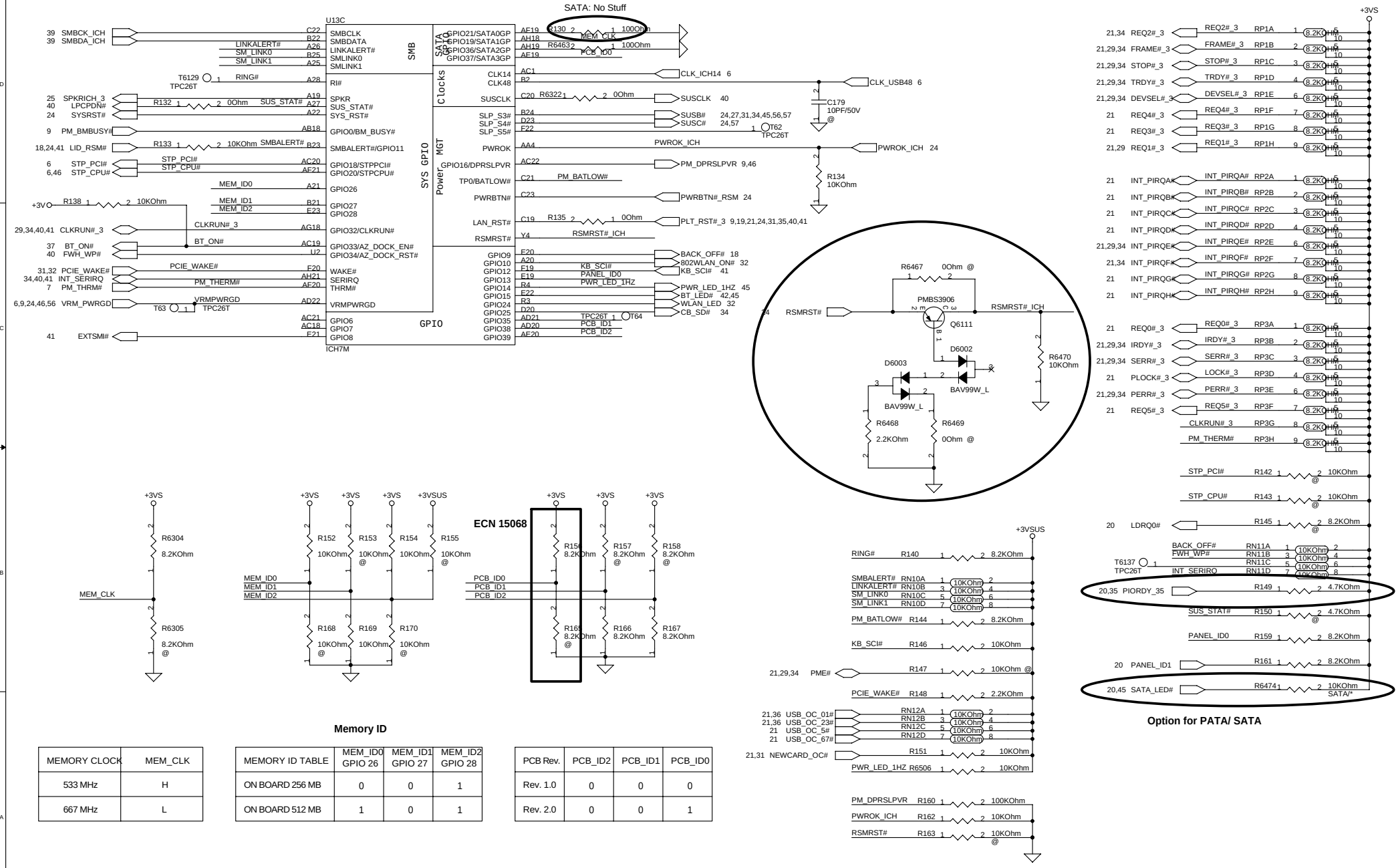
DESIGN ENGINEER : George Chen



PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** ICH7-M (1)	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** *George Chen*
		SHEET 20 **OF** 60		**LIBRARY DATE :**	



PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** ICH7-M (2)	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** *George Chen*
		SHEET 21 **OF** 60		**LIBRARY DATE :**	



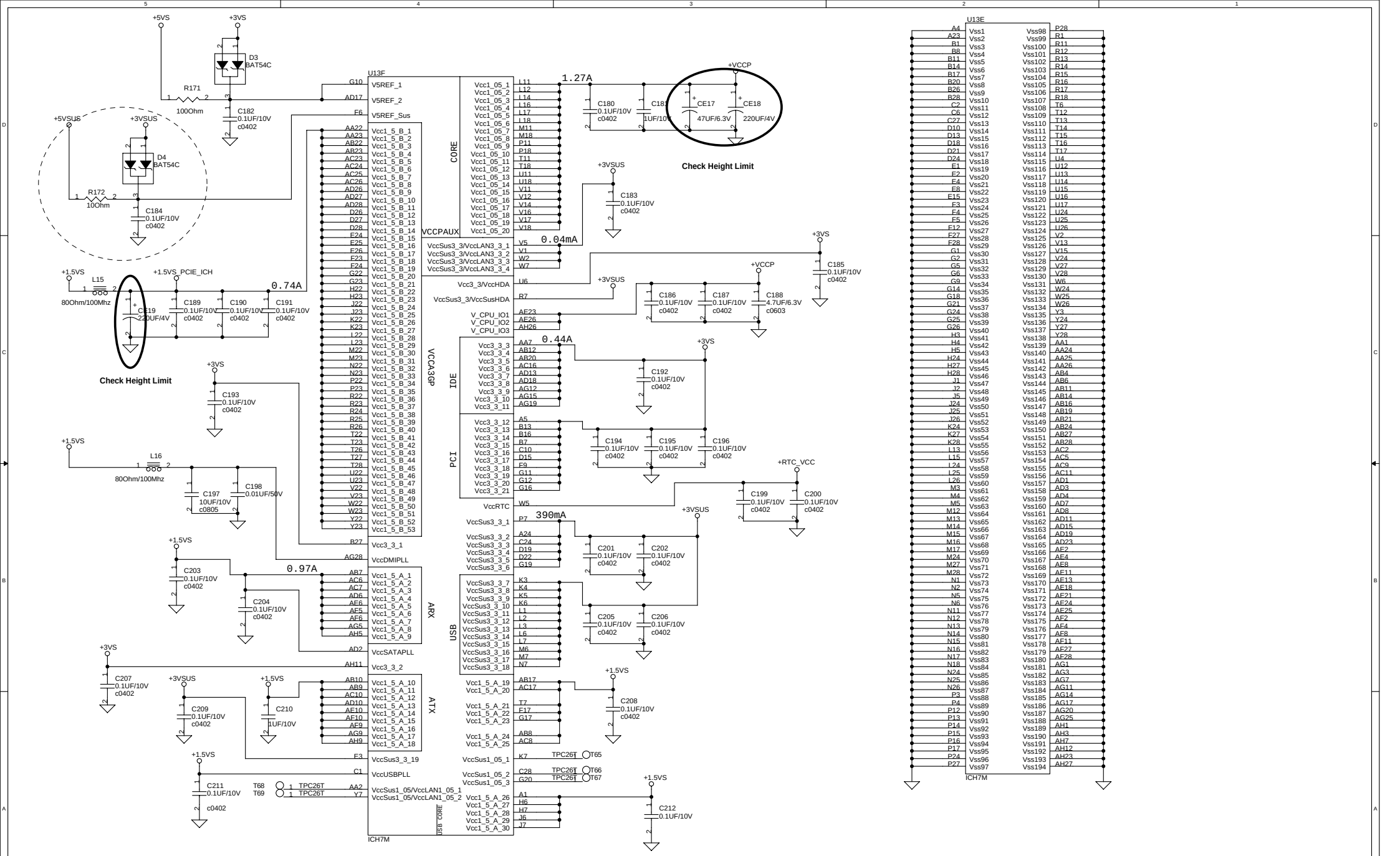
Memory ID

MEMORY CLOCK	MEM_CLK
533 MHz	H
667 MHz	L

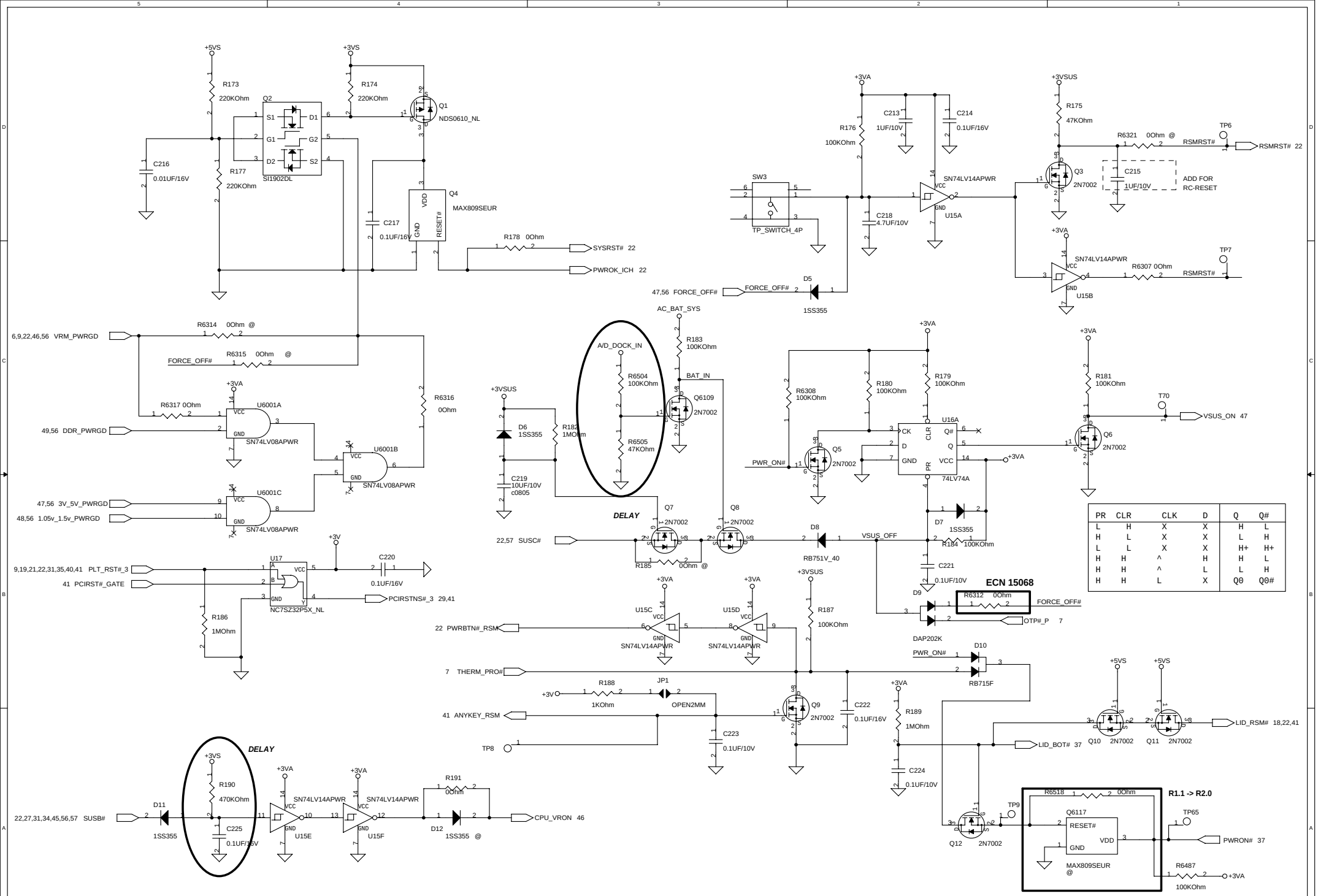
MEMORY ID TABLE	MEM_ID0 GPIO 26	MEM_ID1 GPIO 27	MEM_ID2 GPIO 28
ON BOARD 256 MB	0	0	1
ON BOARD 512 MB	1	0	1

PCB Rev.	PCB_ID2	PCB_ID1	PCB_ID0
Rev. 1.0	0	0	0
Rev. 2.0	0	0	1

PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006 **SHEET** 22 **OF** 60	**DESCRIPTION:** ICH7-M (3)
	SCHEMATIC FILE NAME : <Doc> **LIBRARY DATE :**		**DESIGN ENGINEER :** *George Chen*



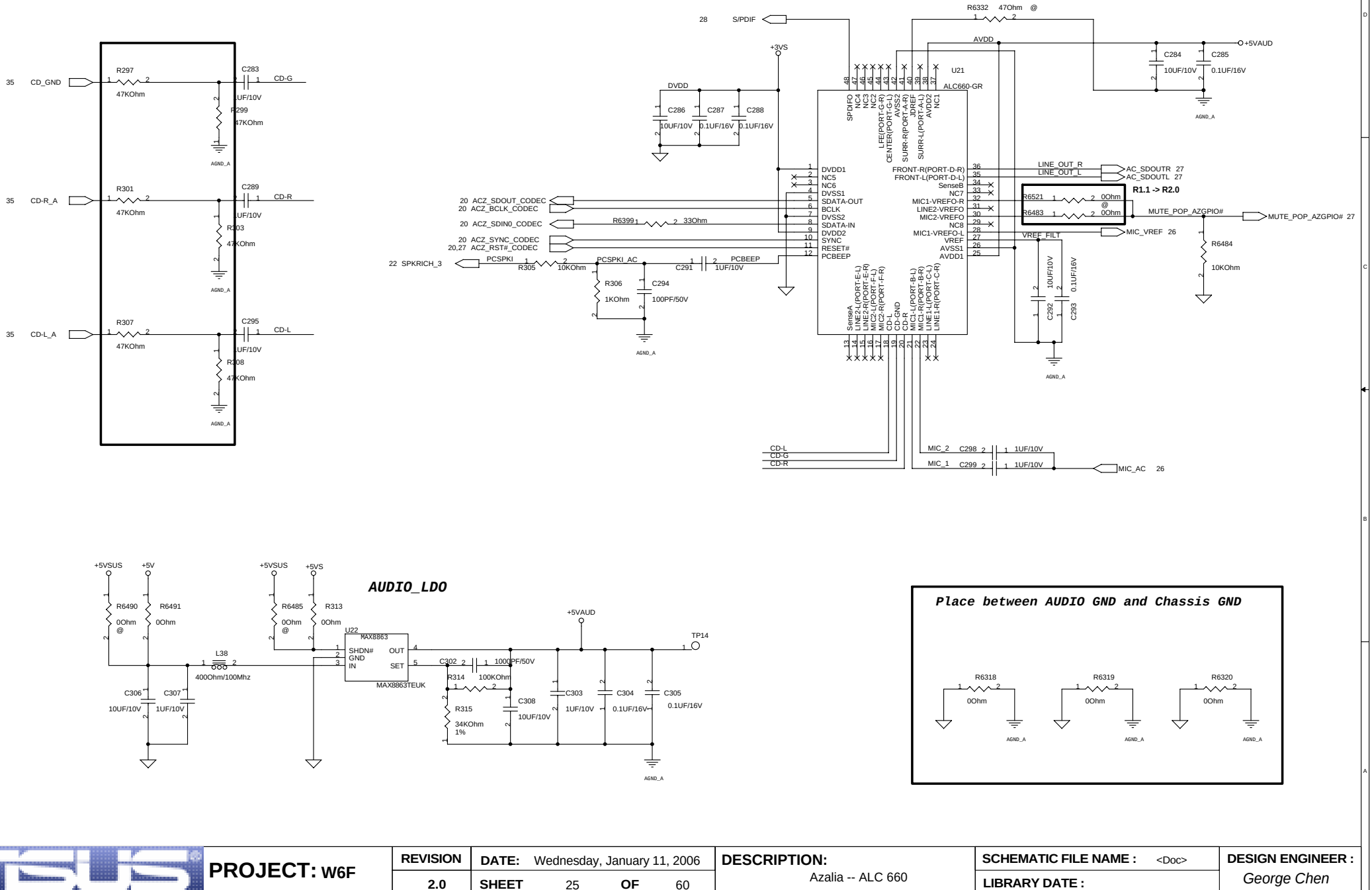
PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**SHEET** 23	**OF** 60	**DESCRIPTION:** ICH7-M POWER/ GND (4)	**SCHEMATIC FILE NAME :** <Doc> **LIBRARY DATE :**	**DESIGN ENGINEER :** *George Chen*



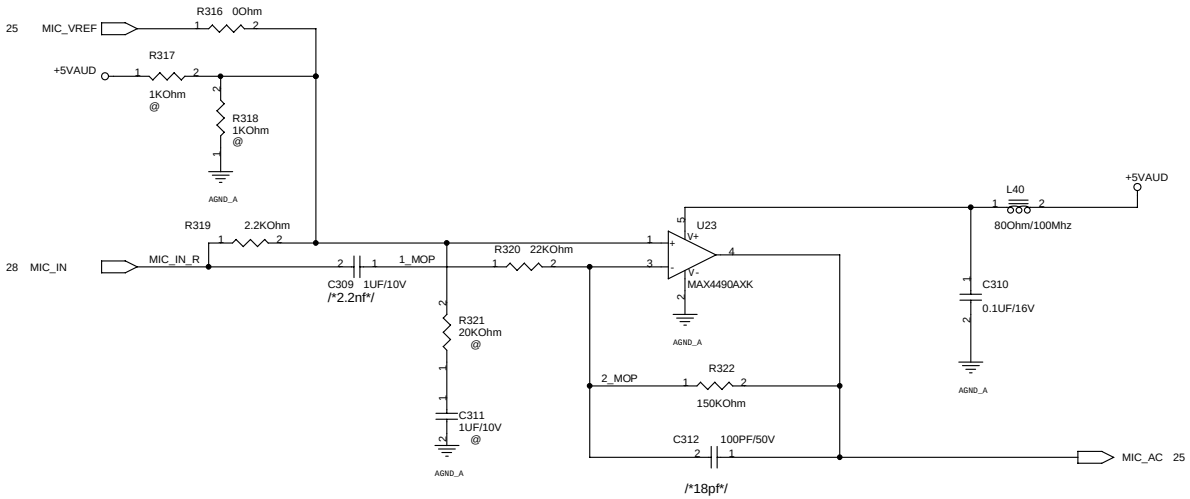
PR	CLR	CLK	D	Q	Q#
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H+	H+
H	H	^	H	H	L
H	H	^	L	L	H
H	H	L	X	Q0	Q0#

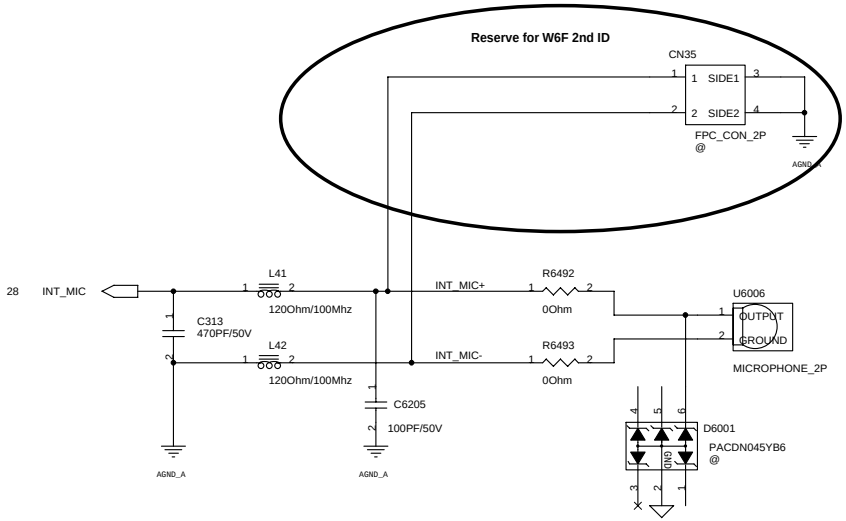
ASUS	**PROJECT:** W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** NEW RESET CIRCUIT	**SCHEMATIC FILE NAME :** <Doc>
			SHEET 24 **OF** 60		**LIBRARY DATE :**

DESIGN ENGINEER : *George Chen*



PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: Azalia -- ALC 660	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 25 OF 60		LIBRARY DATE :	

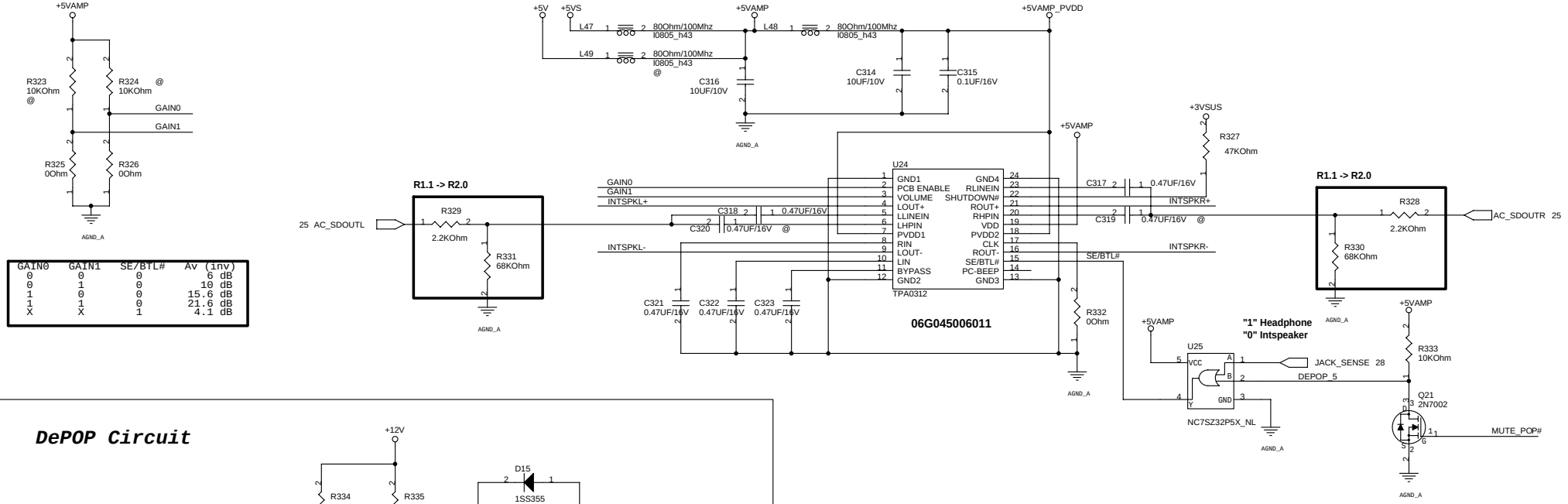




George Chen

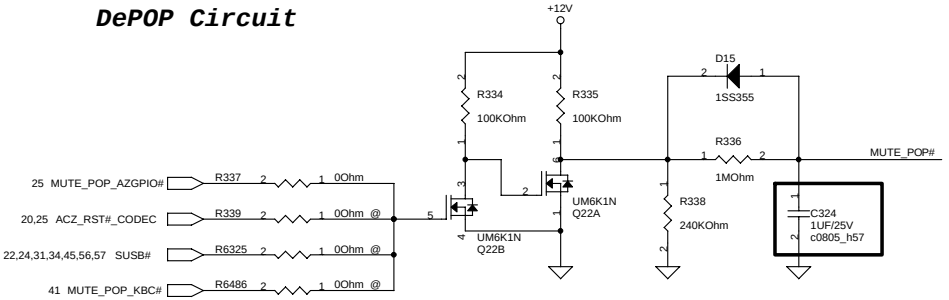
PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** MIC PRE AMP & INT MIC	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :**
		SHEET 26 **OF** 60		**LIBRARY DATE :**	

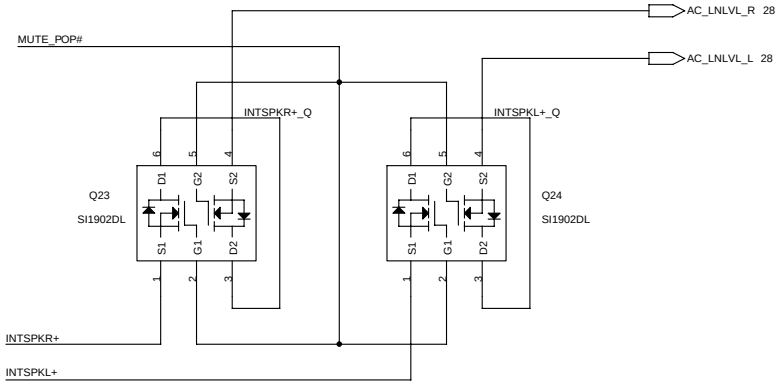
AUDIO AMP



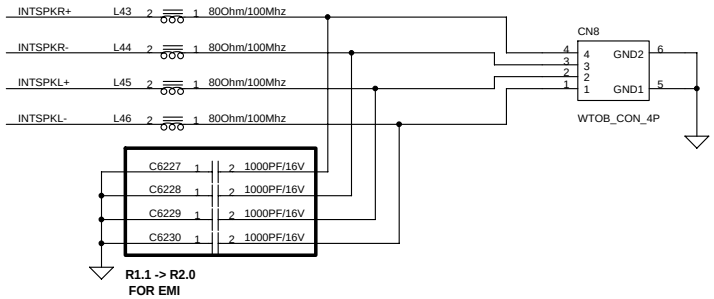
GAIN0	GAIN1	SE/BTL#	Av (inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

DePOP Circuit



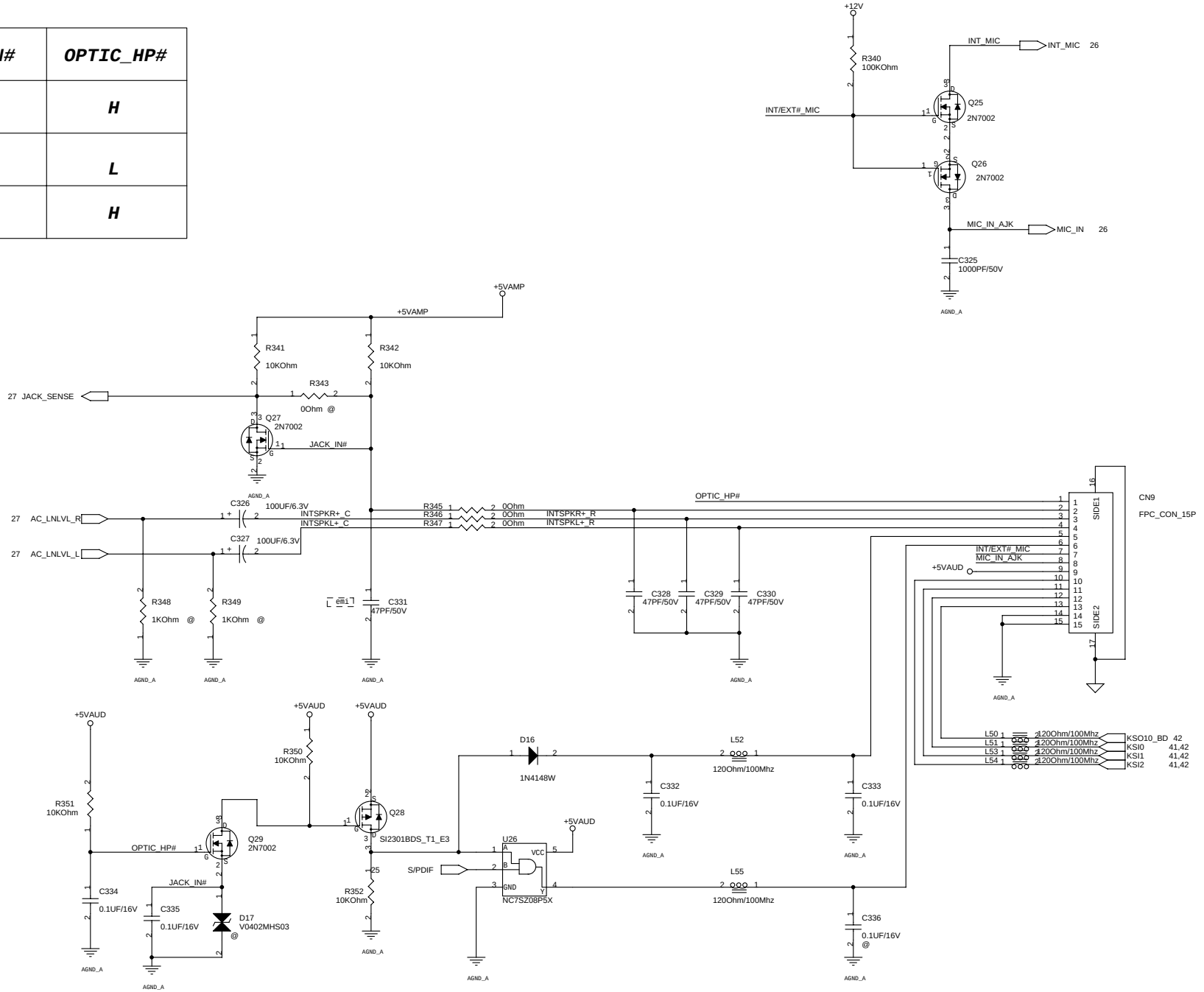


INTERNAL SPEAKER

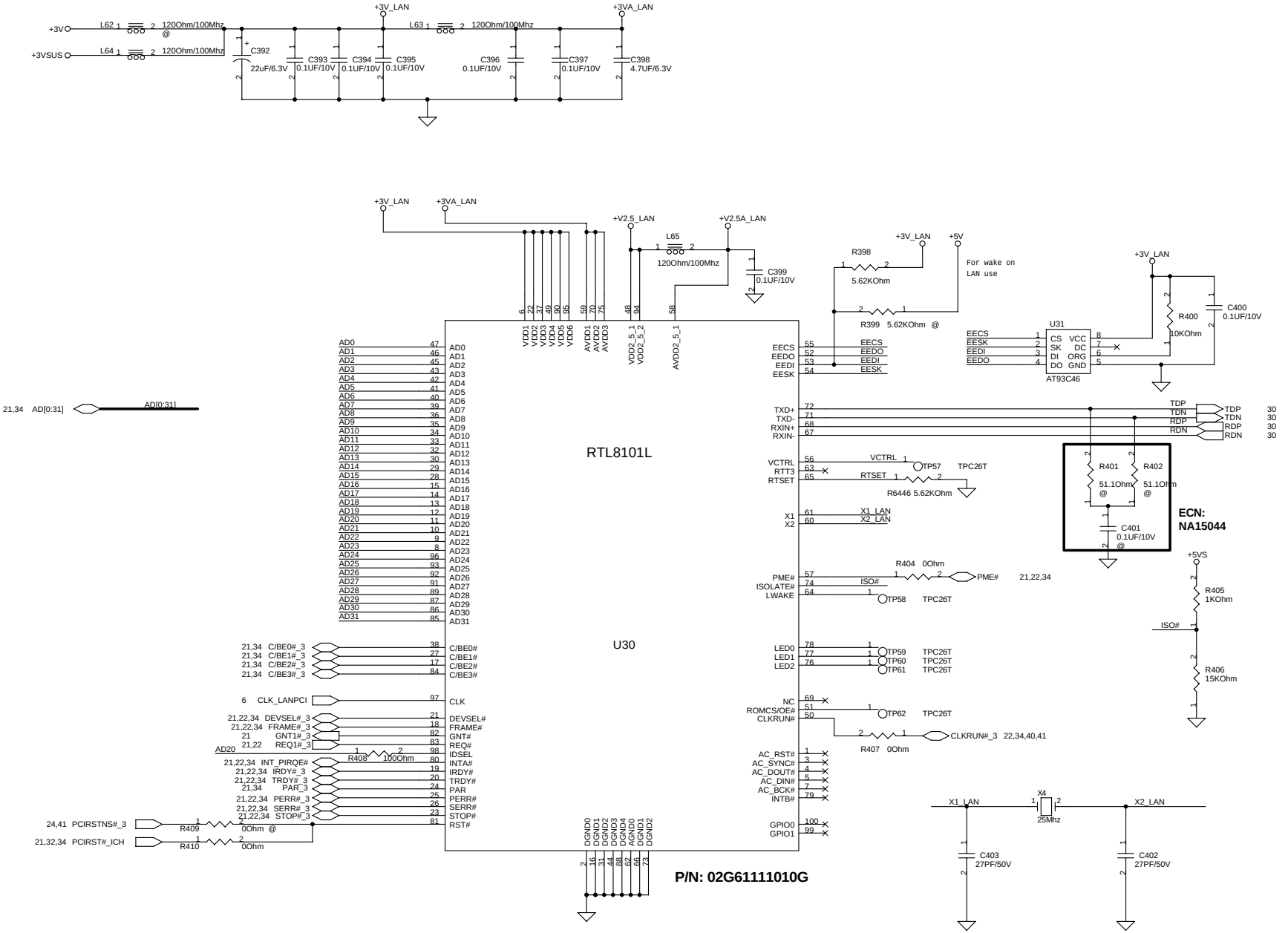


PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: AUDIO AMP & INT SPK	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 27 OF 60		LIBRARY DATE :	

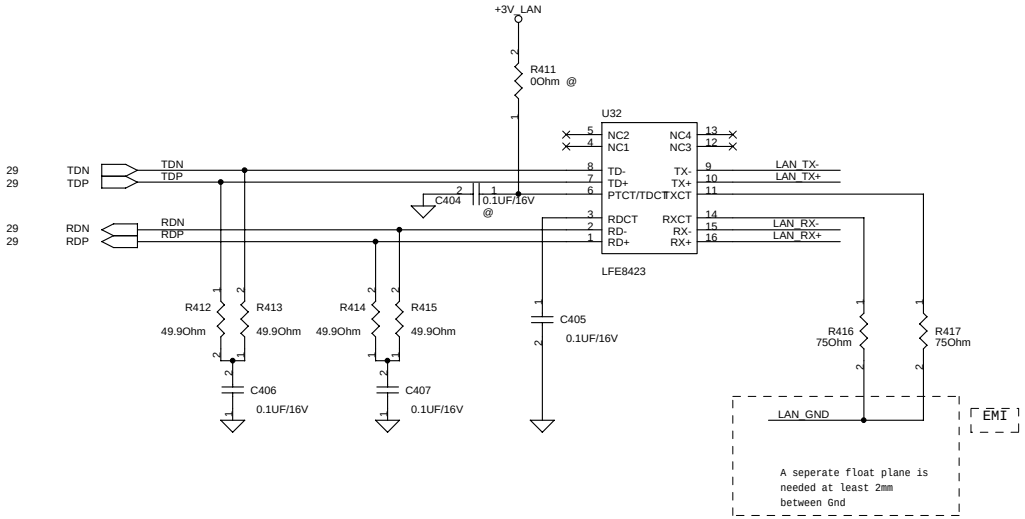
Net Name / Device	JACK_IN#	OPTIC_HP#
SPDIF	L	H
Line Out	L	L
NC	H	H

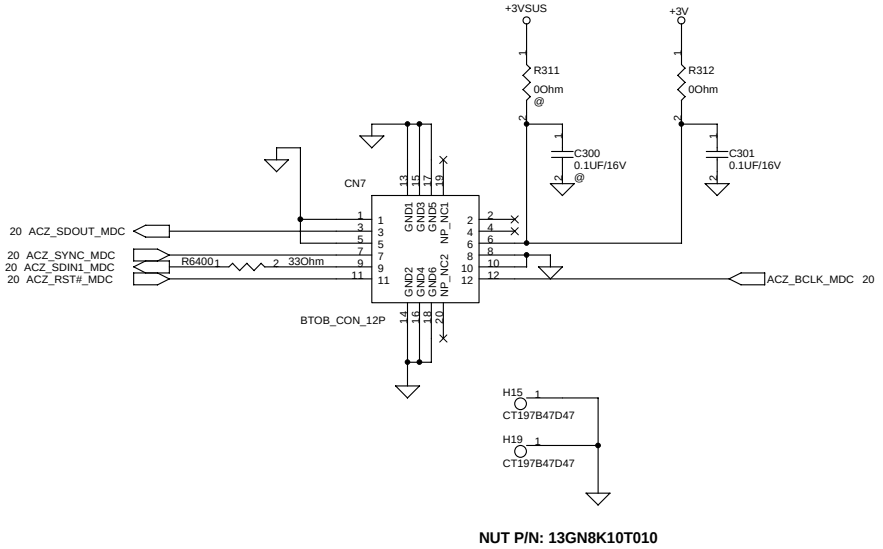


PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: SPDIF & AUDIO BOARD CON	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 28 OF 60		LIBRARY DATE :	

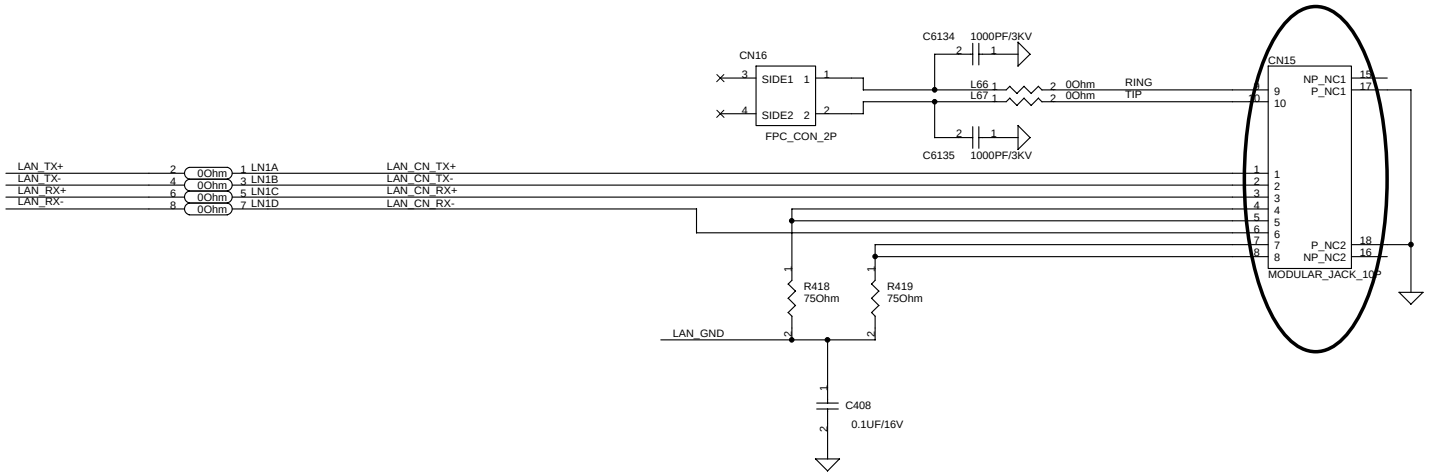


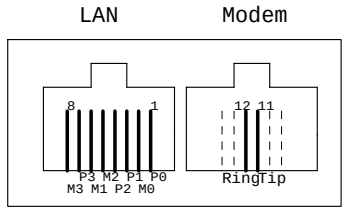
PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: LAN RTL8101L	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 29 OF 60		LIBRARY DATE :	



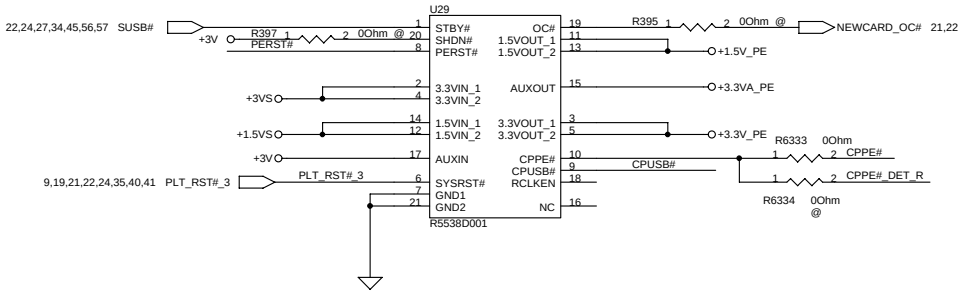


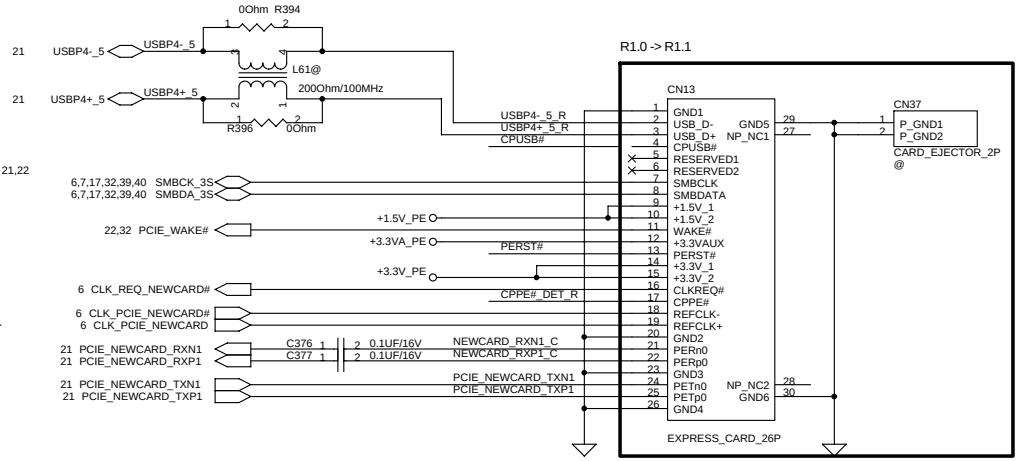
NUT P/N: 13GN8K10T010

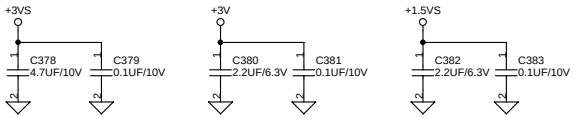


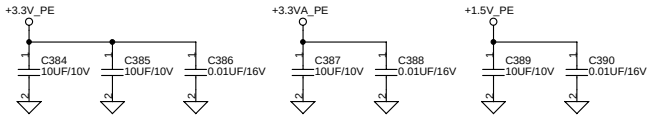


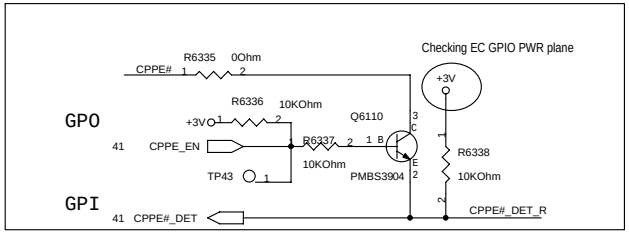
PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: LAN I/O & MDC	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 30 OF 60		LIBRARY DATE :	





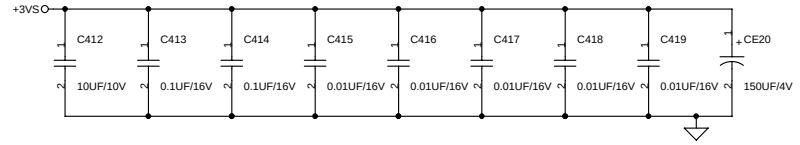


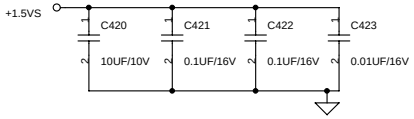




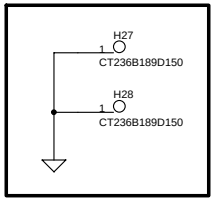
For soft ware disable issue

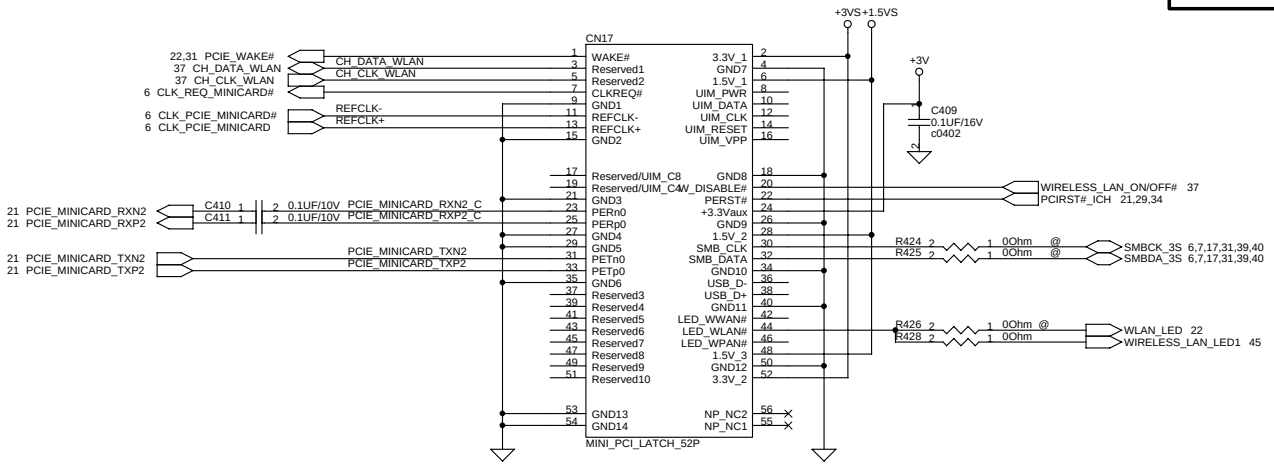
PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** EXPRESS CARD	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** *George Chen*
		SHEET 31 **OF** 60		**LIBRARY DATE :**	

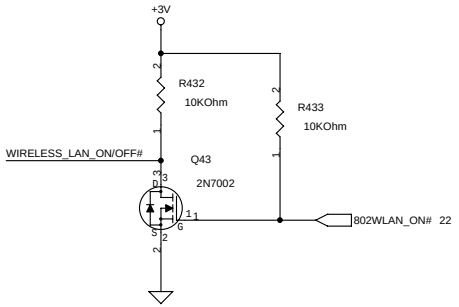




R1.1 -> R2.0 For Golan Nut

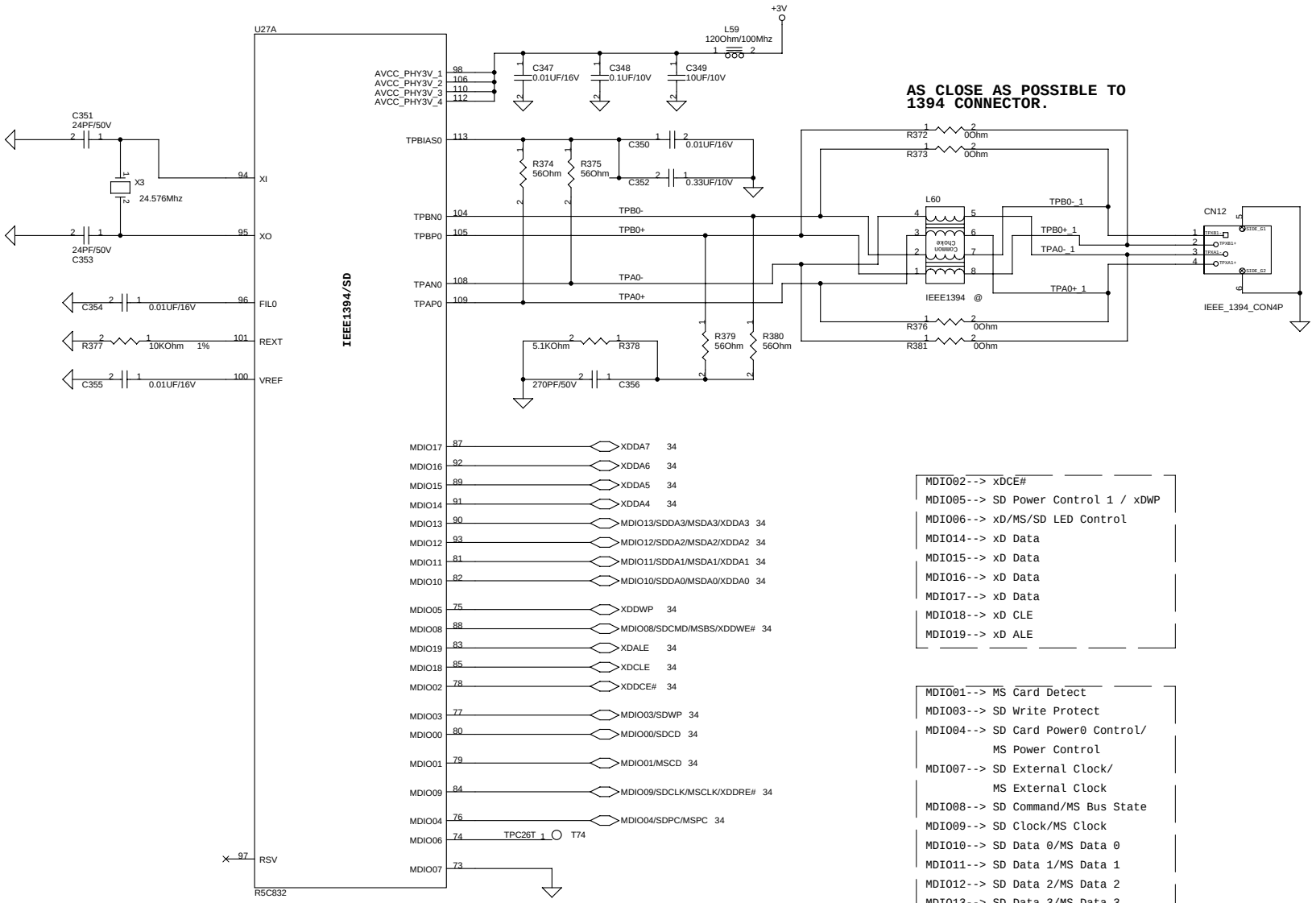






PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** MINI CARD	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :**
		SHEET 32 **OF** 60		**LIBRARY DATE :**	

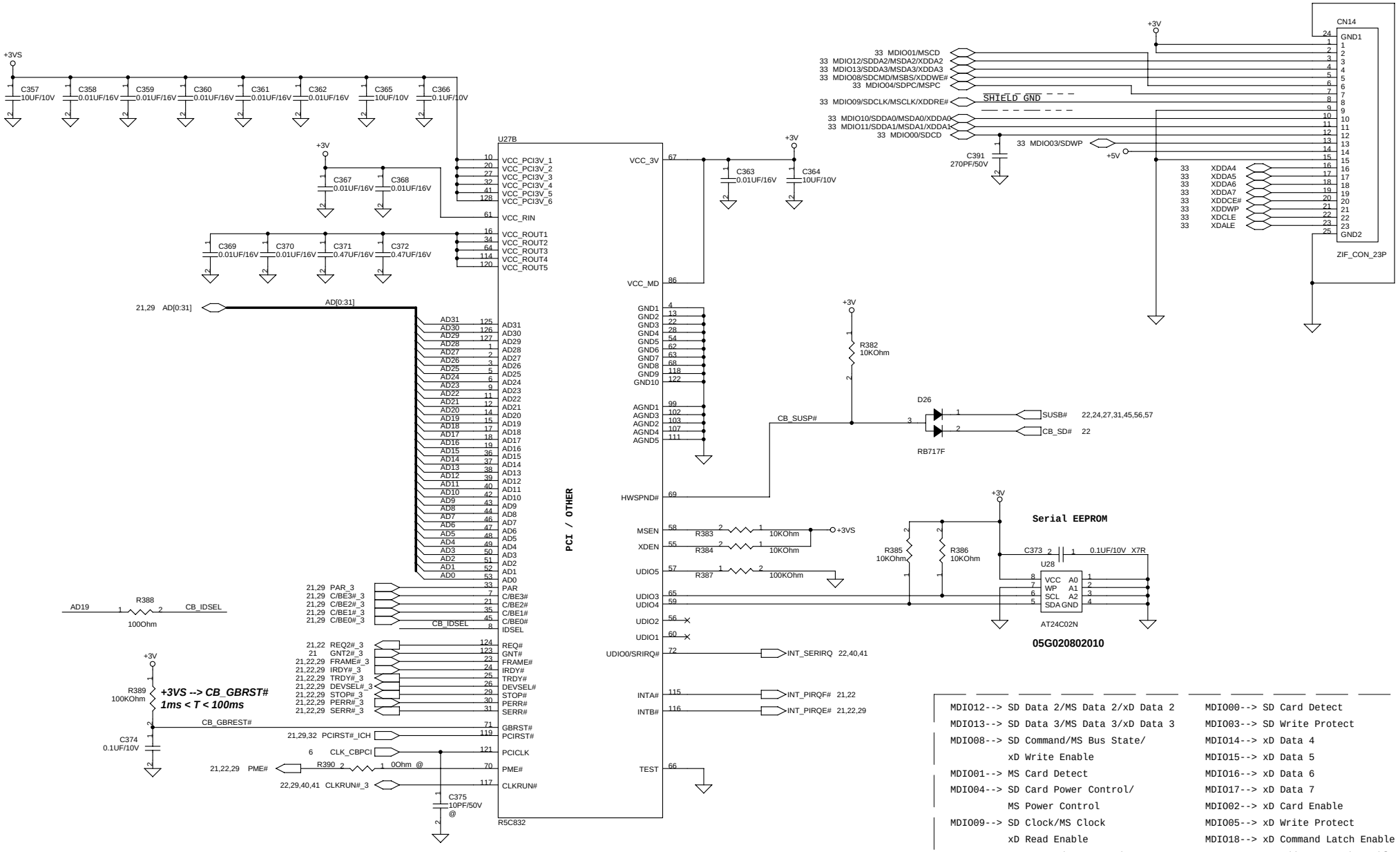
George Chen



PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006 SHEET 33 OF 60	DESCRIPTION: RICOH R5C832 - 1394 (1)	SCHEMATIC FILE NAME : <Doc> LIBRARY DATE :	DESIGN ENGINEER : George Chen

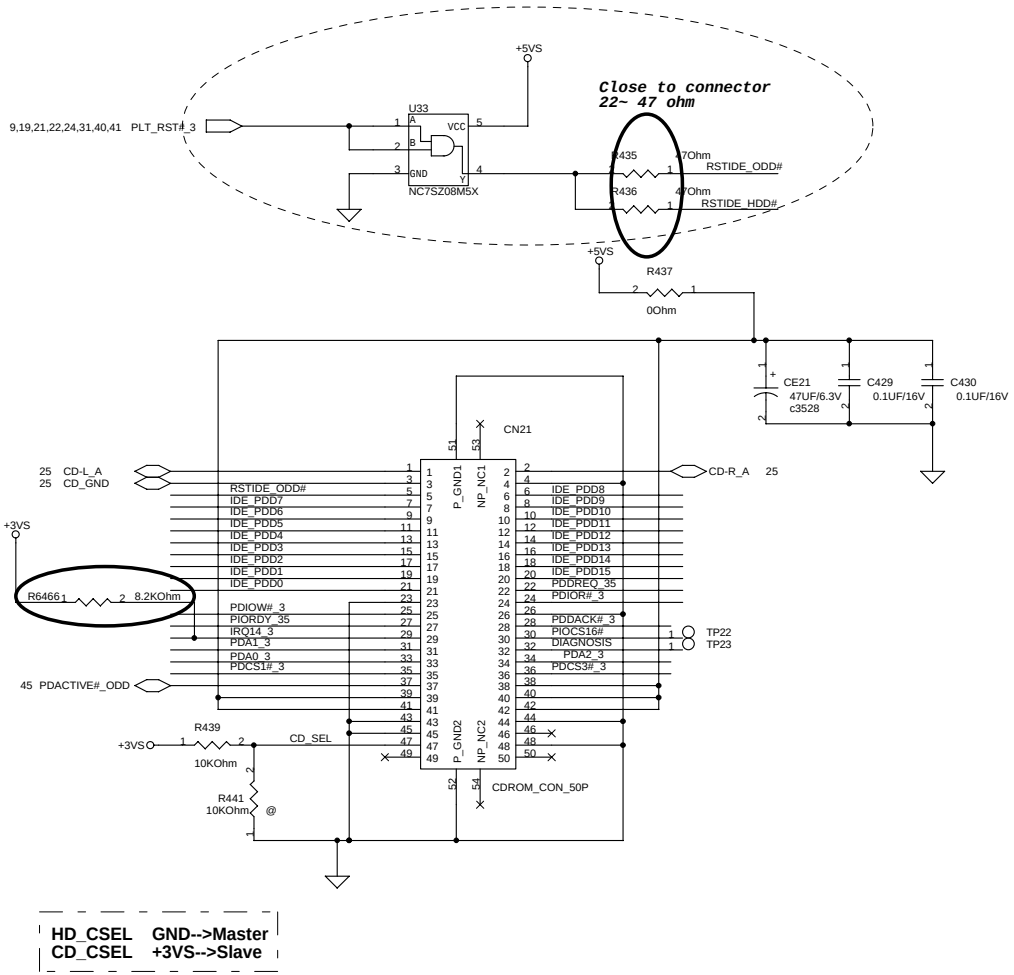
SD/MMC/MS/MS-PRO Card Reader Socket

[3] CLK LINE : SHIELDED BY GND. (RECOMMENDED) [5] R5C841 OPTIONS.



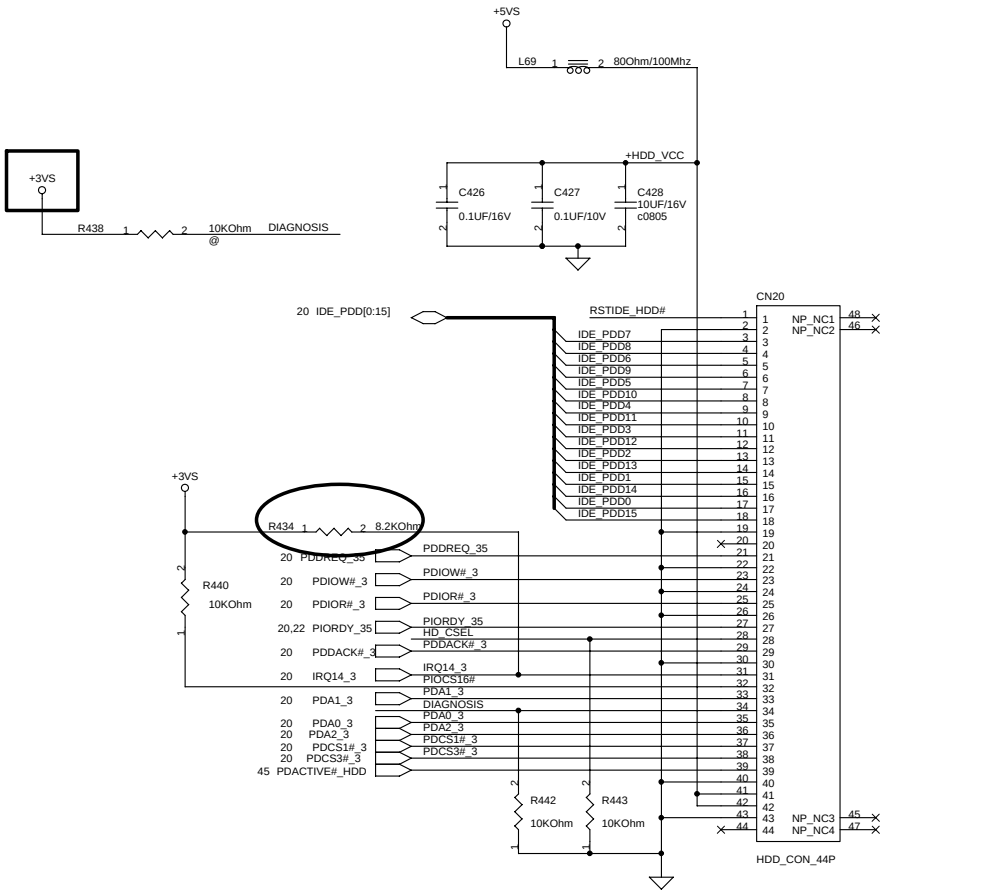
PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** RICOH R5C832 - PCI, 4IN1 CARD	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** George Chen
		SHEET 34 **OF** 60		**LIBRARY DATE :**	

CDROM Connector

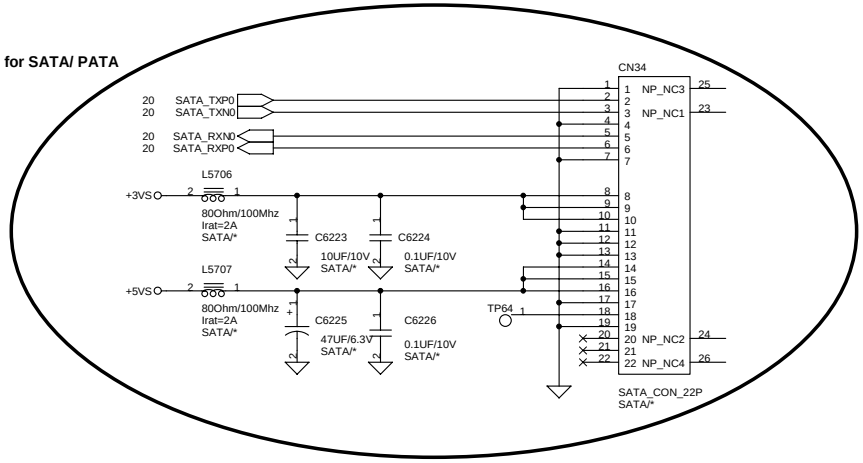


HD_CSEL GND-->Master
CD_CSEL +3VS-->Slave

HDD Connector

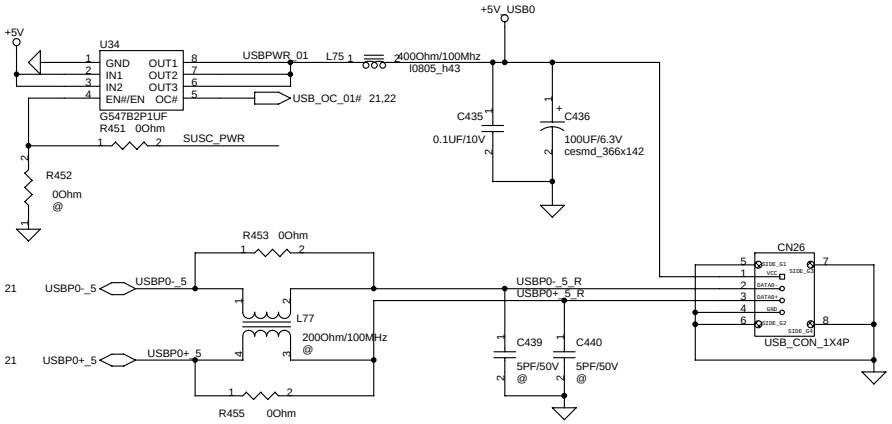


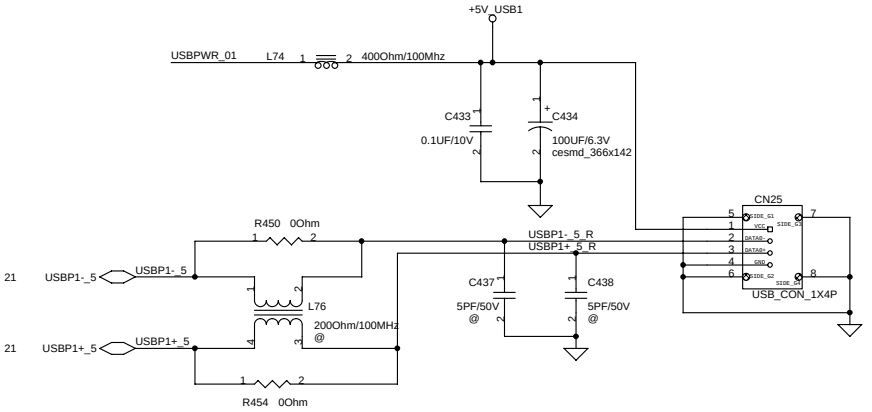
Option for SATA/ PATA

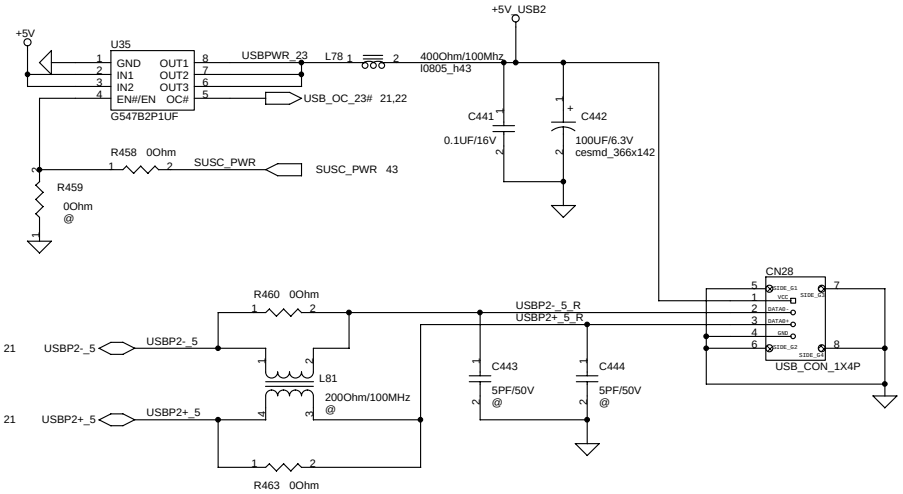


ASUS	**PROJECT:** W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006 **SHEET** 35 **OF** 60	**DESCRIPTION:** HDD & CDROM CONN	**SCHEMATIC FILE NAME :** <Doc> **LIBRARY DATE :**

DESIGN ENGINEER : *George Chen*

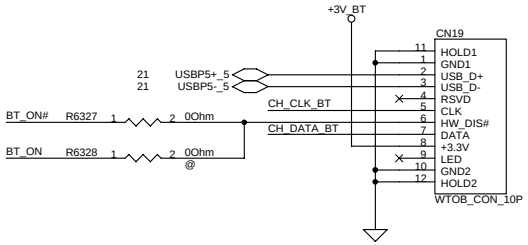


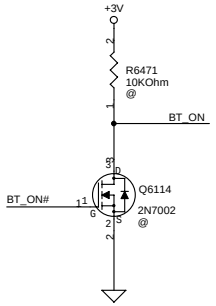


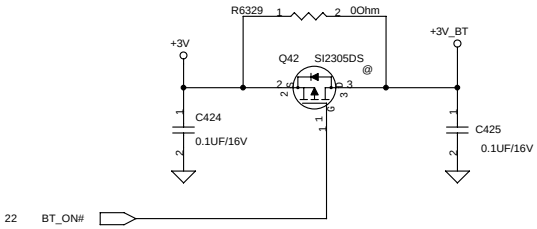


PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** USB2.0 CN * 3	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** *George Chen*
		SHEET 36 **OF** 60		**LIBRARY DATE :**	

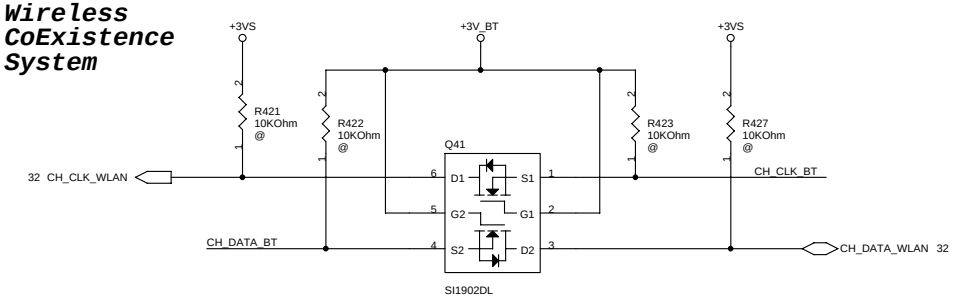
Bluetooth



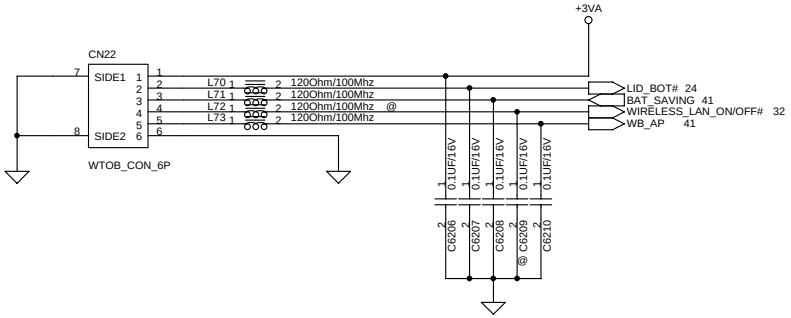




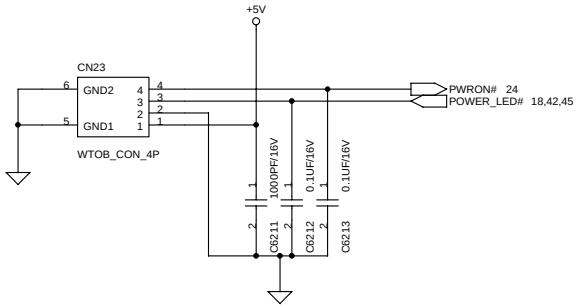
For Intel Wireless CoExistence System



LID Switch



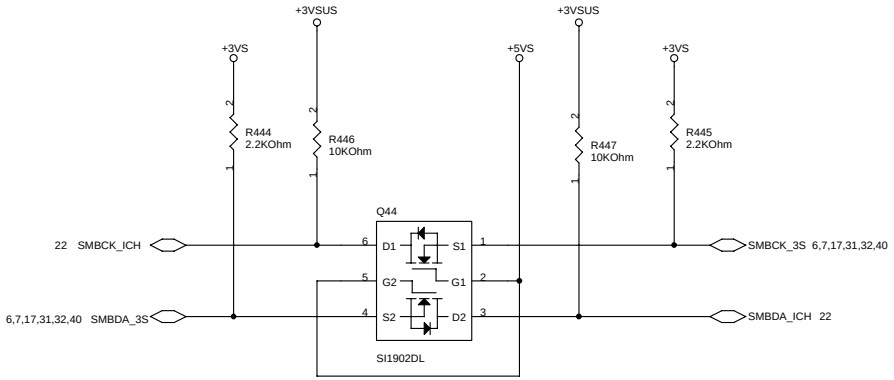
Power Switch



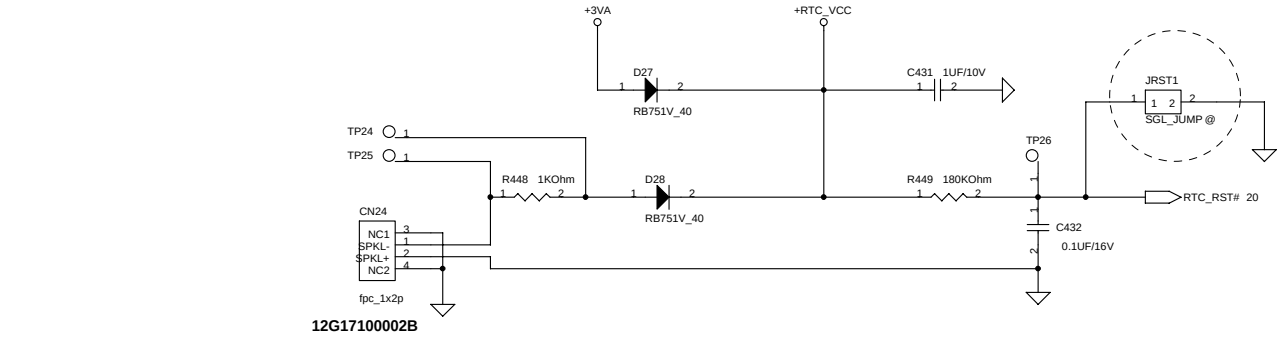
PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: BT & EXT. BOARD	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 37 OF 60		LIBRARY DATE :	

PROJECT: W6F	REVISION	DATE: Wednesday, January 11, 2006	DESCRIPTION:	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
	2.0	SHEET 38 OF 60	N/A	LIBRARY DATE :	

SM BUS

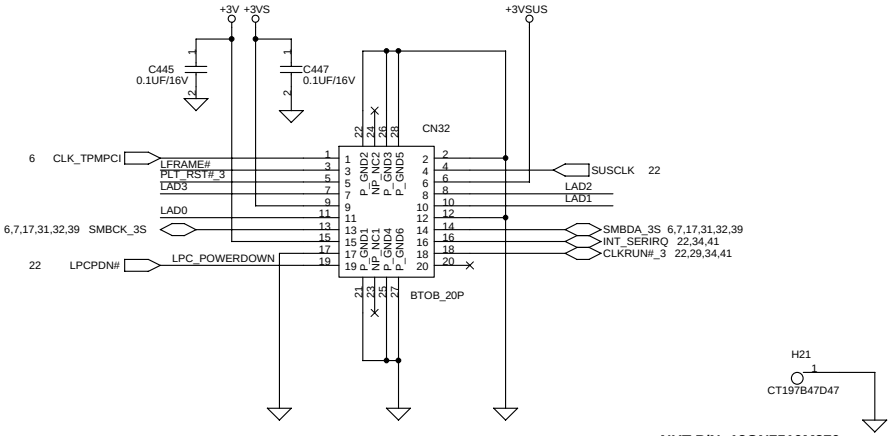


RTC Connector



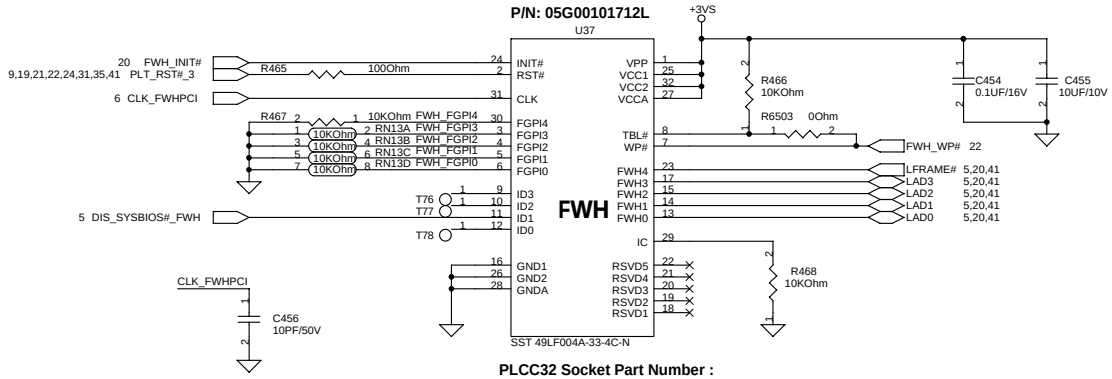
PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: SM BUS & RTC CN	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 39 OF 60		LIBRARY DATE :	

TPM 1.2 Infieon



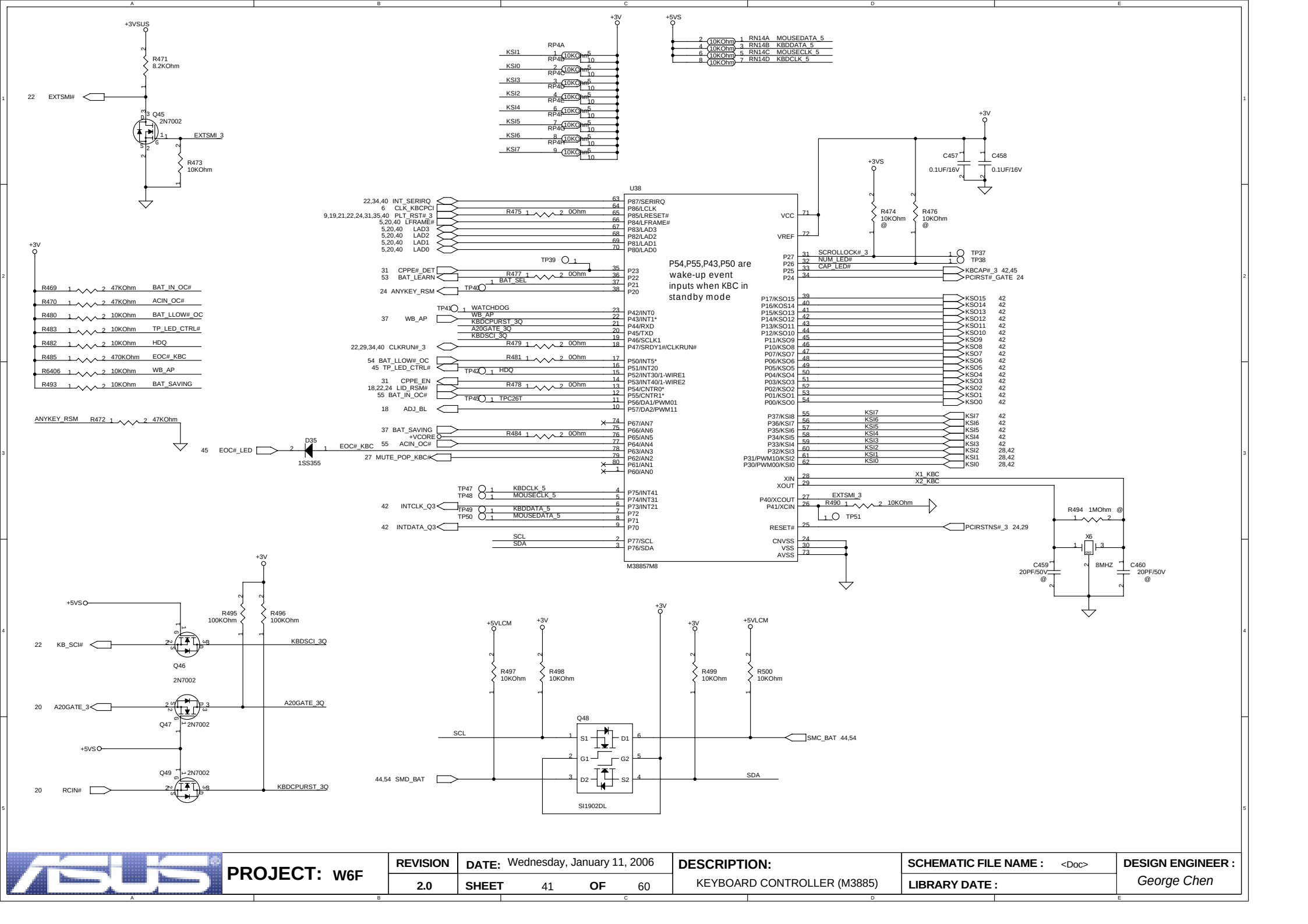
NUT P/N: 13GN7510M270

FWH



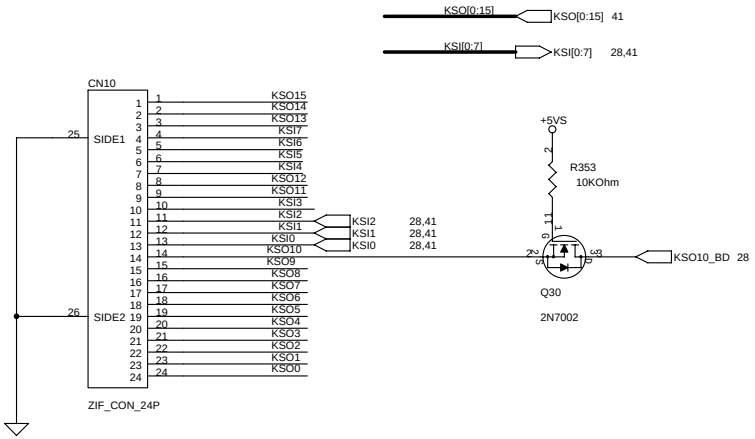
PLCC32 Socket Part Number :
12G04300032F

PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** FWH & TPM 1.2	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** George Chen
		SHEET 40 **OF** 60		**LIBRARY DATE :**	



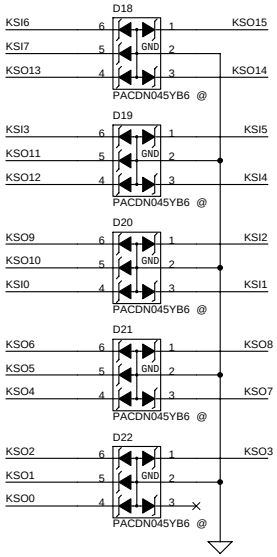
PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** KEYBOARD CONTROLLER (M3885)	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** George Chen
		SHEET 41 **OF** 60		**LIBRARY DATE :**	

Internal Keyboard

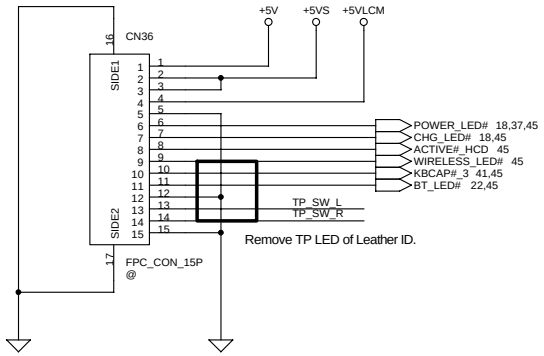


Each IC needs 2 vias to ground.

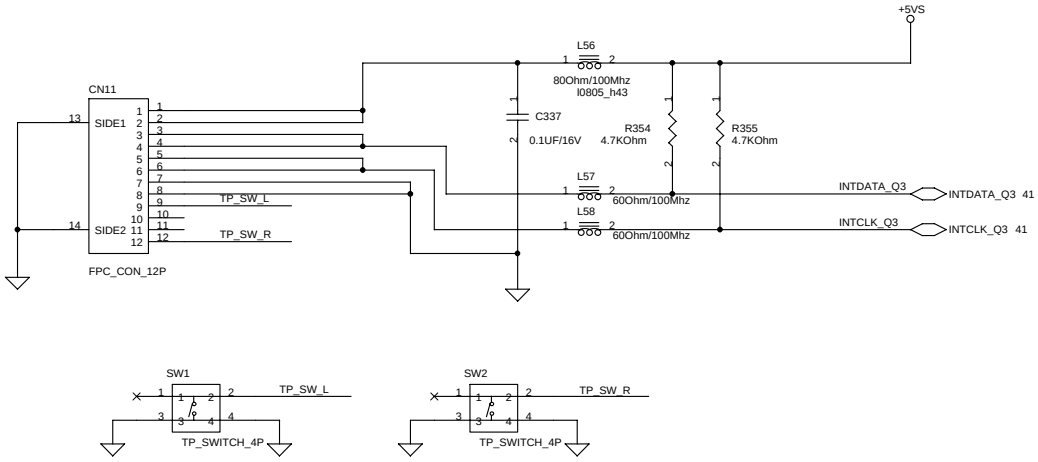
EMI recommandation. To protect KBC destroy by ESD. Need put between KB connector and KBC, and close to the connector as possible.



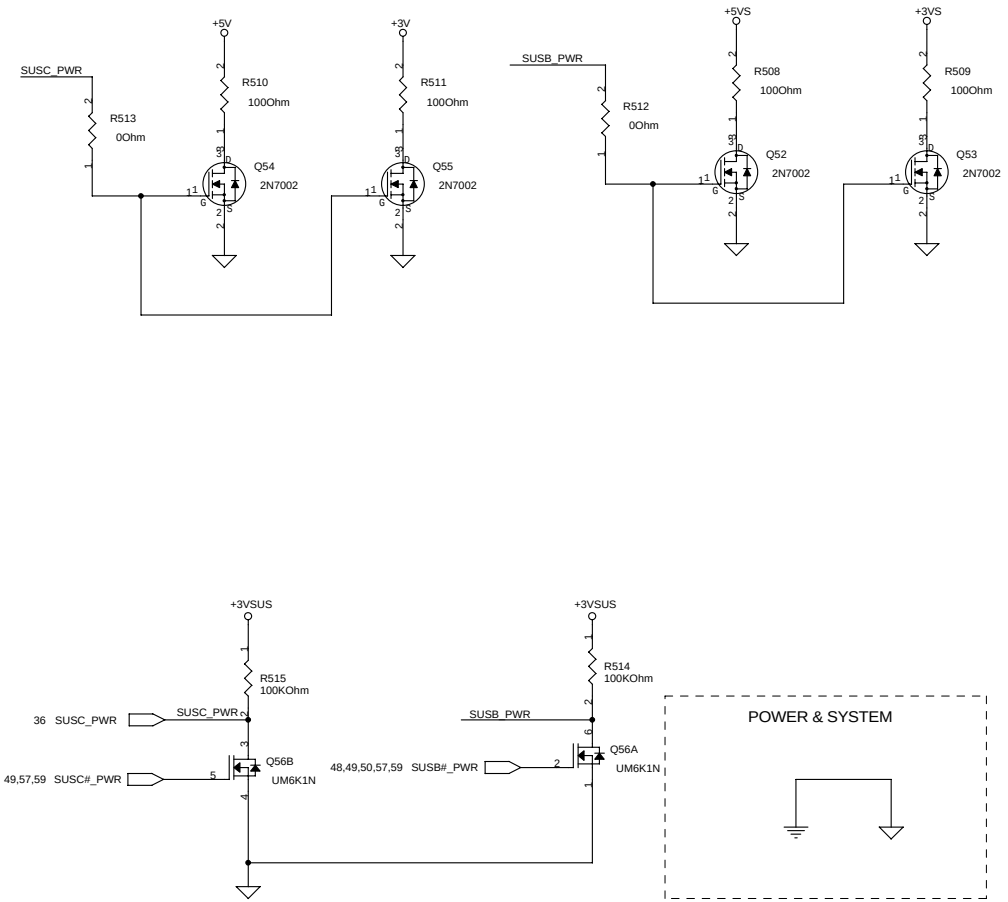
Reserve for W6F 2nd ID



Touch Pad



PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: INTERNAL KB & TP	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 42 OF 60		LIBRARY DATE :	

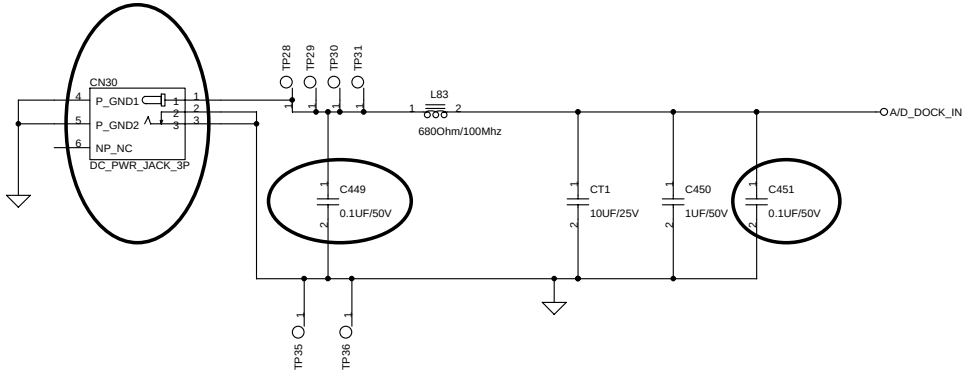


POWER RAIL

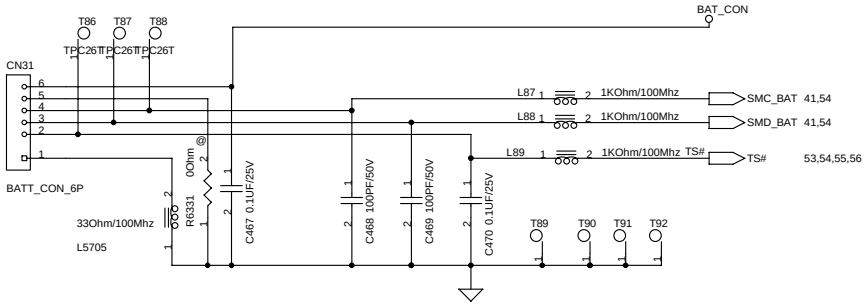
+VCORE	+VCORE	4,7,41,46
+VCCP	+VCCP	3,4,6,8,11,12,20,23,48
+RTC_VCC	+RTC_VCC	20,23,39
+5VLCM	+5VLCM	18,41,42,45,53,54,55,56
+3VS_TVDAC	+3VS_TVDAC	11
+3VS_TVDACA	+3VS_TVDACA	11
+3VS_TVDACB	+3VS_TVDACB	11
+3VS_TVDACC	+3VS_TVDACC	11
+3VS_TVBG	+3VS_TVBG	11
+1.5VS_DPLLA	+1.5VS_DPLLA	11
+1.5VS_DPLLB	+1.5VS_DPLLB	11
+1.5VS_HPLL	+1.5VS_HPLL	11
+1.5VS_MPLL	+1.5VS_MPLL	11
+1.5VS_QTVDAC	+1.5VS_QTVDAC	11
+1.5VS_TVDAC	+1.5VS_TVDAC	11
+1.5VS_3GPLL	+1.5VS_3GPLL	11
+1.5VS_PCIE	+1.5VS_PCIE	11
SM_VREF_DDR	SM_VREF_DDR	9,14,15,17
+1.5VS_PCIE_ICH	+1.5VS_PCIE_ICH	23
LCD_+3VS	LCD_+3VS	18
LCD_VCC	LCD_VCC	18
+5VAMP	+5VAMP	27,28
+5VAMP_PVDD	+5VAMP_PVDD	27
+5VAUD	+5VAUD	25,26,28
+3V_BT	+3V_BT	37
SM_VREF_DIMM	SM_VREF_DIMM	9,14,15,17
+3VA	+3VA	24,37,39,50,59
+3VSUS	+3VSUS	19,22,23,24,27,29,30,39,40,41,47
+5VSUS	+5VSUS	7,23,25,47,56
BAT_S	BAT_S	53,56
BAT	BAT	53
+1.5VS	+1.5VS	4,9,11,12,21,23,31,32,48
+2.5VS	+2.5VS	11,50
+1.8V	+1.8V	9,12,14,15,17,49
BAT_CON	BAT_CON	44,53
A/D_DOCK_IN	A/D_DOCK_IN	24,44,53,55,56

PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006	**DESCRIPTION:** DISCHARGE & POWER RAIL	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :** *George Chen*
		SHEET 43 **OF** 60		**LIBRARY DATE :**	

DCIN JACK

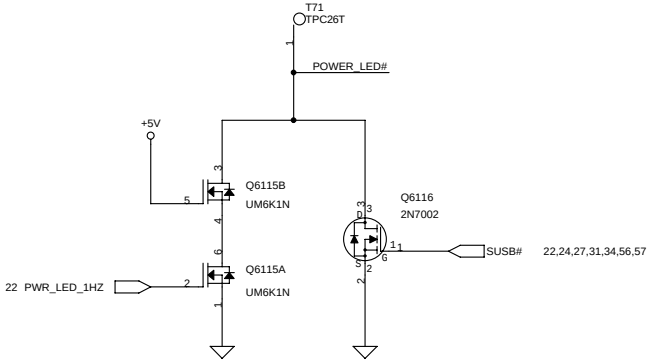


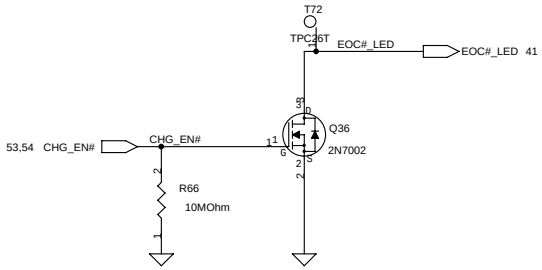
Battery Connector

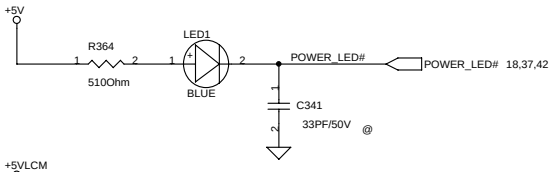


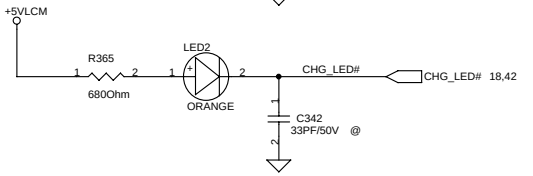
PROJECT: W6F	**REVISION** 2.0	**DATE:** Wednesday, January 11, 2006 **SHEET** 44 **OF** 60	**DESCRIPTION:** DCIN JACK & BAT CON	**SCHEMATIC FILE NAME :** <Doc> **LIBRARY DATE :**	**DESIGN ENGINEER :** *George Chen*

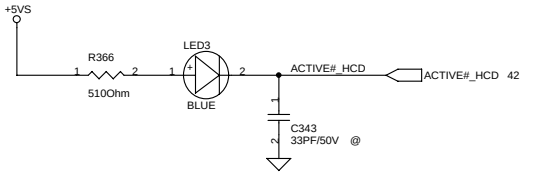
LEDs

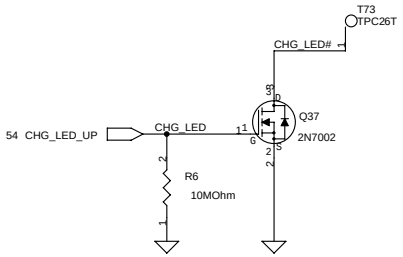




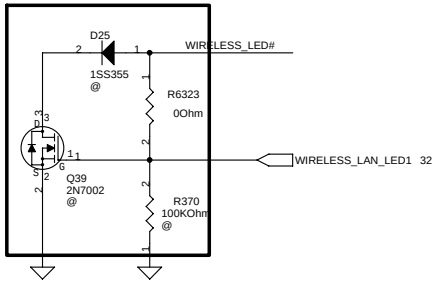


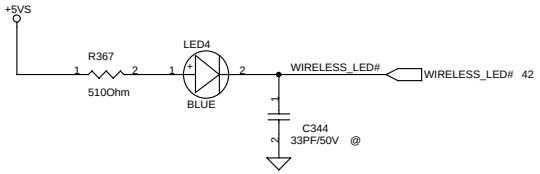


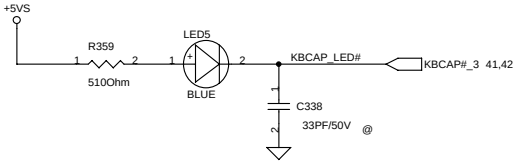


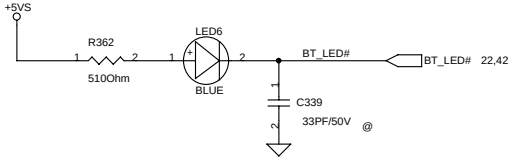


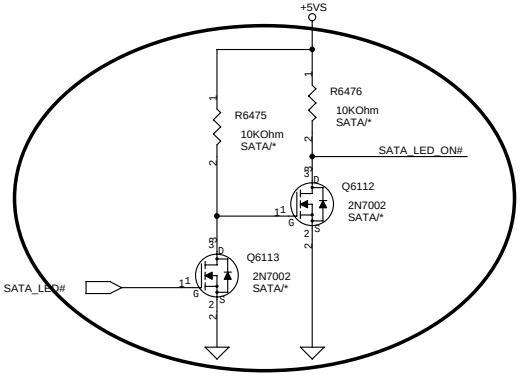
R1.1 -> R2.0



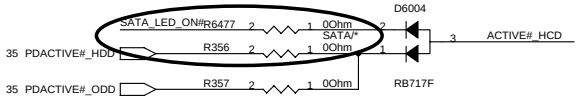




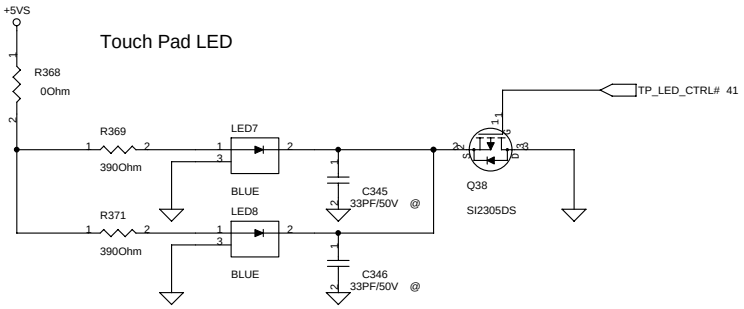




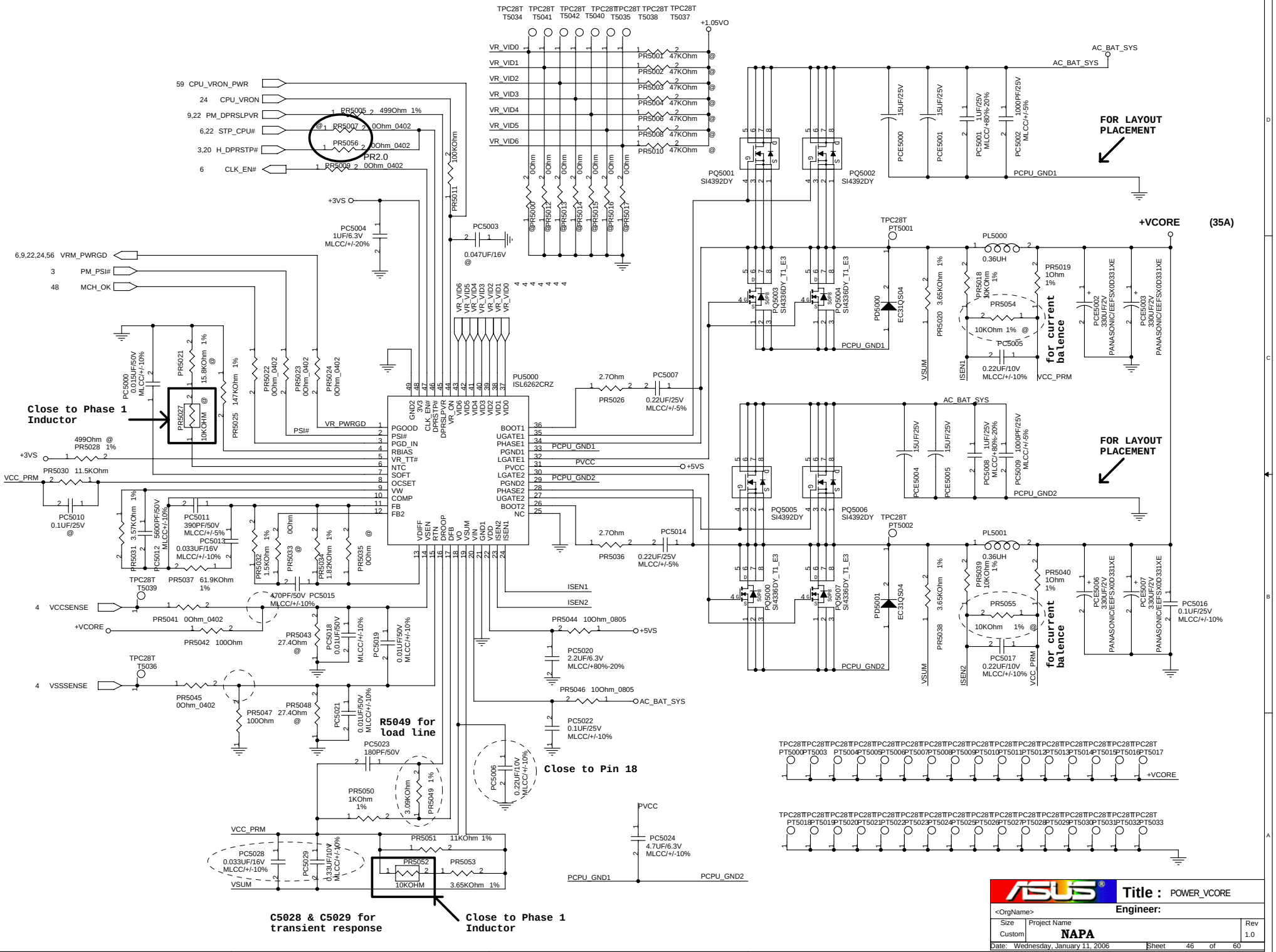
Option for SATA

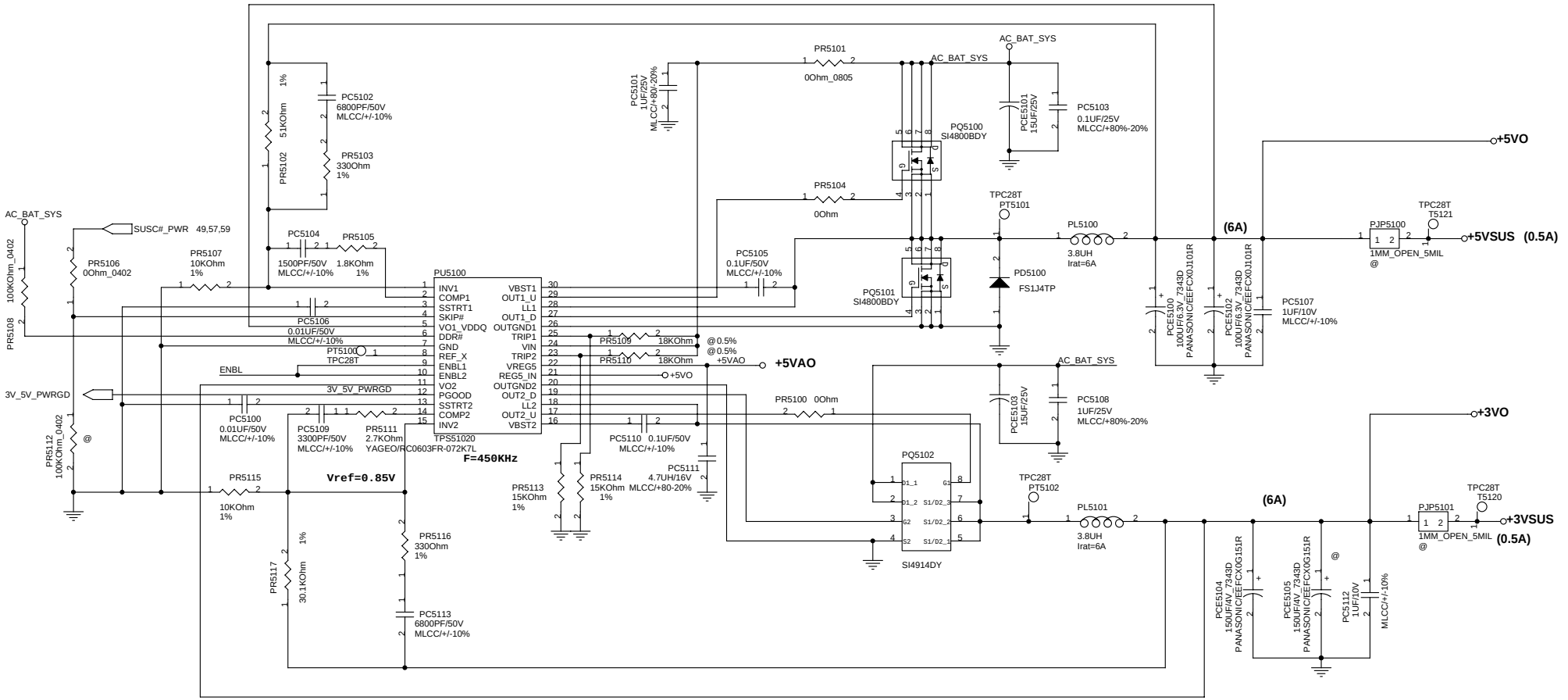


Touch Pad LED

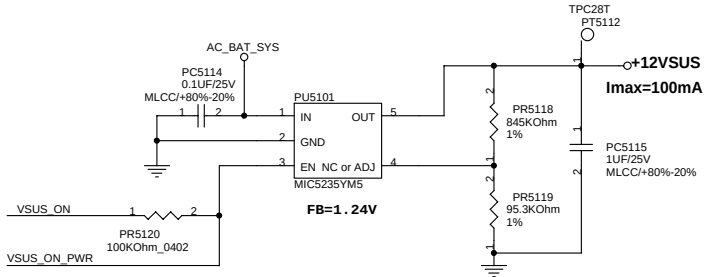


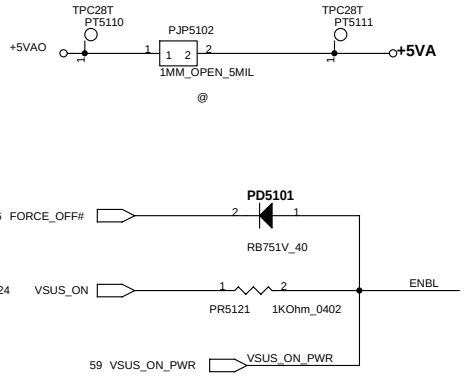
PROJECT: W6F	REVISION 2.0	DATE: Wednesday, January 11, 2006	DESCRIPTION: LEDs	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER : George Chen
		SHEET 45 OF 60		LIBRARY DATE :	

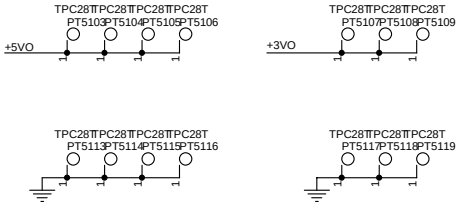

+1.05VO
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
PR5001 47KOhm
PR5002 47KOhm
PR5003 47KOhm
PR5004 47KOhm
PR5006 47KOhm
PR5008 47KOhm
PR5010 47KOhm
59 CPU_VRON_PWR
24 CPU_VRON
9,22 PM_DPRSLPVR
6,22 STP_CPU#
3,20 H_DPRSTP#
6 CLK_EN#
PR5005 499Ohm 1%
PR5007 0Ohm_0402
PR5056 0Ohm_0402
PR2.0
PR5009 0Ohm_0402
PR5011 100KOhm
+3VS
PC5004 1UF/6.3V MLCC/+/-20%
PC5003 0.047UF/16V
6,9,22,24,56 VRM_PWRGD
3 PM_PSI#
48 MCH_OK
PU5000 ISL6262CRZ
PGOOD
PSI#
PGD_IN
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
VDD1
VDD
ISEN2
ISEN1
VR_PWRGD
PSI#
Close to Phase 1 Inductor
PR5027 10KOHM @
PR5025 147KOhm 1%
PR5024 0Ohm_0402
PR5023 0Ohm_0402
PR5022 0Ohm_0402
PC5000 0.015UF/50V MLCC/+/-10%
PR5021 15.8KOhm 1% @
499Ohm @ PR5028 1%
PR5030 11.5KOhm
VCC_PRM
PC5010 0.1UF/25V @
PR5031 3.57KOhm 1%
PC5012 5600PF/50V MLCC/+/-10%
PC5011 390PF/50V MLCC/+/-5%
PC5013 0.033UF/16V MLCC/+/-10%
PR5037 61.9KOhm 1%
PR5032 1.5KOhm 1%
PR5033 0Ohm @
PR5034 1.82KOhm 1%
PR5035 0Ohm @
TPC28T T5039
4 VCCSENSE
+VCORE
PR5041 0Ohm_0402
PR5042 100Ohm
470PF/50V PC5015 MLCC/+/-10%
PR5043 27.4Ohm @
PC5018 0.01UF/50V MLCC/+/-10%
PC5019 0.01UF/50V MLCC/+/-10%
TPC28T T5036
4 VSSENSE
PR5045 0Ohm_0402
PR5047 100Ohm
PR5048 27.4Ohm @
PC5021 0.01UF/50V MLCC/+/-10%
R5049 for load line
PC5023 180PF/50V
PR5050 1KOhm 1%
PR5049 3.09KOhm 1%
PC5006 0.22UF/10V MLCC/+/-10%
Close to Pin 18
VCC_PRM
PR5051 11KOhm 1%
PC5028 0.033UF/16V MLCC/+/-10%
PC5029 0.33UF/10V MLCC/+/-10%
PR5052 10KOHM
PR5053 3.65KOhm 1%
VSUM
C5028 & C5029 for transient response
Close to Phase 1 Inductor
2.7Ohm PC5007
PR5026 0.22UF/25V MLCC/+/-5%
PCPU_GND1
PVCC
+5VS
PCPU_GND2
2.7Ohm PC5014
PR5036 0.22UF/25V MLCC/+/-5%
ISEN1
ISEN2
PR5044 10Ohm_0805
PC5020 2.2UF/6.3V MLCC/+80%-20%
PR5046 10Ohm_0805
AC_BAT_SYS
PC5022 0.1UF/25V MLCC/+/-10%
PC5024 4.7UF/6.3V MLCC/+/-10%
PQ5001 SI4392DY
PQ5002 SI4392DY
PCE5000 15UF/25V
PCE5001 15UF/25V
PC5001 1UF/25V MLCC/+80%-20%
PC5002 1000PF/25V MLCC/+/-5%
FOR LAYOUT PLACEMENT
PQ5003 SI4336DY_T1_E3
PQ5004 SI4336DY_T1_E3
PD5000 EC31QS04
PR5020 3.65KOhm 1%
PR5018 10KOhm 1%
PR5019 1Ohm 1%
PR5054 10KOhm 1% @
PC5005 0.22UF/10V MLCC/+/-10%
for current balence
PCE5002 330UF/2V PANASONIC/EEFSX0D331XE
PCE5003 330UF/2V PANASONIC/EEFSX0D331XE
+VCORE (35A)
PL5000 0.36UH
PQ5005 SI4392DY
PQ5006 SI4392DY
PCE5004 15UF/25V
PCE5005 15UF/25V
PC5008 1UF/25V MLCC/+80%-20%
PC5009 1000PF/25V MLCC/+/-5%
PQ5007 SI4336DY_T1_E3
PD5001 EC31QS04
PR5038 3.65KOhm 1%
PR5039 10KOhm 1%
PR5040 1Ohm 1%
PR5055 10KOhm 1% @
PC5017 0.22UF/10V MLCC/+/-10%
PCE5006 330UF/2V PANASONIC/EEFSX0D331XE
PCE5007 330UF/2V PANASONIC/EEFSX0D331XE
PC5016 0.1UF/25V MLCC/+/-10%
PL5001 0.36UH
TPC28T PT5001
TPC28T PT5002
TPC28T PT5000 PT5003 PT5004 PT5005 PT5006 PT5007 PT5008 PT5009 PT5010 PT5011 PT5012 PT5013 PT5014 PT5015 PT5016 PT5017
TPC28T PT5018 PT5019 PT5020 PT5021 PT5022 PT5023 PT5024 PT5025 PT5026 PT5027 PT5028 PT5029 PT5030 PT5031 PT5032 PT5033
Title : POWER_VCORE
<OrgName>
Engineer:
Size Custom
Project Name NAPA
Rev 1.0
Date: Wednesday, January 11, 2006
Sheet 46 of 60



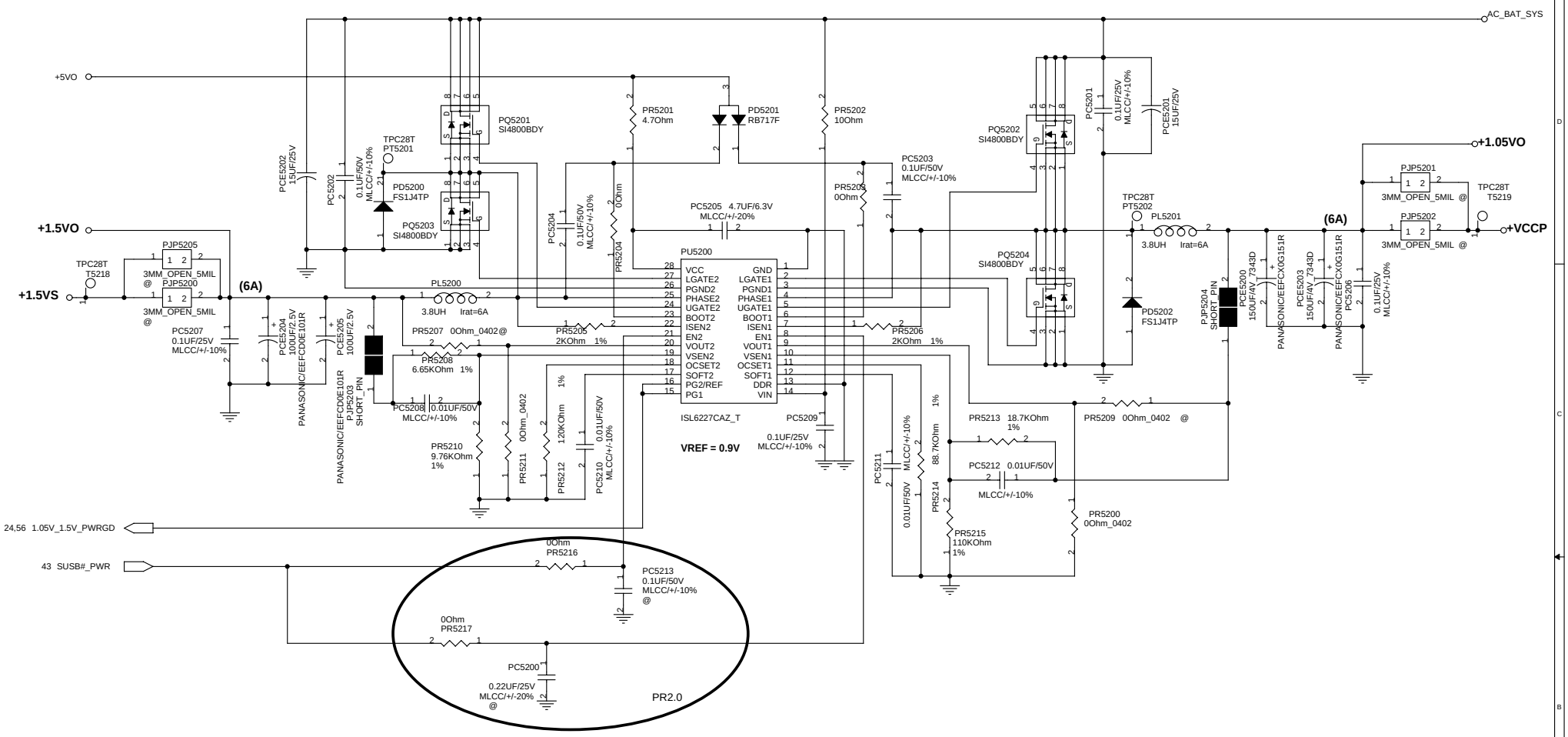
+12VSUS



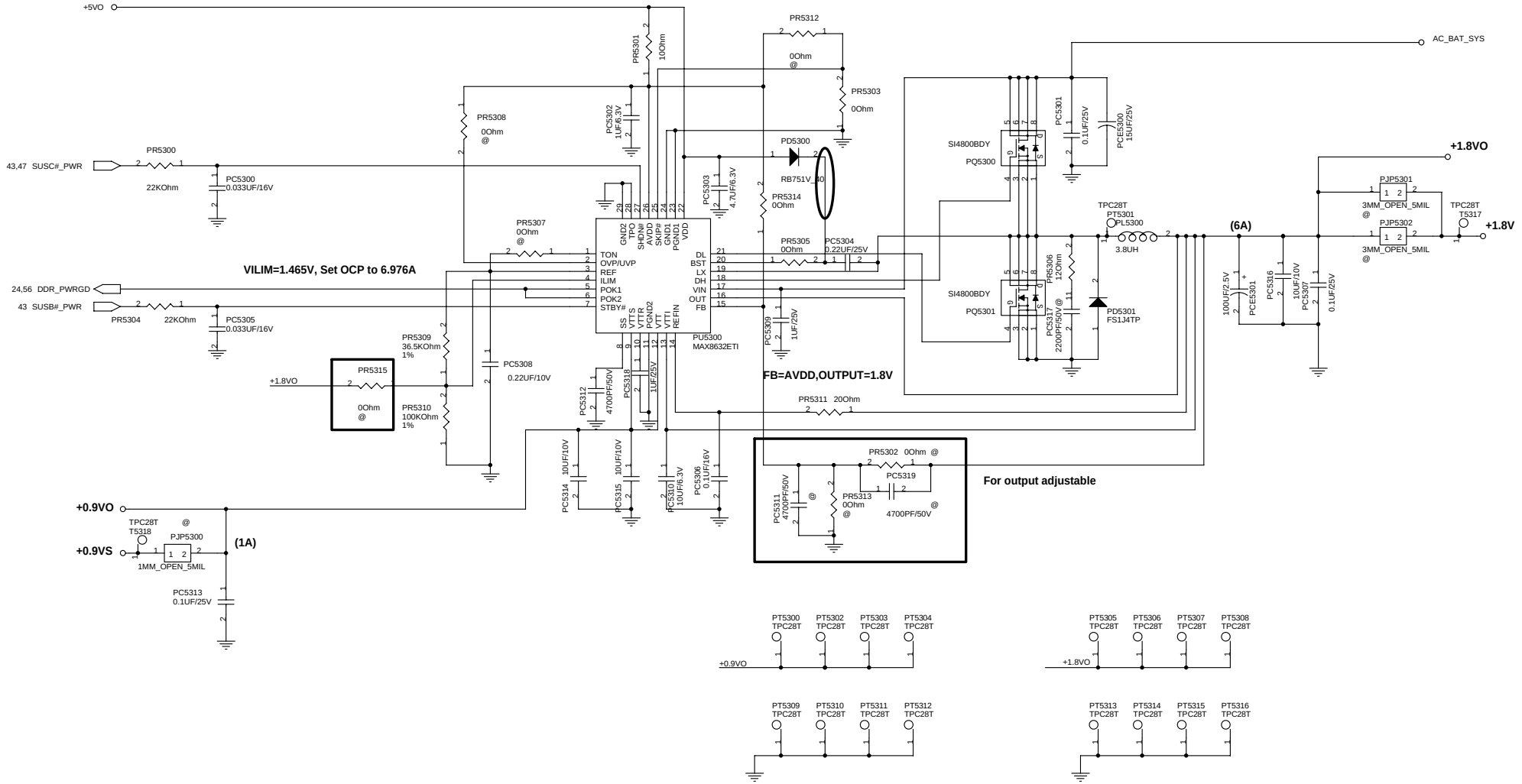




ASUS	Title : POWER_SYSTEM	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Wednesday, January 11, 2006	Sheet 47 of 60	

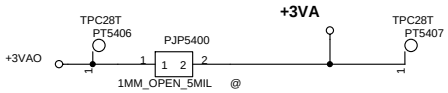


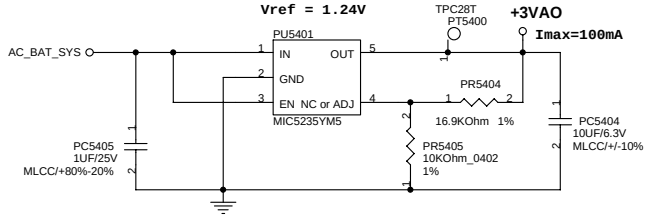
ASUS	Title : POWER_I/O_1.5VS & 1.05VS	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Wednesday, January 11, 2006	Sheet 48 of 60	



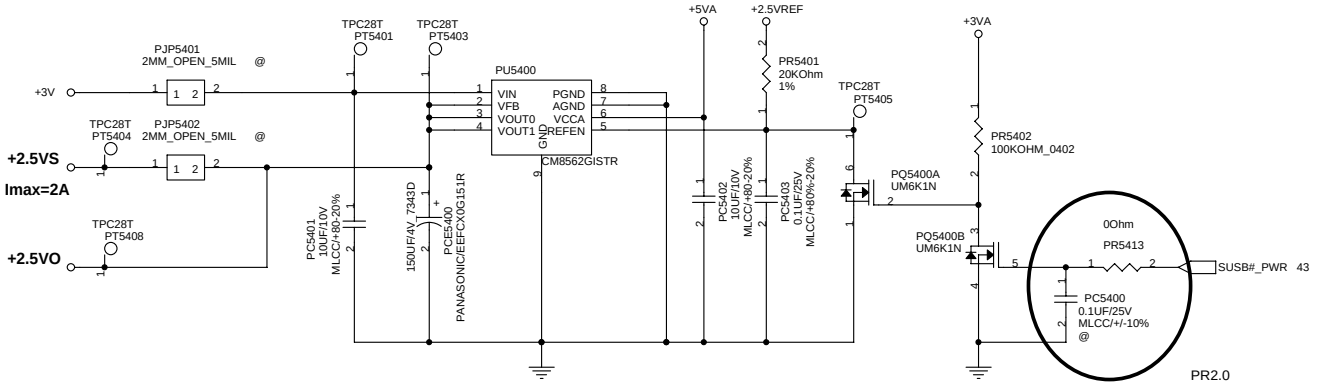
ASUS	Title :	POWER_I/O_DDR & VTT
<OrgName>	Engineer:	Mia / Charlse
Size: Custom	Project Name: A8J	Rev: 1.2
Date: Wednesday, January 11, 2006	Sheet 49 of 60	

+3VA0





+2.5VS



Title : POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Wednesday, January 11, 2006	Sheet 50 of 60	

Title : VGA_CORE & RAM

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	1.0

Date: Wednesday, January 11, 2006 Sheet 51 of 60

Title : +1.2VSP

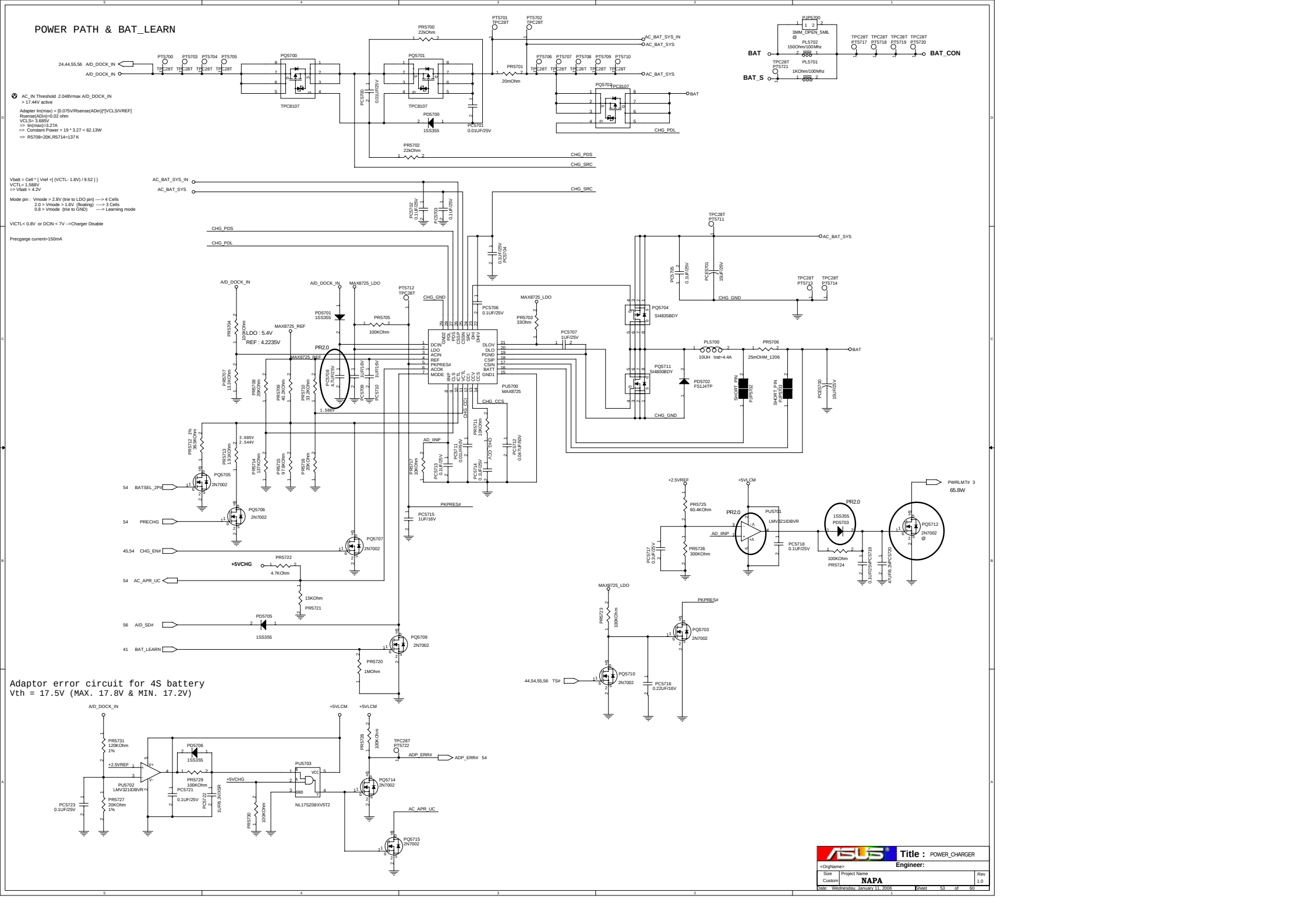
<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	1.0

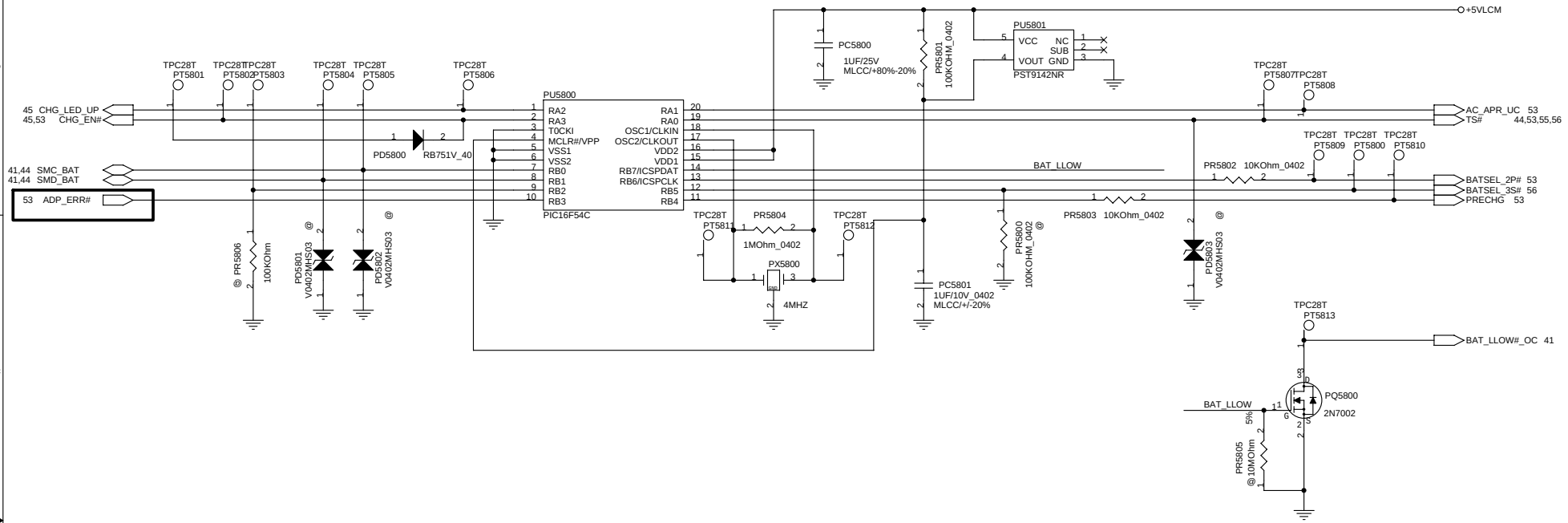
Date: Wednesday, January 11, 2006 Sheet 52 of 60

POWER PATH & BAT_LEARN



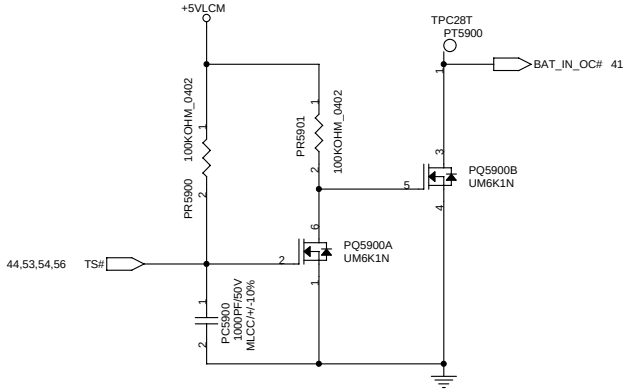
Title : POWER_CHARGER			
<OrgName>	Engineer:		
Size: Custom	Project Name: NAPA		Rev: 1.0
Date: Wednesday, January 11, 2006	Sheet 53 of 60		

PIC16F54C

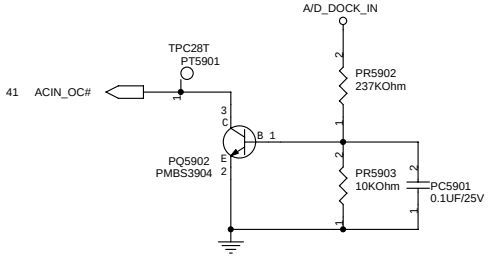


ASUS	Title : POWER_PIC	
<OrgName>	Engineer:	
Size: Custom	Project Name: W6F	Rev: 1.0
Date: Wednesday, January 11, 2006	Sheet 54 of 60	

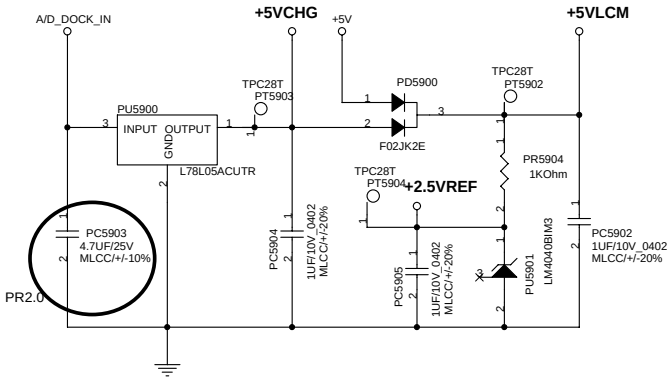
BATTERY IN DETECT



ADAPTER IN DETECT

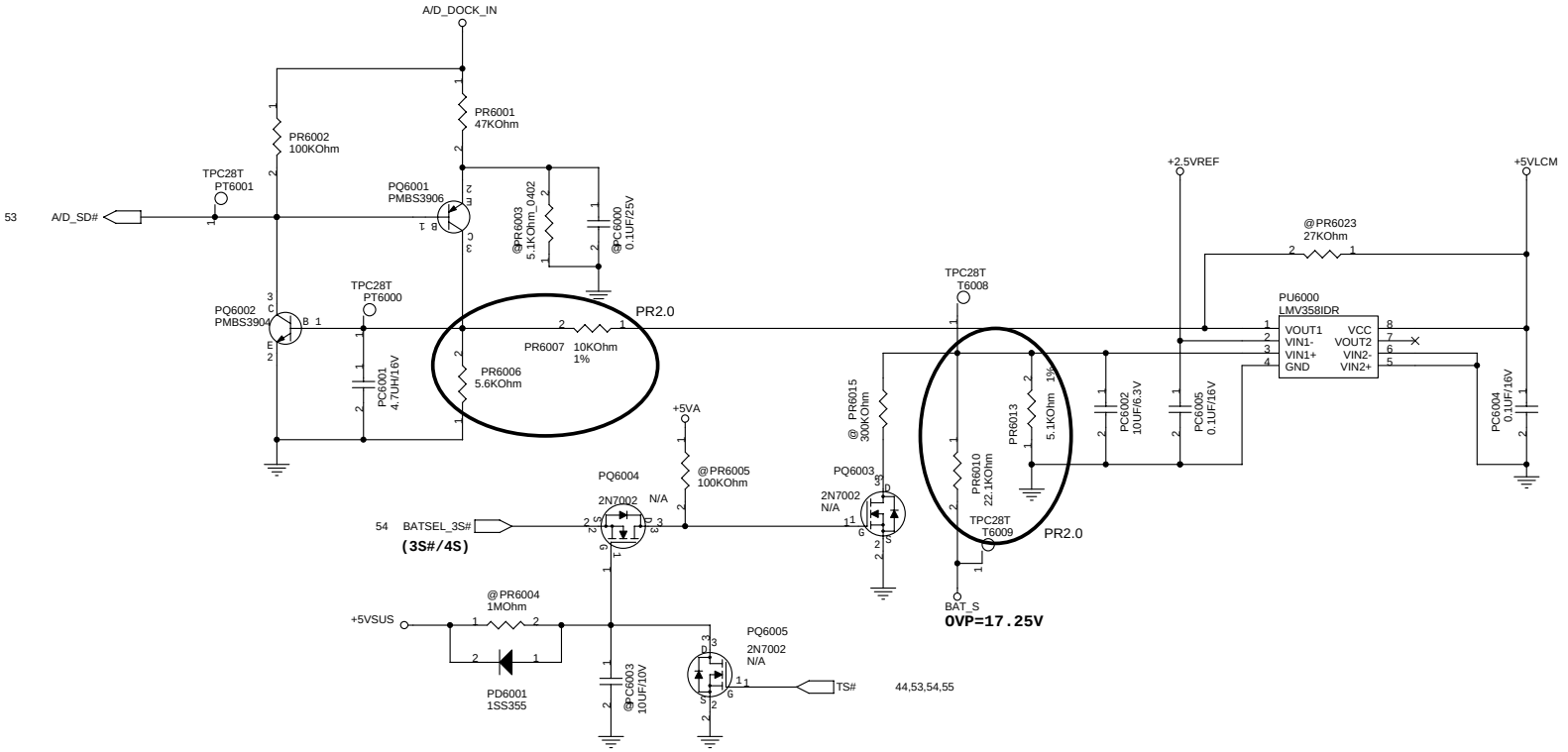


+5VLCM, +5VCHG & +2.5VREF

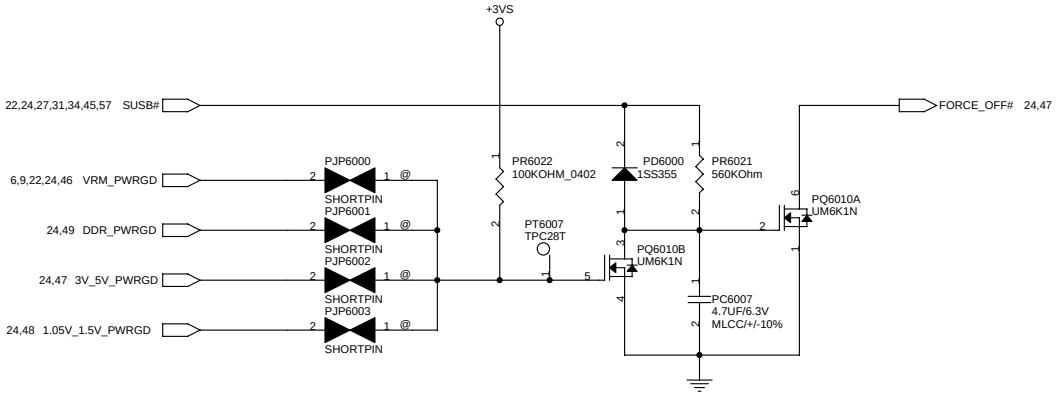


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Wednesday, January 11, 2006	Sheet 55 of 60	

BATTERY A/D_SD# (OVP)



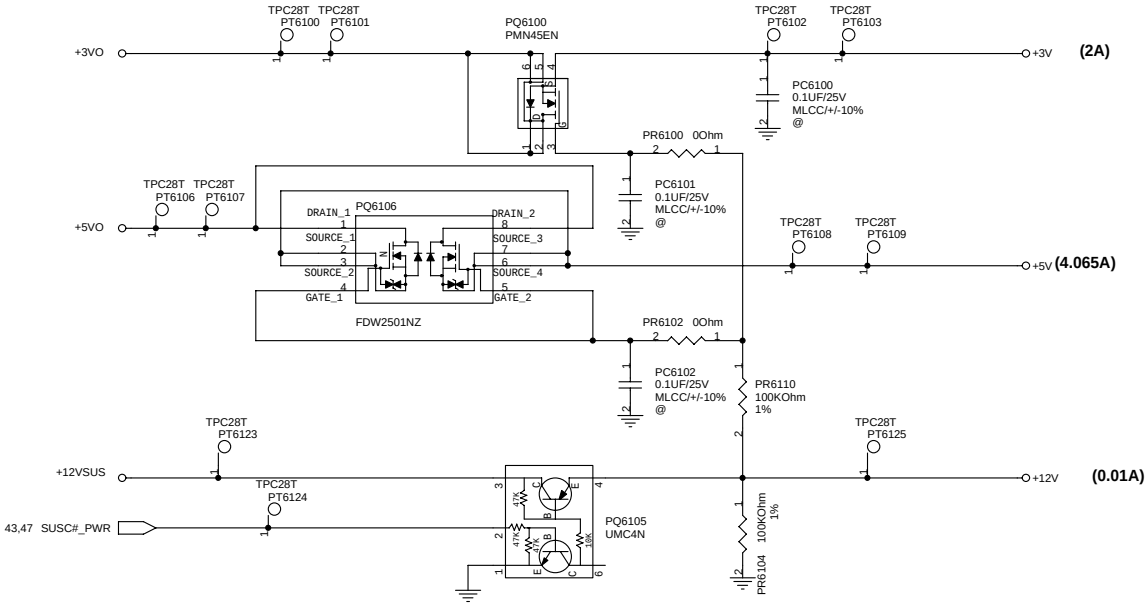
POWER GOOD DETECTER

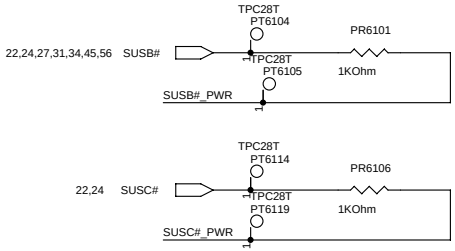


TPC28T PT6003 1 VRM_PWRGD
TPC28T PT6004 1 DDR_PWRGD
TPC28T PT6005 1 3V_5V_PWRGD
TPC28T PT6006 1 1.05V_1.5V_PWRGD

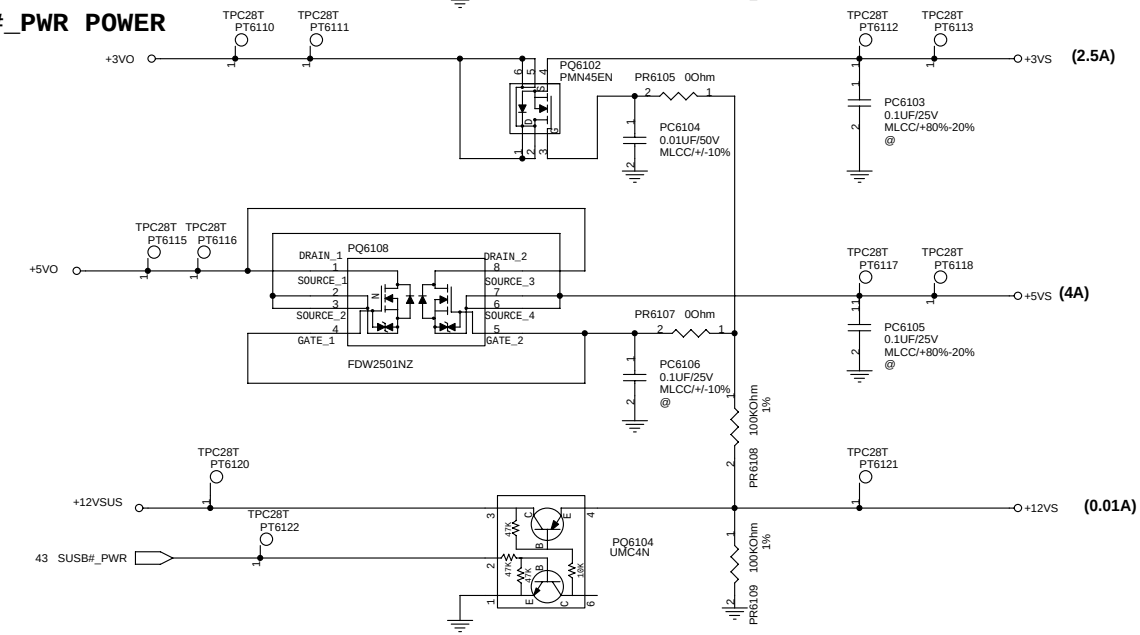
Title : POWER_PROTECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Wednesday, January 11, 2006	Sheet 56 of 60	

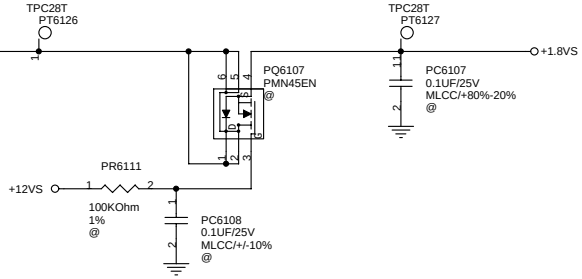
SUSC#_PWR POWER



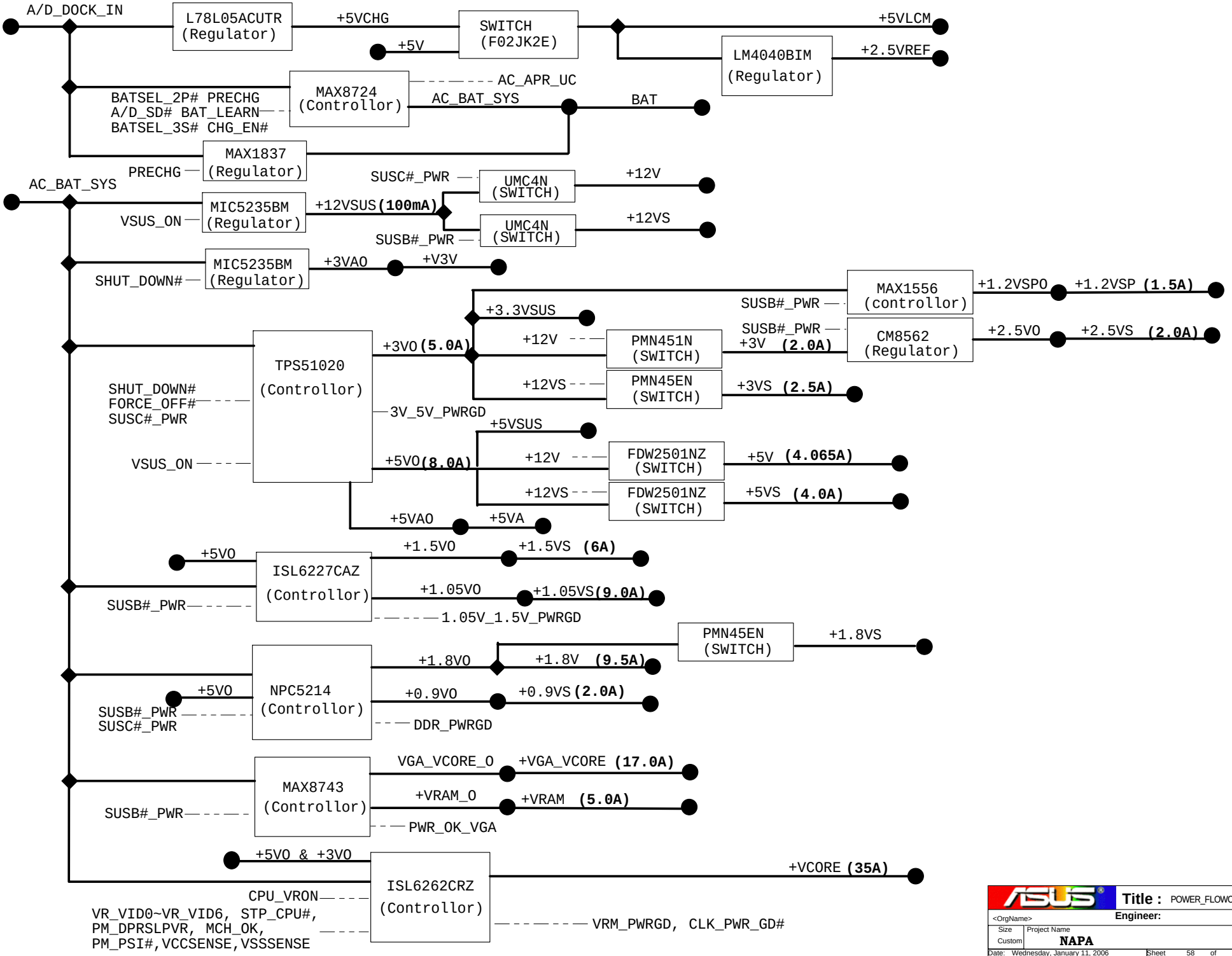


SUSB#_PWR POWER





ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Wednesday, January 11, 2006	Sheet 57 of 60	



Title : POWER_FLOWCHART		
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Wednesday, January 11, 2006	Sheet 58 of 60	

AC_BAT_SYS → AC_BAT_SYS 18,24,46,47,48,49,50,53

+3VA → +3VA 24,37,39,50

+5VA → +5VA 47,50,56

+5VO → +5VO 47,48,49,57

+3VO → +3VO 47,48,57

+3VSUS → +3VSUS 19,22,23,24,27,29,30,39,40,41,43,47

+5VSUS → +5VSUS 7,23,25,47,56

+3V → +3V 22,24,29,30,31,32,33,34,37,40,41,43,50,57

+3VS → +3VS 5,6,7,9,11,13,17,18,21,22,23,24,25,31,32,34,35,37,39,40,41,43,46,48,56,57

+12VSUS → +12VSUS 47,57

+12V → +12V 27,28,57

+12VS → +12VS 18,19,57

+5V → +5V 9,11,25,27,29,34,36,37,42,43,45,55,57

+5VS → +5VS 7,9,11,19,23,24,25,27,29,35,39,41,42,43,45,46,57

+2.5VO → +2.5VO 50

+2.5VS → +2.5VS 11,50

+1.8VO → +1.8VO 49,57

+1.8V → +1.8V 9,12,14,15,17,49

+1.8VS → +1.8VS 57

+VCCP → +VCCP 3,4,6,8,11,12,20,23,48

+0.9VS → +0.9VS 16,49

BAT → BAT 53

+5VCHG → +5VCHG 53,55

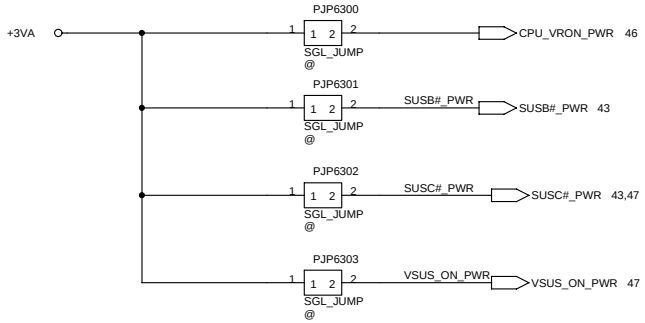
+5VLCM → +5VLCM 18,41,42,45,53,54,55,56

+2.5VREF → +2.5VREF 50,53,55,56

+VCORE → +VCORE 4,7,41,46

BAT_CON → BAT_CON 44,53

FOR POWER TEST



Title : POWER_SIGNAL		
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Wednesday, January 11, 2006	Sheet 59 of 60	

Rev	Date	Description
R1.0	2005/10/15	1. Initial release.
R1.1	2005/11/25	1. CHANGE CLOCK GEN. (ICS954213 -> ICS954310) - PAGE6 2. ADD SPREAD SPECTRUM LCD DIFFERENTIAL CLOCK TO MCH - PAGE6 3. CHANGE EXPRESS CARD CONNECTOR VENDOR (TYCO -> TAI-TWUN) - PAGE 31
R2.0	2005/11/30	1. RESERVE Q6117 TO KEEP RESET DELAY TIME - PAGE24
	2005/12/06	1. CHANGE CLOCK GEN. ICS954310BGLFT TO ICS954310CGLFT - PAGE6 2. ADD CLOCK GEN. STRAPPING FOR PIN 8 TO CONTROLL SRC CLOCK/ PCIECLK -PAGE6 3. SHIFT CLK_CPU_BCLK TO CPUCLK1, AND CLK_MCH_BCLK TO CPUCLK0 - PAGE6
	2005/01/06 ECN 15044	1. REMOVE R401, R402 AND C401 TO KEEP LAN TRANSITION DIFFERENTIAL PAIR IMPEDANCE IN REASONABLE REGION - PAGE 29 2. REMOVE R109 FOR CPU_SLP INTEL RECOMMAND. THIS SIGNAL SHOULD BE CONNECTED TO MCH OR ICH ONLY - PAGE 20
	2005/01/10 ECN 15068	1. ADD R6312 FOR FORCE OFF PROTECTION FUNCTION - PAGE 24 2. ADD R156 AND R165 TO CHANGE PCB ID FROM 000 TO 001 (REV 2.0 -> 2.1) - PAGE 22

Rev	Date	Description

ASUS	**PROJECT:** W6F	**REVISION** 1.1	**DATE:** Wednesday, January 11, 2006 **SHEET** 60 **OF** 60	**DESCRIPTION:** REV. HISTORY	**SCHEMATIC FILE NAME :** <Doc> **LIBRARY DATE :**	**DESIGN ENGINEER :** *George Chen*