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22	SIO(IT8772E-EX)	
23	LAN(RTL8111GA)	
24	Audio Codec(ALC662-VD)	
25	HDMI Level Shifter/Conn	
26	CRT BORAD CONNECTOR	
27	FAN CONTROL	
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Project Name: Borg
Project Code: 3PD007010001
PCB Number : 13057-1

On Board Header

CONN	Default	DESCRIPTION
CMOS1	1-2	CMOS CLEAR
SPDIF1		HDMI SPDIF 1x4 pin
AUDH1		Audio Front Panel 2x5 pin
FANC1/FANC2		CPU FAN CONN 3/4 pin
FANS1/FANS2		CPU FAN CONN 3/4 pin
USB2F1		Front USB 2.0
USB2F2		Front USB 2.0
LEDH1		Front Panel 2x7 pin
DBGH1		Debug Port 2x7
GPIO1		GPIO 1x2 pin
GPIO2		GPIO 1x2 pin
BT1		Battery Holder
XDP1		XDP CONN (CPU Debug)
ATX1/ATX2		ATX Power 24/20 pin

XTAL Description

XTAL	Function	Frequency	Spec	Capacitance
X1801	CPU	25M	+/-30ppm CL:12P	C1814=12pF C1815=12pF
X1802	CPU	32.768K	+/-20ppm CL:7P	C1817=15pF C1818=15pF
X2101	LAN	25M	+/-30ppm CL:12P	C2116=15pF C2117=15pF
X3501	HUB	12M	+/-20ppm CL:20P	C4603=12pF C4604=12pF
OSC1	SIO	48M		

BOM Configuration

Unmount: (R)

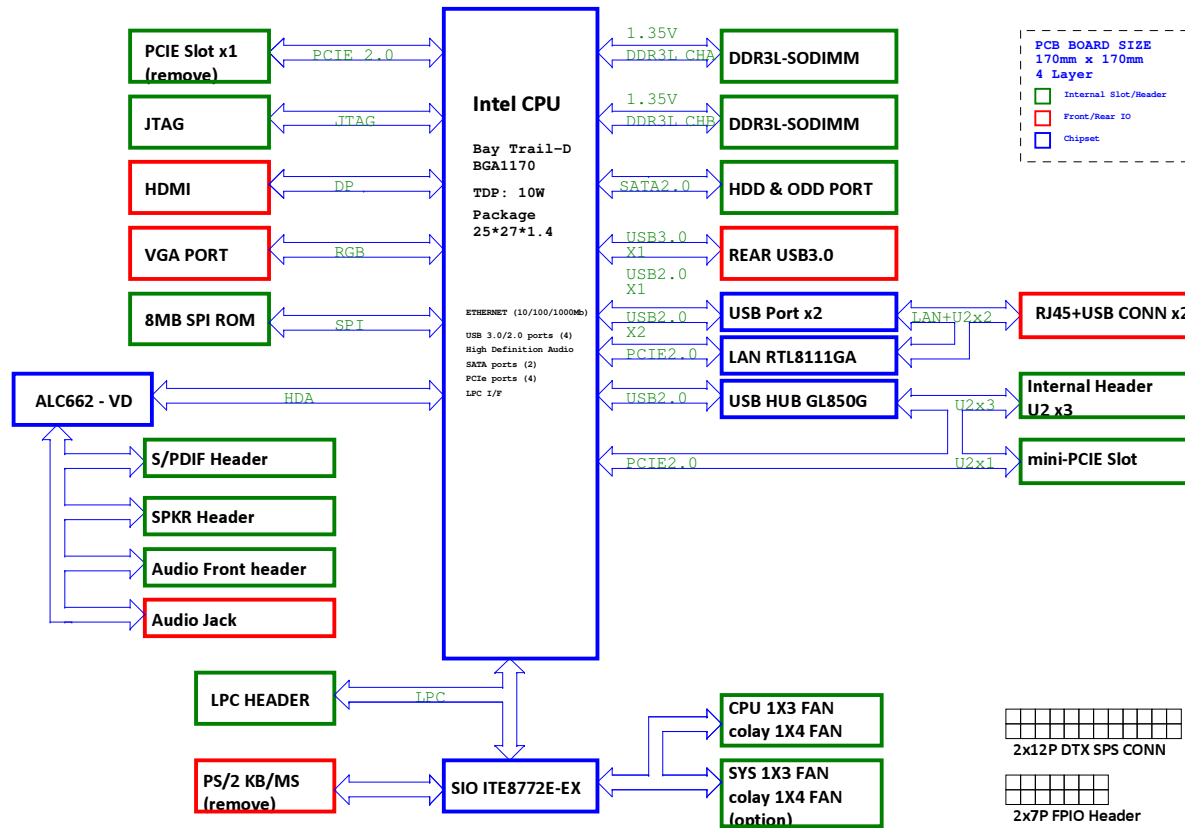
Compliant with RoHS
Compliant with Win8 WHCK
Compliant with ES 6.0
Compliant with MS MDA 2013
Compliant with HDMI v1.4a Certificate
Compliant with EuP LOT 3

CPU cooler: 360.00702.0001

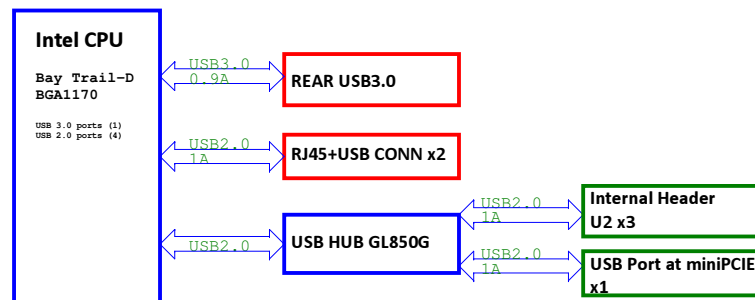
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Title Cover Page			
Size	Document Number	Rev	
Custom	Bay Trail-D	SB	
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Project Name: Borg
Project Code: 3PD007010001
PCB Version: -1
PCB Number : 13057-1




USB Port



2x12P DTX SPS CONN

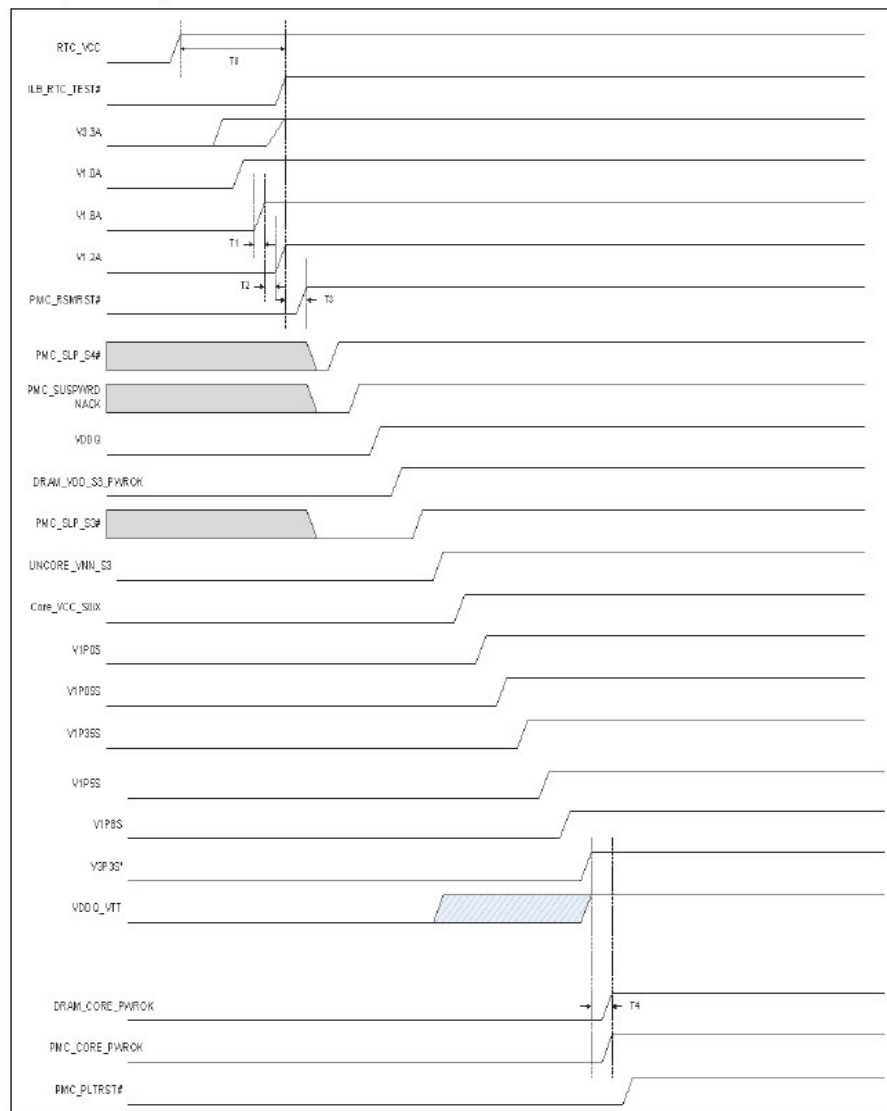
2x7P FPIO Header

+VDDIO	SO-DIMM
+DDR3_VTT	V_MEM_8 1.350V / 3A
	V_MEM_VTT 0.675V / 1A
+3P3V_AUX	mini-PCI-E
+3P3V_MAIN	3.3V; 1A
	1.5V; 0.5A
+3P3V_AUX	LAN: RTL8111GA
	3.3V; 70mA
+1.05V_LAN (Internal)	1.05V/300mA (Internal Switch)
+3P3V_MAIN	SIO: PT872E-EX
+3P3V_AUX	3.3V; 300mA
	3.3V; 50mA
+3P3V_AUX	HD CODEC ALC662-VD
+3P3V_MAIN	DVDD 3.3V; 50mA
	DVDD 3.3V; 50mA
V1P8S	BIOS ROM
	1.8V; 67mA
+12V_MAIN	CPU FAN
	12V; 200mA
SB5VCC	USB HUB - GL850-G
	5V; 52.4mA
SB5VCC	USB2.0 VBUS
	5V; 500mA
+5V_MAIN	HDD
+12V_MAIN	5V; 850mA
	12V; 662mA
+5V_MAIN	ODD
+12V_MAIN	5V; 900mA
	12V; 1500mA

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Title Power Delivery Chart			
Size A4	Customer Document Number Bay Trail-D		Rev SB
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Power-up Sequencing for the Bay Trail Platform

Figure 4-41. Entry Desktop SoC Cold Boot



Bay Trail-D SoC			TDP = 10W
VCORE	VCORE	0.700 - 1.100V ; 15A	TDC
GFX_CORE	GFX_CORE	0.700 - 1.000V ; 10A	TDC
V1P35S	V1P35S	1.350V ; 1.056A	
V1P0A	V1P0A	1.000V ; 0.202A	
V1P0S	V1P0S	1.000V ; 0.549A	
V1P05S	V1P05S	1.050V ; 0.720A	
V1P2A	V1P2A	1.200V ; 0.035A	
V1P8A	V1P8A	1.800V ; 0.053A	
V1P8S	V1P8S	1.800V ; 0.142A	
V3P3A	V3P3A	3.300V ; 0.010A	
V3P3S	V3P3S	3.300V ; 0.013A	
+RTCVCC	VRTC	3.000V ; 1.600uA	

+VDDIO	SO-DIMM	X2
+DDR3_VTT	V_MEM_S 1.350V ; 3A	
	V_MEM_VTT 0.675V ; 1A	
+3P3V_AUX	mini-PCI-E	
(+1P5V_MAIN)	3.3V ; 1A	
	1.5V ; 0.5A	
+3P3V_AUX	LAN- RTL81111GA	
	3.3V ; 70mA	
+1.05V_LAN (Internal)	1.05V ; 300mA (Internal Switch)	
+3P3V_MAIN	SIO- IT8772E-EX	
+3P3V_AUX	3.3V ; 300mA	
	DVDD 3.3V ; 50mA	
+3P3V_MAIN	HD CODEC ALC662-VD	
	AVDD 3.3V ; 50mA	
	DVDD 3.3V ; 50mA	
V1P8S	BIOS ROM	
	1.8V ; 67mA	

+12V_MAIN	CPU FAN	
	12V ; 200mA	
USBVCC	USB HUB - GL850-G	
	5V ; 52.4mA	
USBVCC	USB2.0 VBUS	X6
	5V ; 500mA	
+5V_MAIN	HDD	
+12V_MAIN	5V ; 858mA	
	12V ; 662mA	
+5V_MAIN	ODD	
+12V_MAIN	5V ; 900mA	
	12V ; 1500mA	

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Title

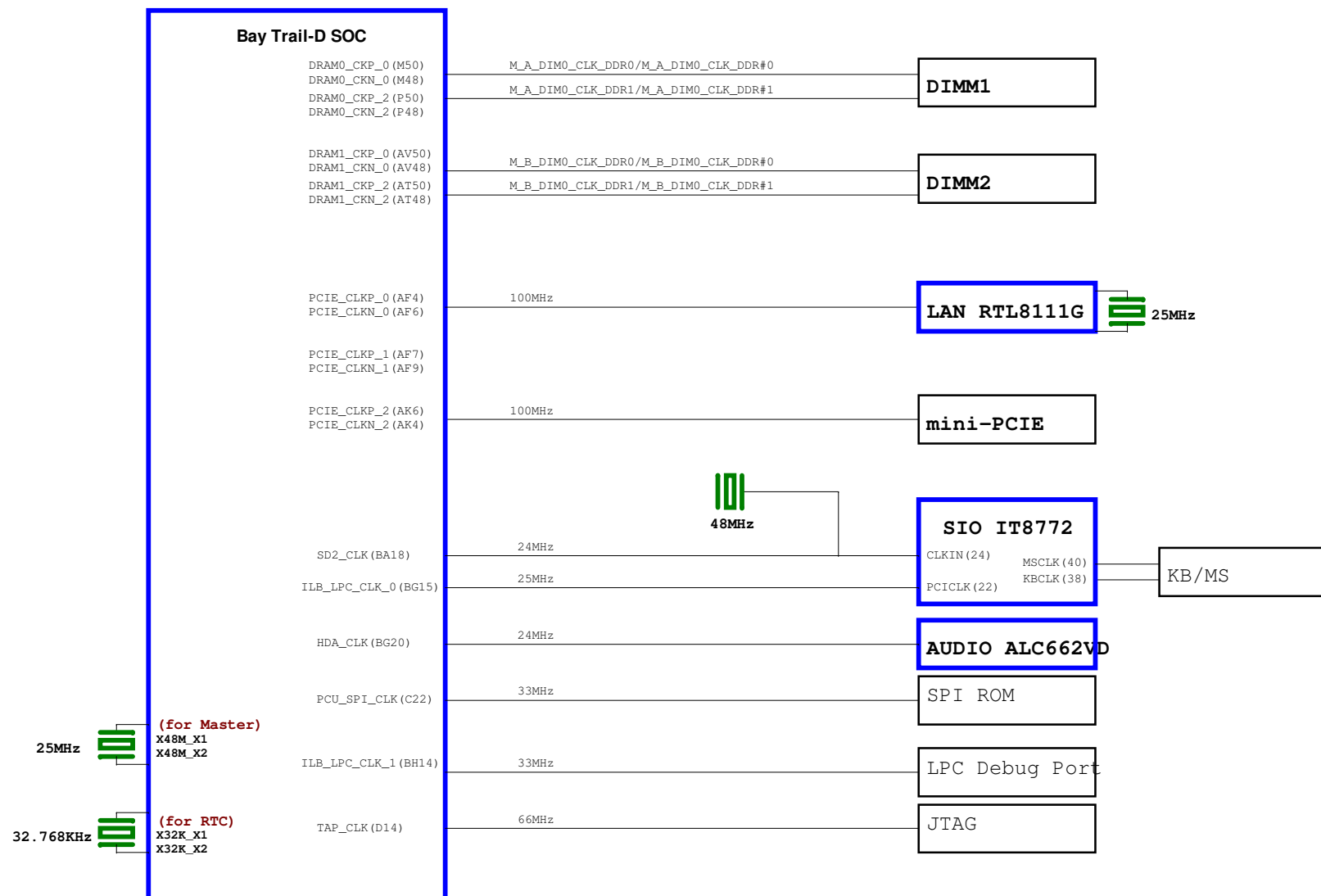
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BDocument Number
Bay Trail-DRev
SB

Date:

Friday, November 15, 2013

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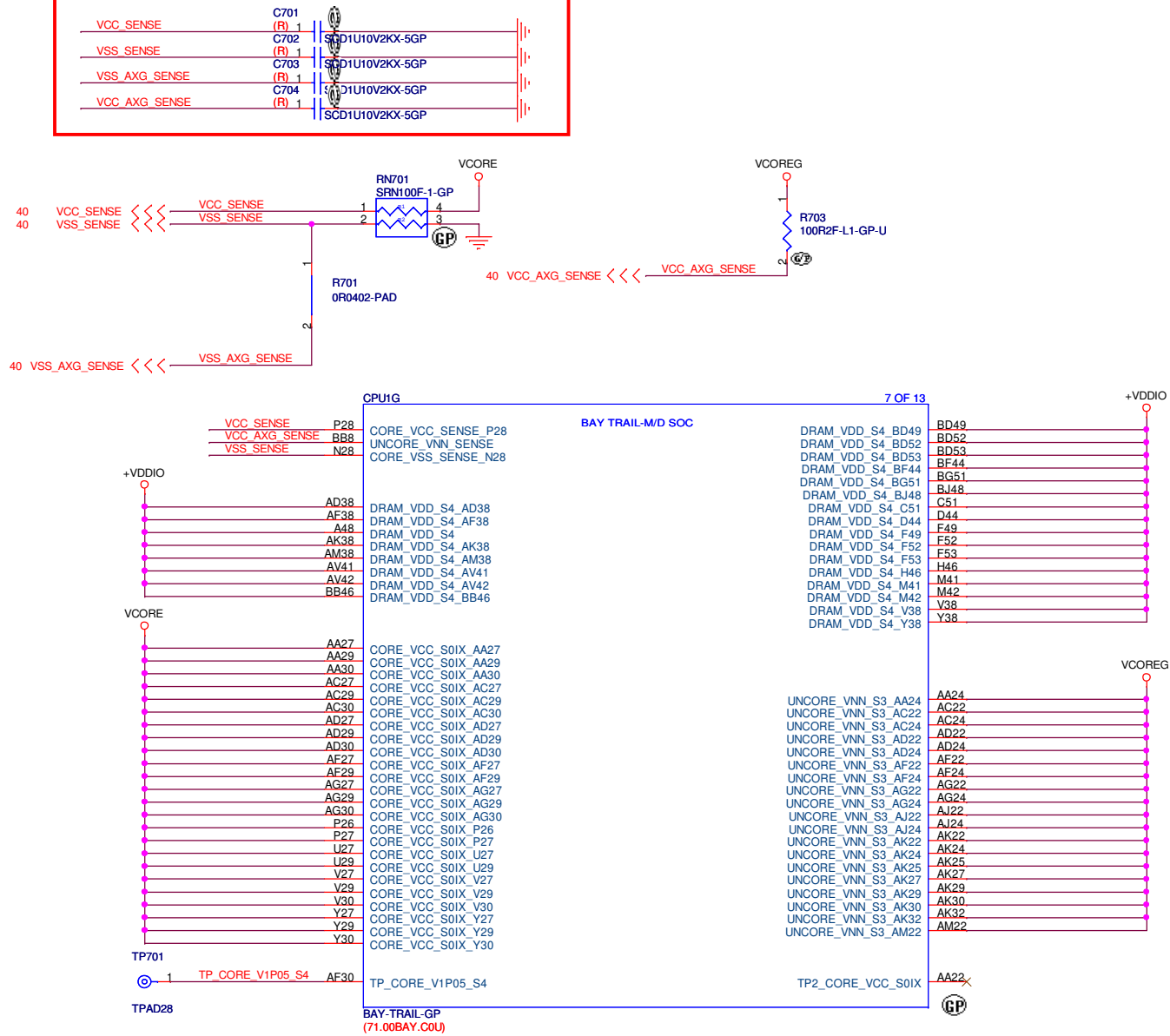
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IC Pin Name	Power Well	Default	Default State	Usage	GPIOs Programming				
					S0	S1	S2	S4	S5
GENINT1_L/GPIO32	VDD_33	General input	Input 5.2K PU	ID0	GPI	GPI	GPI	GPI	GPI
GENINT2_L/GPIO33	VDD_33	General input	Input 5.2K PU	ID1	GPI	GPI	GPI	GPI	GPI
SC0/GPIO43	VDD_33	Input Tri-state	Input Tri-state	SM0_CLK	Native	Native	Native	Native	Native
SD_LED/GPIO45	VDD_33	Output HIGH	no use	no use	N/A	N/A	N/A	N/A	N/A
SDA0/GPIO27	VDD_33	Input Tri-state	Input Tri-state	SM0_DAT_A	Native	Native	Native	Native	Native
SERIRQ/GPIO48	VDD_33	Input 5.2K PU	Input 5.2K PU	SERIRQ_N	Native	Native	Native	Native	Native
GPIO49	VDD_33	Input 5.2K PU	Input 5.2K PU	RISER_ID_0	GPI	GPI	GPI	GPI	GPI
GPIO50	VDD_33	Input 5.2K PU	Input 5.2K PU	RISER_ID_1	GPI	GPI	GPI	GPI	GPI
GPIO51	VDD_33	Input 5.2K PU	Input 5.2K PU	PCIE1_RST_N	GPO	GPO	GPO	GPO	GPO
FANOUT0/GPIO52	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	N/A	N/A	N/A	N/A	N/A
DEVSLP[0]/GPIO55	VDD_33	Input 5.2K PU	Input 5.2K PU	SIO_GP11	GPO	GPI	GPI	GPI	GPI
FANIN0/GPIO56	VDD_33	Input 5.2K PU	Input 5.2K PU	ST0_GP15	GPO	GPI	GPI	GPI	GPI
GPIO57	VDD_33	Input 5.2K PU	Input 5.2K PU	X16_PRESENT	GPO	GPO	GPO	GPO	GPO
GPIO58	VDD_33	Input 5.2K PU	Input 5.2K PU	PCIE15_DET0	GPO	GPO	GPO	GPO	GPO
DEVSLP[1]/GPIO59	VDD_33	Input 5.2K PU	Input 5.2K PU	PCIE15_DET1	GPO	GPO	GPO	GPO	GPO
CLK_REQ0_L/ SATA_0S0_L	VDD_33	Input 5.2K PU	Input 5.2K PU	BLANK_CLK_REQ_N_1	Native	Native	Native	Native	Native
CLK_REQ1_L/GPIO61	VDD_33	Input 5.2K PU	Input 5.2K PU	ID0_CLK_N	GPO	GPO	GPO	GPO	GPO
CLK_REQ2_L/GPIO62	VDD_33	Input 5.2K PU	Input 5.2K PU	Test Point	N/A	N/A	N/A	N/A	N/A
CLK_REQ3_L/ SATA_1S1_L	VDD_33	Input 5.2K PU	Input 5.2K PU	LIM_BEL	GPI	GPI	GPI	GPI	GPI
SATA_3P1_L/GPIO63	VDD_33	Input 5.2K PU	Input 5.2K PU	FP_AUDIO_PRESENCE_N	GPI	GPI	GPI	GPI	GPI
GPIO64	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	N/A	N/A	N/A	N/A	N/A
CLK_REQ6_L/GPIO65/ QSD1N	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	Native	Native	Native	Native	Native
SPK0/GPIO66	VDD_33	Input 5.2K PU	Input 5.2K PU	FCH_SATA_LED_N	Native	Native	Native	Native	Native
SATA_ACT_L/GPIO67	VDD_33	Input 5.2K PU	Input 5.2K PU	AUD_DET	GPO	GPO	GPO	GPO	GPO
GPIO68	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	GPI	GPI	GPI	GPI	GPI
GPIO69	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	GPI	GPI	GPI	GPI	GPI
GPIO70	VDD_33	Tri-State	Tri-State	no use	N/A	N/A	N/A	N/A	N/A
GPIO71	VDD_33	Tri-State	Tri-State	APU_PROCHOT_N	GPO	GPO	GPO	GPO	GPO
SD_CLK/CLK_2/ GPIO72	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_CMD/GPIO73	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_CD/GPIO75	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_WP/GPIO76	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_DATA0/ SDAT1_2/ GPIO77	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_DATA1/ SDAT0_2/ GPIO78	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_DATA2/GPIO79	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SD_DATA3/GPIO80	VDD_33	Input 5.2K PU	Input 5.2K PU	no use	N/A	N/A	N/A	N/A	N/A
SPI_WF_L/GPIO161	VDD_33_ALW	Input 5.2K PU	Input 5.2K PU	no use	GPO	GPO	GPO	GPO	GPO
SPI_CLK/GPIO162	VDD_33_ALW	Input 5.2K PU	Input 5.2K PU	no use	Native	Native	Native	Native	Native
SPI_DO/GPIO163	VDD_34_ALW	Input 10K PU	Input 10K PU	SPI_CLK	Native	Native	Native	Native	Native
SPI_DI/GPIO164	VDD_36_ALW	Input 10K PU	Input 10K PU	SPI_DATAOUT	Native	Native	Native	Native	Native
SPI_CS1_L/GPIO165	VDD_37_ALW	Input 10K PU	Input 10K PU	SPI_DATAIN	Native	Native	Native	Native	Native
SPI_CS2_L/GPIO166	VDD_38_ALW	Input 10K PU	Input 10K PU	Test Point	N/A	N/A	N/A	N/A	N/A
AZ_S0IN0/GPIO167	VDD_33_SVDDIO_AZ_ALW	Input 50K PU	Input 50K PU	AZ_S0IN0	Native	Native	Native	Native	Native
AZ_S0IN1/GPIO168	VDD_33_SVDDIO_AZ_ALW	Input 50K PU	Input 50K PU	AZ_S0IN1	Native	Native	Native	Native	Native
AZ_S0IN2/GPIO169	VDD_33_SVDDIO_AZ_ALW	Input 50K PU	Input 50K PU	AZ_S0IN2	Native	Native	Native	Native	Native
AZ_S0IN3/GPIO170	VDD_33_SVDDIO_AZ_ALW	Input 50K PU	Input 50K PU	AZ_S0IN3	Native	Native	Native	Native	Native
GPIO174	VDD_33_ALW	Input 5.2K PU	Input 5.2K PU	no use	N/A	N/A	N/A	N/A	N/A
IR_LED_L/L8_L/ GPIO184	VDD_33_ALW	Input 10K PU	Input 10K PU	no use	N/A	N/A	N/A	N/A	N/A
SC1/GPIO227	VDD_33_ALW	Input Tri-state	Input Tri-state	SM1B1_CLK	Native	Native	Native	Native	Native
SDA1/GPIO228	VDD_33_ALW	Input Tri-state	Input Tri-state	SM1B1_DATA	Native	Native	Native	Native	Native
GA20IN/GEVENT0#	VDD_33	Input 5.2K PU	Input 5.2K PU	KADGATE	Native	Native	Native	Native	Native
GEVENT2#	VDD_33_ALW	Input 10K PU	Input 10K PU	SPI_SW	Native	Native	Native	Native	Native
LPC_PM0#/ GEVENT3#	VDD_33_ALW	Input 10K PU	Input 10K PU	PM0_B0_M	Native	Native	Native	Native	Native
GEVENT4#	VDD_33_ALW	Input 10K PU	Input 10K PU	THERMAL_SHUT#	GPI	GPI	GPI	GPI	GPI
LPC_P0W/ GEVENT5#	VDD_33_ALW	Input 10K PU	Input 10K PU	LPC_PD_N (Test point)	N/A	N/A	N/A	N/A	N/A
IR_TX1/ GEVENT6#	VDD_33_ALW	Input 10K PU	Input 10K PU	no use	N/A	N/A	N/A	N/A	N/A
GEVENT7#	VDD_33_ALW	Input 10K PU	Input 10K PU	no use	N/A	N/A	N/A	N/A	N/A
WAKE#/ GEVENT8#	VDD_33_ALW	Input 10K PU	Input 10K PU	PC_WAKE_N	Native	Native	Native	Native	Native
SPI_HOLD#/ GEVENT9#	VDD_33_ALW	Input 10K PU	Input 10K PU	no use	Native	Native	Native	Native	Native
GEVENT10#	VDD_33_ALW	Input 10K PU	Input 10K PU	no use	N/A	N/A	N/A	N/A	N/A
GEVENT11#	VDD_33_ALW	Input 10K PU	Input 10K PU	no use	N/A	N/A	N/A	N/A	N/A
USB_OC0#/ SPI_TPM_CS#/ TSTW/ GEVENT12#	VDD_33_ALW	Input 10K PU	Input 10K PU	USB_OC_01	Native	Native	Native	Native	Native
USB_OC1#/TDI/ GEVENT13#	VDD_33_ALW	Input 10K PU	Input 10K PU	USB_OC_02	Native	Native	Native	Native	Native
USB_OC2#/TCK/ GEVENT14#	VDD_33_ALW	Input 10K PU	Input 10K PU	USB_OC_03	Native	Native	Native	Native	Native
USB_OC3#/TDO/ GEVENT15#	VDD_33_ALW	Input 10K PU	Input 10K PU	USB_OC_04	Native	Native	Native	Native	Native

AC_PRE#/IR_RX0/ GEVENT16#	VDD_33_ALW	Input 10K PU	no use	N/A	N/A	N/A	N/A	N/A	N/A
GEVENT17#	VDD_33_ALW	Input 10K PU	no use	N/A	N/A	N/A	N/A	N/A	N/A
BLINK/ GEVENT18#	VDD_33_ALW	Input 10K PU	no use	N/A	N/A	N/A	N/A	N/A	N/A
SYS_RESET#/ GEVENT19#	VDD_33_ALW	Input 10K PU	PP_RST_N	GPI	Native	GPI	Native	GPI	Native
IR_RX1/ GEVENT20#	VDD_33_ALW	Input 10K PU	no use	N/A	N/A	N/A	N/A	N/A	N/A
IR_TX0/ GEVENT21#	VDD_33_ALW	Input 10K PU	no use	N/A	N/A	N/A	N/A	N/A	N/A
RIR/GEVENT22#	VDD_33_ALW	Input 10K PU	no use	N/A	N/A	N/A	N/A	N/A	N/A
LPC_SM1#/ GEVENT23#	VDD_33_ALW	Input 5.2K PU	no use	N/A	N/A	N/A	N/A	N/A	N/A

reserve the 0402 0.1u caps on reset for EMI.



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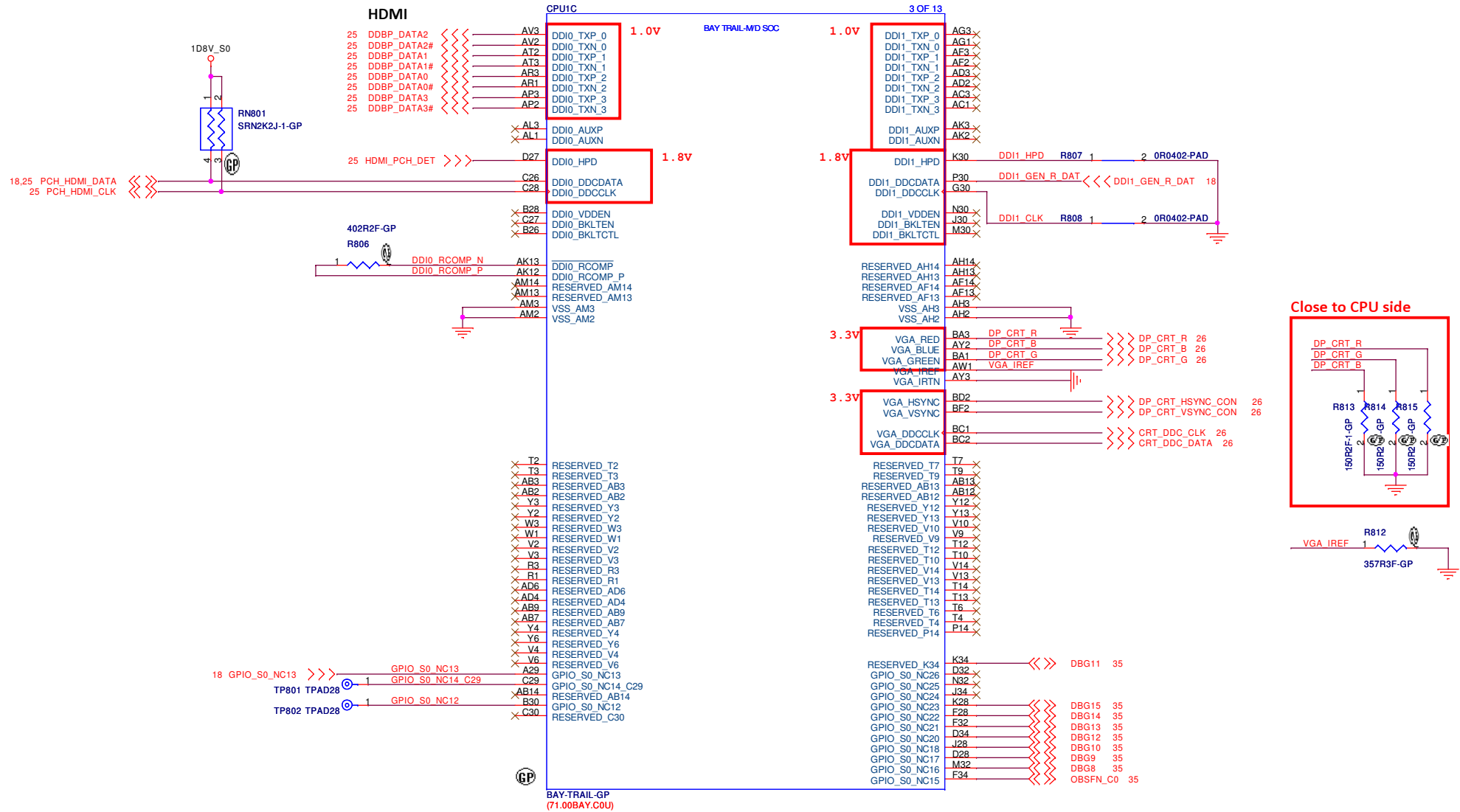
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CPU (VCC_CORE)

Size
Custom
Document Number
Bay Trail-D

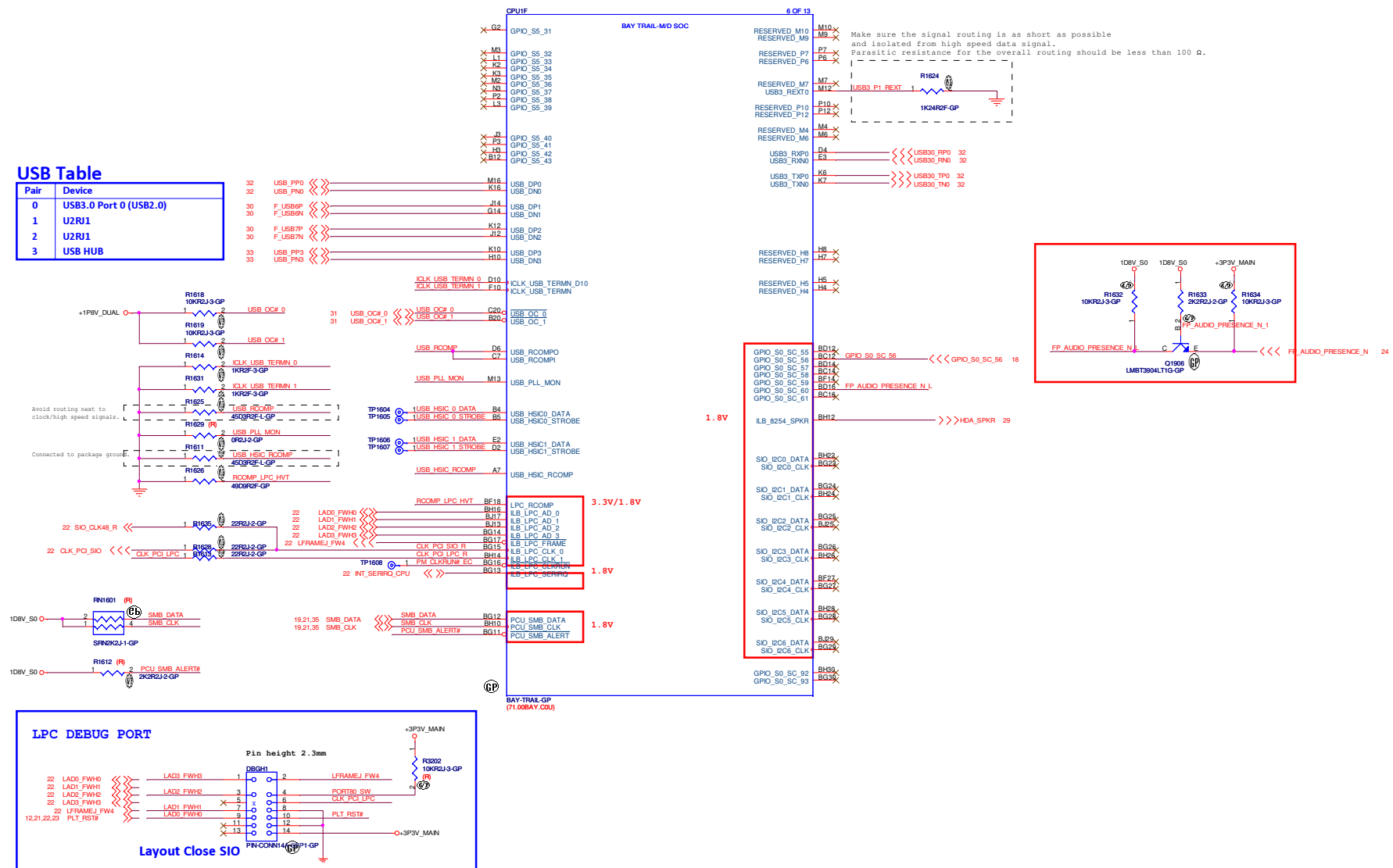
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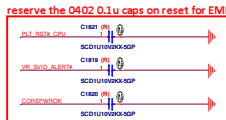
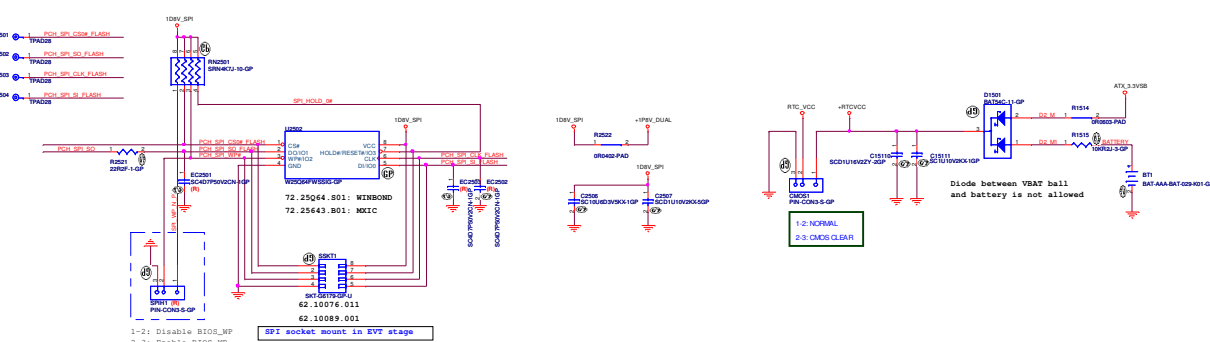
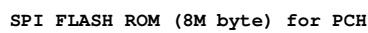
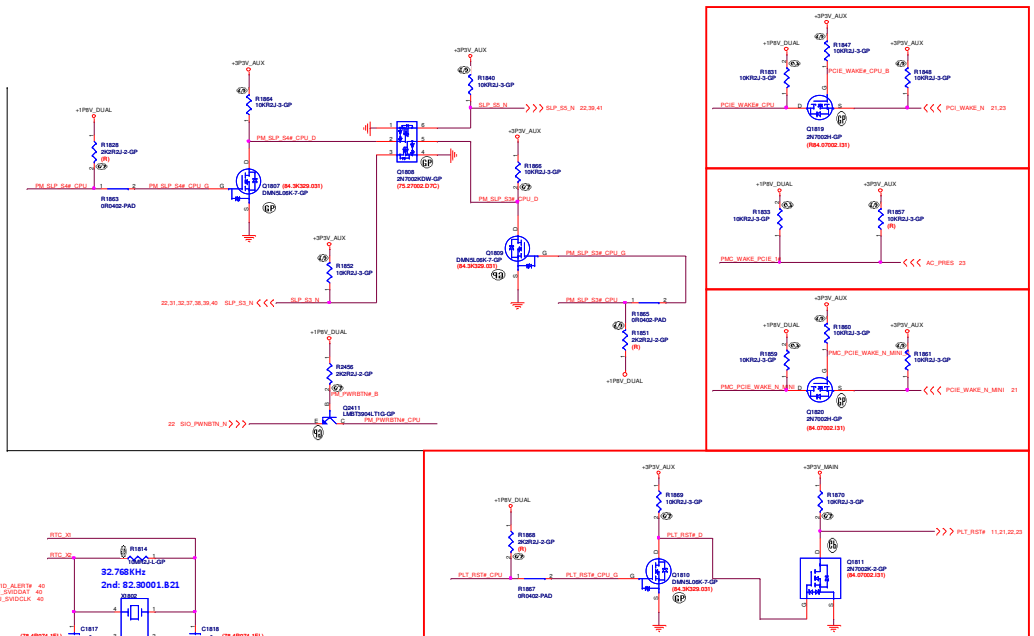
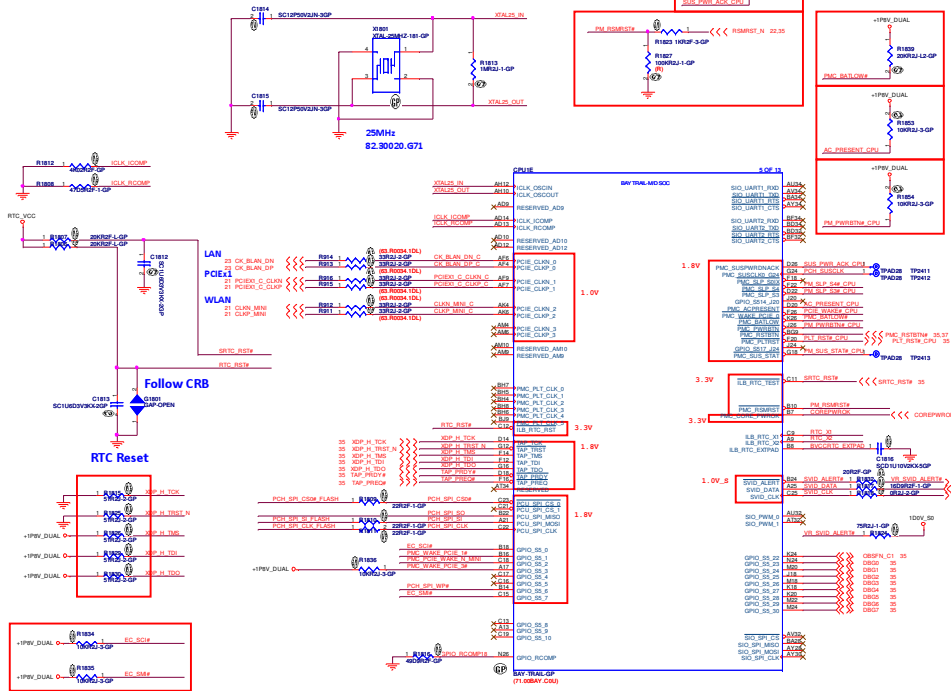
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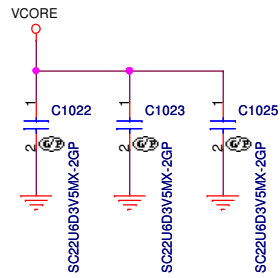


Pair	Device
0	USB3.0 Port 0 (USB2.0)
1	U2RJ1
2	U2RJ1
3	USB HUB

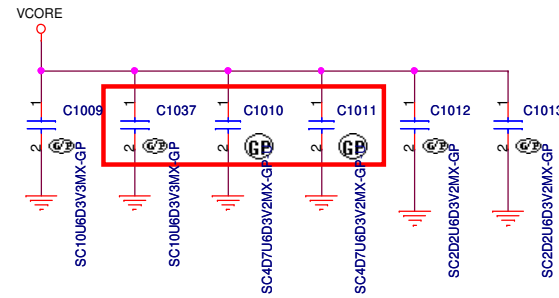
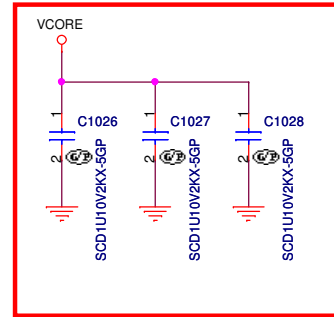




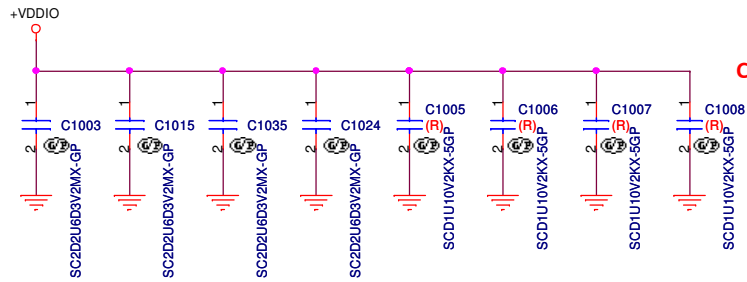
VCORE



reserve the 0402 0.1u caps
on reset for EMI (5/9) .

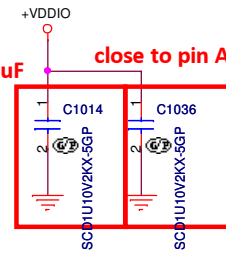


+VDDIO

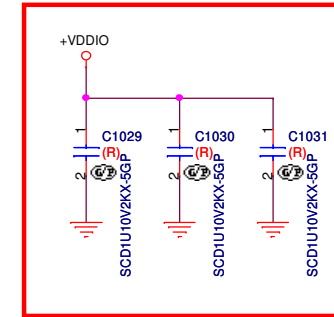


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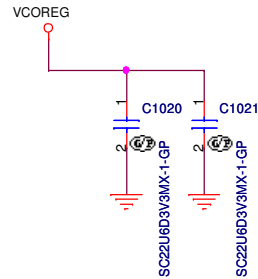
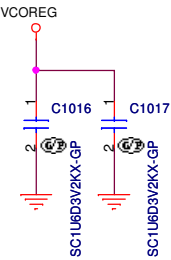
close to pin AD38 & AF38



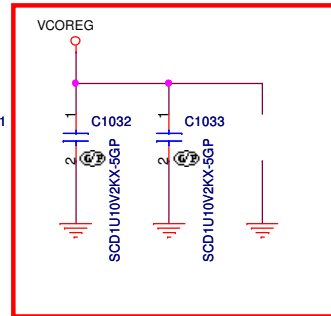
reserve the 0402 0.1u caps
on reset for EMI (5/9) .



VCOREG

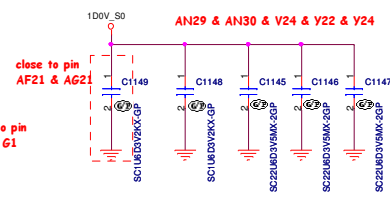
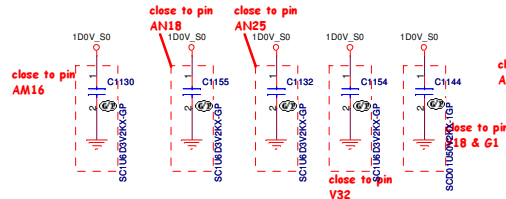
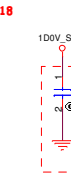
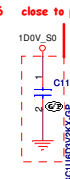
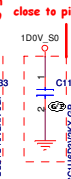
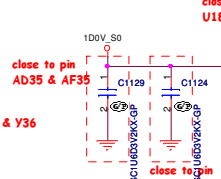
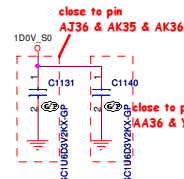
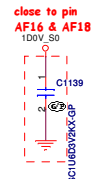
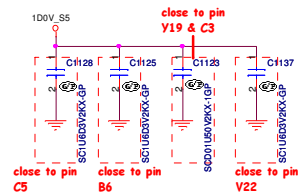
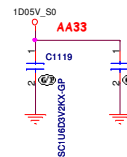
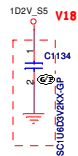
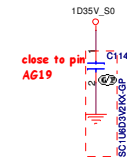
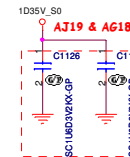
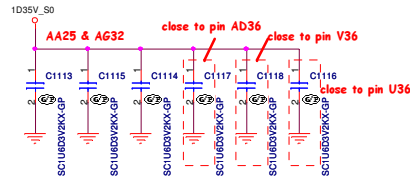
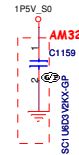
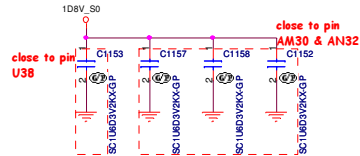
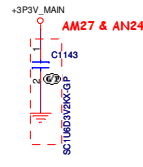
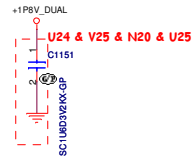
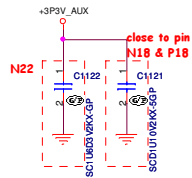


reserve the 0402 0.1u caps
on reset for EMI (5/9) .



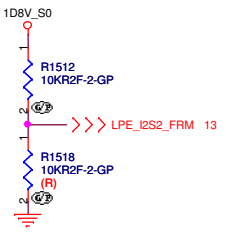
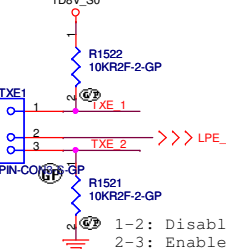
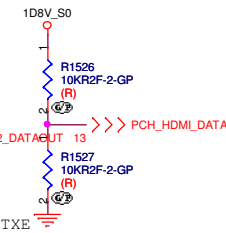
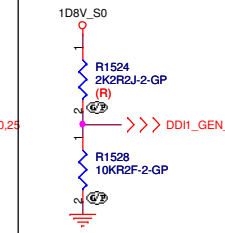
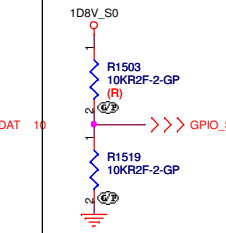
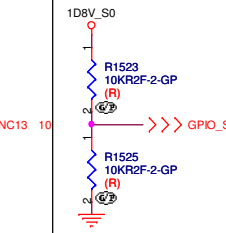
Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title			CPU (Power CAP1)
Size	Document Number	Rev	
Custom	Bay Trail-D	SB	
Date:	Friday, November 15, 2013	Sheet	15 of 43





STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDIO Detect	DDI1 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDIO_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI	Normal Operation	DDIO detected	DDI1 detected	DDI1 detected	
Low	LPC	Override	DDIO not detected	DDI1 not detected	DDI1 not detected	

2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

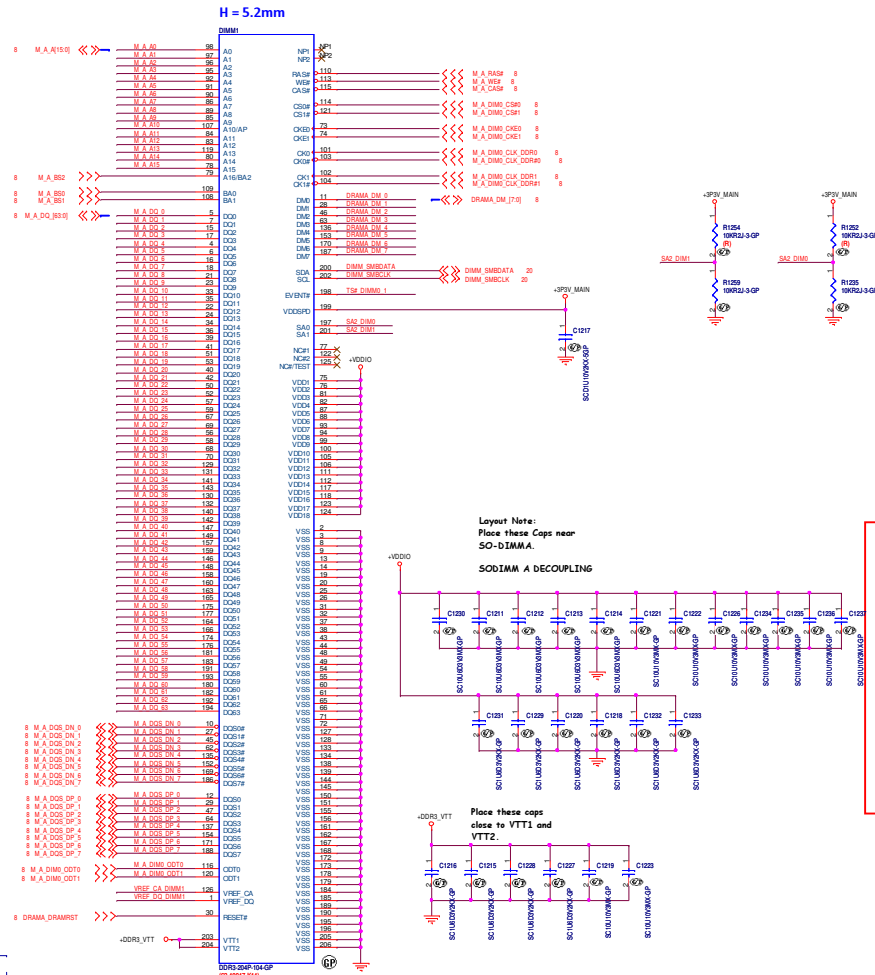
Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDIO_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDIO Detect 0 = DDIO not detected 1 = DDIO detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0x40
SO-DIMMA TS Address is 0x30

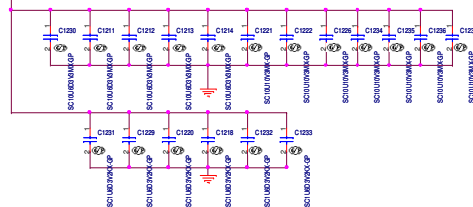
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0x42
SO-DIMMA TS Address is 0x32

Thermal EVENT

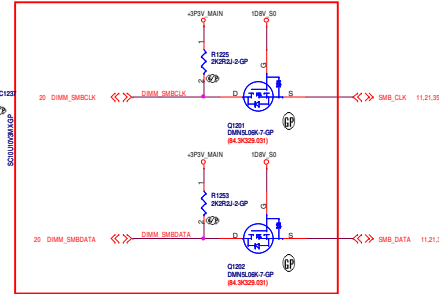
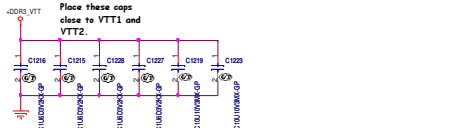


Layout Note:
Place these Cops near
SO-DIMMA.

SODIMM A DECOUPLING



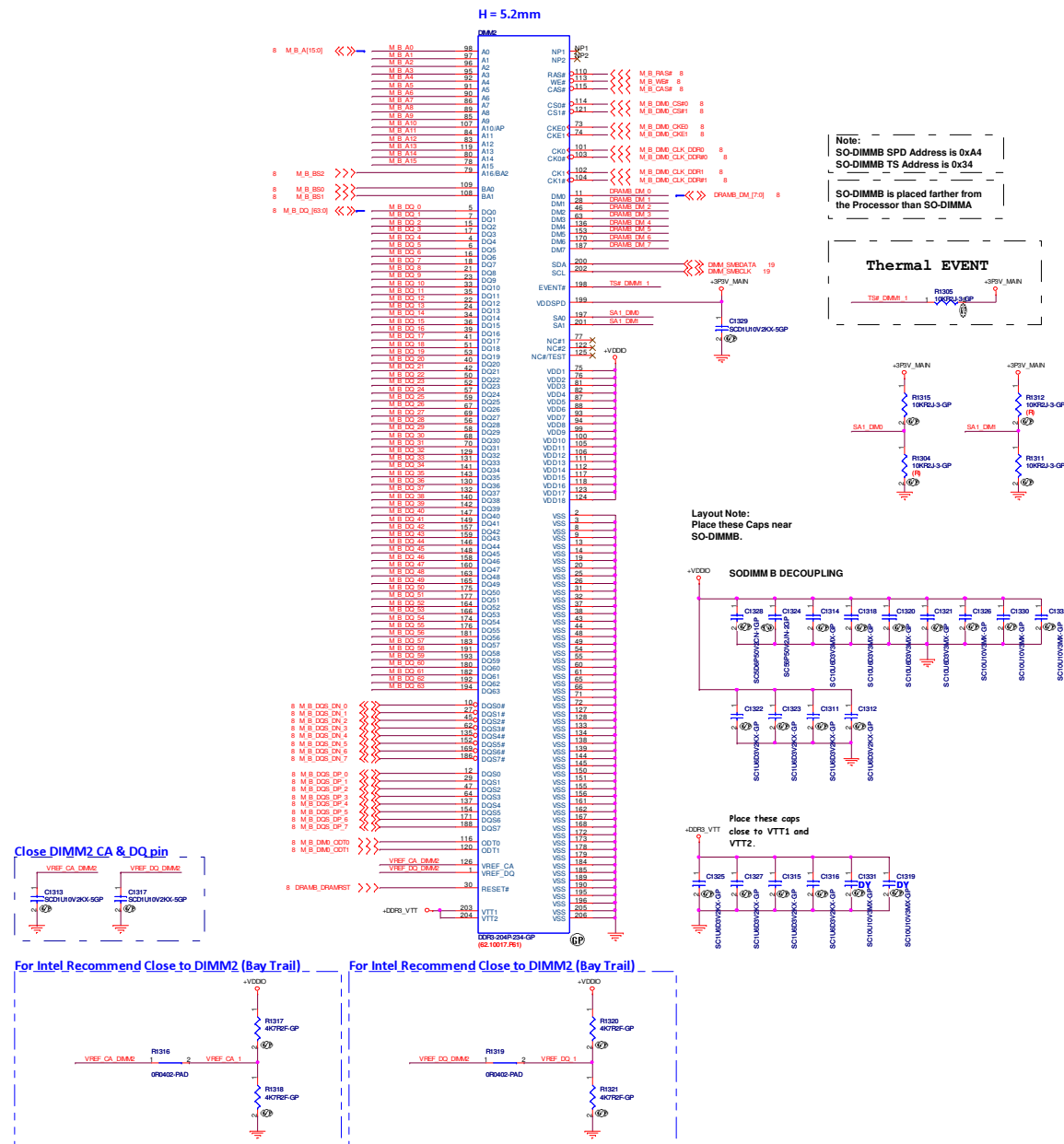
Place these caps
close to VTT1 and
VTT2.

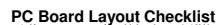
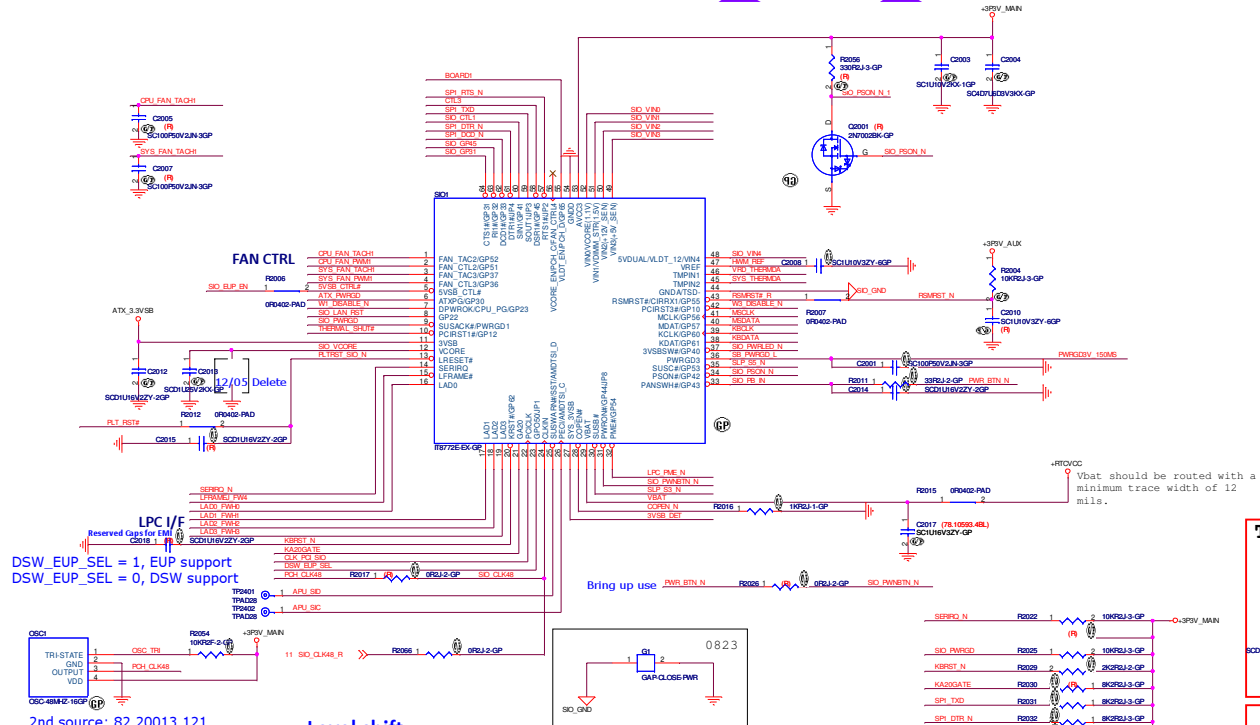
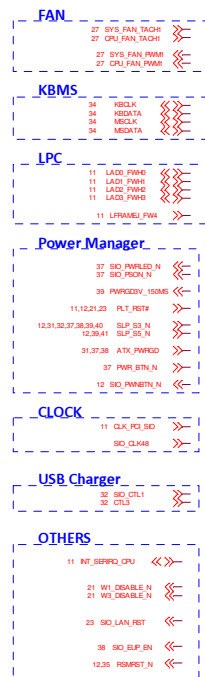


wistron

Wistron Incorporated
21F, 8F, Sec. 1, Hsin Tai Wu Rd
Hsinchu, Taipei Hsinchu

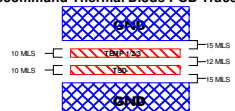
Rev	D0R3-DIMM1	Rev	01
Doc	Document Number	Rev	01
Doc	Buy Trail-0	Rev	01
Rev	01	Rev	01



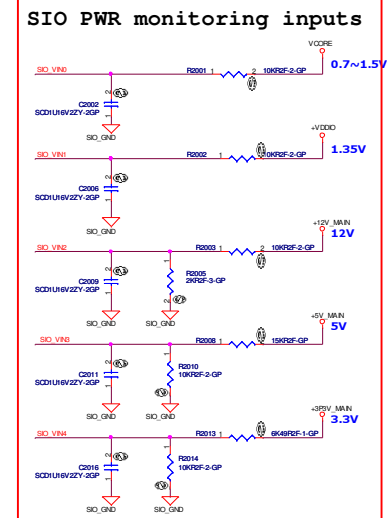
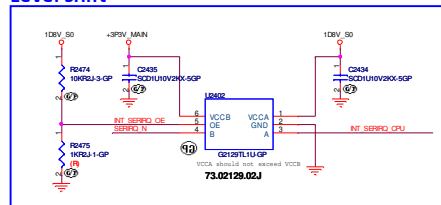


1. Keep traces away from high voltages (+12V bus).
2. Keep traces away from fast data buses and CRTs.
3. Use recommended trace widths and spacing.
4. Place a ground plane under the traces.

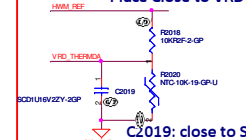
Recommand Thermal Diode PCB Traces



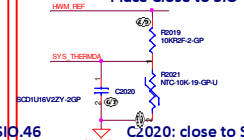
Level shift



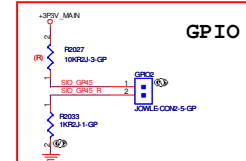
Thermistor (VRD)
Place Close to VRD



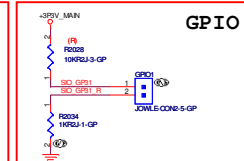
Thermistor (SYS)
Place Close to SIO



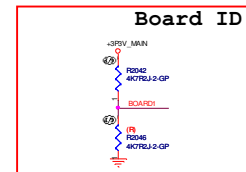
GPIO



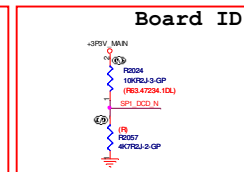
GPIO

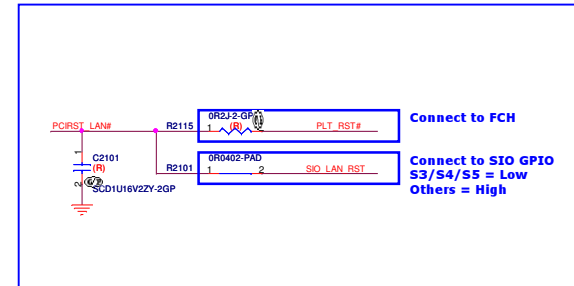
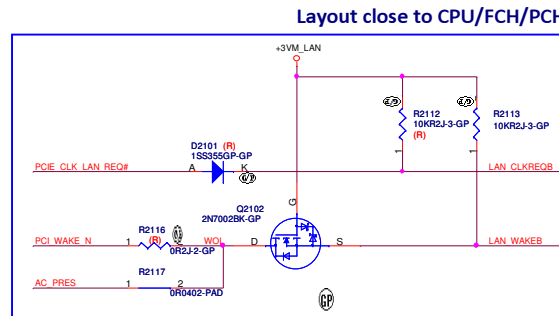
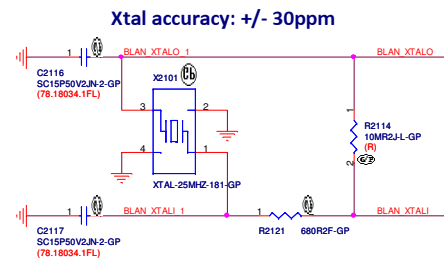
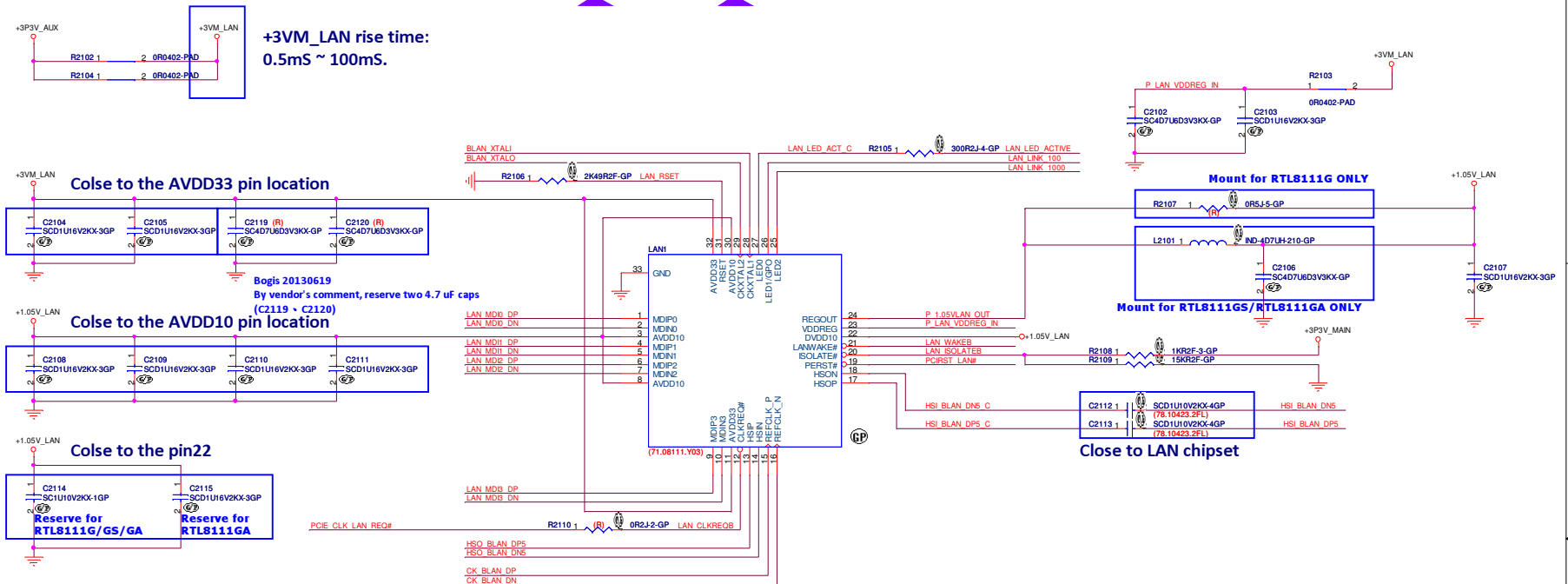


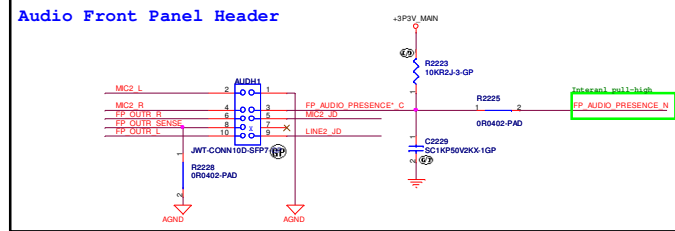
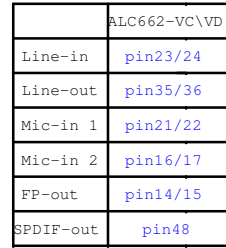
Board ID



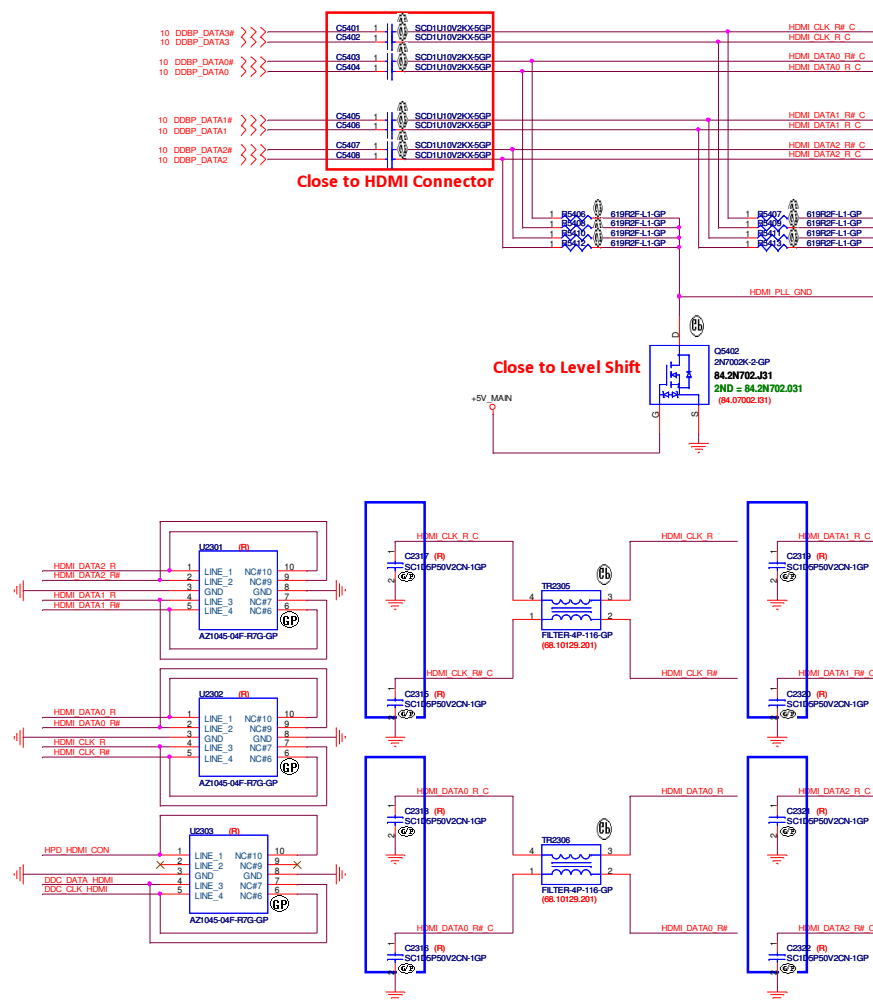
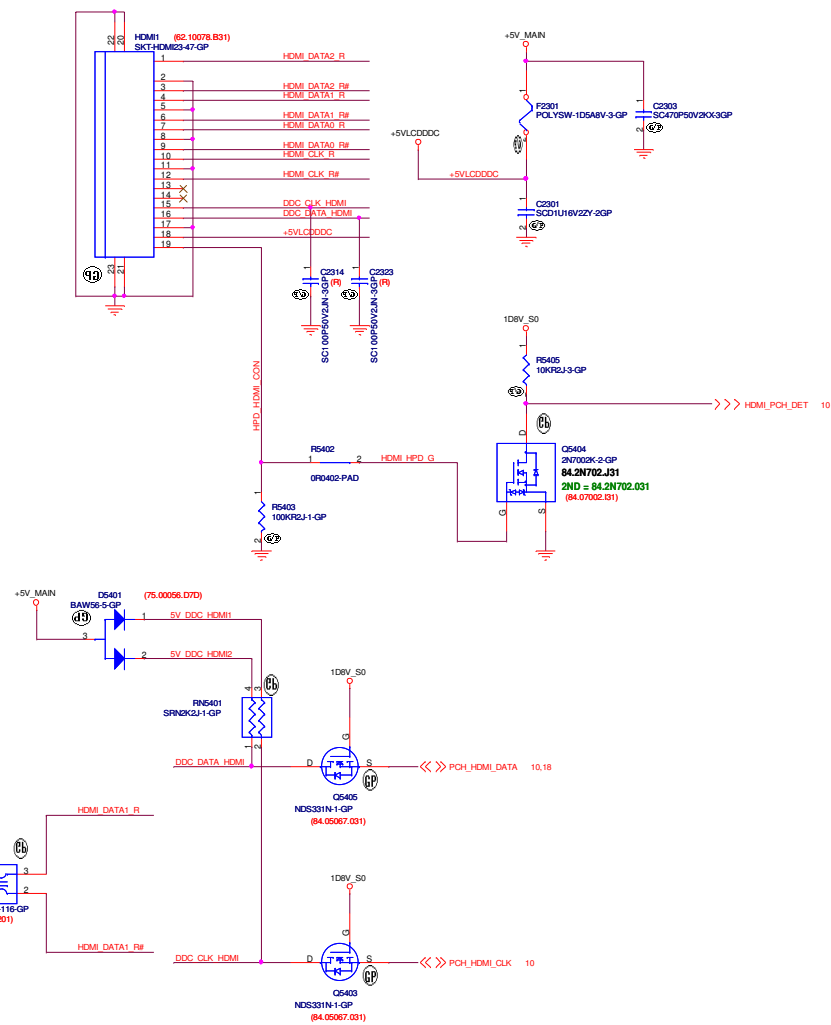
Board ID

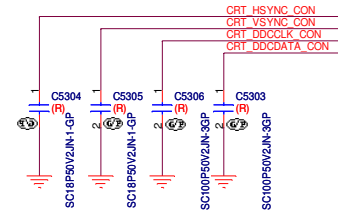
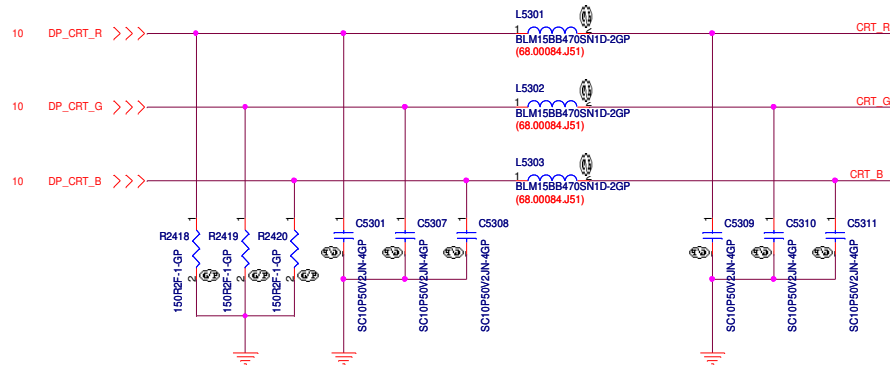
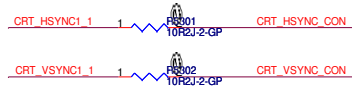
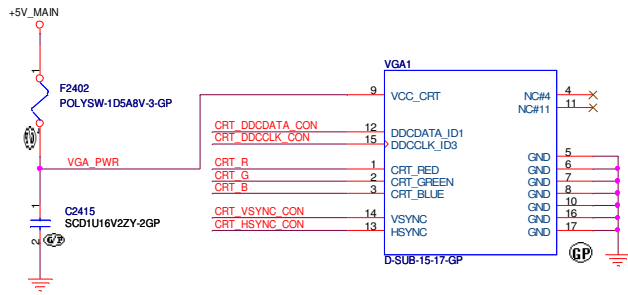




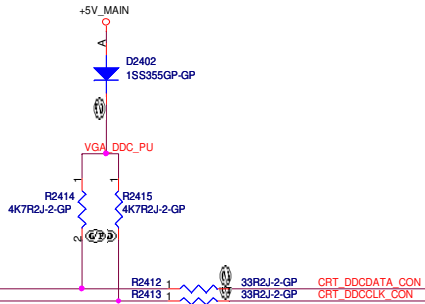
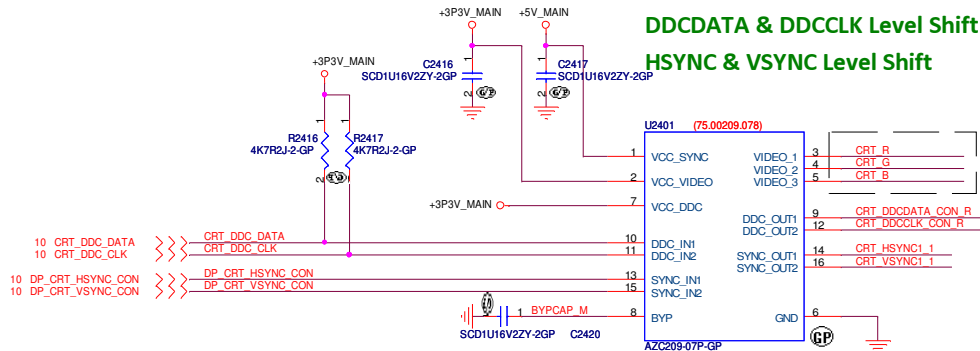


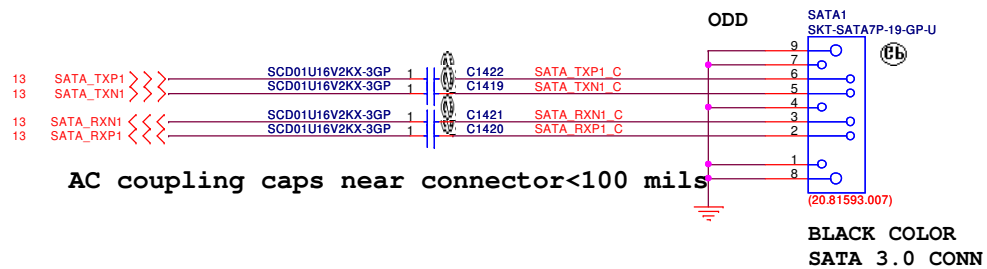
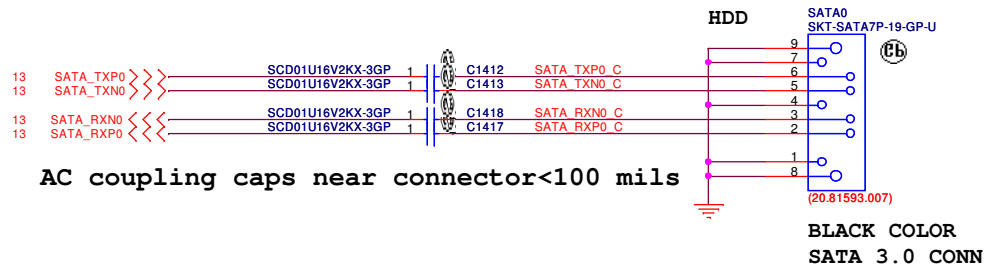
HDMI Level Shifter & CONNECTOR

**HDMI CONN**

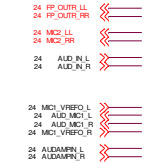


VGA ESD DDCDATA & DDCCLK Level Shift HSYNC & VSYNC Level Shift

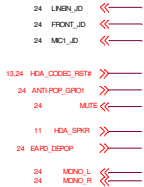




AUDIO PORT



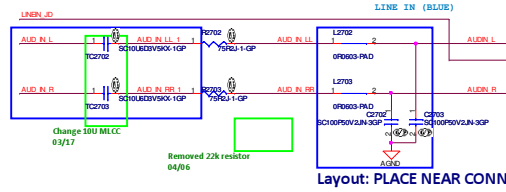
MISC



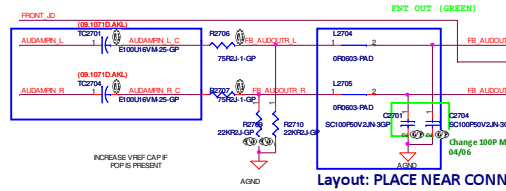
The cap need to close codec on layout.

The cap need to close codec on layout.

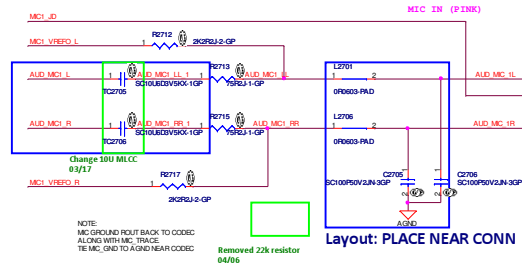
The cap need to close codec on layout.



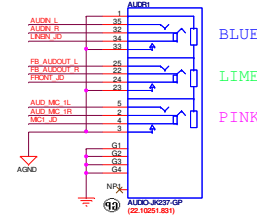
Layout: PLACE NEAR CONN



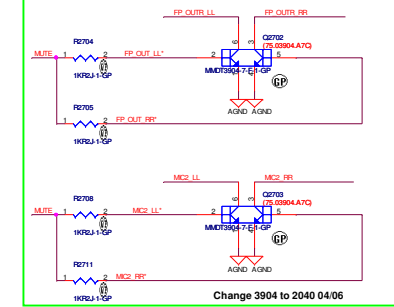
Layout: PLACE NEAR CONN



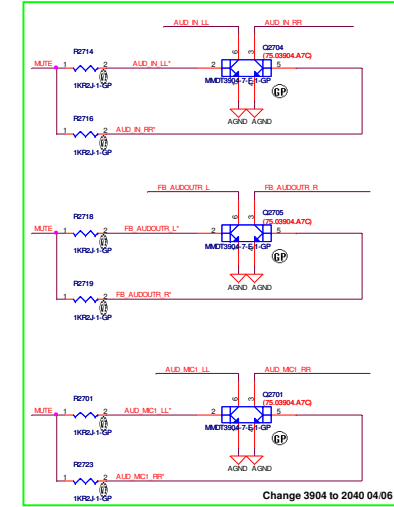
Layout: PLACE NEAR CONN



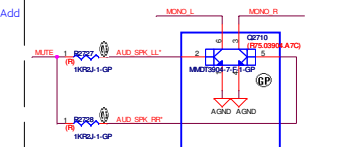
Front Audio Port De-Pop Circuit



Rear Audio Port De-Pop Circuit



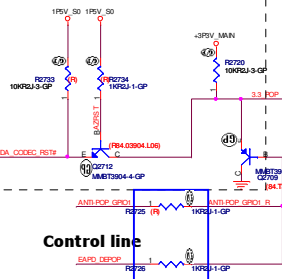
11/14 Add



11/21 Change to HN1C03FU

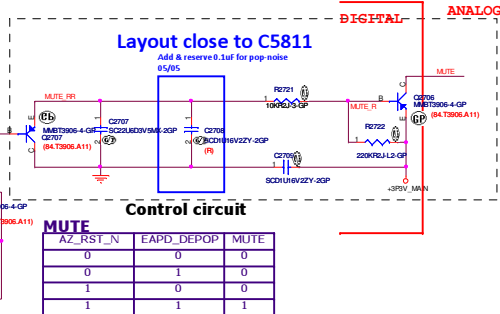
POP Circuit ReaZ

Control by software driver and CODEC GPIO.
GPIO driving low etc:
1).Initial state
2).Suspend to S1
3).Resume from S1.

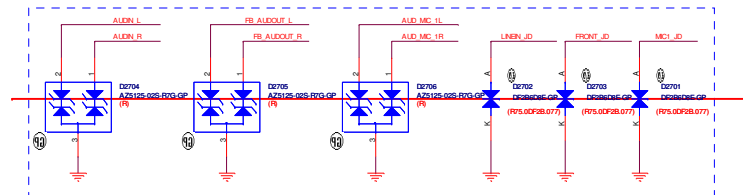
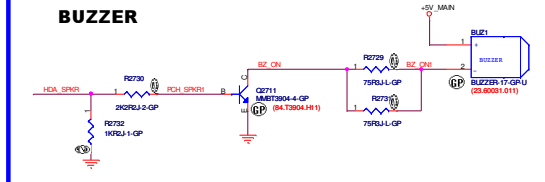


Control line

Unmount R2725, Mount R2726



BUZZER



USB

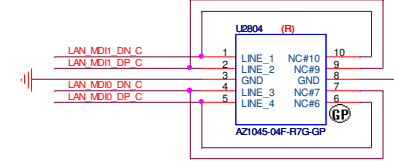
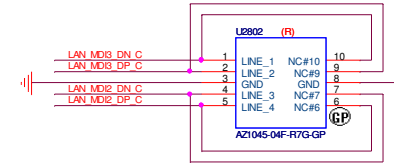
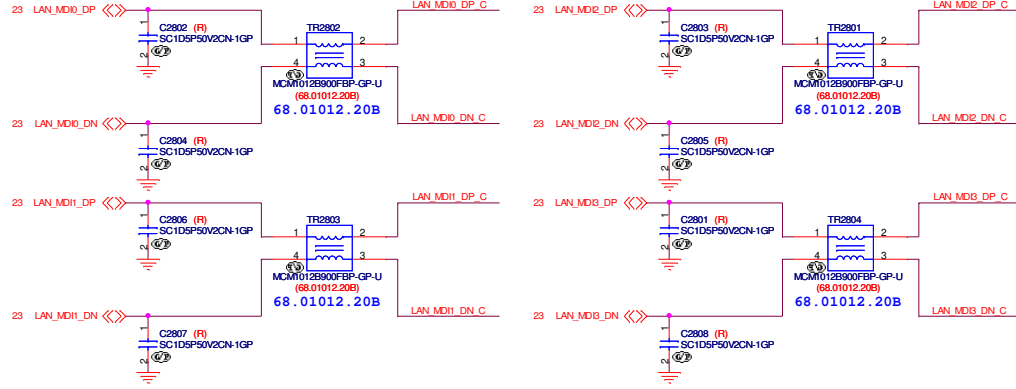
11 F_USB6N <<<<
11 F_USB6P <<<<
11 F_USB7N <<<<
11 F_USB7P <<<<

LAN

23 LAN_LINK_100 <<<<
23 LAN_LINK_1000 <<<<
23,37 LAN_LED_ACTIVE <<<<

23 LAN_MDIO_DP <<<<
23 LAN_MDIO_DN <<<<
23 LAN_MDII_DP <<<<
23 LAN_MDII_DN <<<<
23 LAN_MDIE_DP <<<<
23 LAN_MDIE_DN <<<<
23 LAN_MDIS_DP <<<<
23 LAN_MDIS_DN <<<<

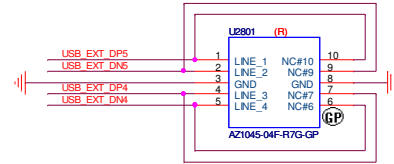
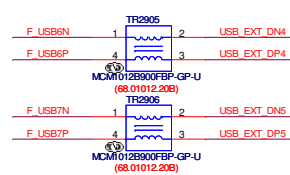
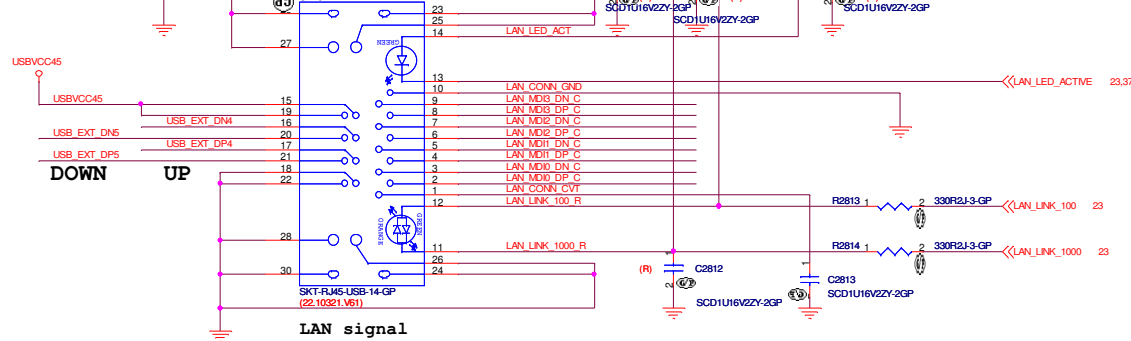
LAN common choke



J5901 : 22.10321.V31 change 22.10321.V61
L:GREEN/ORANGE R:GREEN -> L:GREEN R:GREEN/ORANGE
04/28

	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

USB+RJ45



From Hub IC to USB2F1

33 F_USB5P
33 F_USB5N

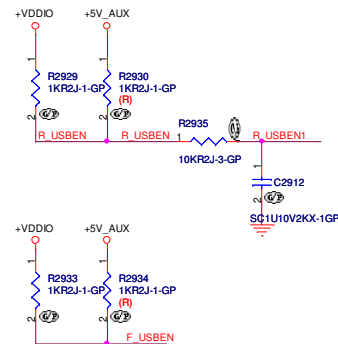
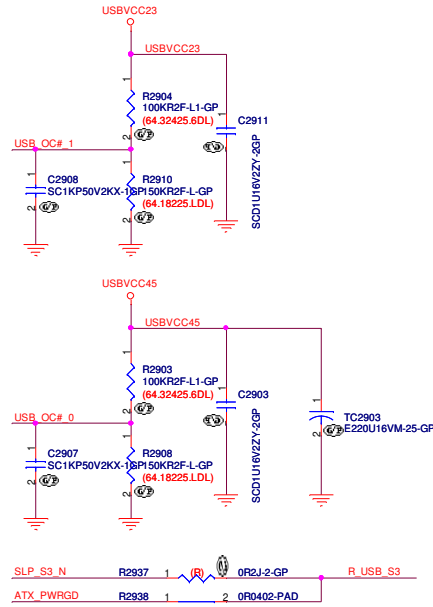
From Hub IC to USB2F2

33 F_USB2P
33 F_USB2N
33 F_USB3P
33 F_USB3N

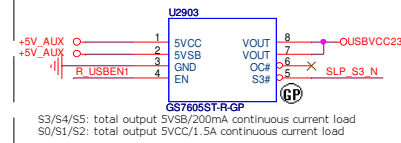
11 USB_OC#_0
11 USB_OC#_1

12,22,32,37,38,39,40 SLP_S3_N

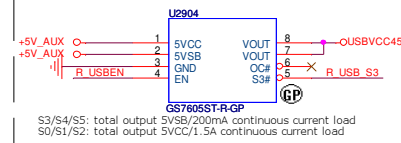
22,37,38 ATX_PWRGD



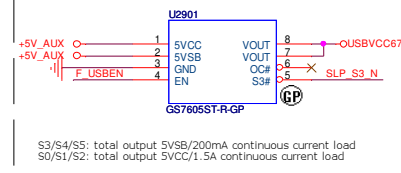
For USB2F2



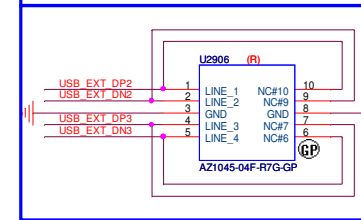
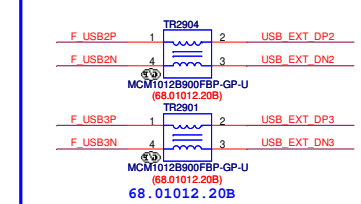
For U2RJ1



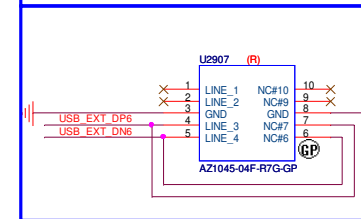
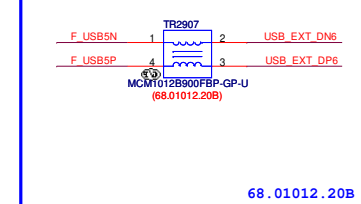
For USB2F1



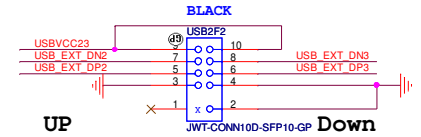
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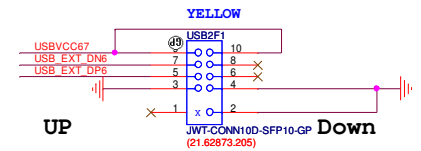
For USB2F1



FP Header USB2.0



FP Header USB2.0



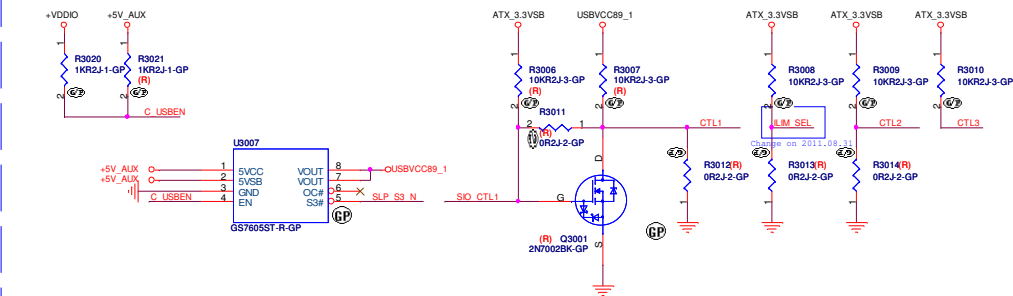
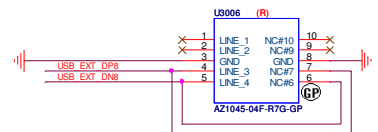
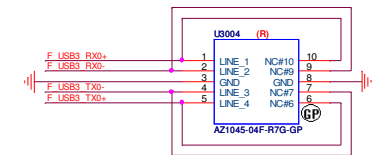
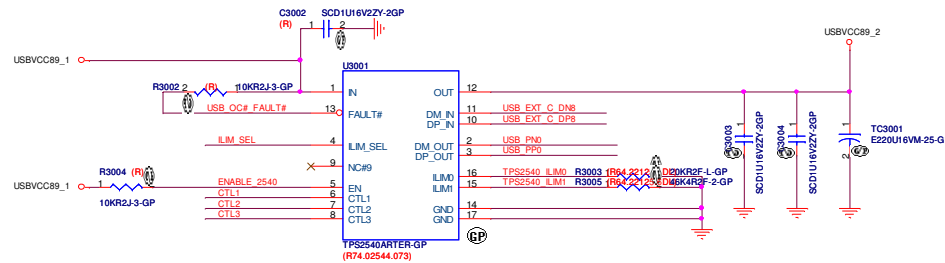
wistron

Wistron Incorporated
21F, 88, Sec.1, Hei Tai Wu Rd
Hsichih, Taipei Hsien

Title	USB2.0	
Size	Document Number	Rev
Custom	Bay Trail-D	SB
Date:	Friday, November 15, 2013	Sheet 31 of 43

Truth Table for TPS2540A/TPS2543/TPS2546

ACPI Control	CTL1	CTL2	CTL3	ILIM_SEL	PWR	Control Mode
S0	1	1	1	1	+5V_MAIN	CDP
S1	1	1	1	1	+5V_MAIN	CDP
S3	0	1	0	1	ATX_5VSB	SDP
S4	0	1	1	1	ATX_5VSB	DCP
S5	0	1	1	1	ATX_5VSB	DCP
S5_EuP	0	1	1	1	ATX_5VSB	DCP
G3->S5	0	1	1	1	ATX_5VSB	DCP



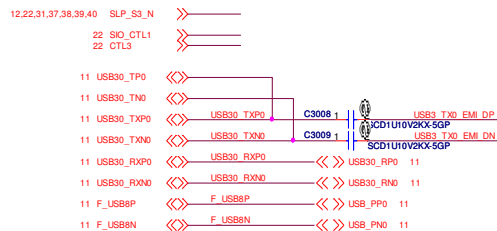
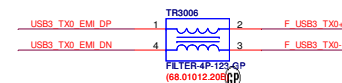
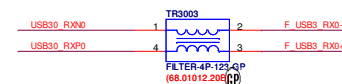
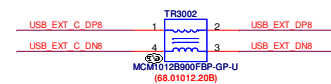
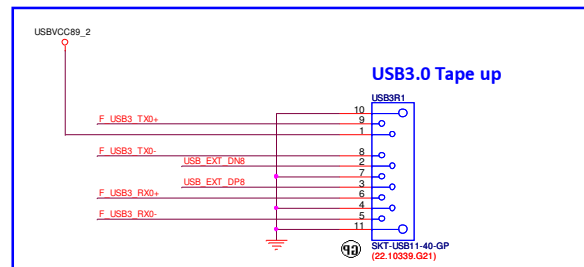
S3/S4/S5: total output 5VSB/200mA continuous current load
S0/S1/S2: total output 5VCC/1.5A continuous current load

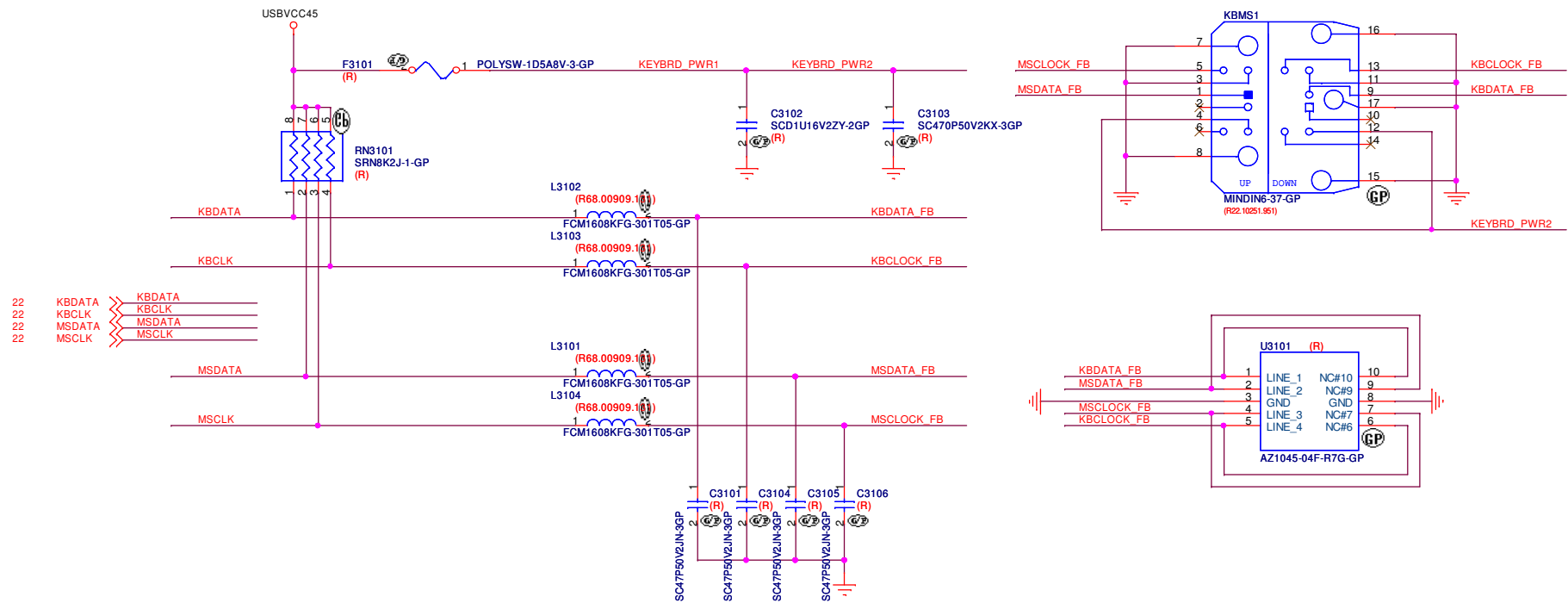
Reserve for no USB charger support

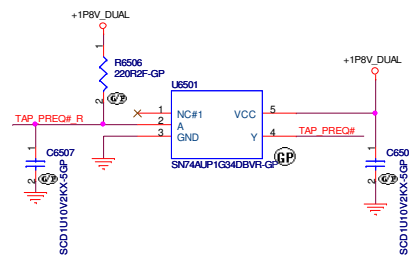
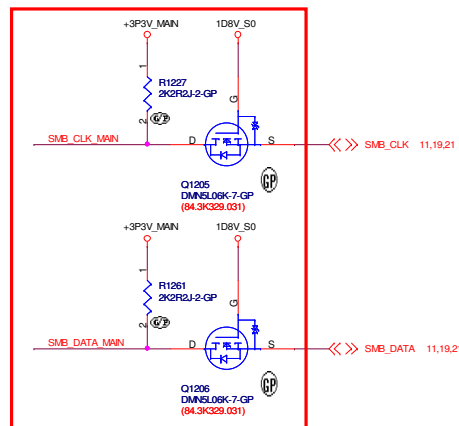
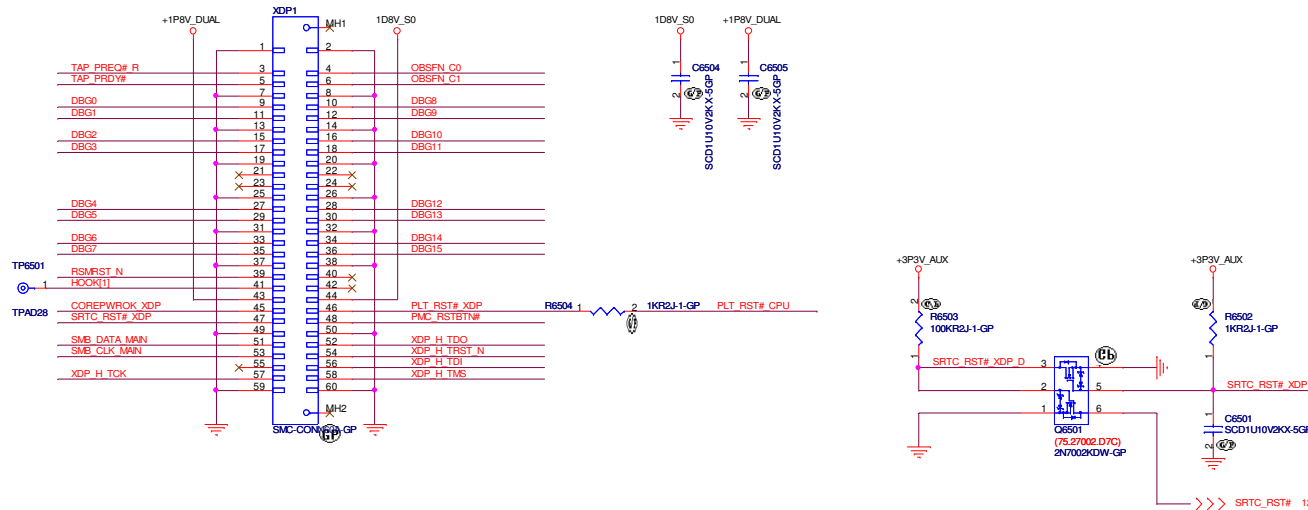
USB_PND	R3015	1	2	0R0402-PAD	USB EXT C DN8
USB_PP0	R3016	1	2	0R0402-PAD	USB EXT C DP8
	R3017	1	2	0R0603-PAD	
USBVCC89_1	R3018	1	2	0R0603-PAD	USBVCC89_2



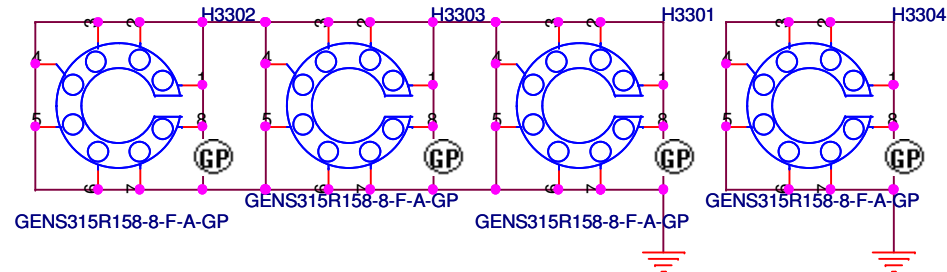
USB 3.0 Rear Port







Scre Hole (PCB New type MOUNTING HOLES)



LABEL



LAN ID :
F80F4105EB9A

LBL1 LABEL
W70*H8
(45.41107.011)



LAN ID :
F80F4105EB9A

LBL2 LABEL
W35*H15
(R45.41101.011)



LAN ID :
F80F4105EB9A

LBL3 LABEL
(R)

+12V_MAIN



C3301
SC1KP50V2KX-1GP

+12V_MAIN



C3302
SC1KP50V2KX-1GP

Battery Symbol



BAT1
BATTERY CR2032
(23.20068.001)

23.20068.001 KTS BBB CR2032 BX

23.20023.311 MITSUBISHI CR2032 MITSUBISHI

23.22063.001 JHT CR2032 JHT

wistron

Wistron Incorporated

21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title

Screw Hole

Size
A

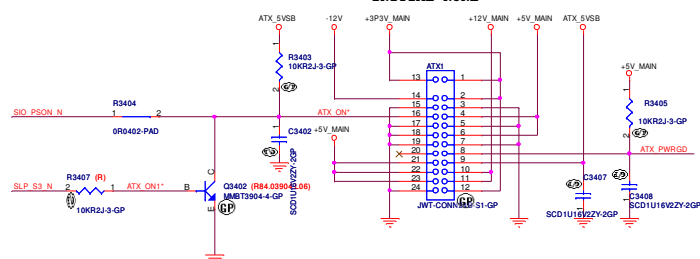
Document Number
Bay Trail-D

Rev
SB

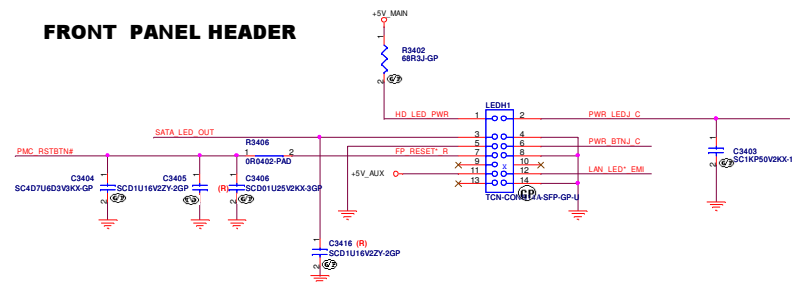
Date: Friday, November 15, 2013

Sheet 36 of 43

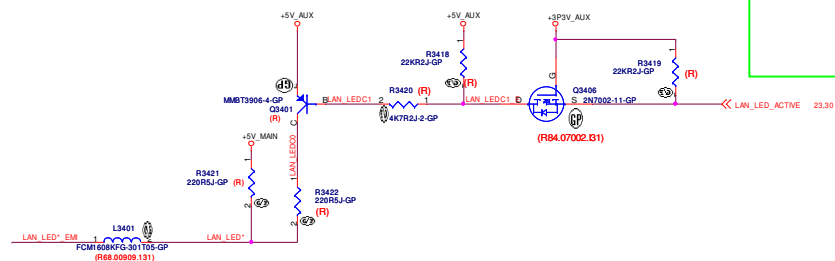
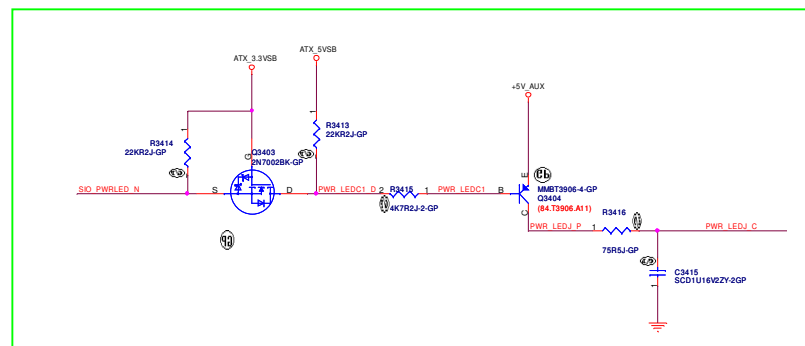
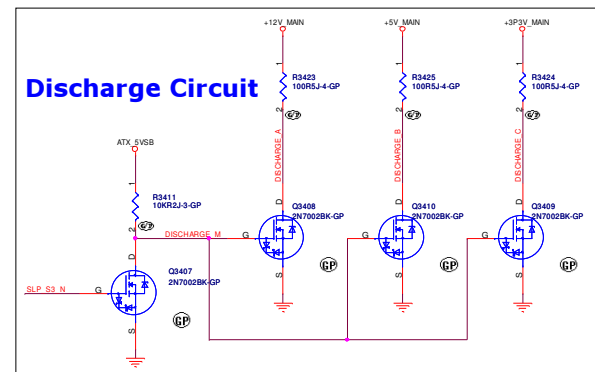
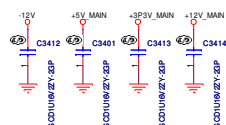
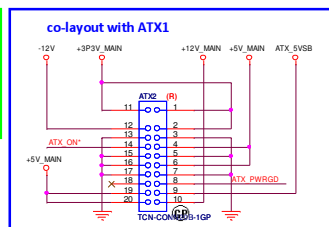
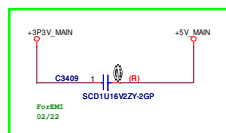
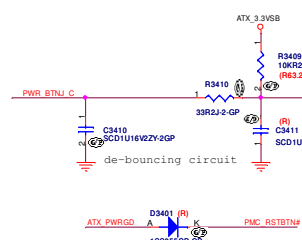
INITIAL NONE



Discharge Circuit

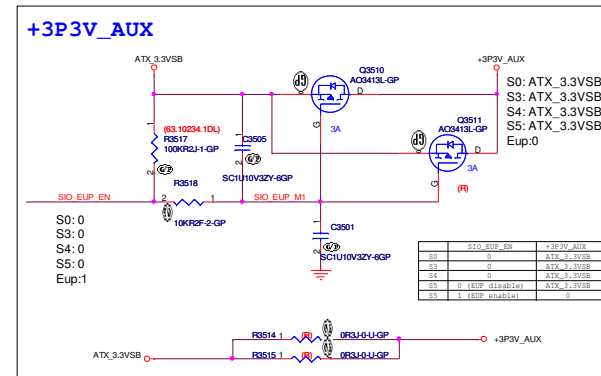
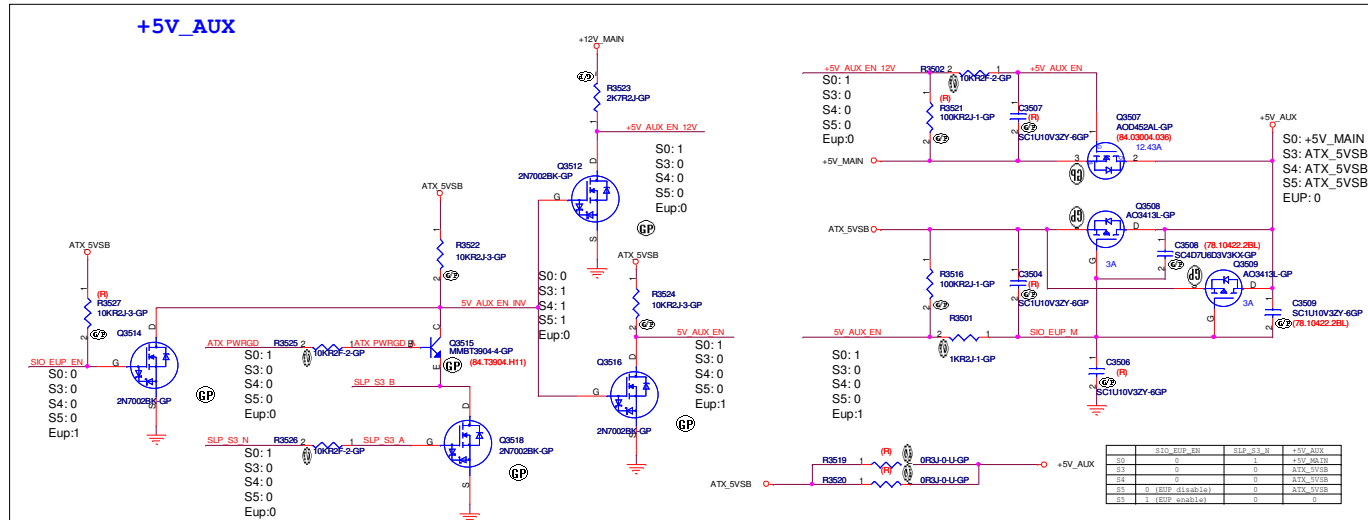


co-layout with ATX1

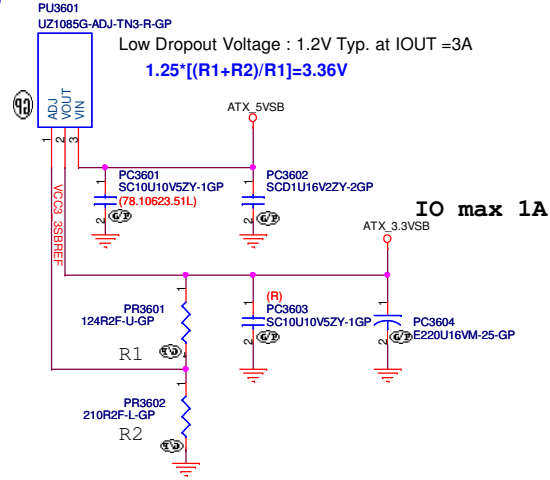


12,22,31,32,37,39,40 SIO_EUP_EN
22,31,37 SLP_S3_N
22,31,37 ATX_PWRGD

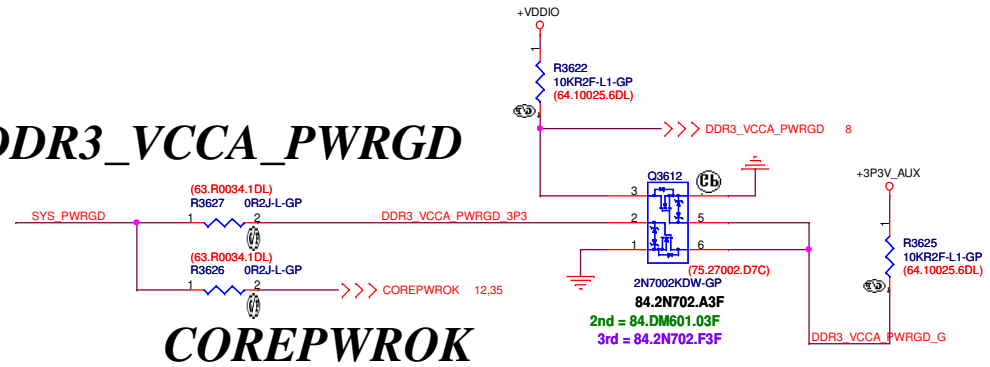
Dual Power Control GROUP A POWER(S5_Eup)



ATX_3.3VSB



DDR3_VCCA_PWRGD



COREPWROK

DDR3_DRAM_PWROK

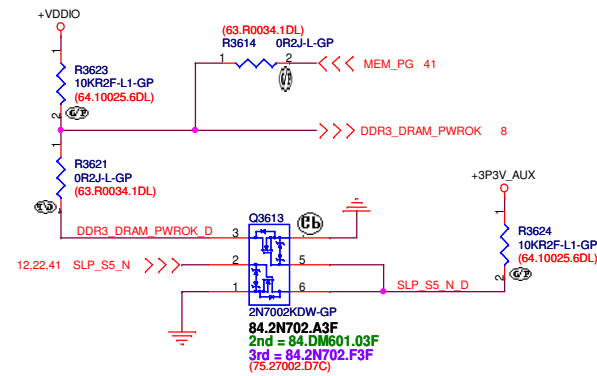
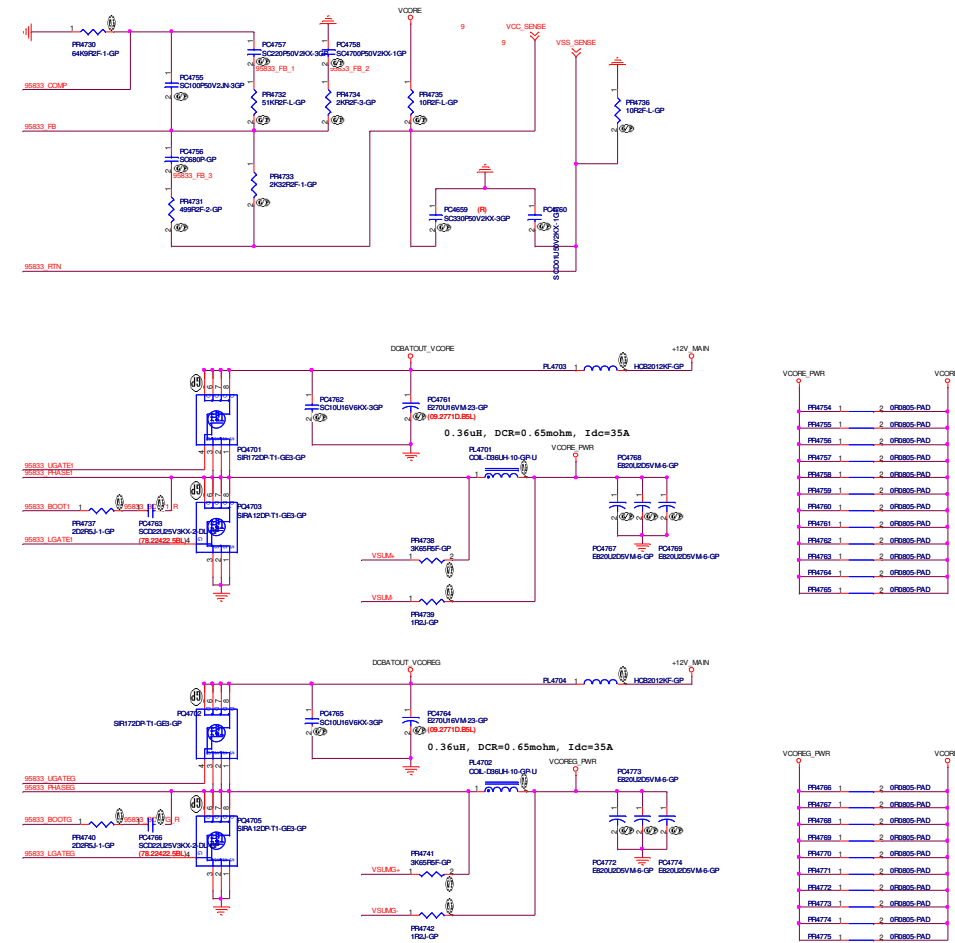
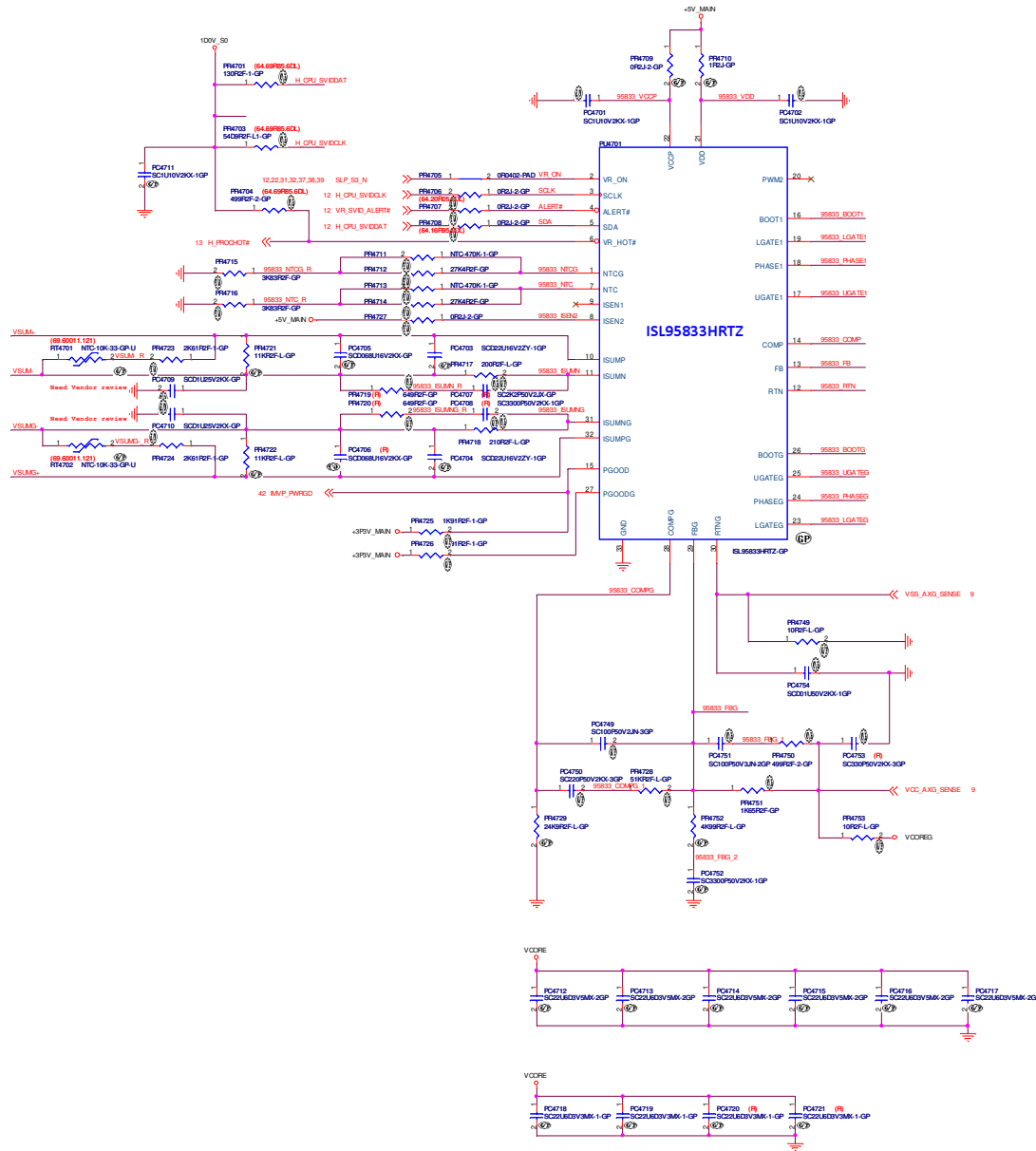
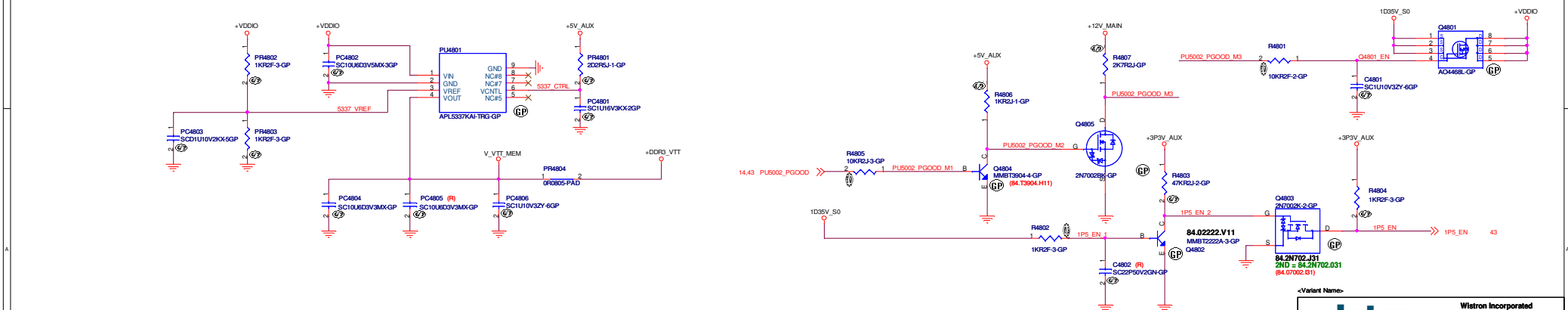
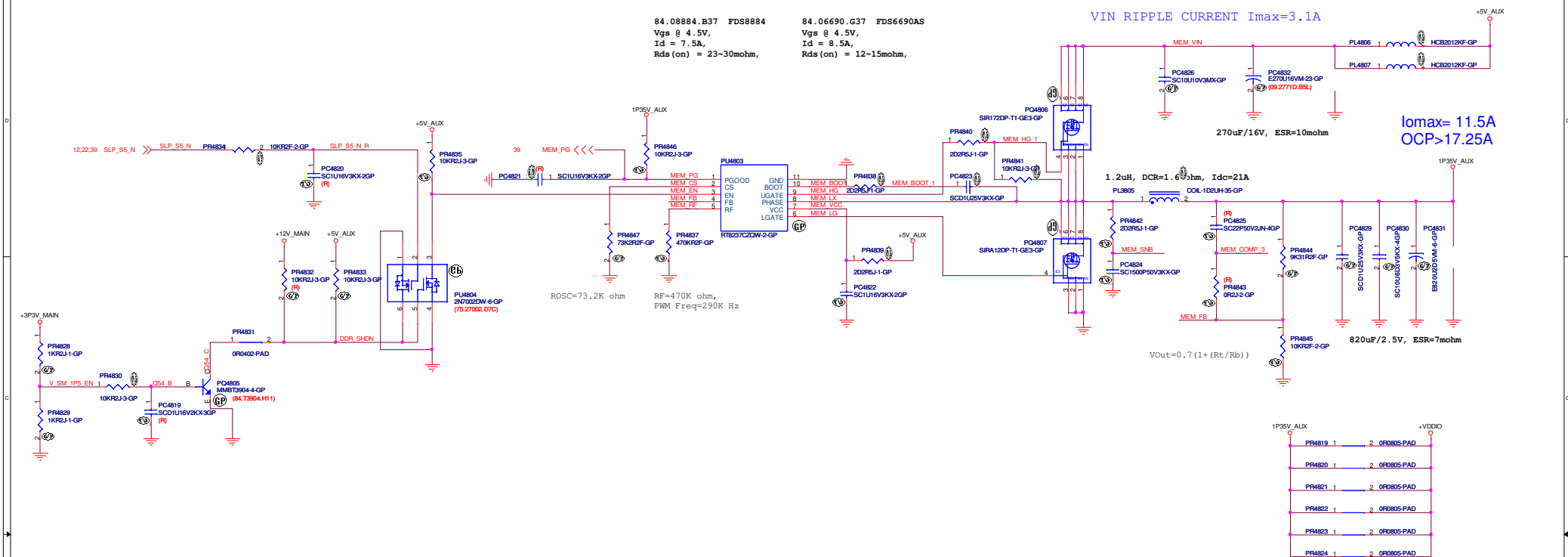
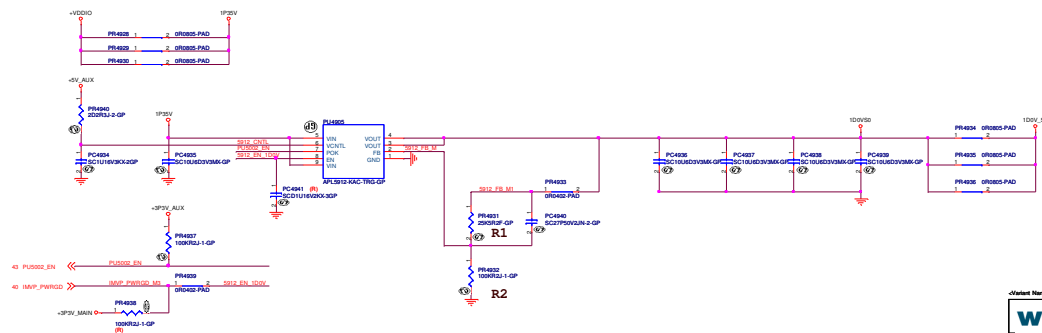
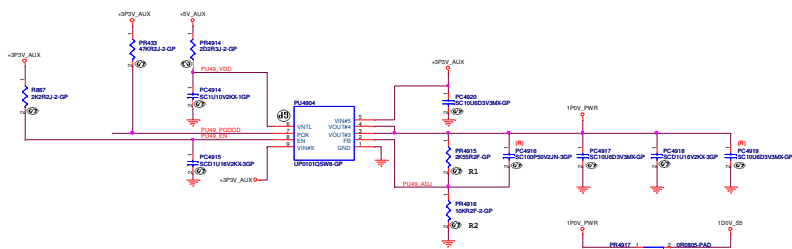
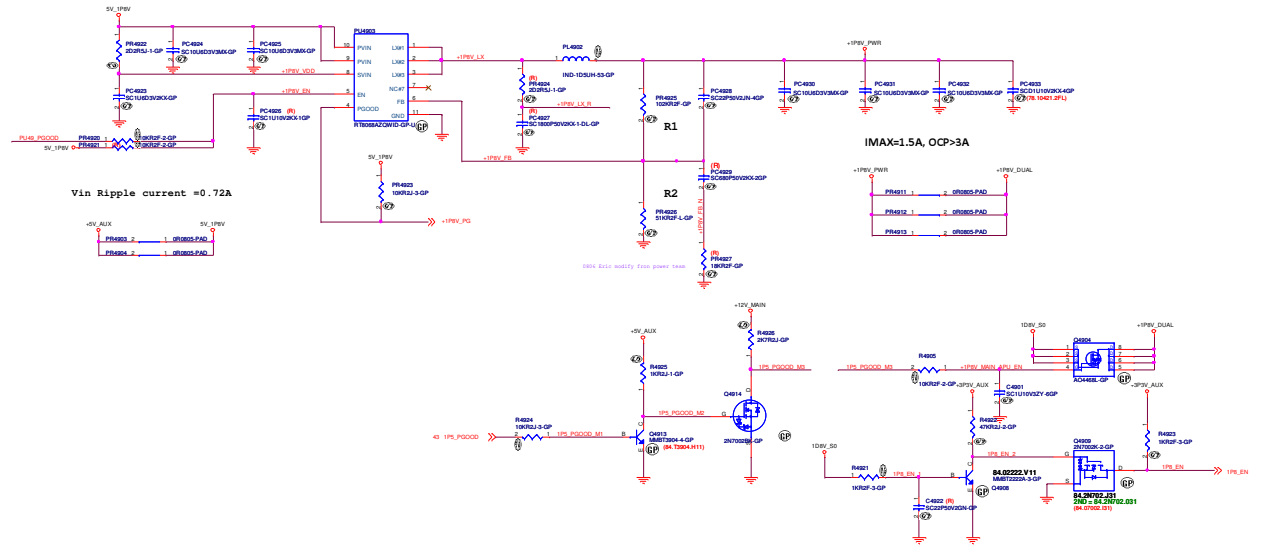


Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion	100		ms	
T3					





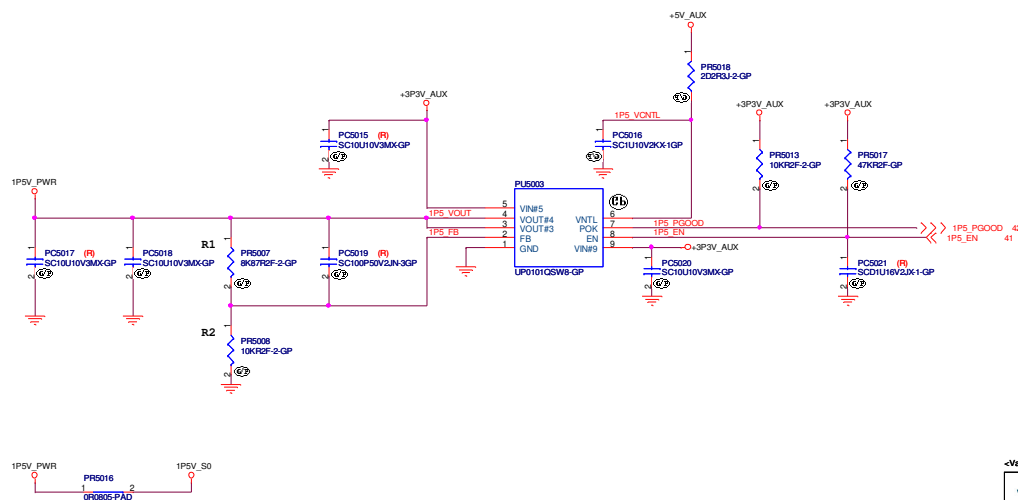
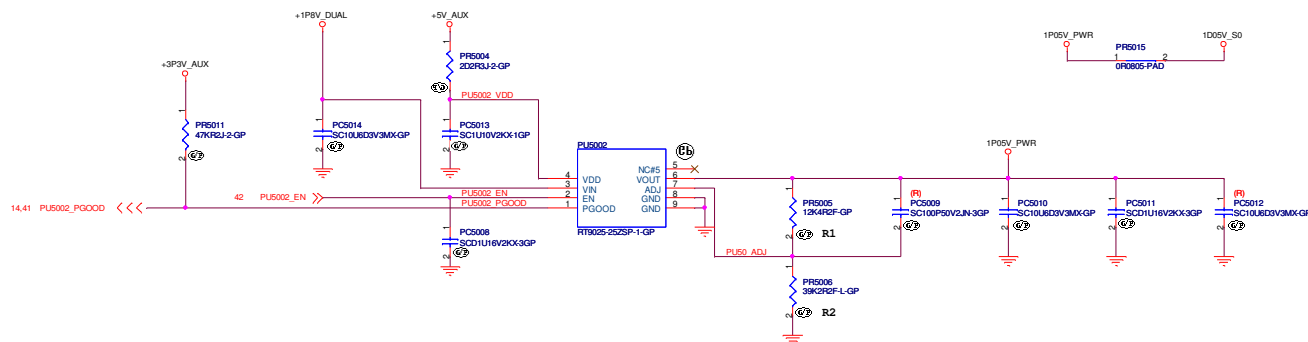
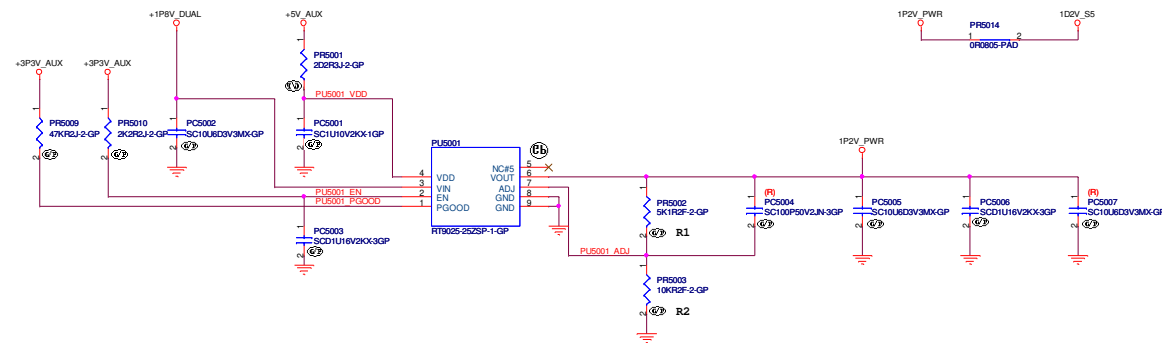


Variant Name:

Wistron Incorporated
21F, 8B, Vain Tai Hu Rd
Hsinchu, Taiwan

DC to DC 100V 100V

Document Number
Wistron 100V 100V
Date: 2010-01-01
Version: 1.0



<Variant Name>

wlstron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Heichih, Taipei	
Title DC to DC_1D2V_1D05V_1D5V			
Size	Document Number		Rev
	Customer Trail-D		SB
Date:	Friday, November 15, 2013	Sheet	43 of 43