

MODEL NAME : *VAZA0*PCB NO : *LA-9262P ( DAB0000I010 )*

BOM P/N :

# Dell/Compal Confidential

## Schematic Document

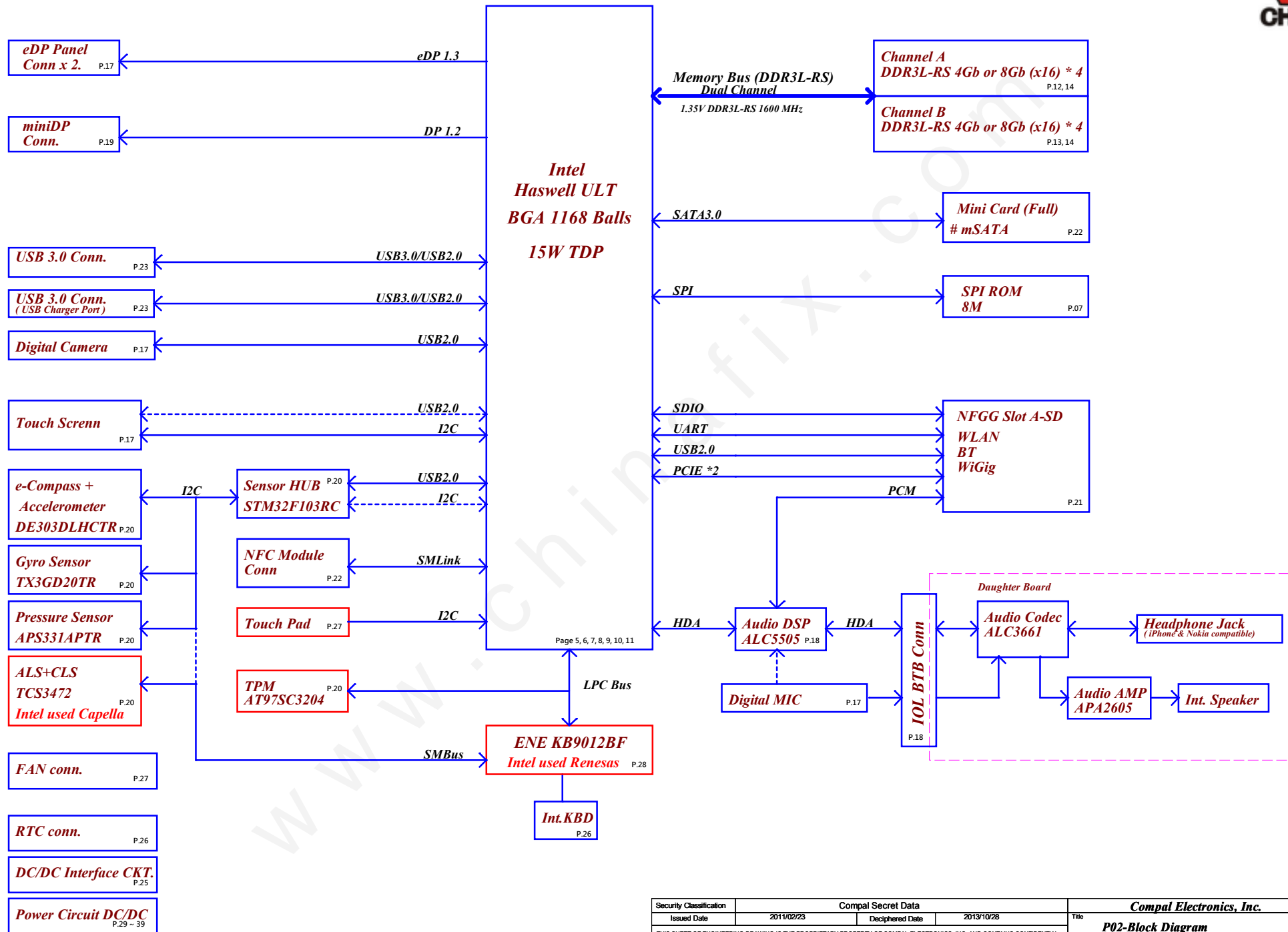
### Murcielgo MLK (Haswell ULT)

2013-04-19

Rev: 1.0

Highlight the short pad for 0 ohm

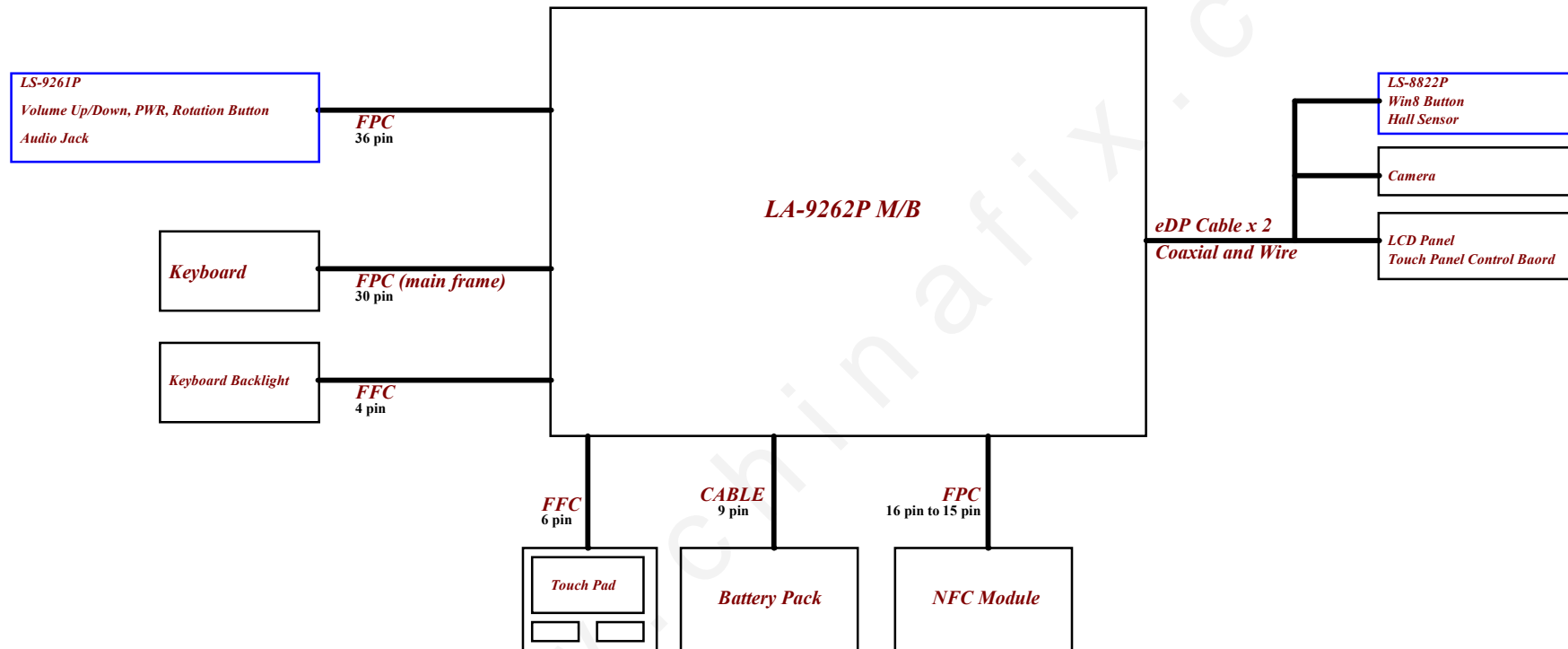
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LA-9262P					



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Project Code : VAZA0

File Name : LA-9262P



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### BOARD ID Table

Board ID	Rb	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	EC AD3
0	0				
1	12K +/- 1%				
2	15K +/- 1%				
3	20K +/- 1%				
4	27K +/- 1%				
5	33K +/- 1%				
6	43K +/- 1%				
7	56K +/- 1%				
8	75K +/- 1%				
9	100K +/- 1%				
10	130K +/- 1%				
11	160K +/- 1%				
12	200K +/- 1%				
13	240K +/- 1%				
14	270K +/- 1%				
15	330K +/- 1%				
16	430K +/- 1%				
17	560K +/- 1%				
18	750K +/- 1%				
19	NC				

Board ID	PCB Revision
0	CS 0.1
1	CS 0.2
2	CS 0.3
3	CS 0.4
4	CS 0.5
5	CS 1.0
6	
7	
8	
9	
10	Non-CS 0.1
11	Non-CS 0.2
12	Non-CS 0.3
13	Non-CS 0.4
14	Non-CS 1.0
15	
16	
17	
18	
19	

PCH USB Port Mapping	USB PORT#	DESTINATION
	0	External USB3
	1	External USB3
	2	NGFF CARD WLAN
	3	Touch Panel
	4	Camera
	5	Sensors HUB
	6	
	7	

<b>PCH DDI Port Mapping</b>	<b>DDI PORT#</b>	<b>DESTINATION</b>
	<b>B</b>	<b>mini-DP</b>
	<b>C</b>	

### SMBUS Control Table

	SOURCE	NGFF	BATT	Charger	NFC	XDP	DDR3 SPD	ALS	Touch Pad
EC_SMB_CK1 EC_SMB_DA1	KB9012		V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012							V	
PCH_SML0CLK PCH_SML0DATA	PCH	V			V				
PCH_SML1CLK PCH_SML1DATA	PCH								
MEM_SMBCLK MEM_SMBDATA	PCH					V	V		V

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0		CLKOUT_LPC_0	EC LPC
	CLKOUT_PCIE1		CLKOUT_LPC_1	TPM
	CLKOUT_PCIE2			
	CLKOUT_PCIE3	NGFF CARD WLAN		
	CLKOUT_PCIE4			
	CLKOUT_PCIE5			

SATA	DESTINATION
SATA0	m-SATA
SATA1	
SATA2	
SATA3	

PCI EXPRESS	DESTINATION
Lane 1	
Lane 2	
Lane 3	NGFF CARD WLAN
Lane 4	NGFF CARD WLAN
Lane 5	
Lane 6	

**Symbol Note :**



7 : means Digital Ground

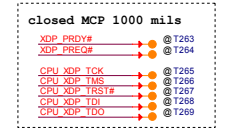
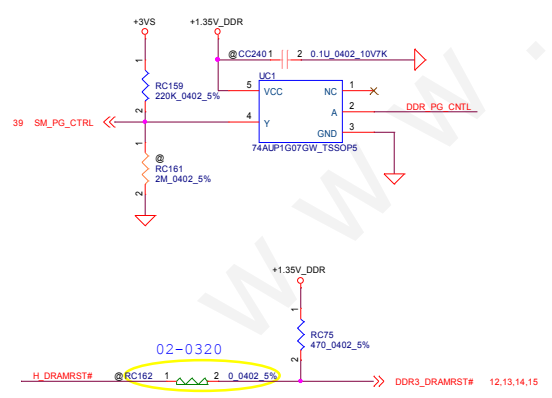
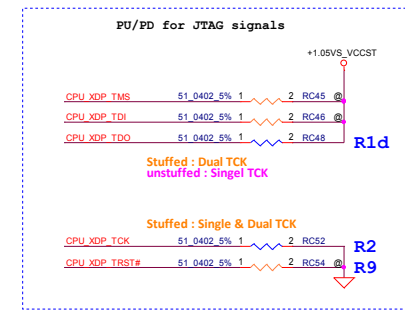
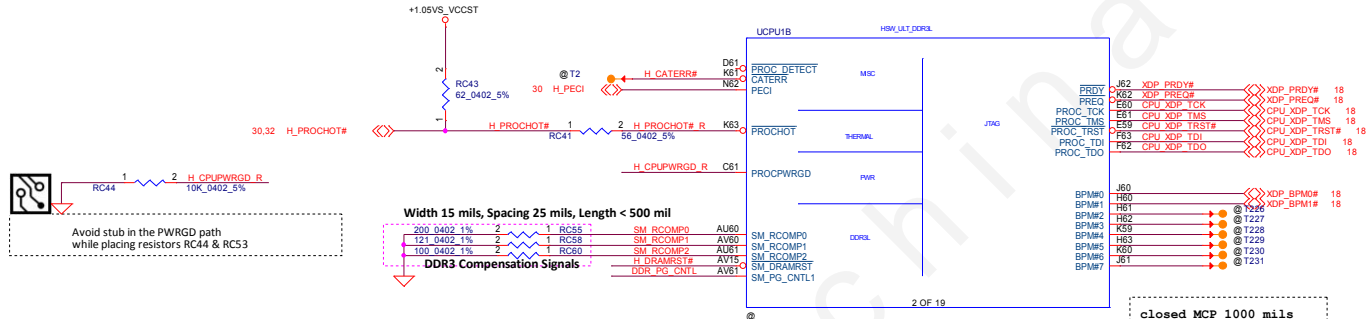
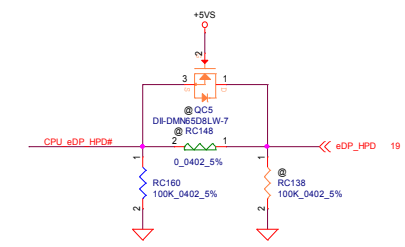
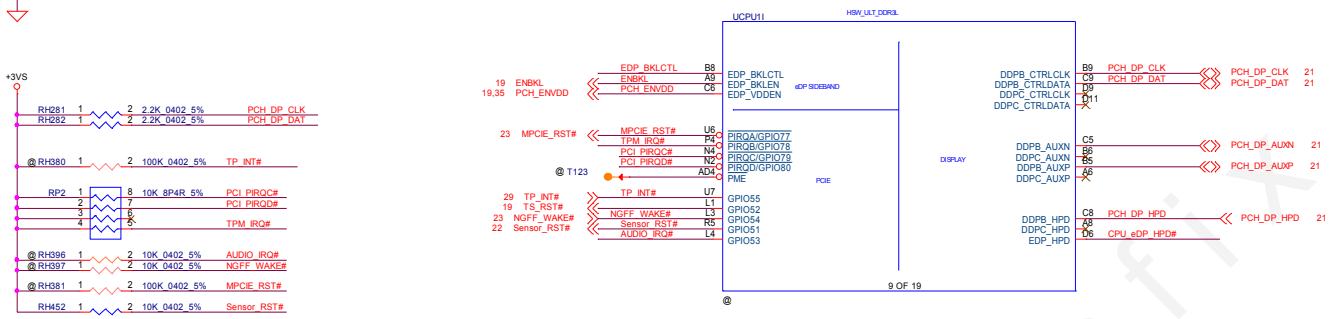
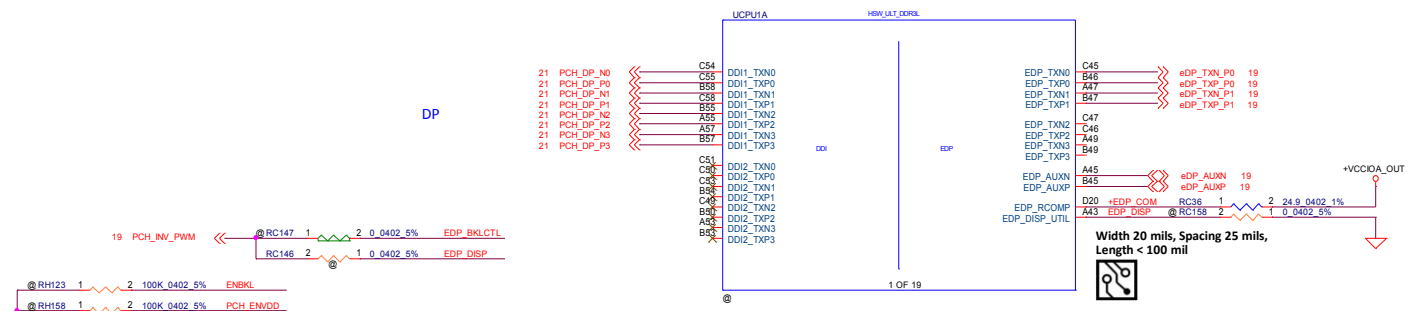


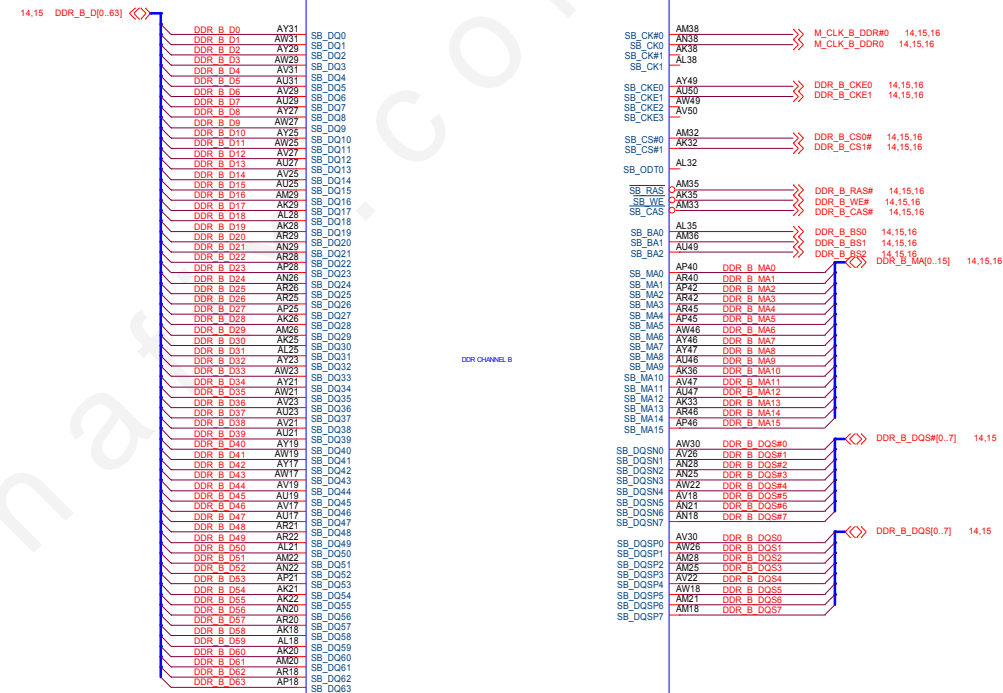
- : means Analog Ground

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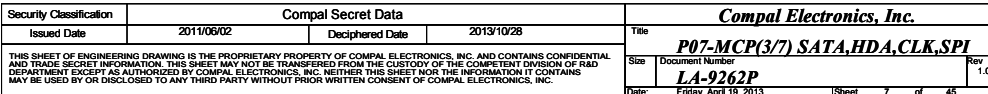


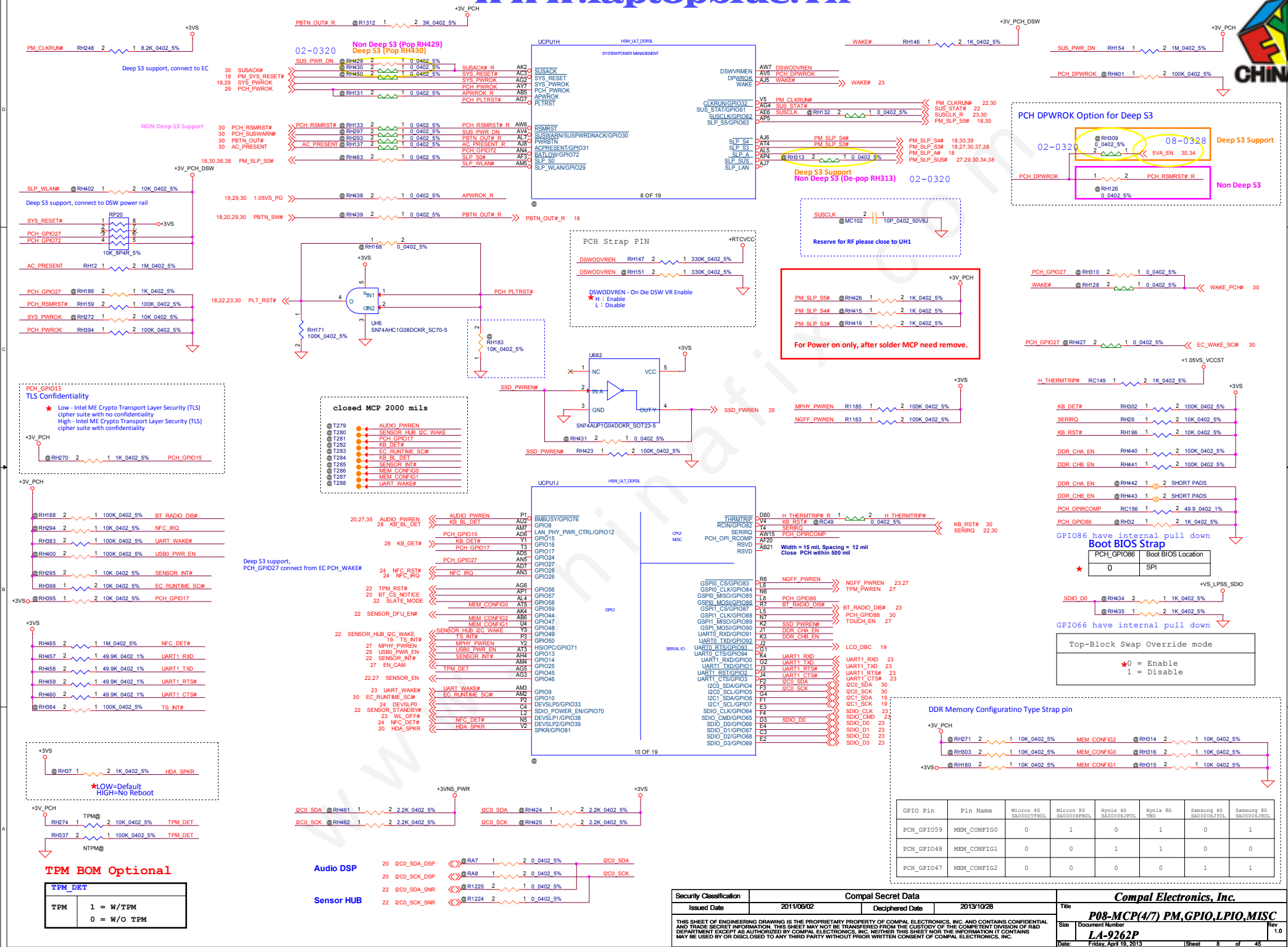
DP



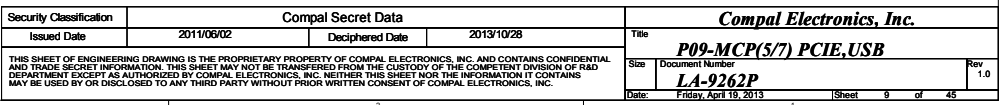
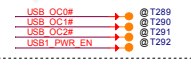
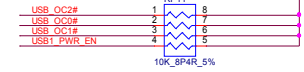


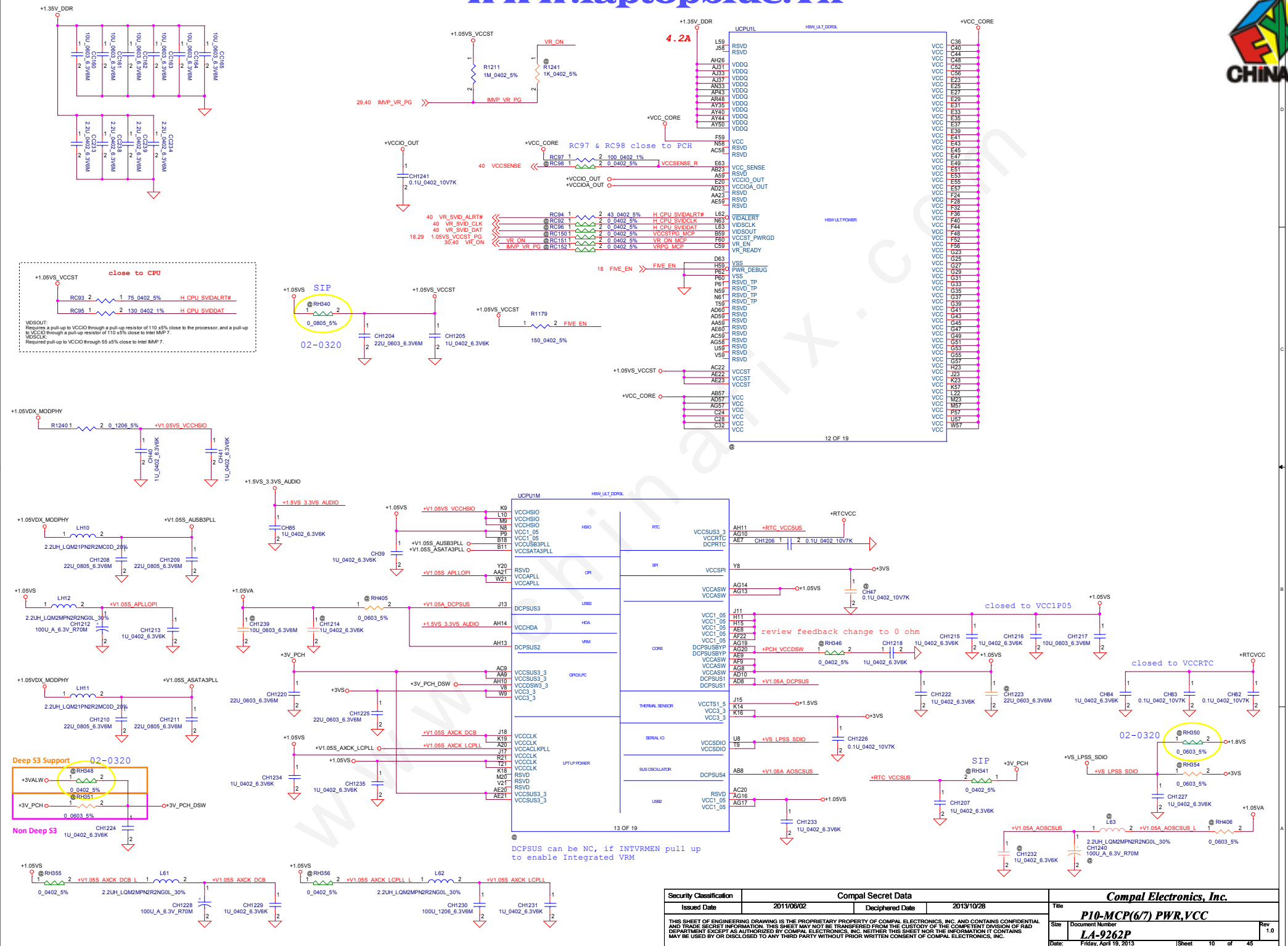
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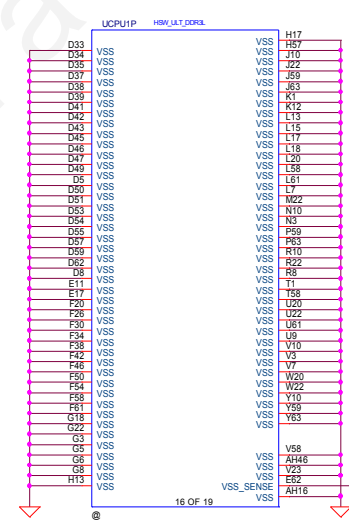
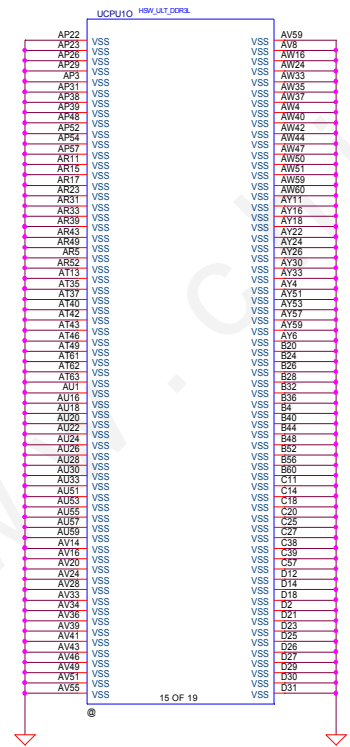
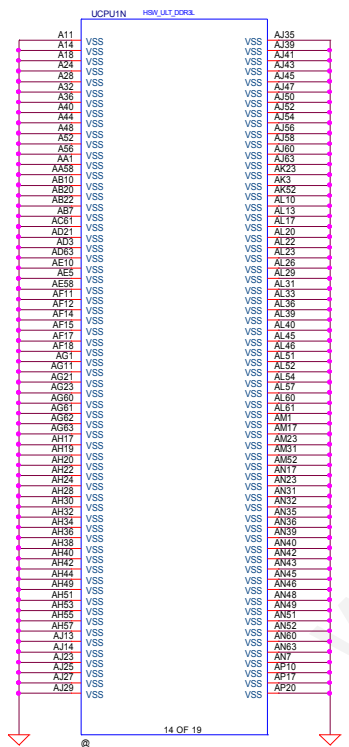
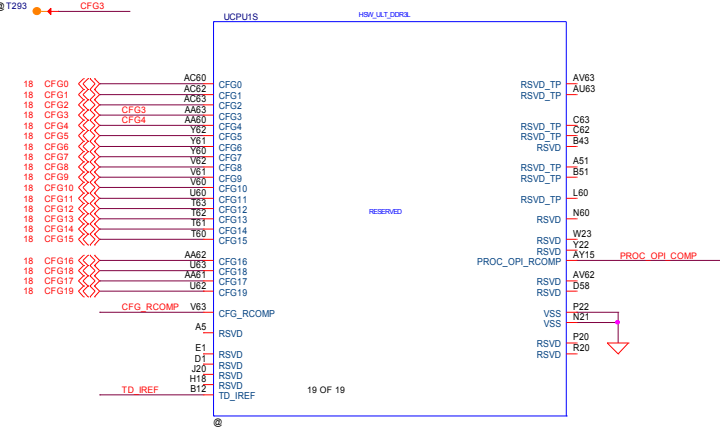
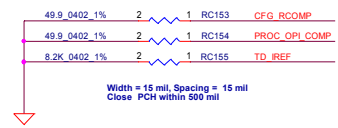
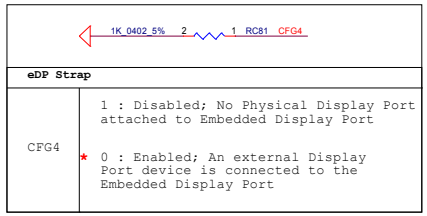


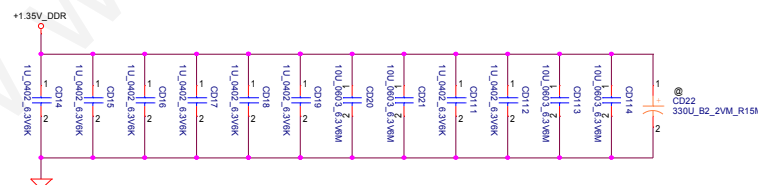
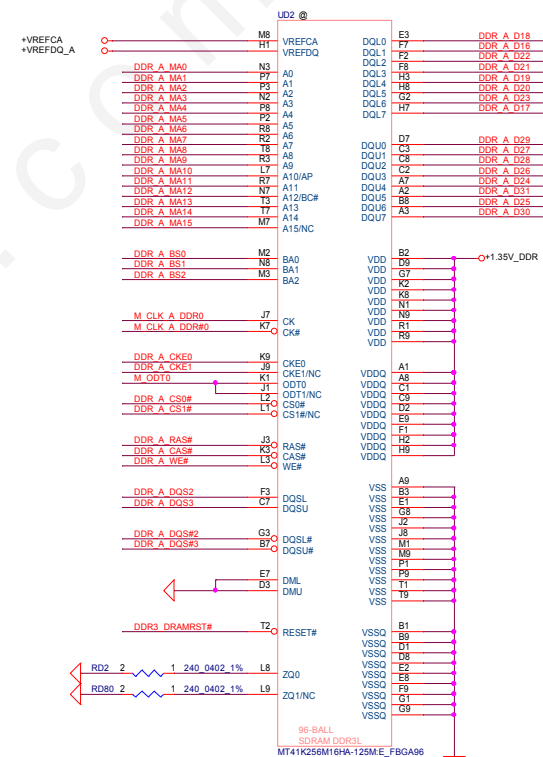
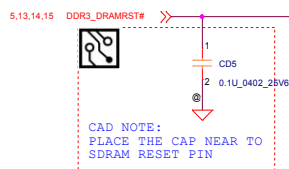






closed MCP 1000 mils  
@ T293





7,14,18,19 PCH\_SMBCLK  
7,14,18,19 PCH\_SMBDATA

+3V5

UD3

8 VCC A0 1 @ RD3 2 1K 0402 5%  
6 WP A1 2 @ RD4 2 1K 0402 5%  
5 SCL A2 3  
4 SDA 4  
7 GND

AT24C02C-10W-TSSOP8

+3V5

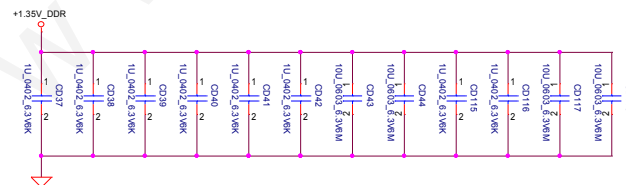
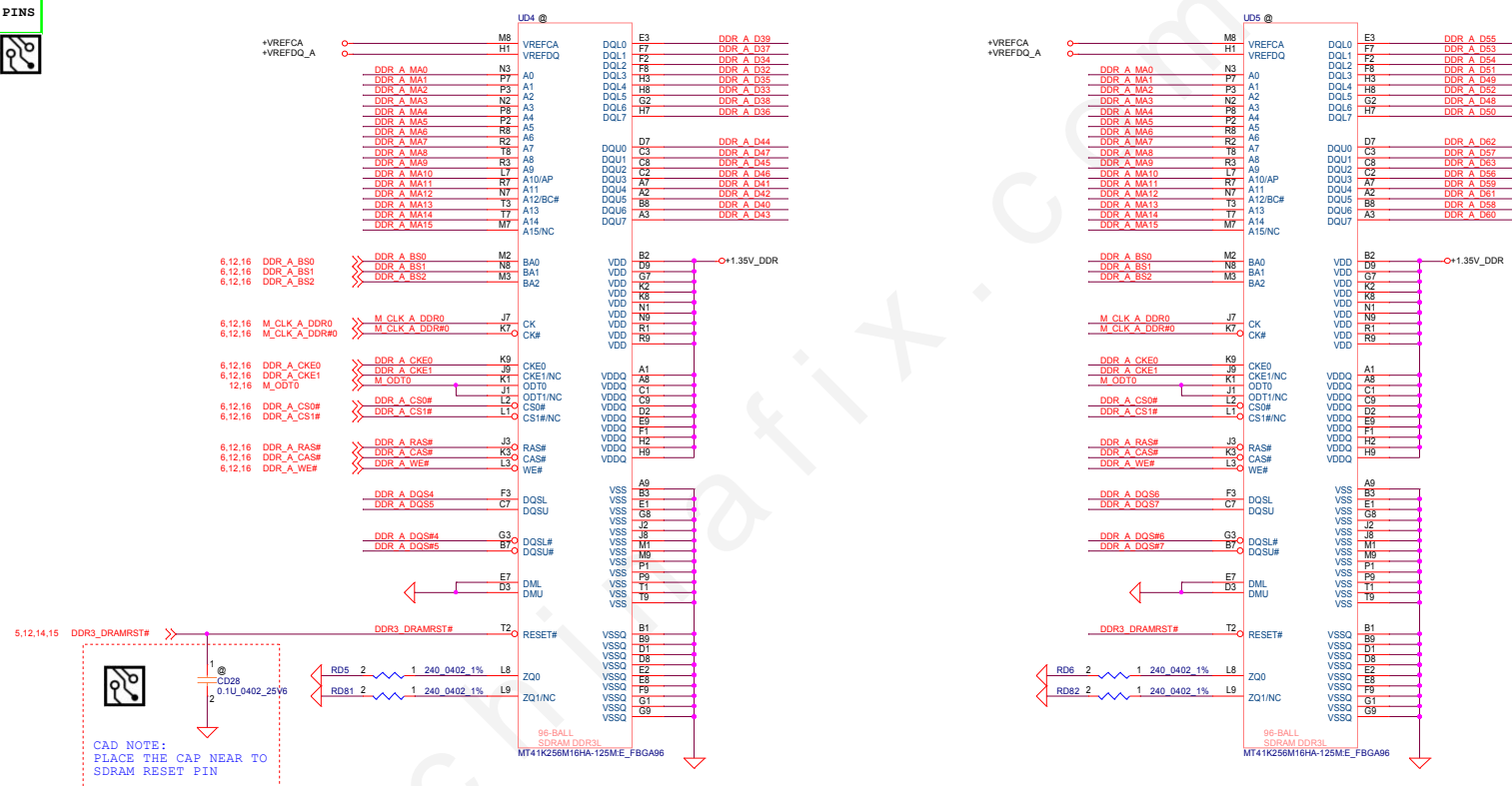
CD23  
01U\_0402\_10V7

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PLACE THESE CAPS  
NEAR TO RESPECTIVE DIMM PINS

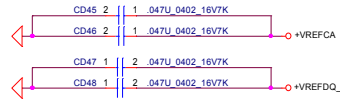


| All VREF traces should  
| have 10 mil trace width



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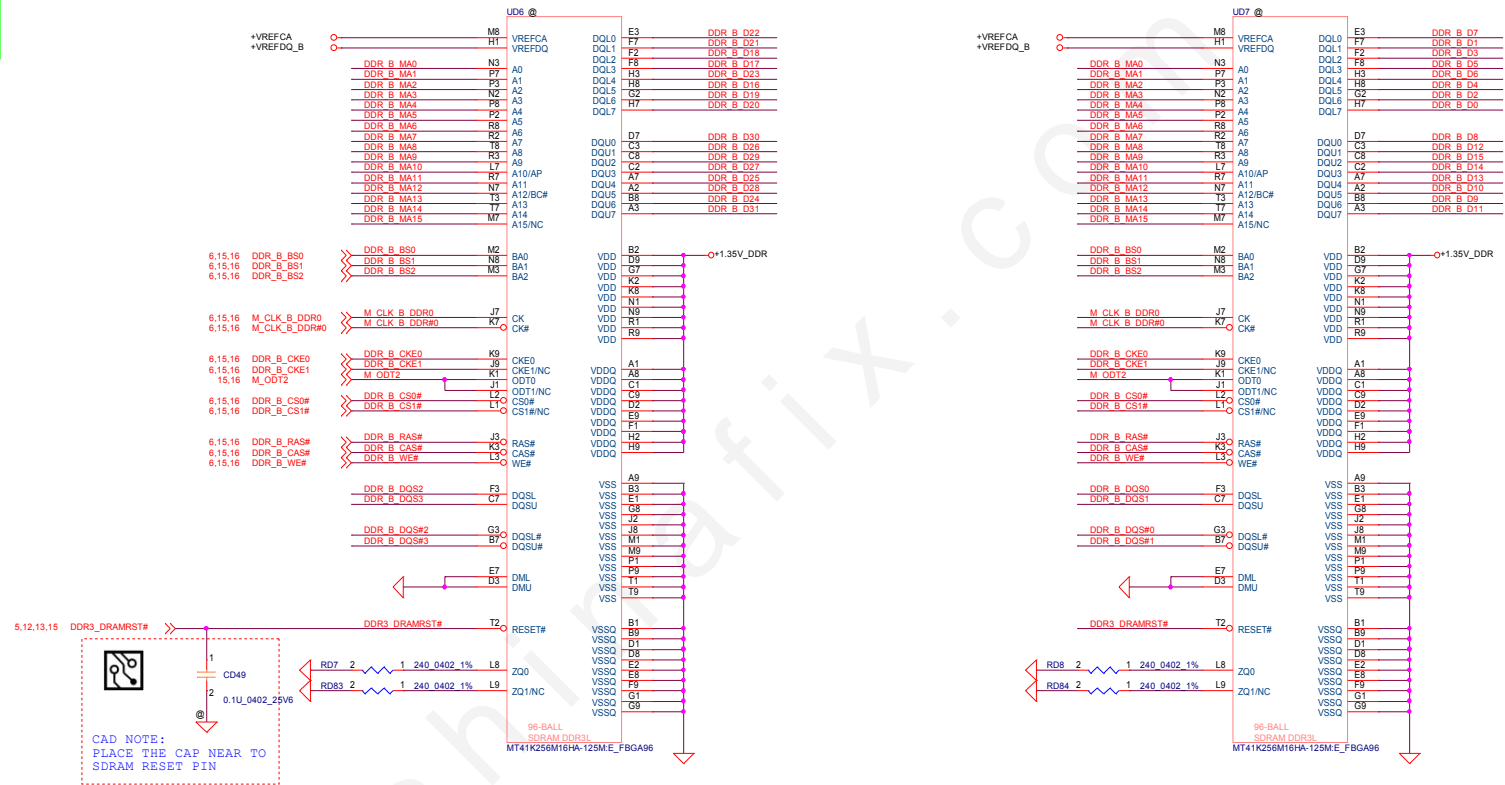
follow INTEL PDG



PLACE THESE CAPS  
NEAR TO RESPECTIVE DIMM PINS



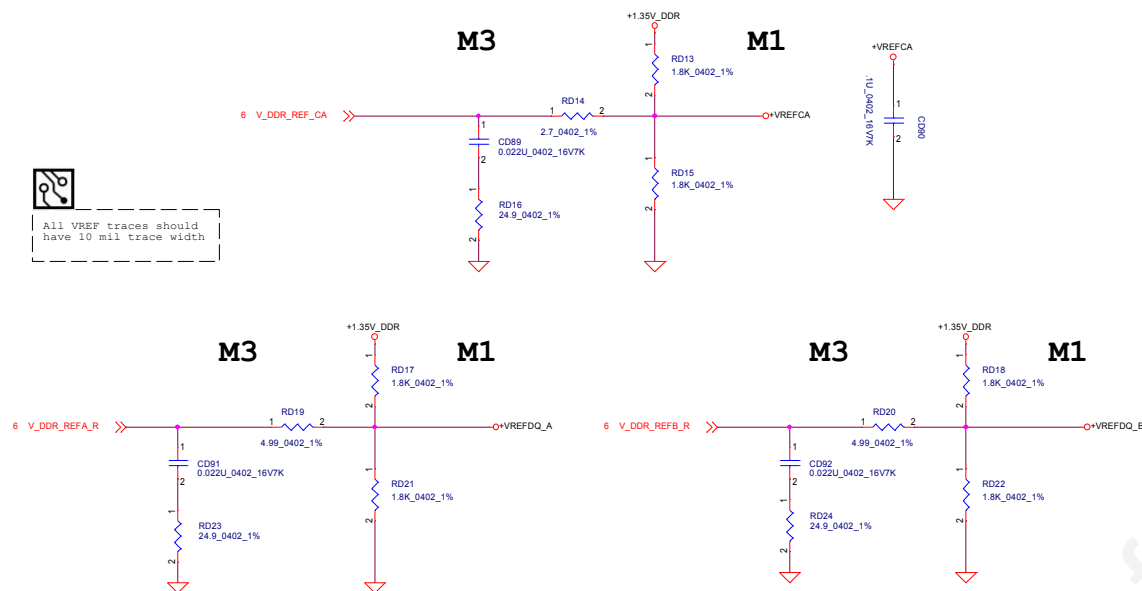
All VREF traces should  
have 10 mil trace width



5



All VREF traces should have 10 mil trace width



DDR A MA12 RD25 1 2 34.8 0402 1%  
DDR A MA15 RD27 1 2 34.8 0402 1%  
DDR A MA9 RD29 1 2 34.8 0402 1%  
DDR A MA10 RD31 1 2 34.8 0402 1%

DDR A MA4 RD33 1 2 34.8 0402 1%  
DDR A MA2 RD35 1 2 34.8 0402 1%  
DDR A MA1 RD37 1 2 34.8 0402 1%  
DDR A MA6 RD39 1 2 34.8 0402 1%

DDR A MA3 RD41 1 2 34.8 0402 1%  
DDR A MA9 RD43 1 2 34.8 0402 1%  
DDR A MA11 RD45 1 2 34.8 0402 1%  
DDR A MA5 RD47 1 2 34.8 0402 1%

DDR A MA14 RD49 1 2 34.8 0402 1%  
DDR A MA7 RD51 1 2 34.8 0402 1%  
DDR A MA8 RD53 1 2 34.8 0402 1%  
DDR A MA13 RD55 1 2 34.8 0402 1%

6.12.13 DDR\_A\_CKE0 RD57 1 2 34.8 0402 1%  
6.12.13 DDR\_A\_RAS# RD59 1 2 34.8 0402 1%  
6.12.13 DDR\_A\_CSM# RD61 1 2 34.8 0402 1%  
6.12.13 DDR\_A\_CAS# RD63 1 2 34.8 0402 1%

6.12.13 DDR\_A\_WE# RD65 1 2 34.8 0402 1%  
6.12.13 DDR\_A\_BS0 RD67 1 2 34.8 0402 1%  
6.12.13 DDR\_A\_BS2 RD69 1 2 34.8 0402 1%  
6.12.13 DDR\_A\_BS1 RD71 1 2 34.8 0402 1%

6.12.13 DDR\_A\_CKE1 RD87 1 2 34.8 0402 1%  
6.12.13 DDR\_A\_CS1# RD88 1 2 34.8 0402 1%

12.13 M\_ODT0 RD73 1 2 30 0402 1%

6.12.13 M\_CLK\_A\_DDR0 RD75 1 2 26.1 0402 1%

6.12.13 M\_CLK\_A\_DDR#0 RD77 1 2 26.1 0402 1%

DDR B MA12 RD26 1 2 34.8 0402 1%  
DDR B MA15 RD28 1 2 34.8 0402 1%  
DDR B MA9 RD30 1 2 34.8 0402 1%  
DDR B MA10 RD32 1 2 34.8 0402 1%

DDR B MA14 RD34 1 2 34.8 0402 1%  
DDR B MA6 RD36 1 2 34.8 0402 1%  
DDR B MA4 RD38 1 2 34.8 0402 1%  
DDR B MA2 RD40 1 2 34.8 0402 1%

DDR B MA8 RD42 1 2 34.8 0402 1%  
DDR B MA1 RD44 1 2 34.8 0402 1%  
DDR B MA13 RD46 1 2 34.8 0402 1%  
DDR B MA7 RD48 1 2 34.8 0402 1%

DDR B MA3 RD50 1 2 34.8 0402 1%  
DDR B MA9 RD52 1 2 34.8 0402 1%  
DDR B MA11 RD54 1 2 34.8 0402 1%  
DDR B MA5 RD56 1 2 34.8 0402 1%

6.14.15 DDR\_B\_CKE0 RD58 1 2 34.8 0402 1%  
6.14.15 DDR\_B\_CSM# RD60 1 2 34.8 0402 1%  
6.14.15 DDR\_B\_CAS# RD62 1 2 34.8 0402 1%  
6.14.15 DDR\_B\_RAS# RD64 1 2 34.8 0402 1%

6.14.15 DDR\_B\_BS1 RD66 1 2 34.8 0402 1%  
6.14.15 DDR\_B\_BS2 RD68 1 2 34.8 0402 1%  
6.14.15 DDR\_B\_BS0 RD70 1 2 34.8 0402 1%  
6.14.15 DDR\_B\_WE# RD72 1 2 34.8 0402 1%

6.14.15 DDR\_B\_CKE1 RD89 1 2 34.8 0402 1%  
6.14.15 DDR\_B\_CS1# RD90 1 2 34.8 0402 1%

14.15 M\_ODT2 RD74 1 2 30 0402 1%

6.14.15 M\_CLK\_B\_DDR0 RD76 1 2 26.1 0402 1%

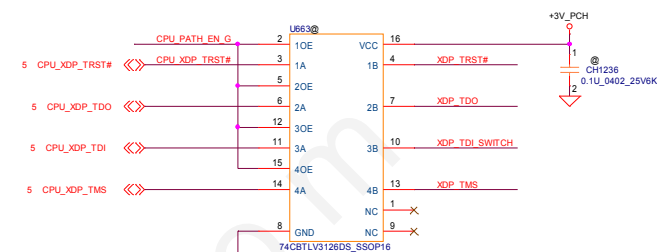
6.14.15 M\_CLK\_B\_DDR#0 RD78 1 2 26.1 0402 1%

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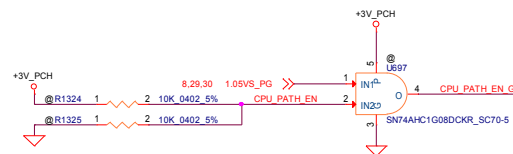




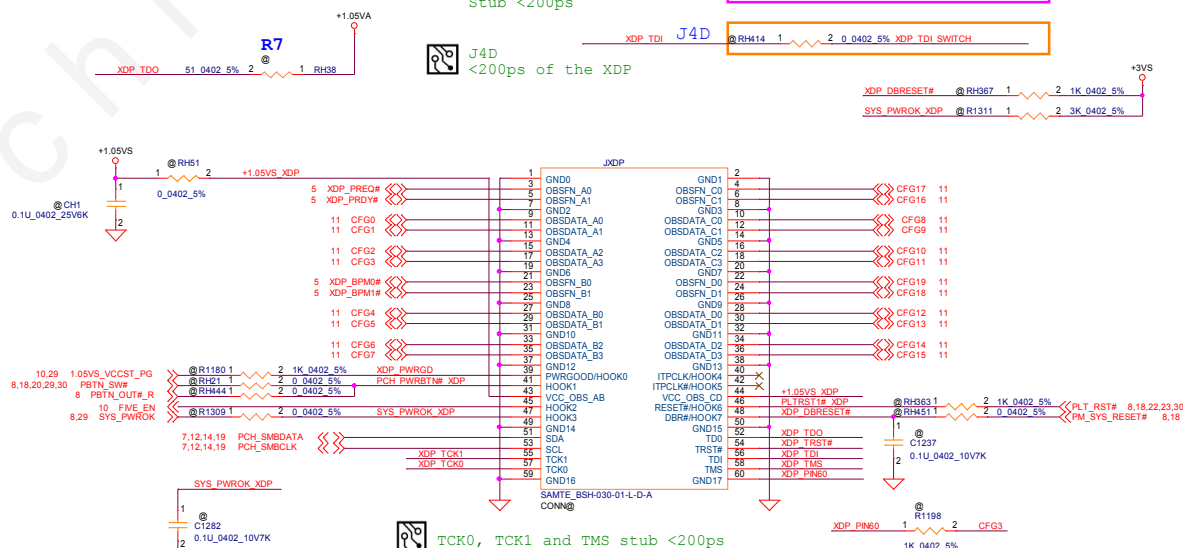
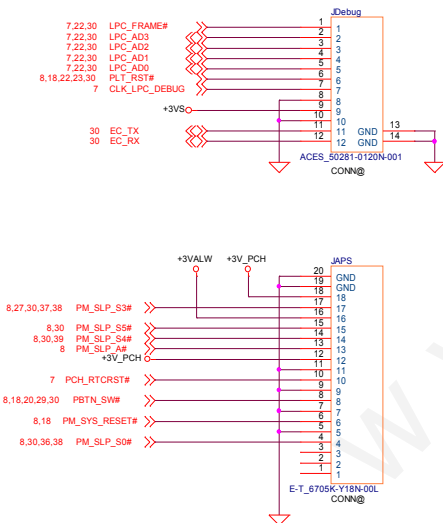
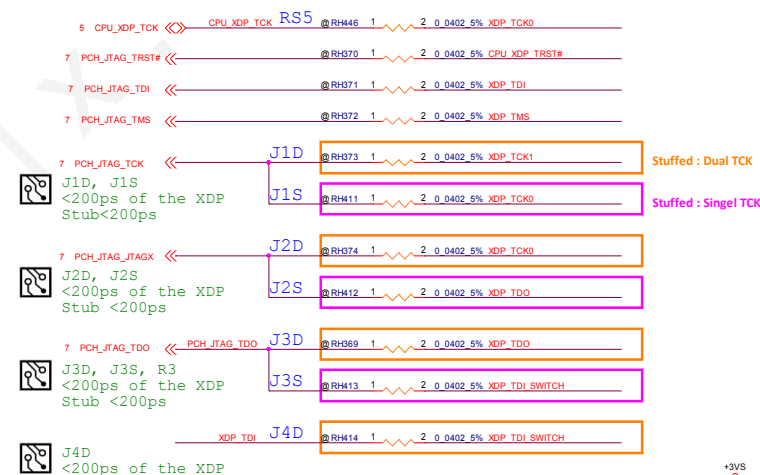
U663 200ps of XDP



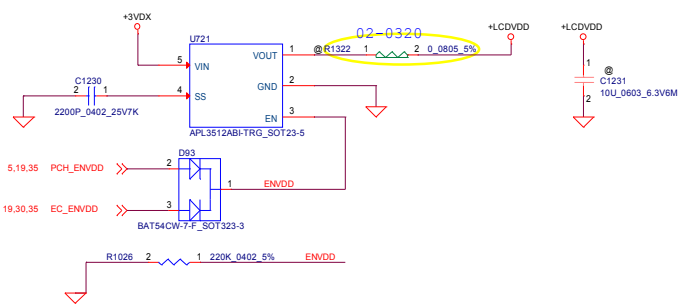
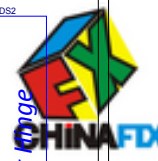
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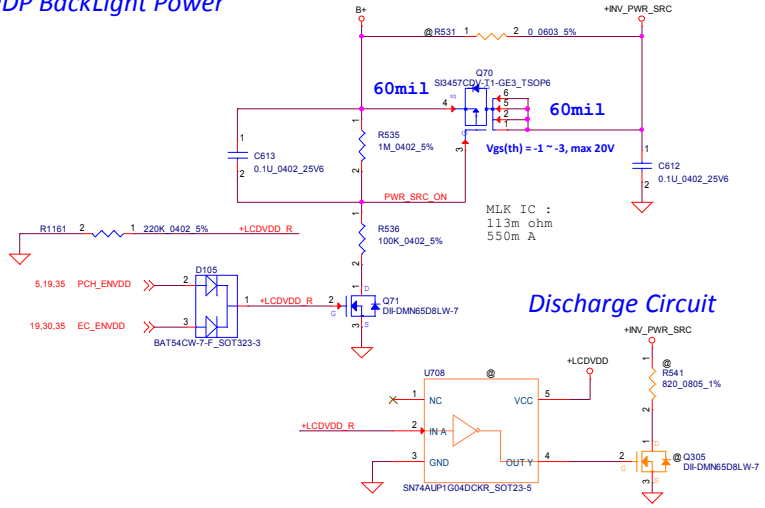
Topology	Description	Best Use for	Resistors Stuffed	Resistors uStuffed
Default Setting: Dual TCK Scan Chains (also known as "Shared JTAG" in other document)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1, R2, J1d, J2d, J3d, J4d, R3, R4, R5	J1s, J2s, J3s
Single TCK scan chain (also known as "Common JTAG" in other document)	In this topology, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	- Boundary Scan/Manufacturing test	J1s, J2s, J3s, J4d, R2, R3, R4, R5	R1, J1d, J2d, J3d, J4d



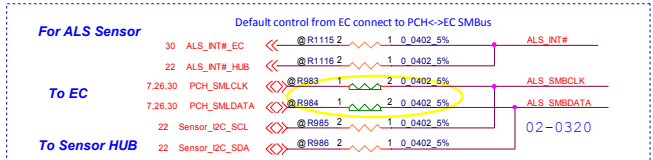
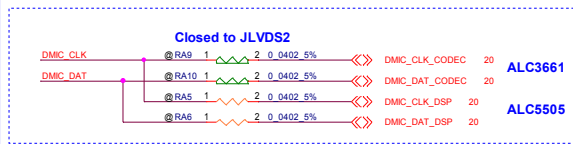
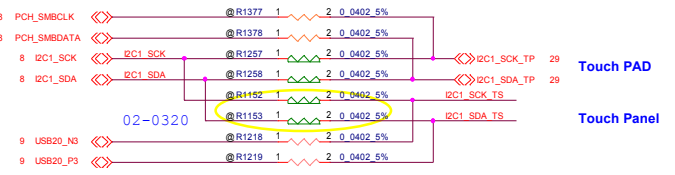
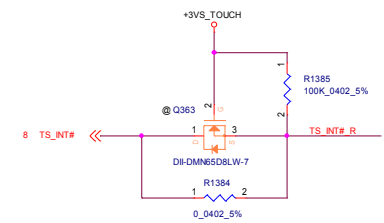
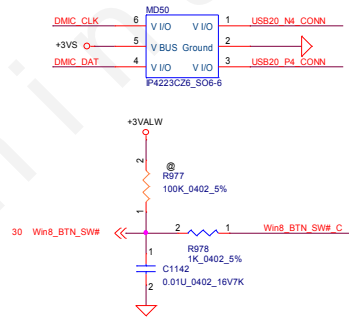
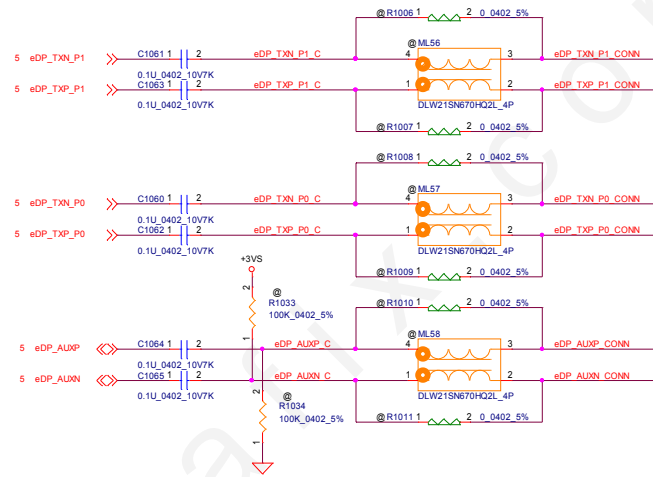
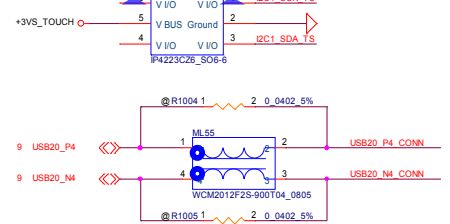
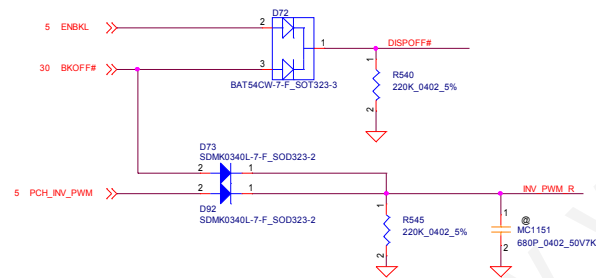
TCK0, TCK1 and TMS stub &lt;200ps



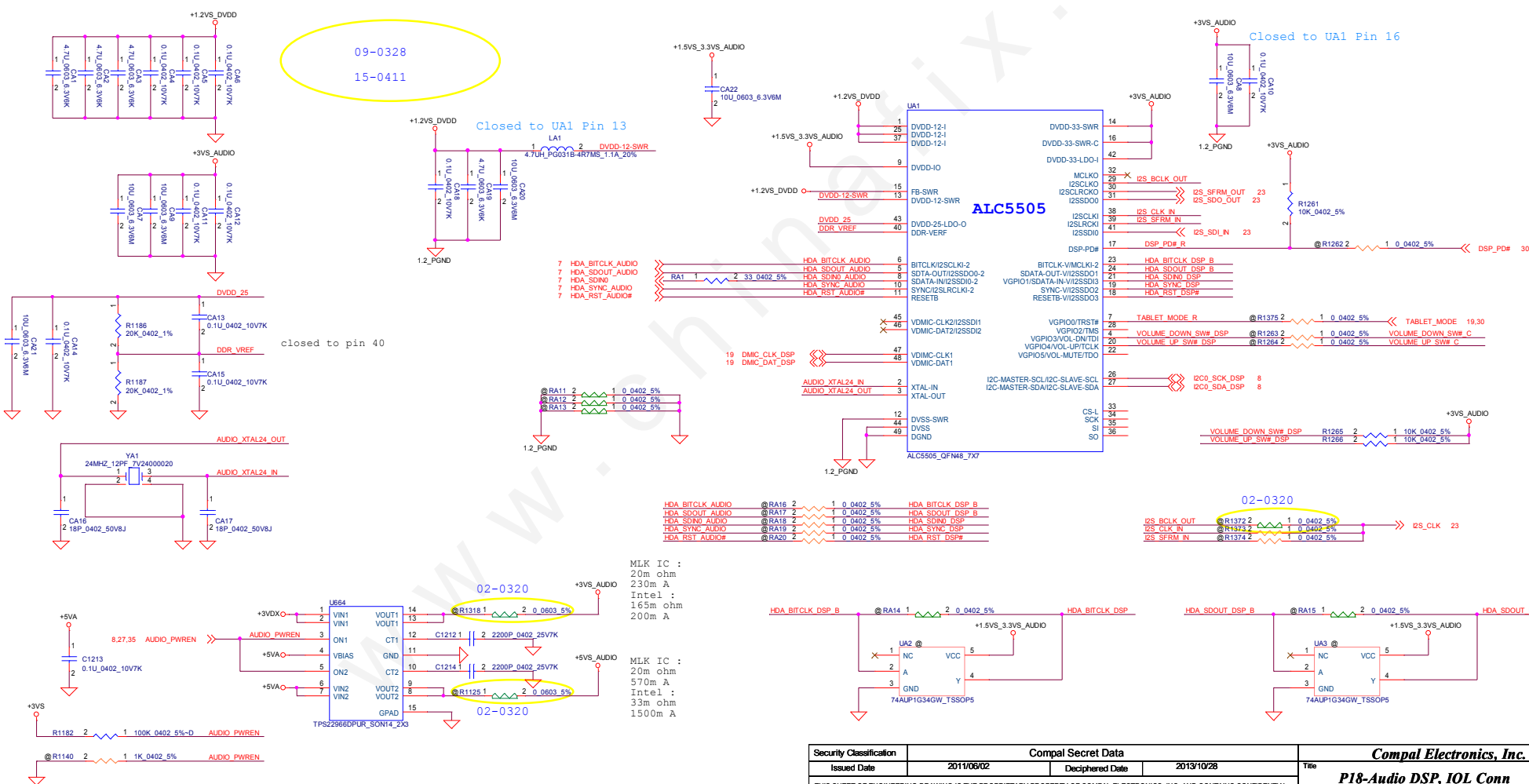
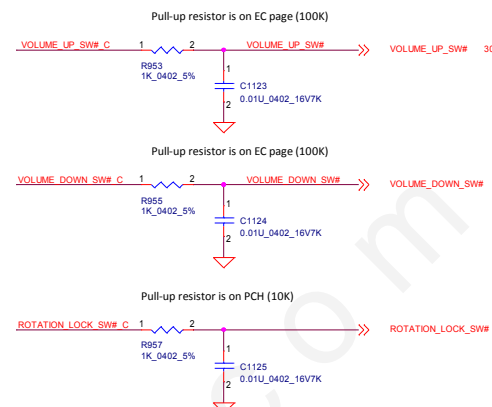
### eDP BackLight Power



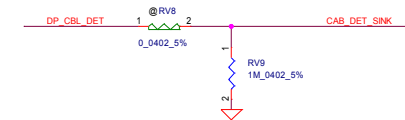
### BackLight PWM Control



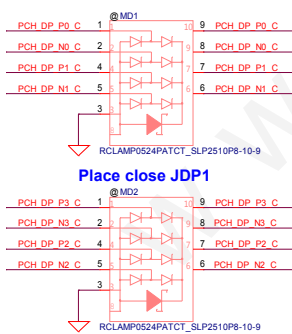
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Compall Electronics, Inc.	
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Size		Document Number		Rev	
Friday, April 19, 2013		LA-9262P		1.0	
Sheet		19		of	
1		1		45	



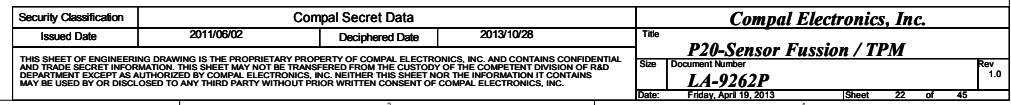
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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				Size	Document Number
				LA-9262P	
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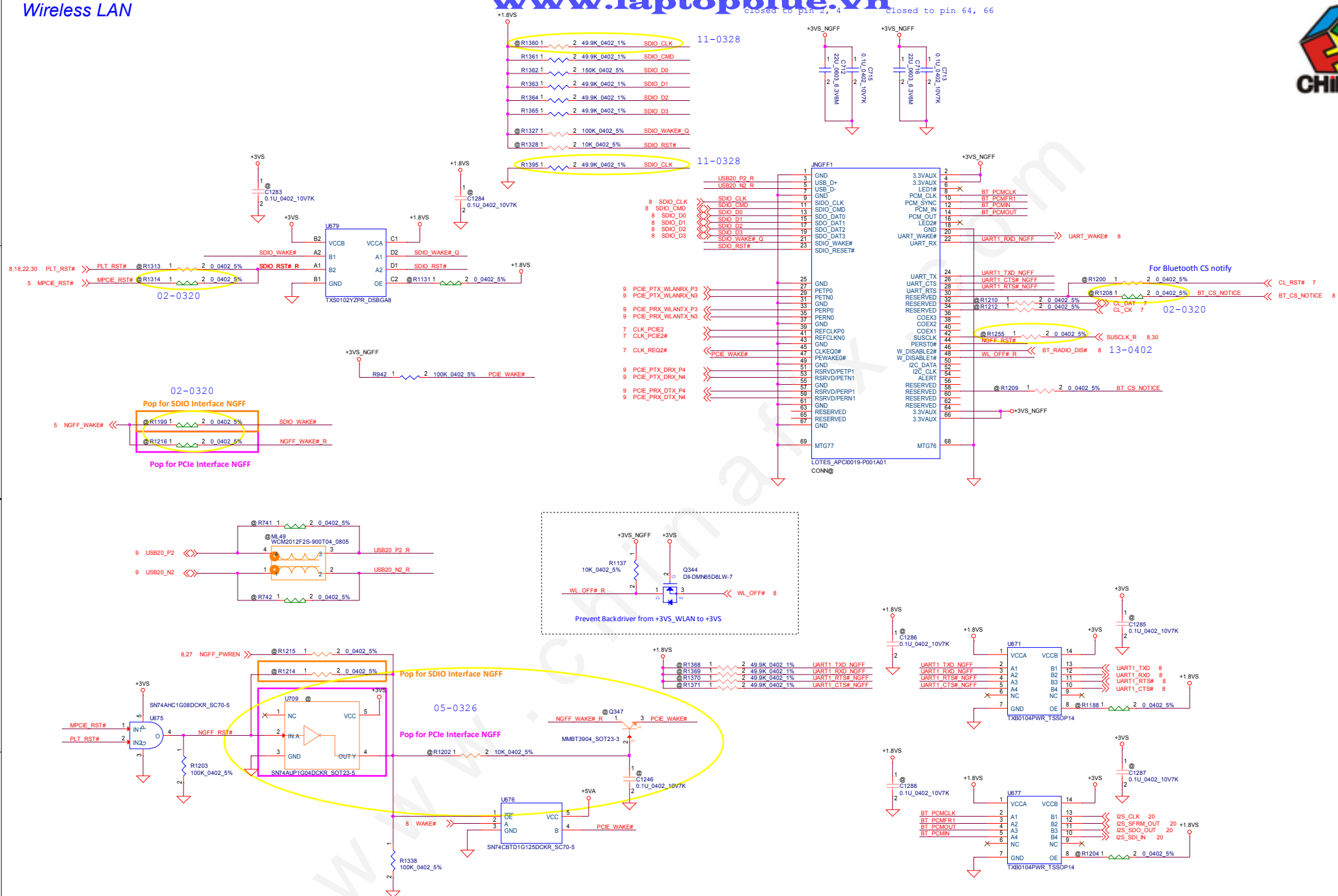


*DP Signal ESD*



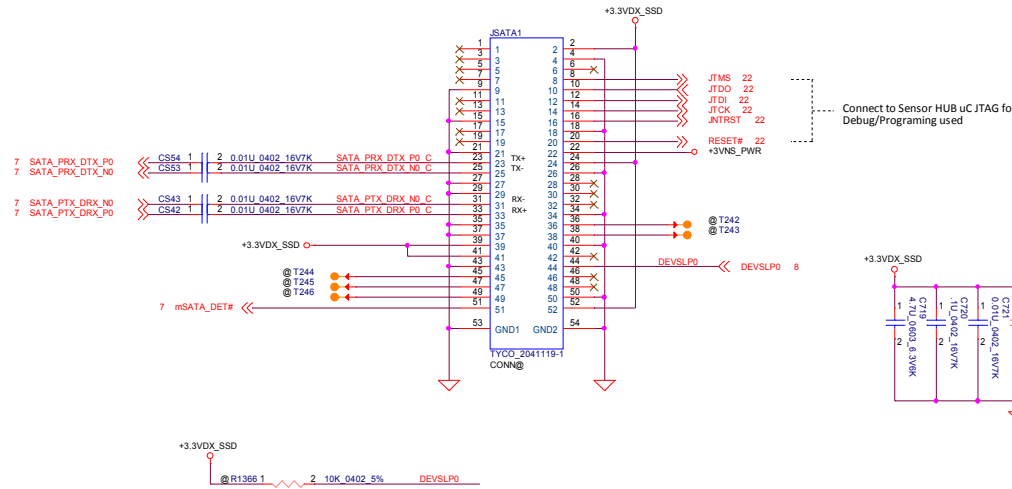
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Time
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			Size	Document Number
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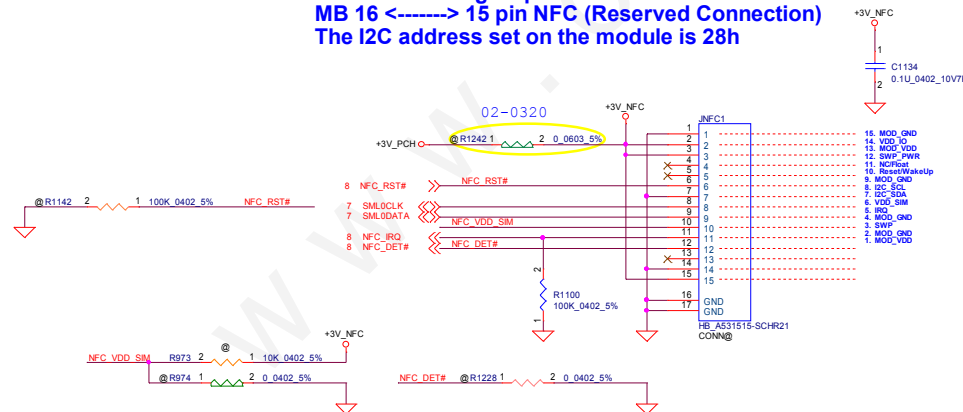


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				(Sheet	91 of 45

# mSATA Card



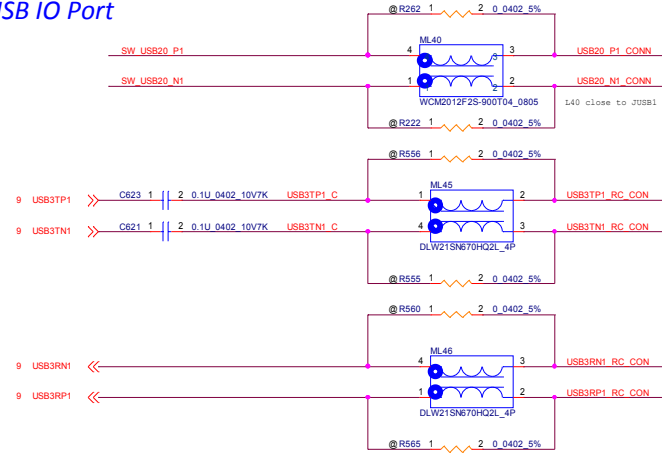
ME Decide using 16 pin conn  
MB 16 <-----> 15 pin NFC (Reserved Connection)  
The I2C address set on the module is 28h



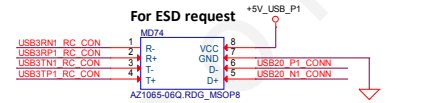
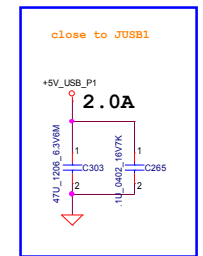
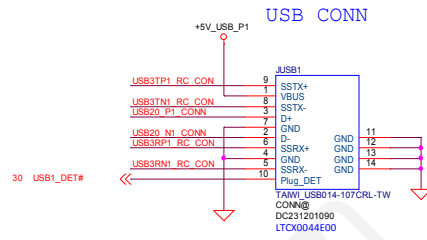
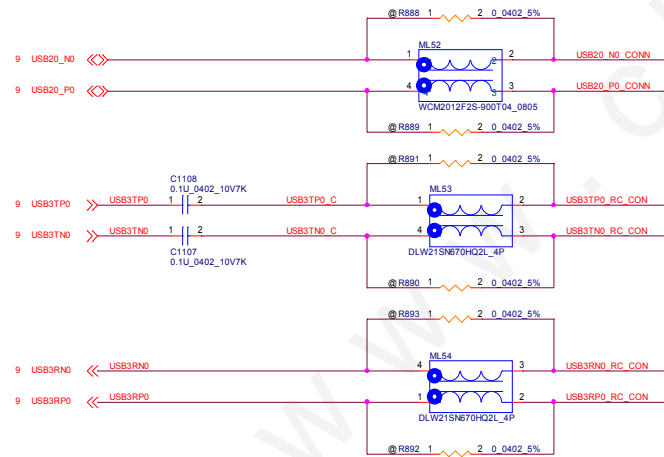
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Issued Date	2011/05/02	Deciphered Date	2013/10/28	Title	
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Size	C	Document Number	LA-9262P	Rev	1.0
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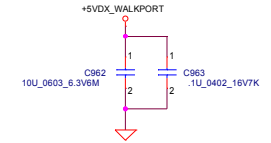
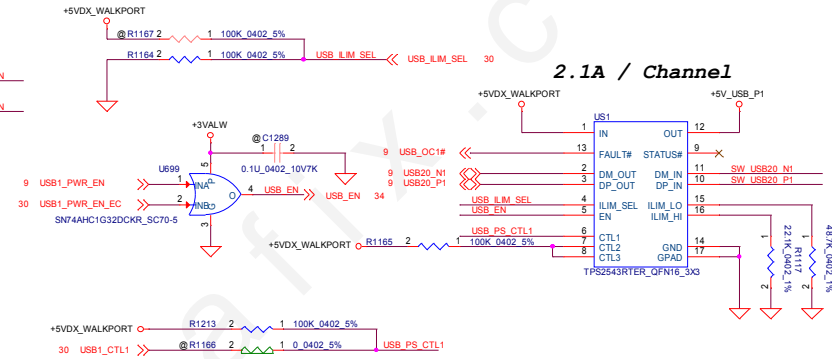
## USB IO Port



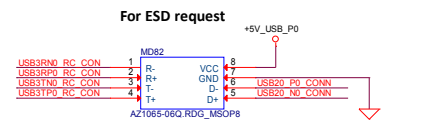
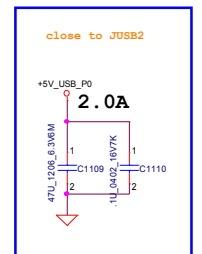
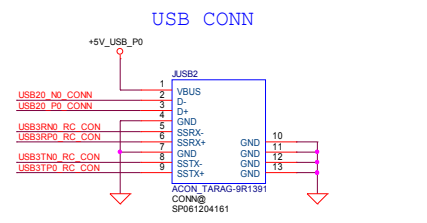
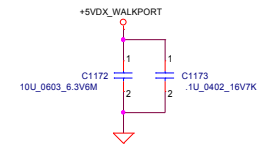
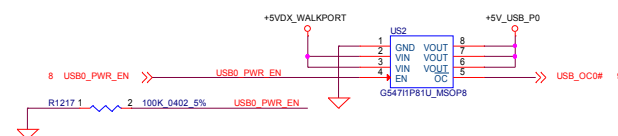
CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDP
1	1	1	1	CDP

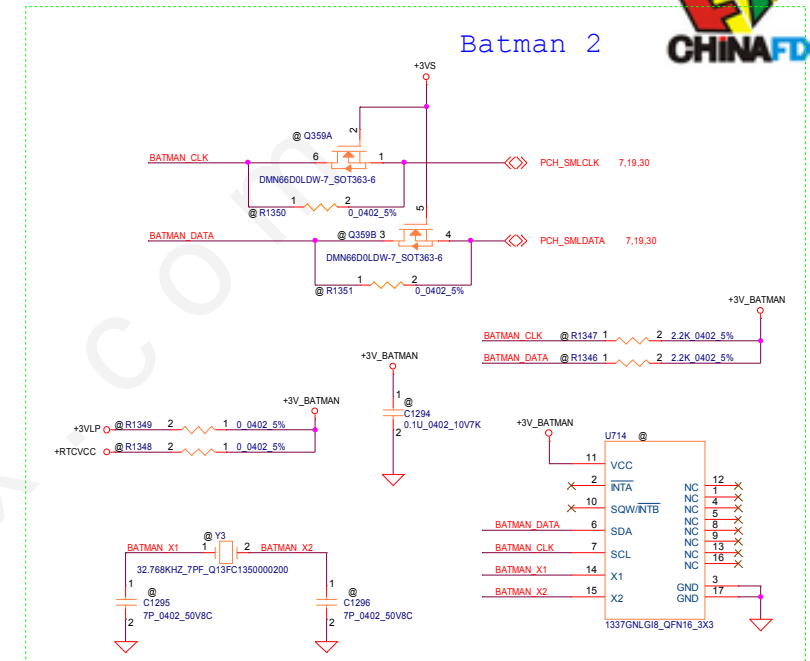
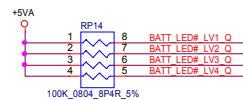
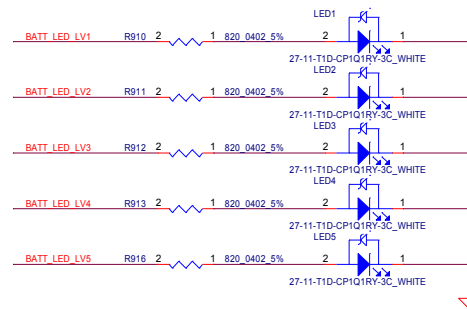
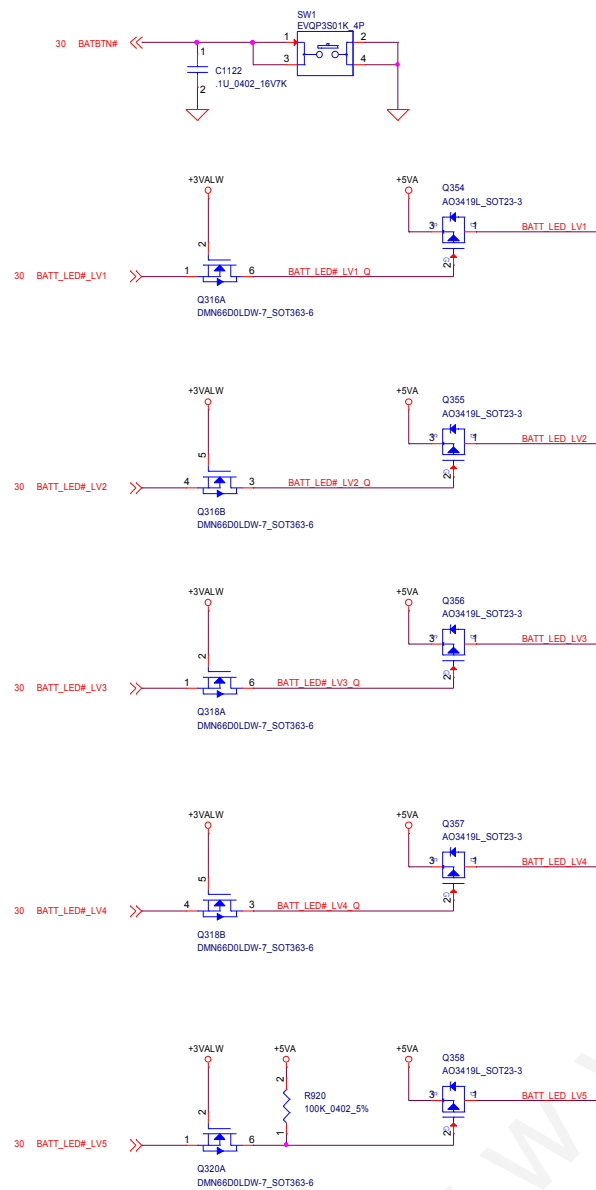


## 2.1A / Channel



## 2A / Channel



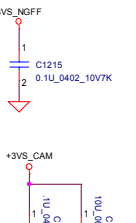
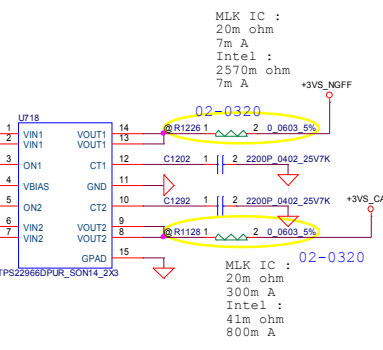
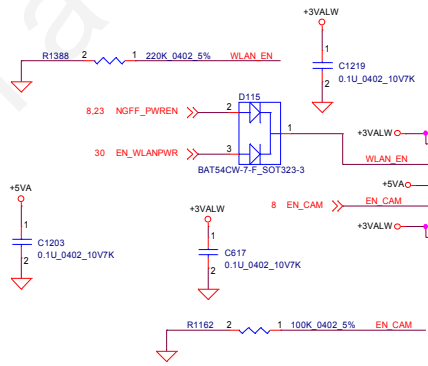
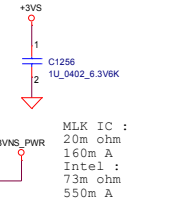
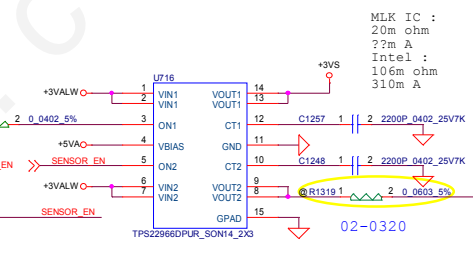
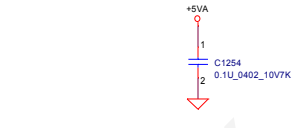
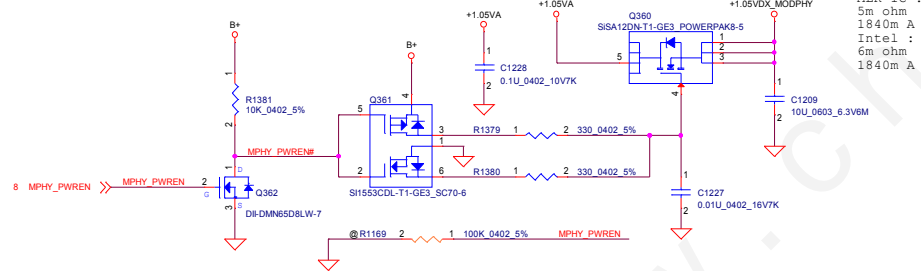
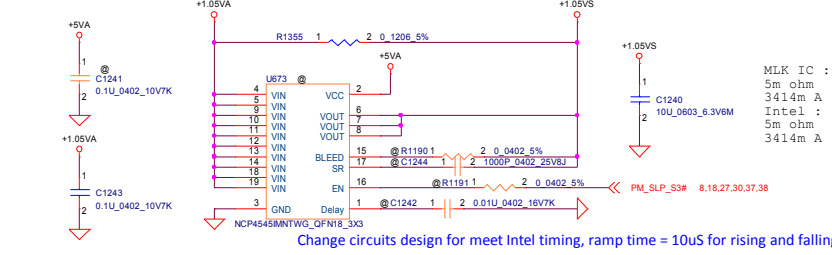
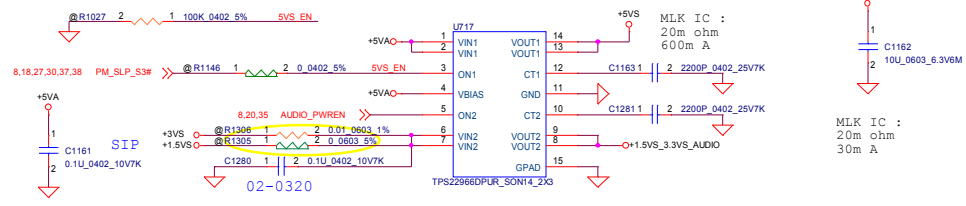
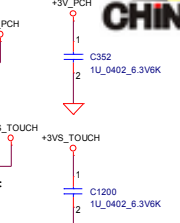
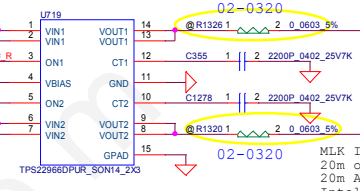
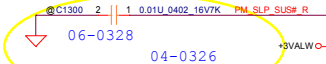
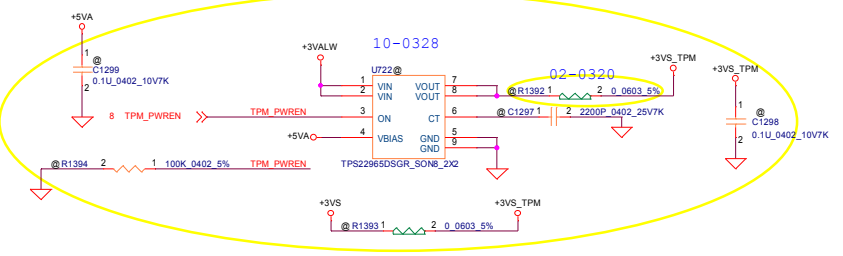


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				Rev
				1.0
				Date
				Friday, April 19, 2013
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				26 of 45

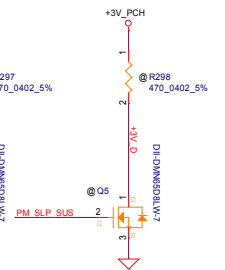
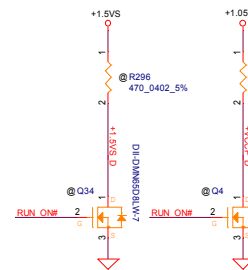
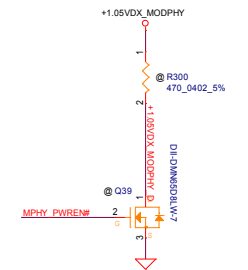
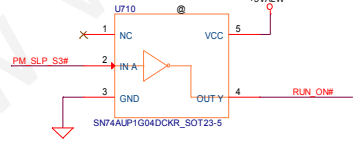
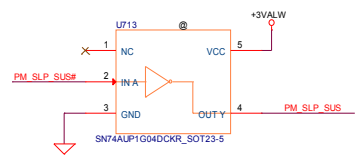


PM\_SLP\_SUS# : Deep Sx Indication  
When asserted (low), this signal indicates PCH is in Deep Sx state where internal Sx power is shut off for enhanced power saving.  
When deasserted (high), this signal indicates exit from Deep Sx state and Sx power can be applied to PCH

MLK IC :  
20m ohm  
500m A  
Intel :  
532m ohm  
62m A



# Discharge



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Diagram of a 16-pin connector with pins H1 through H17. Pins H1, H5, H6, H3, and H8 are connected to ground. Pins H14, H16, and H17 are marked with an 'X' and are not connected. Pins H2P3, H2P1, H2P3, H4P0, H3P2, H2P0XP5N, and H2P0N are connected to a common bus labeled 'CONNECT'.

H13

H<sub>2</sub>4PEN  
CONING

→X

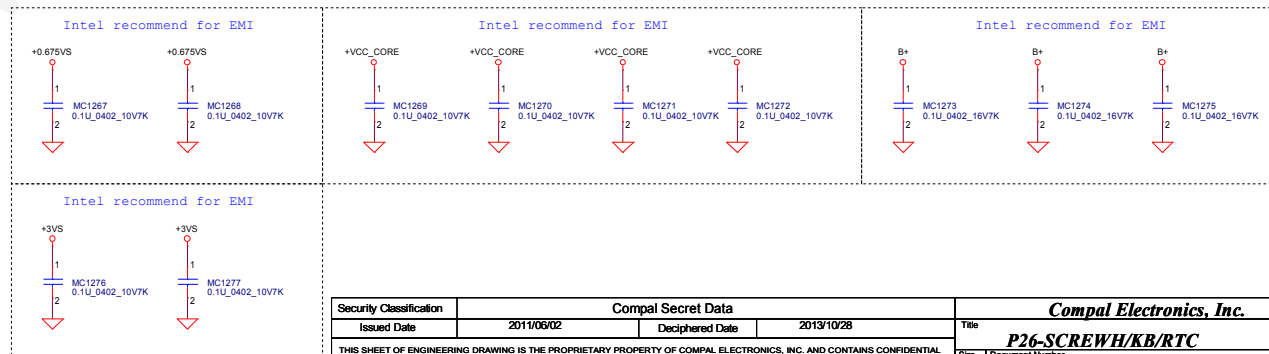
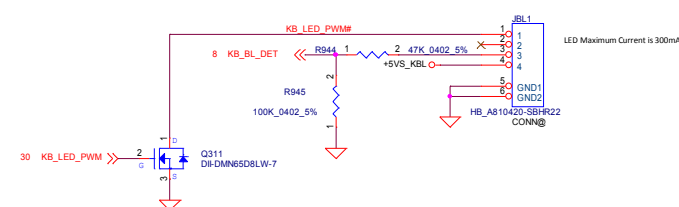
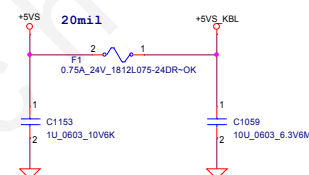
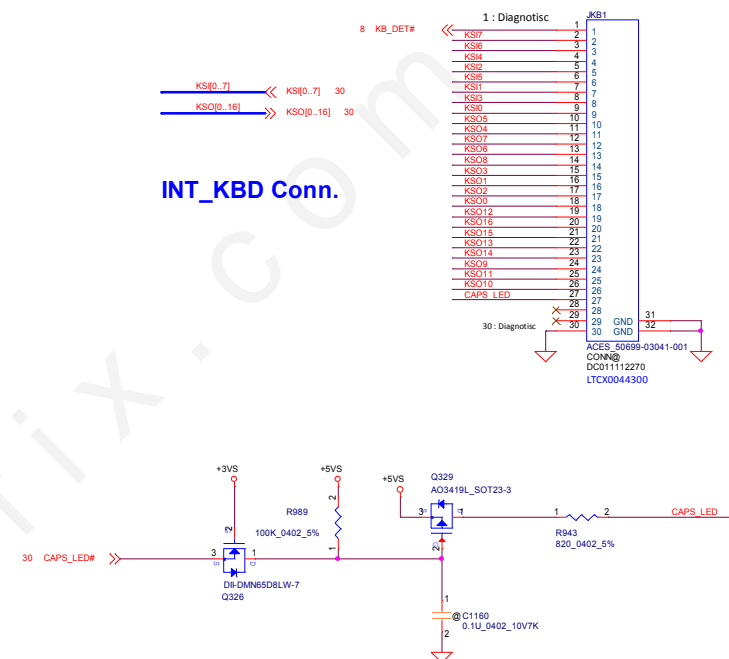
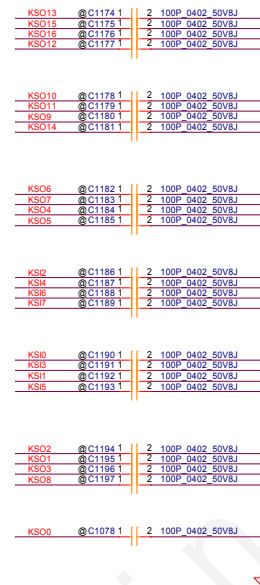
The image contains two circuit diagrams for the RTCD1 BAT54CW-7-F\_SOT323-3 component.

**Left Diagram:**

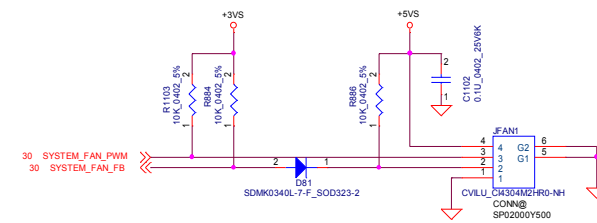
- +RTCBATT:** Connected to the positive terminal of the component.
- +3VLP:** Connected to the negative terminal of the component. A note indicates  $W=20\text{mils}$ .
- +RTCVCC:** Connected to the positive terminal of the component. A note indicates  $W=20\text{mils}$ .
- Component:** RTCD1 BAT54CW-7-F\_SOT323-3.
- Other components:** RTCR1 1K\_0402\_5% and CH65 TU\_0402\_8.3V8K.

**Right Diagram:**

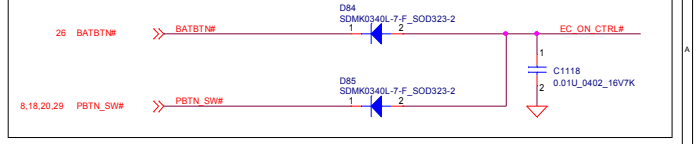
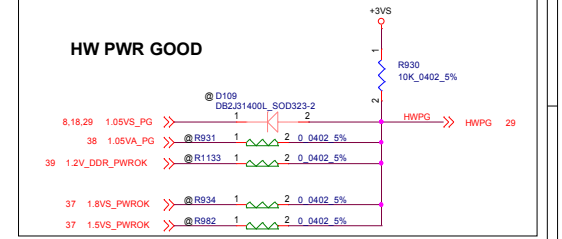
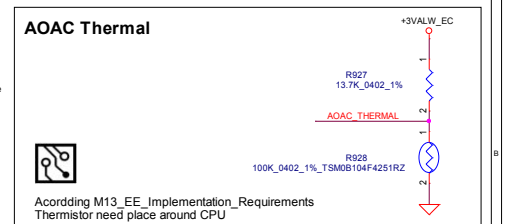
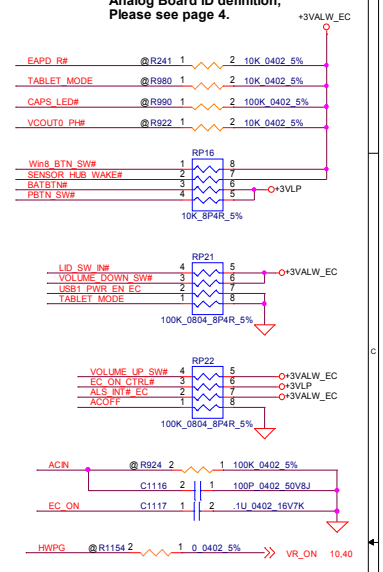
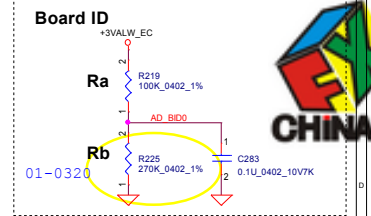
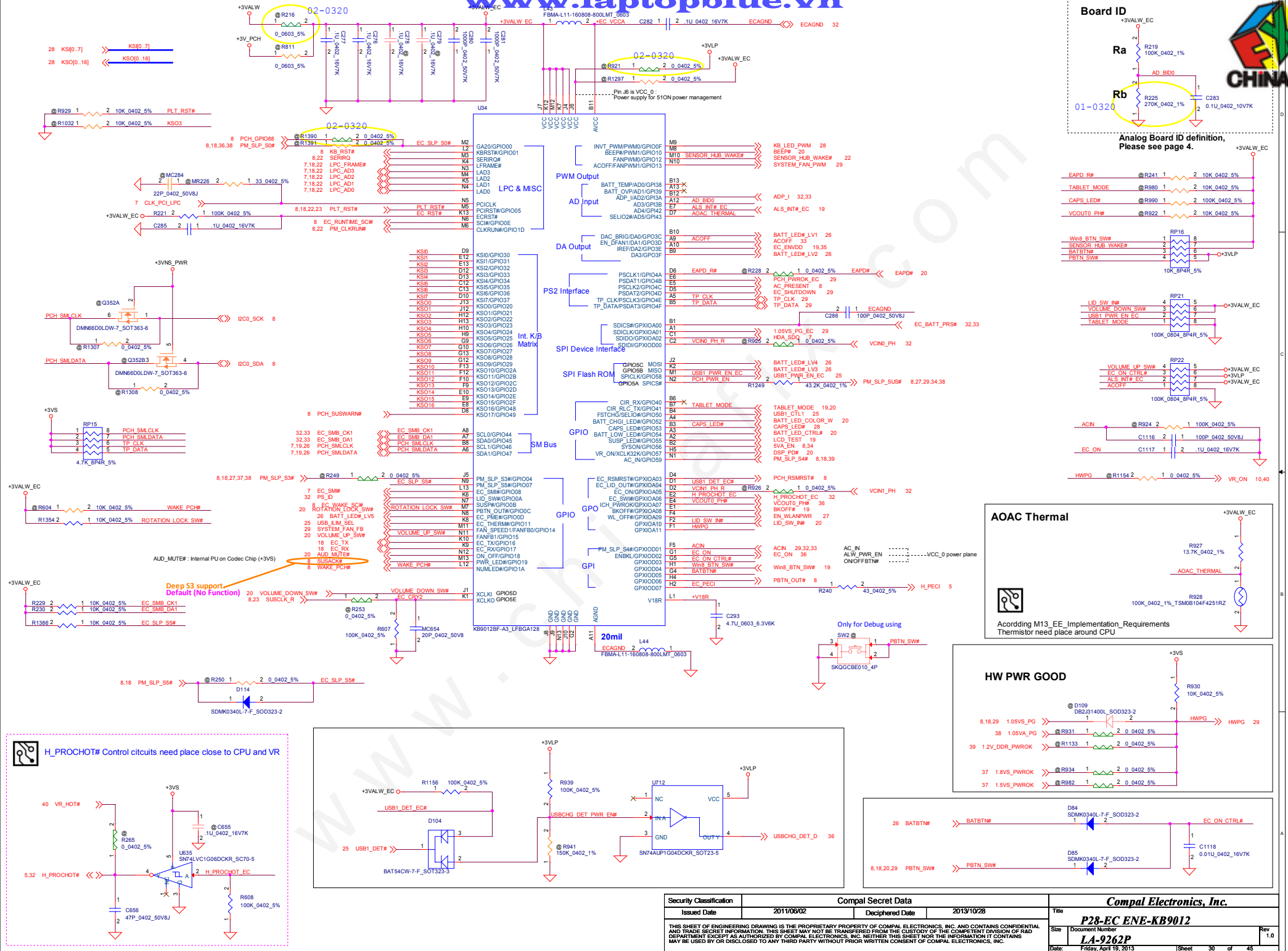
- +RTCBATT:** Connected to the positive terminal of the component.
- +RTCVCC:** Connected to the positive terminal of the component. A note indicates  $12-0328$ .
- Component:** RTCD1 BAT54CW-7-F\_SOT323-3.
- Other components:** RT1 (pin 1), G1 (pin 2), G2 (pin 3), and a note: ACES 50271-00201-001 CONN®.



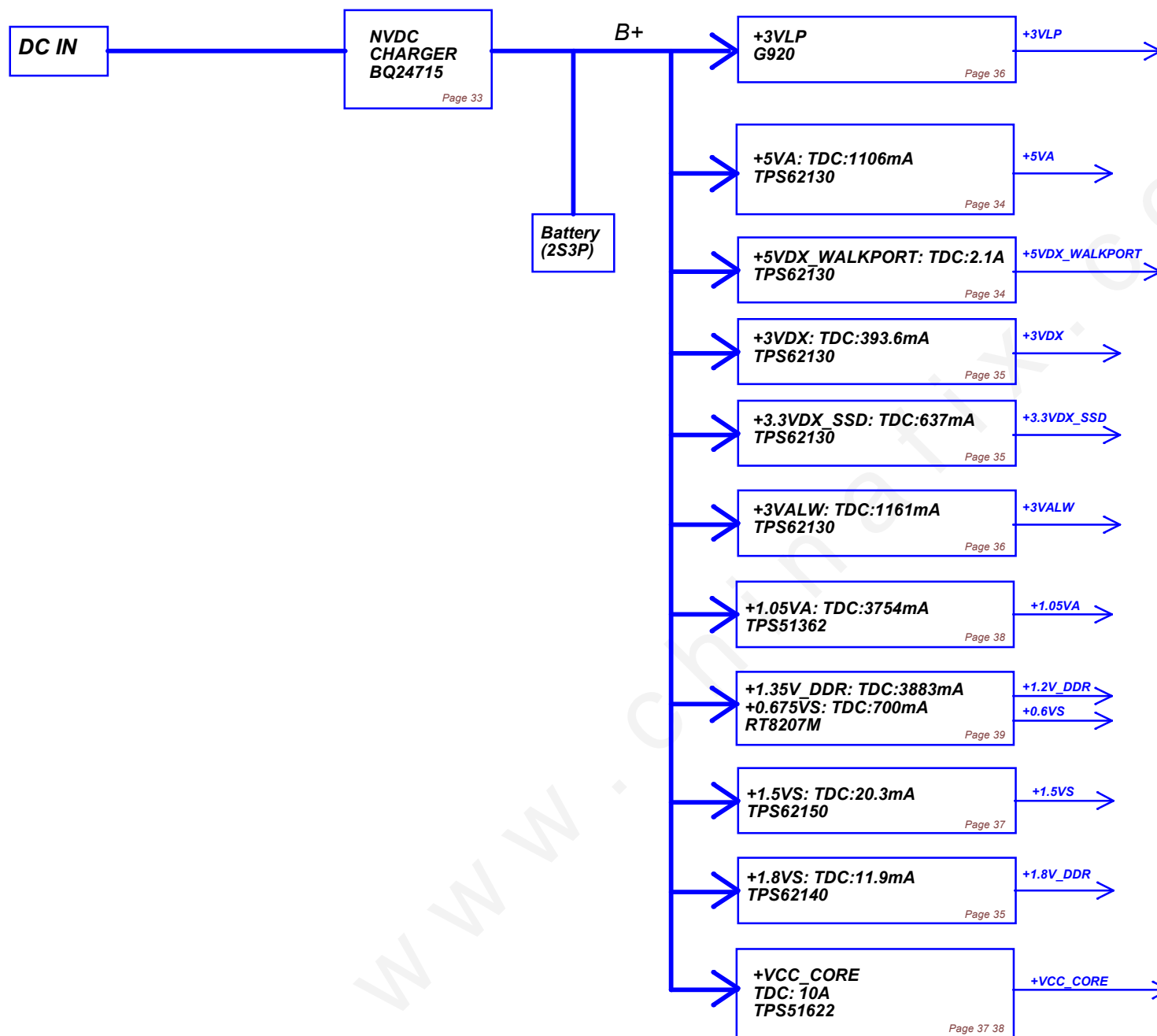
Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	<b>Compal Electronics, Inc.</b> <b>P26-SCREWH/KB/RTC</b> P26-SCREWH/KB/RTC Size Document Number <b>LA-9262P</b> LA-9262P1
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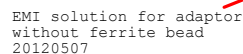
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				<b>LA-9262P</b>
			Issue	Rev
			1	1.0



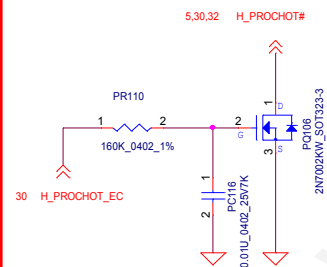
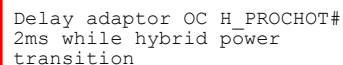
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Issued Date	Deciphered Date	2013/10/28	
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<b>Compal Electronics, Inc.</b> <b>P28-EC ENE-KB9012</b> Size: Document Number <b>LA-9262P</b> Date: Friday, April 19, 2013		Title: P28-EC ENE-KB9012 Rev: 1.0 Sheet: 30 of 45	



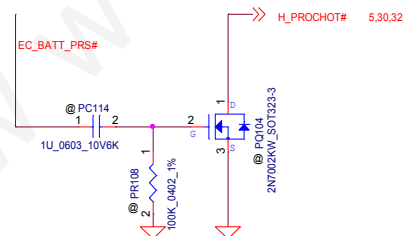
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/09/02	Deciphered Date	2013/10/28	Title	P29-PWR Block Diagram
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				Date	Rev
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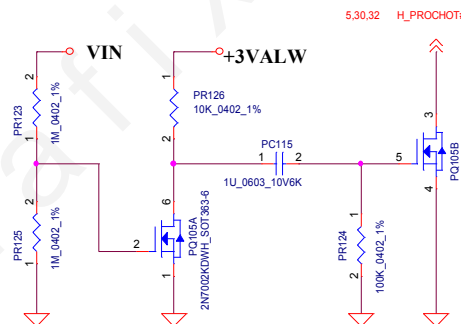
**SMART  
Battery:**  
1.GND  
2.GND  
3.BAT\_ALERT  
4.SYS\_PRES  
5.BATT\_PRS  
6.DAT\_SMB  
7.CLK\_SMB  
8.BATT++  
9.BATT++



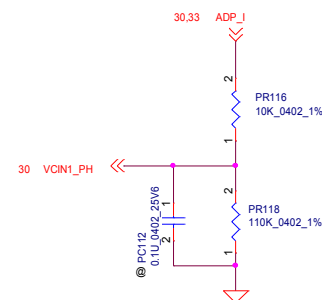
if battery removed, adaptor only,  
then trigger the H\_PROCHOT#,  
keep DNP in BOM since battery can not  
be removed by end user



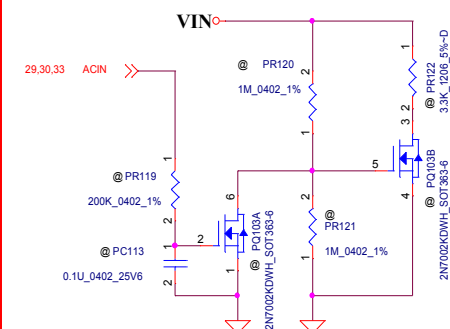
```
asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW_PROCHOT# is issued by EC
```



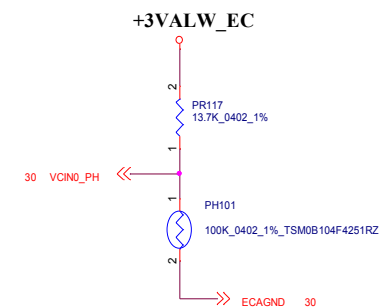
```
if CP and IPCC failed, adaptor output
=rating 100% and over load 20W
then trigger the H PROCHOT# by EC
```



keep DNP in BOM since Dell 45W  
adaptor has no hiccup mode

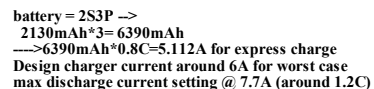


```
CPU thermal protection
@88+-3 degree C
Recovery at 80+-3 degree C
```

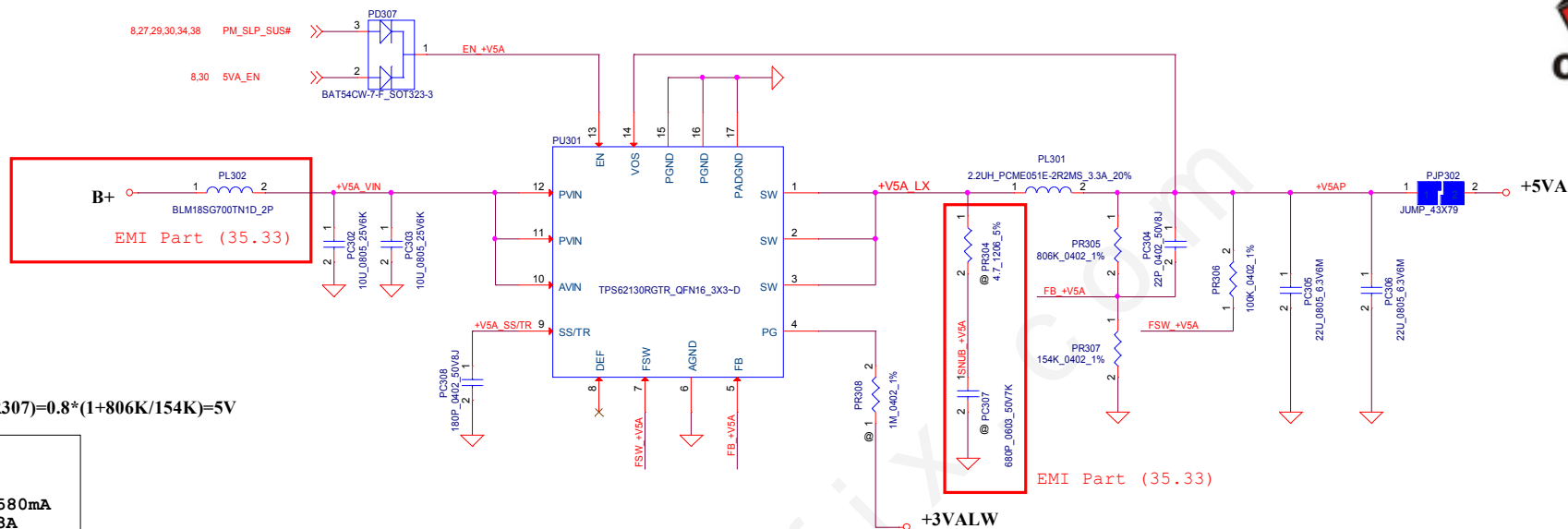


Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>P30-PWR DCIN/BATT CONN/OTP</b>	
Issued Date	2011/06/02	Deciphered Date	2013/10/28		
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				Size	Document Number
				Date:	Rev
				Friday, April 12, 2013 <b>LA-9262P</b>	1
				Sheet 32 of 45	



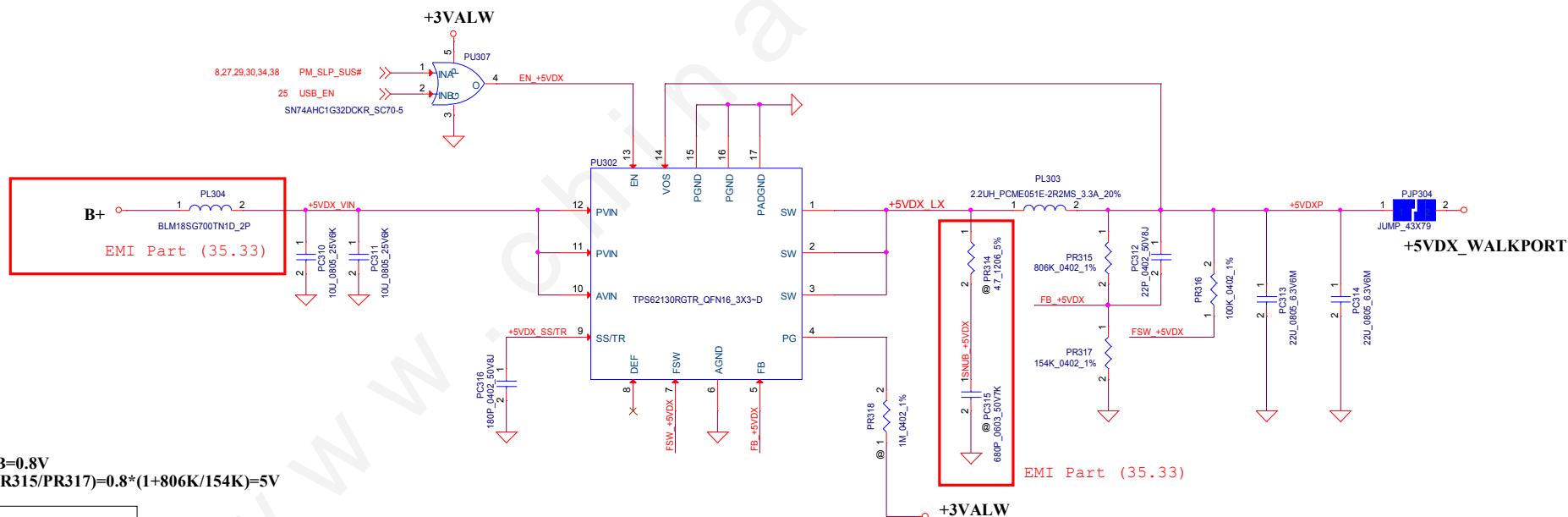


Security Classification	Compal Secret Data			<div>Compal Electronics, Inc.</div>	
Issued Date	20110602	Deciphered Date	2013/0228	<div>Title</div> <div>P31-PWR NVDC CHARGER</div>	
<div>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</div>				Size	Document Number
					LA-9262P
				Date:	Edgday 2013.09.10.2013
				Sheet	33 of 45



<V<sub>o</sub>=5V> VFB=0.8V  
V<sub>o</sub>=VFB\*(1+PR305/PR307)=0.8\*(1+806K/154K)=5V

+5VA  
TDC 1106mA  
Peak Current 1580mA  
OCP setting @ 3A

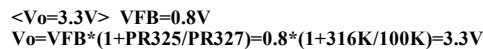


<V<sub>o</sub>=5V> VFB=0.8V  
V<sub>o</sub>=VFB\*(1+PR315/PR317)=0.8\*(1+806K/154K)=5V

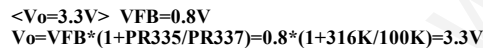
+5VDX\_WALKPORT  
TDC 2.1A  
Peak Current 3A  
OCP setting @ 3A

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/06/02				Title			
				Deciphered Date				P32-PWR +5V_VR			
				2013/10/28				LA-9262P			
								Rev			
								1.0			
								Date			
								Friday, April 19, 2013			
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								34 of 45			

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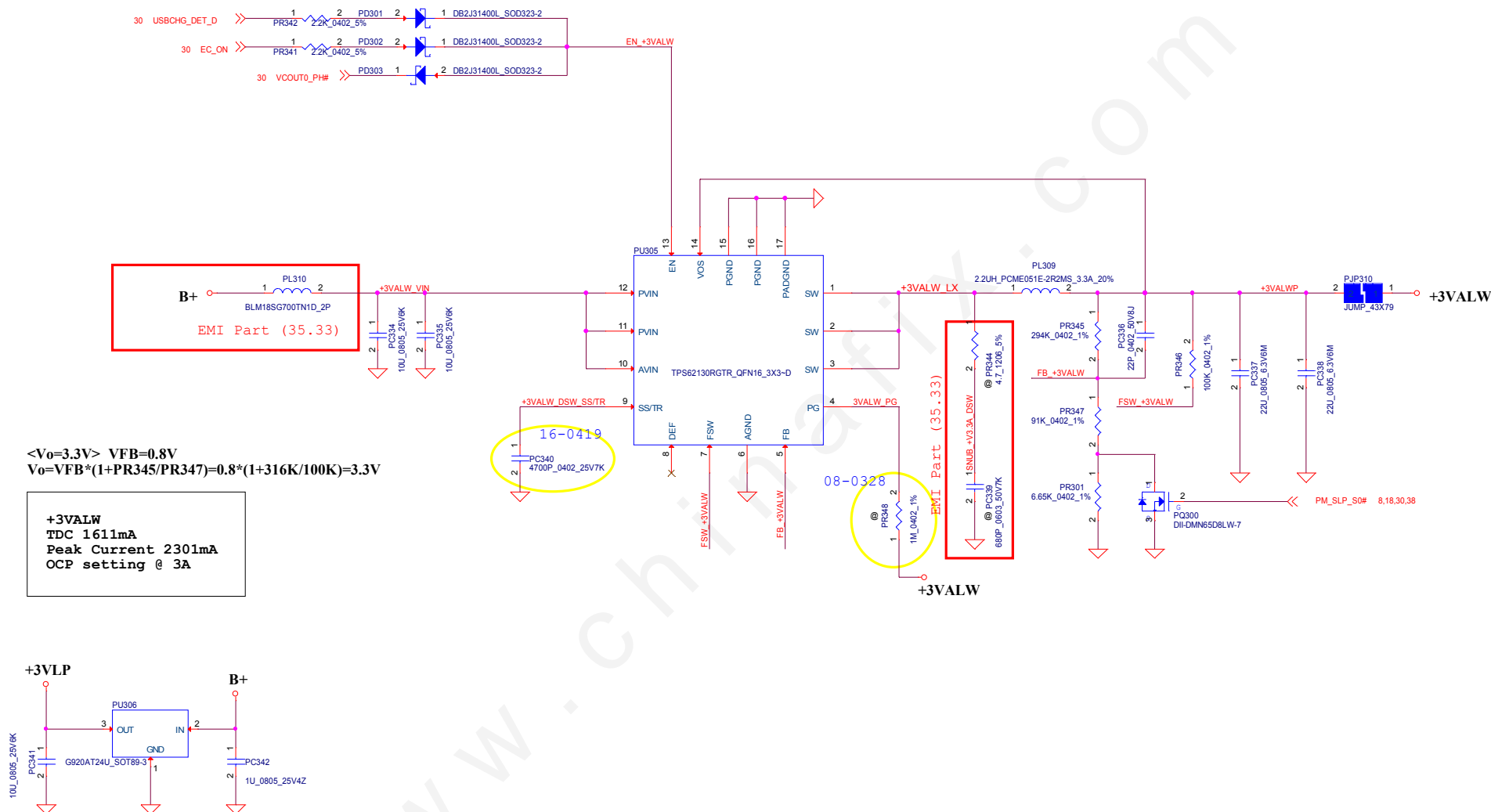


```
+3VDX
TDC 393.6mA
Peak Current 562.3mA
OCP setting @ 3A
```



```
+3.3VDX SSD
TDC 637mA
Peak Current 910mA
OCP setting @ 3A
```

Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title <b>P33-PWR +3.3V VR(1/2)</b>		
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					<b>LA-9262P</b>	1.
Date: Friday, April 19, 2013				Sheet	35	of 45



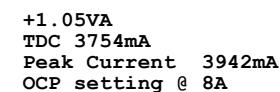
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<b>P34-PWR +3.3V VR(2/2)</b>
				Size Document Number
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+1.5VS  
TDC 20.3mA  
Peak Current 30.5mA  
OCP setting @ 1A



+1.8VS  
TDC 11.9mA  
Peak Current 17mA  
OCP setting @ 2A

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>P35-PWR +1.5VS/+1.8V_DDR</b>	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title <b>P36-PWR +1.05VS</b>		
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EMI Part (35.33)



**1.35V for DDR3L**  
**VFB = 0.75V**  
 **$V_o = 0.75(1 + PR608/PR610) = 0.75(1 + 8.2/10) = 1.35V$**

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>P37-PWR +1.35V DDR+0.675VS</b>		
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title		
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				<b>LA-9262P</b>		
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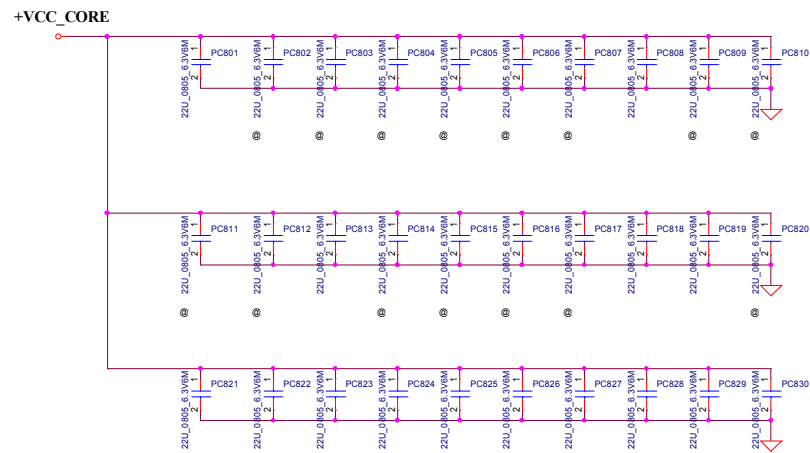
VCCSENSE and VSSSENSE  
have been already pull-high to +VCC\_CORE and GND  
by 100-OHM in HW side, P10 and P11

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>P38-PWR CPU CORE</b>	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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for VCORE:2 phase ---> reserved 30pcs, 15-pcs is OK after fine-tune



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						Size	Document Number		Rev
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
X	XX	XXX	XX'XX/XX	Compal_XX	XXXXXX	Change PRXX from Xohm to XXKohm.	
36			20121008	Compal_Power	create one more input cap for TPS51362 Vin	add PC513_10U_0805_16V6K for TPS51362's input	
34			20121012	Compal_HW	create one more resistor for TPS62130 enable pin	add PR342_2.2K_0402_5%	
34			20121018	Compal_Power	design change, delete PU301-PU305, TPS62130 and related components, create PU301, TPS51225 for 3.3V and 5V power rails		
35							
36							
36			20121018	Compal_Power	design change, delete PU401, PU402, TPS62140 and TPS62150 and related components, create PU401and PU402, SY8003D for 1.5V and 1.8V power rails		
34			20121023	dell	reject power design change of 3.3V, 5V, 1.8V and 1.5V		
35							
36							
38			20121203	Compal_EMI	change PL501 for EMI and layout routing	change from SUPPRE_FBMA-L11-453215-800LMA90T_1812 to HCB2012KF-121T50_0805	
39			20121203	Compal_EMI	change PL601 for EMI and layout routing	change from SUPPRE_FBMA-L11-453215-800LMA90T_1812 to HCB2012KF-121T50_0805	
40			20121203	Compal_EMI	add PL703 for EMI	add PL701 HCB2012KF-121T50_0805	
38			20121203	Compal_Power	create PR509 0_0402_5% for debug	add PR509 0_0402_5%	
32			20121205	Compal_HW	create PR5107 10K_0402_1% for test	add PR107 10K_0402_1%	
40			20121213	Compal_Power	fine tune VR transient	de-pop PC714, change PR711 from 150K to be 100K	
40			20130122	Compal_Power	follow Intel's recommendation	change PR737 from 110 OHM to be 130 OHM	
33			20130131	Compal_RF	reserved a MLCC for RF consideration	create PC206 2200P_0402_50V7K	
40			20130221	Compal_RF	for RF noise reducing	pop PC703, PR719 and PC712, PR734 and PC722 for VCORE	
39			20130221	Compal_RF	for RF noise reducing	pop PR605 and PC613 for DDR	

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				Size	Document Number	Rev
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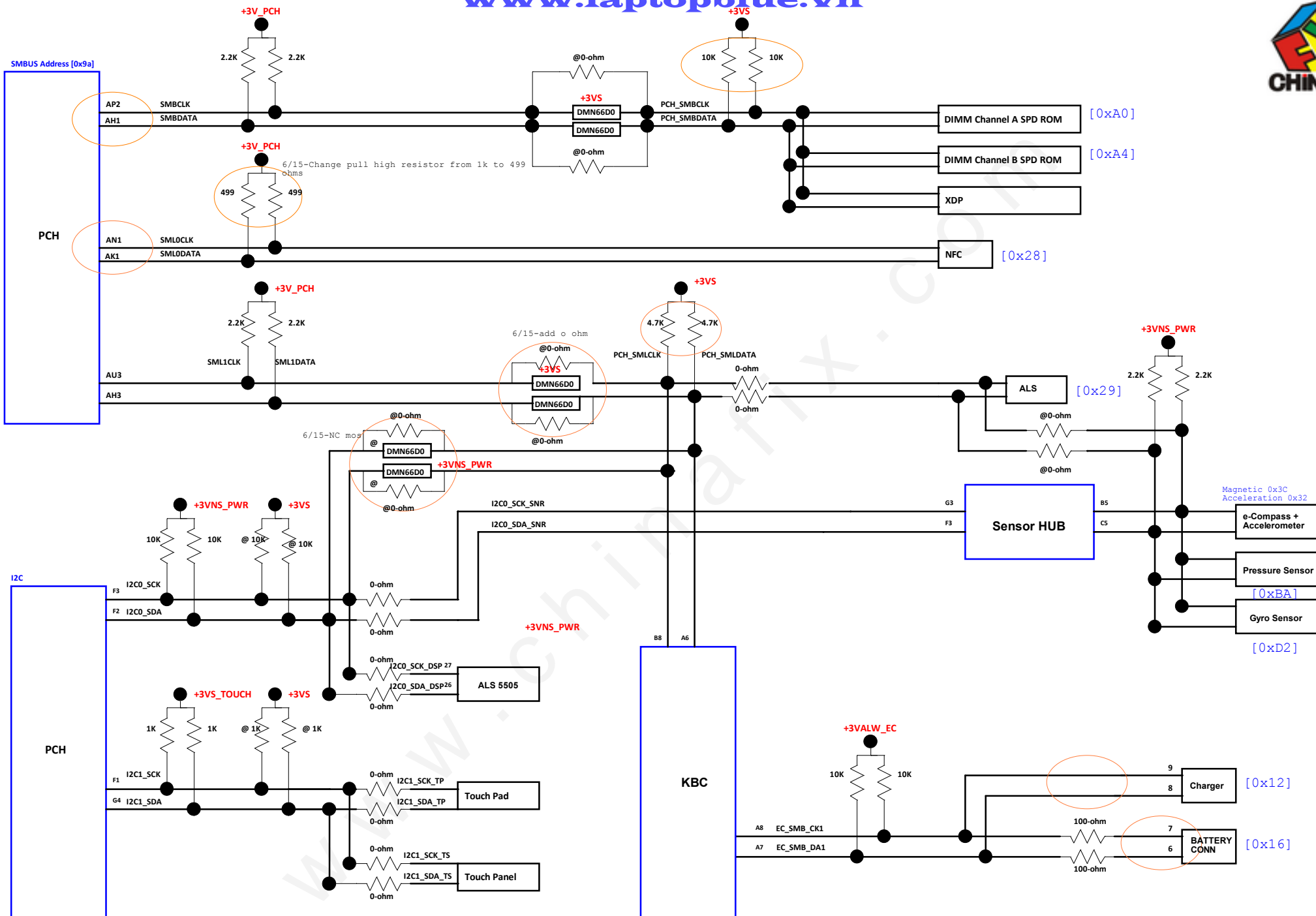


Version Change List ( P. I. R. List )

Page 2

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description
X	XX	XXX	XX'XX/XX	Compal_XX	XXXXX	Change PRXX from Xohm to XXKohm.

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Issued Date		2011/06/02	Deciphered Date	2013/10/28	Title	
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## Discrete Power On Sequence



[AC in]

[Battery only, AC absent]

EC pay attention timing

[AC in]

[Battery only, AC absent]

ITEM	Measure Point	Time
Ta	VIN	To
Tb	VIN	To
Tc	B+	To
Td	+3VLP	To
Te	EC_ON	To
Tf	+3VALW (+3V_PCH_DSW)	To
Tg	5VA_EN (PCH_DPWRK)	To
Th	5VA	To
	PBTN_SW#	Low pulse width

ITEM	Measure Point	Time
	To	
Tc	B+	To
Th	+3VLP	To
Td	PBTN_SW#	Low pulse width
Te	EC_ON	To
Tf	+3VALW	To
Tg	PCH_DPWRK	To
	+5VA	To

ITEM	Measure Point	Time
T1	PM_SLP_SUS#	To
T2	PM_SLP_SUS#	To
T3	PM_SLP_SUS#	To
T4	PM_SLP_SUS#	To
T5	PM_SLP_SUS#	To
T6	PCH_RSMRST#	To
T7	PCH_RSMRST#	To
T8	PCH_RSMRST#	To
T9	PBTN_OUT#	To
T10	PCH_RSMRST#	To
T11	SUSCLK	To
T12	PM_SLP_S5#	To
T13	PM_SLP_S4#	To
T14	PM_SLP_S4#	To
T15	+1.35V_DDR	To
T16	+1.35V_DDR	To
T17	PM_SLP_S4#	To
T18	PM_SLP_S4#	To
T19	PM_SLP_S3#	To
T20	PM_SLP_S3#	To
T21	PM_SLP_S3#	To
T22	PM_SLP_S3#	To
T23	PM_SLP_S3#	To
T24	+1.8VS	To
T25	PM_SLP_S3#	To
T26	+1.8VS	To
T27	PM_SLP_S3#	To
T28	+1.05VS	To
T29	MPHY_PWREN	To
T30	MPHY_PWREN	To
T31	ALL_VS_PG	To
T32	HMPG	To
T33	1.05VS_PG	To
T34	1.05VS_VCCST_PG	To
T35	VR_ON	To
T36	+VCC_CORE	To
T37	PCH_PWROK	To
T38	SM_PG_CTRL	To
T39	HMPG	To
T40	PCH_PWROK_EC	To
T41	SYS_PWROK	To
T42	HMPG	To

