

## PCB STACK UP

LAYER 1 : TOP  
 LAYER 2 : GND  
 LAYER 3 : IN1  
 LAYER 4 : SVCC  
 LAYER 5 : IN2  
 LAYER 6 : IN3  
 LAYER 7 : GND  
 LAYER 8 : BOT

## BD9 FT3 Kabini Block Diagram

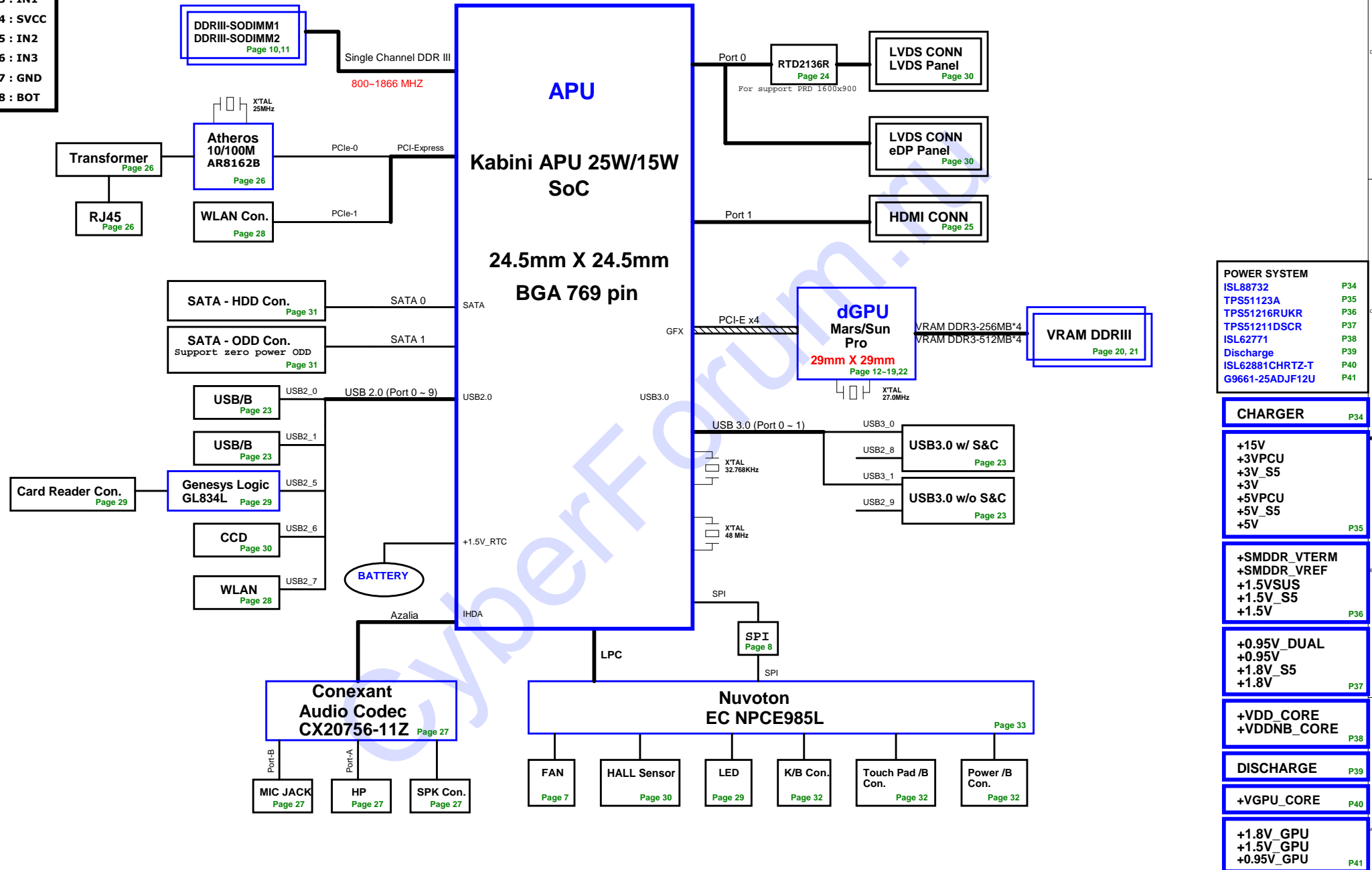





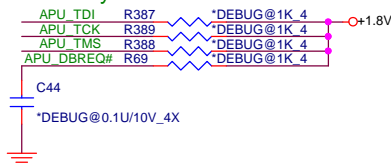


Table of Contents

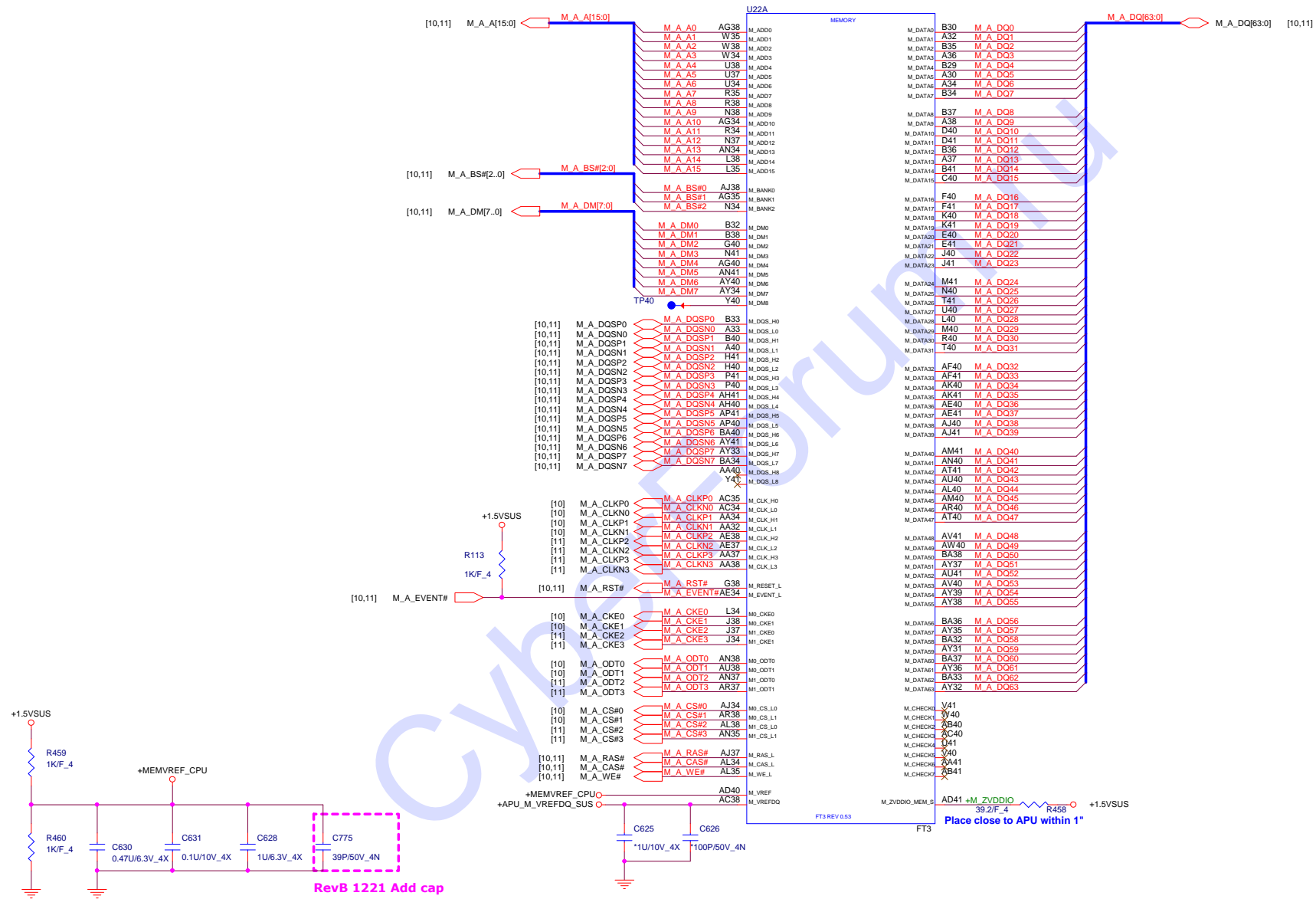
PAGE	DESCRIPTION	BOI-FUNCTION
1	Schematic Block Diagram	
2	Power Stage	
3 - 8	Processor	CPU
9	Straps	CPU
10	SO-DIMM 1	DDR
11	SO-DIMM 2	DDR
12 - 19	Mars/Sun Pro(M2)	VGA
20 - 21	VRAM - DDR3	VGA
22	PX5	VGA
23	USB	U3B/USB
24	eDP to LVDS(RTD2136R)	LDS
25	HDMI/Touch Screen	HDM/TSN
26	LAN(1A8162B)	LAN
27	Codec (CX20756-11Z)	ADO
28	MINI CARD (WLAN)	MNW
29	CARD READER(GL834L)/LED	MMC/LED
30	LDS/CRT/CCD	LDS/CRT/CCD
31	HDD/ODD	HDD/ODD
32	KB/TouchPad	KBC/TPD
33	EC 985L	KBC
34	Charger (ISL88731CHRTZ-T)	CHR
35	System 5V/3V	PWM
36	DDR 1.5V	PWM
37	+0.95V_DUAL	PWM
38	+VCC_CORE	PWM
39	Discharge	PWM
40	GPU_CORE	PWM
41	+0.95V_GPU/+1.8V_GPU/+1.5V_GPU/+3V_GPU	PWM

GND PLANE	PAGE
 GND_SIGNAL	
 8769GND	
	
 GND	ALL
 ADOGND	

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+1.5V		S0~S5
+3V	+3.3V	MAIND	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3VPCU	+3.3V	AC/DC Insert enable	S0~S5
+5V	+5V	MAIND	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+WIMAX_P	+3.3V	IOAC_EN	S0
+1.5VSUS	+1.5V	SUSON	S0~S3
+1.5V	+1.5V	MAIND	S0
+1.8V_S5	+1.8V	PE_PWRGD ^ PE_GPIO1	S0~S5
+0.95V_DUAL	+0.95V	+0.95V_DUAL_EN	S0~S5
+0.95V	+0.95V	MAIND	S0
+VDD_CORE	~	VRON	S0
+VDDNB_CORE	~	VRON	S0
+VGPU_CORE		GPU_MAINON ^ PE_GPIO1	S0
+1.8V_GPU	+1.8V	GPU_MAIND	S0
+0.95V_GPU	+0.95V	GPU_MAINON ^ PE_GPIO1	S0
+3V_GPU	+3.3V	GPU_MAIND	S0
+1.5V_GPU	+1.5V	GPU_MAIND	S0



**RevB 1221 Add 0 ohm for debug**



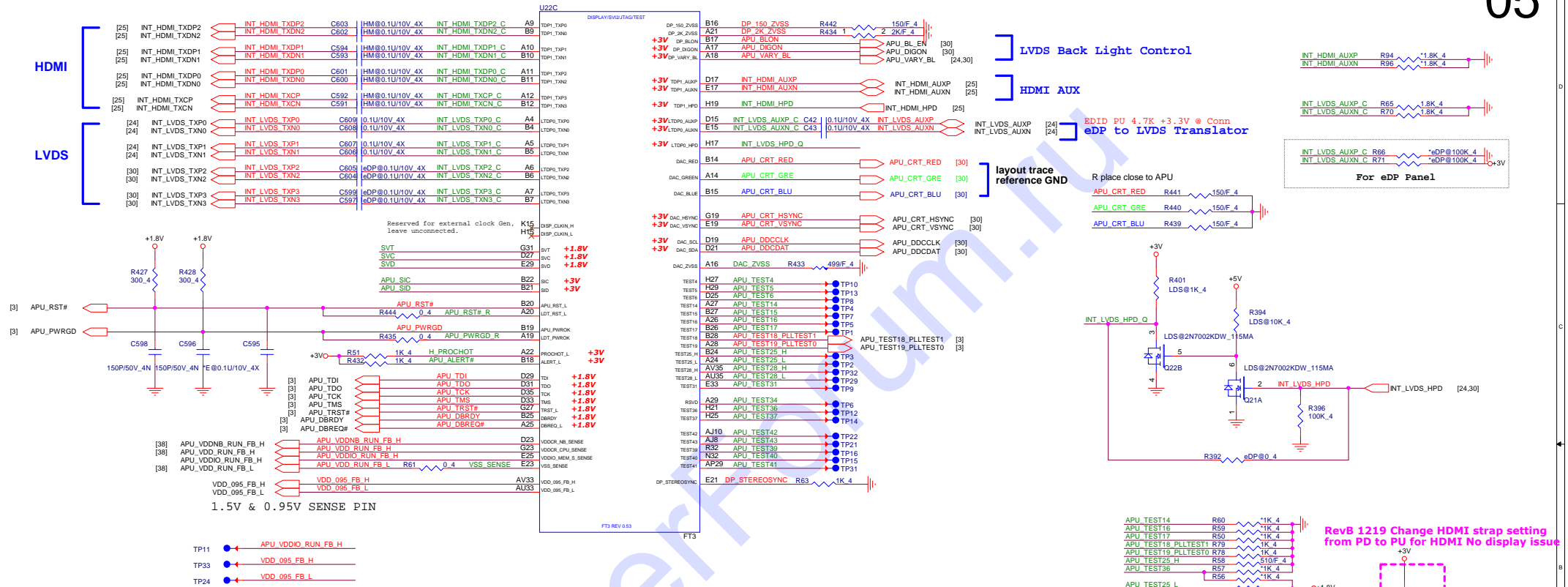
Quanta Computer Inc.

PROJECT : BD9

Size	Document Number	Rev
	APU 2/6(DDR3 MEM)	A1A
Date:	Tuesday, December 25, 2012	Sheet 4 of 41

HDMI

LVDS



LVDS Back Light Control

HDMI AUX

layout trace reference GND

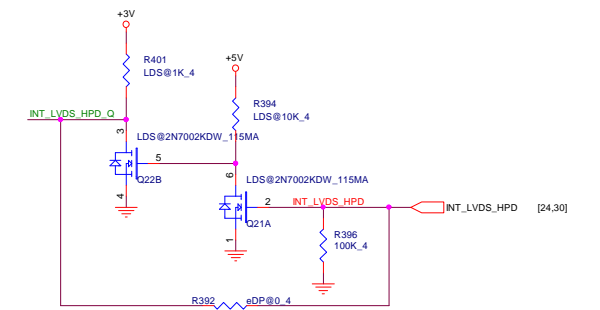
eDP to LVDS Translator

INT\_HDMI\_AUXP

INT\_LVDS\_AUXP C

INT\_LVDS\_AUXN C

For eDP Panel

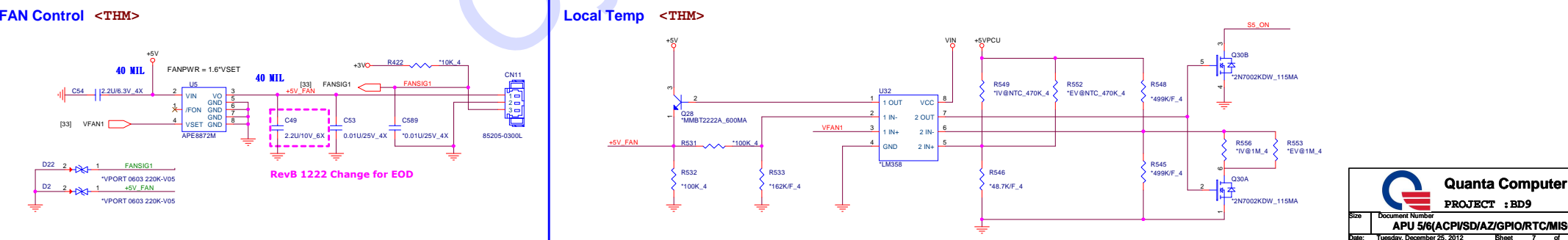
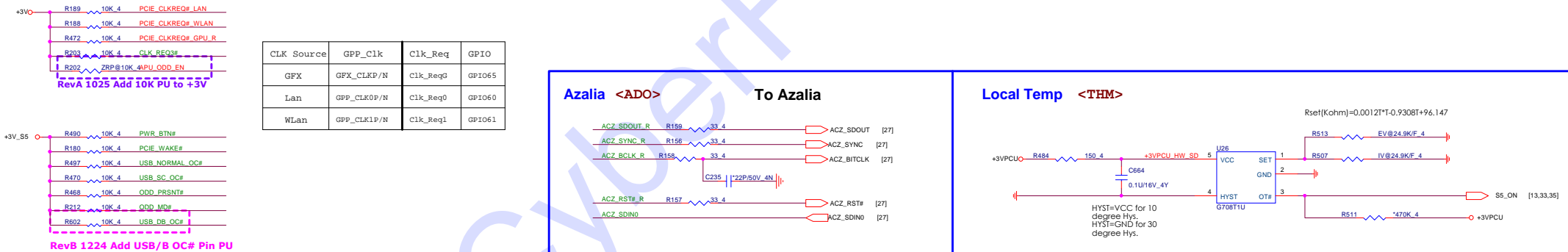


RevB 1219 Change HDMI strap setting from PD to PU for HDMI No display issue

Note:  
To override VID, Remove Rd, Re, Rf, Rg, install Rc  
set VID via SVC & SVD option RES Ra, Rb

SVC	SVD	BOOT VOLTAGE
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8







## SATA HDD

[31] SATA\_TXP0  
[31] SATA\_TXN0  
[31] SATA\_RXN0  
[31] SATA\_RXP0

## SATA ODD

[31] SATA\_TXP1  
[31] SATA\_TXN1  
[31] SATA\_RXN1  
[31] SATA\_RXP1

+0.95V  
R170 1K/F 4  
R169 1K/F 4  
SATA\_CALRN  
SATA\_CALRP

TP41 SATA\_LED# BA30  
SATA\_ACT\_LSPROST +3V

Integrated Clock Mode:  
Leave unconnected.

BA12  
SATA\_X2

INT\_CLK\_PCIE\_VGAP  
INT\_CLK\_PCIE\_VGAPN

INT\_CLK\_PCIE\_LAMP  
INT\_CLK\_PCIE\_LAMPN

INT\_CLK\_PCIE\_WLAMP  
INT\_CLK\_PCIE\_WLAMPN

Integrated Clock Mode:  
Leave unconnected.

Cardreader pass through PCIE  
Leave unconnected.

48M\_X1  
N2

48M\_X2  
N1

15P50V\_4C  
R178 0.4  
R164 22.4  
R172 22.4  
R167 22.4

LPC\_CLK0 R AY2  
LPC\_CLK1 R AV2

LAD0 +3V\_SS  
LAD1 +3V\_SS  
LAD2 +3V\_SS  
LAD3 +3V\_SS

LFRAME# +3V\_SS  
LAD0 +3V\_SS  
LAD1 +3V\_SS  
LAD2 +3V\_SS  
LAD3 +3V\_SS

SEIRIO +3V\_SS  
CLKRUN# +3V\_SS  
LPCPD# +3V\_SS

+3V\_SS R485 10K\_4

TP25

TP26

TP27

TP28

TP29

TP30

TP31

TP32

TP33

TP34

TP35

TP36

TP37

TP38

TP39

TP40

TP41

TP42

TP43

TP44

TP45

TP46

TP47

TP48

TP49

TP50

TP51

TP52

TP53

TP54

TP55

TP56

TP57

TP58

TP59

TP60

TP61

TP62

TP63

TP64

TP65

TP66

TP67

TP68

TP69

TP70

TP71

TP72

TP73

TP74

TP75

TP76

TP77

TP78

TP79

TP80

TP81

TP82

TP83

TP84

TP85

TP86

TP87

TP88

TP89

TP90

TP91

TP92

TP93

TP94

TP95

TP96

TP97

TP98

TP99

TP100

TP101

TP102

TP103

TP104

TP105

TP106

TP107

TP108

TP109

TP110

TP111

TP112

TP113

TP114

TP115

TP116

TP117

TP118

TP119

TP120

TP121

TP122

TP123

TP124

TP125

TP126

TP127

TP128

TP129

TP130

TP131

TP132

TP133

TP134

TP135

TP136

TP137

TP138

TP139

TP140

TP141

TP142

TP143

TP144

TP145

TP146

TP147

TP148

TP149

TP150

TP151

TP152

TP153

TP154

TP155

TP156

TP157

TP158

TP159

TP160

TP161

TP162

TP163

TP164

TP165

TP166

TP167

TP168

TP169

TP170

TP171

TP172

TP173

TP174

TP175

TP176

TP177

TP178

TP179

TP180

TP181

TP182

TP183

TP184

TP185

TP186

TP187

TP188

TP189

TP190

TP191

TP192

TP193

TP194

TP195

TP196

TP197

TP198

TP199

TP200

TP201

TP202

TP203

TP204

TP205

TP206

TP207

TP208

TP209

TP210

TP211

TP212

TP213

TP214

TP215

TP216

TP217

TP218

TP219

TP220

TP221

TP222

TP223

TP224

TP225

TP226

TP227

TP228

TP229

TP230

TP231

TP232

TP233

TP234

TP235

TP236

TP237

TP238

TP239

TP240

TP241

TP242

TP243

TP244

TP245

TP246

TP247

TP248

TP249

TP250

TP251

TP252

TP253

TP254

TP255

TP256

TP257

TP258

TP259

TP260

TP261

TP262

TP263

TP264

TP265

TP266

TP267

TP268

TP269

TP270

TP271

TP272

TP273

TP274

TP275

TP276

TP277

TP278

TP279

TP280

TP281

TP282

TP283

TP284

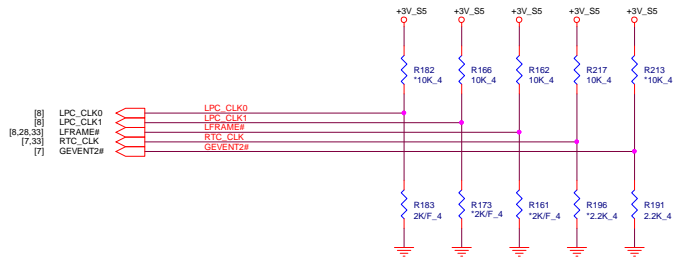
TP285

TP286



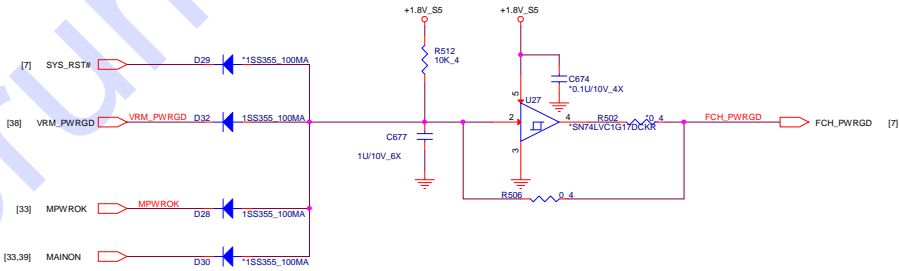
STRAPS PINS

09



REQUIRED STRAPS

	LPC_CLK0	LPC_CLK1	LFRAME#	RTC_CLK	GEVENT2#
PULL HIGH	BOOT Fail Timer ENABLE	Internal CLKGEN ENABLE DEFAULT	SPI ROM DEFAULT	Normal Power Timing ENABLE DEFAULT	SPI Voltage 1.8V DEFAULT
PULL LOW	BOOT Fail Timer DISABLE DEFAULT	Internal CLKGEN DISABLE	LPC ROM	Normal Power Timing DISABLE	SPI Voltage 3.3V DEFAULT

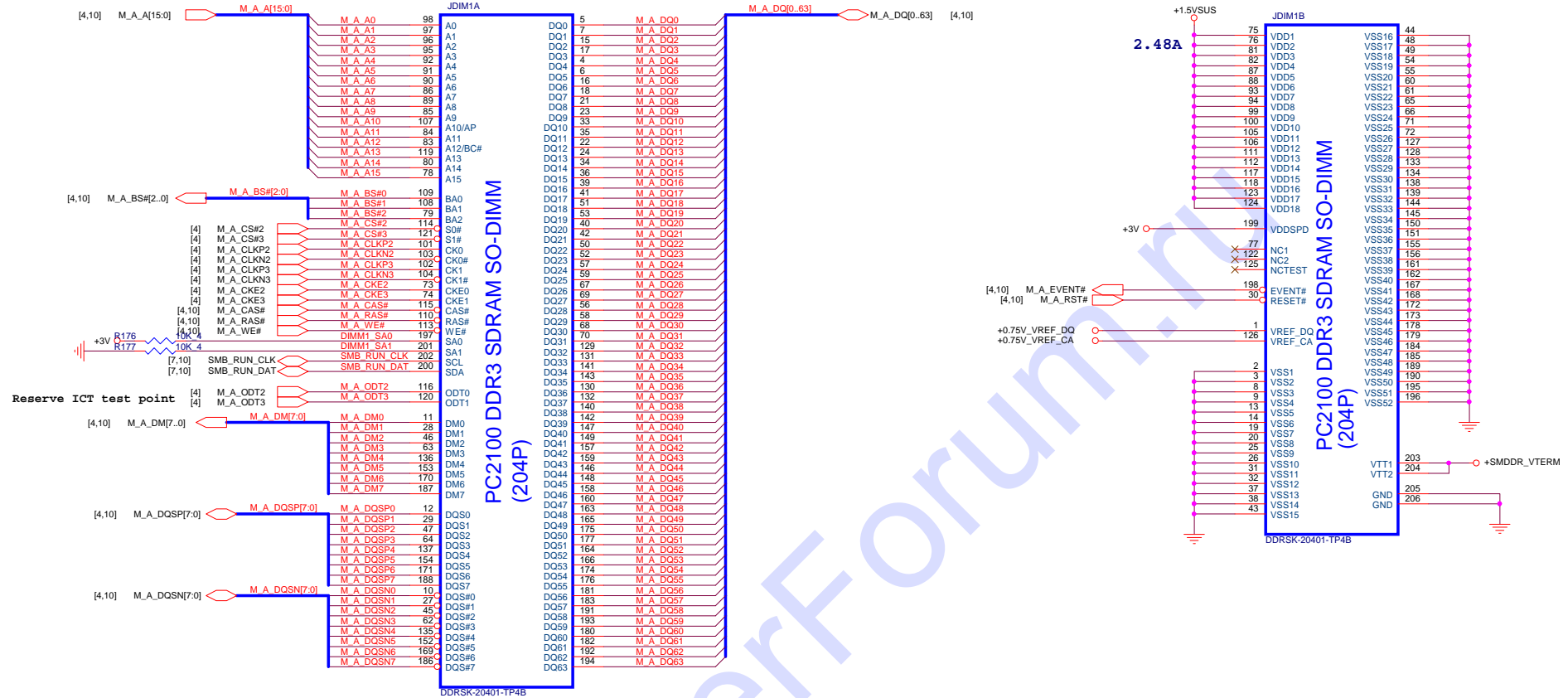


PWRGD CIRCUIT

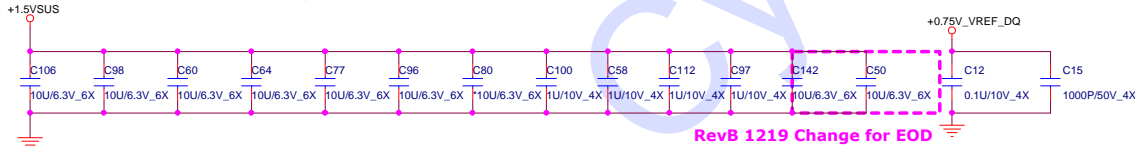


# DDR\_STD(DDR)

11

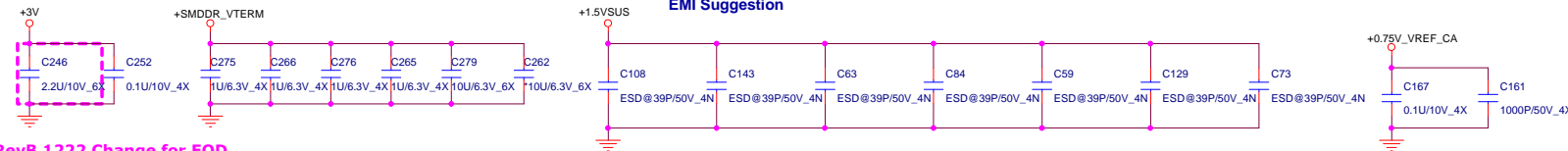


Place these Caps near So-Dimm0.



RevB 1219 Change for EOD

EMI Suggestion



Quanta Computer Inc.

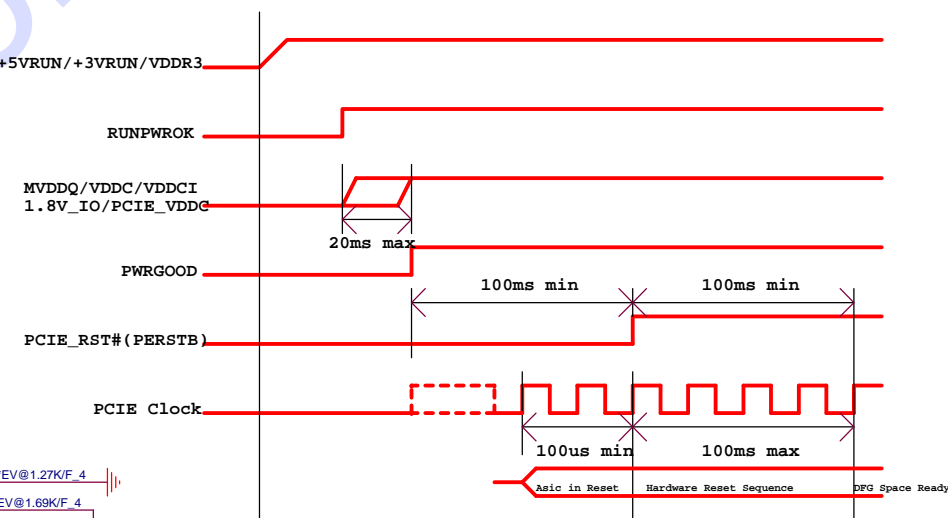
PROJECT : BD9

Size	Document Number	Rev
	DDR3 DIMM-1	A1A
Date:	Tuesday, December 25, 2012	Sheet 11 of 41



1 => +3V\_GPU  
2 => +VDDC,+VDDCI,+1.5V\_GPU,+0.95V\_GPU  
3 => +1.8V\_GPU

Intel platform: Lane0 ~ Lane15  
Brazos platform: Lane12 ~ Lane15  
Comal and Sabine platform: Lane8 ~Lane15  
Richland and Kabini platform: Lane0 ~ Lane7

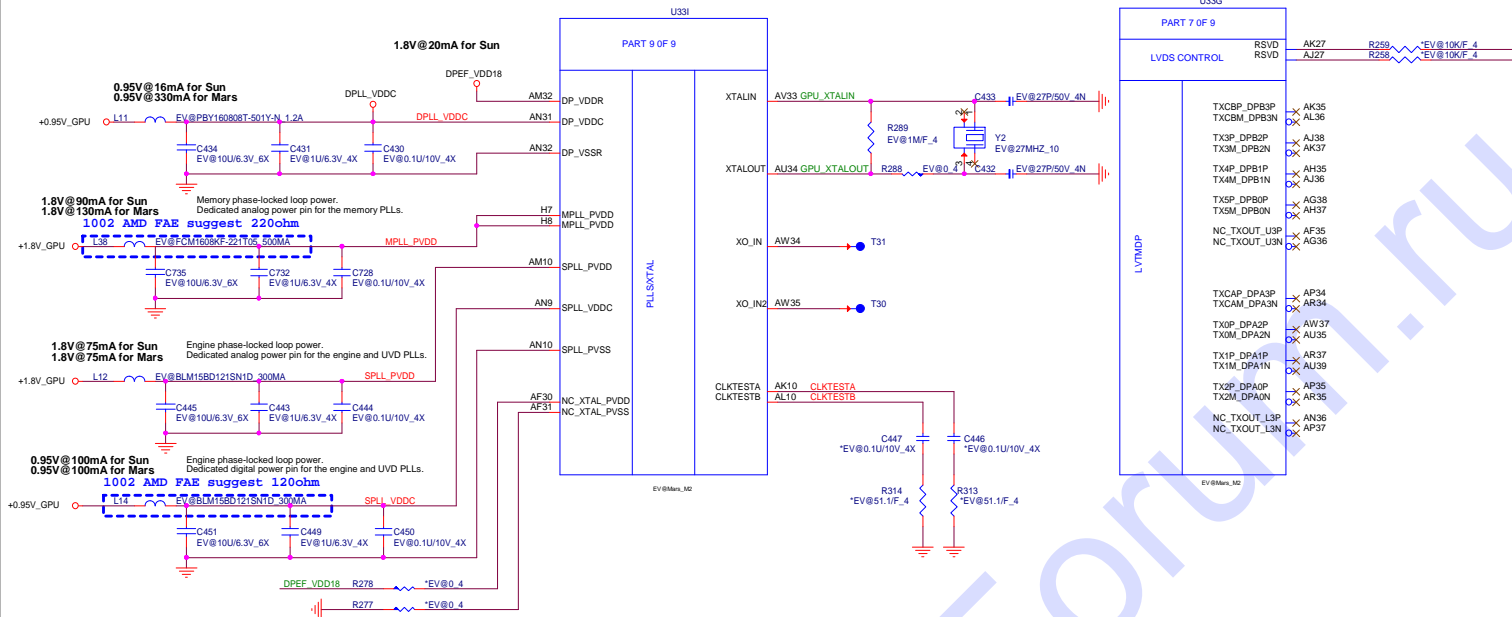
+5V<sub>RIN</sub> / +3V<sub>RIN</sub> / VDD<sub>R3</sub>

**Quanta Computer Inc.**  
**PROJECT : BD9**

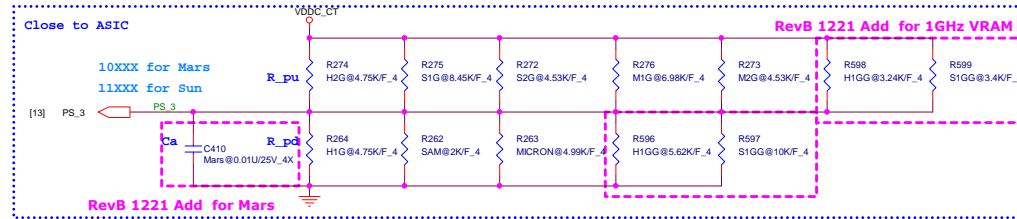
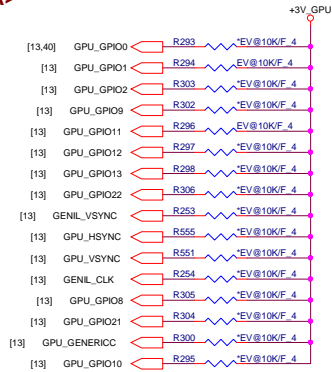
Size	Document Number	Rev
	<b>Mars_M2/ PEG*8</b>	A1
Date:	Tuesday, December 25, 2012	Sheet 12 of 41



DPE/DPF/LVDS



## &lt;VGA&gt;



## MLPS

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

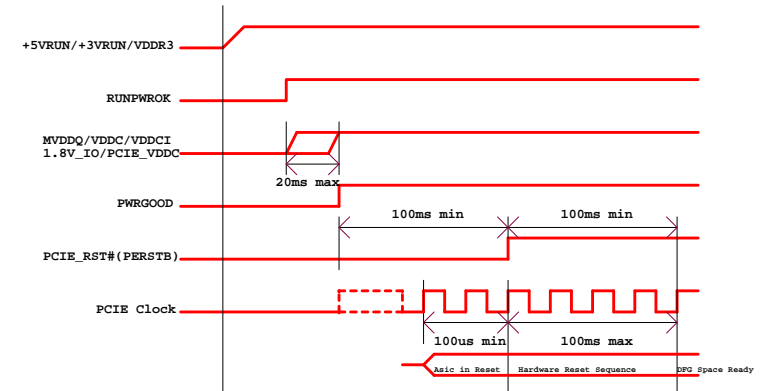
## DDR3 Memory TYPE

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

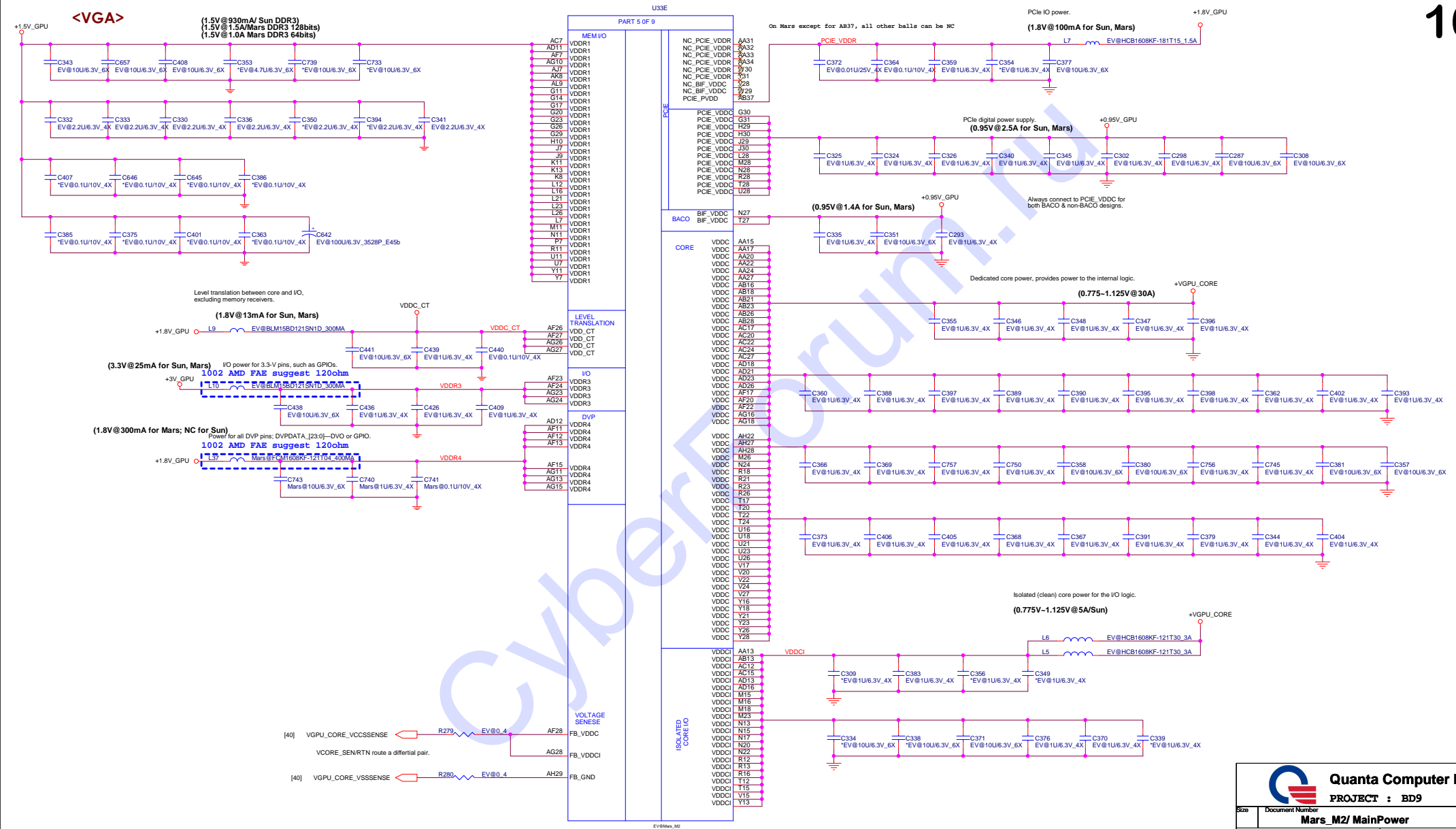
Vendor	Vendor P/N	B/S P/N (QC1 P/N)	Size	MLPS
Hynix	H5TQ2G63DFR-11C (128M*16)	AKD5MGWTW16 * 4	1GB	000
	H5TC4G63AFR-11C (256M*16)	AKD5PGWTW05 * 4	2GB	111
Micron	MT41J128M16JT-107G:K (128M*16)	AKD5DGSTL00 * 4	1GB	011
	MT41K256M16HA-107G:E (256M*16)	AKD5PGSTL00 * 4	2GB	100
Samsung	K4W2G1646E-BC11 (128M*16)		1GB	001
	K4W4G1646B-HC11 (256M*16)		2GB	010

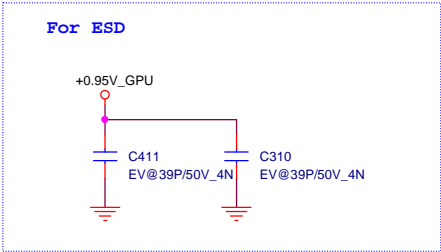
CONFIGURATION STRAPS -- SEE EACH DATABASE FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	0
STRAP_TX_CFG_DRV_FULL_SWING	PS_1[4]		Control the transmitter full-half swing mode 0: 50% Tx output swing 1: Full Tx output swing	1
STRAP_TX_DEEMPH_EN	PS_1[5]		PCIe transmitter, de-emphasis enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
STRAP_BIF_GEN3_EN_A	PS_1[1]		PCIe GEN3 Capability 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	0 for Kabini
STRAP_BIF_VGA_DIS	PS_2[4]		VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space) 0: VGA controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
ROM_CONFIG[2:0]	PS_0[3..1]		Serial ROM type or Memory Aperture Size Select  If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
STRAP_BIOS_ROM_EN	PS_2[3]		Enable external BIOS ROM device 0: Disabled 1: Enabled	0
AUD[1] AUD[6]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
N/A	PS_0[4]		Reserved for internal use only. Must be 1 at reset	1
N/A	PS_1[3]	GENLK_CLK	Reserved	0
STRAP_BIF_CLK_PM_EN	PS_1[2]	GPIO8	PCIe reference clock power management capability is reported in the PCI 0: The CLKREQ power management capability is disabled 1: The CLKREQ power management capability is enabled	0
RESERVED RESERVED	NA NA	GPIO21 GENERICC	Reserved Reserved (for Thames/Whistler/Seymour only)	0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

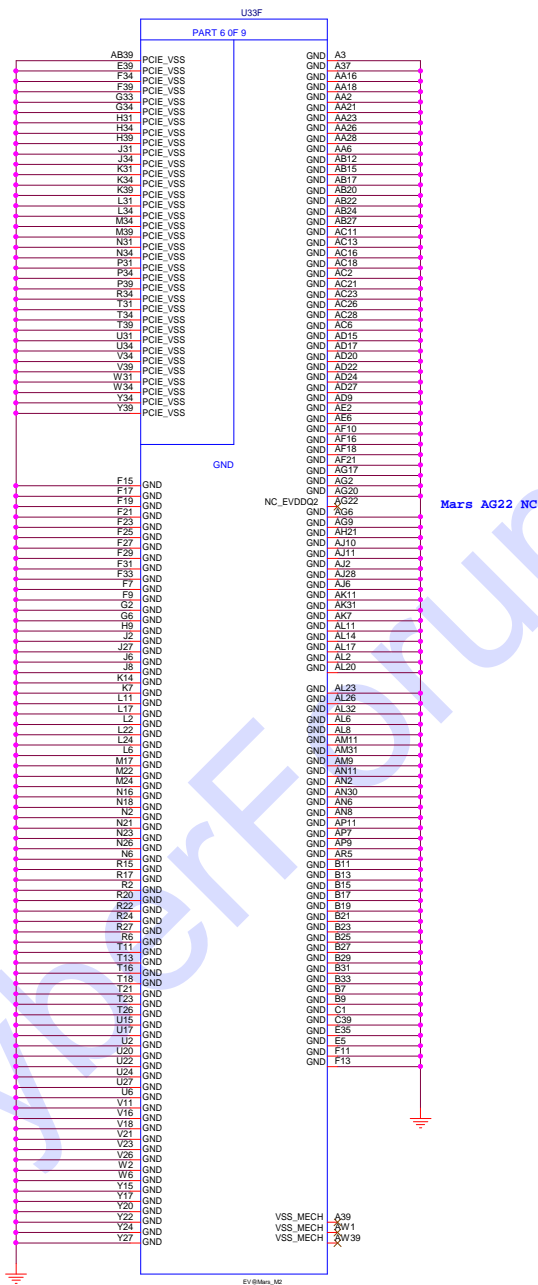
## Power Up Reset Sequence

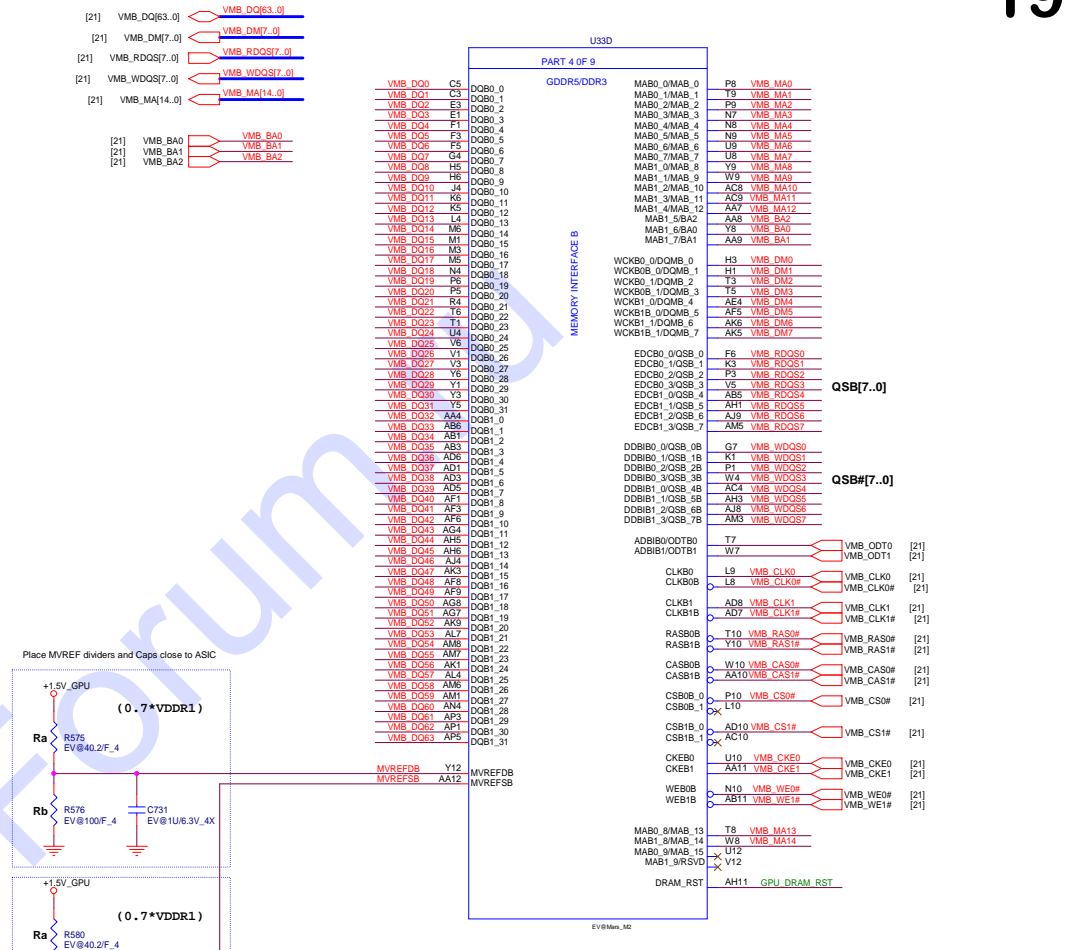
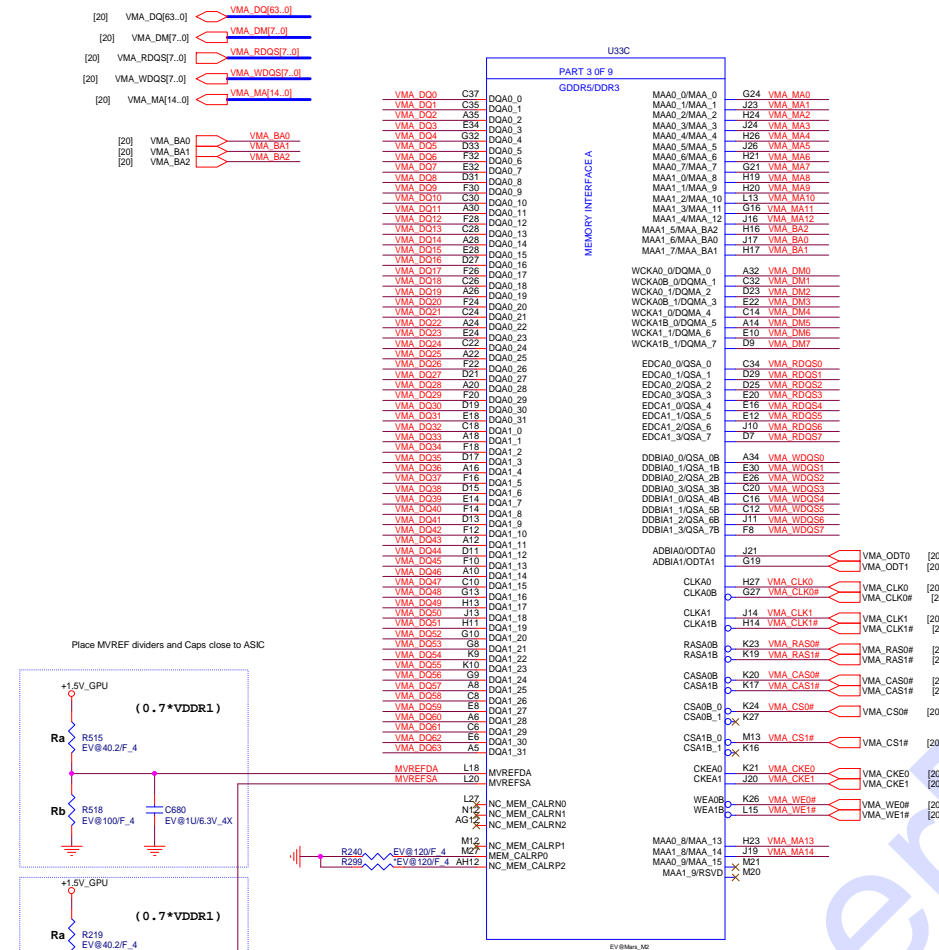




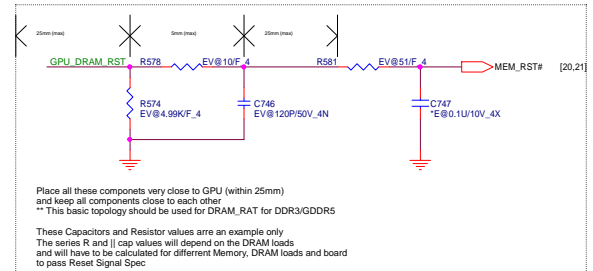




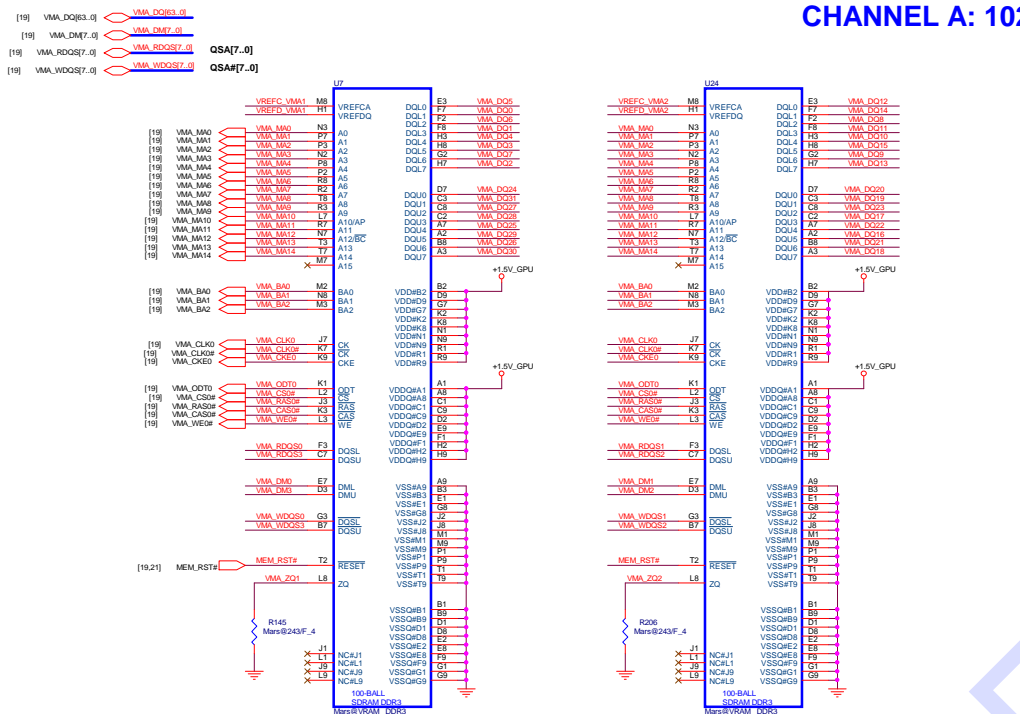


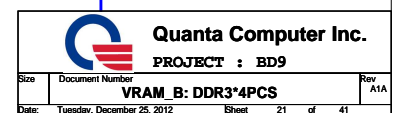


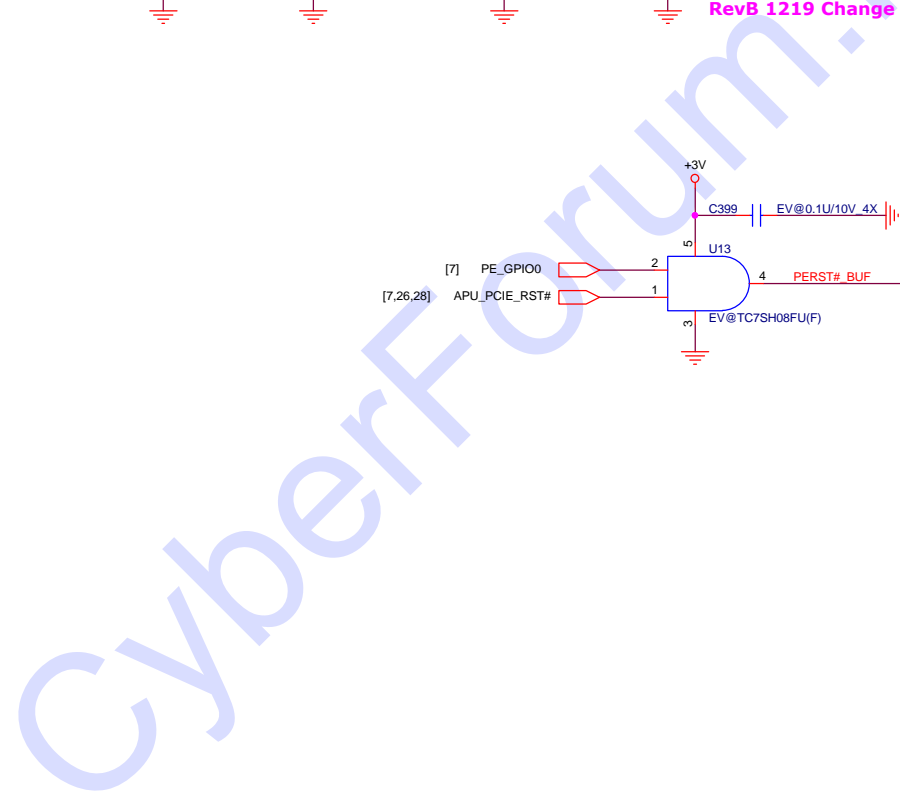
Ball Name	Thames	Seymour	Mars
MEM_CALRN0	243R	X	X
MEM_CALRN1	X	243R	X
MEM_CALRN2	243R	X	X
MEM_CALRP0	243R	X	120R
MEM_CALRP1	X	243R	X
MEM_CALRP2	243R	X	X



## CHANNEL A: 1024MB DDR3 (128M\*16\*4pcs) &lt;VGA&gt;









<USB> <U3B>

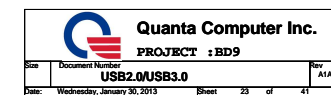


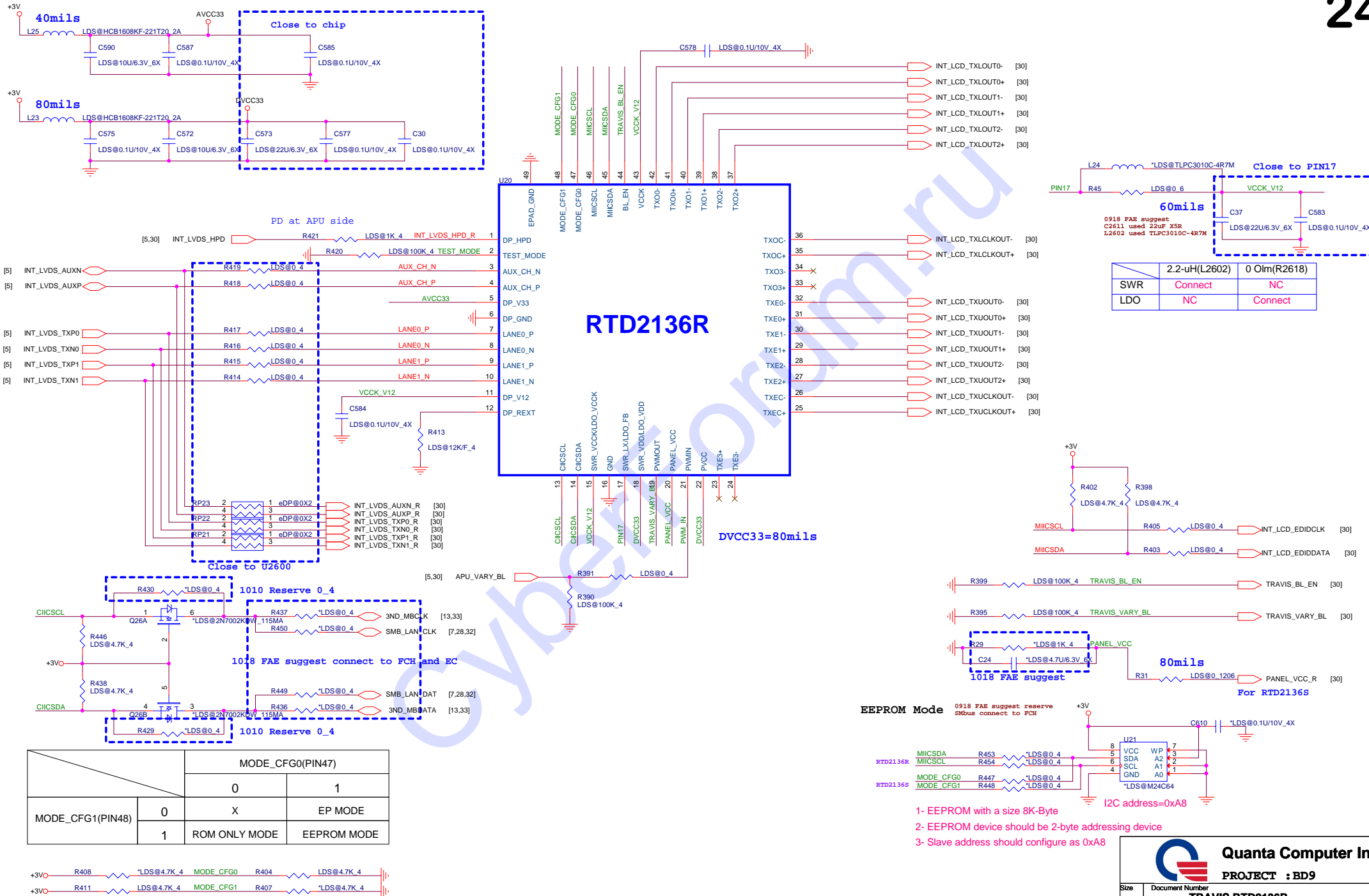
	Charger , AM
	Charger , FM
	USB , PM
	USB , CM

	Charger , AM2
	Charger , FM
	USB , PM
	USB , CM

	Charger , A
	Charger , A
	USB , PM
	USB , CM

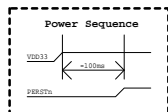
	Charger , A
	USB , PM
	USB , CM



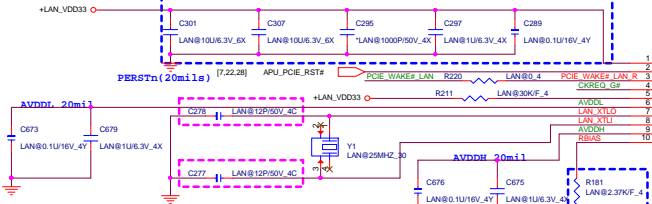




## Atheros Lan <LAN> <LNG>



0.163A(30mils)



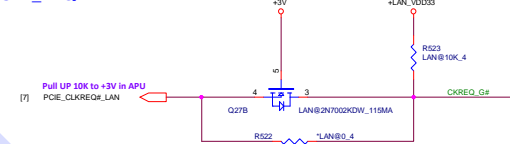
## Atheros AR8161/8162

GIGA:AR8161B  
10/100:AR8162B

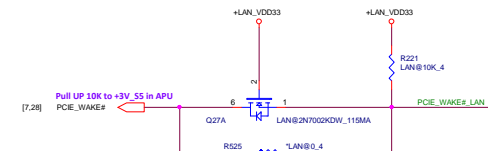
For EMI



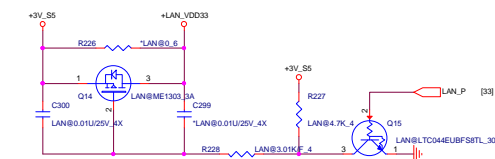
## CLK\_REQ# <LAN>



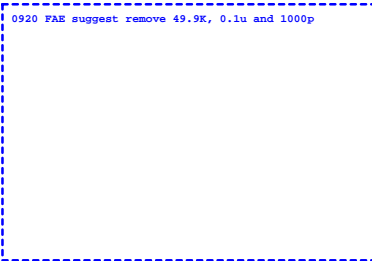
## LAN-Wake up function <LAN>



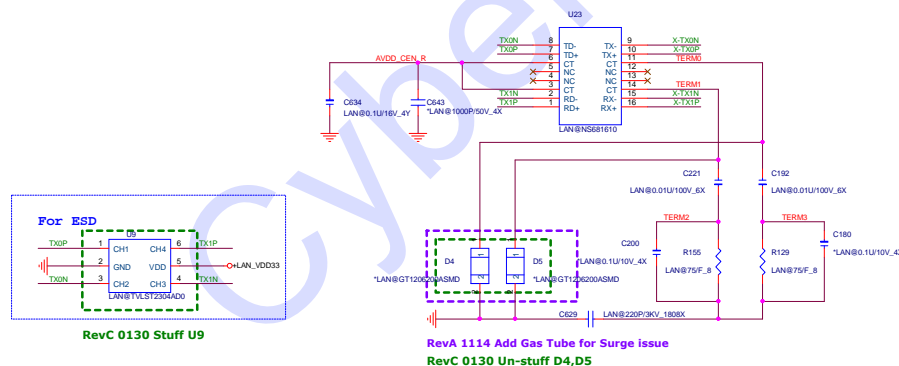
## Wake on LAN function <LAN>



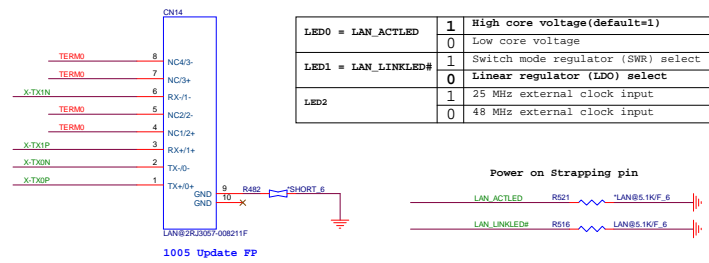
## PLACE NEAR LAN IC SIDE <LAN> <LNG>



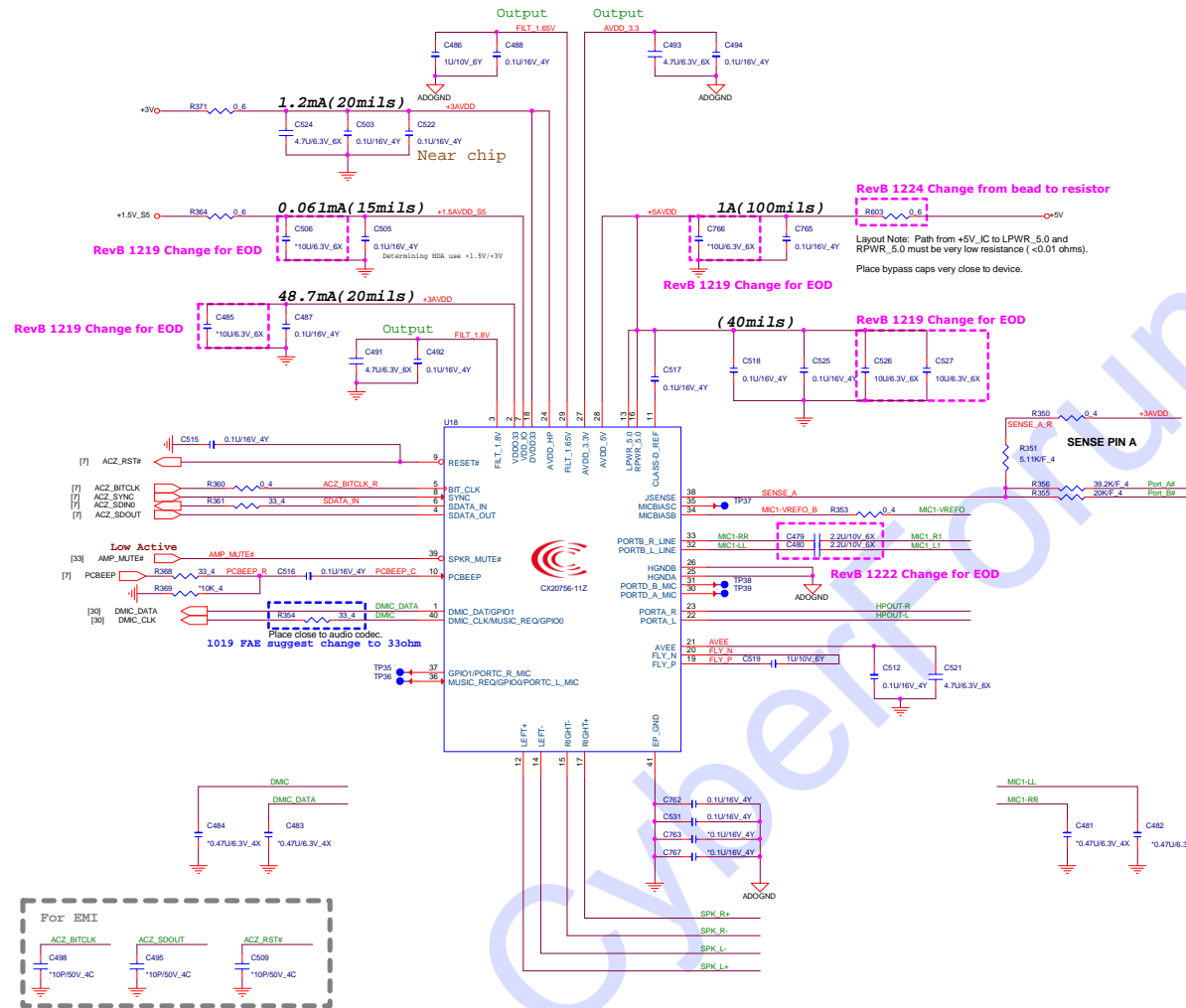
## TRANSFORMER CONN <LAN> <LNG>



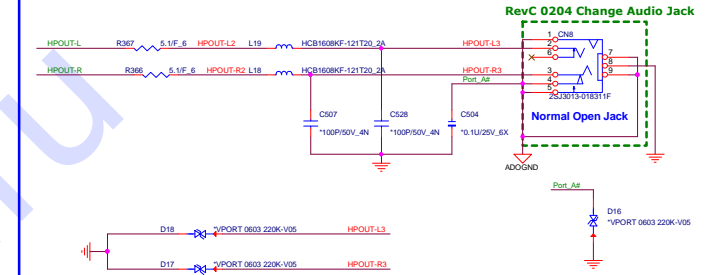
## RJ45 <LAN> <LNG> <LN1>



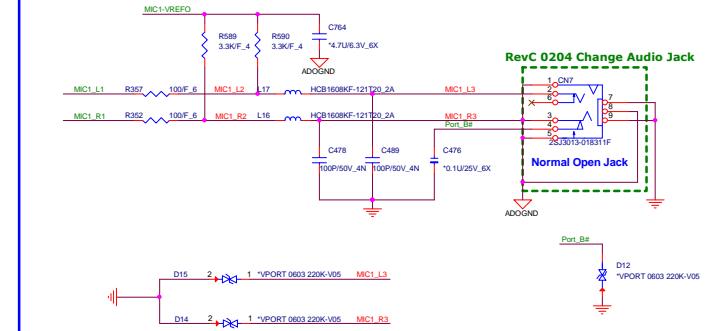
## Codec (CX20756-11Z) &lt;ADO&gt; &lt;EMI&gt;



## HP &lt;ADO&gt; &lt;EMC&gt;

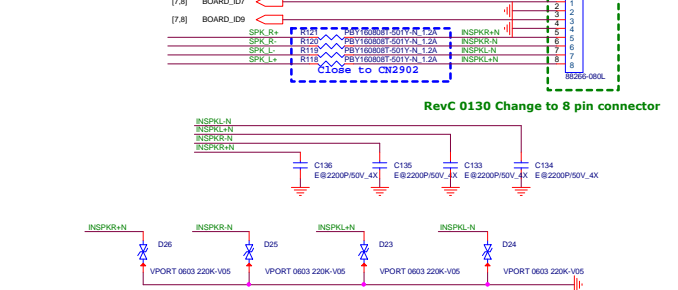


## External MIC &lt;ADO&gt; &lt;EMC&gt;



## Internal Speaker

&lt;ADO&gt; &lt;EMC&gt;

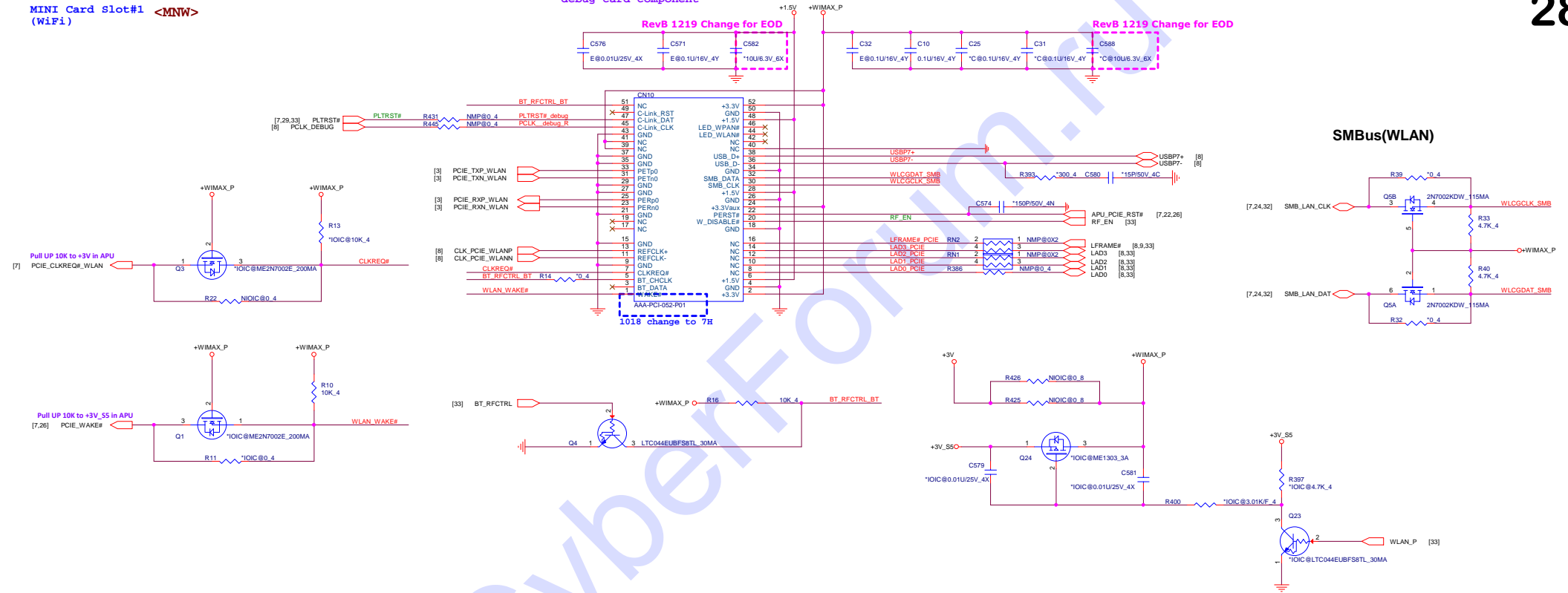


# MINI Card Slot#1 <MNW> (WiFi)

Before RAMP must to remove  
debug card component

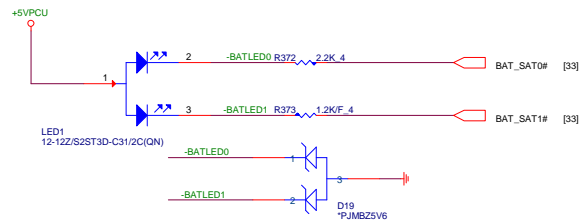
RevB 1219 Change for EOD

RevB 1219 Change for EOD

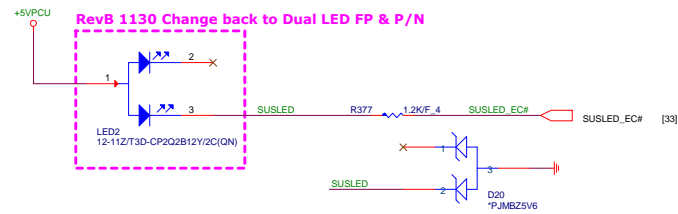


## SMBus(WLAN)

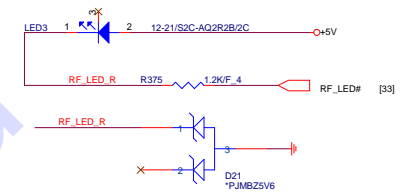
## BATTERY



## POWER

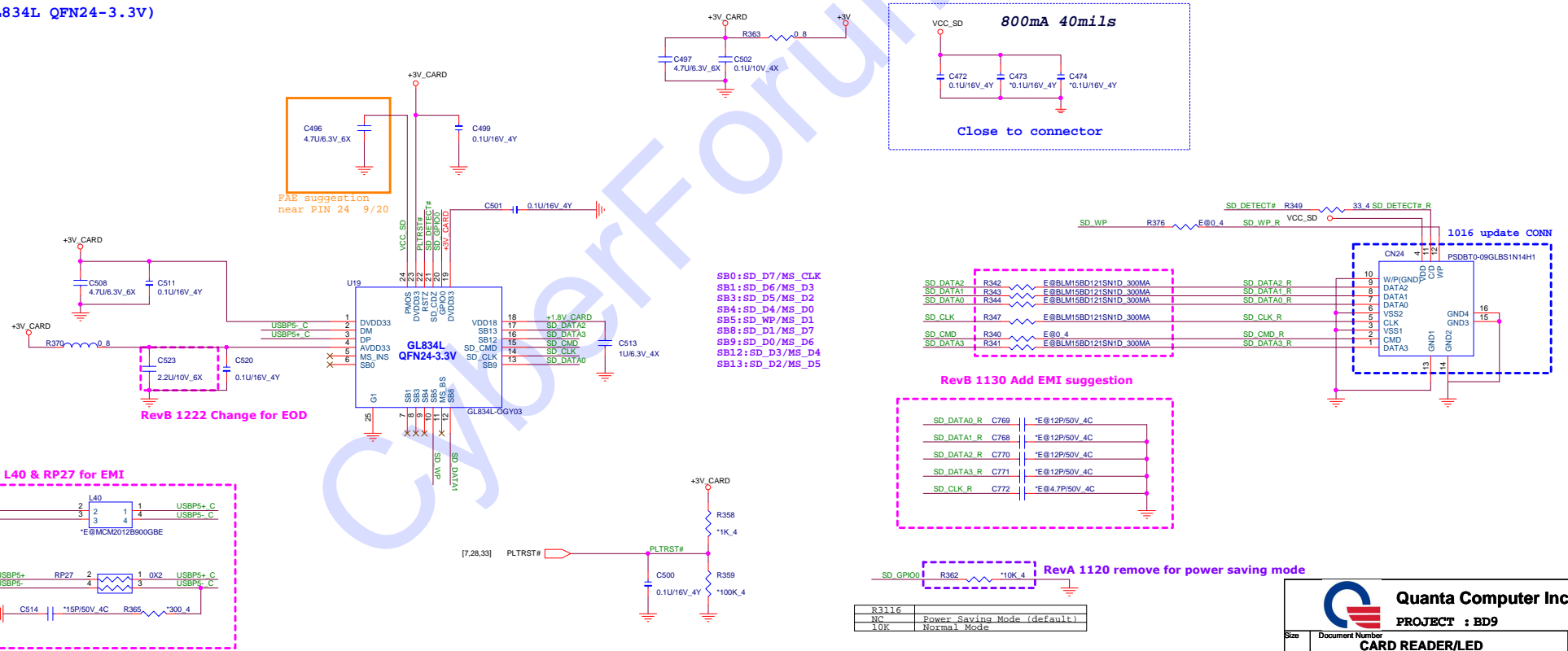


## RF LED



**2 IN 1 CARD READER (Type: MS/SD) <MMC>**

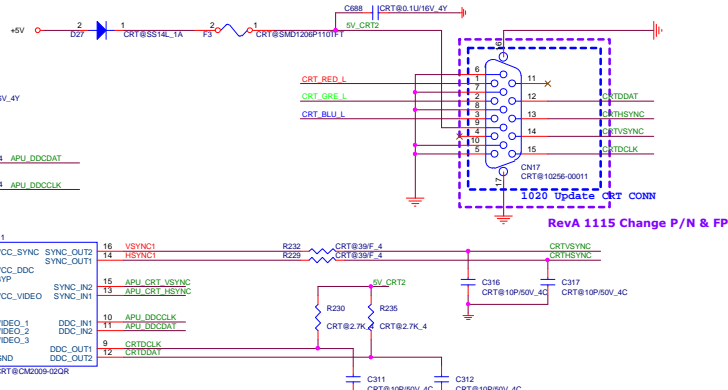
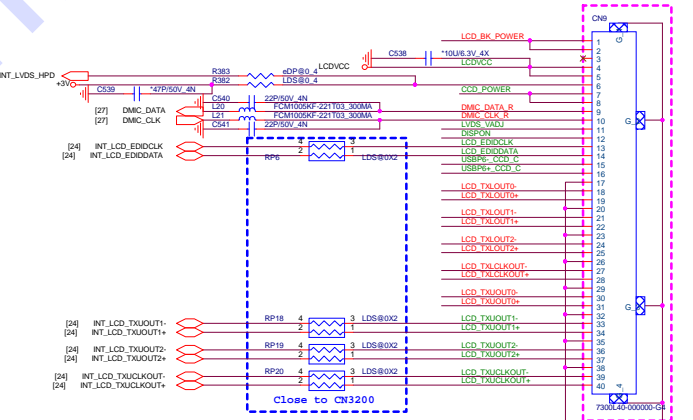
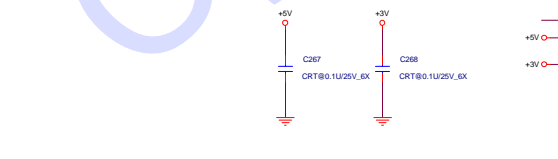
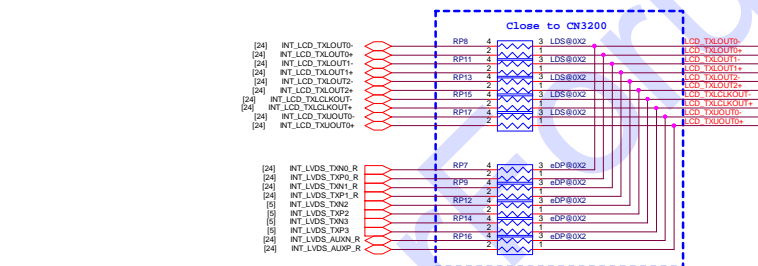
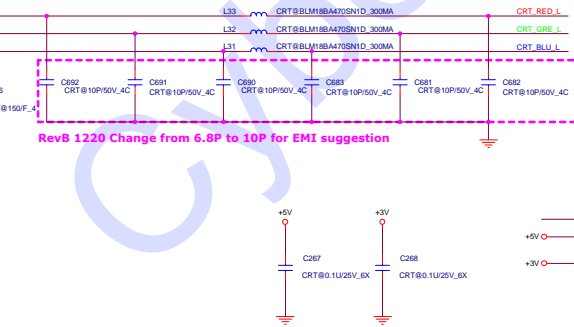
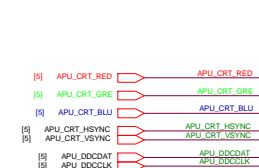
Card Reader (GL834L QFN24-3.3V)



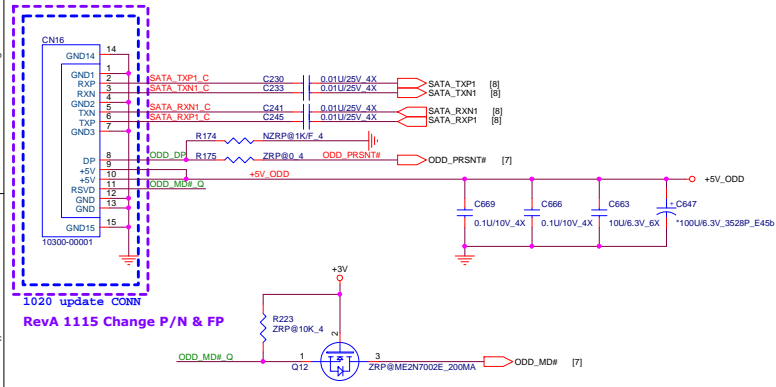
R3116	
NC	Power Saving Mode (default)
10K	Normal Mode



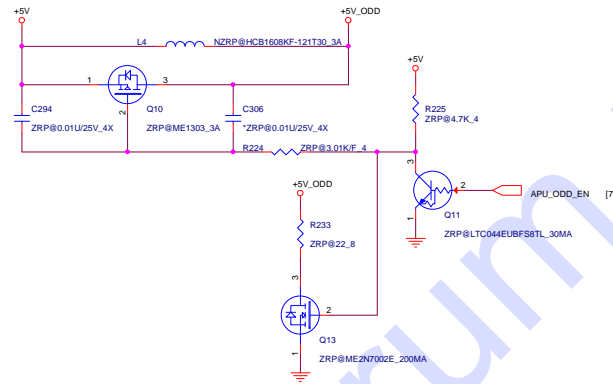
**CRT** [CRT]



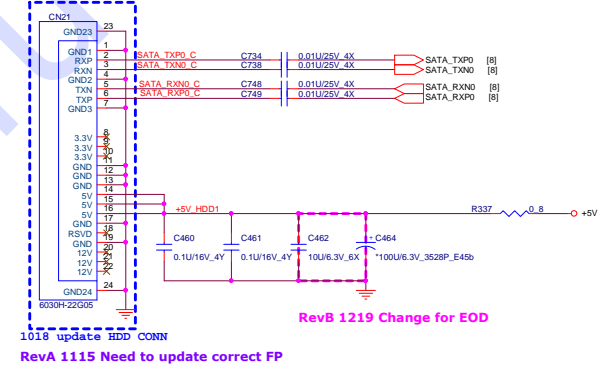
### SATA ODD [ODD]



### ODD Zero power <OZP>



### SATA HDD [HDD]



### 3D-LDO Power <GSR>

### 3D-u-micro P <GSR>

### 3D-SMBus <GSR>

### 3D-Sensor IC <GSR>

# KEY BOARD Connector <KBC> <EMI>

# TOUCH PAD BOARD <TPD> <EMI>

## INT KeyBoard

C557 ESD@39P/50V\_4N MX7  
C558 ESD@39P/50V\_4N MX2  
C559 ESD@39P/50V\_4N MX3  
C560 ESD@39P/50V\_4N MX4

C561 ESD@39P/50V\_4N MX0  
C562 ESD@39P/50V\_4N MX5  
C563 ESD@39P/50V\_4N MX6  
C564 ESD@39P/50V\_4N MX1

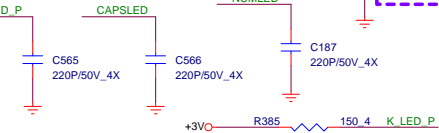
C553 ESD@39P/50V\_4N MY7  
C554 ESD@39P/50V\_4N MY13  
C555 ESD@39P/50V\_4N MY12  
C556 ESD@39P/50V\_4N MY15

C549 ESD@39P/50V\_4N MY3  
C550 ESD@39P/50V\_4N MY6  
C551 ESD@39P/50V\_4N MY14  
C552 ESD@39P/50V\_4N MY5

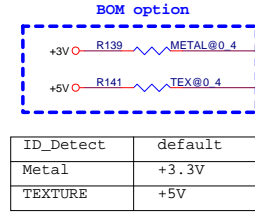
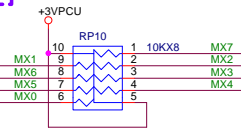
C545 ESD@39P/50V\_4N MY2  
C546 ESD@39P/50V\_4N MY1  
C547 ESD@39P/50V\_4N MY0  
C548 ESD@39P/50V\_4N MY4

C543 ESD@39P/50V\_4N MY16  
C544 ESD@39P/50V\_4N MY17

## ESD Issue

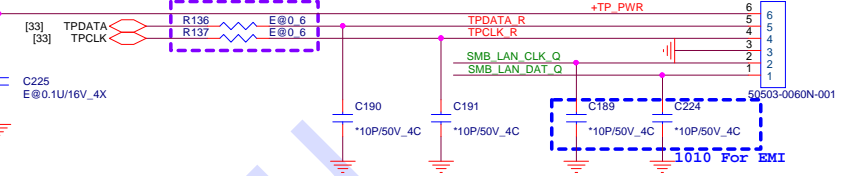


## RevA 1115 Change P/N



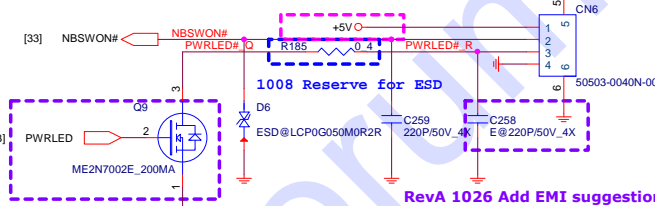
ID_Detect	default
Metal	+3.3V
TEXTURE	+5V

## RevA 1026 Add EMI suggestion



## Power Board (UIF) <PSW>

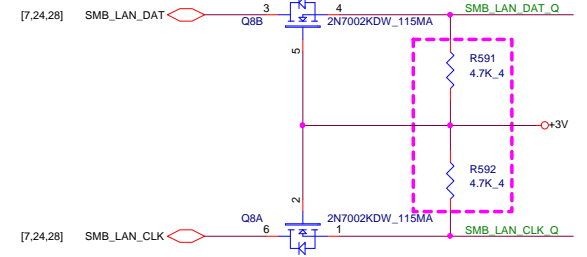
## RevB 1204 Change power rail from +5VPCU to +5V



## RevA 1114 Add Q3402 for PWRLED

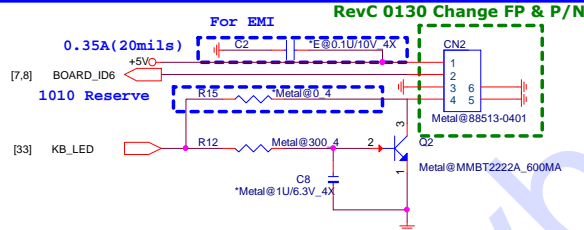
## TP board <TPD>

## RevB 1130 Add 4.7K PU

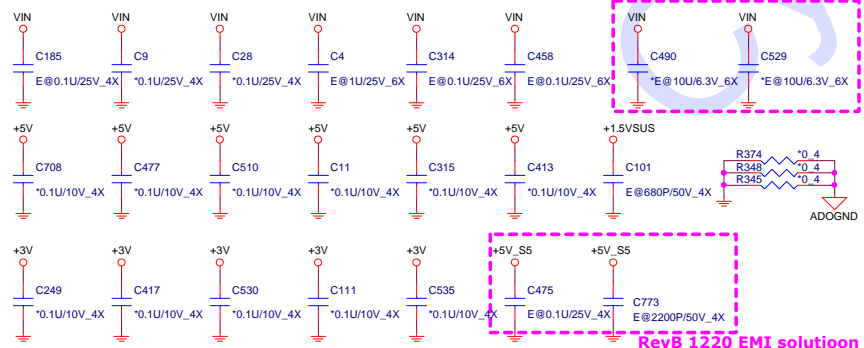


## KEY BOARD LED

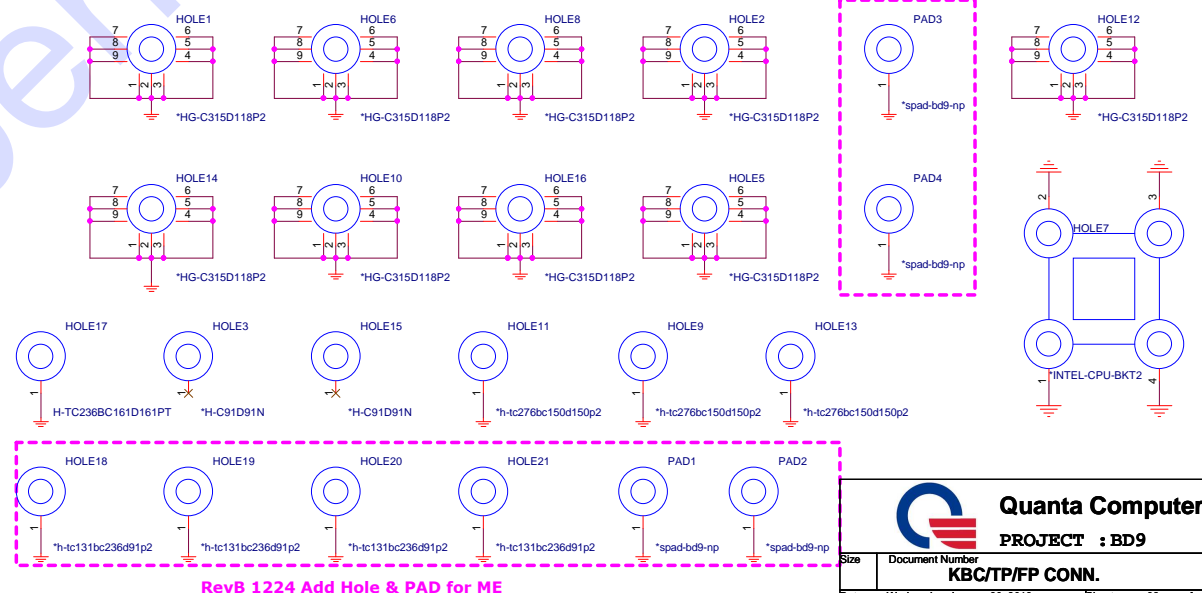
## <KBP> <EMI>



## EMI PAD <EMI>

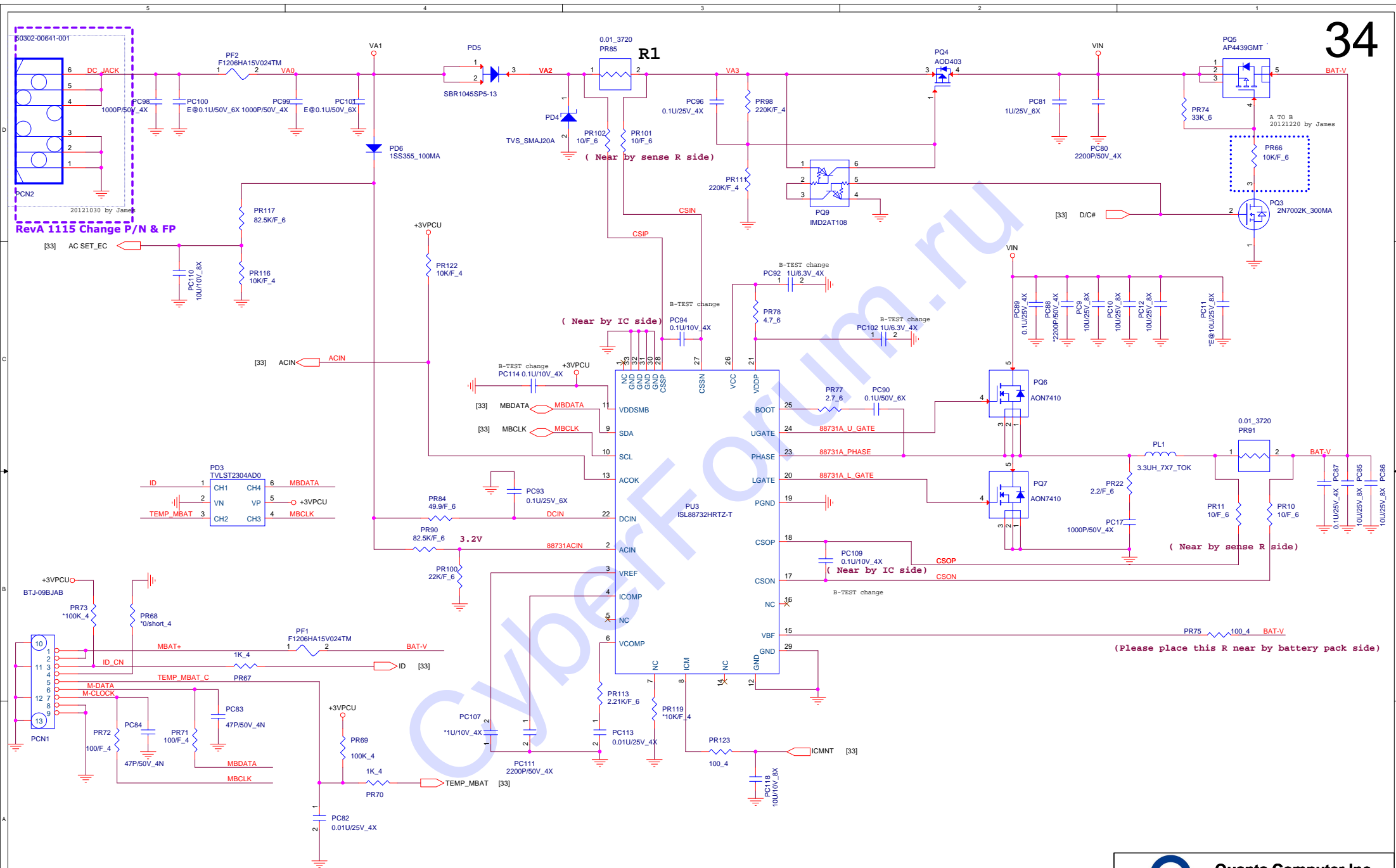


## HOLE <OTH>





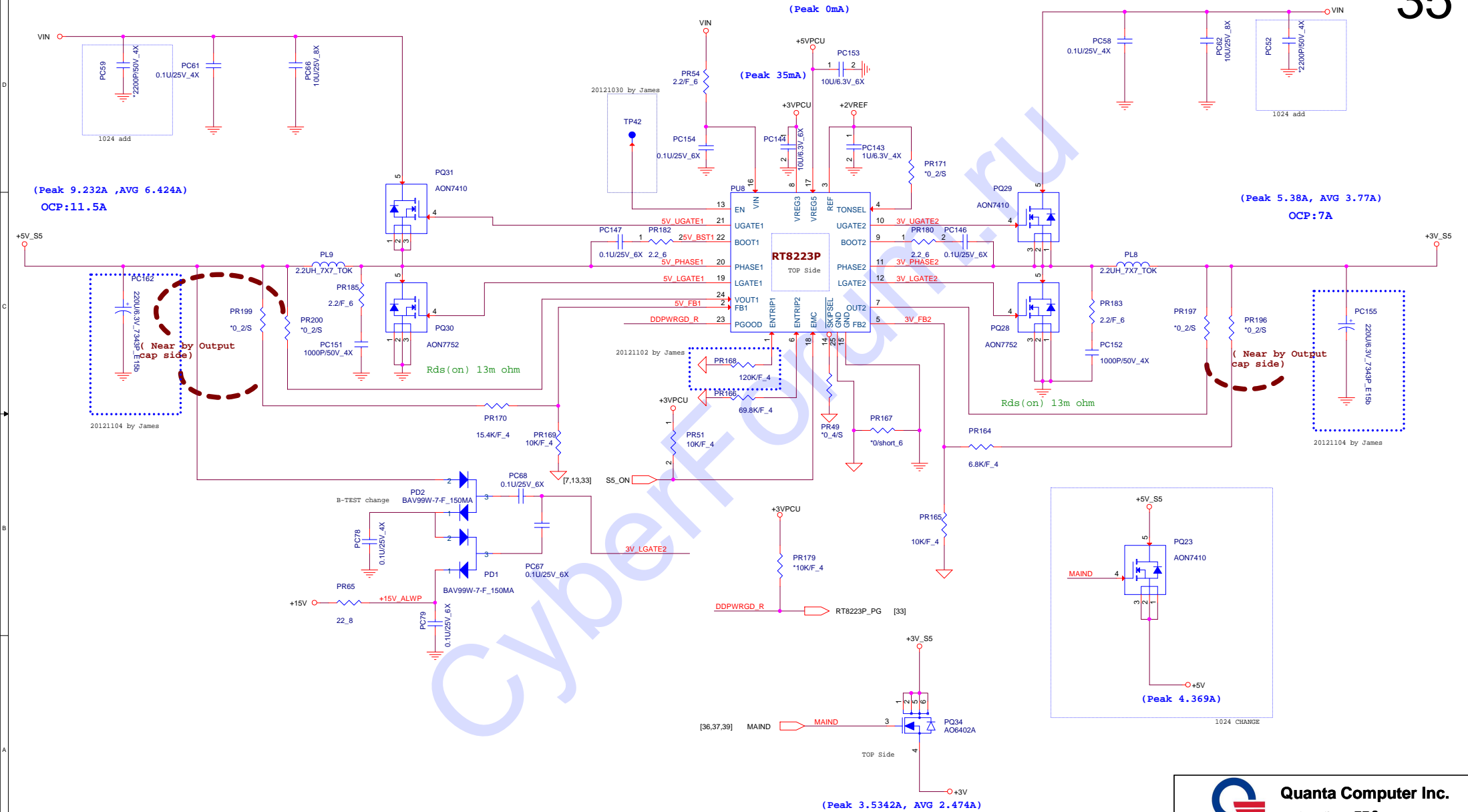
**PAID FOR**



**Quanta Computer Inc.**

**PROJECT : BD9**

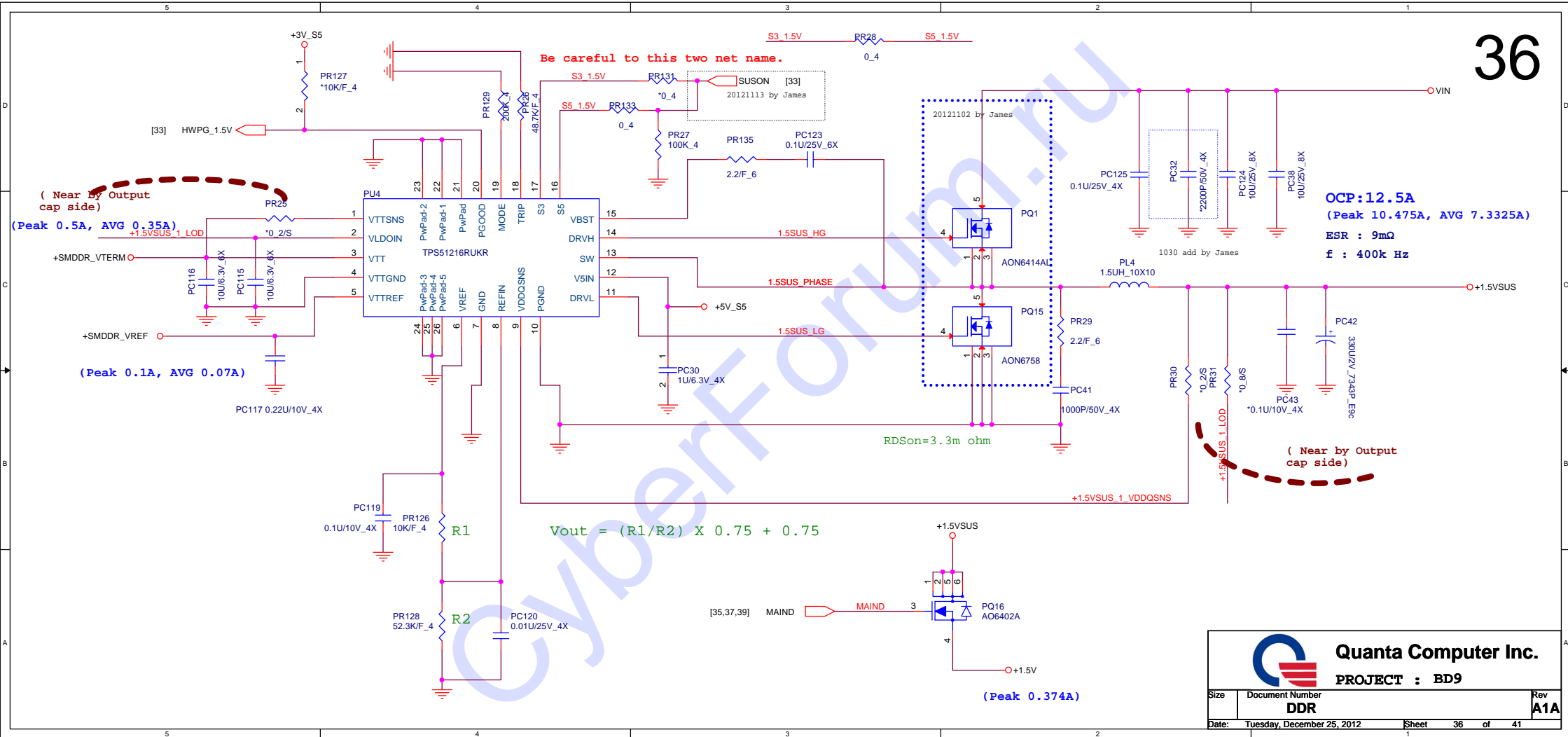
Size	Document Number	Rev
	<b>CHARGER-ISL88731C</b>	<b>A1A</b>
Date:	Thursday, December 27, 2012	Sheet 34 of 41



**Quanta Computer Inc.**

**PROJECT : BD9**

Size	Document Number	Rev
	<b>System 3V/5V(TPS51123A)</b>	<b>A1A</b>
Date:	Tuesday, December 25, 2012	Sheet 35 of 41

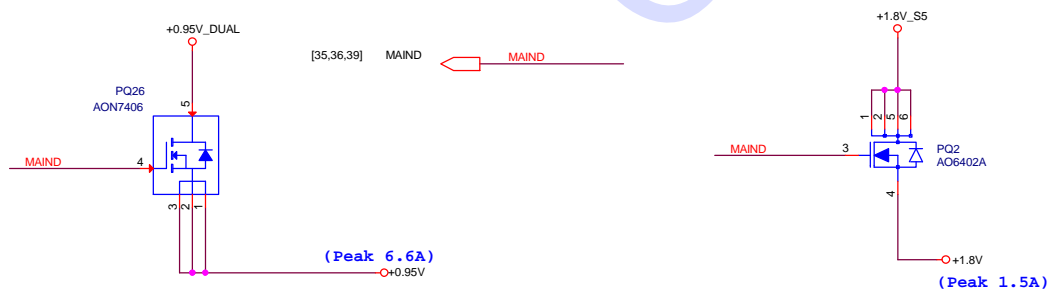
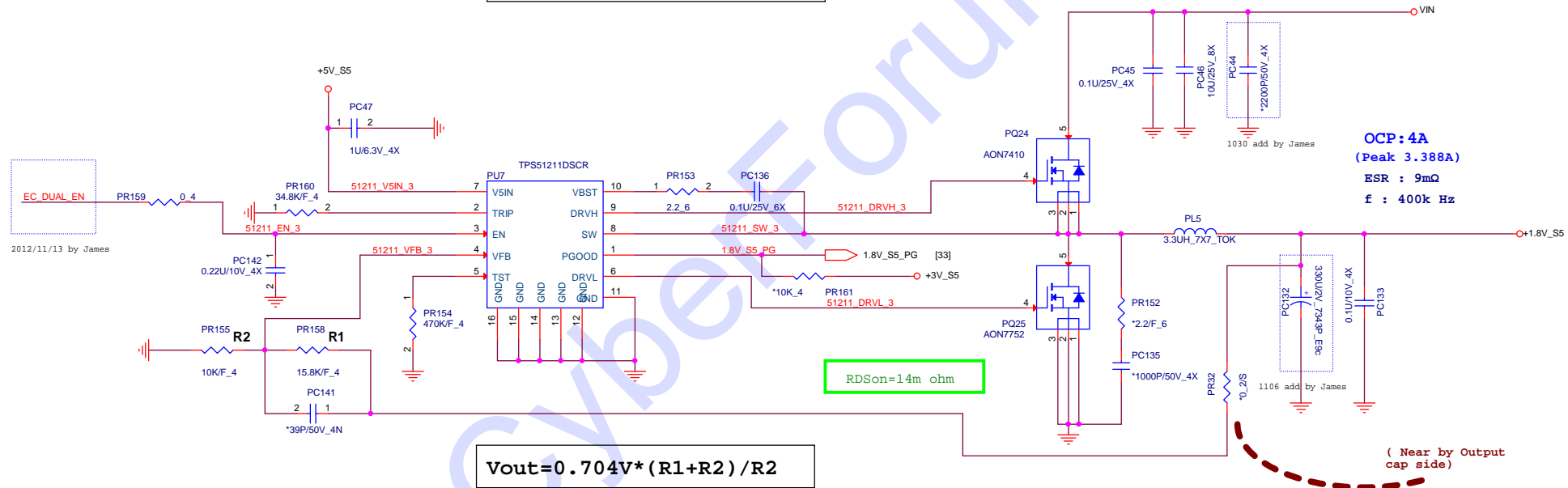
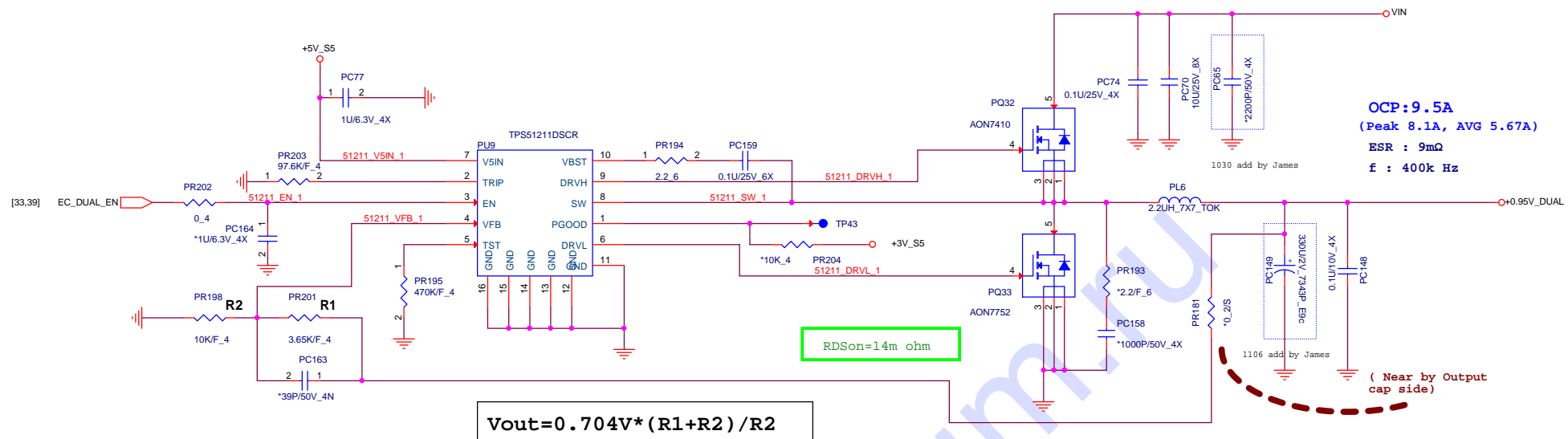


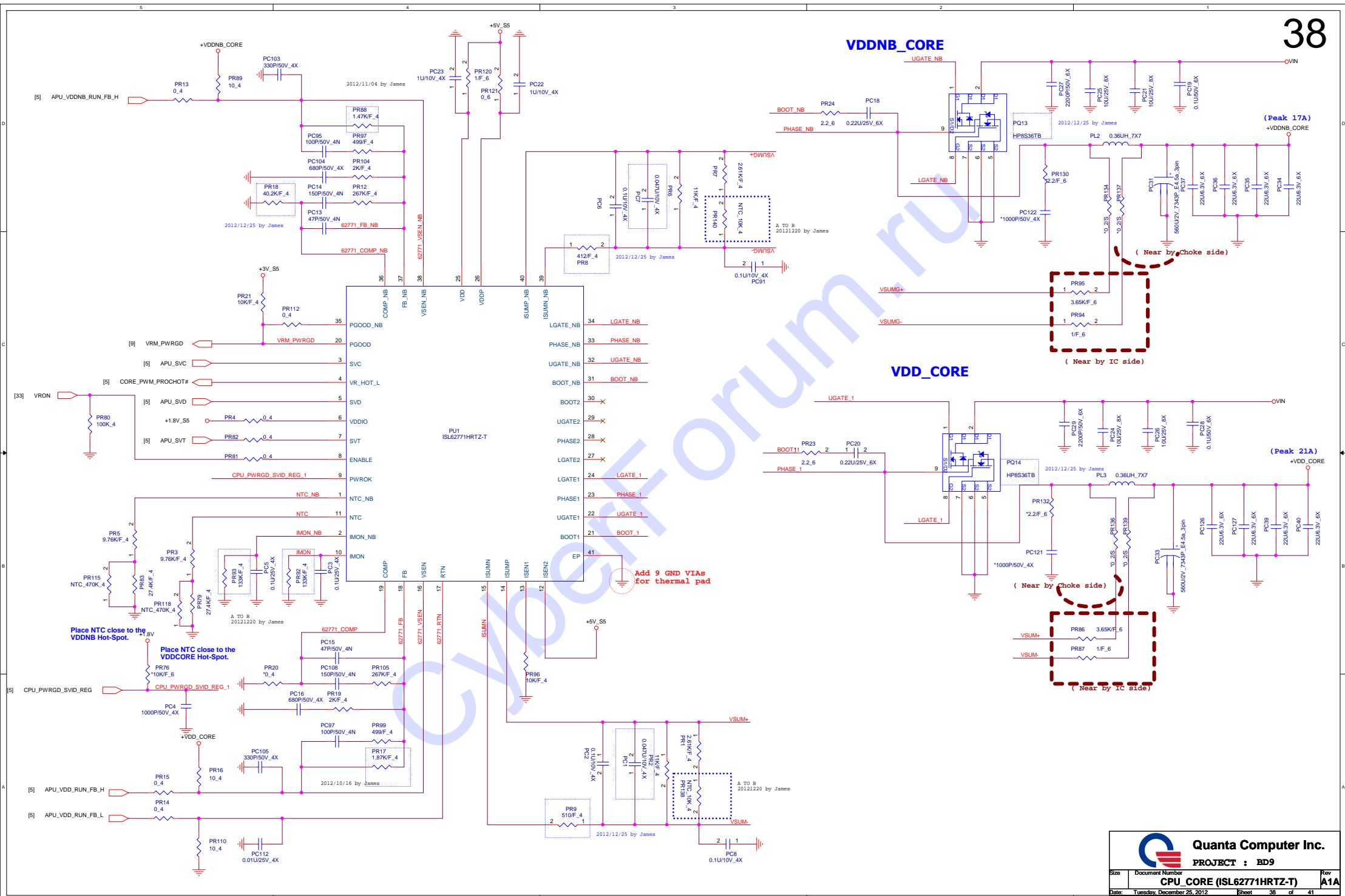
Quanta Computer Inc.

PROJECT : BD9

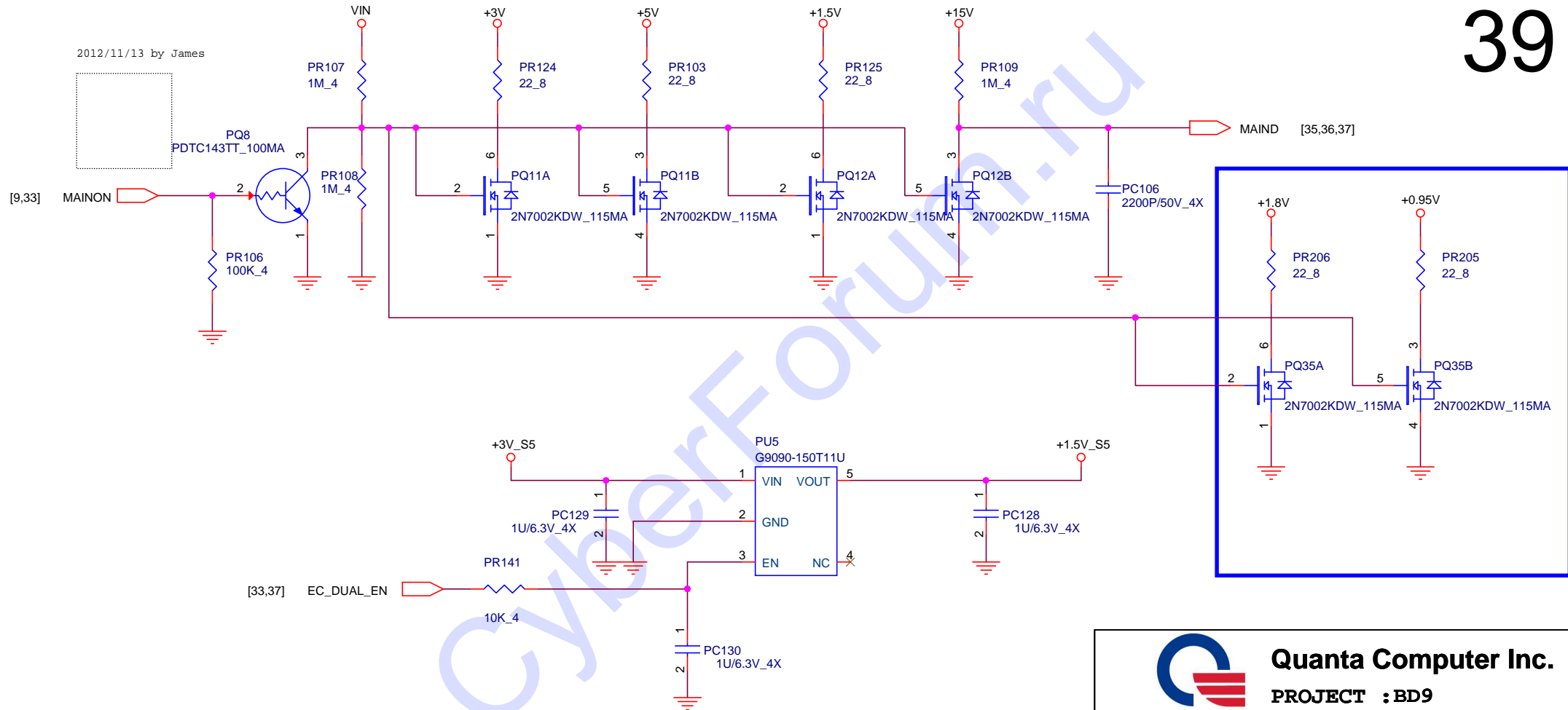
Size	Document Number	Rev
	DDR	A1A
Date:	Tuesday, December 25, 2012	Sheet 36 of 41







2012/11/13 by James



Quanta Computer Inc.

PROJECT : BD9

Size	Document Number	Rev
	Discharge	A1A

Date: Tuesday, December 25, 2012 Sheet 39 of 41



VDDC(V)	GPIO_CORE_CNTRL5 (VID5)	GPIO_CORE_CNTRL4 (VID4)	GPIO_CORE_CNTRL3 (VID3)	GPIO_CORE_CNTRL2 (VID2)	GPIO_CORE_CNTRL1 (VID1)
1.175	0	1	1	0	1
1.150	0	1	1	1	0
1.125	0	1	1	1	1
1.100	1	0	0	0	0
1.075	1	0	0	0	1
1.050	1	0	0	1	0
1.025	1	0	0	1	1
1.000	1	0	1	0	0
0.975	1	0	1	0	1
0.950	1	0	1	0	0
0.925	1	0	1	1	1
0.900	1	1	0	0	0
0.875	1	1	0	0	1
0.850	1	1	0	1	0
0.825	1	1	0	1	1
0.800	1	1	1	0	0
0.775	1	1	1	0	1

```
+VGPU_CORE
Continue current:18A
Peak current:24A
OCP minimum 30A
Loadline=1.5mV/A
```

10K NTC put close with Inductor

**PROJECT : BD9**

Size	Document Number <b>GPU</b>
------	-------------------------------

Sheet 41 of 41

Rev  
**A1A**