ZRMAE/ZEMAE

Juno/Iakros 10AN/10ANG

LA-A551P REV 1.0 Schematic

AMD KABINI Quad Core 25W for UMA+DIS
AMD KABINI Quad Core 15W
2013-07-05 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2013/05/15	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: *Cover Page*

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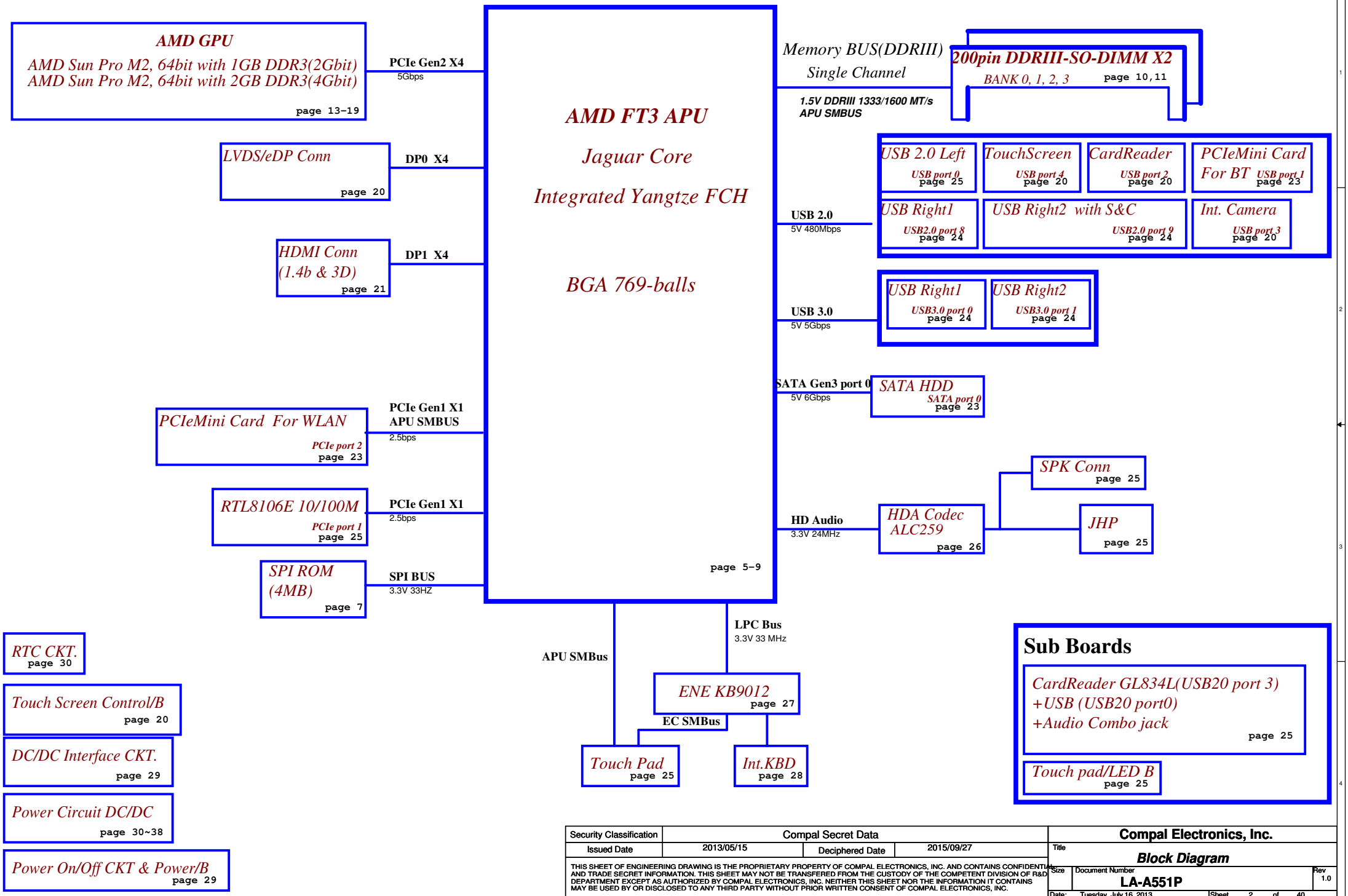

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Title	Block Diagram		
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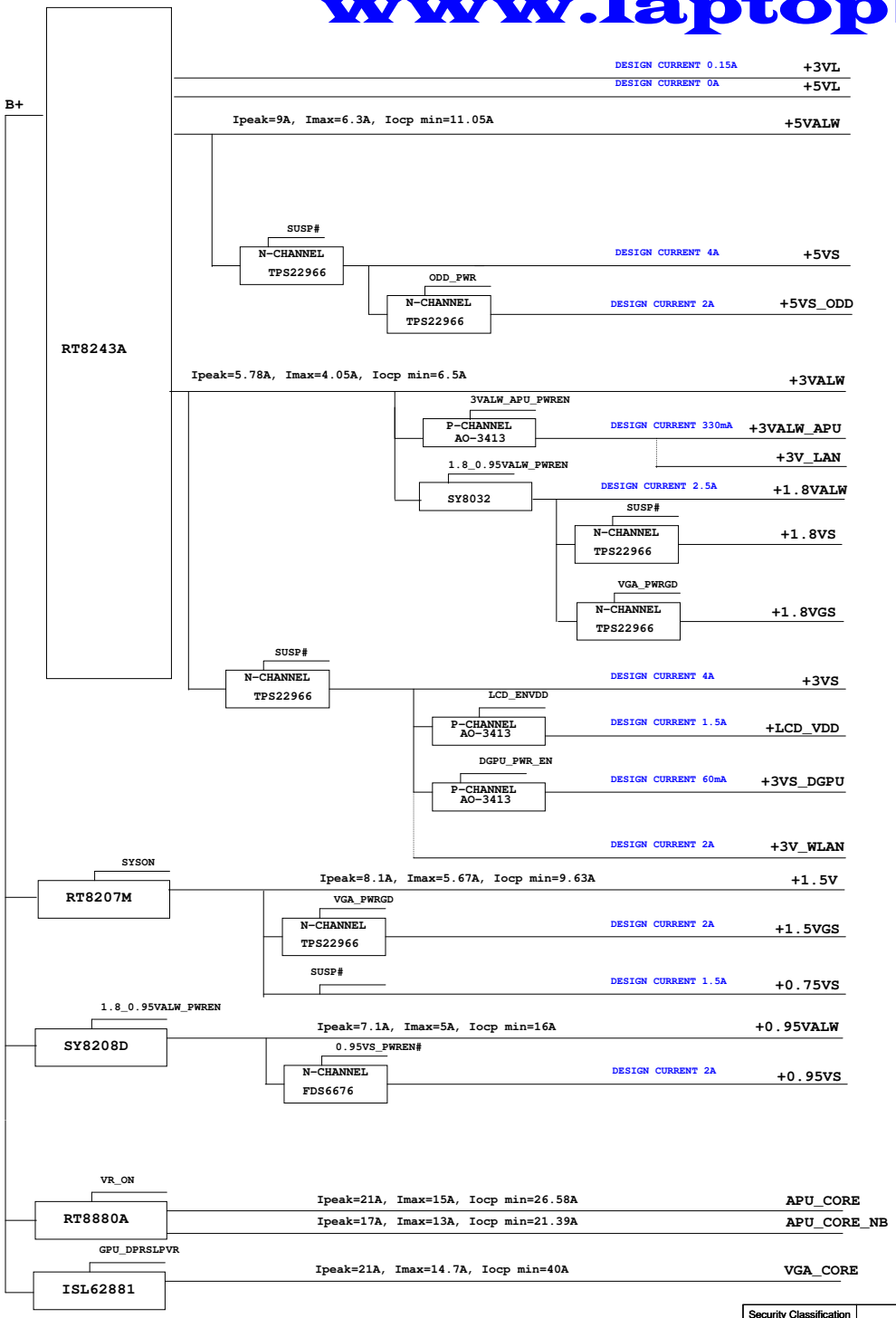

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Title: Power Tree

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	LA-A551P	0.2

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UMA

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.8VALW +0.95VALW +VSB	+1.5V	+5VS +3VS +0.95VS +1.8VS +1.5VS +0.75VS +APU_CORE +APU_CORE_NB
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	APU	
description	CPU A4-5000	CPU A6-5200
explain	15W 4C	25W 4C
BTO	A4R1@	A6R1@

Function	GPU	EC			LVDS-eDP		Camera & Mic			KB Light
description	Sun-Pro M2	9012	885		LVDS-eDP		Camera & Mic			KB Light
explain	VGA	9012	w/	w/ EMI	LVDS	eDP	Camera & Mic			KB Light
BTO	VGA@	9012@	885@	885_EMI@	LVDS@	IEDP@	CAM@	CAM@EMI@	@CAM@EMI@	KBL@

Function	LAN	S&C		Size		Codec	Touch Screen	
description	8106E	TI solution		Size		ALC259	Touch Screen	
explain	8106E	TPS2546	TPS2544	14"	15"	ALC259	W/ Touch	W/O EMI Touch
BTO	8106E@	2546@	2544@	14@	15@	259@	Touch_EMI@	@Touch_EMI@

Function	EMI/ESD/RF part					
description	EMI/ESD/RF part					
explain	EMI/ESD/RF part					
BTO	EMI@	@EMI@	ESD@	@ESD@	@RF@	

APU SM Bus Address (SCL0/SDA0)

Power	Device	HEX Address
+3VS	DDR SO-DIMM A	A0H 1010 0000 b
+3VS	DDR SO-DIMM B	A2H 1010 0010 b
+3VS	WLAN	

EC SM Bus1 Address

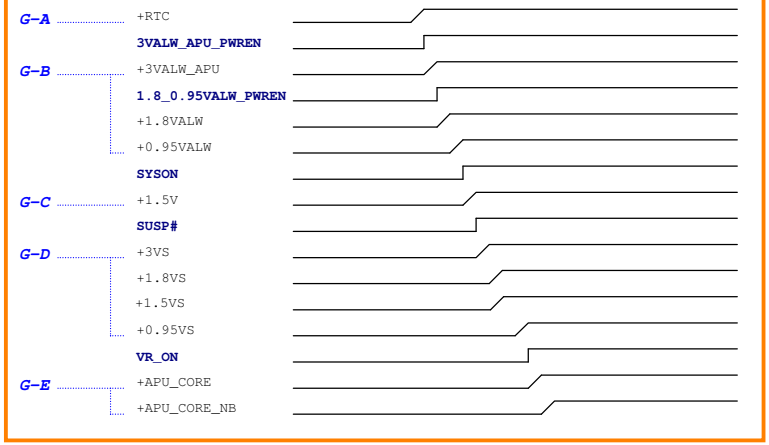
Power	Device	HEX	Address
+3VL	Smart Battery	16H	0001 0110 b
+3VL	Charger	12H	0001 0010 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	VGA thermal	82H	1000 0010 b
+3VS	APU thermal	98H	1001 1000 b

STATE / SIGNAL	SLP_S3#	SLP_S5#
Full ON	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH
S4 (Suspend to Disk)	LOW	HIGH
S5 (Soft OFF)	LOW	LOW
G3	LOW	LOW

APU POWER SEQUENCE



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Title: Notes List

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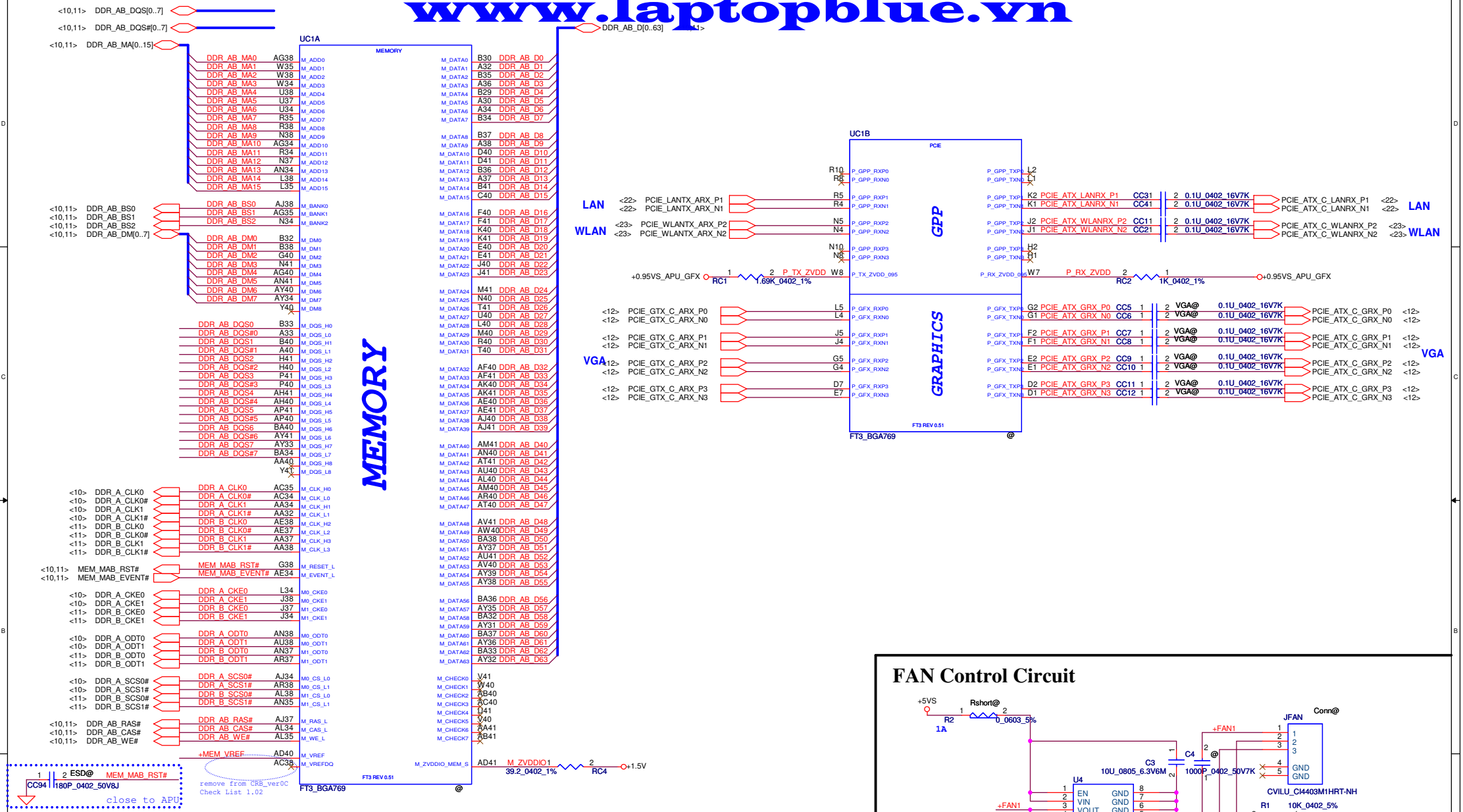
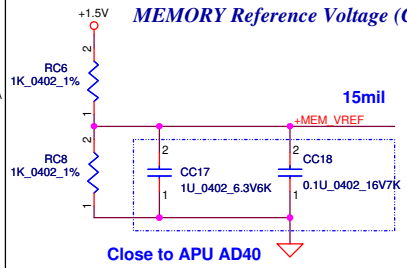


FAN Control Circuit

SA00002XA00 EOL change use SA00003UO00
2nd source SA00005JO00

MEMORY Reference Voltage (Cap follower checklist 1.02)



EVENT# pull high

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Title	FT3 DISP/MISC/HDT		
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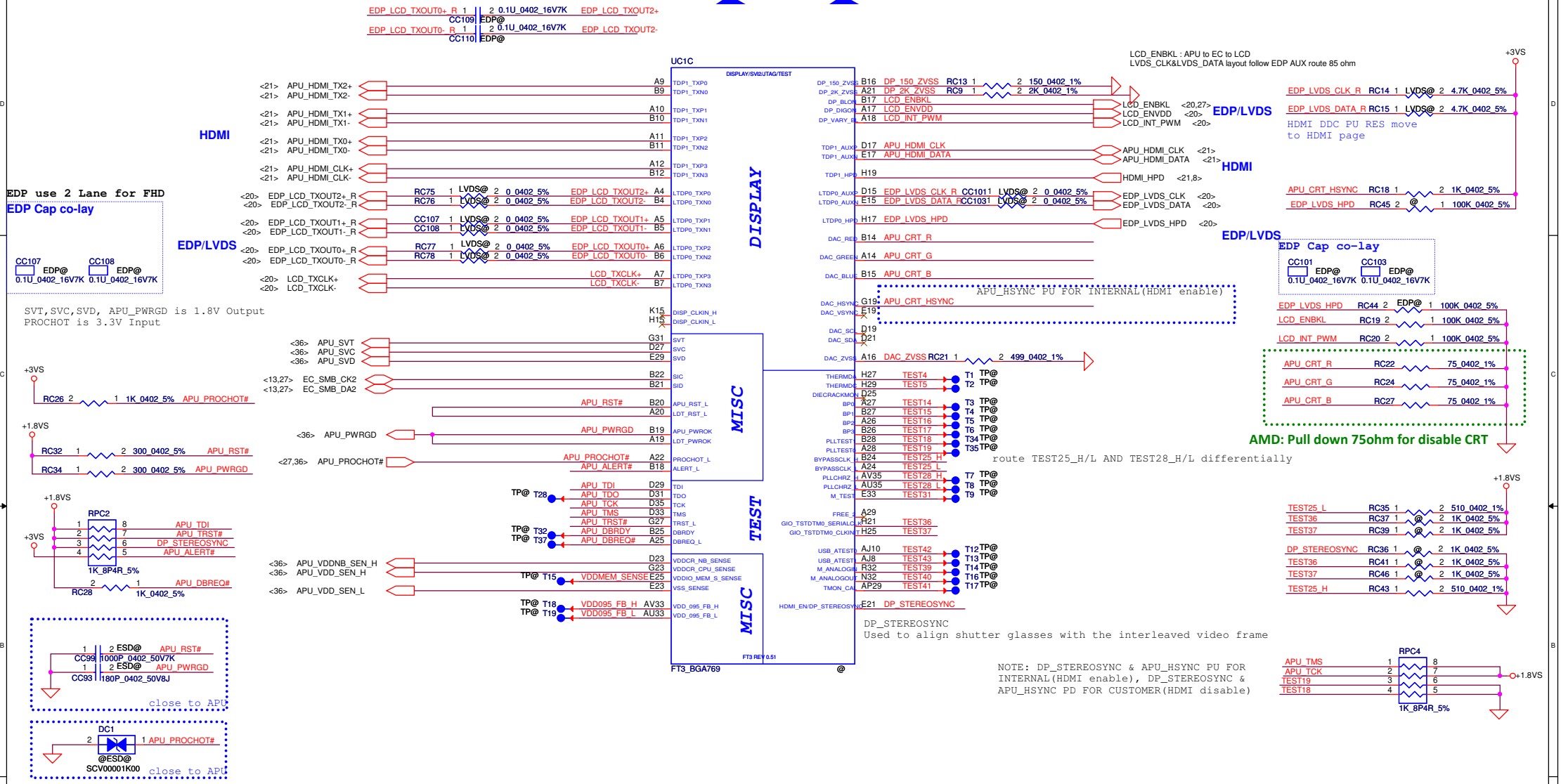

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Title	FT3 DISP/MISC/HDT		
Size	Document Number LA-A551P		Rev 1.0
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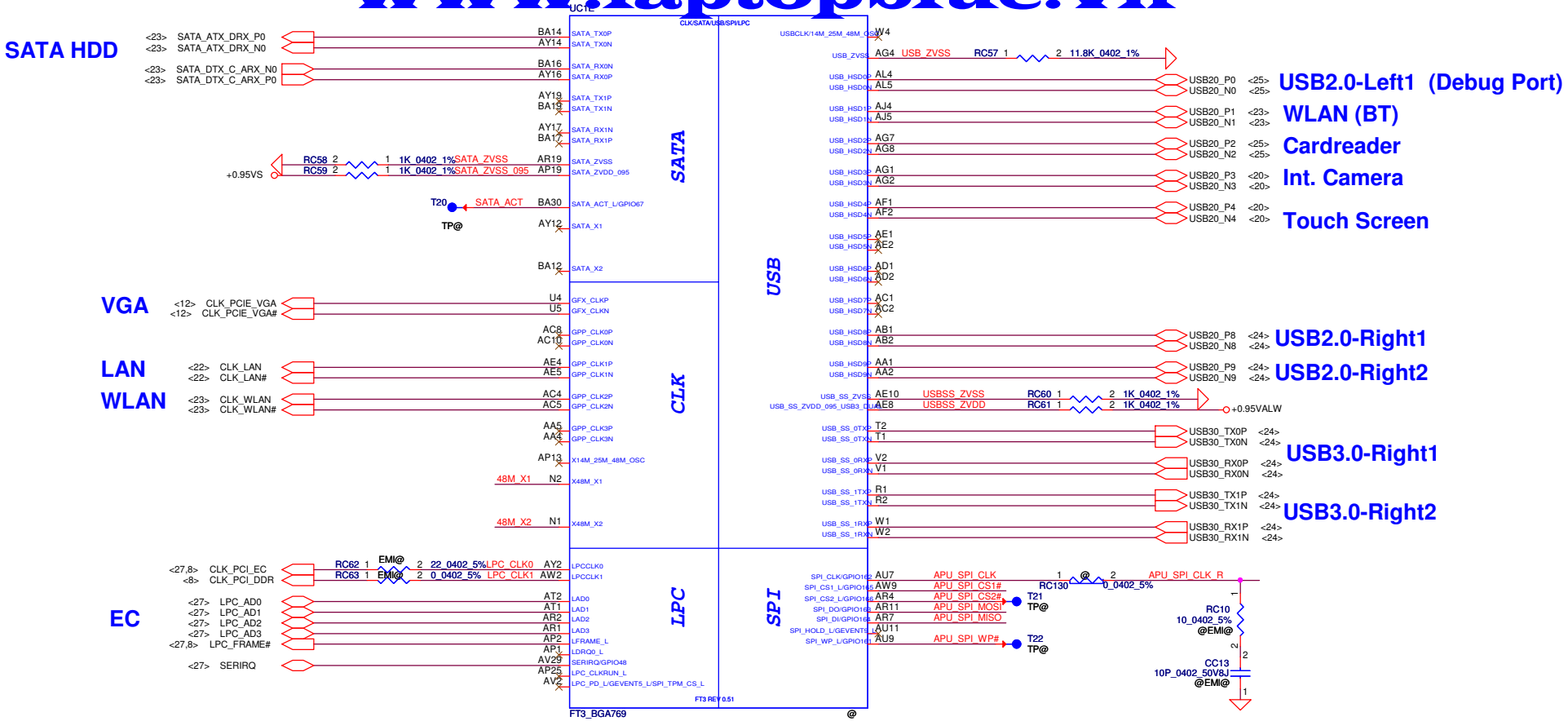
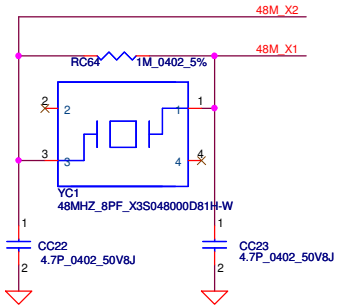
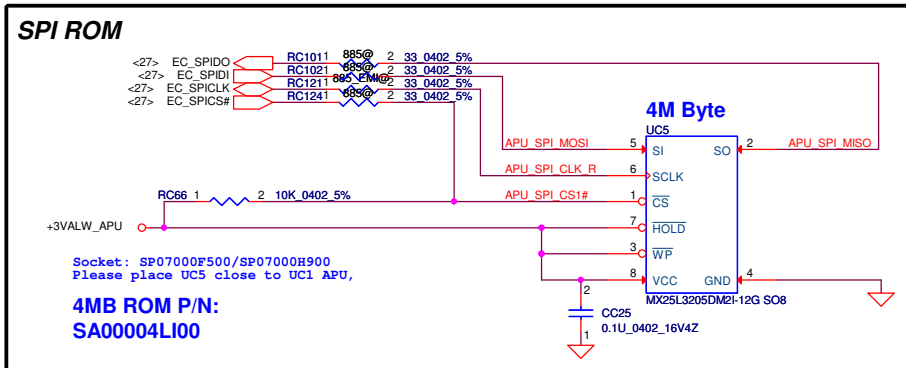


48KMHz CRYSTAL



SPI ROM



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Title	FT3-SATA/CLK/USB/SPI/LPC		
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Follow check list & ORB_0C design 10 ms RC delay circuit on +1.8-V S5 power rail.

STRAP PINS

	CLK_PCI_EC	CLK_PCI_DDR	LPC_FRAME#	GEVENT2	RTC_CLK
PULL HIGH	BOOT FAIL TIMER	CLKGEN ENABLE DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING DEFAULT
PULL LOW	BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT	FAST POWER UP/RESET TIMING FOR SIMULATION

	H	L
PANEL_SEL	eDP panel	LVDS panel

	H	L
TOUCH_SEL	Touch Panel	Non Touch Panel (turn off EHCI)

Board Conf.	Board_ID0	Board_ID1
PX5	0	0
Reserved	0	1
DIS	1	0
UMA	1	1

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Title: FT3 GPIO/AZ/MISC

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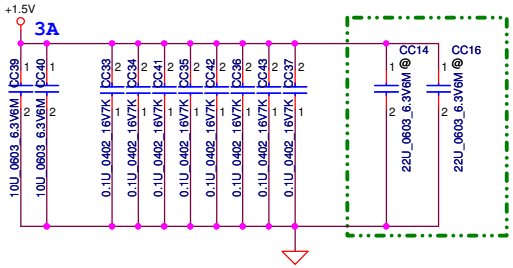
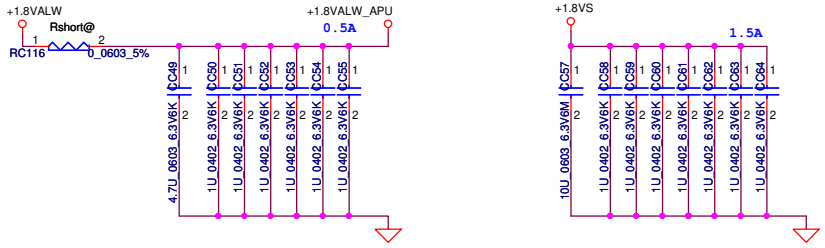
1.5V OF APU

AMD CKL v1.01	10uF	4.7uF	1uF	180pF
VDDIO_MEM_S	2	8	2	4

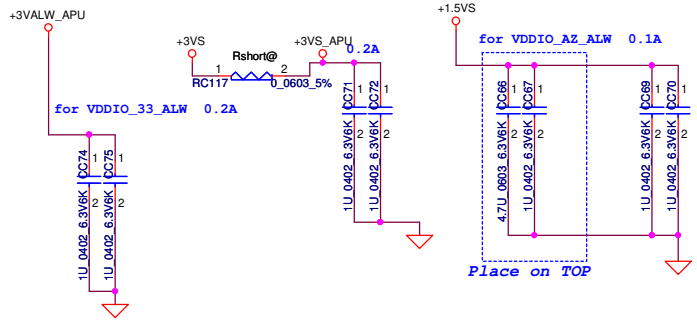


1.8VALW & 1.8VS OF APU

AMD CKL v1.01	10uF	4.7uF	1uF	180pF
VDD_18	1		7	1
VDD_18_ALW		1	6	1

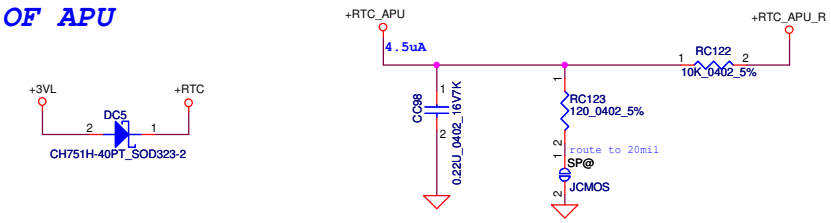


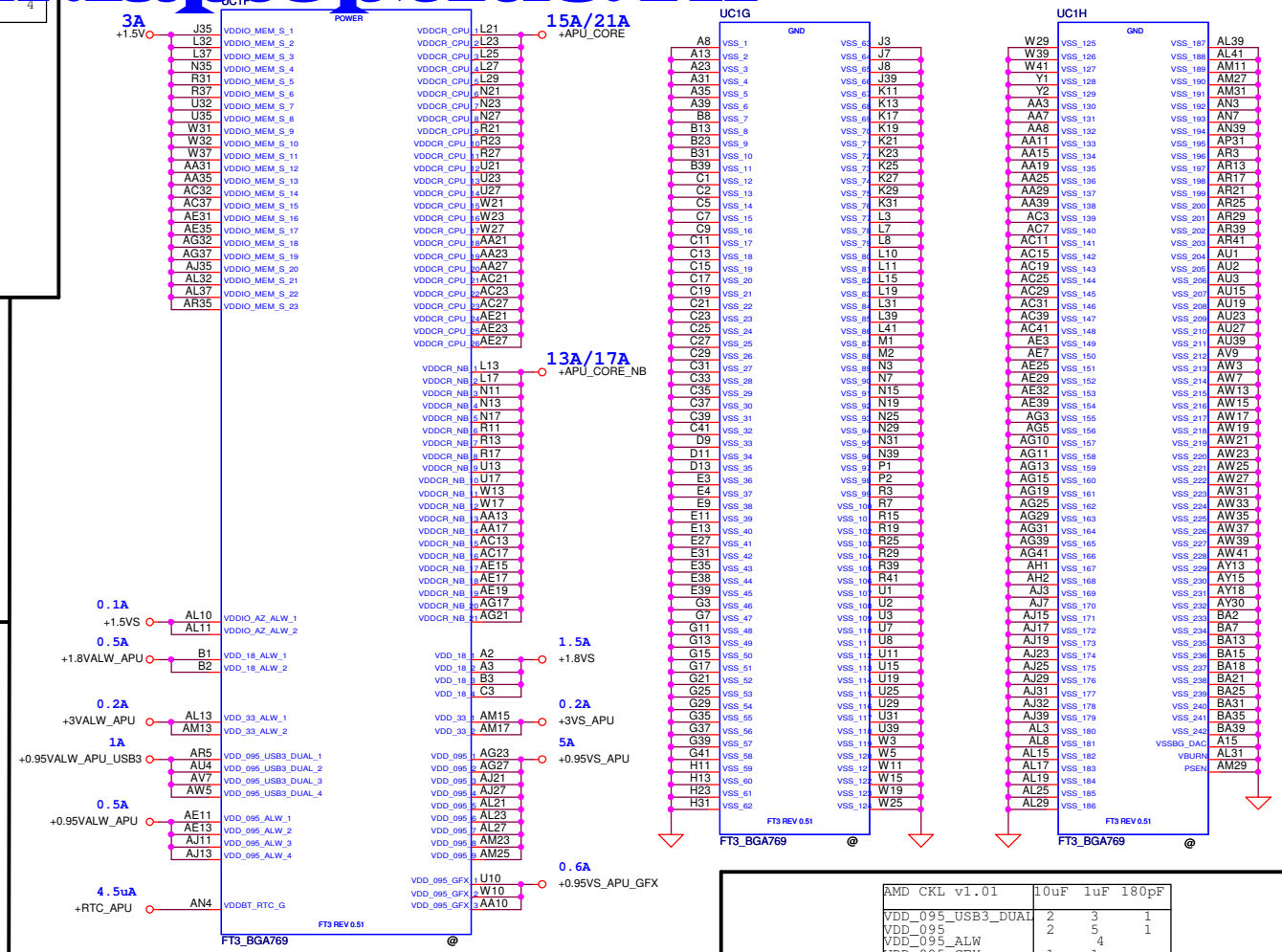
3.3VALW & 3.3VS OF APU



AMD CKL v1.01	4.7uF	1uF	180pF
VDDIO_AZ_ALW	1	3	1
VDDIO_33_ALW		2	
VDDIO_33		2	1

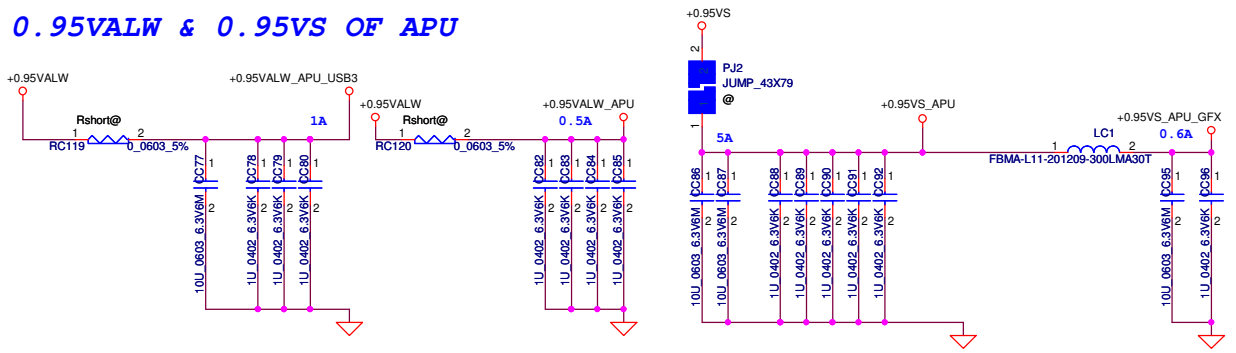
RTC OF APU





AMD CKL v1.01	10uF	1uF	180pF
VDD_095_USB3_DUAL	2	3	1
VDD_095	2	5	1
VDD_095_ALW		4	
VDD_095_GFX	1	1	

0.95VALW & 0.95VS OF APU



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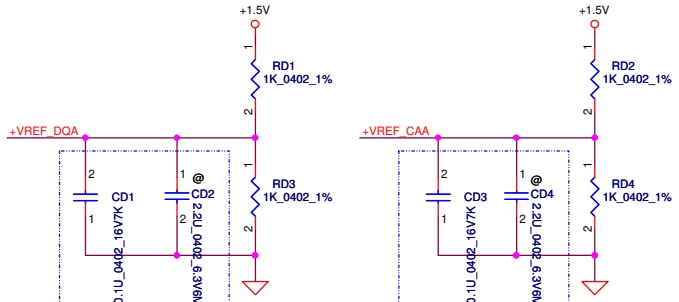
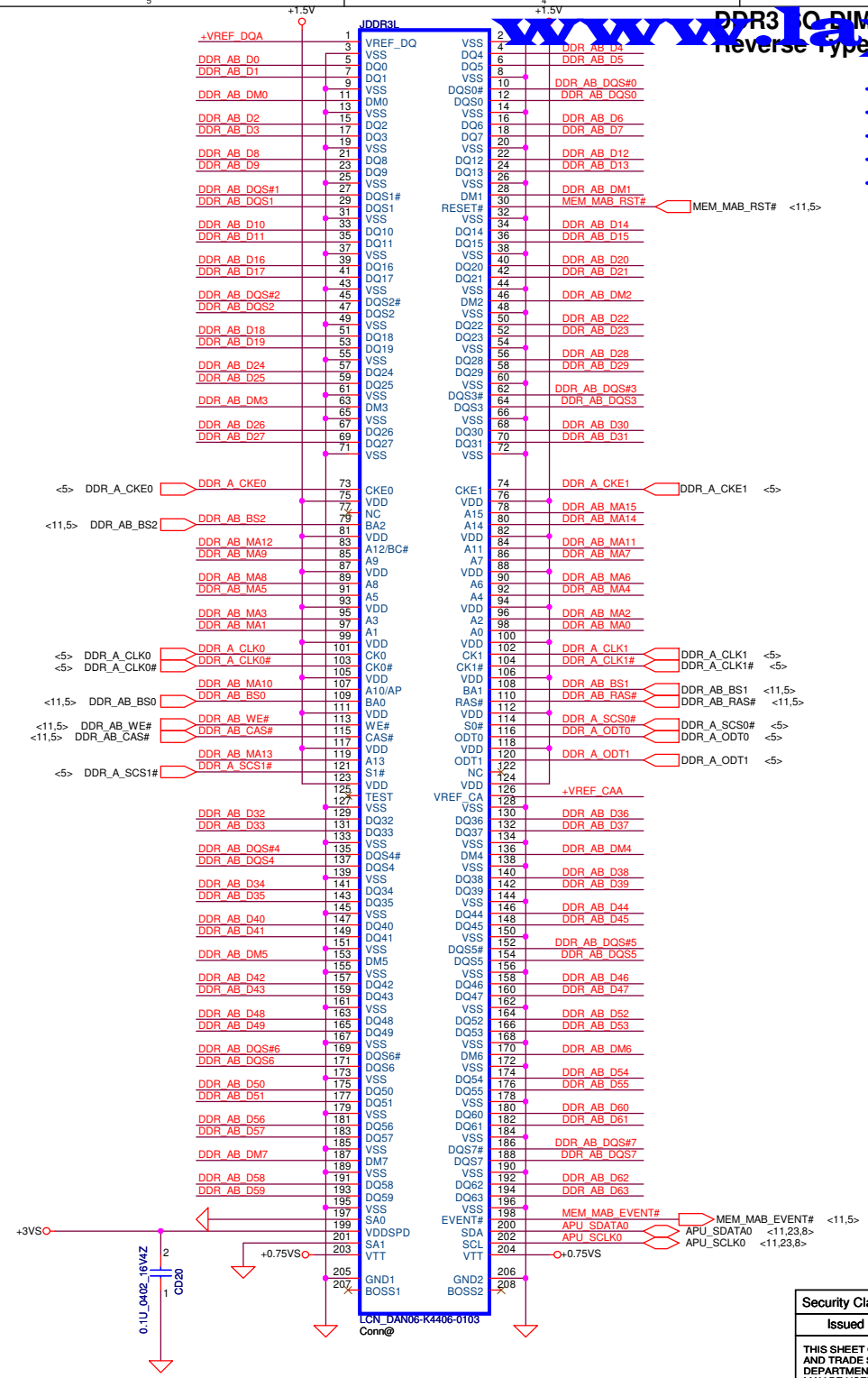
DDR3 SO-DIMM A
Reverse Type

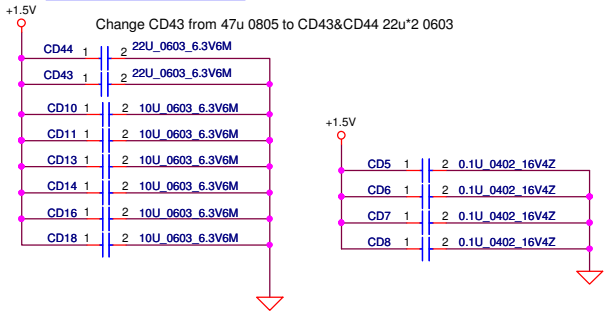
SO-DIMM VREF



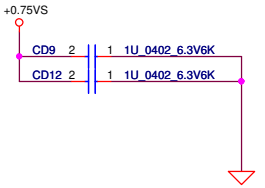


Layout Note:
Place near JDDR3L

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JDDR3L.203 and 204



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Title: ***DDRIII-SODIMMA***

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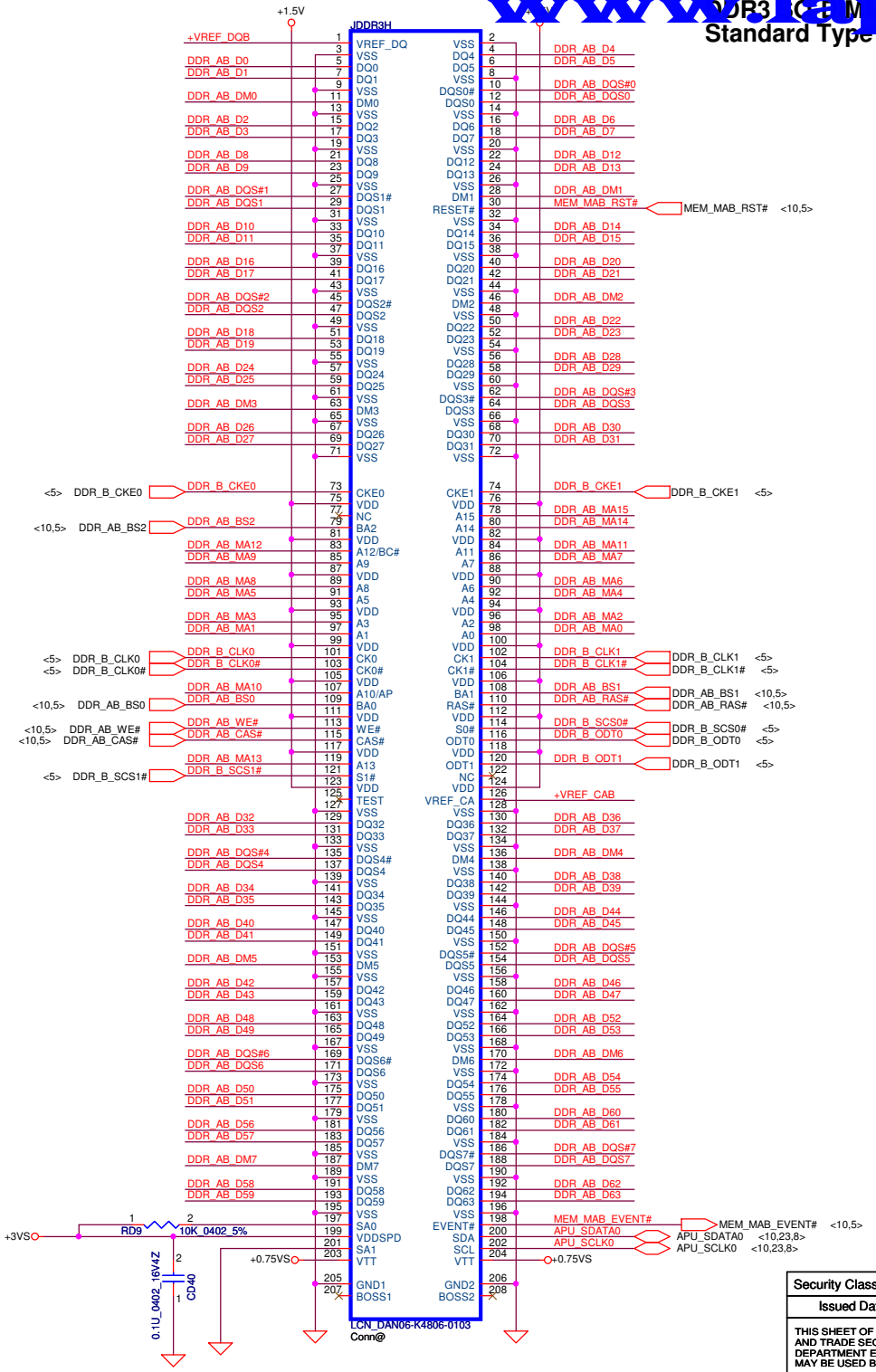
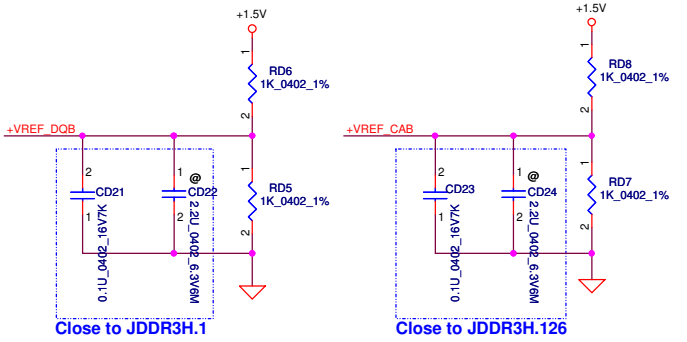
DDR3 SO-DIMM 1
Standard Type

JDDR3H



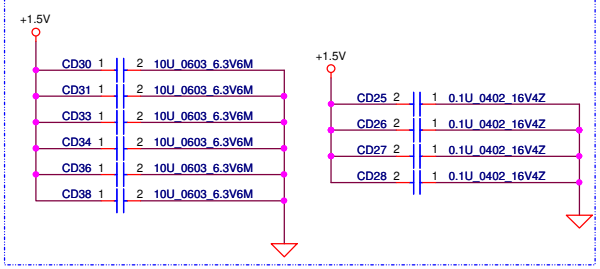
DDR_AB_DQS[0..7] <10,5>
DDR_AB_DQS#[0..7] <10,5>
DDR_AB_D[0..63] <10,5>
DDR_AB_DM[0..7] <10,5>
DDR_AB_MA[0..15] <10,5>

SO-DIMM VREF

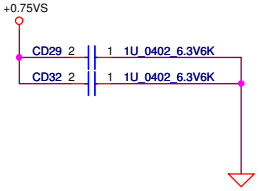


Layout Note:
Place near JDDR3H

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



Layout Note:
Place near JDDRH.203 and 204



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Title: ***DDRIII-SODIMMB***

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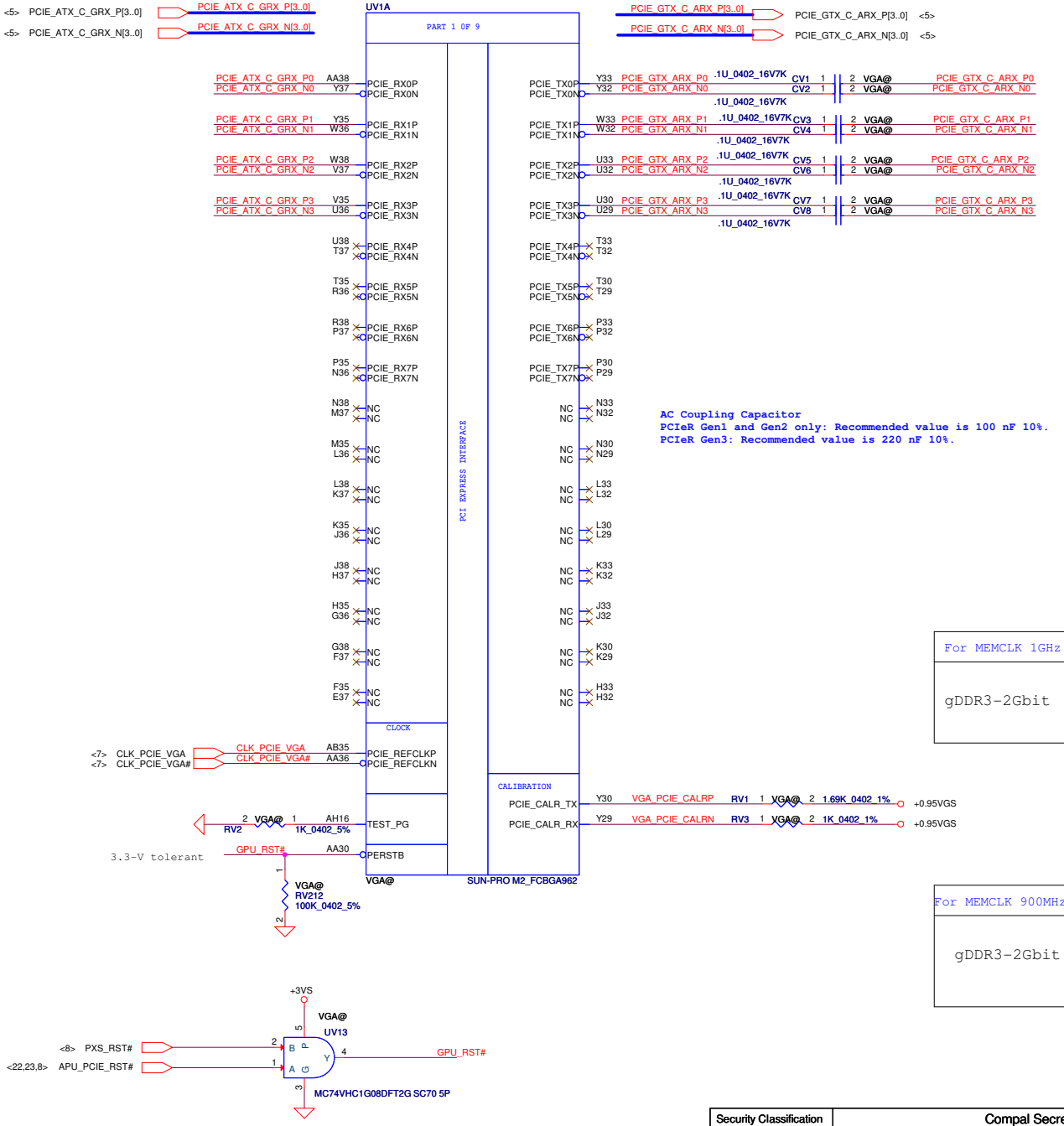
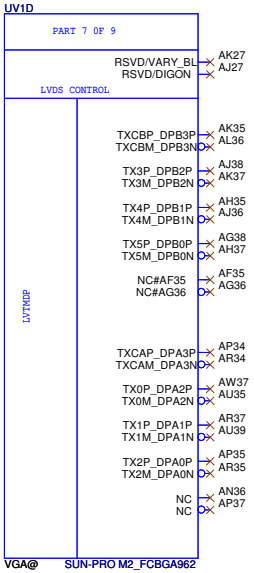


LVDS Interface



For MEMCLK 1GHz	Brand	Description	Comment	PS_3[3:1]	R_pu(ohm)	R_pd(ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-N0C	1.5V/1GHz	000	NC	4750
	Samsung	K4W2G1646E-BC1A	1.5V/1GHz	111	4750	NC

For MEMCLK 900MHz	Brand	Description	Comment	PS_3[3:1]	R_pu(ohm)	R_pd(ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-11C	1.5V/900MHz	000	NC	4750
	Micron	MT41K128M16JT-107G:K	1.35V/900MHz 1.5V/900MHz	001	8450	2000
	Samsung	K4W2G1646E-BC11	1.5V/900MHz	111	4750	NC

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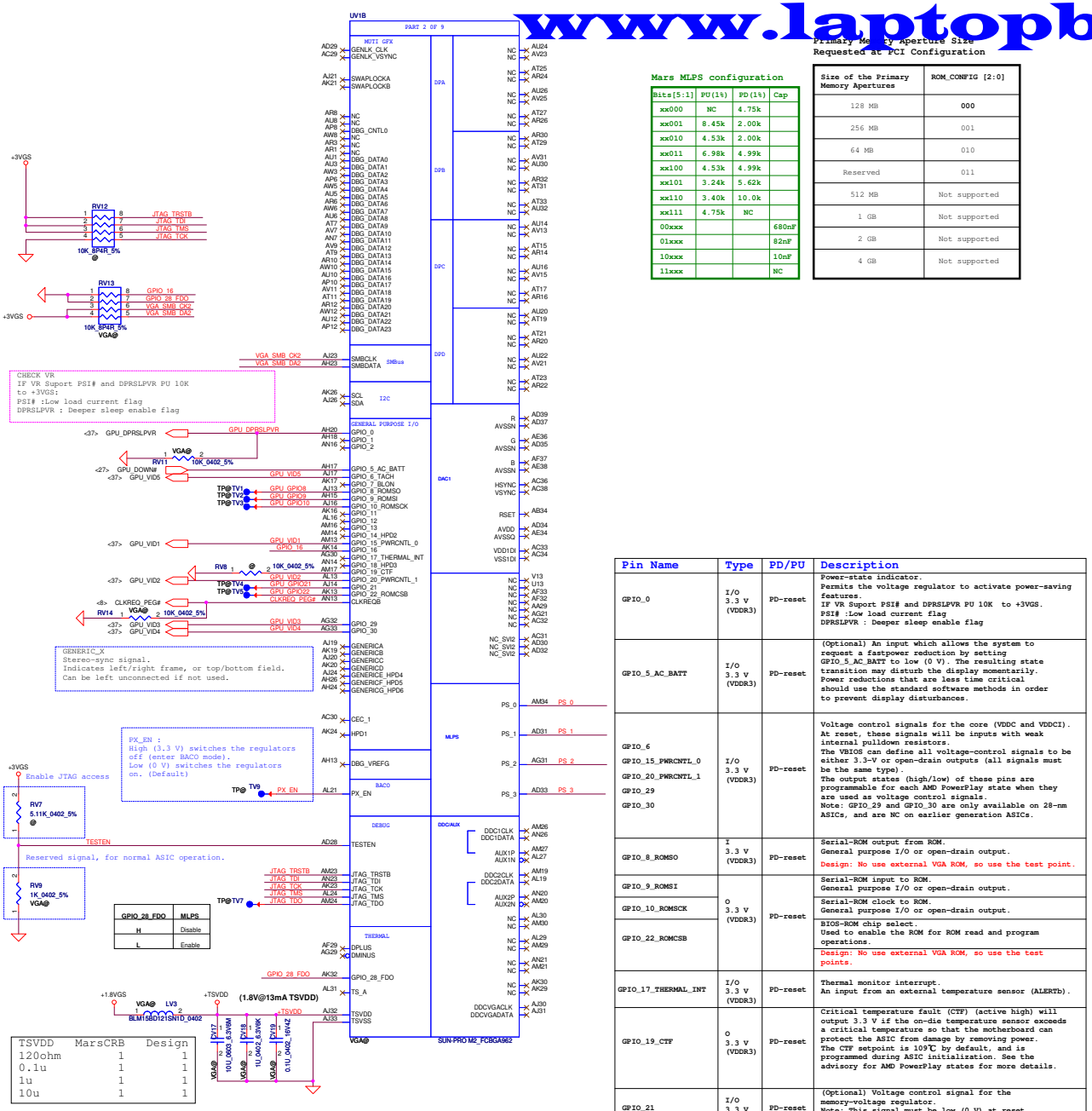


Mars MLPS configuration

Bits[5:1]	PU(1%)	PD(1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

Primary Memory Aperture Size Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG [2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not supported
1 GB	Not supported
2 GB	Not supported
4 GB	Not supported

MLPS

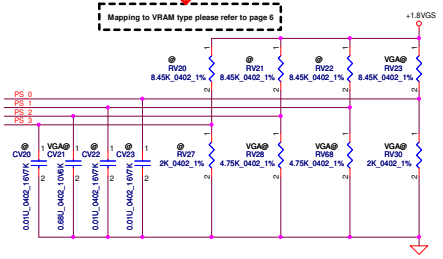
MLPS Bit	Strap Name	Legacy	Description	Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	GPIO[13:11]	If BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. Refer to current databooks for details.	001
PS_0[4]	N/A	GENLK_VSYNC	Reserved for internal use only. Must be 1 at reset.	1
PS_1[1]	STRAP_BIF_ GEN3_EN_A	GPIO_2	Re-defined strap to indicate PCIe GEN3 capability. 1 = PCIe GEN3 supported. 0 = PCIe GEN3 not supported.	0
PS_1[2]	STRAP_BIF_ CLK_PM_EN	GPIO_8	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	GENLK_CLK	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	TX_PWRS_ENB	GPIO_0	Transmitter (Tx) power savings enable. 0 = 50% Tx output swing. 1 = Full Tx output swing.	1
PS_1[5]	TX_DEEMPH_EN	GPIO_1	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	1
PS_2[1]	N/A	N/A	Reserved.	0
PS_2[2]	N/A	N/A	Reserved.	0
PS_2[3]	BIOS_ROM_EN	GPIO_22	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0
PS_2[4]	BIF_VGA_DIS	GPIO_9	VGA disable determines whether or not the card will be recognized as the system's VGA controller. 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	N/A	Reserved.	0
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	N/A	Board configuration related strapping (such as memory ID).	Base on VRAM ID
PS_0[5] PS_3[4] PS_3[5]	AUD_PORT_CONN_ PINSTRAP[0] AUD_PORT_CONN_ PINSTRAP[1] AUD_PORT_CONN_ PINSTRAP[2]	N/A	Together with PS_0[5] form the three-bit strap option to indicate the number of audio-capable display outputs. In a given ASIC there are as many endpoints as there are digital display outputs, though not all outputs are audio capable. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	111

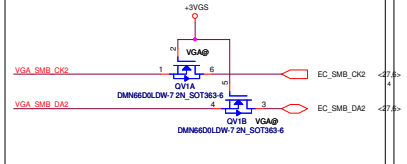
Pin Name	Type	PD/PU	Description
GPIO_0	I/O 3.3 V (VDDR3)	PD-reset	Power-state indicator. Permits the voltage regulator to activate power-saving features. IF VR Suport PSI# and DPRSLPVR PU 10K to +3VGS. PSI# :Low load current flag DPRSLPVR : Deeper sleep enable flag
GPIO_5_AC_BATT	I/O 3.3 V (VDDR3)	PD-reset	(Optional) An input which allows the system to request a fastpower reduction by setting GPIO_5_AC_BATT to low (0 V). The resulting state transition may disturb the display momentarily. Power reductions that are less time critical should use the standard software methods in order to prevent display disturbances.
GPIO_6 GPIO_15_PWRCNTL_0 GPIO_20_PWRCNTL_1 GPIO_29 GPIO_30	I/O 3.3 V (VDDR3)	PD-reset	Voltage control signals for the core (VDDC and VDDCI). At reset, these signals will be inputs with weak internal pulldown resistors. The VBIOS can define all voltage-control signals to be either 3.3-V or open-drain outputs (all signals must be the same type). The output states (high/low) of these pins are programmable for each AMD PowerPlay state when they are used as voltage control signals. Note: GPIO_29 and GPIO_30 are only available on 28-nm ASICs, and are NC on earlier generation ASICs.
GPIO_8_ROMSO	I 3.3 V (VDDR3)	PD-reset	Serial-ROM output from ROM. General purpose I/O or open-drain output. Design: No use external VGA ROM, so use the test point.
GPIO_9_ROMSI	O 3.3 V (VDDR3)	PD-reset	Serial-ROM input to ROM. General purpose I/O or open-drain output.
GPIO_10_ROMSCK			Serial-ROM clock to ROM. General purpose I/O or open-drain output.
GPIO_22_ROMCSB			BIOS-ROM chip select. Used to enable the ROM for ROM read and program operations. Design: No use external VGA ROM, so use the test points.
GPIO_17_THERMAL_INT	I/O 3.3 V (VDDR3)	PD-reset	Thermal monitor interrupt. An input from an external temperature sensor (ALERTb).
GPIO_19_CTF	O 3.3 V (VDDR3)	PD-reset	Critical temperature fault (CTF) (active high) will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power. The CTF setpoint is 109℃ by default, and is programmed during ASIC initialization. See the advisory for AMD PowerPlay states for more details.
GPIO_21	I/O 3.3 V (VDDR3)	PD-reset	(Optional) Voltage control signal for the memory-voltage regulator. Note: This signal must be low (0 V) at reset (failure to do so will prevent booting).
GPIO_28_FDO	I/O 3.3 V (VDDR3)	PD-reset	Disable MLPS: PU 10K ohm to 3.3V. (Do not install for Mars) Enable MLPS: PD 10K ohm to GND. (Install for Mars)
CLKREQB	O		Supports the CLKREQB feature for saving power to turn on/off the REFCLK clock on the ASIC.
PX_EN	O	PD	On/off regulator switch in AMD PowerXpress? (switchable graphics) BACO mode. High (3.3 V) switches the regulators off (enter BACO mode). Low (0 V) switches the regulators on. (Default) PX_EN is tri-state before internal TEST_PG is asserted and PERSTb is deasserted.

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 6





Security Classification	Compal Secret Data	
Issued Date	2013/05/15	Deciphered Date 2015/09/27

Compal Electronics, Inc.

Title: Main_MSIC

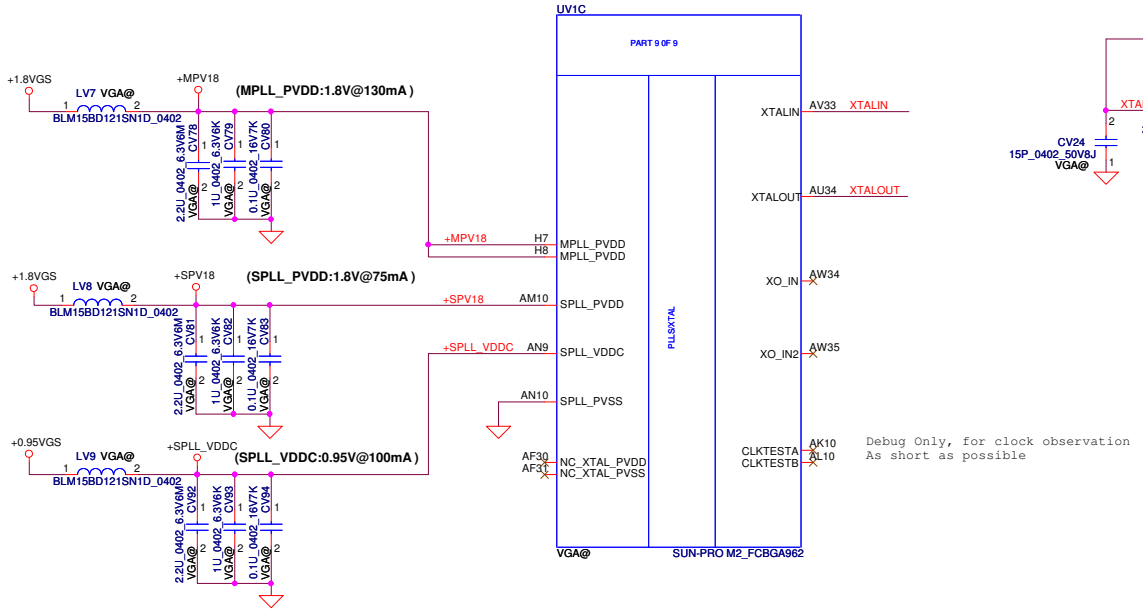
Size: Custom | Document Number: LA-A551P | Rev: 1.0

Date: Tuesday, July 16, 2013 | Sheet 13 of 40

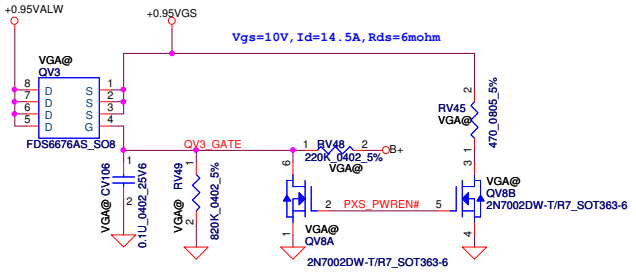
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

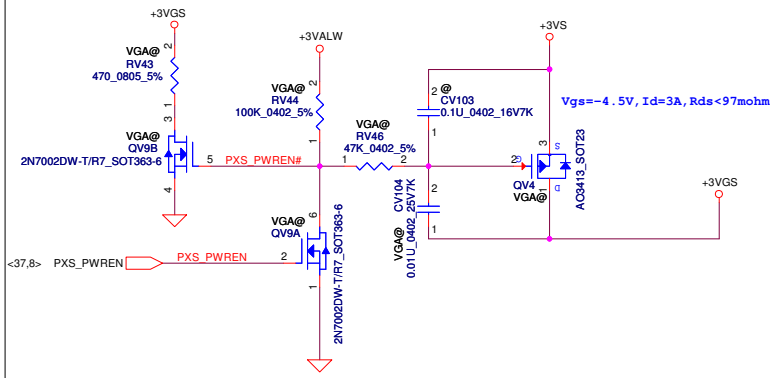
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1



+0.95VS to +0.95VGS



+3VS to +3VGS



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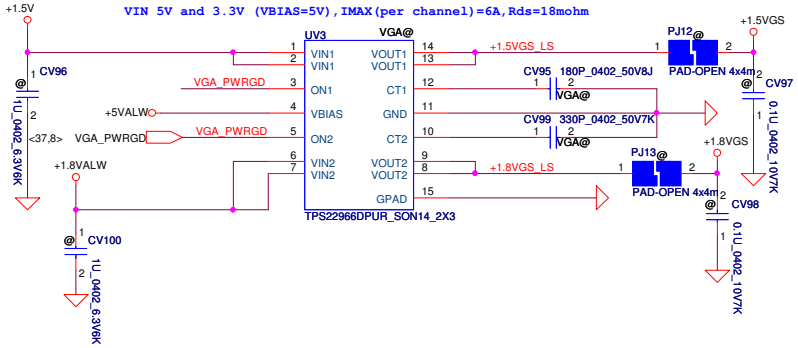
Issued Date	2013/05/15	Deciphered Date 2015/09/27	Title BACO POWER
Size Custom	Document Number LA-A551P		Rev 1.0
Date: Tuesday, July 16, 2013	Sheet 14 of 40		

Only for Kabini

+1.8VALW to +1.8VGS
+1.5V to +1.5VGS



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/05/15	Deciphered Date 2015/09/27	Title: BACO POWER
Size: Custom	Document Number: LA-A551P		Rev: 1.0
Date: Tuesday, July 16, 2013	Sheet 15 of 40		

VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	0
2.2u	5	5
10u	3	3

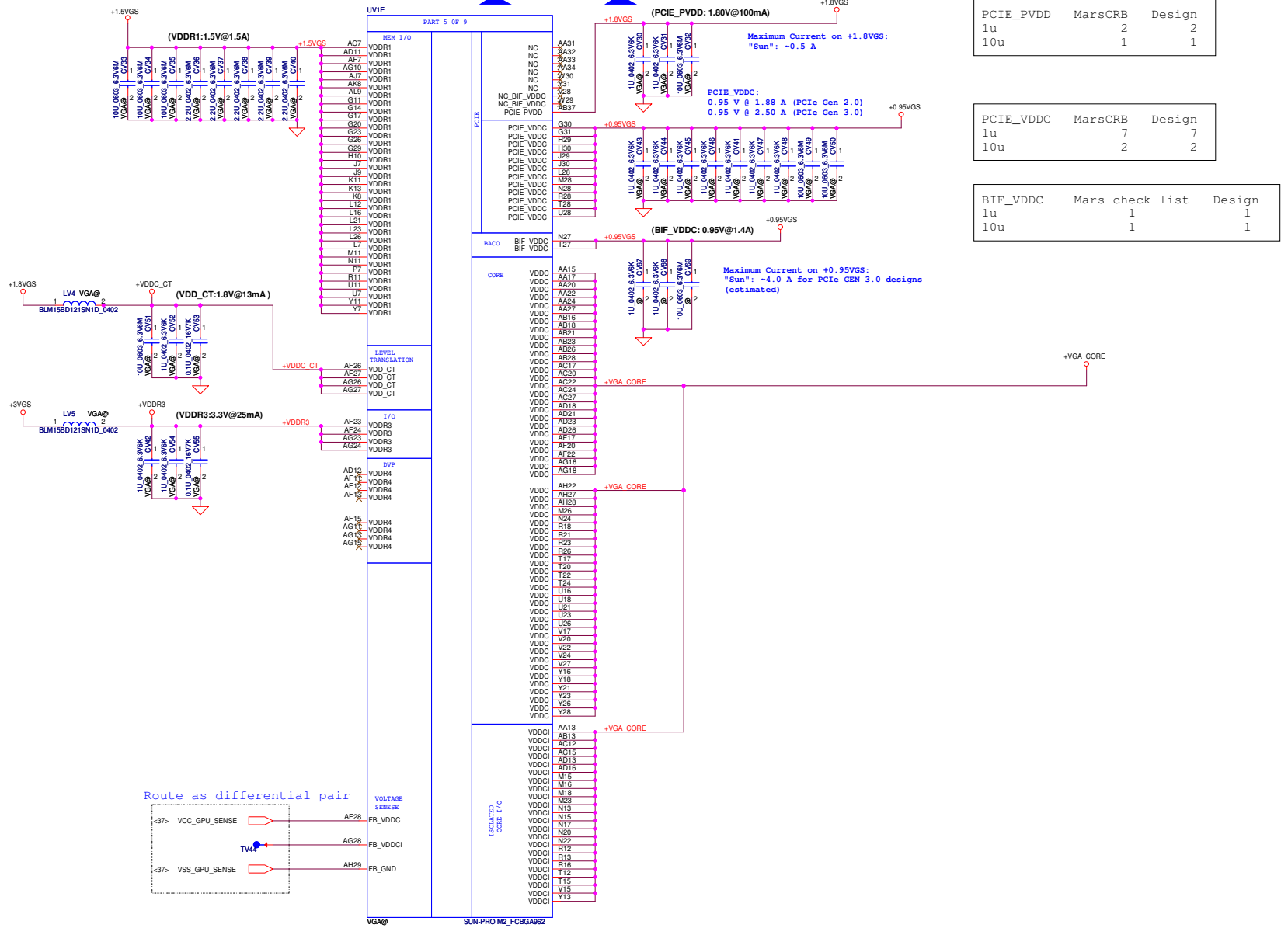
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDDR3	Mars check list	Design
120ohm	1	1
1u	3	2
10u	1	0
0.1u	0	1

PCIE_PVDD	MarsCRB	Design
1u	2	2
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	7
10u	2	2

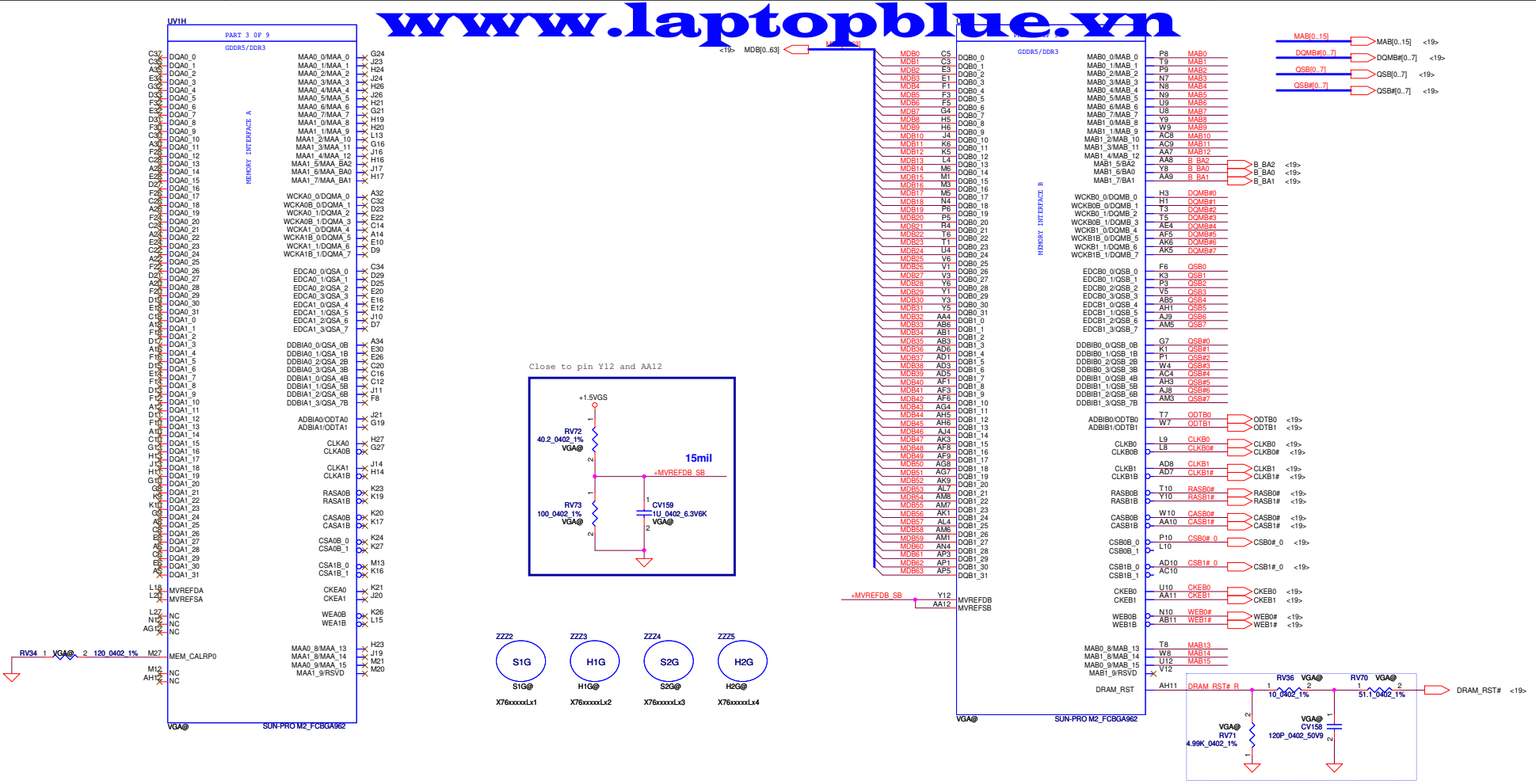
BIF_VDDC	Mars check list	Design
1u	1	1
10u	1	1



Need check all power current and decoupling capacitors after got SUN databook and reference schematic.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/05/15	Deciphered Date	2015/09/27

Title	Power		
Size C	Document Number LA-A551P		Rev 1.0
Date: Tuesday, July 16, 2013		Sheet 16 of 40	



Memory clock 900MHz

R_pu & R_pd resistor:
0402 1% resistors are required.

GPU Type	Memory Bus Width	VRAM Vendor	Compal P/N	Manufacturer P/N	X76 P/N	Size per part	Configuration	Total Memory Size/Qty	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
SUN PRO-M2	64bit	Samsung	SA000068U20	K4W2G1646E-BC1A		2Gbit	128M*16	1GB/4pcs	0	0	0	RV20 NC	RV27 4.75K
SUN PRO-M2	64bit	Micron	SA00005XB00	MT41K128M16JT-107G:K		2Gbit	128M*16	1GB/4pcs	0	0	1	RV20 8.45K	RV27 2K
SUN PRO-M2	64bit	Samsung	SA00005SH00	K4W2G1646E-BC11		2Gbit	128M*16	1GB/4pcs	0	1	0	RV20 4.53K	RV27 2K
SUN PRO-M3	64bit	Micron	SA000065D30	MT41K256M16HA-107G:E		4Gbit	128M*16	2GB/4pcs	1	1	0	RV20 3.4K	RV27 10K
SUN PRO-M4	64bit	Samsung	SA000068R20	K4W4G1646B-HC11		4Gbit	128M*16	2GB/4pcs	1	1	1	RV20 4.75K	RV27 NC

Place all these components close to GPU (Within 25mm) and keep all component close to each other

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Issued Date	2013/05/15	Deciphered Date 2015/09/27	Title: MEM Interface
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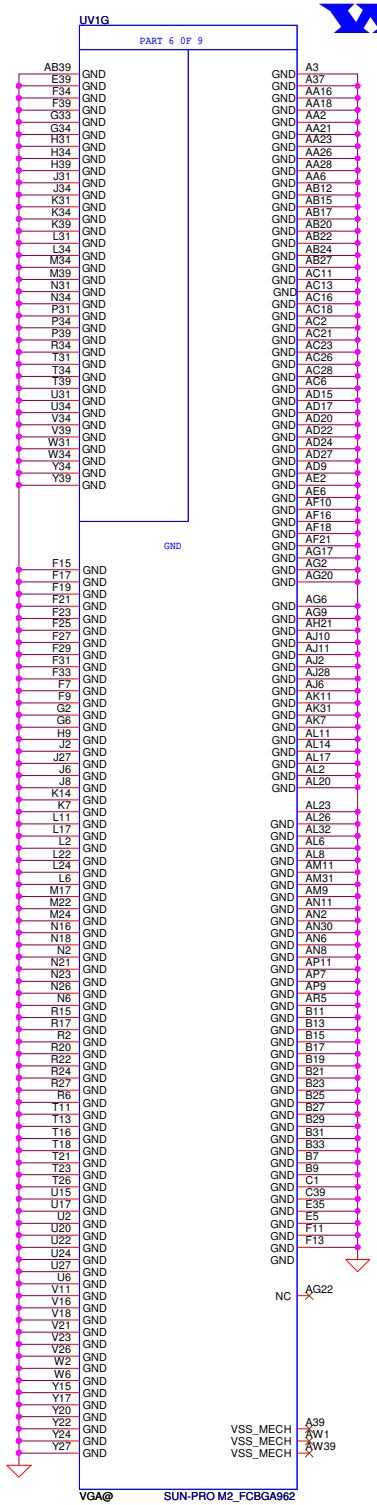
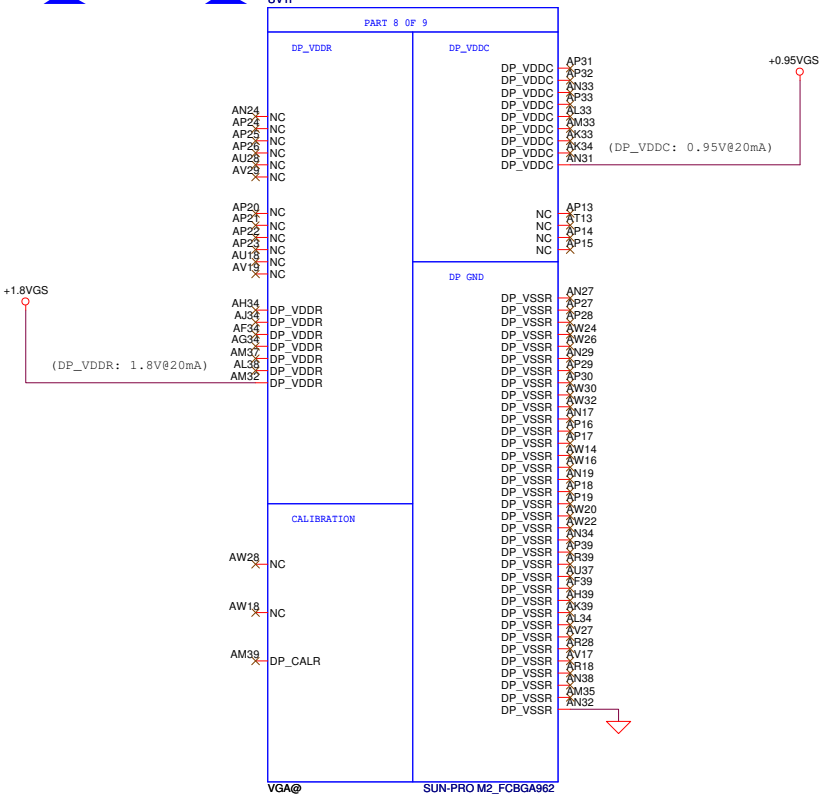
			Date: Tuesday, July 16, 2013; Sheet 17 of 40





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Issued Date	2013/05/15	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: PWR_GND

Size: Custom | Document Number: LA-A551P | Rev: 1.0

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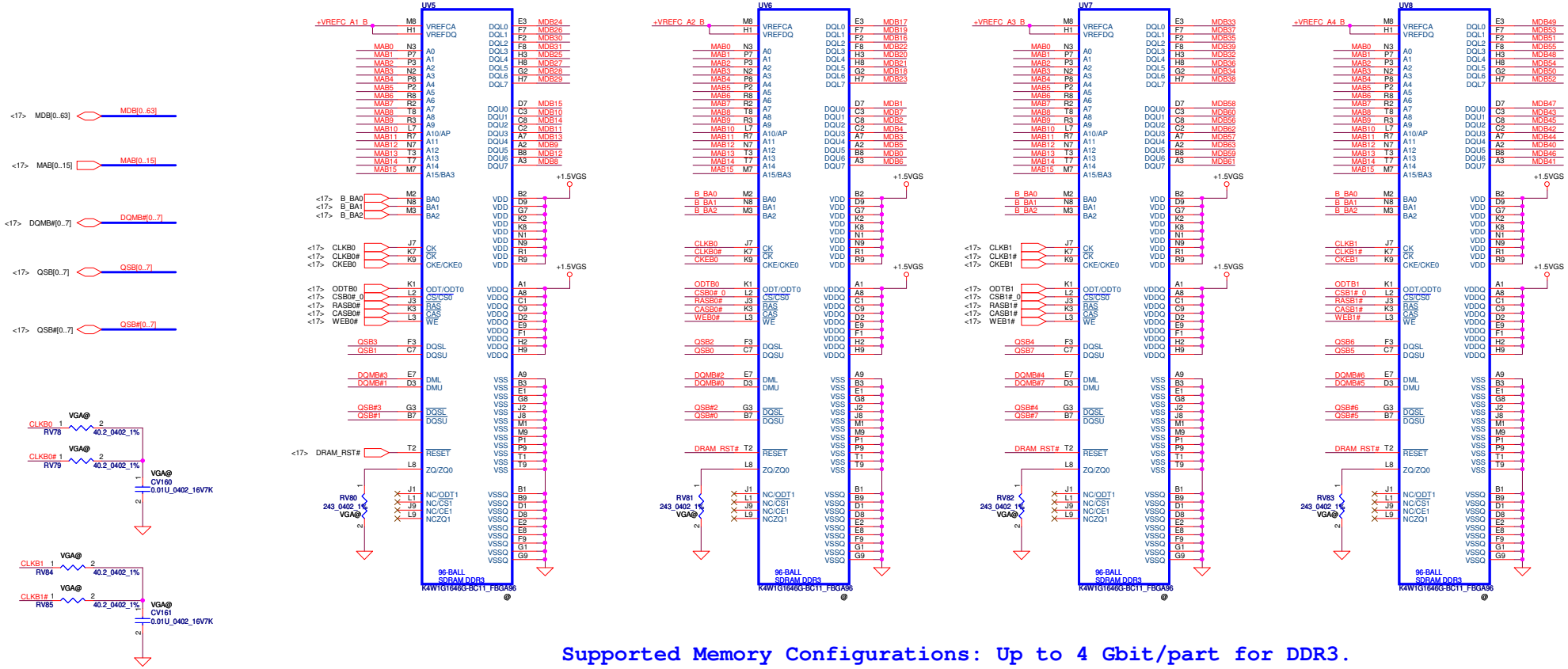
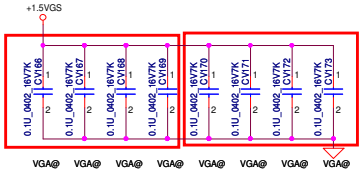
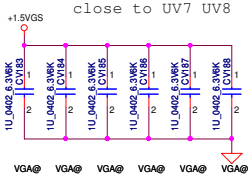
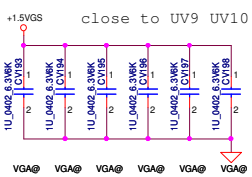


Supported Memory Configurations: Up to 4 Gbit/part for DDR3.







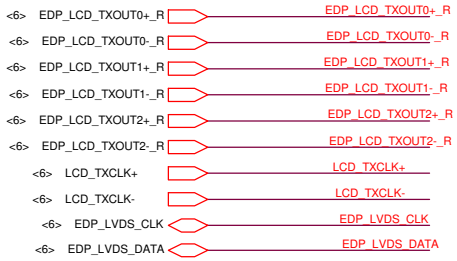
Security Classification	Compal Secret Data		
Issued Date	2013/05/15	Deciphered Date	2015/09/27

Compal Electronics, Inc.

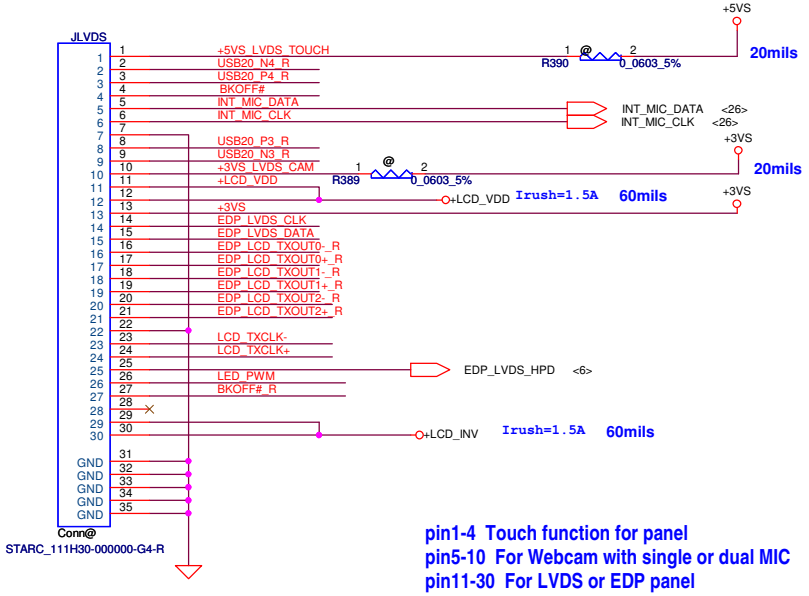
Title: VRAM Channel B

Size	Document Number	Rev
C	LA-A551P	1.0

Date: Tuesday, July 16, 2013 | Sheet 19 of 40

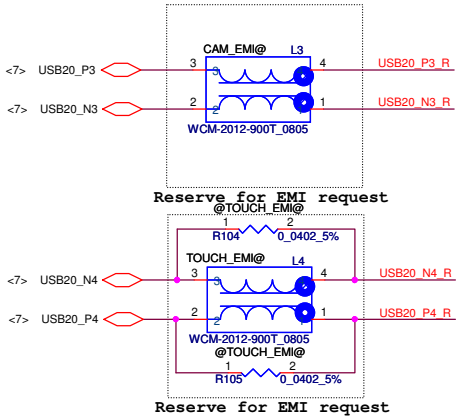


If it's EPD, they're become
LCD_TXOUT2+_R = EDP_TX0+
LCD_TXOUT2-_R = EDP_TX0-
LCD_TXOUT1+_R = EDP_TX1+
LCD_TXOUT1-_R = EDP_TX1-
LVDS_CLK = EDP_AUXP
LVDS_DATA = EDP_AUXN



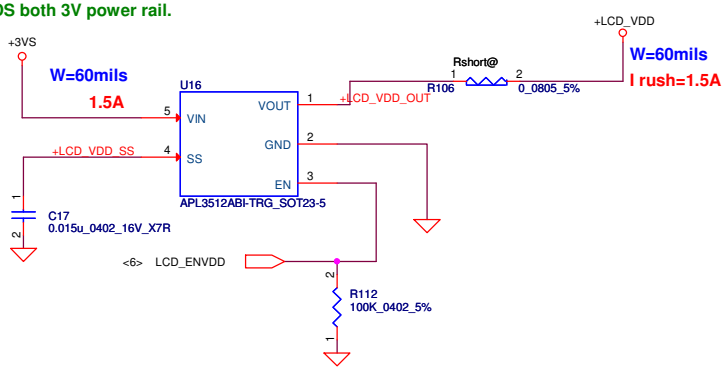
pin1-4 Touch function for panel
pin5-10 For Webcam with single or dual MIC
pin11-30 For LVDS or EDP panel

Carmera & Touch Screen

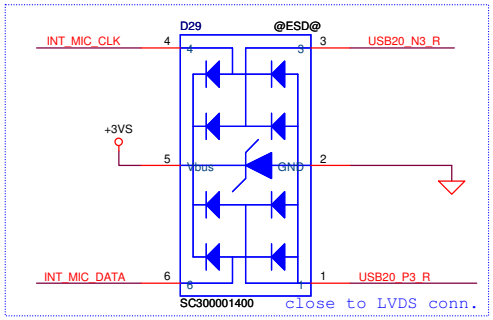


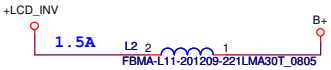
LCD_VDD

Need check eDP&LVDS both 3V power rail.

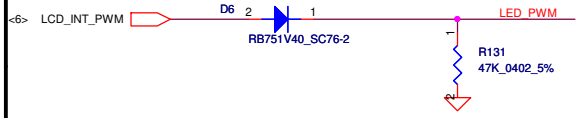


LCD_INV

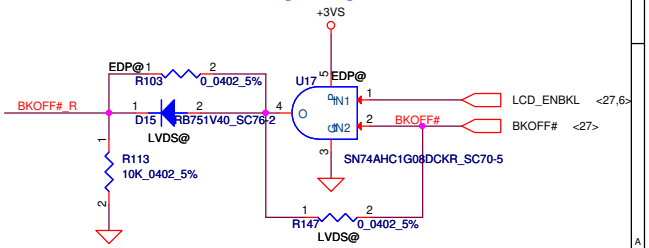




LCD Control

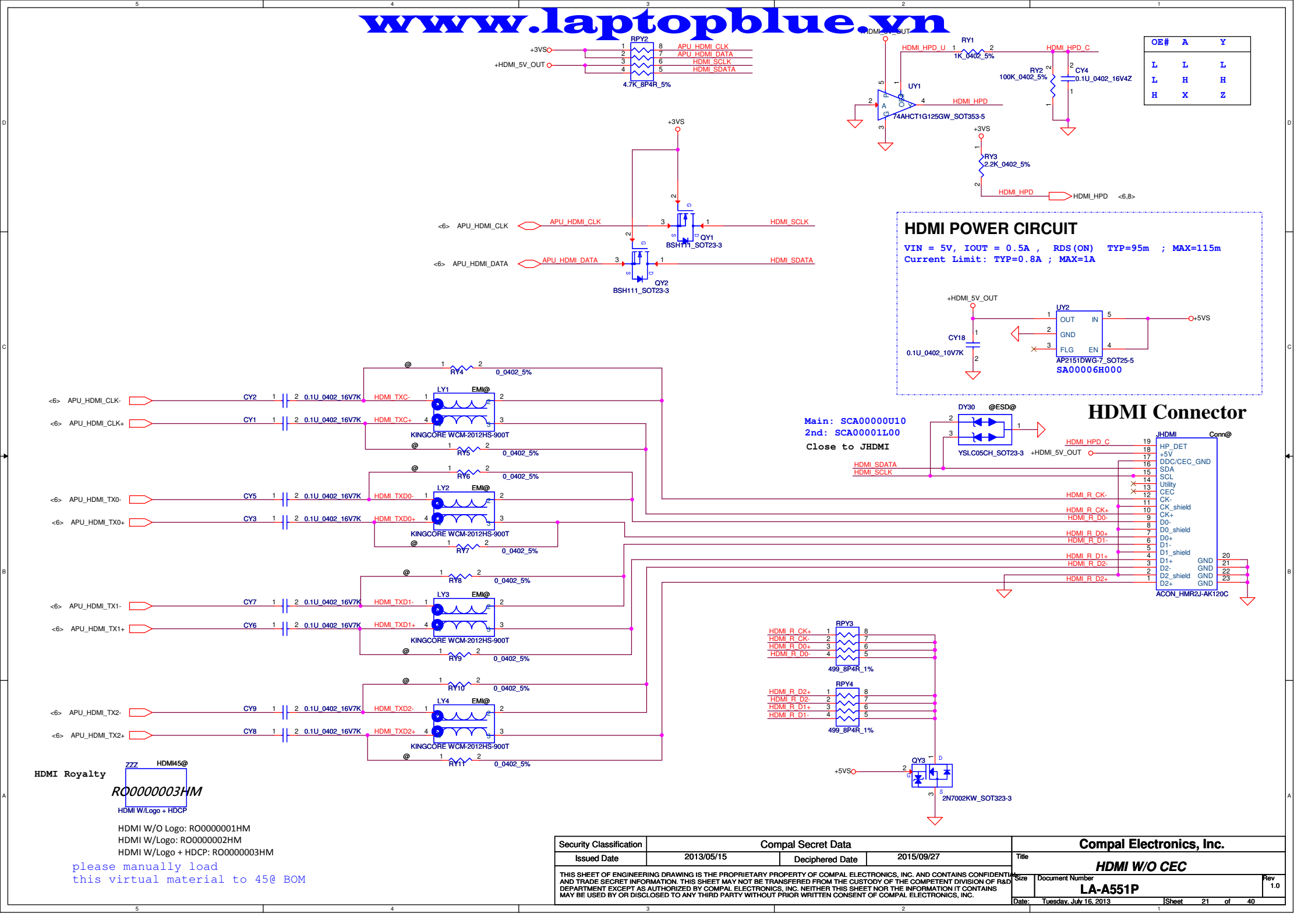


Reserve for eDP panel potential issue



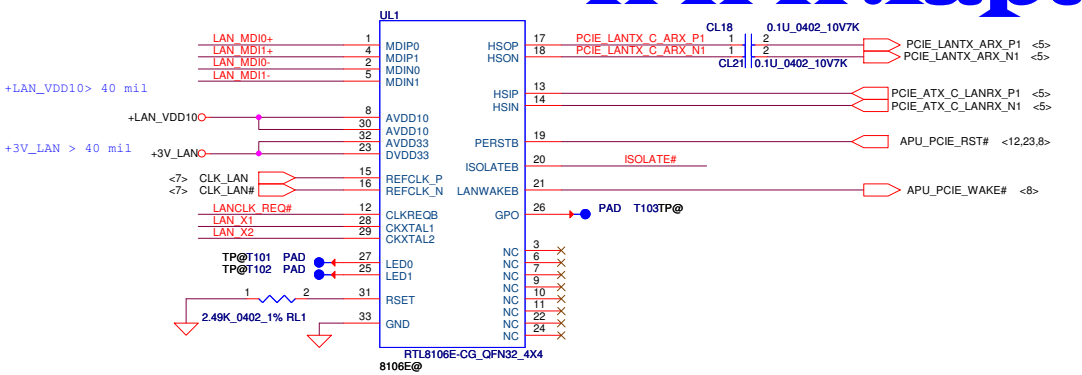
Security Classification	Compal Secret Data		
Issued Date	2013/05/15	Deciphered Date	2015/09/27

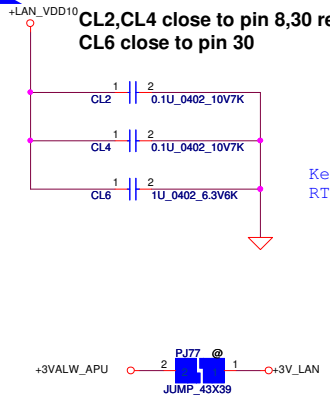
Compal Electronics, Inc.			
Title	LVDS/EDP W/ CAMERA		
Size	Document Number	LA-A551P	Rev 0.2
Date:	Tuesday, July 16, 2013	Sheet 20 of 40	

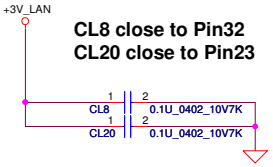


Security Classification	Compal Secret Data		
Issued Date	2013/05/15	Deciphered Date	2015/09/27

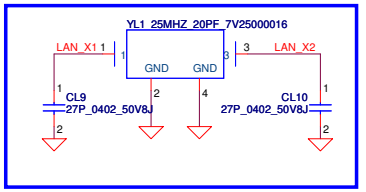
Compal Electronics, Inc.			
Title	HDMI W/O CEC		
Size	Document Number	LA-A551P	Rev 1.0
Date: Tuesday, July 16, 2013	Sheet 21 of 40		

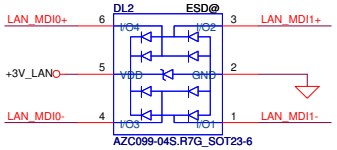




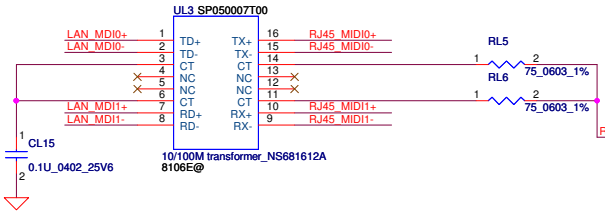


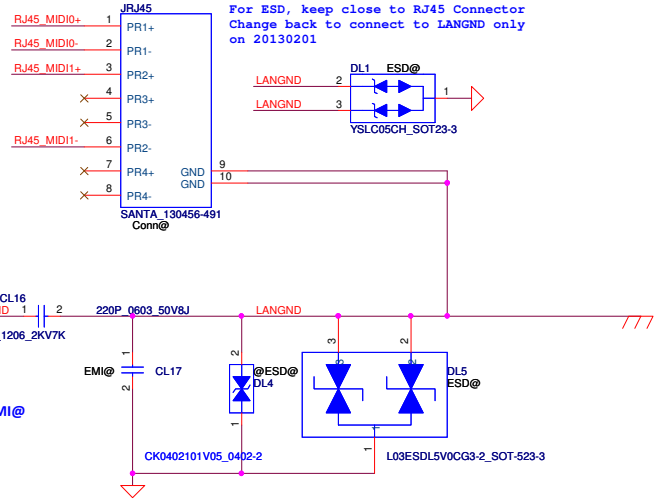
Keep de-coupling capacitors close to RTL8106E within 200 mil





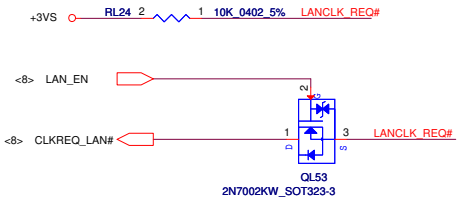
main: SP050007T00
2nd: SP050007K00
3nd: SP050006H00

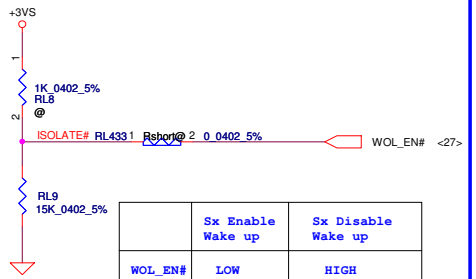




2013/5/3 EMI request change CL17 BOM structure to EMI@
2013/6/7 ESD request reserve DL14
2013/6/7 ESD request add DL5

For LAN function





	Sx Enable Wake up	Sx Disable Wake up
WOL_EN#	LOW	HIGH

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

Security Classification	Compal Secret Data		
Issued Date	2013/05/15	Deciphered Date	2015/09/27

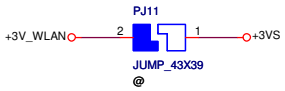
Compal Electronics, Inc.

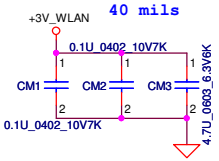
Title: PCIe-LAN-RTL8106E

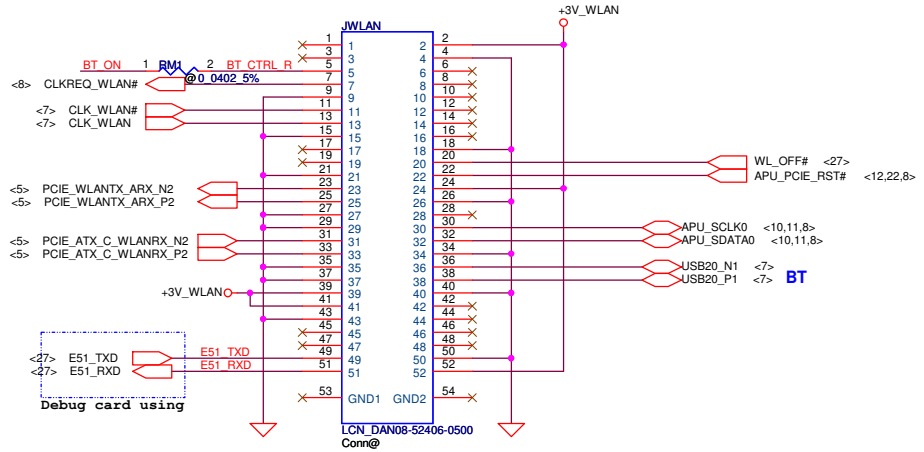
Size: Custom | Document Number: LA-A551P | Rev: 1.0

Date: Tuesday, July 16, 2013 | Sheet 22 of 40

Slot 1 Half PCIe Mini Card-WLAN

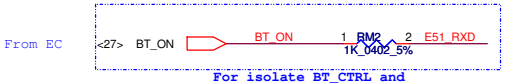




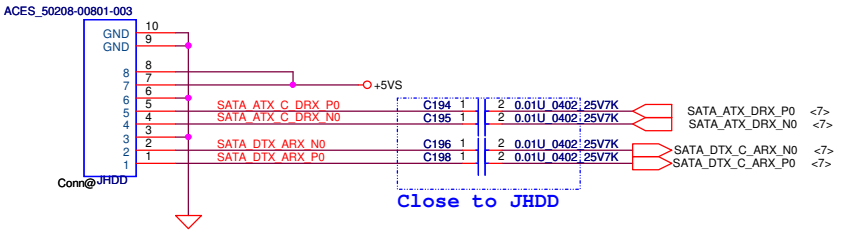


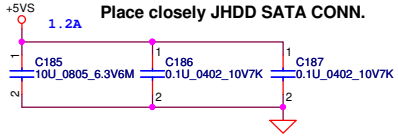
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L



SATA HDD Conn.





Security Classification	Compal Secret Data		
Issued Date	2013/05/15	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: ***WLAN/SATA HDD&ODD***

Size | Document Number: **LA-A551P** | Rev: 1.0

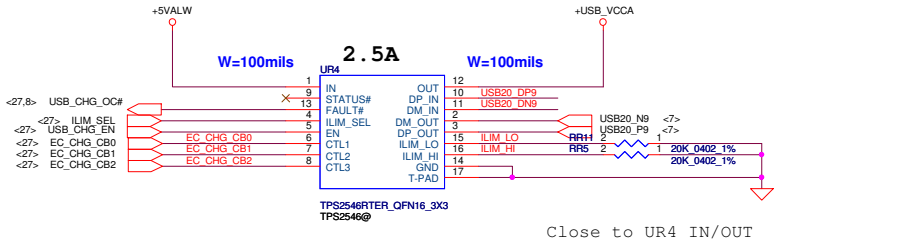
Date: Tuesday, July 16, 2013 | Sheet 23 of 40

USB Sleep & Charge

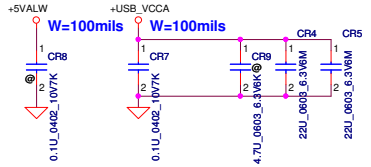
State table for TPS2546RTER

CB0	CB1	CB2	ILIM_SEL	Mode	STATUS
0	1	1	1	Auto/Alternate	Auto-detection charger mode for Apple device(2A,1A). Resistor dividers are connected to DP/DM. Including DCP
1	1	1	0	SDP	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	1	1	CDP	USB pass-through mode with CDP emulation. DP/DM are connected to TDP/TDM

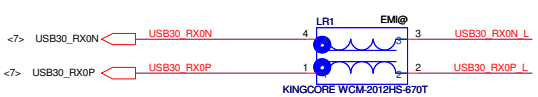
Right side USB 3.0 x 1 W/ Sleep&Charge

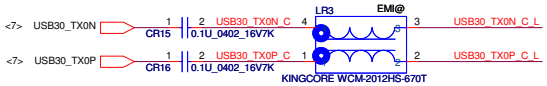


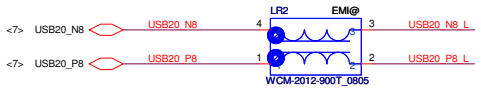
Close to UR4 IN/OUT

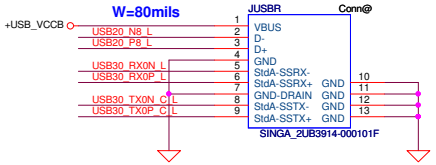


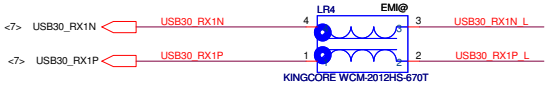
Right side USB 3.0 x 1

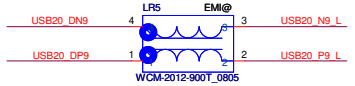




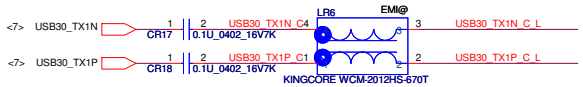


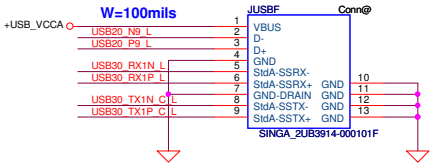




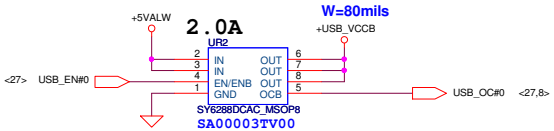


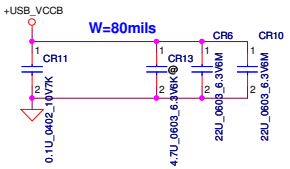
Sleep & Charge Port

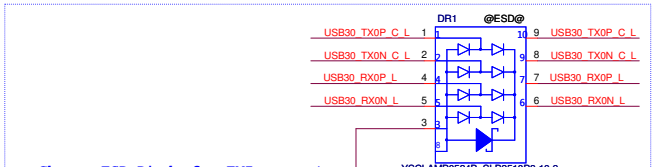


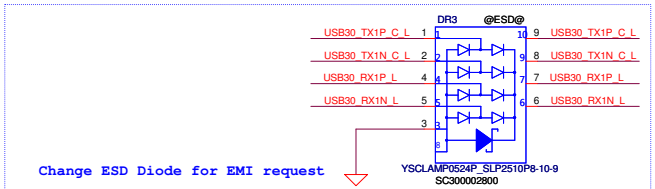


USB POWER SWITH









Security Classification	Compal Secret Data		
Issued Date	2013/05/15	Deciphered Date	2015/09/27

Compal Electronics, Inc.	
Title	LUSB/RUSB/S&C
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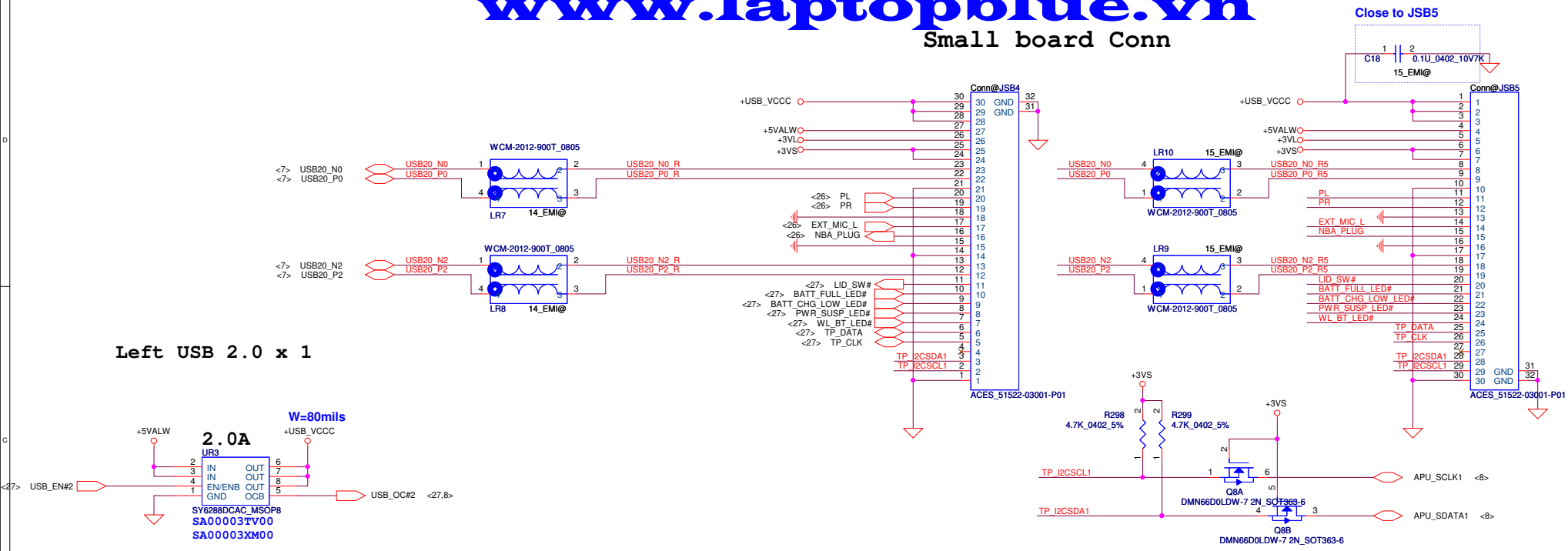
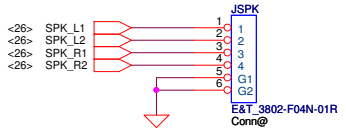
Small board Conn



Left USB 2.0 x 1

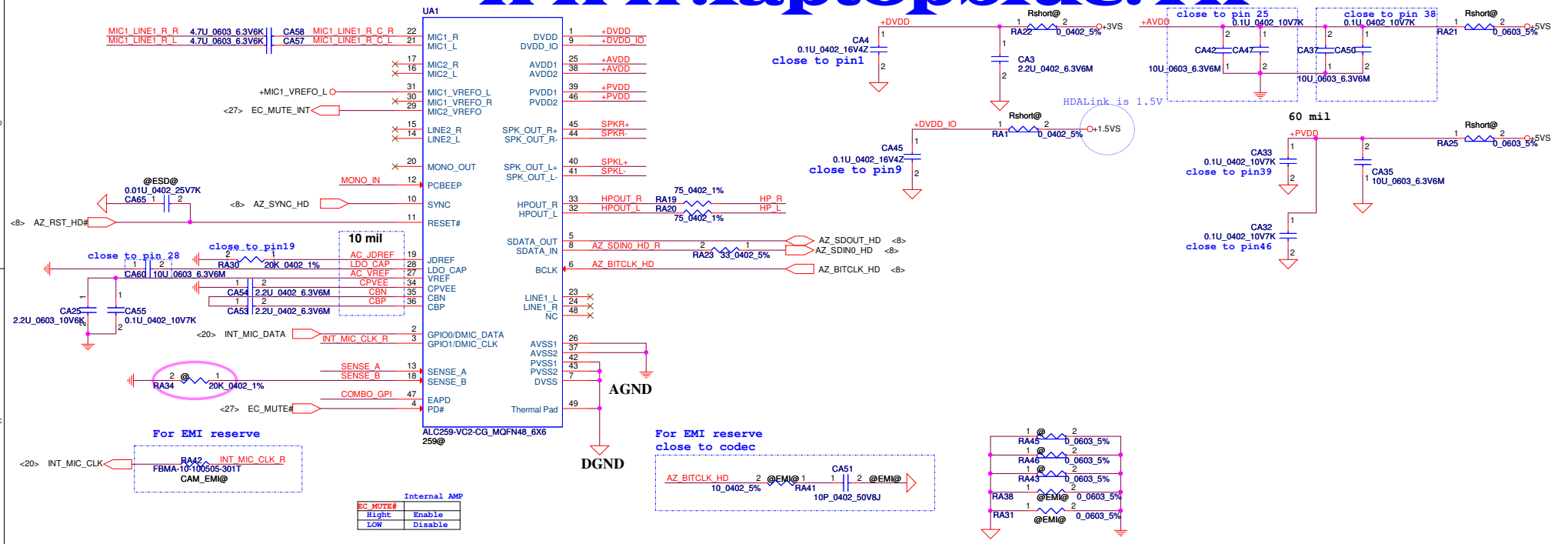
SPK Conn.



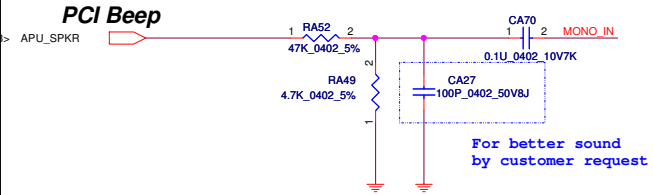
Security Classification	Compal Secret Data		
Issued Date	2013/05/15	Deciphered Date	2015/09/27

Compal Electronics, Inc.			
Title	USB-CardReader Genesys GL834L		
Size: Custom	Document Number: LA-A551P		Rev: 1.0
Date: Tuesday, July 16, 2013	Sheet 25 of 40		

650mA for 5V level



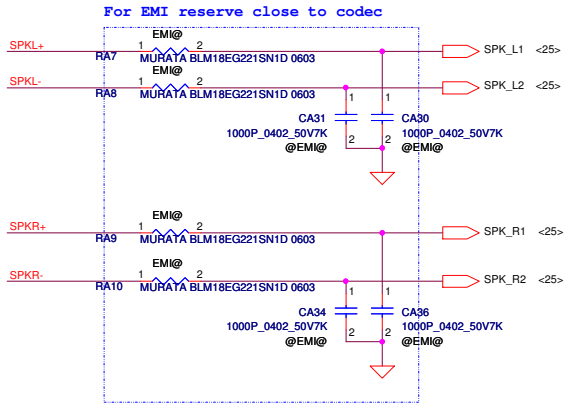
Beep sound



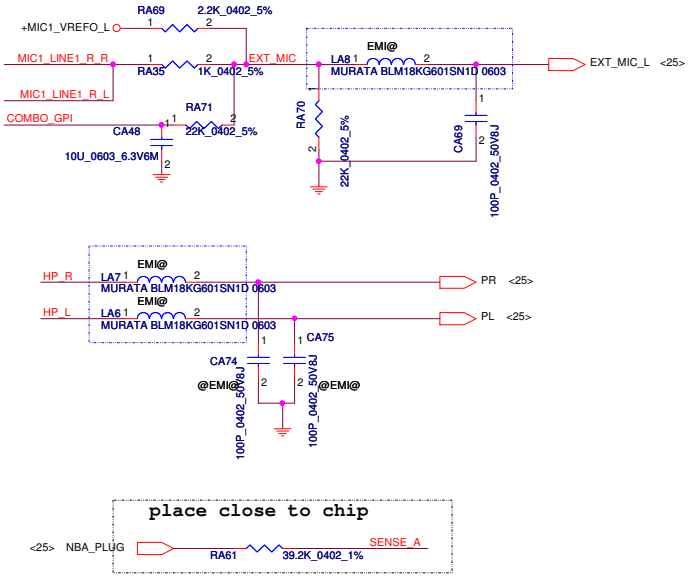
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

SPK

2W 4ohm =40mil
1W 8ohm =20mil



Combo Jack



Security Classification	Compal Secret Data		
Issued Date	2013/05/15	Deciphered Date	2015/09/27

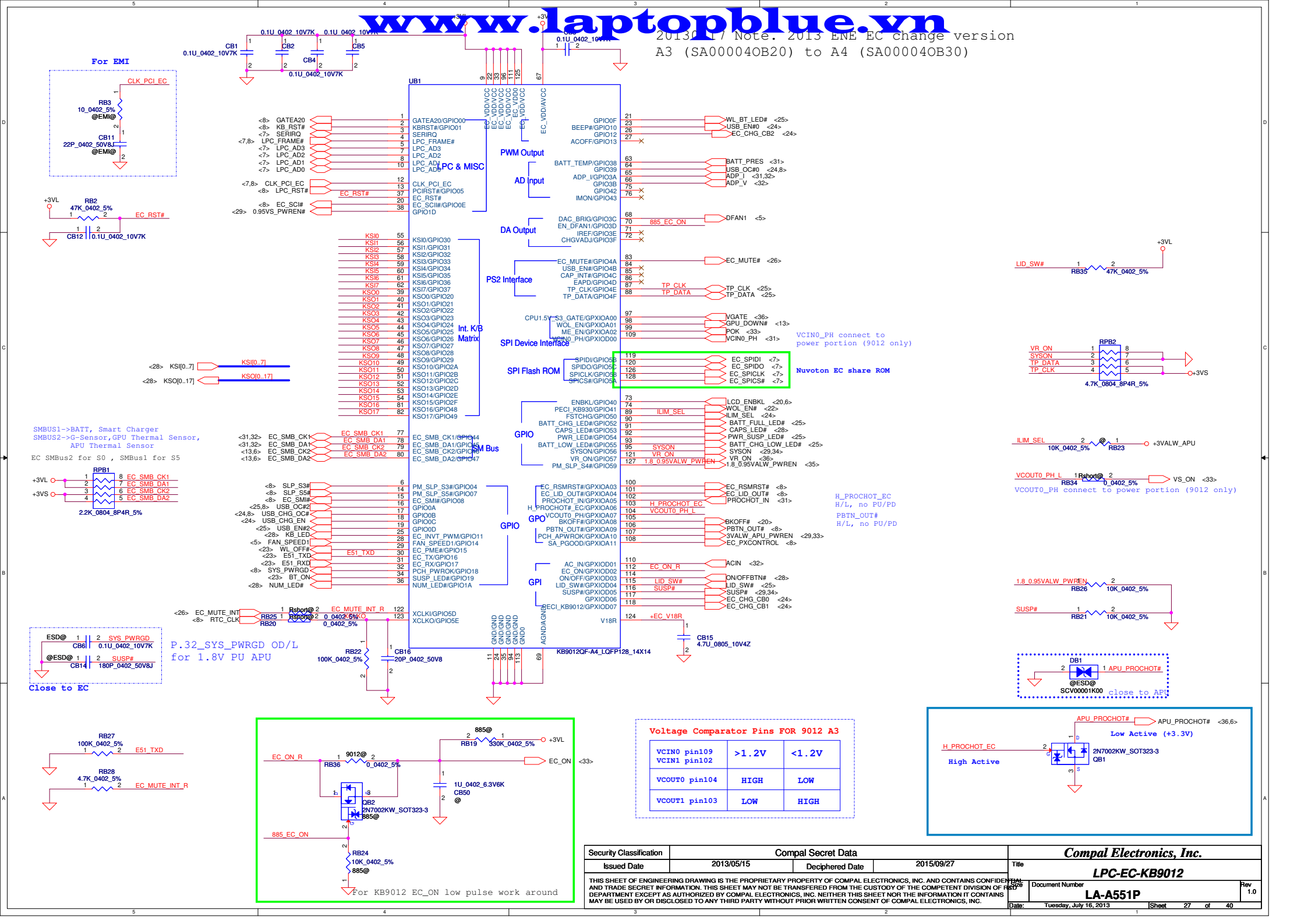
Compal Electronics, Inc.

Title: Cover Sheet

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, July 16, 2013 | Sheet 26 of 40

2013/5/17 Note: 2013 ENE EC change version
A3 (SA00004OB20) to A4 (SA00004OB30)



Security Classification	Compal Secret Data		
Issued Date	2013/05/15	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: LPC-EC-KB9012

Size: C | Document Number: LA-A551P | Rev: 1.0

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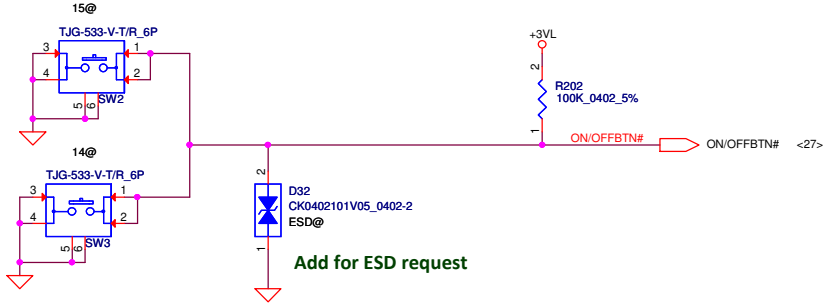
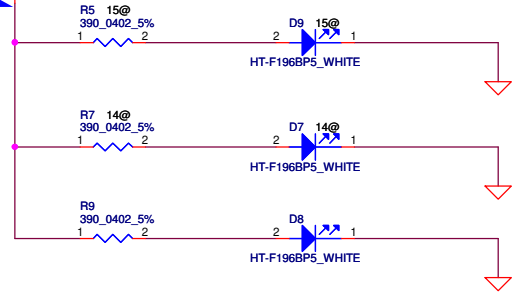
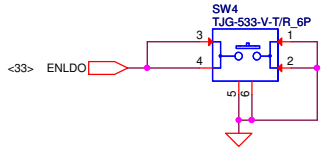
Power Button

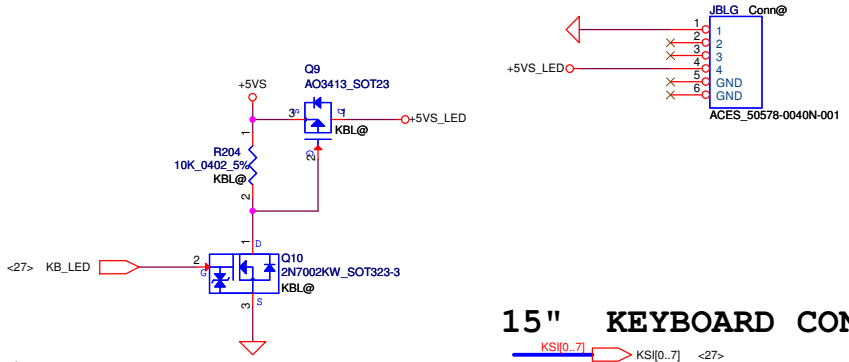




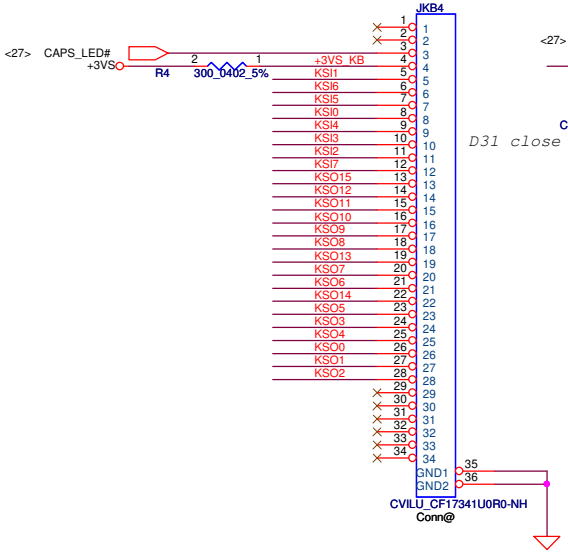
Battery Reset



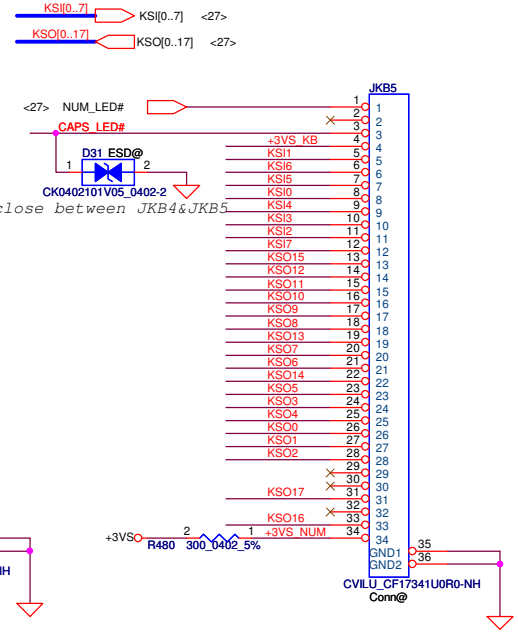
Keyboard LED



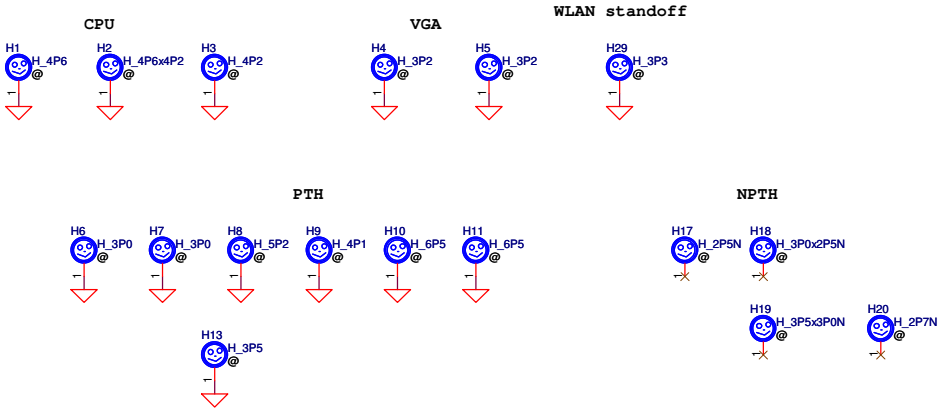
14" KEYBOARD CONN.



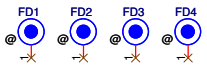
15" KEYBOARD CONN.



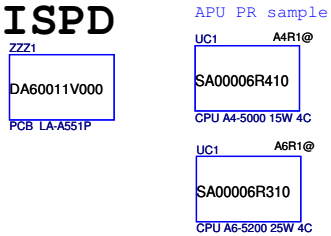
Screw Hole



PCB Fedical Mark PAD

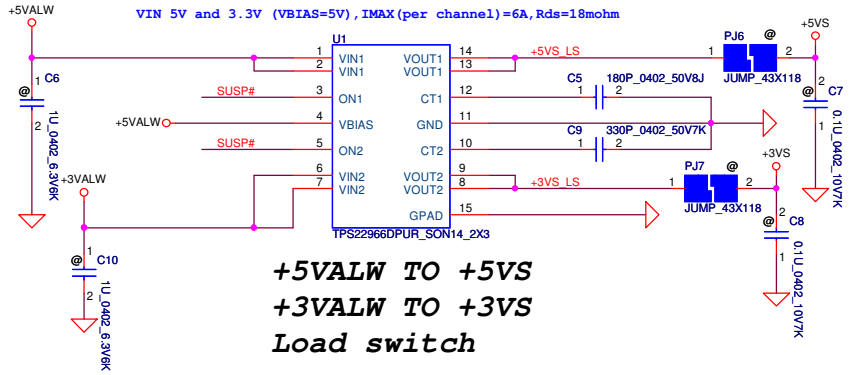


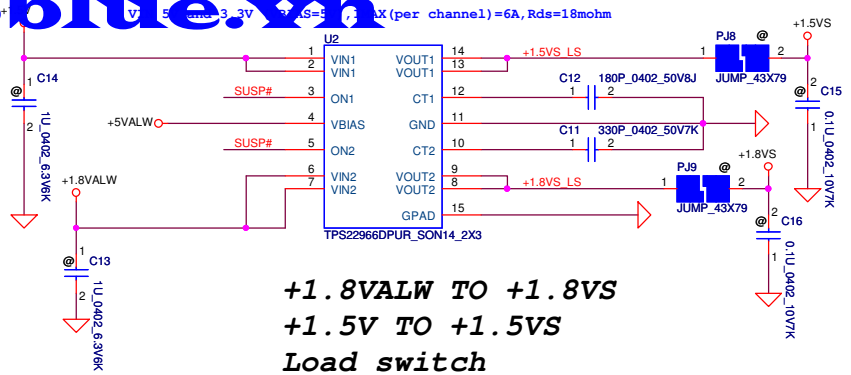
ISPD

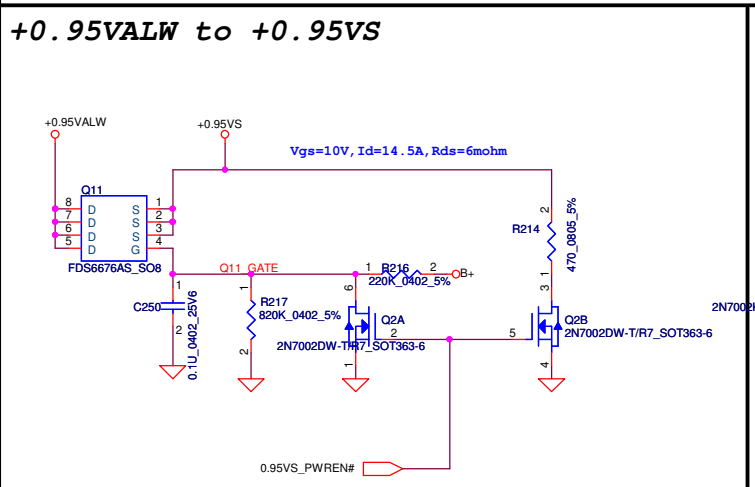


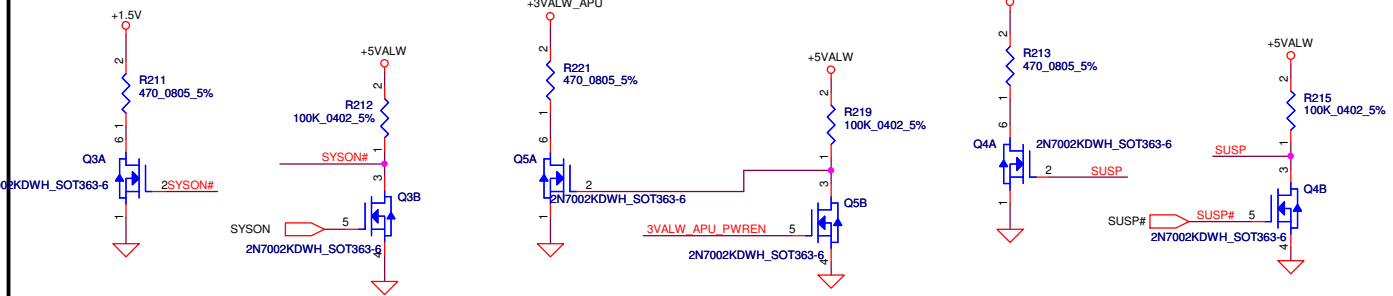
Security Classification	Compal Secret Data		
Issued Date	2013/05/15	Deciphered Date	2015/09/27

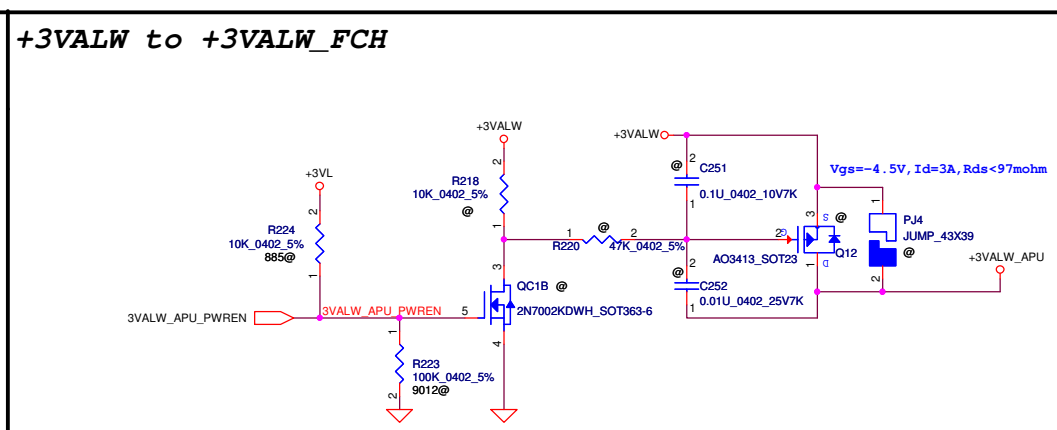
Compal Electronics, Inc.			
Title	KB/TP/LED/LID/DEBUG/ISPD		
Size	Document Number	LA-A551P	Rev 1.0
Date: Tuesday, July 16, 2013	Sheet 28 of 40		











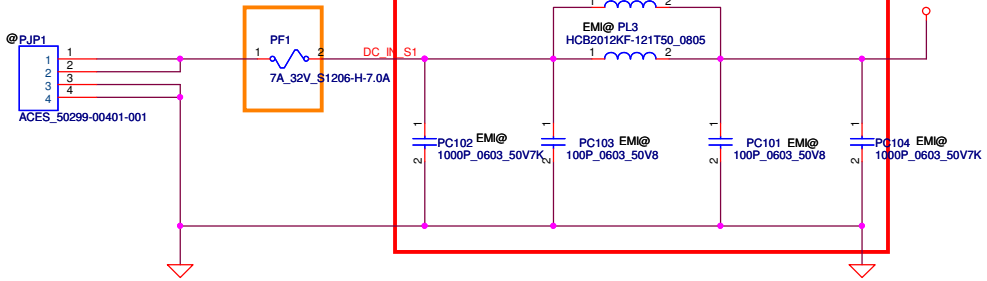
Security Classification	Compal Secret Data		
Issued Date	2013/05/15	Deciphered Date	2015/09/27

Compal Electronics, Inc.			
Title	DC TO DC INTERFACE		
Size	Document Number LA-A551P		Rev 1.0
Date: Tuesday, July 16, 2013	Sheet 29 of 40		

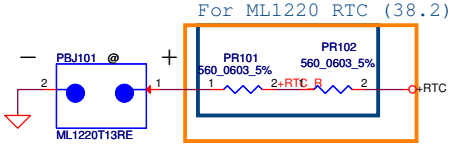
EMI Part (47.1)

Other component (37.1)

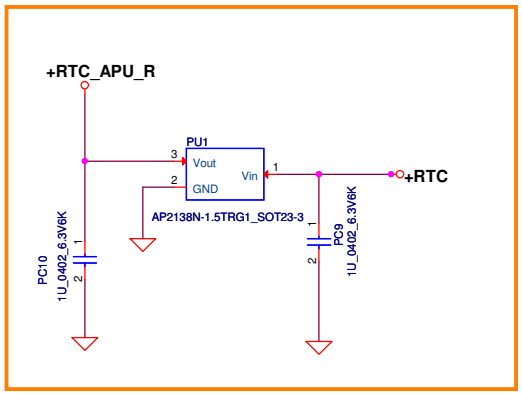
A51 need add fuse



For ML1220 RTC (38.2)



For RTC (38.2)



Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

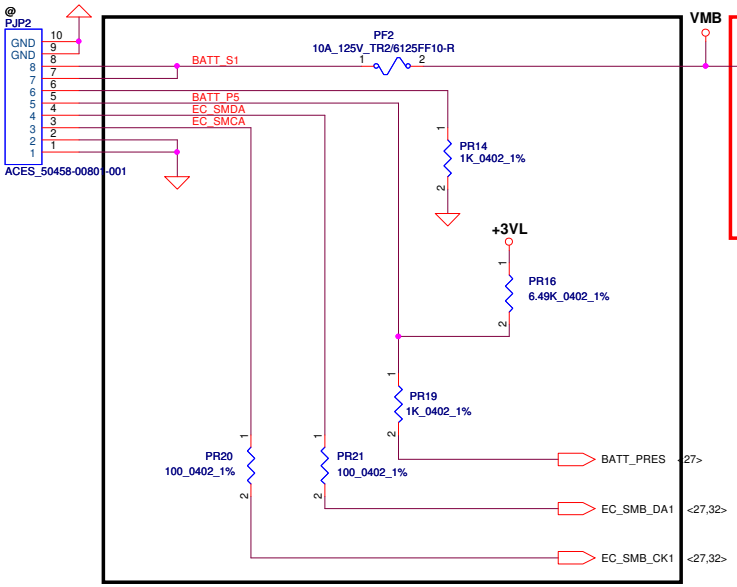
Compal Electronics, Inc.

Title: DCIN/PRECHARGE

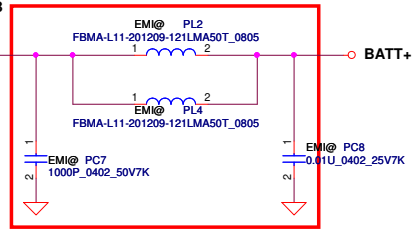
Size: Custom | Document Number: LA-A551P | Rev: 0.1

Date: | Sheet 30 of 40

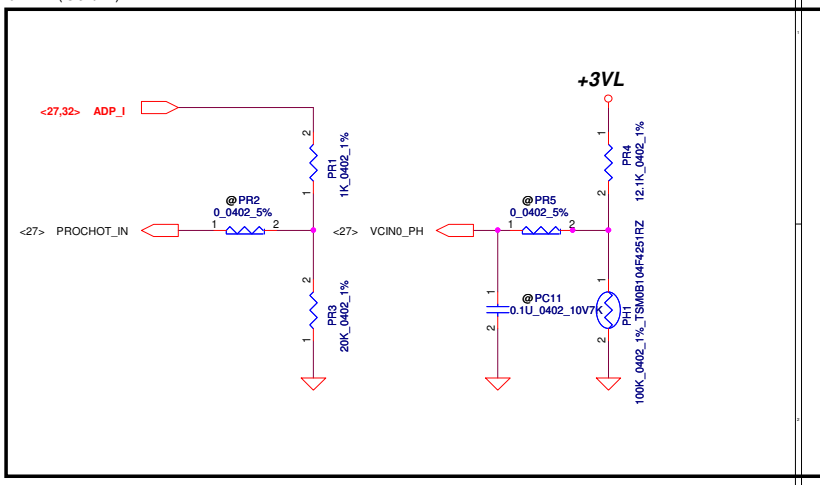
Other component (37.1)



EMI Part (47.1)



OTP (39.7)



Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

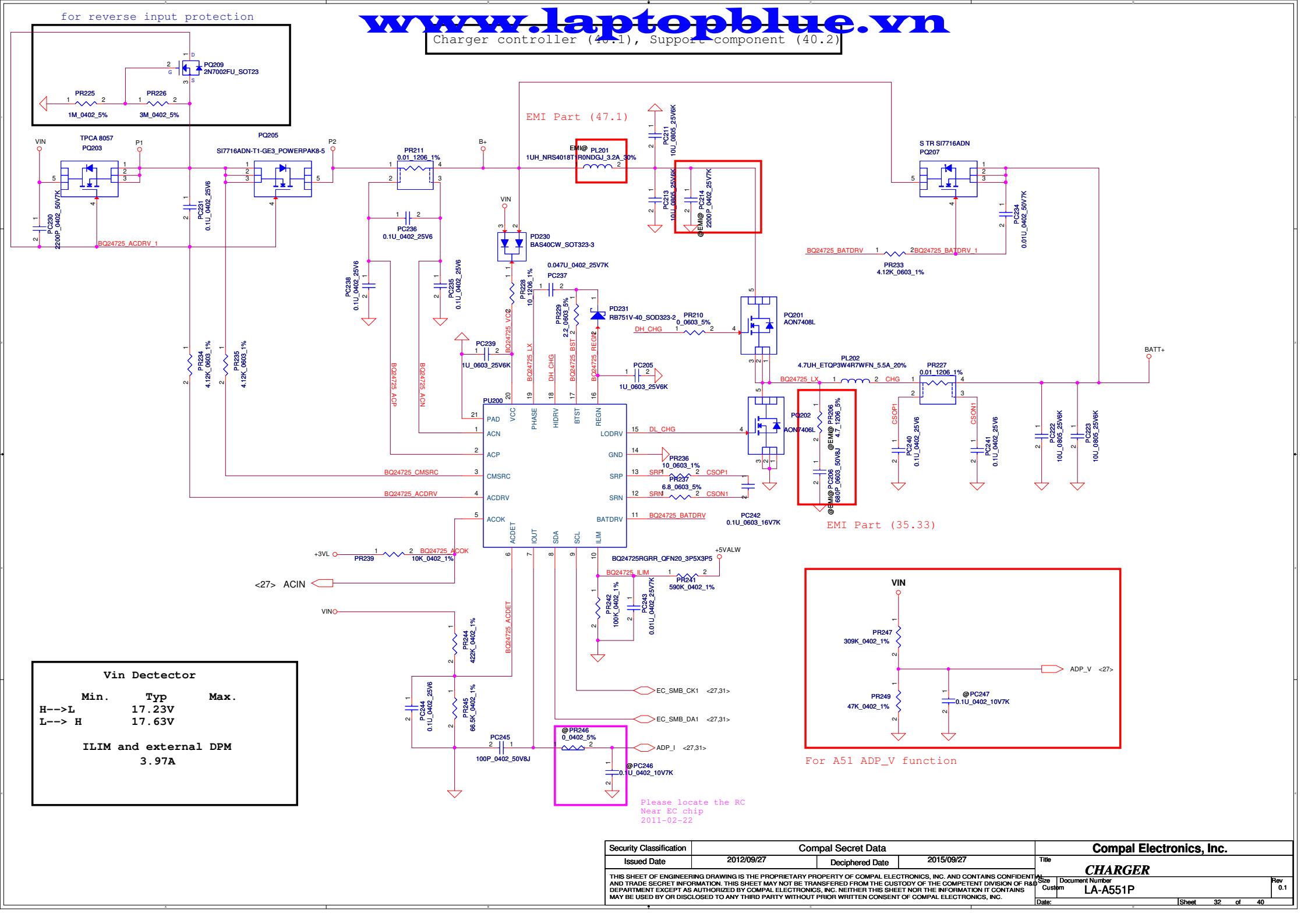
Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size: Custom | Document Number: LA-A551P | Rev: 0.1

Date: | Sheet 31 of 40

Charger controller (40.1), Support component (40.2)



Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.97A

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

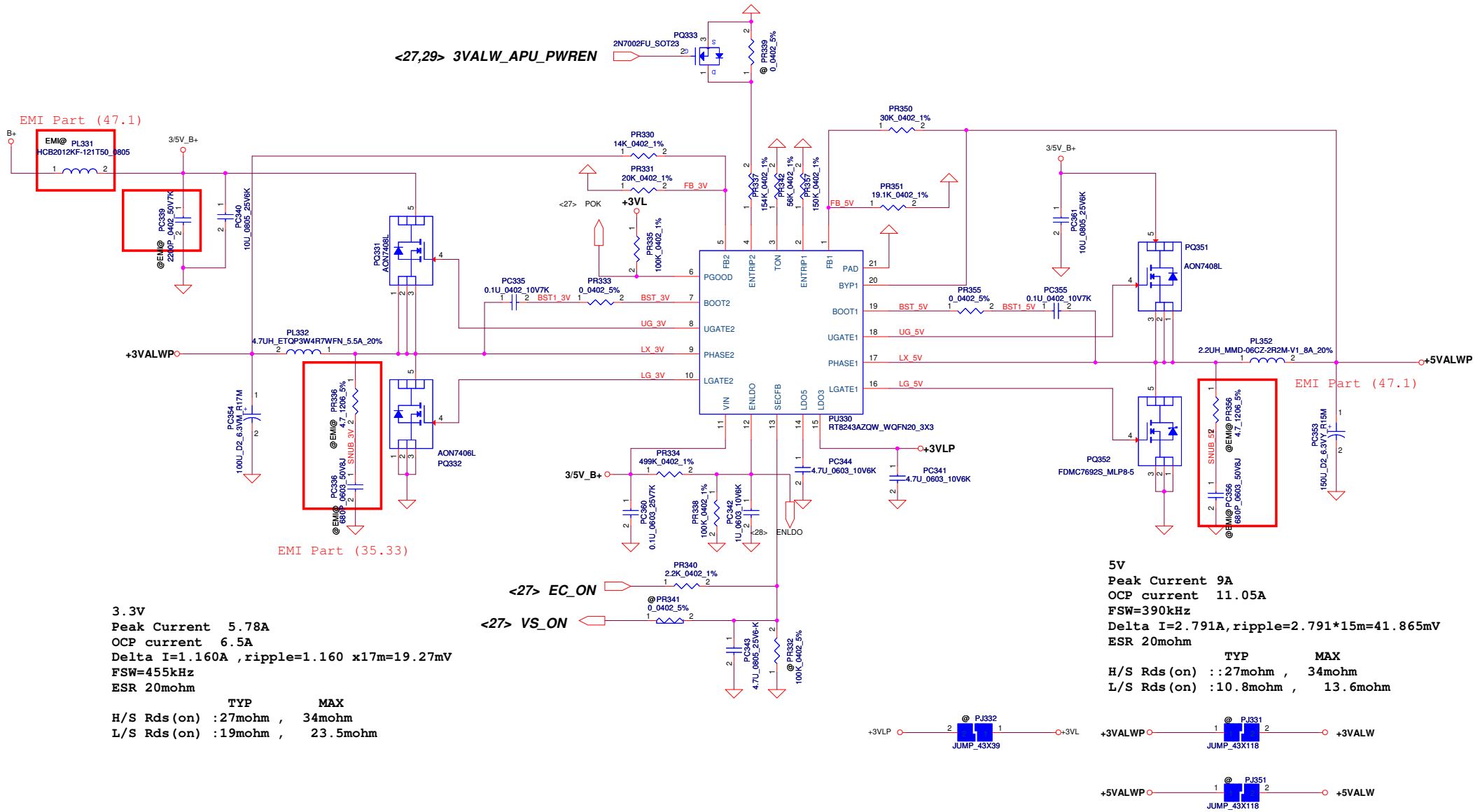
Compal Electronics, Inc.

Title: **CHARGER**

Size: Custom | Document Number: LA-A551P | Rev: 0.1

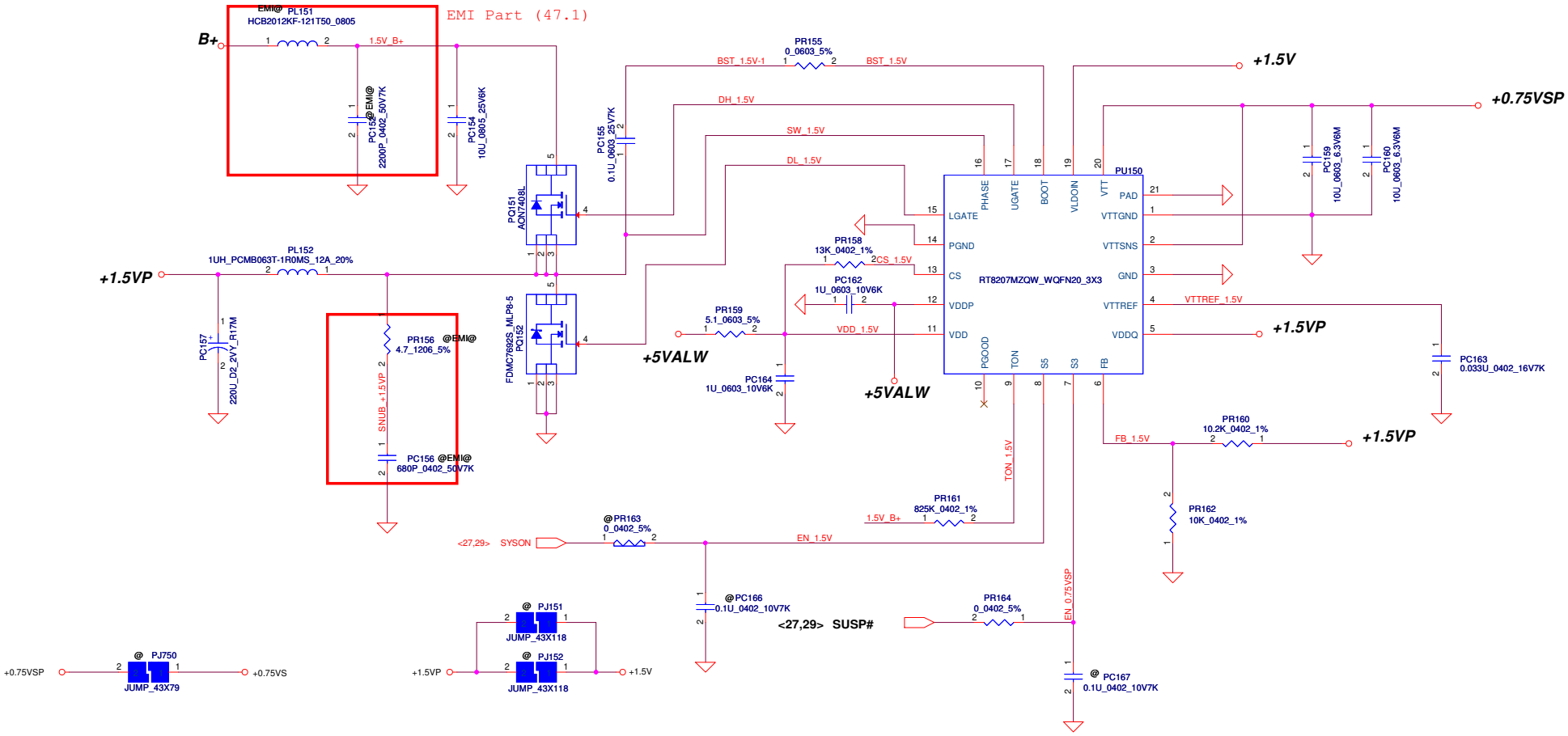
Date: | Sheet 32 of 40

3/5VALW controller (35.1), Support component (35.2)



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	3VALW/5VALW		
Size: Custom	Document Number: LA-A551P		Rev: 0.1
Date:	Sheet 33 of 40		

DDR controller (35.3), Support component (35.4)



1.5V
Peak Current 8.1A
OCP current 9.63A
FSW=500kHz
DCR 8.3 ~ 10mohm

	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:10.8mohm ,	13.6mohm

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

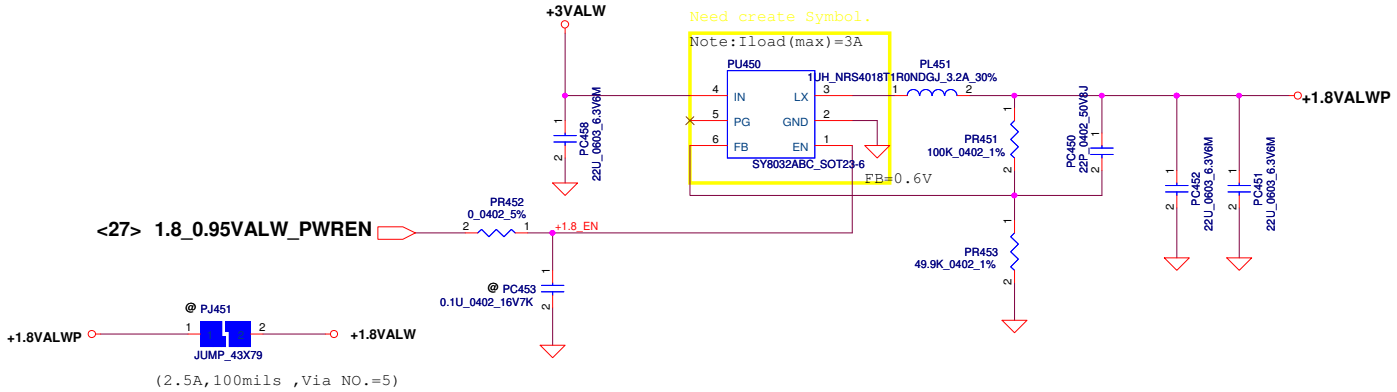
Compal Electronics, Inc.

Title: 1.5VP/0.75VSP/1.8VSP

Size: Custom | Document Number: LA-A551P | Rev: 0.1

Date: | Sheet 34 of 40

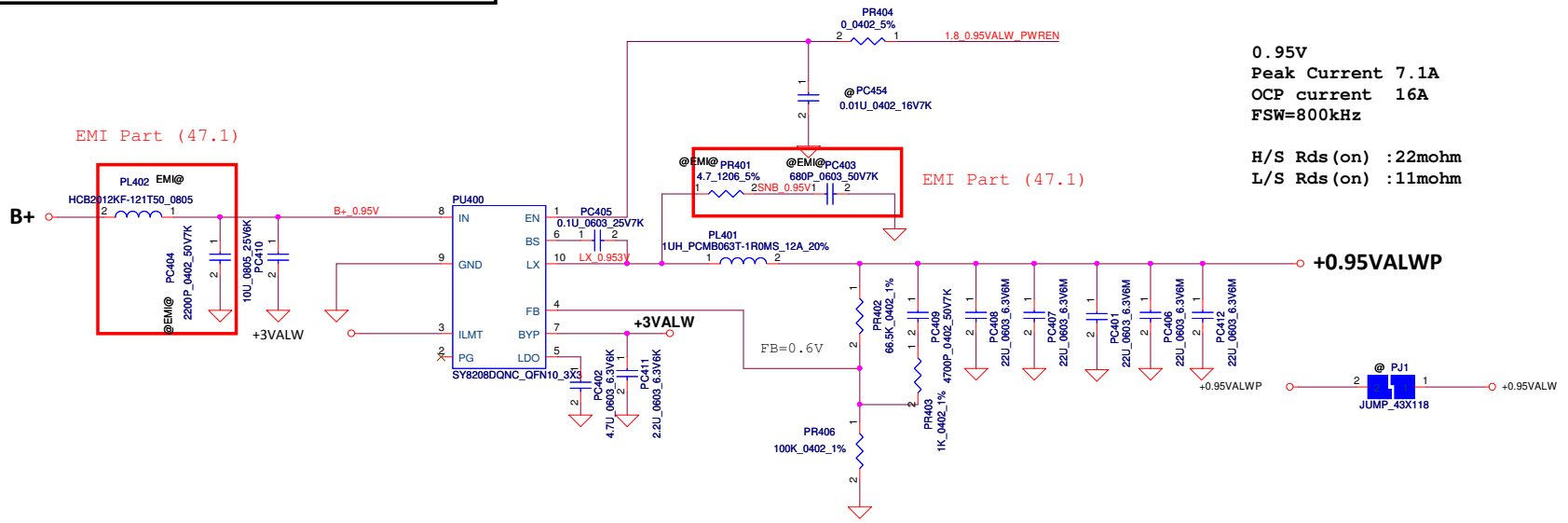
1.8V controller (35.15), Support component (35.16)



1.8V
Peak Current 2.5A
OCP current 3.5A
FSW=800kHz

H/S Rds(on) :100mohm ,
L/S Rds(on) :80mohm ,

0.95V controller (35.27), Support component (35.28)



0.95V
Peak Current 7.1A
OCP current 16A
FSW=800kHz

H/S Rds(on) :22mohm
L/S Rds(on) :11mohm

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: *+1.8VALWP/+0.95VALWP*

Size: Custom | Document Number: *ZRMAE* | Rev: 0.1

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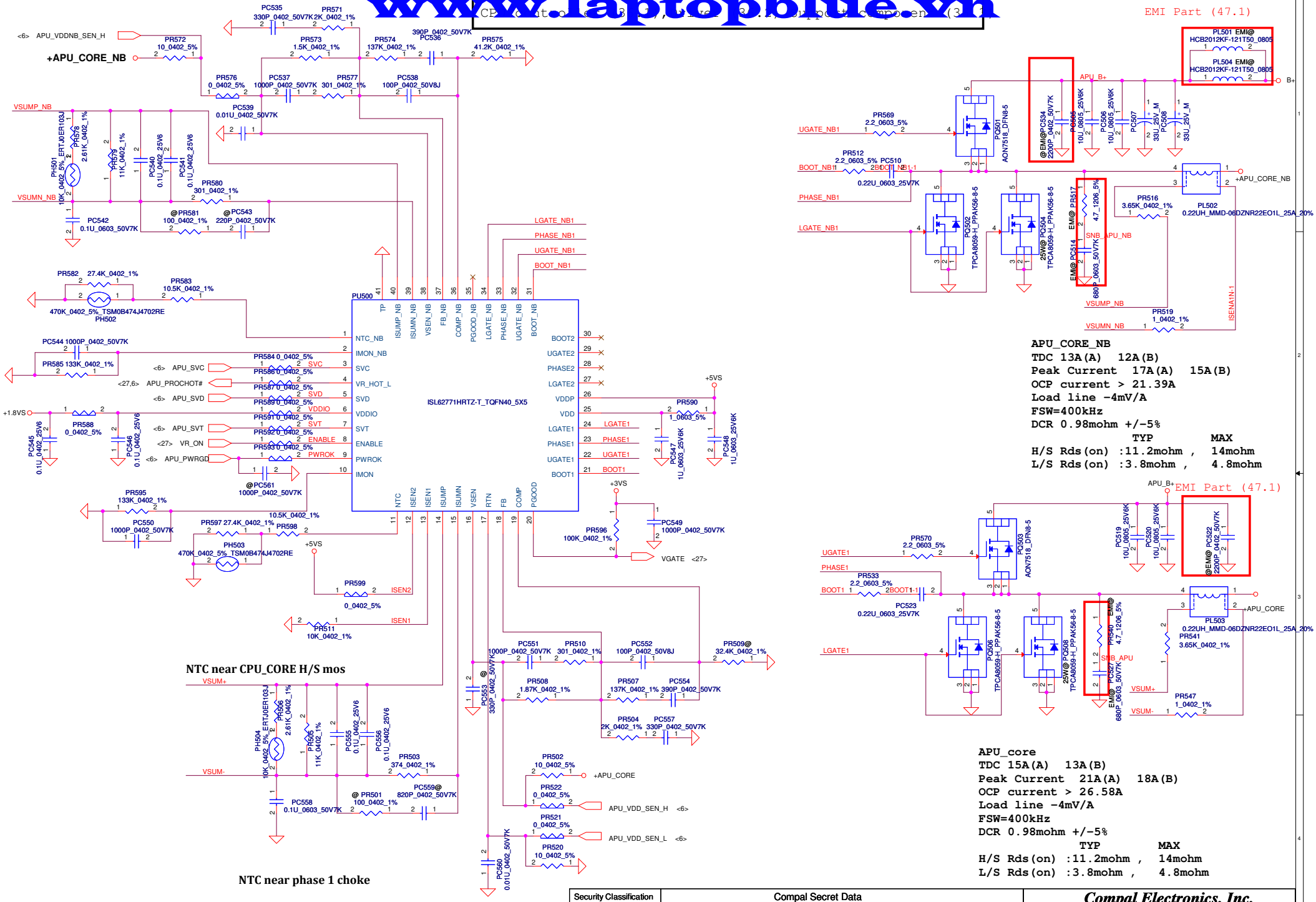

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	

Compal Electronics, Inc.			
Title	+CPU_CORE/VDDNBP		
Size Custom	Document Number LA-A551P		Rev 1.0
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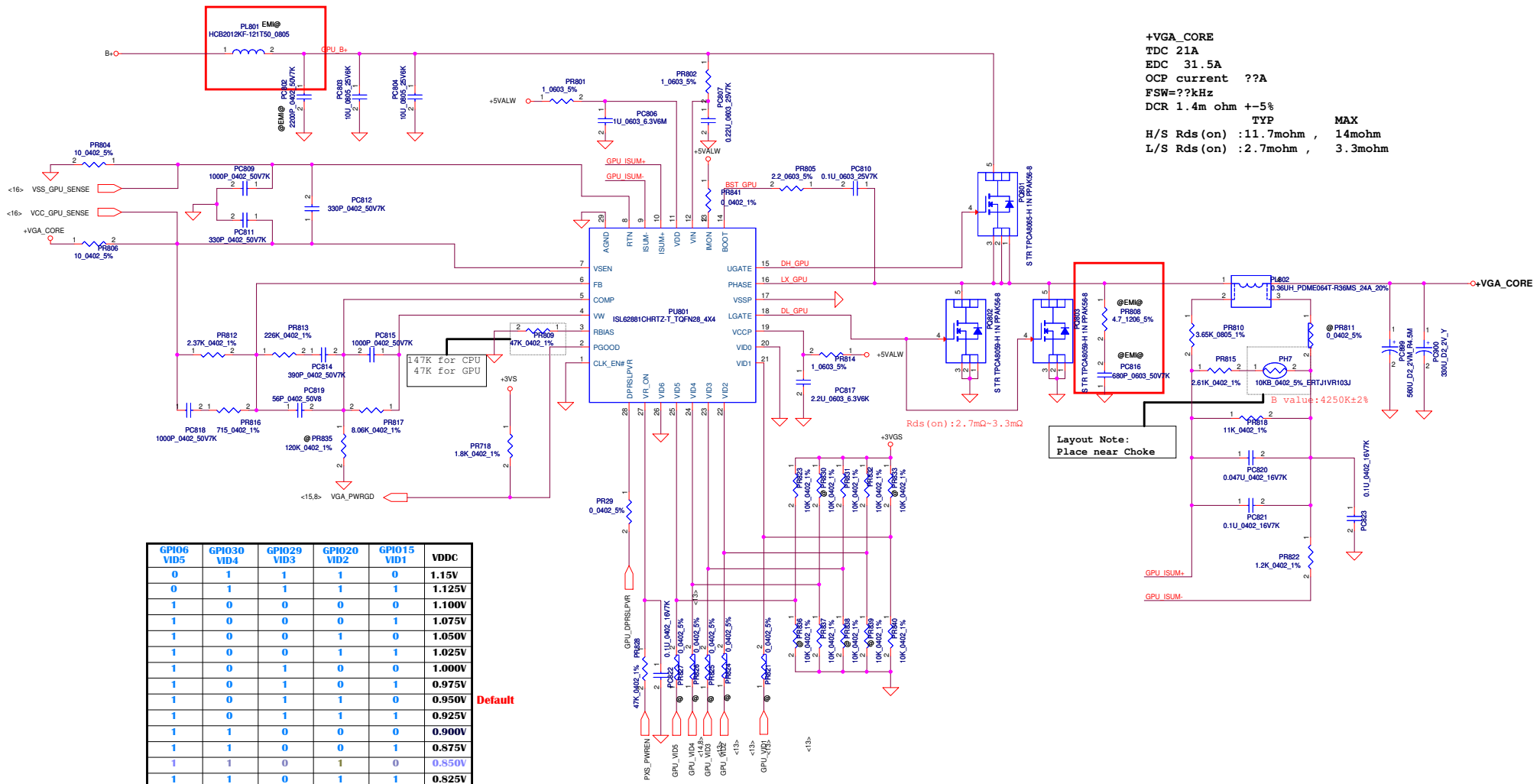
VGA controller (43.1),Driver (43.2) Support component (43.3)

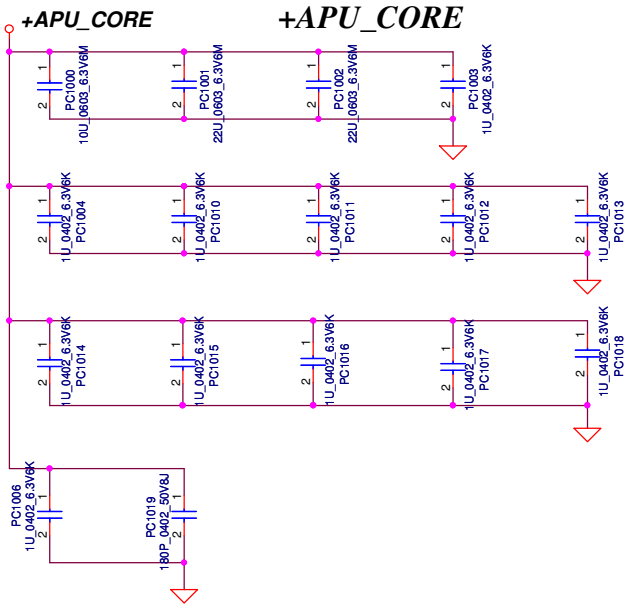
EMI Part (47.1)

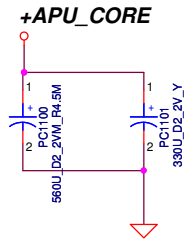


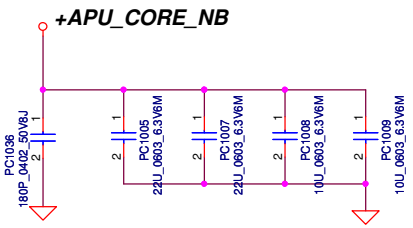
GPIO6 VID5	GPIO30 VID4	GPIO29 VID3	GPIO20 VID2	GPIO15 VID1	VDDC	
0	1	1	1	0	1.15V	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	Default
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	
1	1	1	0	1	0.775V	

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/27	Deciphered Date	2015/09/27
Title	+VPU_COREP		
Size C	Document Number LA-A551P		Rev 0.1
Date: Tuesday, July 16, 2013	Sheet 37 of 40		

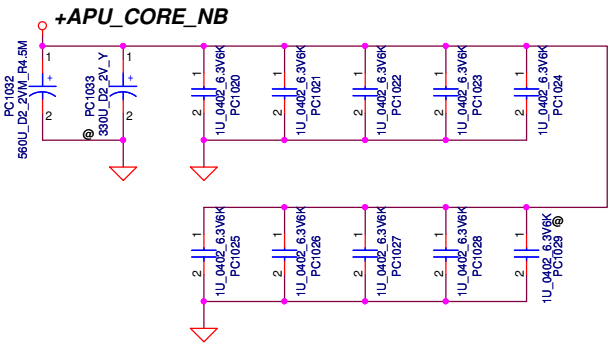
CPU_Core output CAP (Including MLCC) 38.4



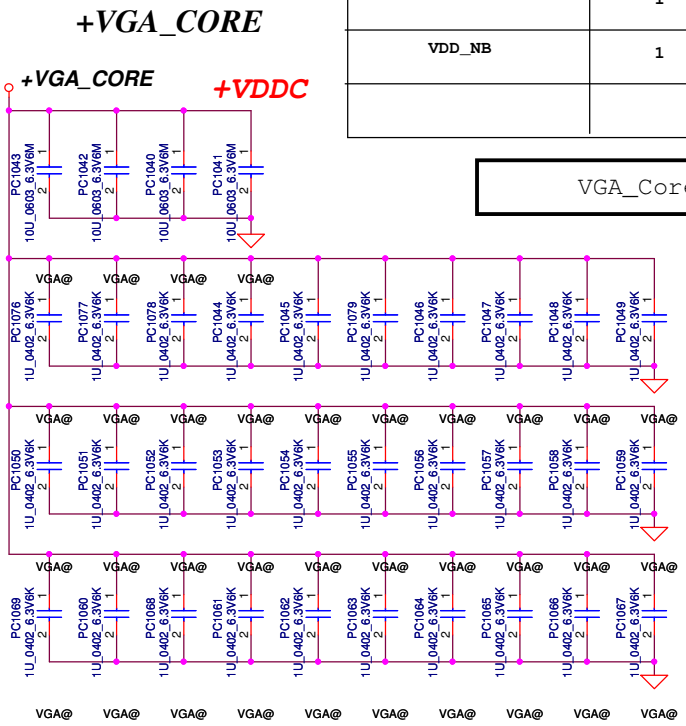




GFX output CAP (Including MLCC) 36.5



kABINI	560uF*4.5m	330uF	22uF (0603)	10uF (0603)	1u (0402)	180P (0402)
VDD	1	1	2	1	12	1
VDD_NB	1		2	2	9	1



VGA_Core output CAP (Including MLCC 43.9)

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size	Document Number	Rev
A3	LA-A551P	0.1

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for PWR

Item Reason for change PG# Modify List Date Phase

Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)	for design change
1	DVT--2013/05/03	P32-PWR-CHARGER	PR248/Remove 10K	PWR	double count for parts
2	DVT--2013/05/03	P33-PWR-3VALW/5VALW	PR337 PR357/change to 107K 150K	PWR	For 3/5 V OCP Setting
3	DVT--2013/05/03	P34-PWR-+1.5VP/0.75VSP	PR158/ change to 15K	PWR	For 1.5 V OCP Setting
4	DVT--2013/05/03	P34-PWR-+1.5VP/0.75VSP	PC157 / change to 220U	PWR	for design change
5	DVT--2013/05/03	P34-PWR-+1.5VP/0.75VSP	PL152 / change PN	PWR	Common with PL401(1UH)
6	DVT--2013/05/03	P35-PWR_+1.8VALWP/+0.95VALWP	PR405 /Remove 10K	PWR	EC pull low 10k
7	DVT--2013/05/03	P36-PWR-CPU_CORE/VDDNBP	PQ504 PQ508 / Remove TPCA8059	PWR	For 15W APU
8	DVT--2013/05/07	P38-PWR-PROCESSOR DECOUPLING	PC1044,PC1045,PC1046,PC1047,PC1048, PC1049,PC1050,PC1051,PC1052,PC1053, PC1054,PC1055,PC1056,PC1057,PC1058, PC1059,PC1060,PC1061,PC1062,PC1063, PC1064,PC1065,PC1066,PC1067,PC1068, PC1069, PC1076, PC1077,PC1078,PC1079	PWR	Remove VGA MLCC
9	DVT--2013/05/07	P38-PWR-PROCESSOR DECOUPLING	PC1040,PC1041,PC1042,PC1043	PWR	Remove VGA MLCC
10	PVT--2013/06/10	P38-PWR-PROCESSOR DECOUPLING	PC1006/add 1U	PWR	for APU Transient test
11	PVT--2013/06/10	P38-PWR-PROCESSOR DECOUPLING	PC1001,PC1002/change 22U	PWR	for APU Transient test
12	PVT--2013/06/10	P38-PWR-PROCESSOR DECOUPLING	PC1101/change 330U	PWR	for APU Transient test
13	PVT--2013/06/10	P35-PWR_+1.8VALWP/+0.95VALWP	PC412/add 22U	PWR	for 0.95v Ripple
14	PVT--2013/06/10	P33-PWR-3VALW/5VALW	PC353 / change to 150U	PWR	for 3/5V design change
15	PVT--2013/06/10	P33-PWR-3VALW/5VALW	PC354 / change to 100U	PWR	for 3/5V design change
16	PVT--2013/06/10	P33-PWR-3VALW/5VALW	PC343/ add 4.7U	PWR	for 3/5V design change
17	PVT--2013/06/10	P36-PWR-CPU_CORE/VDDNBP	PC540 PC555/ change to 0.1U	PWR	for APU Transient test
18	PVT--2013/06/17	P33-PWR-3VALW/5VALW	PR337/change to 154K	PWR	for 3V OCP Setting
19	PVT--2013/06/17	P36-PWR-CPU_CORE/VDDNBP	PC538,PC552/ change to SE071101J80	PWR	SE068101K80 - X1 Code
20	PreMP--2013/07/15	P38-PWR-PROCESSOR DECOUPLING	PC1005 PC1007/change 22U	PWR	for APU_NB Transient test

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: ZRMAE | Rev: 1.0

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HW PIR (Product Improve Record)

ZEMAE LA-A551P SCHEMATIC CHANGE
LIST
REVISION CHANGE: 0.1 to 0.2

NO.	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	05/29	P24.	Delete RR2,RR3,RR7,RR6,RR12,RB7 for USB trace.	Part conut reduce
2.	05/29	P24.	Change CR13 to 0603.	HW4 Common design
3.	05/29	P24.	Delete SLP_CHG_CB0 & SLLP_CHG_CB1 from APU.	Reduce reserve
4.	05/29	P24,27,28.	EC_CHG_CB2(GPIO1A) move to GPIO12、ADD NUM_LED#(JKB5.1 to JUB1.36)	Design change
5.	05/30	P08.	Add QC2 and connect HDMI_HDP_N to HDMI_HDP.	For HDMI utility
6.	05/30	P08.	Delete T24,T25,T27	For RTC issue
7.	05/30	P08.	Add RC3 15K pull down and reserve RC12,RC16,RC17 pull +3VALW_APU and RC5,RC11 pull gnd.	For RTC issue
8.	06/03	P24.	Change CR3&CR2 47u 0805 to CR6&CR10 and CR4&CR5 22u 0603	For hight limit
9.	06/03	P10.	Change CD43 from 47u 0805 to CD43&CD44 22u*2 0603	For hight limit
10.	06/03	P09.	Change CC14 from 47u 0805 to CC14&CC16 22u*2 0603	For hight limit
11.	06/07	P22.	Reserve varistor DL14 for LANGND to DGND	For ESD request
12.	06/07	P22.	Add diode DL5 for LANGND to DGND	For ESD request
13.	06/07	P26.	Remove RA18 and RA24	Remove reserve 0 ohm
14.	06/07	P25.	Add C18 0.1uF 0402 on +USB_VCCC close to JSB5	For EMI request
15.	06/10	P20.	Change C17 form 1500P to 0.015uF	For LCD sequence
16.	06/10	P25.	Remove 0ohm for 14 and 15 and add LR10 and LR9	For part count reduce
17.	06/11	P26.	Change LA7 and LA6 form 0402 to 0603 size	For EMI request
18.	06/11	P25.	Swap LR7/LR8 pin1&4 and pin3&2	For layout smooth
19.	06/11	P24.	Add test point for S&C IC T10&T11&T24	For NPI debug
20.	06/13	P28.	Change H4&H5 form H_3P3 to H_3P2	For ME limite
21.	06/14	P21.	Colay RY4,RY5,RY6,RY7,RY8,RY9,RY10,RY11 with HDMI chock	For EMI request

ZEMAE LA-A551P SCHEMATIC CHANGE
LIST
REVISION CHANGE: 0.2 to 1.0

NO.	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	07/05	All	Change R2,R130,RC116,RC117,RC119,RC120,R106,RA22,RA25,RA1,RA21,LA8 to shortpad	MP Part reduce
2.	07/05	P28	Delete SW5	Remove debug part
3.	07/05	P29	Reserve QC1B	Remove non-used part
4.	07/05	P06	Add APU_CRT_R/G/B pull 75ohm to GND	For disable CRT
5.	07/05	P08	Change CC31 form 10P to 8PF	XTRAL PPM fine tune
6.	07/08	P28	Change H20 screw hole to 2.7mm from 2.8mm	ME change
7.	07/08	P08	Add RC11 15K pull GND	AMD request
8.	07/08	P26	Change LA8 shortpad form 0402 to 0603	EMI request
9.	07/11	P28	Change C24 100pF cap to D32 100p varistor	ESD request
10.	07/15	P24	Update PCB footprint	DFB request

Title: HW PIR		
Size: B	Document Number: LA-A551P	Rev: 1.0
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