

LCFC Confidential


ACLU9 M/B Schematics Document

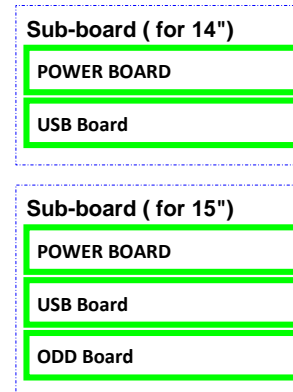
Intel BayTrail M-Processor with DDRIII + NV (N15V-GM/N15S-GT) GPU


2013-12-22

REV:0.2

| | | | | | |
|---|------------------------------|-----------------|------------|---------------------------------|-----------------|
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| | | | | Rev 0.2 | ACLU9 |





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| SIGNAL \ STATE | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VAL# | +V | +VS | Clock |
|----------------------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1(Power On Suspend) | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

USB Port Table

BOM Structure Table

SMBUS Control Table

PCIE PORT LIST

EC SM Bus1 address


EC SM Bus2 address

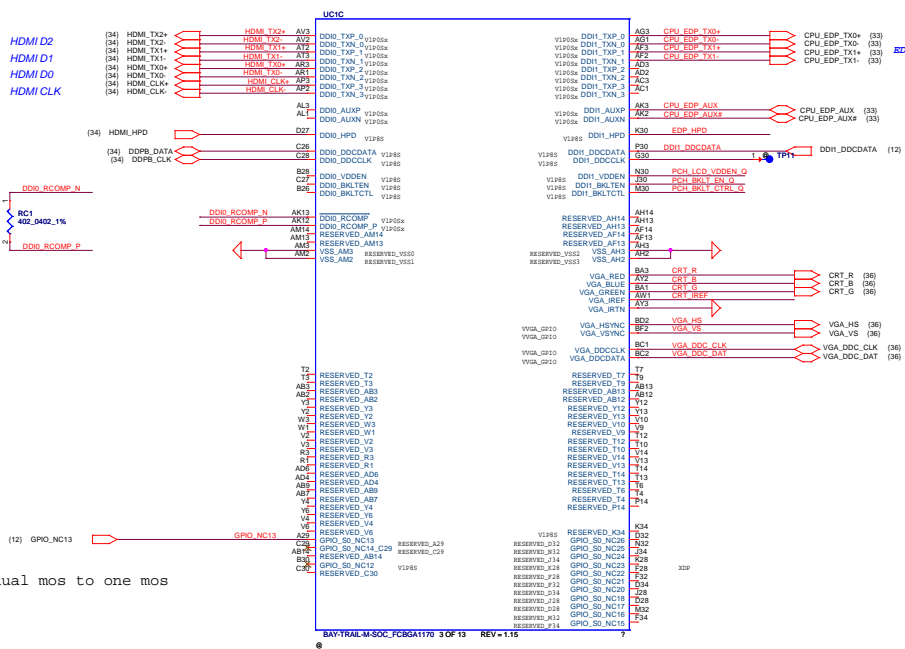
PCH SM Bus address

| Device | Address |
|--------------------------|------------|
| Thermal Sensor EMC1403-2 | 1001_100xb |
| VGA | 0x9E |
| PCH | 0x96 |

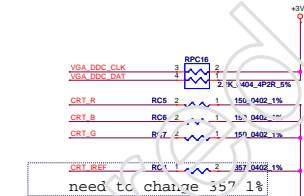
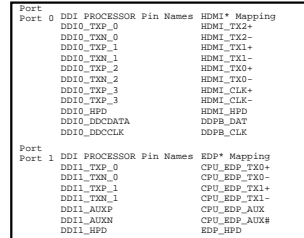
| Device | Address |
|-----------|-------------|
| DDR DIMMA | 1001 000Xb |
| Wlan | Rsvd |
| TP | need to upo |

| | | | |
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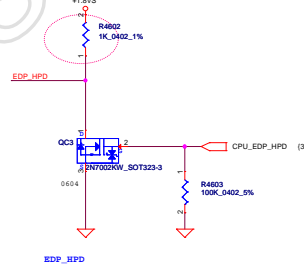
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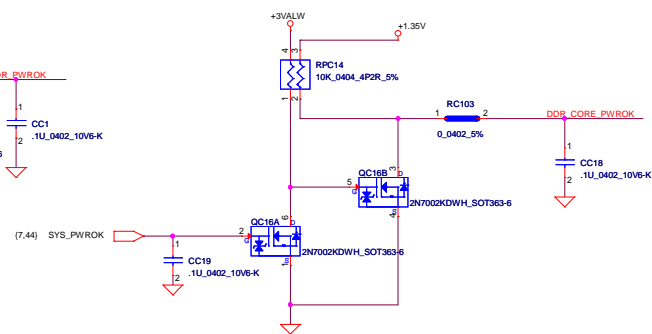
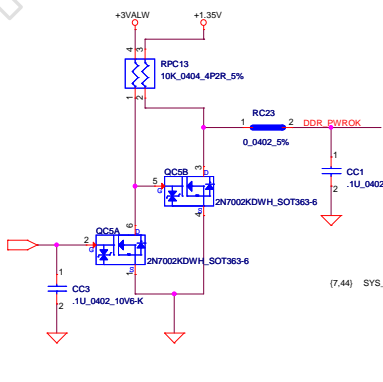
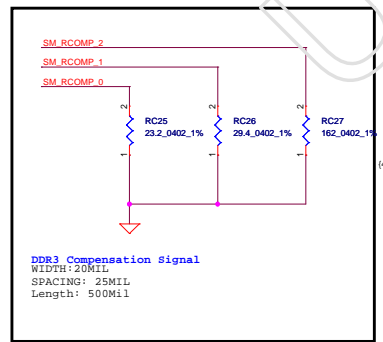
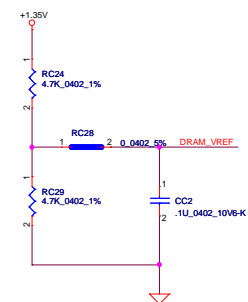
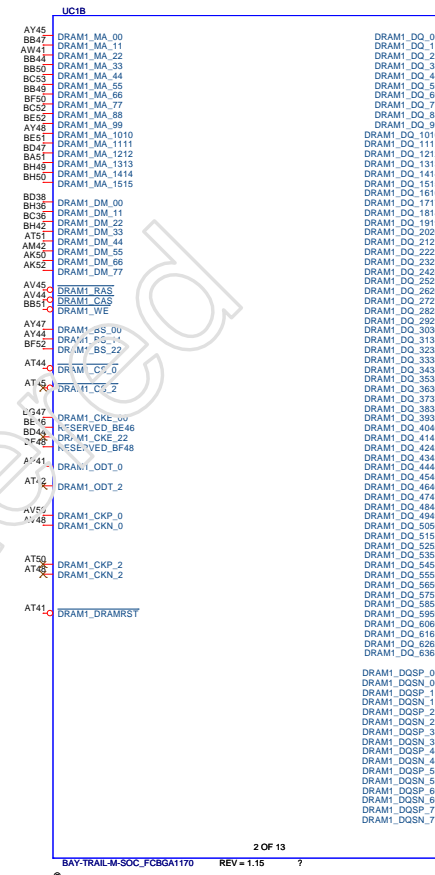
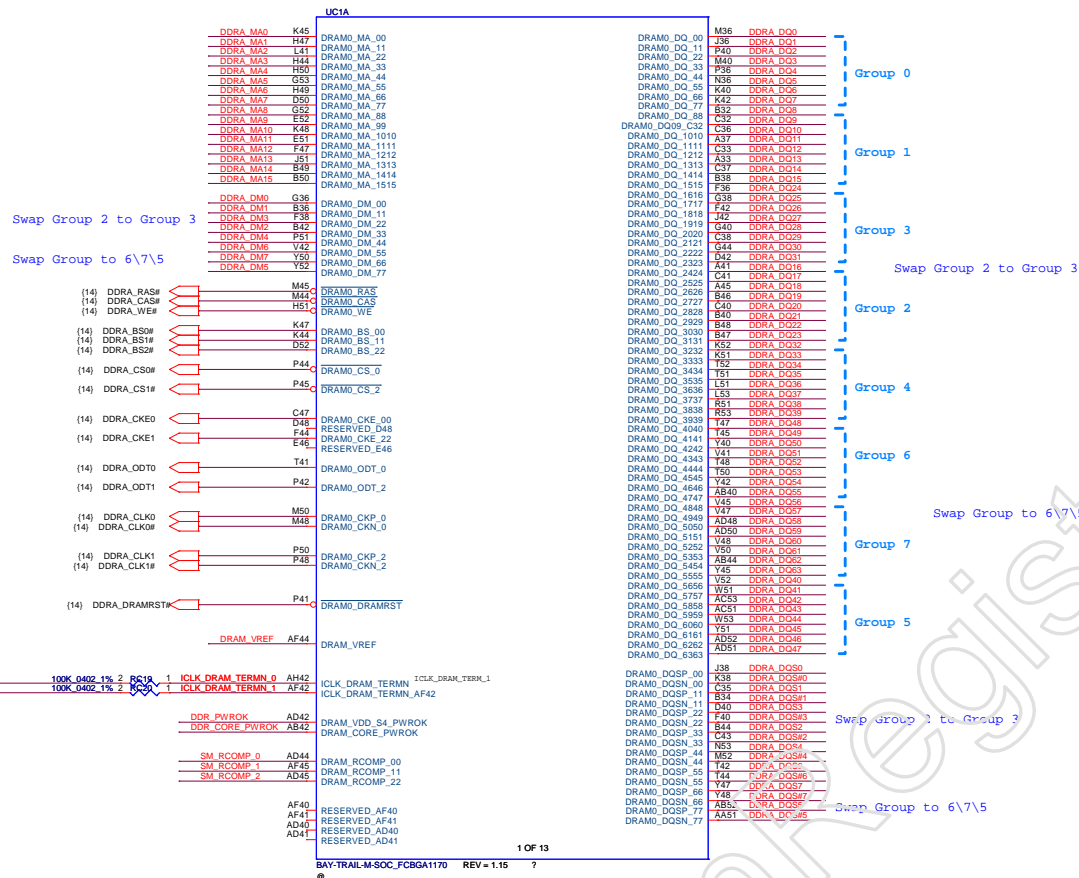
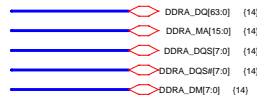
change dual mos to one mos



R4602 change from 10K to 1K,
as Vienna



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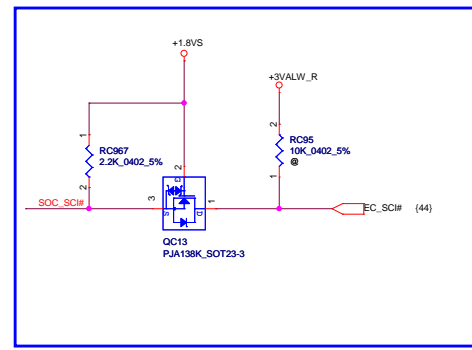
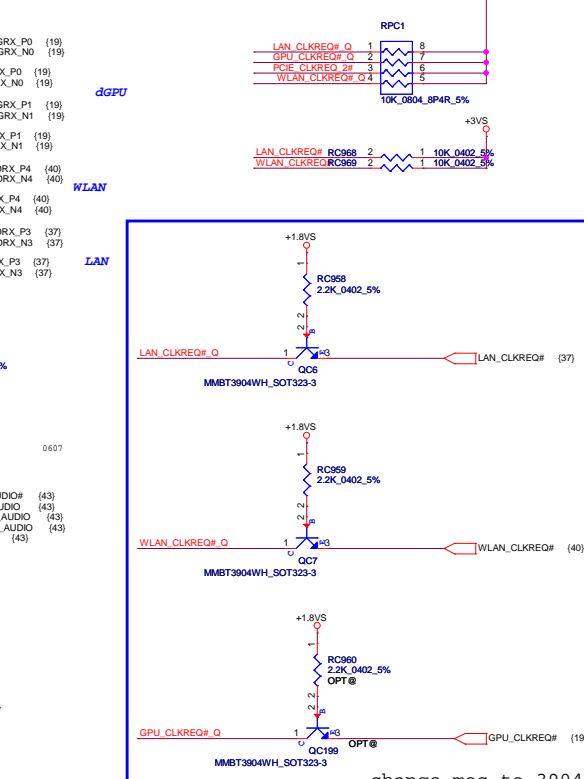
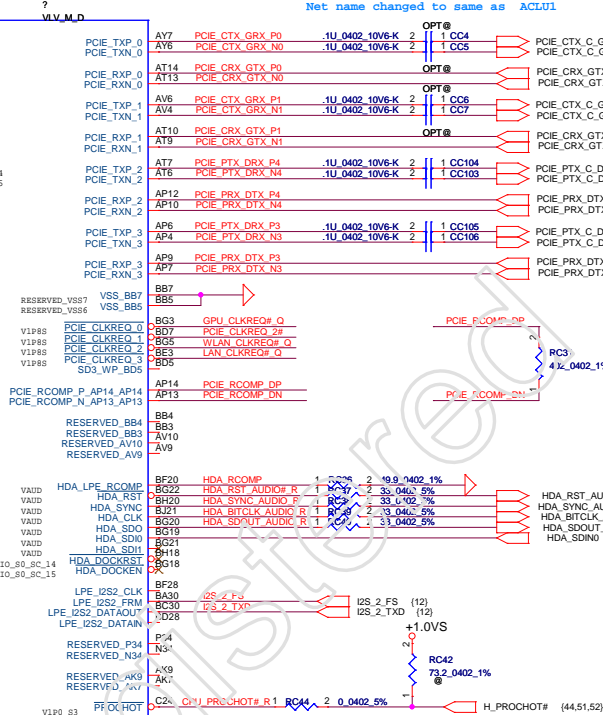
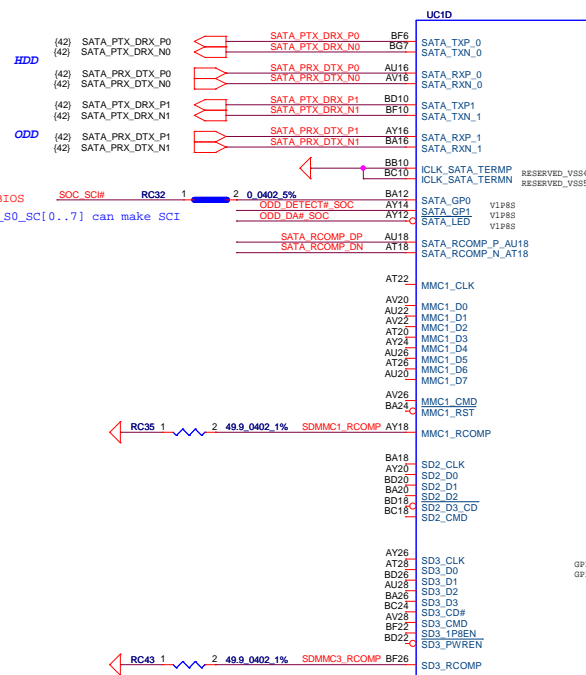
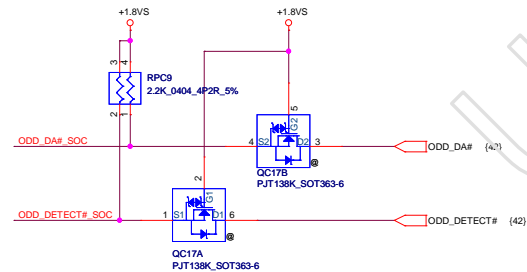
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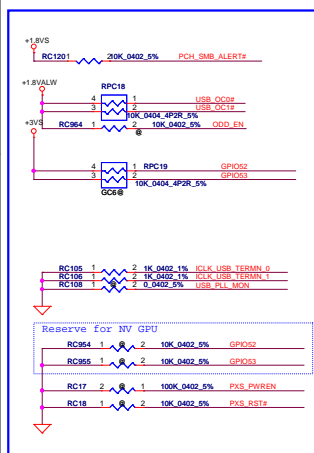
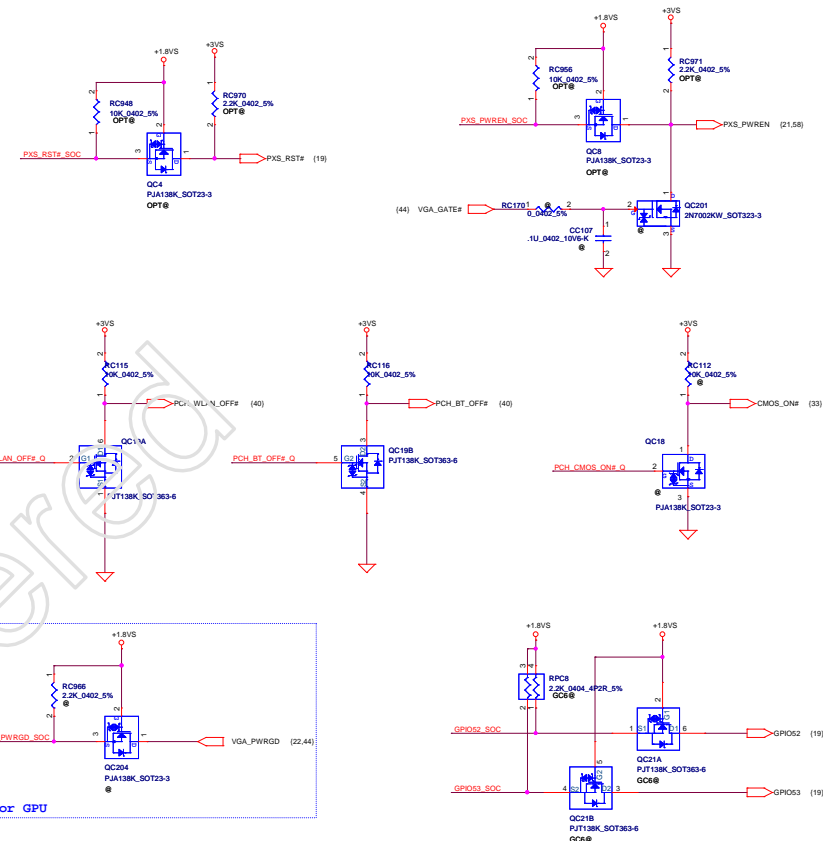
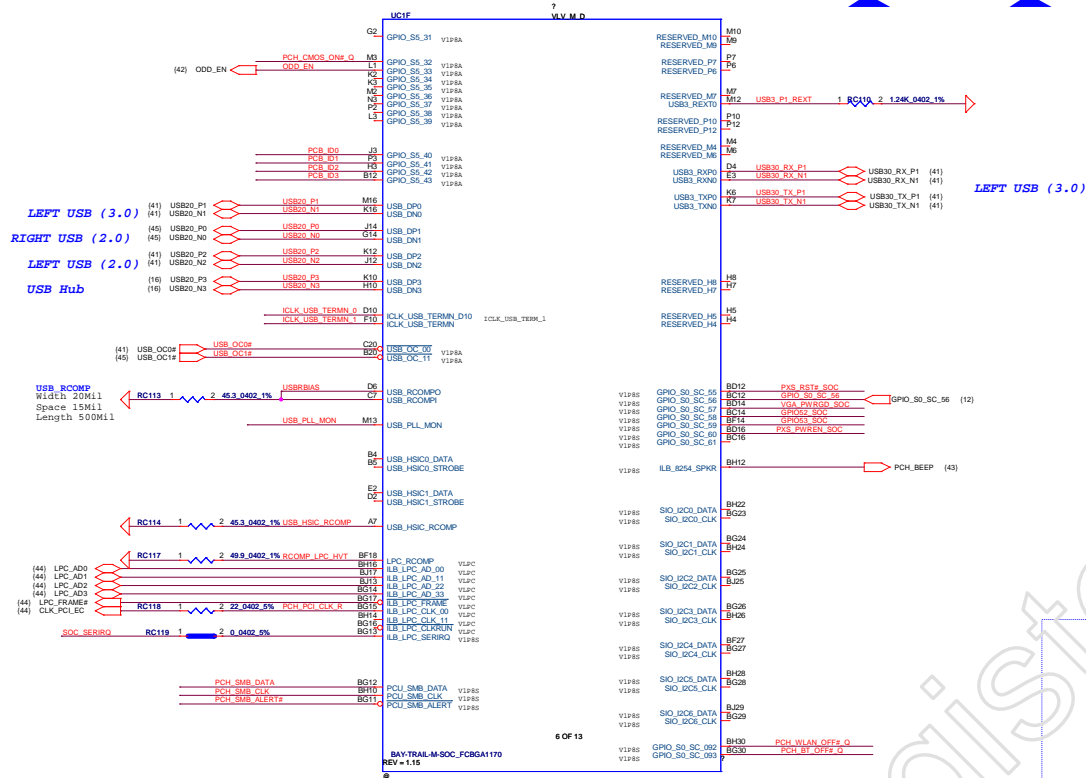
1

CRB USE SATA_GP0
need check with BIOS
only GPIO_S0_SC[0..7] can make SCI

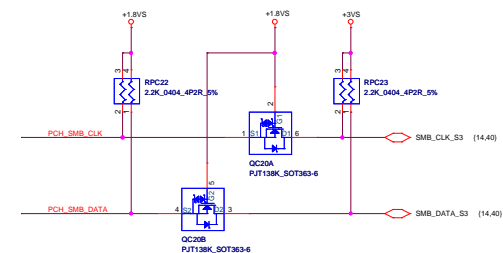
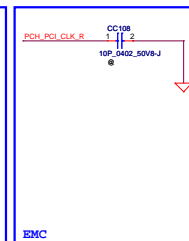
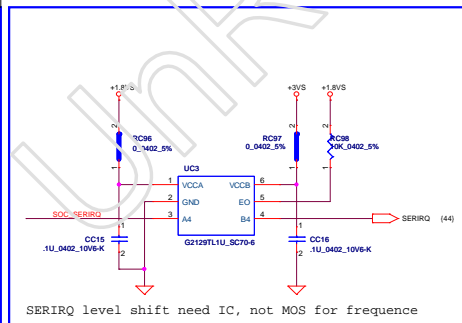
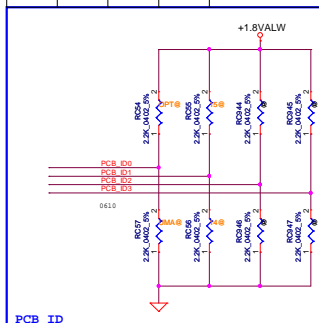
SATA_RCOMP_DP
RC30
402_0402_1%
SATA_RCOMP_DN





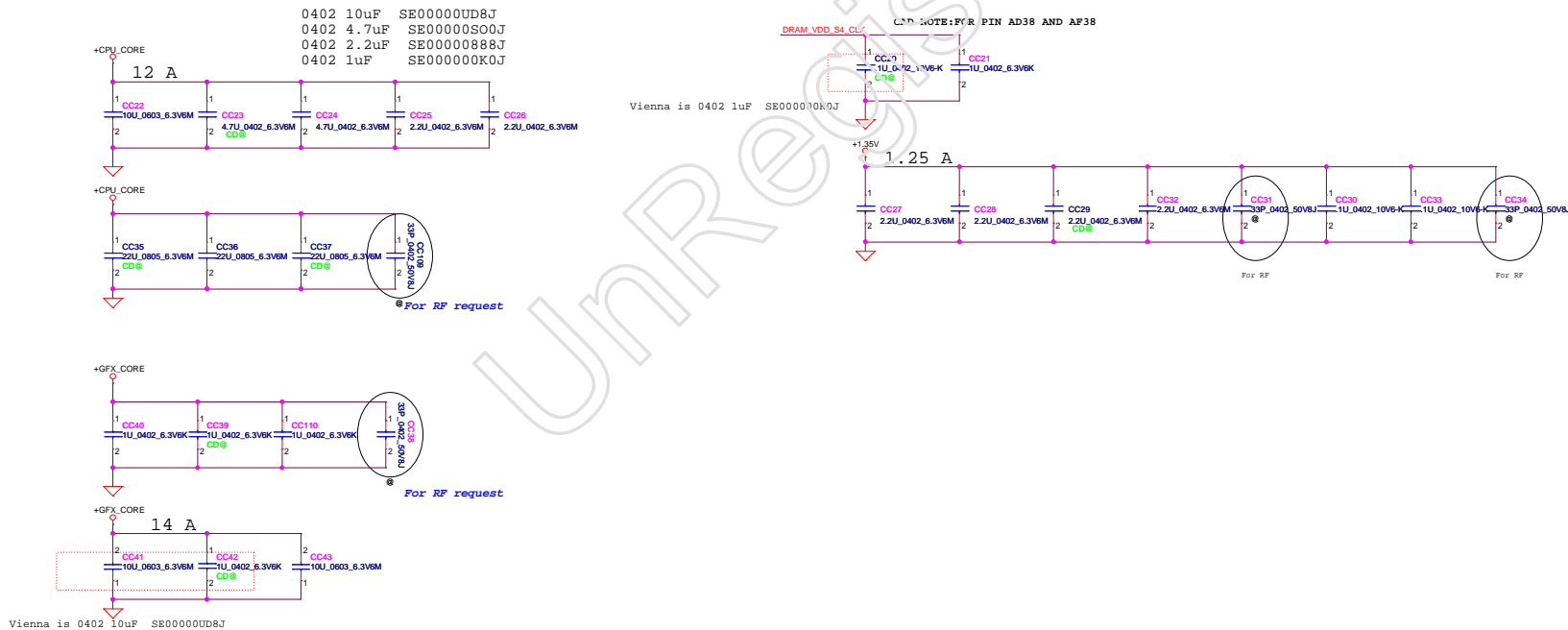
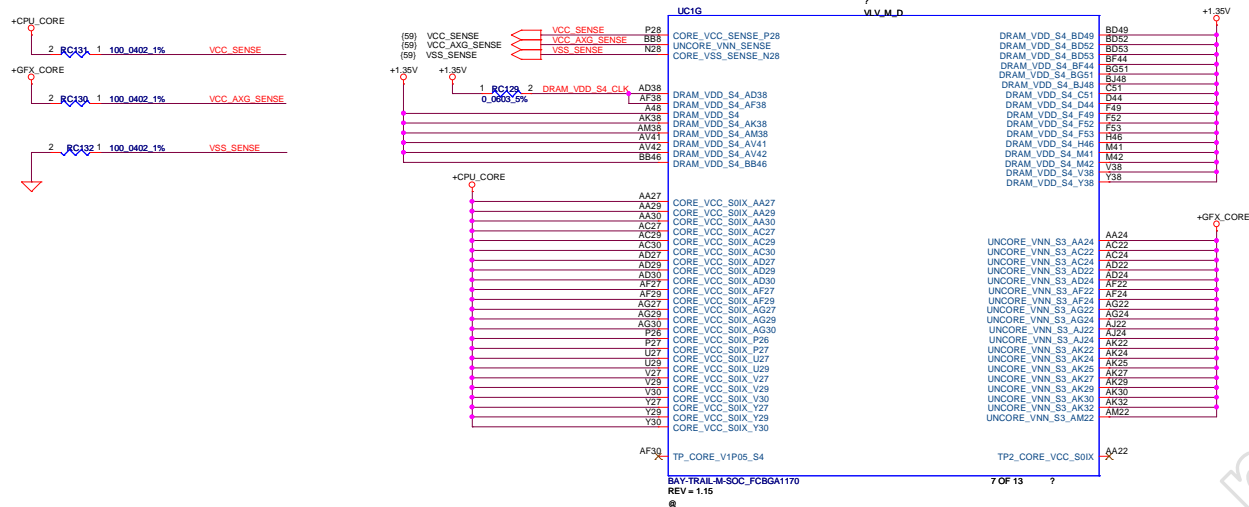
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| PCB_ID0 | PCB_ID1 | PCB_ID2 | PCB_ID3 | Description |
|---------|---------|---------|---------|-------------|
| 0 | | RESERVE | RESERVE | UMA SKU |
| 1 | | RESERVE | RESERVE | GPU SKU |
| | 0 | RESERVE | RESERVE | 14" panel |
| | 1 | RESERVE | RESERVE | 15" panel |

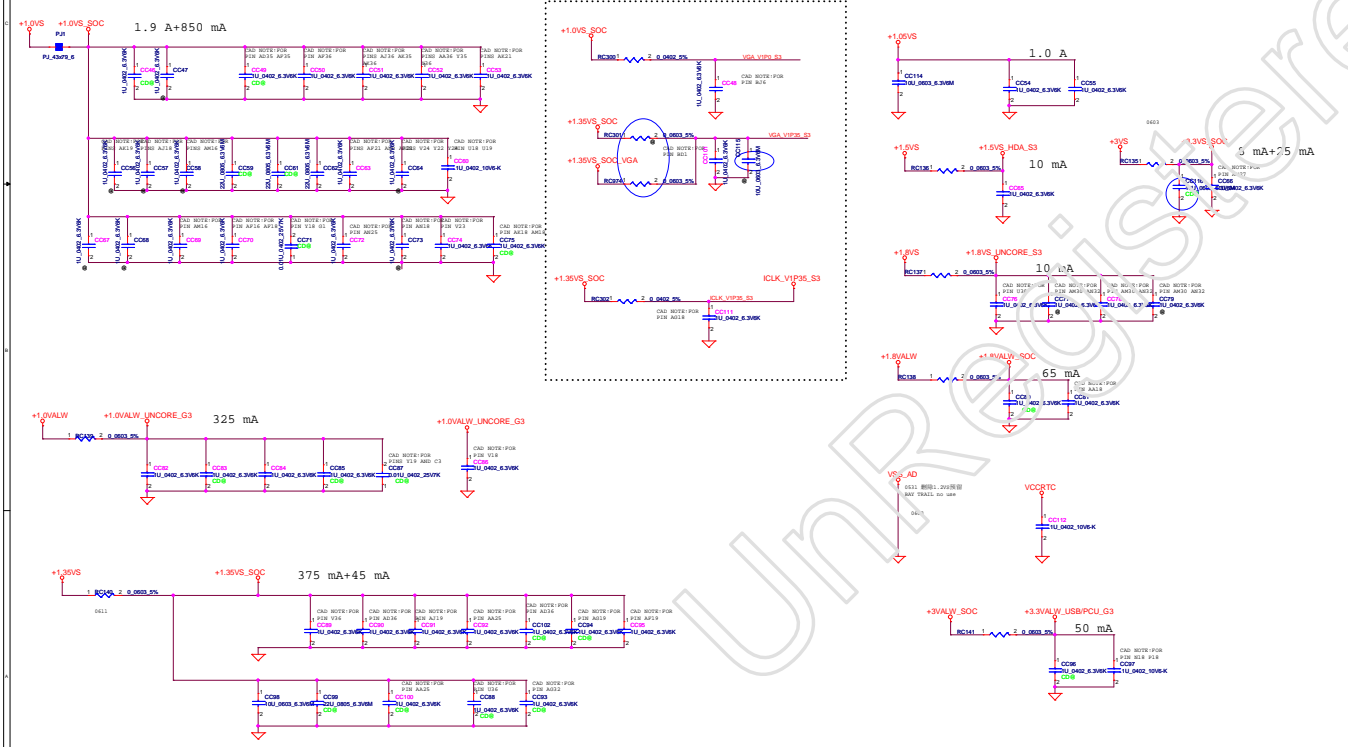



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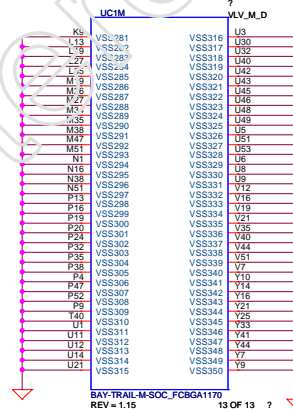
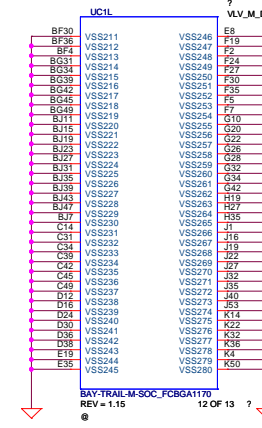
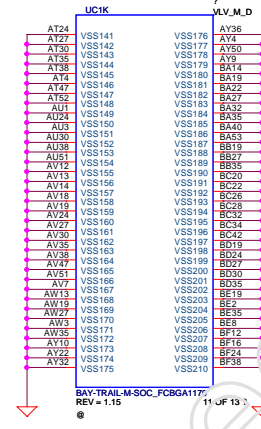
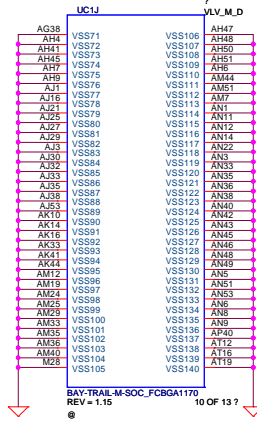
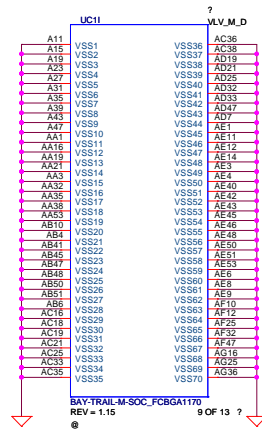


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| <p>Date: 10/20/2013</p> | | <p>Mode: Decoding 2013</p> | |
| <p>10/20/2013</p> | | <p>10/20/2013</p> | |



Hardware STRAPS (Follow up CRB& VIENNA)

GPIO_NC13
GPIO_S0_SC_56
I2S_2_FS
I2S_2_TXD
PCH_HDMI_DDC_DAT
DDI0_DDCDATA

MDSI_DDCDATA(Checklist request 10K pull down)
GPIO_S0_SC_56(Internal Pull-up)
GPIO_S0_SC[063] (Internal Pull-up)
GPIO_S0_SC[065](Internal Pull-up)
DDI1_DDCDATA
DDI0_DDCDATA

GPIO_S0_SC_56:

A16 Top Swap

0=Top address bit is unchanged

1=Top address bit is inverted

GPIO_S0_SC[063]

Multiplexed with Hardware Straps Pin LPE_I2S2_FRM

BIOS boot selection

0=LPC

1=SPI

GPIO_S0_SC[065]

Multiplexed with LPE_I2S2_DATAOUT

Security Flash Descriptors

0=Override

1=Normal Operation

DDI0_DDCDATA:

DDI0 strap

0=DDI0 not detected

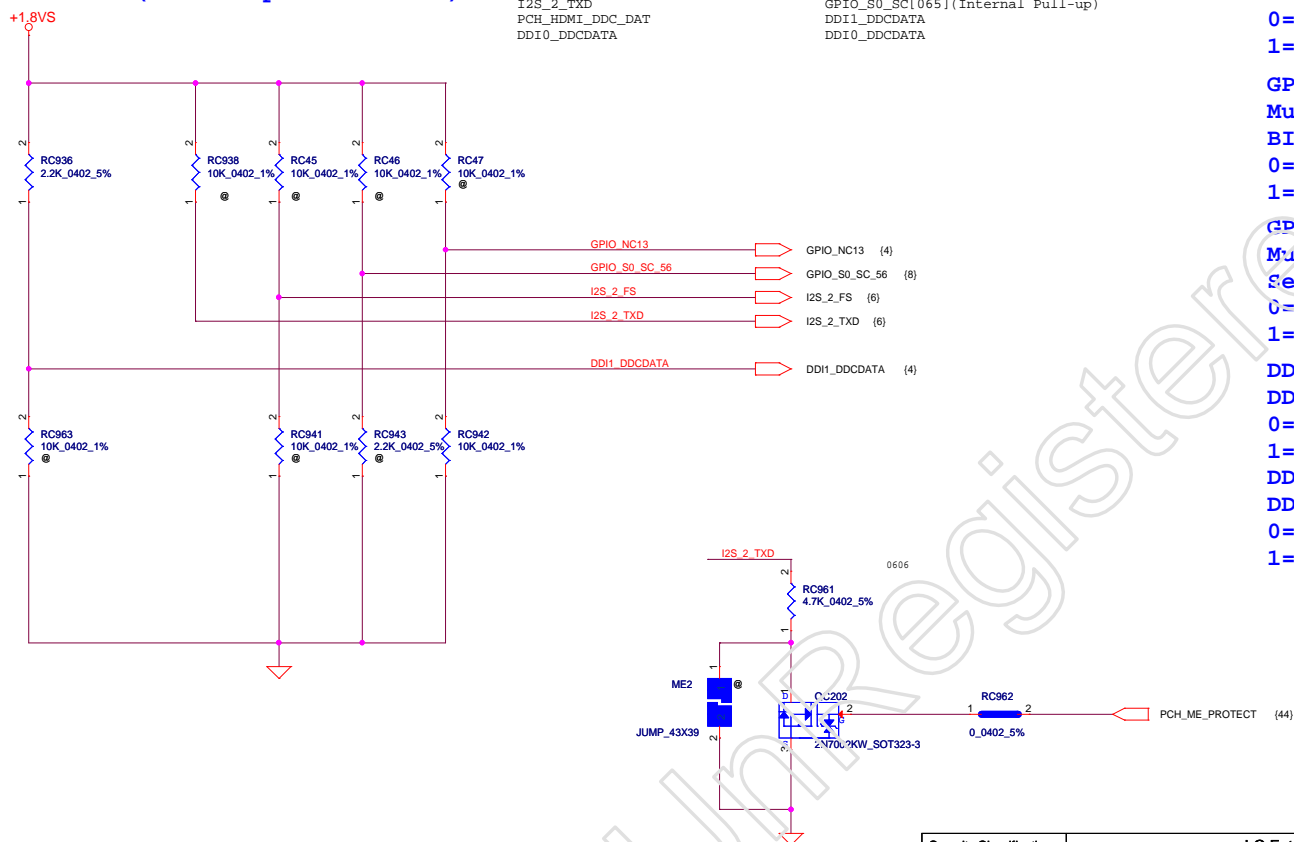
1=DDI0 detected

DDI1_DDCDATA:

DDI1 strap


0=DDI1 not detected

1=DDI1 detected




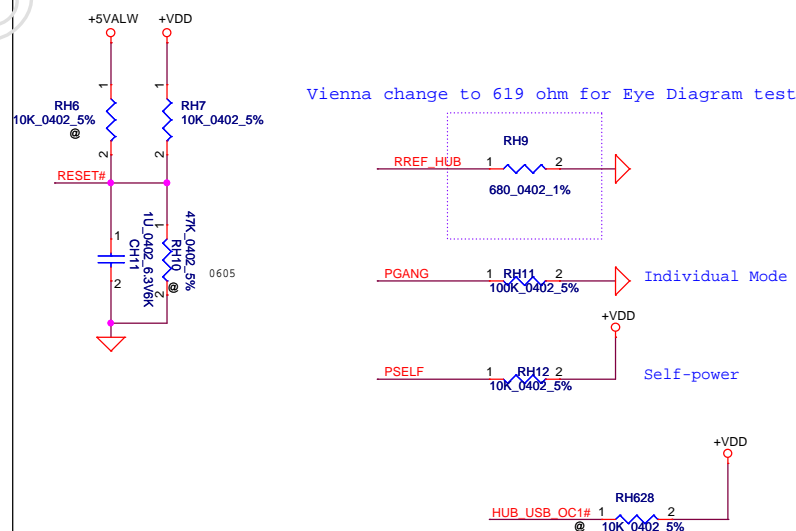
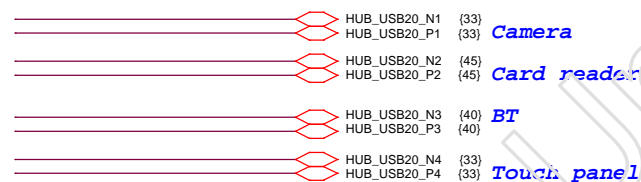
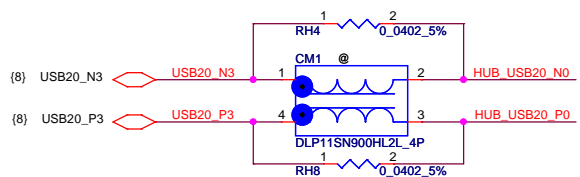
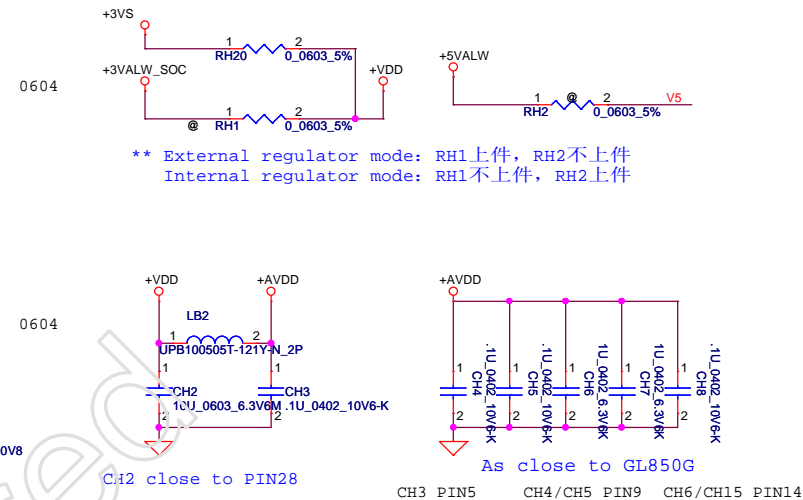
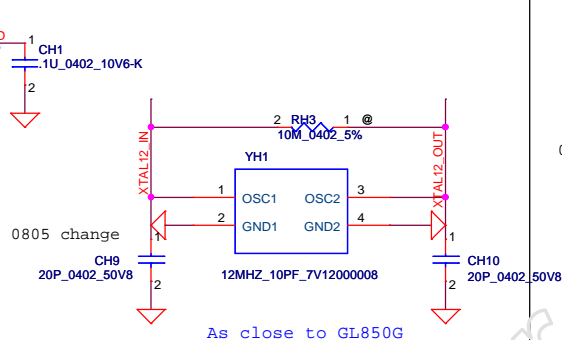
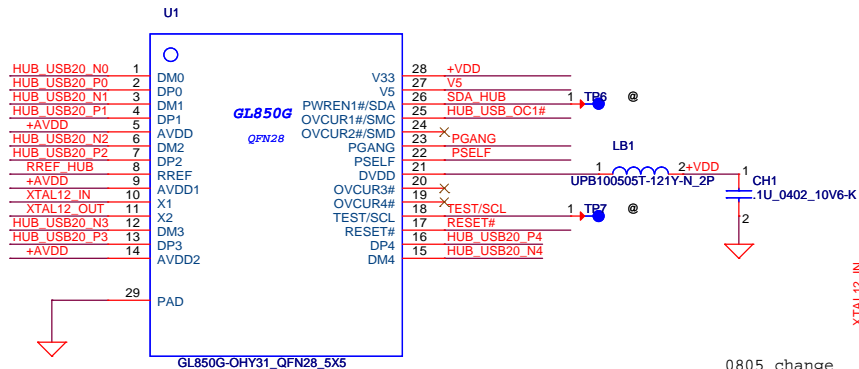
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UnRegistered

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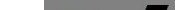
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| | | | | Custm | ACLU9 | 0.2 | |
| Date: | | | | Monday, December 23, 2013 | Sheet | 17 of 59 | |

N15x GPIO

| GPIO | I/O | ACTIVE | Function Description |
|--------|-----|--------|--|
| GPIO0 | OUT | - | FB Enable for GC6 2.0 |
| GPIO1 | OUT | N/A | |
| GPIO2 | OUT | N/A | |
| GPIO3 | OUT | N/A | |
| GPIO4 | OUT | N/A | |
| GPIO5 | OUT | N/A | GPU power sequencing---3V3_MAIN_EN |
| GPIO6 | IN | - | GPU wake signal for GC6 2.0 |
| GPIO7 | OUT | N/A | |
| GPIO8 | I/O | - | System side PCIe reset Monitor |
| GPIO9 | I/O | N/A | 2.2K Pull-up |
| GPIO10 | OUT | N/A | |
| GPIO11 | OUT | - | GPU Core VDD PWM control signal |
| GPIO12 | IN | | AC Power Detect Input (10K pull High) |
| GPIO13 | OUT | - | Phase Shedding |
| GPIO14 | IN | N/A | |
| GPIO15 | IN | N/A | |
| GPIO16 | | N/A | |
| GPIO17 | IN | N/A | |
| GPIO18 | IN | N/A | |
| GPIO19 | IN | N/A | |
| GPIO20 | | N/A | |
| GPIO21 | OUT | | GPU PCIe self-reset control |
| OVERT | OUT | | Active Low Thermal Catastrophic Over Temperature |

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

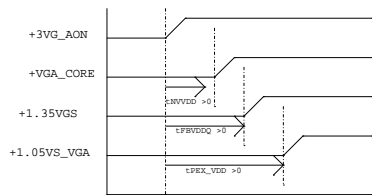
| Products | GPU (4) (W) | Mem (1.5) (W) | NVCLK /MCLK (MHz) | NVVDD (V) (A) (W) | | | FBVDD (1.35V) (A) (W) | | FBVDDQ (GPU+Mem) (1.35V) (A) (W) | | PCI Express (1.05V) (mA) (W) | | I/O and PLLVDD (1.05V) (mA) (W) | | Other (3.3V) (mA) (W) | |
|----------------------|----------------|------------------|----------------------|----------------------|-----|-----|--------------------------|-----|-------------------------------------|-----|---------------------------------|-----|------------------------------------|-----|--------------------------|-----|
| N14X 128bit 2GB DDR3 | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD |

N15x Multi-level Straps

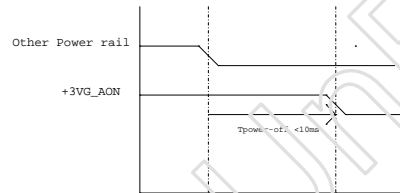
| Physical Strapping pin | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|------------------------|------------|---|------------------------|------------------------|------------------------|
| ROM_SCLK | +3VGS | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| ROM_SI | +3VGS | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] |
| ROM_SO | +3VGS | DEVID_SEL | PCIE_CFG | SMB_ALT_ADDR | VGA_DEVICE |
| STRAP0 | +3VGS | Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up) | | | |
| STRAP1 | +3VGS | Reserved(keep pull-up and pull-down footprint and not stuff by default) | | | |
| STRAP2 | +3VGS | | | | |
| STRAP3 | +3VGS | | | | |
| STRAP4 | +3VGS | | | | |

| SMBUS_ALT_ADDR | |
|----------------|------------------------|
| 0 | 0x9E (Default) |
| 1 | 0x9C (Multi-GPU usage) |

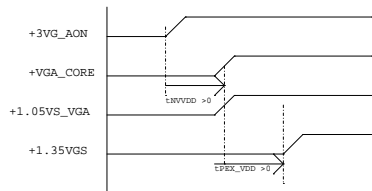
N15V-GM Power Sequence



1. all power rail ramp up time should be larger than 40us

1. all GPU power rail should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

N15S-GT Power Sequence

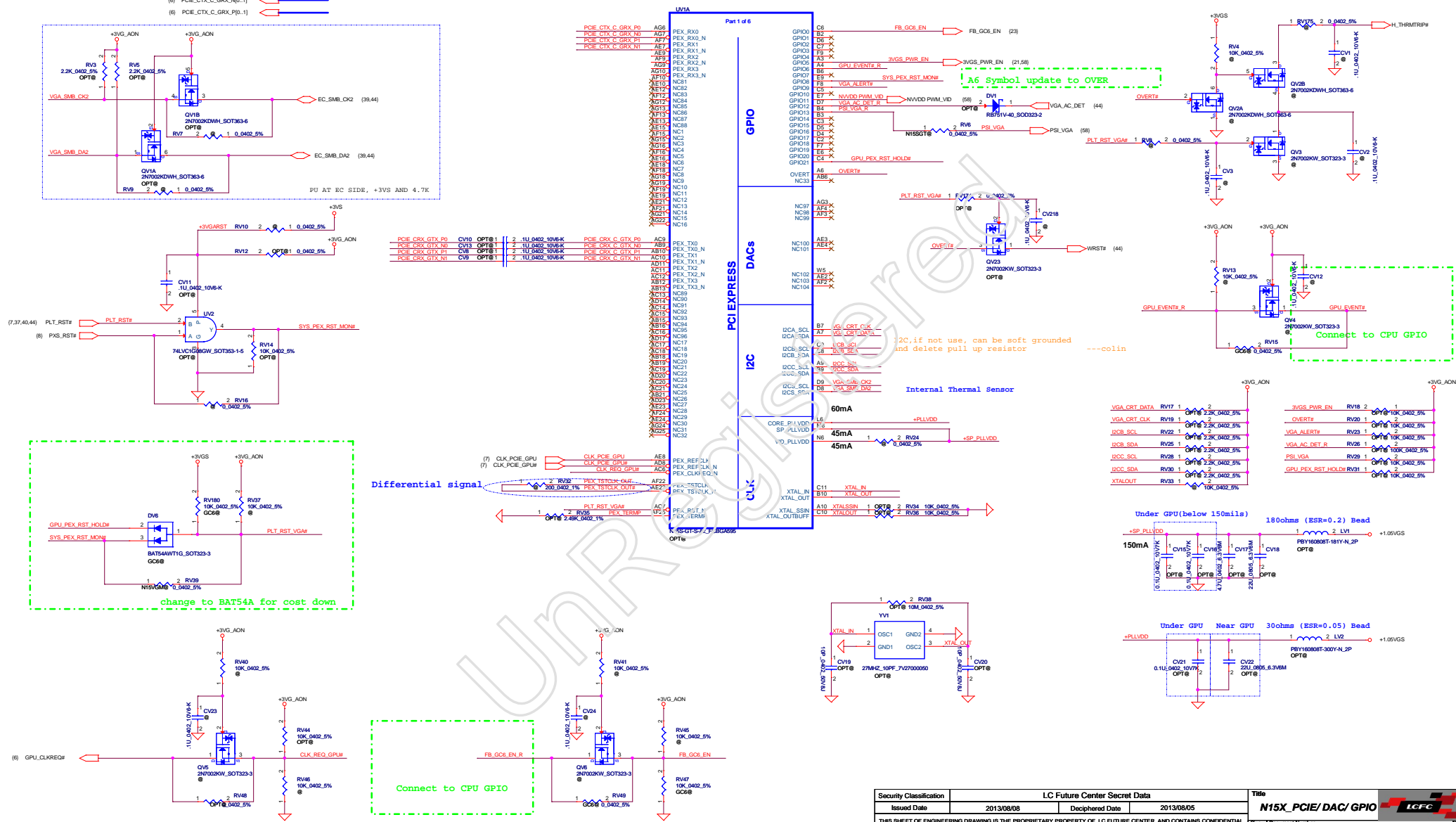



1. all power rail ramp up time should be larger than 40us

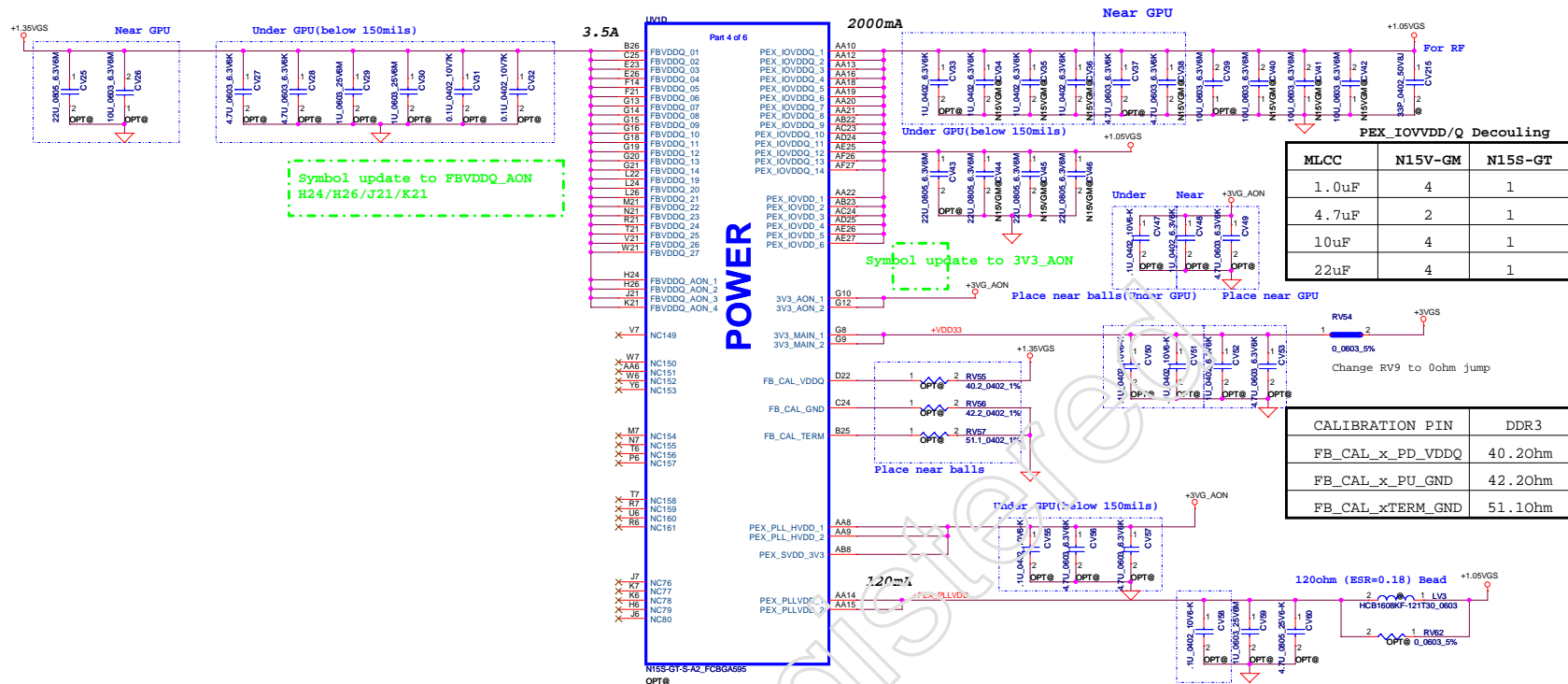
N15x Binary Straps

| Physical Strapping pin | Power Rail | Strap Mapping |
|------------------------|------------|----------------|
| ROM_SCLK | +3VGS | SMB_ALT_ADDR |
| ROM_SI | +3VGS | SUB_VENDOR |
| ROM_SO | +3VGS | VGA_DEVICE |
| STRAP0 | +3VGS | RAM_CFG[0] |
| STRAP1 | +3VGS | RAM_CFG[1] |
| STRAP2 | +3VGS | RAM_CFG[2] |
| STRAP3 | +3VGS | RAM_CFG[3] |
| STRAP4 | +3VGS | PCIE_MAX_SPEED |

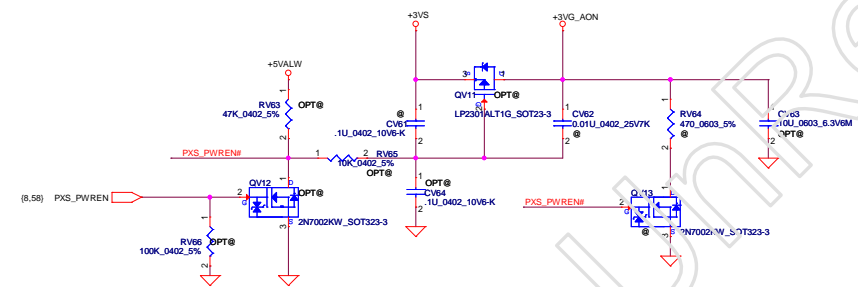
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|--|------------------------------|-----------------|------------|---------------------------------|----------------|
| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 | VGA Notes List | |
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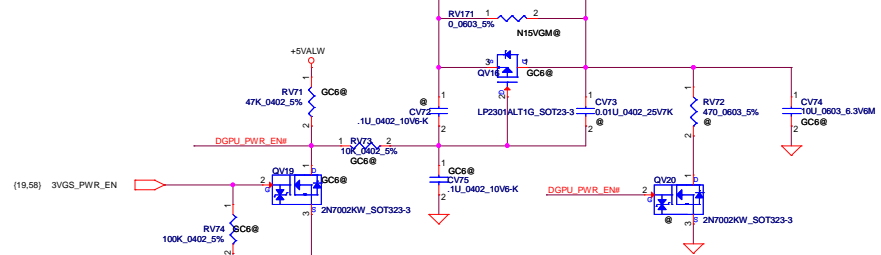
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|---|--|--|------------------------------|--|------------|-------|---------------------------|---|----------------|
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| Date | | | | | | | Monday, December 23, 2013 | | Sheet 19 of 59 |



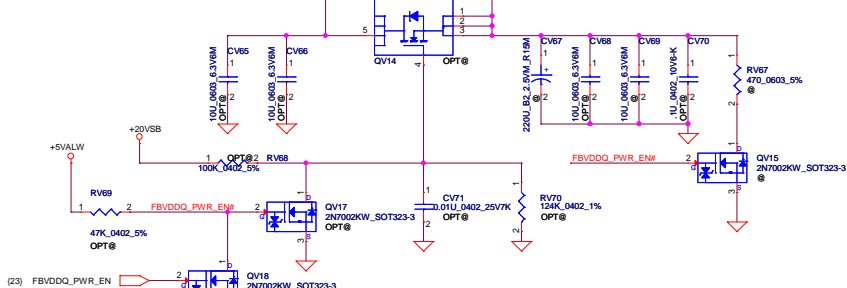
+3.3VS TO +3V3_AON

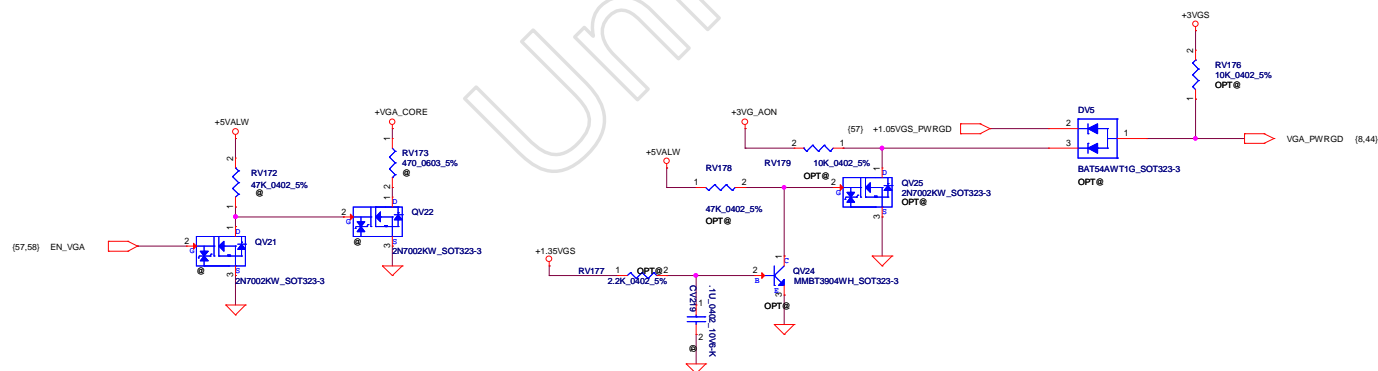
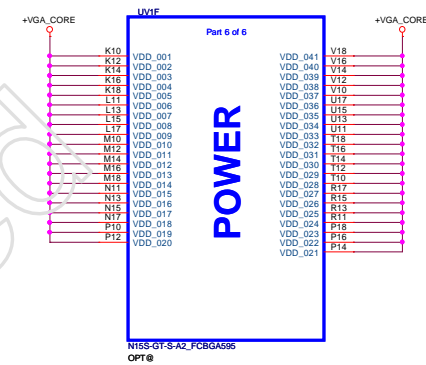
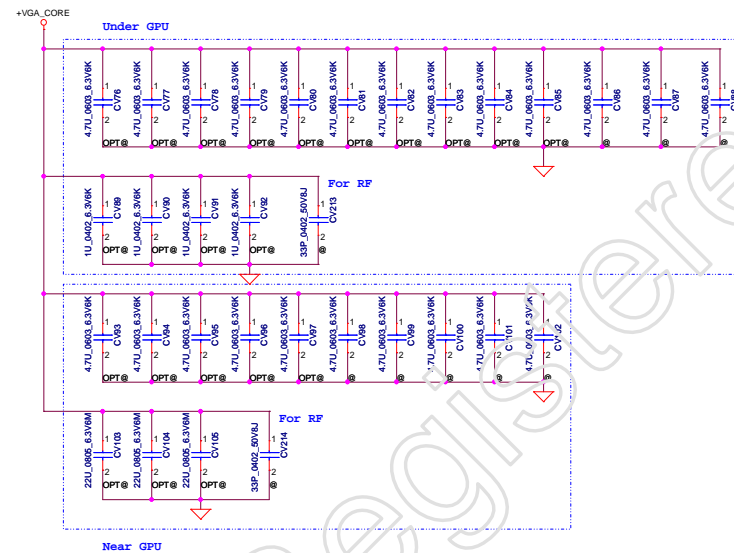
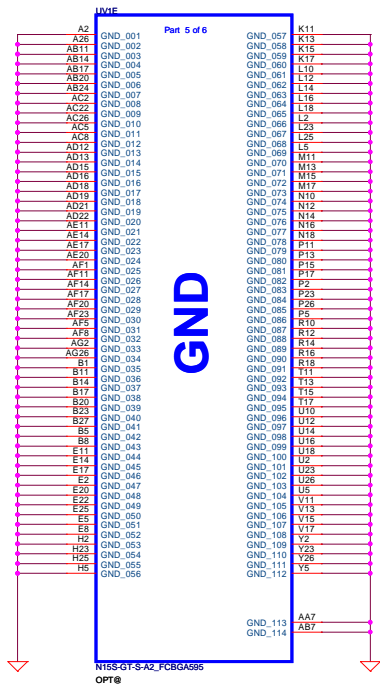




+3.3VS TO +3VGS



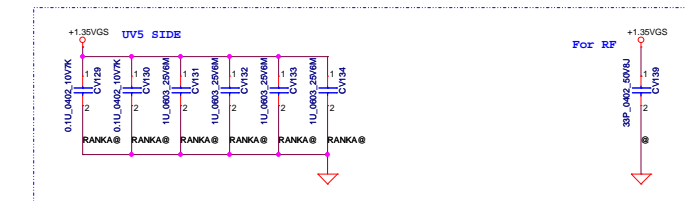
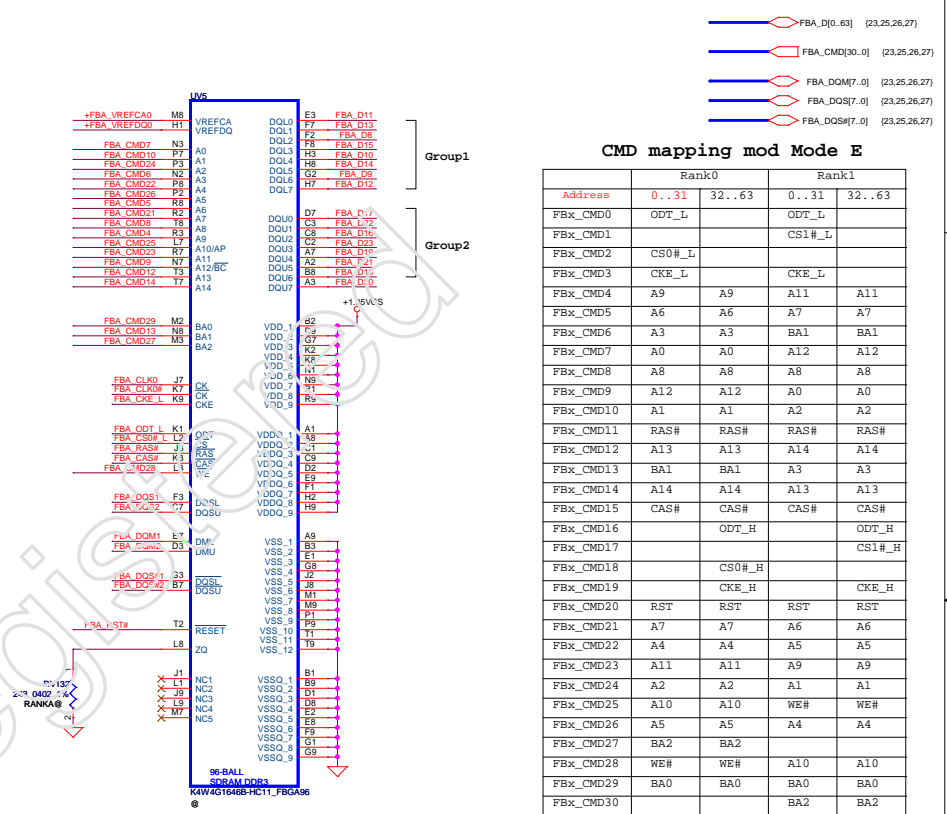
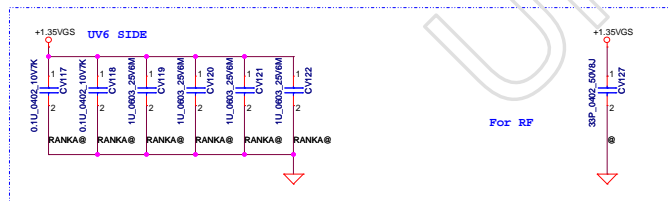
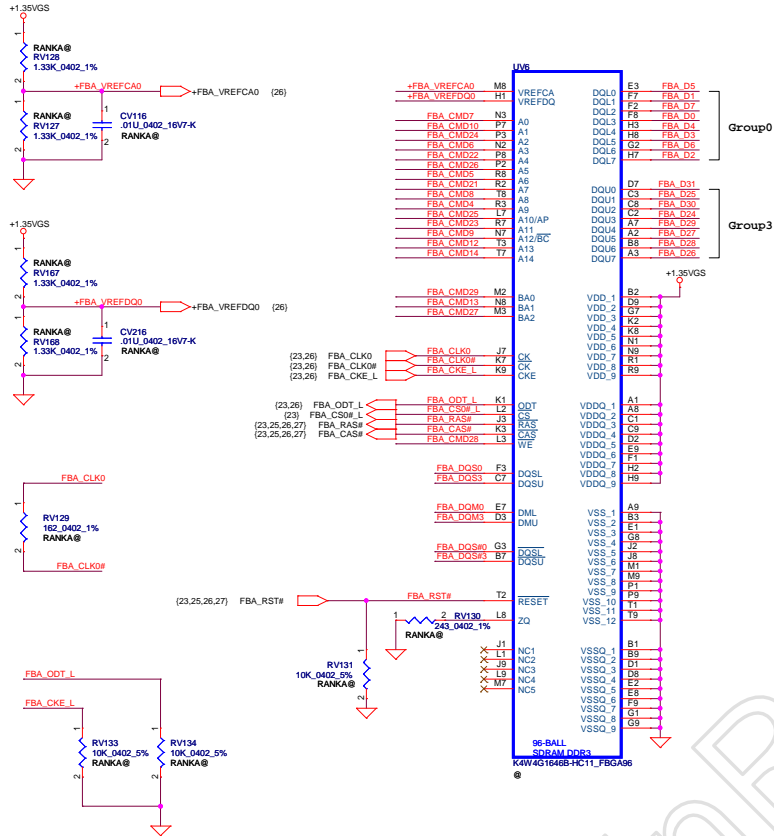
+1.35V TO +1.35VGS





| | | | | |
|---|------------------------------|-----------------|--|--|
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| | | | Page 22 of 56 | |

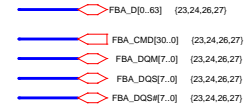
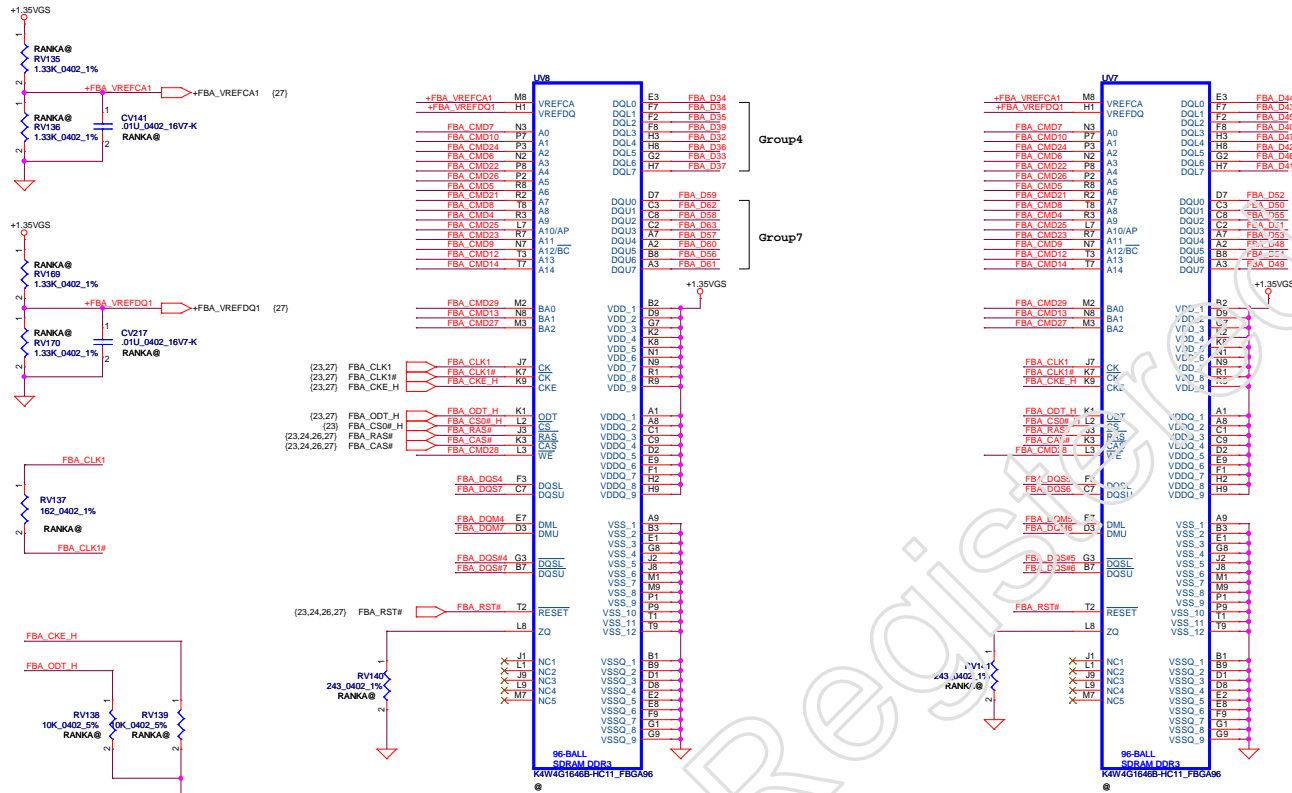
at least 16 mils width(optimal)
20 mils spacing to other signals/planes



CMD mapping mod Mode E

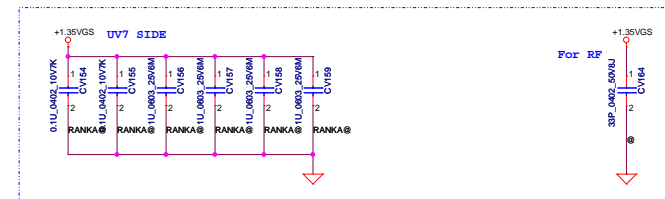
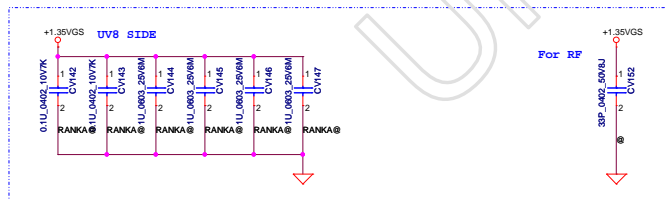
| Address | Rank0 | Rank1 |
|-----------|--------|---------|
| FBX_CMD0 | 0...31 | 32...63 |
| FBX_CMD1 | ODT_L | ODT_L |
| FBX_CMD2 | CS0#_L | CS1#_L |
| FBX_CMD3 | CKE_L | CKE_L |
| FBX_CMD4 | A9 | A11 |
| FBX_CMD5 | A6 | A7 |
| FBX_CMD6 | A3 | BA1 |
| FBX_CMD7 | A0 | A12 |
| FBX_CMD8 | A8 | A8 |
| FBX_CMD9 | A12 | A0 |
| FBX_CMD10 | A1 | A2 |
| FBX_CMD11 | RAS# | RAS# |
| FBX_CMD12 | A13 | A14 |
| FBX_CMD13 | BA1 | A3 |
| FBX_CMD14 | A14 | A13 |
| FBX_CMD15 | CAS# | CAS# |
| FBX_CMD16 | ODT_H | ODT_H |
| FBX_CMD17 | | CS1#_H |
| FBX_CMD18 | CS0#_H | |
| FBX_CMD19 | CKE_H | CKE_H |
| FBX_CMD20 | RST | RST |
| FBX_CMD21 | A7 | A6 |
| FBX_CMD22 | A4 | A5 |
| FBX_CMD23 | A11 | A9 |
| FBX_CMD24 | A2 | A1 |
| FBX_CMD25 | A10 | WE# |
| FBX_CMD26 | A5 | A4 |
| FBX_CMD27 | BA2 | |
| FBX_CMD28 | WE# | A10 |
| FBX_CMD29 | BA0 | BA0 |
| FBX_CMD30 | | BA2 |

at least 16 mils width(optimal)
20 mils spacing to other signals/planes

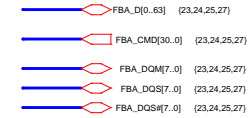
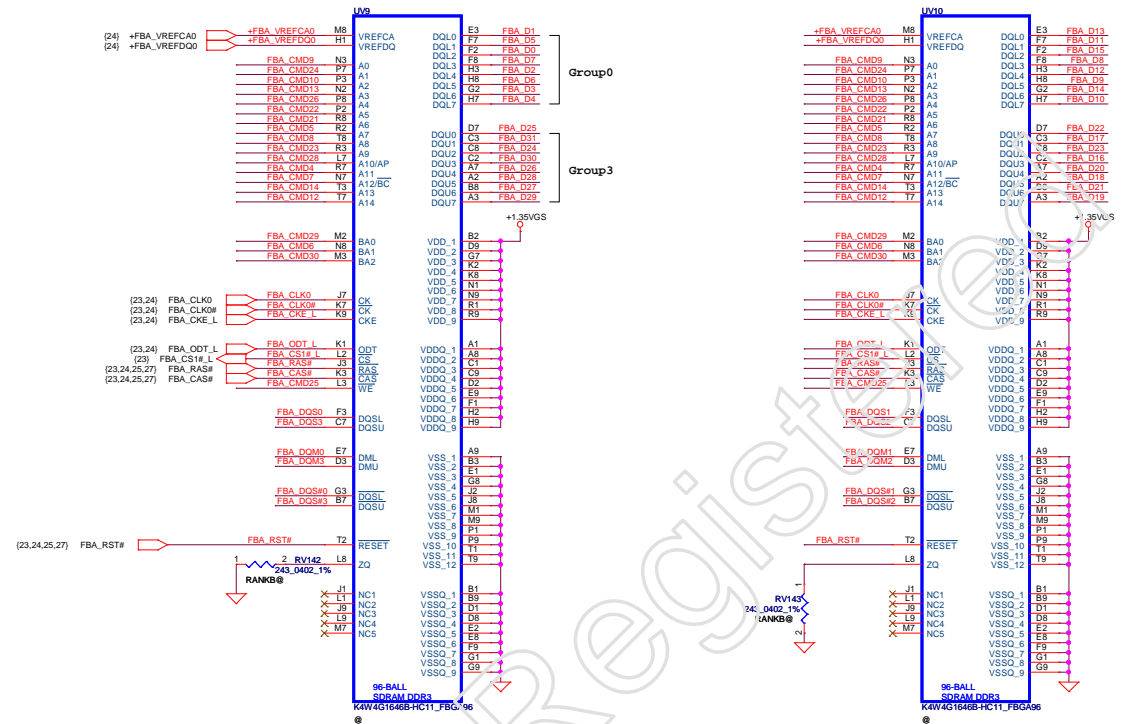


CMD mapping mod Mode E

| Address | Rank0 | Rank1 |
|-----------|--------|--------|
| FbX_CMD0 | 0..31 | 32..63 |
| FbX_CMD1 | ODT_L | ODT_L |
| FbX_CMD2 | CS0#_L | CS1#_L |
| FbX_CMD3 | CKE_L | CKE_L |
| FbX_CMD4 | A9 | A11 |
| FbX_CMD5 | A6 | A7 |
| FbX_CMD6 | A3 | BA1 |
| FbX_CMD7 | A0 | A12 |
| FbX_CMD8 | A8 | A8 |
| FbX_CMD9 | A12 | A0 |
| FbX_CMD10 | A1 | A2 |
| FbX_CMD11 | RAS# | RAS# |
| FbX_CMD12 | A13 | A14 |
| FbX_CMD13 | BA1 | A3 |
| FbX_CMD14 | A14 | A13 |
| FbX_CMD15 | CAS# | CAS# |
| FbX_CMD16 | ODT_H | ODT_H |
| FbX_CMD17 | | CS1#_H |
| FbX_CMD18 | CS0#_H | |
| FbX_CMD19 | CKE_H | CKE_H |
| FbX_CMD20 | RST | RST |
| FbX_CMD21 | A7 | A6 |
| FbX_CMD22 | A4 | A5 |
| FbX_CMD23 | A11 | A9 |
| FbX_CMD24 | A2 | A1 |
| FbX_CMD25 | A10 | WE# |
| FbX_CMD26 | A5 | A4 |
| FbX_CMD27 | BA2 | BA2 |
| FbX_CMD28 | WE# | A10 |
| FbX_CMD29 | BA0 | BA0 |
| FbX_CMD30 | | BA2 |

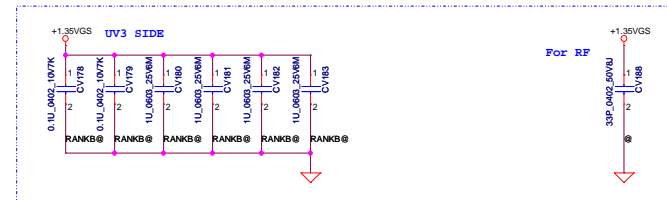
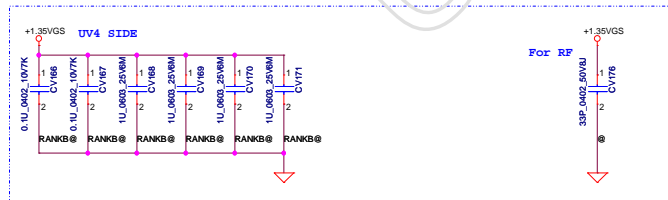


at least 16 mils width (optimal)
20 mils spacing to other signals / planes

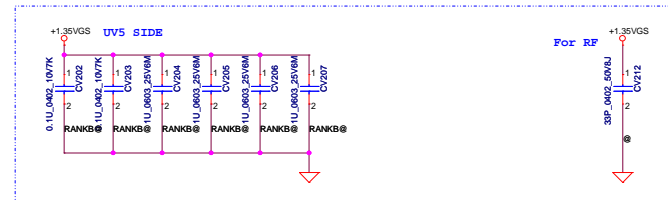
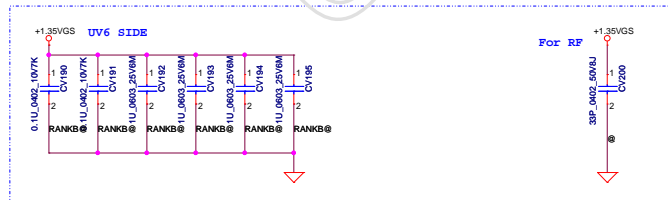
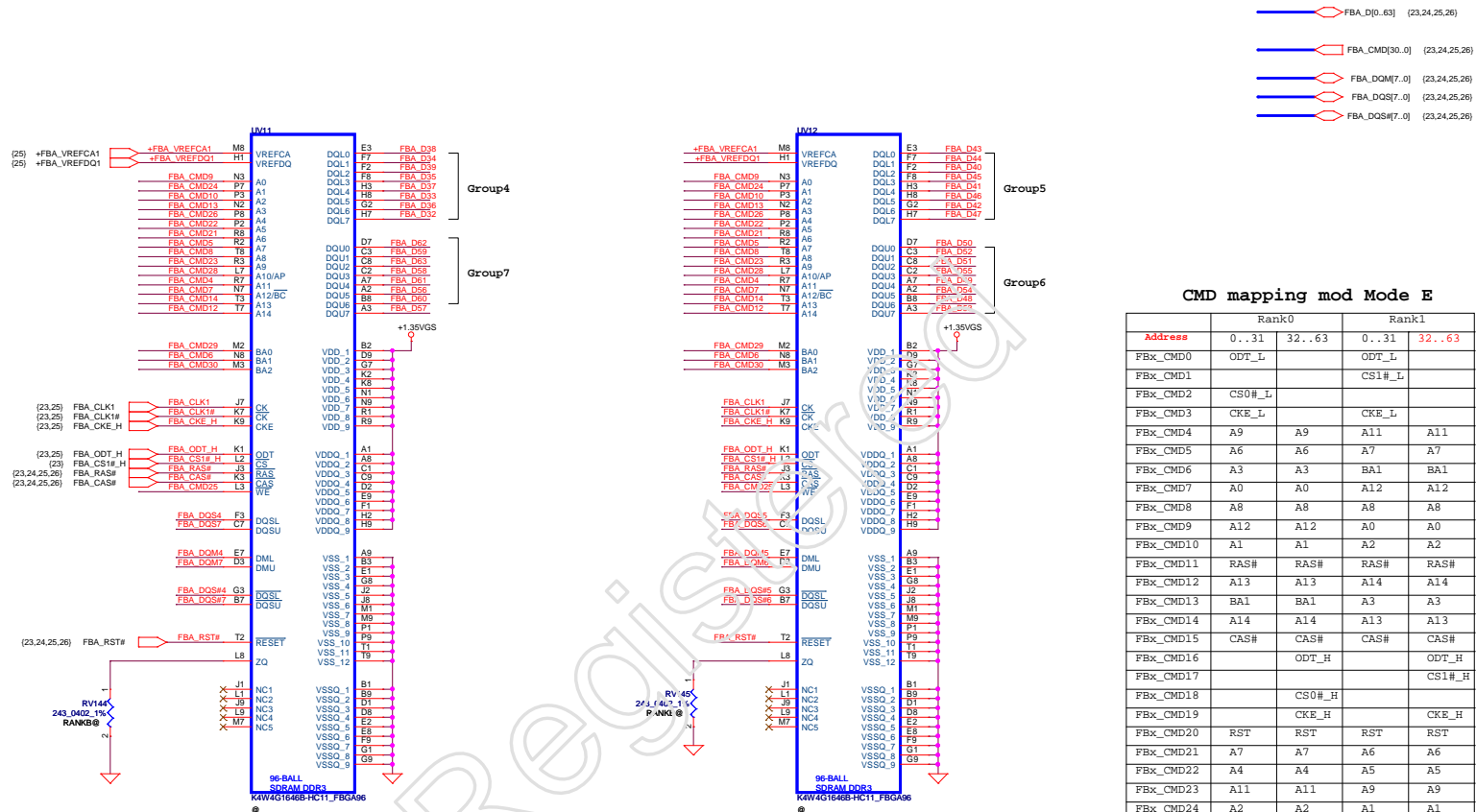


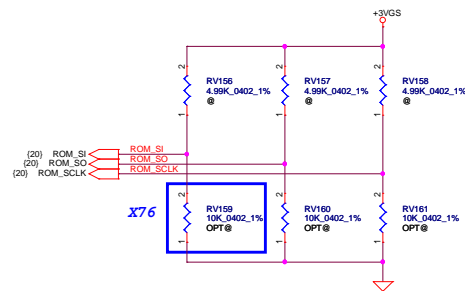
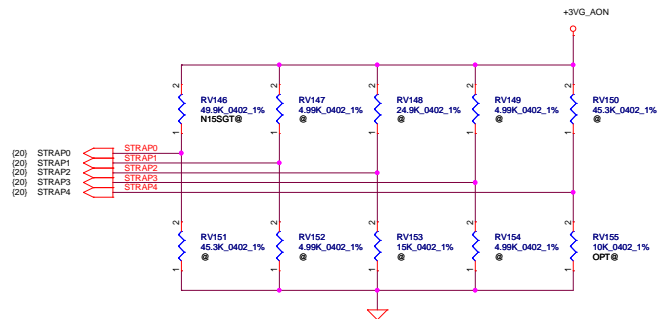
CMD mapping mod Mode E

| | Rank0 | Rank1 |
|-----------|--------------|--------------|
| Addresses | 0..31 32..63 | 0..31 32..63 |
| FBx_CMD0 | ODT_L | ODT_L |
| FBx_CMD1 | CS0#_L | CS1#_L |
| FBx_CMD3 | CKE_L | CKE_L |
| FBx_CMD4 | A9 | A9 |
| FBx_CMD5 | A6 | A6 |
| FBx_CMD6 | A3 | A3 |
| FBx_CMD7 | A0 | A0 |
| FBx_CMD8 | A8 | A8 |
| FBx_CMD9 | A12 | A12 |
| FBx_CMD10 | A1 | A1 |
| FBx_CMD11 | RAS# | RAS# |
| FBx_CMD12 | A13 | A13 |
| FBx_CMD13 | BA1 | BA1 |
| FBx_CMD14 | A14 | A14 |
| FBx_CMD15 | CAS# | CAS# |
| FBx_CMD16 | ODT_H | ODT_H |
| FBx_CMD17 | | CS1#_H |
| FBx_CMD18 | CS0#_H | |
| FBx_CMD19 | CKE_H | CKE_H |
| FBx_CMD20 | RST | RST |
| FBx_CMD21 | A7 | A7 |
| FBx_CMD22 | A4 | A4 |
| FBx_CMD23 | A11 | A11 |
| FBx_CMD24 | A2 | A2 |
| FBx_CMD25 | A10 | A10 |
| FBx_CMD26 | A5 | A5 |
| FBx_CMD27 | BA2 | BA2 |
| FBx_CMD28 | WE# | WE# |
| FBx_CMD29 | BA0 | BA0 |
| FBx_CMD30 | | BA2 |



at least 16 mils width(optimal)
20 mils spacing to other signals/planes





| Physical Strapping pin | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|------------------------|------------|---|------------------------|------------------------|------------------------|
| ROM_SCLK | +3VGS | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| ROM_SI | +3VGS | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] |
| ROM_SO | +3VGS | DEVID_SEL | PCIE_CFG | SMB_ALT_ADDR | VGA_DEVICE |
| STRAP0 | +3VGS | Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up) | | | |
| STRAP1 | +3VGS | | | | |
| STRAP2 | +3VGS | | | | |
| STRAP3 | +3VGS | | | | |
| STRAP4 | +3VGS | Reserved(keep pull-up and pull-down footprint and not stuff by default) | | | |

| Resistor Values | Pull-up to +3VGS | Pull-down to Gnd |
|----------------------|------------------|------------------|
| 4.99K SD03445918J | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 24.9K SD03445428J | 1100 | 0100 |
| 30.1K SD03440128J | 1101 | 0101 |
| 34.8K SD03443428J | 1110 | 0110 |
| 45.3K SD03445328J | 1111 | 0111 |

| DEVID_SEL | |
|-----------|-----------|
| 0 | (Default) |
| 1 | |

| PCIE_CFG | |
|----------|-----------|
| 0 | (Default) |
| 1 | |

| SMBUS_ALT_ADDR | |
|----------------|------------------------|
| 0 | 0x9E (Default) |
| 1 | 0x9C (Multi-GPU usage) |

| VGA_DEVICE | |
|------------|-----------------------------|
| 0 | 3D Device (Class Code 302h) |
| 1 | VGA Device (Default) |

| Physical Strapping pin | Power Rail | Strap Mapping |
|------------------------|------------|----------------|
| ROM_SCLK | +3VGS | SMB_ALT_ADDR |
| ROM_SI | +3VGS | CUB_VFNOR |
| ROM_SO | +3VGS | VGA_DEVICE |
| STRAP0 | +3VGS | RAM_CFG[0] |
| STRAP1 | +3VGS | RAM_CFG[1] |
| STRAP2 | +3VGS | RAM_CFG[2] |
| STRAP3 | +3VGS | RAM_CFG[3] |
| STRAP4 | +3VGS | PCIE_MAX_SPEED |

X76

| GPU | FB Memory (DDR3) | ROM_SI | ROM_SO | ROM_SCLK | STRAP0 | STRAP1 | STRAP2 | STRAP3 | STRAP4 |
|---------|------------------|----------------------|----------|----------|----------|----------|----------|----------|----------|
| N15S-GT | Hynix 900MHz | H5TC4G63AFR-11C | 0x3 | | | | | | |
| | 256M x 16 | PD 20K | | | | | | | |
| | Micron 900MHz | MT41J256M16HA-093G:E | 0x4 | | | | | | |
| | 256M x 16 | PD 24.9K | | | | | | | |
| | Samsung 900MHz | K4W4G1646D-BC1A | 0x5 | | | | | | |
| | 256M x 16 | PD 30.1K | PD 4.99K | PD 4.99K | PU 49.9K | Un-stuff | Un-stuff | Un-stuff | Un-stuff |


| GPU | FB Memory (DDR3) | STRAP3 | STRAP2 | STRAP1 | STRAP0 | STRAP4 | ROM_SI | ROM_SO | ROM_SCLK |
|---------|------------------|----------------------|--------|--------|--------|--------|--------|--------|----------|
| N15V-QM | Hynix 900MHz | H5TC4G63AFR-11C | 0x4 | PD 10K | PU 10K | PD 10K | PD 10K | | |
| | 256M x 16 | 0x4 | | | | | | | |
| | Micron 900MHz | MT41J256M16HA-093G:E | 0xD | PU 10K | PU 10K | PD 10K | PU 10K | | |
| | 256M x 16 | 0xD | | | | | | | |
| | Hynix 900MHz | H5TC2G63FFR-11C | 0xC | PU 10K | PU 10K | PD 10K | PD 10K | PD 10K | PD 10K |
| | 128M x 16 | 0xC | | | | | | | |
| | Micron 900MHz | MT41J128M16JT-093G | 0x1 | PD 10K | PD 10K | PD 10K | PU 10K | | |
| | 128M x 16 | 0x1 | | | | | | | |
| | Samsung 900MHz | K4W2G1646Q-BC1A | 0xE | PU 10K | PU 10K | PU 10K | PD 10K | | |
| | 128M x 16 | 0xE | | | | | | | |

| VRAM | X76 | VRAM P/N |
|---------|-------------|-------------|
| Samsung | X7604112001 | SA00005SH40 |
| | | |
| Micron | X7604012002 | SA00005M120 |
| | | |
| Hynix | X7604012001 | SA00005VS00 |

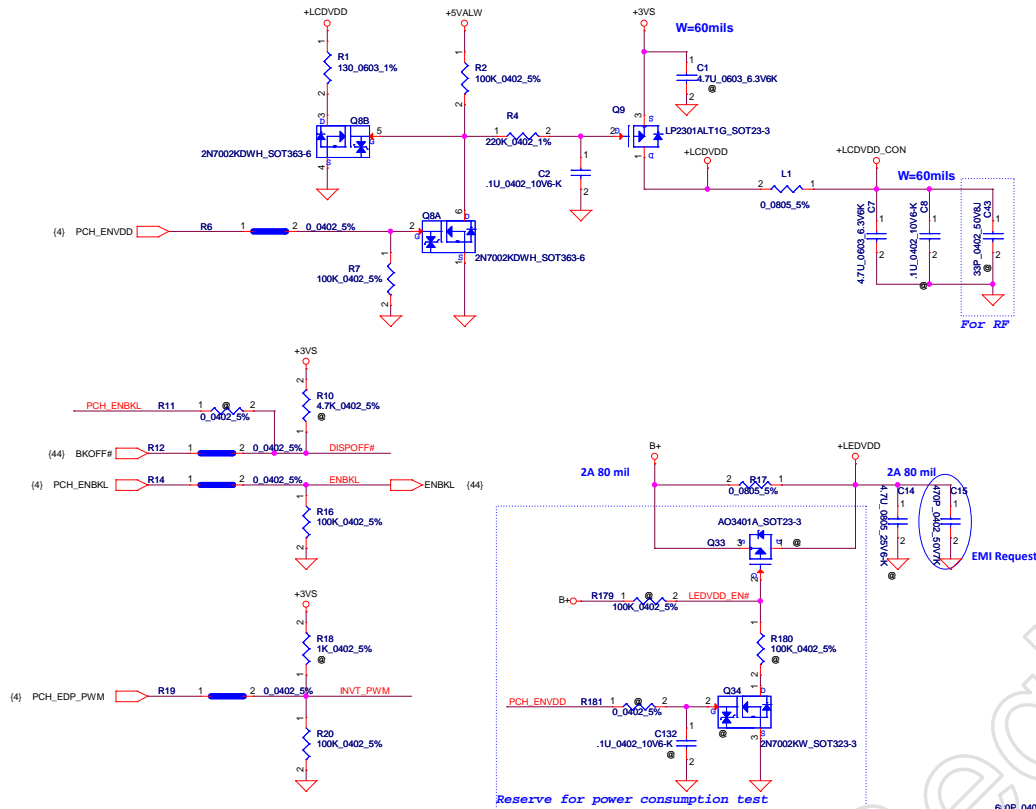
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|--|------------|------------------------------|------------|
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| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 |
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|-----|-----------------|------|---------------------------|-------|----|----|----|
| C | ACLU9 | | | | | | |
| 0.2 | | | | | | | |

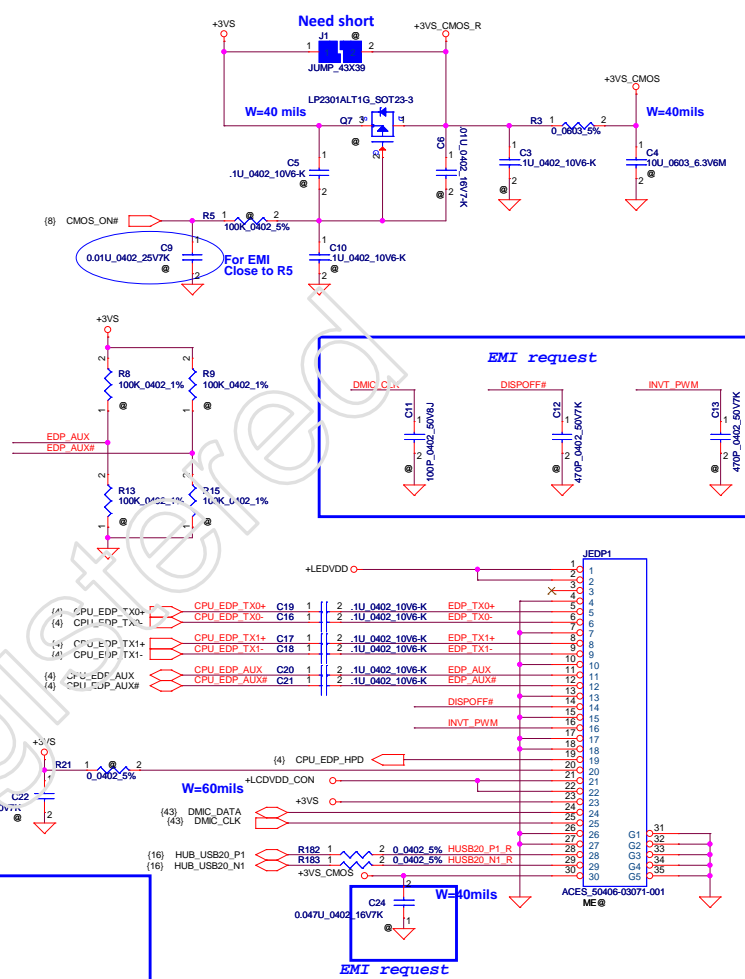
UnRegistered

| | | | | | | |
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| Security Classification | LC Future Center Secret Data | | | Title |  | |
| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 | Blank | | |
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| | | | | Date: Monday, December 23, 2013 | ACTU9 | 0.2 |
| | | | | Sheet 29 of 59 | | |

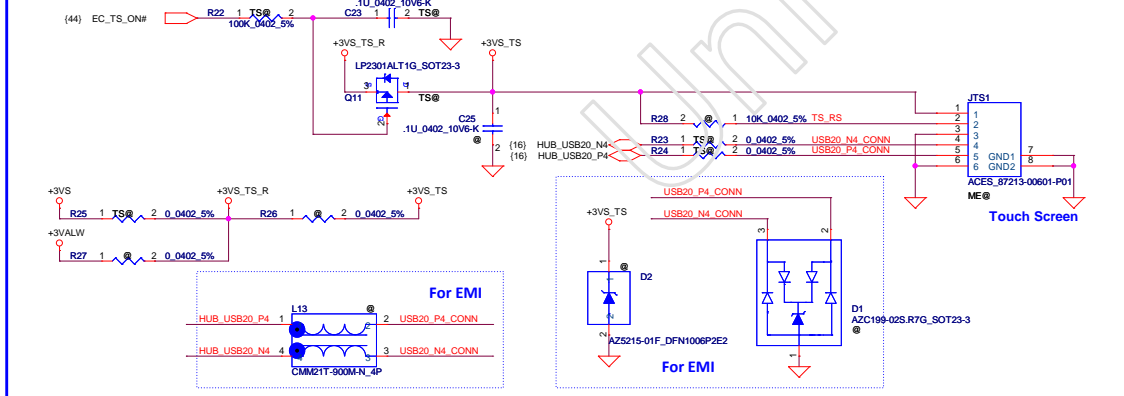
LCD POWER CIRCUIT



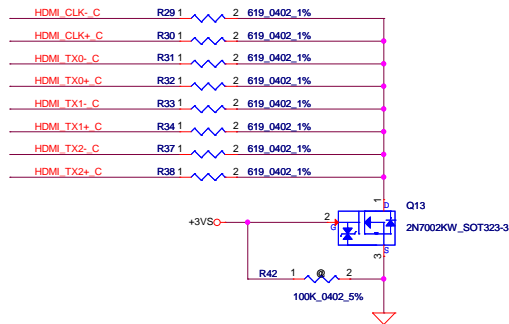
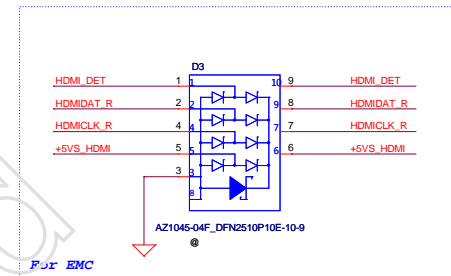
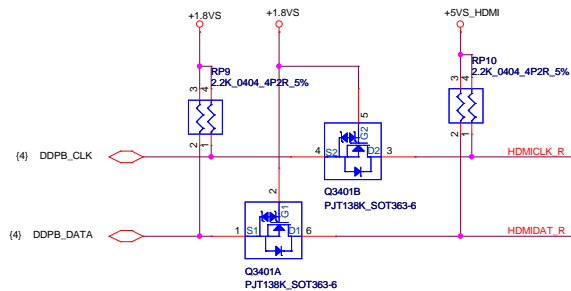
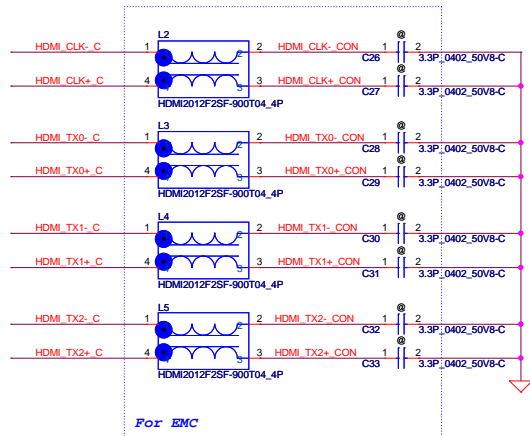
CMOS Camera



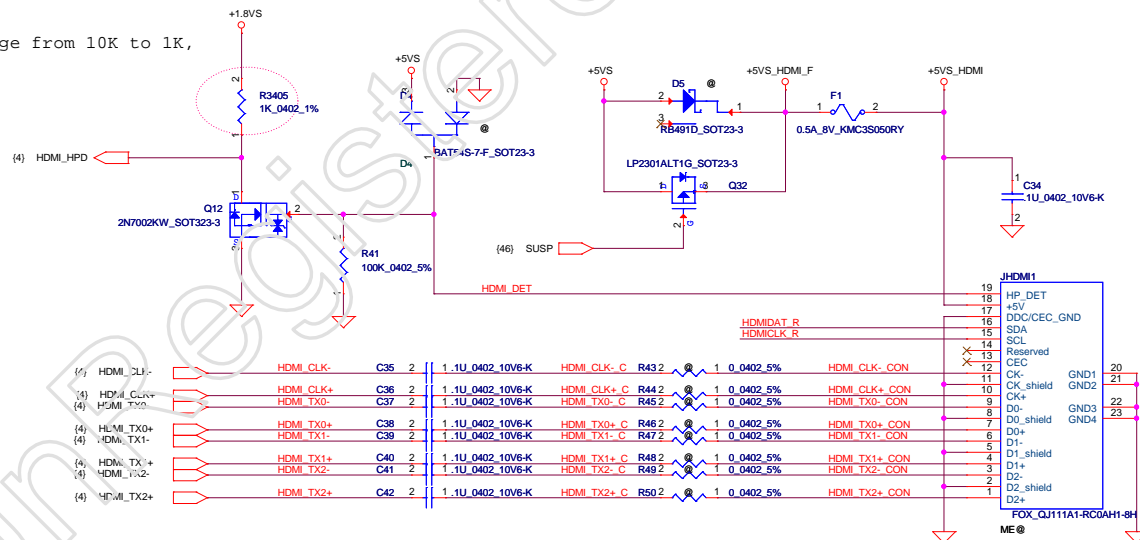
Touch Screen



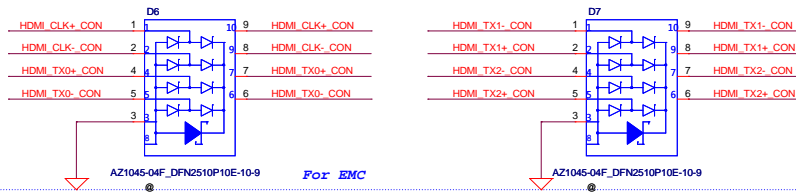
| Security Classification | | | |
|--|------------|---------------------------|------------|
| LC Future Center Secret Data | | | |
| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 |
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| Title | | eDP/ CMOS/Touch screen | |
| Document Number | | ACLU9 | |
| Date | | Monday, December 23, 2013 | |
| Sheet | | 33 of 59 | |
| Rev | | 0.2 | |



R4602 change from 10K to 1K, as Vienna



Close to JHDMI1

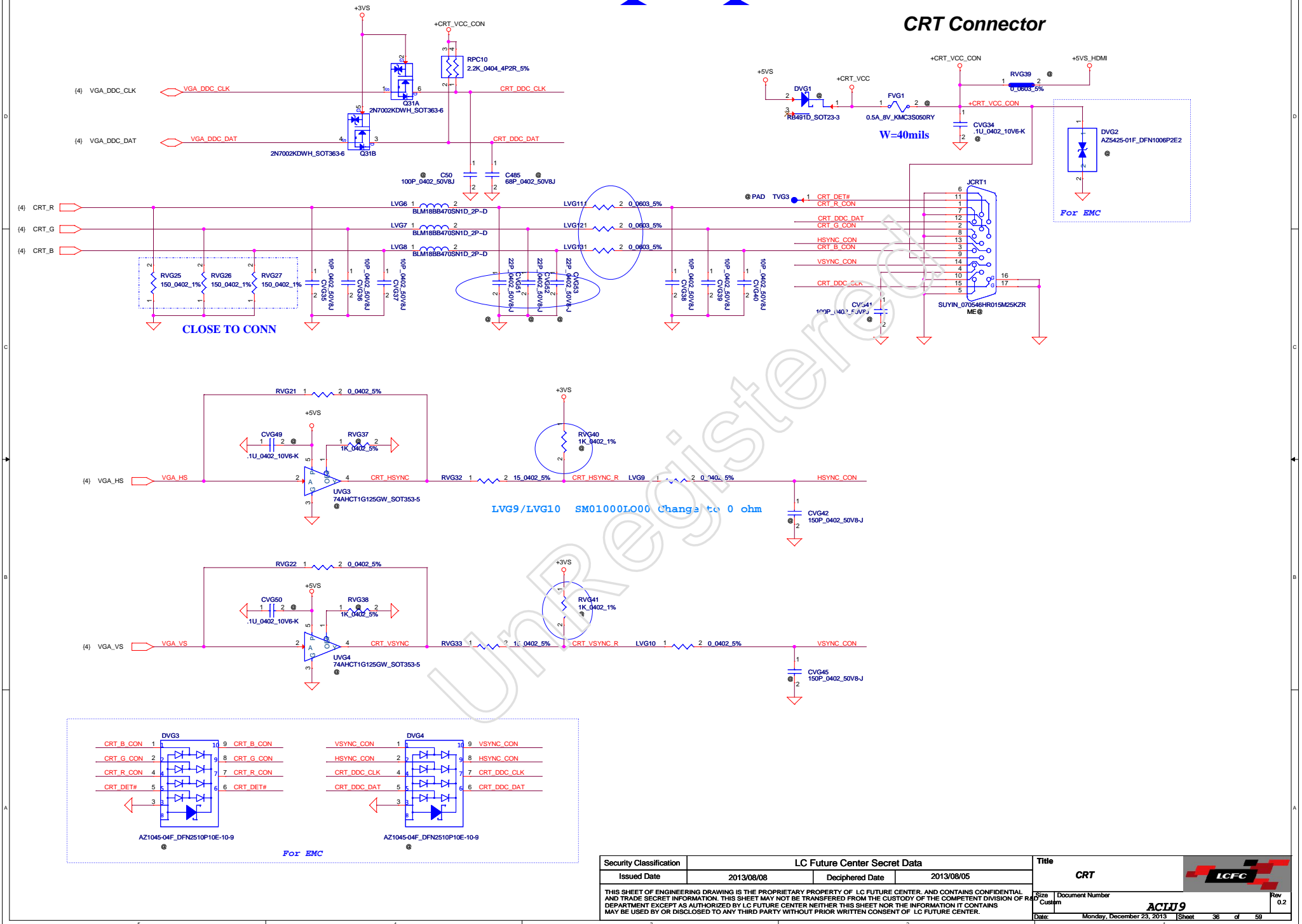


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| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 | Size | | |
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| | | | | | ACLU9 | 0.2 |
| | | | | Date: | Monday, December 23, 2013 | Sheet 34 of 59 |

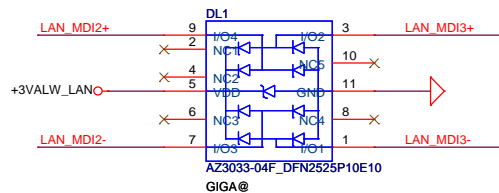
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| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | | 2013/08/08 | Deciphered Date | 2013/08/05 | DP to CRT Converter(PS8613) |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER. | | | | Size | Document Number |
| | | | | Custom | ACLU 9 |
| | | | | Date: | Monday, December 23, 2013 |
| | | | | Sheet | 36 of 59 |
| | | | | Rev | 0.2 |

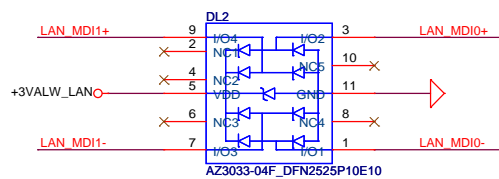
CRT Connector



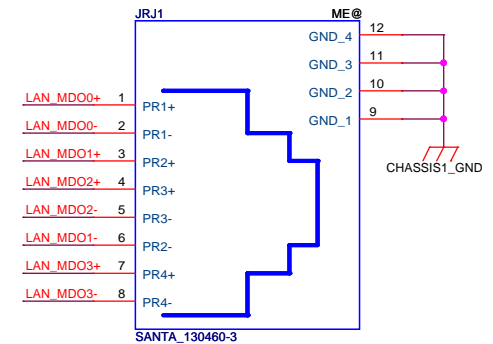
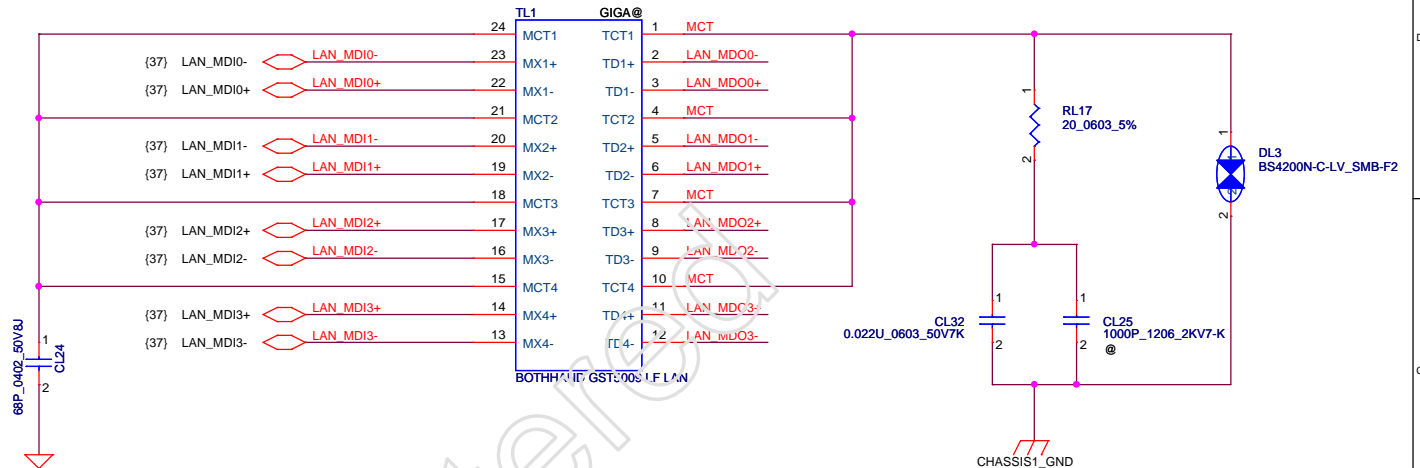
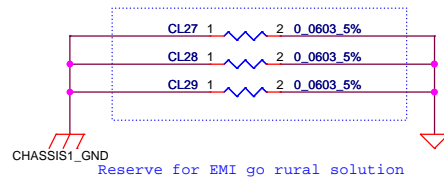
DL1/DL2
1'S PN:SC300003M00



Place Close to TL1

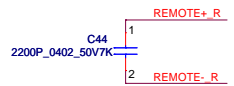


Place Close to TL2

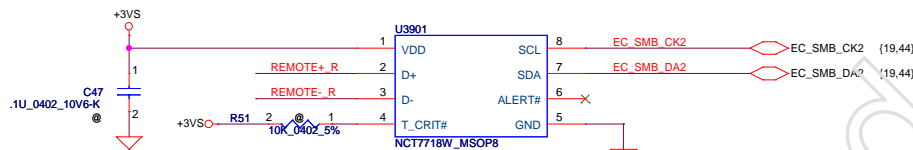


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| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 | LAN Transformer | |
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| | | | | Date: | Monday, December 23, 2013 |
| | | | | Sheet | 38 of 59 |
| | | | | Rev | 0.2 |

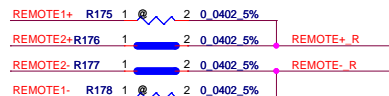
Close to U3901



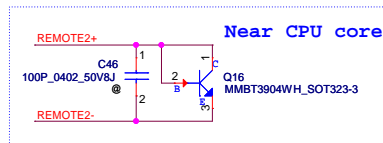
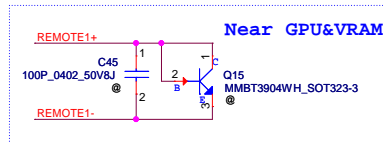
SMSC thermal sensor
placed near DIMM



Address 1001_100xb

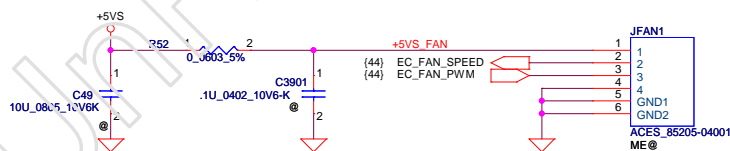


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

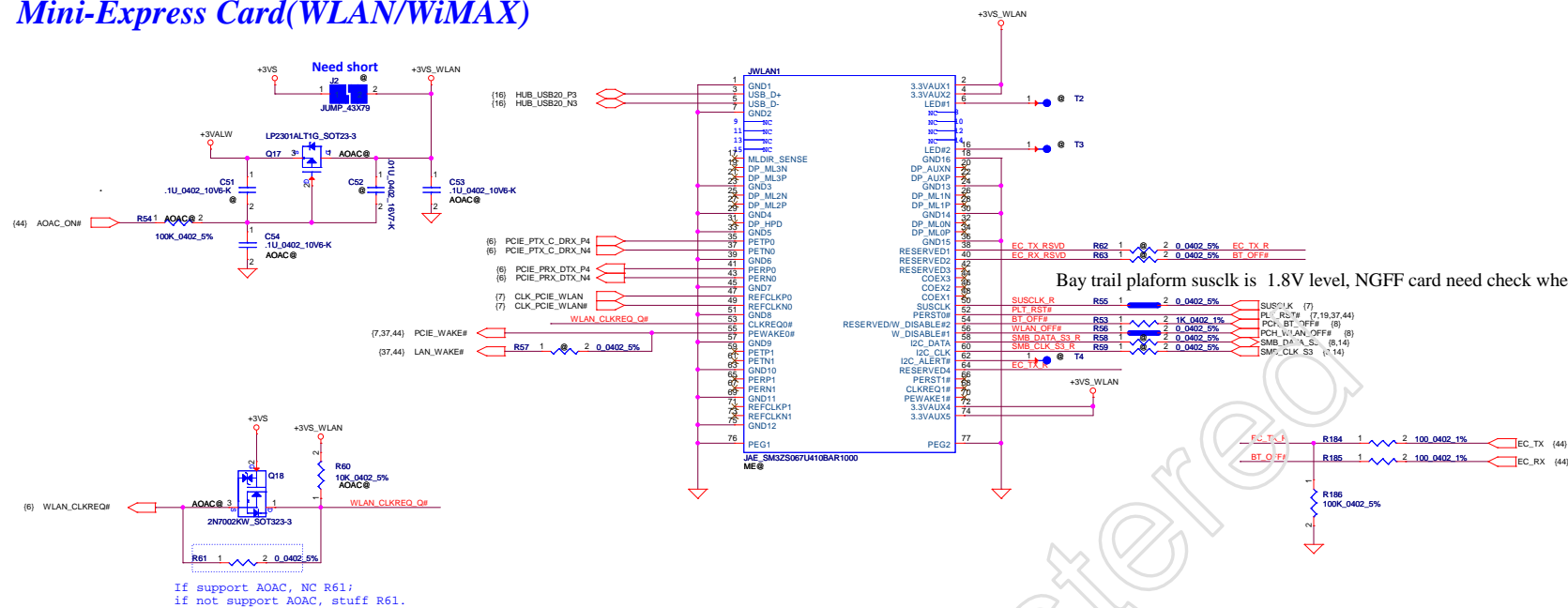


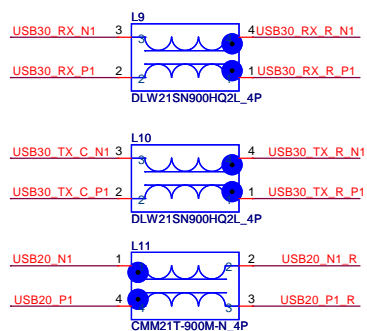
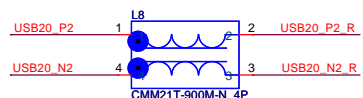
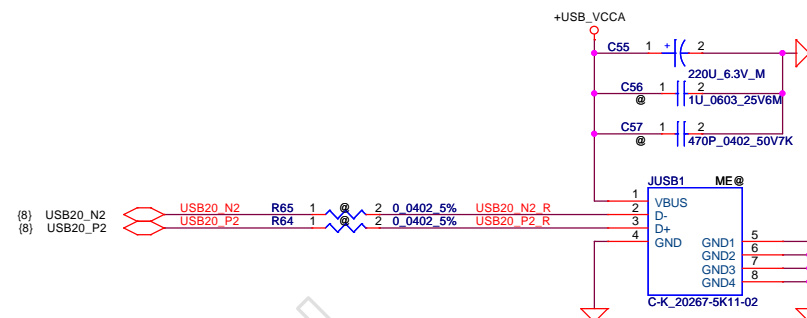
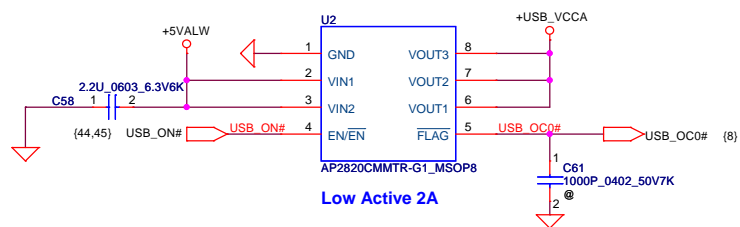
Baytrail SOC use thermal sensor to read the thermal,
Baytrail don't has PECI signal

FAN Conn

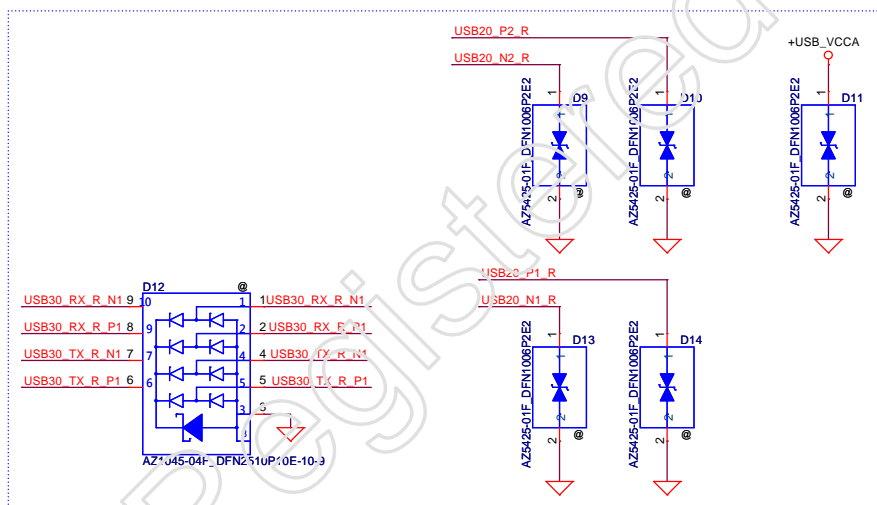


| | | | | | |
|--|------------------------------|-----------------|------------|-------------------------|---------------------------|
| Security Classification | LC Future Center Secret Data | | Title | Thermal sensor/FAN CONN | |
| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 | Size | Document Number |
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| | | | | Date: | Monday, December 23, 2013 |
| | | | | Sheet | 39 of 59 |

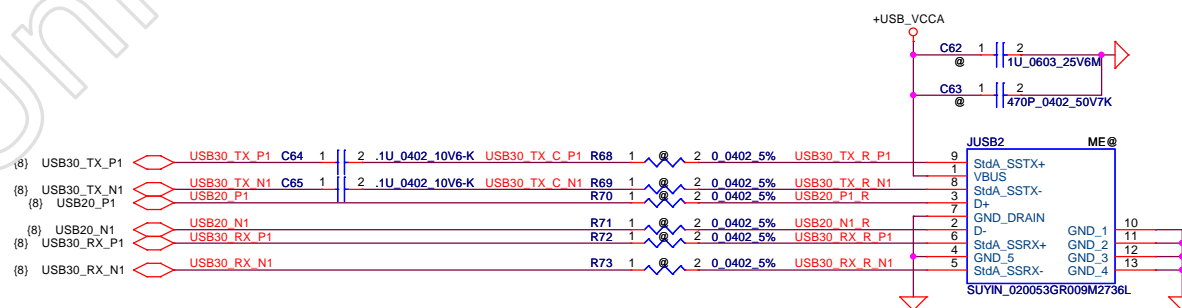





For EMC

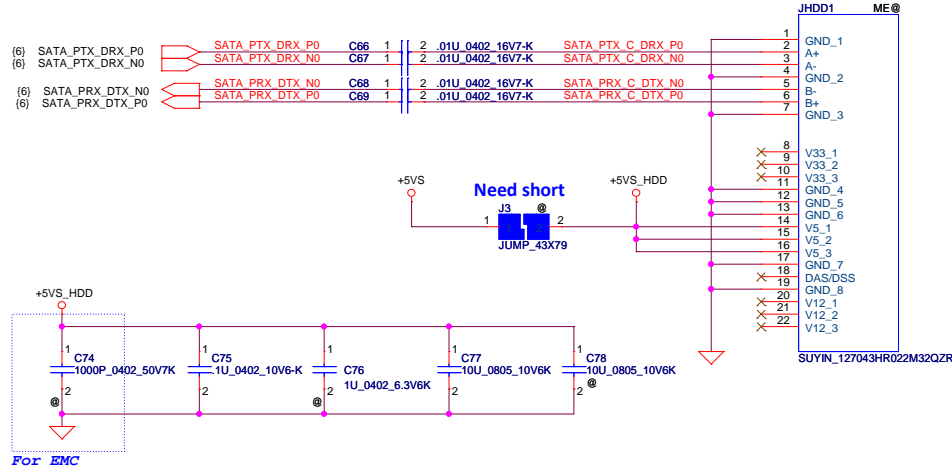


.....
For EMC

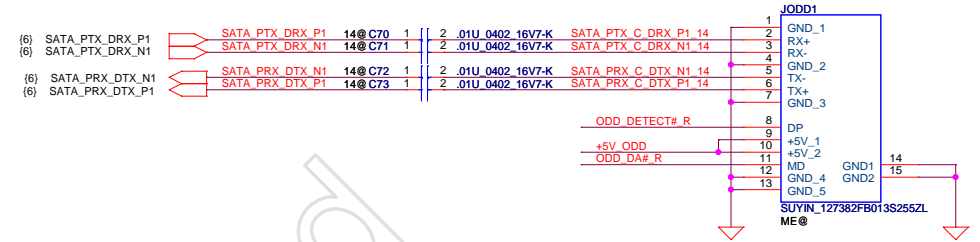


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|--|------------|------------------------------|------------|--|---------------------------------|
| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 | USB2.0/USB3.0 PORT (LEFT)  | |
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| Date: | | Monday, December 23, 2013 | | Sheet | 41 of 59 |

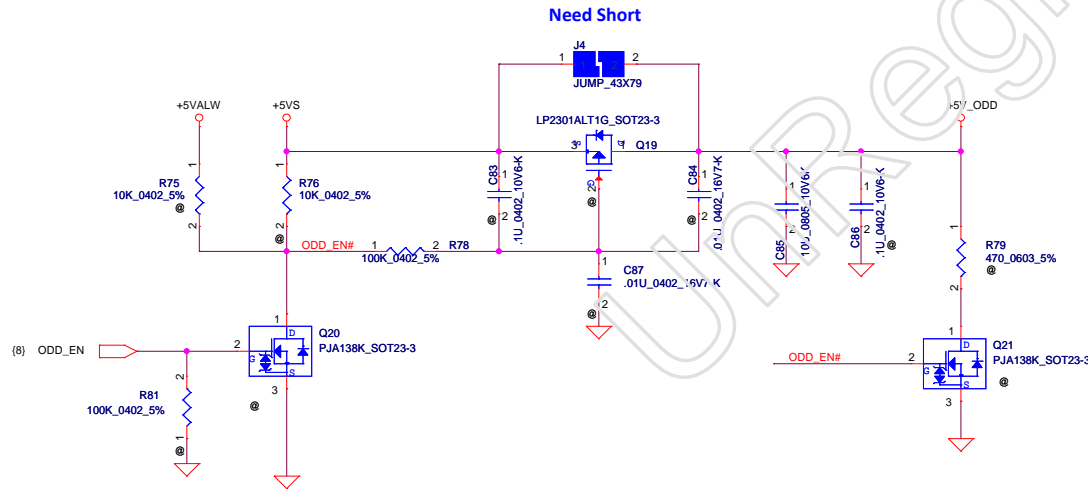
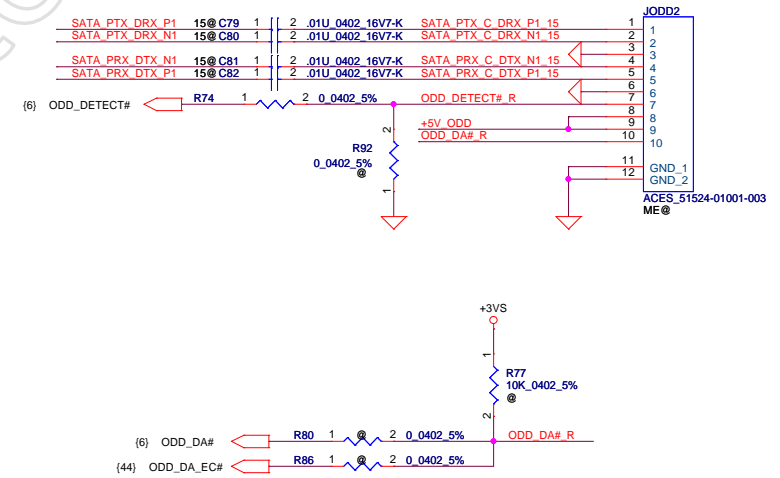
SATA HDD Conn.



FOR 14" SATA ODD Conn.

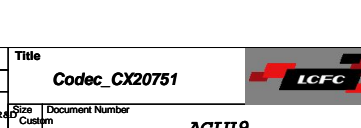
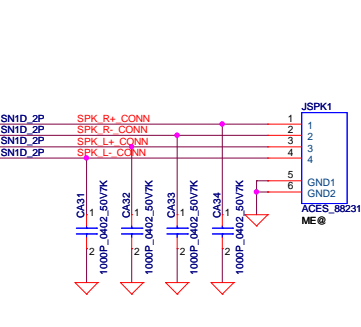
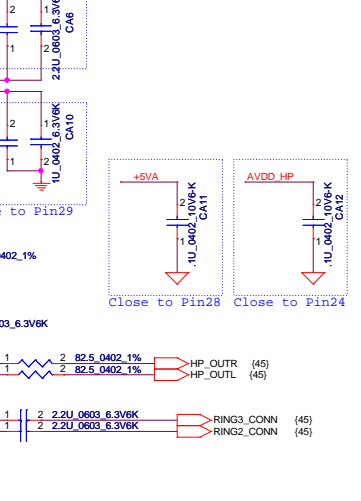
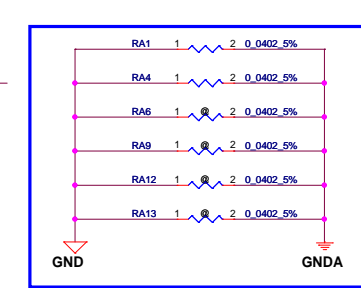
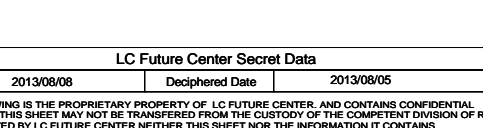
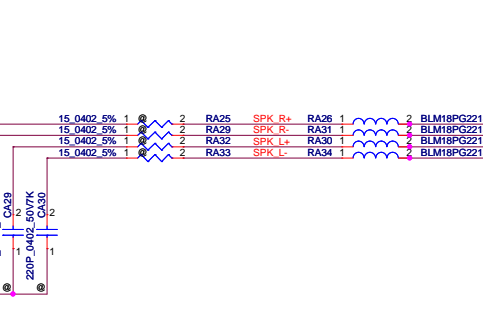
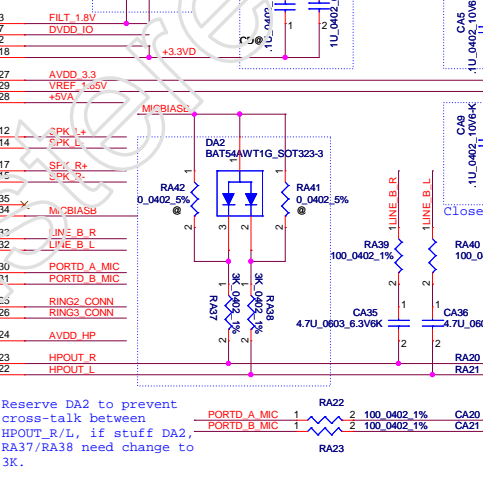
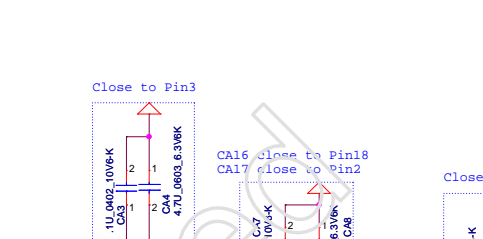
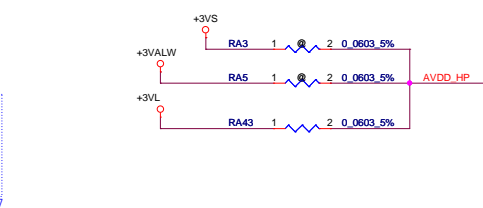
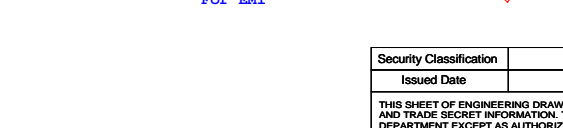
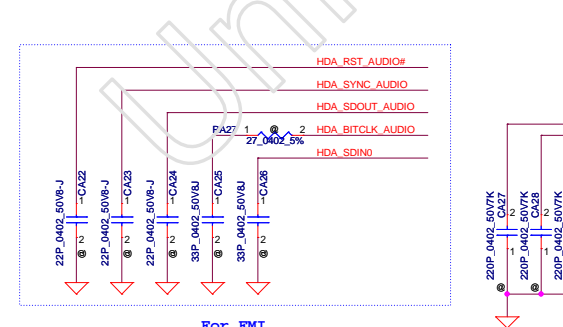
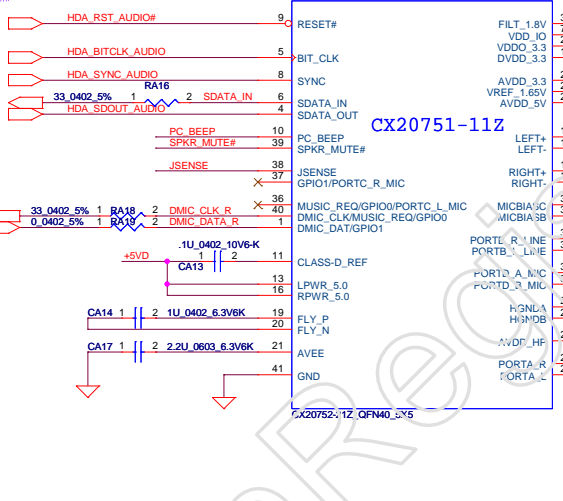
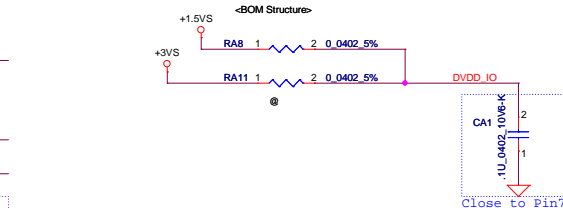
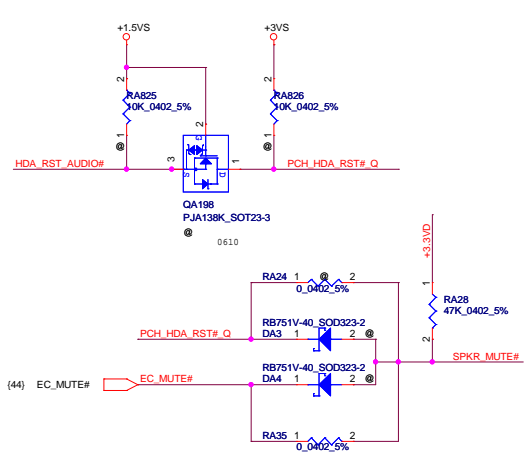
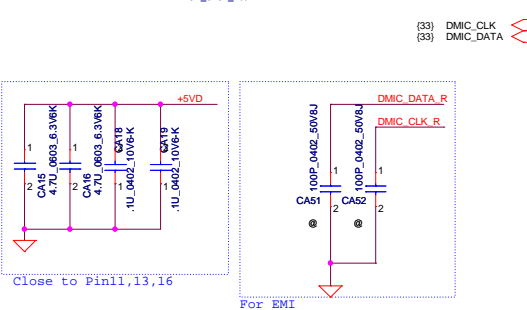
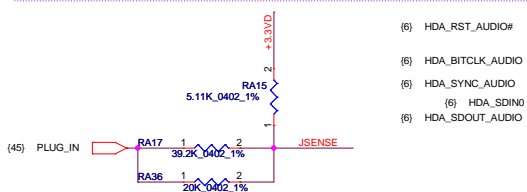
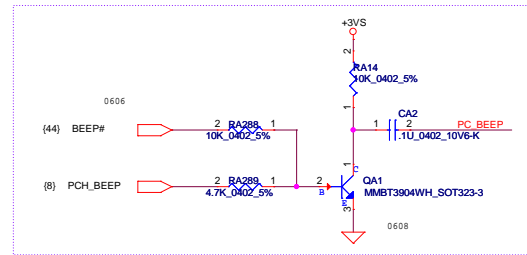


FOR 15" SATA ODD FFC Conn

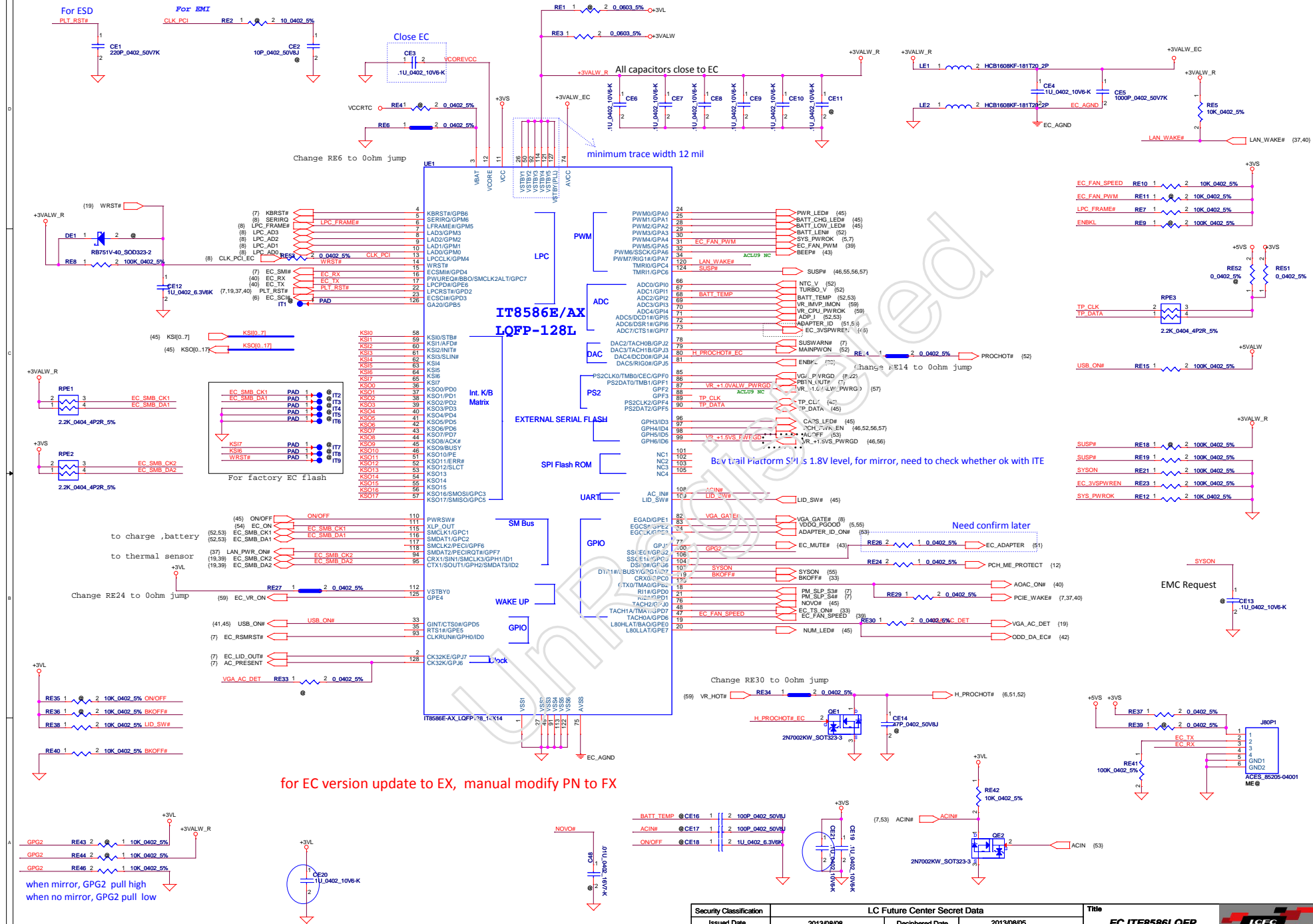



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| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 | Size | Document Number |
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| ACLU9 | | | | Rev | 0.2 |
| Date: Monday, December 23, 2013 | | | | Sheet | 42 of 59 |

Same as Vienna

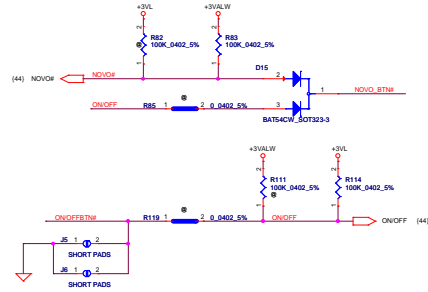


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| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 | Size | Document Number | Rev |
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| | | | | Date | Monday, December 23, 2013 | Sheet 43 of 59 |



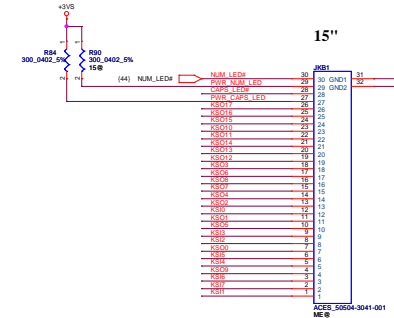
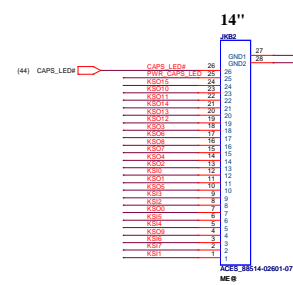
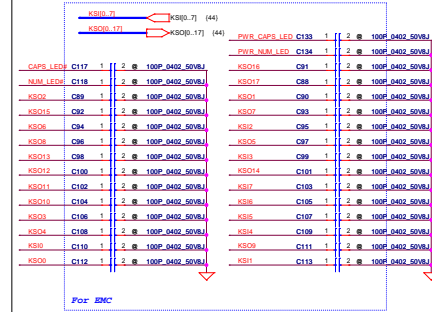
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| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 | EC ITE8586LQPP | |
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ON/OFF switch

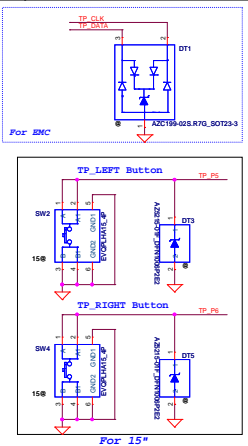
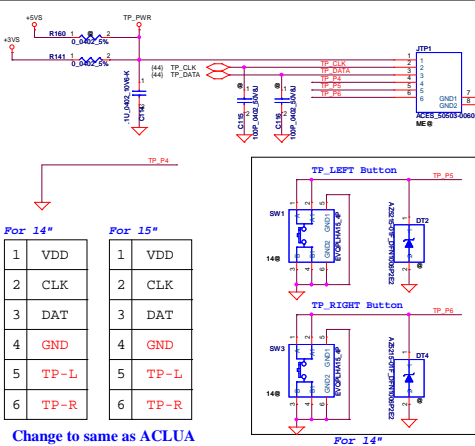


TP/B Connector

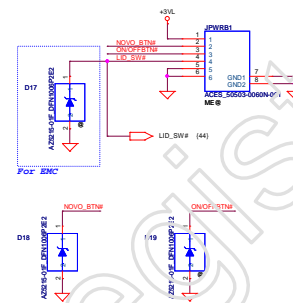
K/B Connector



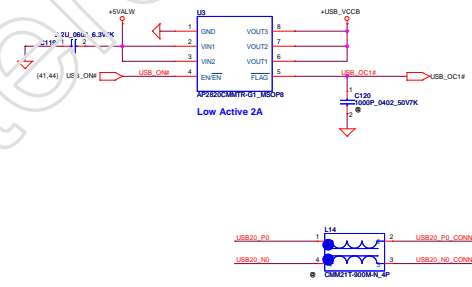
| 14" | 15" |
|--------|----------|
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| KB_2 | KB12_14 |
| KB_3 | KB13_14 |
| KB_4 | KB14_14 |
| KB_5 | KB15_14 |
| KB_6 | KB16_14 |
| KB_7 | KB17_14 |
| KB_8 | KB18_14 |
| KB_9 | KB19_14 |
| KB_10 | KB20_14 |
| KB_11 | KB21_14 |
| KB_12 | KB22_14 |
| KB_13 | KB23_14 |
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| KB_58 | KB68_14 |
| KB_59 | KB69_14 |
| KB_60 | KB70_14 |
| KB_61 | KB71_14 |
| KB_62 | KB72_14 |
| KB_63 | KB73_14 |
| KB_64 | KB74_14 |
| KB_65 | KB75_14 |
| KB_66 | KB76_14 |
| KB_67 | KB77_14 |
| KB_68 | KB78_14 |
| KB_69 | KB79_14 |
| KB_70 | KB80_14 |
| KB_71 | KB81_14 |
| KB_72 | KB82_14 |
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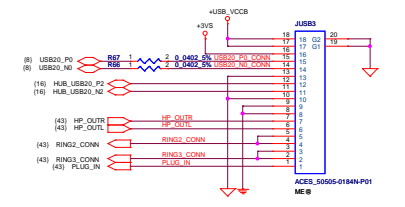
PWR/B Connector



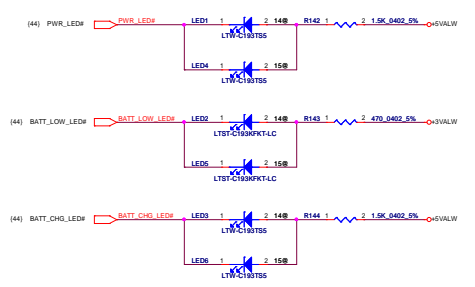
Eight S/ds USB2.0 Port X 1 (USB/B)



USB I/O Connector

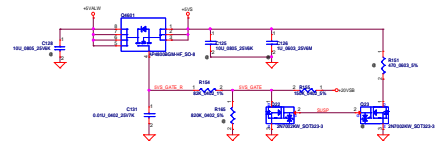


LED

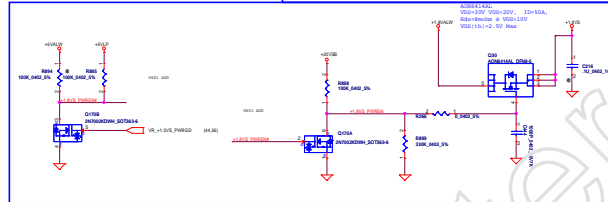
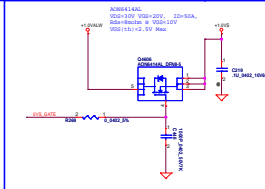
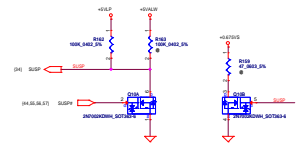
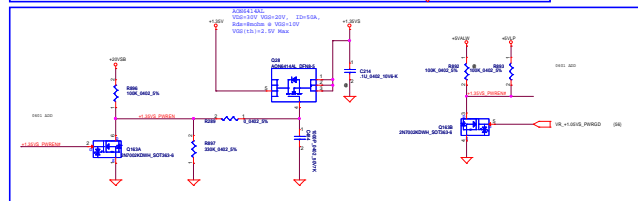
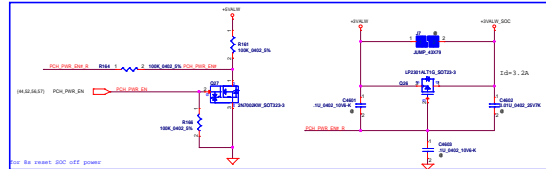
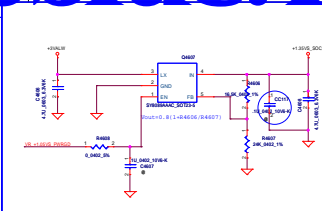
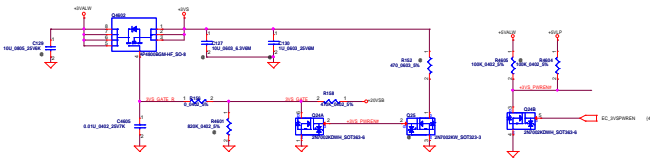


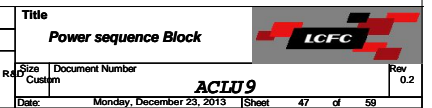
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|-------------------------|------------------------------|-----------------|
| Issued Date | 2013/08/08 | Deciphered Date |
| Deciphered Date | 2013/08/05 | 2013/08/05 |
| Document Number | KB/PWR/IO/LED/TP Conn. | Rev |
| Version | 0.2 | 0.2 |
| Date | Monday, December 25, 2012 | 08:45 |

+5VAIN to +5VS
AP4800BQM
VGS=10V, ID=9A, Rds=18m ohm
VGS=-25V




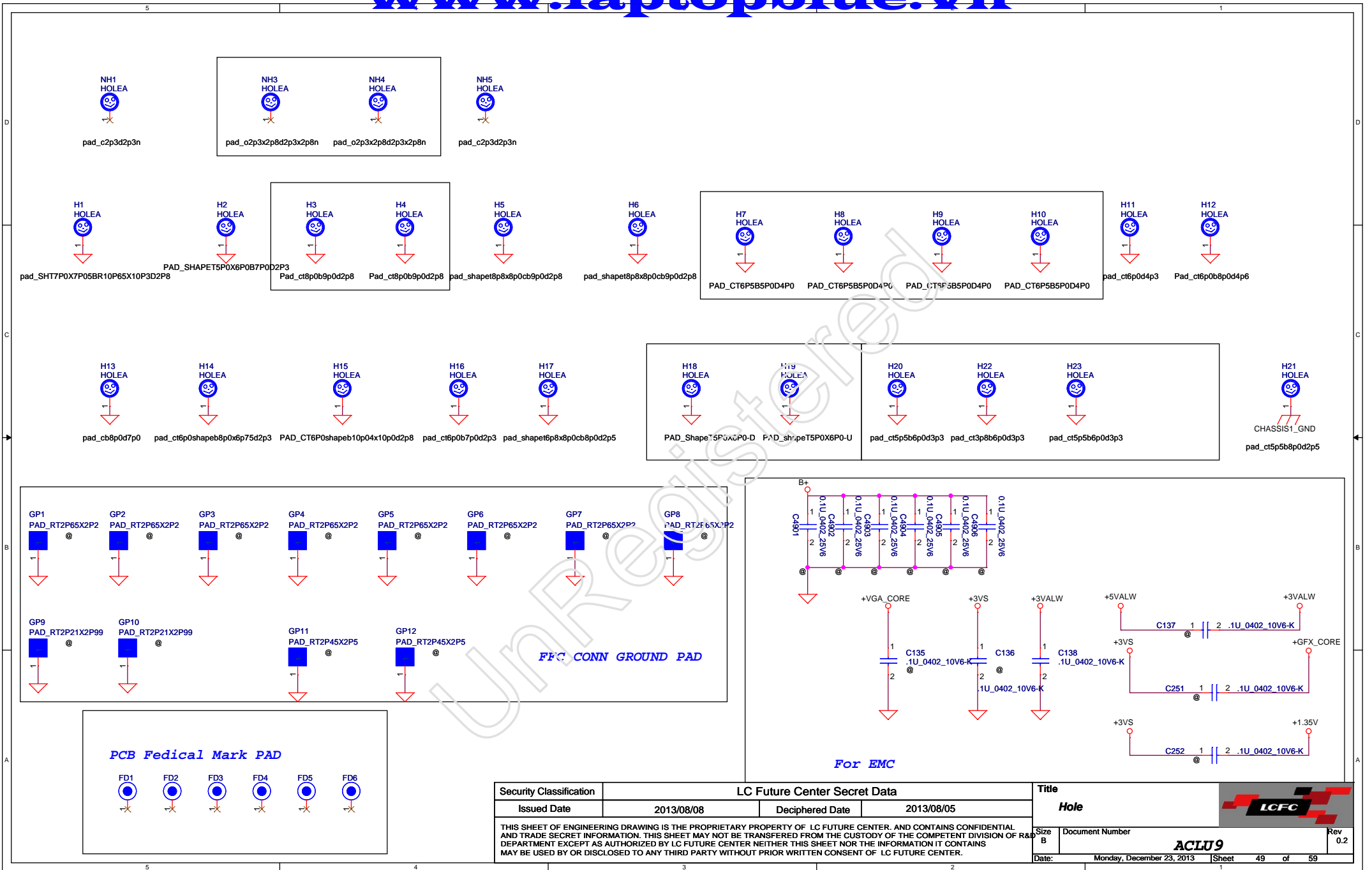
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VGS=10V, ID=9A, Rds=18m ohm
VGS=-25V





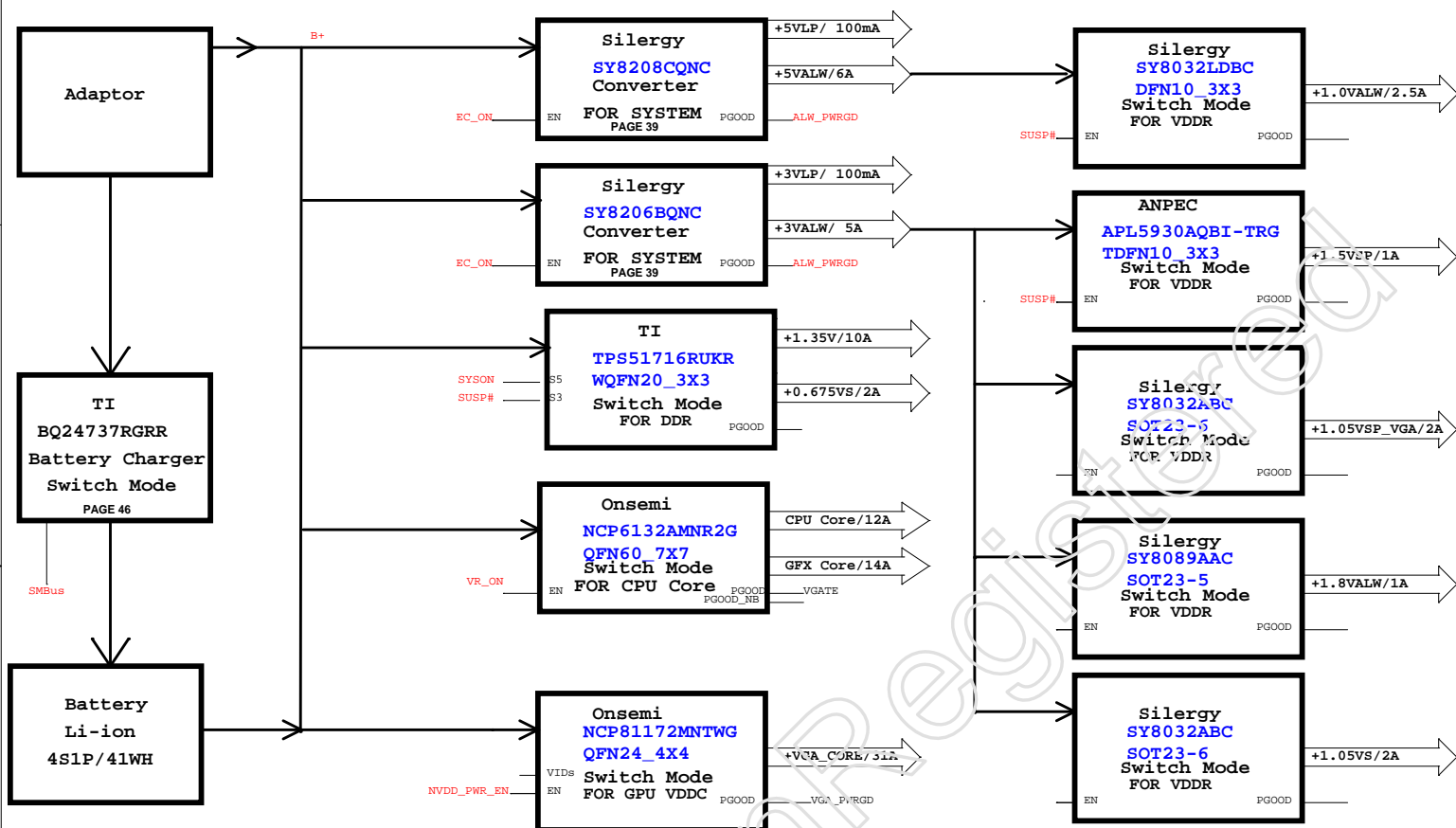
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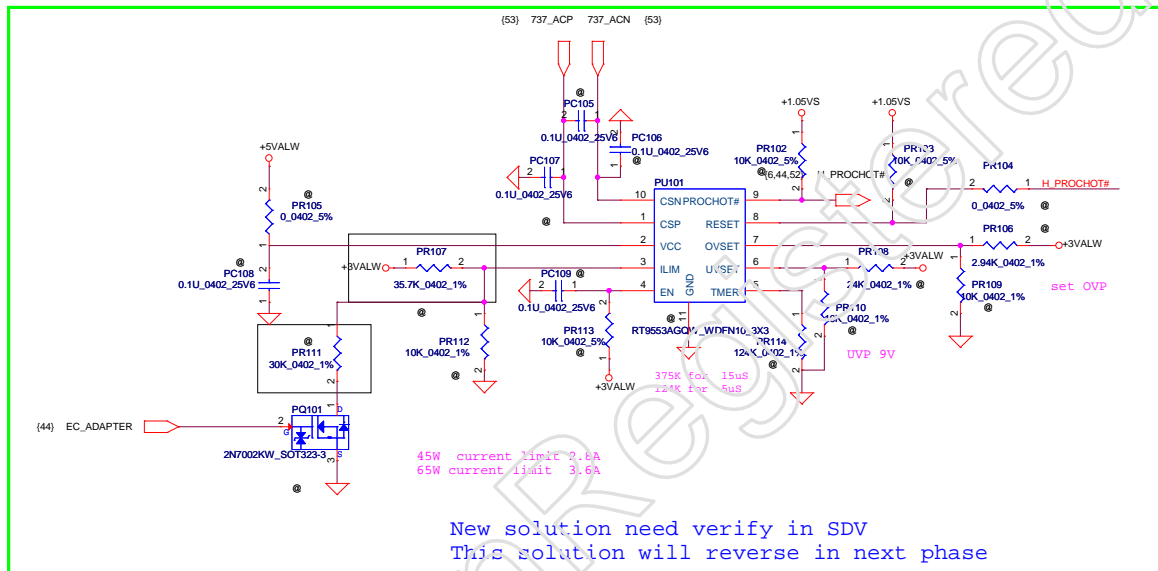
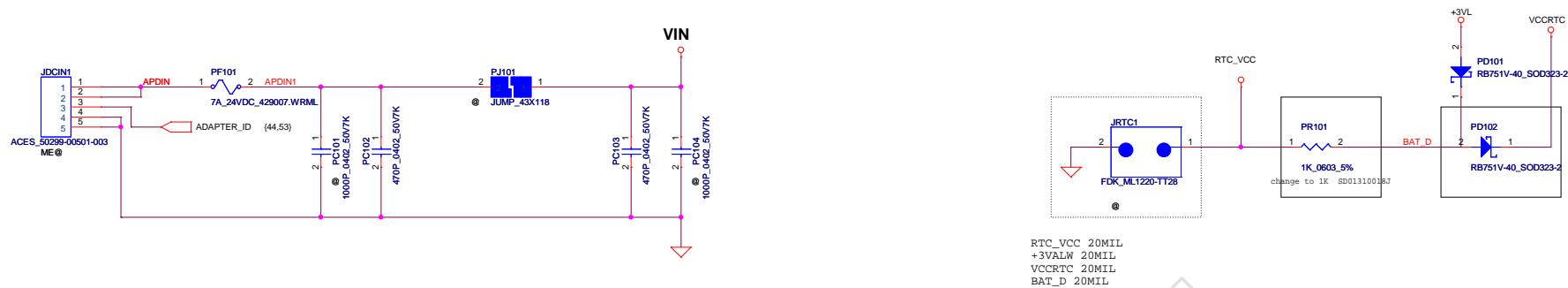
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| | | | | Date: | Monday, December 23, 2013 | Sheet 48 of 59 | |



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| Title | | Hole | |
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| Size B | Document Number | ACLU9 | |
| Date: | Monday, December 23, 2013 | Sheet | 49 of 59 |
| | | Rev | 0.2 |



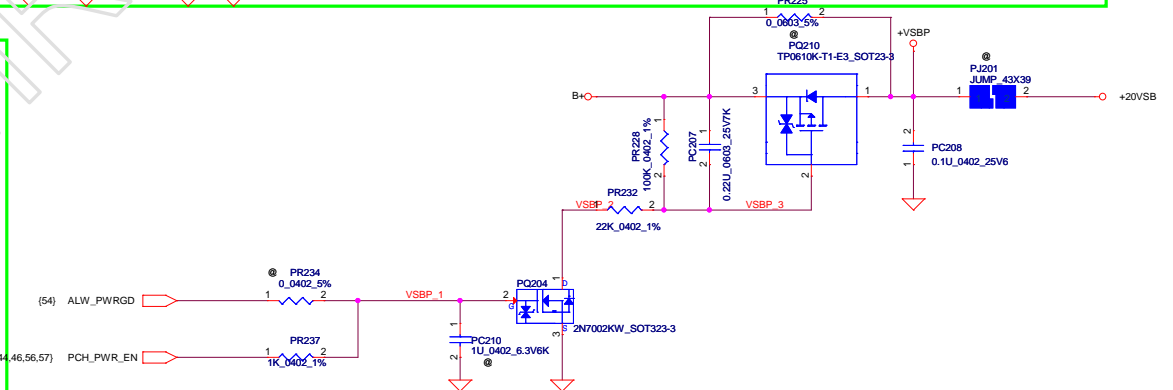
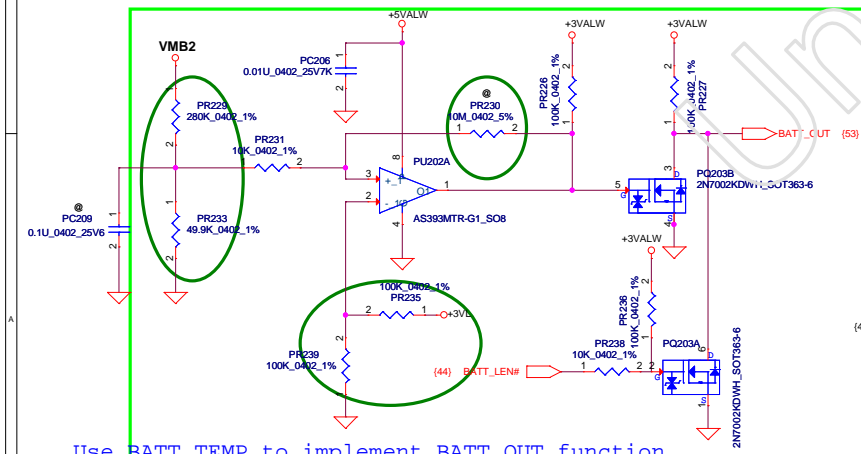
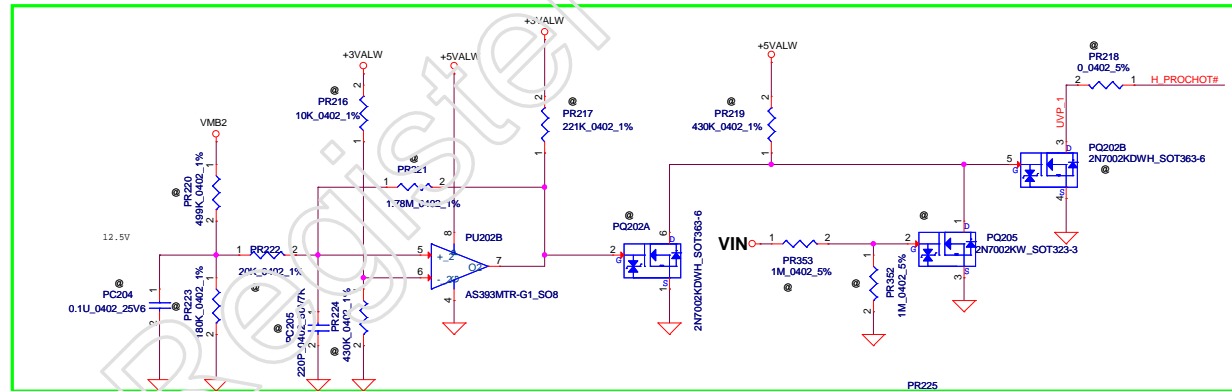
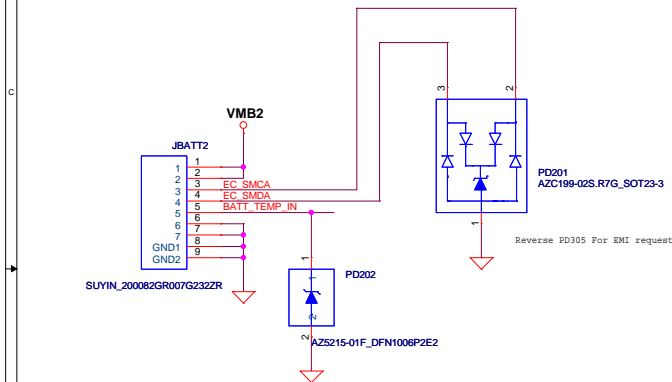
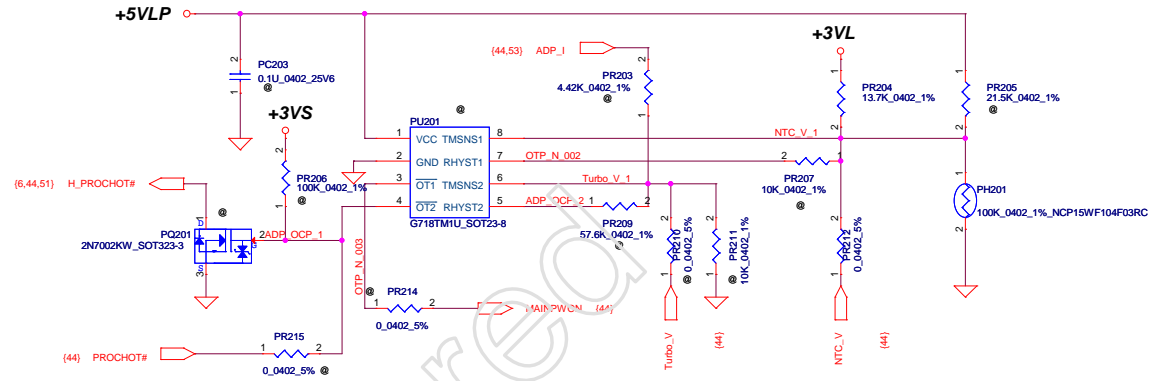
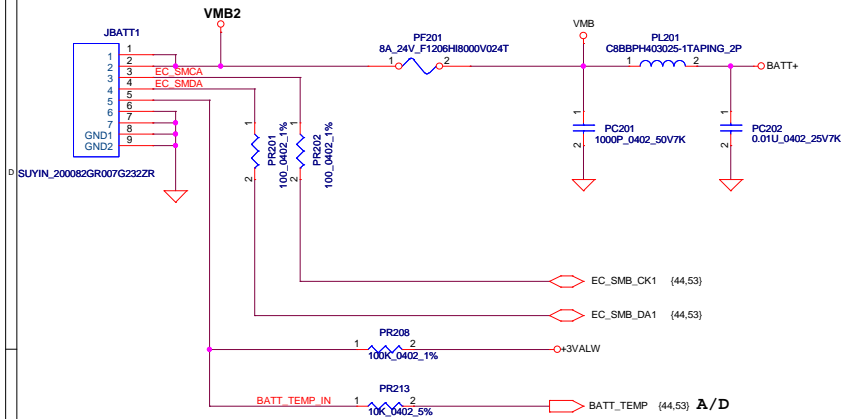


PH201 under CPU bottom side :
CPU thermal protection at 92+3 degree C
Recovery at 56 +3 degree C


For KB930 --> Keep PU1 circuit

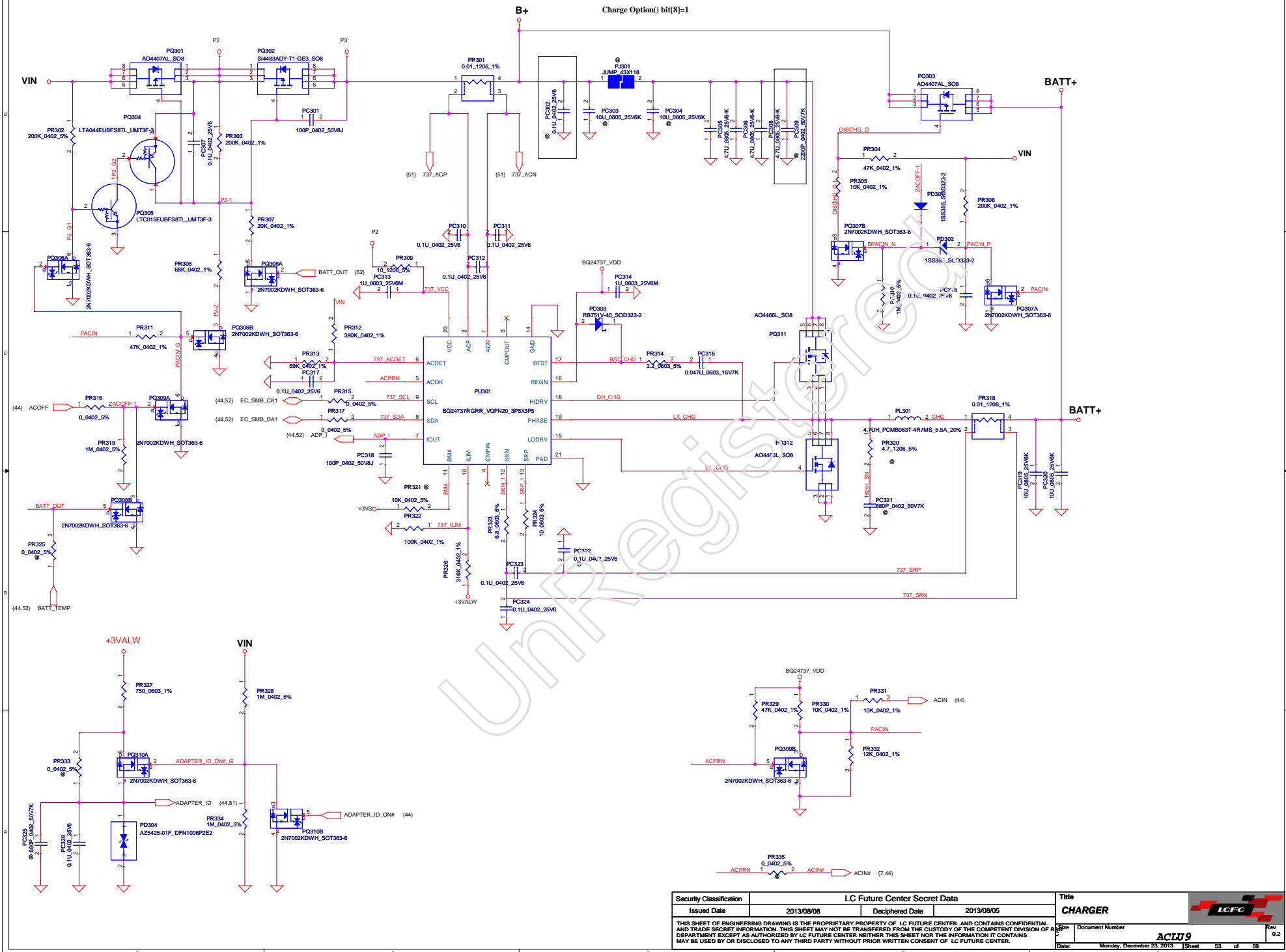
(Vth = 0.825V)

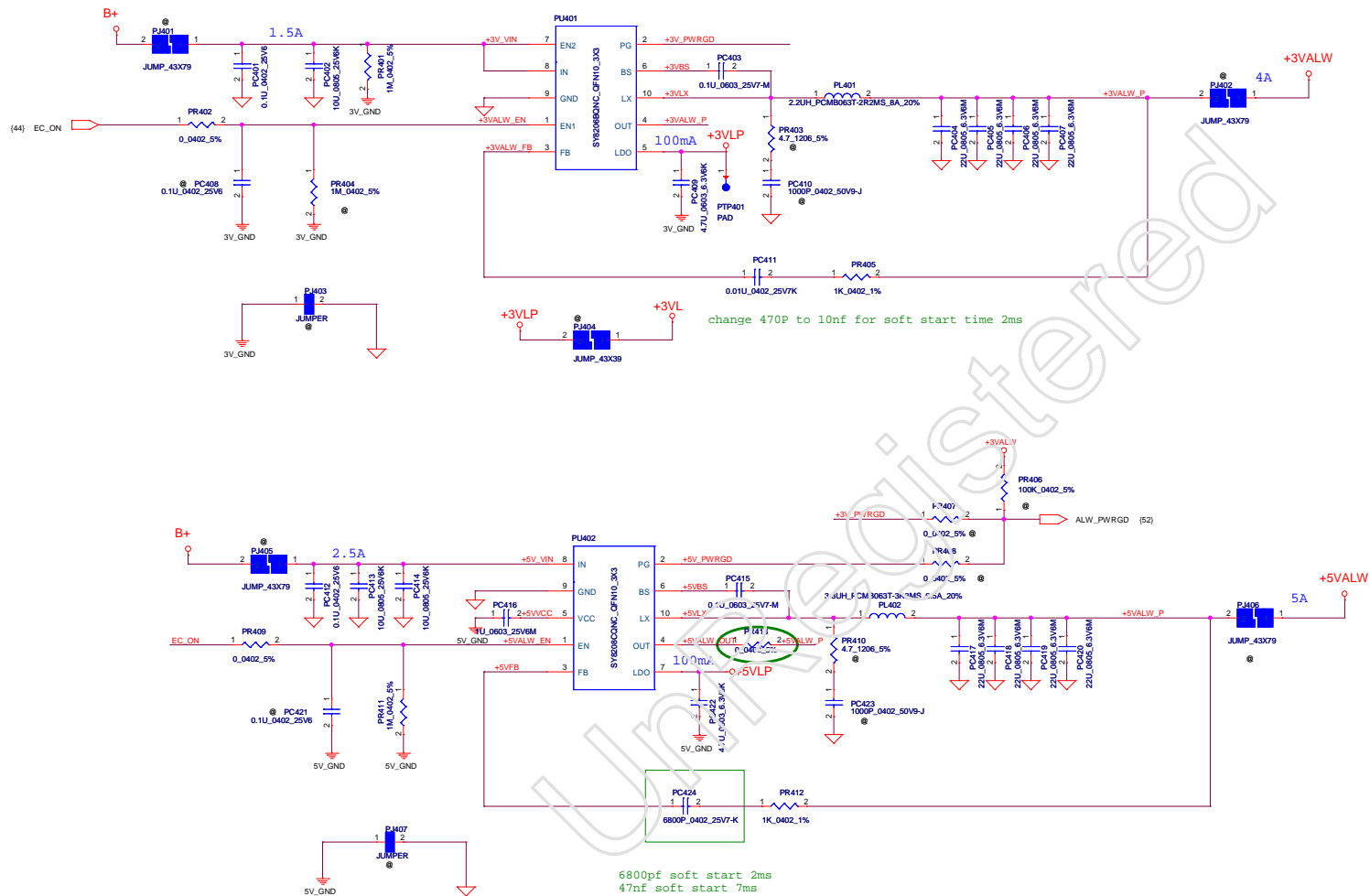
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212



Use BATT_TEMP to implement BATT_OUT function,
New solution need verify in SDV, maybe can reverse in next phase

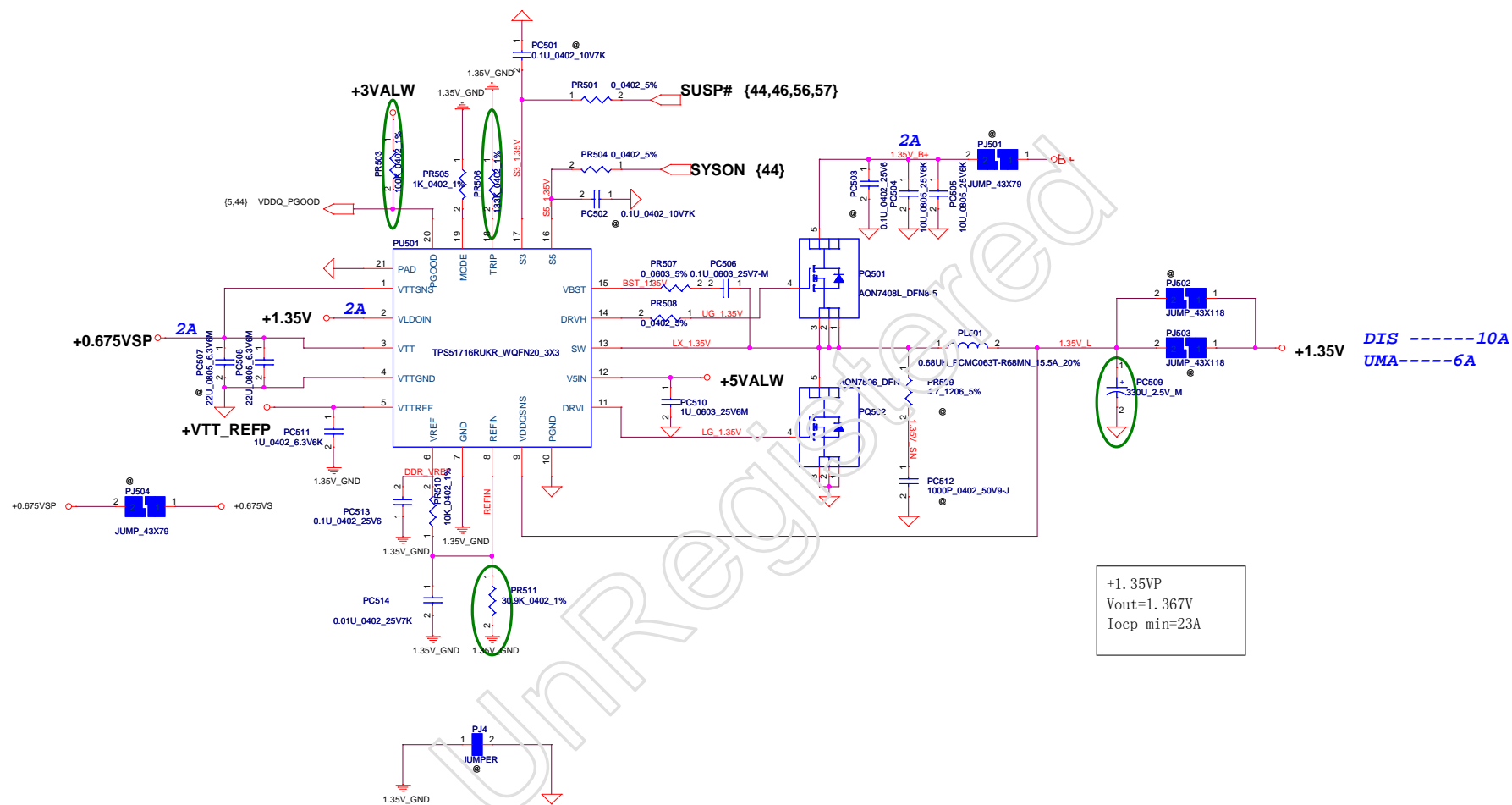
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| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 | BATTERY CONN/OTP | | | |
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| | | | | Custom | | 0.2 | |
| | | | | Date: | Monday, December 23, 2013 | Sheet | 52 of 59 |




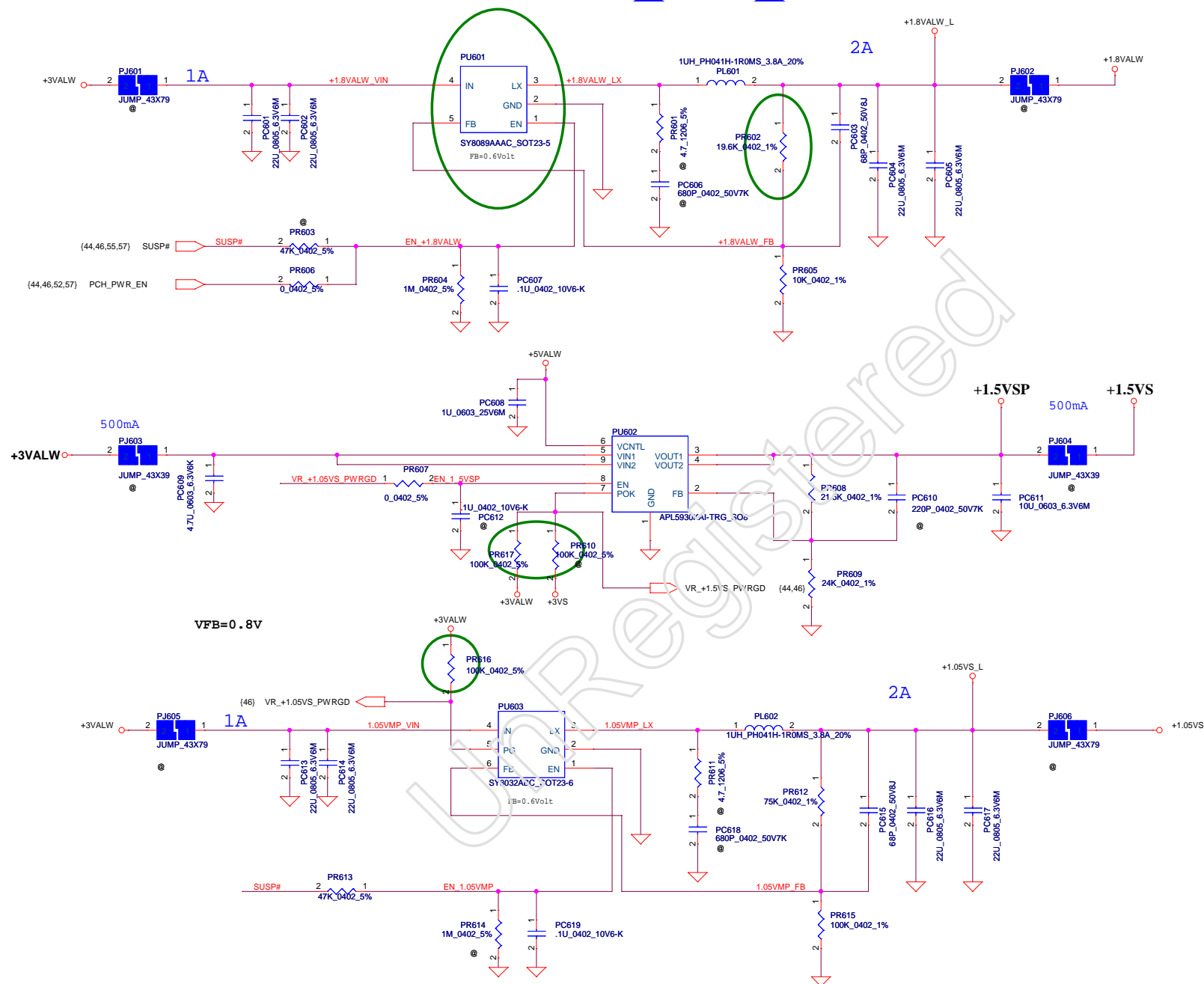


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| | | | Rev |


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| PWR_3VALW/5VALW | | LCFC | |
| Date | Monday, December 23, 2013 | Sheet | 54 of 59 |

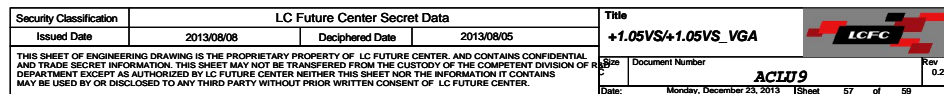


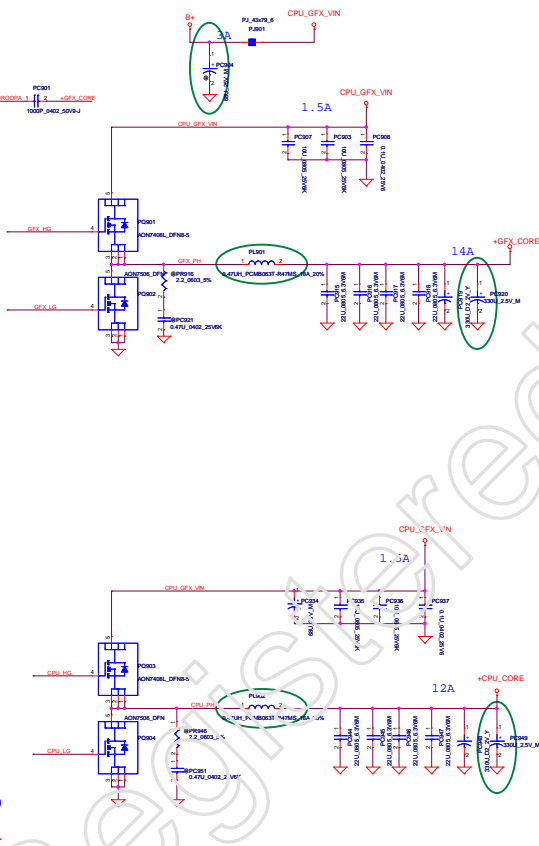
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| Size Custom | Document Number | | | ACLU9 | Rev 0. |
| Date: | Monday, December 23, 2013 | | | Sheet 55 of 59 | |



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| Title | |  | |
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| Size | Document Number | ACLU9 | |
| Custom | | | |
| Date: | Monday, December 23, 2013 | Sheet | 56 of 59 |
| | | | Rev 0. |





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| Issued Date | 2012/09/03 | Declassified Date | 2012/09/03 | PWR_CPU_CORE/GFX_CORE LCFC | |
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