



PCB
Part Number = DAZ0J200100

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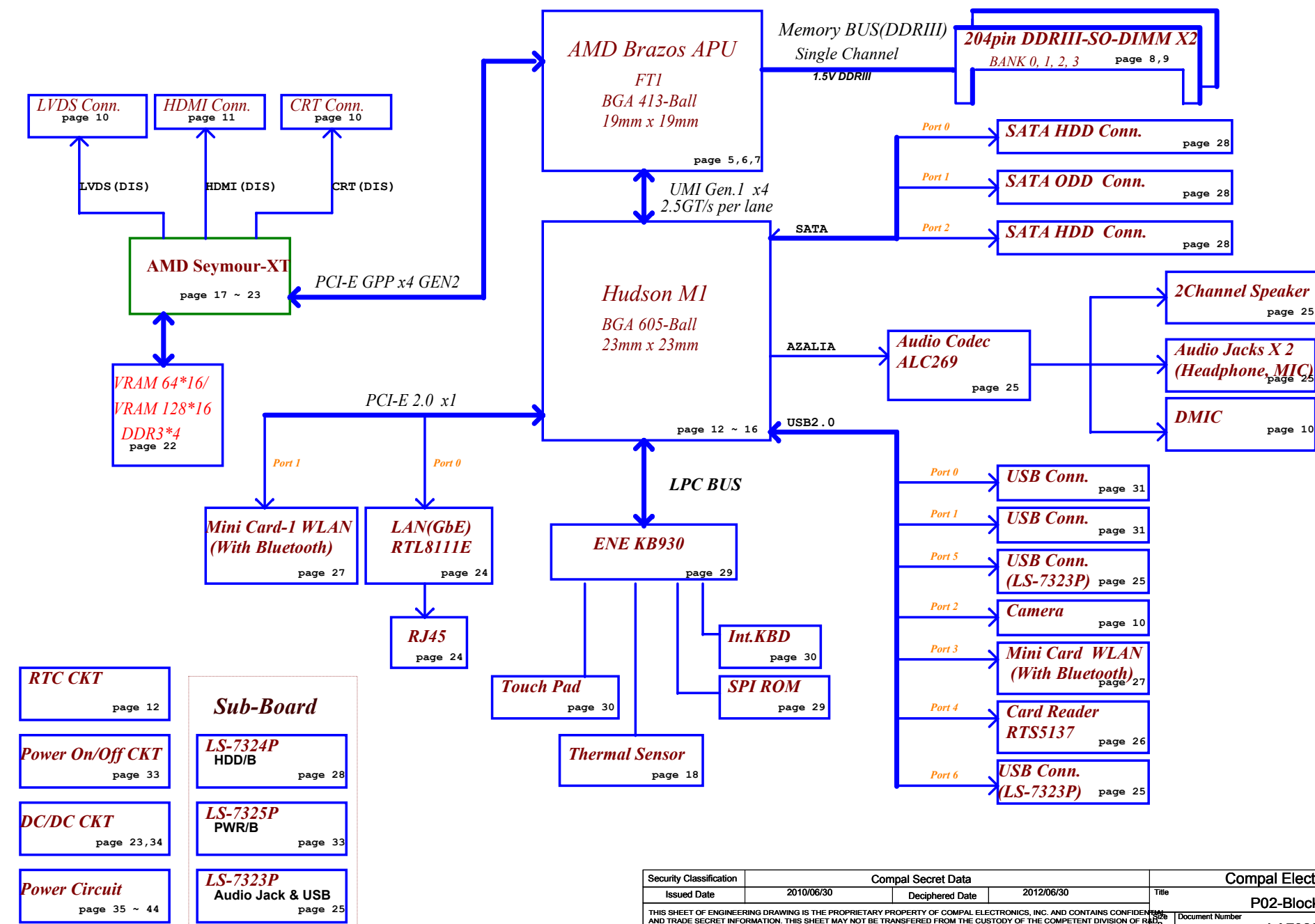
K73 Schematics Document

AMD APU Zacate-FT1 + FCH Hudson-M1 + GPU Seymour XT-M2

2010-02-22

REV: 0.22

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SMBUS Control Table

	SOURCE	MIINI1	BATT	APU	FCH	SODIMM	VRAM
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	V	X	V
FCH_SMCLK0 FCH_SMDAT0	PCH	V	X	X	X	V	X
FCH_SMCLK3 FCH_SMDAT3	PCH	X	X	V	X	X	X

BOM Structure

15@ : E240 1.5GHz
16@ :E350 1.6GHz
X76@ : VRAM second source
LS@ : Level Shift
NLS@ :non Level Shift
USB30@ :USB3.0

FCH Hudson-M1

USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	JUSB1
Port1	JUSB2
Port2	Camera
Port3	JMINI (WLAN)
Port4	Card Reader
Port5	JUSB3
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

PCIE Port List

APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

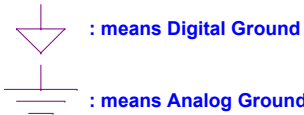
FCH Hudson-M1

SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

SCL0, SDA0 (Primary SMBUS in the S0 domain)
SCL1, SDA1 (Secondary SMBUS supporting ASF)
SCL2, SDA2 (Primary SMBUS in the S5 domain)
SCL3, SDA3 (Primary low-voltage SBMBUS for Processor TSI)
SCL4, SDA4 (Primary SMBUS in the S5 domain)

Symbol Note :



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Power-Up/Down Sequence

1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
2. VDDR3 should ramp-up before or simultaneously with VDDC.
3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.
4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.
5. VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)

VDDR3(3.3VSG)

PCIE_VDDC(1.0V)

VDDR1(1.5VSG)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset

Note: Do not drive any IOs before VDDR3 is ramped up.

T4+16clock

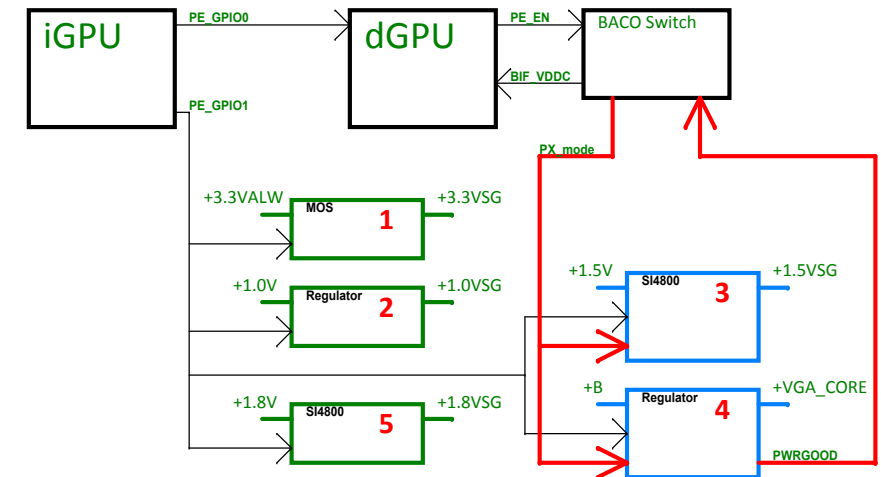
Wincc7.0 v7.0.0.0

PE_GPIO0 : Low -> Reset dGPU ; High -> Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High -> Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A

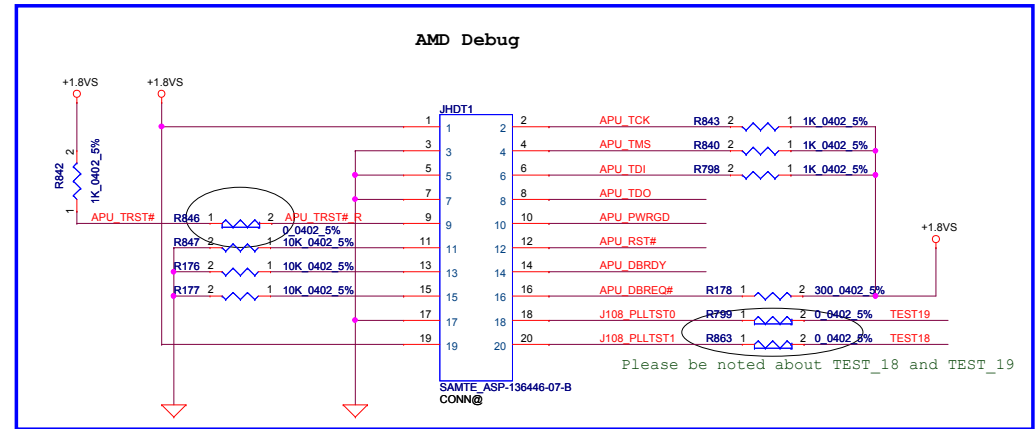
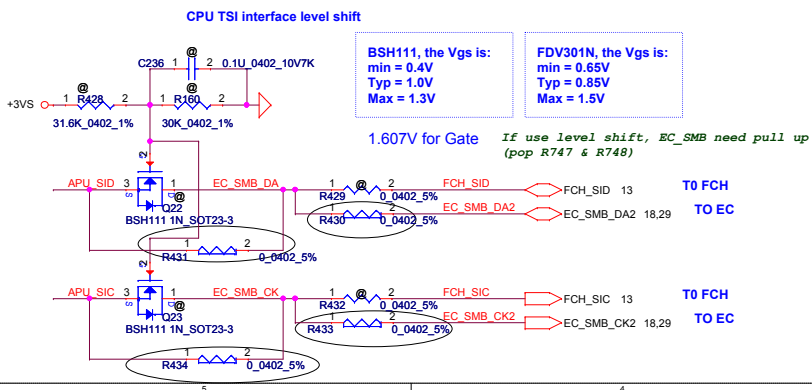
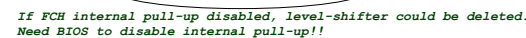
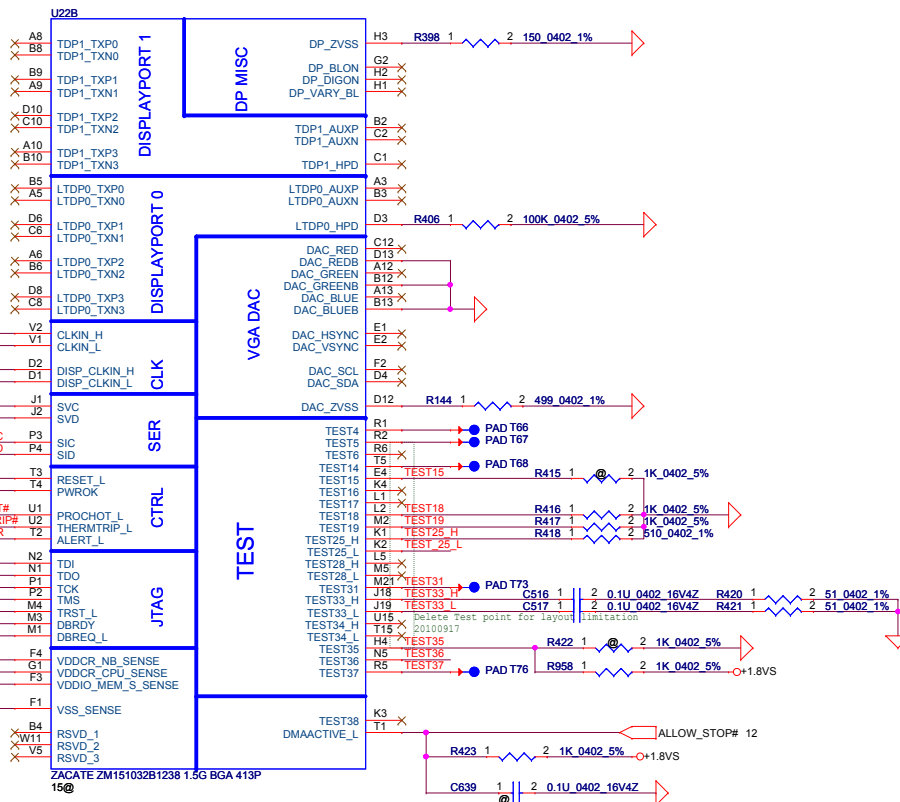
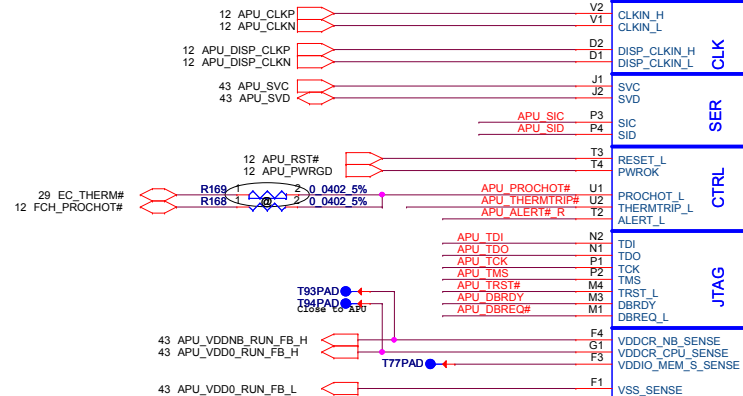


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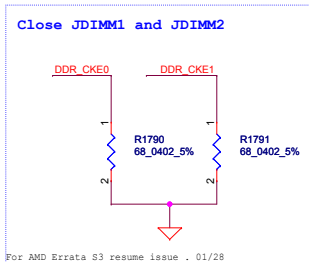
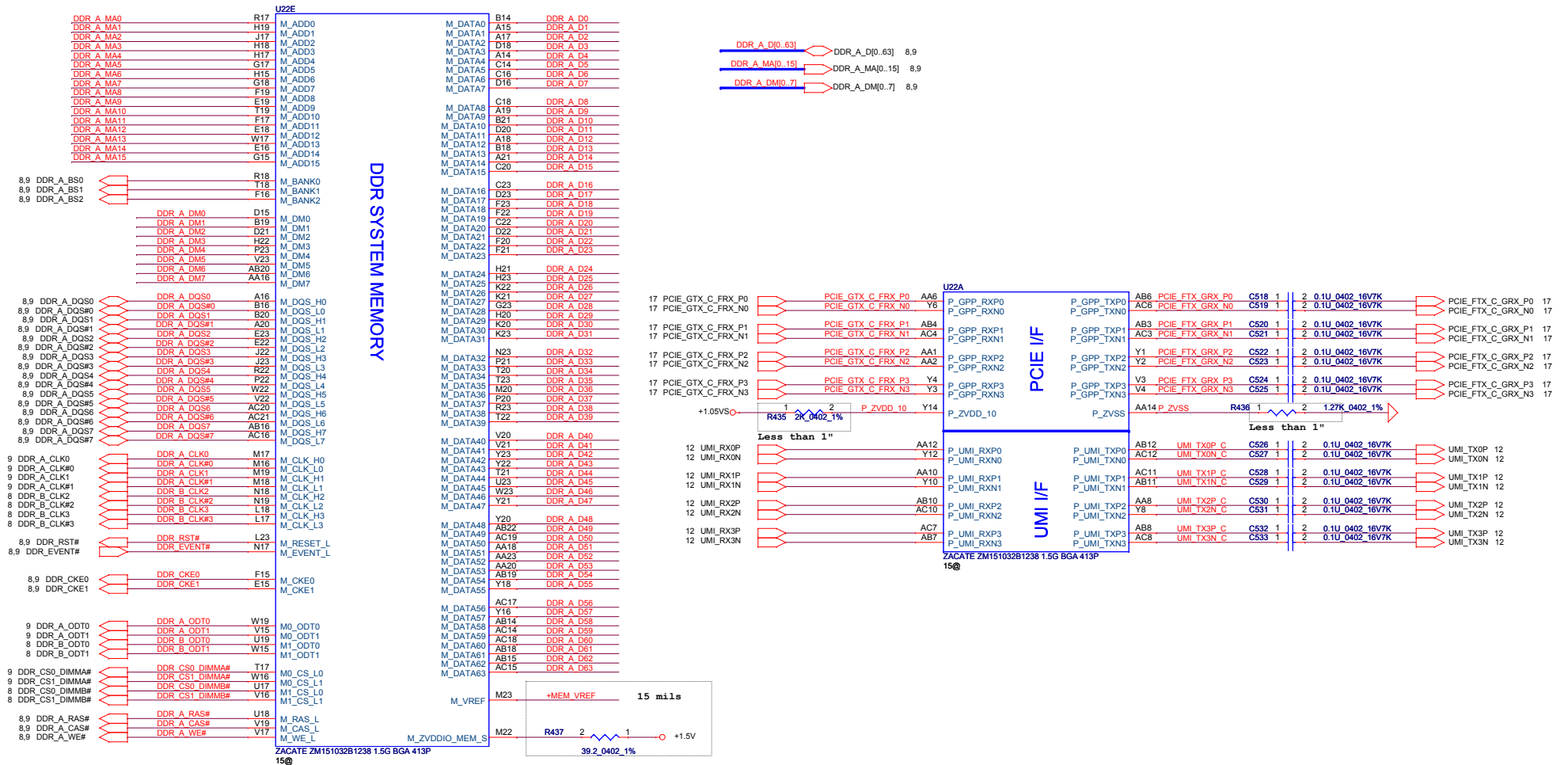
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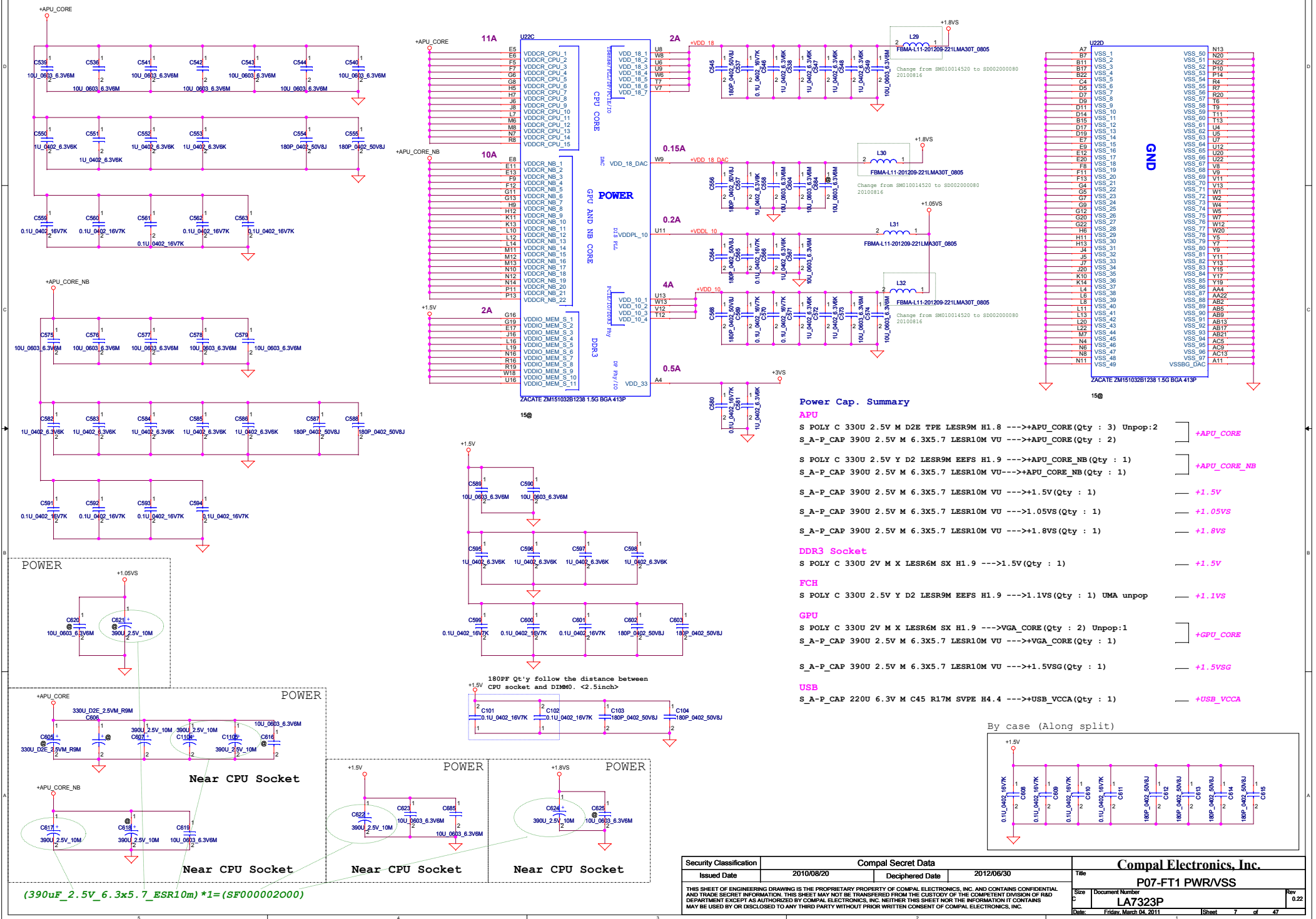
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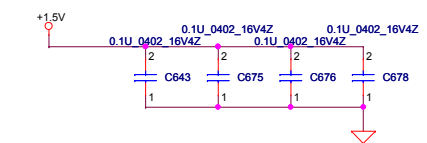


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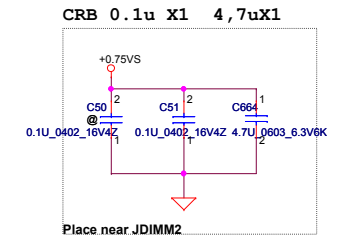
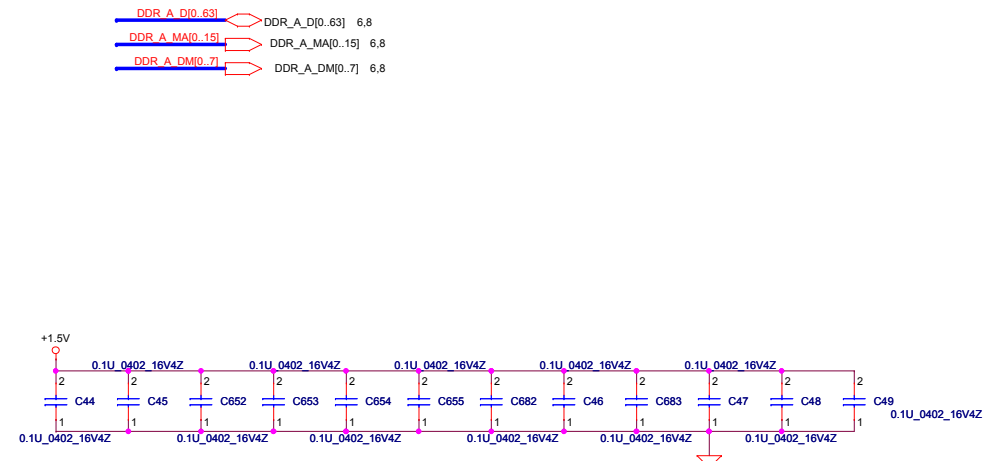
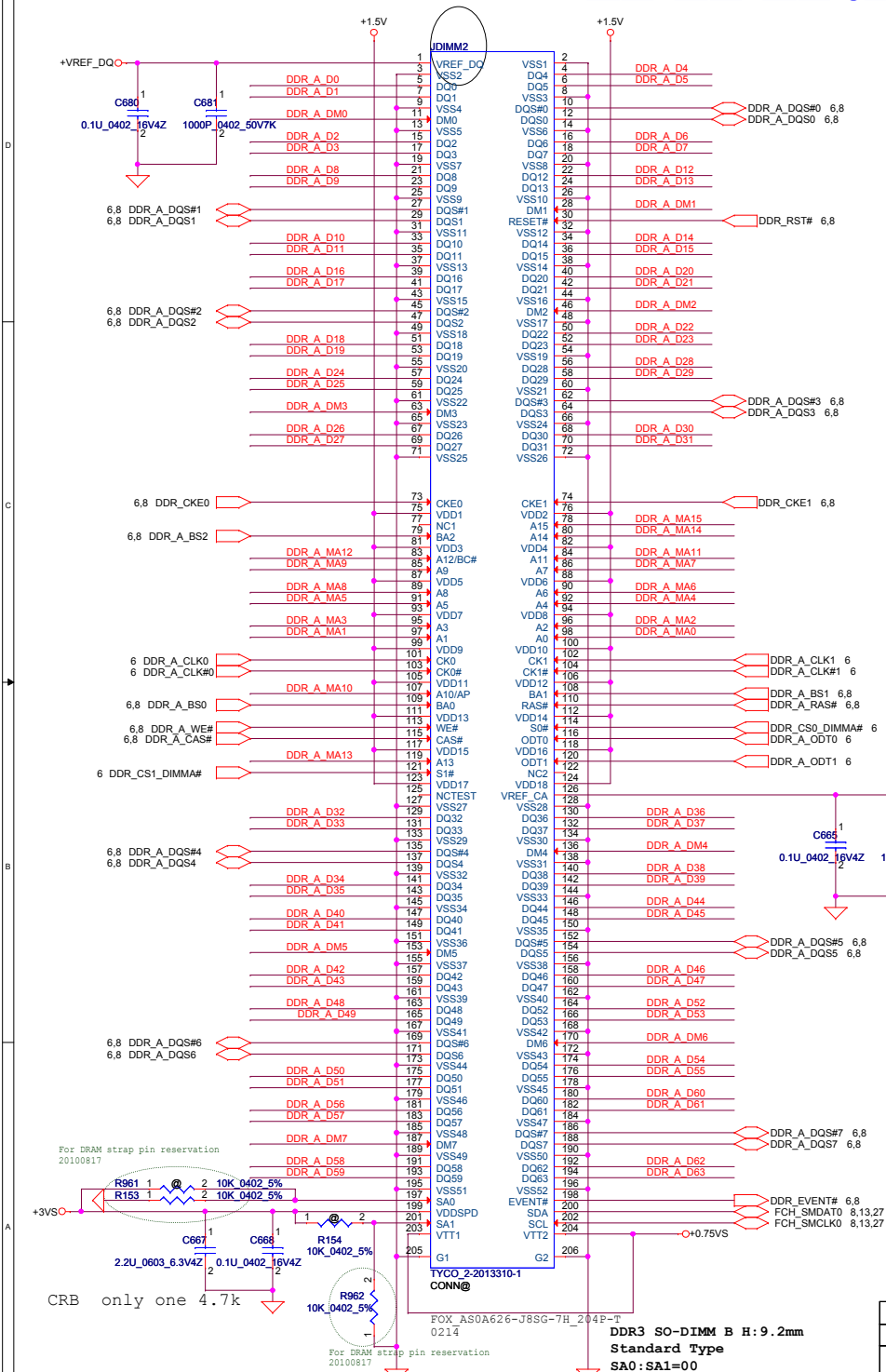


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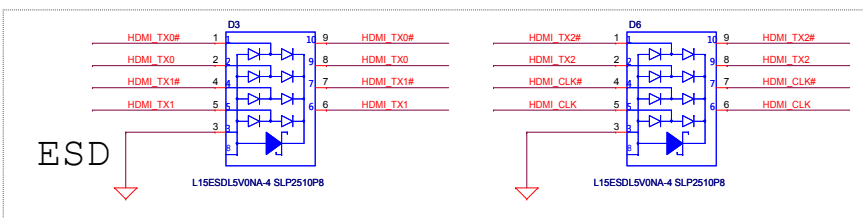
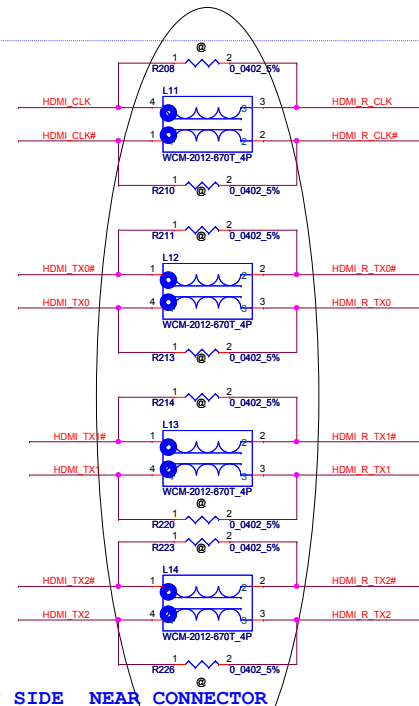
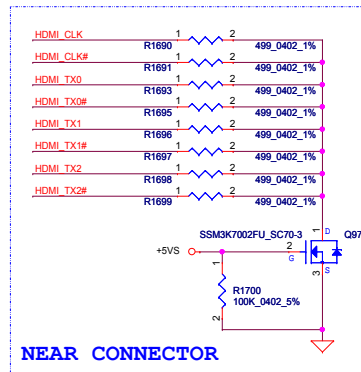
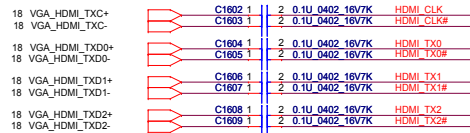
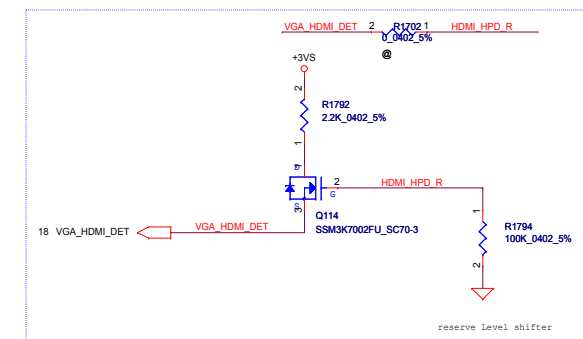
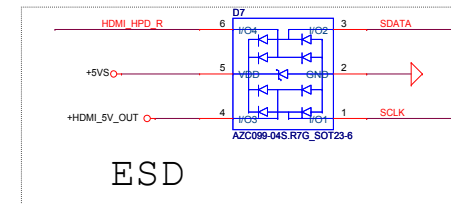
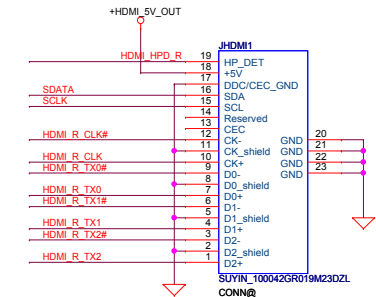
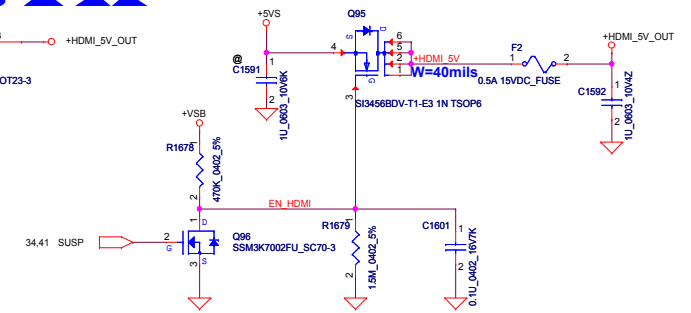




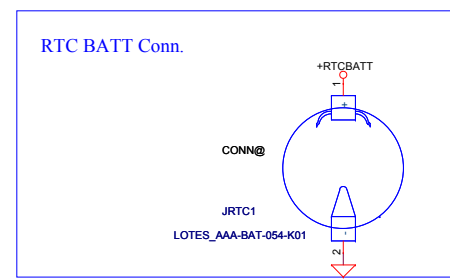
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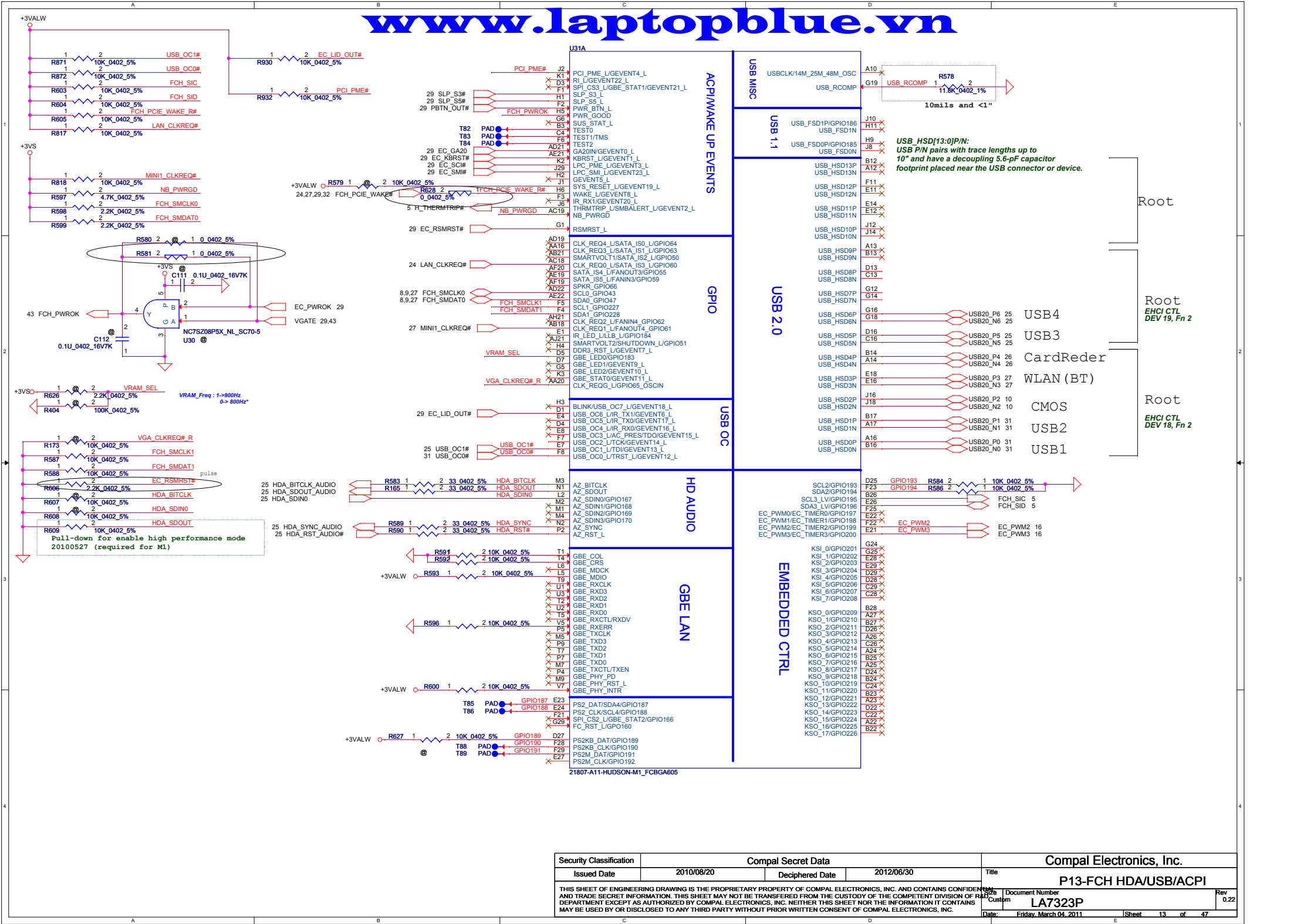
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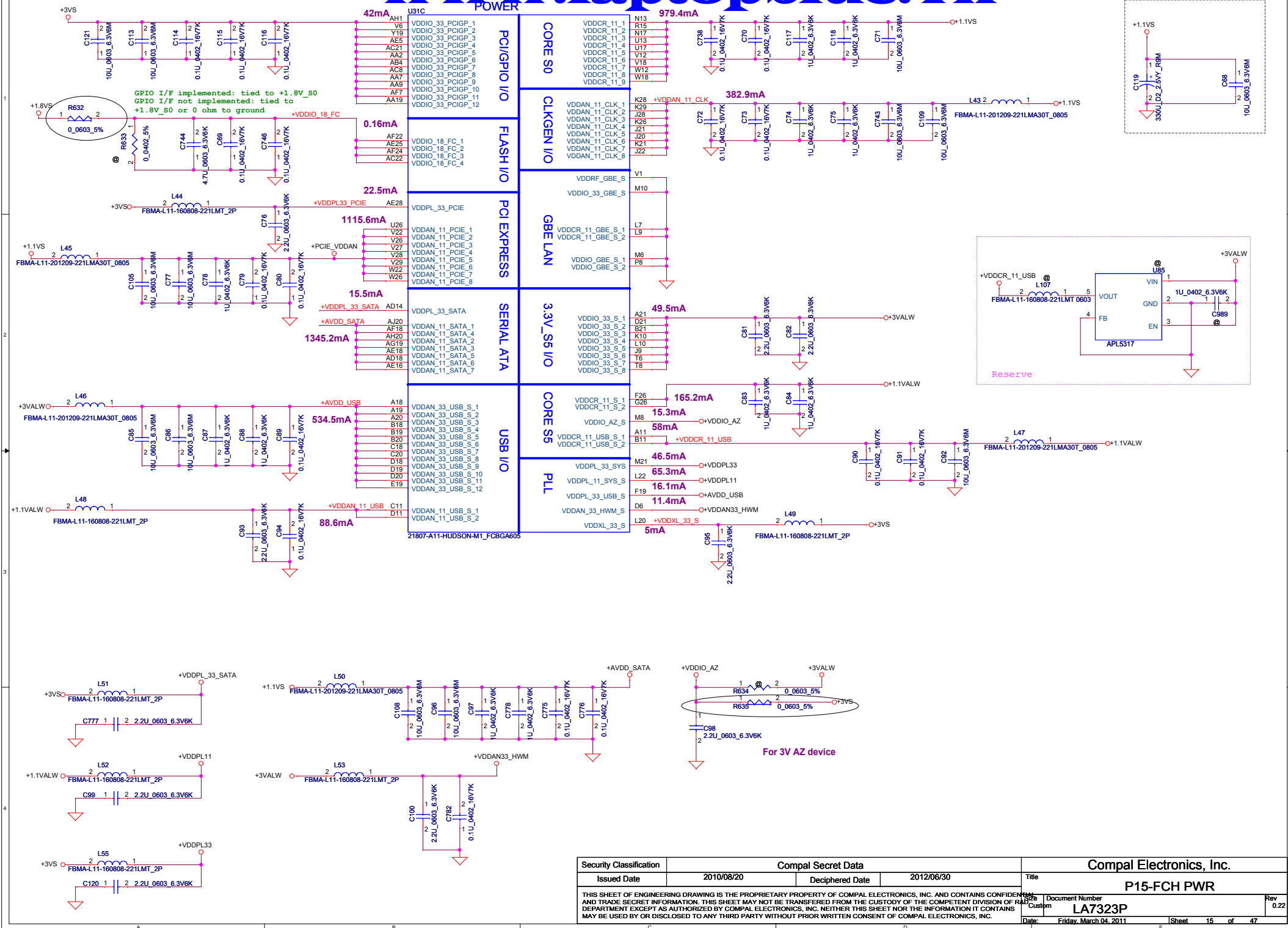


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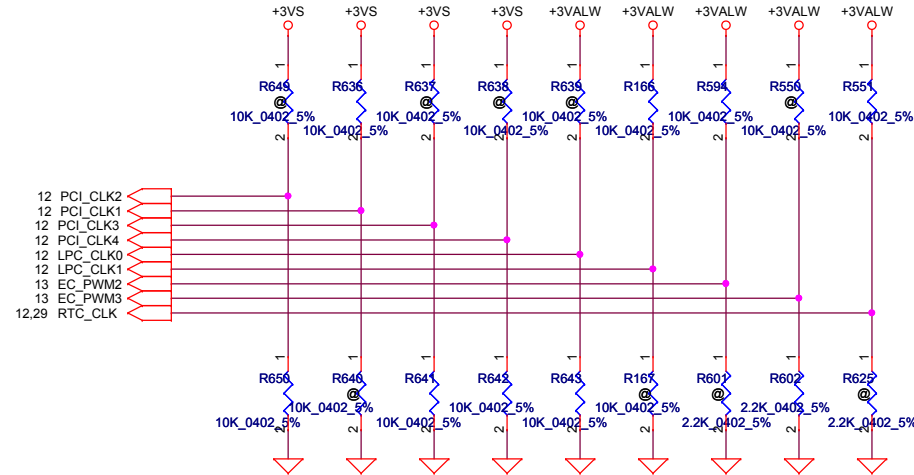
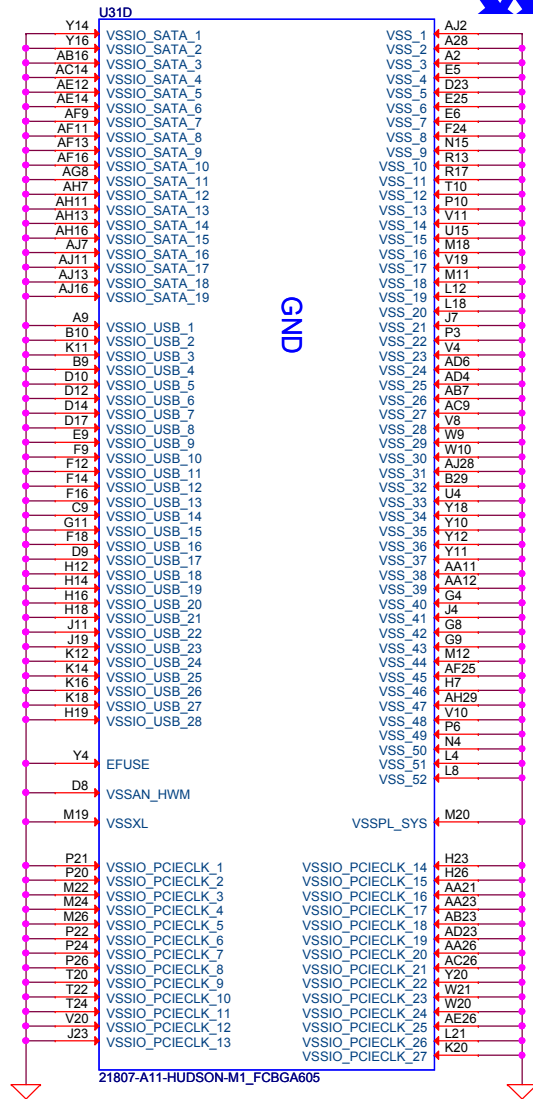
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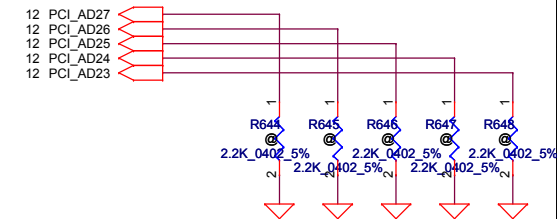
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PULL HIGH	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H,L) *
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK Mode DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode	S5 PLUS MODE ENABLED	SPI ROM(L,H)



DEBUG STRAPS

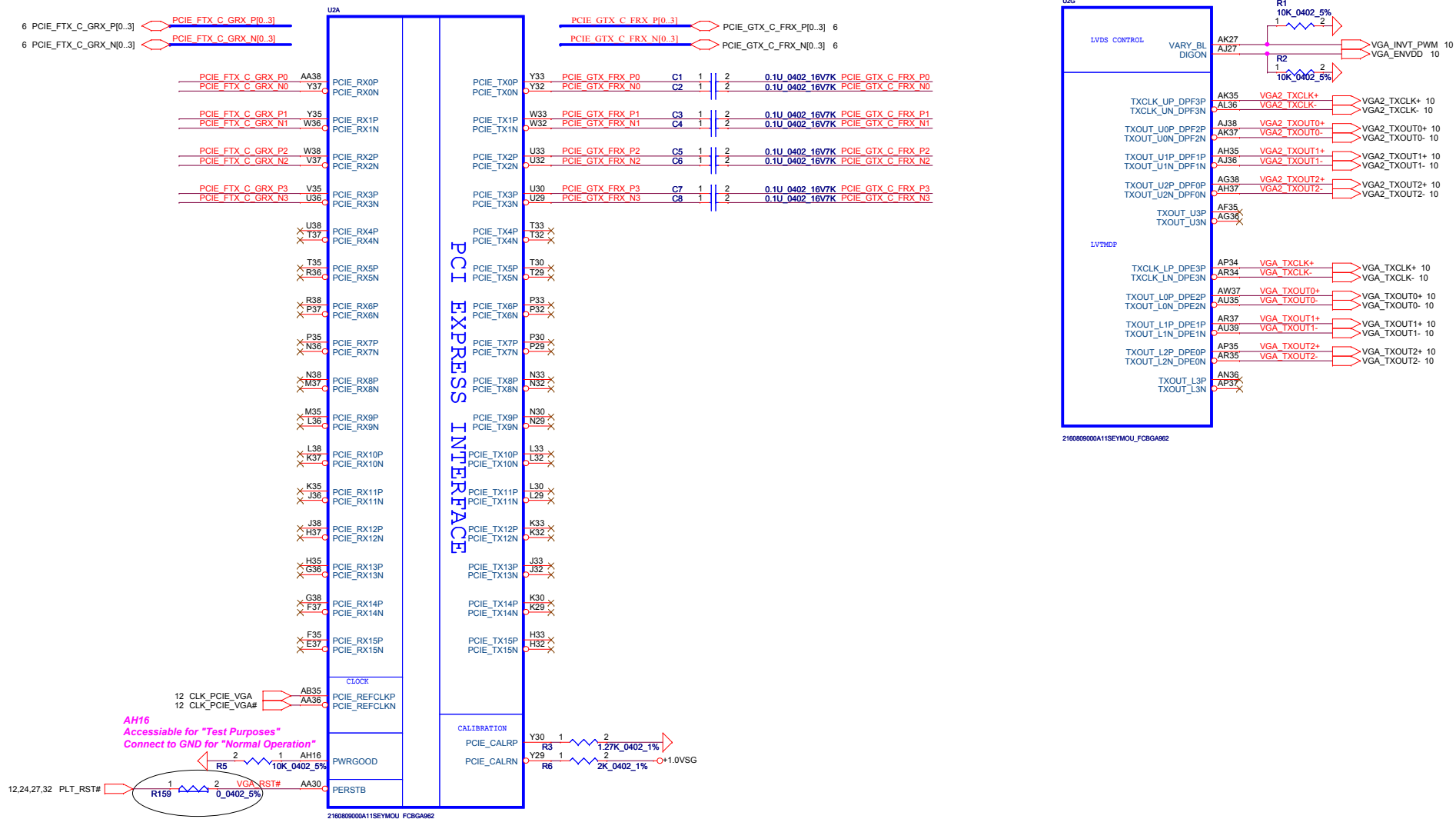
FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved



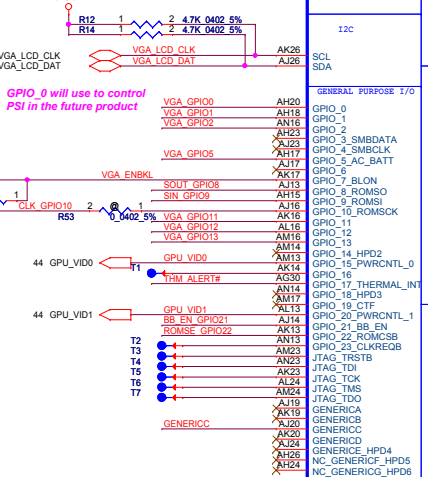
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GFX PCIE LANE REVERSAL

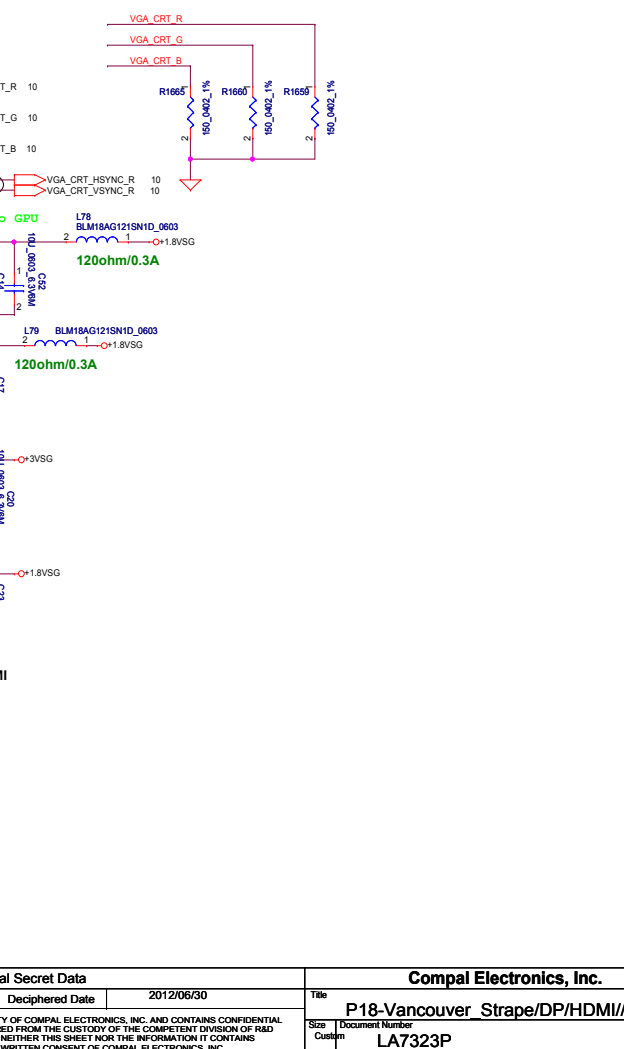
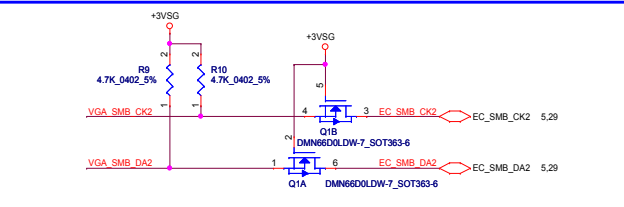
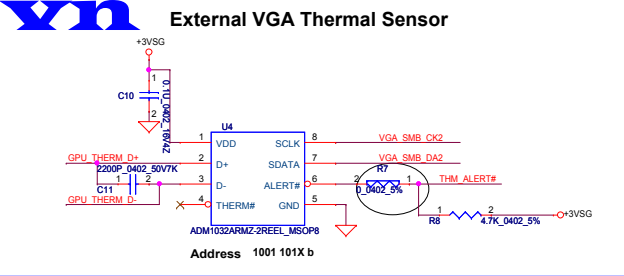
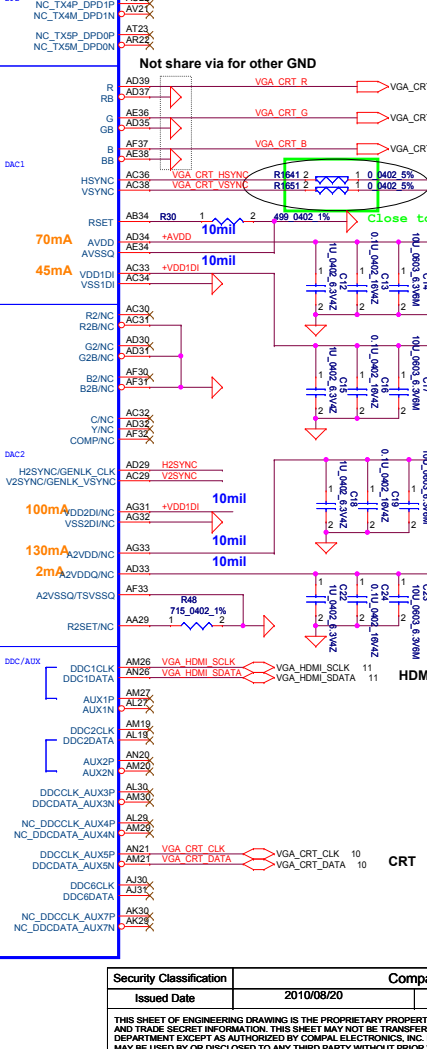
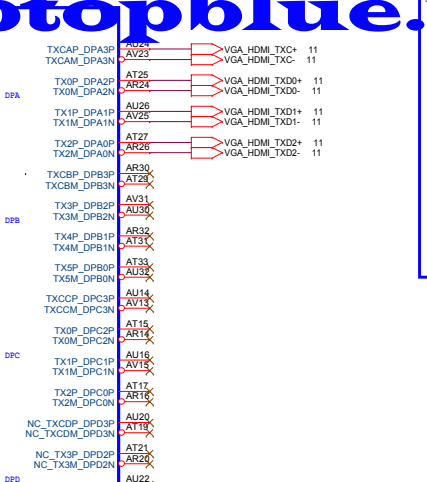
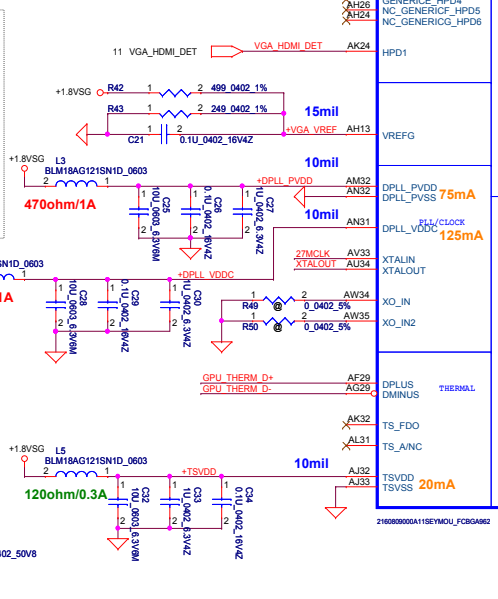
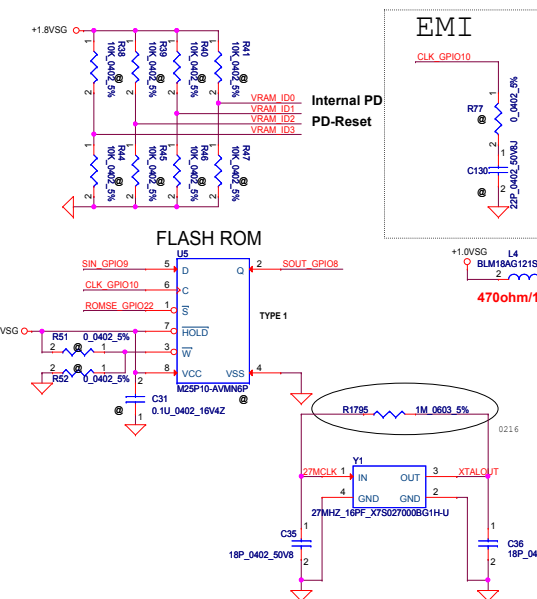


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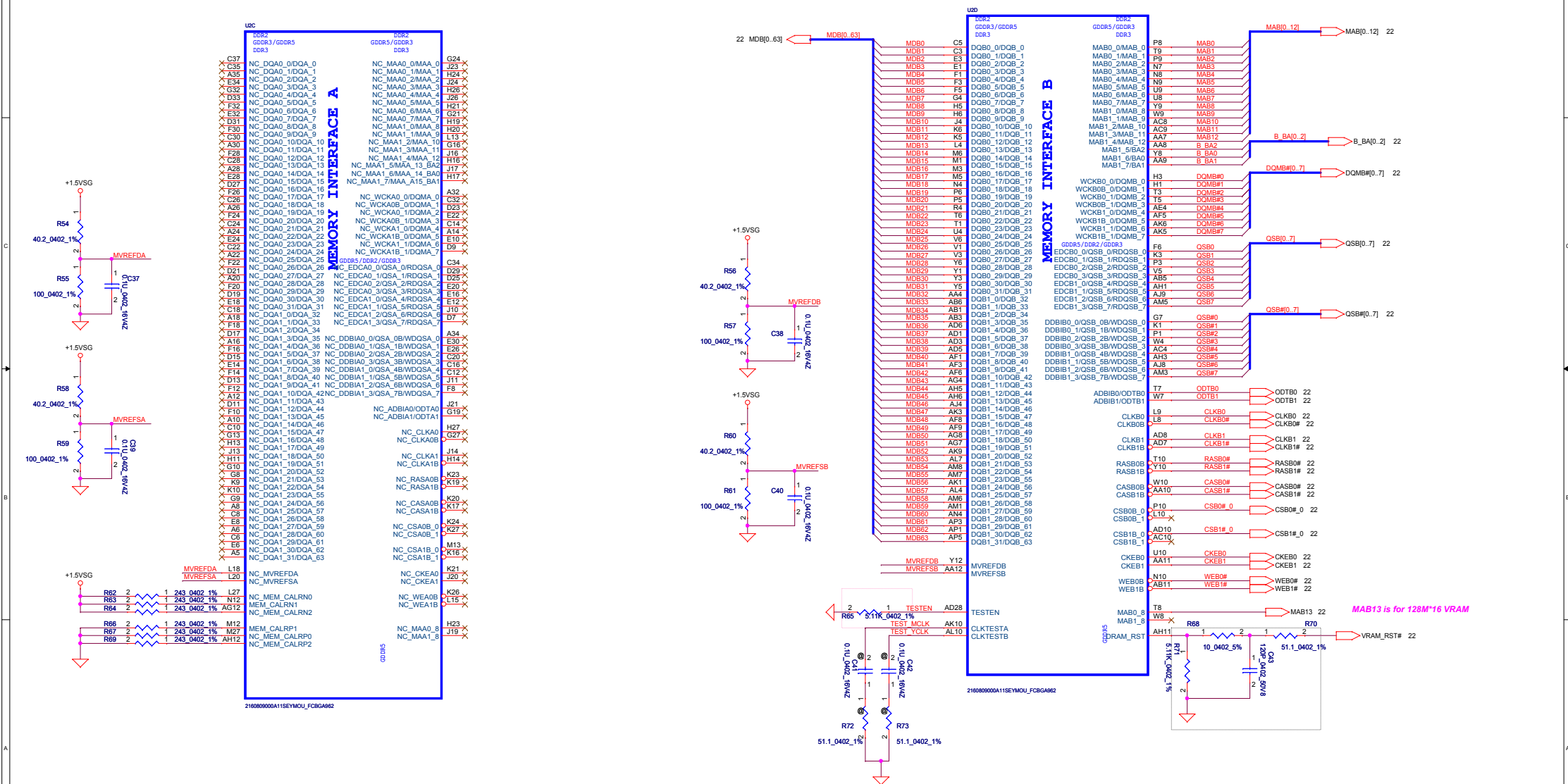
Strap Name		Pin Straps description <all internal PD>	Setting
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13, 12, 11 (config 2, 1, 0): a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	memory apertures - CONFIG[3]: 128 MB 000 256 MB 001 * 64 MB 010
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCIe device as 2.5 GT/s capable at power-on 1= Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENCLK_CLK) GPIO8 GPIO21 GENERRCC GPIO5	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI



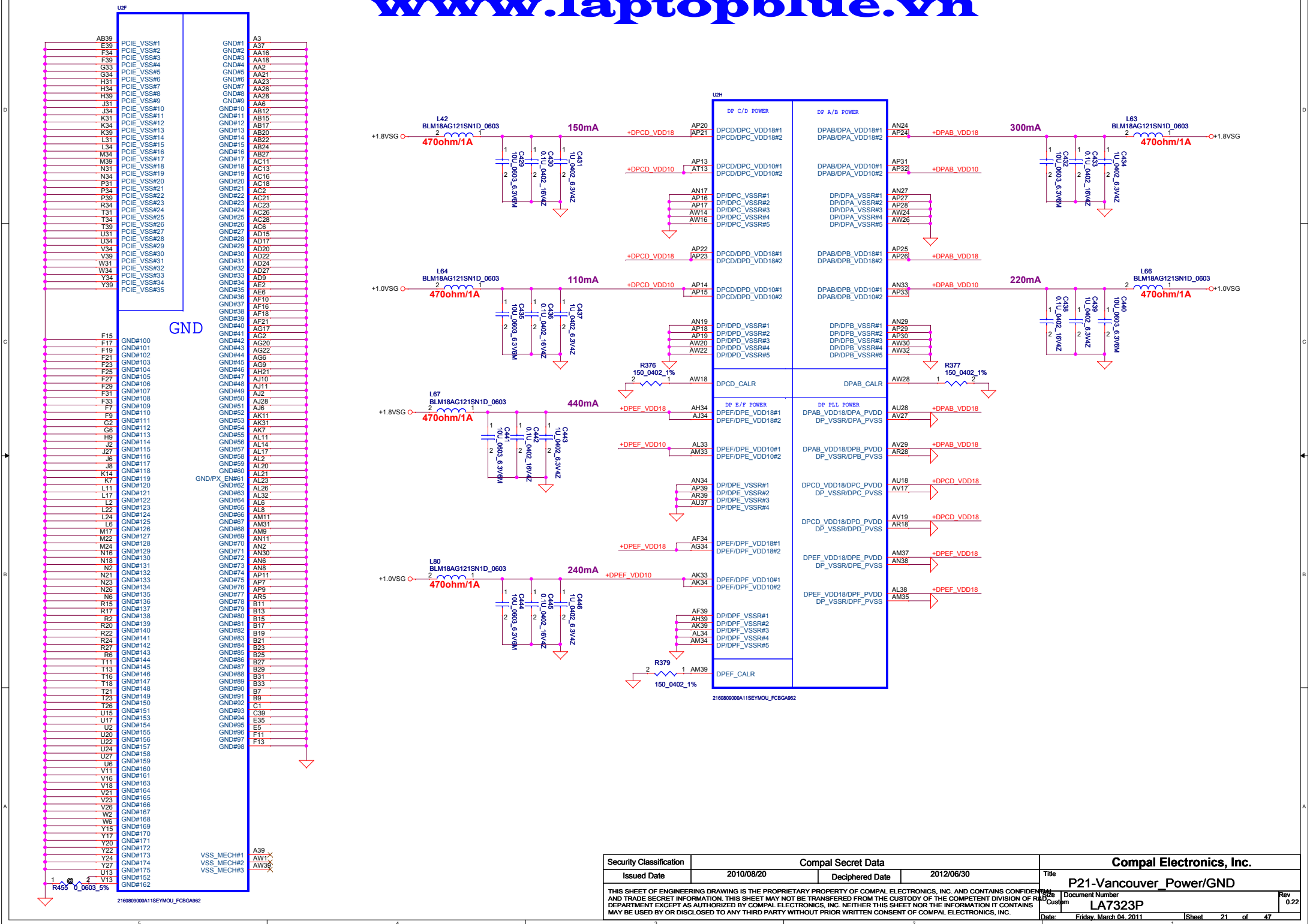
Seymour(XT)					
VRAM	Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung					
SA00004G830	64M16	0	0	0	0
K4W1G16466G-BC11					
Samsung					
SA000047A00	128M16	0	0	0	1
K4W2G16466C-HC11					
Hynix					
SA000041S60	64M16	0	1	0	0
H5TQ16638FR-11C					
Hynix					
SA00003Y330	128M16	0	1	0	1
H5TQ26638FR-11C					



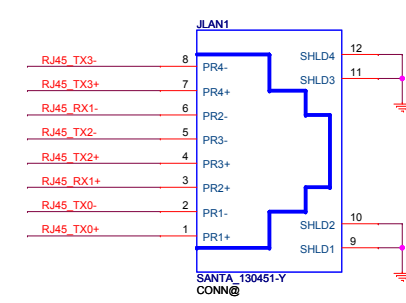
Robson, Seymour only support single channel memory (channel B only)



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				Date Friday, March 04, 2011	Rev 0.22



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				Customer	0.22	
				Date	Sheet	
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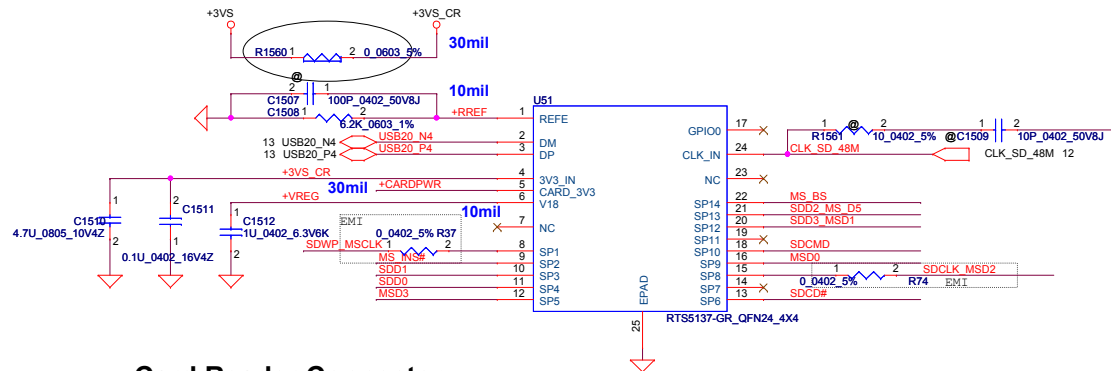


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				Document Number LA7323P	0.22
Date:	Enforce March 04, 2011	Sheet	24	of	47

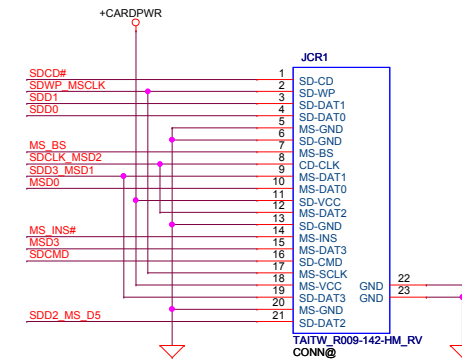
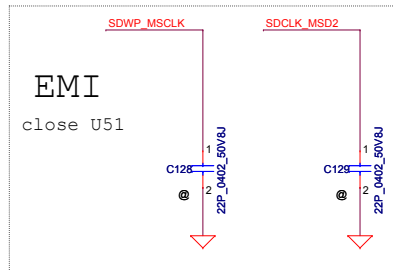
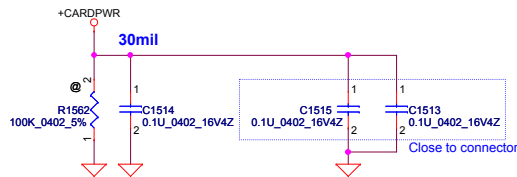


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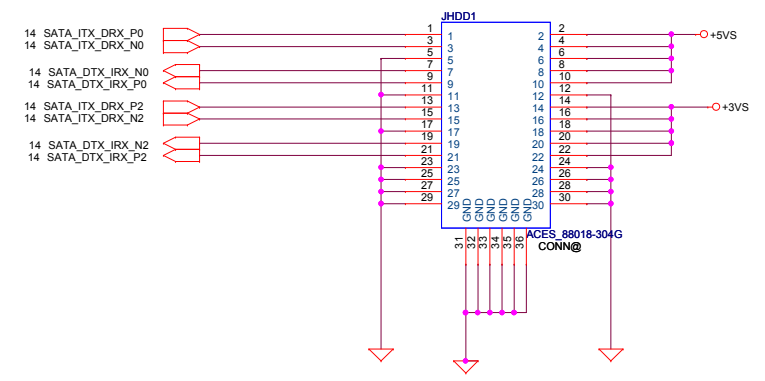
Card Reader RTS5137 (only SD/MMC/MS function)



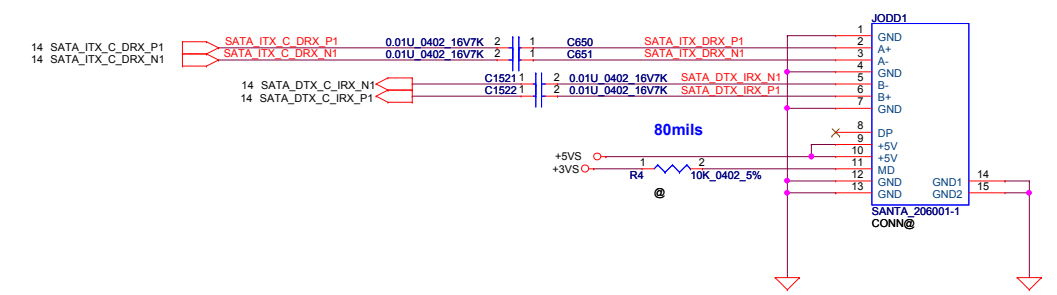
Card Reader Connector

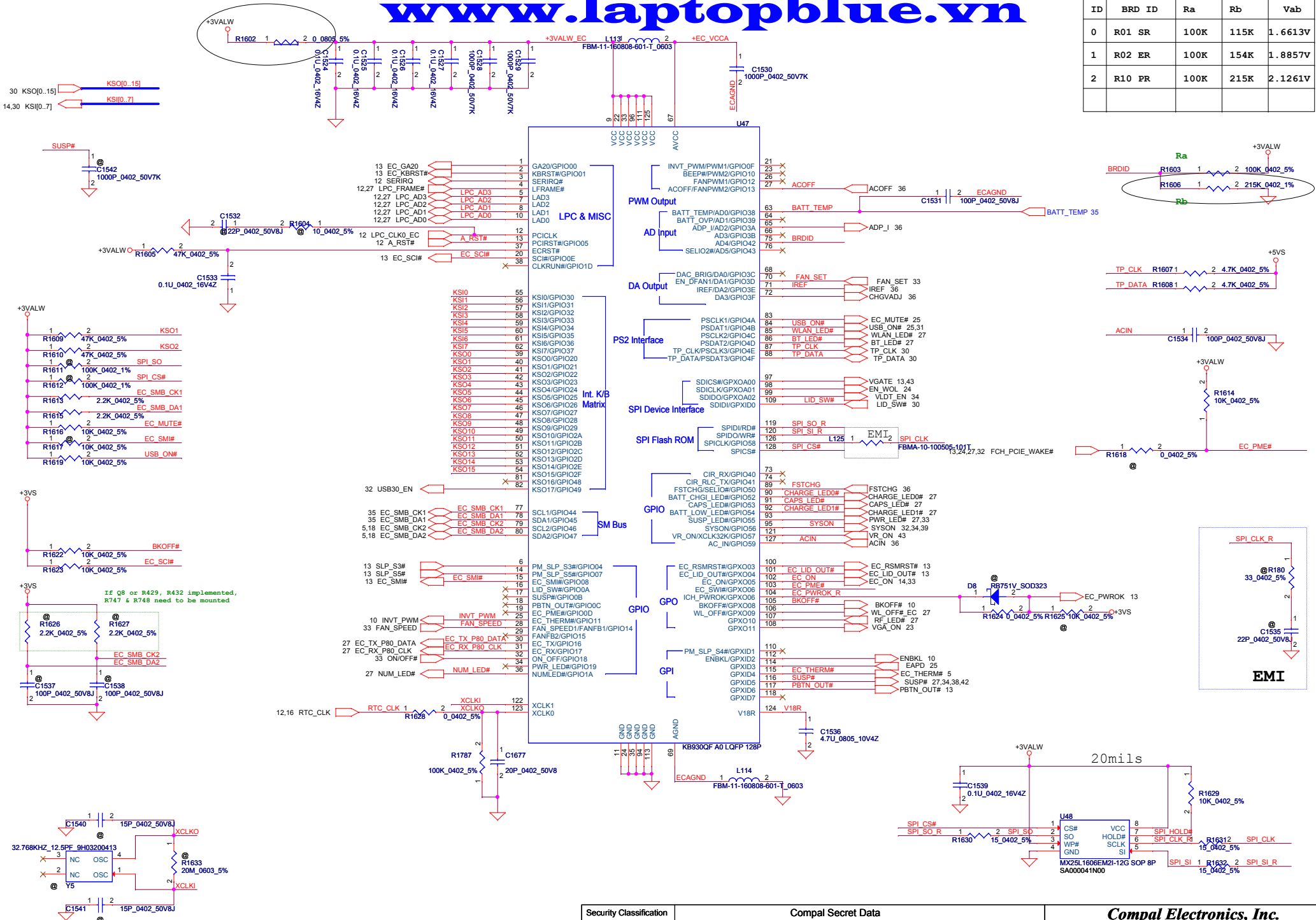


SATA HDD BTB Conn.

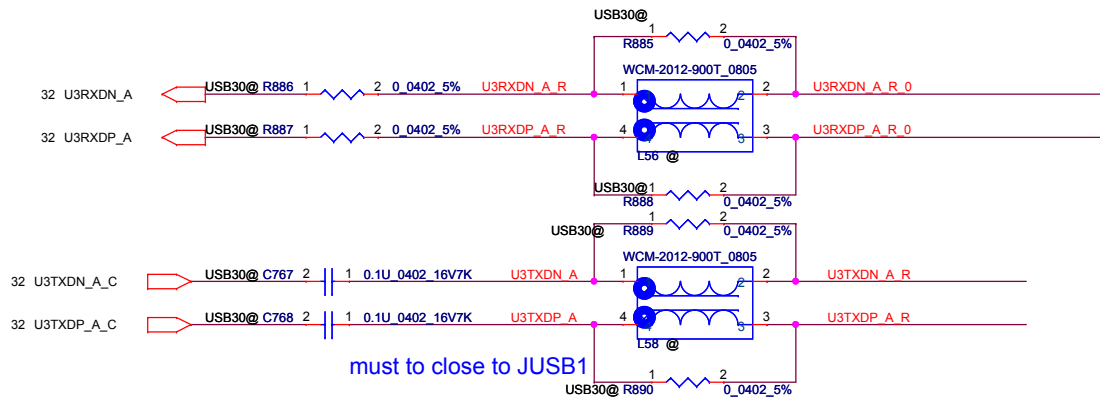
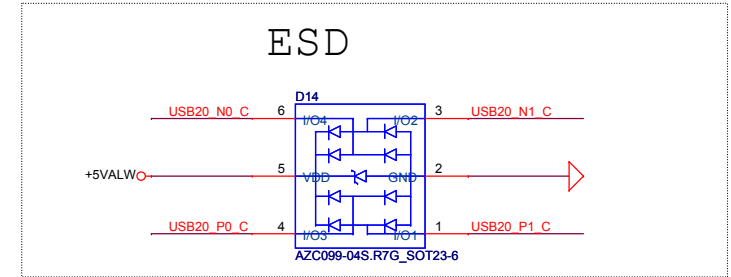
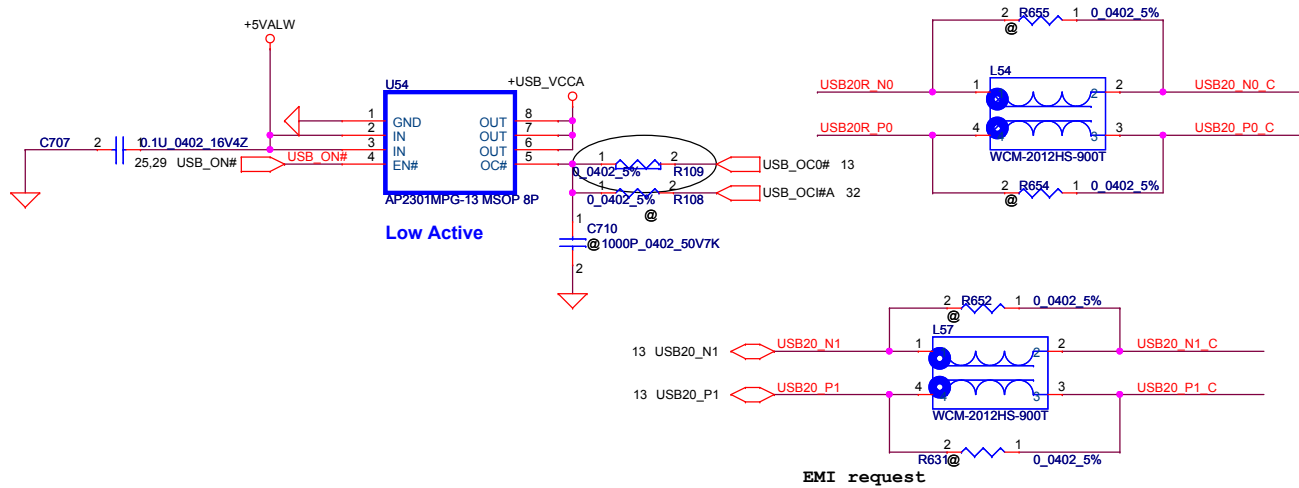


SATA ODD FFC Conn.

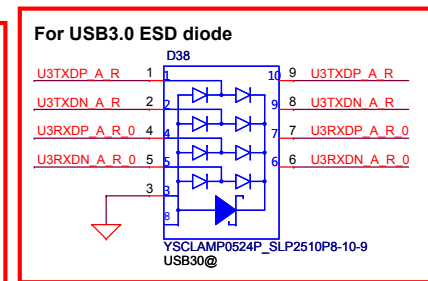
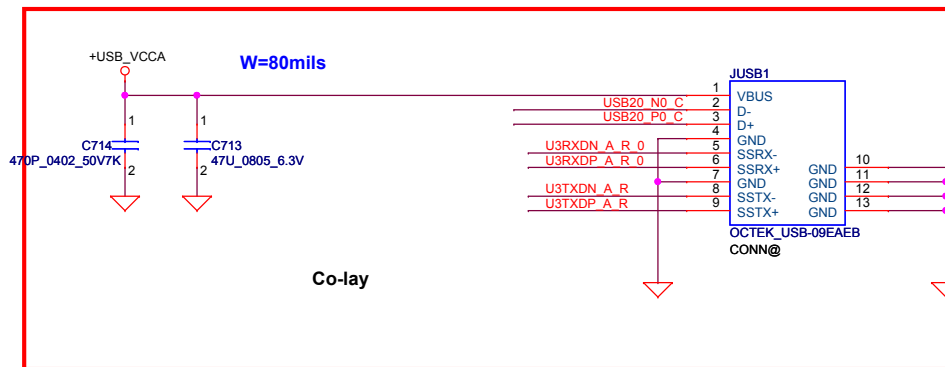
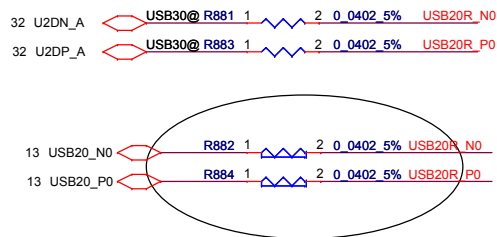
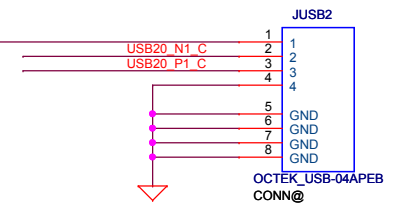
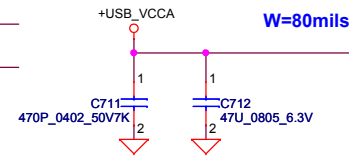




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Left USB Conn.



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	B1710	B1710
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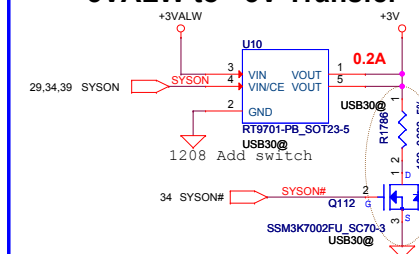
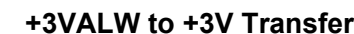
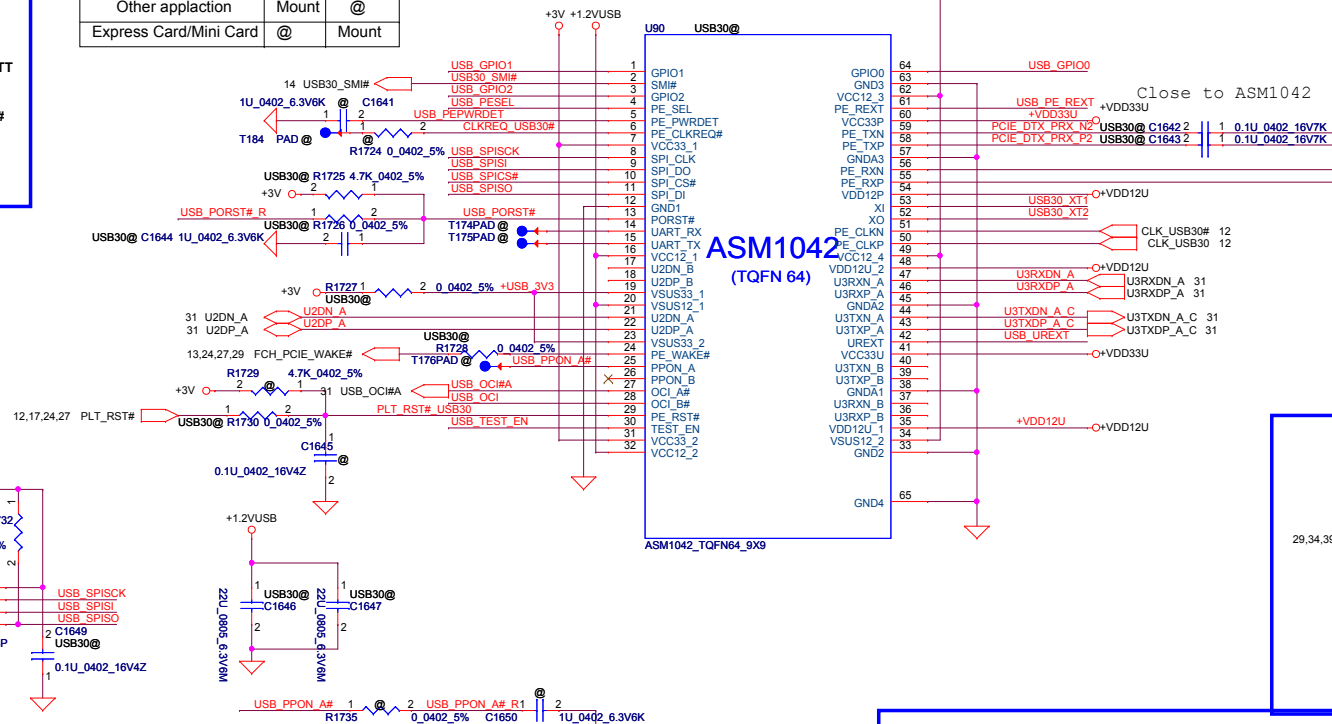
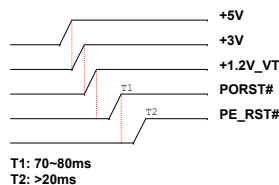
	R1719	R1706
S1	Mount	@
S3	@	Mount

USB PESEL

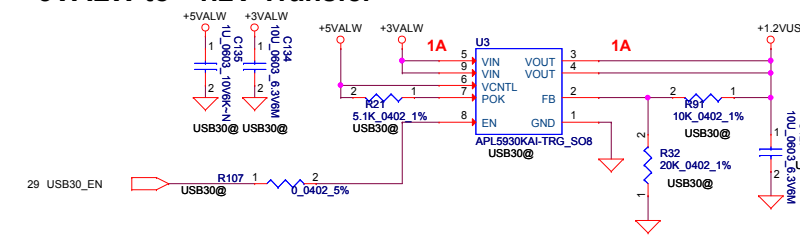
	R808	R825
Other applaction	Mount	@
Express Card/Mini Card	@	Mount

Power Sequence

ASM1042

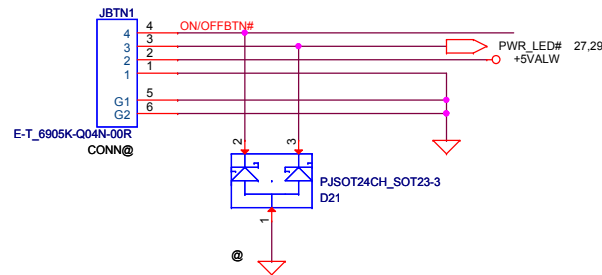
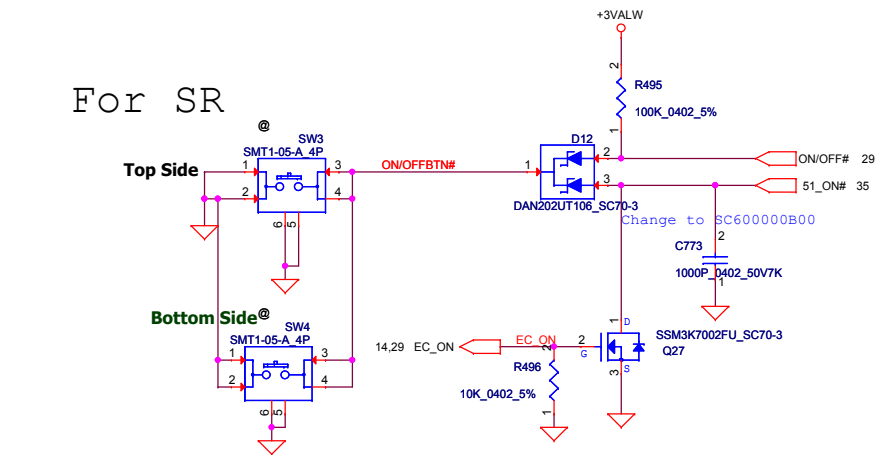


+3VALW to +1.2V Transfer

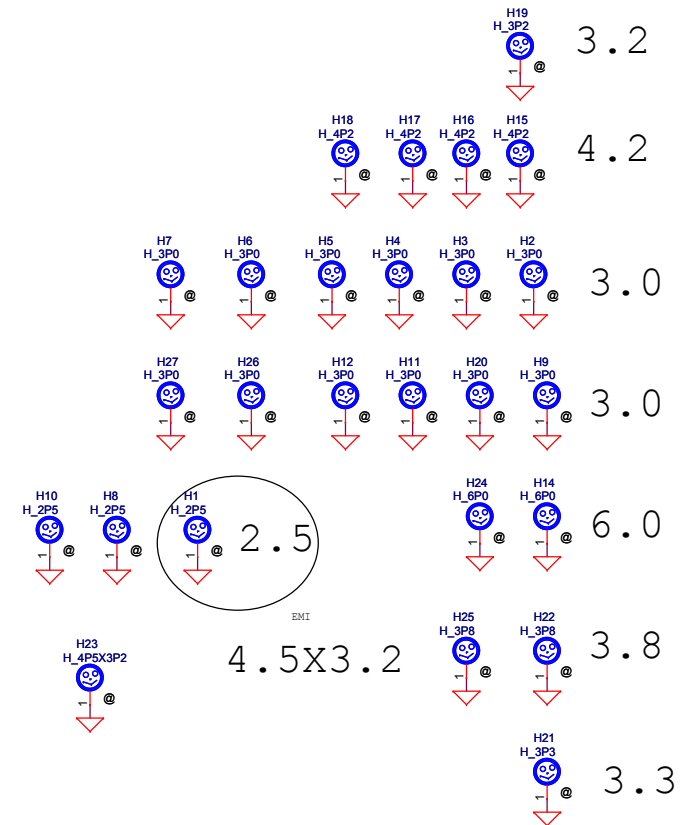
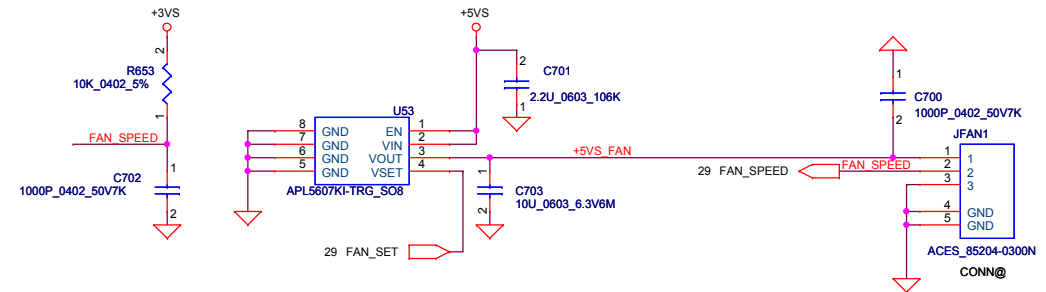


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For SR

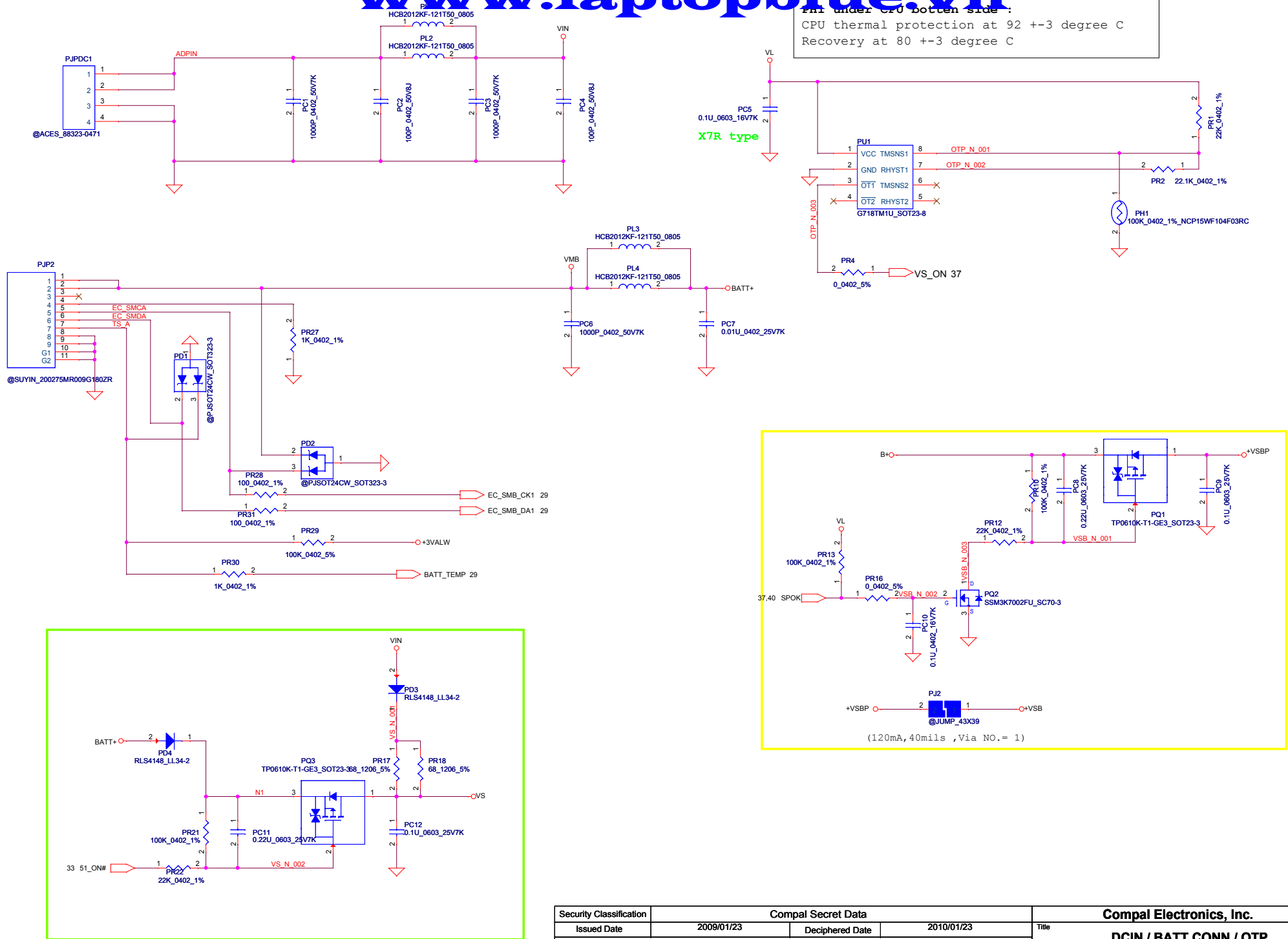


Fan Control Circuit

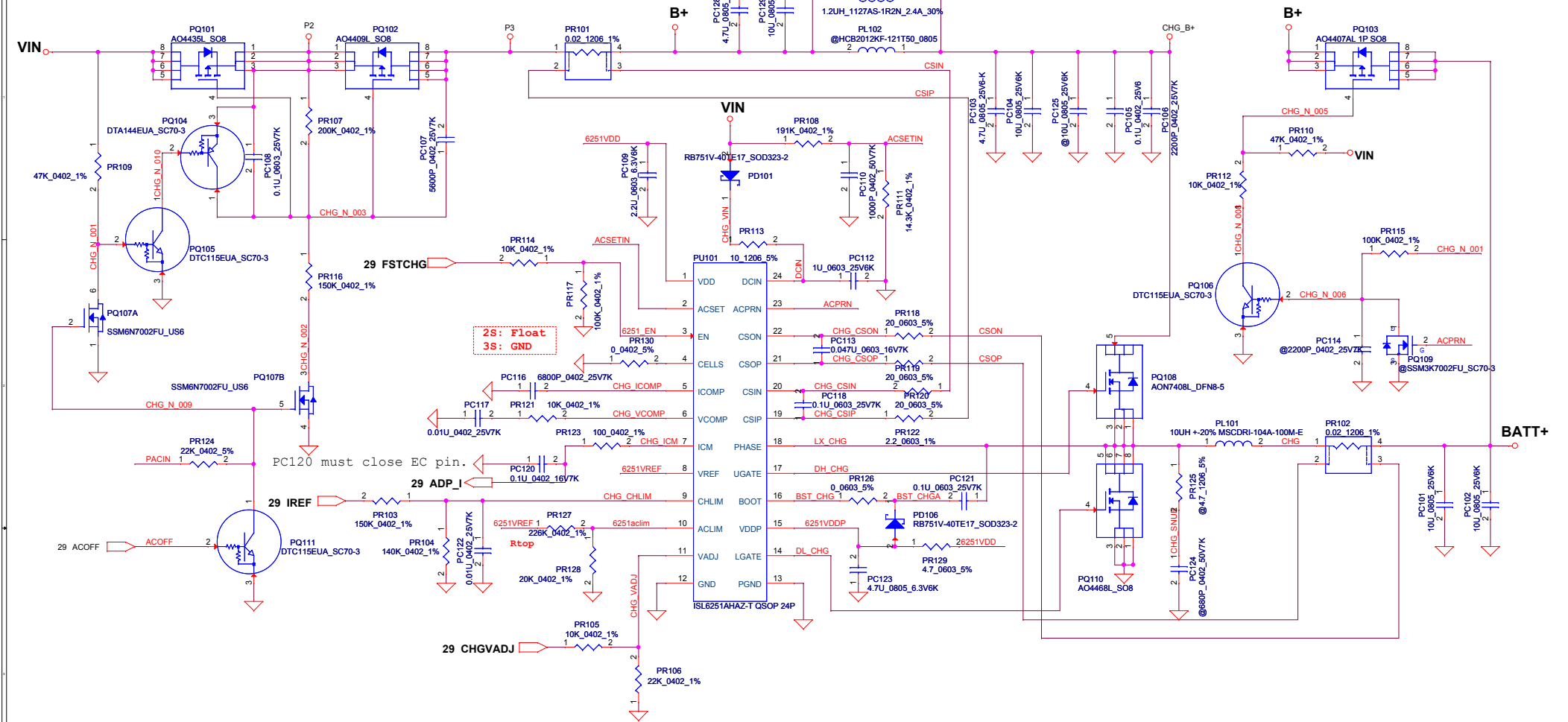


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Pin under CPU bottom side :
CPU thermal protection at 92 +-3 degree C
Recovery at 80 +-3 degree C



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CP= 85%*Iada;
Iada=0~4.737A(90W);CP=4.03A;where Raccdet=0.020ohm,where Rtop=12.4K
90W for Dis:Rtop:SD00000AJ80
Iada=0~3.421A(65W);CP=2.91A;where Raccdet=0.020ohm,where Rtop=226K
65W for UMA:Rtop:SD034226380
Astro2010_01_15 need confirm P/N

CP mode
Vaclim=VREF*(Rbot/(Rinternal/(Rtop/(Rinternal+Rbot)/(Rinternal)))
when 90W Vaclim=2.39*(20K/(152K/(20K/(152K+12.4K/(152K)))=1.44966V
when 65W Vaclim=2.39*(20K/(152K/(20K/(152K+226K/(152K)))=0.38914V
Iinput=(1/Racdet)*(0.05*Vaclim/VREF+0.05)
when 90W,Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W,Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A

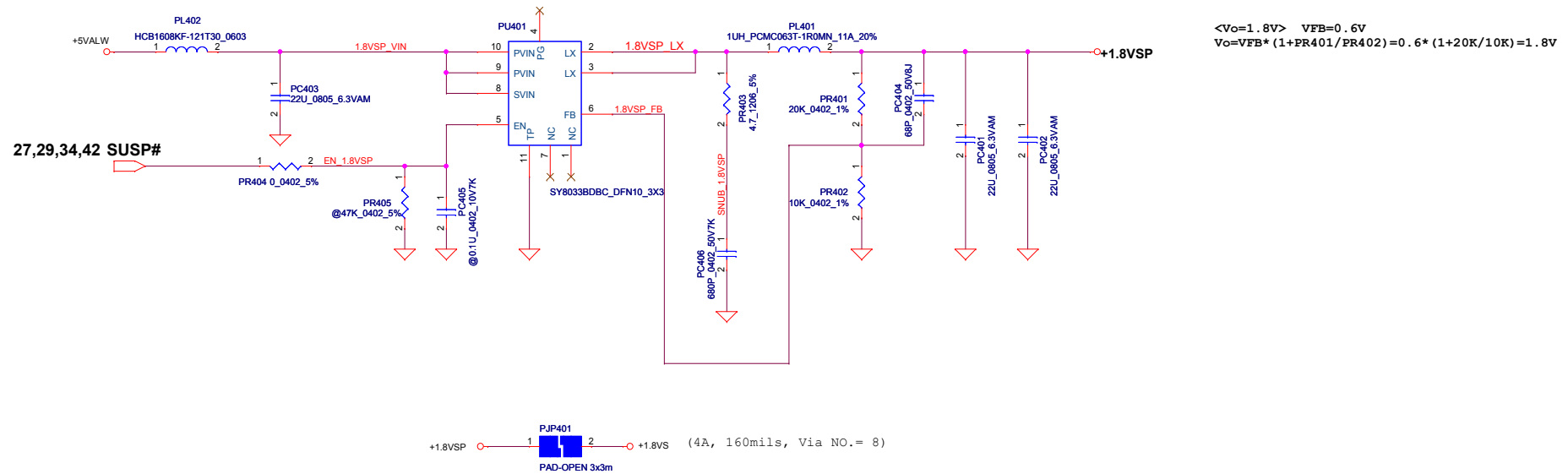
CC=0.25A-3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627
Vcell CHGVADJ
4V 0V
4.2V 1.882V

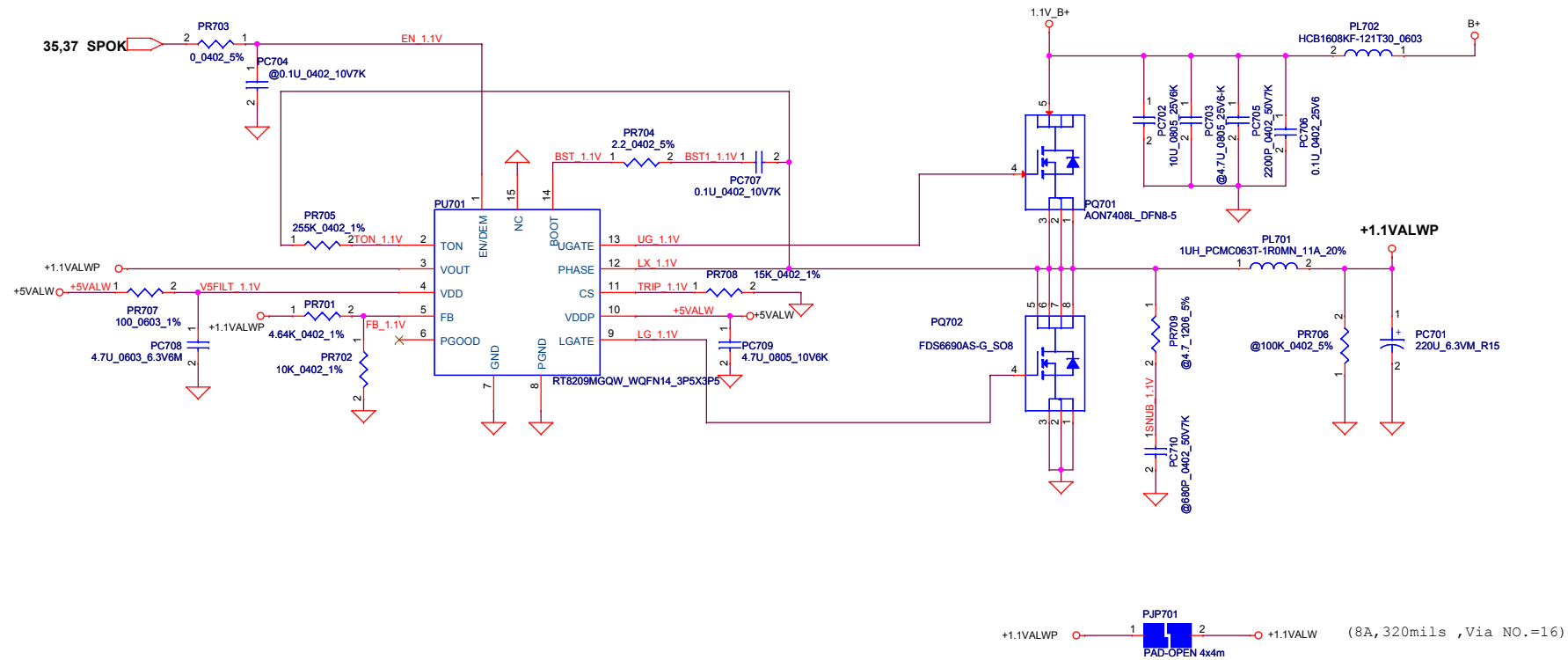
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EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

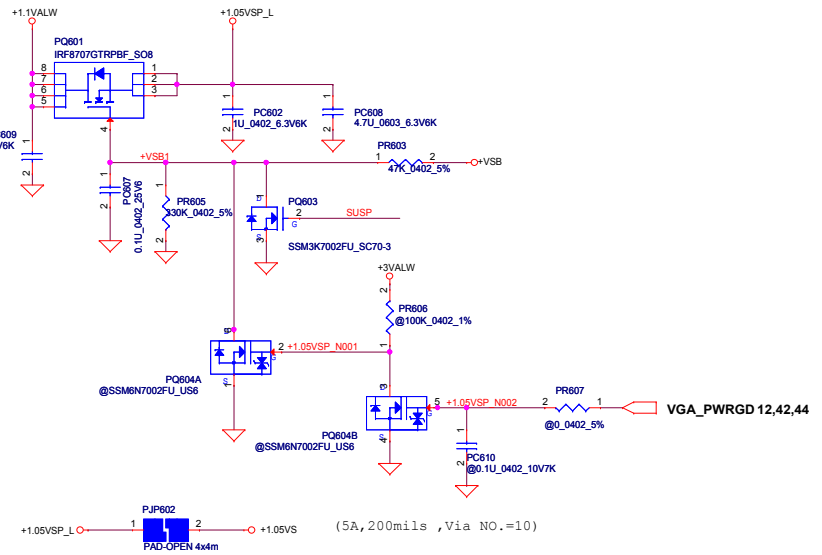
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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title	
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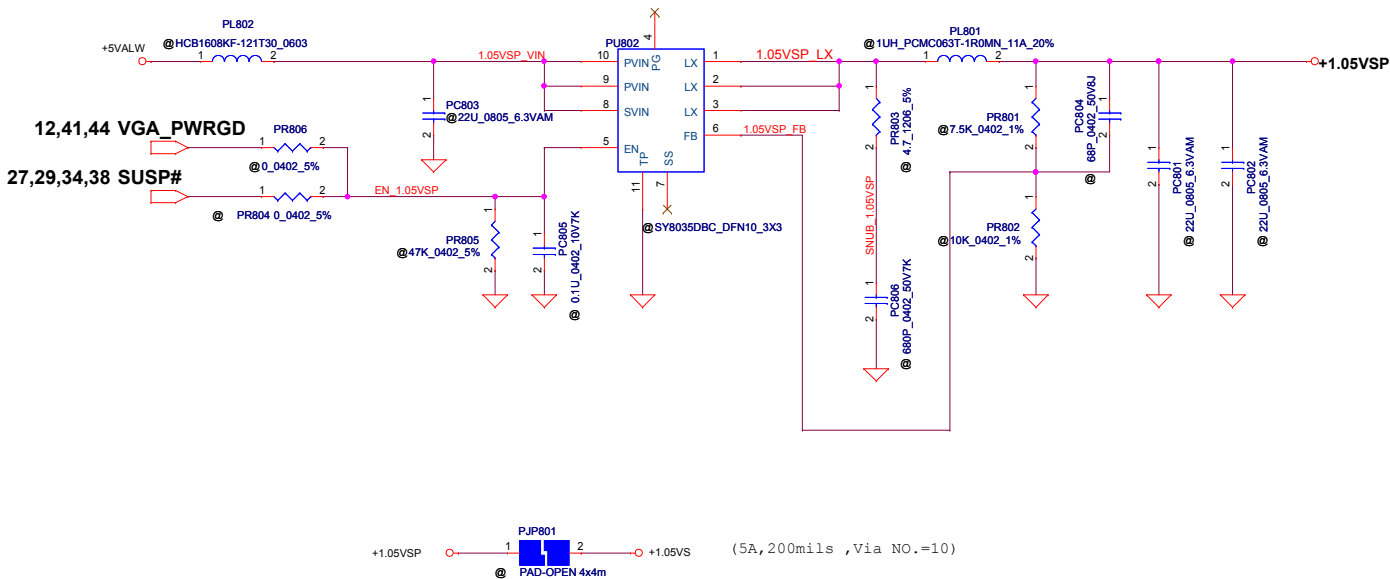
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				Document Number
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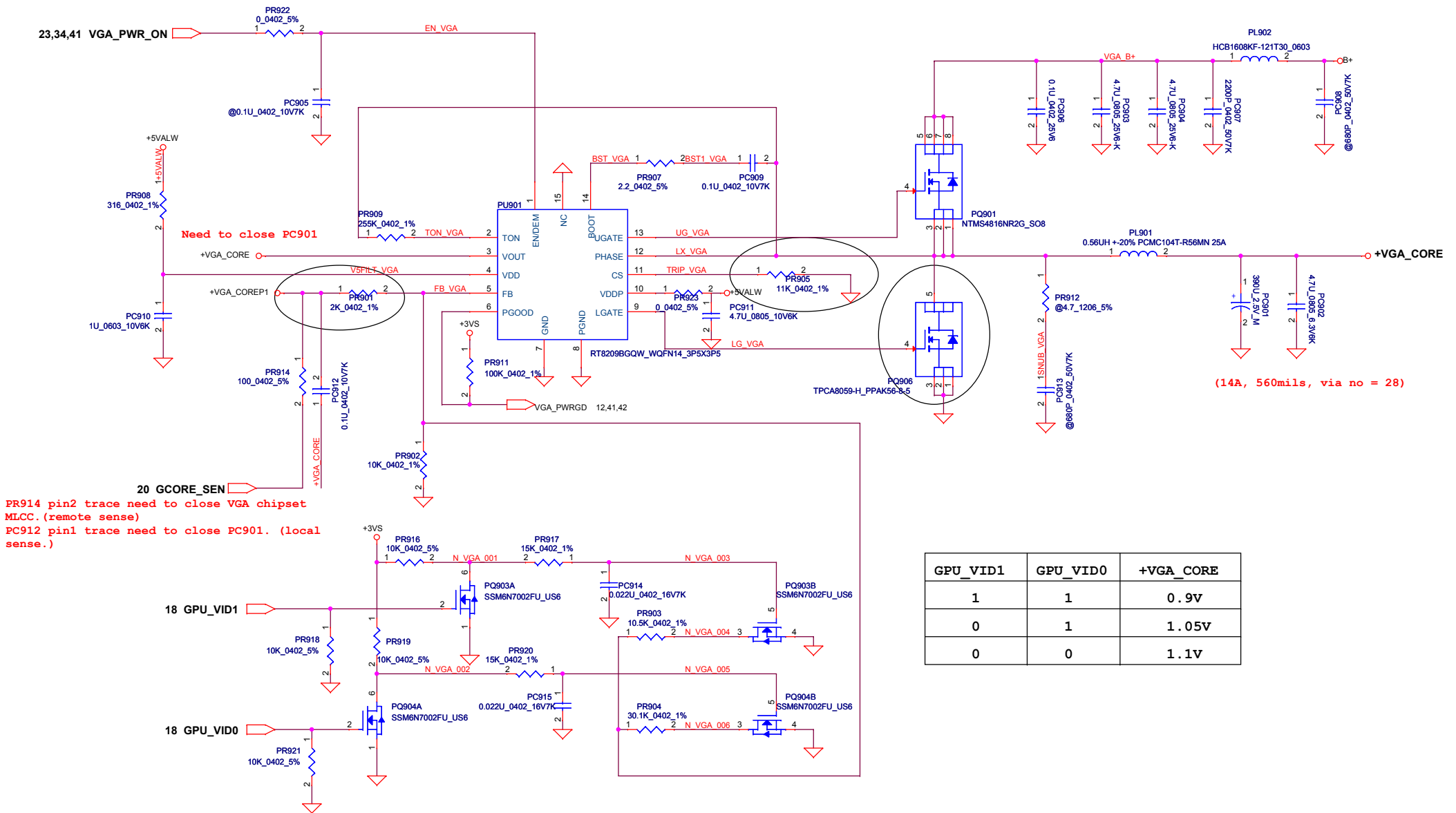
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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

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Issued Date	2008/09/15	Deciphered Date	2010/12/31	Changed-List History	
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		DFB request	0.11	PG#10	change JLVD51 connector to 40 pin and add JCM1 6pin	12/17	ER
2		EC remove ext crystal	0.11	PG#29	Add R1787 and C1677	12/17	ER
3		DFB request for soldering	0.11	PG#30 PG#33	Change JTP1 and JBTN1 footprint	12/17	ER
4		JUSB2 no function	0.11	PG#31	Update JUSB2 symbol	12/17	ER
5		LID issue	0.11	PG#13	R930 change to pop	12/17	ER
6		LID issue	0.11	PG#29	LID_SW# added a pull up 10Kohm. (R35)	12/17	ER
7		Update Broad ID	0.11	PG#29	Change R1606 to 154Kohm	12/17	ER
8		for BIOS crisis	0.12	PG#14	Add U11	12/17	ER
9		DDR3 SPD	0.12	PG#8	Reserve R152 , R155	12/17	ER
10		For discharge spec	0.13	PG#24	Add R1788 and Q113 discharge schematic	12/17	ER
11		For EMI test	0.2	PG#11	Remove Level Shifter schematic	12/17	ER
12		BIOS change to share ROM	0.2	PG#16 PG#29	Pop R594 and R602 , unpop R601 and R550 change U48 meterial	12/17	ER
13		Fix S3 resume black screen	0.21	PG#6	Add R1790 , R1791 68ohm pull down	02/18	PR
14		DFX request	0.21	PG#11	Update JDIMM2 footprint	02/18	PR
15		Fix S3 resume too long	0.21	PG#18	Add R1795 1M ohm	02/18	PR
16		Fix assembly issue	0.21	PG#29 PG#25	Update JKB1 and JAU1 footprint for ME connector	02/18	PR
17		EMI request	0.22	PG#11	pop L11~L14	02/22	PR
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