

Compal Confidential

Model Name : Z5WAH

File Name : LA-B162P

Compal Confidential

EA50_HB M/B Schematics Document

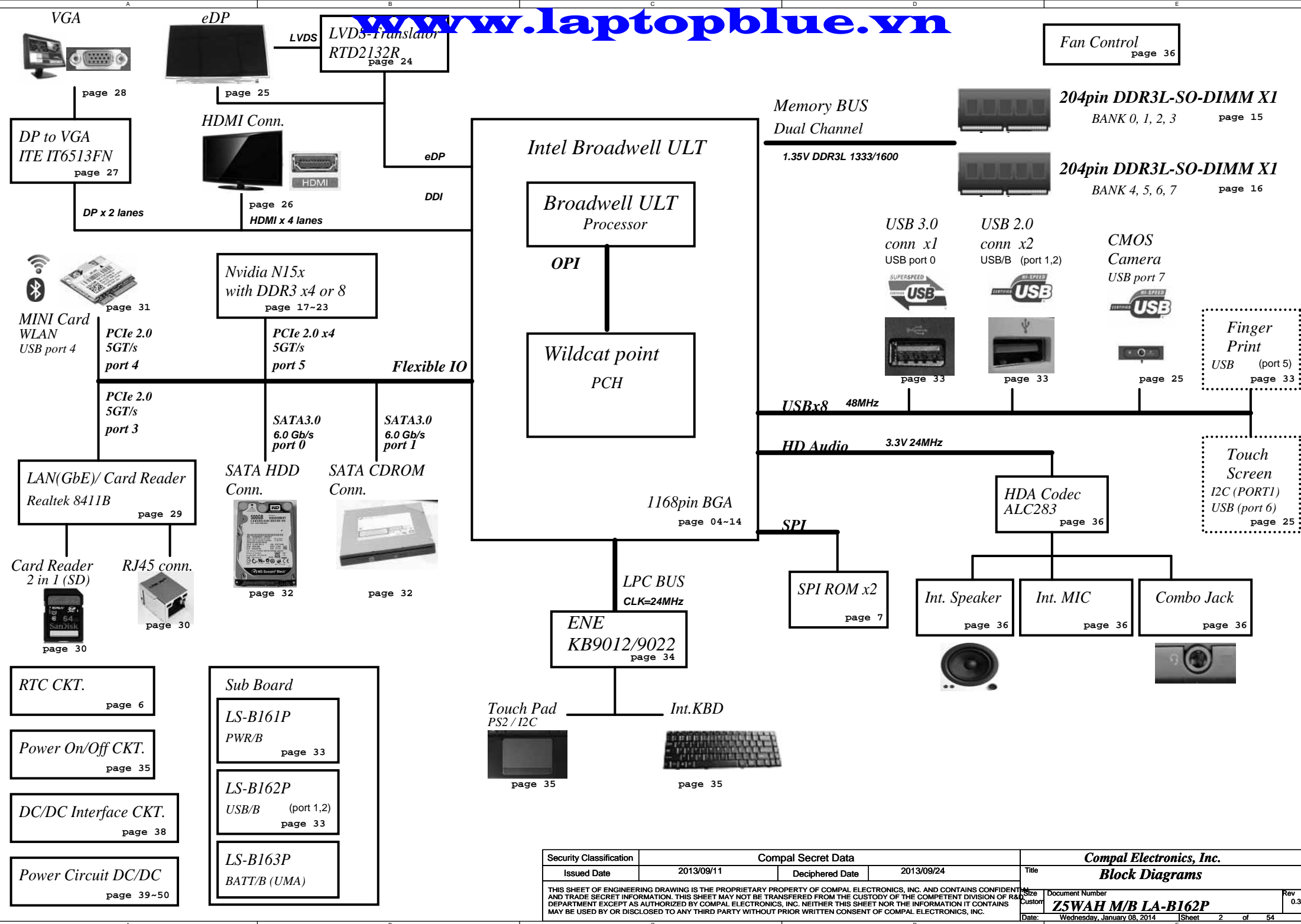
Intel Broadwell ULT (Broadwell + Wildcat point)

Nvidia N15S-GT / N15V-GM / N15V-GL

2013-12-24

REV:0.2

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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EC SM Bus1 address EC SM Bus2 address

PCH SM Bus address

State	CS#	CS#	CS#	CS#	CS#	CS#	CS#	CS#
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

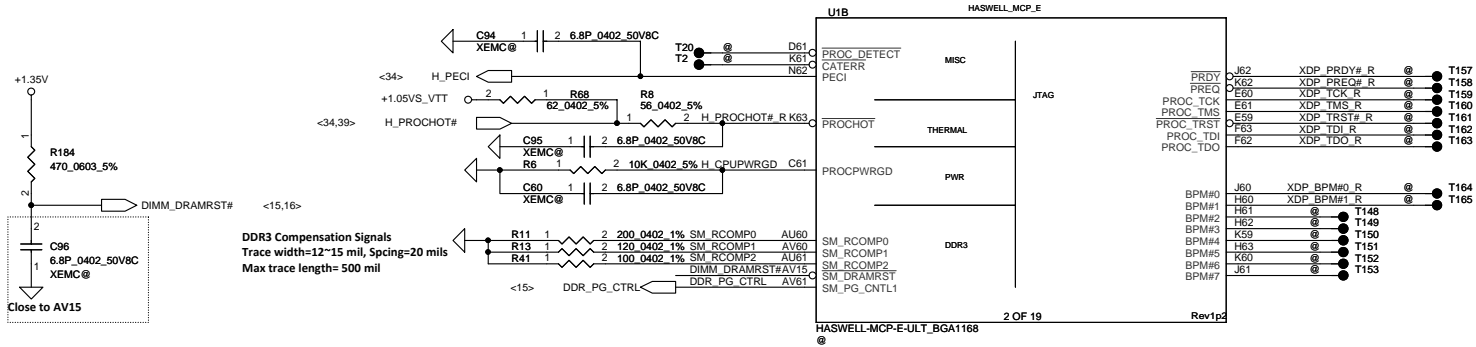
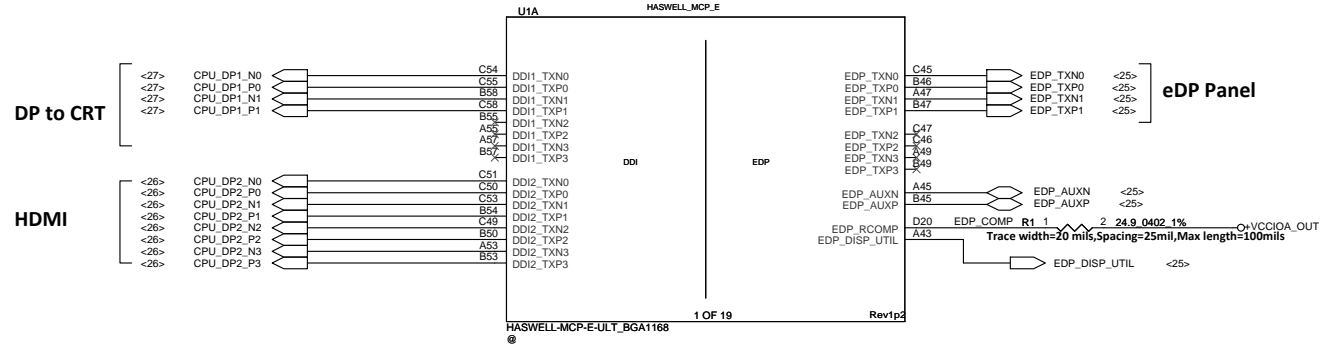
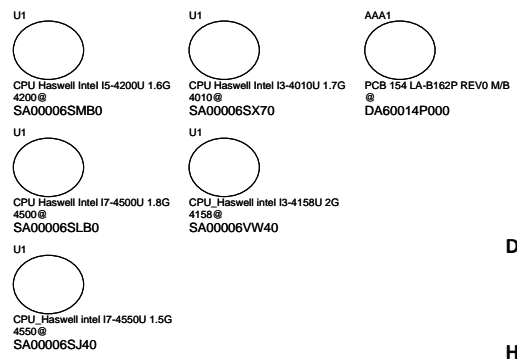
VCC	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	12K +/- 5%	0.347 V	0.354 V	0.360 V
2	15K +/- 5%	0.423 V	0.430 V	0.438 V
3	20K +/- 5%	0.541 V	0.550 V	0.559 V
4	27K +/- 5%	0.691 V	0.702 V	0.713 V
5	33K +/- 5%	0.807 V	0.819 V	0.831 V
6	43K +/- 5%	0.978 V	0.992 V	1.006 V
7	56K +/- 5%	1.169 V	1.185 V	1.200 V
8	75K +/- 5%	1.398 V	1.414 V	1.430 V
9	100K +/- 5%	1.634 V	1.650 V	1.667 V
10	130K +/- 5%	1.849 V	1.865 V	1.881 V
11	160K +/- 5%	2.015 V	2.031 V	2.046 V
12	200K +/- 5%	2.185 V	2.200 V	2.215 V
13	240K +/- 5%	2.316 V	2.329 V	2.343 V

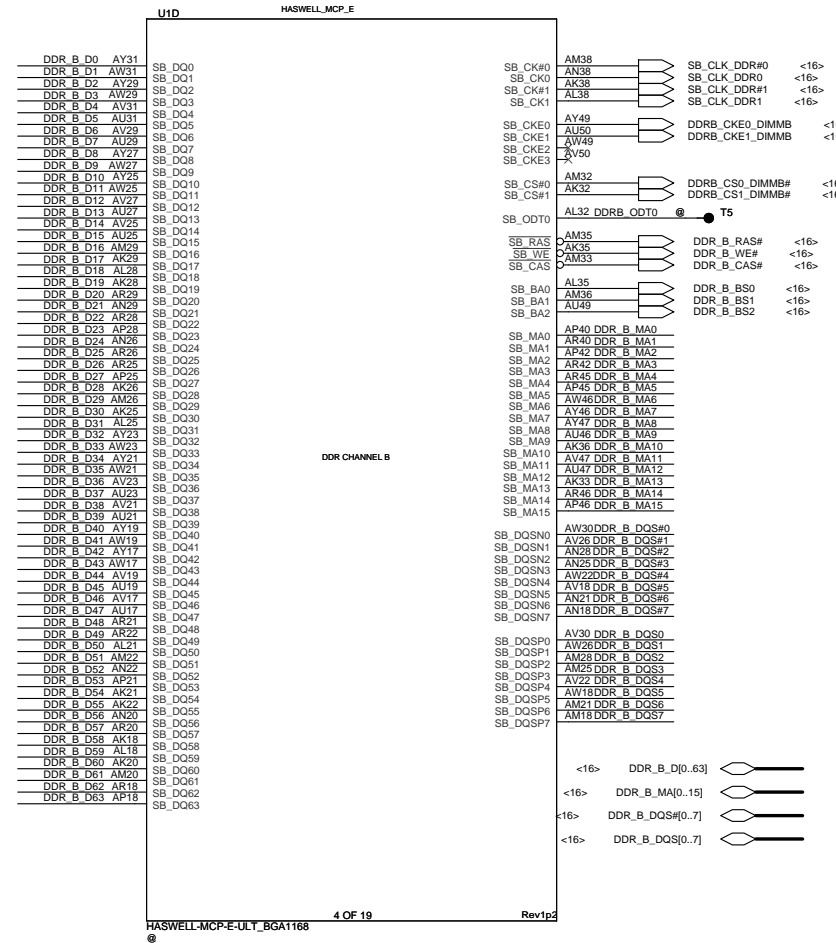
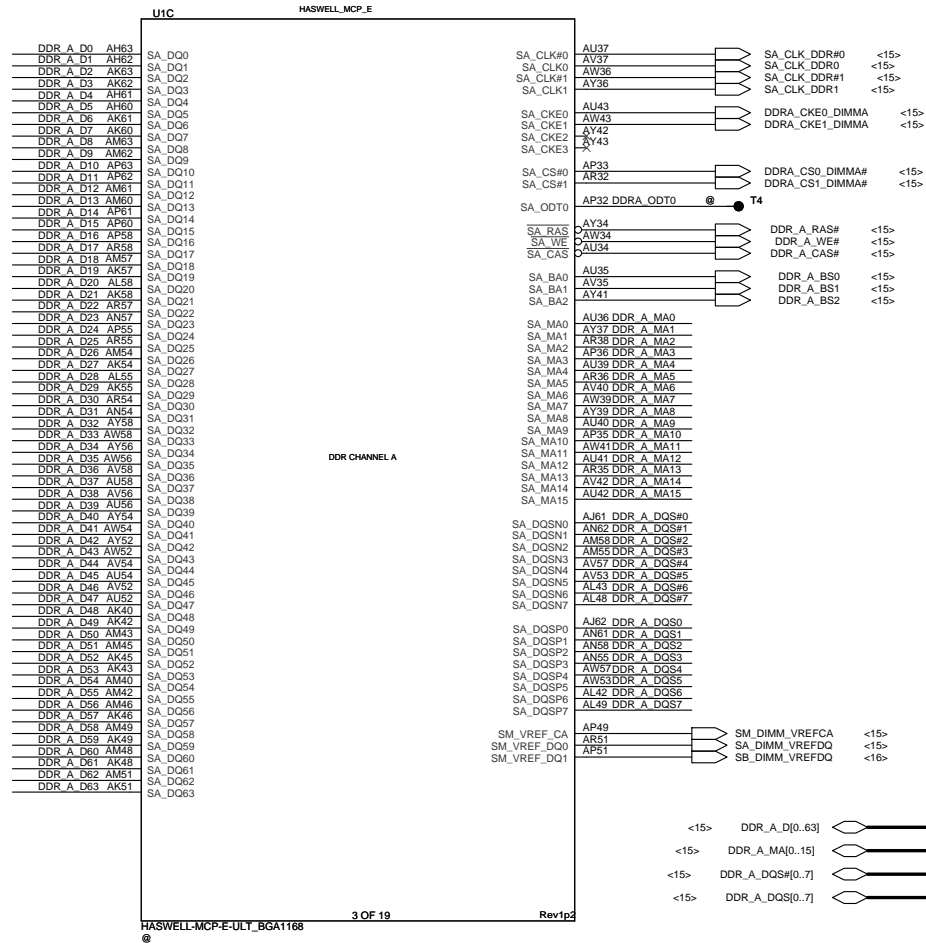
BTO Option Table

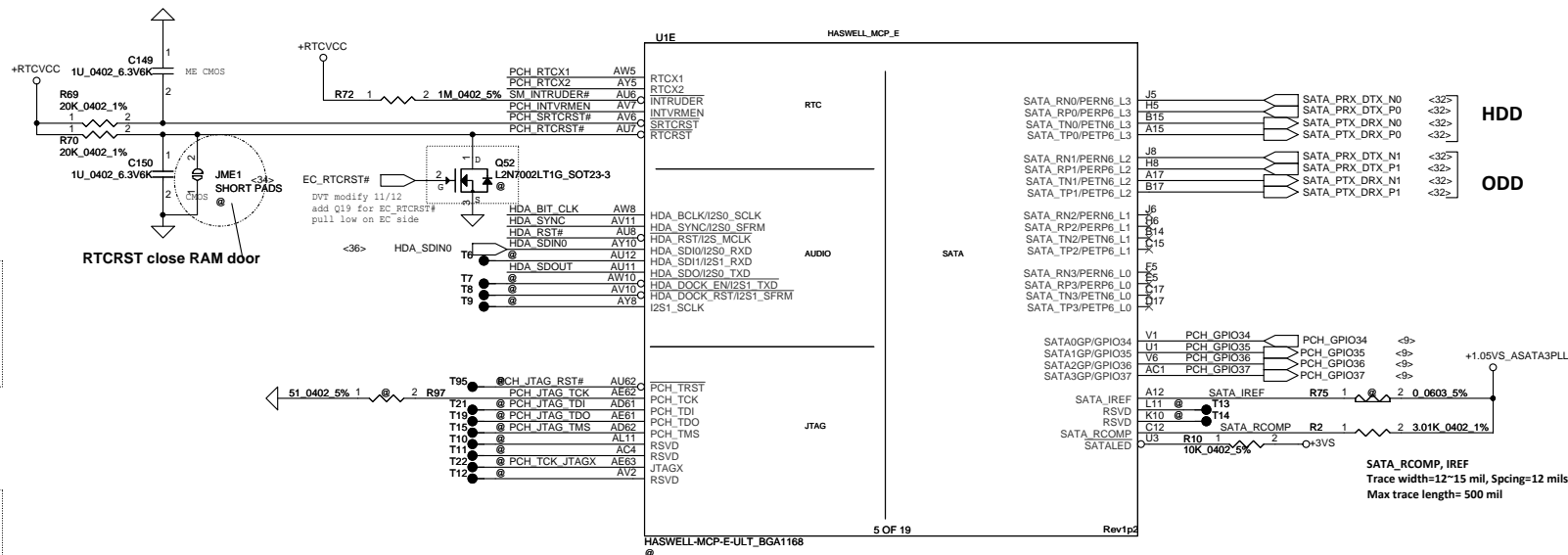
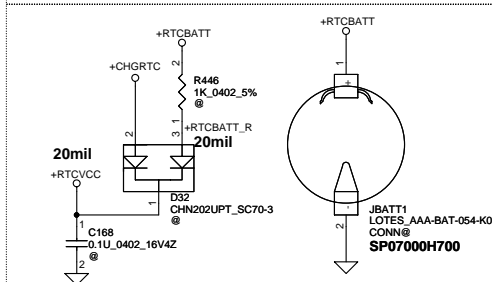
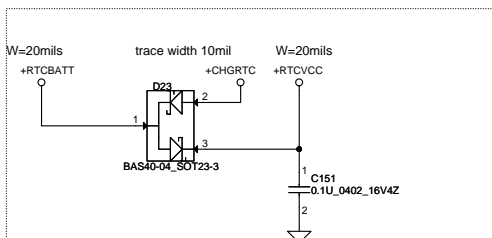
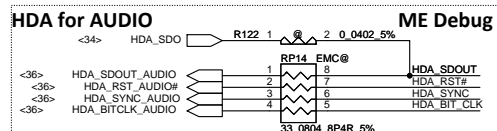
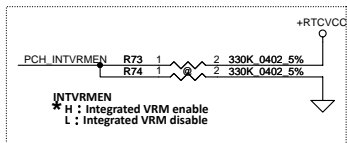
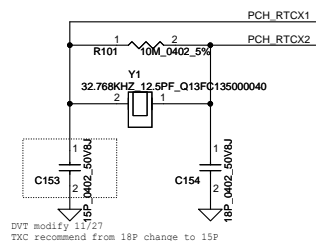
BTO Option Table	
BTO Item	BOM Structure
Unpop	@
Connector	CONN@
EC 9022	9022@
EC 9012	9012@
UMA Component	UMA@
GPU	VGA @
VRAM x 8pcs	128@
EDP panel	EDP@
eDP to LVDS	LVDS@
EMC Component	EMC@
EMC Reserve	XEMC@
On Board HDD	HDD@
G-Sensor	BA@
TPM Module	BA@
Redriver HDD	BA@
Touch Screen	TS@
DGPU_IDEN	VGL@, VGM@, SGT@
CPU_IDEN	HW@, BW@
GC6 2.0	GC6@
non GC6	NGC6@
One DMIC	EA50@
Two DMIC	EA54@
VRAM Selection	X76@

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	1.0
6	
7	

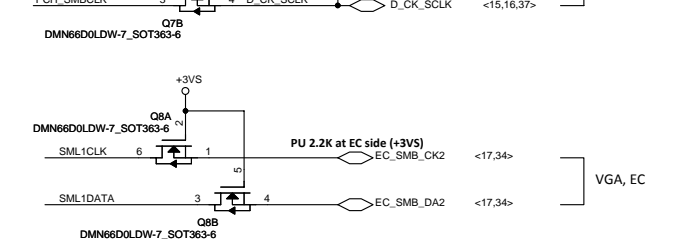
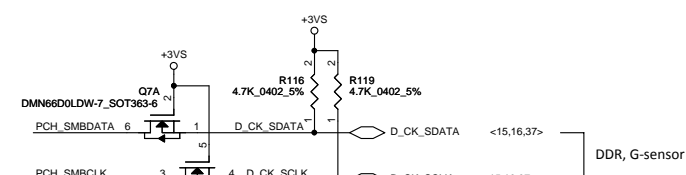
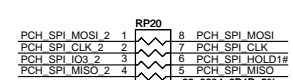
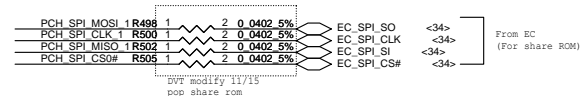
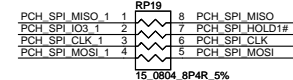
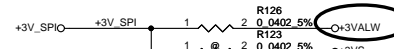
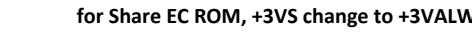
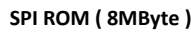
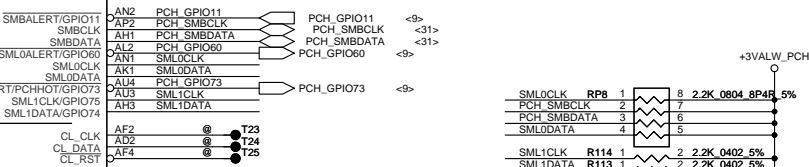
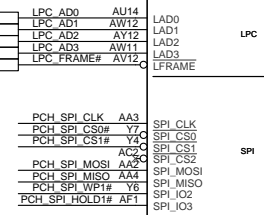
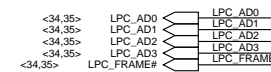
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Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> BDW MCP(3/11) RTC,SATA,XDP	
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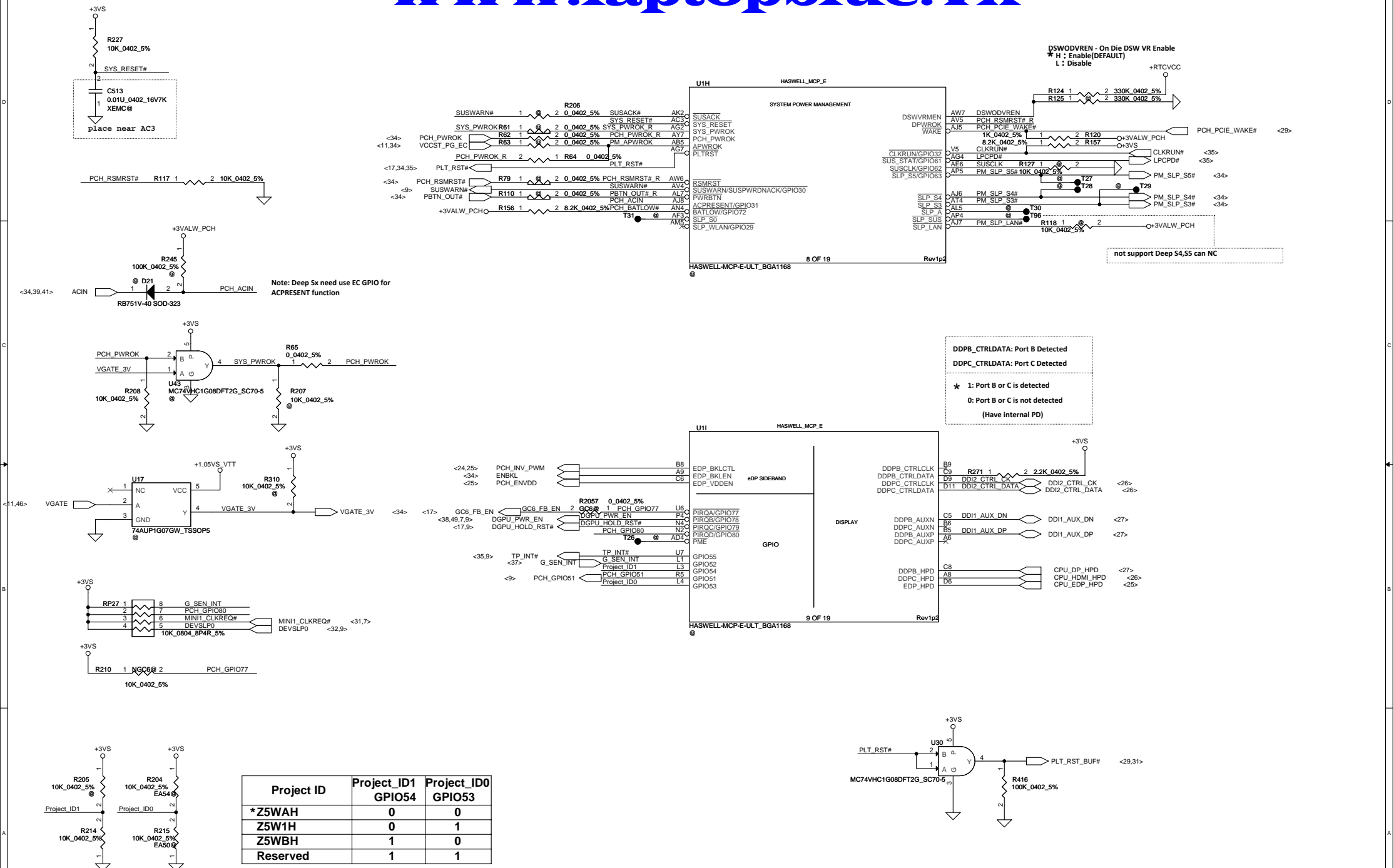
2ROM is SPI ROM 2M + 4M Byte

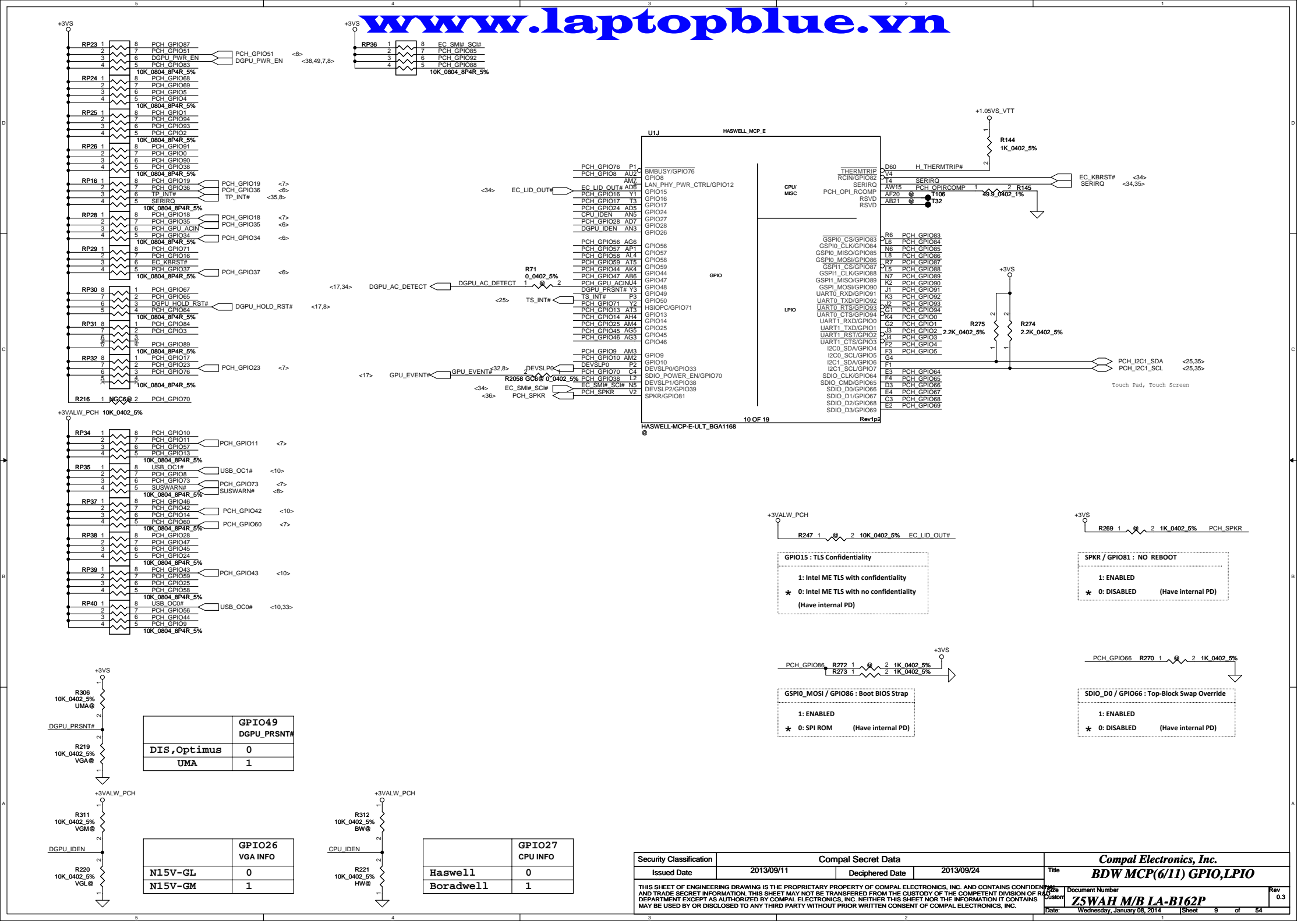
```
2ROM POP
U6 - EN25QH16-104HIP_S08 (SA00004UG00
RP19 - 33_0804_8P4R_5% (SD309330A80)
R108 - 33_0402_5% (SD028330A80)
```

Reserve for EMI(Near SPI ROM)

C453
10P_0402_50V8J
1 2
XEMC@ R402 2 1 PCH SPI C
XEMC@ 33_0402_5%

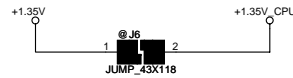
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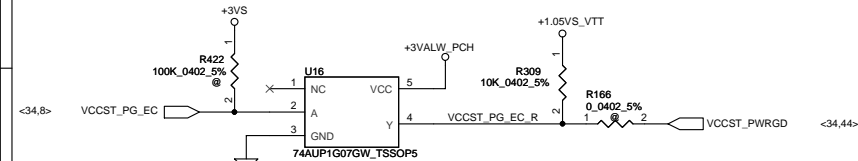


	GPIO26 VGA INFO
N15V-GL	0
N15V-GM	1

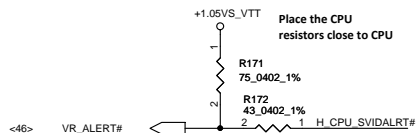
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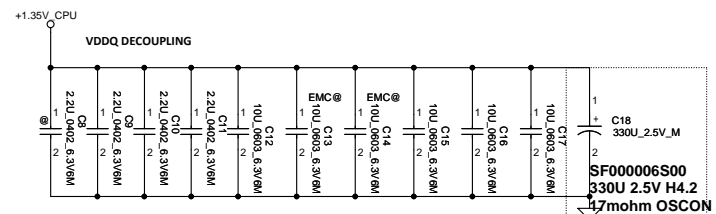
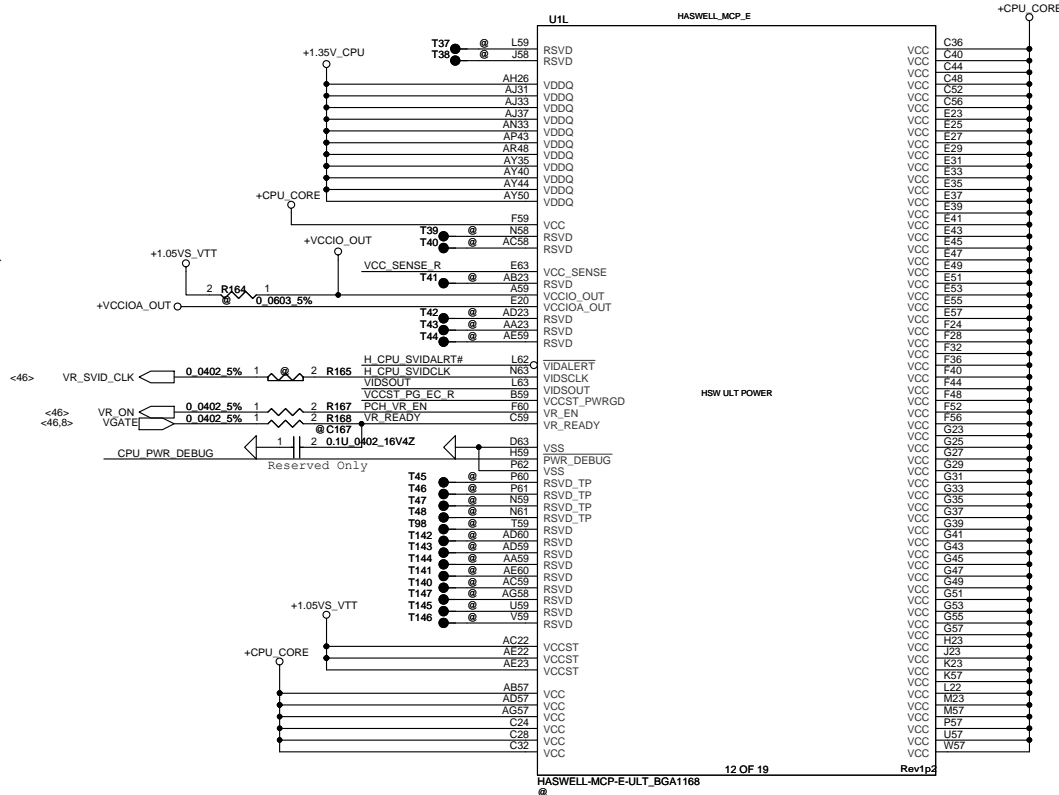
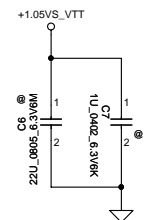
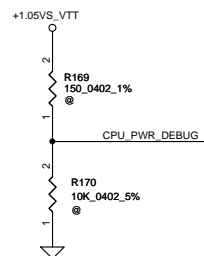
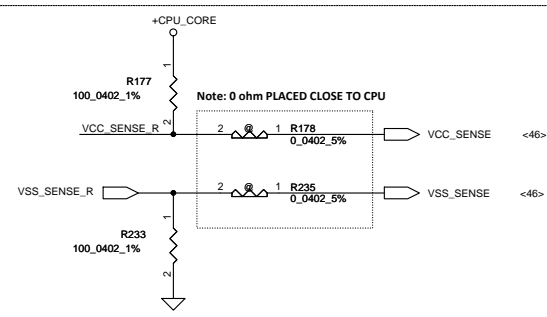
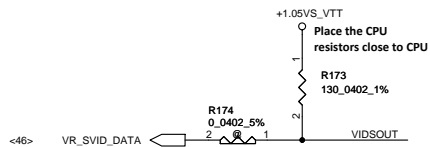
Shark Bay ULT have internal gate for VDDQ



SVID ALERT



SVID DATA



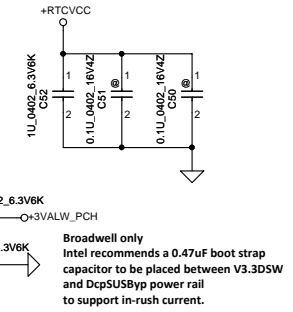
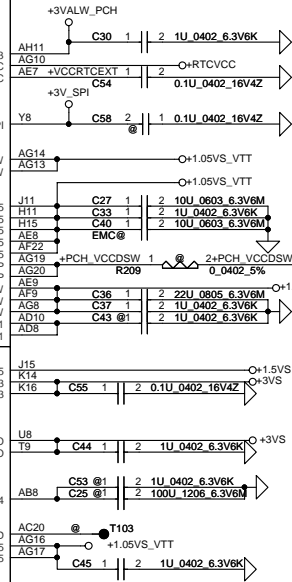
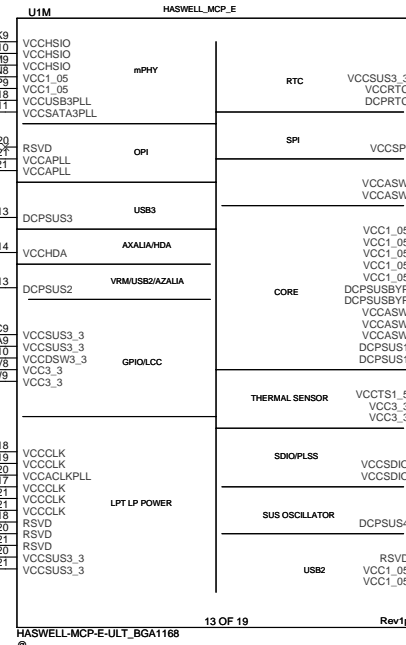
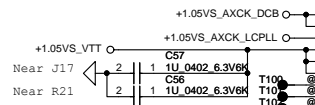
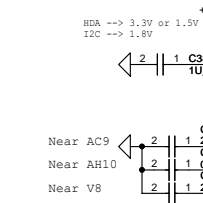
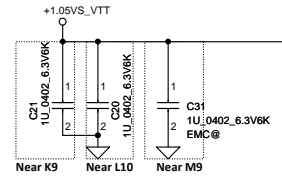
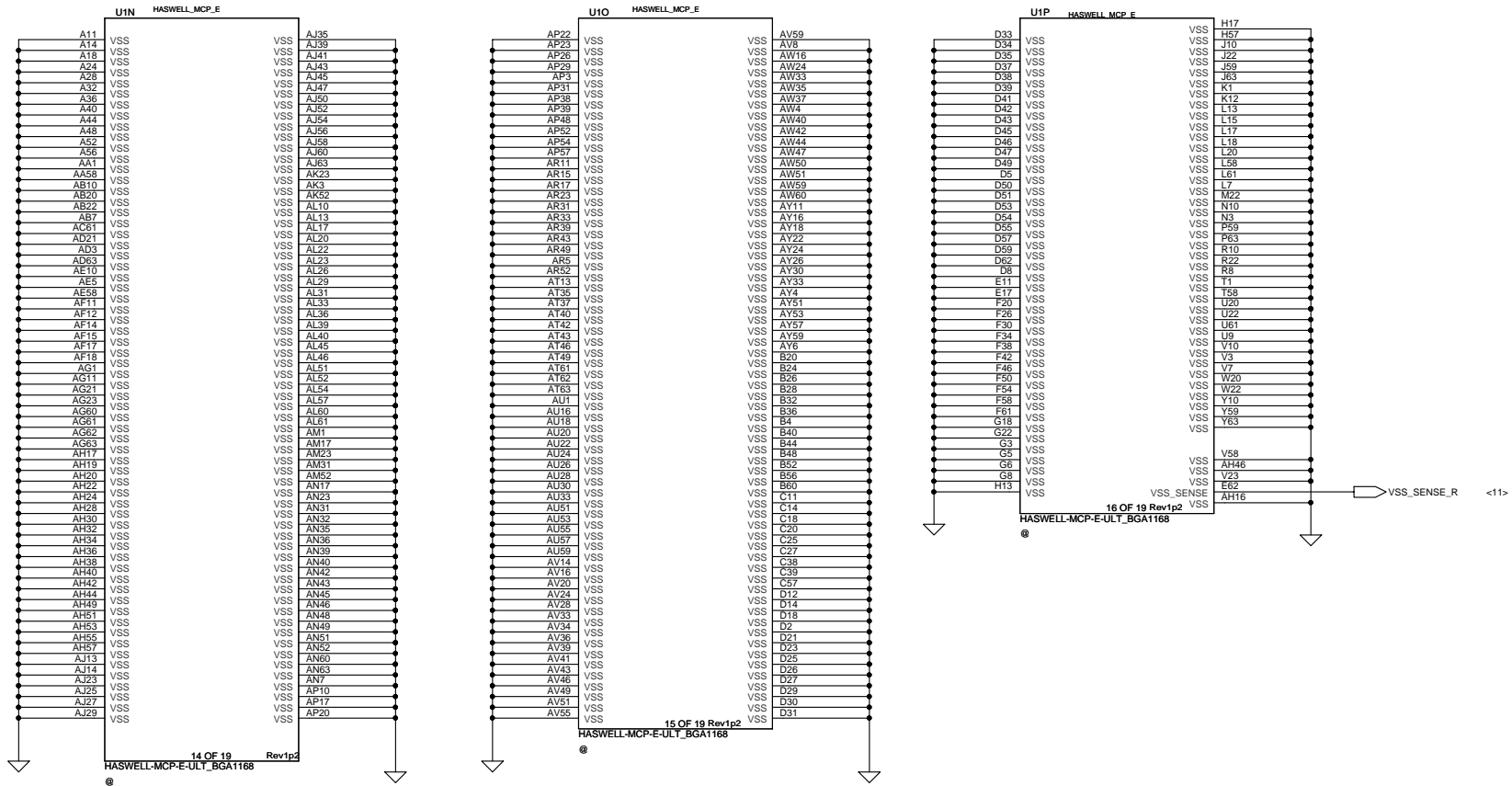
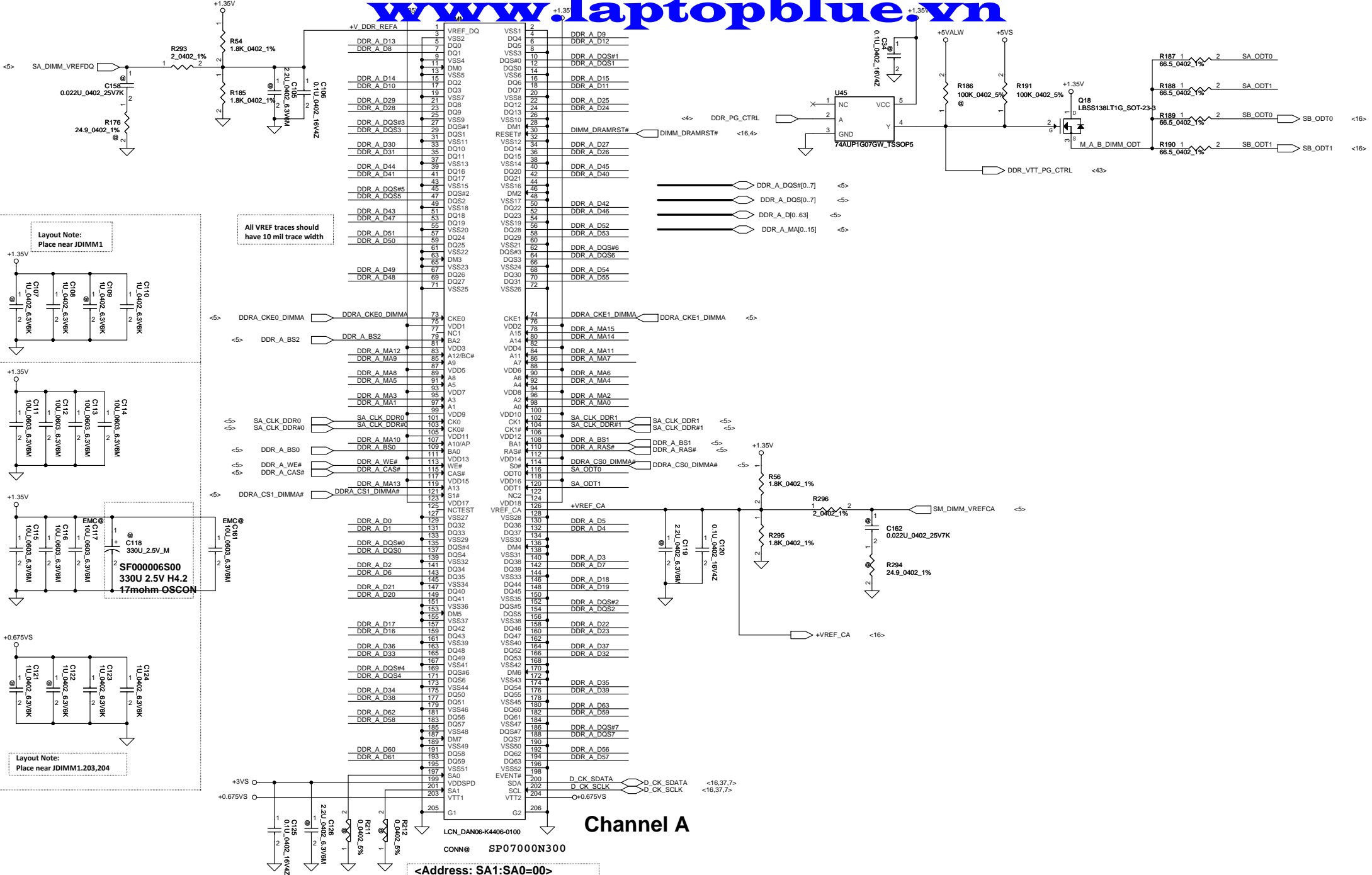
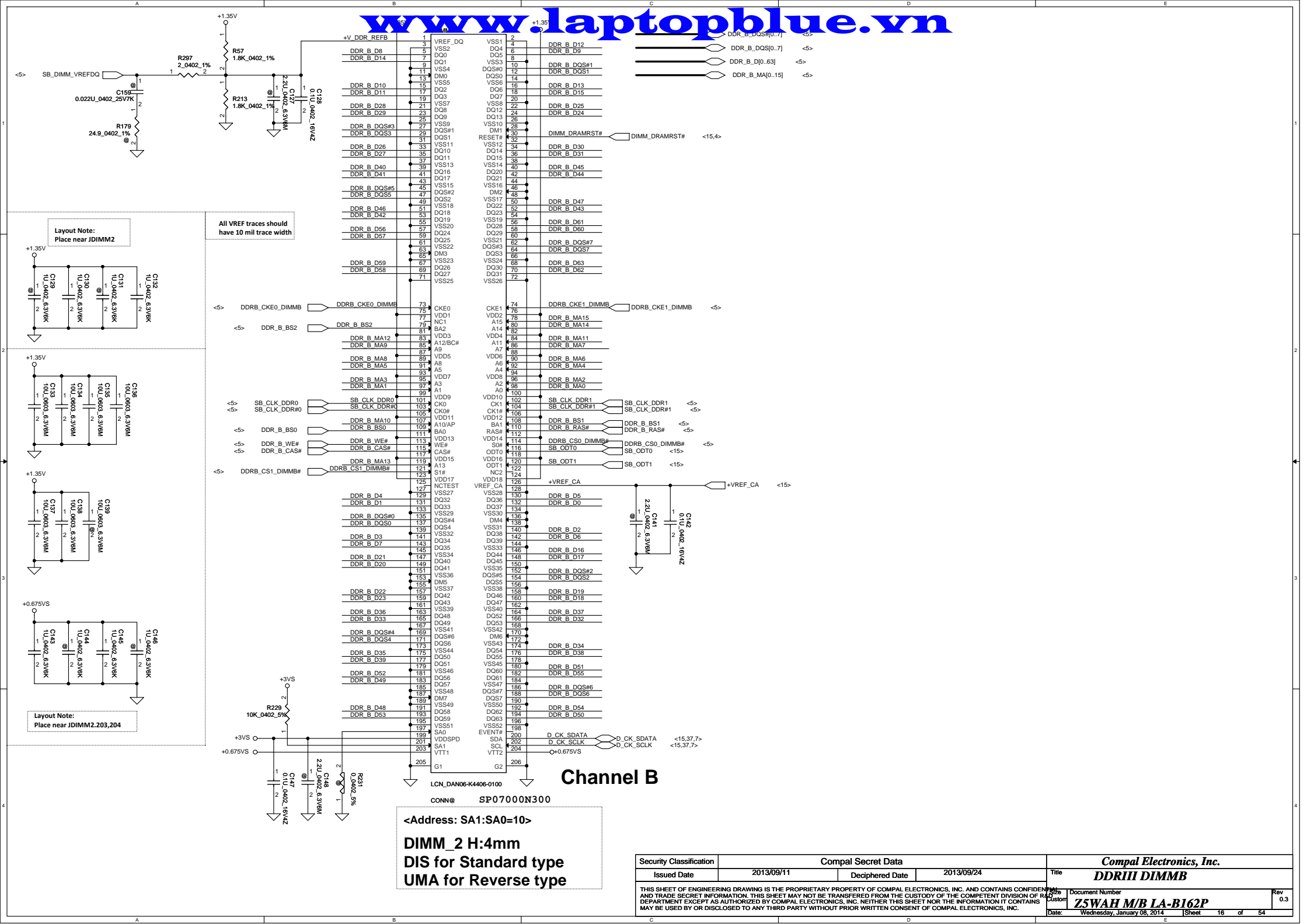


Diagram of the J8 connector. The connector is a two-pin header. Pin 1 is connected to the +3VALW signal. Pin 2 is connected to the +3VALW_PCH signal. The connector is labeled J8 @ JUMP 43X39.







<10> PEG_HTX_C_GRX_P0
<10> PEG_HTX_C_GRX_N0
<10> PEG_HTX_C_GRX_P1
<10> PEG_HTX_C_GRX_N1
<10> PEG_HTX_C_GRX_P2
<10> PEG_HTX_C_GRX_N2
<10> PEG_HTX_C_GRX_P3
<10> PEG_HTX_C_GRX_N3

UGPU1A
Part 1 of 6
GPIO
DACs
PCI EXPRESS
I2C
CLK

C6 GC6_FB_EN → GC6_FB_EN <8>
GPIO0 B2
GPIO1 D6
GPIO2 C7
GPIO3 F9
GPIO4 A3
GPIO5 A4
GPIO6 B6
GPIO7 A6
GPIO8 F8
GPIO9 A9
GPIO10 E7
GPIO11 D7
GPIO12 B4
GPIO13 B3
GPIO14 C3
GPIO15 D5
GPIO16 D4
GPIO17 C2
GPIO18 F7
GPIO19 E6
GPIO20 C4
GPIO21 A6
PEX_WAKE_NC
AG3
AG4
AG5
AG6
AG7
AG8
AG9
AG10
AG11
AG12
AG13
AG14
AG15
AG16
AG17
AG18
AG19
AG20
AG21
AG22

AG3
AG4
AG5
AG6
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AG8
AG9
AG10
AG11
AG12
AG13
AG14
AG15
AG16
AG17
AG18
AG19
AG20
AG21
AG22

B7 R2003 1 VGA@ 2 1.8K 0402 5%
A7 R2004 1 VGA@ 2 1.8K 0402 5%
C9 R2005 1 VGA@ 2 1.8K 0402 5%
C8 R2006 1 VGA@ 2 1.8K 0402 5%
A9 R2007 1 VGA@ 2 1.8K 0402 5%
B9 R2008 1 VGA@ 2 1.8K 0402 5%
D9 I2CS_SCL
D8 I2CS_SDA
L6 +PLLVD
M6 +GPU_PLLVD
N6 +GPU_PLLVD
C2000 0.1u_0402_16V4Z
C2001 0.1u_0402_16V4Z

C11 XTALIN
B10 XTALOUT
A10 XTAL_SSIN R2012 1 VGA@ 2 10K 0402 5%
C10 XTAL_OUTBUR R2013 1 VGA@ 2 10K 0402 5%

RP2000
10K 0804 8P4R 5%
GPIO8_OVERT 1
GPIO9_ALERT 2
GPIO9_ALERT_GATE 3
ACIN_BUF 4
VGA@

RP2001
10K 0804 8P4R 5%
3VSDGPU_MAIN_EN 1
GPU_PEX_RST_HOLD# 2
GPU_EVENT# 3
GC6_FB_EN 4
VGA@

SYS_PEX_RST_MON#2 R2056 1 10K 0402 5%
I2CS_SDA 1 VGA@ 2 1.8K 0402 5%
I2CS_SCL 1 VGA@ 2 1.8K 0402 5%
PSI 2 VGA@ 1 10K 0402 5%

PLTRST VGA#
GPIO8_OVERT 1
VGA@ 2
DMN66D0LDW-7_SOT363-6 Q2000A

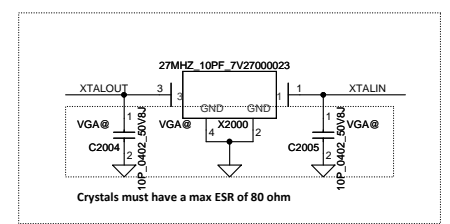
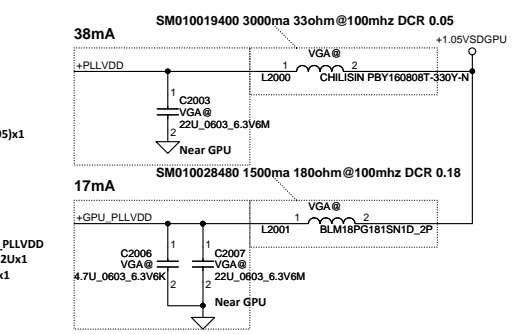
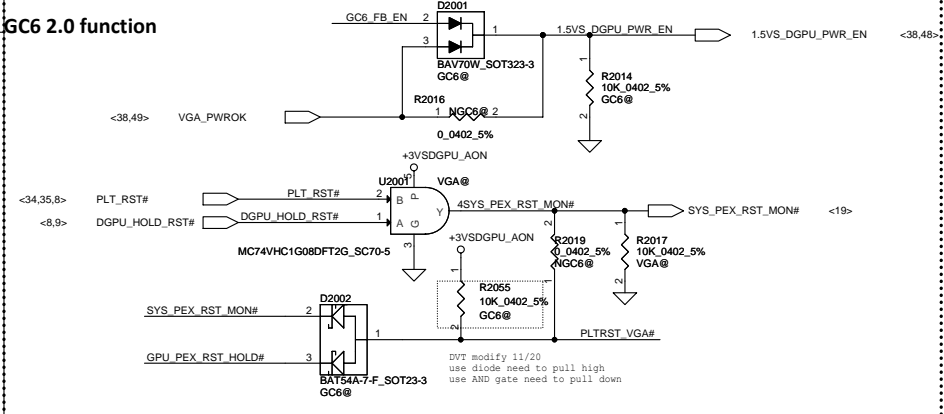
GPIO9_ALERT_GATE
GPIO9_ALERT 4
VGA@ 2
DMN66D0LDW-7_SOT363-6 Q2000B

+3VSDGPU_AON
I2CS_SCL 1
VGA@ 2
DMN66D0LDW-7_SOT363-6 Q2001A

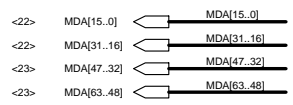
+3VSDGPU_AON
I2CS_SDA 4
VGA@ 2
DMN66D0LDW-7_SOT363-6 Q2001B

GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		

+3VSDGPU_AON R2009 1 VGA@ 2 10K 0402 5% <7>
PEG_CLKREQ# PEG_CLKREQ# <7>
CLK_PEG_VGA CLK_PEG_VGA# <7>
PEG_TSTCLK_OUT+ AF22 200_0402_1%
PEG_TSTCLK_OUT- AE22
PEX_TSTCLK_OUT PEX_TSTCLK_OUT_N
PEX_RST_N AF27
PEX_TERM AF25
PLTRST VGA# AC7
PEX_TREMP AF25
R2011 2.49K 0402_1%



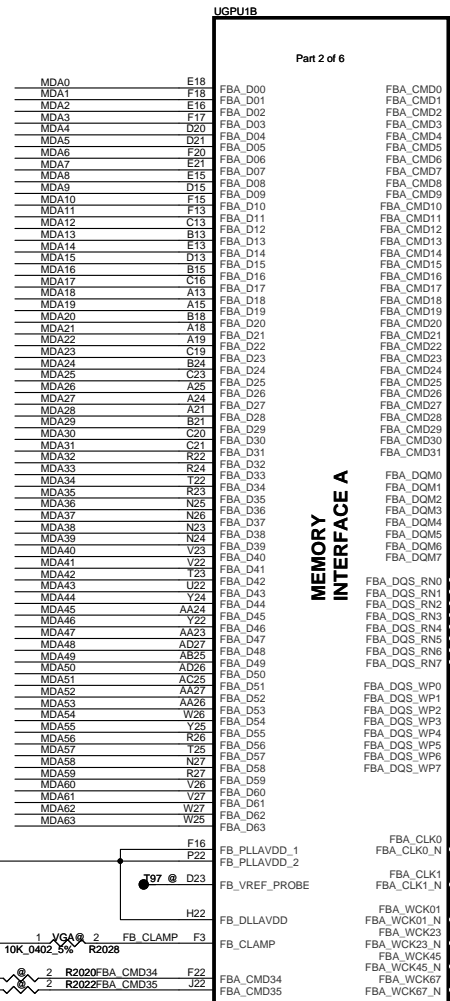
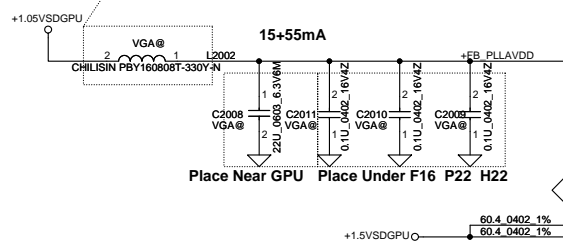
VRAM Interface



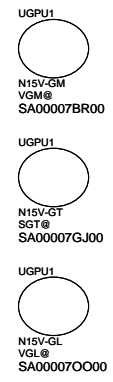
NV 15x DG-06803-V03

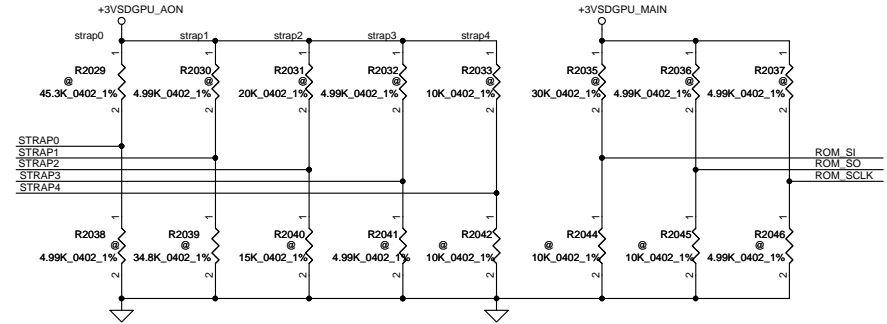
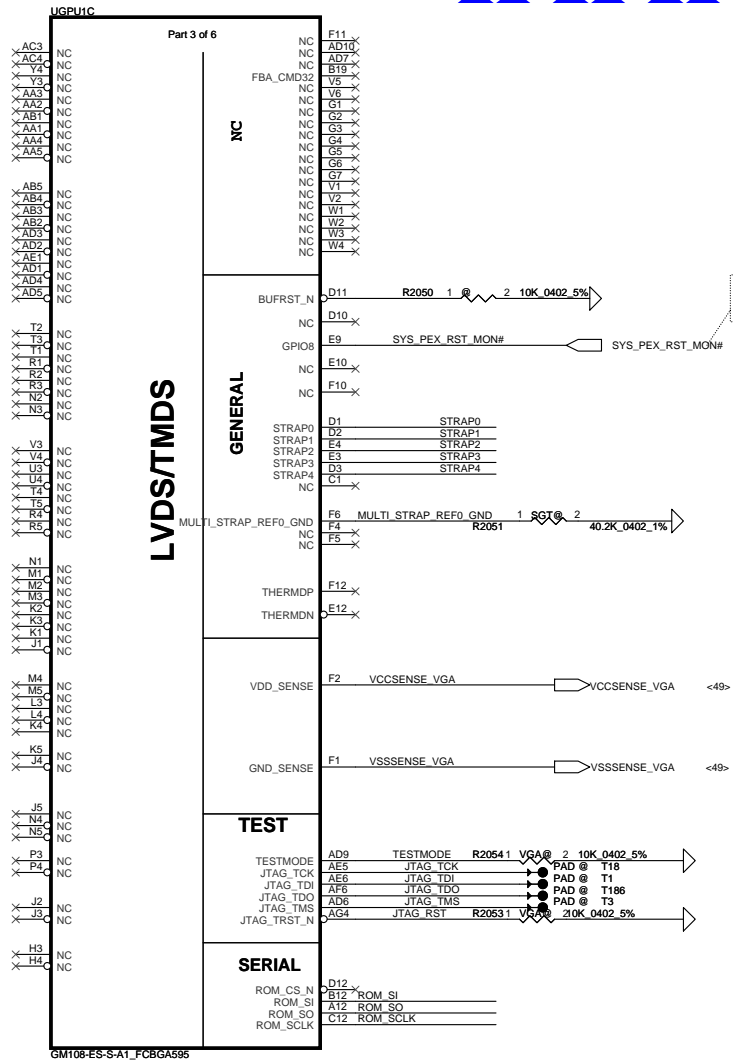
GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2
		22 µF	X5R	0805	1
		Bead Type			
		30 Ω (ESR=0.010 Ω)	0603	1	Near GPU

SM010019400 3000ma 330hm@100mhz DCR 0.05



MEMORY INTERFACE A





For N15S-GT Binary strap table

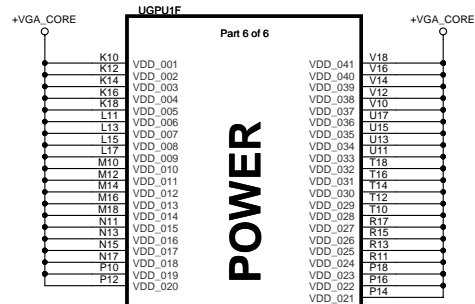
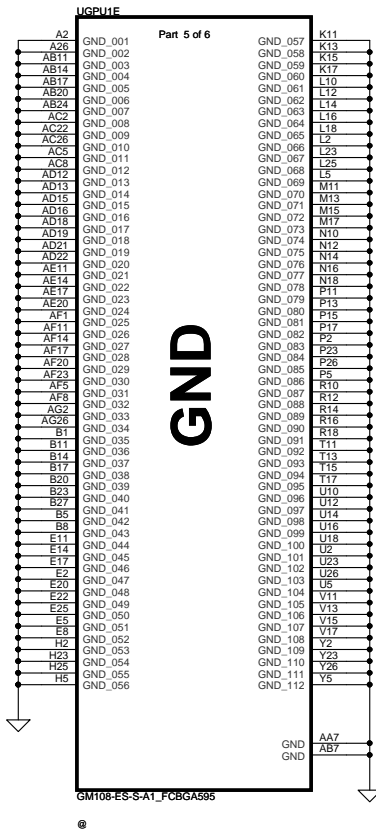
Decive ID : 0x1341

GPU	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N15S-GT	X76550BOL01	1GHz	128Mx16x4	0x7 (SA000067550) Micron MT41J128M16JT-093G-K	PU 50K	NC	NC	NC	NC	PD 45.3K	PD 4.99K	PD 4.99K
	X76550BOL02			0x8 (SA000068U90) Samsung K4W2G1646Q-BC1A						PU 4.99K		
	X76550BOL07			0x6 (SA00006H430) Hynix H5TC2G63FFR-11C						PD 34.8K		
	X76550BOL05	2GHz	256Mx16x4	0x1 (SA000077K20) Micron MT41J256M16HA-093G-E						PD 10K		
	X76550BOL06			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
	X76550BOL06			0x0 (SA00006E840) Hynix H5TC4G63AFR-11C						PD 4.99K		

For N15V-GL/GM Binary strap table

Decive ID : 0x1140

GPU	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GL N15V-GM	X76550BOL03	1GHz	128Mx16x4	0x1 (SA000067550) Micron MT41J128M16JT-093G-K	PU 10K	PD10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
	X76550BOL04			0x5 (SA000068U90) Samsung K4W2G1646E-BC1A	PU 10K	PD10K	PU 10K	PD 10K				
	X76550BOL08			0xC (SA00006H430) Hynix H5TC2G63FFR-11C	PD 10K	PD10K	PU 10K	PU 10K				
		2GHz	256Mx16x4	0xE (SA000068U90) Samsung K4W2G1646Q-BC1A	PD 10K	PU 10K	PU 10K	PU 10K				
				0x9 (SA000076P20) Samsung K4W4G1646D-BC1A	PU 10K	PD10K	PD 10K	PU 10K				
				0xD (SA000077K20) Micron MT41J256M16HA-093G-E	PU 10K	PD10K	PU 10K	PU 10K				
				0x4 (SA00006E840) Hynix H5TC4G63AFR-11C	PD 10K	PD10K	PU 10K	PD 10K				



NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint	Population	Location	Comments
GB2B-64	4.7 μ F	X65	0603	10	10	Under GPU
	1 μ F	X65	0402	4	4	Under GPU
	47 μ F	X5R	0805	1	1	Near GPU
	22 μ F	X5R	0805	1	1	Near GPU
	4.7 μ F	X5R	0805	5	5	Near GPU
	330 μ F	POS	7343	1	1	Near GPU ESR \leq 6 m Ω

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core	FB Total	1.05V Total
		—	1.5/1.35V	1.05V
N155-GM	DDR3/L	48.11	4.23	0.91
N155-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

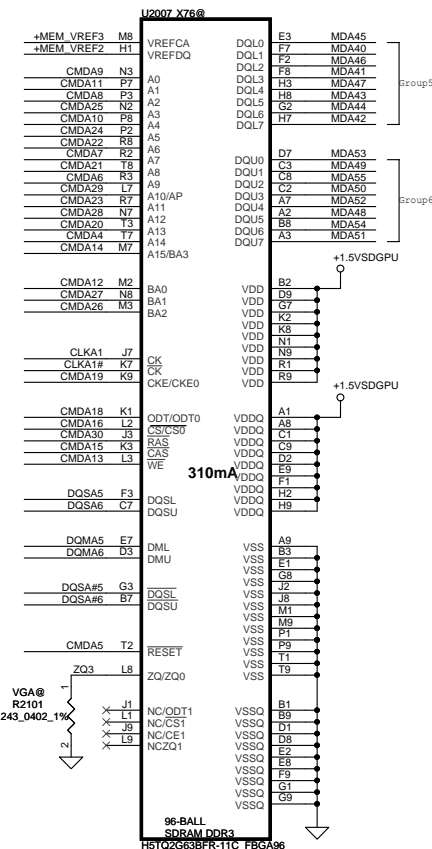
Table 6. EDP-Peak at T_J = 102 °C

Power Supply Rail	N15V-GM-S
	DDR3/L
(V)	(A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

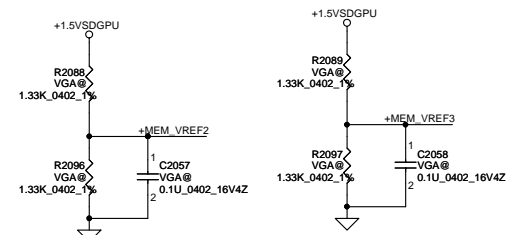
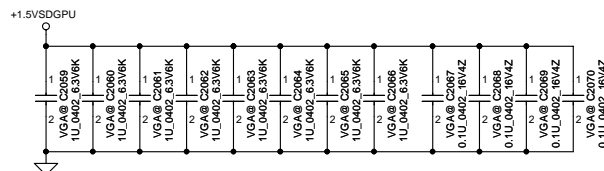
DA07075-V01

Table 7. EDP-Peak at T_J = 102 °C

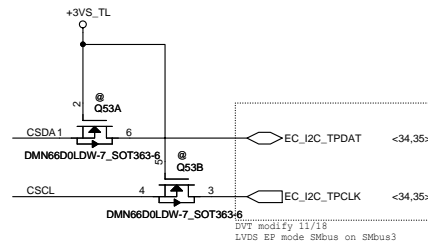
Power Supply Rail	N15V-GL
	DDR3
(V)	(A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



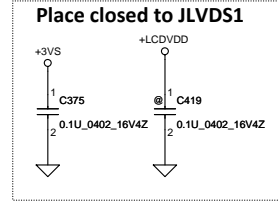
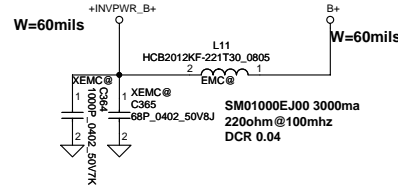
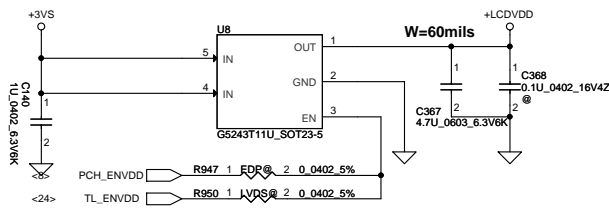
www.laptopblue.vn



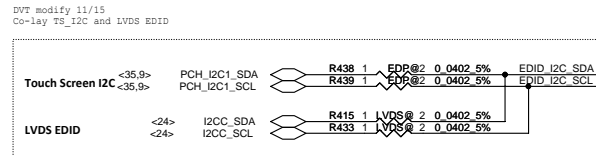
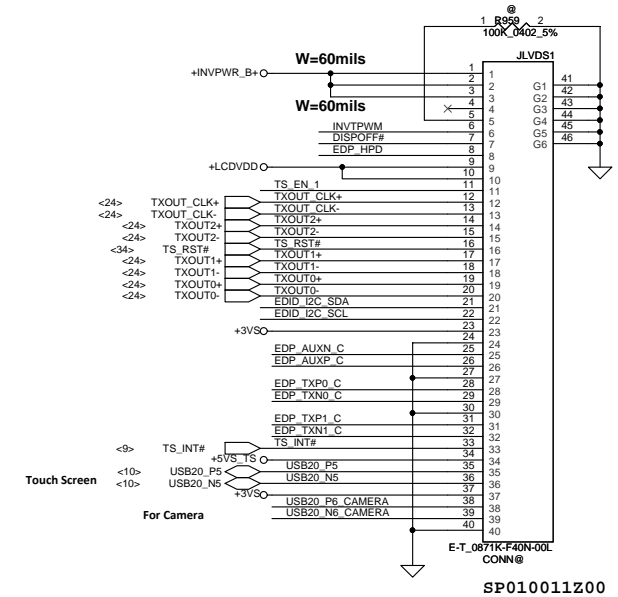
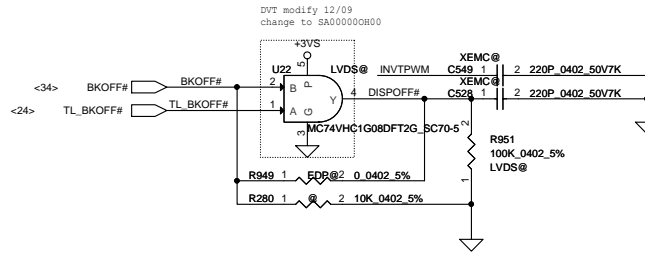
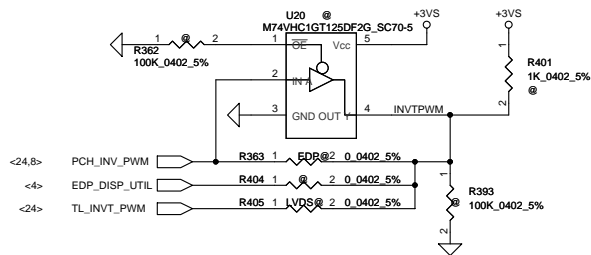
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Issued Date	2013/09/11	Deciphered Date	2013/09/24	Title		
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				Date: Wednesday, January 08, 2014		Sheet 24 of 54

EDP / LVDS conn.

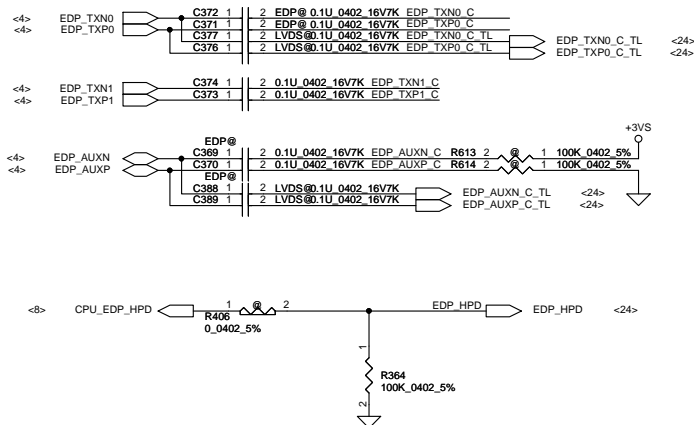
LCD POWER CIRCUIT



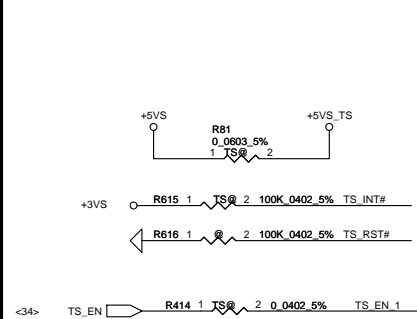
LCD/ LED PANEL Conn.



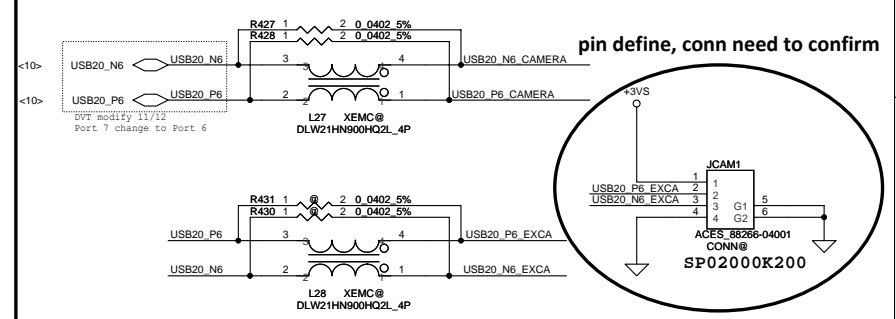
eDP



Touch Screen

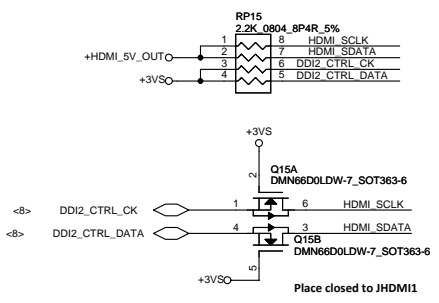
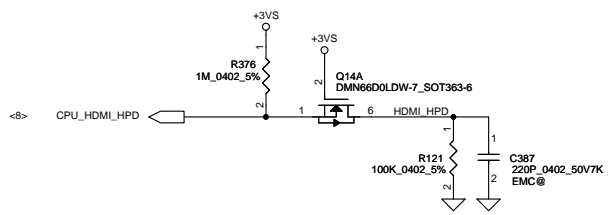
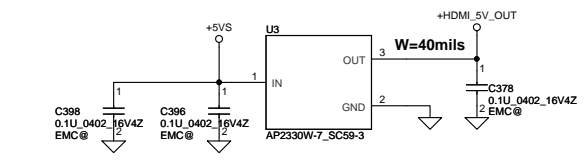


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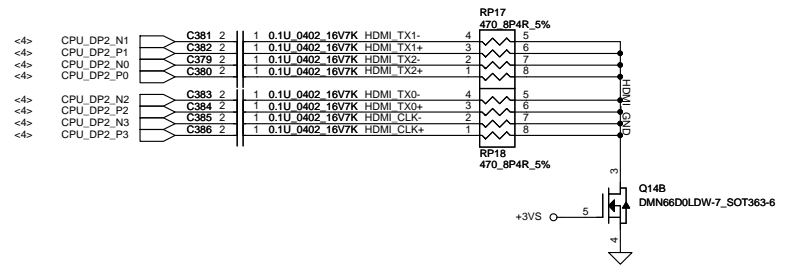


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		Z5WAH M/B LA-B162P		0.3	
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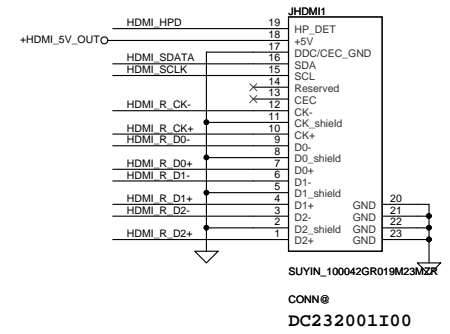
HDMI conn.



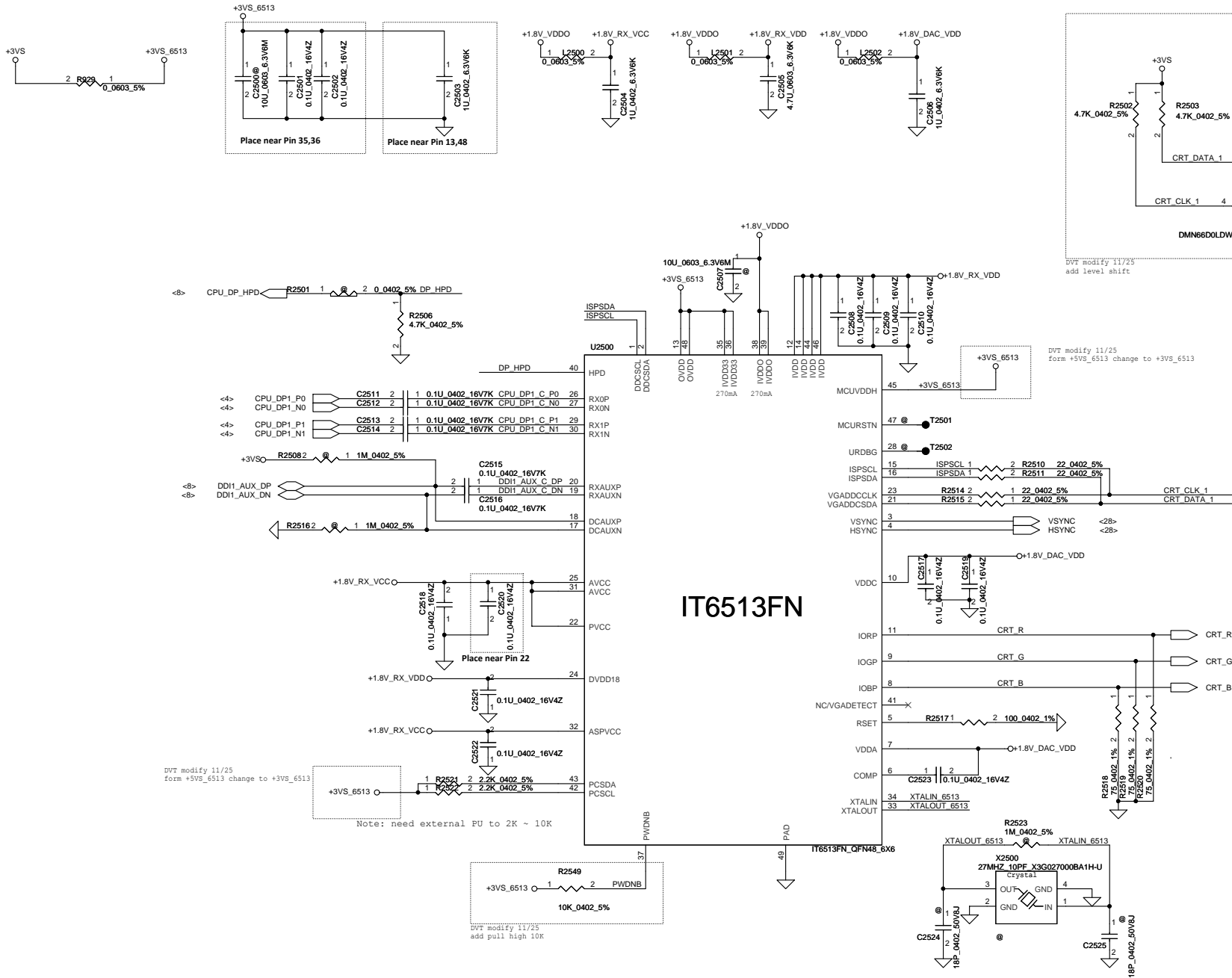
SM070001310 400ma 90ohm @100mhz DCR 0.3					
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HDMI_CLK+	R369	1	XEMC@ 2	0.0402_5%	HDMI_R_CLK+
HDMI_TX0-	R370	1	XEMC@ 2	0.0402_5%	HDMI_R_D0-
HDMI_TX0+	R371	1	XEMC@ 2	0.0402_5%	HDMI_R_D0+
HDMI_TX1-	R372	1	XEMC@ 2	0.0402_5%	HDMI_R_D1-
HDMI_TX1+	R373	1	XEMC@ 2	0.0402_5%	HDMI_R_D1+
HDMI_TX2-	R374	1	XEMC@ 2	0.0402_5%	HDMI_R_D2-
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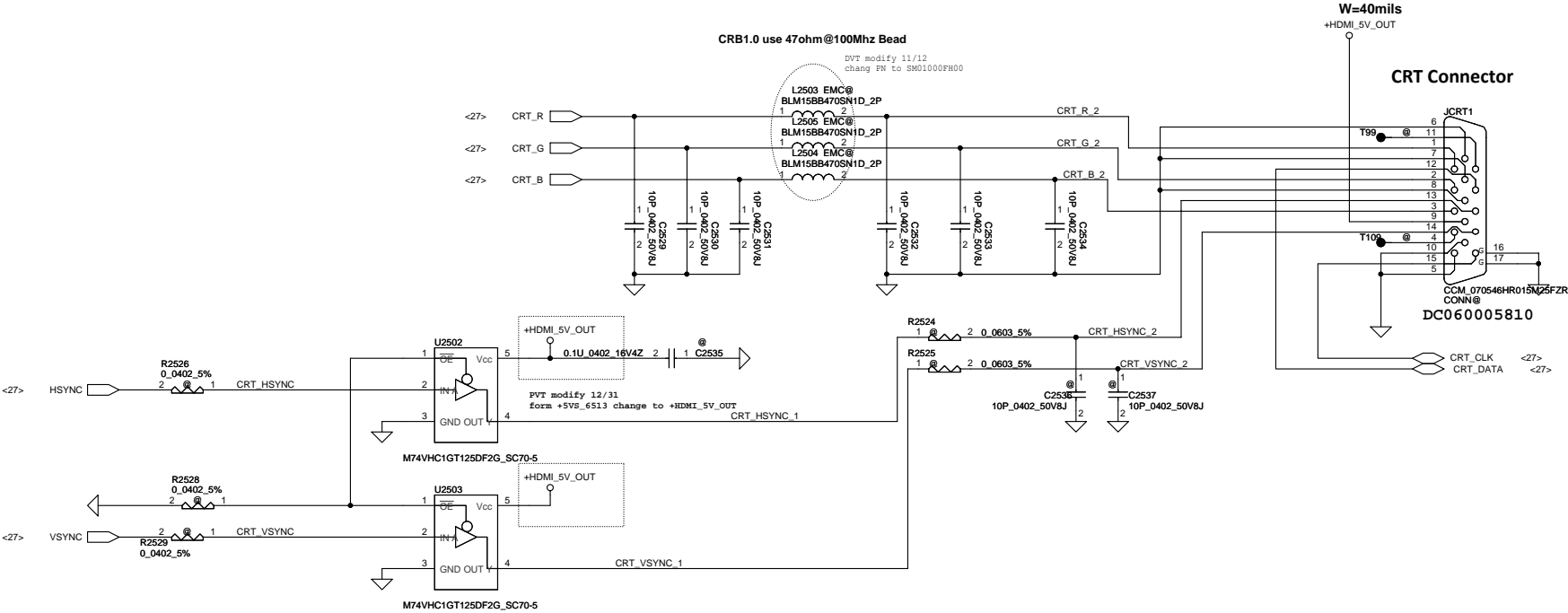
HDMI connector



DP to VGA-IT6513

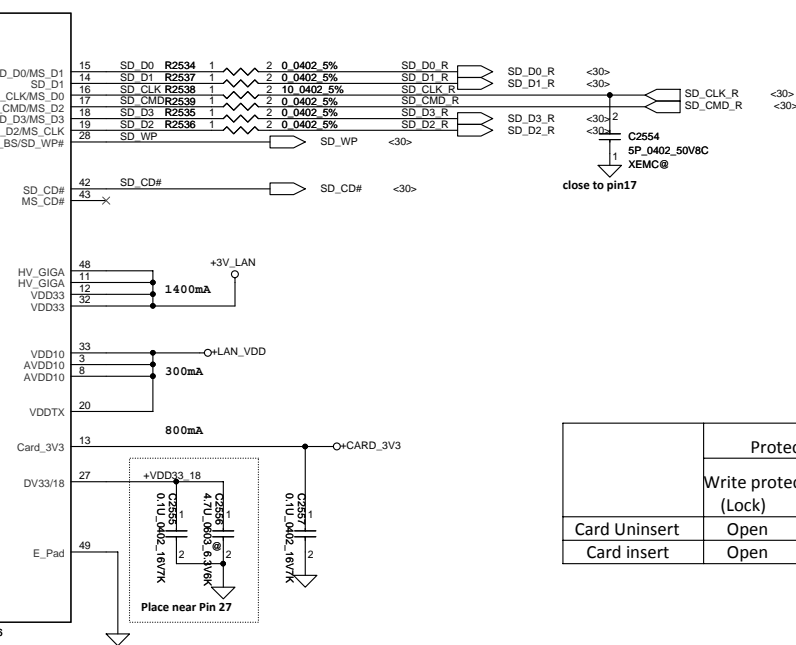
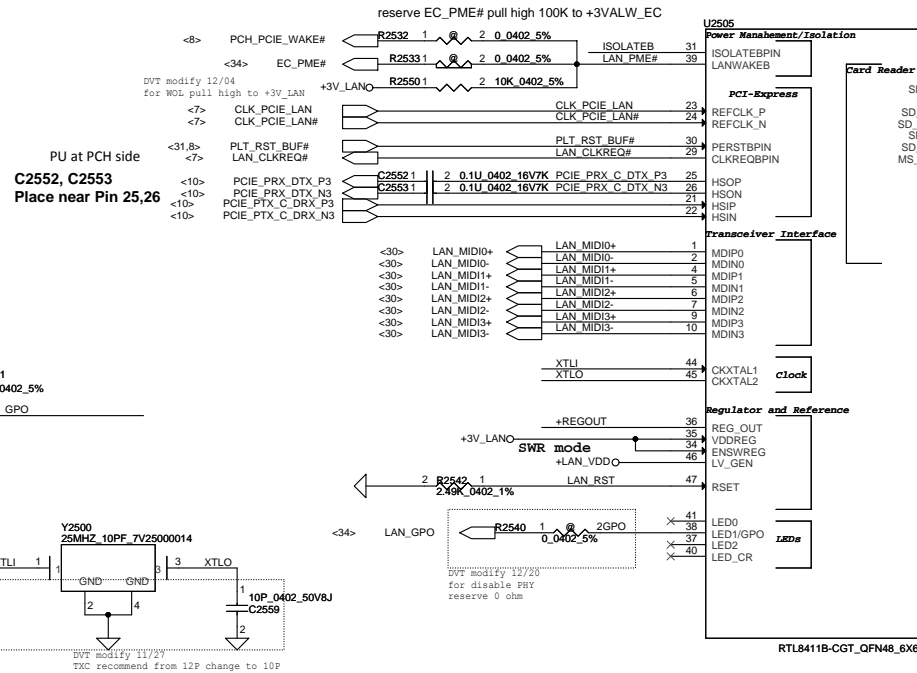
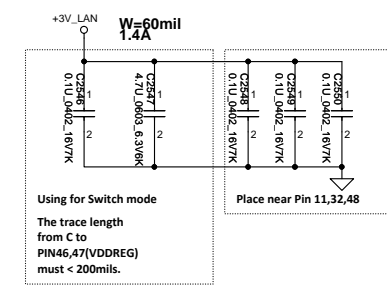
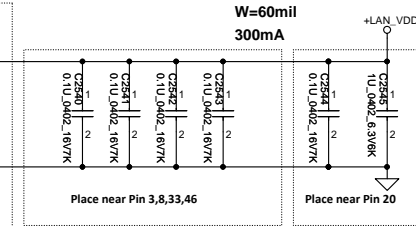
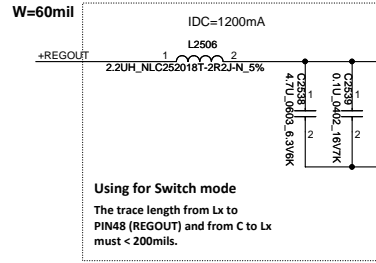
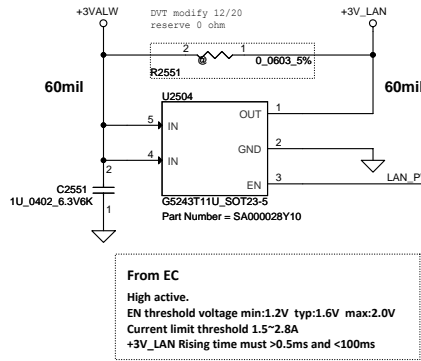


CRT conn.

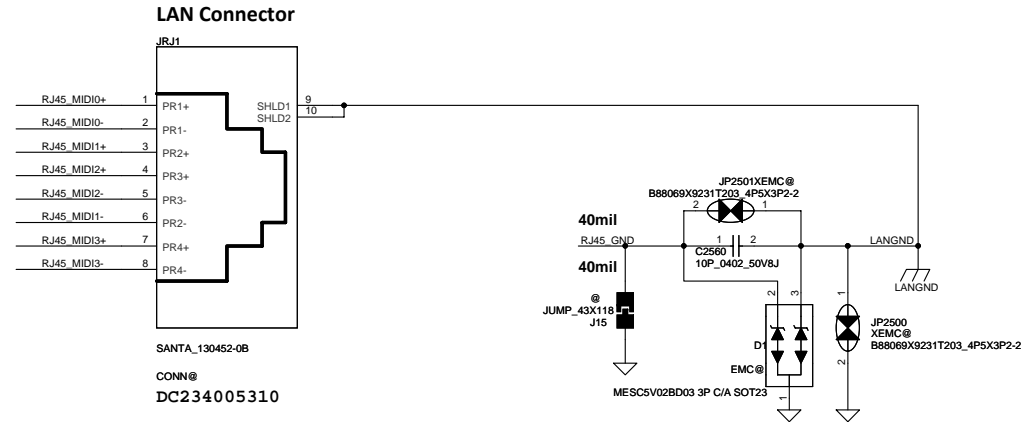


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					Date:	Wednesday, January 08, 2014	Sheet	28 of 54

LAN-RTL8411B

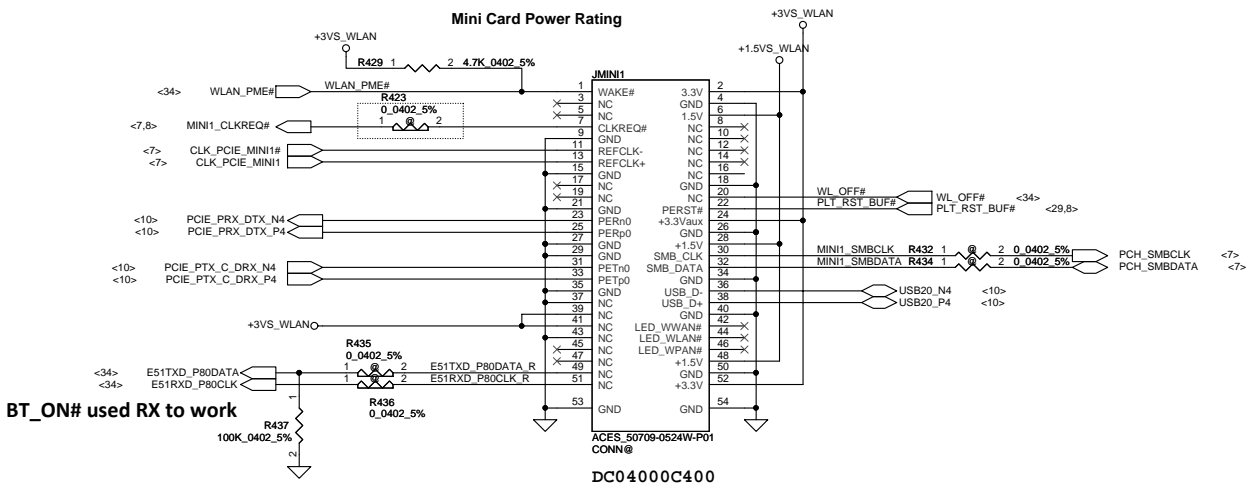
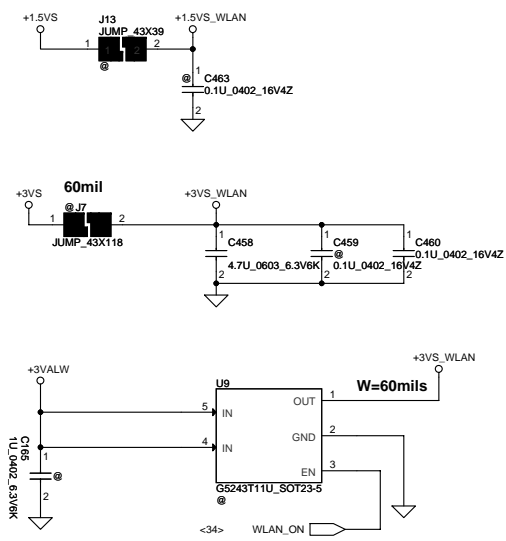


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	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

[illegible]

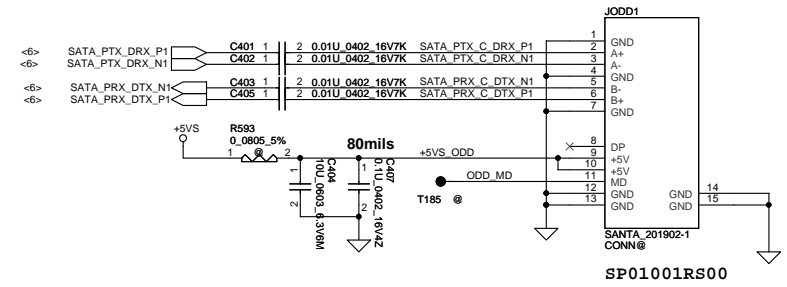
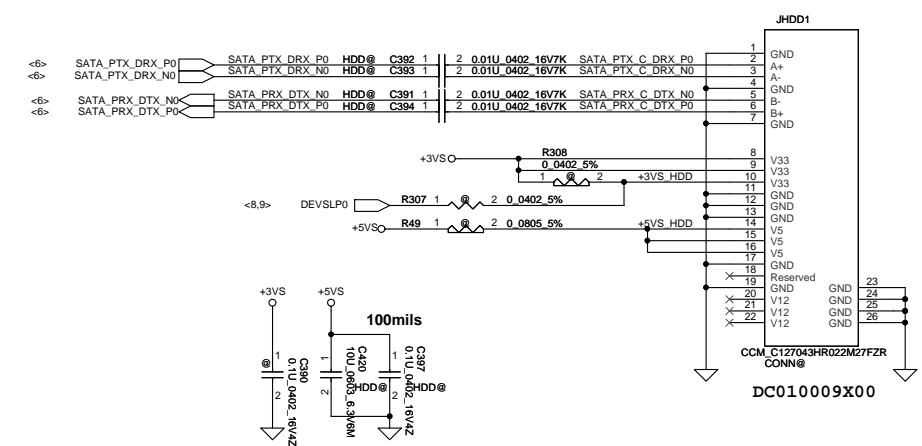
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				Date:	Wednesday, January 08, 2014	Sheet	30

Wireless LAN

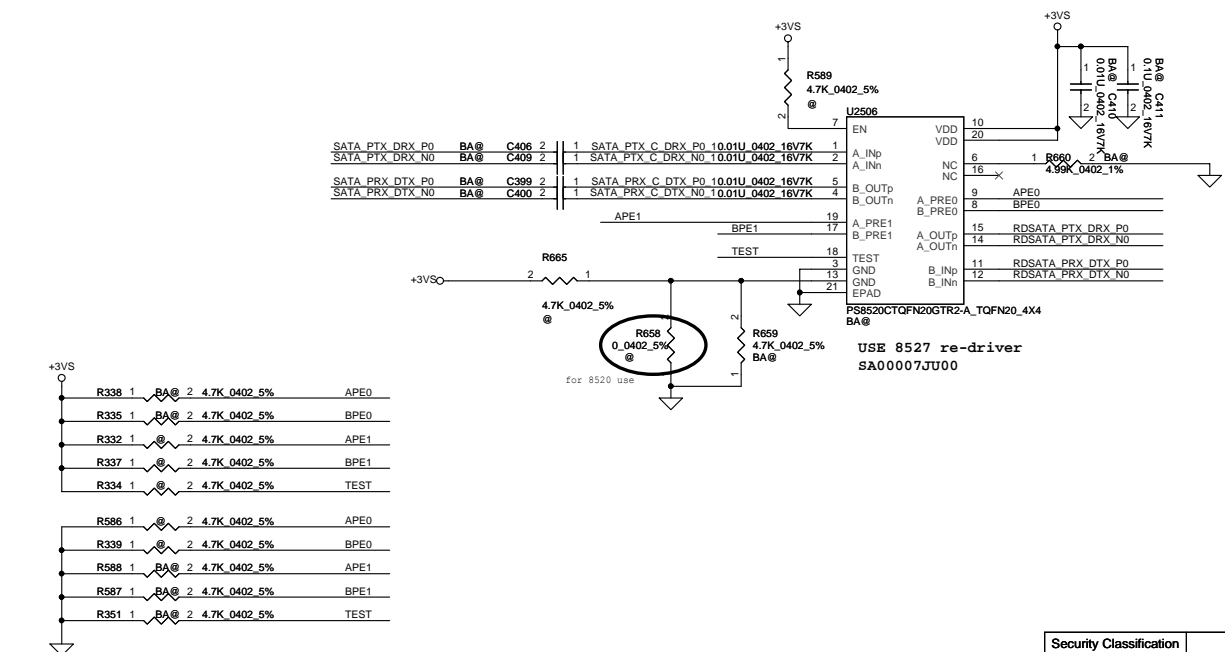


SATA HDD1 Conn.

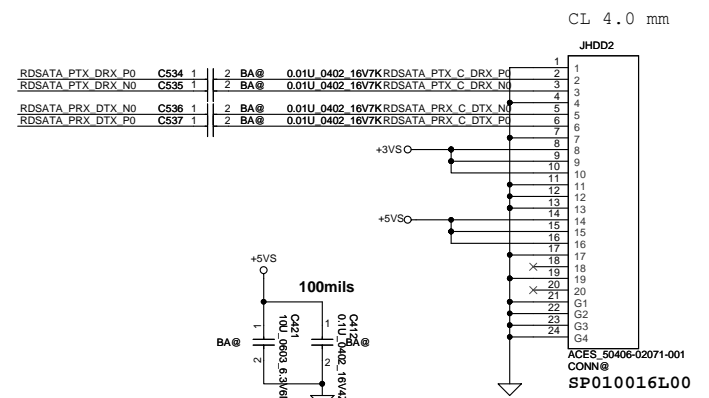
SATA ODD Conn.



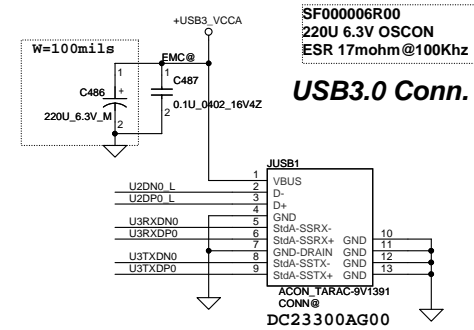
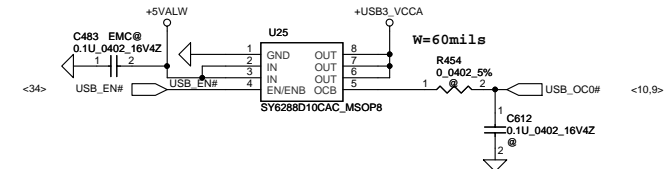
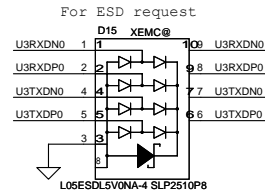
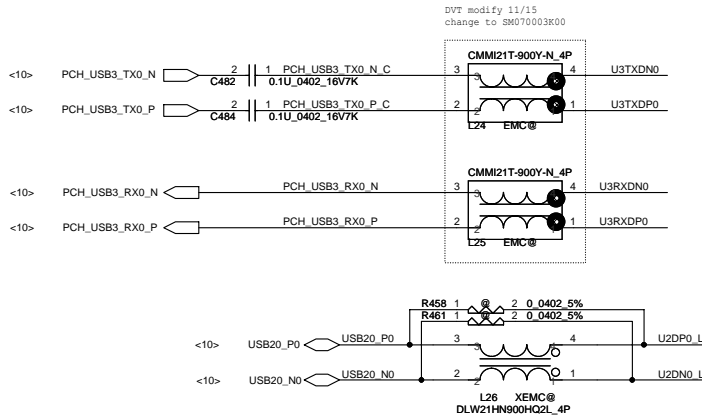
SATA Re-Driver HDD Conn. for BA50



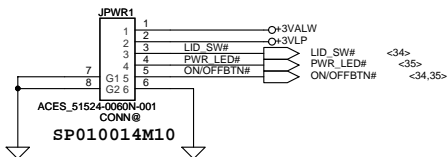
SATA HDD1 Conn.



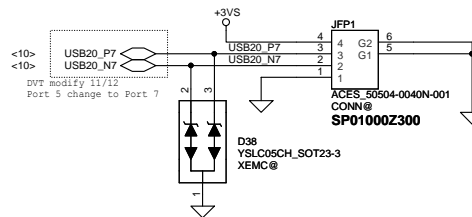
USB3.0 (Port 0)



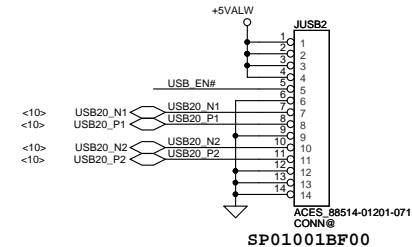
PWR/B

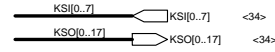
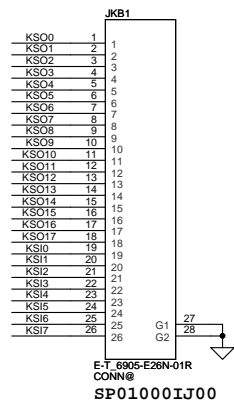


Finger Print /B for BA50

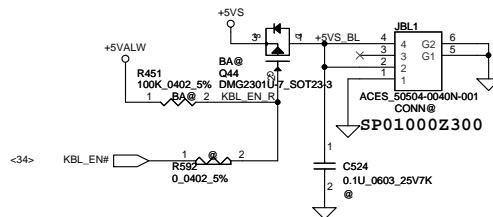


USB/B (USB Port 1, Port2)

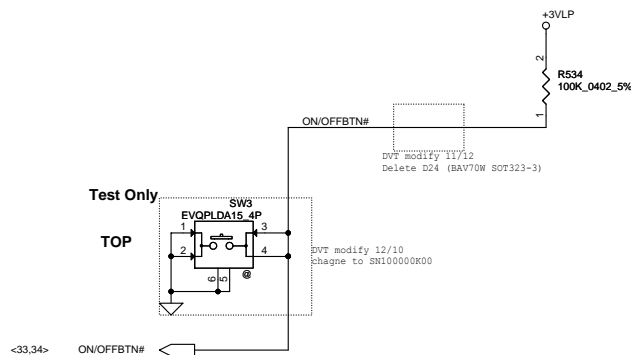


KB Conn.

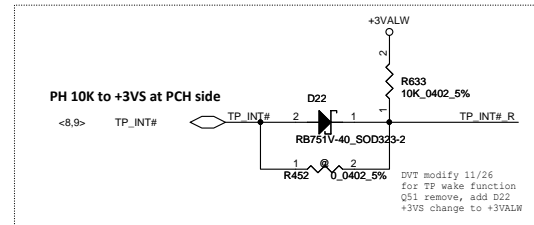
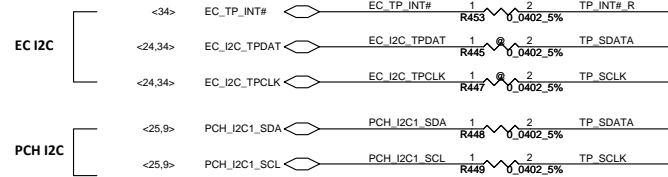
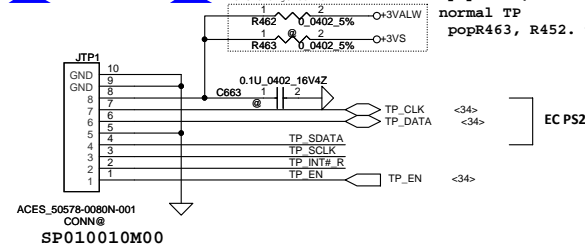
KB BackLight Conn. Reserve



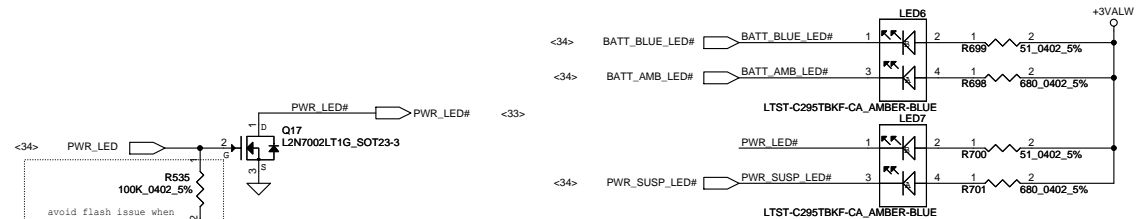
ON/OFF BTN



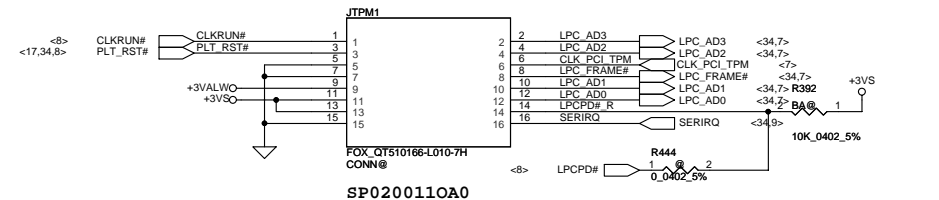
TP/B Conf.



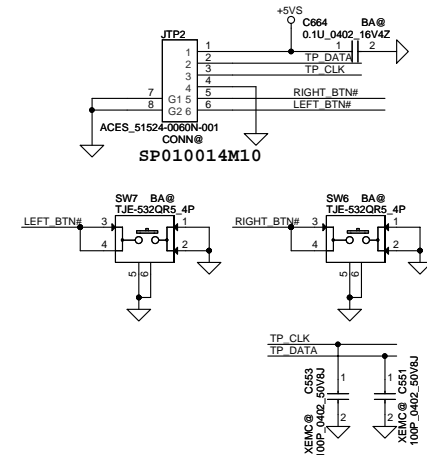
LED



TPM Board for BA50

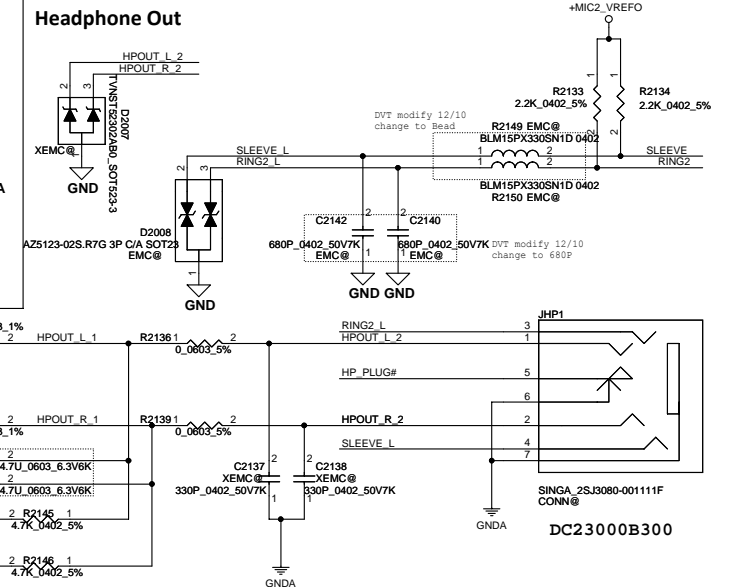
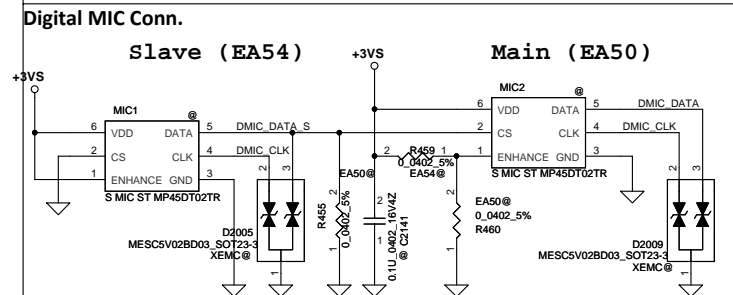
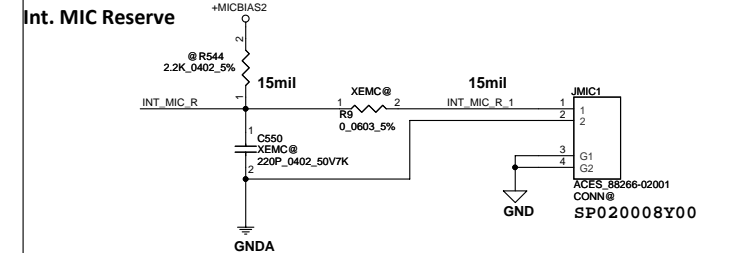
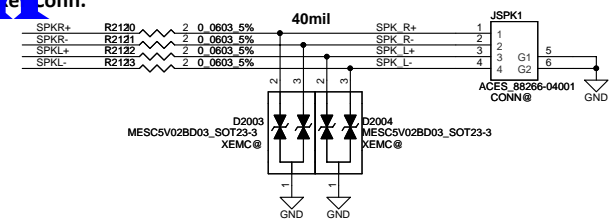
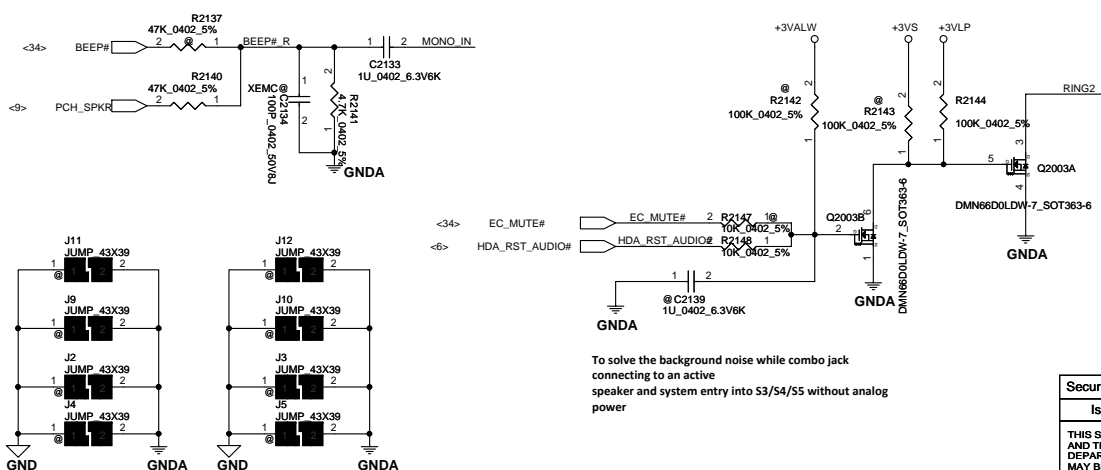
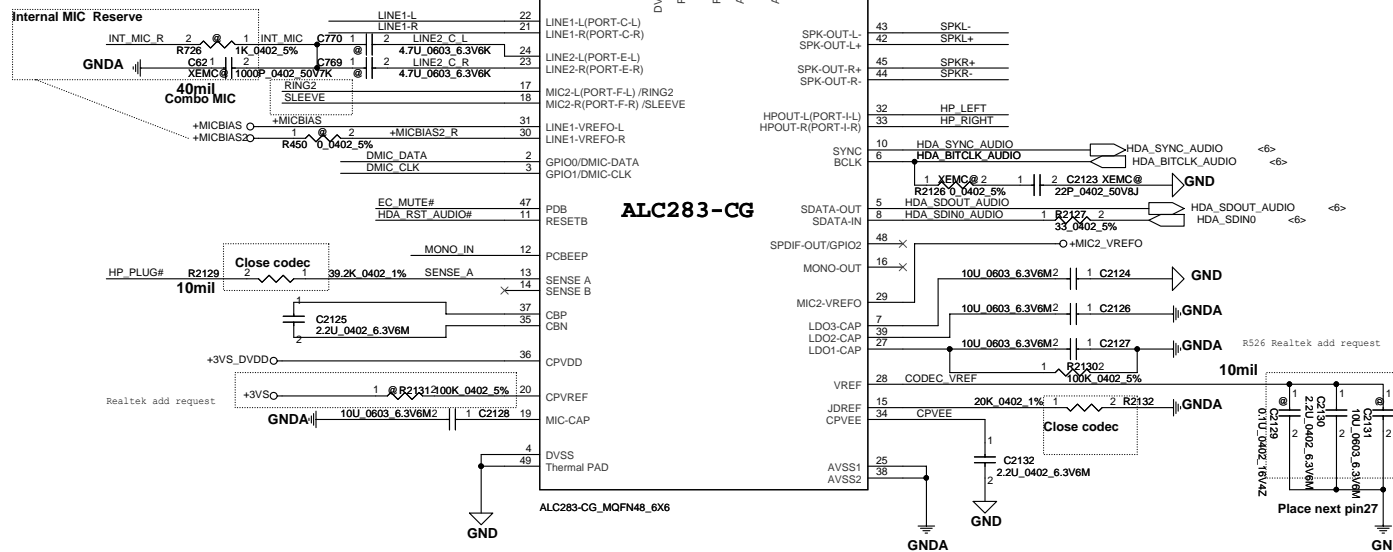
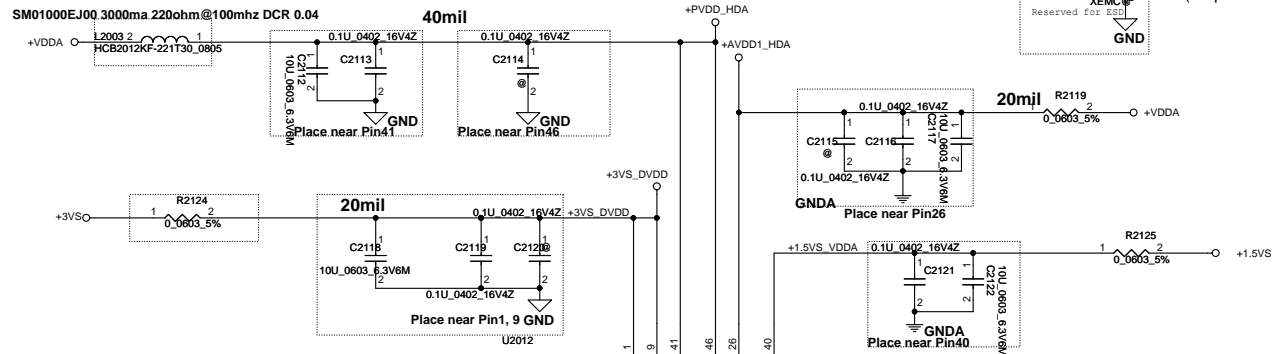


To BA50 TP/B Conn.



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Issued Date	2013/09/11	Deciphered Date	2013/09/24	Title	KB & TP & TPM Connector & LED	
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				Customer	Z5WAH M/B LA-B162P	0.3
Date:				Wednesday, January 08, 2014	Sheet	35 of 54

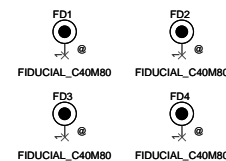
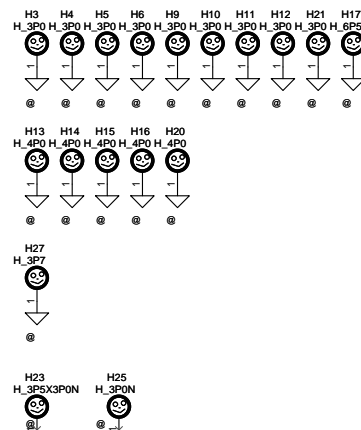
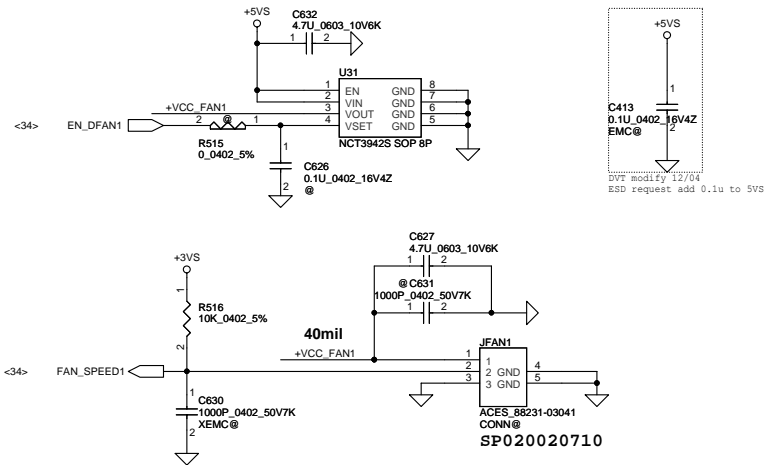
HD Audio Codec



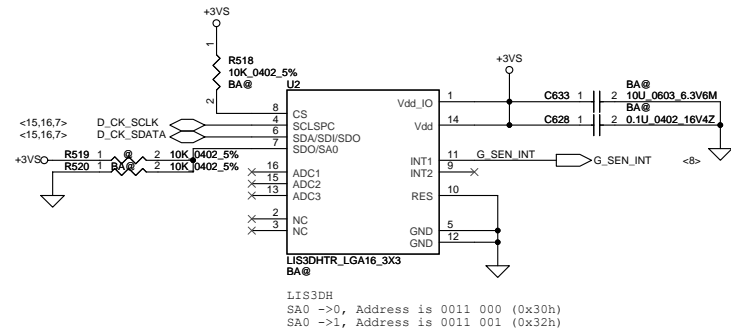
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/09/11	Deciphered Date	2013/09/24	Title	HD Audio Codec ALC283
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				Customer Document Number	0.3
Date: Wednesday, January 08, 2014				Sheet	36 of 54
				Z5WAH M/B LA-B162P	

FAN1 Conn

Screw Hole

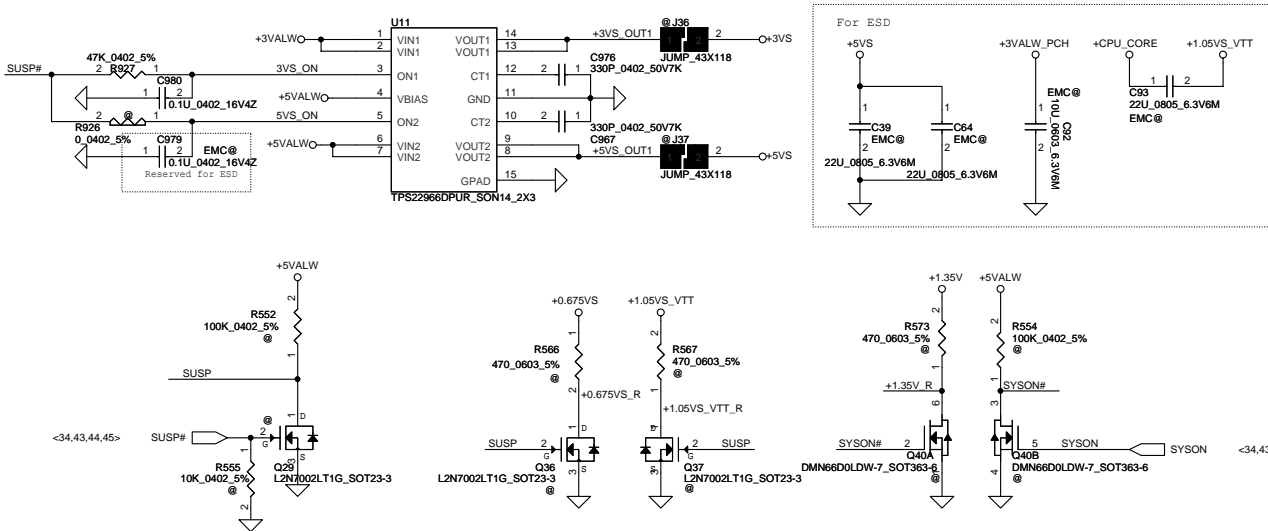


G-Sensor for BA50

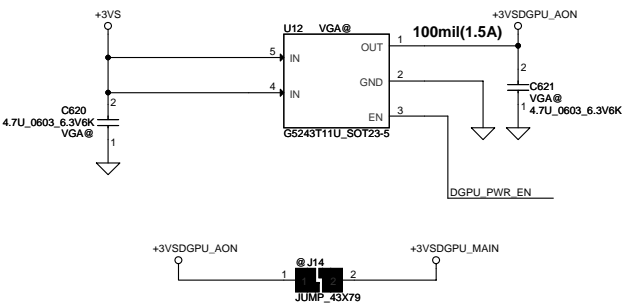


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/09/11	Deciphered Date	2013/09/24	Title	FAN & Screw Hole & G-Sensor
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				Customer	0.3
				Date	Wednesday, January 08, 2014
				Sheet	37 of 54

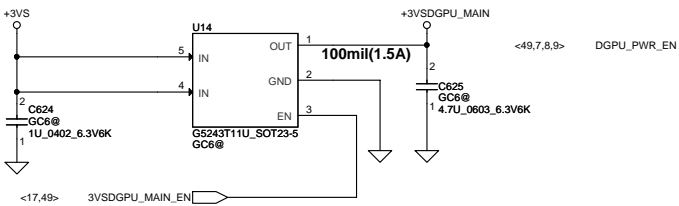
DC & VGA Interface



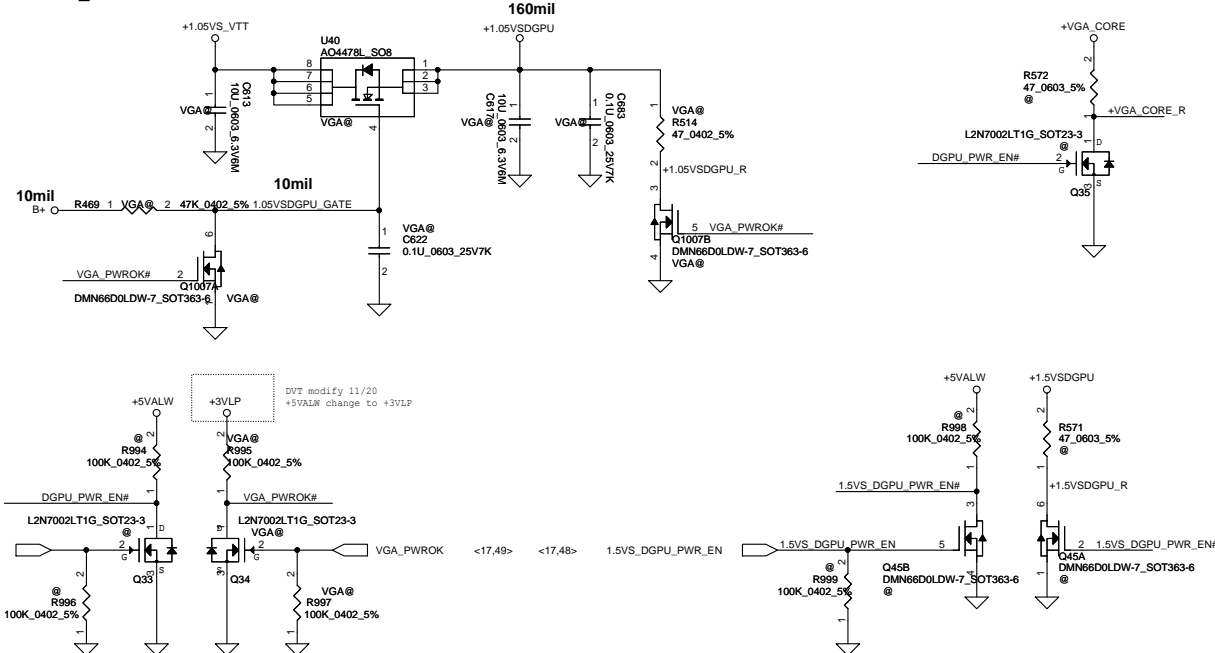
+3VS to +3VSDGPU_AON for GPU



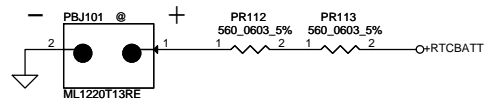
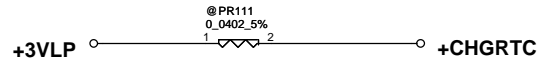
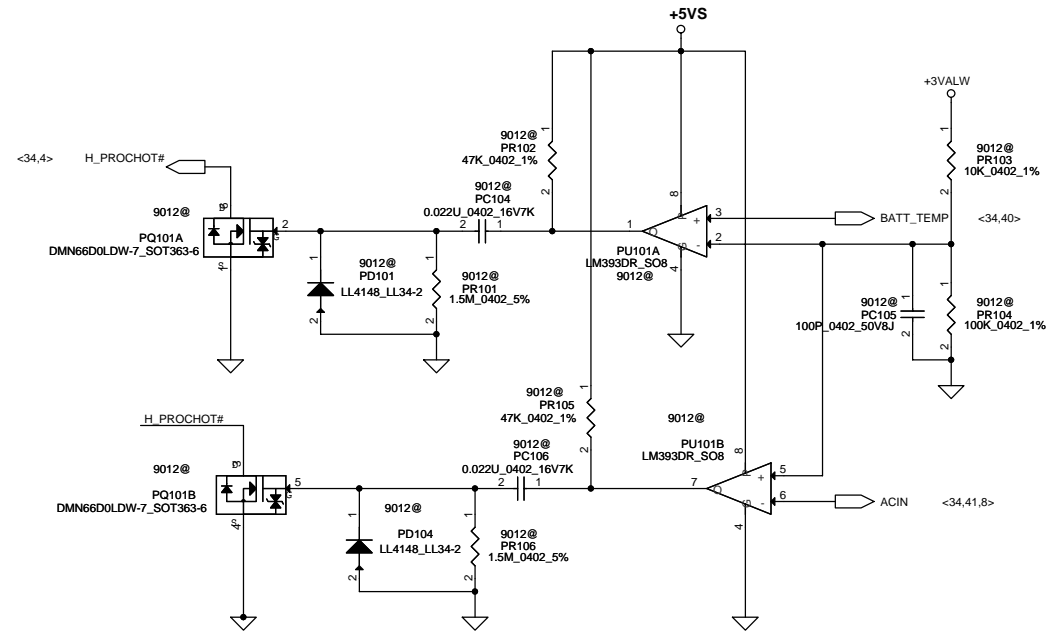
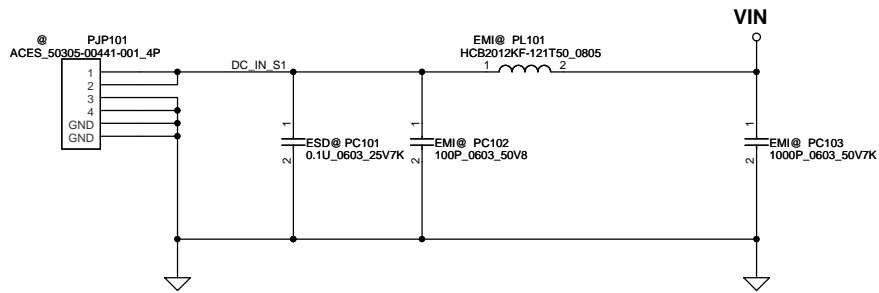
+3VS to +3VSDGPU_MAIN for GC6-2.0



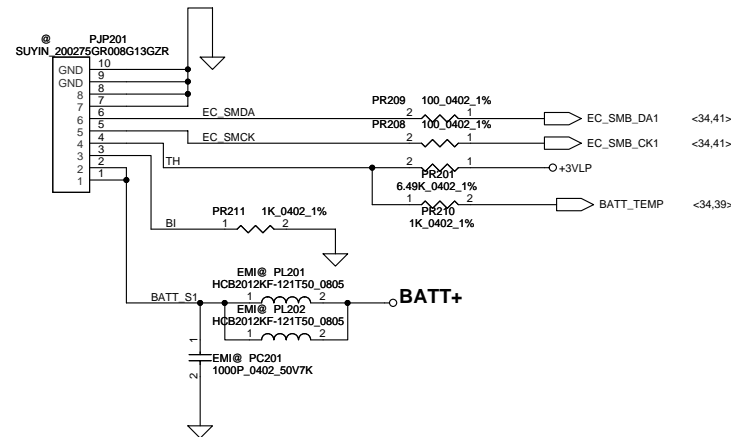
+1.05VS_VTT to +1.05VSDGPU



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Issued Date		Deciphered Date		DC Interface	
2013/09/11		2013/09/24		Customer	
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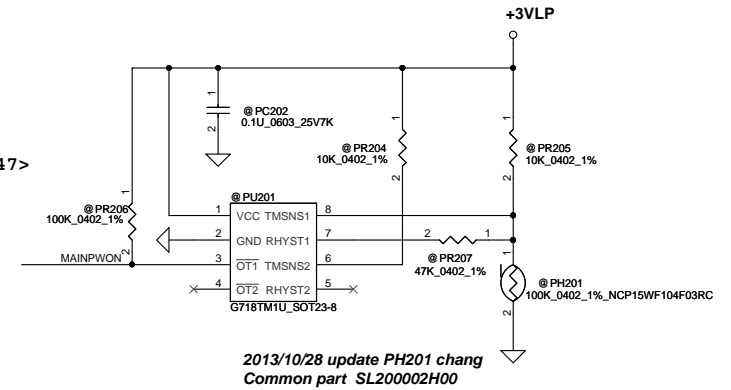
---Battery_pin define---

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TS
PIN6 B/I
PIN7 Batt+
PIN8 Batt+

---Battery Con_pin define---

PIN8 GND
PIN7 GND
PIN6 SMD
PIN5 SMC
PIN4 TS
PIN3 B/I
PIN2 Batt+
PIN1 Batt+

<45,47>



2013/10/28 update PH201 chang
Common part SL200002H00

	For KB9012 OTP	For KB9022 OTP
92	1.2V	1.0V
56	1.2V	1.0V
PR216	22.6K ohm	32.4K ohm
PR227	26.1K ohm	30K ohm

2013/10/14 update

For KB9022 sense 20ms	Active	Recovery
40W	52W, 0.51V	40W, 0.51V
65W	84.5W, 0.82V	65W, 0.82V

PH201 under CPU botten side :

CPU thermal protection at 92 degree C (shutdown)

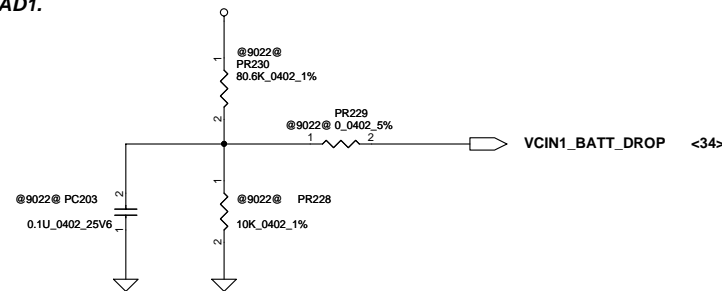
Recovery at 56 degree C +EC_VCCA

2013/10/02

Add for ENE9022 Battery Voltage drop detection. B+
Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.

B+=9V



2013/10/28 update PH202 chang
Common part SL200002H00

For 65W adapter==>action 70W , Recovery 54W

For 40W adapter==>action 52W , Recovery 40W

<34>

ECAGND

ADP_I <34,41>

VCIN1_PROCHOT <34>

H_PROCHOT#_EC <34>

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Issued Date	2012/07/10	Deciphered Date	2013/09/24	Compal Electronics, Inc.
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Date:	Wednesday, January 08, 2014	Sheet	40	of 54

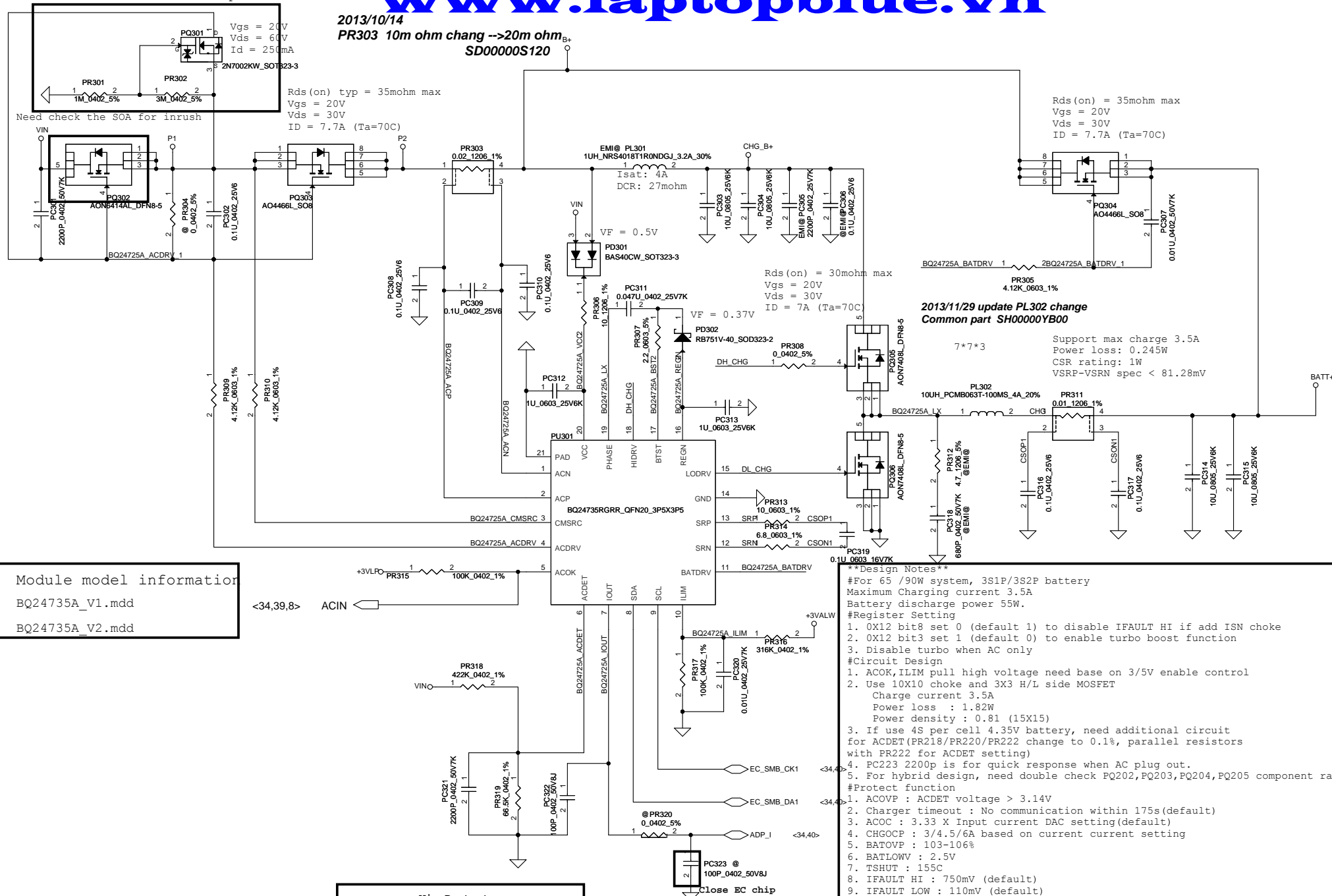
Protection for reverse input

2013/10/14

PR303 10m ohm chang -->20m ohm
SD00000S120

Rds(on) typ = 35mohm max
Vgs = 20V
Vds = 30V
ID = 7.7A (Ta=70C)

Need check the SOA for inrush



Module model information

BQ24735A_V1.mdd

BQ24735A_V2.mdd

<34,39,8>

ACIN

VINO

PR318

422K_0402_1%

PC321

2200P_0402_50V7K

PC319

66.5K_0402_1%

PC322

100P_0402_50V6J

PC320

100P_0402_50V6J

PC323

100P_0402_50V8J

PC324

100P_0402_50V8J

PC325

100P_0402_50V8J

PC326

100P_0402_50V8J

PC327

100P_0402_50V8J

PC328

100P_0402_50V8J

PC329

100P_0402_50V8J

PC330

100P_0402_50V8J

Vin Detector

Min. Typ Max.

L-->H 17.16V 17.63V 18.12V

H-->L 16.76V 17.22V 17.70V

VILIM = 20*ILIM*Rsr

ILIM = 3.3*100/(100+107)/20/0.02

= 3.986 A

PC323 @

100P_0402_50V8J

Close EC chip

Design Notes

#For 65 /90W system, 3S1P/3S2P battery

Maximum Charging current 3.5A

Battery discharge power 55W.

#Register Setting

1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke

2. 0X12 bit3 set 1 (default 0) to enable turbo boost function

3. Disable turbo when AC only

#Circuit Design

1. ACOK,ILIM pull high voltage need base on 3/5V enable control

2. Use 10X10 choke and 3X3 H/L side MOSFET

Charge current 3.5A

Power loss : 1.82W

Power density : 0.81 (15X15)

3. If use 4S per cell 4.35V battery, need additional circuit

for ACDET (PR218/PR220/PR222 change to 0.1%, parallel resistors

with PR222 for ACDET setting)

4. PC223 2200p is for quick response when AC plug out.

5. For hybrid design, need double check PQ202,PQ203,PQ204,PQ205 component rating

#Protect function

1. AC0VP : ACDET voltage > 3.14V

2. Charger timeout : No communication within 175s(default)

3. AC0C : 3.33 X Input current DAC setting(default)

4. CHG0CP : 3/4.5/6A based on current current setting

5. BAT0VP : 103-106%

6. BATLOWV : 2.5V

7. TSHUT : 155C

8. IFAULT HI : 750mV (default)

9. IFAULT LOW : 110mV (default)

Security Classification

Compal Secret Data

Issued Date

2014/07/02

Deciphered Date

2013/09/24

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Compal Electronics, Inc.

CHARGER

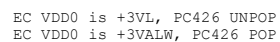
Document Number

Common Circuit

Rev

0.3

Date: Wednesday, January 08, 2014 Sheet 41 of 54

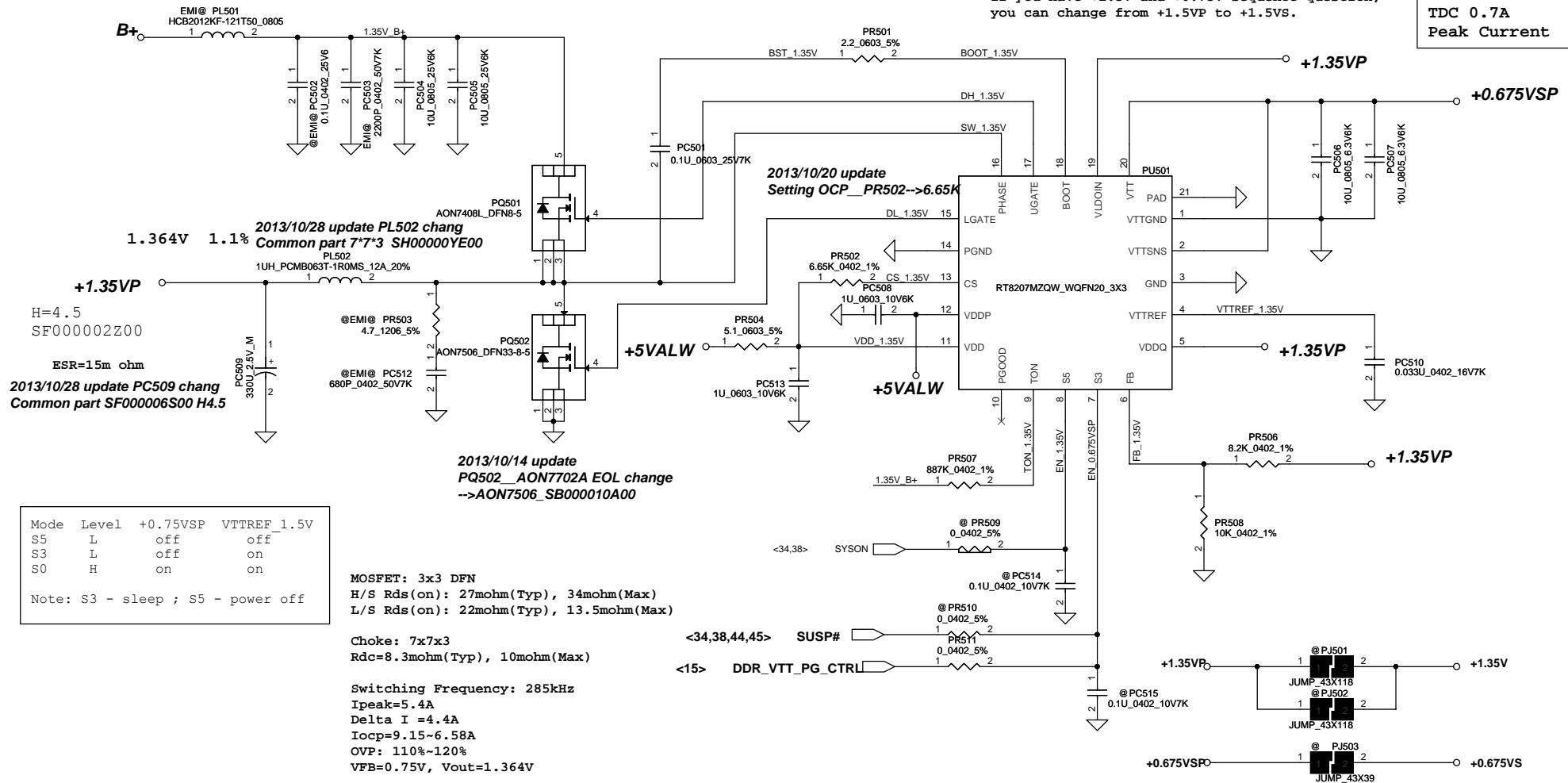
Rev
0,3

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

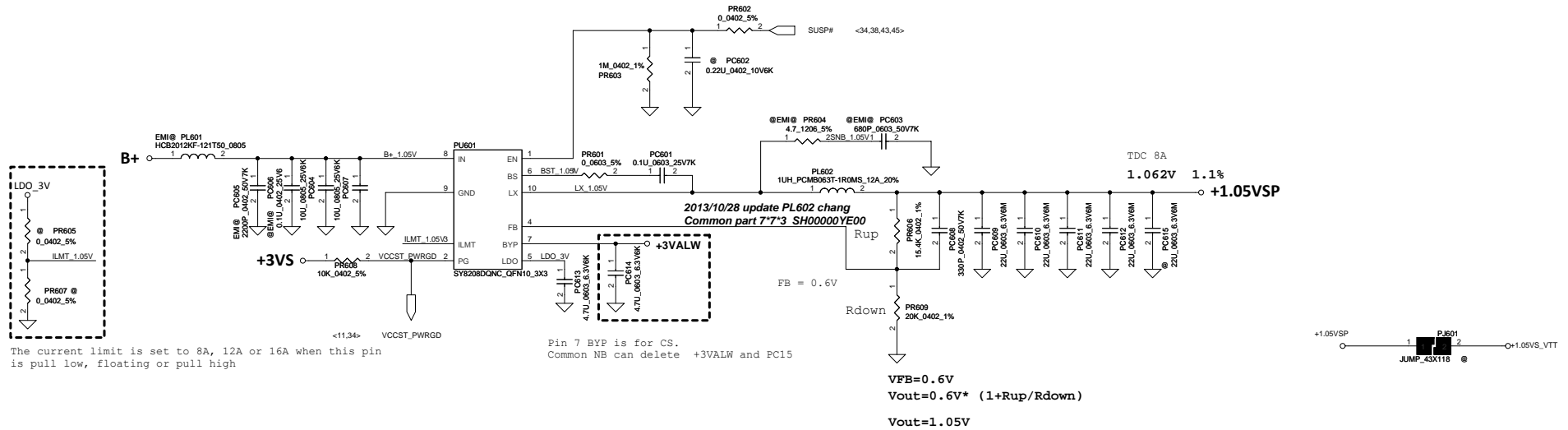
Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

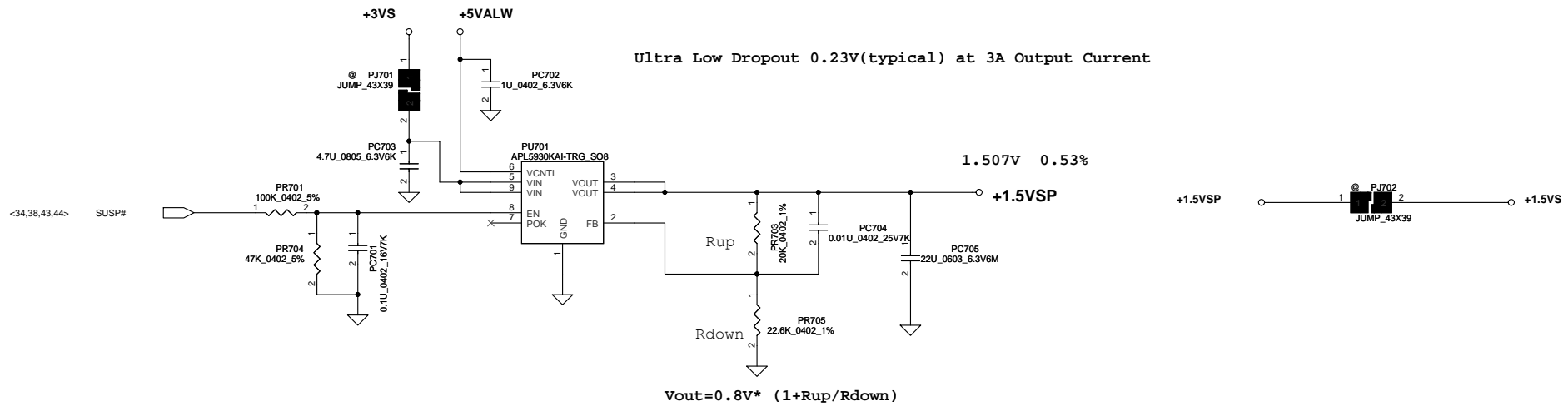
0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



Module model information
SY8208D_V1.mdd

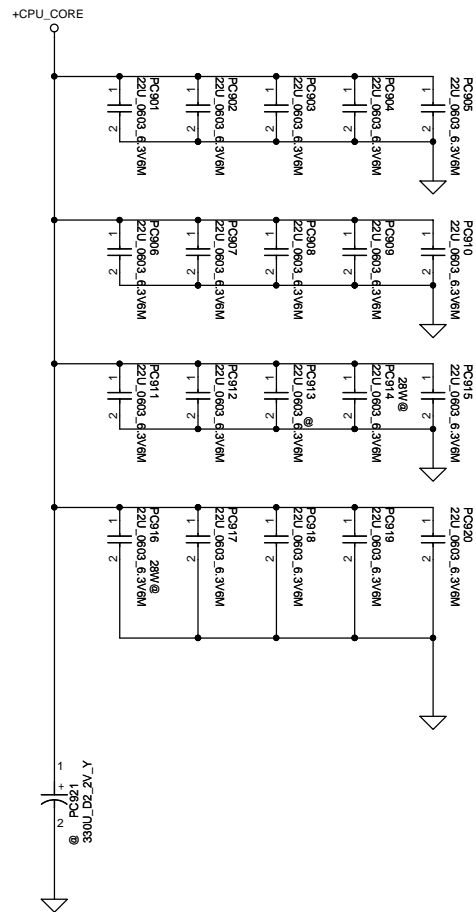
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2





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					Custom
					Date: Wednesday, January 08, 2014
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**PWR Rule
需確認最新SPEC.
Modify 8/6.**

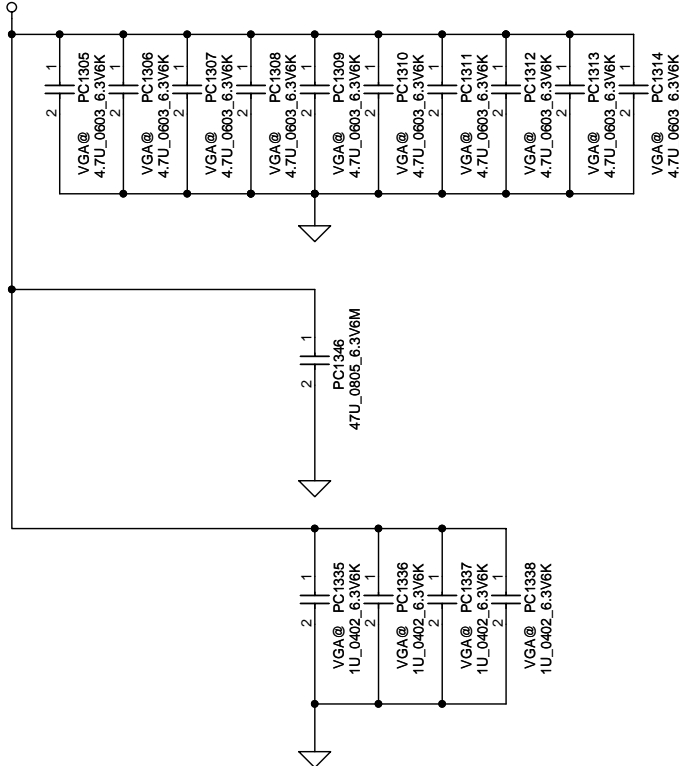


```
30 X 22uF 0805
2012/10/23
check the output cap Qty!!!
2012/10/24
23 pcs 22uF and reserve 7 pcs
2013/01/14
22uF*17      unpop:22uF*3
```

20130828
15W: 22uF*14
28W: 22uF*16

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Issued Date	2012/07/10	Deciphered Date	2013/09/24	Title CPU CORE CAP		
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				Custom		0.3
				Date:	Wednesday, January 08, 2014	1 Sheet 47 of 54

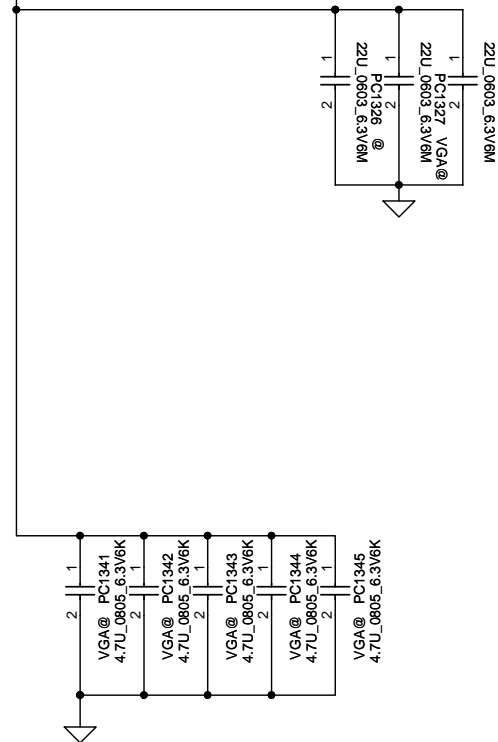
+VGA_CORE Under VGA Core



+VGA_CORE

+VGA_CORE

Near VGA Core



N15x 2013/12/10
Under
4.7uF_0603_10pcs
1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0603_1pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/17
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0603_9pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/07
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_9pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/02
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_14pcs
4.7uF_0805_5pcs

N14x
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2013/09/24	Title	
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				Custom	0.3
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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	design update		P42 P44 P44 P46 P41	Add unpop PC428 PC427,22U_0603_6.3V6M_SE00000M000 Add unpop PC615,22U_0603_6.3V6M_SE00000M000 PC609 PC610,SE00000PL00 change to 0603_6.3V6M_SE00000M000 PL801 PC807,Swap positions. PL302,10uH_10104_SH000005Z80 change to 10uH_773_SH00000YB00	11/29	EVT
2	design update	Update Common part	P42	PR410_R-short change to PD401_SCS00000Z00	12/09	EVT
3	design update	VGA 29*29 change to 23*23	P50	ADD 1pcs PC1346_47U_0805_6.3V6M_SE00000PL00 Del 5pcs PC1315~PC1319 4.7U_0603_6.3V6K_SE107475K80 Del 4pcs PC1331~PC1334 1U_0402_6.3V6K_SE000000K80 Del 6pcs PC1322~1325&PC1329~1330_22U_0603_6.3V6M_SE00000M000	12/10	EVT
4	design update	VGA 29*29 change to 23*23 (GM config SPEC change)		PR1206_39K_0402_1% change to 27K_0402_1%(GL->GM) PR1204_30K_0402_1% change to 7.5K_0402_1%(GL->GM) PR1205_3K_0402_1% change to 0_0402_5%(GL->GM) PR1209_24K_0402_1% change to 6.2K_0402_1%(GL->GM) PR1212_3K_0402_1% change to 1.74K_0402_1%(GL->GM) PC1209_1800P_0402_50V7K change to 5600P_0402_50V7K(GL->GM)	12/12	EVT
5	design update	CPU Transient Test & Update Common part		PR820_274_0402_SD00000EI80 change to 316_0402_SD000003480 PR814_2K_0402_1%_SD034200180 change to unpop PC814_330P_0402_50V7K_SE074331K80 change to unpop PR813_5.9K_0402_SD034590180 change to 1.91K_0402_SD000009080 PR807_95.3K_0402_SD034953280 change to 121K_0402_SD034121380 PR817_Unpop change to 4.99M_0402_SD00000VO00 PL1202 PL1203_SH000000200_7*7*4 change to Common part SH000011H00 PL802_SH00000U300 change to Common part SH000011P00 PC909 PC918 PC919 22U_0603_SE00000M000 SMT PC914 22U_0603_SE00000M000,SMT change to 28W@ PC913 22U_0603_SE00000M000 ,SMT change to @ PR227_30.9K_0402_1%_SD034309280 change to 30K_0402_1%_SD034300280 PR1210 1K_0402_5%_SD028100180change to unpop PR1226 0_0402_5%_SD028000080change to SMT	12/12	EVT

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Issued Date	2012/07/10	Deciphered Date	2013/09/24	Title	PIR (PWR)	
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				0.3	Custom	0.3
				Date:	Wednesday, January 08, 2014	Sheet 51 of 54

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	Module Design	Module Design change 3/5V solution	3/5V	Un-pop PR1	11/13	DVT
2						
12						
13						
14						
15						
16						
17						

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/07/10	Deciphered Date	2013/09/24	Title	PIR (PWR)	
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				Custom		0.3
				Date:	Wednesday, January 08, 2014	Sheet 52 of 54

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	material update		P28	L2503/2504/2505 Change P/N from SM01000GA00 to SM01000FH00	11/12	DVT
2	material update		P34	L31/L32 Change P/N from SM010030010 to SM010009U00	11/12	DVT
3	design update		P35	Delete D24, ON/OFF change to ON/OFFBTN#	11/12	DVT
4	schematics update	for TP_INT# wake function	P35	TP PIN1 VCC Connect to +3VALW, add R462, R463@, pop D22, R633, R453	11/12	DVT
5	design change		P10	Change USB port 5 for TS/port 6 for CCD / port 7 for CR(USB)_FP	11/12	DVT
6	design update		P6	reserve RTCRST# to EC pin 27 for clear CMOS add R490, and Q52 reserve to EC_RTCRST#	11/12	DVT
7	design update	EC board ID	P34	Pop R503(100K), R506(12K)	11/15	DVT
8	material update		P36	change C2135, C2136 to 0603 size	11/15	DVT
9	material update		P33	L24, L25 form SM070003Y00 to SM070003K00	11/15	DVT
10	material update		P7	pop share rom	11/15	DVT
11	design update	Co-lay TS_I2C and LVDS EDID	P25	R415, R433 for LVDS EDID R438, R439 for TS I2C	11/15	DVT
12	design update	for LVDS EP mode SMBus2 change to SMBus3	P24	Add R491 reserve for RTD2132 EP_MODE	11/18	DVT
13	design update	for TP_INT# wake function	P34	GPIO55 change to GPIO13	11/18	DVT
14	design update	for GC62.0 function	P17	R2055 change to Pull high +3VSDGPU_AON	11/20	DVT
15	design update	for +1.05VS_VTT leakage issue	P38	+5VALW change to +3VLP add level shift(Q2501), R2503, R2502, R2549 Del R930	11/20	DVT
16	design update	for IT 6513 leakage issue	P27	IT6513 change to use 3VS	11/26	DVT
17	material update	for TXC recommend	P6	C153, C2, C3 to 15PF, C2004, C2005, C2558, C2559 to 10PF	11/27	DVT
18	design update	for wake on LAN function	P29	add R2550 10K pull high to +3V_LAN , PCH side pull high reserve	12/04	DVT
19	design update	for ESD request	P37	add C413 0.1u to +5VS	12/04	DVT
20	design update	for EMI request	P33	add choke(L29,L30) and R(R456, R457,R462,R463) co-lay for USB/B comm	12/04	DVT
21	design update	for ESD request	P36	add R2149, R2150(SM01000NH00), C2140, C2142(680PF) D2008(SCA00001B00) change to SOT23 R2135,R2138 chagne to 60 ohm	12/10	DVT
22	material update			SW3 SN100007700 chagne to SN100000K00 C408, C486 SF000002Y00 change to SF000006R00 C18, C118 SF000002Z00 change to SF000006S00	12/13	DVT
23	design update		P37	reserve R2551 0 ohm +3VALW to +3VLAN reserve R2540 for disable PHY	12/20	DVT

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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	design issue		P28	U2052, U2503 change power rail to +HDMI_5V_OUT	12/31	PVT
2	material update	PVT board ID	P34	R506 change to 15K	12/31	PVT
3	design update	modify DQS P/N pin	P18		01/08	PVT
4	schematics update					
5	design change					
6	design update					
7	design update					
8	material update					
9	material update					
10	material update					
11	design update					
12	design update					
13	design update					
14	design update					
15	design update					
16	design update					
17	material update					
18	design update					
19	design update					
20	design update					
21	design update					
22	material update					
23	design update					

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