

Compal Confidential

HM51_TR/HM70_TR Discrete

NDWG2/NDWH1 LA5992 Schematic Document

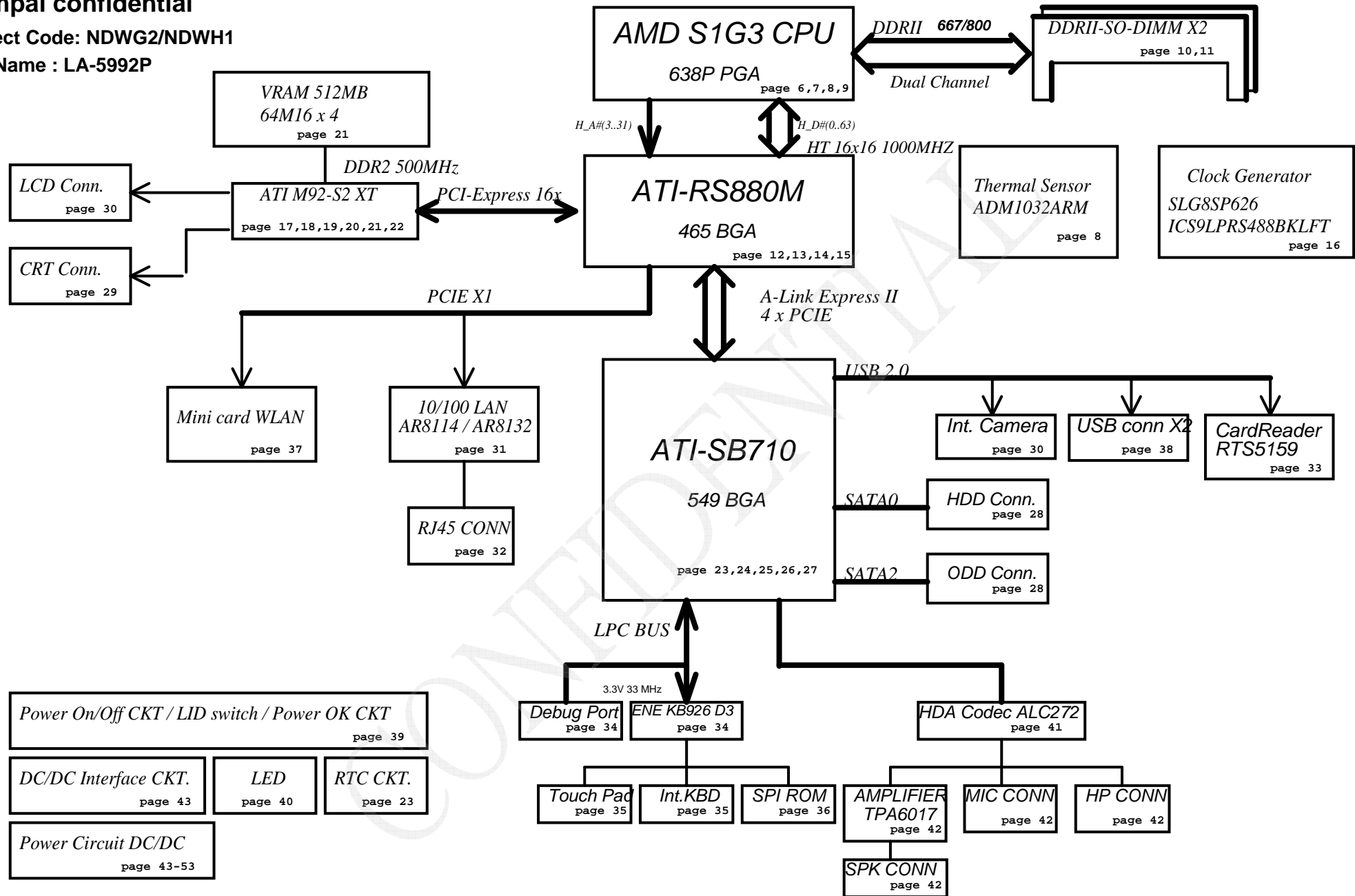
Mobile AMD S1G3/RS880M/SB710
2009/12/02 Rev 1.0

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				Rev	C

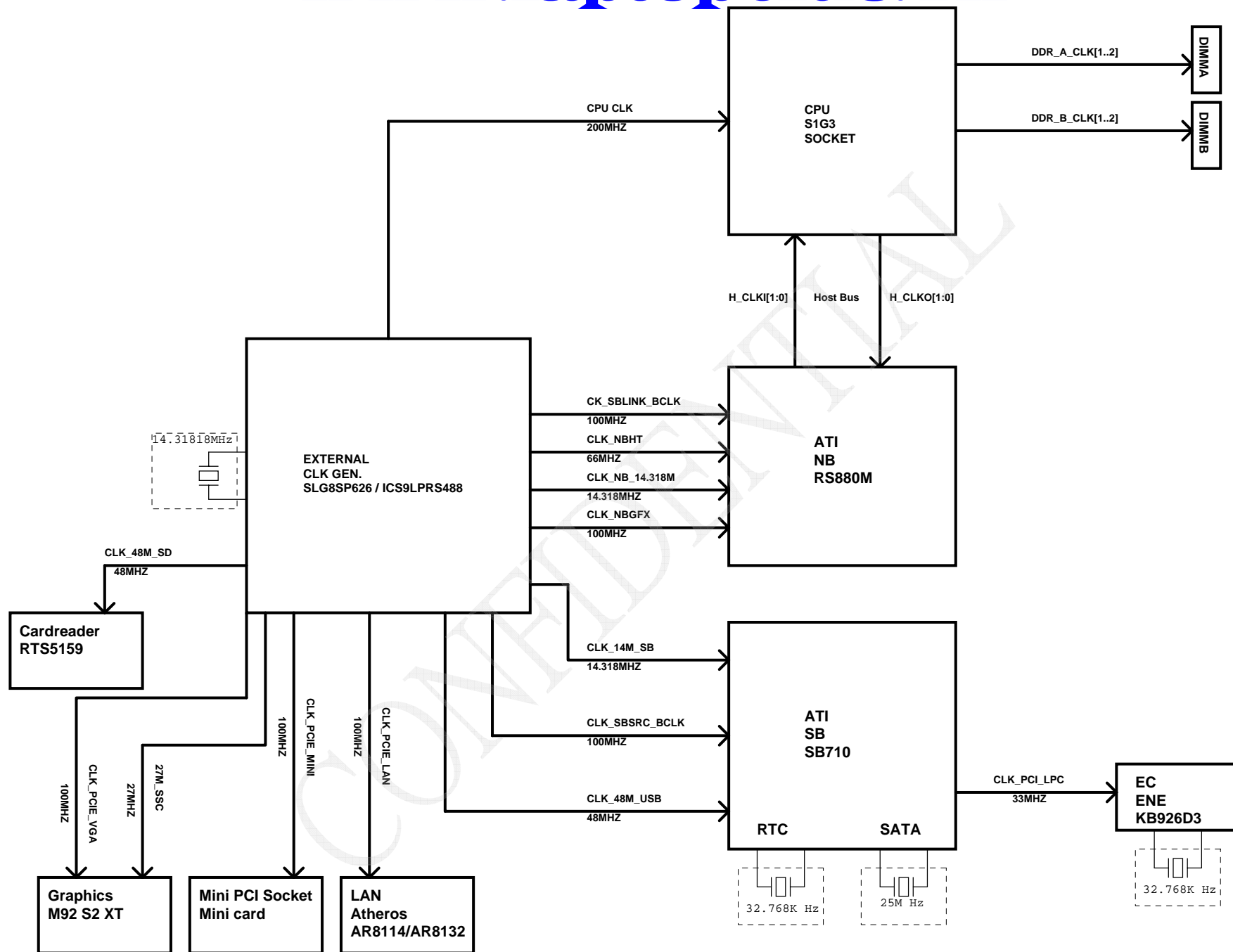
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Project Code: NDWG2/NDWH1

File Name : LA-5992P



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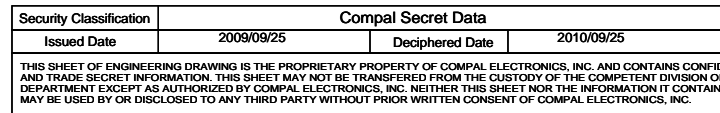
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DDR2 SODIMMx2		
VDD_MEM	1.8V	7 A
VTT_MEM	0.9V	430 mA

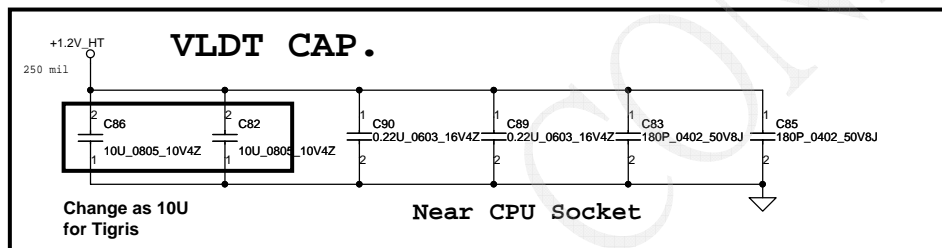
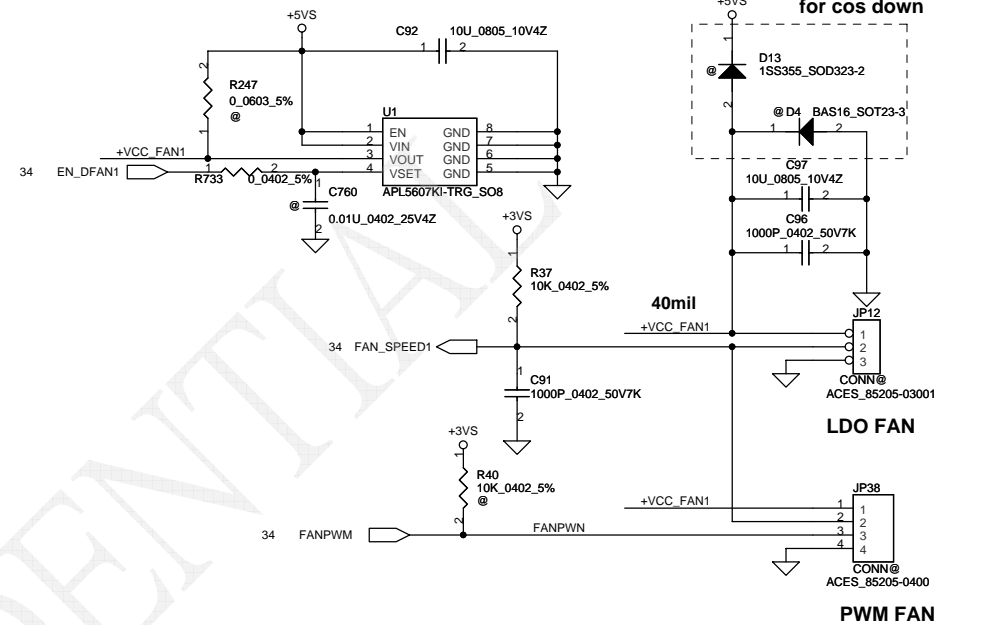
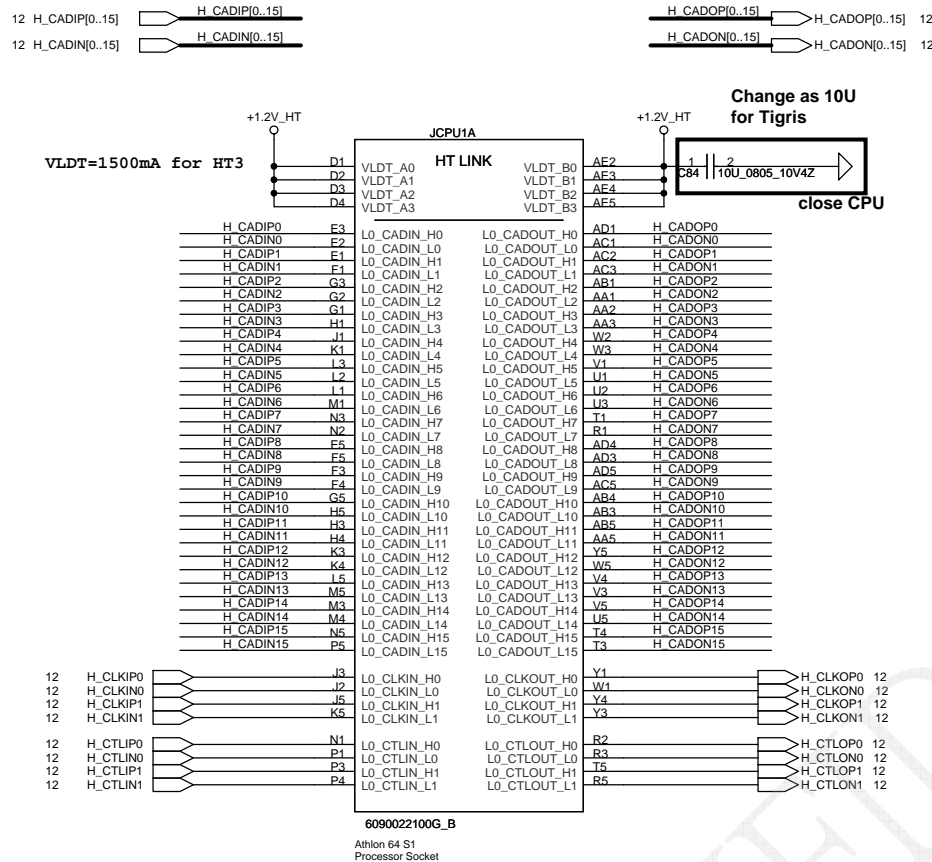
NB RS880MN		
VDDC	0.95-1.1V	10 A
VDDHT	1.1V	680 mA
PLLVD		65 mA
VDDPCIE		2.5 A
VDDHTRX		680 mA
IOPLLVD		
VDDHTTX	1.2V	400 mA
AVDDDI	1.8V	20 mA
AVDDQ		4 mA
IOPLLVD18		
PLLVD18		20 mA
VDD18		10 mA
VDDA18PCIE		700 mA
VDDA18HTPLL		20 mA
VDDA18PCIEPLL		120 mA
VDDL18		300 mA
VDDLTP18		15 mA
VDD33	3.3V	60 mA
AVDD		110 mA

SB		SB710	
S5_1.2V	1.2V		510mA
USB_PHY_1.2V			113 mA
VDD			197 mA
AVDDCK_1.2V			62 mA
CKVDD_1.2V			
AVDD_SATA			43 mA
PLLVD_SATA			600 mA
PCIE_VDDR			567 mA
PCIE_PVDD	3.3V		93 mA
S5_3.3V			32 mA
AVDD TX/RX			17 mA
AVDDC			658 mA
VDDQ			131 mA
VDD33_18			71 mA
AVDDCK_3.3V			47 mA
XTLVDD_SATA			6 mA
V5_VREF		5V	1 mA
VBAT		2.5~3.6V	

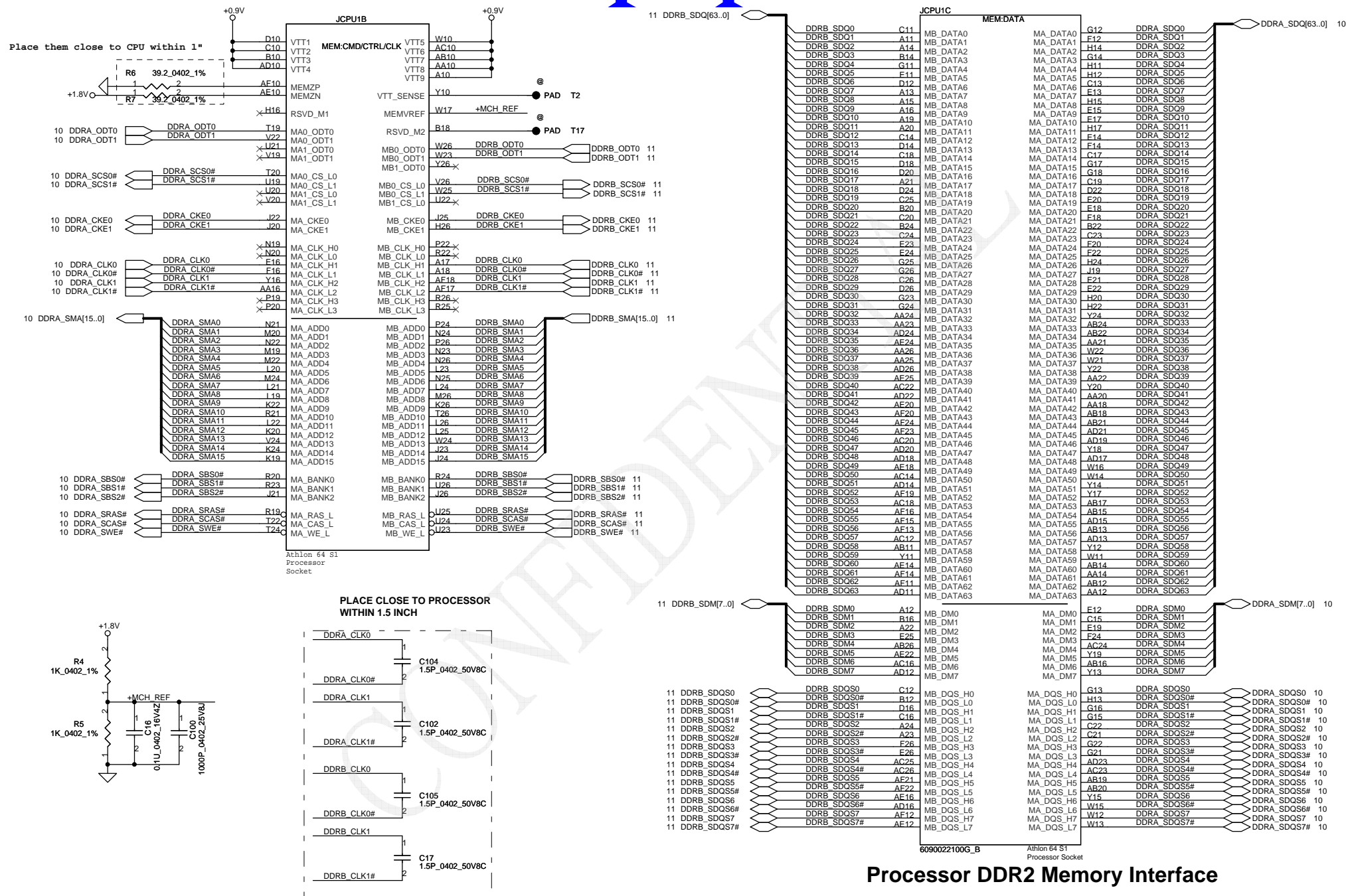
VRAM HYB18T256161BF x4	
VDD	1.8V
VDDL	
VDDQ	



FAN Control Circuit

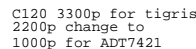


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Processor DDR2 Memory Interface

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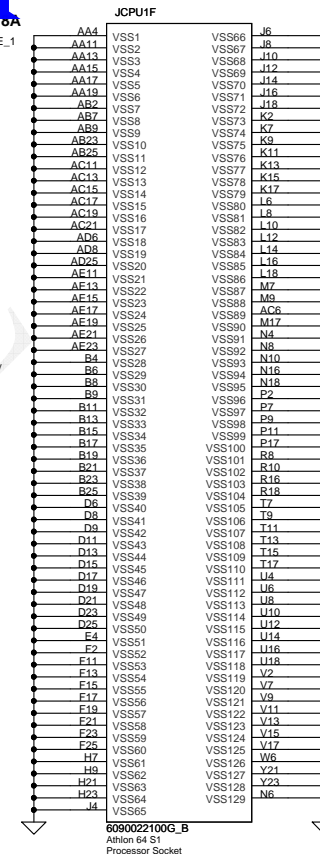
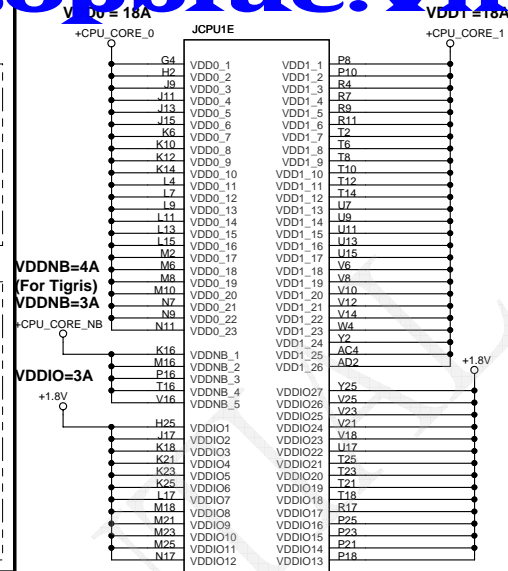
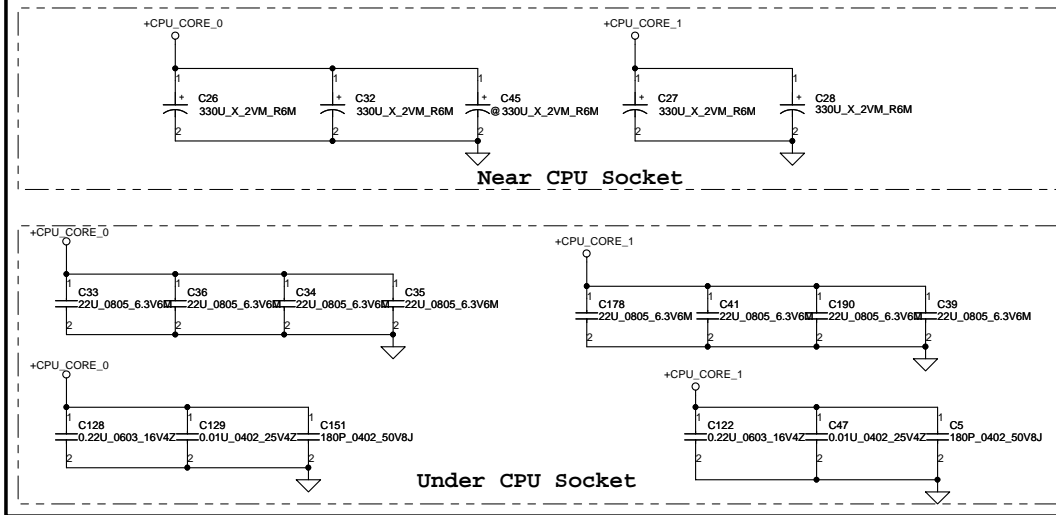


ADM1032ARMZ_MSOP8
Address:100_1101

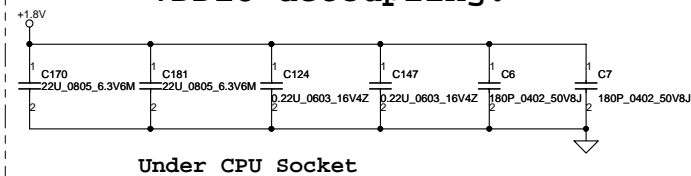
NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

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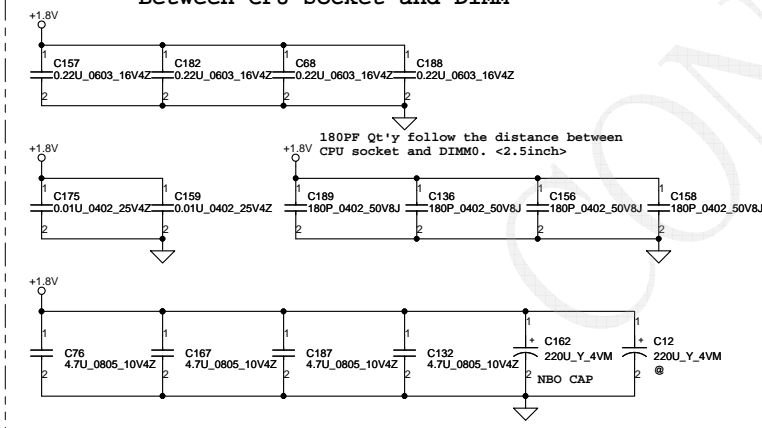
VDD(+CPU_CORE) decoupling.



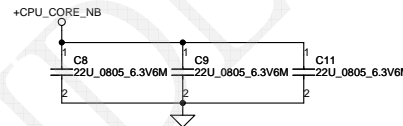
VDDIO decoupling.



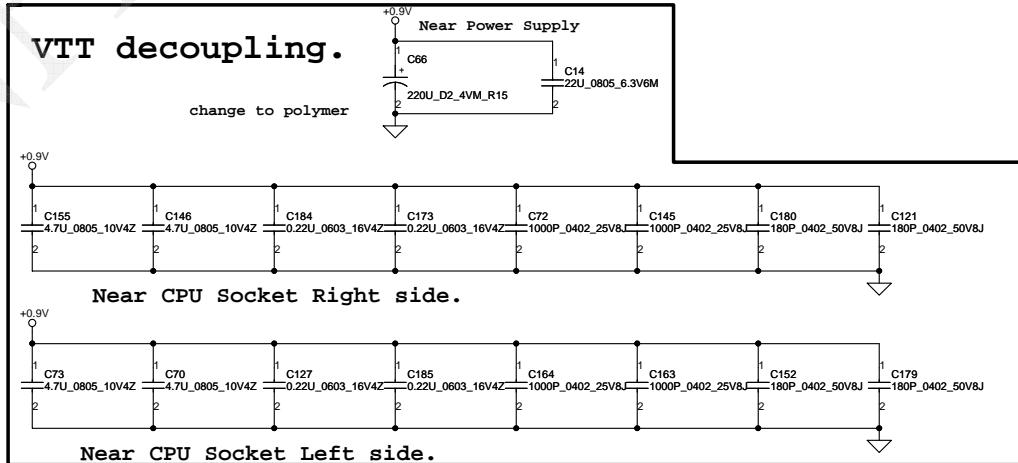
Between CPU Socket and DIMM



+CPU_CORE_NB decoupling.

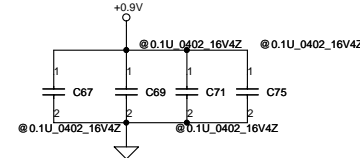
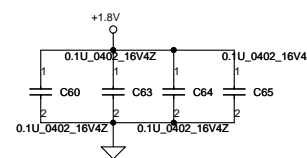
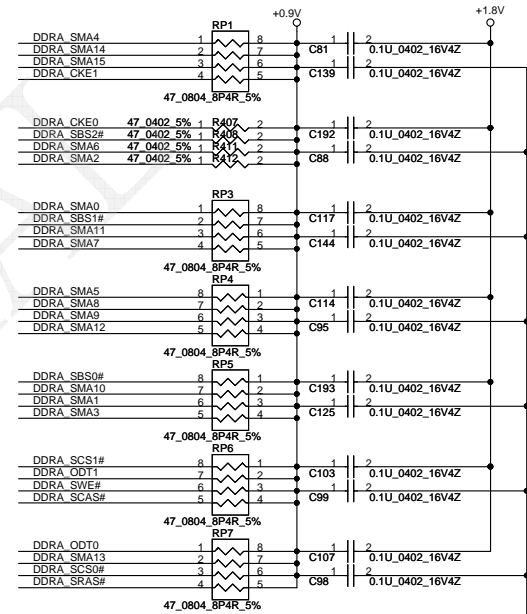
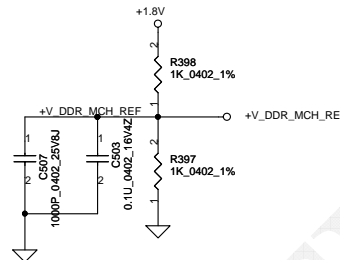


VTT decoupling.



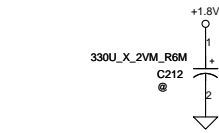
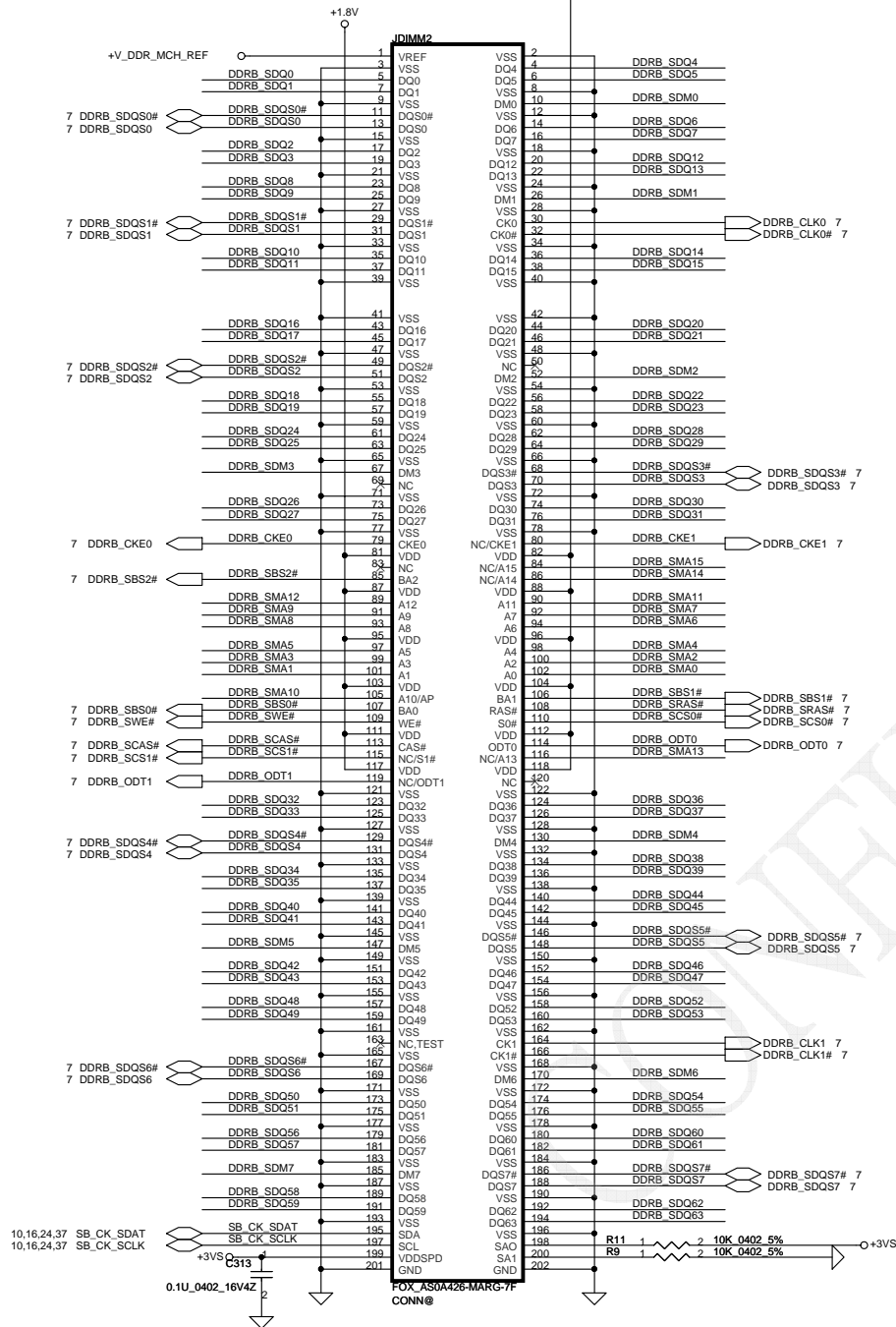
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RESERVE
+V_DDR_MCH_REF BUFFER CIRCUIT

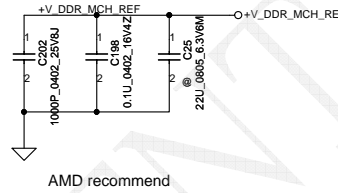


DIMM1 REV H:5.2mm (BOT)

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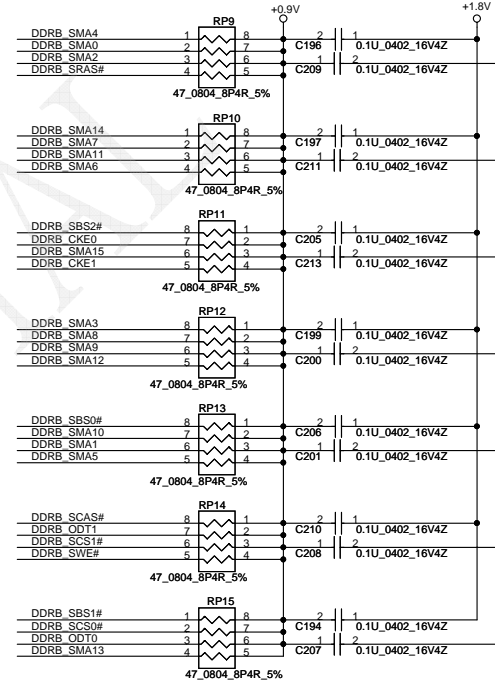
Place near to DIMM2



DDR_B_SDQ[0..63] 7

DDR_B_SDM[0..7] 7

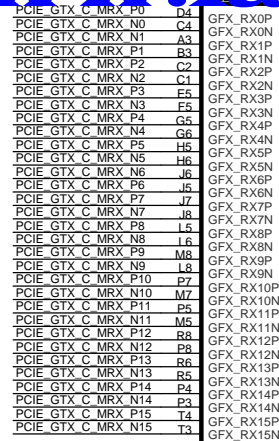
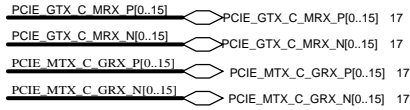
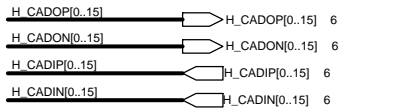
DDR_B_SMA[0..15] 7



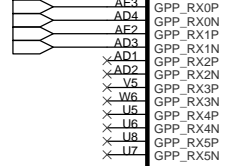
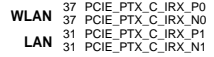
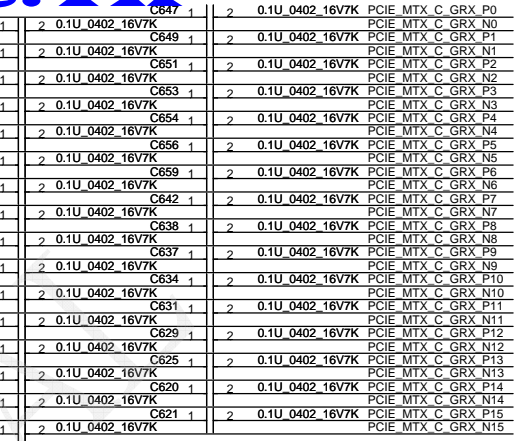
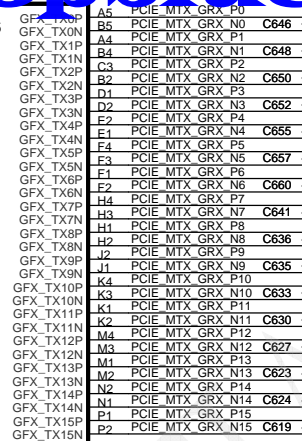
DIMM1 REV H:9.2mm (BOT)

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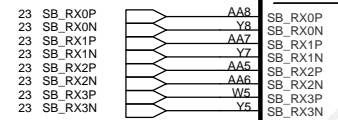
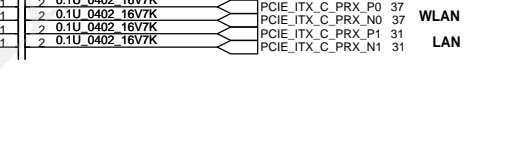
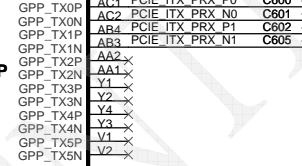
PART 2 OF 6



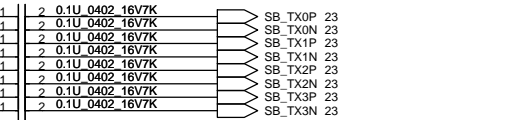
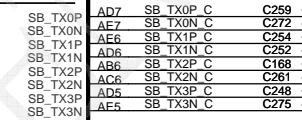
PCIE I/F GFX



PCIE I/F GPP

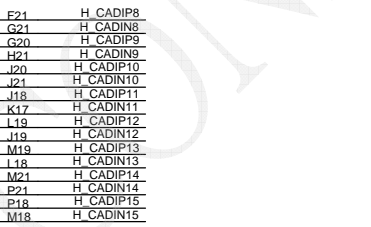
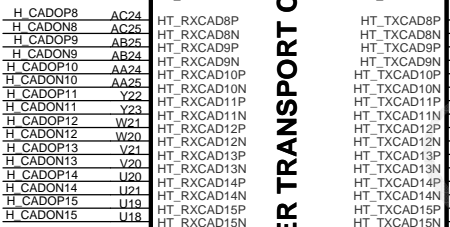
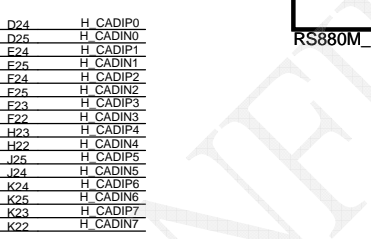
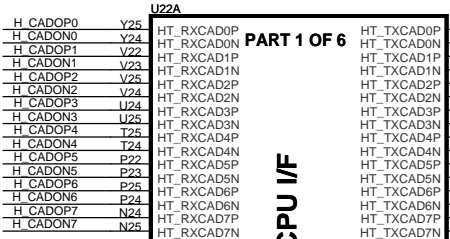


PCIE I/F SB

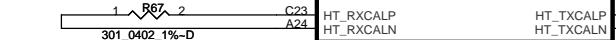
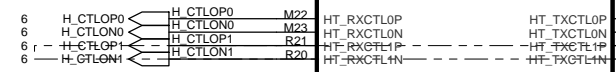
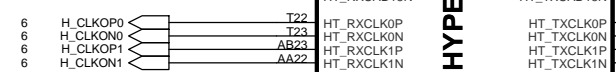
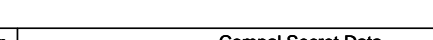
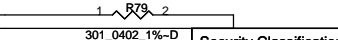
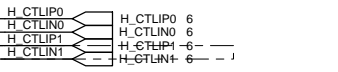
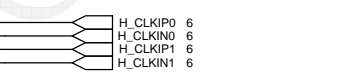


PCIE_CALRPP(PCIE_CALRNP)
PCIE_CALRNP(PCIE_CALRNP)
RS880M_FCBGA528

PART 1 OF 6



HYPER TRANSPORT CPU I/F

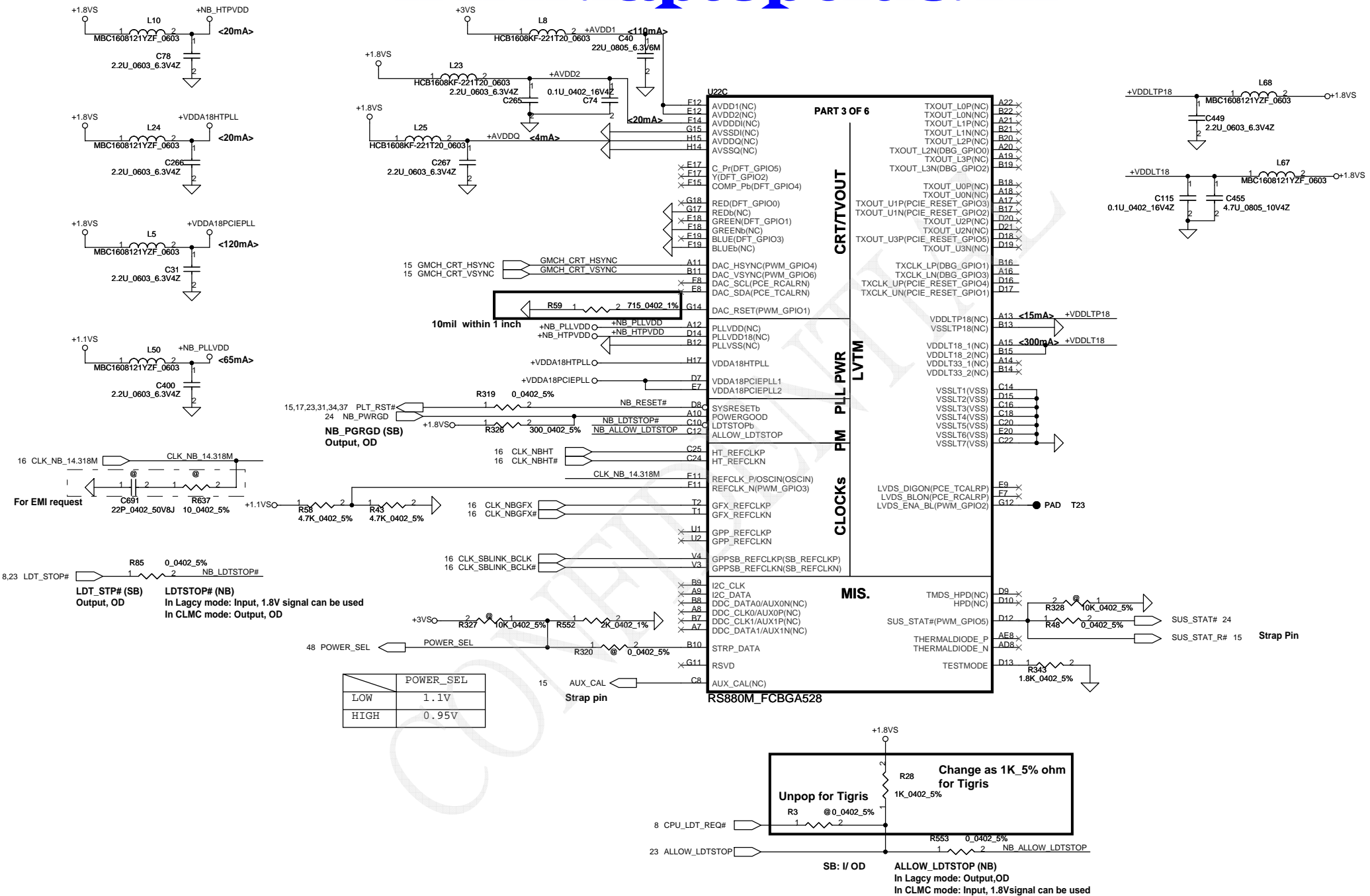


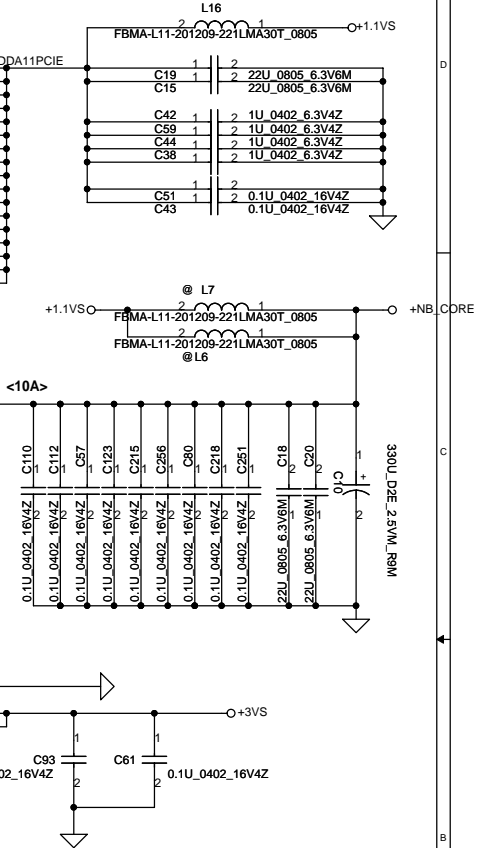
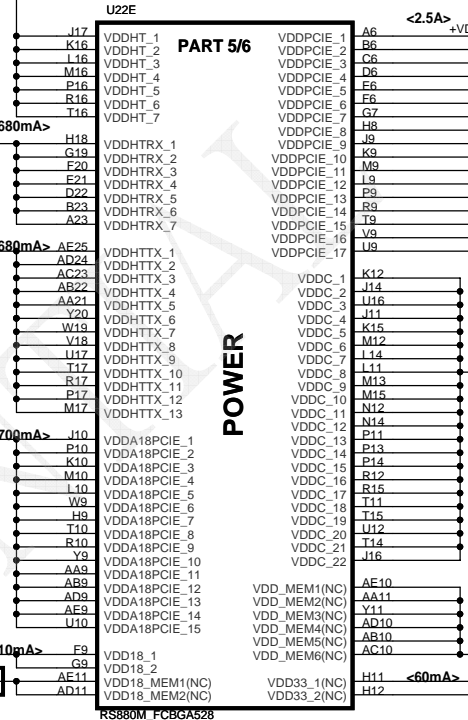
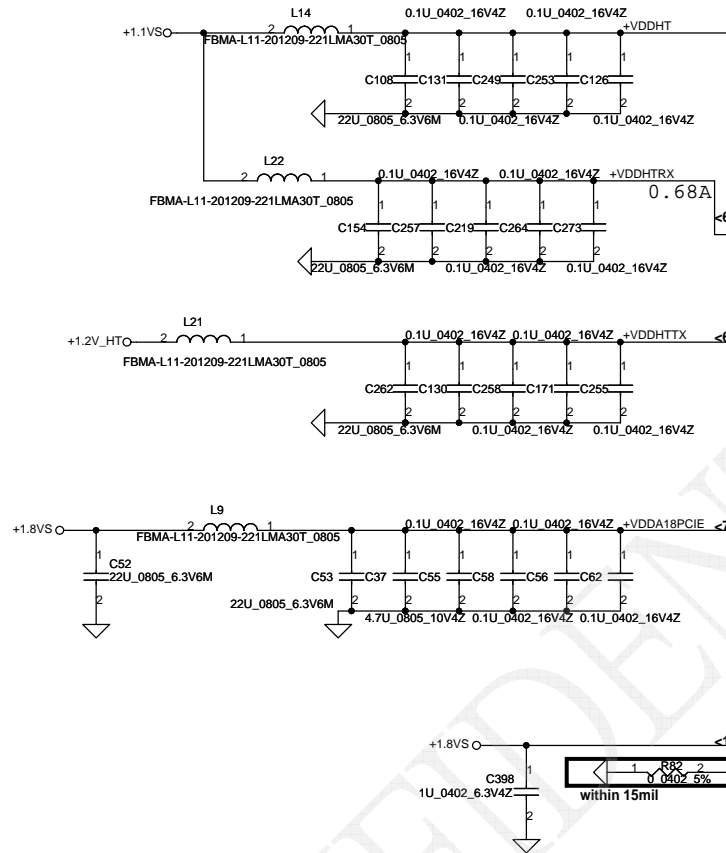
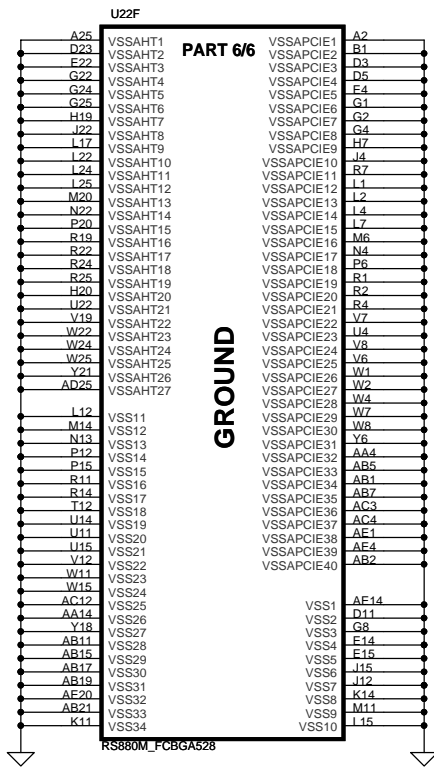
Place within 1" layout 4/8

HT Link
When tune trace length, must keep 1:4 on self-trace

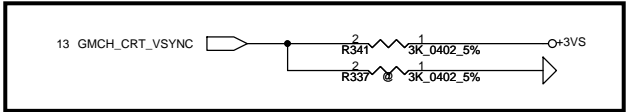
RS880M_FCBGA528

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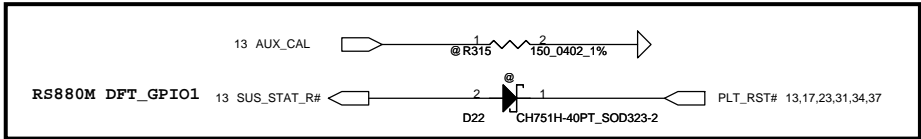


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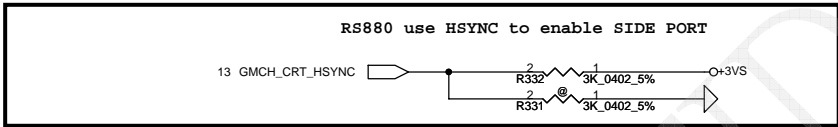
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS880)
0 : Enable (Rs880)



DFT_GPIO1: LOAD_EEPROM_STRAPS

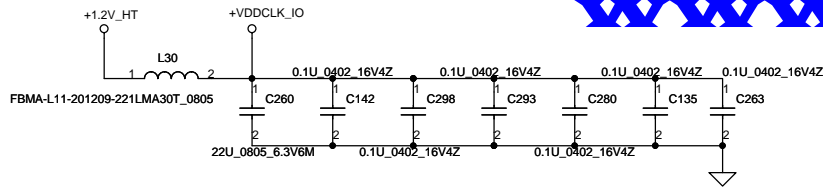
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780/RS880M: DFT_GPIO1 RS880M:SUS_STAT



RS880 use HSYNC to enable SIDE PORT

RS740/RS780/RS880M: Enables Side port memory (RS880M use HSYNC#)
0. Enable (RS880M)
1 : Disable(RS880M)

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SEL_27M	1	configure as 27M and 27M_SS output
	0	configure as SRC 7 output

27M_SEL	1 *	configure as 27M and 27M_SS output
	0	configure as SRC 7 output

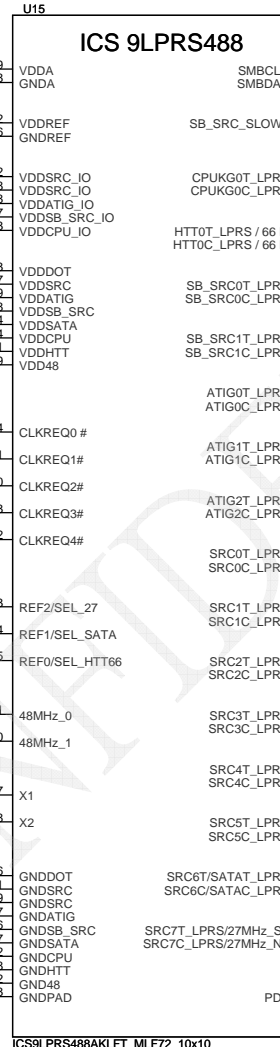
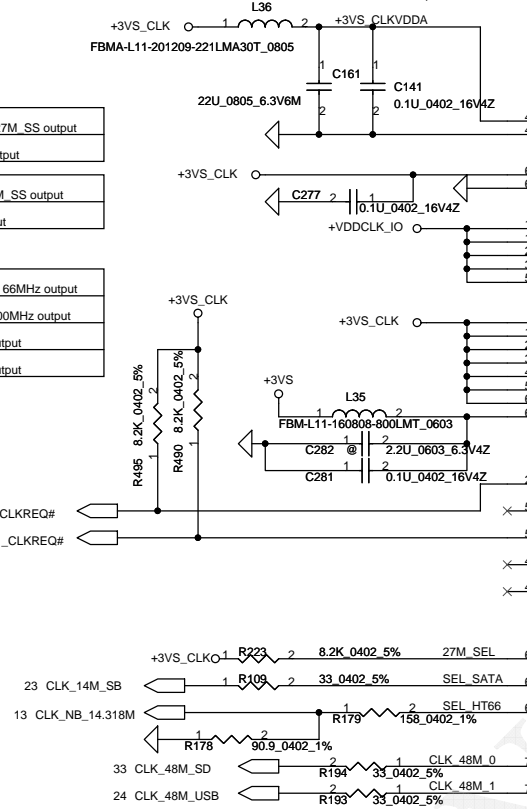
SEL_HTT66	1	configure as single-ended 66MHz output
	0 *	configure as differential 100MHz output
SEL_SATA	1 *	SS 100M SATA SRC6 output
	0	SS 100M SATA SRC6 output

LAN request
MiniCard1 request

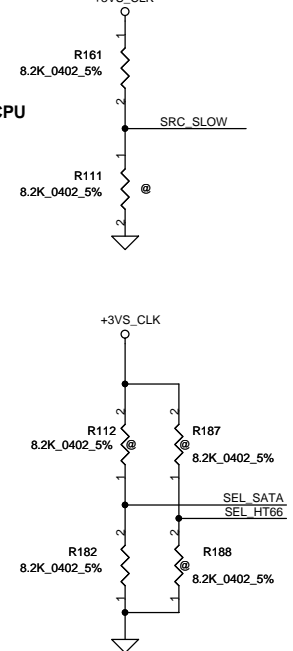
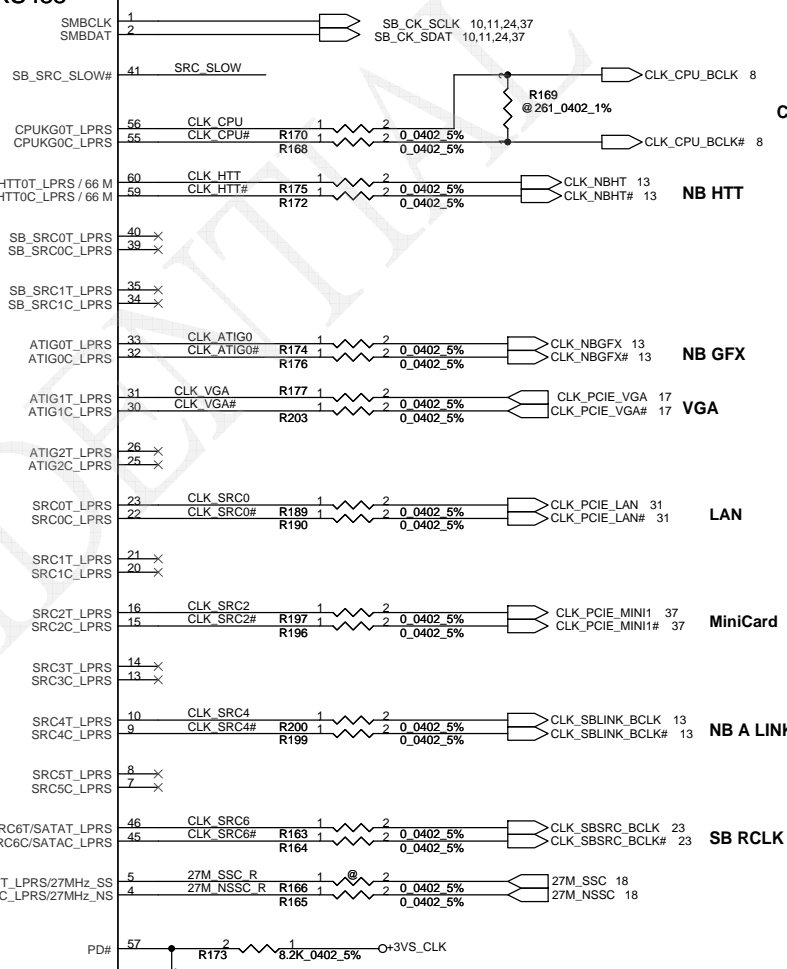
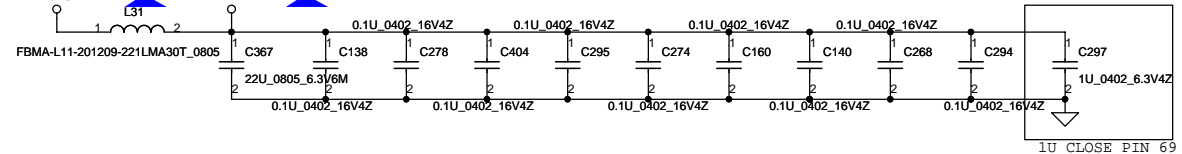
External 14MHz CLK
for SB710

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF

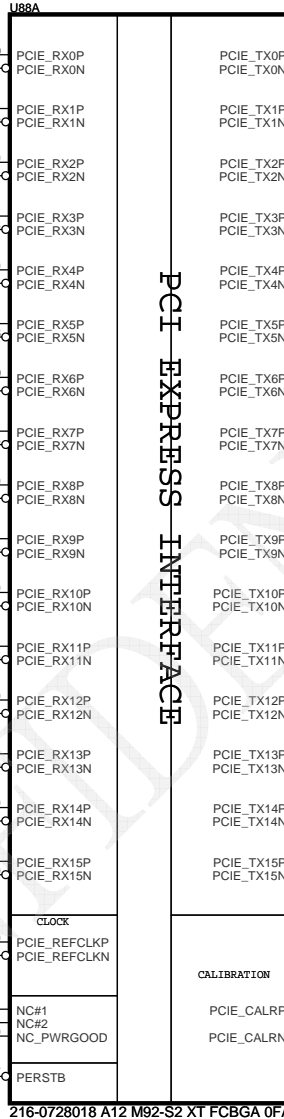
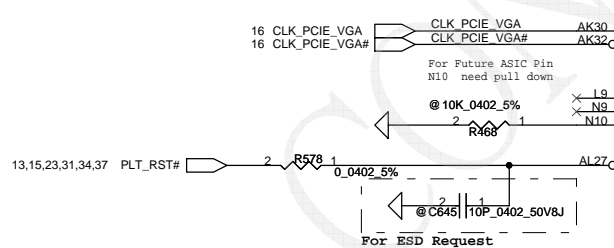
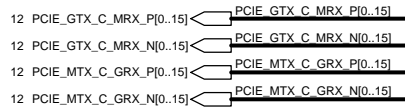


Main--SLG8SP626VTR-SA00001Z310
Second--ICS9LPRS488CKLFT-SA000023H10

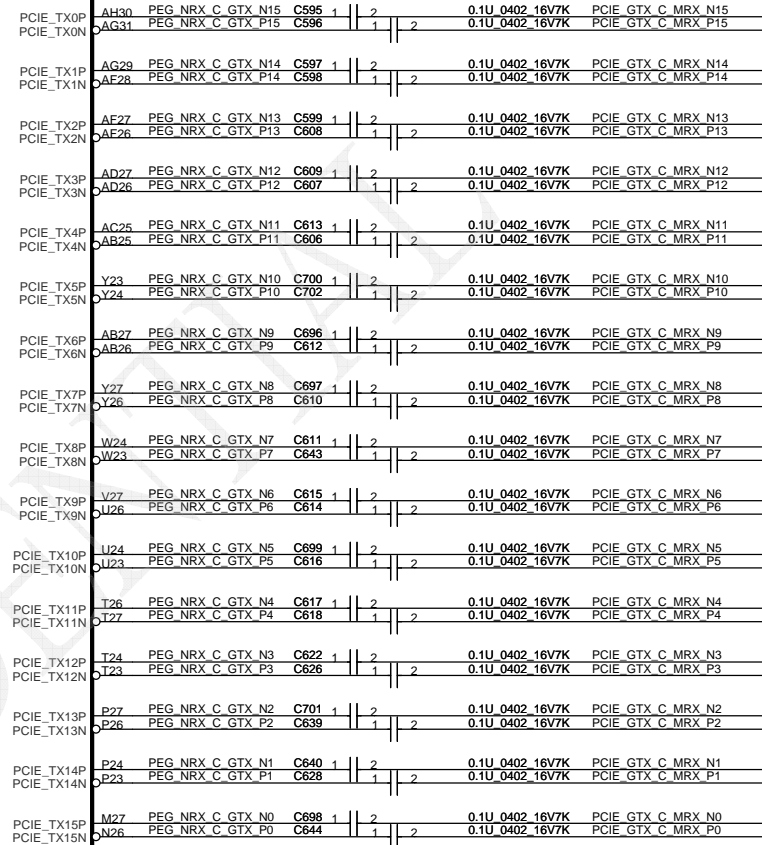


SRC 0	LAN
SRC 1	
SRC 2	MINI1 (WLAN)
SRC 3	
SRC 4	NB-Alink
SRC 5	
SRC 6	SB-Alink

PCIE LANE REVERSAL



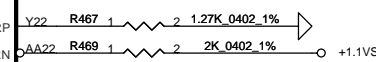
PCIE LANE REVERSAL



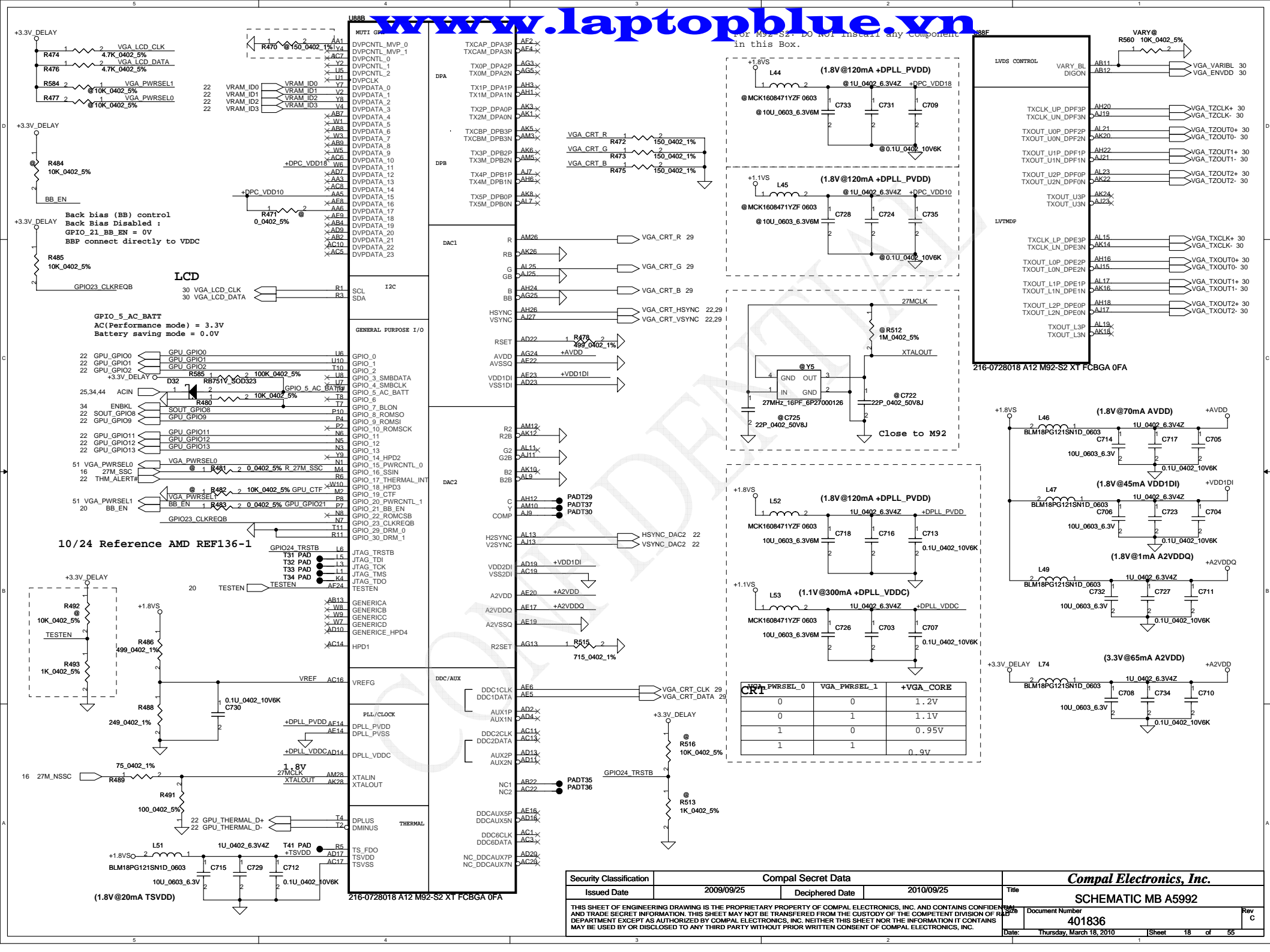
CALIBRATION

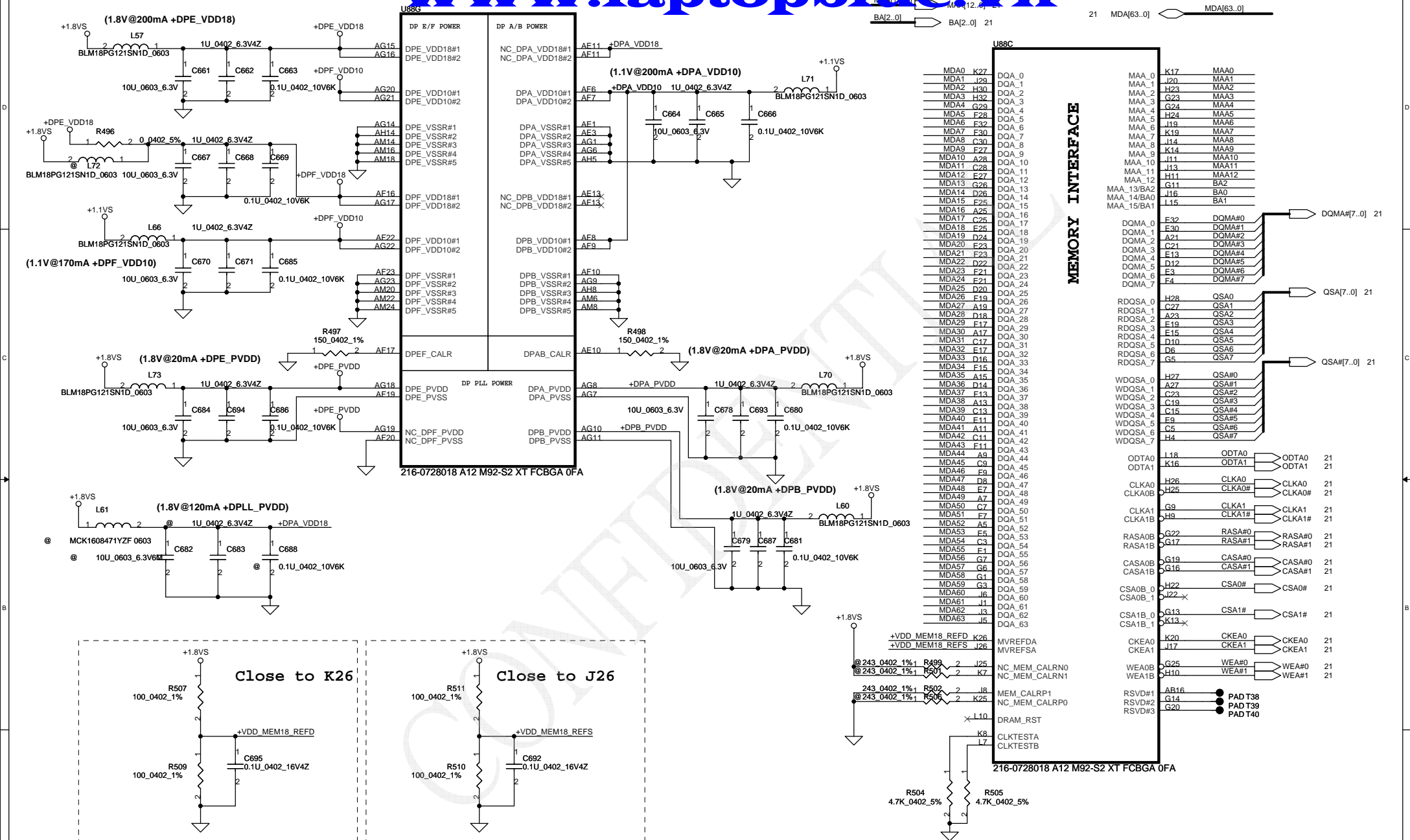
PCIE_CALRP

PCIE_CALRN



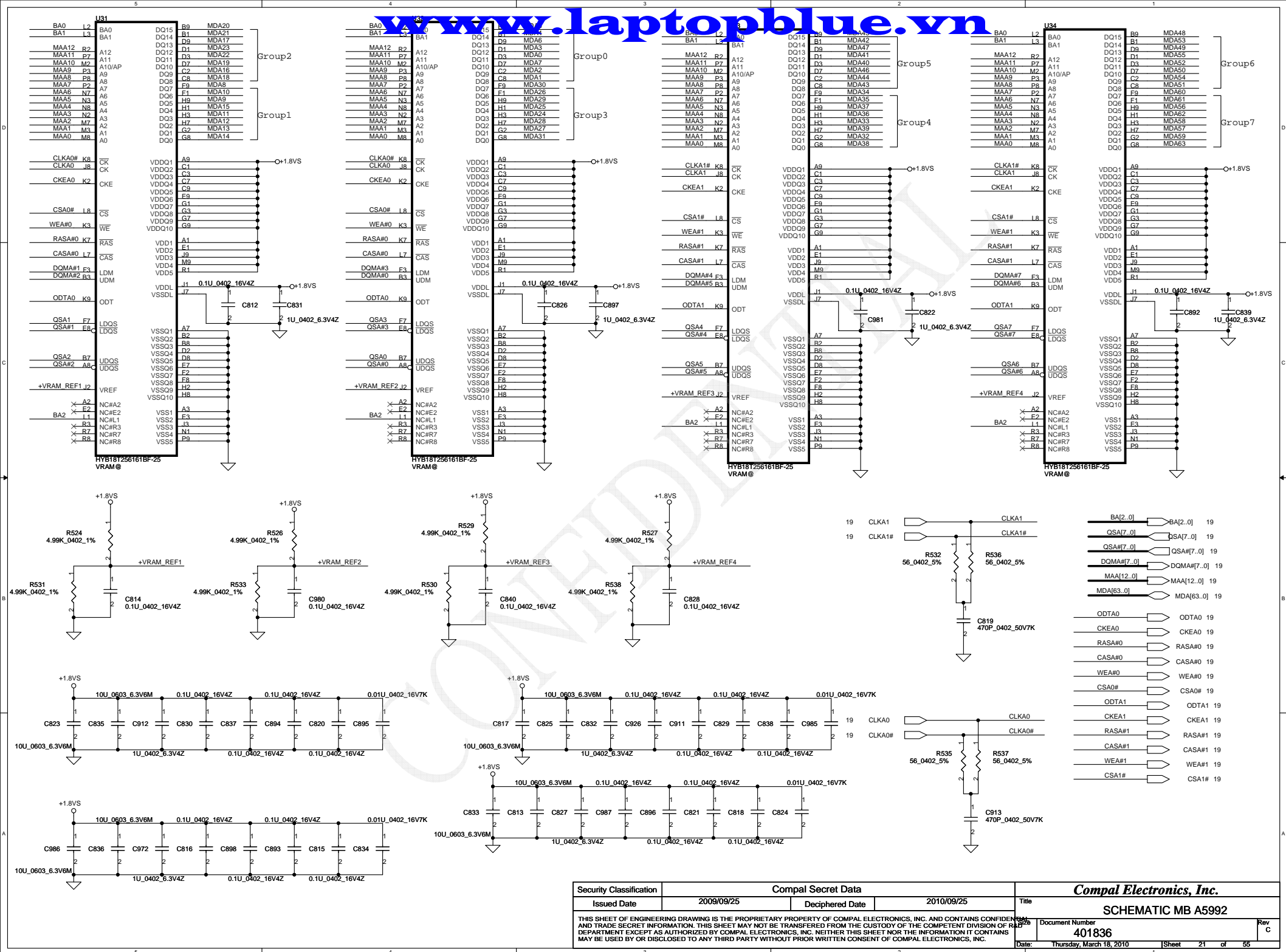
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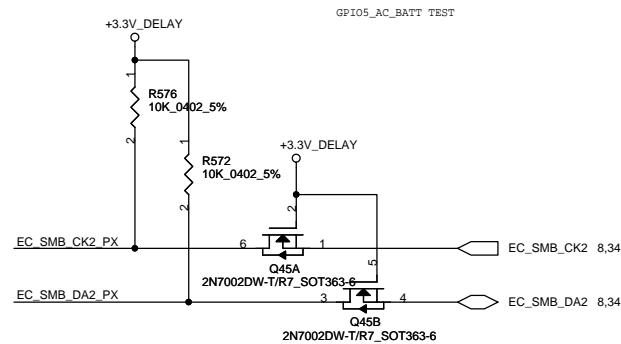


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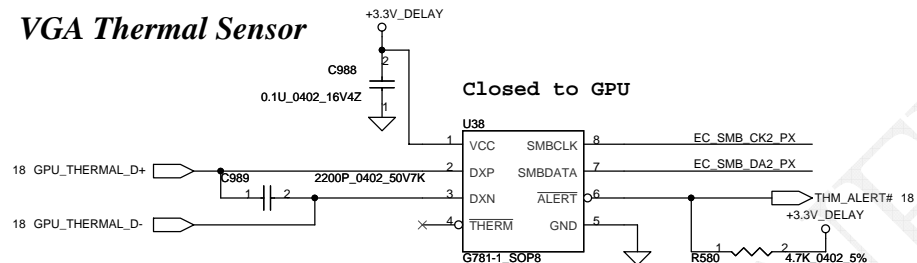


CONFIGURATION STRAPS



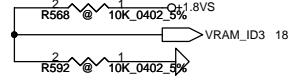
VSYNC_DAC1 and HSYNC_DAC1
pull up to HDMI & DISPLAYPORT
AUDIO function

VGA Thermal Sensor



Change to SA007810210

Address 1001 101X b



```
VRAM_ID0=VRAM_ID0_0
VRAM_ID1=VRAM_ID1_1
VRAM_ID2=VRAM_ID2_2
VRAM_ID3=VRAM_ID3_3
```

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		1
ROMIDCFG(2:0)	GPIO[13:11]	BIF_RX_PLL_CALIB_BP	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	ENABLE EXTERNAL BIOS ROM	0
SMS_EN_HARD	H2SYNC	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0
CCBYPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

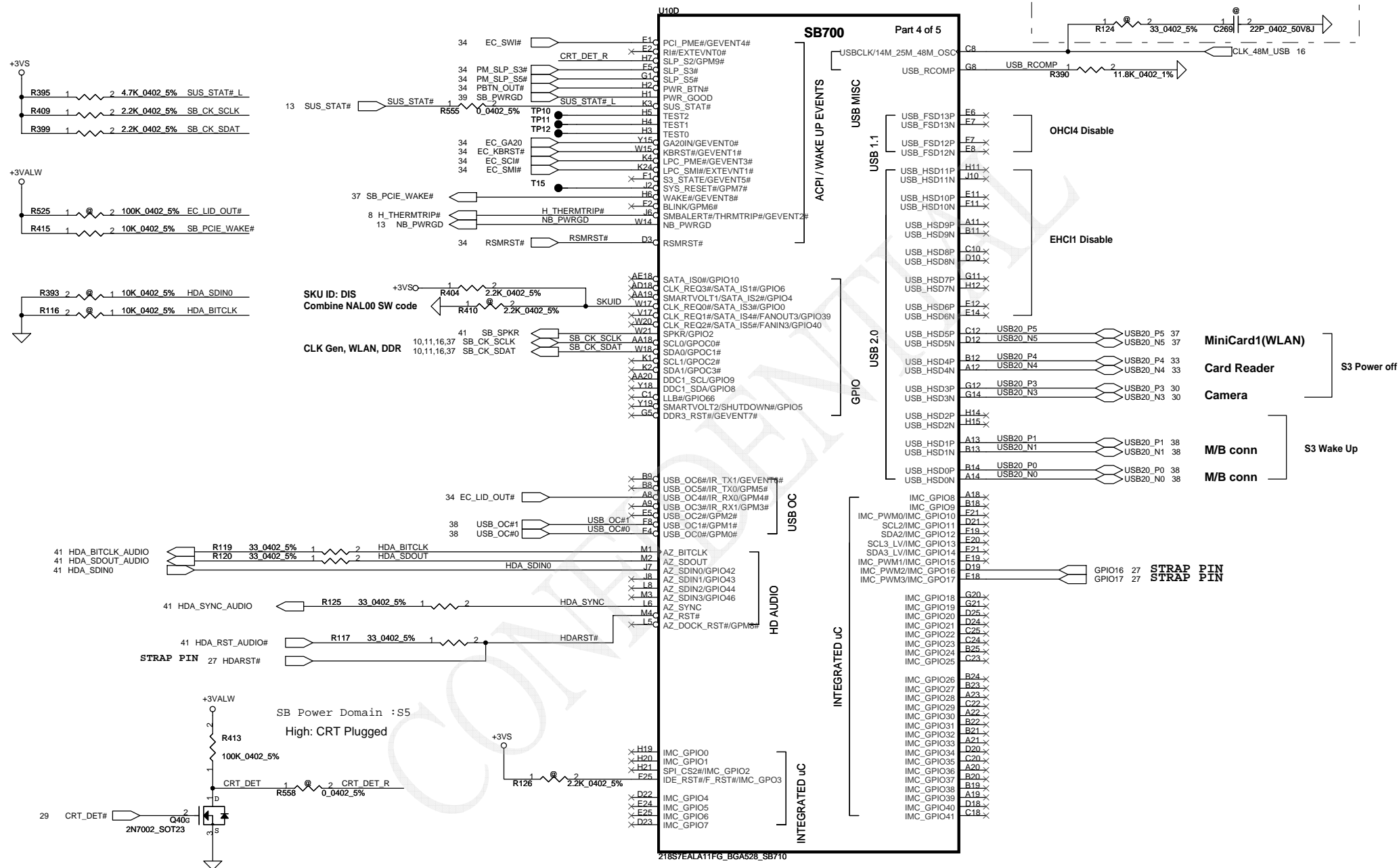
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
<p>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
GPIO_28_TDO	GPIO21_BB_EN

STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (3,2,1,0)	M92 S2-XT		512MB(x4)	Hynix 64Mx16 1.8V	SA00002UH20	0 0 0 1
				512MB(x4)	ATI 64Mx16 1.8V	SA00003LT10	0 0 1 0
				512MB(x4)	Samsung 64Mx16 1.8V (E-die)	SA00003TO10	0 1 0 0

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D

Main

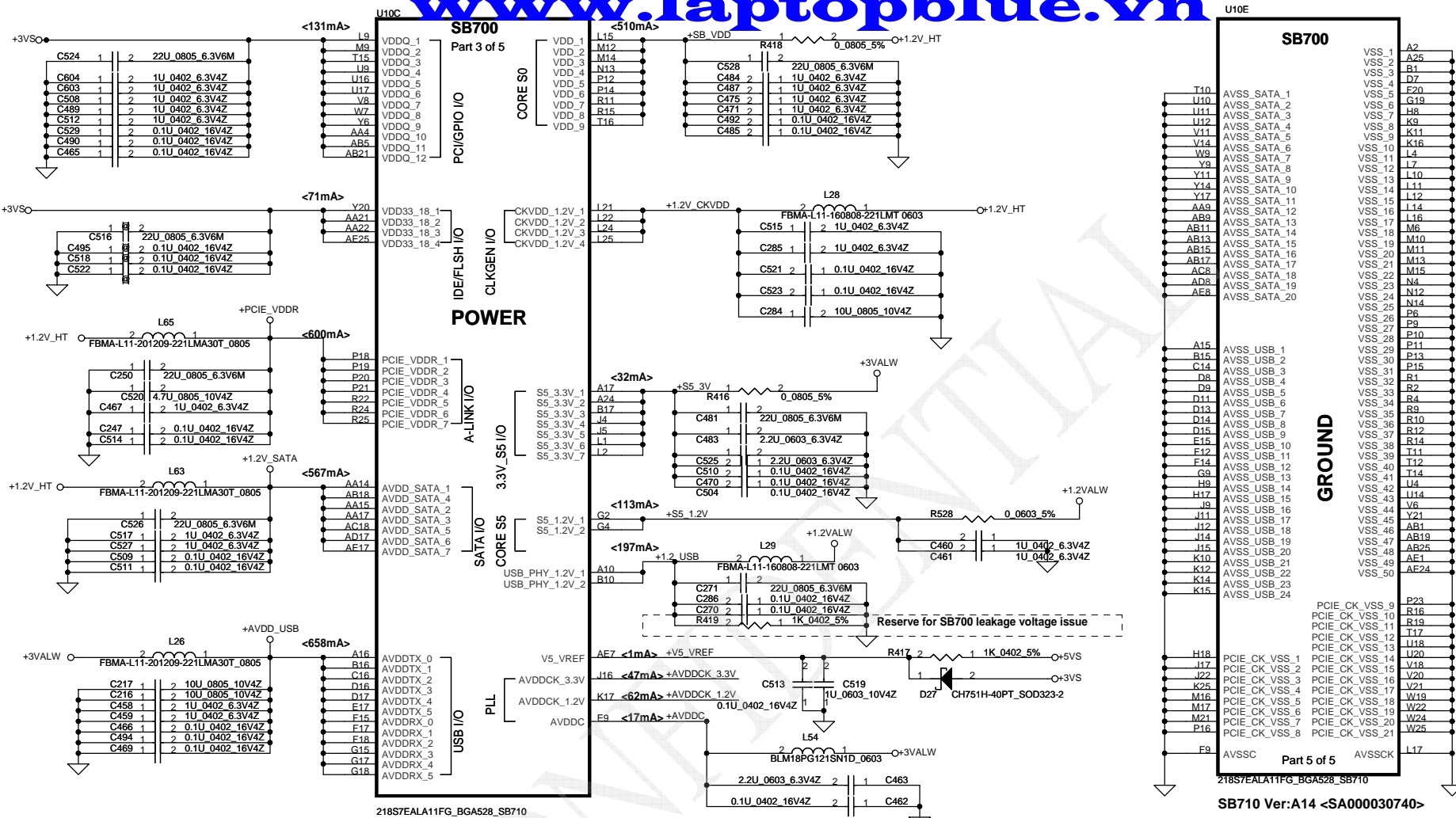
**2nd
ODD**



218S7EALA11FG BGA528 SB710



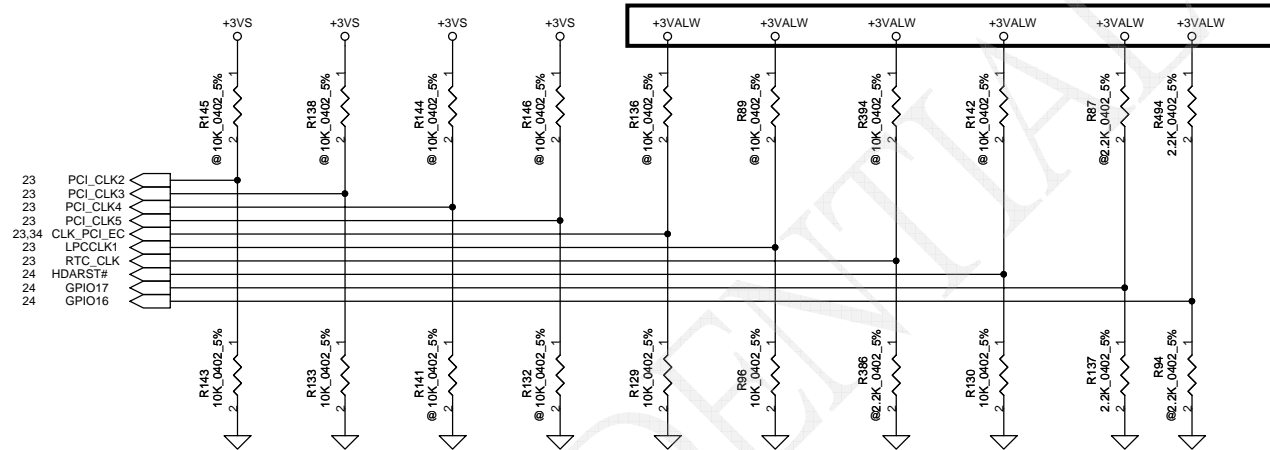
for ACIN level issue



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REQUIRED STRAPS

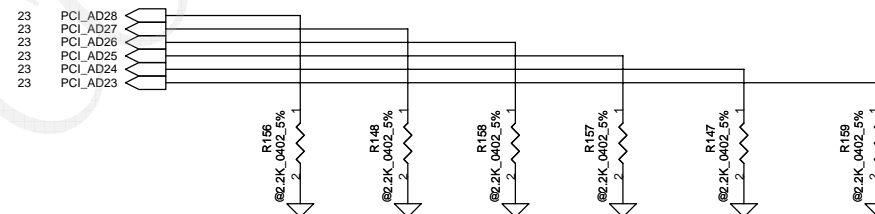
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	L,H = LPC ROM (Default L,NC) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



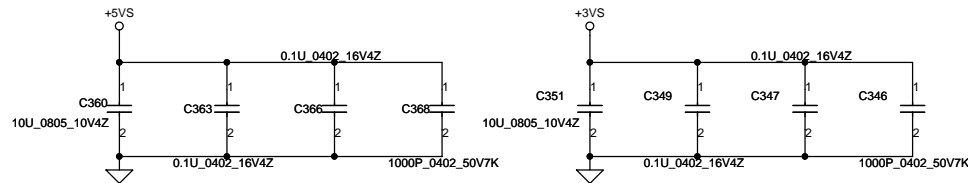
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

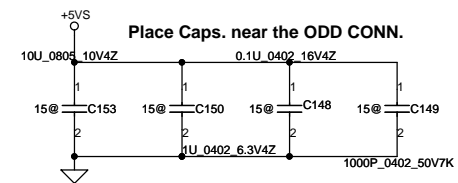
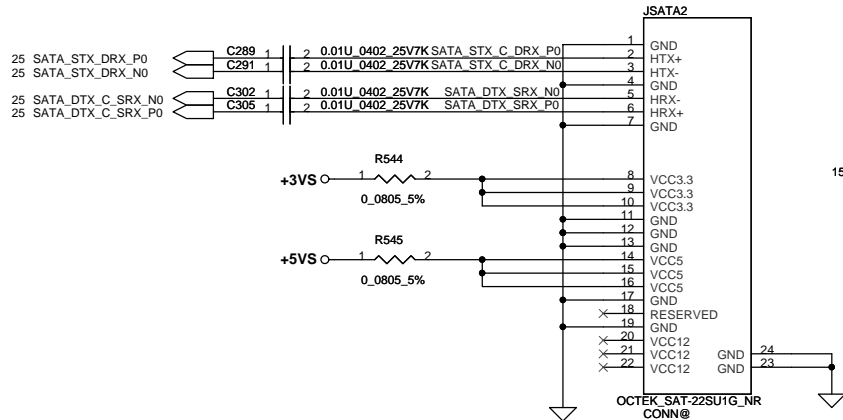
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



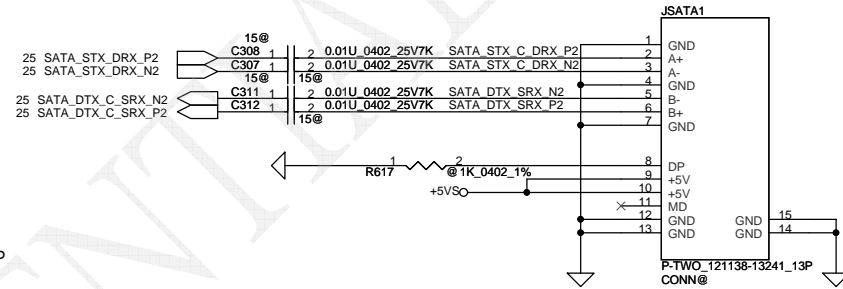
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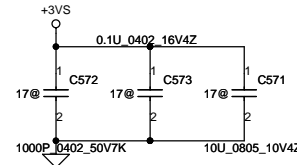
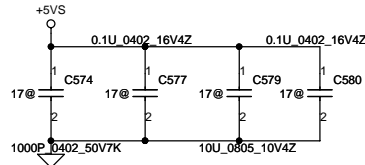
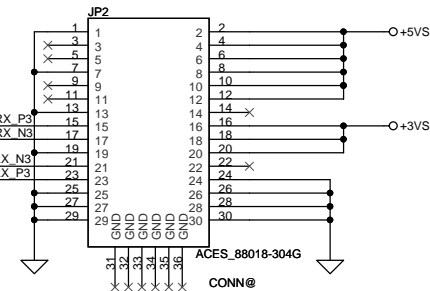
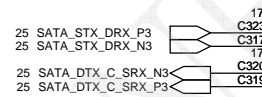
SATA HDD CONN



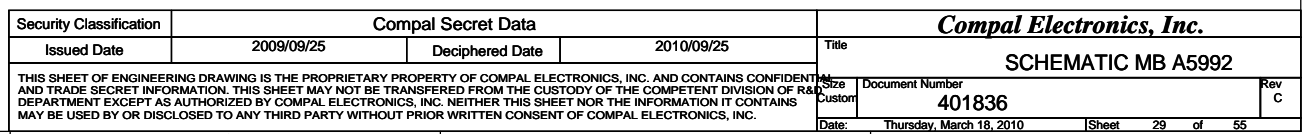
SATA ODD CONN



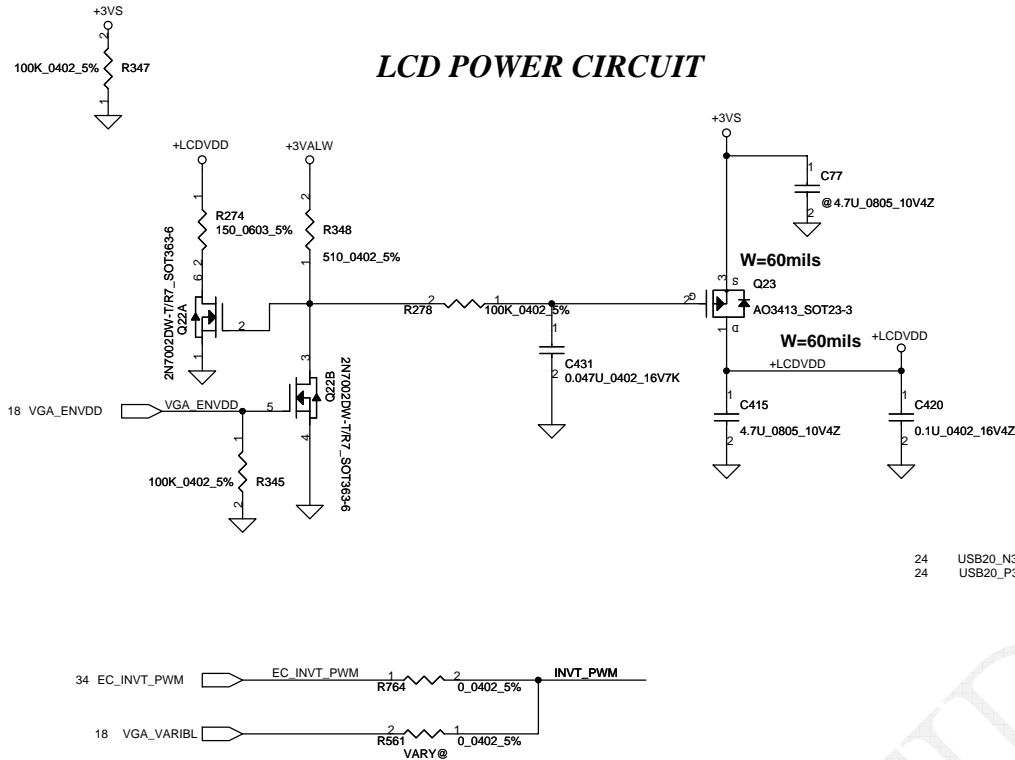
Second ODD



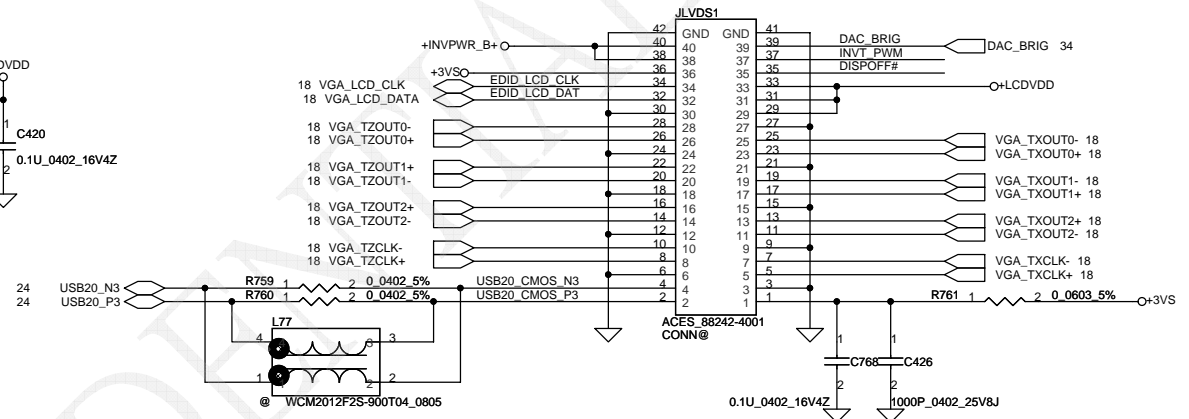
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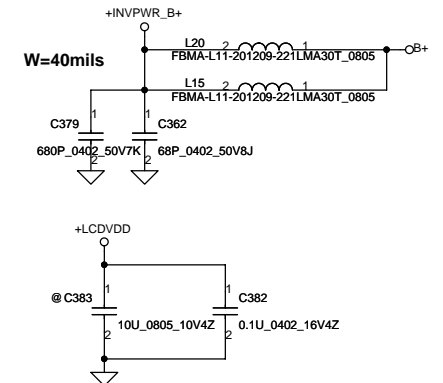
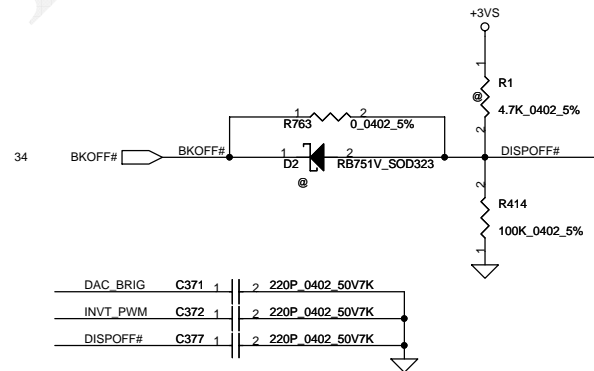
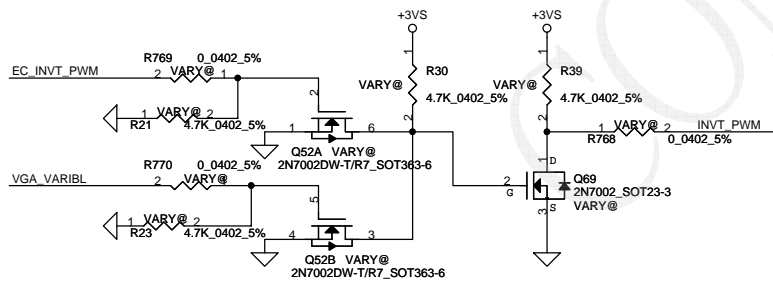
LCD POWER CIRCUIT



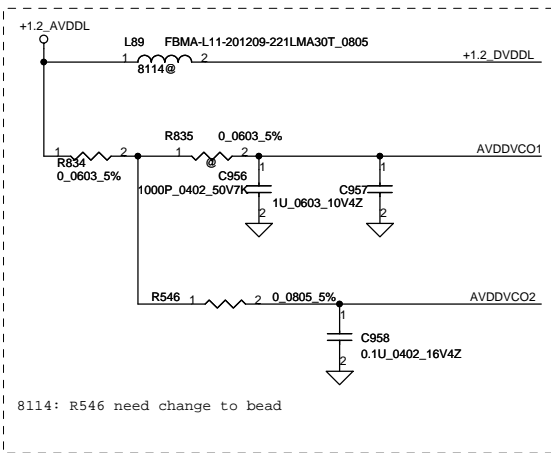
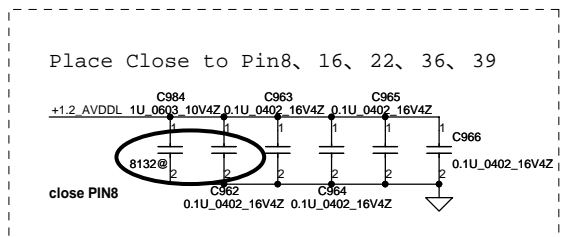
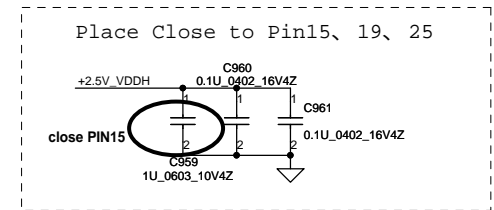
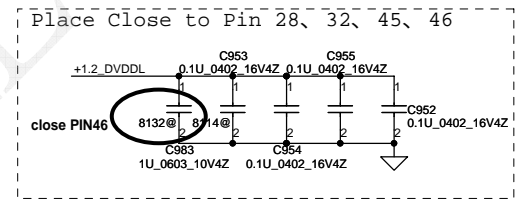
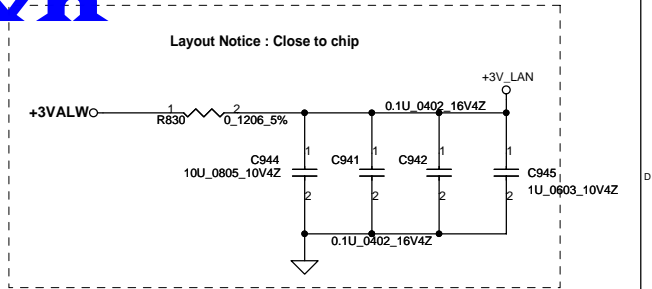
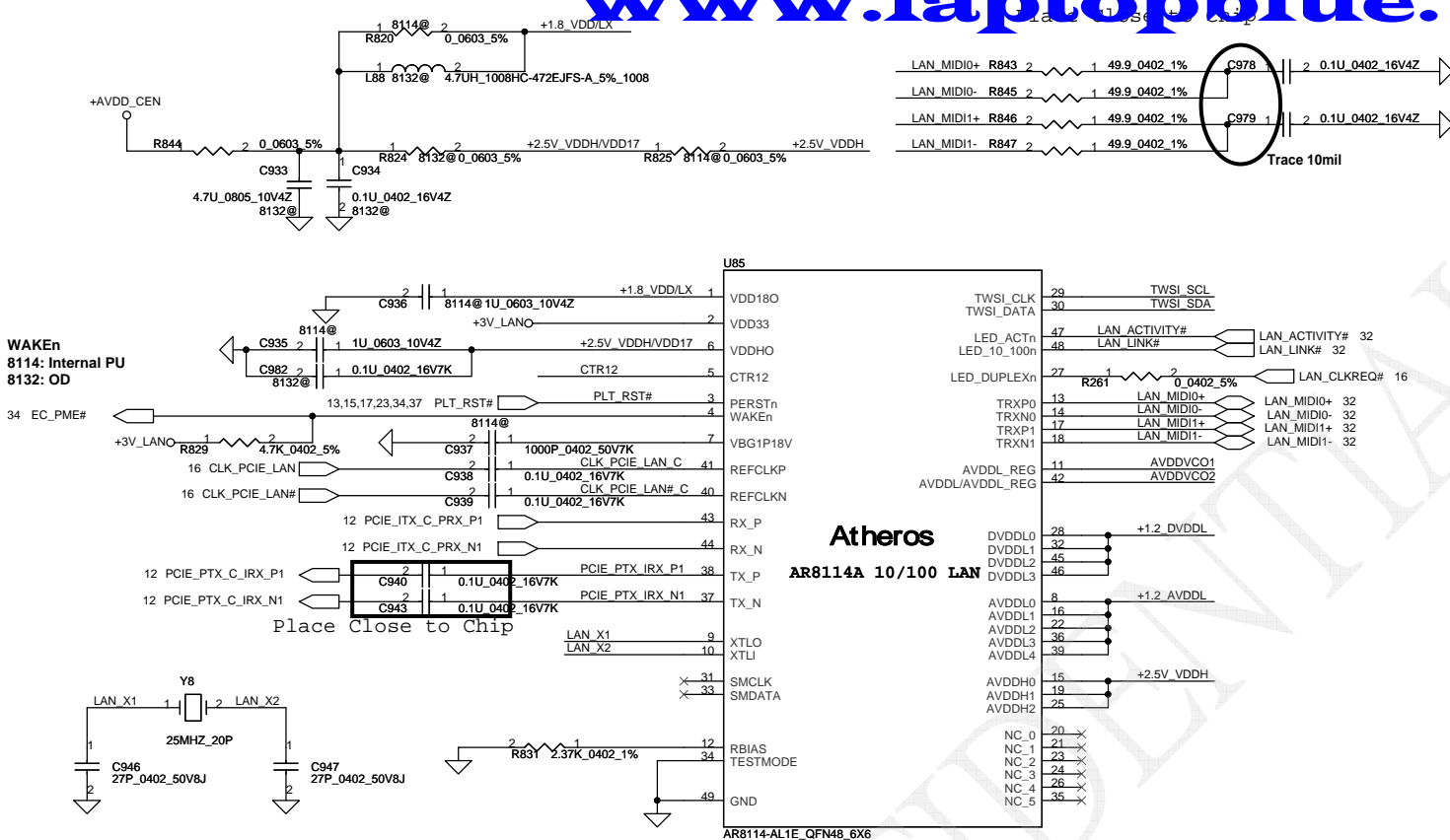
LCD/PANEL CONN.



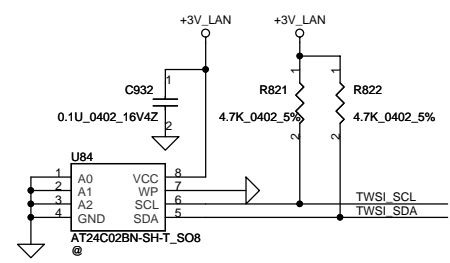
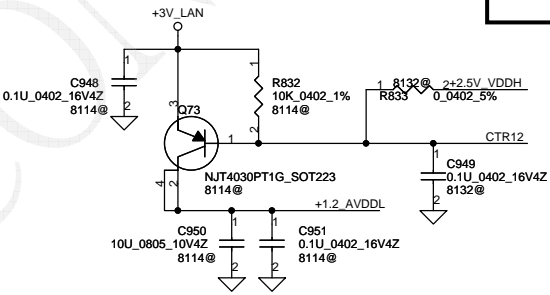
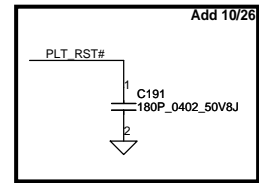
VARYBRIGHT FUNCTION



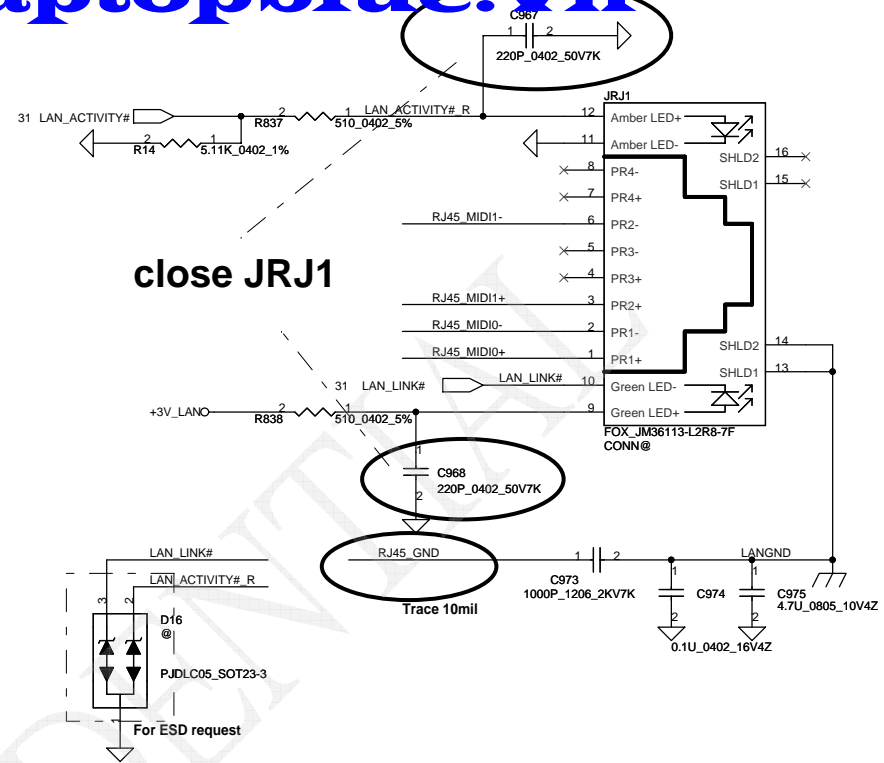
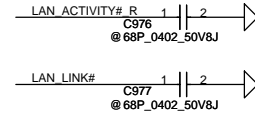
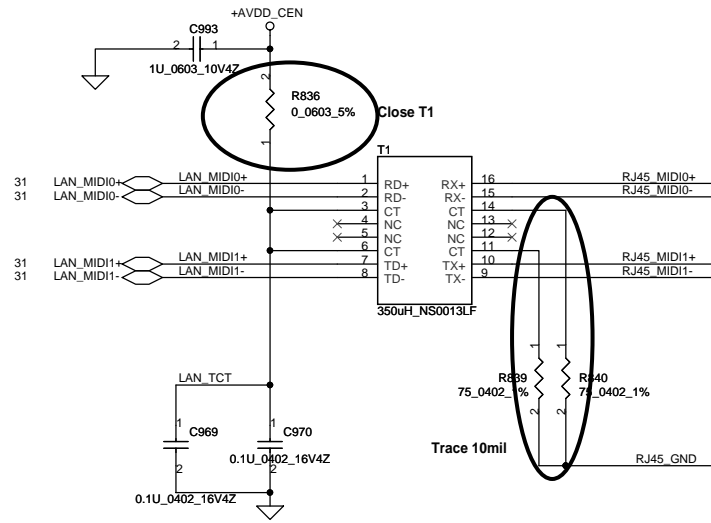
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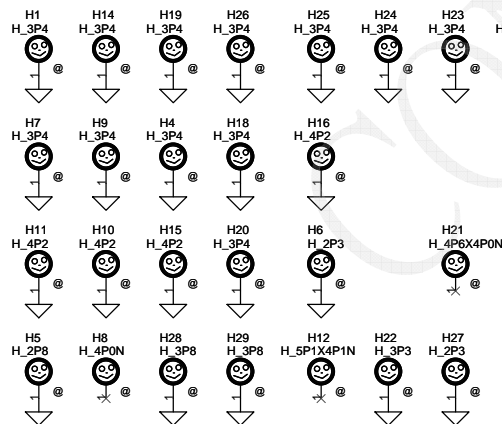
change to AR8132L-AL1E



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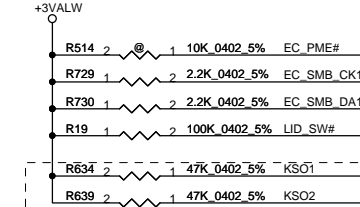
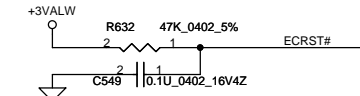
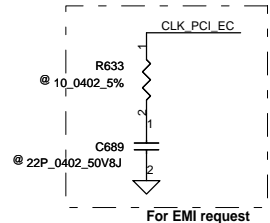
Screw Hole



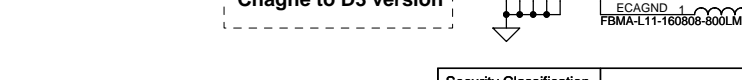
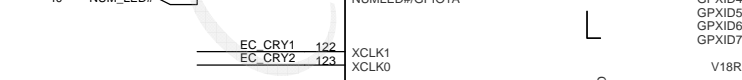
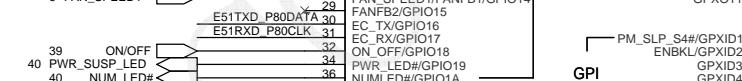
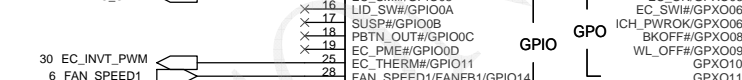
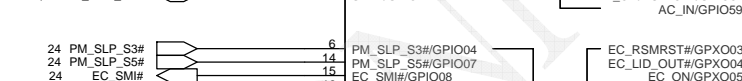
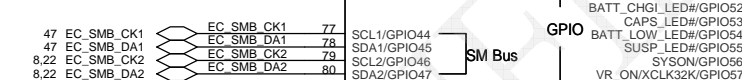
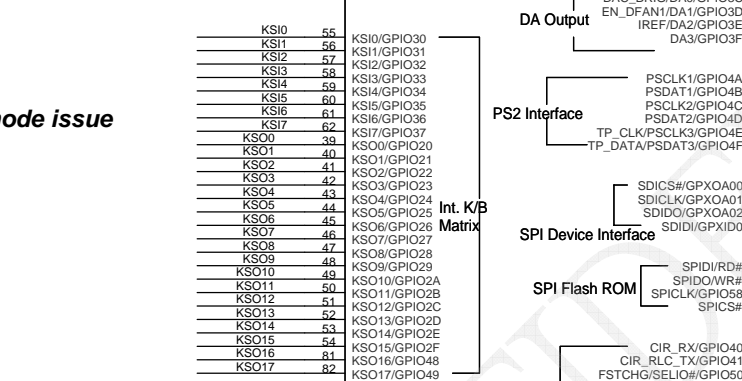
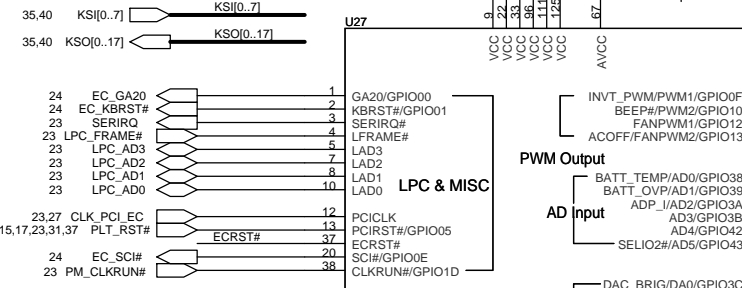
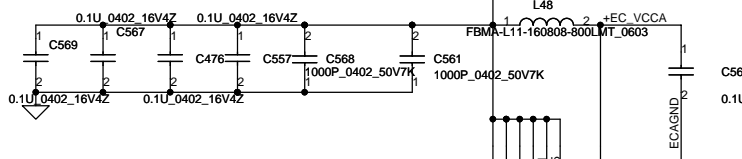
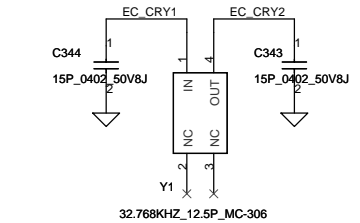
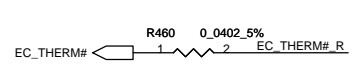
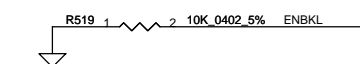
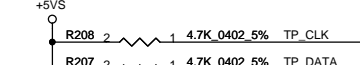
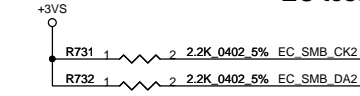
PCB Federal Mark PAD



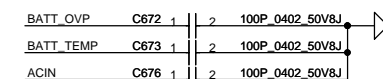
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EC test-mode issue

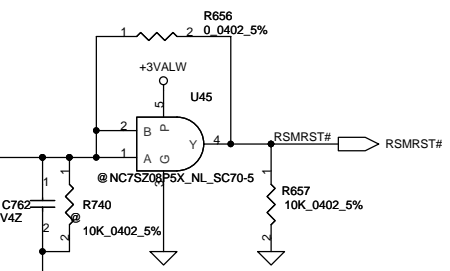
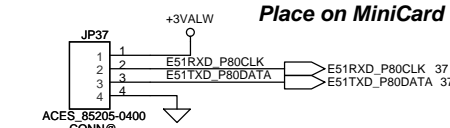


Please close to EC pin

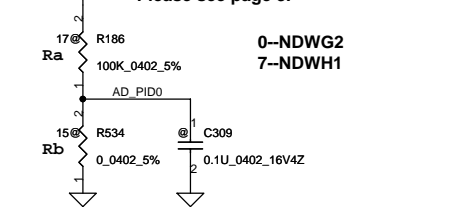


For EC Tools

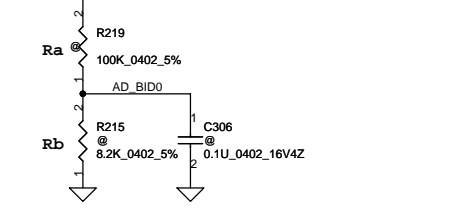
Place on MiniCard



Project ID Please see page 3.

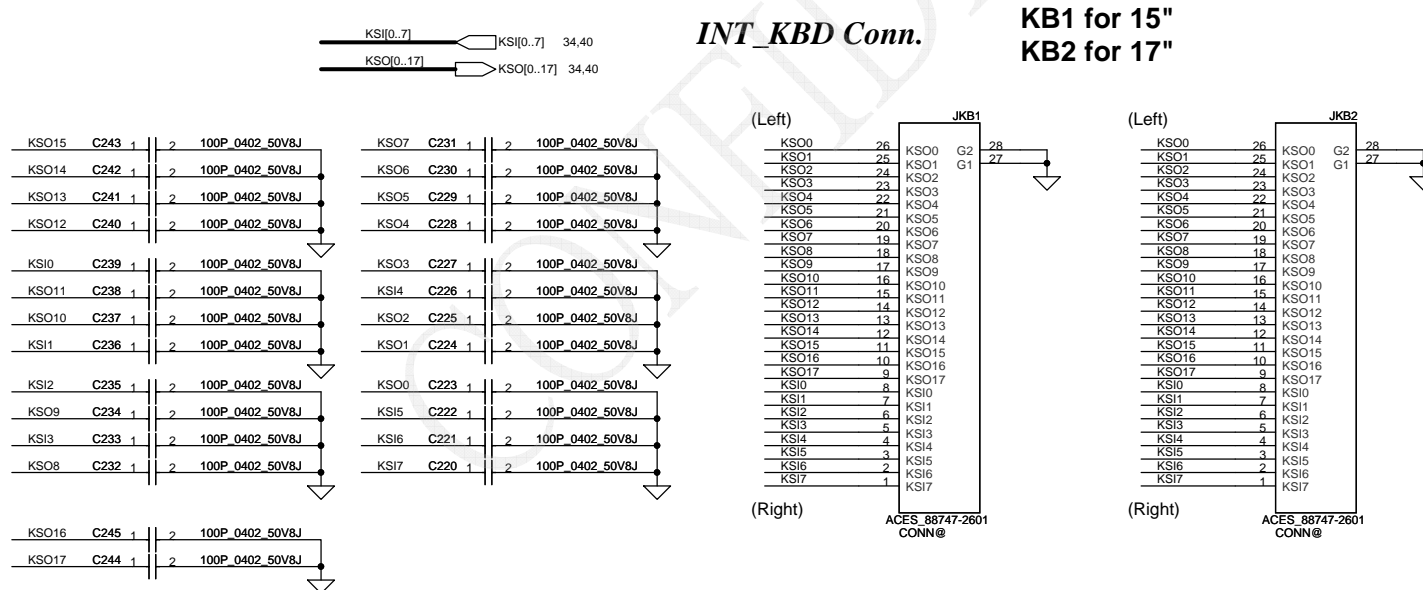
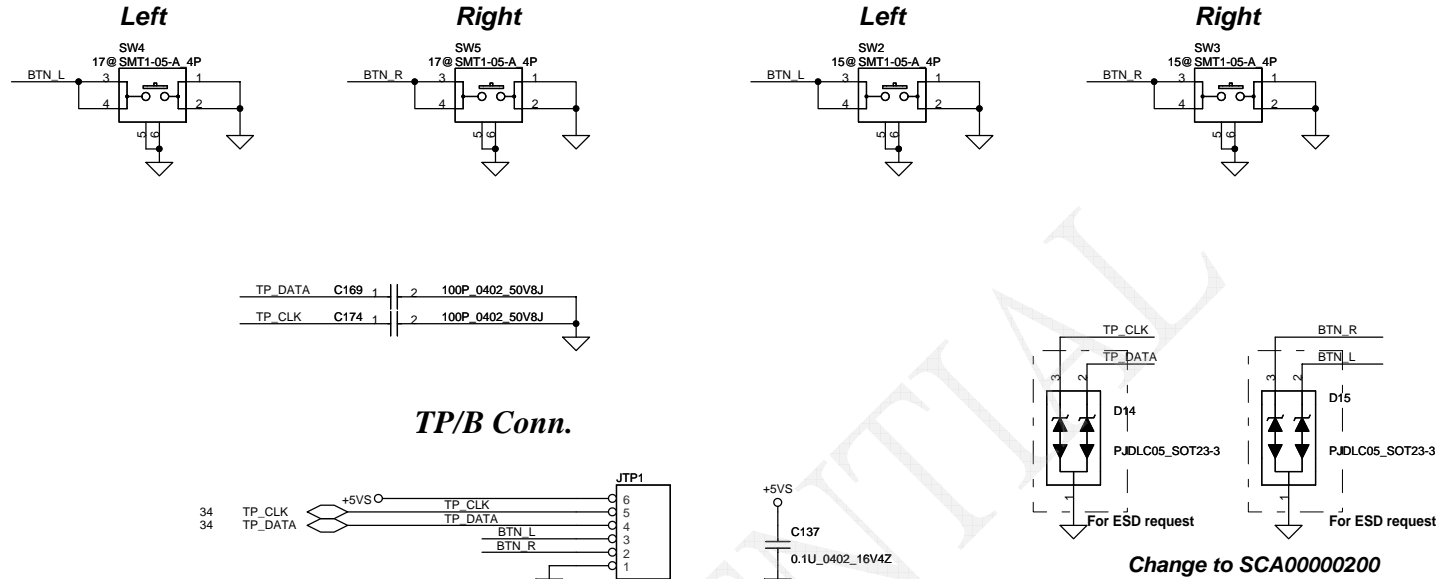


Board ID <VB support> Please see page 3.

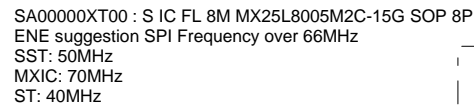




Chagne to D3 version

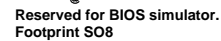
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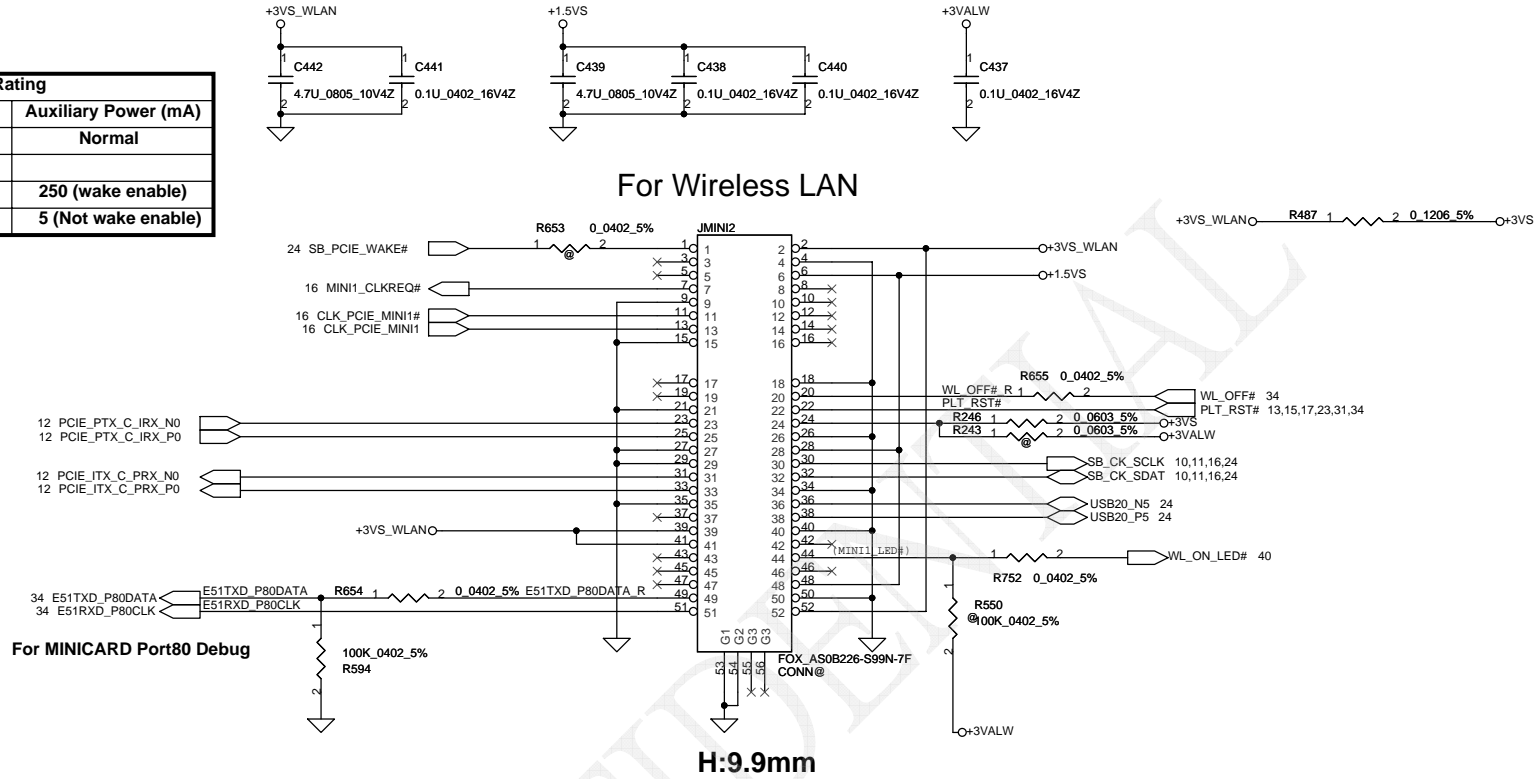


EC_SPICLK_R 1  2 R257
@ 22_0402_5%
1  2 C296
@ 10P_0402_50VBJ
For EMI request



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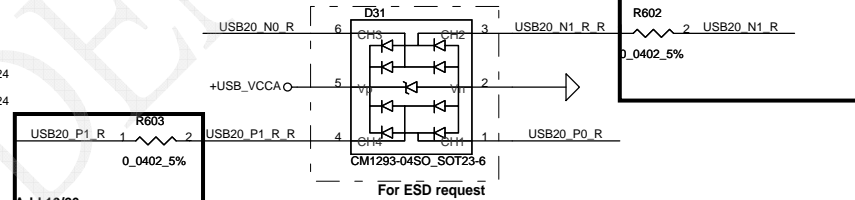
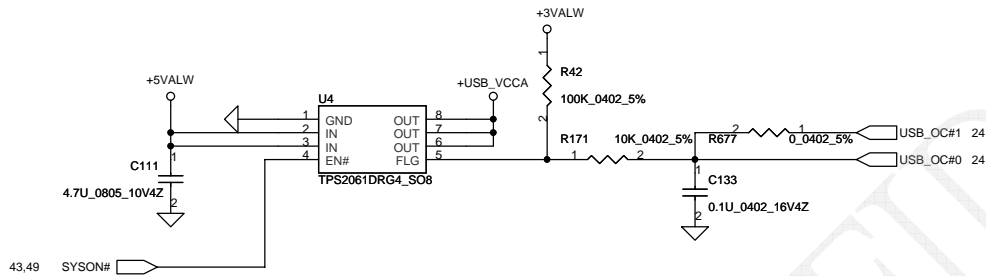
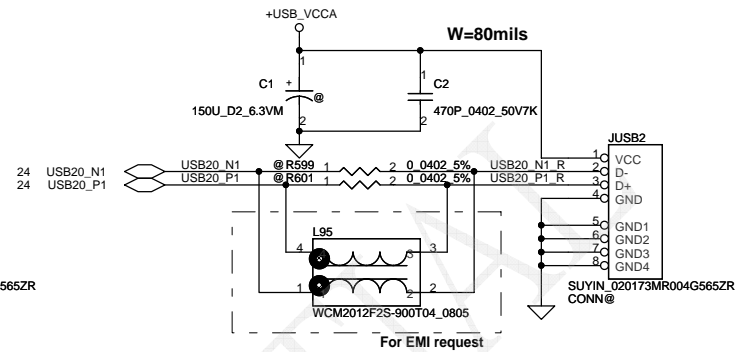
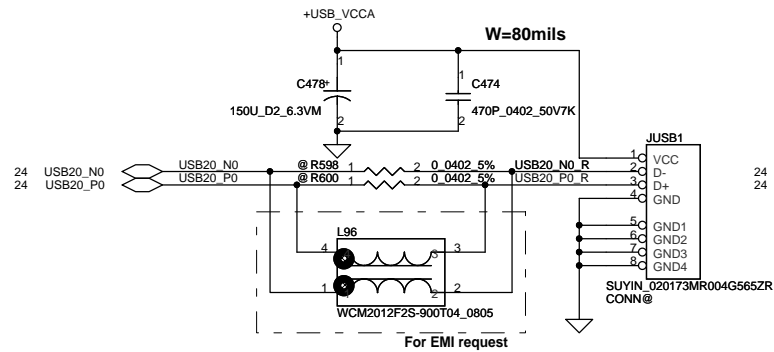
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



H:9.9mm

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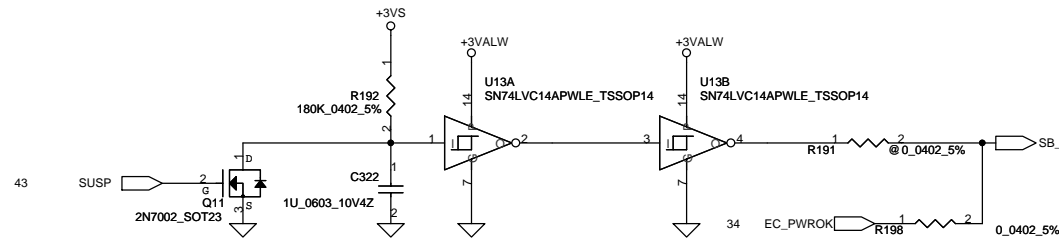
USB CONN. 1 & 2



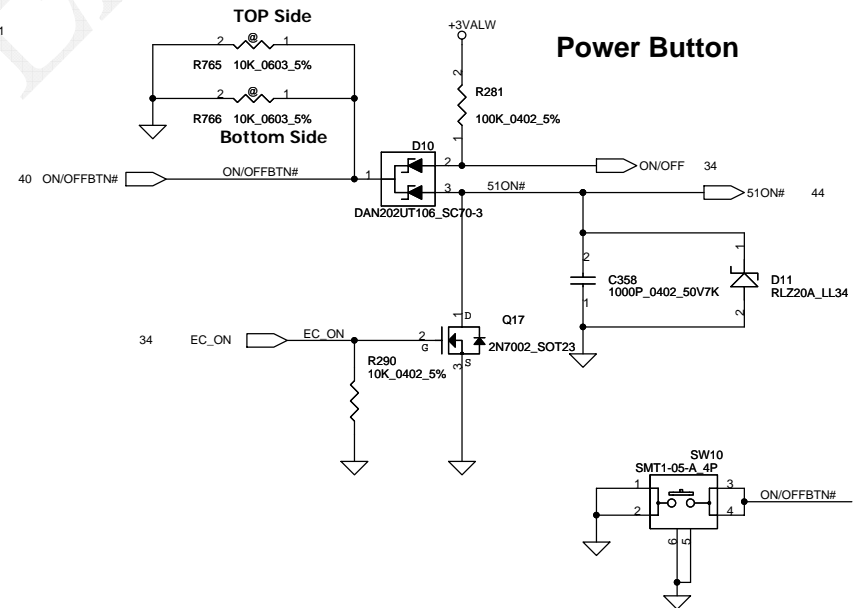
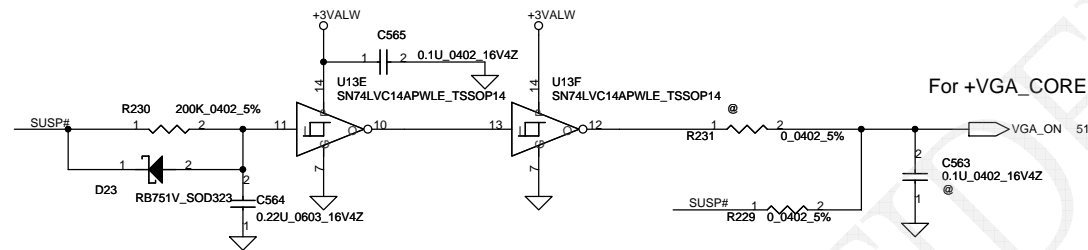
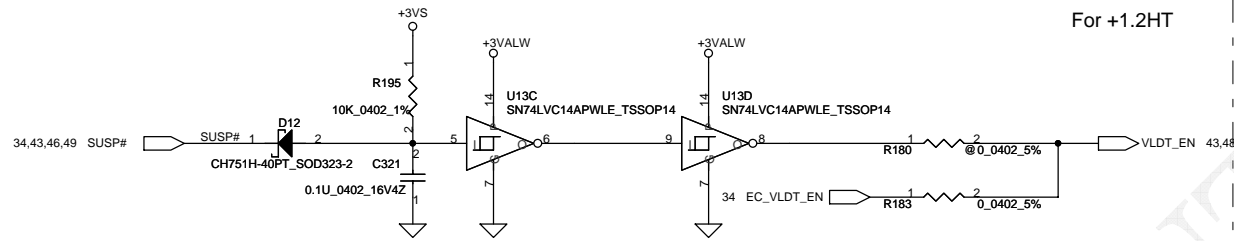
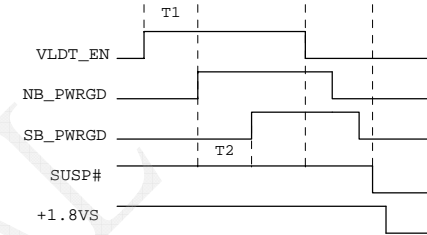
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Power On Circuit

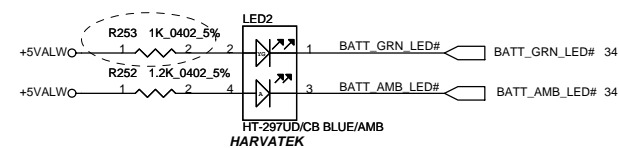
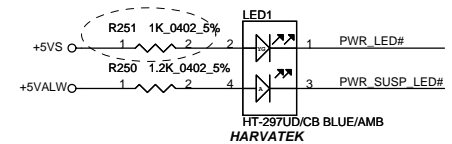
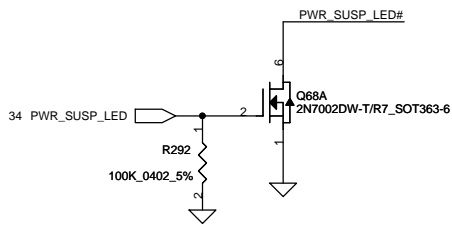
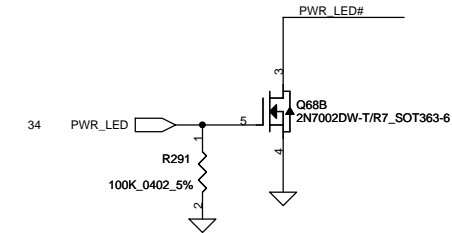
For South Bridge



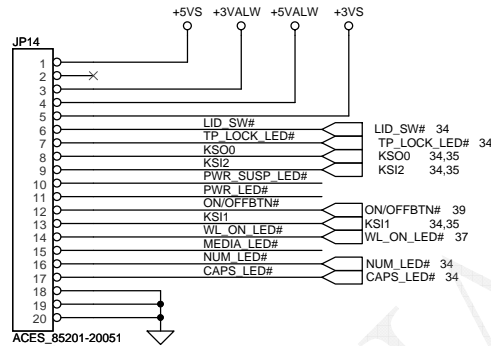
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power down.



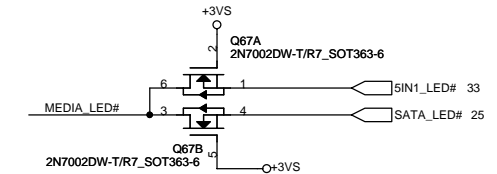
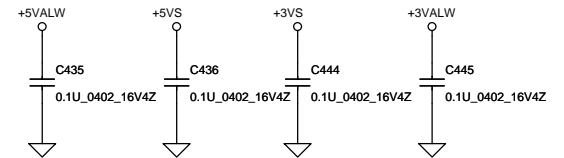
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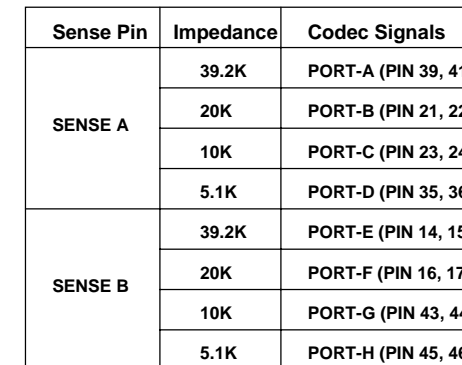
BLUE/AMB LED



	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	

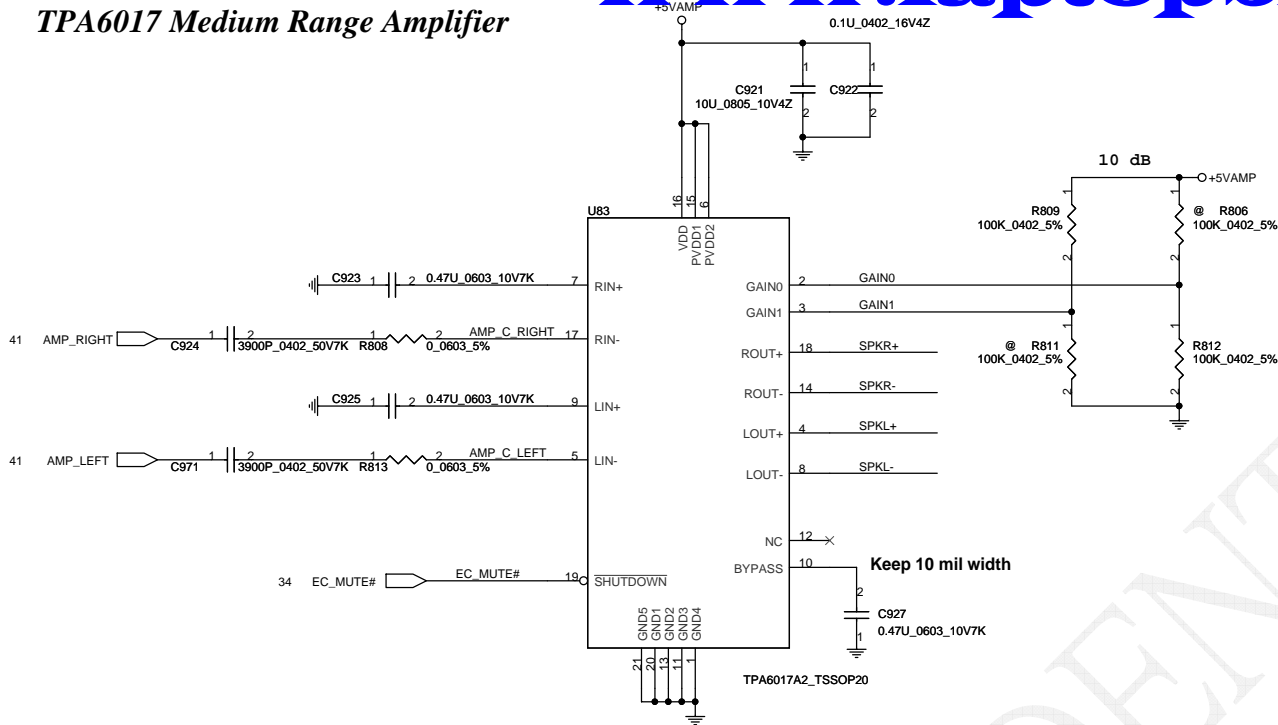


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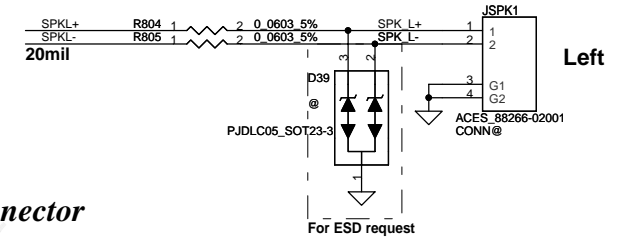


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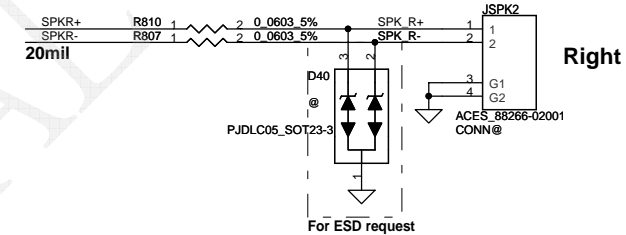
TPA6017 Medium Range Amplifier



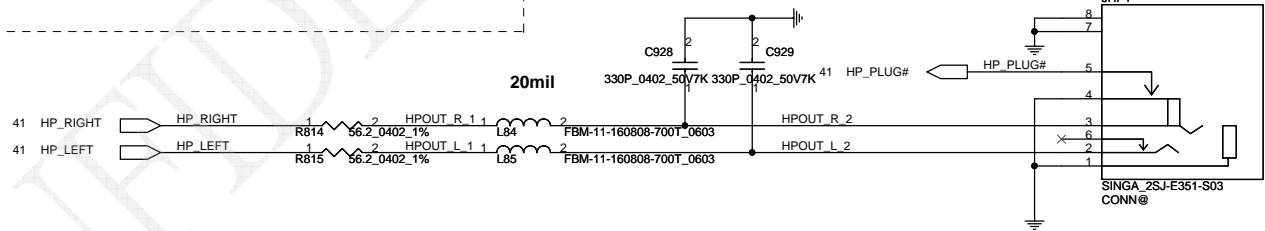
Left Connector



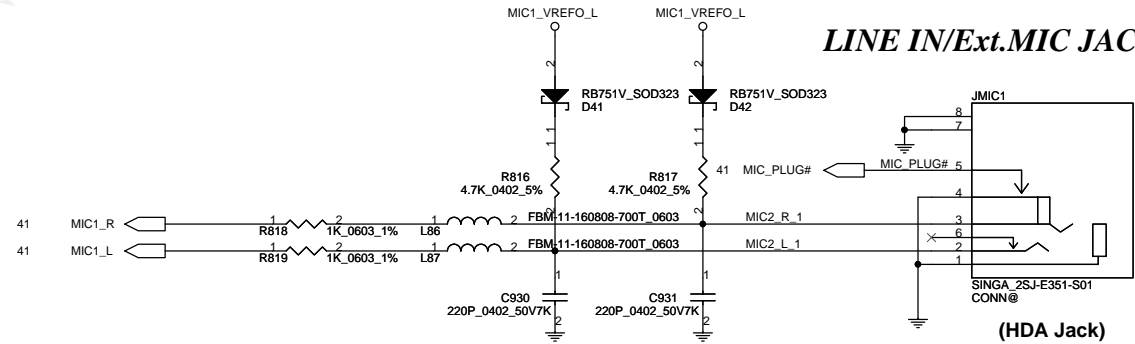
Right Connector



LINE Out/Headphone Out

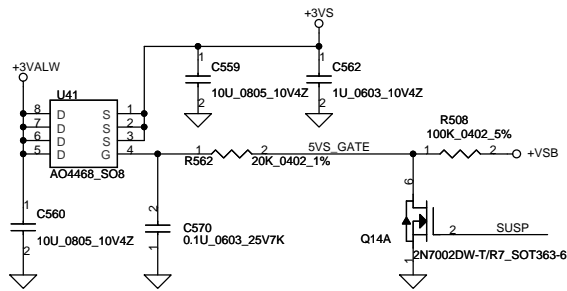


LINE IN/Ext.MIC JACK

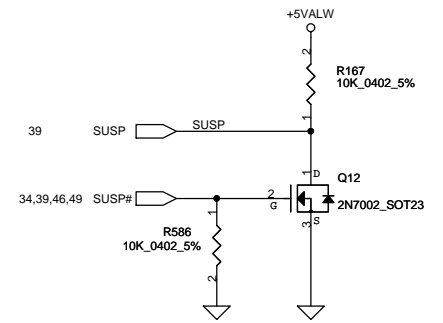
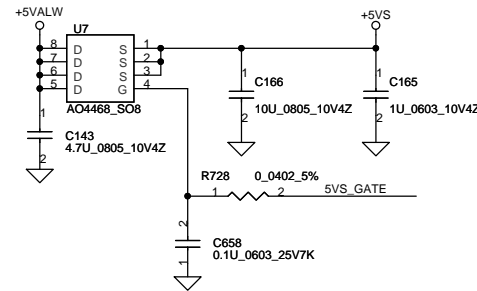


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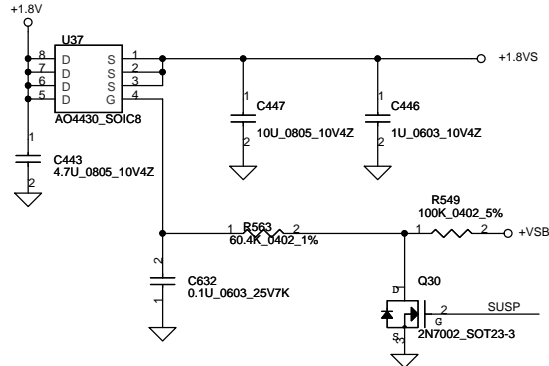
+3VALW TO +3VS



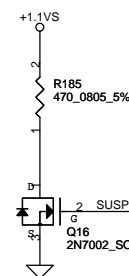
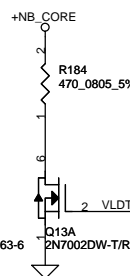
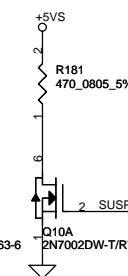
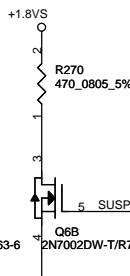
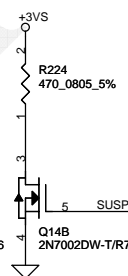
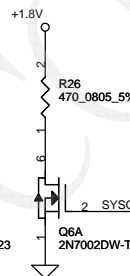
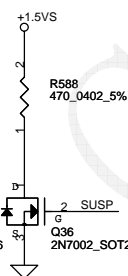
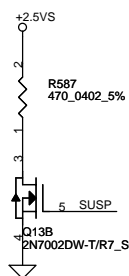
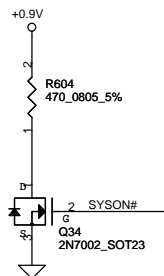
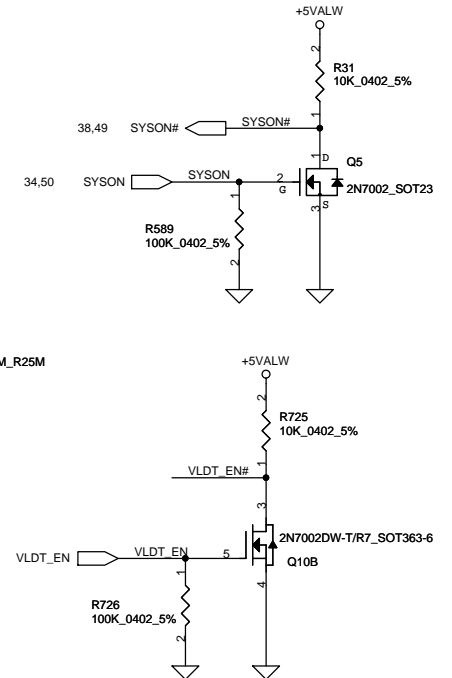
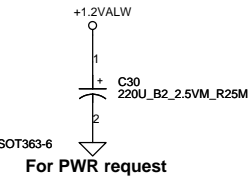
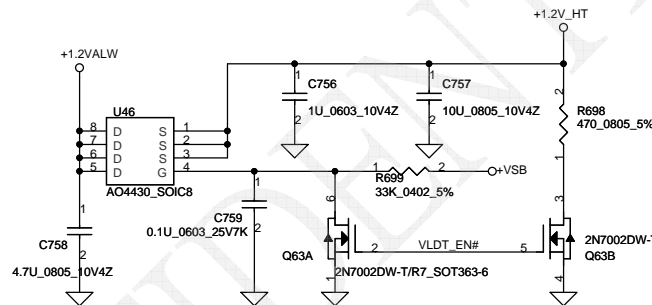
+5VALW TO +5VS



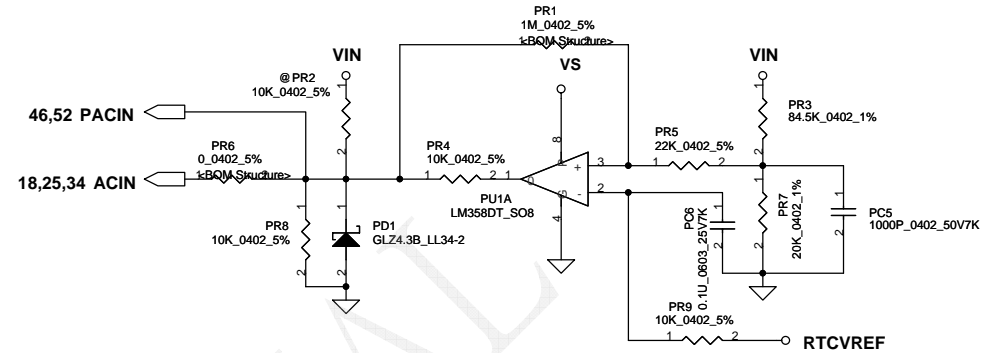
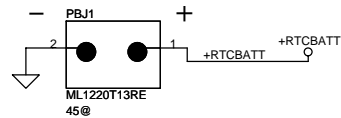
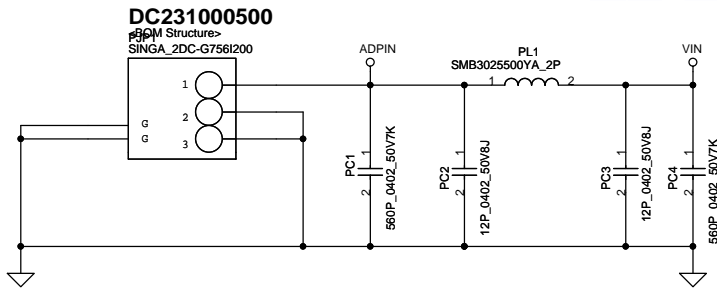
+1.8V TO +1.8VS



+1.2VALW TO +1.2V_HT

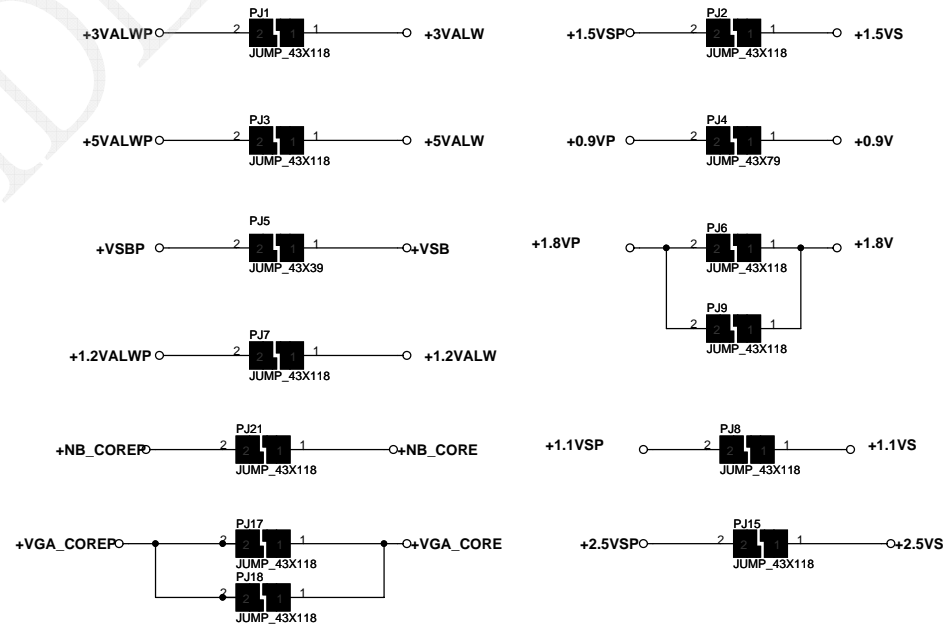
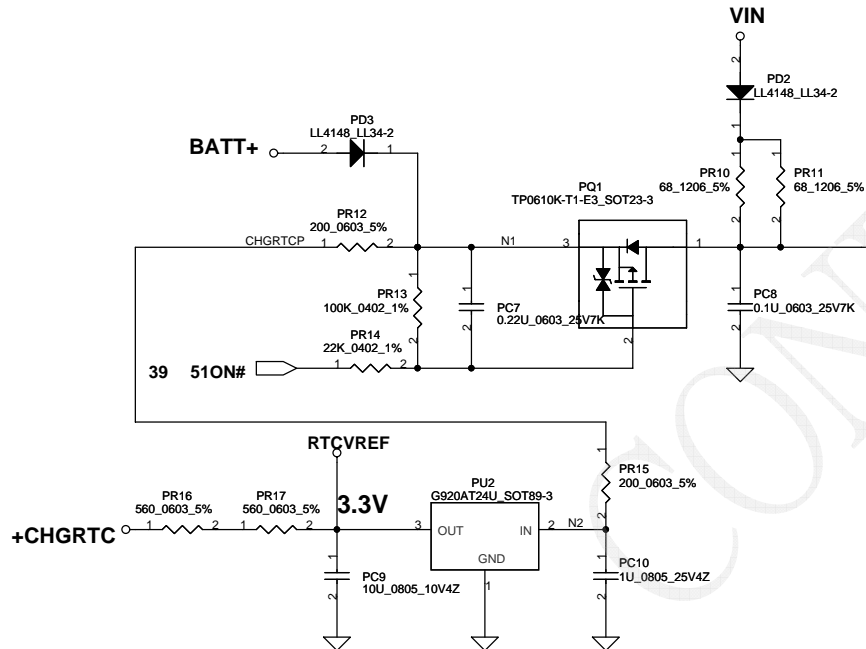


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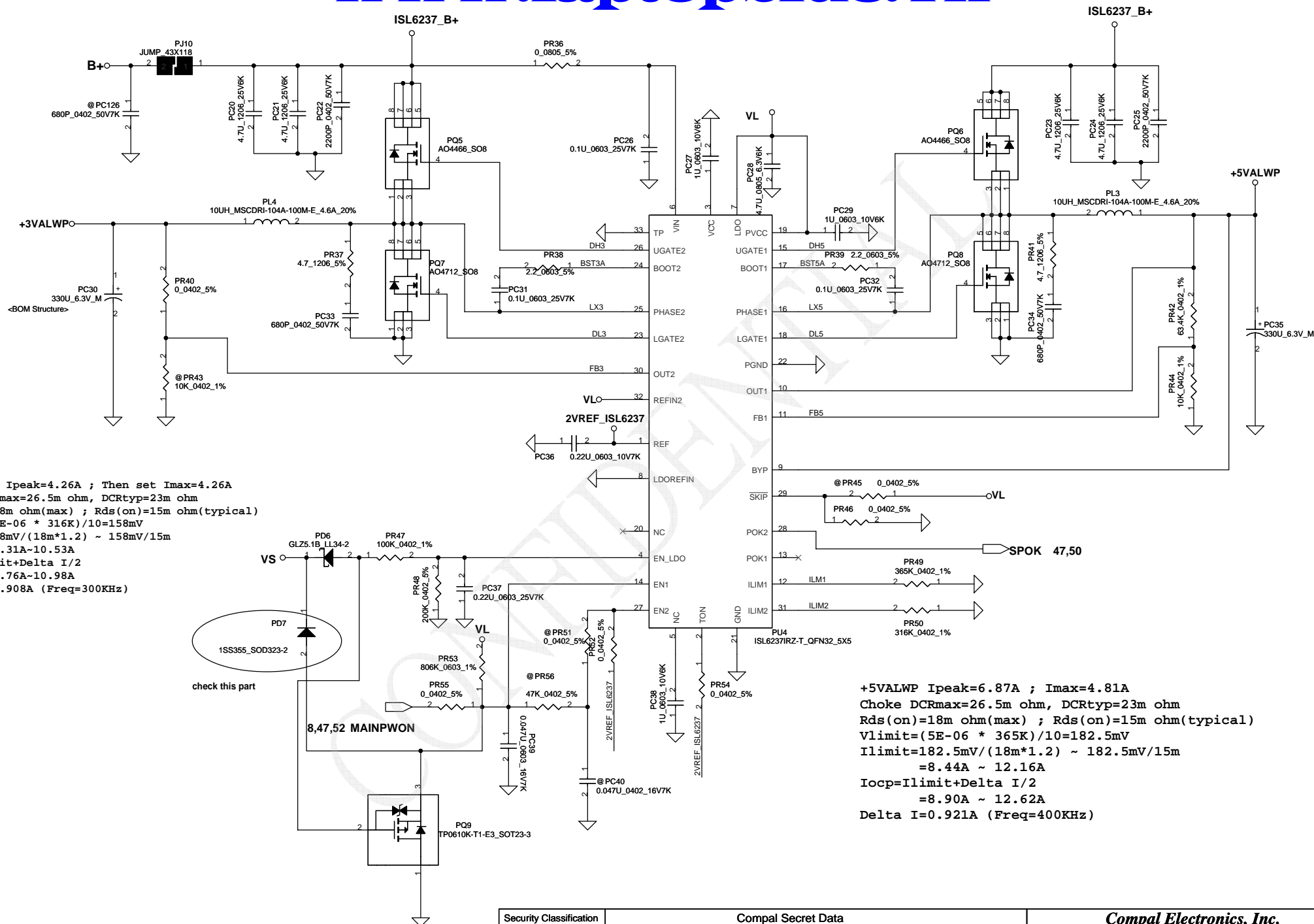


Vin Detector

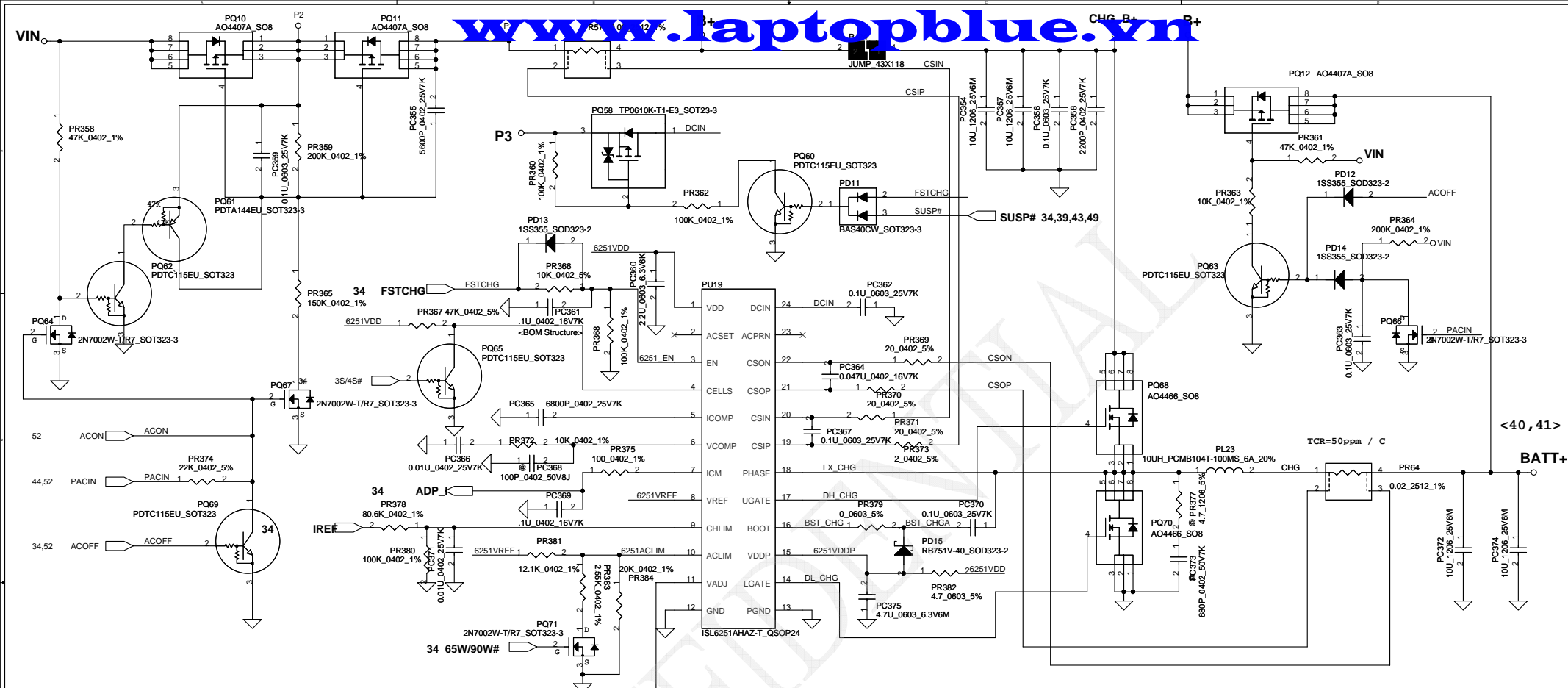
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

CC=0.6~4.48A
 $I_{ref} = 0.7224 * I_{charge}$
 $\Rightarrow K_i = 0.7224$
 $I_{REF} = 0.43V \sim 3.24V$

K_i
 $V_{chlim} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{chlim} / 3.3V)$
 $= (165m / 20m) * (1 / 3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow K_i = 0.7224$

K_v
 $R_{internal} = 514K$, $R_{ec} = 3K$, $R_1 = PR379 = 15.4K$, $R_2 = PR381 = 31.6K$
 $R = 514K // 31.6K // (15.4K + 3K) = 11.372K$
 $r = 514K // 514K // 31.6K = 28.14K$
 $V_{cell} = 0.175 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell} + A * 0.175)) * K_v = (4.2 - (4.2 + A * 0.175)) * K_v$
 $A = V_{ref} * (R / (R + 514K)) = 0.052$
 $K_v = 9.451$

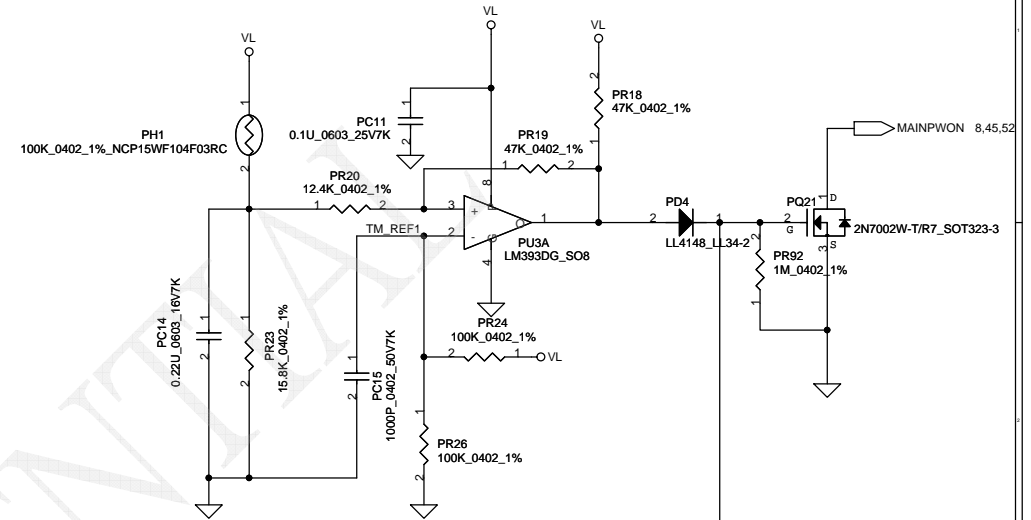
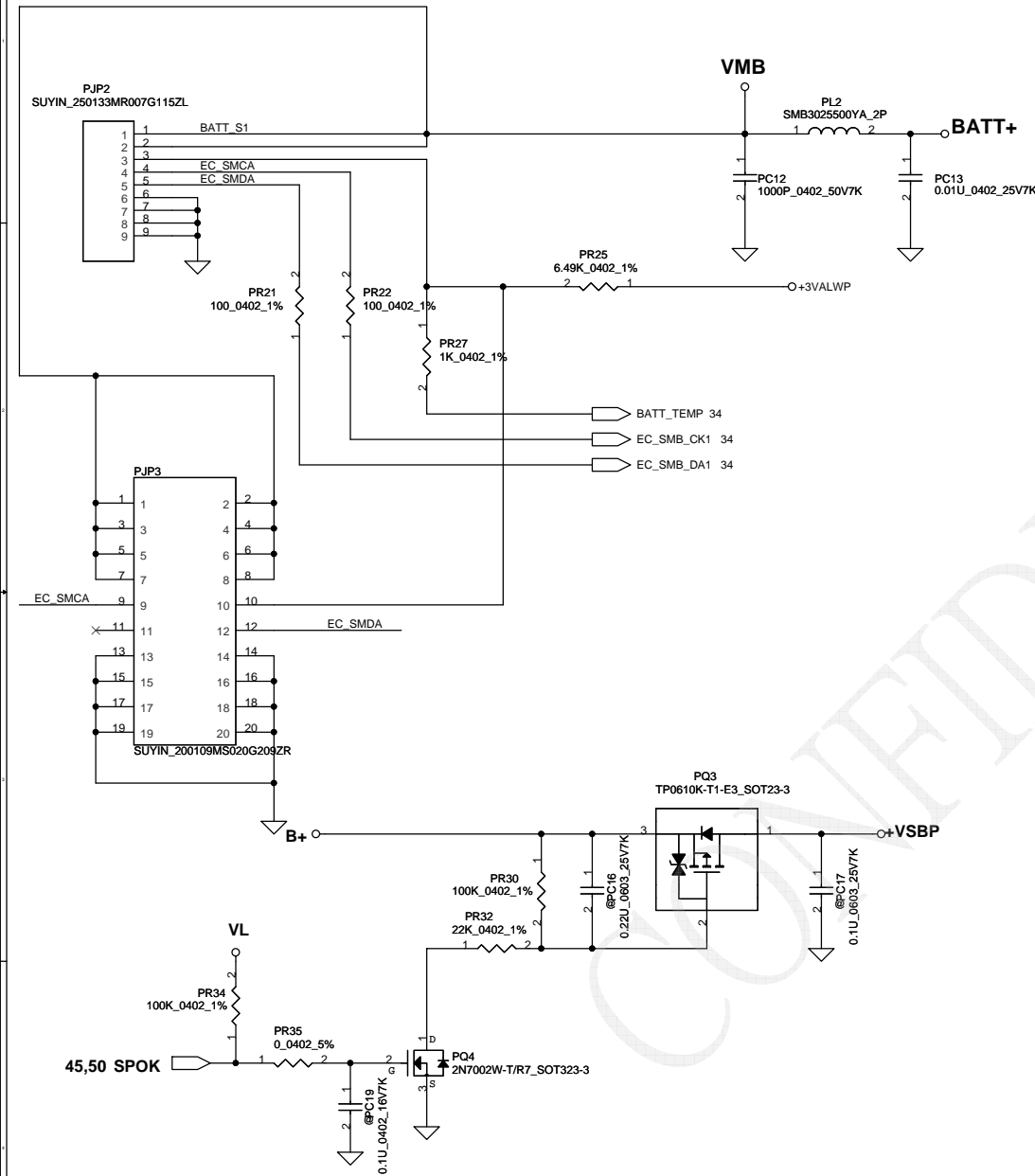
LI-3S :13.5V---BATT-OVP=2.007V
BATT-OVP=0.1487*VMB
Per cell=3.5V

Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

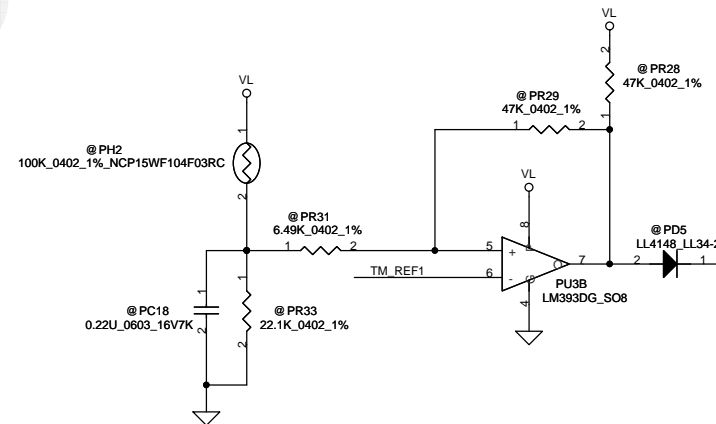
34 BATT_OVP

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

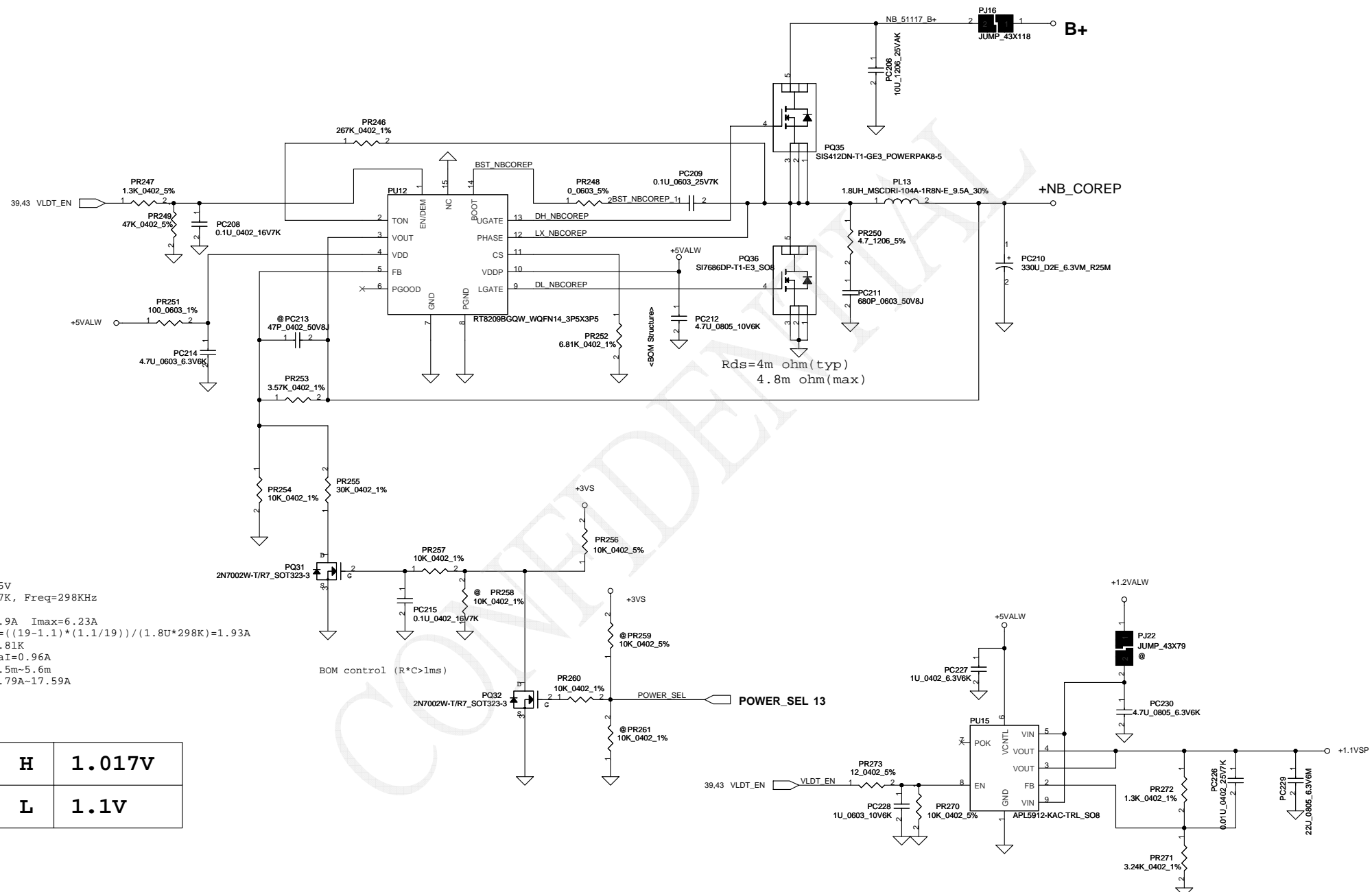
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C

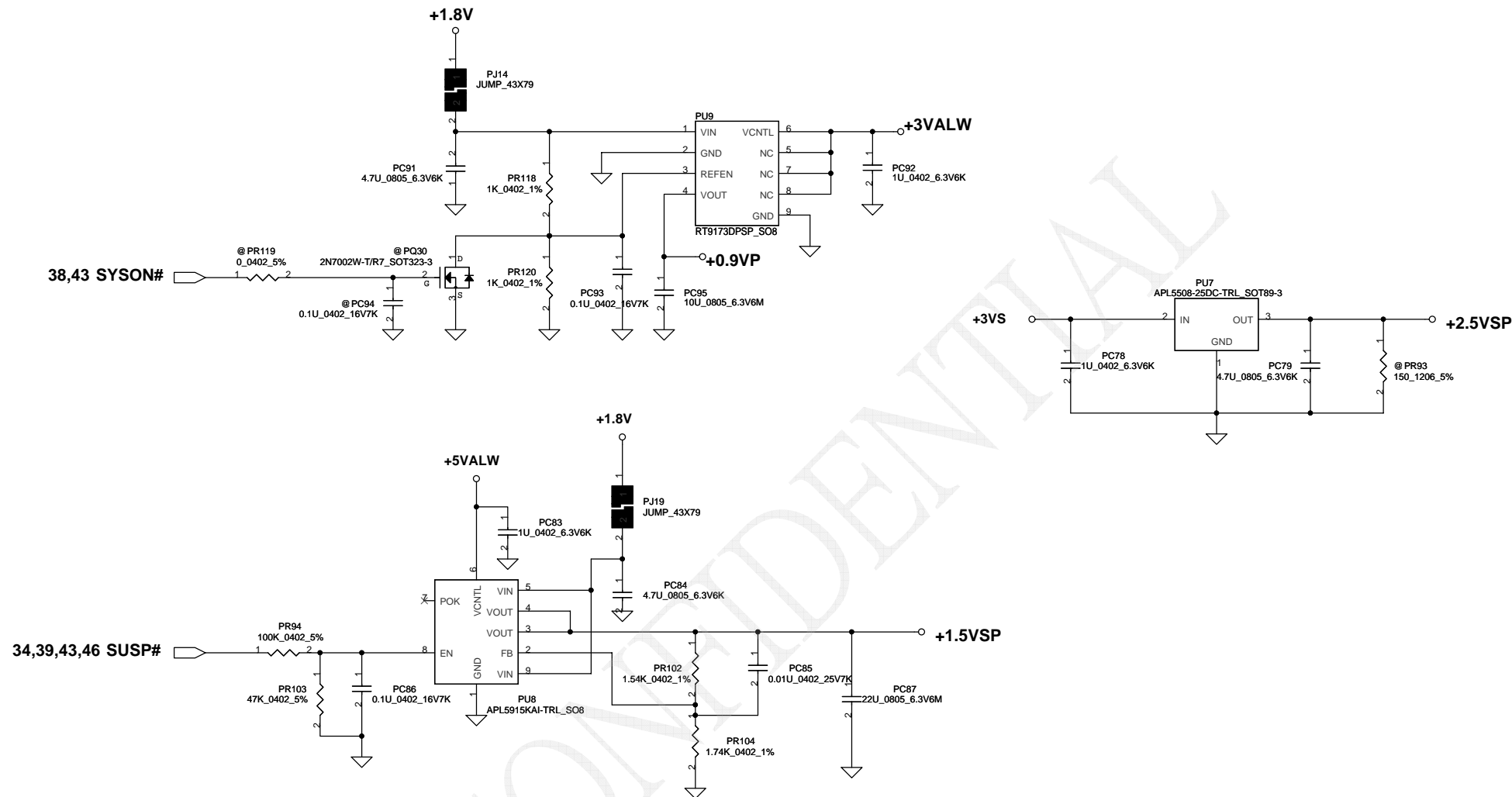


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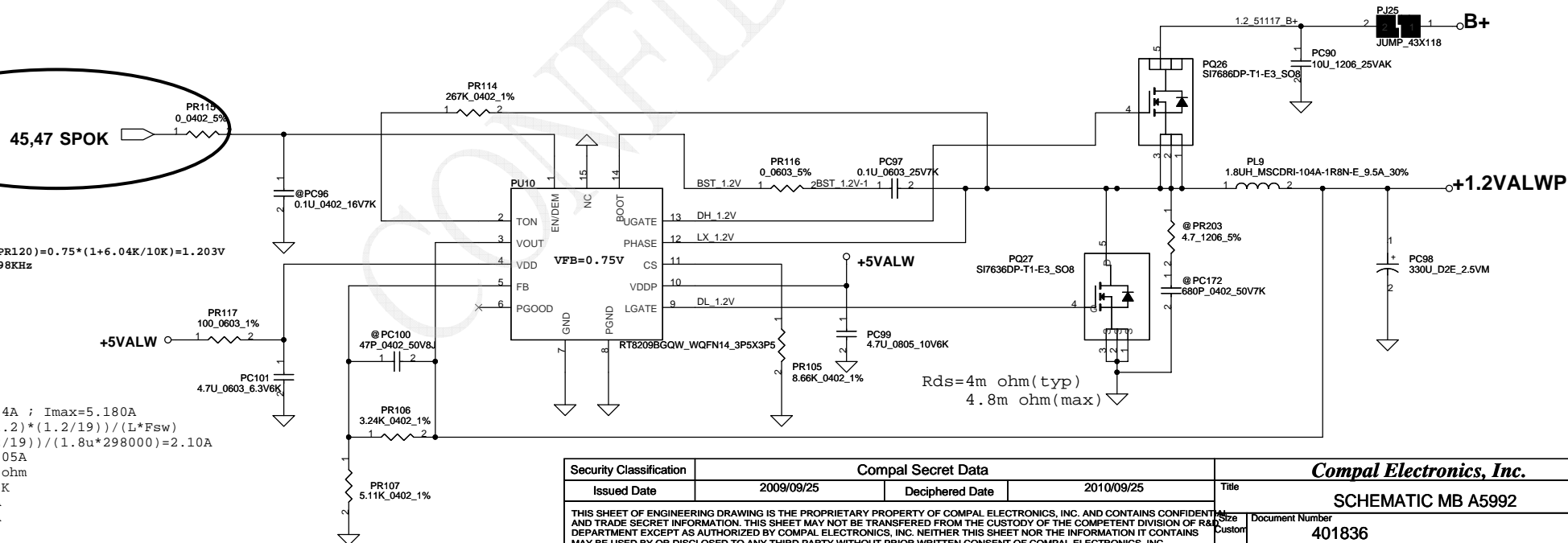
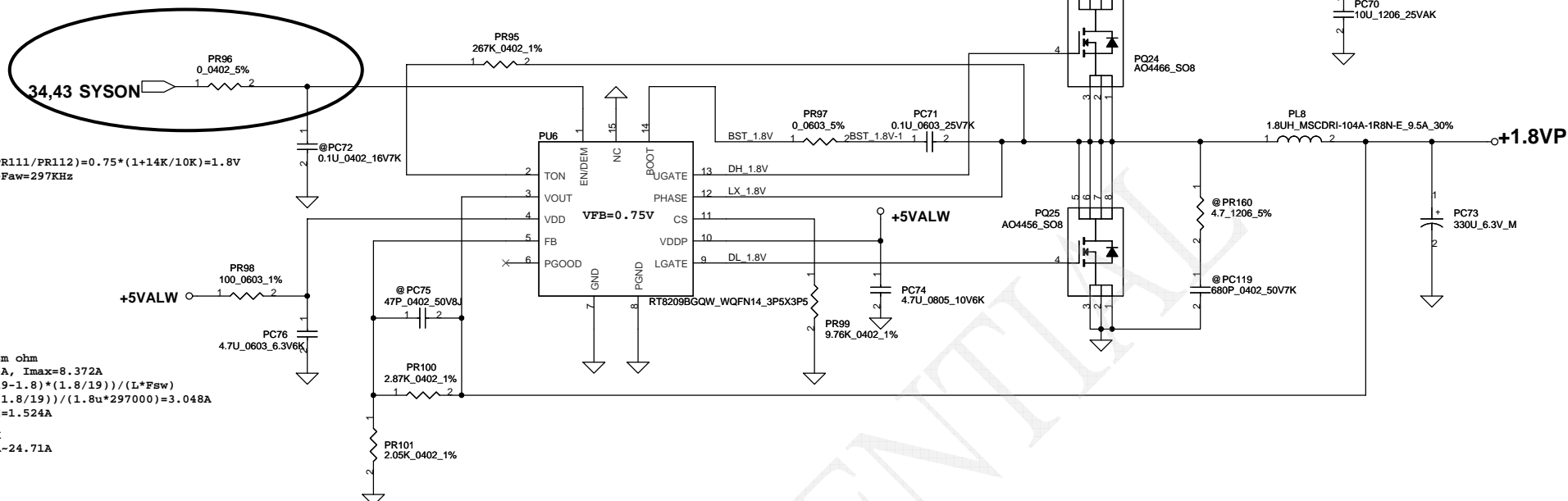


H	1.017V
L	1.1V

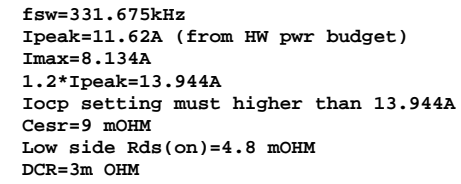
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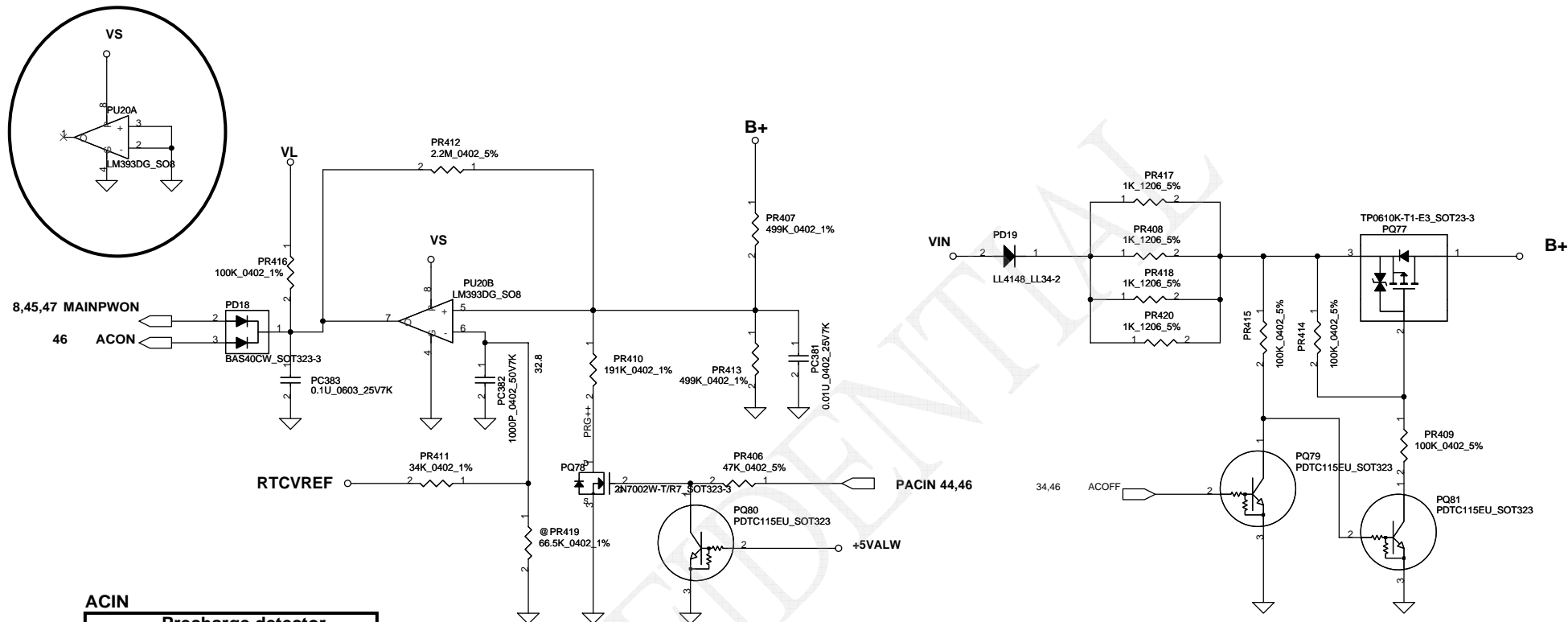


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		M92-S2 XT
VGA_PWRSEL_0	VGA_PWRSEL_1	Core Voltage Level
0	0	1.20V
0	1	1.14V
1	0	0.96V
1	1	0.90V

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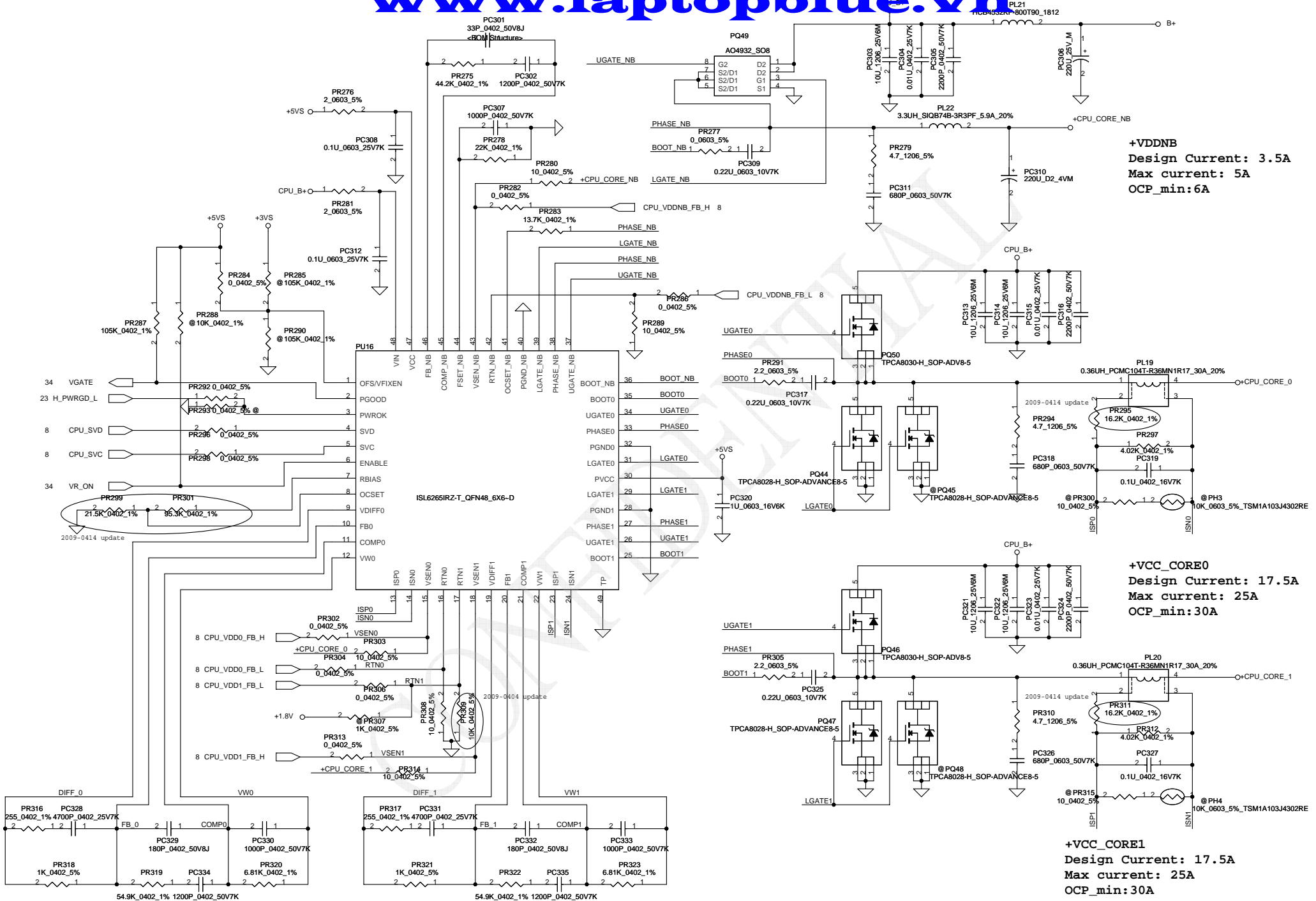
ACIN

Precharge detector			
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW required to adjust from 1.14V to 1.12V	HW required to adjust from 1.14V to 1.12V	0.1	42	Change PR271 from SD034300180 (S RES 1/16W 3K +-1% 0402) to SD034324180 (S RES 1/16W 3.24K 0402 1%)	09, 05/07	to PVT
2	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Add PC208 SE076104K80 (S CER CAP .1U 16V K X7R 0402)	09, 05/07	to PVT
3	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Change PR247 from SD028000080 (S RES 1/16W 0 +-5% 0402) to SD028130180 (S RES 1/16W 1.3K 0402 5%)	09, 05/07	to PVT
4	NB_COREP working frequency has issue.	Because NB_COREP working frequency will be glitter while system at heavy loading. Change to larger ESR Cap will be solve.	0.1	42	Change PC210 from SGA19331D00 (S POLY C 330U 2.5V M D2 TPE LESR15M H1.8) to SGA00002B00 (S POLY C 330U 6.3V M D2E ESR25M TPE H1.8)	09, 05/07	to PVT
5	BOM error	BOM error	0.1	42	Add PR270 SD28100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
6	BOM error	BOM error	0.1	42	Change PR103 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
7							
8	Change Power Source	For WLAN wakeup	1.0	37	Change R550 to +3VALW	09, 05/07	Pre-MP
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							

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