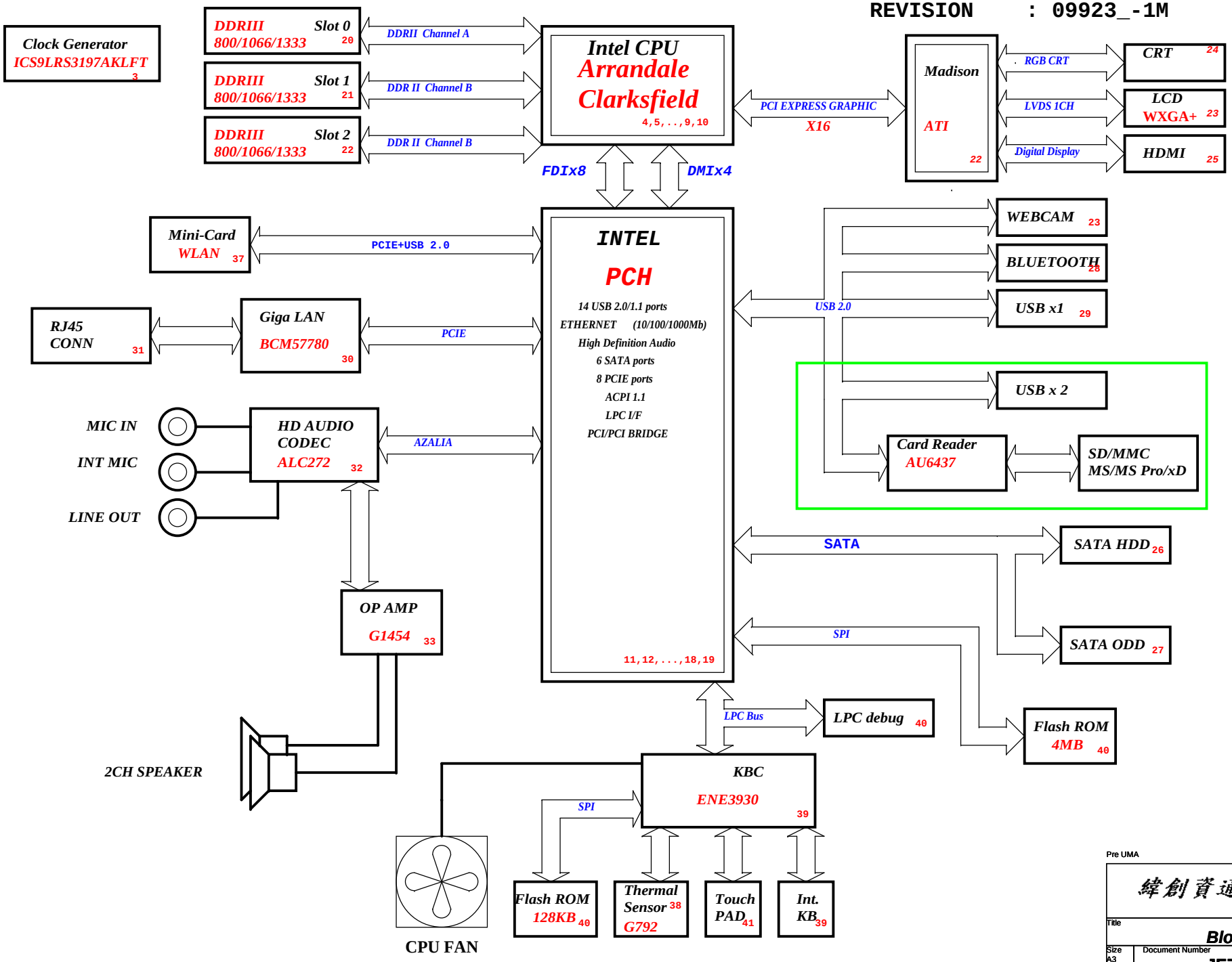
JE70-CP Block Diagram

Project code : 91.4HN01.001
PCB P/N : 48.4HN01.0SD
REVISION : 09923_-1M



SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 47

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 48

SYSTEM DC/DC RT8209B	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 49

SYSTEM DC/DC TPS51611	
INPUTS	OUTPUTS
DCBATOUT	GFX_CORE 52

CPU DC/DC TPS51621	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 45,46

MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
DCBATOUT	BT+ 51

PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

Pre UMA

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

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Title: Table of Content

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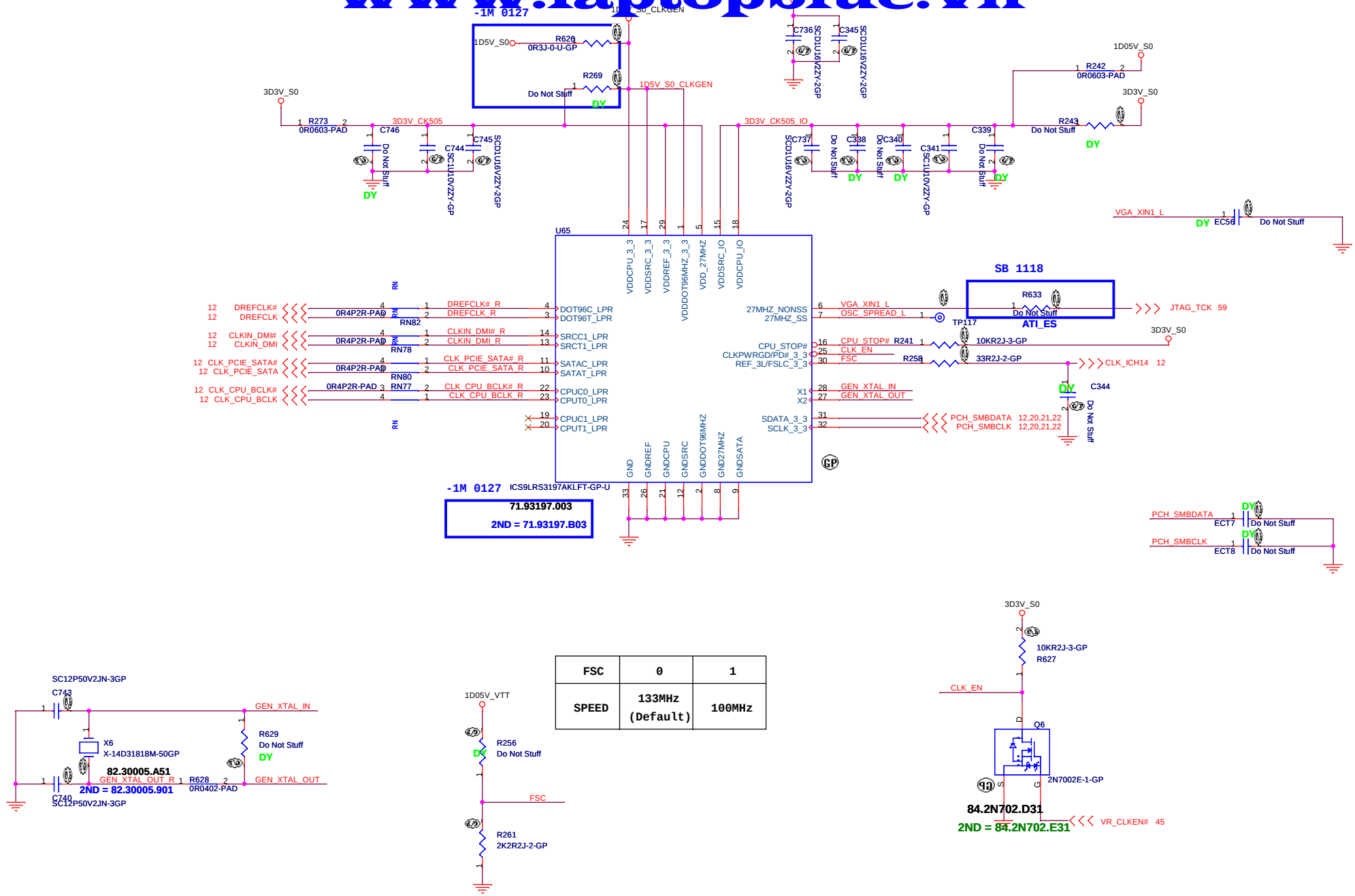

FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator

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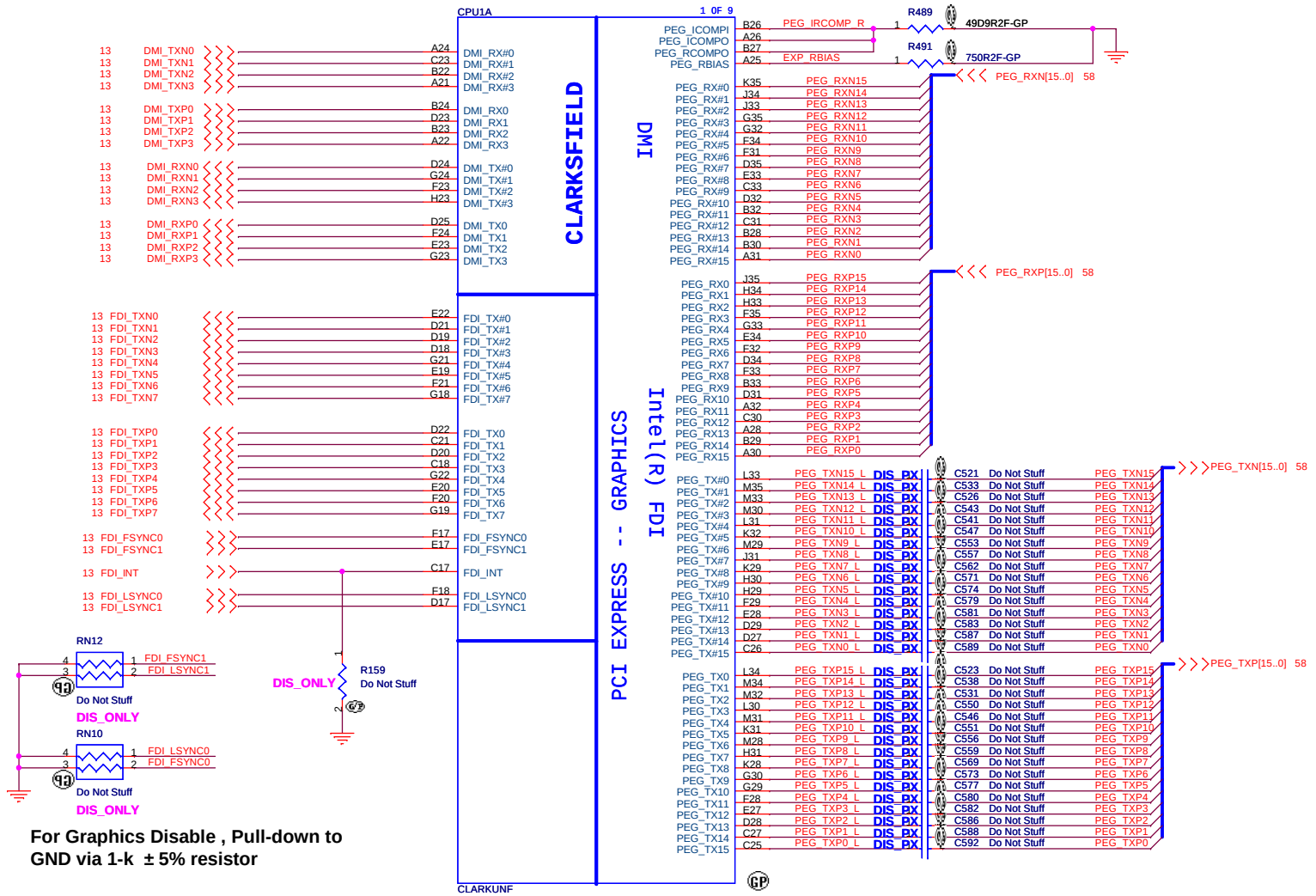

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Title: CPU (1/7)		
Size: A3	Document Number: JE70-CP	Rev: -1M
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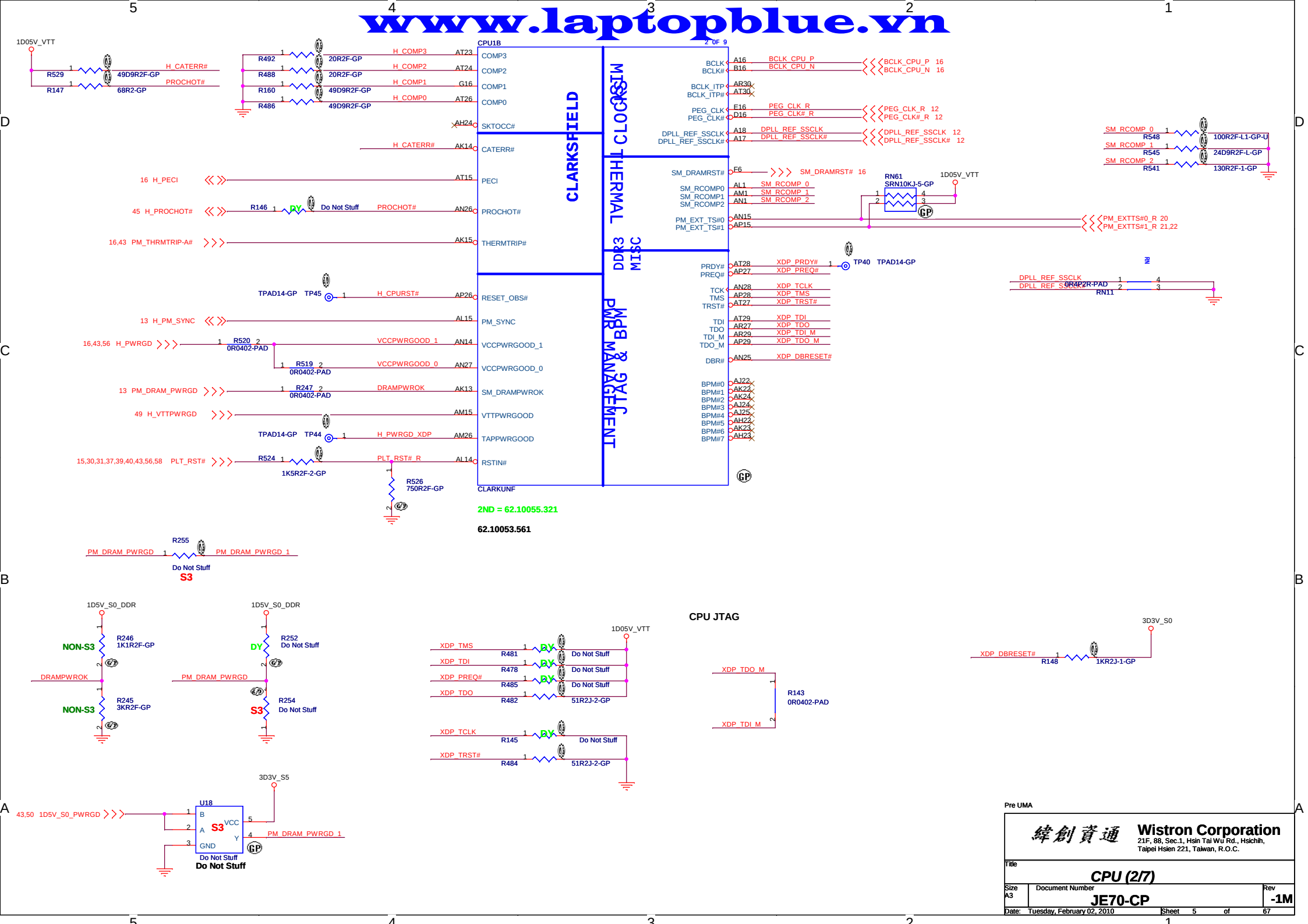

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Title: CPU (2/7)

Size	Document Number	Rev
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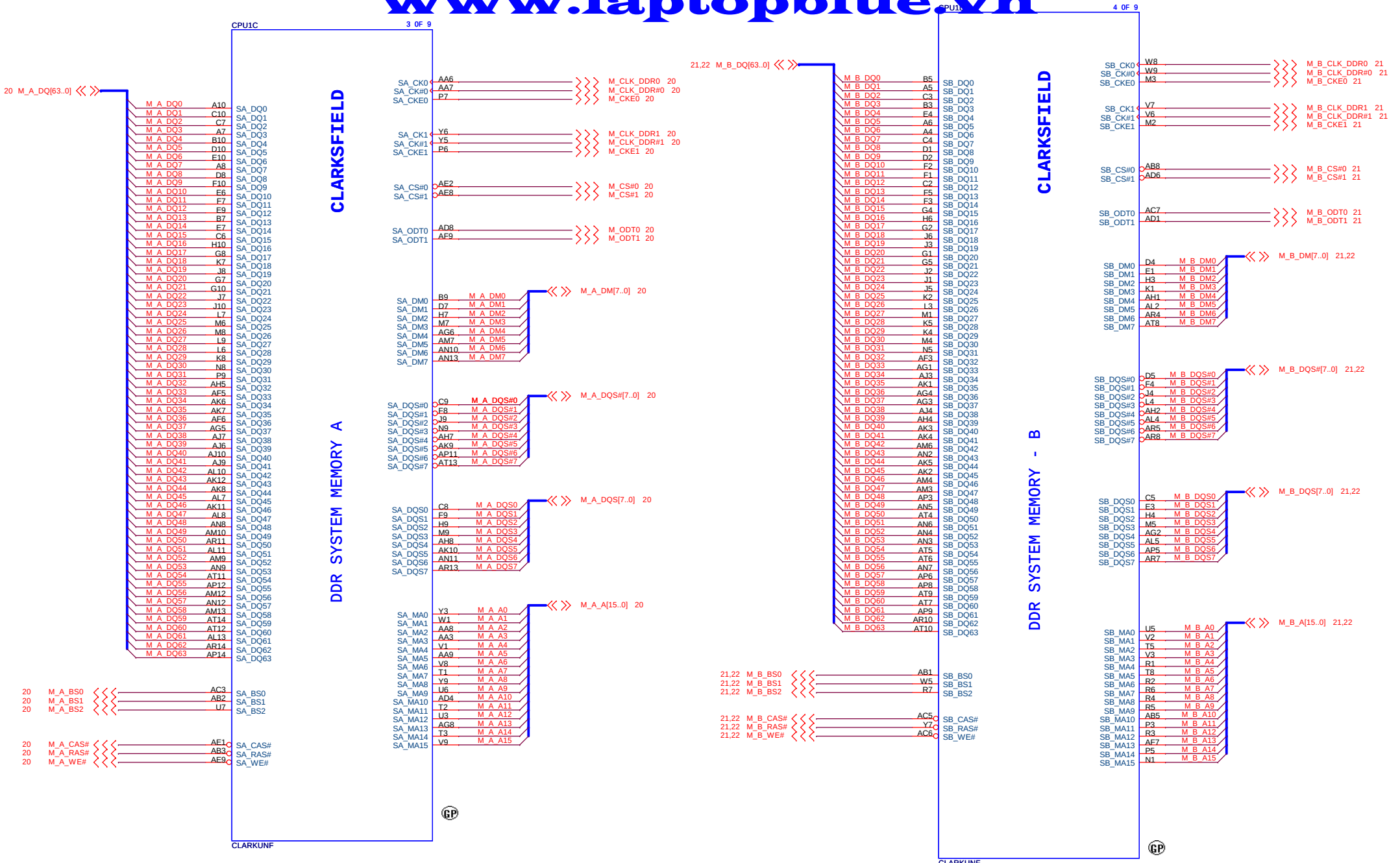

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Title: CPU (3/7)

Size	Document Number	Rev
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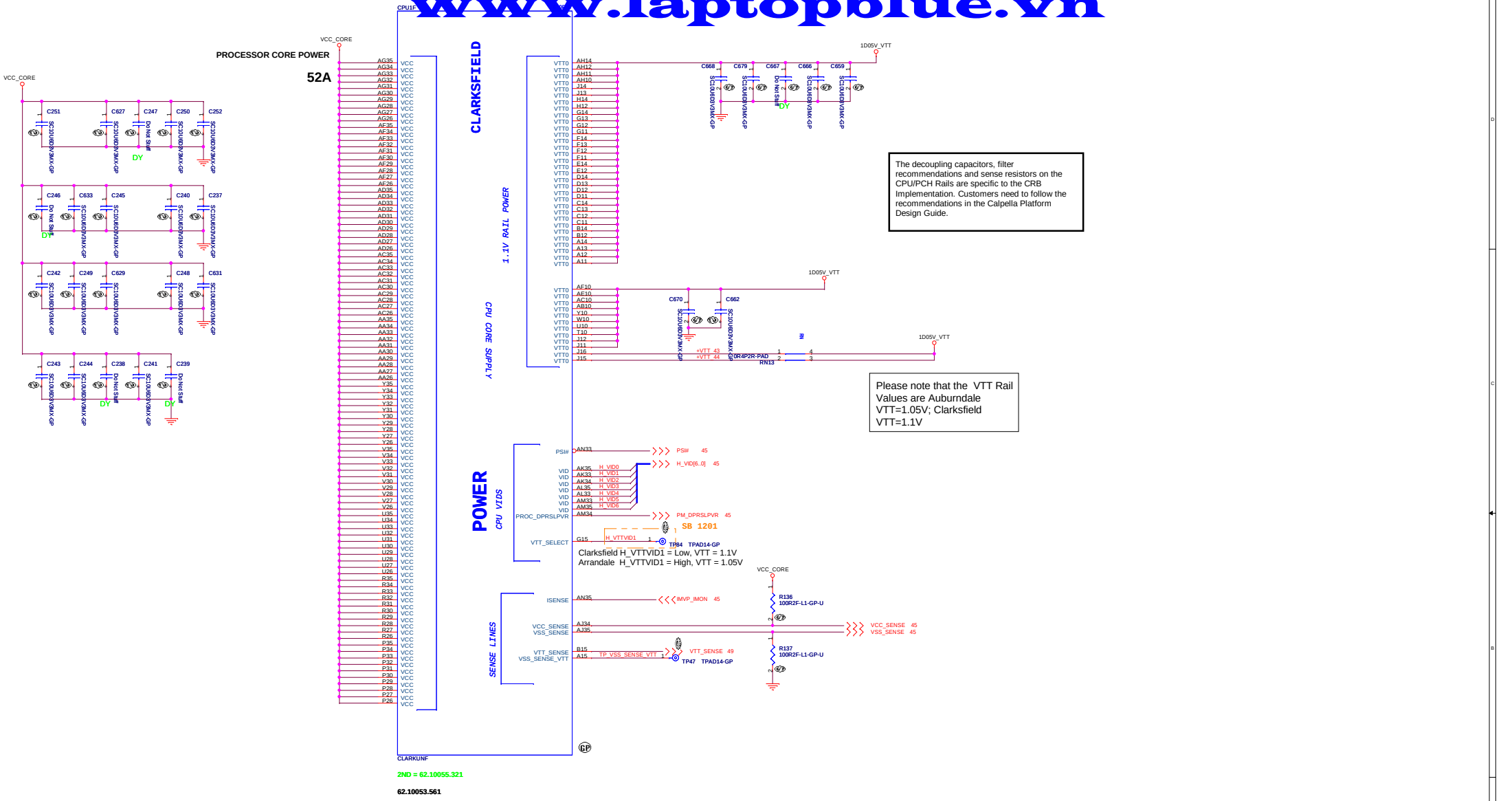

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

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Title	CPU (4/7)
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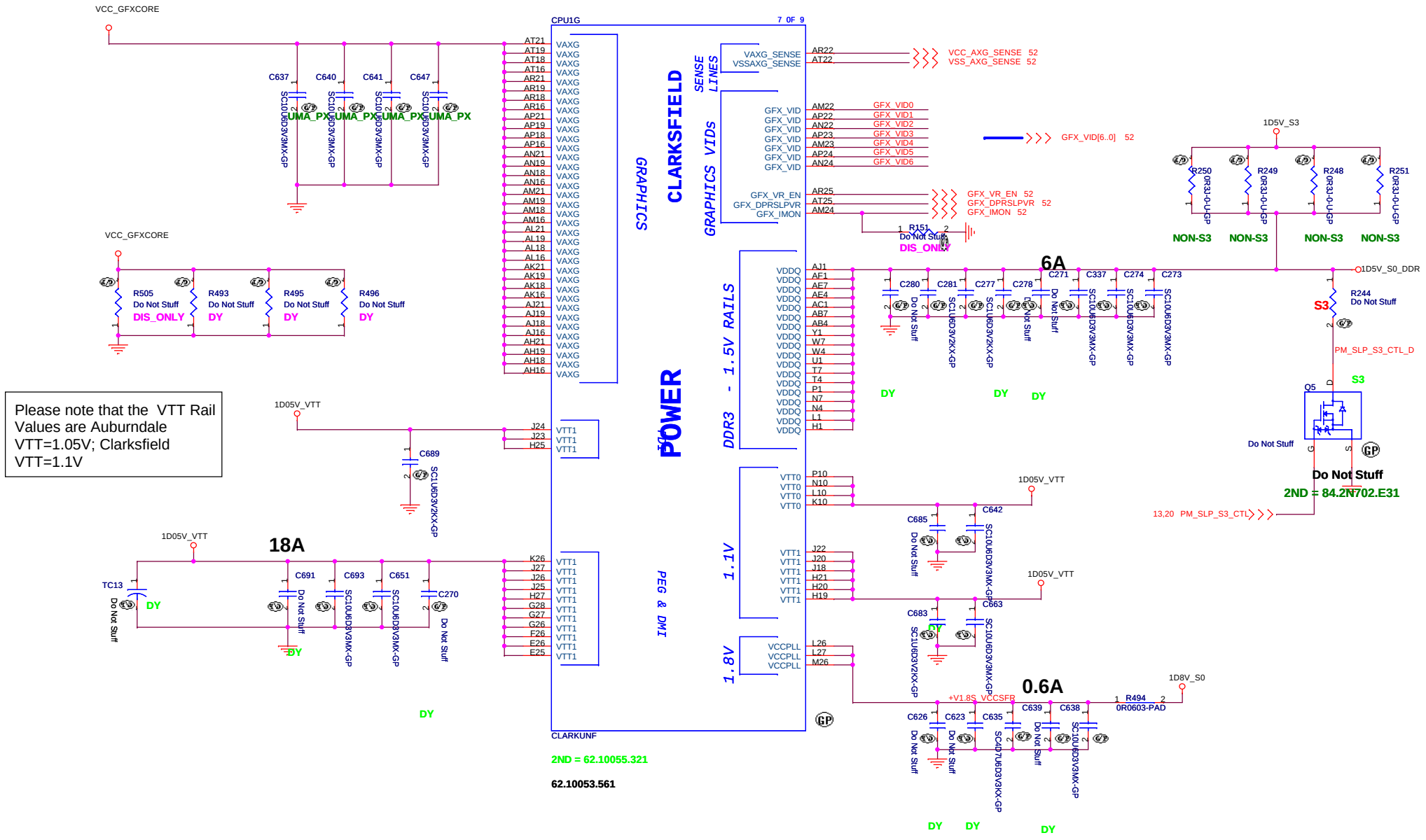

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Title	CPU (5/7)	
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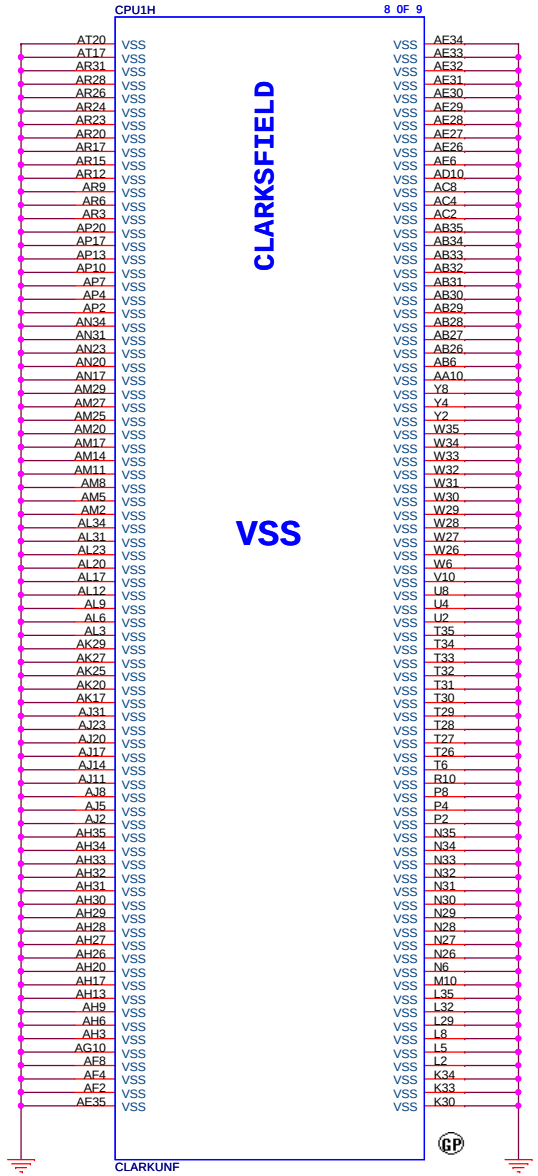

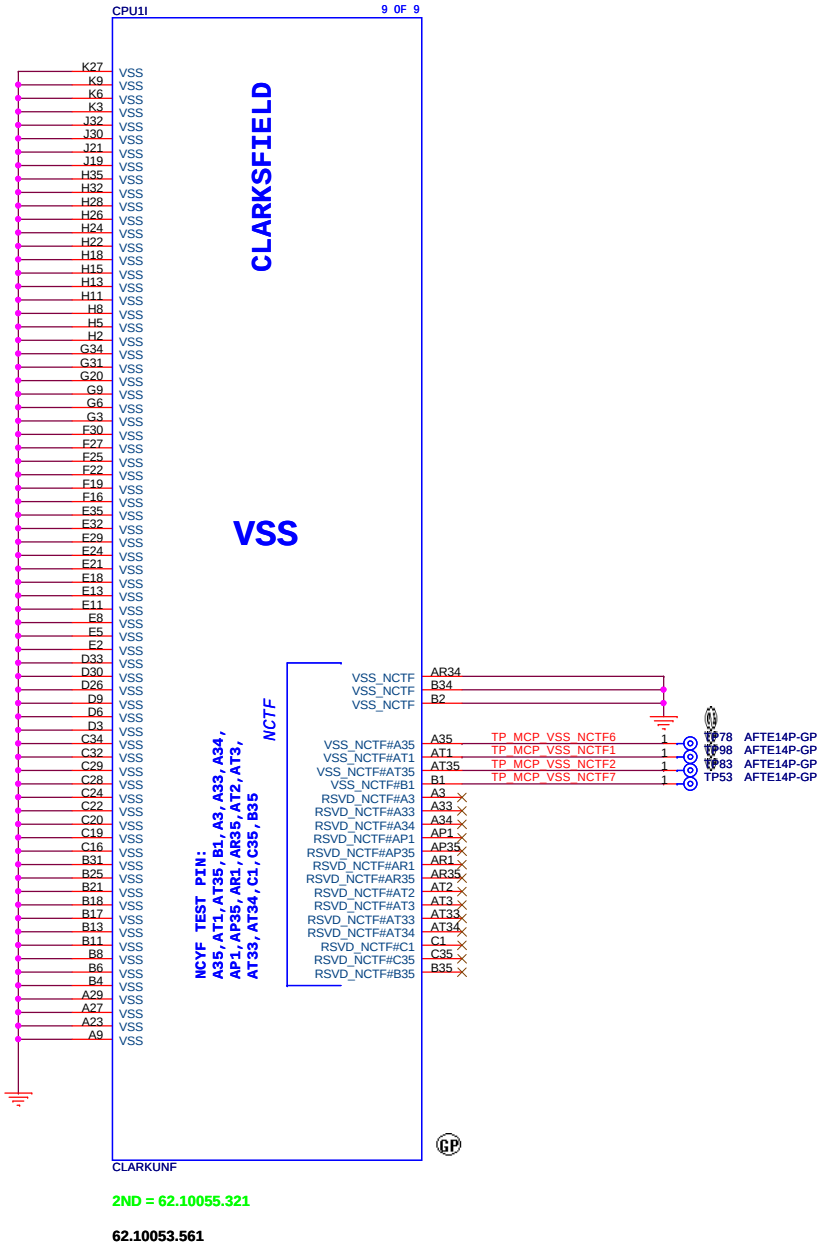

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Title: CPU (6/7)

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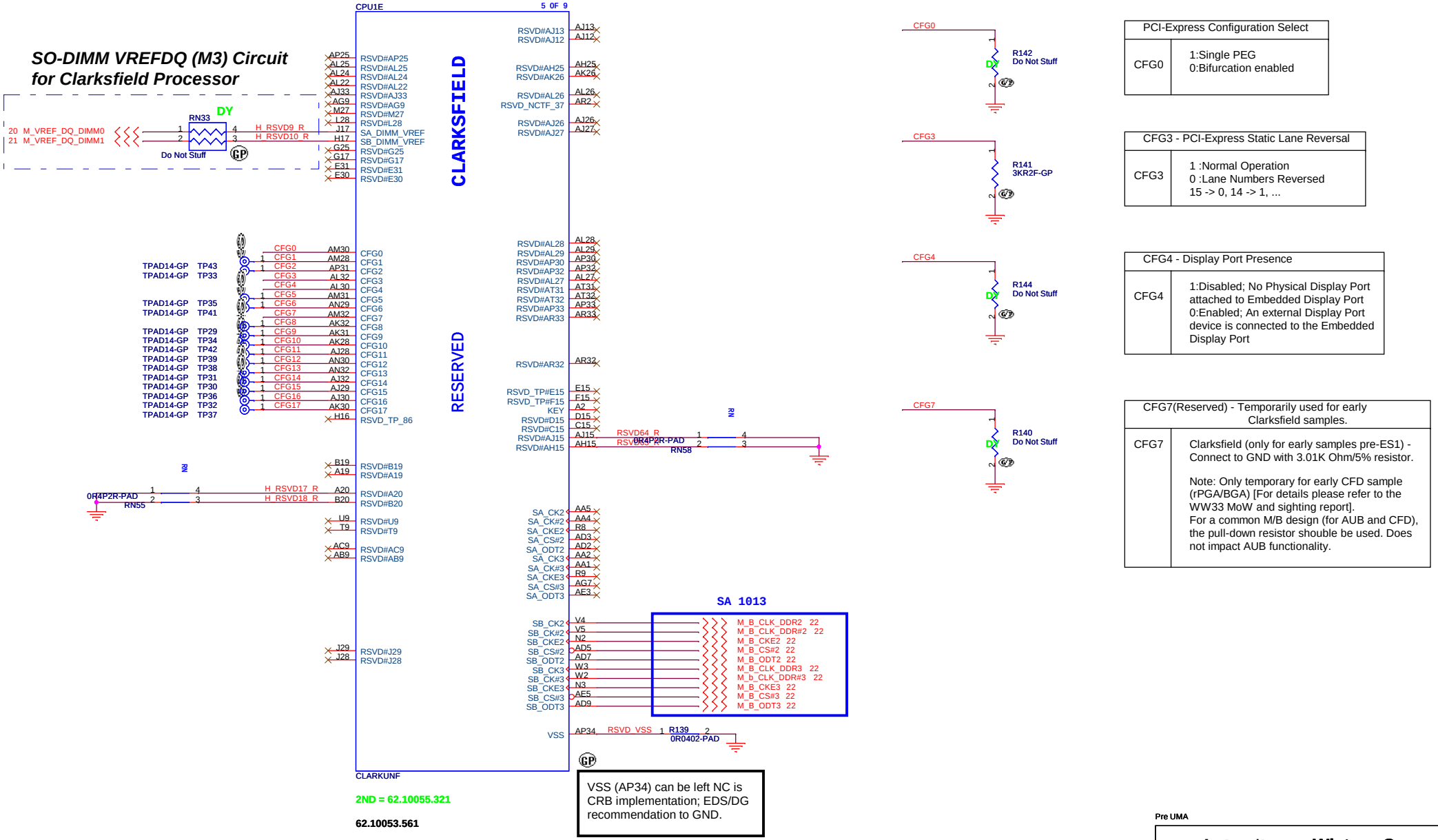

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

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Title: CPU (7/7)

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integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

ICH_RTCX1 — R553 10MR2J-L-GP — ICH_RTCX2
X5 — X-32D768KHZ-34GPU — 82.30001.661
C712, C709 — SC7P50V2DN-2GP
2nd = 82.30001.B21

RTC_AUX_S5 — RN22 — SRN20KJ-GP-U — C315 SC1U6D3V2KX-GP
RTC_X — R550 1MR2J-1-GP — SM_INTRUDER#
R551 330KR2F-L-GP — ICH_INTVRMEN

ACZ_RST# — DY ECT3 — Do Not Stuff
ACZ_SYNC — DY ECT5 — Do Not Stuff
ACZ_BIT_CLK — DY ECT4 — Do Not Stuff
ACZ_SDATAOUT — DY ECT6 — Do Not Stuff

C322 SC1U6D3V2KX-GP — G121 GAP-OPEN — Close to DM1 connector
SRTCRST# new signal Pin

33 ACZ_RST#_AUDIO
33 ACZ_SYNC_AUDIO
33 ACZ_BITCLK_AUDIO
33 ACZ_SDATAOUT_AUDIO
SRN33J-4-GP — RN20 — ACZ_RST# ACZ_SYNC ACZ_BIT_CLK ACZ_SDATAOUT

1D5V_S0 — R549 — DY — Do Not Stuff — ACZ_SYNC

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.

NO REBOOT STRAP

3D3V_S0 — R583 — DY — Do Not Stuff — ACZ_SPKR

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

3D3V_S5
PCH_JTAG_TMS — R592 — Do Not Stuff
PCH_JTAG_TDO — R589 — DY — Do Not Stuff
PCH_JTAG_TDI — R591 — DY — Do Not Stuff
PCH_JTAG_RST# — R590 — DY — Do Not Stuff

PCH_JTAG_TMS — R224 — DY — Do Not Stuff
PCH_JTAG_TDO — R221 — DY — Do Not Stuff
PCH_JTAG_TDI — R223 — DY — Do Not Stuff
PCH_JTAG_RST# — R220 — DY — Do Not Stuff
PCH_JTAG_TCK — R593 — 51R2F-2-GP

When unused all JTAG pins may be NC

PCH1A — 1 OF 10

ICH_RTCX1	B13	RTCX1	RTC
ICH_RTCX2	D13	RTCX2	
ICH_RTCRST#	C14	RTCRST#	
SRTCRST#	D17	SRTCRST#	
SM_INTRUDER#	A16	INTRUDER#	
ICH_INTVRMEN	A14	INTVRMEN	
ACZ_BIT_CLK	A30	HDA_BCLK	IHDA
ACZ_SYNC	D29	HDA_SYNC	
33 ACZ_SPKR	P1	SPKR	
ACZ_RST#	C30	HDA_RST#	
33 ACZ_SDATAIN0	G30	HDA_SDIN0	
ACZ_SDATAIN1	F30	HDA_SDIN1	
HDA_SDIN2	E32	HDA_SDIN2	
	F32	HDA_SDIN3	
ACZ_SDATAOUT	B29	HDA_SDO	
39 ME_UNLOCK# — R182 0R0402-PAD	H32	HDA_DOCK_EN#/GPIO33	SATA
R186 — DY — Do Not Stuff	J30	HDA_DOCK_RST#/GPIO13	
PCH_JTAG_TCK	M3	JTAG_TCK	JTAG
PCH_JTAG_TMS	K3	JTAG_TMS	
PCH_JTAG_TDI	K1	JTAG_TDI	
PCH_JTAG_TDO	J2	JTAG_TDO	
PCH_JTAG_RST#	J4	TRST#	
40 PCH_SPI_CLK — R239 15R2J-GP — SPI_CLK_R	BA2	SPI_CLK	SPI
40 PCH_SPI_CS#0 — R236 15R2J-GP — SPI_CS#0_R	AV3	SPI_CS0#	
	AY3	SPI_CS1#	
40 PCH_SPI_MOSI — R238 15R2J-GP — SPI_MOSI_R	AY1	SPI_MOSI	
40 SPI_MOSO_R	AV1	SPI_MISO	

FWH0/LAD0	D33	LPC_LAD0 39,40	LPC
FWH1/LAD1	B33	LPC_LAD1 39,40	
FWH2/LAD2	C32	LPC_LAD2 39,40	
FWH3/LAD3	A32	LPC_LAD3 39,40	
FWH4/LFRAME#	C34	LPC_LFRAME# 39,40	
LDRQ0#	A34		
LDRQ1#/GPIO23	F34	PCH_GPIO23 — TP52 TPAD14-GP	
SERIRQ	AB9	INT_SERIRQ — INT_SERIRQ 39	
SATA0RXN	AK7	SATA_RXN0 27	HDD
SATA0RXP	AK6	SATA_RXP0 27	
SATA0TXN	AK11	SATA_TXN0 27	
SATA0TXP	AK9	SATA_TXP0 27	
SATA1RXN	AH6		
SATA1RXP	AH5		
SATA1TXN	AH9		
SATA1TXP	AH8		
SATA2RXN	AF11		
SATA2RXP	AF9		
SATA2TXN	AF7		
SATA2TXP	AF6		
SATA3RXN	AH3		
SATA3RXP	AH1		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	AD9	SATA_RXN4 28	ODD
SATA4RXP	AD8	SATA_RXP4 28	
SATA4TXN	AD6	SATA_TXN4 28	
SATA4TXP	AD5	SATA_TXP4 28	
SATA5RXN	AD3		
SATA5RXP	AD1		
SATA5TXN	AB3		
SATA5TXP	AB1		
SATAICOMPO	AF16		
SATAICOMPI	AF15	SATAICOMP — R192 37D4R2F-GP — 1D05V_S0	
SATALED#	T3	SATA_LED# — SATA_LED# 42	
SATA0GP/GPIO21	Y9	SATA_DET#0_R	
SATA1GP/GPIO19	V1	SATA_DET#1_R	

IBEXPEAK-M-GP-NF

SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
3D3V_S0 — R219 — DY — Do Not Stuff — SPI_MOSI_R

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

RTC_AUX_S5 — R339 0R0603-PAD — RTC_PWR_L — C459 SC1U10V2ZY-GP
D8 BAS40CW-GP — 83.00040.E81 — 2nd = 83.00040.M81
3D3V_AUX_S5 — RTC_PWR — R331 1KR2J-1-GP
RTC_BAT — RTC1 BAT-CON2-1-GP-U — 62.70001.011 — 2nd = 62.70001.041

RN26 — SRN10KJ-7GP
SATA_DET#0_R
SATA_LED#
SATA_DET#1_R
INT_SERIRQ
3D3V_S0

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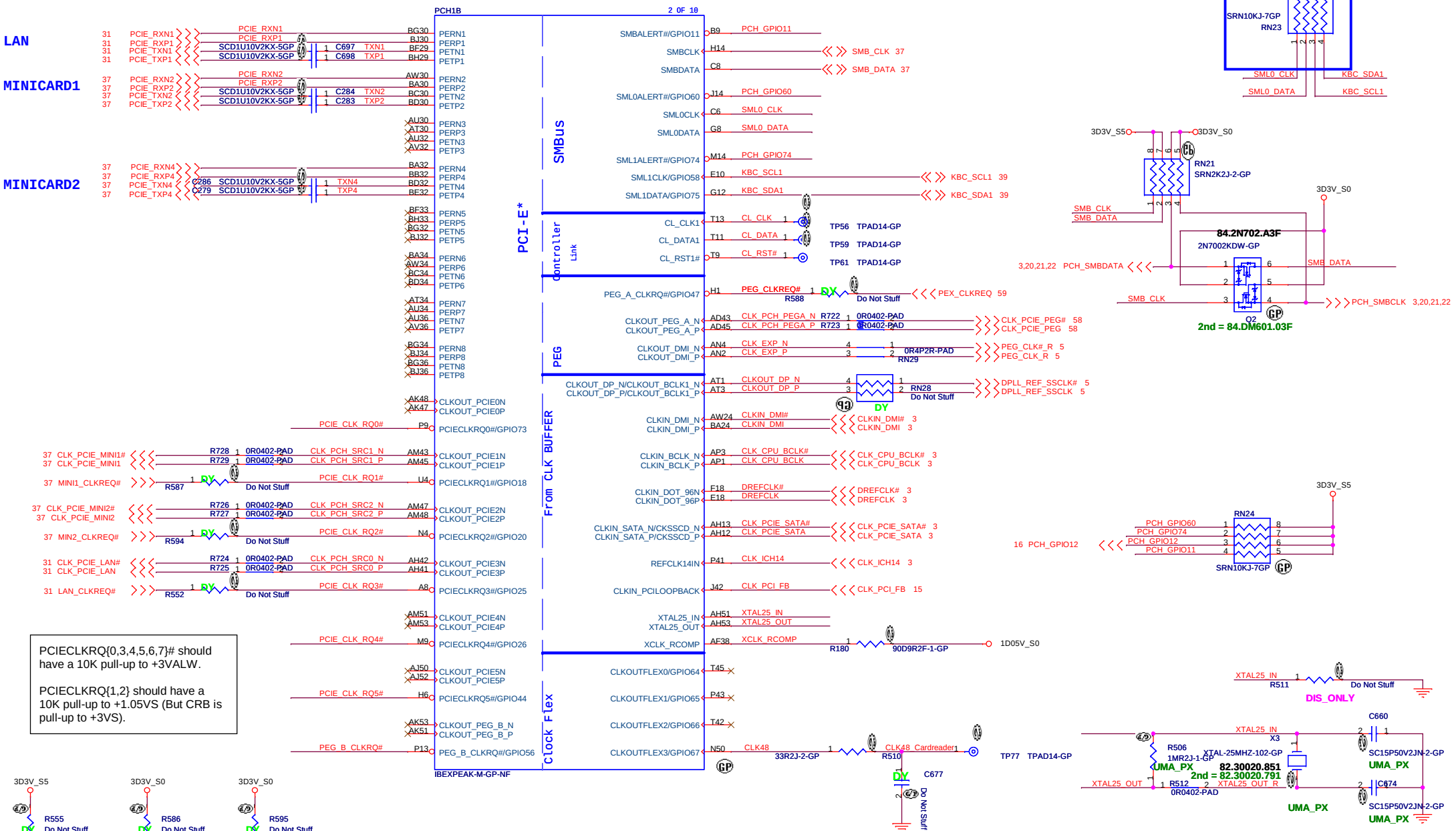

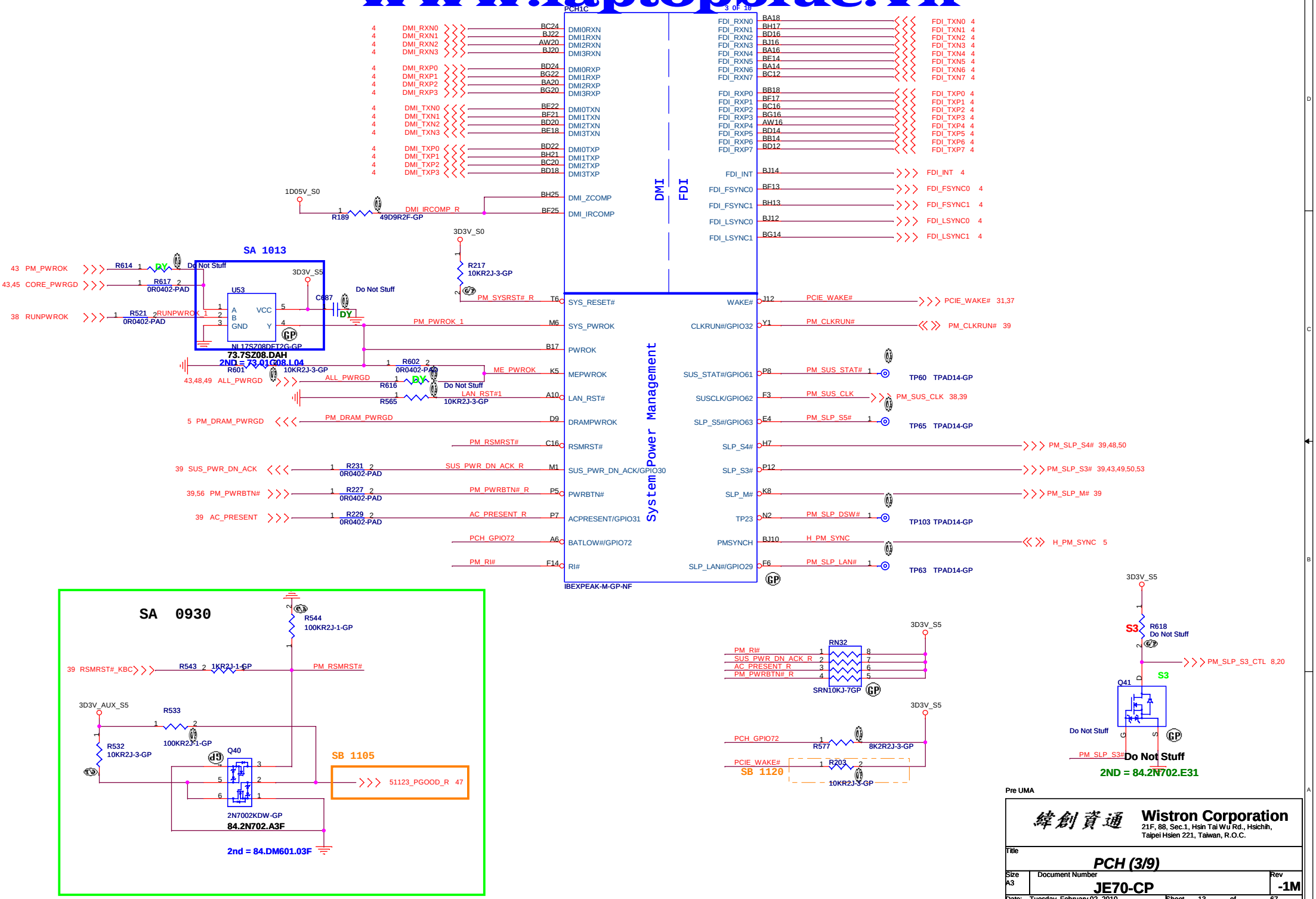

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Title: PCH (3/9)

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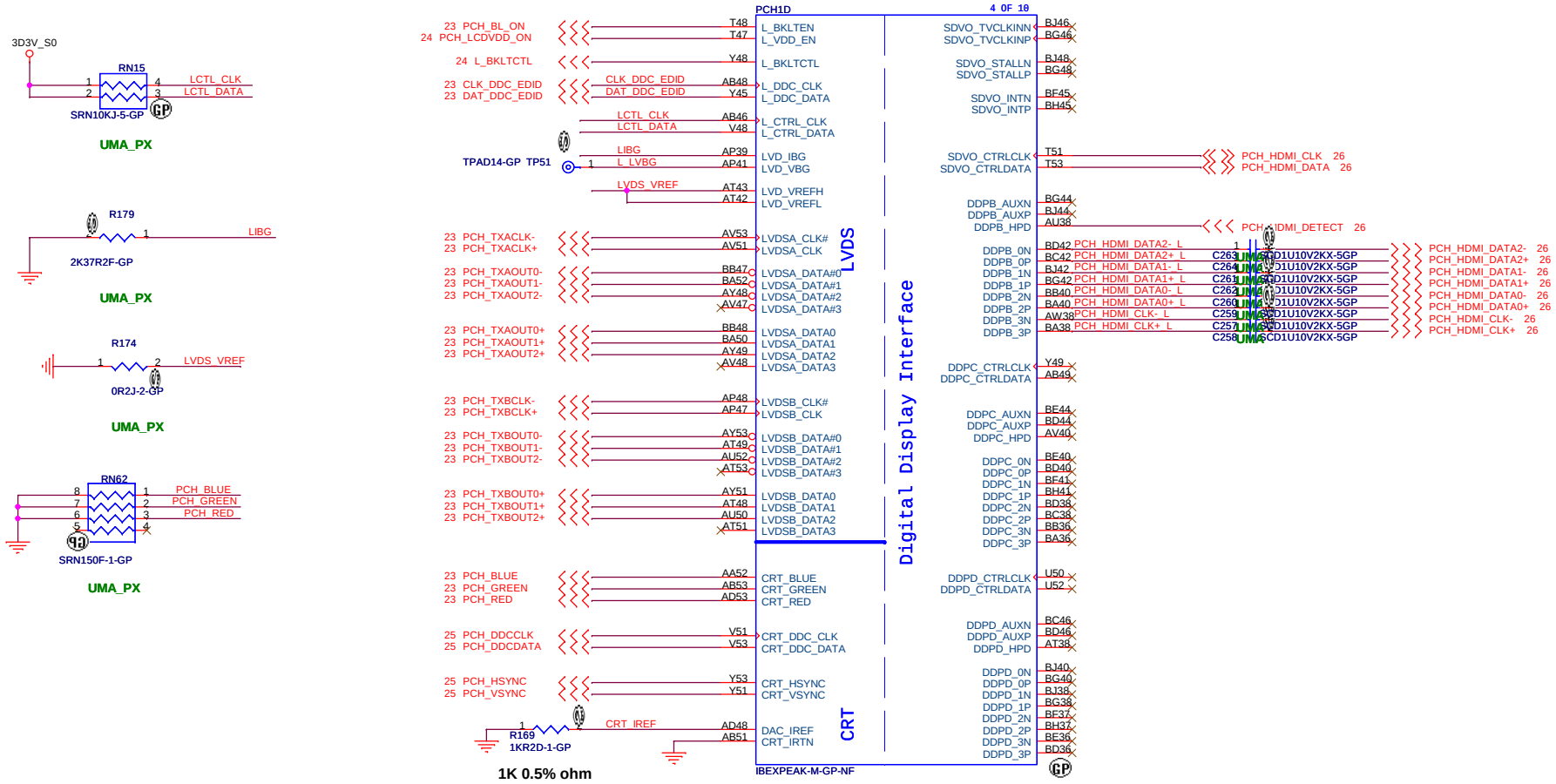

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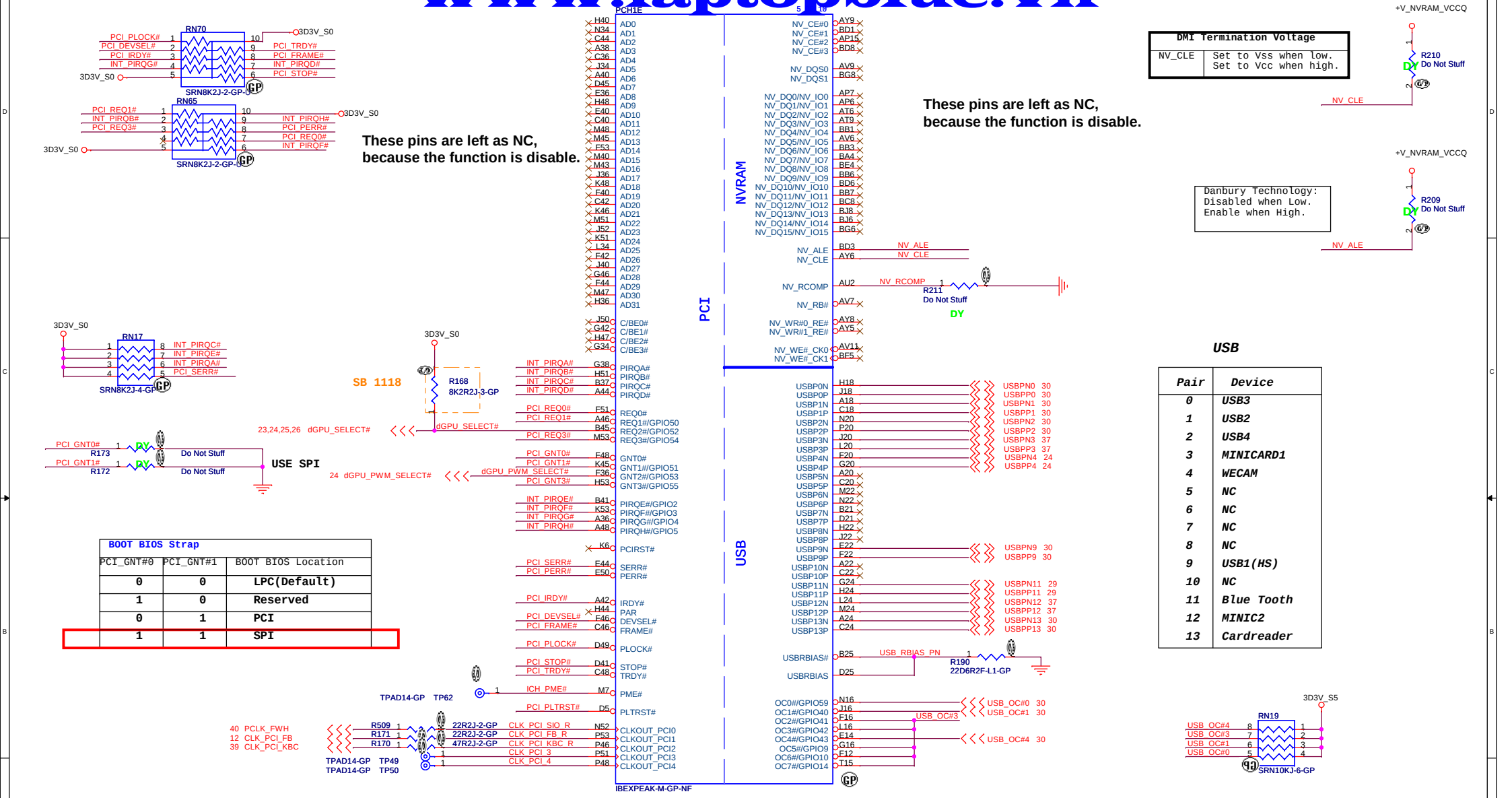

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Title: **PCH (5/9)**

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GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

PCH1F — 6 OF 10 — IBEXPEAK-M-GP-NF

GPIO: PCH_GPIO0 Y3 BMBUSY#/GPIO0; EC_SMI# C38 TACH1/GPIO1; PX_HDMI# D37 TACH2/GPIO6; EC_SCI# J32 TACH3/GPIO7; EC_SWI# F10 GPIO8; PCH_GPIO12 K9 LAN_PHY_PWR_CTRL/GPIO12; PCH_GPIO15 T7 GPIO15; DGPU_HOLD_RST# AA2 SATA4GP/GPIO16; DGPU_PWROK F38 TACH0/GPIO17; PCH_GPIO22 Y7 SCLOCK/GPIO22; PCH_GPIO24 H10 GPIO24; PCH_GPIO27 AB12 GPIO27; PCH_GPIO28 V13 GPIO28; STP_PCI# M11 STP_PCI#/GPIO34; PCH_GPIO35 V6 SATACLKREQ#/GPIO35; DGPU_PWR_EN# AB7 SATA2GP/GPIO36; dGPU_PRSNT# AB13 SATA3GP/GPIO37; dGPU_EDID V3 SLOAD/GPIO38; PCH_GPIO39 P3 SDATAOUT0/GPIO39; PCH_GPIO45 H3 PCIECLKRQ6#/GPIO45; RST_GATE F1 PCIECLKRQ7#/GPIO46; PCH_GPIO48 AB6 SDATAOUT1/GPIO48; PSW_CLR# AA4 SATA5GP/GPIO49; PCH_GPIO57 F8 GPIO57

MISC: CLKOUT_PCIE6N AH45; CLKOUT_PCIE6P AH46; CLKOUT_PCIE7N AF48; CLKOUT_PCIE7P AF47; A20GATE U2 → KA20GATE 39

CPU: CLKOUT_BCLK0_N/CLKOUT_PCIE8N AM3 → BCLK_CPU_N_R; CLKOUT_BCLK0_P/CLKOUT_PCIE8P AM1 → BCLK_CPU_P_R; PECI BG10 → H_PECI 5; RCIN# T1 → KBRCIN# 39; PROCPWRGD BE10 → H_PWRGD 5,43,56; THRMTRIP# BD10 → PCH_THERMTRIP_R

RN73 SRN10KJ-7GP: PCH_GPIO28, EC_SWI#
R218 8K2R2J-3-GP: PCH_GPIO45
R216 1KR2J-1-GP: PCH_GPIO15

RN31 SRN10KJ-7GP: PCH_GPIO39, PSW_CLR#

G122 GAP-OPEN: PSW_CLR#

RP1 SRN10KJ-L3-GP: PCH_GPIO0, EC_SMI#, dGPU_EDID, EC_SCI# → PCH_GPIO22, STP_PCI#, PX_HDMI#

R213 10KR2J-3-GP: DGPU_HOLD_RST#
R206 10KR2J-3-GP: DGPU_PWR_EN#

R204 56R2J-4-GP: 1D05V_VTT
R205 Do Not Stuff: PCH_THERMTRIP_R → PM_THRMTRIP-A# 5,43

Placed Within 2" from PCH

SRN0J-10-GP-U RN30: BCLK_CPU_N_R → BCLK_CPU_N 5; BCLK_CPU_P_R → BCLK_CPU_P 5

TP1 BA22; TP2 AW22; TP3 BB22; TP4 AY45; TP5 AY46; TP6 AV43; TP7 AV45; TP8 AF13; TP9 M18; TP10 N18; TP11 AJ24; TP12 AK41; TP13 AK42; TP14 M32; TP15 N32; TP16 M30; TP17 N30; TP18 H12; TP19 AA23; NC_1 AB45; NC_2 AB38; NC_3 AB42; NC_4 AB41; NC_5 T39; INIT3_3V# P6 → INIT3_3V#; TP24 C10

TP64 TPAD14-GP

NCTF: VSS_NCTF_8 B4; VSS_NCTF_9 B52; VSS_NCTF_16 BH2; VSS_NCTF_17 BH52; VSS_NCTF_28 D2; VSS_NCTF#A4 A4; VSS_NCTF#A49 A49; VSS_NCTF#A5 A5; VSS_NCTF#A50 A50; VSS_NCTF#A52 A52; VSS_NCTF#A53 A53; VSS_NCTF#B2 B2; VSS_NCTF#B53 B53; VSS_NCTF#BE1 BE1; VSS_NCTF#BE53 BE53; VSS_NCTF#BF1 BF1; VSS_NCTF#BF53 BF53; VSS_NCTF#BH1 BH1; VSS_NCTF#BH53 BH53; VSS_NCTF#BJ1 BJ1; VSS_NCTF#BJ2 BJ2; VSS_NCTF#BJ4 BJ4; VSS_NCTF#BJ49 BJ49; VSS_NCTF#BJ5 BJ5; VSS_NCTF#BJ50 BJ50; VSS_NCTF#BJ52 BJ52; VSS_NCTF#BJ53 BJ53; VSS_NCTF#D1 D1; VSS_NCTF#D53 D53; VSS_NCTF#E1 E1; VSS_NCTF#E53 E53

NCTF TEST PIN: A4,A49,A5,A50,A52,A53,B2,B53,BE1,BE53,BF1,BF53,BH1,BH53,BJ1,BJ2,BJ4,BJ49,BJ5,BJ50,BJ52,BJ53,D1,D53,E1,E53

RSVD

AFTE14P-GP TP95 → PCH_TP95; AFTE14P-GP TP101 → PCH_TP96; AFTE14P-GP TP102 → PCH_TP97; AFTE14P-GP TP96 → PCH_TP98

1D5V_S3
R262 Do Not Stuff: DDR3_DRAMRST# 20,21,22
R615 Do Not Stuff
Q7 Do Not Stuff: RST_GATE; QID = 84.T3904.C11
C342 Do Not Stuff
R259 0R2J-2-GP: NON-S3
R257 Do Not Stuff: SM_DRAMRST# 5

DIS_UMA: R194 10KR2J-3-GP: dGPU_PRSNT#; R198 Do Not Stuff — PX

UMA_PX: R215 10KR2J-3-GP: PCH_GPIO57; R214 Do Not Stuff — DIS_ONLY

UMA_DISCRETE#
SG: HIGH
UMA: HIGH
DIS ONLY: LOW

R737 Do Not Stuff (2G) — PCH_GPIO35; R212 Do Not Stuff (512M/1G)
R736 Do Not Stuff (512M) — PCH_GPIO48; R735 Do Not Stuff (1G)

VRAM setting
2G: HIGH
512M/1G: LOW

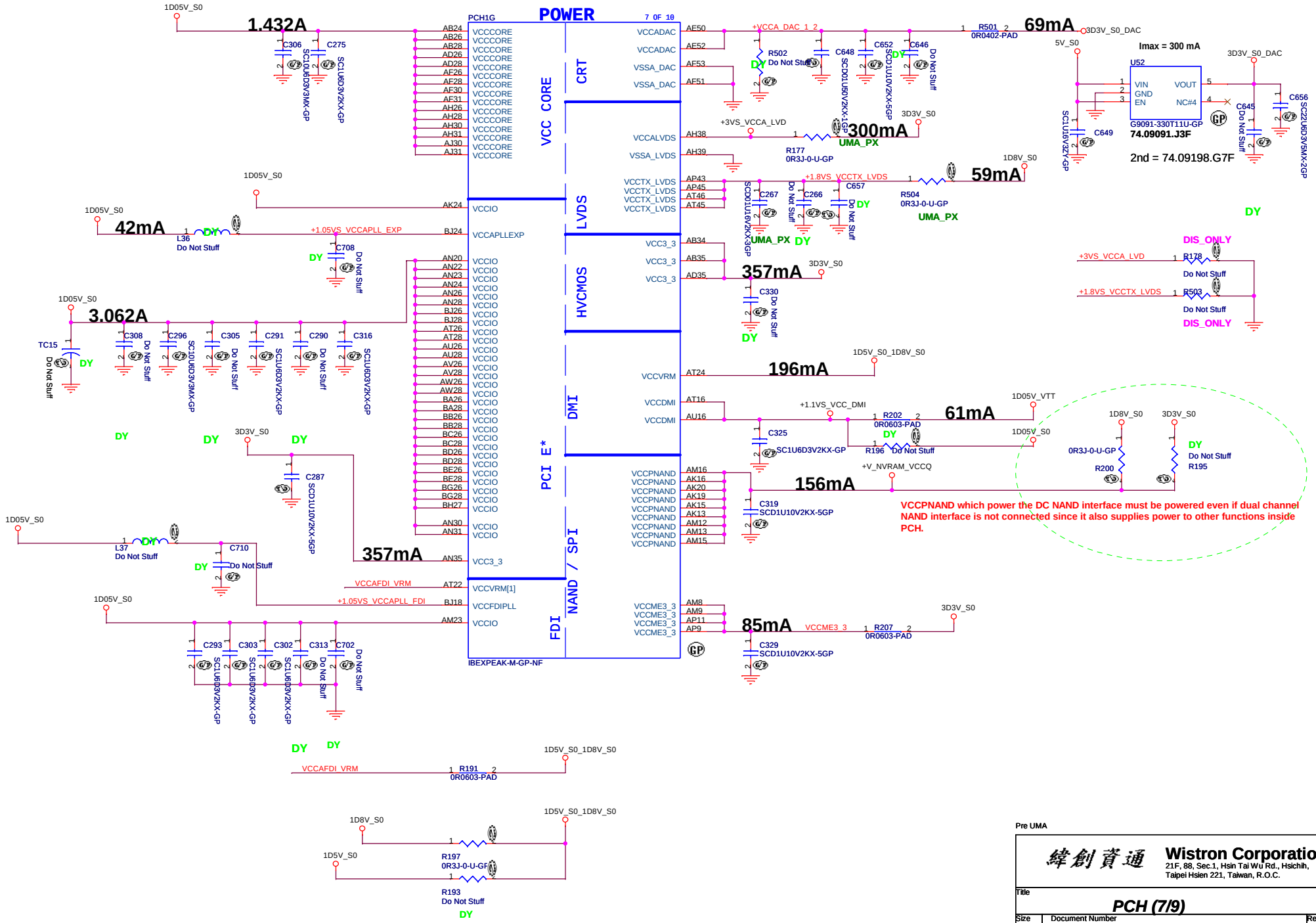
VRAM setting
512M: HIGH
1G: LOW

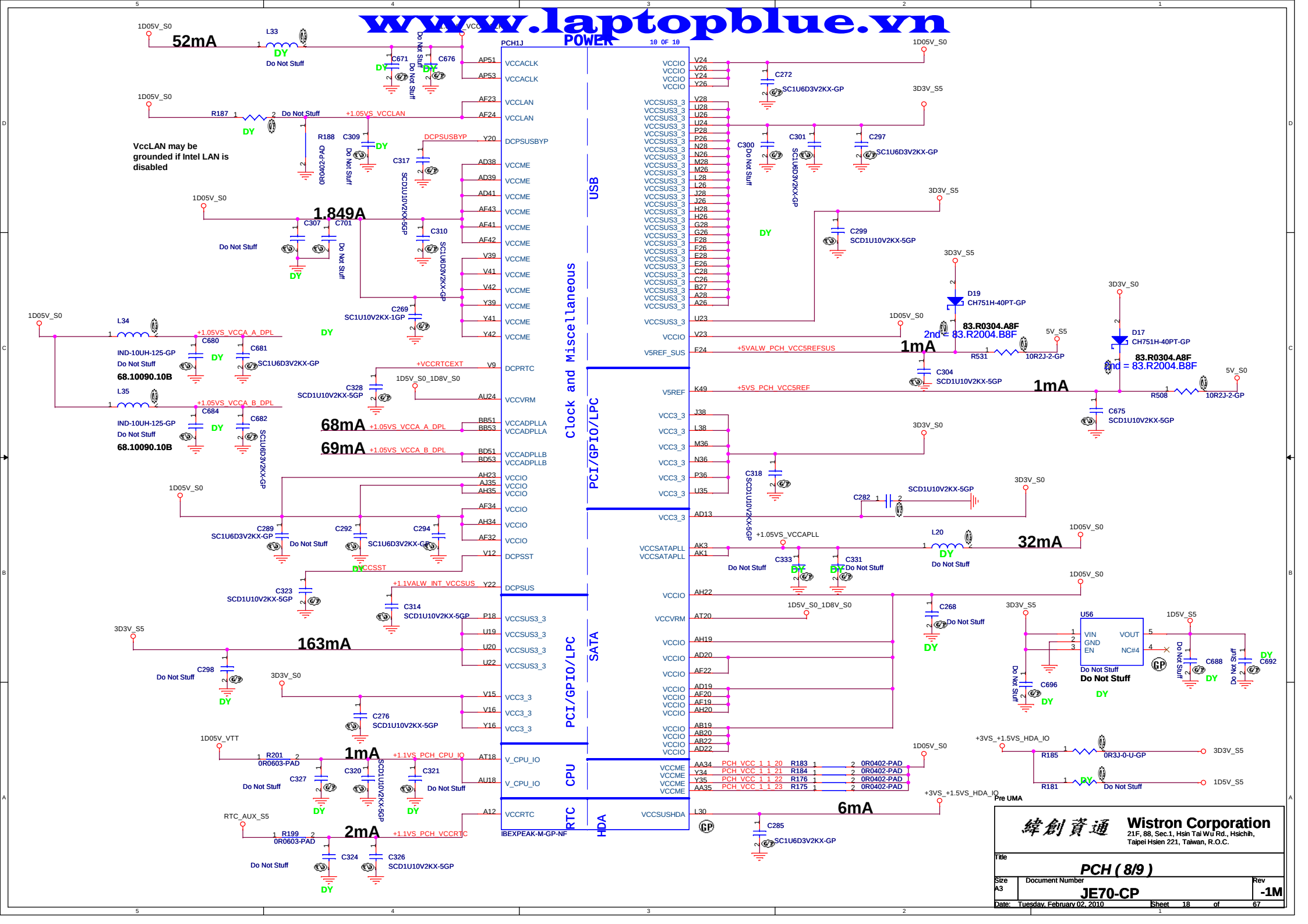
-1 0105

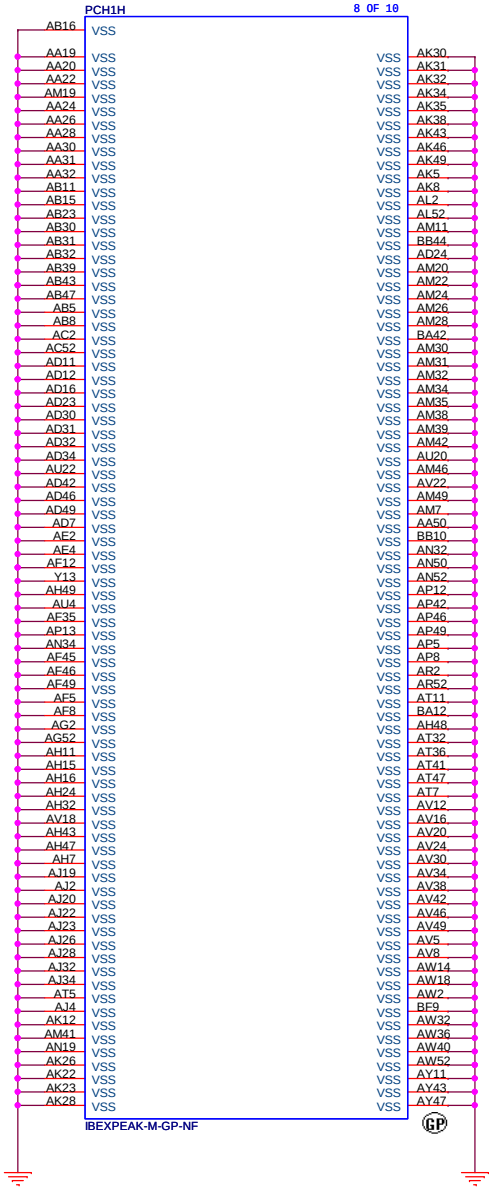
Pre UMA

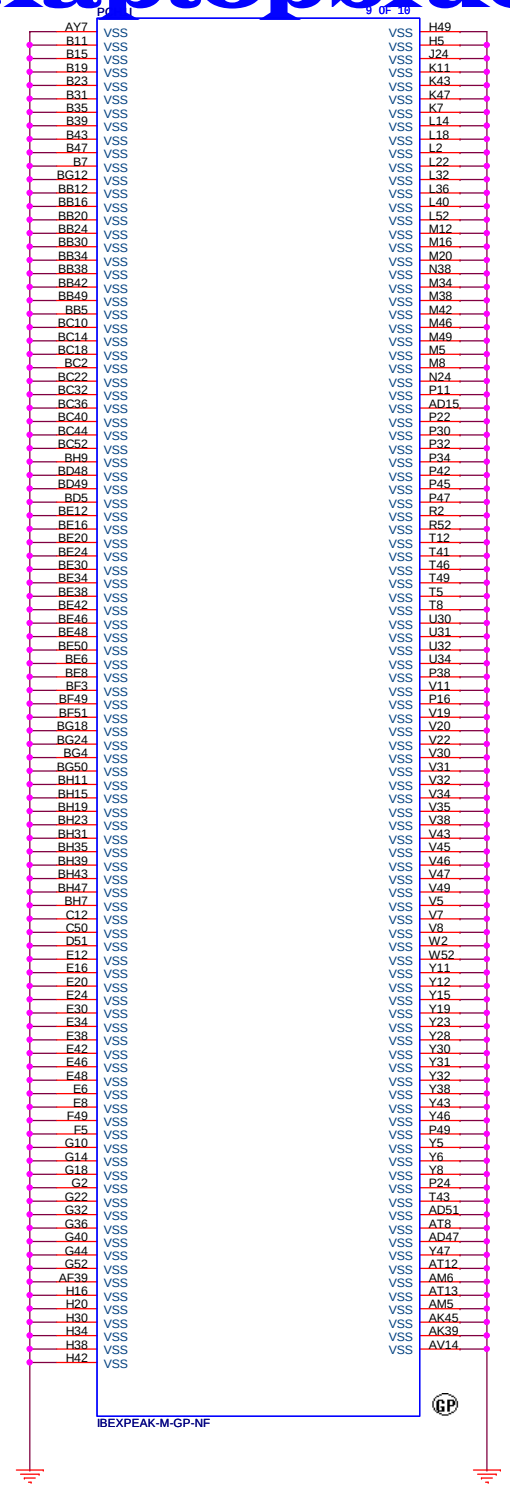
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (6/9)
Size: A3 | Document Number: JE70-CP | Rev: -1M
Date: Tuesday, February 02, 2010 | Sheet 16 of 67









Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (9/9)***

Size	Document Number	Rev
A3	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 19 of 67

DM2

Stardand type

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SB 1116

Layout Note:
Place these Caps near SO-DIMMA.

SODIMM A DECOUPLING

Place these caps close to VTT1 and VTT2.

H =4mm

DDR3-204P-99-GP
62.10017.W01
2nd = 62.10017.V31

Pre UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII Socket DM1
Size: Custom
Document Number: JE70-CP
Rev: -1M
Date: Tuesday, February 02, 2010
Sheet 20 of 67

DM1

REVERSE TYPE

DDR3-204P-97-GP

H = 4mm

62.10017.W11

2ND = 62.10017.V51

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SB 1120

Place these caps close to VTT1 and VTT2.

SODIMM B DECOUPLING

Pre UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII Socket DM2

Size: Custom | Document Number: JE70-CP | Rev: -1M

Date: Tuesday, February 02, 2010 | Sheet 21 of 67

Stardand type

Note:
SO-DIMMB SPD Address is 0xA6
SO-DIMMB TS Address is 0x36

SODIMM B DECOUPLING

Place these caps close to VTT1 and VTT2.

H = 8mm

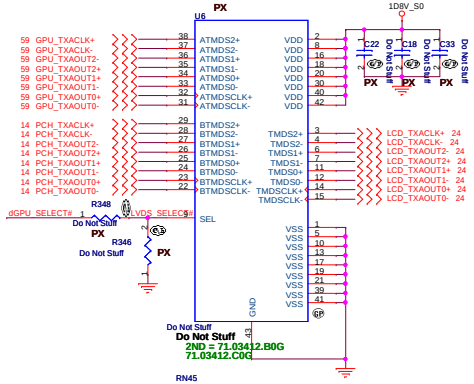
Pre UMA

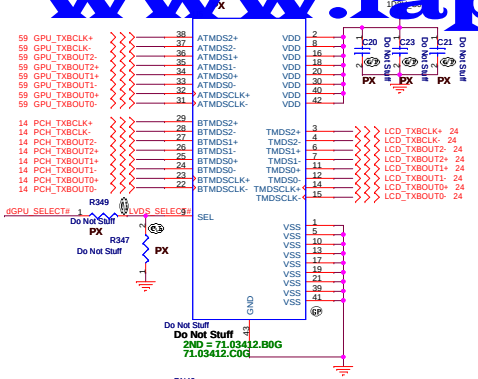
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

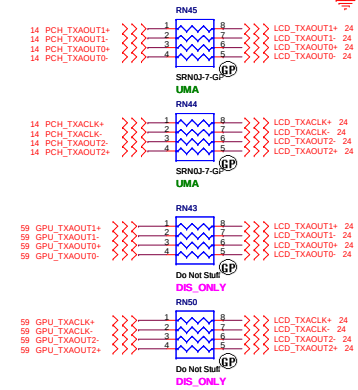
Title: DDRIII Socket DM1

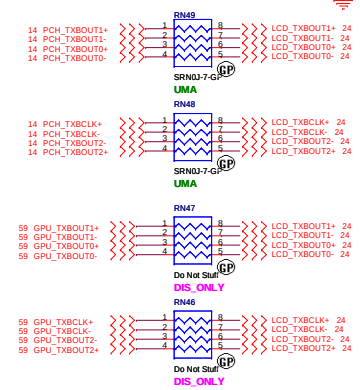
Size: Custom | Document Number: JE70-CP | Rev: -1M

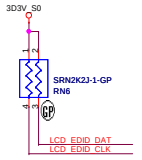
Date: Tuesday, February 02, 2010 | Sheet 22 of 67

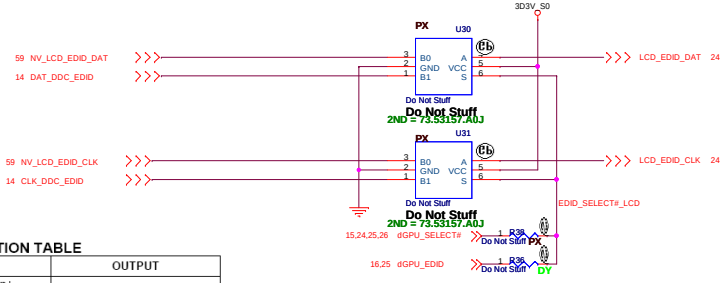






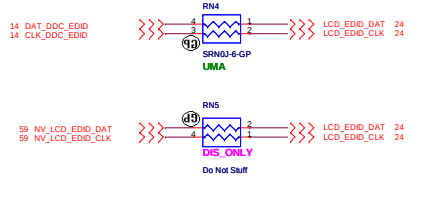


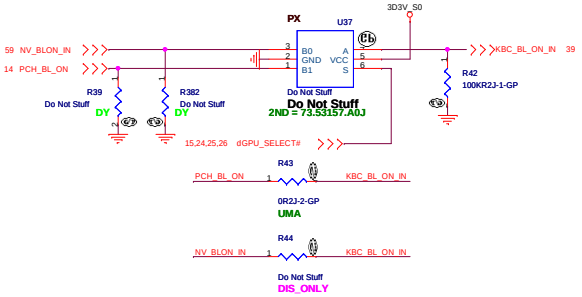


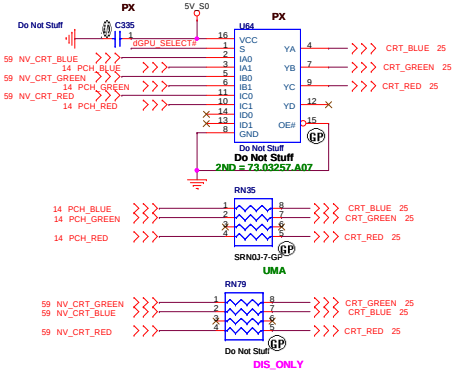


FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-







$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

Pre UMA

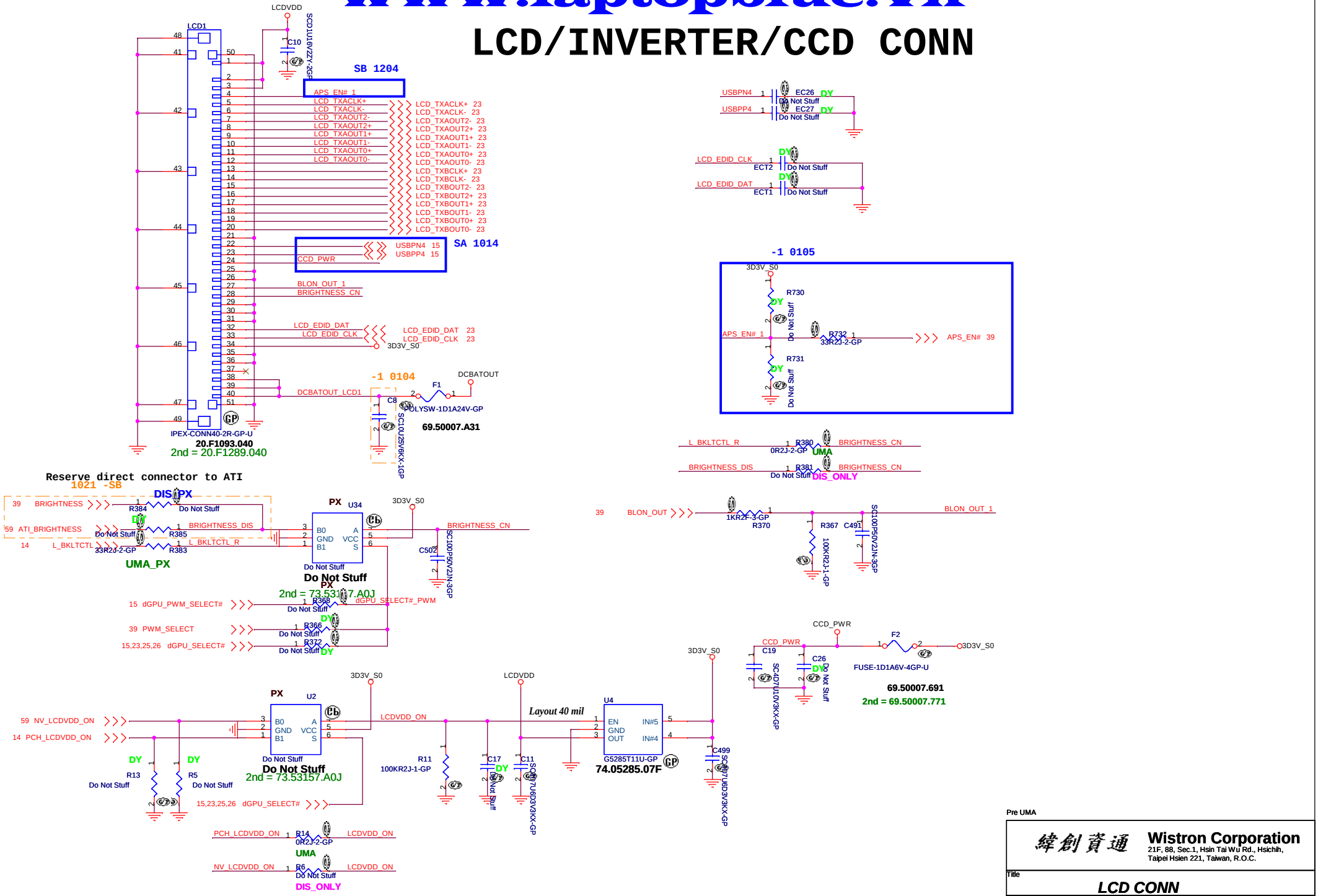
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PX SWITCH

Size: A2 | Document Number: JE70-CP | Rev: -1M

Date: Tuesday, February 02, 2010 | Sheet 23 of 67

LCD/INVERTER/CCD CONN

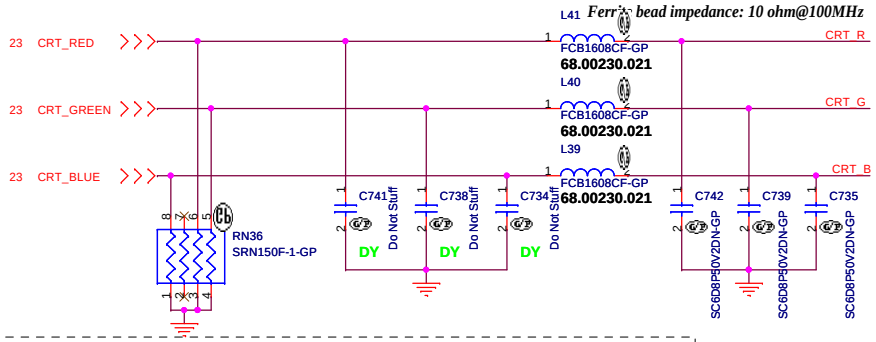


Pre UMA

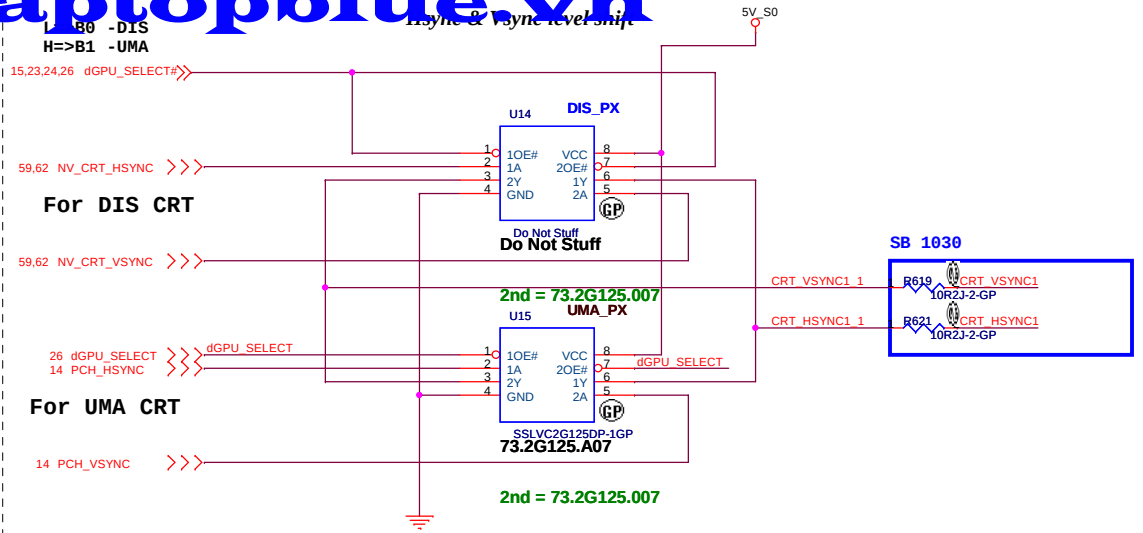
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD CONN	
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 24 of 67	

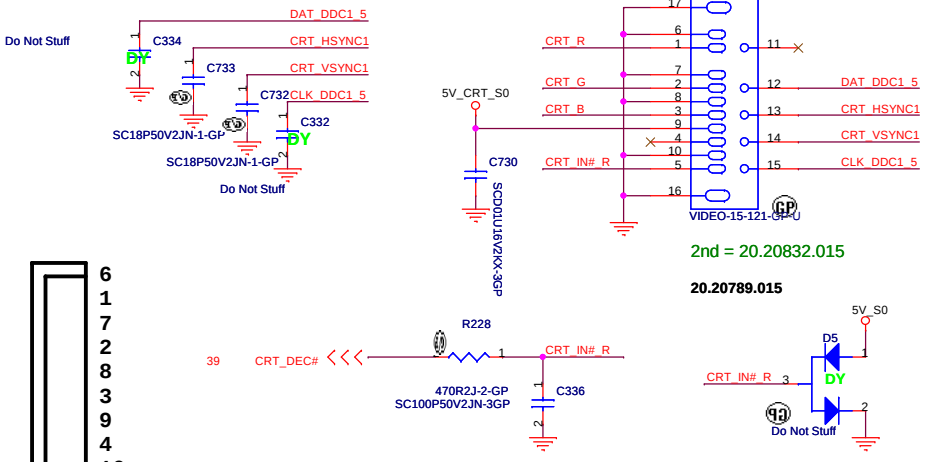
Layout Note:
Place these resistors close to the CRT-out connector



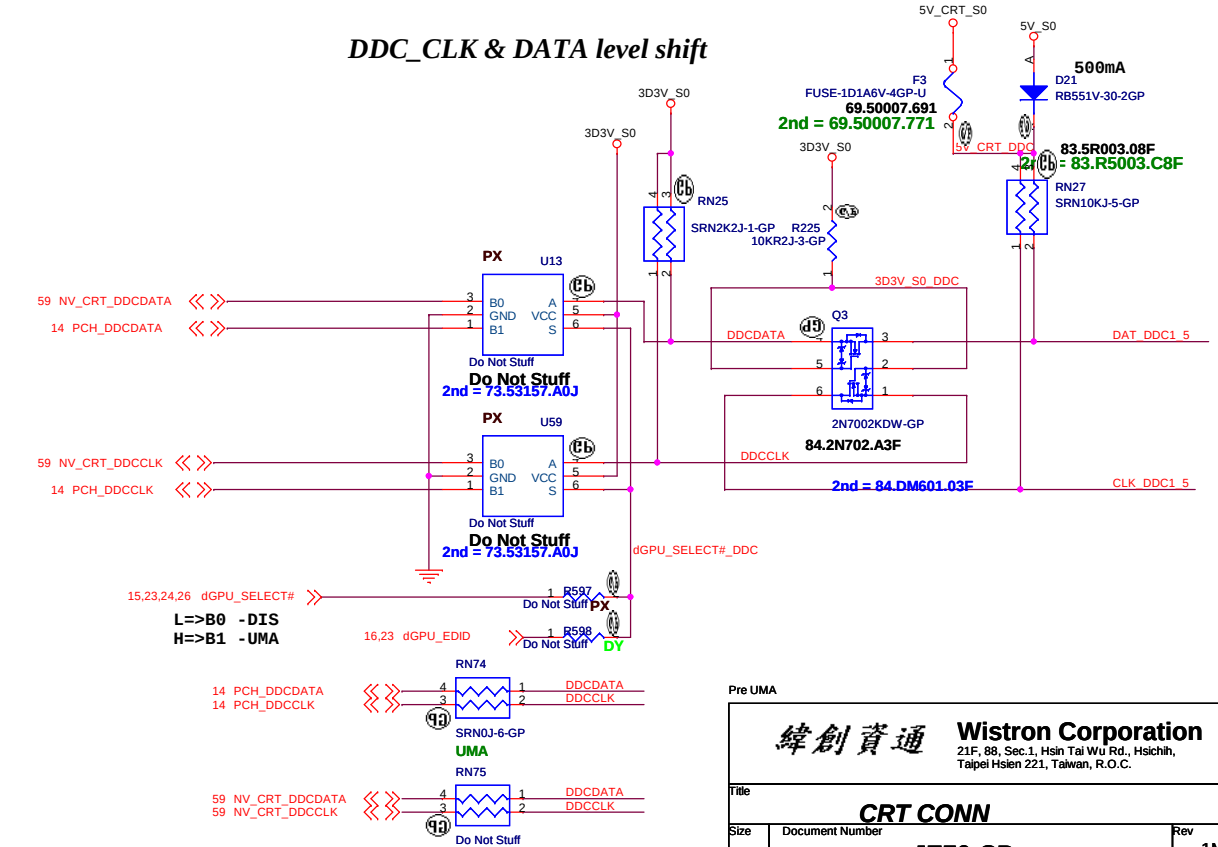
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



CRT I/F & CONNECTOR



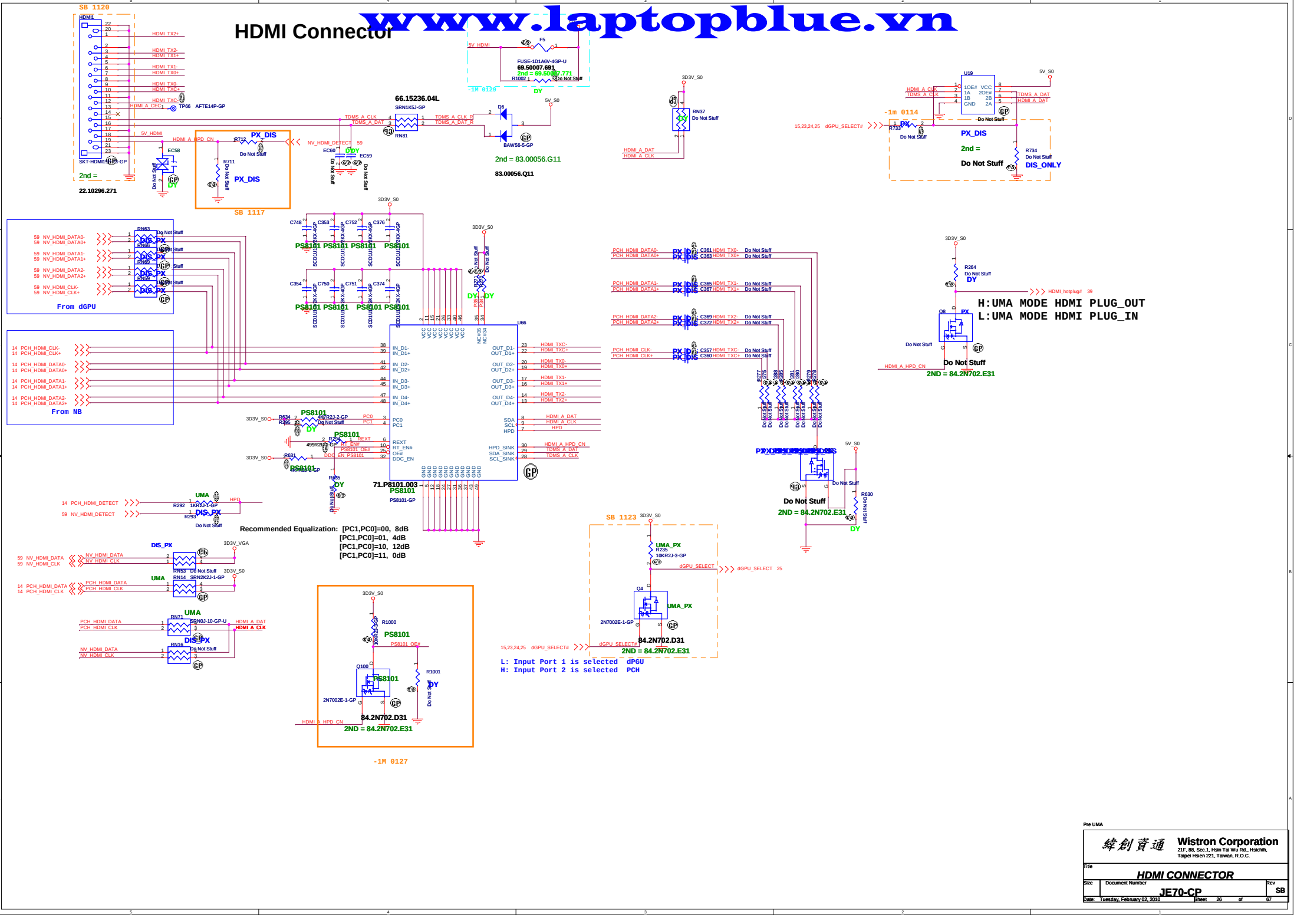
DDC_CLK & DATA level shift



Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CRT CONN**
Size	Document Number: **JE70-CP** — Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 25 of 67

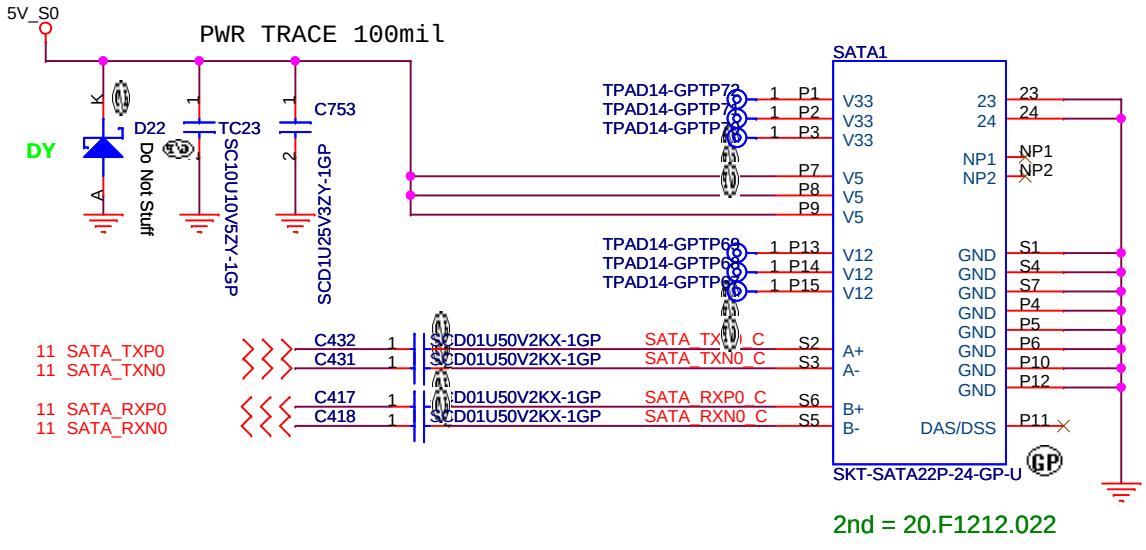
HDMI Connector



Pre UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI CONNECTOR	
Size	Document Number: JE70-CP	Rev: SB
Date: Tuesday, February 02, 2010	Sheet 26 of 67	

SATA Connector



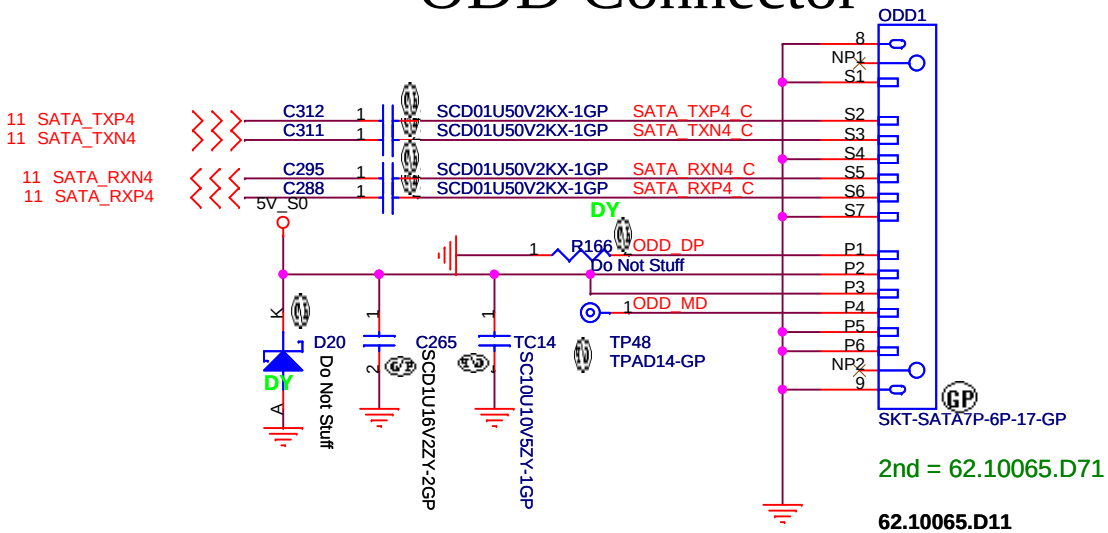
2nd = 20.F1212.022

20.F1265.022

Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD CONN***	
Size	Document Number **JE70-CP**	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 27 of 67	

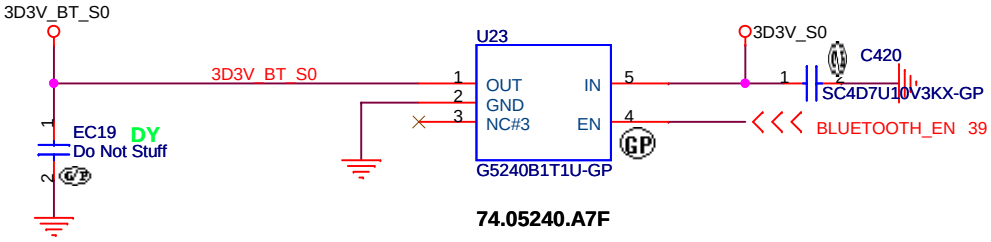
ODD Connector



Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ODD
Size	Document Number: JE70-CP — Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 28 of 67

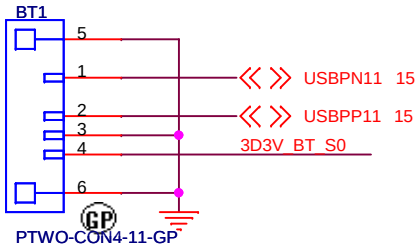
BLUETOOTH MODULE



74.05240.A7F

2nd = 74.09711.A7F

EC20 put near BLUE1 / all USB put one choke near connector by EMI request

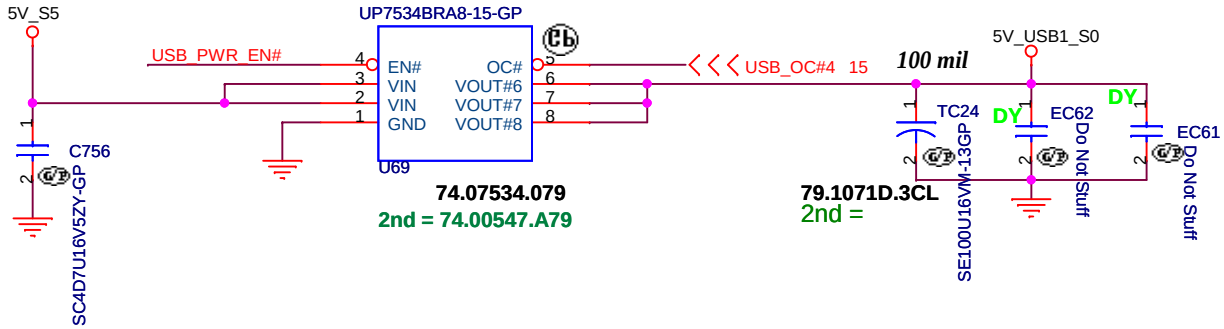


20.F1561.004

2nd = 20.F1621.004

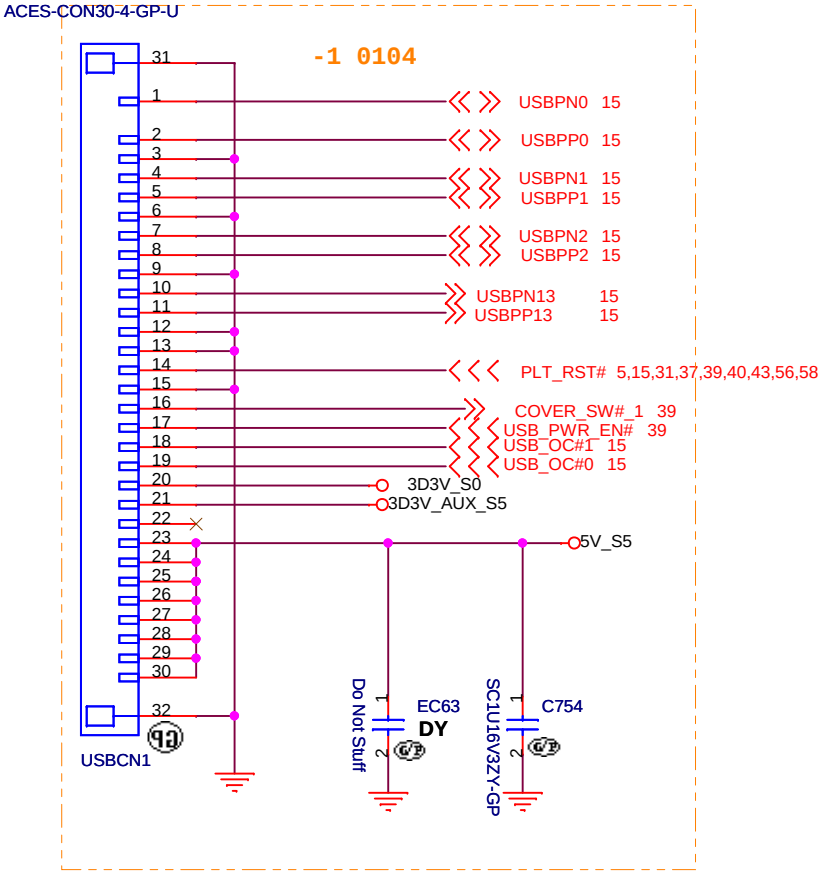
Pre UMA

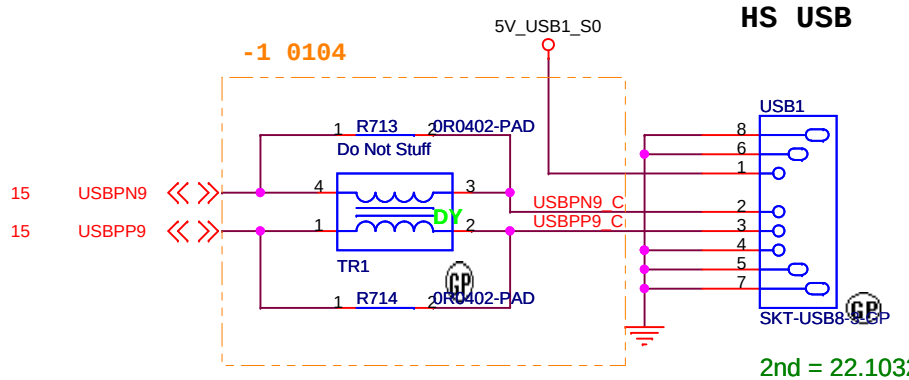
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 29 of 67	



2nd =

20.K0276.030





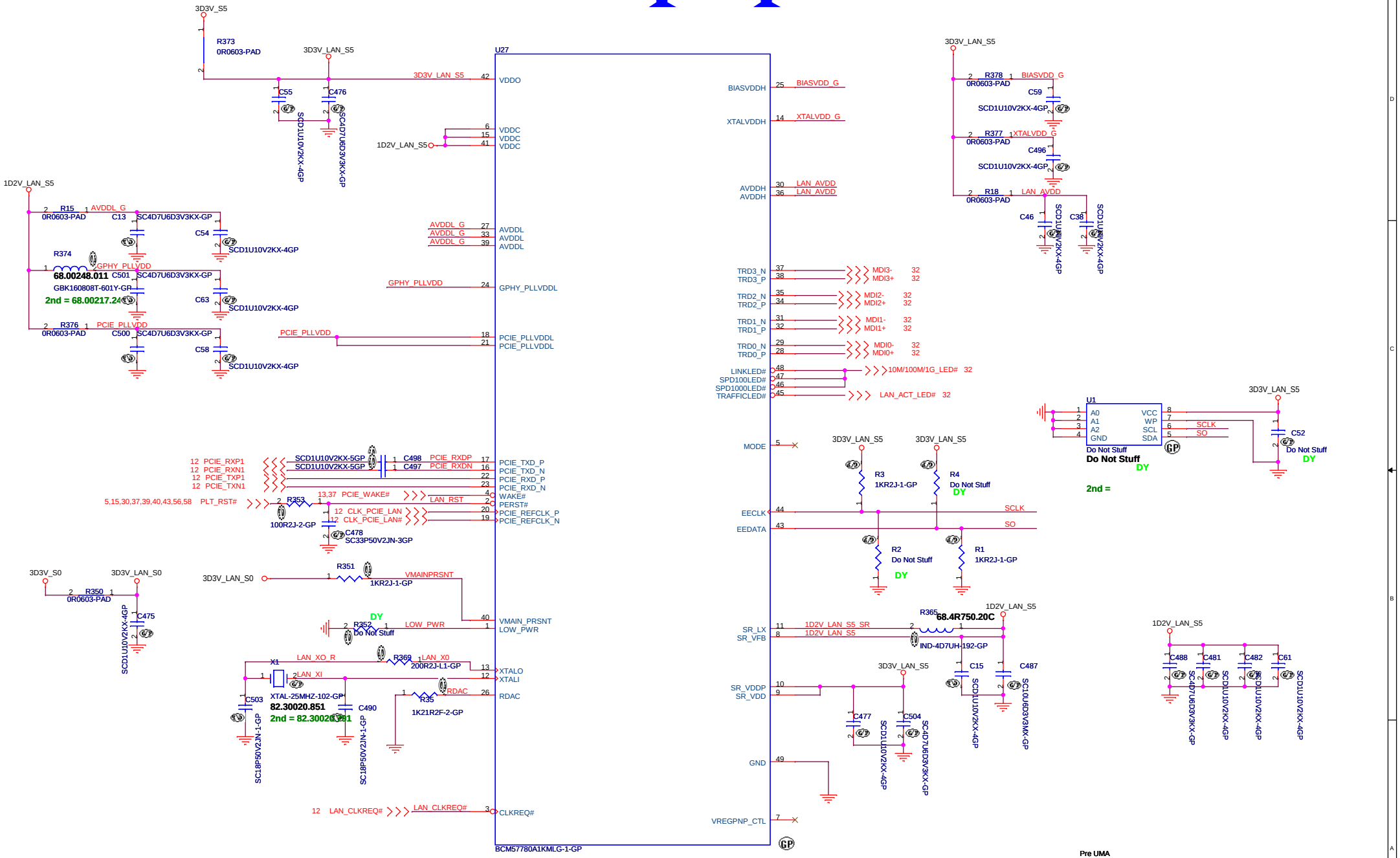
2nd = 22.10321.C41

22.10321.B81

Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*USB CONN*	
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 30 of 67	



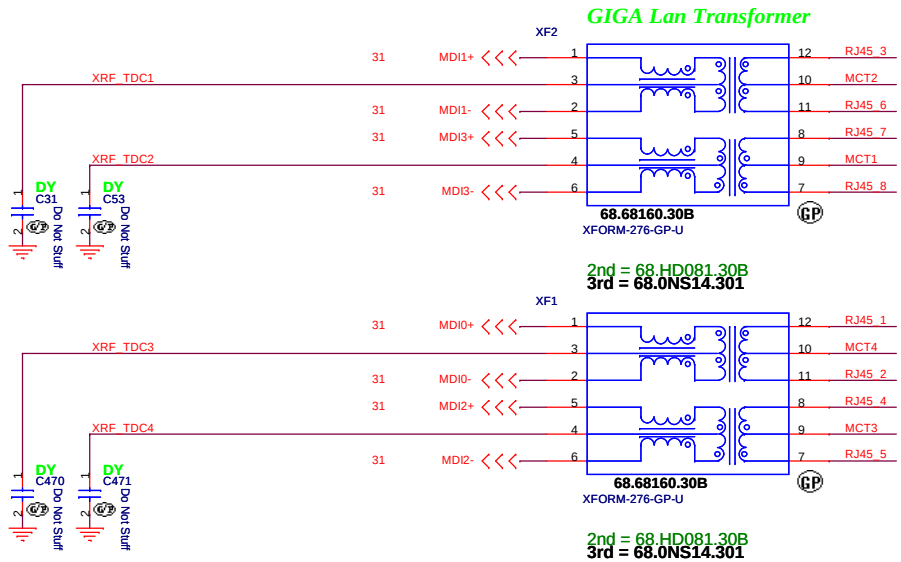
Pre UMA

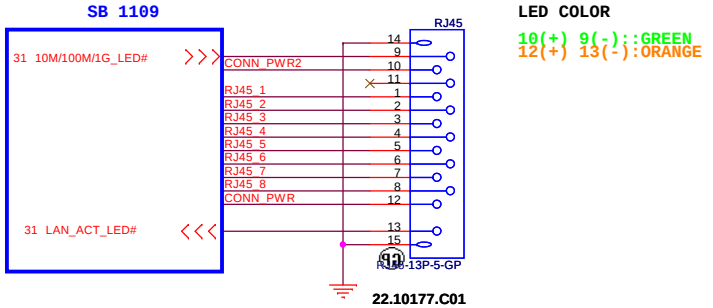
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***BCM57780***
Size: Custom	Document Number: **JE70-CP** — Rev: **-1M**
Date: Tuesday, February 02, 2010	Sheet 31 of 67

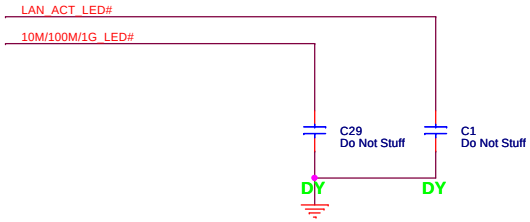
LAN Connector

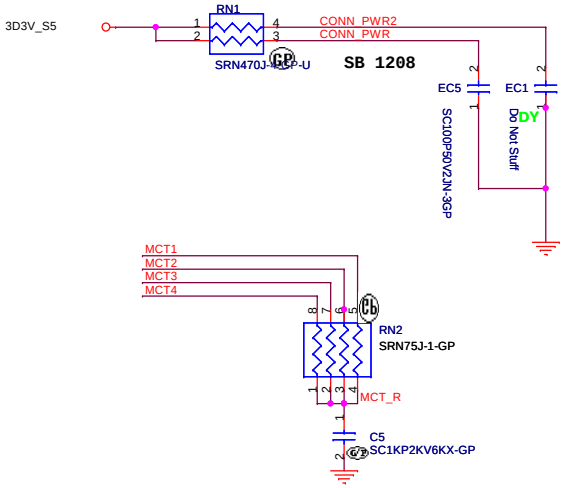
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.









Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN		
Size: A3	Document Number: JE70-CP	Rev: -1M
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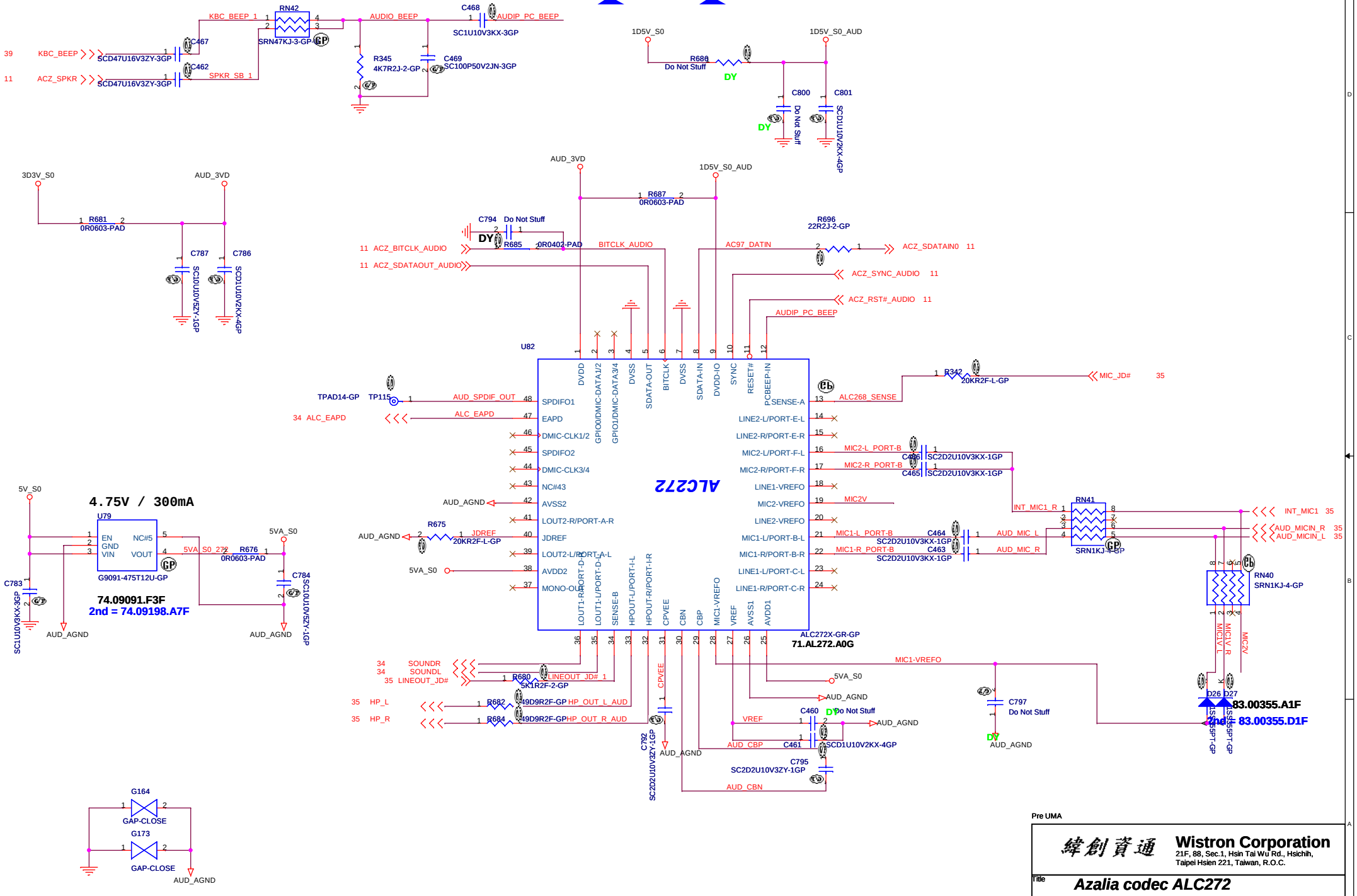


Pre UMA

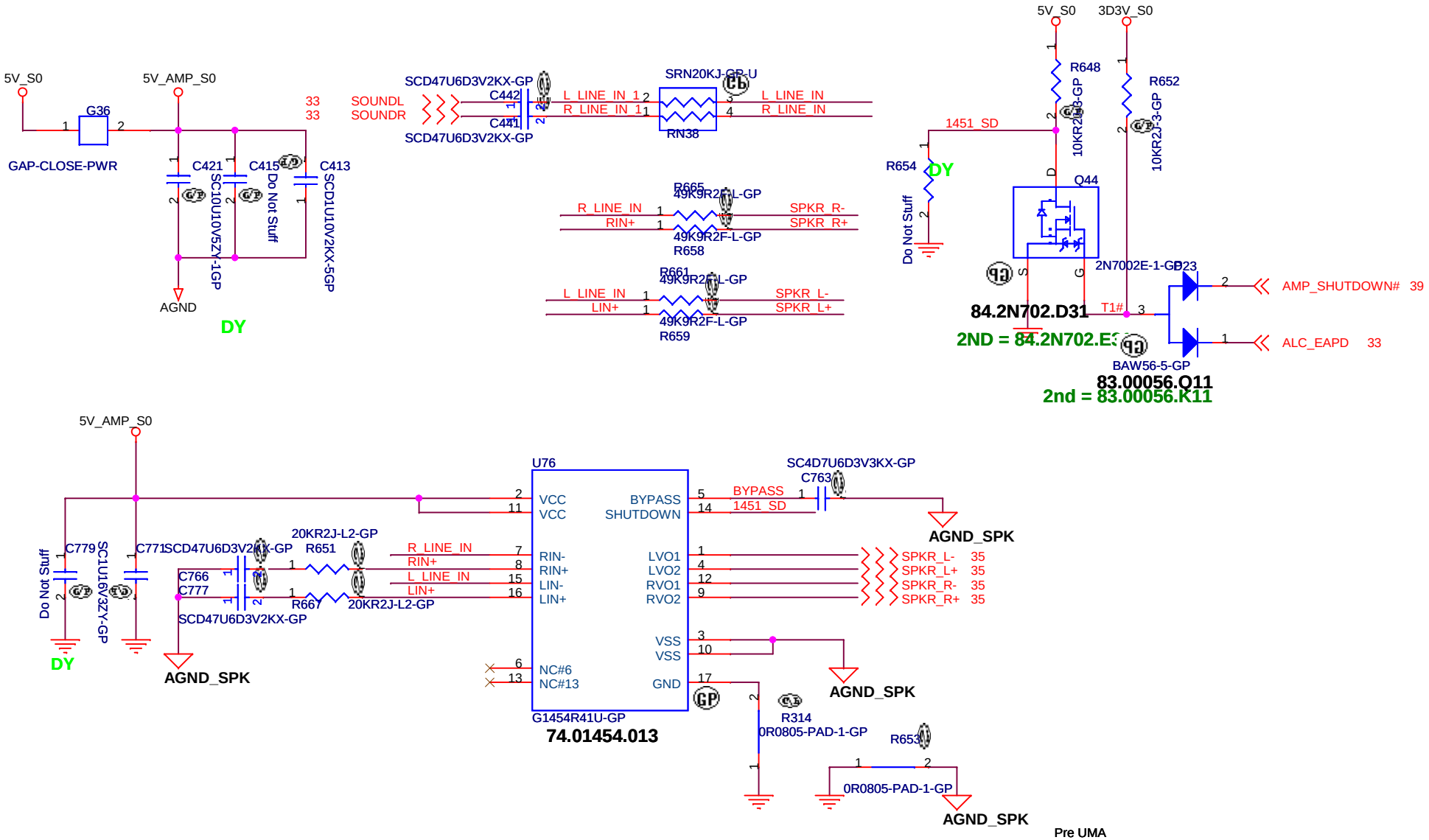
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Azalia codec ALC272

Size	Document Number	Rev
A3	JE70-CP	-1M

Date: Tuesday, February 02, 2010 Sheet 33 of 67

AUDIO OP AMPLIFIER

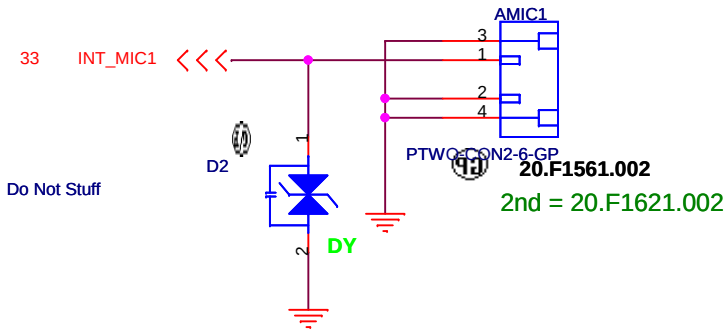


Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO AMP	
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 34 of 67	

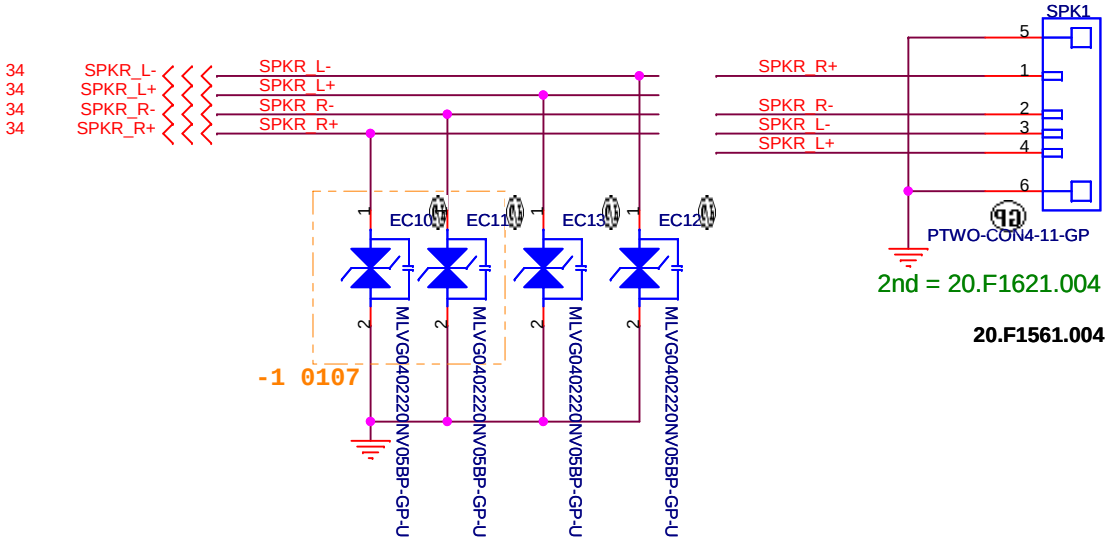
Internal Mic



20.F1561.002

2nd = 20.F1621.002

Internal Speaker



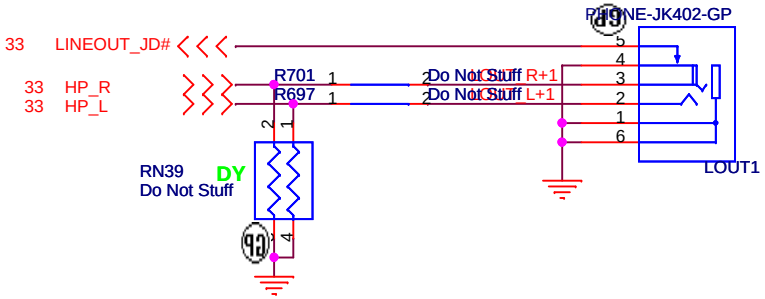
2nd = 20.F1621.004

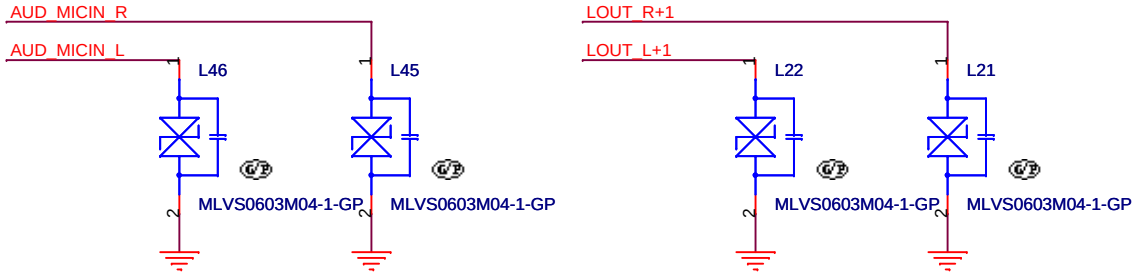
20.F1561.004

LINE OUT

22.10265.261

2nd =

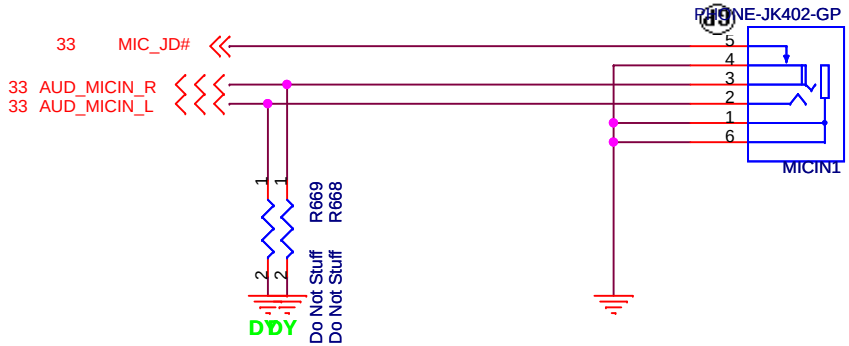




MIC IN

22.10265.261

2nd =



Pre UMA

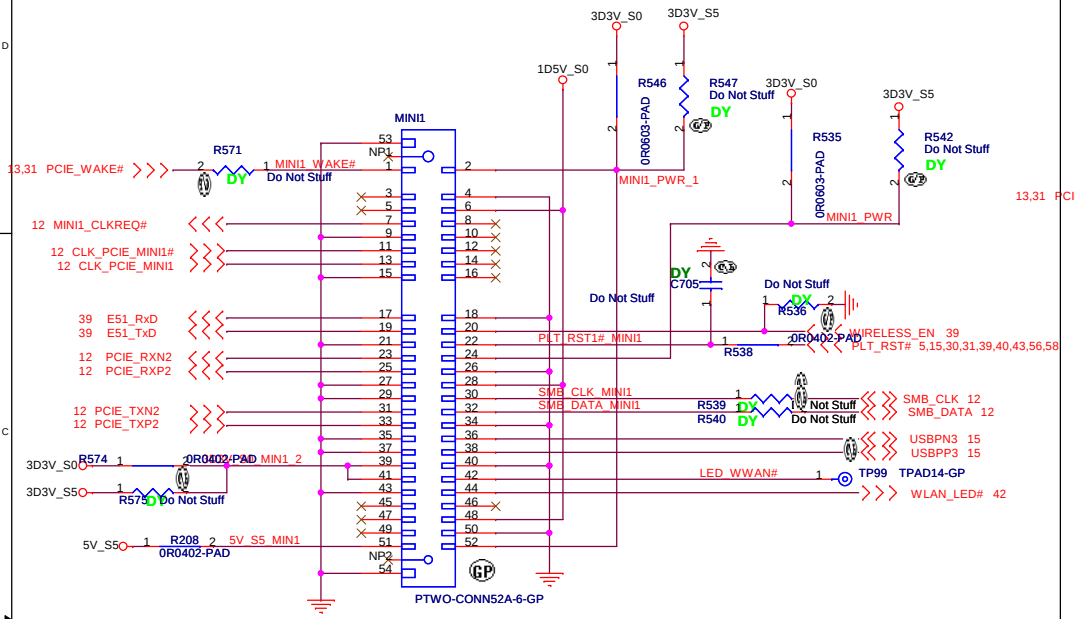
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*AUDIO jack*
Size	Document Number: JE70-CP — Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 35 of 67

Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Cardreader*	
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 36 of 67	

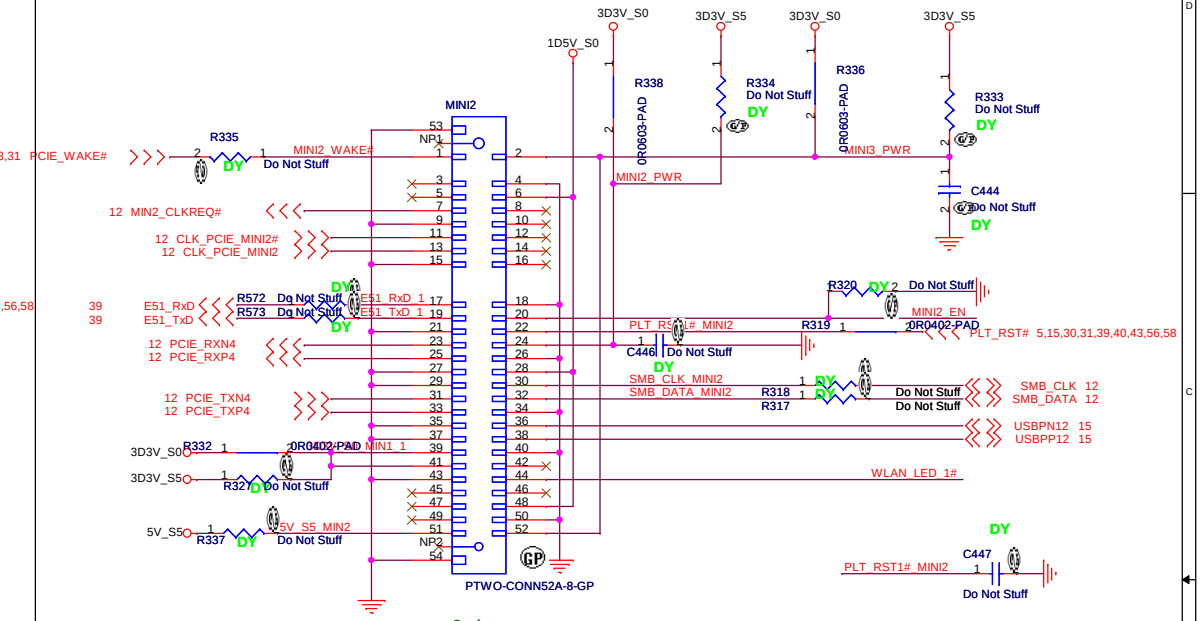
Mini Card Connector(WLAN)
Support debug-card



2nd = 62.10043.461

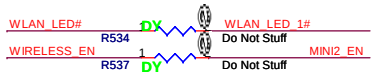
20.F1517.052

Mini Card Connector(Robson2 and 3G)

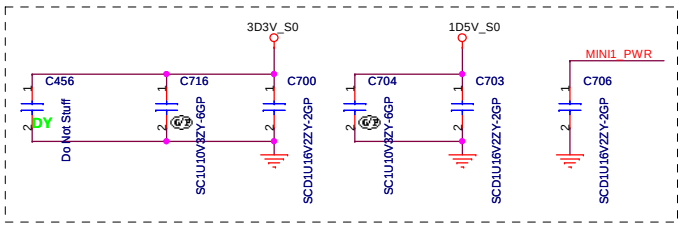


2nd =

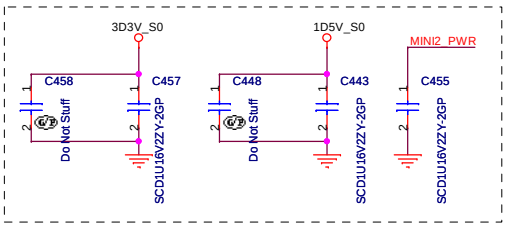
20.F1518.052



Place near MINI1

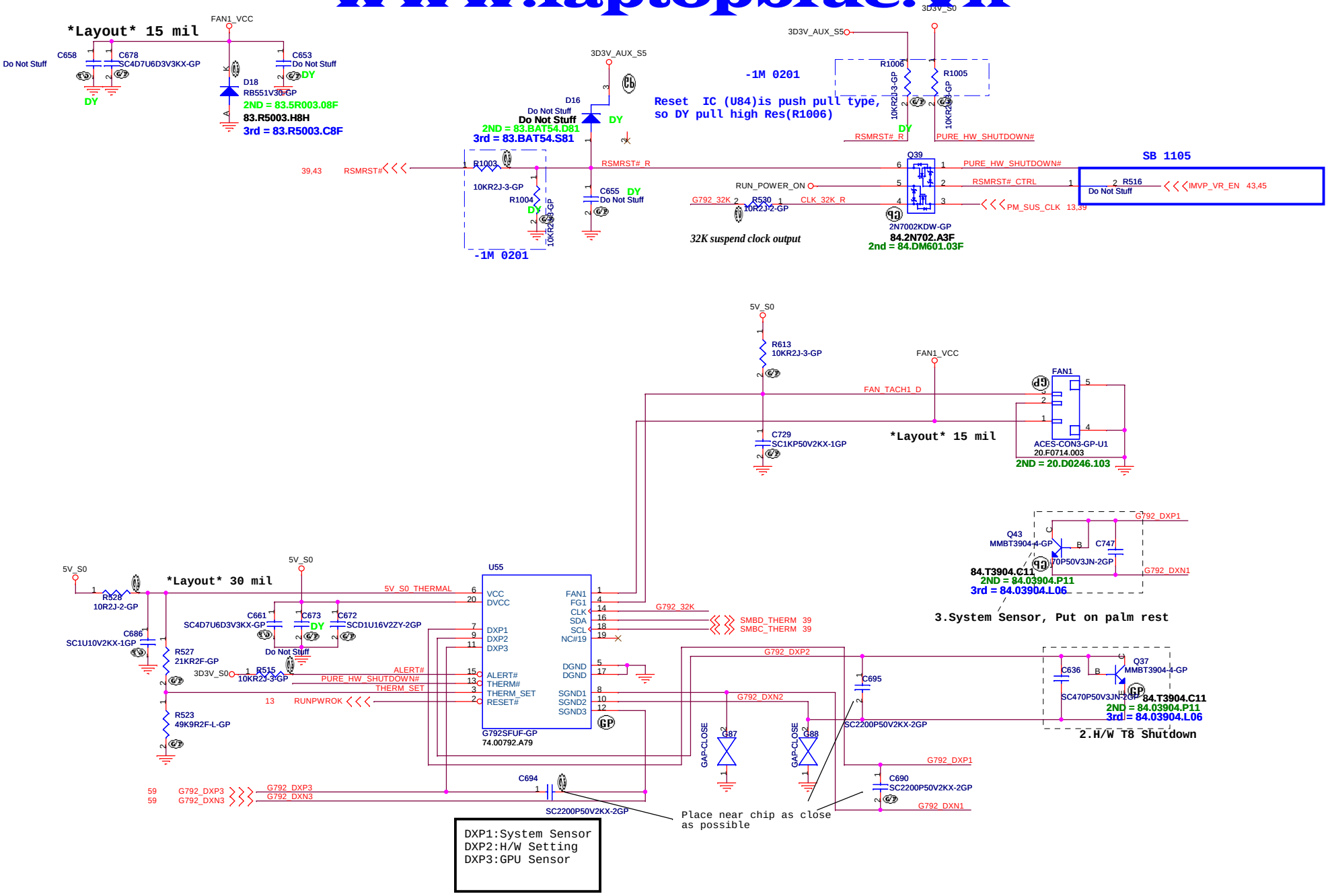


Place near MINIC2



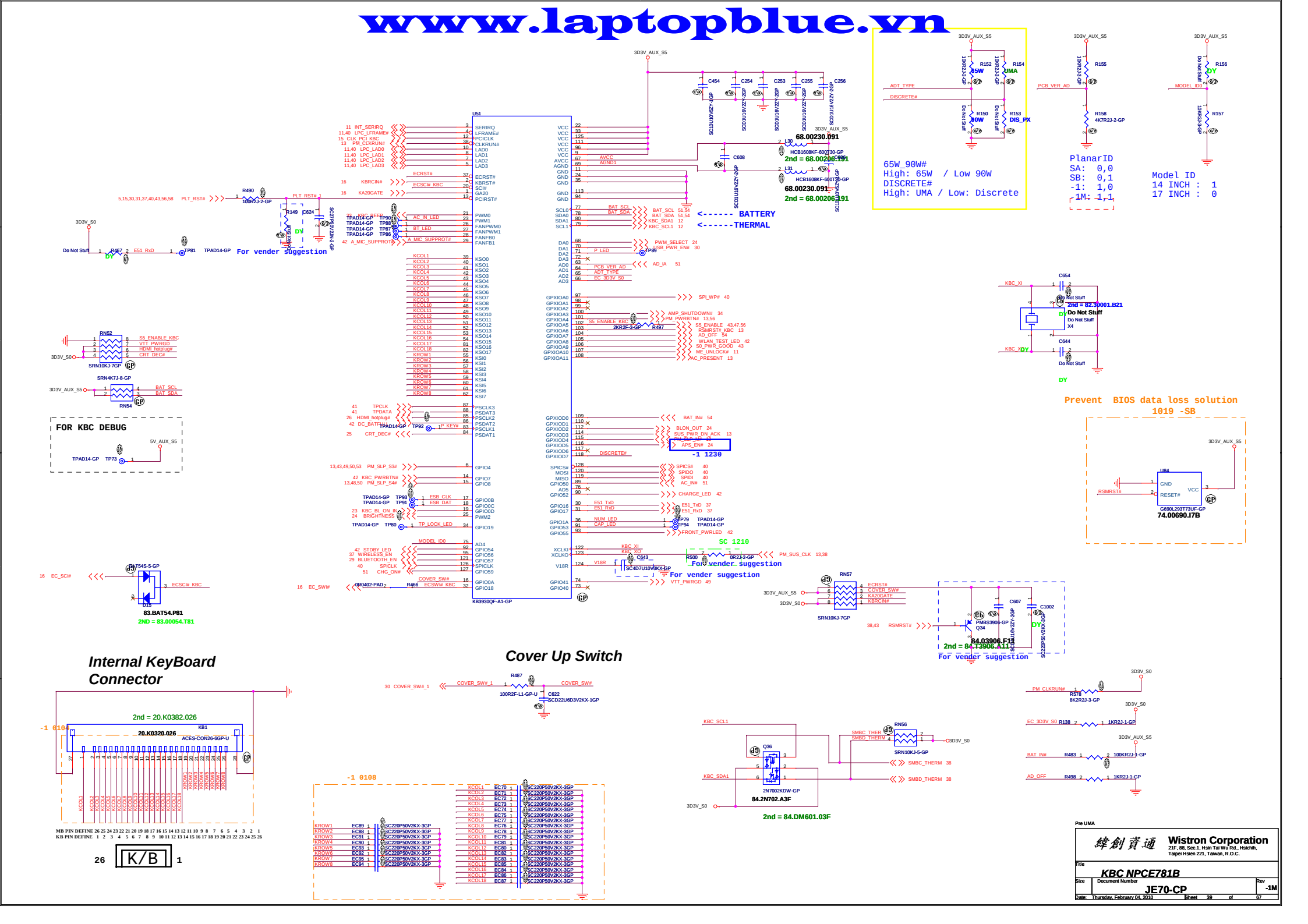
Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
Size: A3	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 37 of 67	

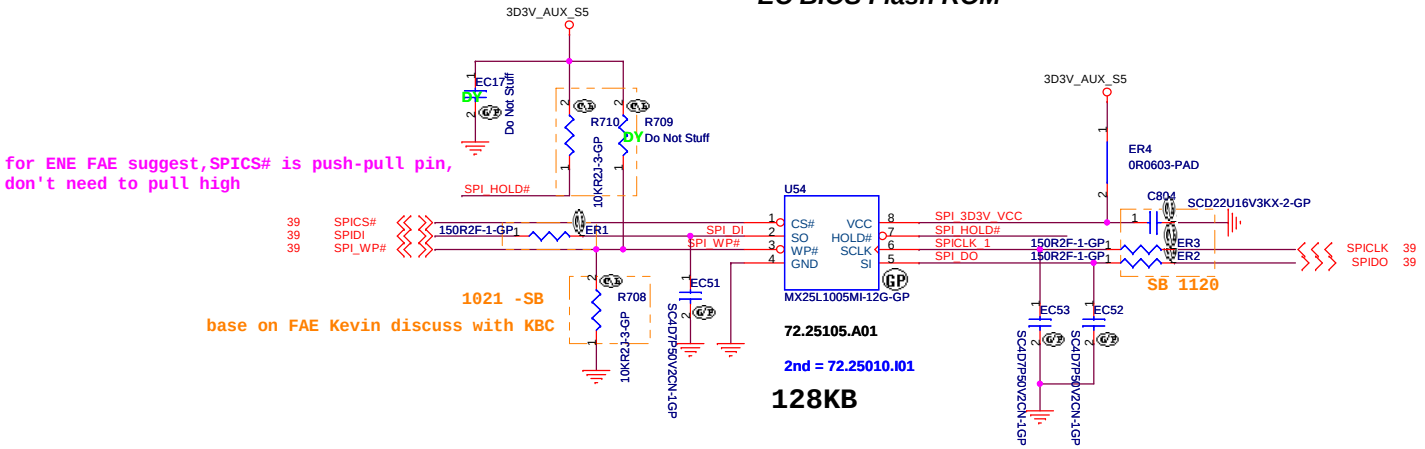


Pre UMA

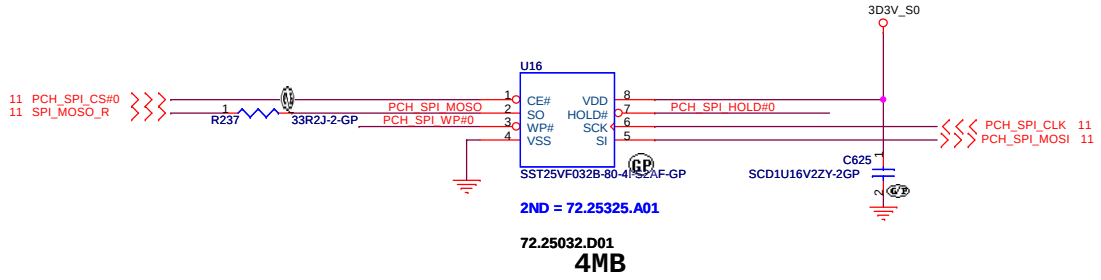
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Thermal/Fan Connector***	
Size	Document Number **JE70-CP**	Rev **-1M**
Date: Wednesday, February 03, 2010	Sheet 38 of 67	



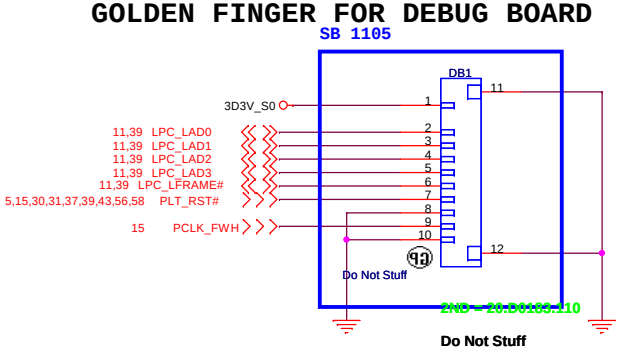
EC BIOS Flash ROM

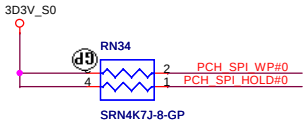


System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD





Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS		
Size	Document Number: JE70-CP	Rev: -1M
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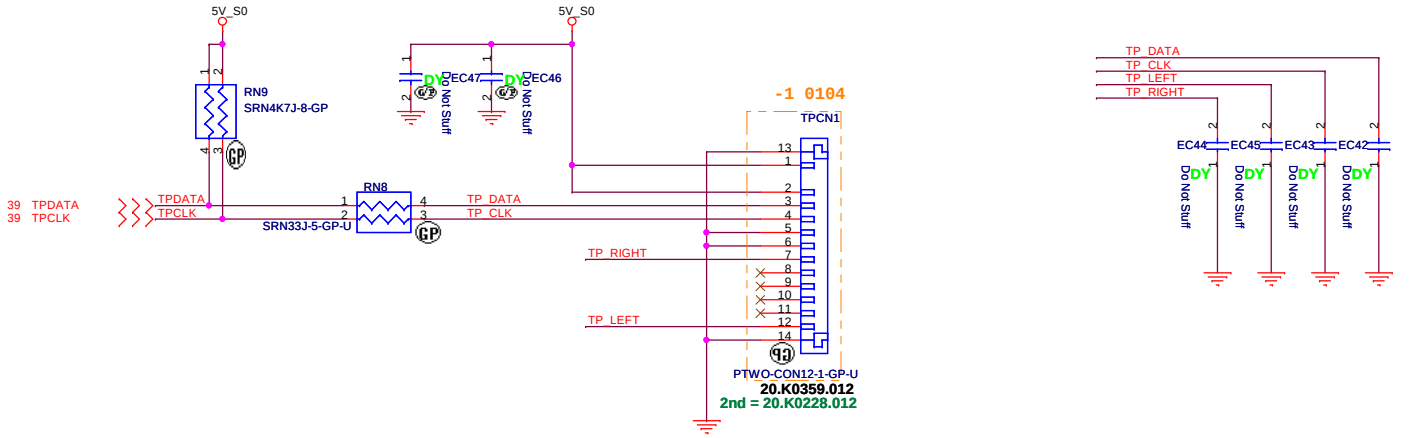
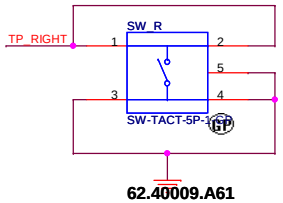
TOUCH PAD

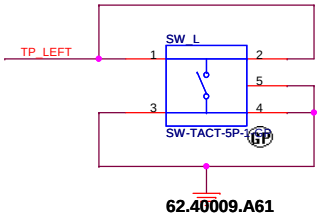


1 12

T/P



62.40009.A61
2nd = 62.40009.B21



62.40009.A61
2nd = 62.40009.B21

Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Touch PAD and FP*

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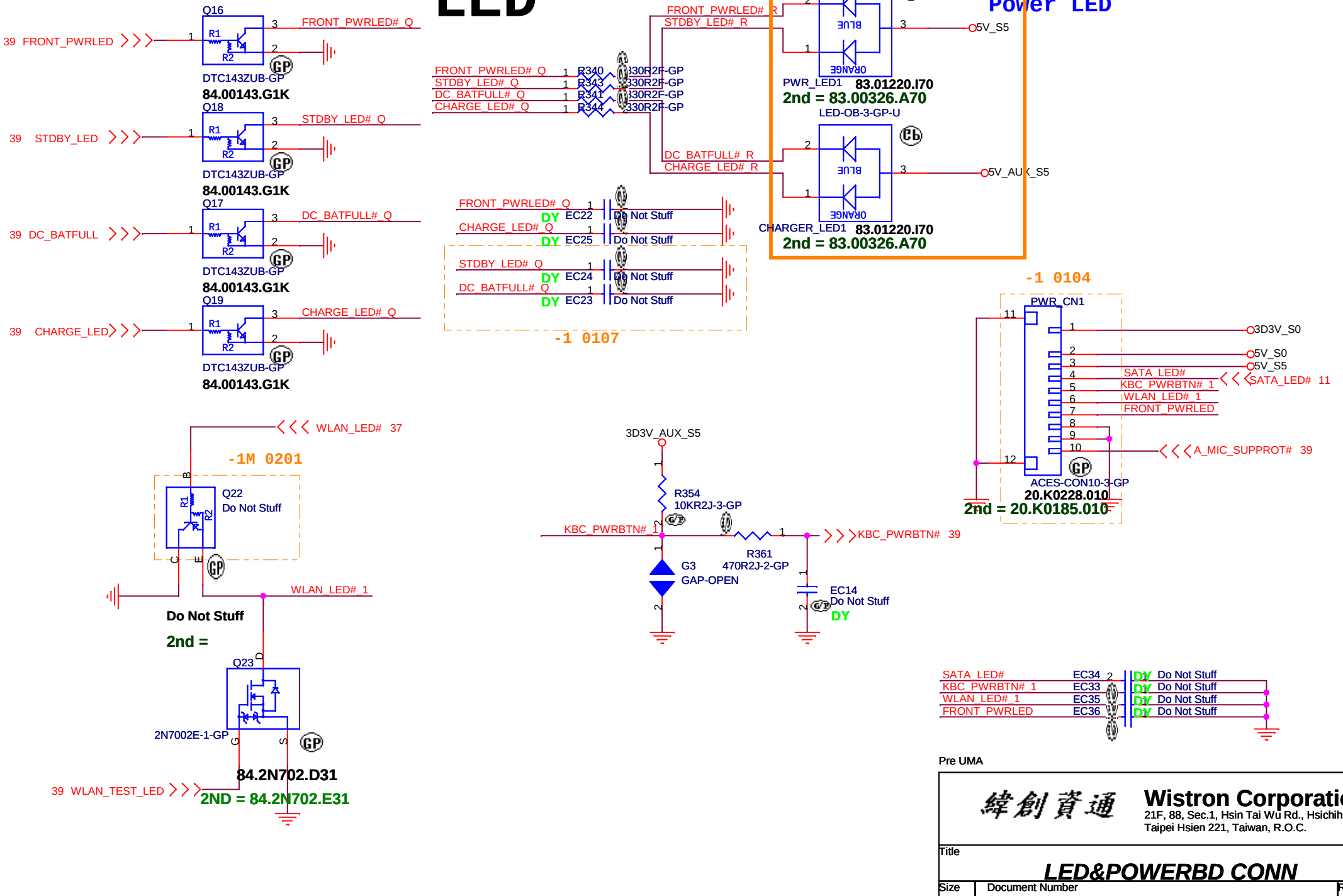
LED

Power LED



Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LED&POWERBD CONN***	
Size	Document Number **JE70-CP**	Rev -1M
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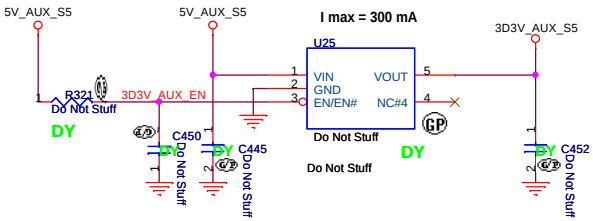
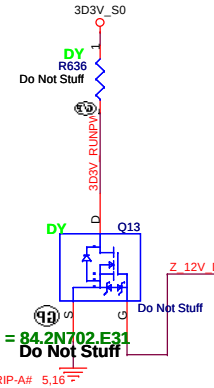
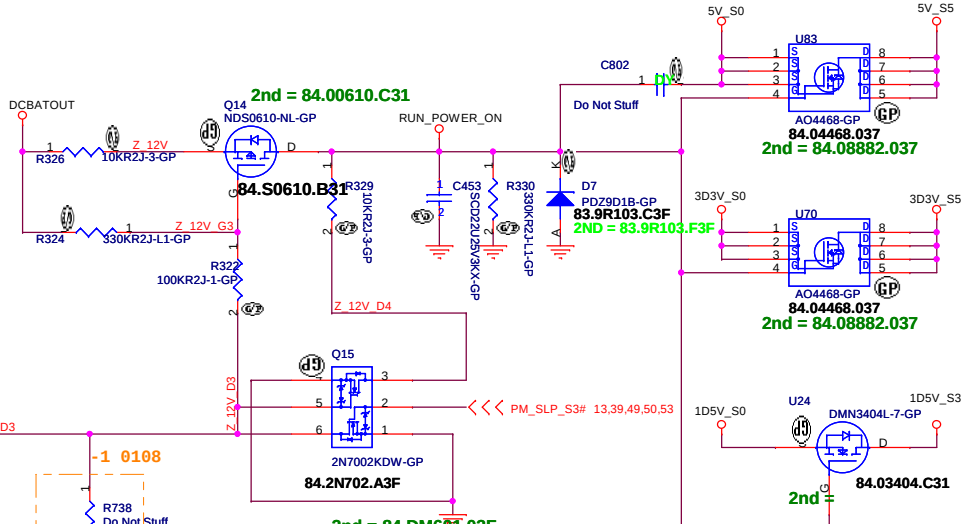
Run Power

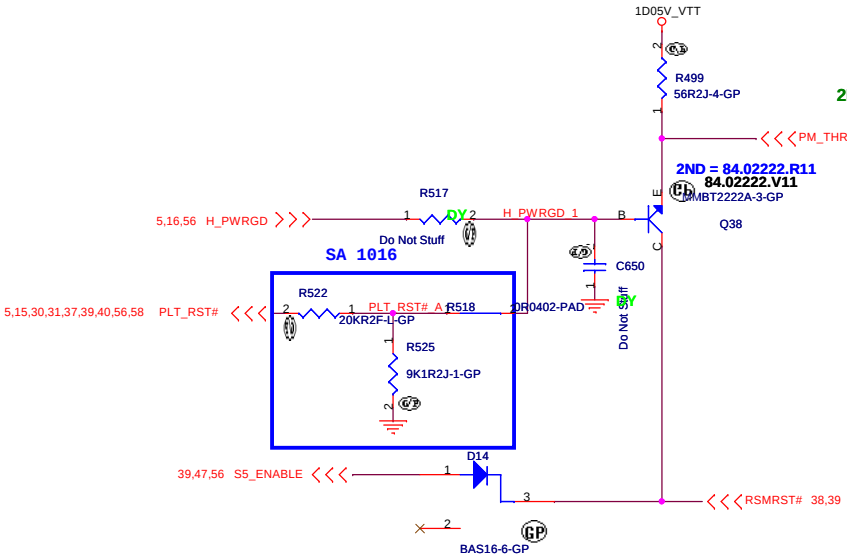
Aux Power

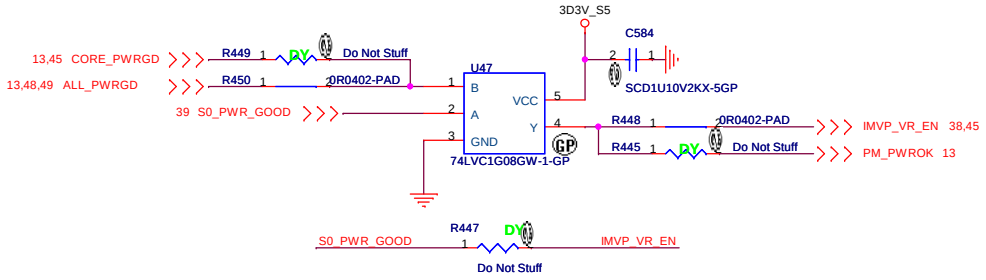
3D3V_AUX_S5

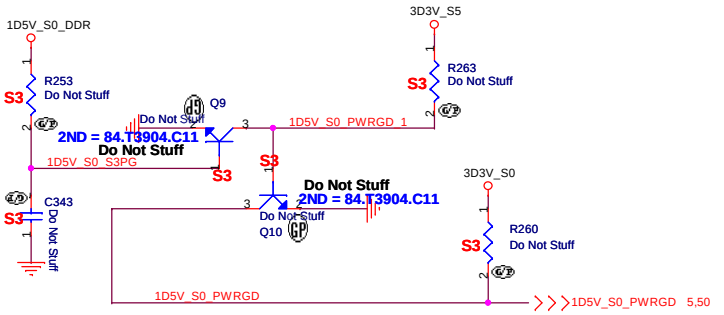












Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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ISL62883 VCC_CORE

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
IMVP_VR_EN
VCC_SENSE
VSS_SENSE
DCBATOUT_62883
5V_S5
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD
CORE_PWRGD
Output Power
VCC_CORE_PWR
VCC_CORE(Imax=65A)

TPS51123 5V/3D3V

DCBATOUT_51123_1
DCBATOUT_51123_2
S5_ENABLE
ALL_PWRGD

Input Power
VIN_1
VIN_2
Input Signal
EN1
EN2
Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)
5V_AUX(O)
3D3V_AUX(O)
5V_S5 (8A)
3D3V_S5 (6A)
5V_AUX_S5 (100mA)
3D3V_AUX_S5 (100mA)

RT9026 0D75V_S0

5V_S5
1D5V_S3
PM_SLP_S3#
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D75V_S0 (1.2A)
DDR_VREF_S3

RT9025 1D5V

5V_S5
DCBATOUT_7141_1D5V
PM_SLP_S4#
ALL_PWRGD

Input Power
VDD
VCC
Input Signal
EN
Output Signal
PGOOD

Output Power
1D5V (O)
1D5V_S3 (10A)

RT9025 1D8V

5V_S5
3D3V_S0
PM_SLP_S3#
ALL_PWRGD

VIN
VLDOIN
EN
PGOOD
1D8V (O)
1D85V_S0

Charger BQ24745

BATT_SENSE
AD+

Input Signal
FBS
Input Power
ACN

Output Signal
ACGOOD#
SRSET
Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA
BT+
DCBATOUT

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)
Input Power
VCC(I)
VCC(I)

Output Signal
(O)
Output Power
VCC(O)

AD_IN#
AD+

RT8209B 1D05V

5V_S5
DCBATOUT_RT8209B_1D05V
PM_SLP_S3#
ALL_PWRGD

Input Power
VDD
VCC
Input Signal
EN
Output Signal
PGOOD

Output Power
1D05V (O)
1D05V_S0 (10A)

Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram
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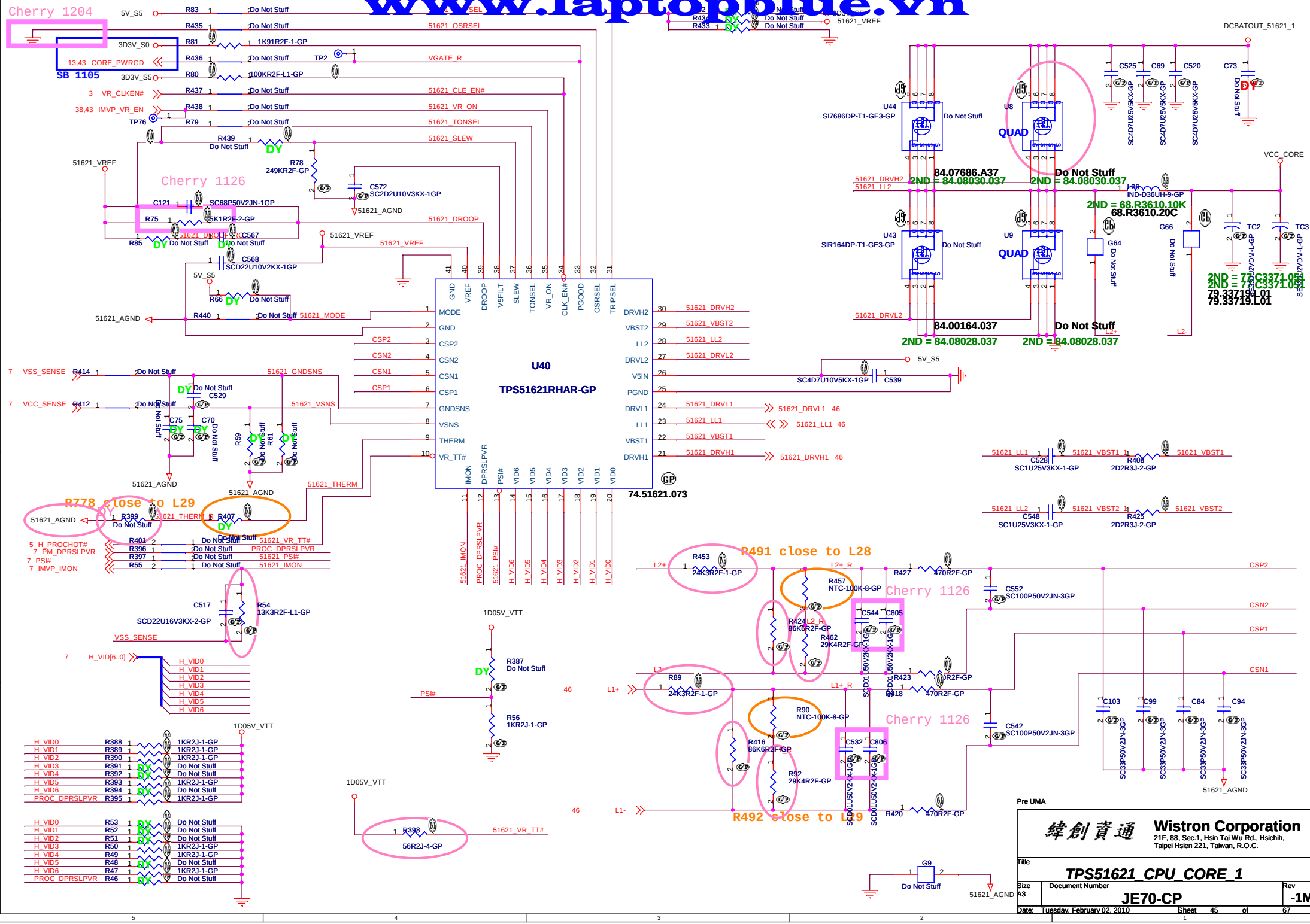
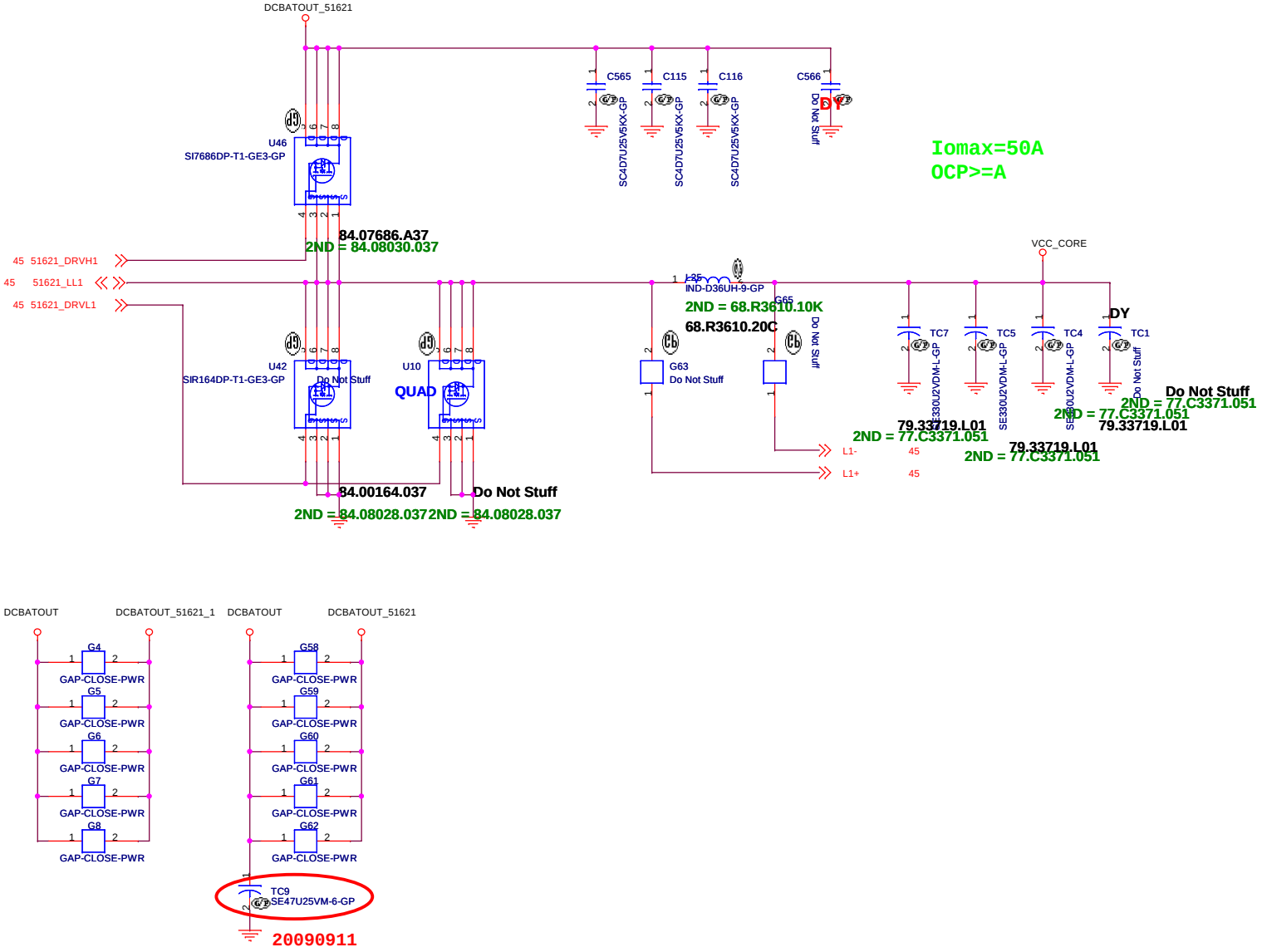
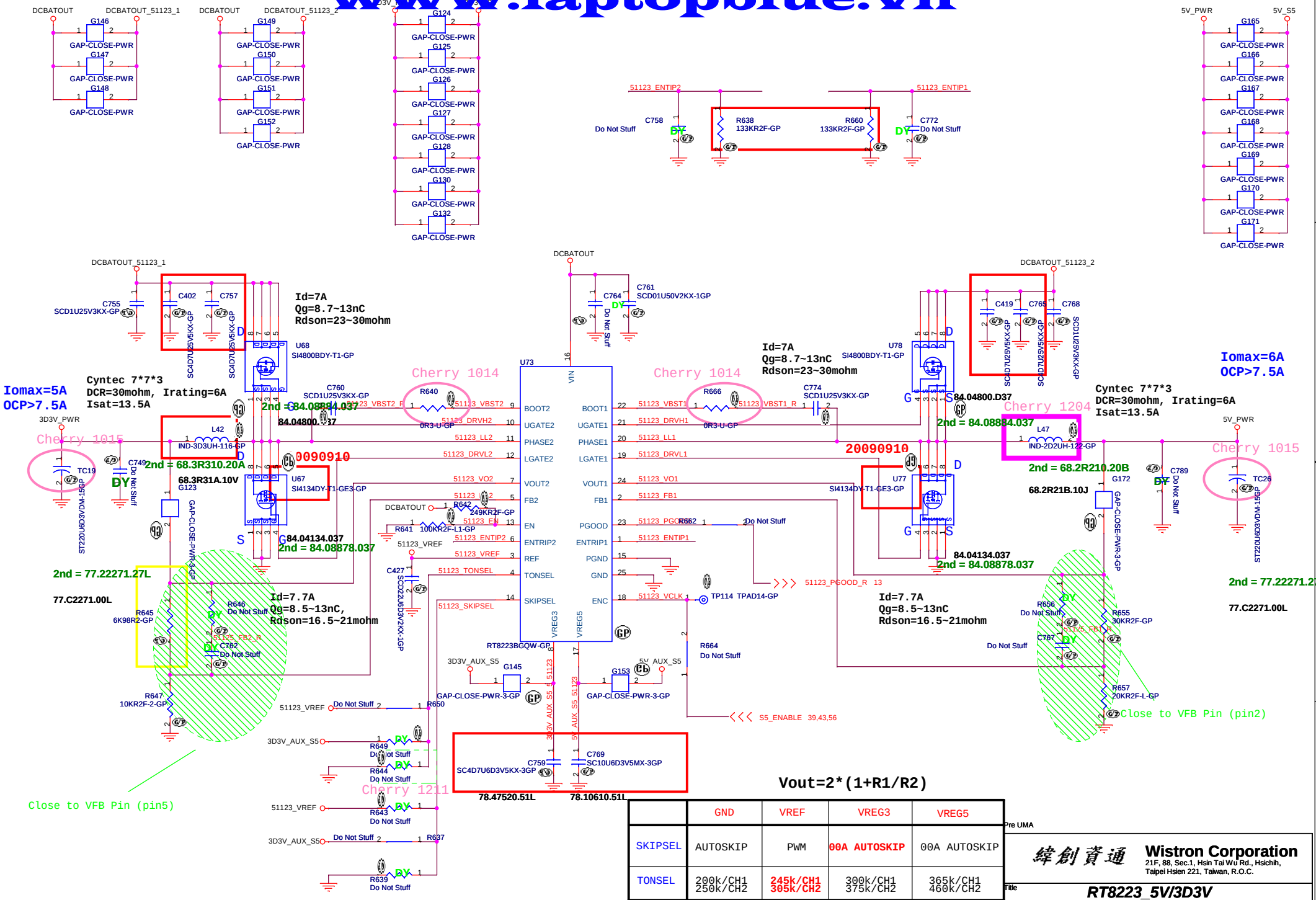




Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *ISL62882 CPU CORE (1/2)*		
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 46 of 67	



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223_5V/3D3V

Size: | Document Number: JE70-CP | Rev: -1M

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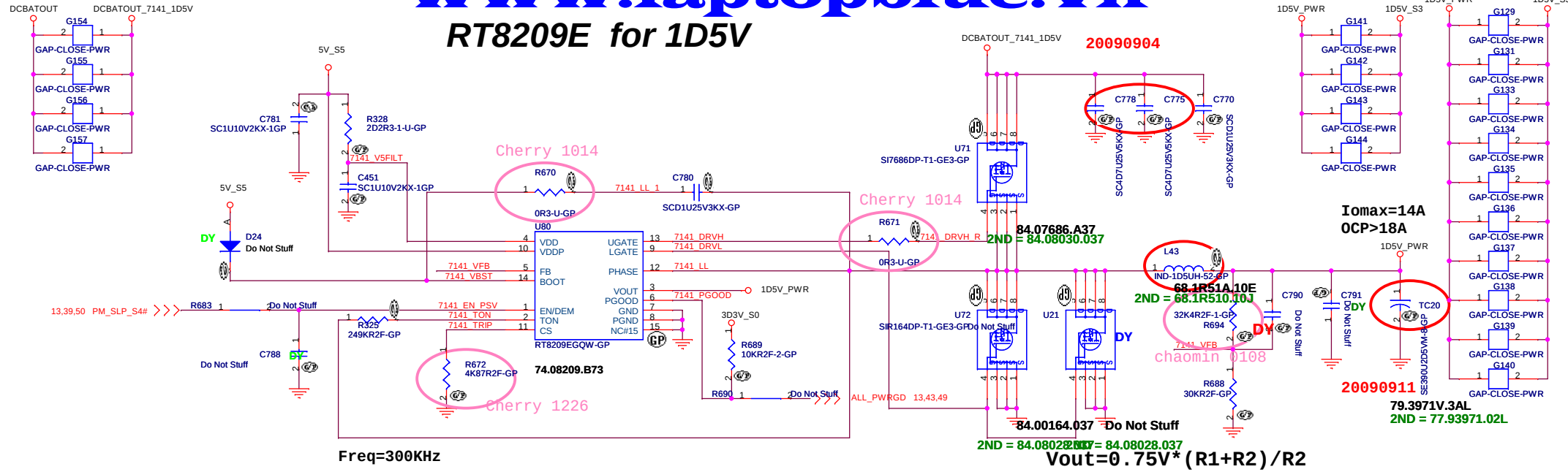
RT8209E for 1D5V



Pre UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E 1D5V

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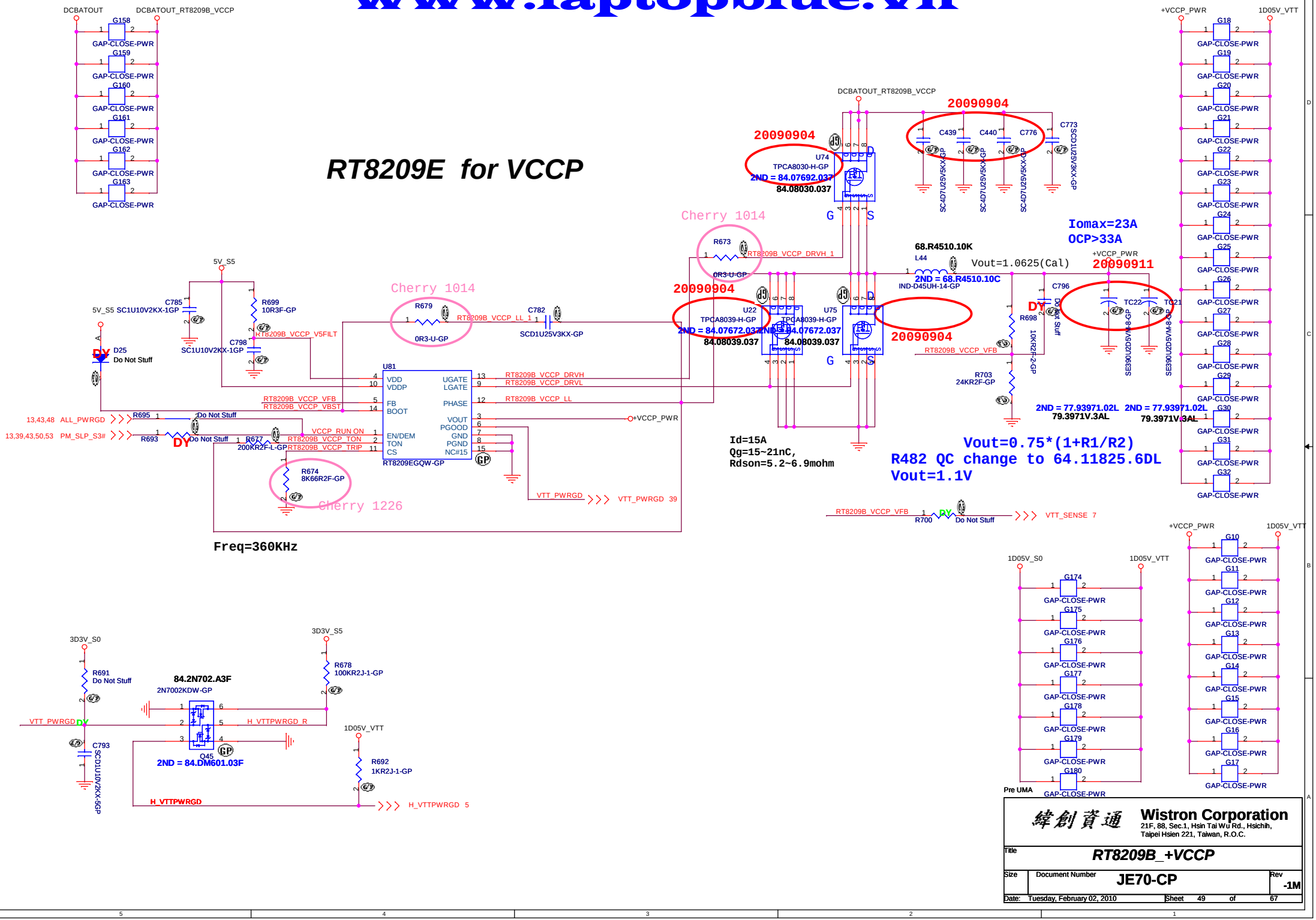
RT8209E for VCCP



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8209B_+VCCP	
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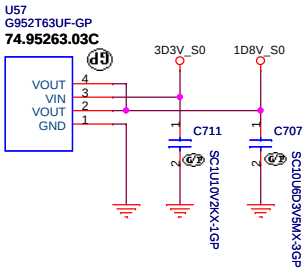
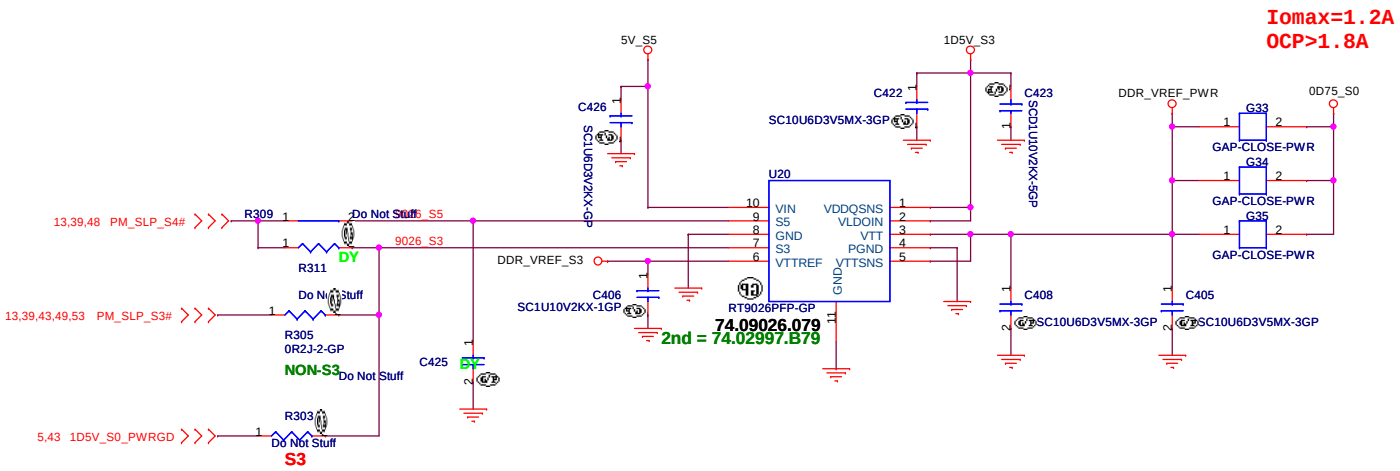
1.8V_S0 1.8V 1A Regulator



RT9026 for 0D75V_S3



Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8015A for 1D8V/RT9026_0D75	
Size	Document Number JE70-CP	Rev -1M
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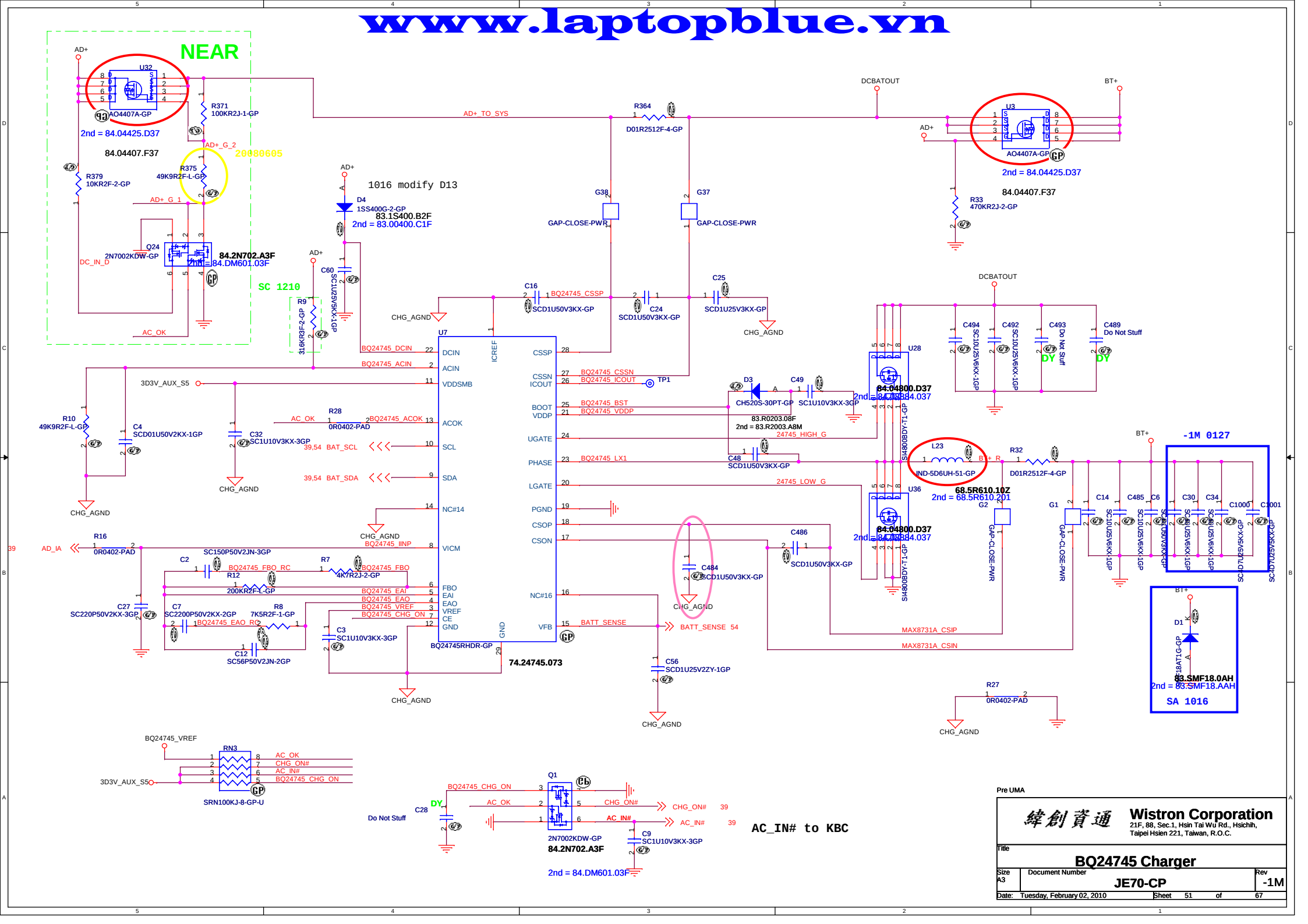

Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BQ24745 Charger**

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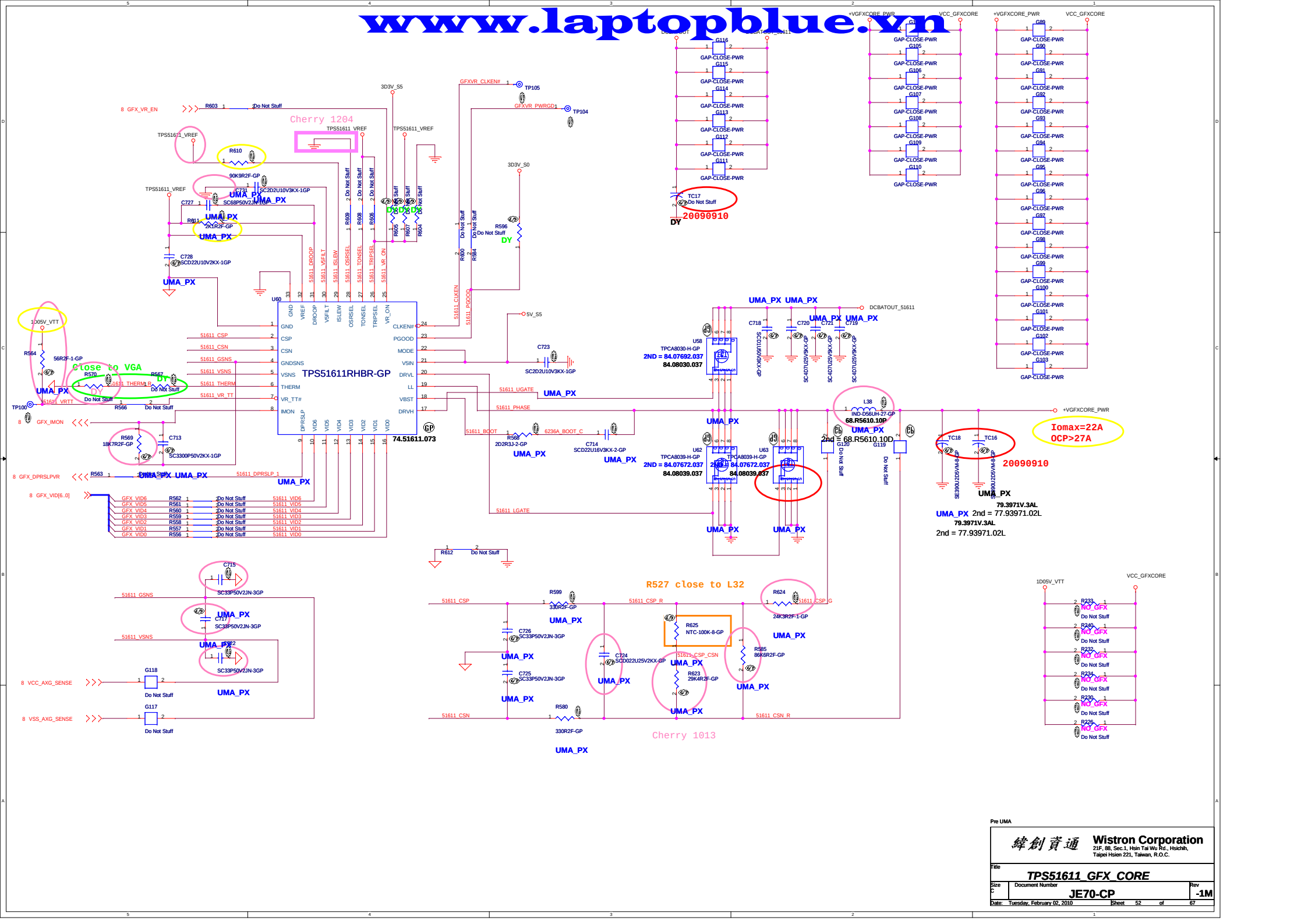

Pre UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51611_GFX_CORE

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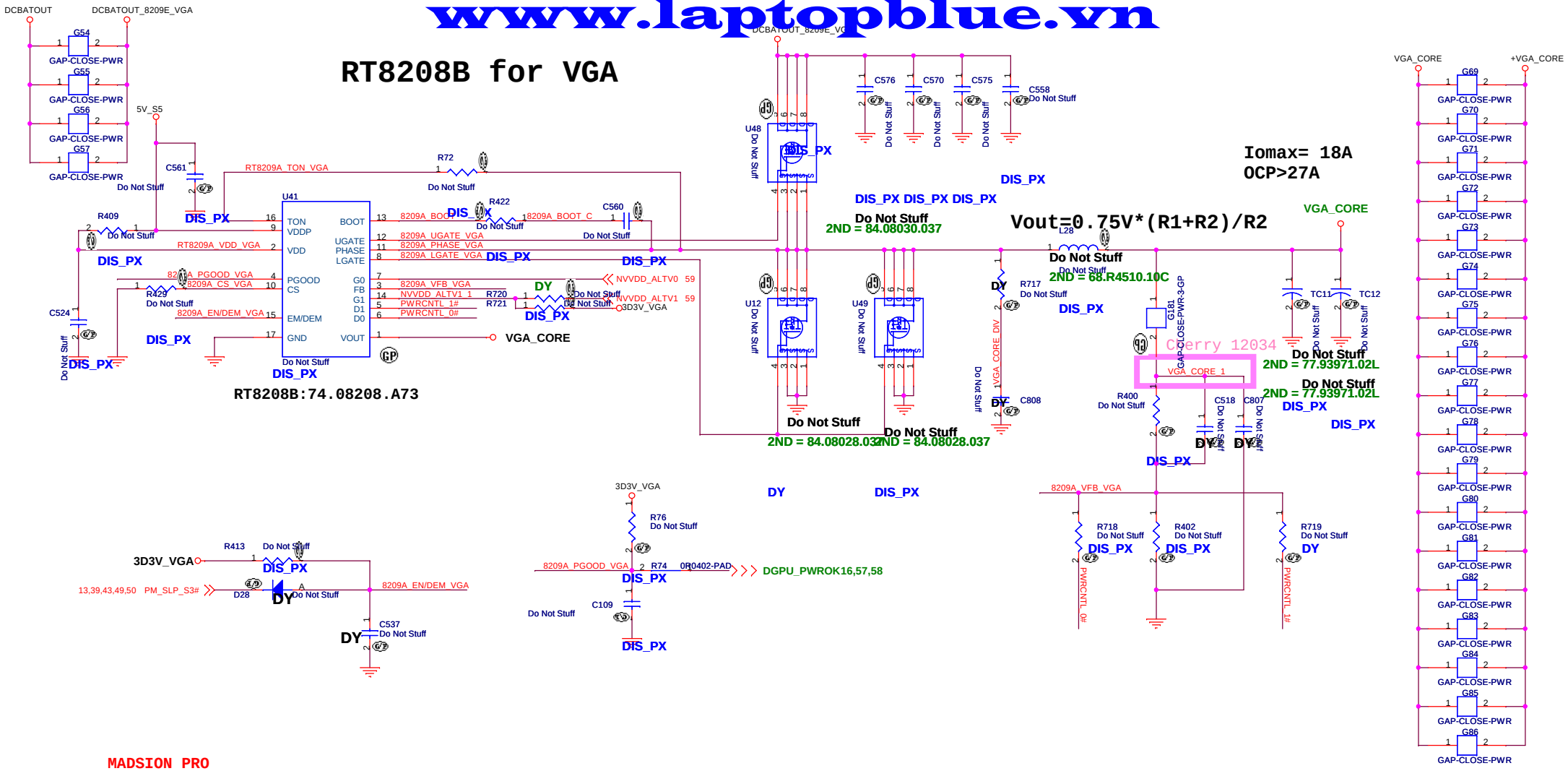
RT8208B for VGA



MADSION PRO

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V

PARK XT

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.12V GPU VOLTAGE H: 0.90V

Park==>R718=33K (64.33025.6DL)
Madison==>R718=71.5K (64.71525.6DL)

NVVDD_ALTV1	NVVDD_ALTV0	+VGA_CORE
H	L	1.12V or 1V OUT=[R400+(R402//R718)}/(R402//R718)
H	H	0.9V OUT=(R400+R402)/R402

Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E VGA CORE

Size: A3 | Document Number: JE70-CP | Rev:

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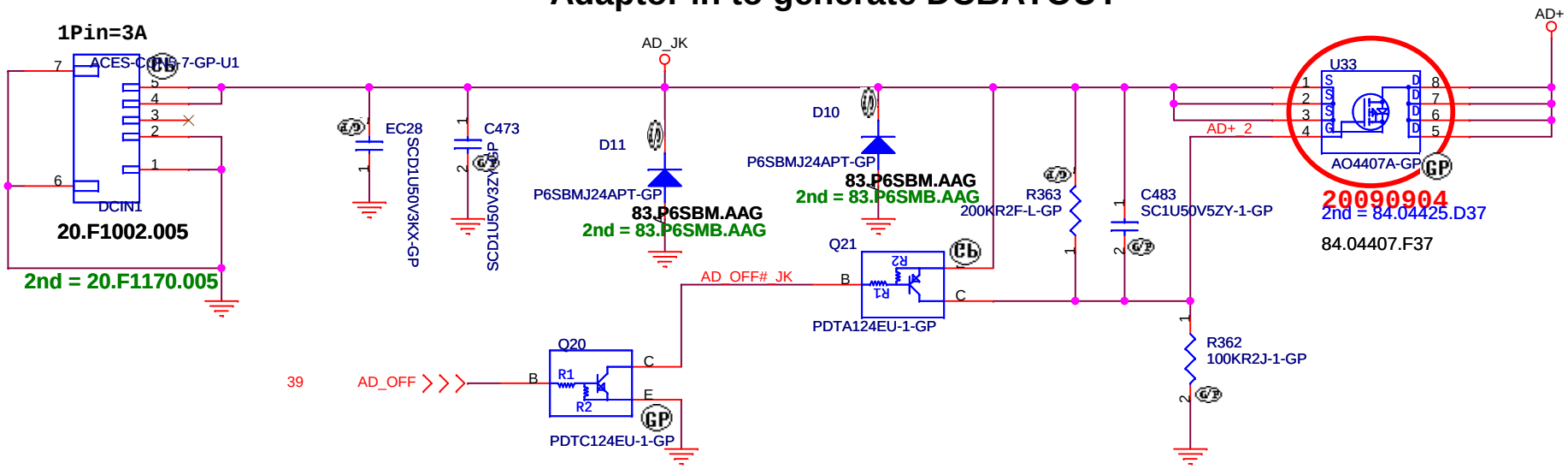
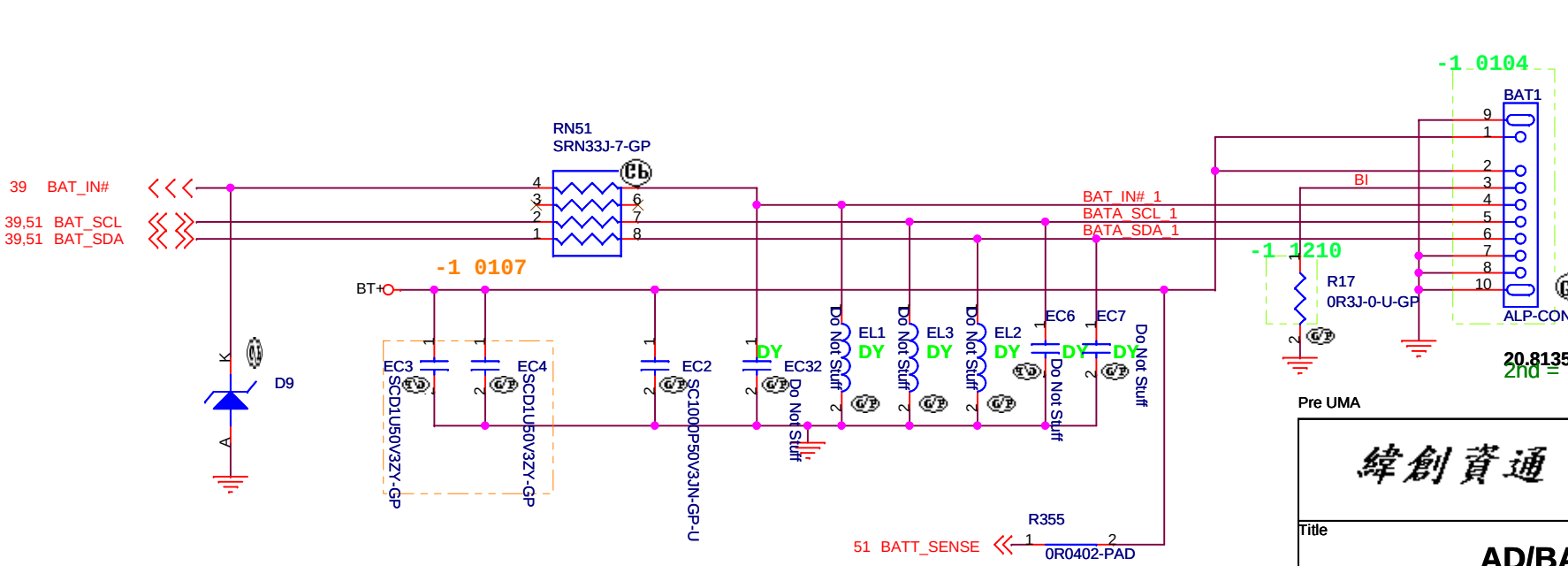
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



Pin NO	Symbol
1	GND
2	GND
3	SMD
4	SMC
5	TS
6	B/I
7	BT+
8	BT+

Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

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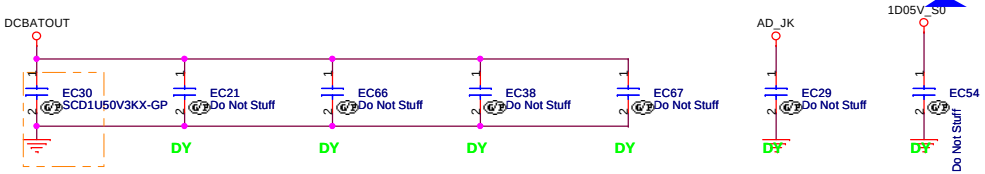
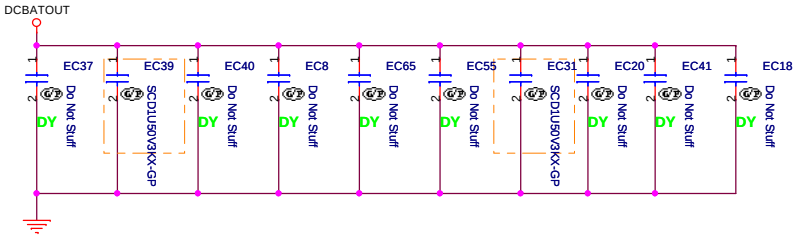
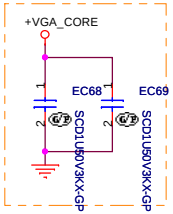
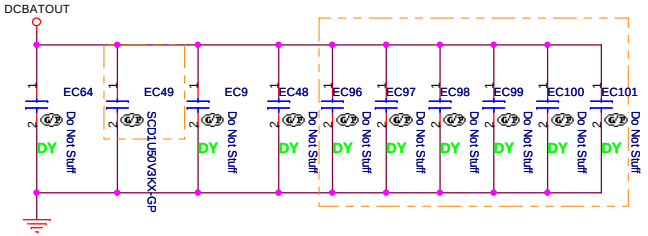


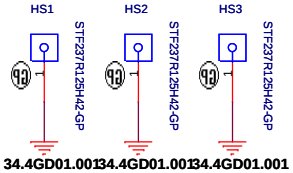


SB 1120

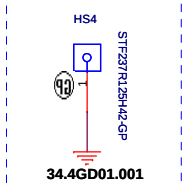




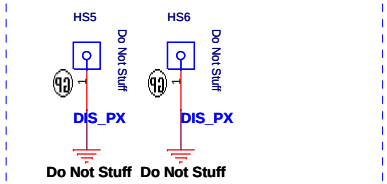
CPU



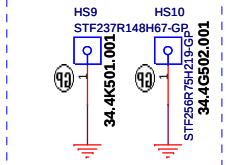
PCH

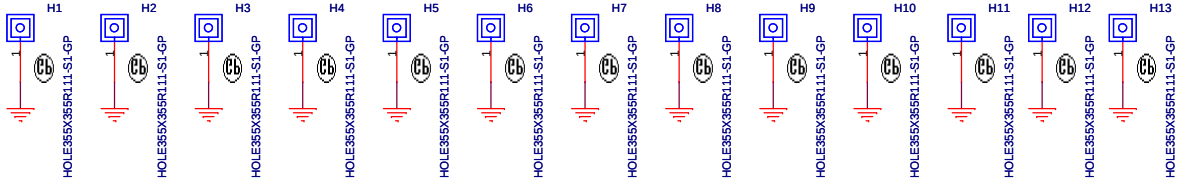


VGA



MINICARD





Pre UMA

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Title	***EMI/Spring/Boss***	
Size	Document Number **JE70-CP**	Rev -1M
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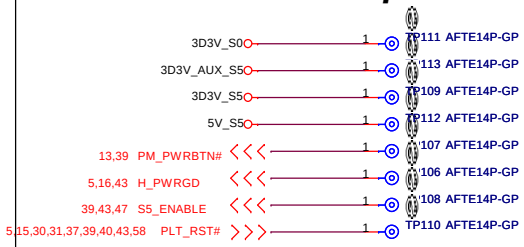
Check test point



Test Point放在Dimm Door打開可量測處

Pre UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	***AFTE_TP***	
Size	Document Number **JE70-CP**	Rev **-1M**
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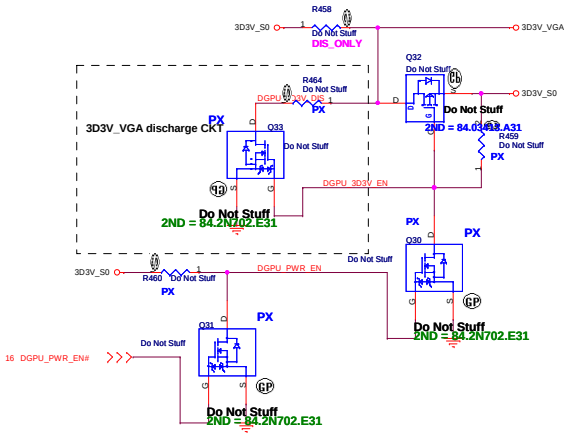
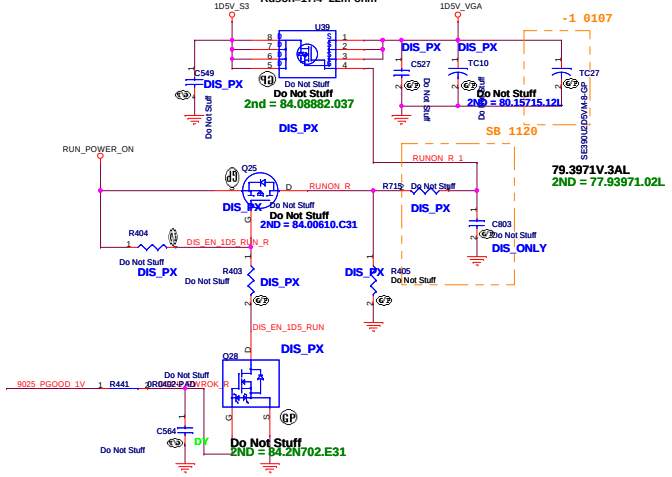
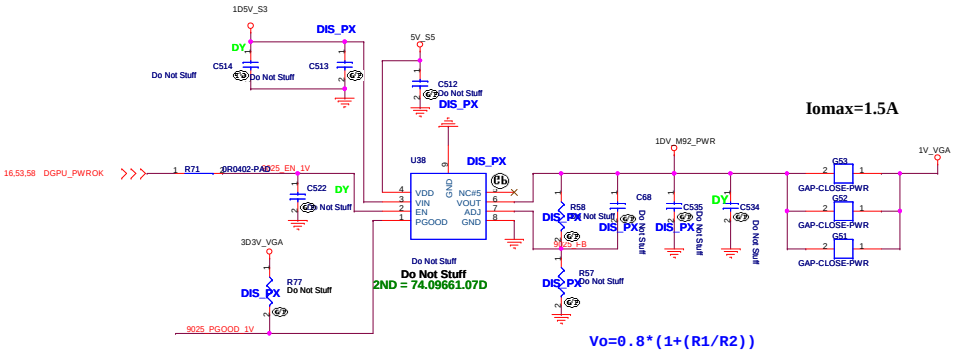
+3VS to 3.3V_DELAY Transfer

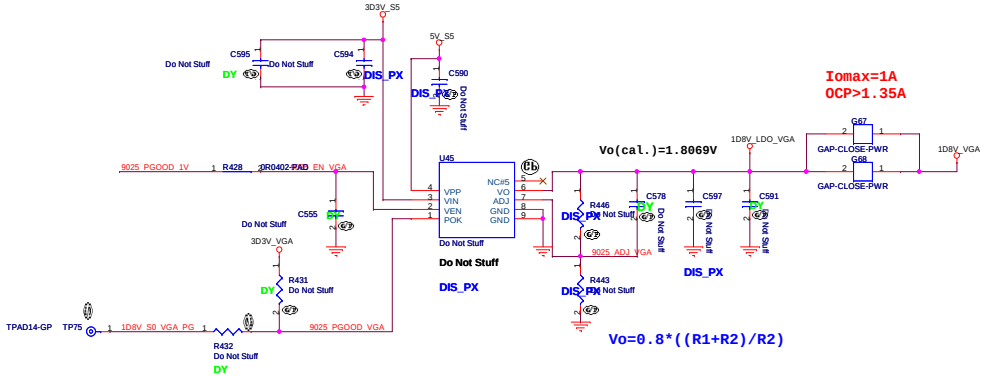




RT9025 for 1V_VGA



G9661 for 1D8V_VGA



Pre UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI POWER

Size	Document Number	Rev
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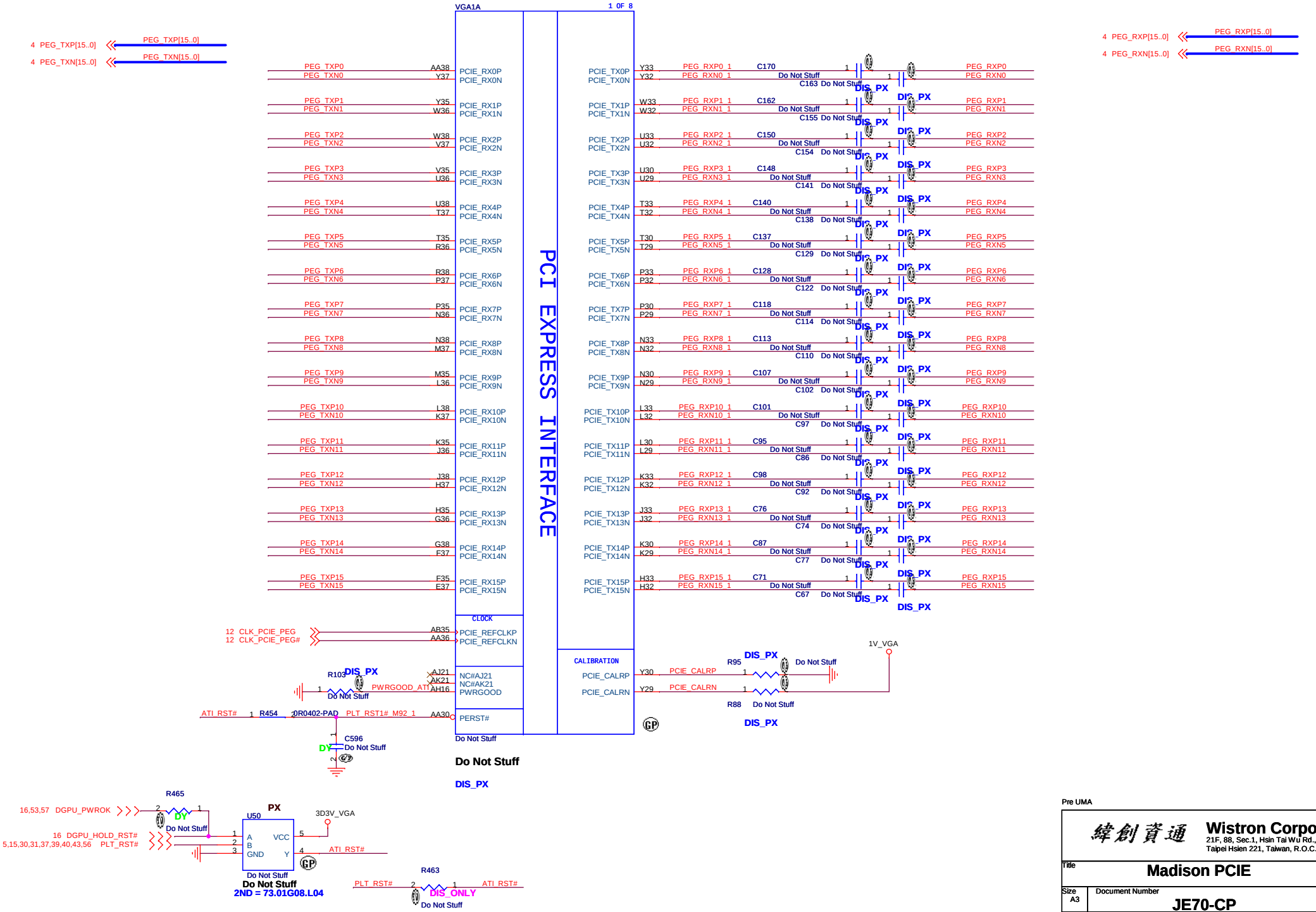

Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Madison PCIE		
Size: A3	Document Number: JE70-CP	Rev: -1M
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Layout notice:
It should be pleace near HDMI connector

JV50-CP_JV70-CP_SJV50-CP / Madsion-Pro

0 1 0 0 Hynix Orion-die (H5TQ1G63BFR-12C, 800MHz)64*16 x 8 pcs2GB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 8 pcs1GB
1 1 0 0 Reserve64*16 x 8 pcs1GB

JV50-CP_JV70-CP_SJV50-CP / Park-XT

0 1 0 0 Hynix Orion-die (H5TQ1G63BFR-12C, 800MHz)64*16 x 4 pcs512MB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 4 pcs512MB
1 1 0 0 Reserve64*16 x 4 pcs512MB

It's strap for GDDR3-136ball
Need to Clarify

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

SB 1118
For Thermal sensor

SB 1120

SB 1117

Pre UMA

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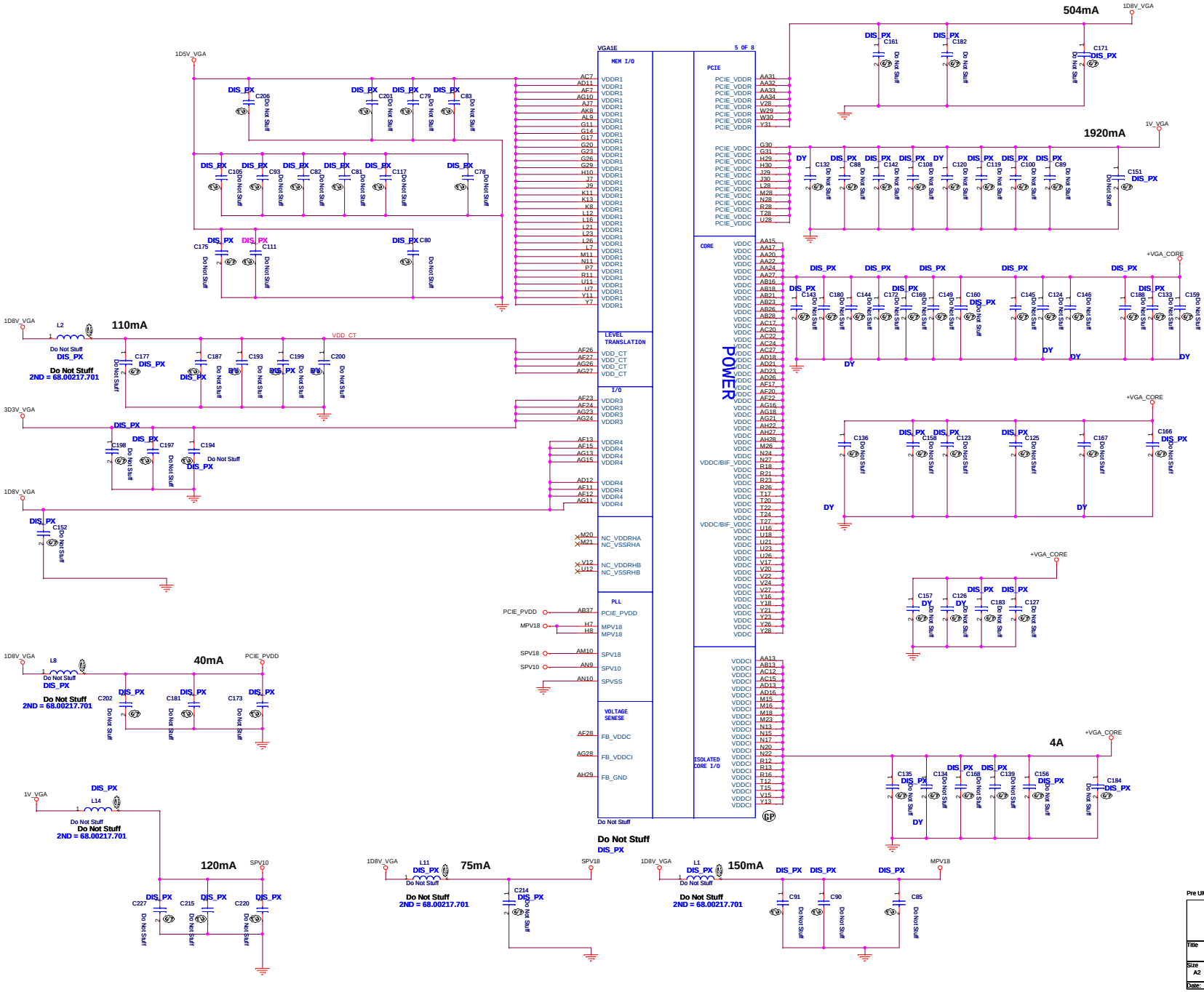
Title: Madison IO		
Size: A2	Document Number: JE70-CP	Rev: SB
Date: Tuesday, February 02, 2010	Sheet 59 of 67	



Pre UMA

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Madison POWER
Size A2 / Document Number	JE70-CP / Rev -1M
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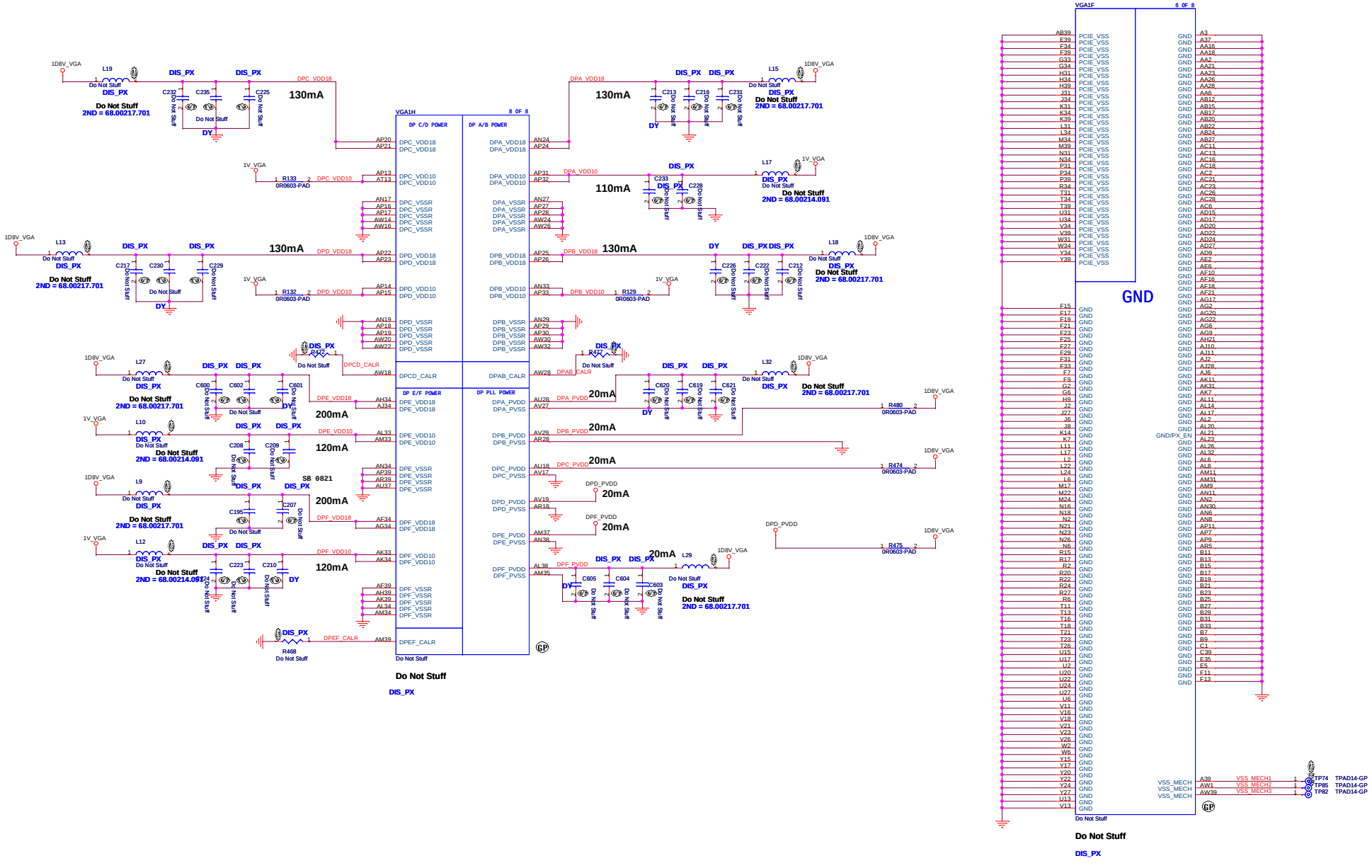
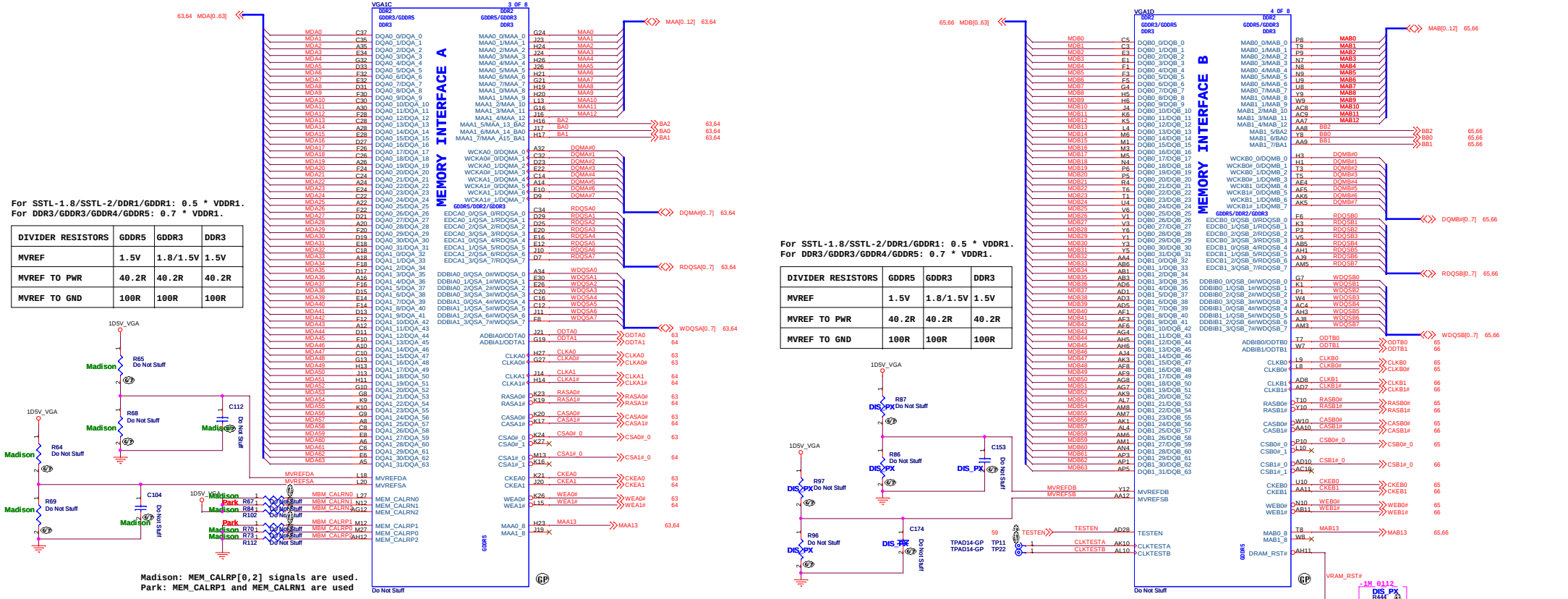


Pre UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DP POWER_GND	
Size: A2	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 61 of 67	



DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

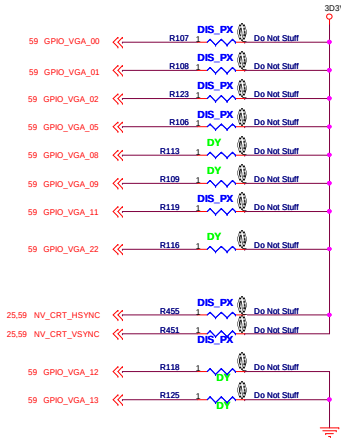
STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			



Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

Pre UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison Memory / Straps

Size: A2 | Document Number: JE70-CP | Rev: -1M

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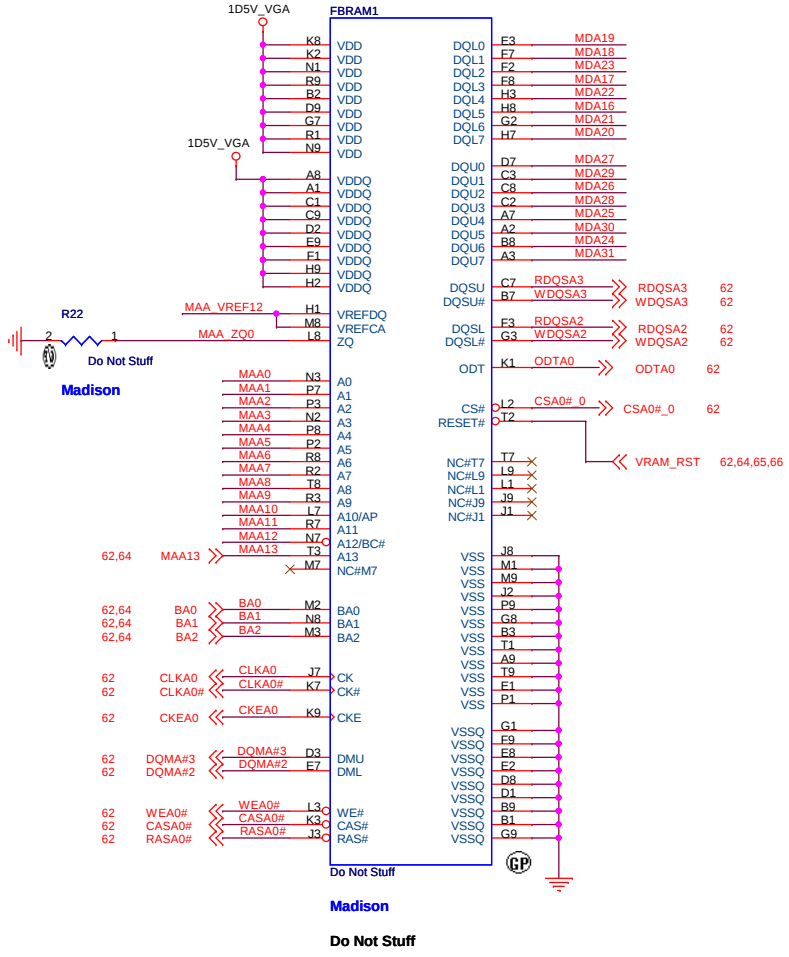
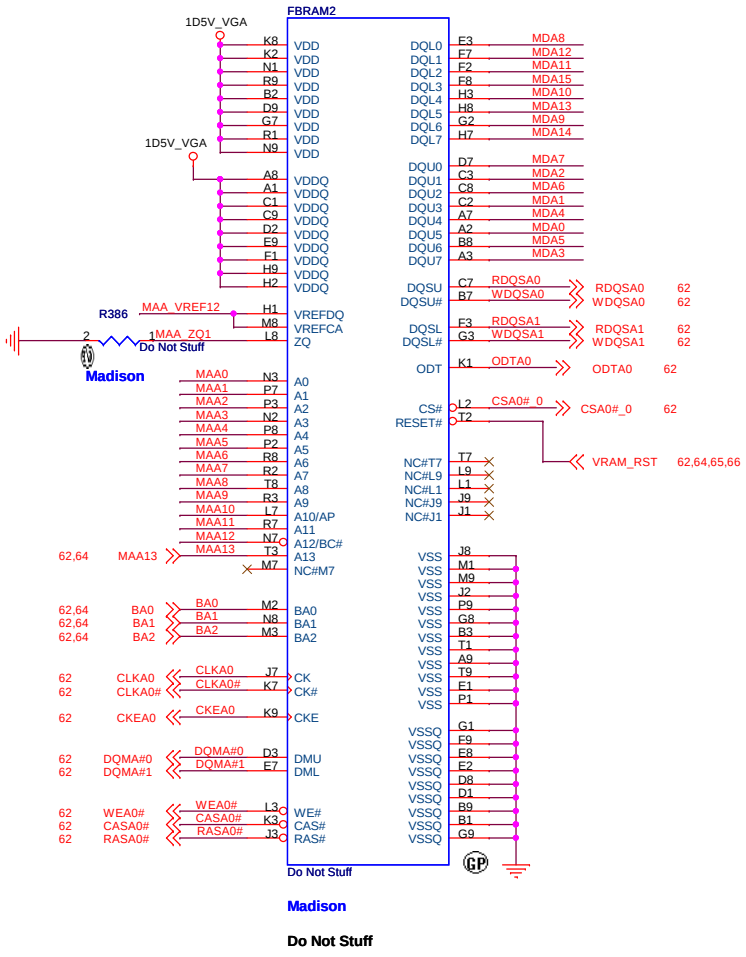
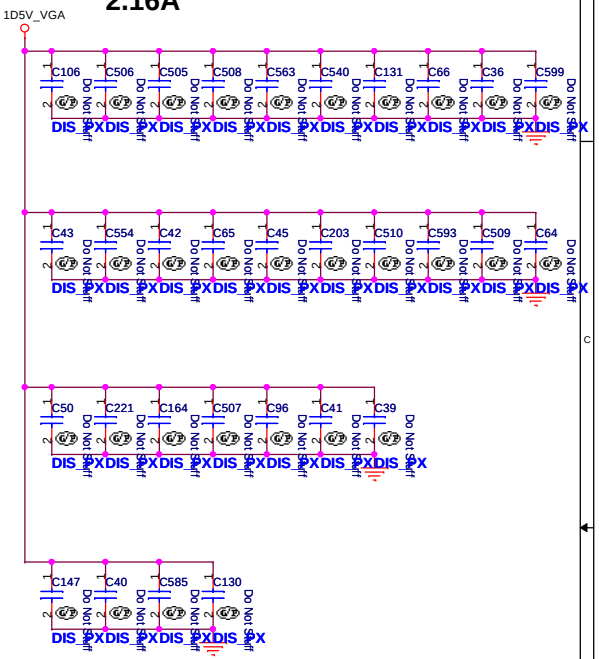
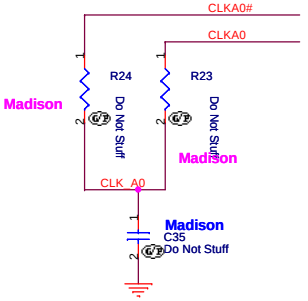
DDR3









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HYNIX: 72.51G63.C0U

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62,64 RDQSA[0..7]
62,64 WDQSA[0..7]
62,64 MAA[0..12] MAA[0..12]
62,64 MDA[0..63] MDA[0..63]

Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM(1/4)

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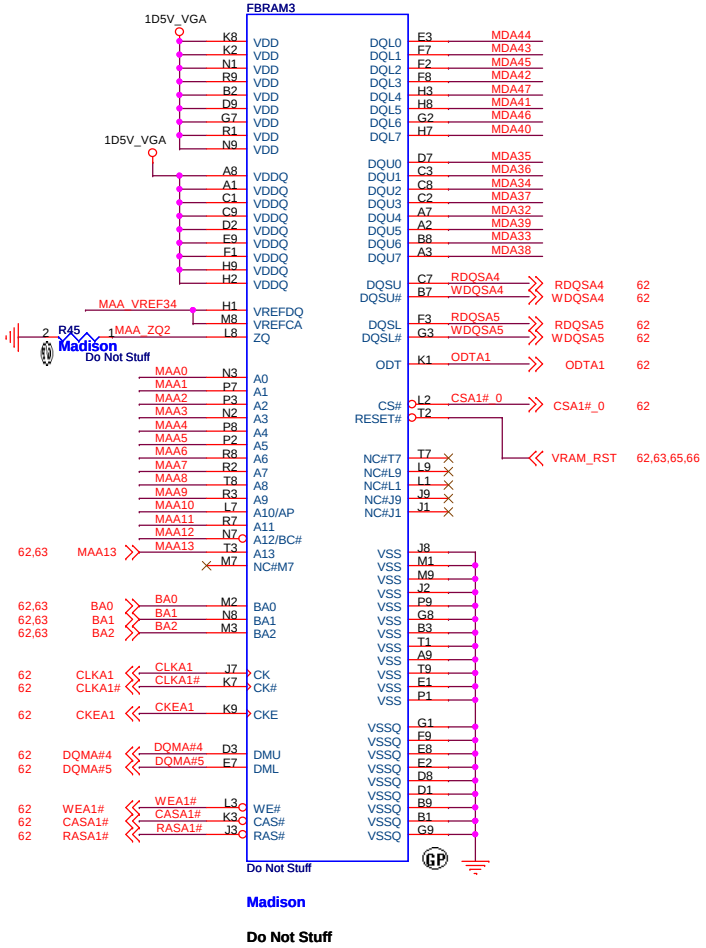
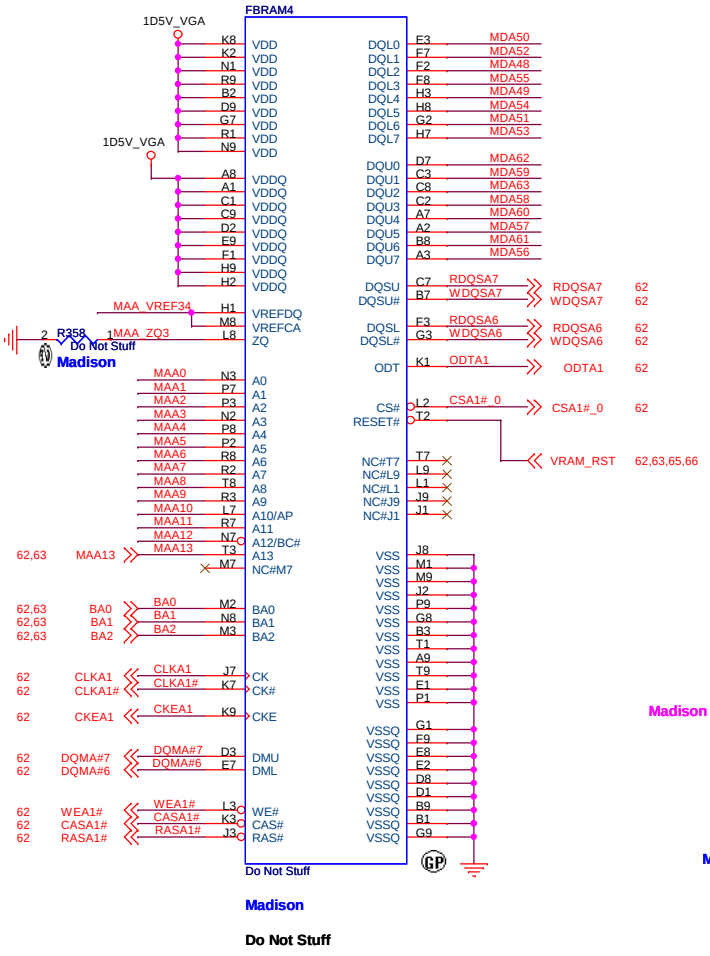
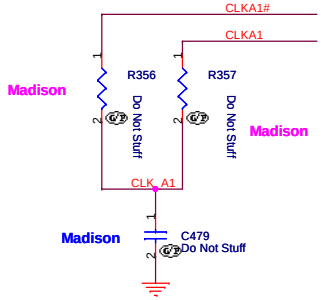
DDR3







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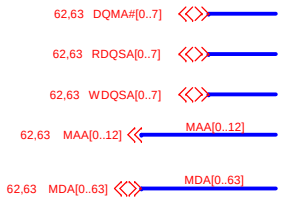

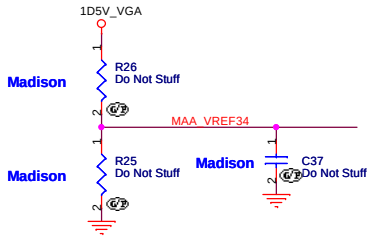

Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(2/4)***	
Size A3	Document Number **JE70-CP**	Rev **-1M**
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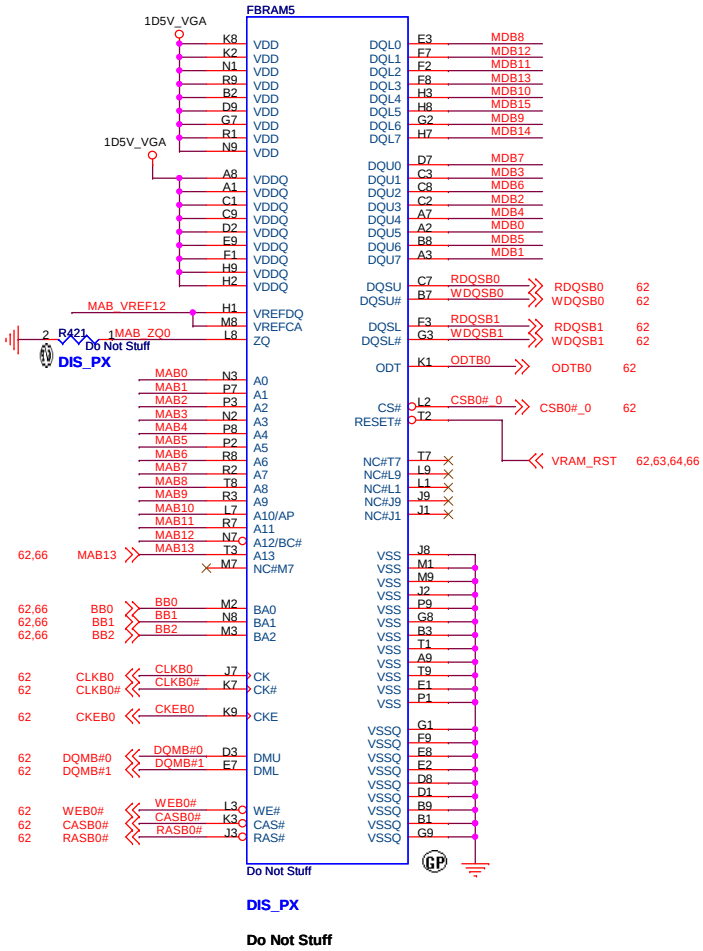
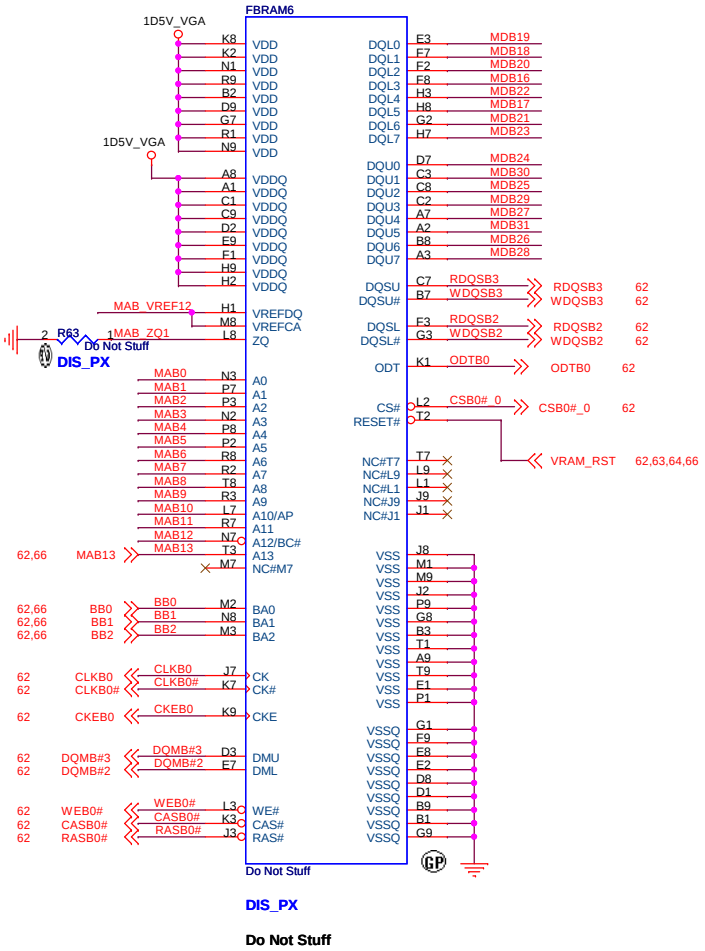
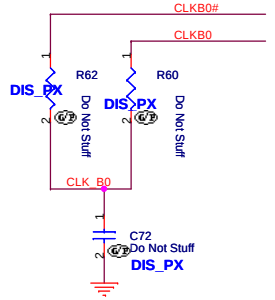
DDR3







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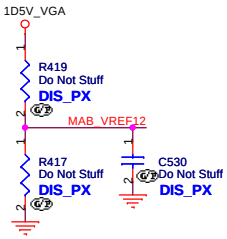

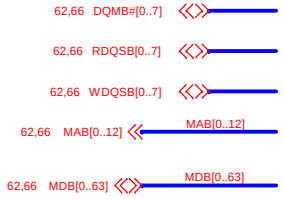

Pre UMA

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM(3/4)***

Size	Document Number	Rev
A3	JE70-CP	-1M

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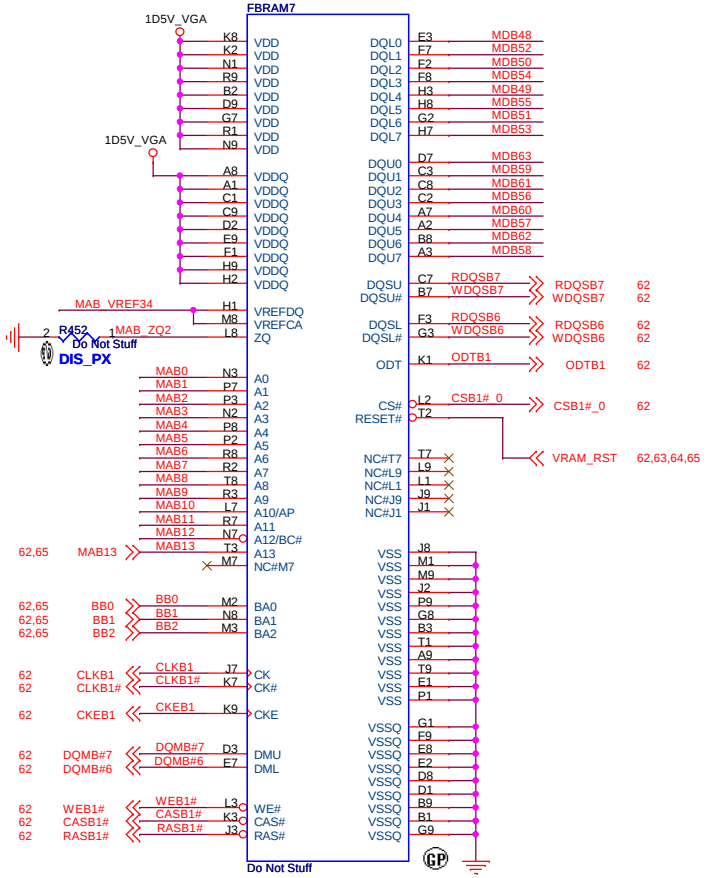
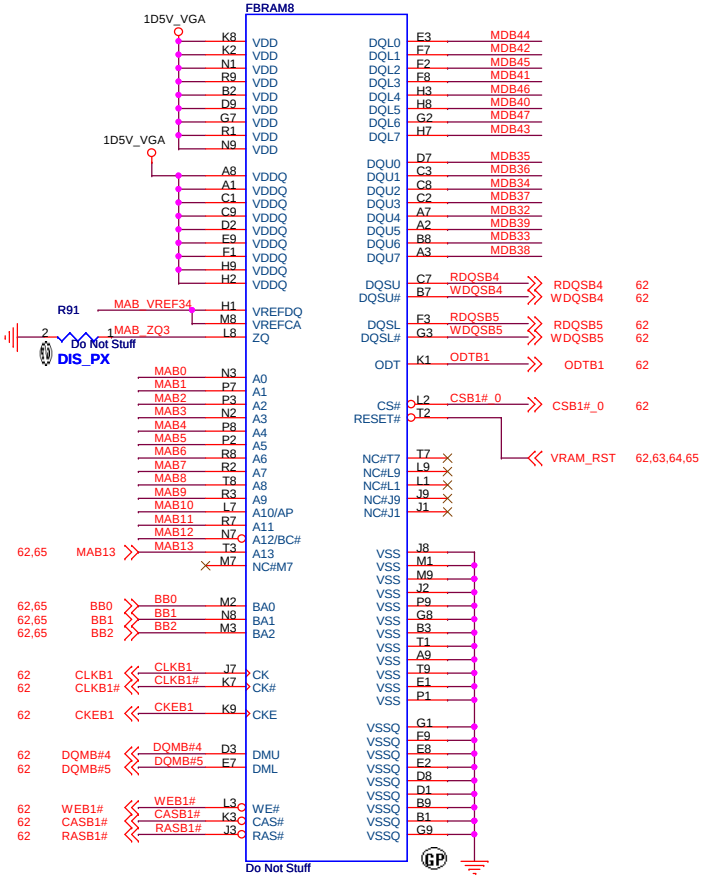
DDR3





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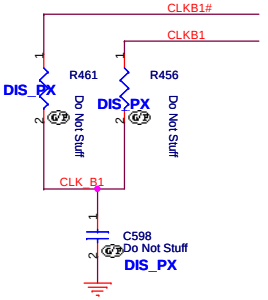
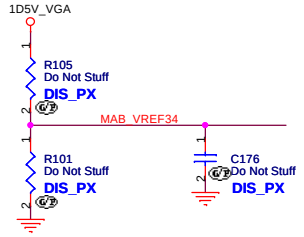
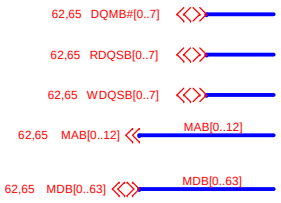
HYNIX: 72.51G63.C0U







Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM(4/4)		
Size: A3	Document Number: JE70-CP	Rev: -1M
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Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Modify History

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