

Compal Confidential

EA50_HWS M/B Schematics Document

Intel Shark Bay SV (Haswell+ Lynx point)

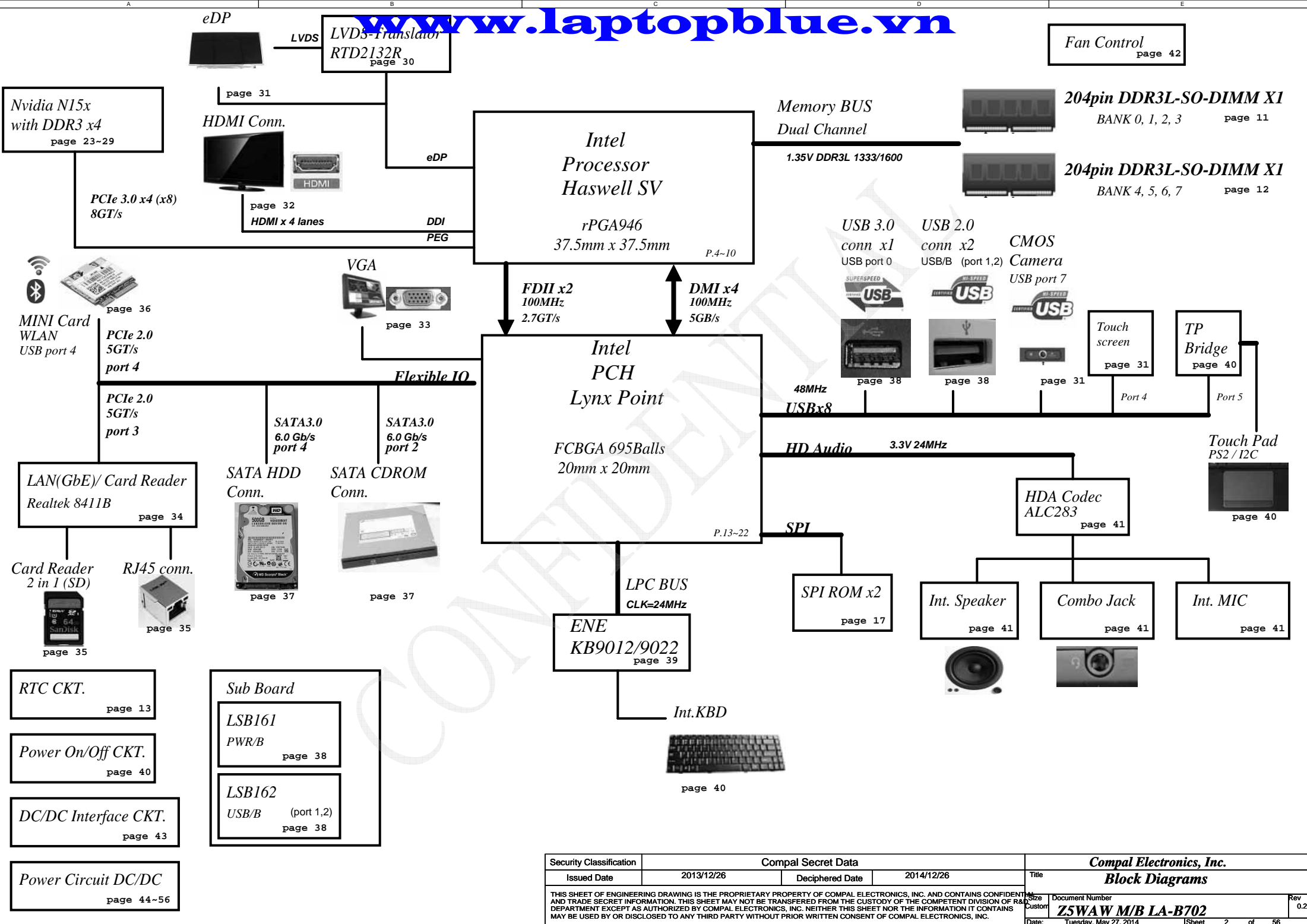
Nvidia N15S-GT / N15V-GM

2014-05-27

REV:1.0

DAX	
Part Number	Description
DAZ17F00100	PCB Z5WAW LA-B702P LS-B161P/B162P

Security Classification		Compal Secret Data		Title	
Issued Date	2013/12/26	Deciphered Date	2014/12/26	Compal Electronics, Inc.	
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				Custom	Z5WAW M/B LA-B702
				Date:	Tuesday, May 27, 2014
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				Rev	0.2



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.675VS	+0.675VS power rail for DDR3L terminator	ON	OFF	OFF
+1.05VS	+1.05V power rail for CPU	ON	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+1.5VSDGPU	+1.5VSDGPU power rail for GPU	ON	OFF	OFF
+1.5VS	+1.5V power rail for CPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X	On Board Thermal Sensor	0100 110x
		VGA Internal Thermal Sensor	0100 000x

EC SM Bus2 address

PCH SM Bus address

Device	Address	
ChannelA DIMM0	1010 0000	JDIMM1
ChannelB DIMM1	1010 0010	JDIMM2

USB Port Table

USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port(Left 3.0)
	1	USB Port(Right 2.0)
	2	USB Port(Right 2.0)
	3	Finger Printer
	4	Touch Screen
	5	USB/I2C Bridge
	6	WLAN
	7	Webcam
USB 3.0	Port	
XHCI	0	USB Port(Left 3.0)
	1	
	2	
	3	

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Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD
0	0	0 V	0 V	0 V	0x00-0x0B
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C-0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D-0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27-0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31-0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C-0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47-0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55-0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65-0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77-0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88-0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97-0xA3
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA4-0xAD
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xAE-0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8-0xC0
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC1-0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA-0xD3
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD4-0xDC
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDD-0xE6
19	NC	3.000 V	3.300 V		0xE7-0xFF

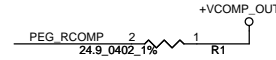
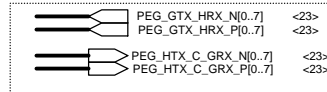
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	-
3	0.3
4	1.0
5	
6	
7	

BTO Option Table

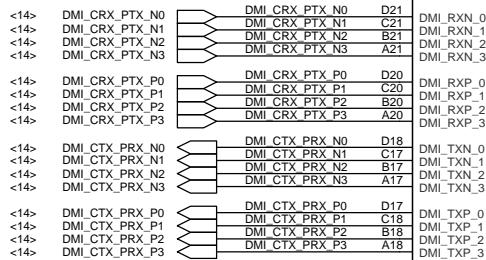
BTO Item	BOM Structure
Unpop	@
Connector	CONN@
EC 9022	9022@
EC 9012	9012@
UMA Component	UMAO@
GPU	VGA@
EDP panel	EDP@
eDP to LVDS	LVDS@
EMC Component	EMC@
EMC Reserve	XEMC@
DGPU_IDEN	VGM®, SGT®
VGM-820M;SGT-840M	
GC6 2.0	GC6@
non GC6	NGC6@
VRAM Selection	X76@
Digital MIC	1Dmic@/2Dmic@
USB/I2C BRI	TPBRI@
Touch Screen	TS@

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Note:
Trace width=12 mils ,Spacing=15mils
Max length= 400 mils.

Haswell rPGA EDS
JCPU1A



Design Guide show:
have to routed

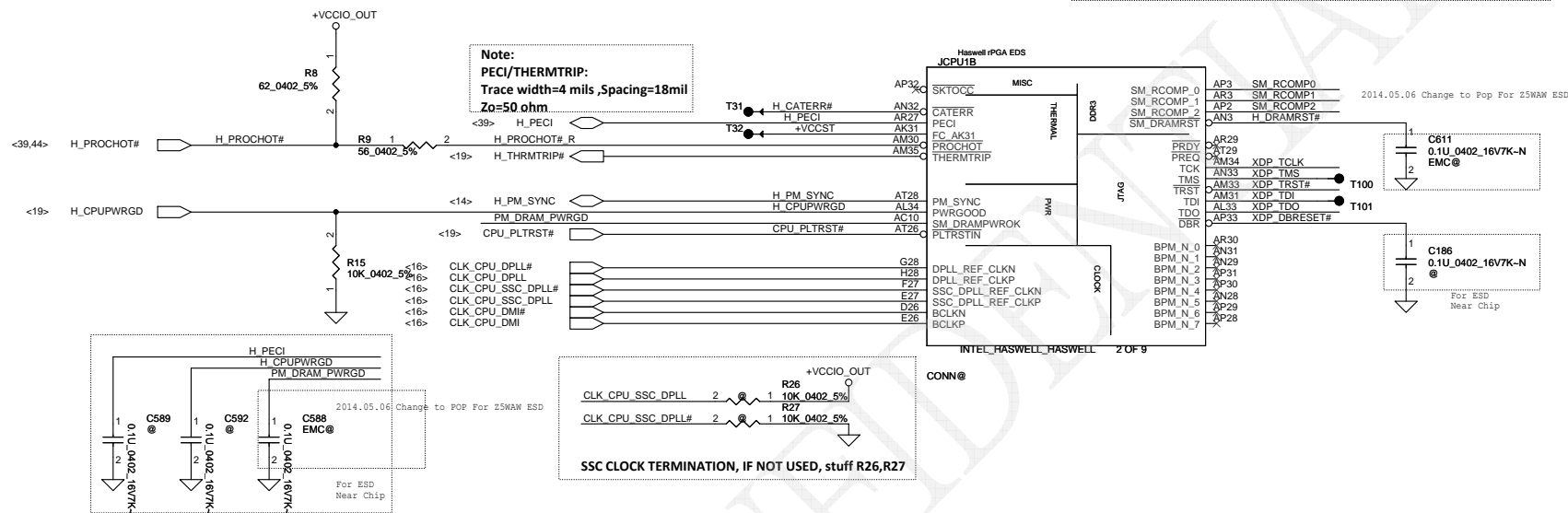
FDI_CSXN
DISP_INT

PEG_RCOMP		E23 PEG_RCOMP	
PEG_RXN_0	M29	PEG_RXN_0	M29
PEG_RXN_1	K28	PEG_RXN_1	K28
PEG_RXN_2	M31	PEG_RXN_2	M31
PEG_RXN_3	L30	PEG_RXN_3	L30
PEG_RXN_4	M33	PEG_RXN_4	M33
PEG_RXN_5	L32	PEG_RXN_5	L32
PEG_RXN_6	M35	PEG_RXN_6	M35
PEG_RXN_7	L34	PEG_RXN_7	L34
PEG_RXN_8	E29	PEG_RXN_8	E29
PEG_RXN_9	D28	PEG_RXN_9	D28
PEG_RXN_10	E31	PEG_RXN_10	E31
PEG_RXN_11	D30	PEG_RXN_11	D30
PEG_RXN_12	E35	PEG_RXN_12	E35
PEG_RXN_13	D34	PEG_RXN_13	D34
PEG_RXN_14	E33	PEG_RXN_14	E33
PEG_RXN_15	D32	PEG_RXN_15	D32
PEG_RXP_0	L29	PEG_RXP_0	L29
PEG_RXP_1	L28	PEG_RXP_1	L28
PEG_RXP_2	L31	PEG_RXP_2	L31
PEG_RXP_3	K30	PEG_RXP_3	K30
PEG_RXP_4	L33	PEG_RXP_4	L33
PEG_RXP_5	K32	PEG_RXP_5	K32
PEG_RXP_6	L35	PEG_RXP_6	L35
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PEG_RXP_10	E30	PEG_RXP_10	E30
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PEG_RXP_12	E34	PEG_RXP_12	E34
PEG_RXP_13	F33	PEG_RXP_13	F33
PEG_RXP_14	D32	PEG_RXP_14	D32
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PEG_TXN_11	A26	PEG_TXN_11	A26
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PEG_TXN_13	A24	PEG_TXN_13	A24
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PEG_TXP_13	B24	PEG_TXP_13	B24
PEG_TXP_14	C23	PEG_TXP_14	C23
PEG_TXP_15	B22	PEG_TXP_15	B22

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Issued Date	2013/12/26	Deciphered Date	2014/12/26	Process	PROCESSOR(1/7) DMI,FDI,PEG
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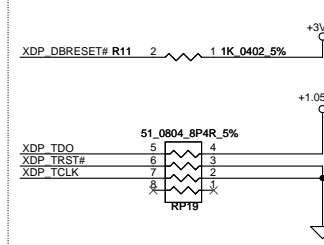


DDR3 COMPENSATION SIGNALS

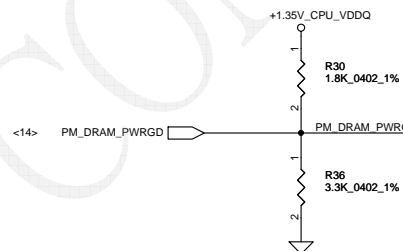
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SM_RCOMP1R6	1	2	75_0402_1%
SM_RCOMP2R7	1	2	100_0402_1%

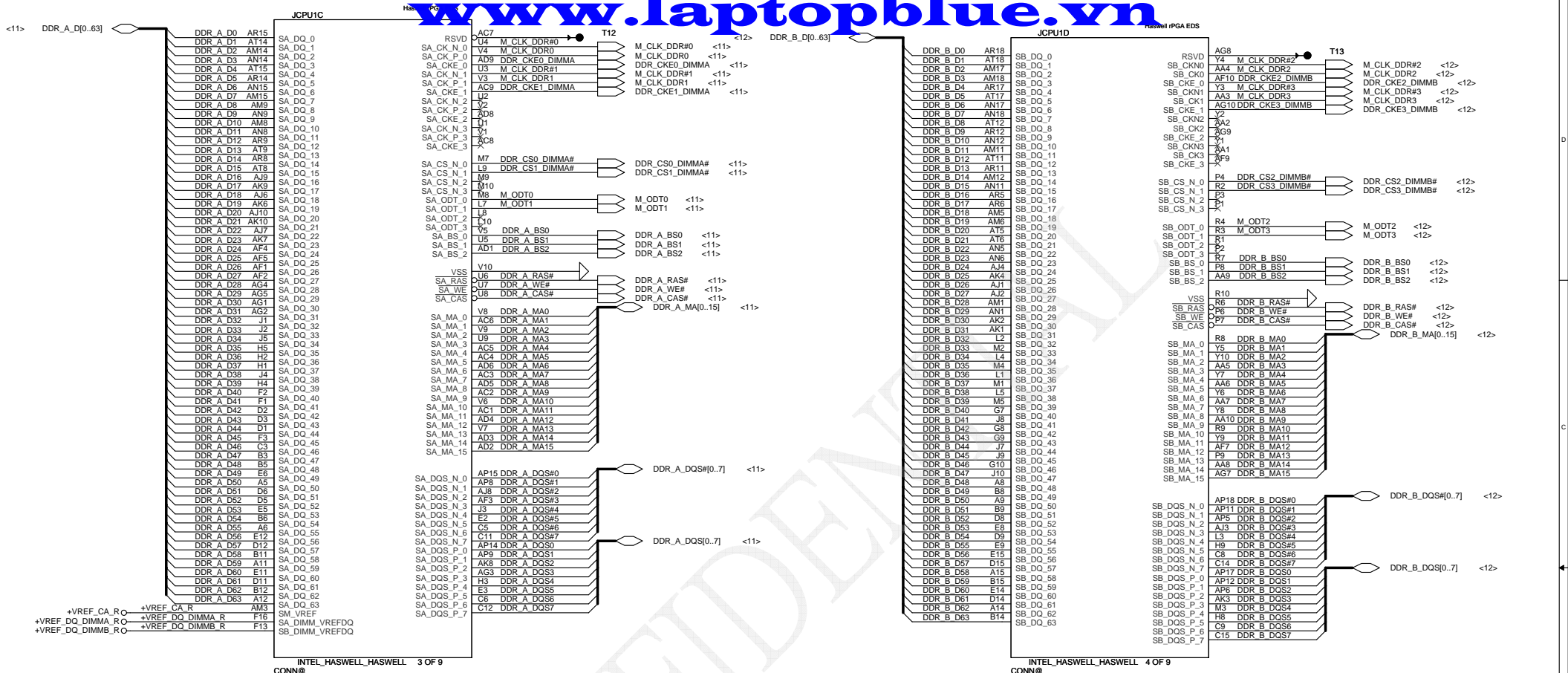
Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mils

PU/PD for JTAG signals



SM_DRAMPWROK with DDR Power Gating Topology





HDMI D2
HDMI D1
HDMI D0
HDMI CLK

HDMI

<32> HDMI_TX2-
<32> HDMI_TX2+
<32> HDMI_TX1-
<32> HDMI_TX1+
<32> HDMI_TX0-
<32> HDMI_TX0+
<32> HDMI_CLK-
<32> HDMI_CLK+

HDMI_TX2- 0.1U 0402 16V7K 1
HDMI_TX2+ 0.1U 0402 16V7K 1
HDMI_TX1- 0.1U 0402 16V7K 1
HDMI_TX1+ 0.1U 0402 16V7K 1
HDMI_TX0- 0.1U 0402 16V7K 1
HDMI_TX0+ 0.1U 0402 16V7K 1
HDMI_CLK- 0.1U 0402 16V7K 1
HDMI_CLK+ 0.1U 0402 16V7K 1

2 C410 CPU DP2_N0 T28
2 C400 CPU DP2_P0 U28
2 C395 CPU DP2_N1 T30
2 C409 CPU DP2_P1 U30
2 C408 CPU DP2_N2 U29
2 C406 CPU DP2_P2 V29
2 C412 CPU DP2_N3 U31
2 C411 GPU DP2_P3 V31

Haswell iPGA EDS

JCPU1H

EDP_AUXN
EDP_AUXP
EDP_HPDI
EDP_RCOMP
EDP_DISP_UT IL

M27
N27
P27
E24
R27

EDP_AUXN <31>
EDP_AUXP <31>
EDP_HPDI <31>
EDP_RCOMP <31>
EDP_DISP_UT IL <31>

EDP_TXN_0
EDP_TXP_0
EDP_TXN_1
EDP_TXP_1
FDI_TXN_0
FDI_TXP_0
FDI_TXN_1
FDI_TXP_1

P35
R35
N34
P34
P33
R33
N32
P32

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EDP_TXN1 <31>
EDP_TXP1 <31>
FDI_CTX_PRX_N0 <14>
FDI_CTX_PRX_P0 <14>
FDI_CTX_PRX_N1 <14>
FDI_CTX_PRX_P1 <14>

DDI_TXCN_0
DDI_TXCP_0
DDI_TXCN_1
DDI_TXCP_1
DDI_TXCN_2
DDI_TXCP_2
DDI_TXCN_3
DDI_TXCP_3

DDI_TXDN_0
DDI_TXDP_0
DDI_TXDN_1
DDI_TXDP_1
DDI_TXDN_2
DDI_TXDP_2
DDI_TXDN_3
DDI_TXDP_3

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CONN@

COMPENSATION PU FOR eDP

Note:
Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

HPD INVERSION FOR EDP

HPD is a active high signal from device.
The HPD processor input is a low voltage
active signal.

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2014/12/26

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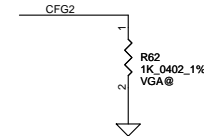
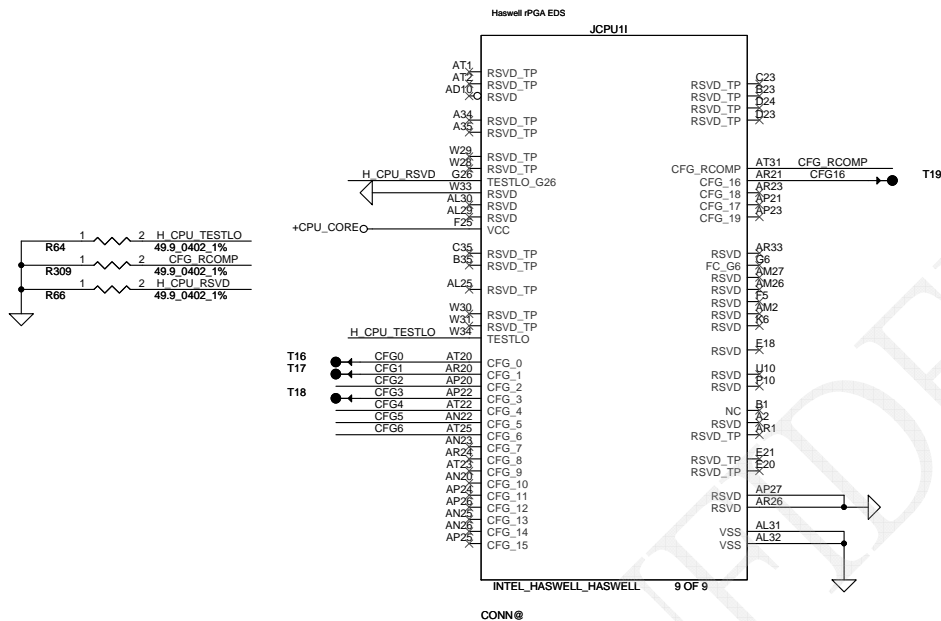
PROCESSOR(4/7) PM,XDP,CLK

ZSWAW M/B LA-B702

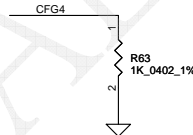
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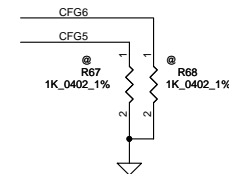
Rev 0.2



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



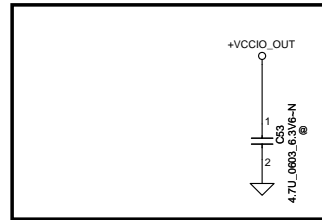
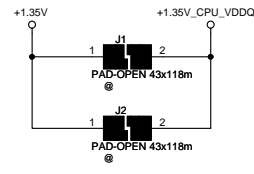
Embedded Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



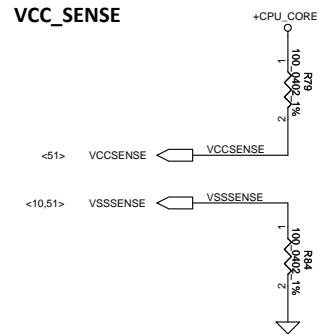
PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

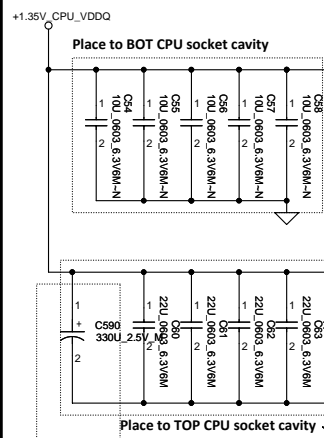
+1.35V_CPU_VDDQ Source



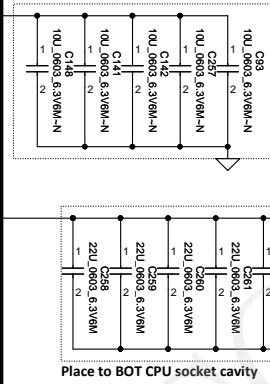
VDDQ MAX 2.1 A



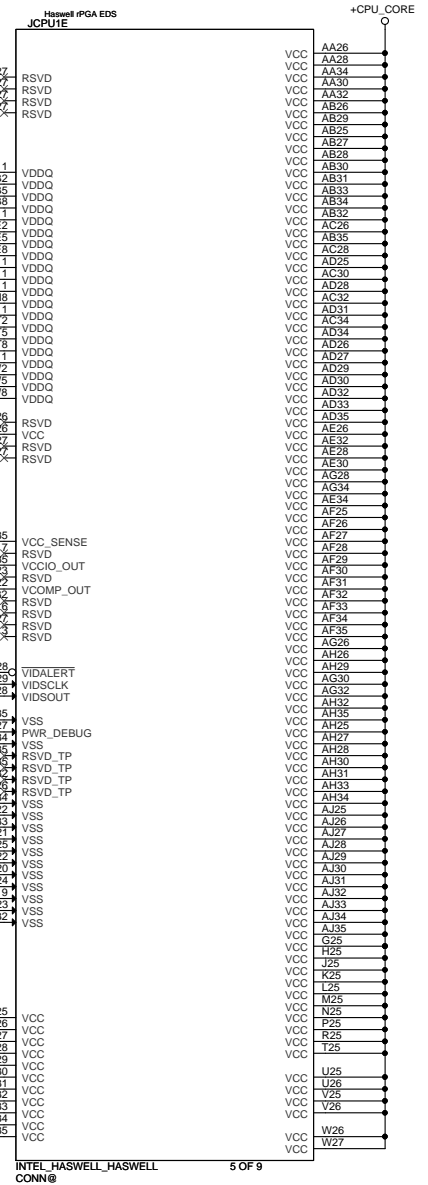
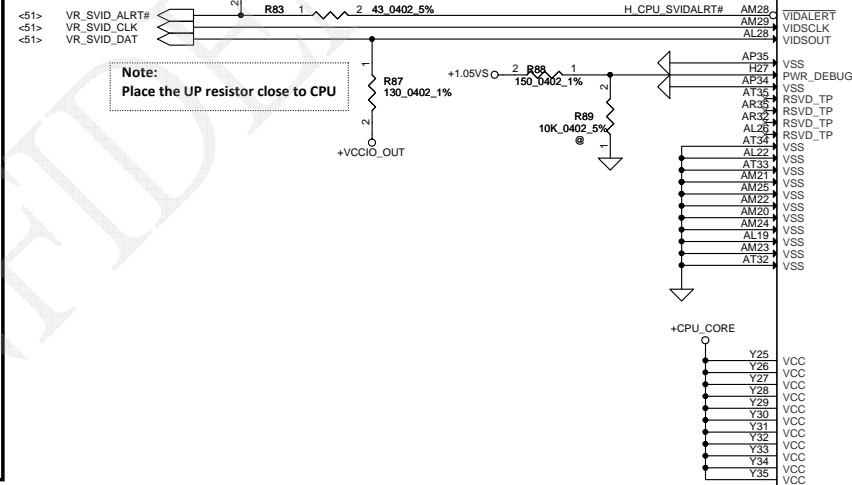
VDDQ DECOUPLING



Place to TOP CPU socket cavity

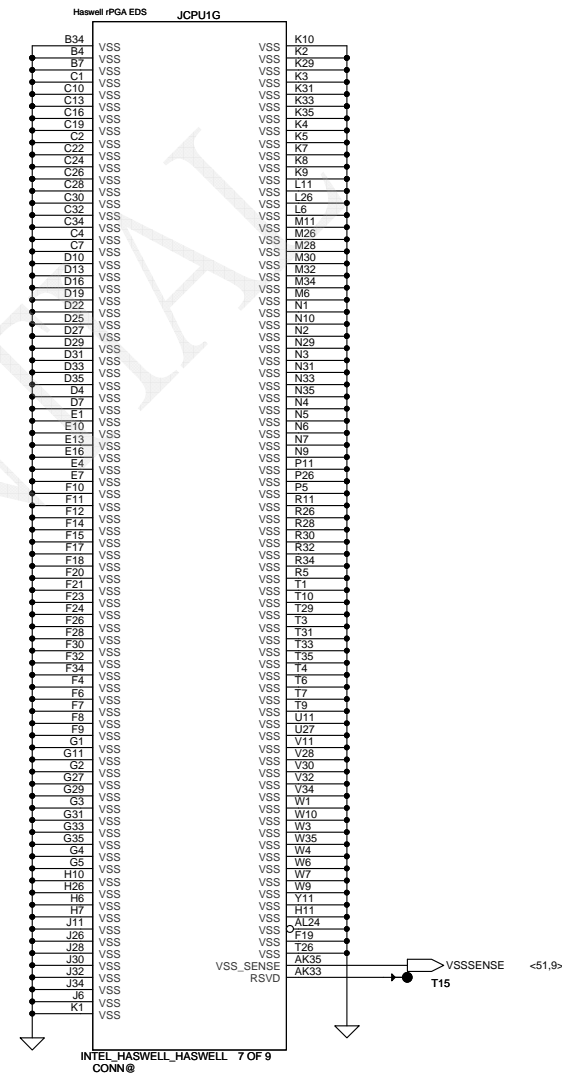
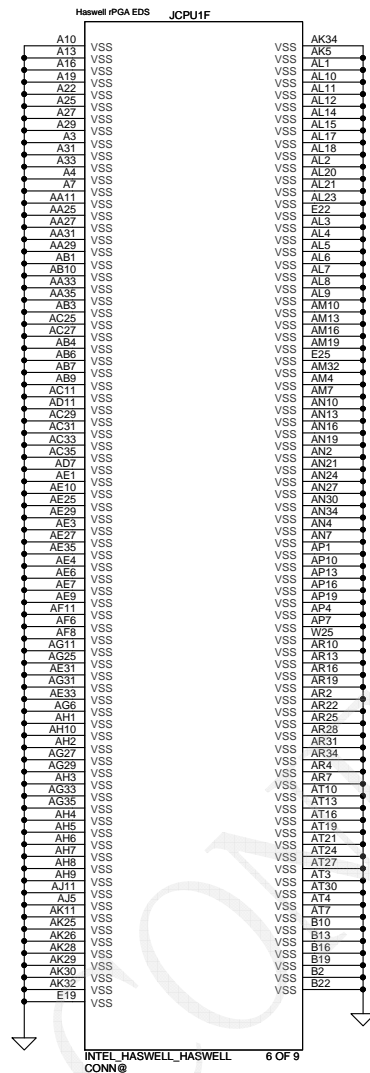


10u *10
22u*11
330u*1

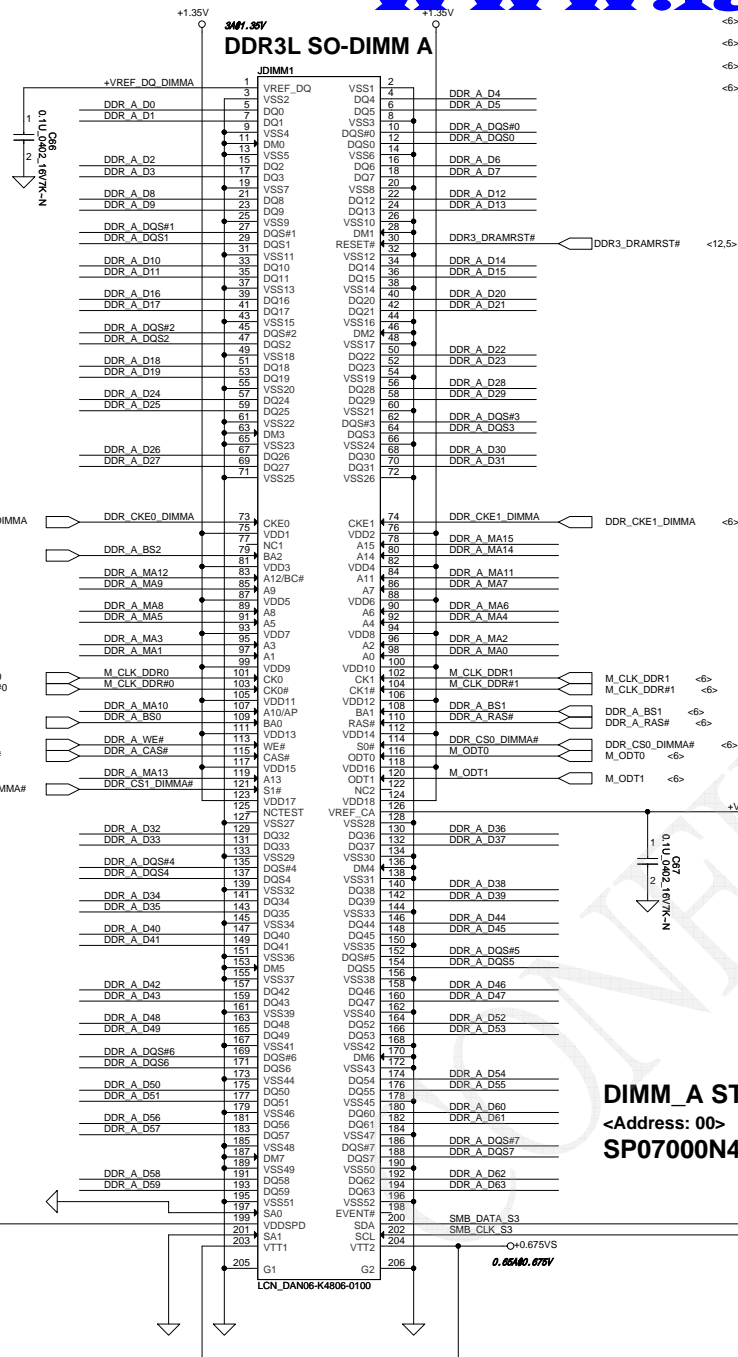


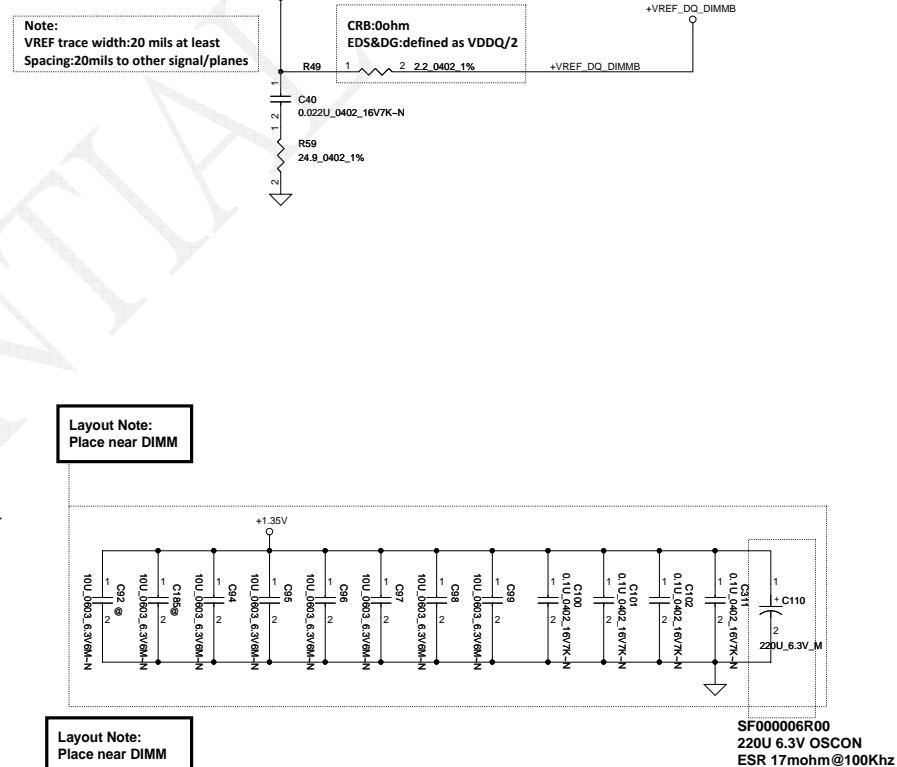
SF000006S00
330U 2.5V H4.2
17mohm OSCON

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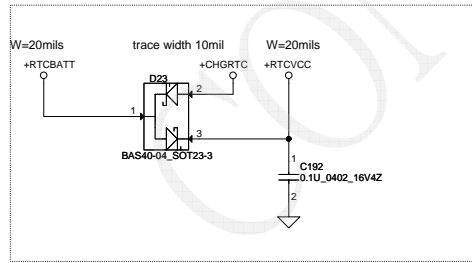
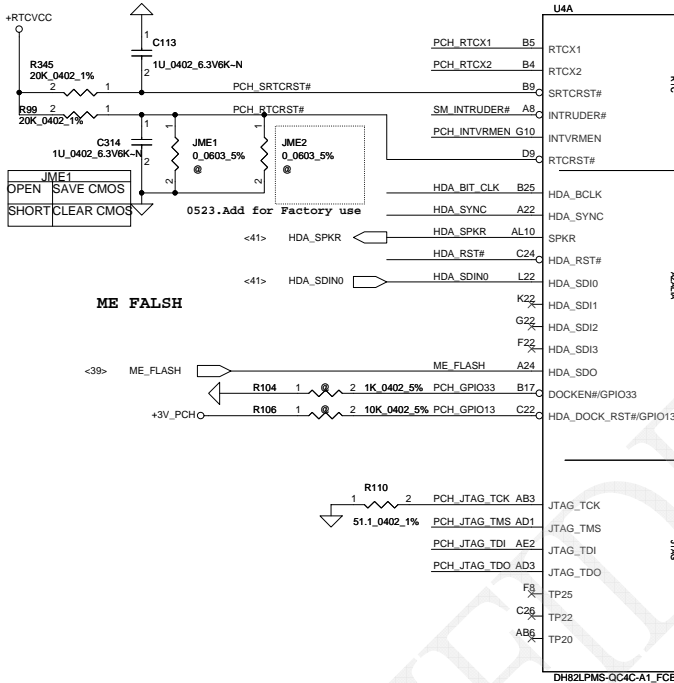
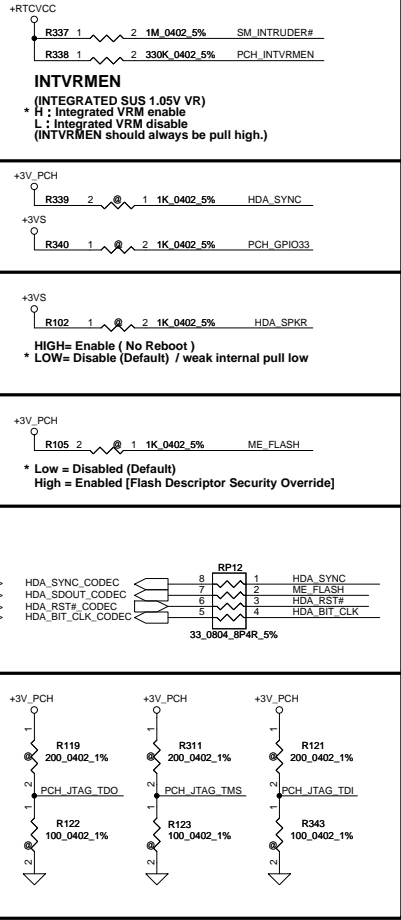
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				Date	Tuesday, May 27, 2014
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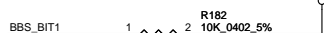
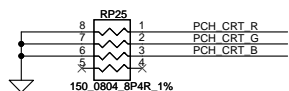


Note:
PCH_RTCX1/PCHRTCX2
Trace length <1000 mils

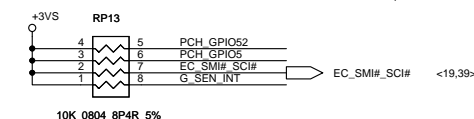
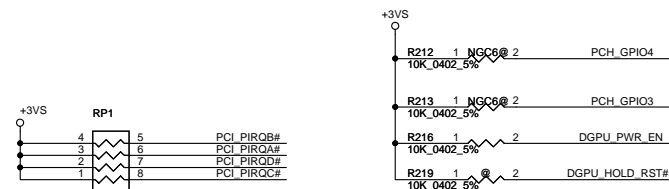
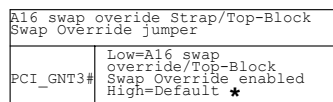
PL 10k at EC side



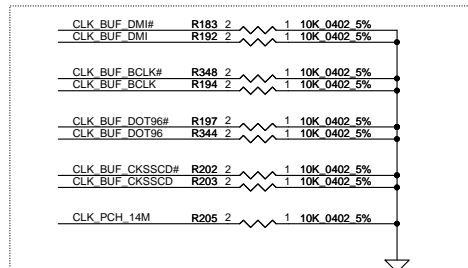
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Issued Date	2013/12/26	Deciphered Date	2014/12/26	Title	PCH (1/10) SATA,HDA,SPI, LPC, XDP
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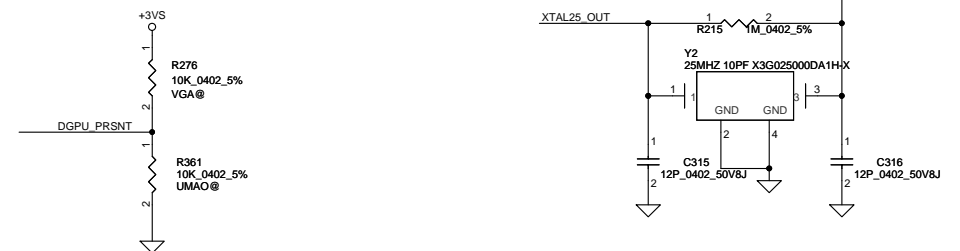
GPIO51 has internal pull up.



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					Docu- ment Number		Rev
					Z5WAW/M/B LA-B702		0.2
					Date: Tuesday, May 27, 2014		Sheet 15 of 56

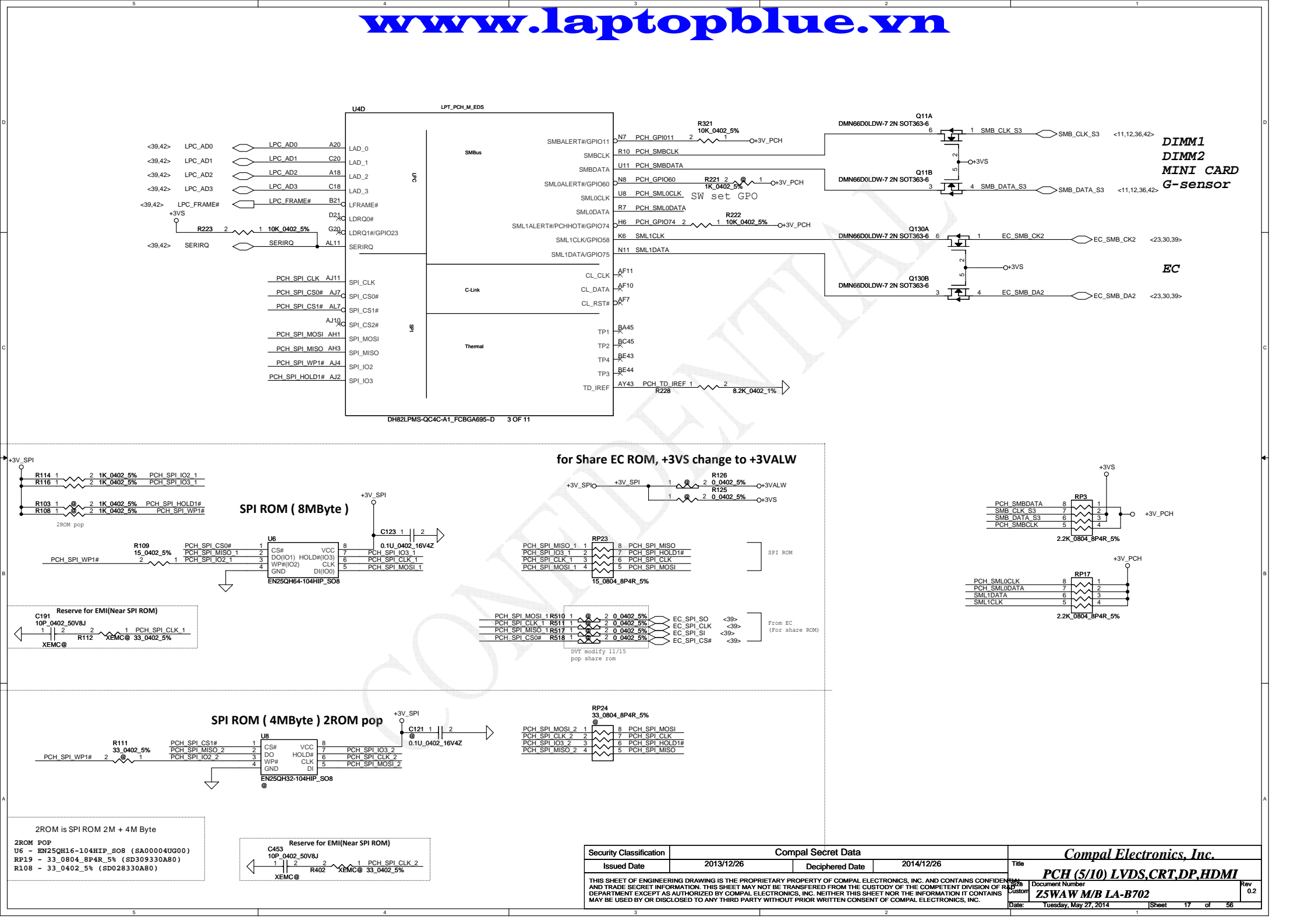
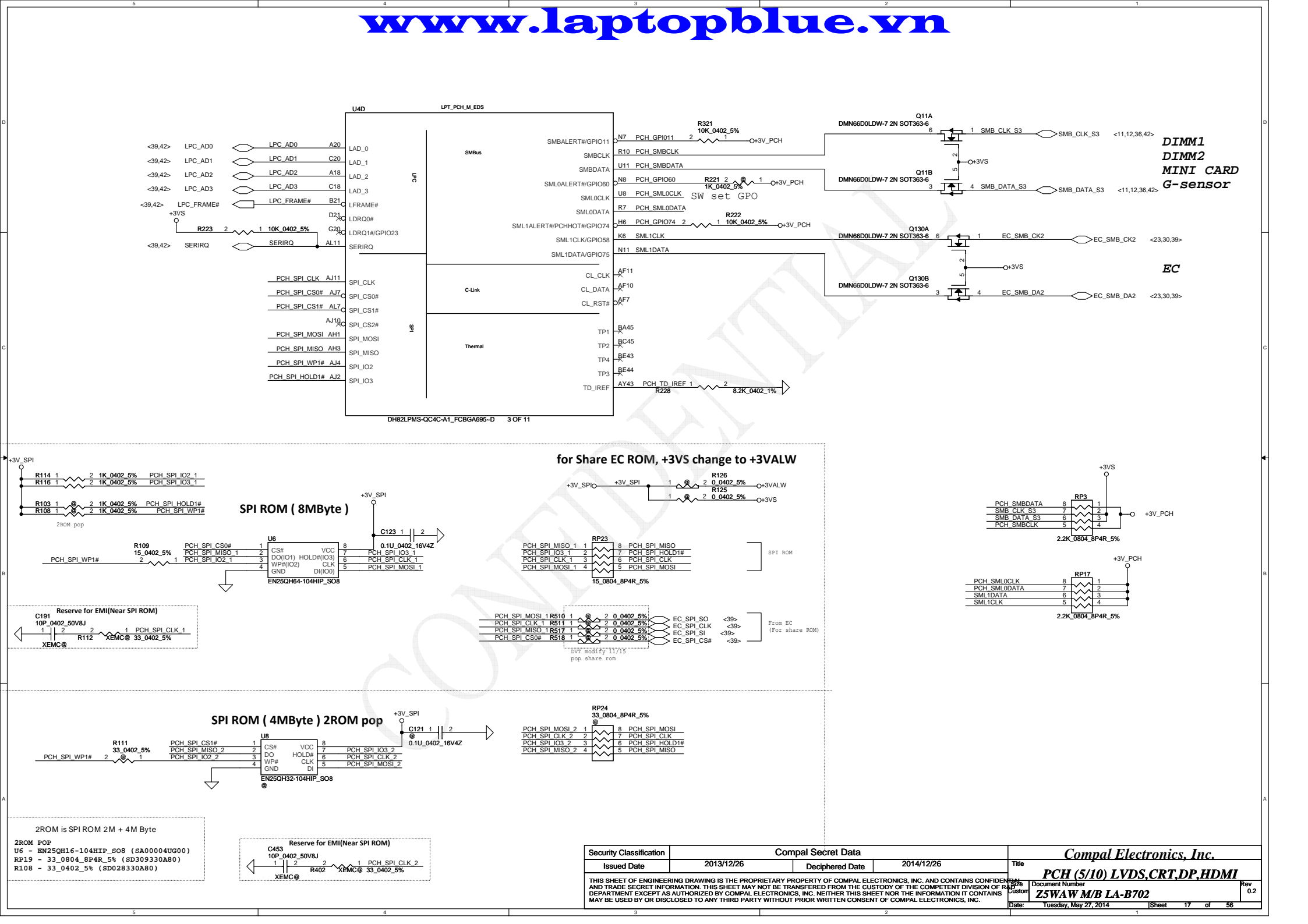
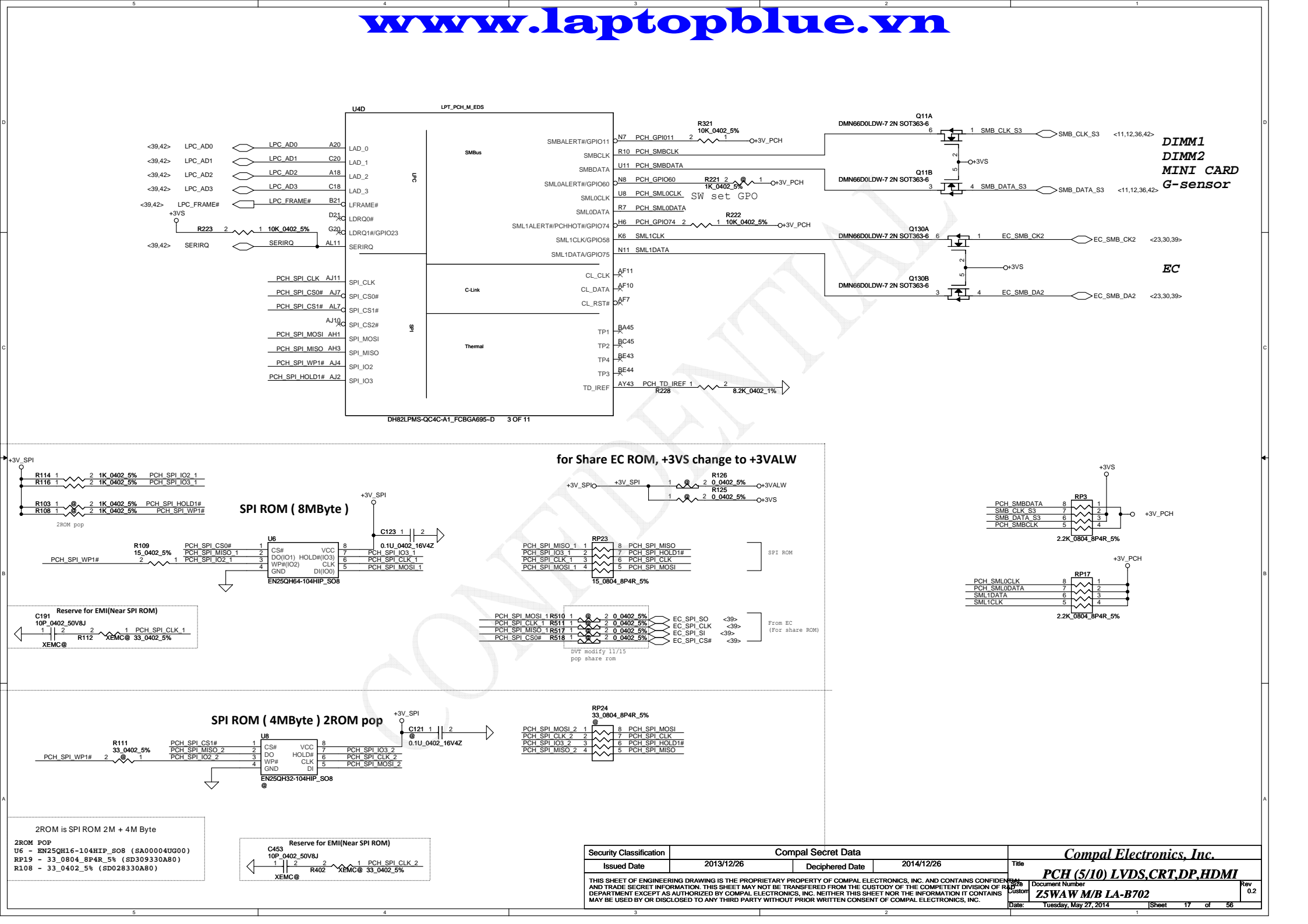
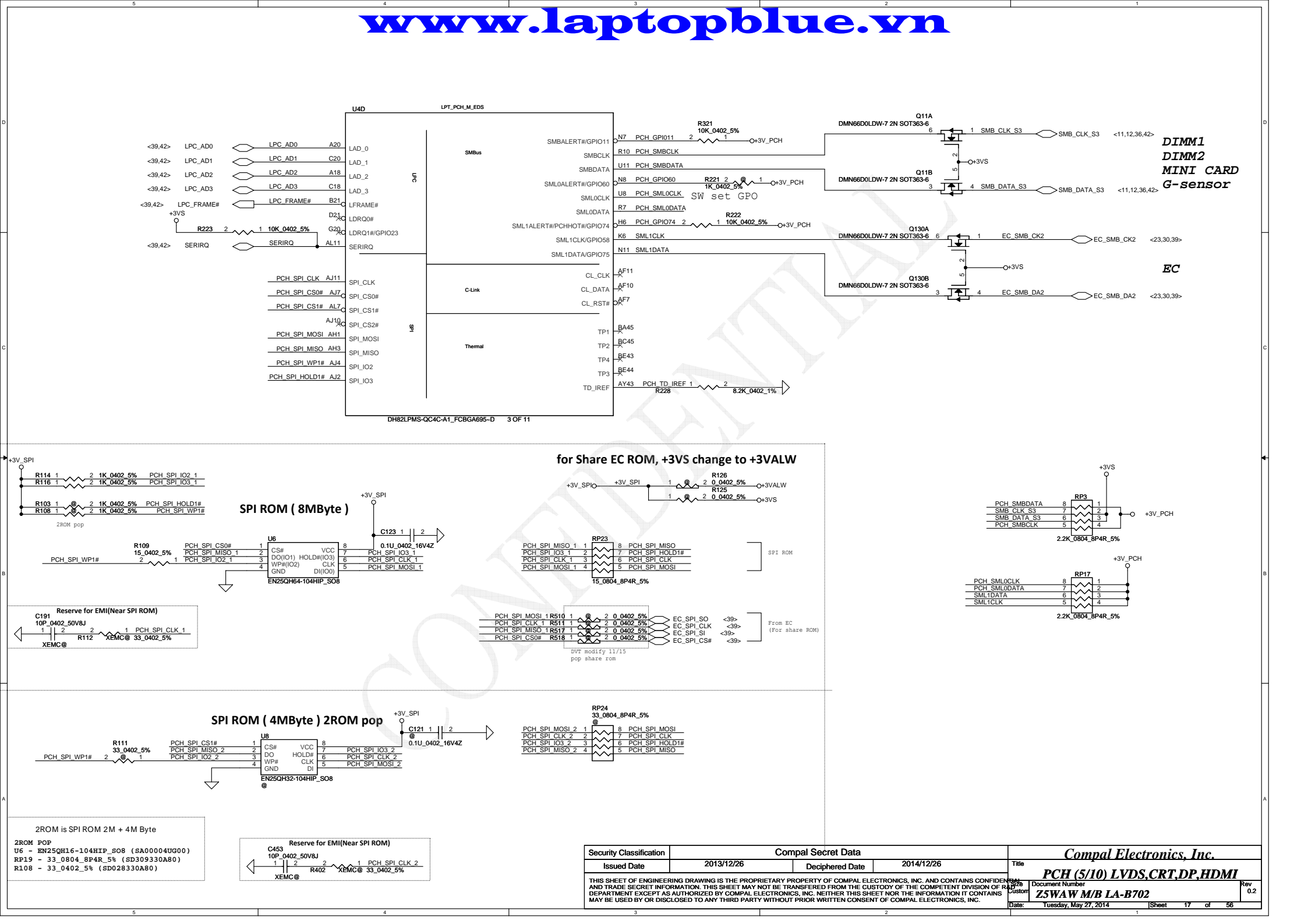


CLOCK TERMINATION for FCIM and need close to PCH



OGPU_PRSNT	Function
0	UMA
1	Optimus

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/12/26	Deciphered Date	2014/12/26	Title	PCH (4/10) DMI,FDI,PM,	
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U4D LPT_PCH_M_EDS

SMBus

C-Link

Thermal

for Share EC ROM, +3VS change to +3VALW

SPI ROM (8MByte)

SPI ROM (4MByte) 2ROM pop

2ROM is SPI ROM 2M + 4M Byte

Security Classification

Compal Secret Data

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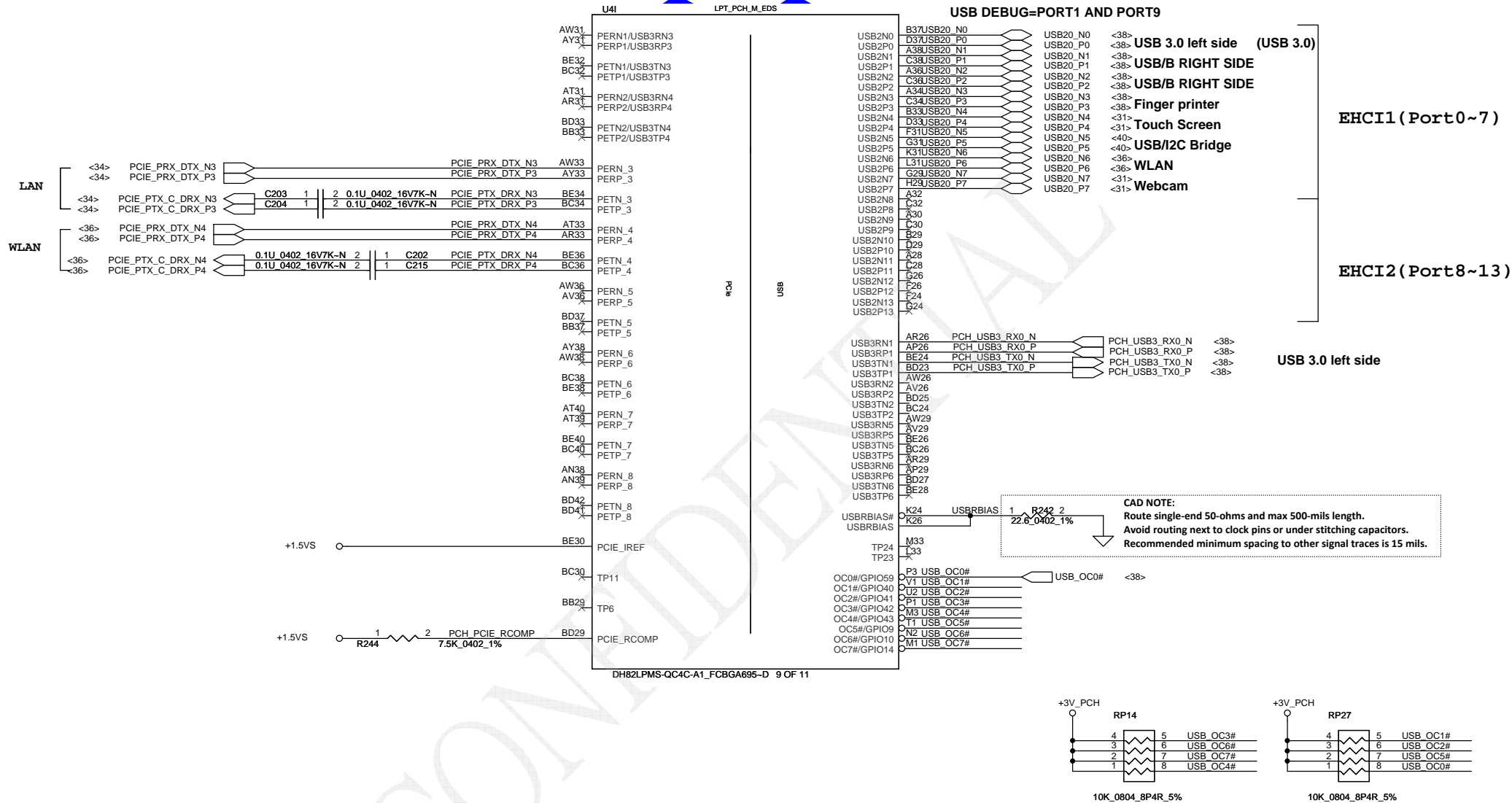
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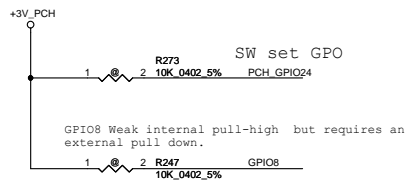
PCH (5/10) LVDS,CRT,DP,HDMI

ZSWAW M/B LA-B702

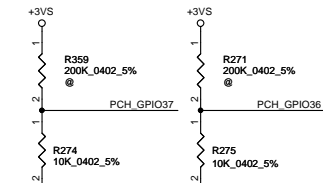
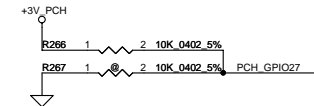
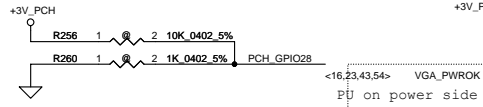
Rev 0.2

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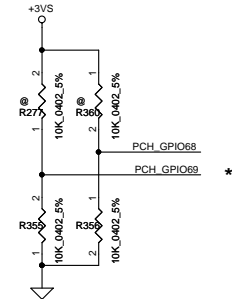




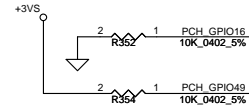
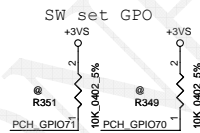
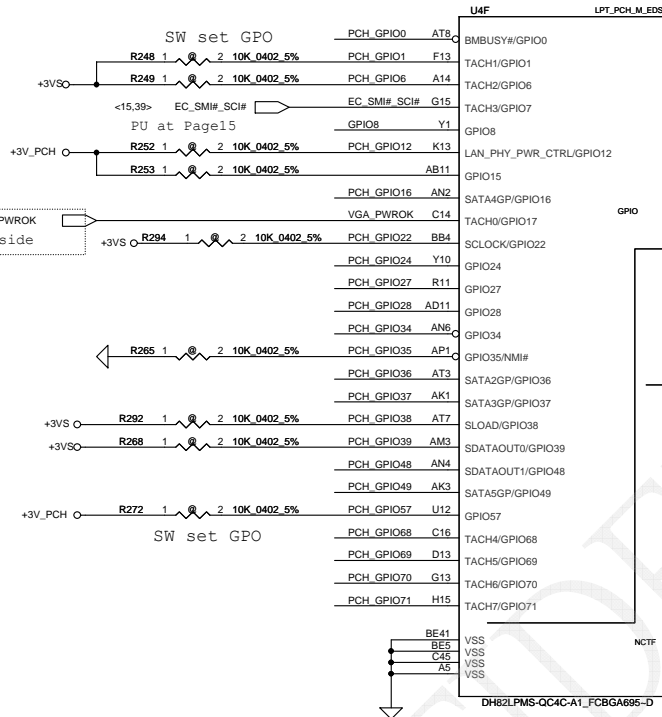
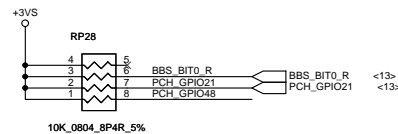
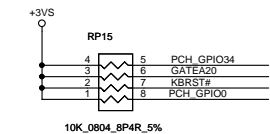
Remove strap description
inform SW set GPO



BIOS Request SKU ID



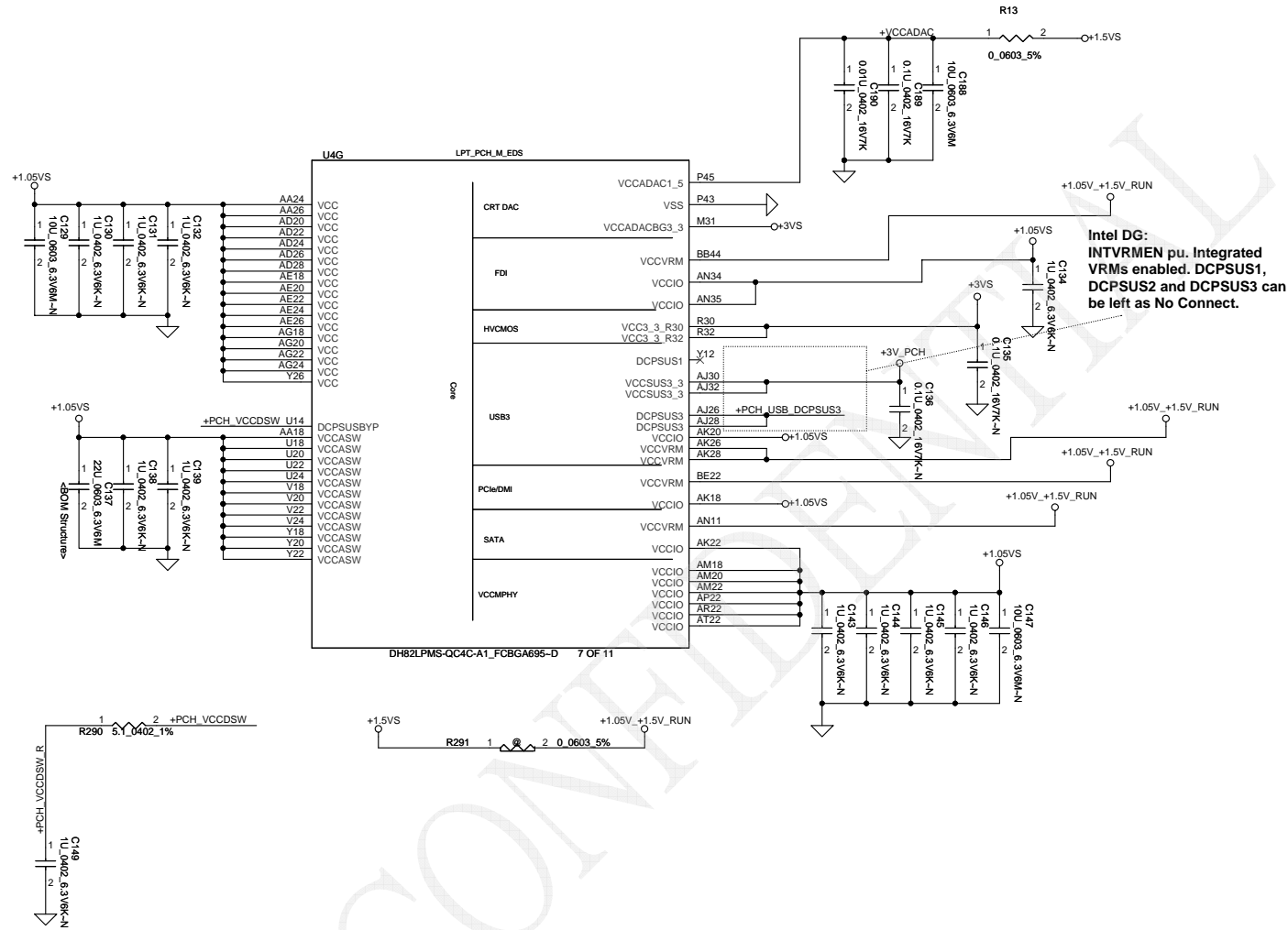
PCH_GPIO68	PCH_GPIO69	Function
0	0	Z5WAW
0	1	Reserved
1	0	Reserved
1	1	Reserved



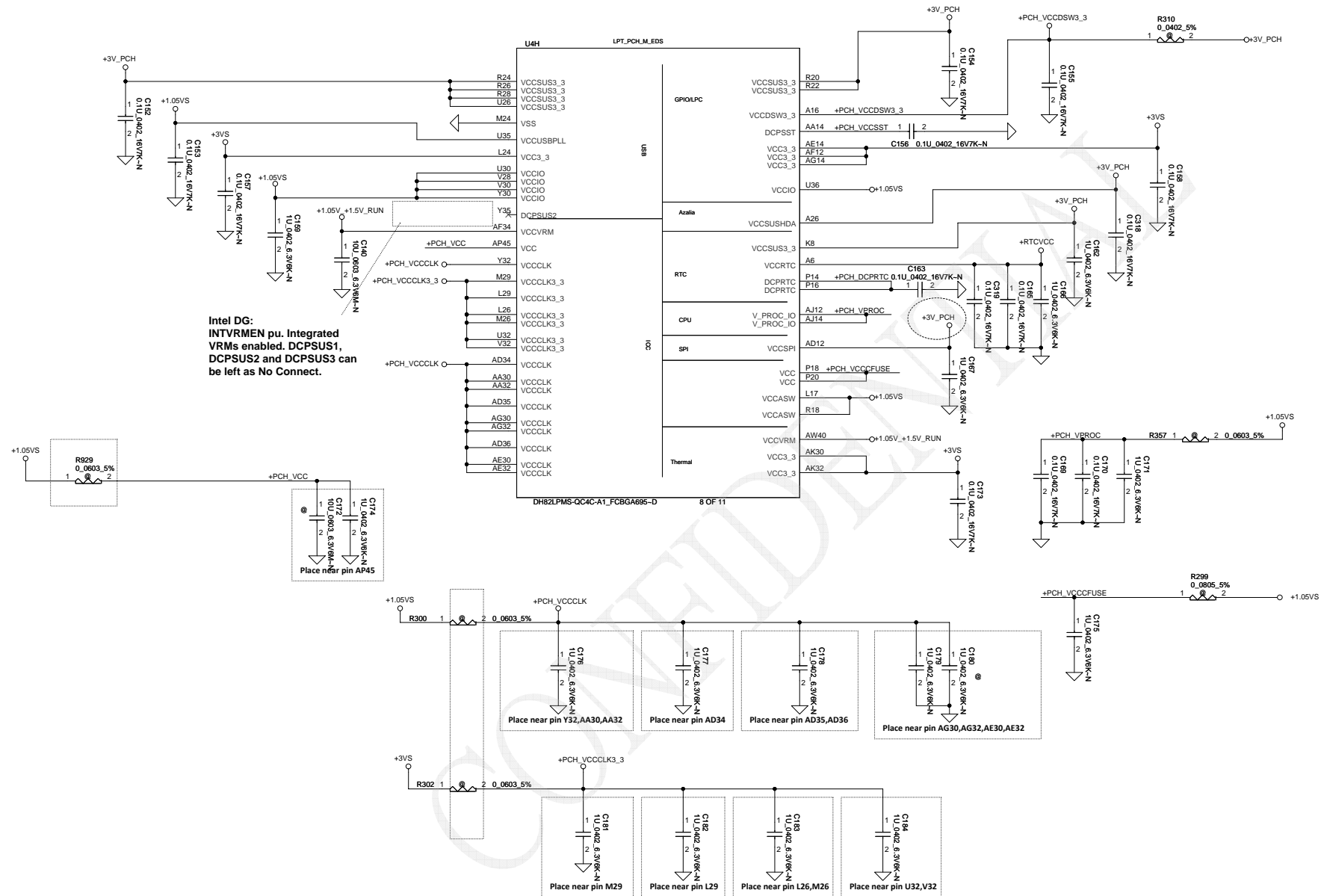
Config	GPIO16 & 49
USB3.0 x4, PCIE x8, SATA x6	11
USB3.0 x6, PCIE x8, SATA x4	01

Fixed Signals	Muxed Signals	Fixed Signals	Muxed Signals	Fixed Signals
USB3_1	USB3_2	PCIE_1	PCIE_2	SATA_1
USB3_3	USB3_4	PCIE_3	PCIE_4	SATA_2
USB3_5	USB3_6	PCIE_5	PCIE_6	SATA_3
USB3_7	USB3_8	PCIE_7	PCIE_8	SATA_4
USB3_9	USB3_10	PCIE_9	PCIE_10	SATA_5
USB3_11	USB3_12	PCIE_11	PCIE_12	SATA_6
USB3_13	USB3_14	PCIE_13	PCIE_14	SATA_7
USB3_15	USB3_16	PCIE_15	PCIE_16	SATA_8

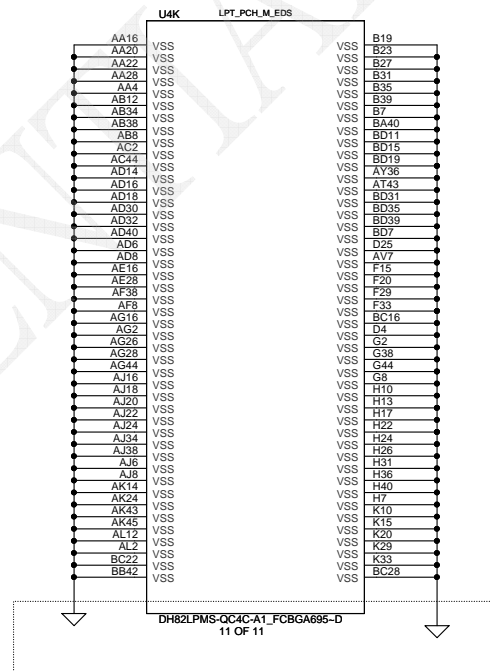
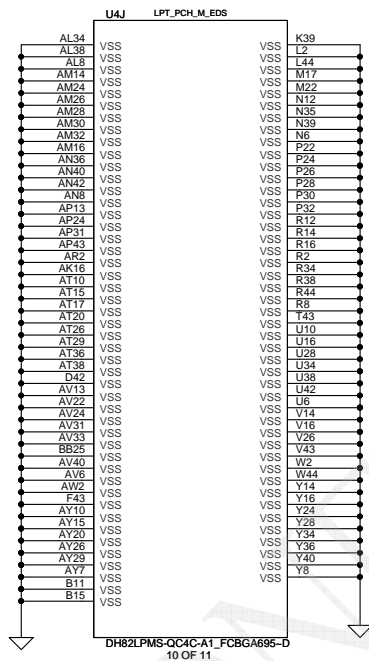
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								PCH (7/10) GPIO, CPU, MISC		
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PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

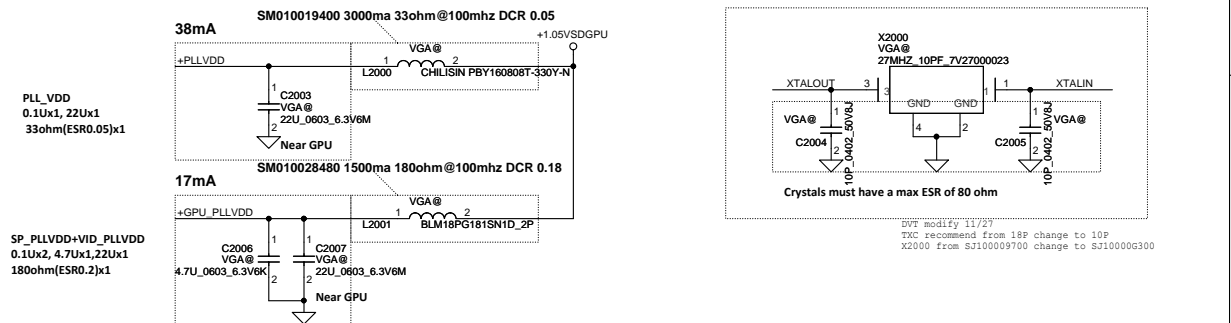
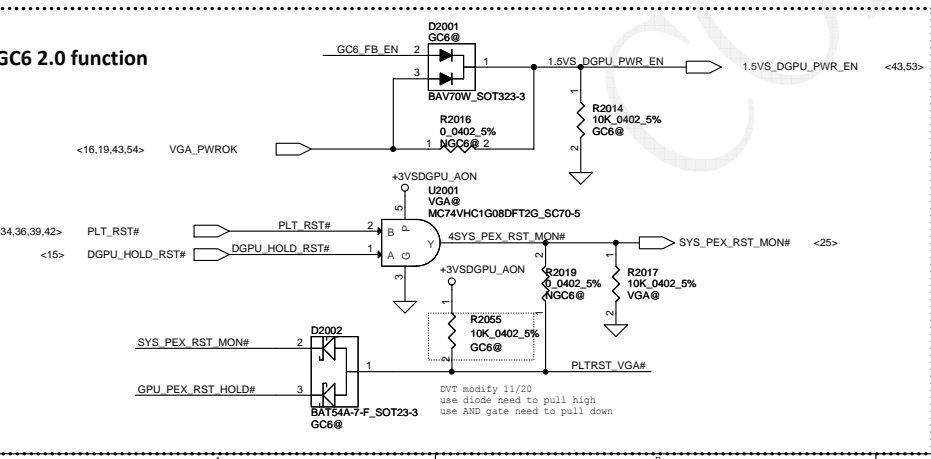
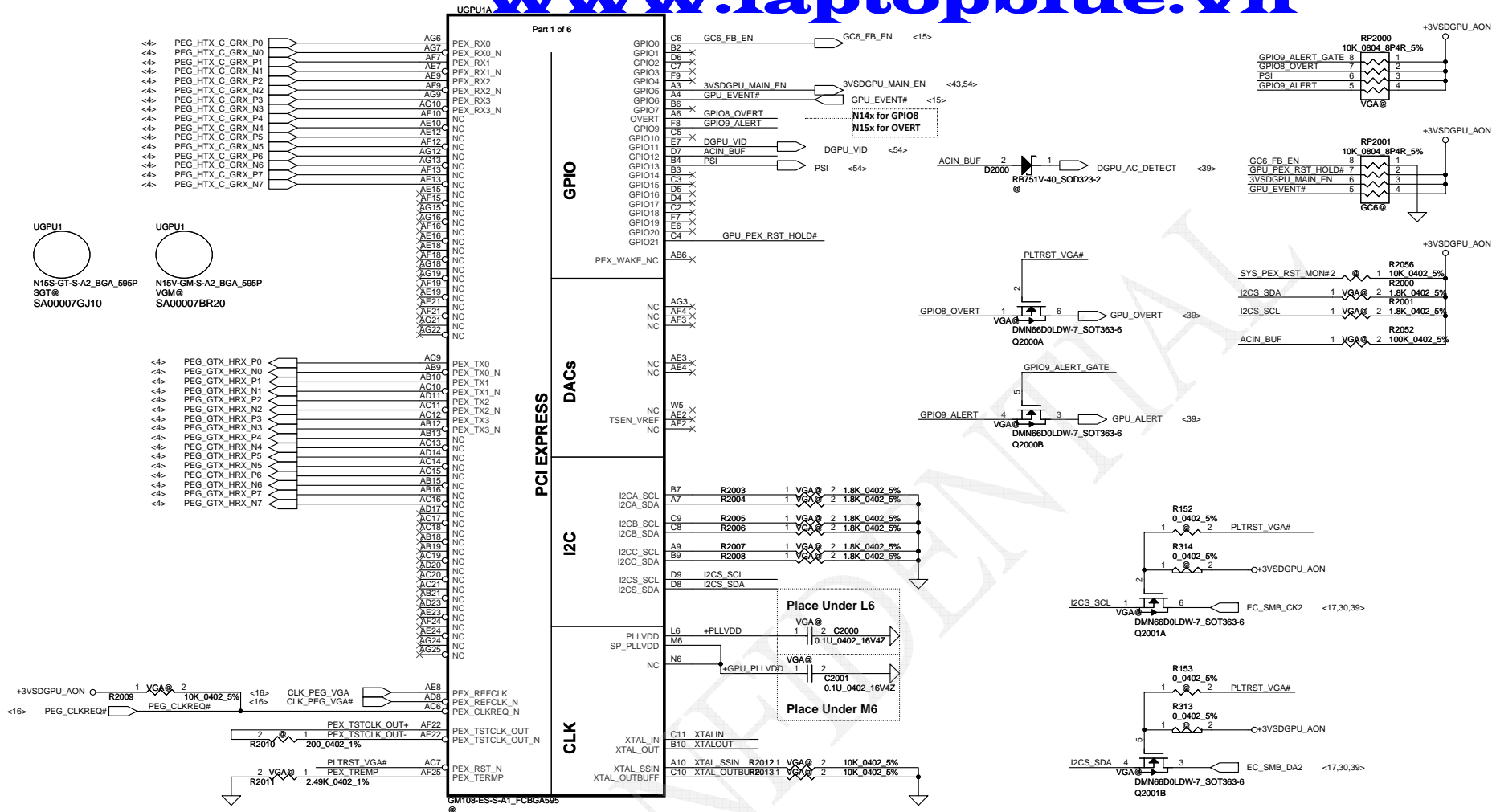


PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



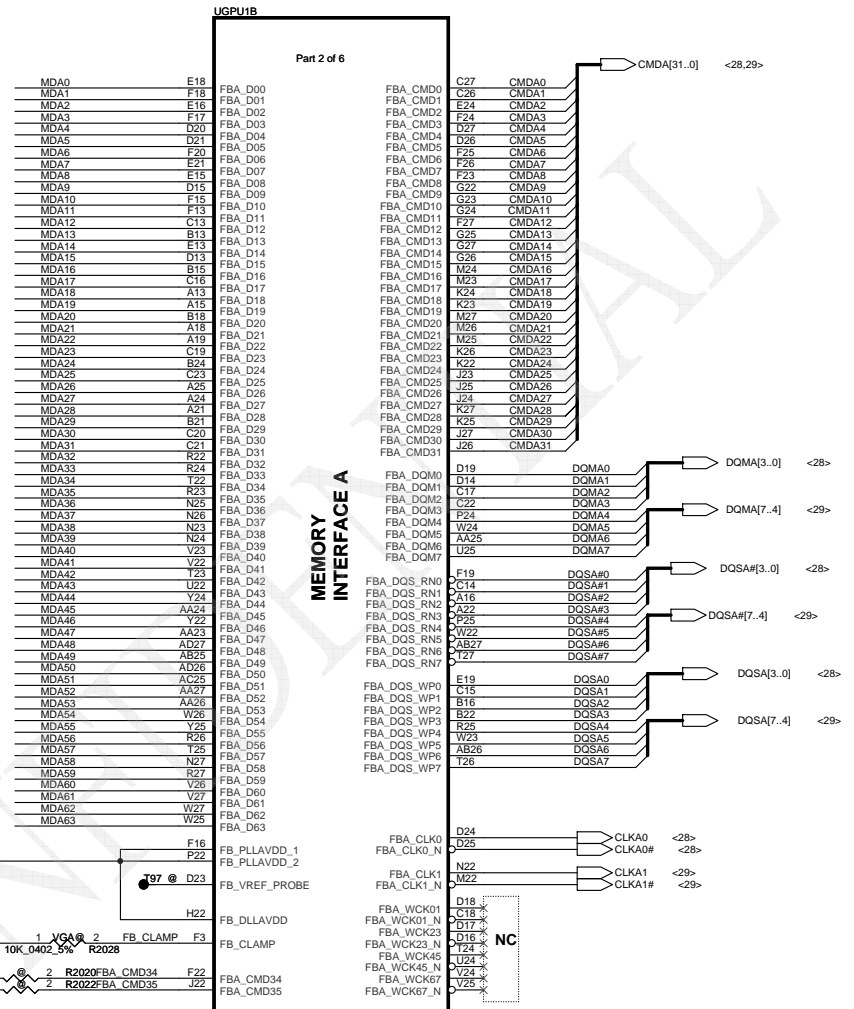
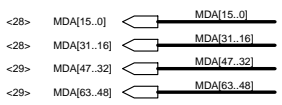
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Issued Date	2013/12/26	Deciphered Date	2014/12/26	Title	PCH (10/10) VSS
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GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		



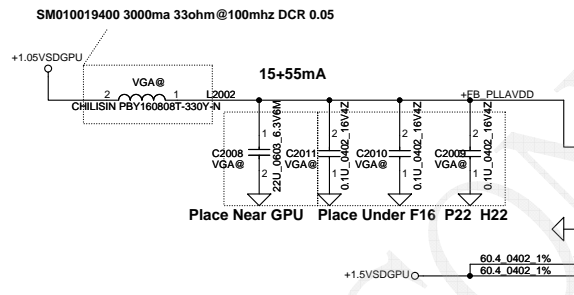
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VRAM Interface

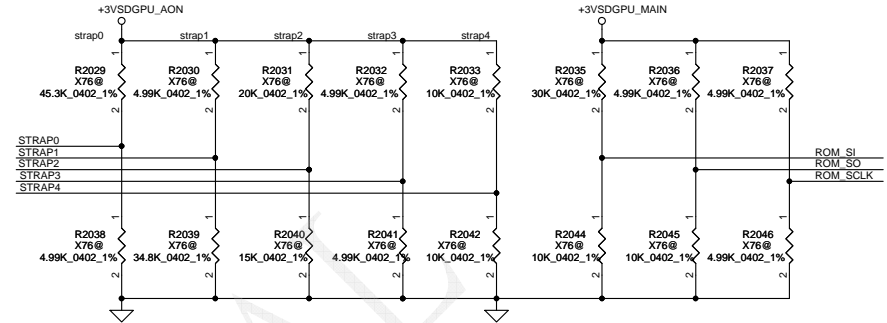
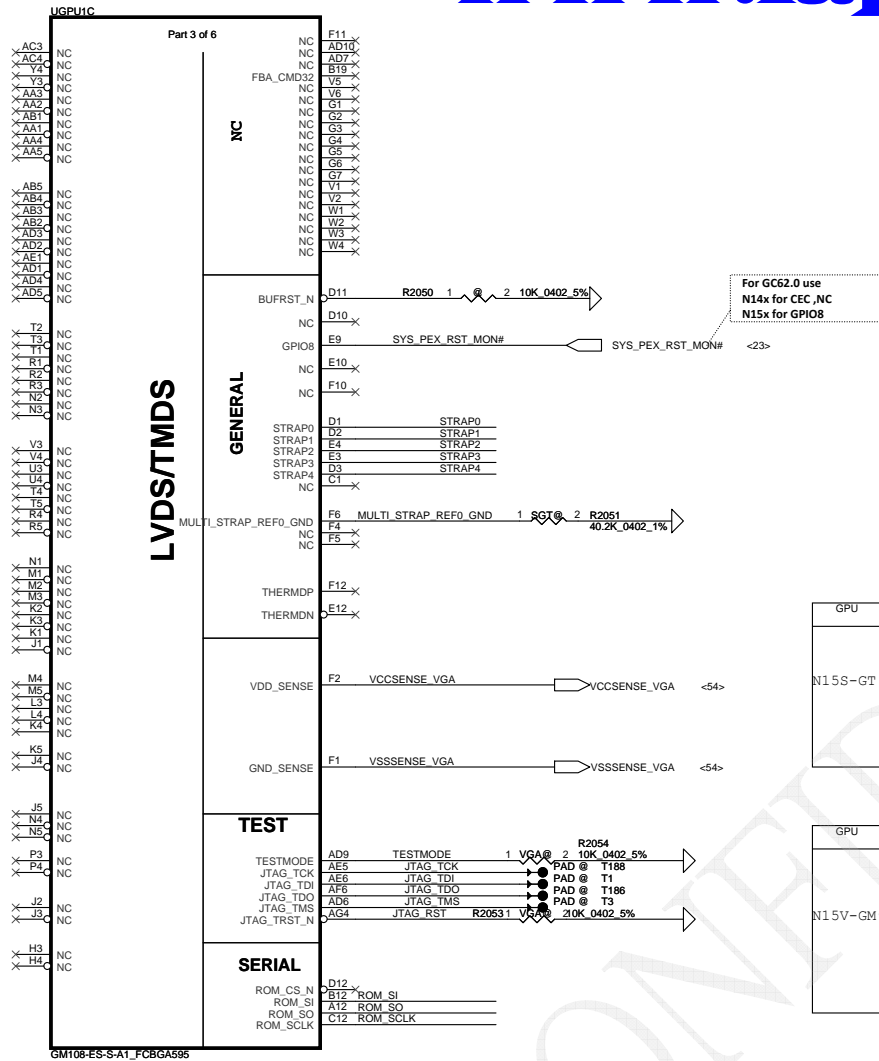


NV 15x DG-06803-V03

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2
		22 µF	X5R	0805	1
		Bead Type			
		30 Ω (ESR=0.010 Ω)	0603	1	Near GPU



GM108-ES-S-A1_FCBGA595



For N15S-GT Multilevel strap table

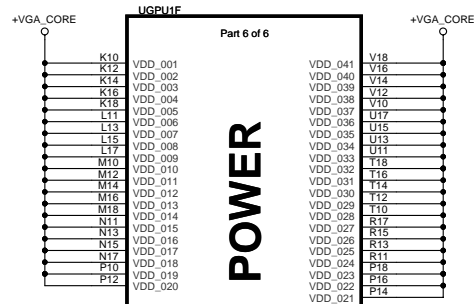
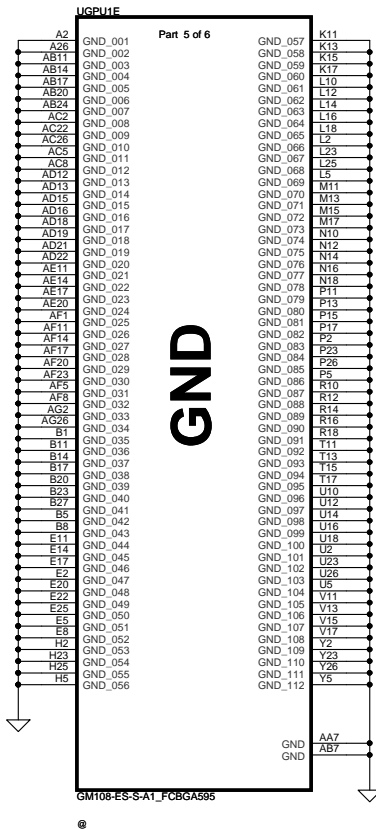
Decive ID : 0x1341

GPU	X76	Size	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N15S-GT		1G	128Mx16x4		PU 50K	NC	NC	NC	NC	PD 24.9K	PD 4.99K	PD 4.99K
				0x4 (SA000077K20) Micron MT41J256M16HA-093G-E								
	X76550BOLA0			0x5 (SA000076P20) Samsung K4W4G1646D-BC1A								
	X76550BOLA1			0x3 (SA00006E840) Hynix H5TC4G63AFR-11C								
	X76550BOLA2	2G	256Mx16x4							PD 30.1K		
										PD 20K		

For N15V-GL/GM Binary strap table

Decive ID : 0x1140

GPU	X76	Size	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GM	X76550BOLA3	1G	128Mx16x4	0x1 (SA000067550) Micron MT41J128M16JT-093G-K	PU 10K	PD10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
	X76550BOLA4			0x5 (SA000068U00) Samsung K4W2G1646E-BC1A	PU 10K	PD10K	PU 10K	PD 10K				
	X76550BOLA5			0xC (SA00006H430) Hynix H5TC2G63FFR-11C	PD 10K	PD10K	PU 10K	PD 10K				
	X76550BOLA6			0xD (SA000077K20) MT41J256M16HA-093G-E	PU 10K	PD10K	PU 10K	PD 10K				
	X76550BOLA7	2G	256Mx16x5	0x9 (-) K4W4G1646D-BC1A	PU 10K	PD10K	PD 10K	PD 10K				
	X76550BOLA8			0x4 (-) H5TC4G63AFR-11C	PD 10K	PD 10K	PU 10K	PD 10K				



NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint	Population	Location	Comments
GB2B-64	4.7 μ F	X6S	0603	10	10	Under GPU
	1 μ F	X6S	0402	4	4	Under GPU
	47 μ F	X5R	0805	1	1	Near GPU
	22 μ F	X5R	0805	1	1	Near GPU
	4.7 μ F	X5R	0805	5	5	Near GPU
	330 μ F	POS	7343	1	1	Near GPU ESR \leq 6 m Ω

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core	FB Total	1.05V Total
		—	1.5/1.35V	1.05V
N155-GM	DDR3/L	48.11	4.23	0.91
N155-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

Table 6. EDP-Peak at T_J = 102 °C

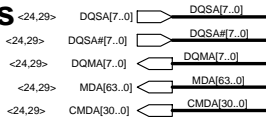
Power Supply Rail (V)	N15V-GM-S
	DDR3/L
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

Table 7. EDP-Peak at T_J = 102 °C

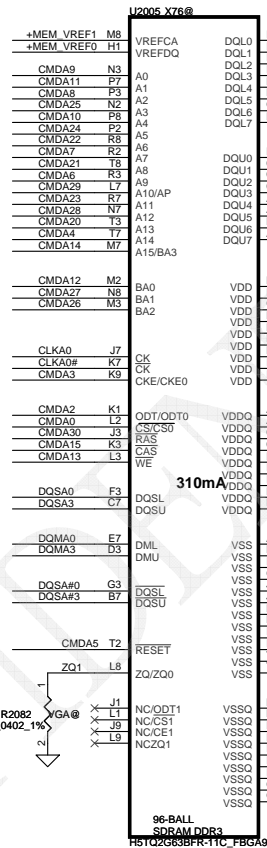
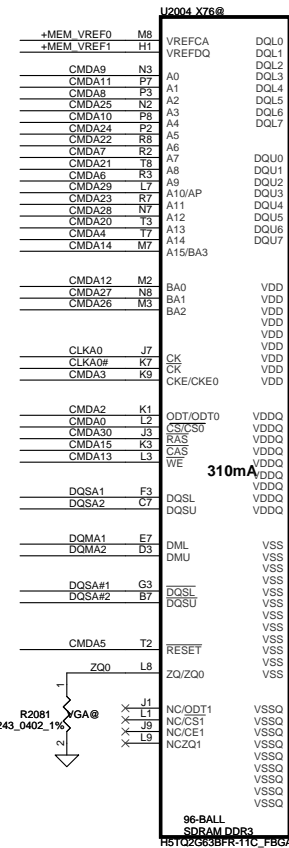
Power Supply Rail (V)	N15V-GL
	DDR3
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

VRAM DDR3 chips



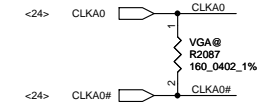
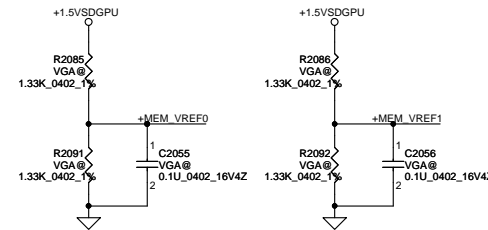
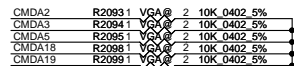
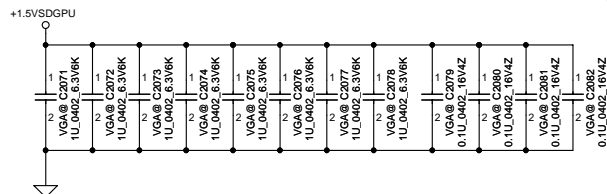
Upper 32

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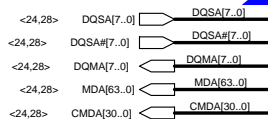


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*

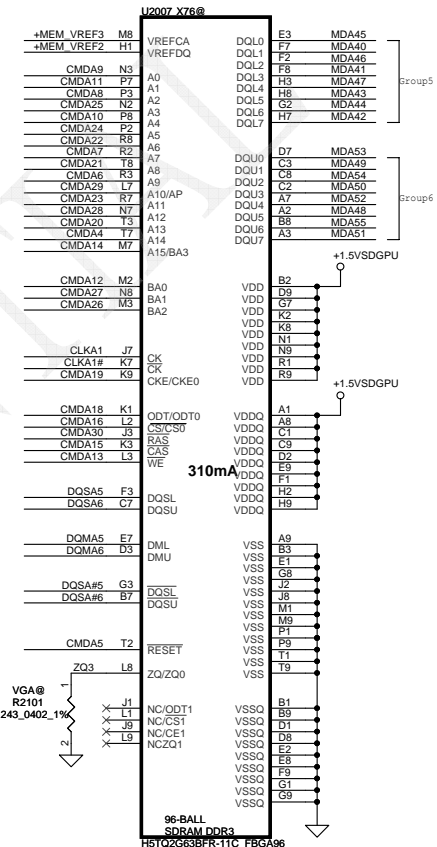
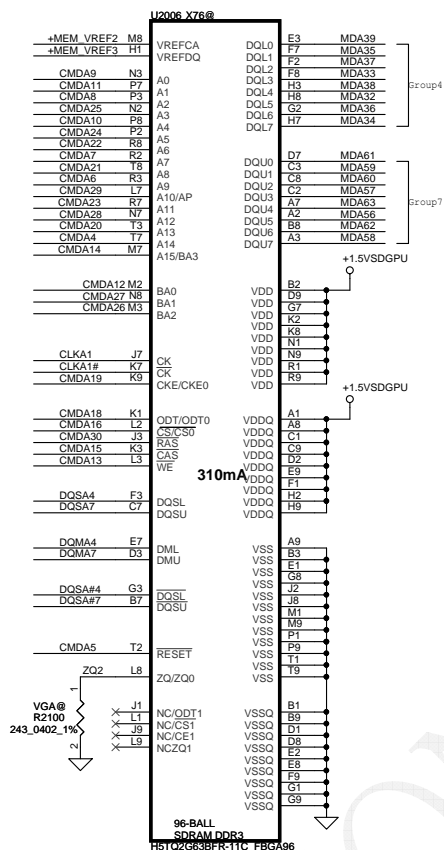
Command Bit	Default Pull-down
ODT#	10k
CKE#	10k
RST	10k
CS*	No Termination



VRAM DDR3 chips

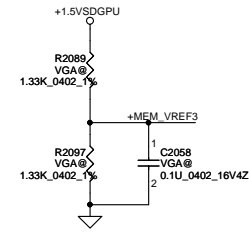
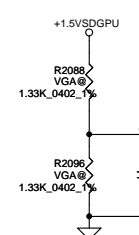
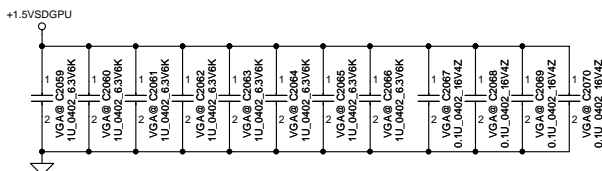
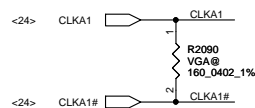


Lower 32

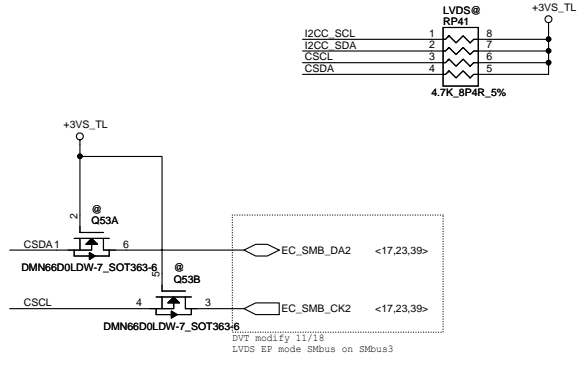
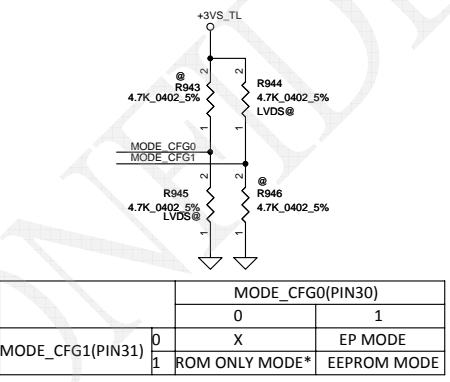
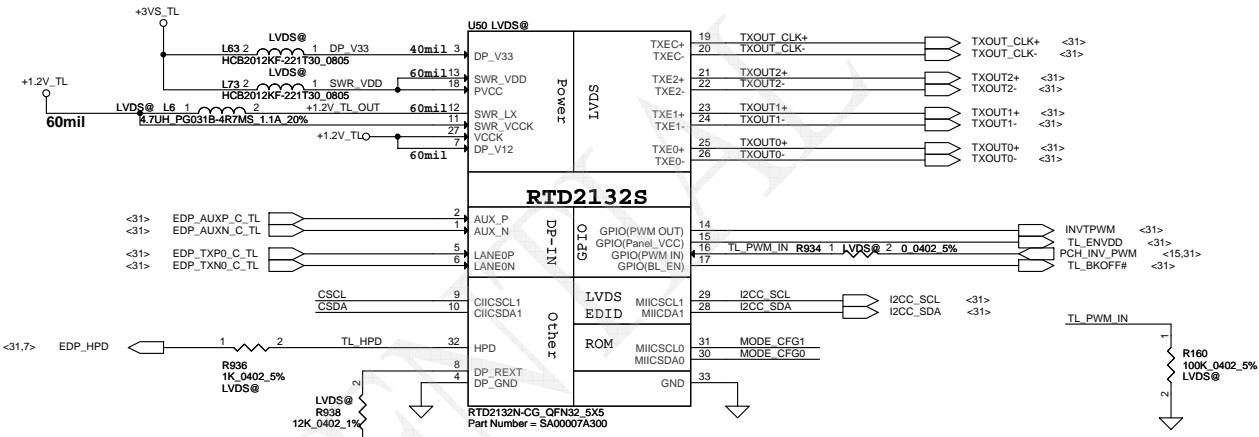
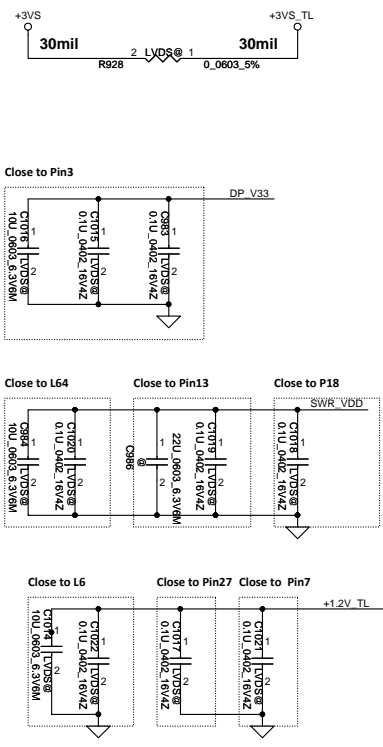


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

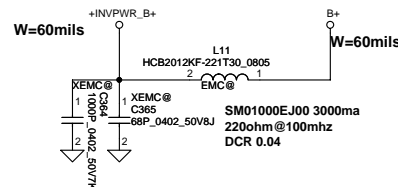
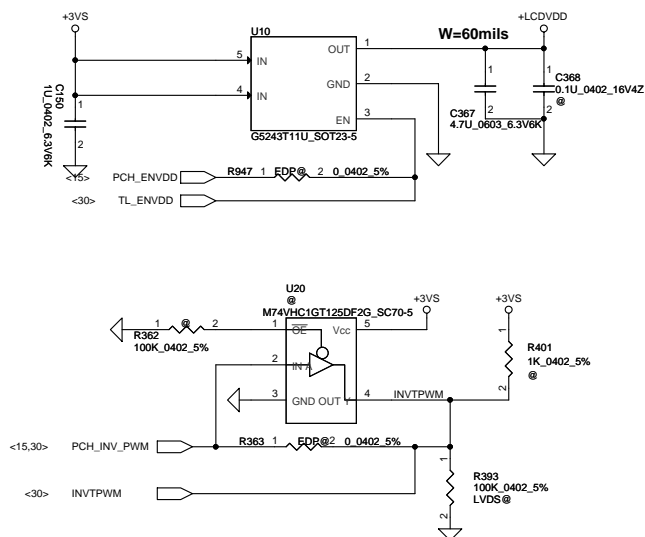


LVDS Translator - RTD2132R

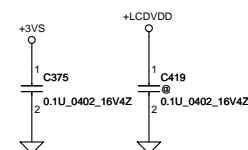


EDP / LVDS conn.

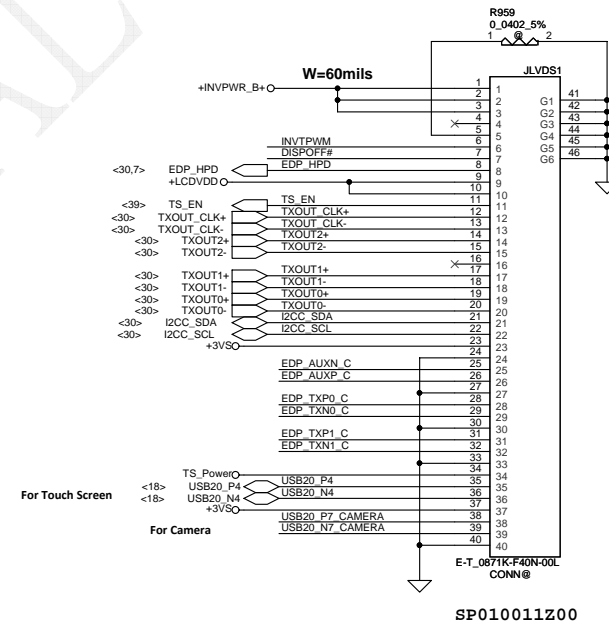
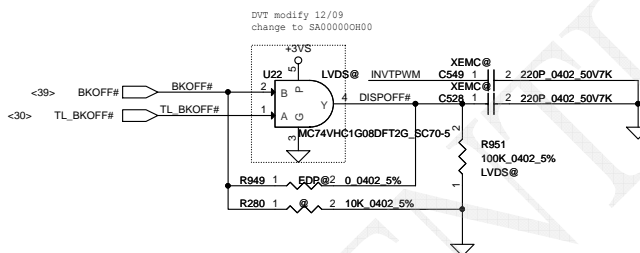
LCD POWER CIRCUIT



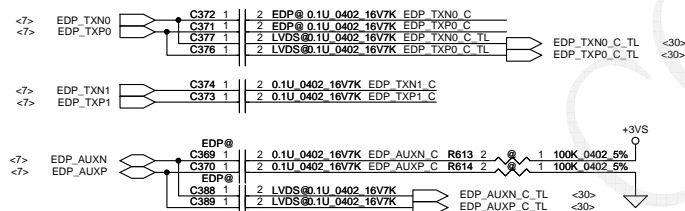
Place closed to JLVDS1



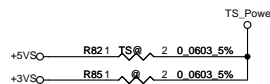
LCD/ LED PANEL Conn.



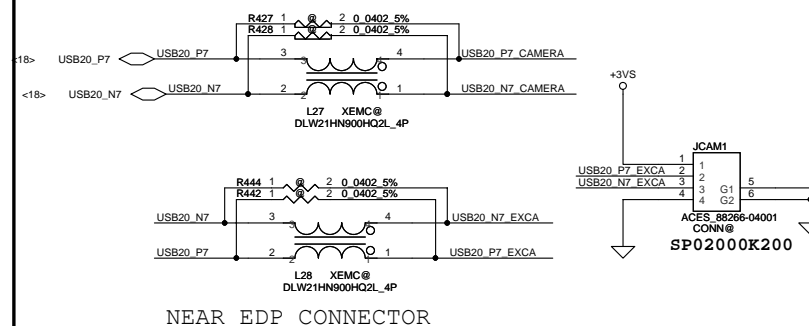
eDP



Touch Screen

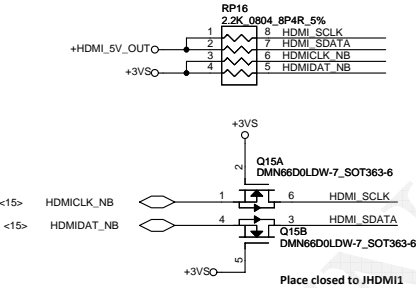
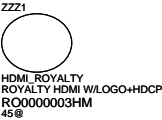
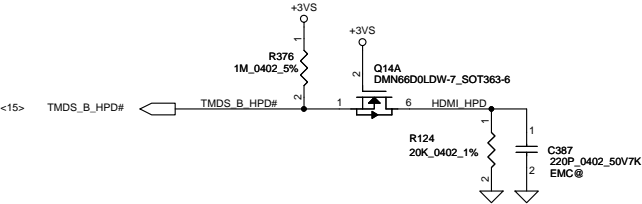
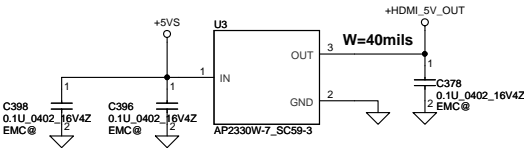


Camera

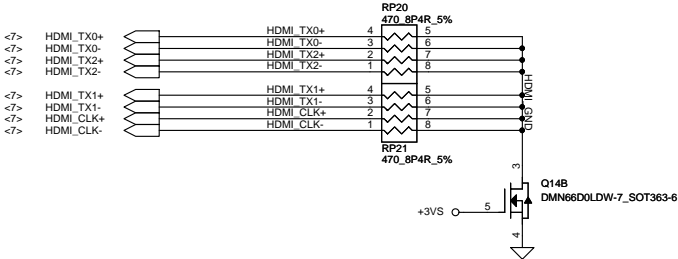
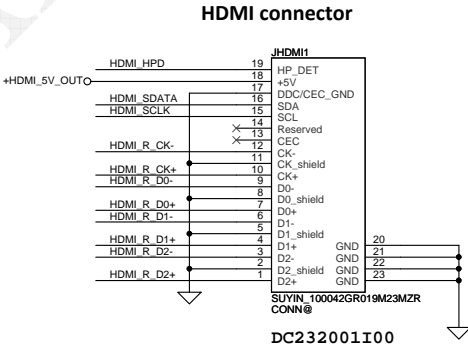


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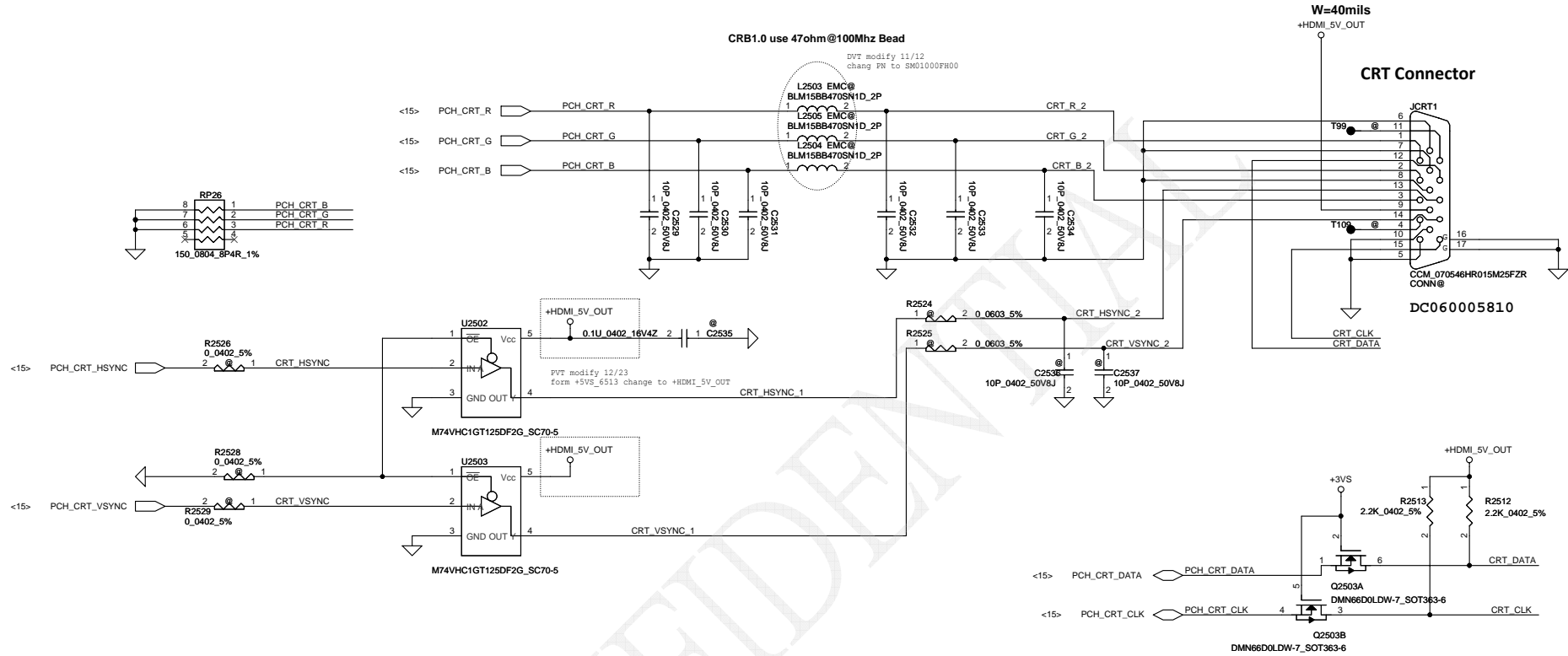
HDMI conn.



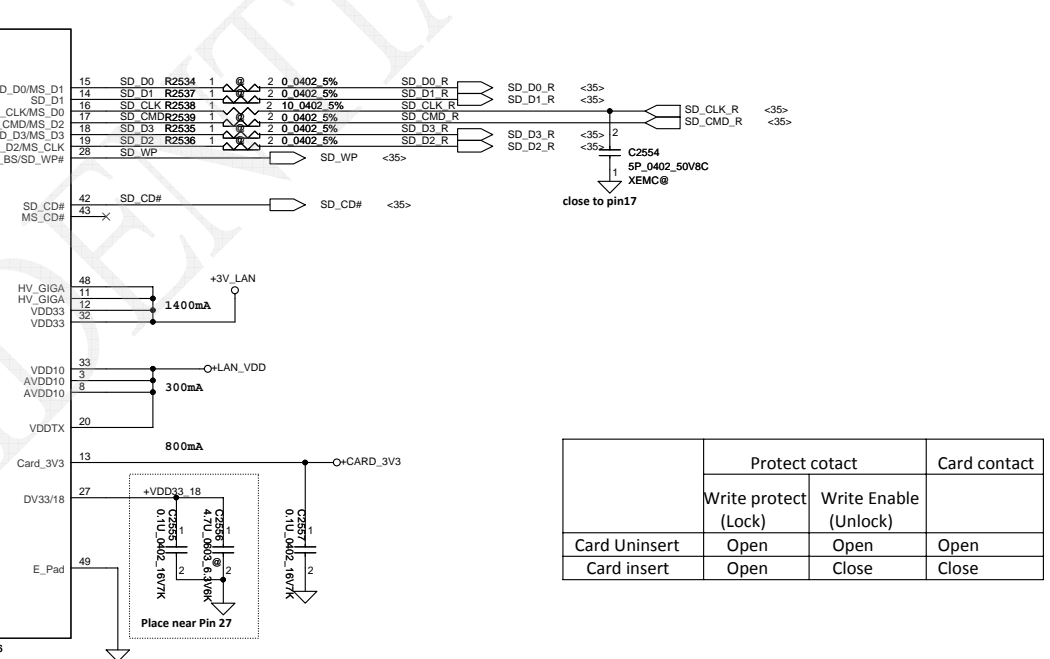
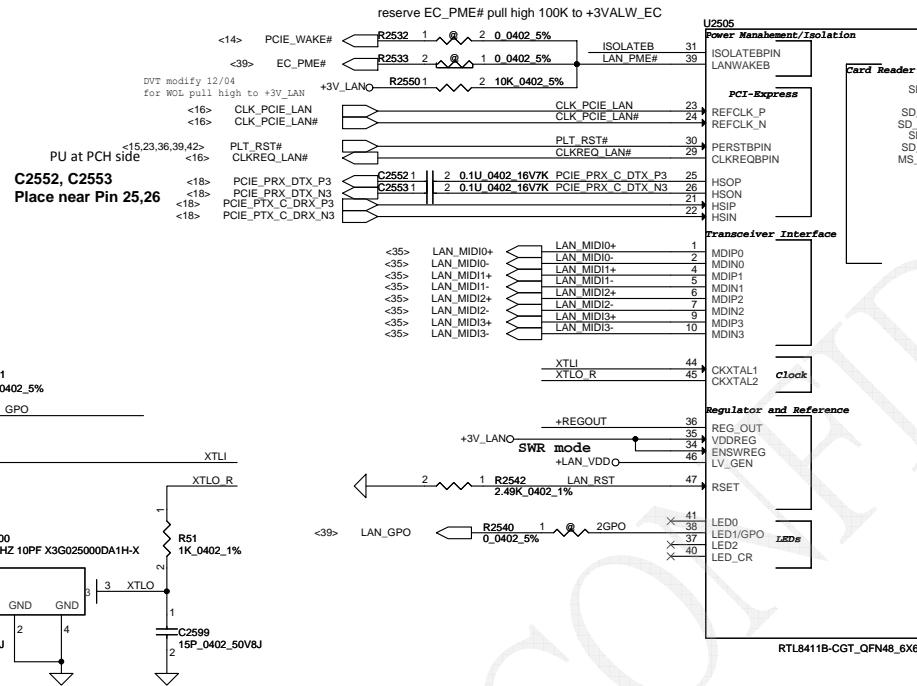
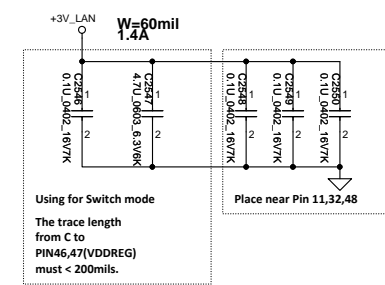
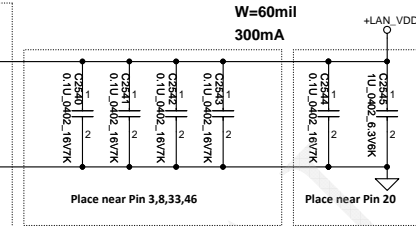
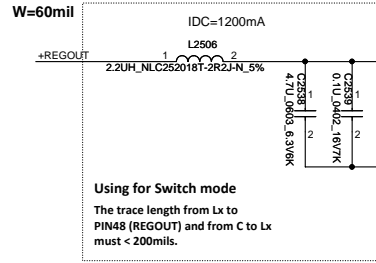
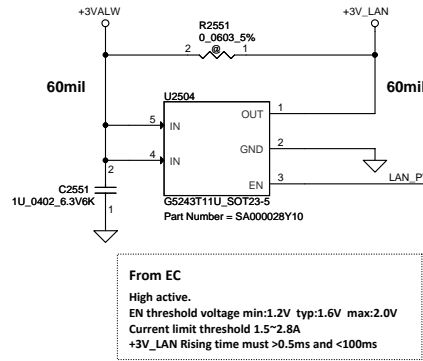
HDMI_CLK-	R368	1	XEMC@ 2	0.0402_5%	HDMI_R_CLK-
HDMI_CLK+	R369	1	XEMC@ 2	0.0402_5%	HDMI_R_CLK+
HDMI_TX0-	R370	1	XEMC@ 2	0.0402_5%	HDMI_R_D0-
HDMI_TX0+	R371	1	XEMC@ 2	0.0402_5%	HDMI_R_D0+
HDMI_TX1-	R372	1	XEMC@ 2	0.0402_5%	HDMI_R_D1-
HDMI_TX1+	R373	1	XEMC@ 2	0.0402_5%	HDMI_R_D1+
HDMI_TX2-	R374	1	XEMC@ 2	0.0402_5%	HDMI_R_D2-
HDMI_TX2+	R375	1	XEMC@ 2	0.0402_5%	HDMI_R_D2+



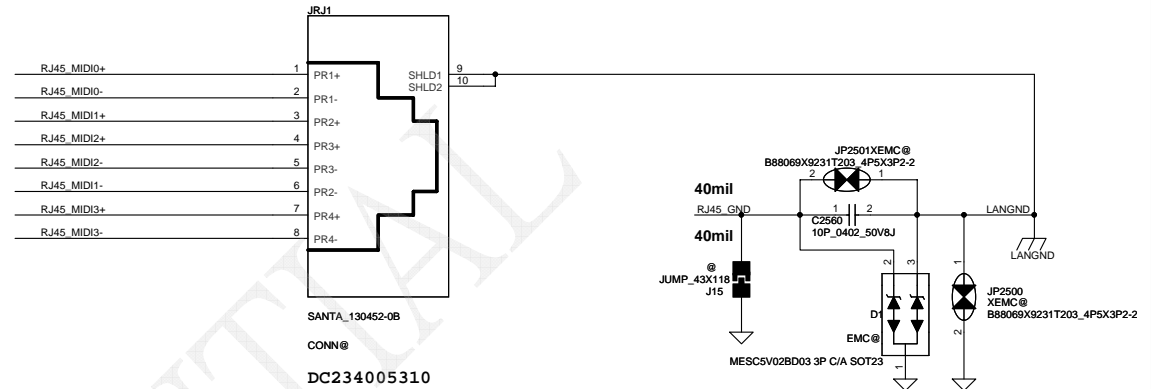
CRT conn.



LAN-RTL8411B

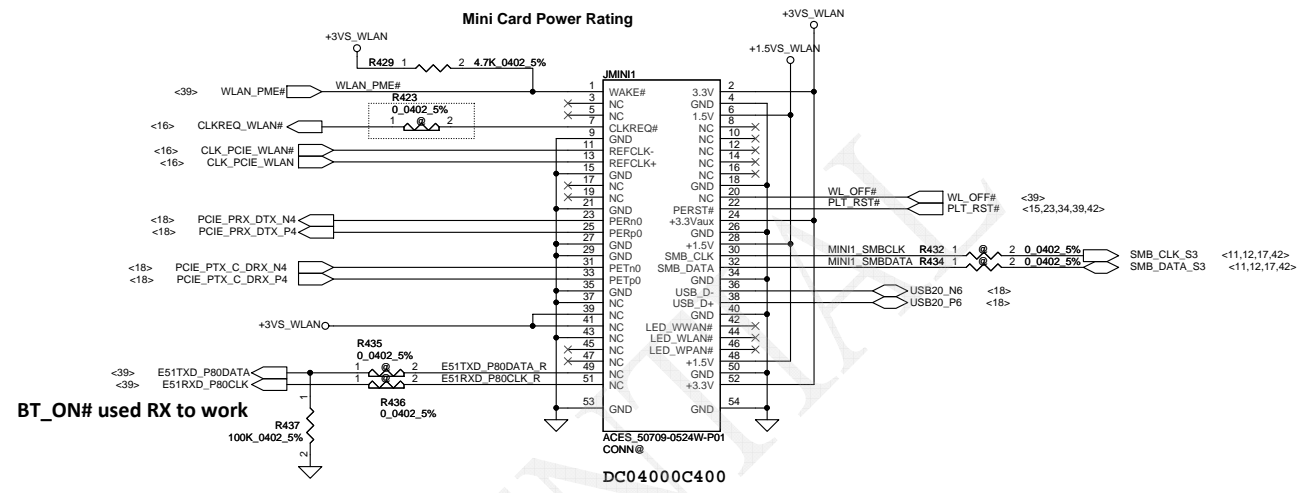
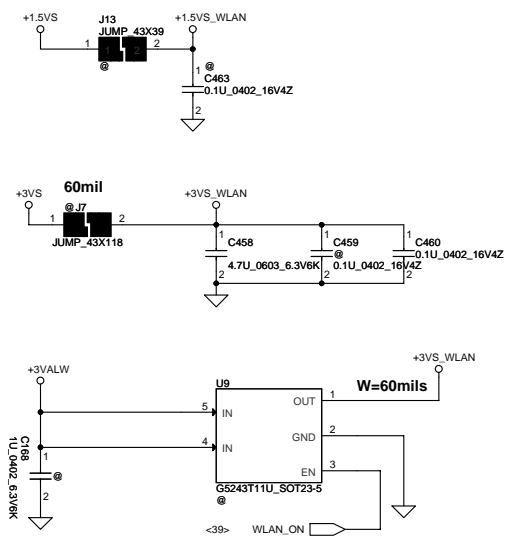


	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close



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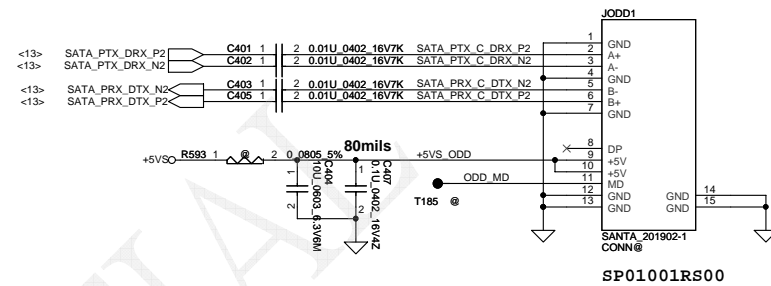
Wireless LAN



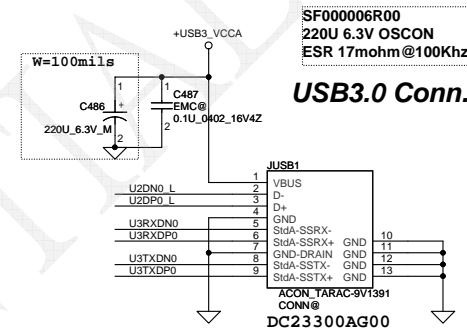
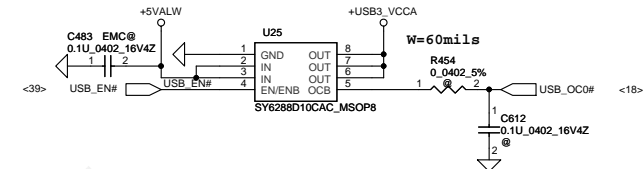
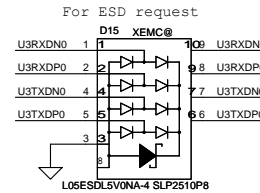
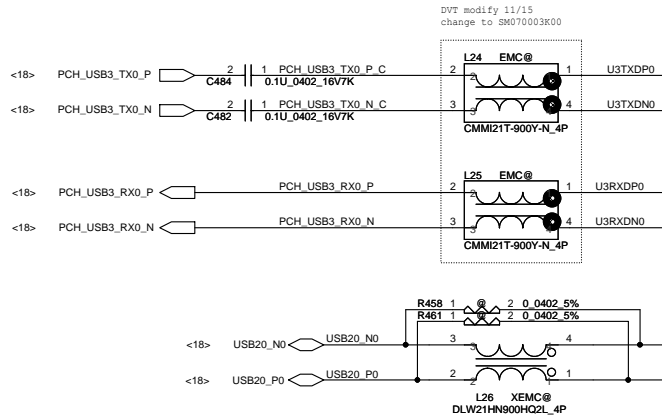
BT_ON# used RX to work

DC04000C400

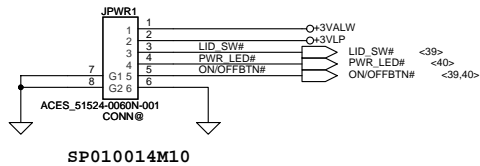
C	D
topblue.vn	
SATA ODD Conn.	



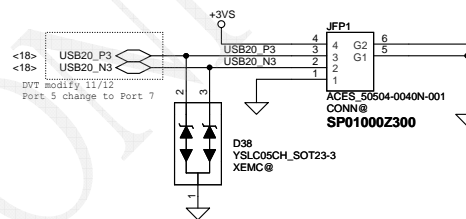
USB3.0 (Port 0)



PWR/B

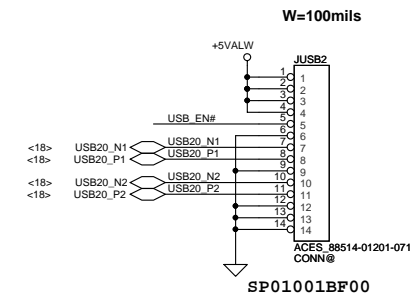


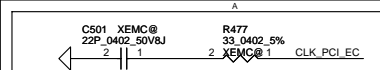
Finger Print /B for BA50



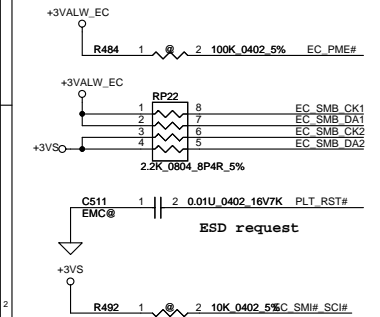
USB/B (USB Port 1, Port2)

USB/B Conn.

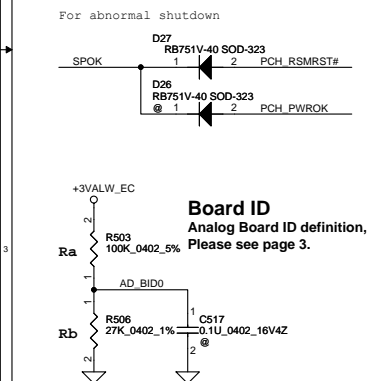




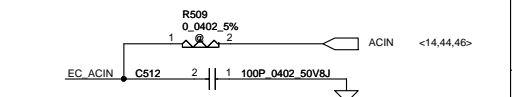
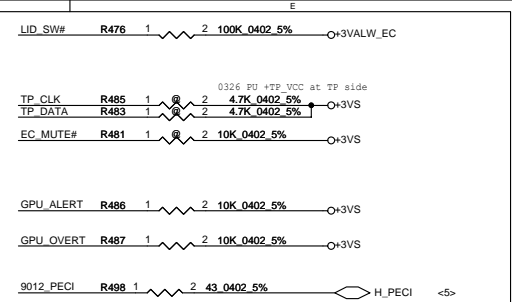
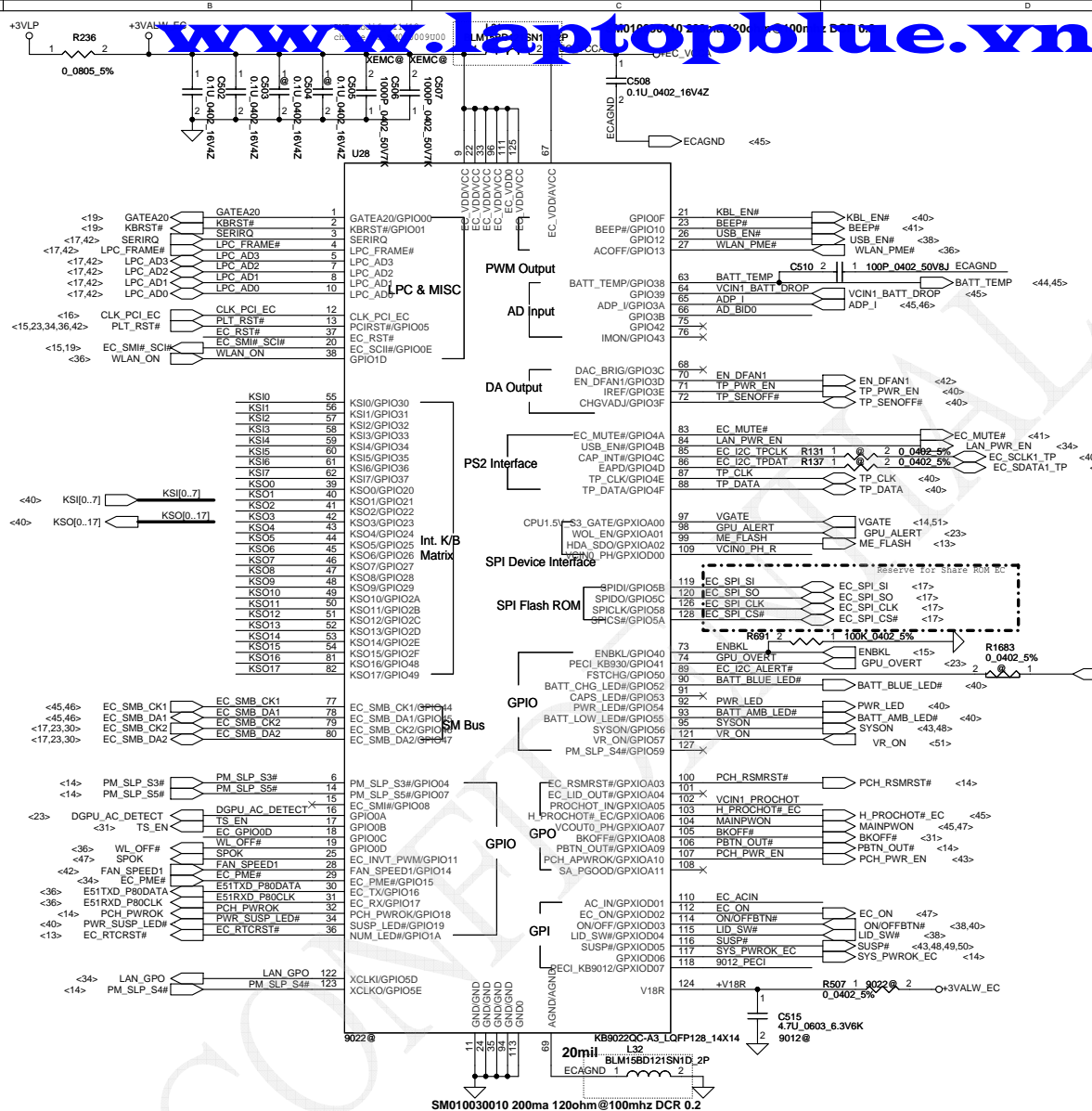
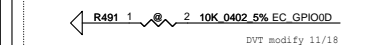
9022: ECRST# is internally pull-up to VCC via 40Kohm resistor, so can remove external pull-up resistor and capacitor.



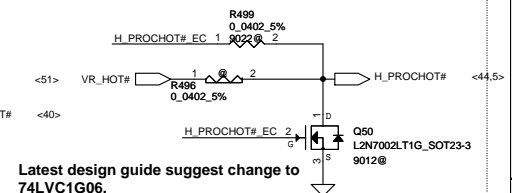
9022:Change control method from push-pull to open-drain,
so EC_SCI# must be pull high. *PU on PCH side
(Pull high in PCH side)



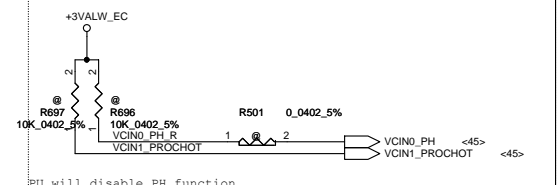
```
reserve for LVDS EP mode
```



KB9022&9012 Co-Layout Item



Latest design guide suggest change to 74LVC1G06.



```

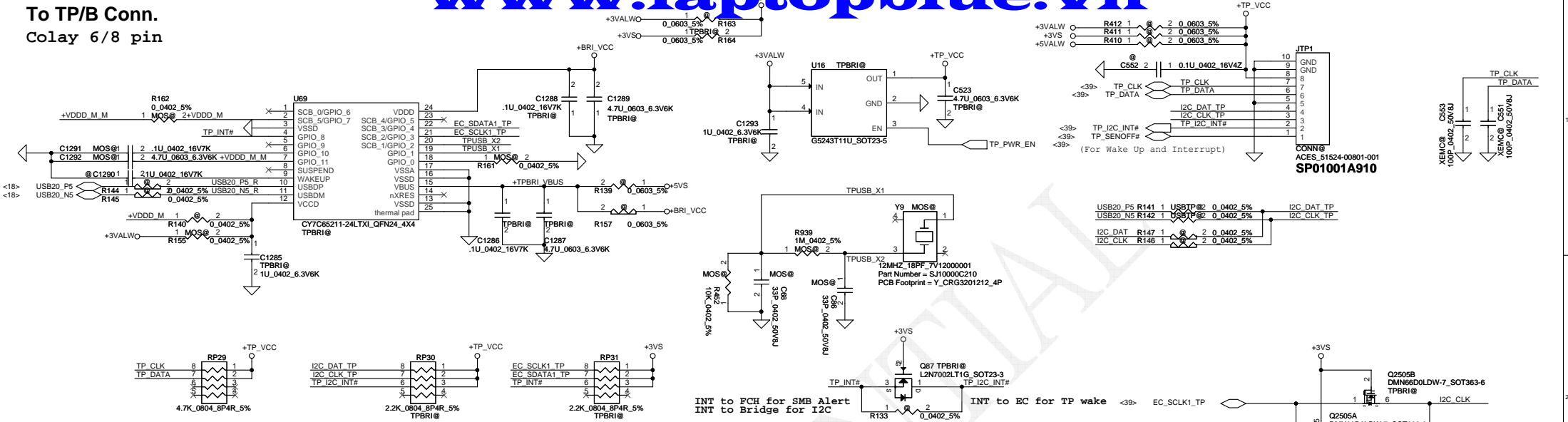
|PU will disable PH function

```

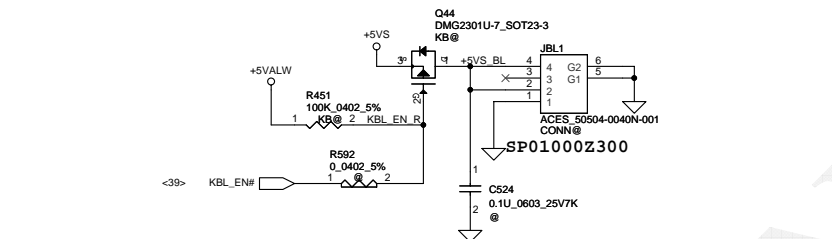


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To TP/B Conn.
Colay 6/8 pin



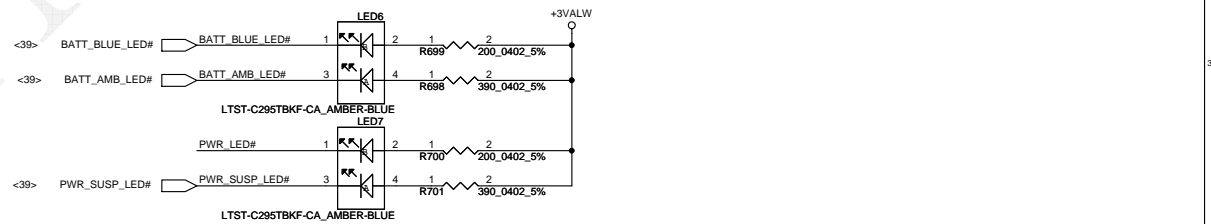
KB BackLight Conn. Reserve



NOTE :
Cypress pop : TPBRI@
MOSART pop : TPBRI@ , MOS@ (default flash type)
EC I2C pop : R128,R129,R132,RP19
USBTP pop : USBTP@, (Q87 or R132, R130 option)

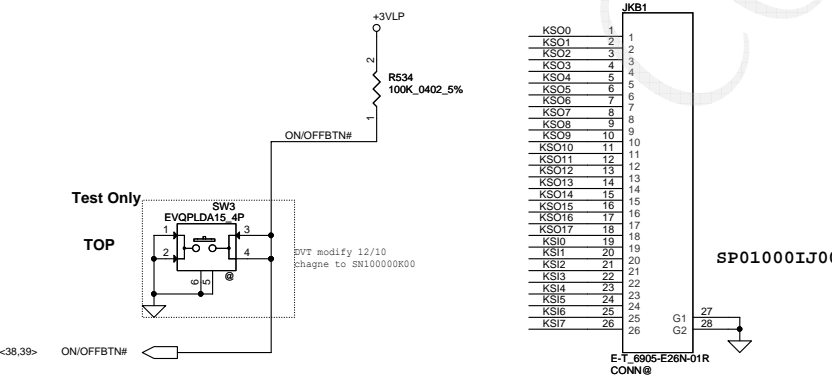


LED



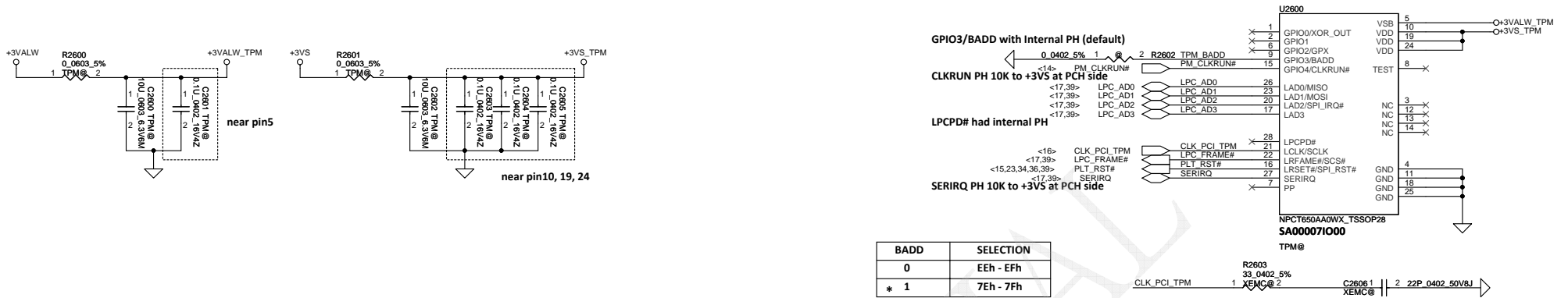
ON/OFF BTN

KB Conn.

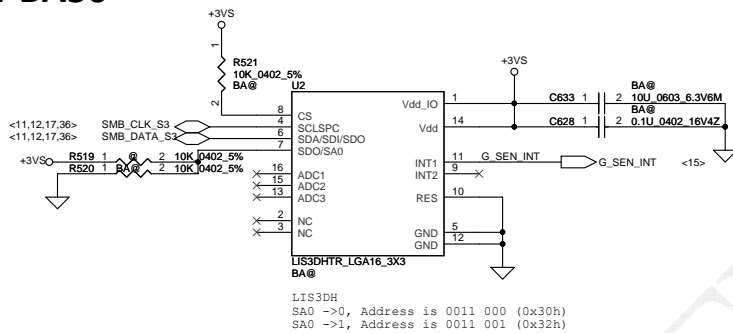


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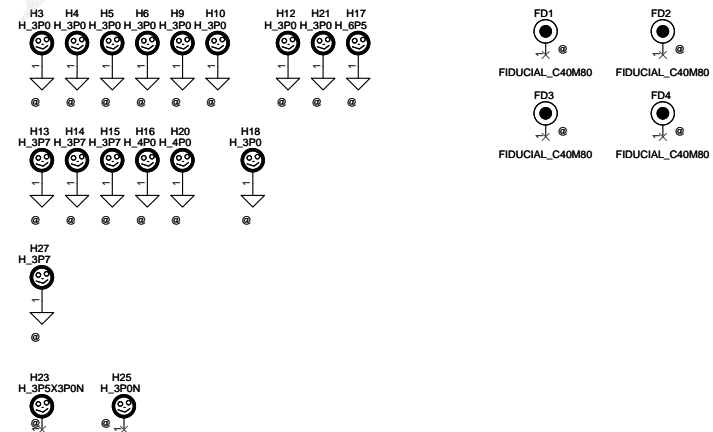
TPM Board for 2015



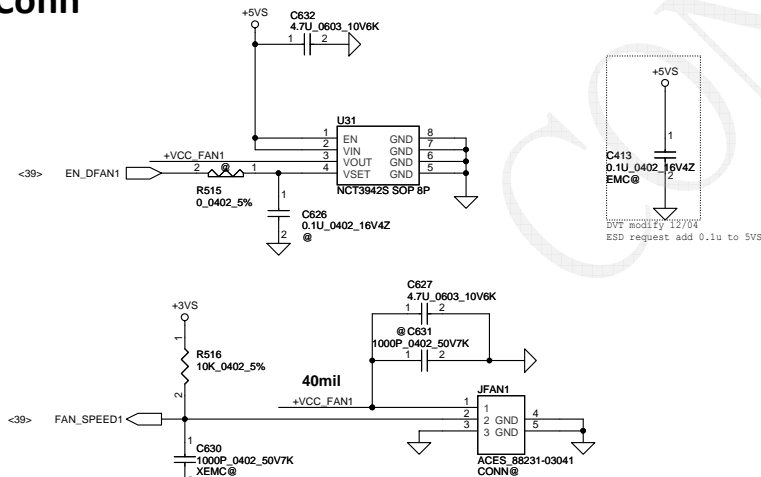
G-Sensor for BA50



Screw Hole

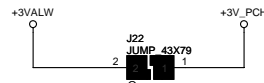


FAN1 Conn

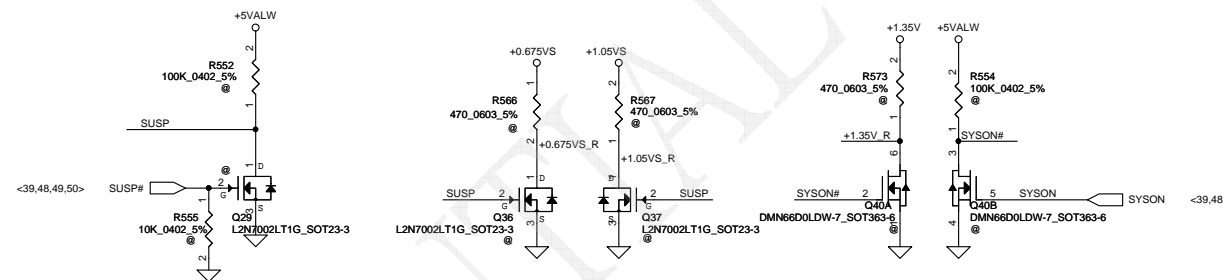
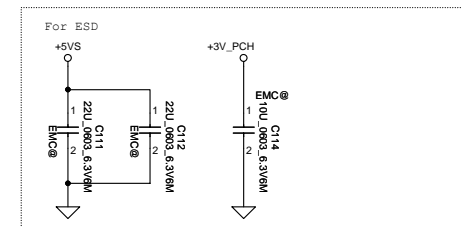
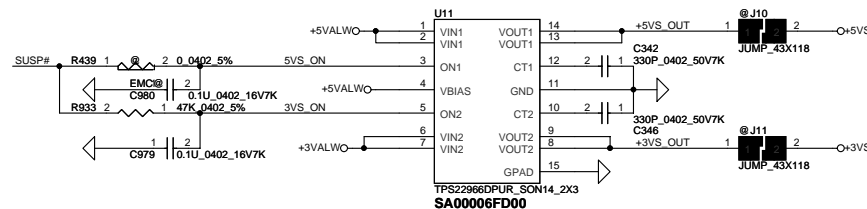
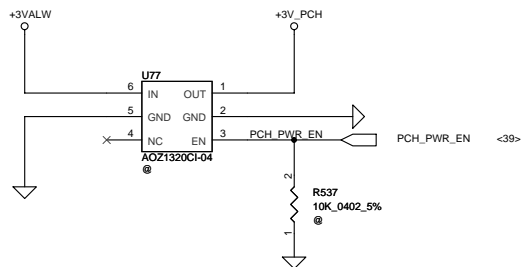


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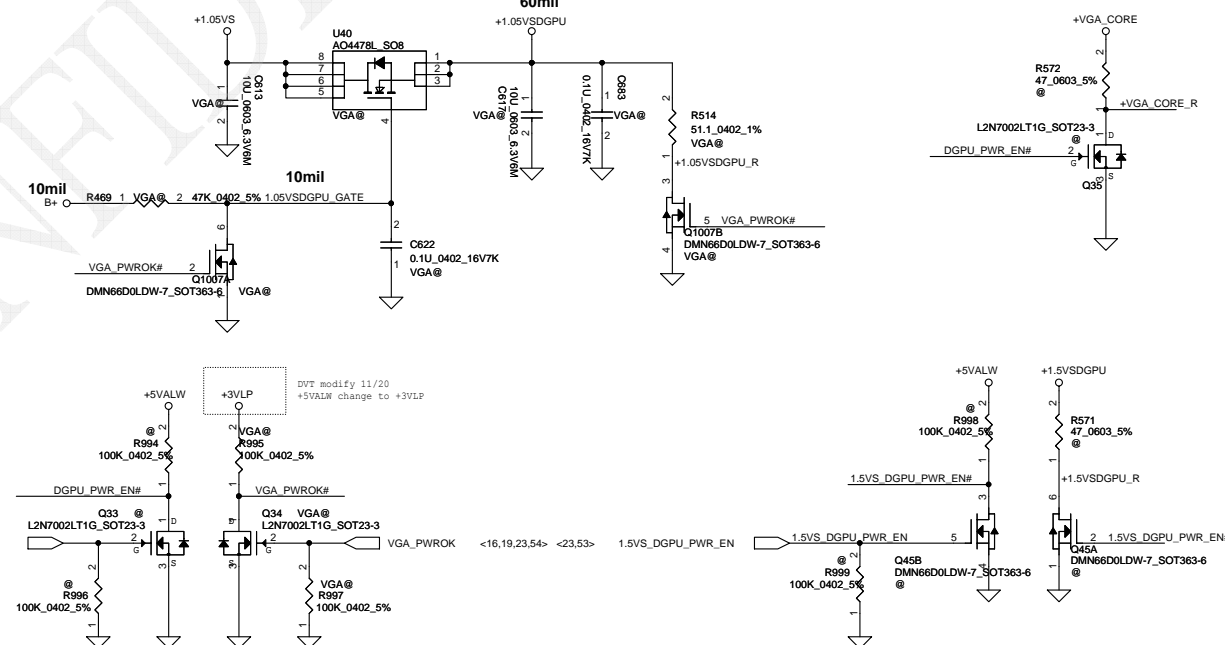
DC & VGA Interface



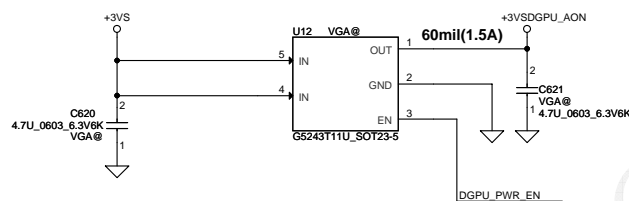
+3VALW to +3V_PCH Transfer



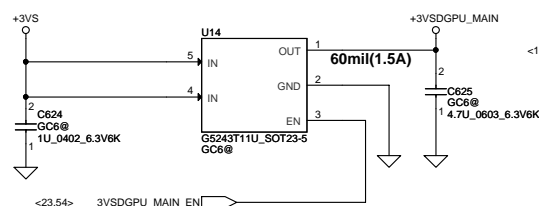
+1.05VS to +1.05VSDGPU



+3VS to +3VSDGPU_AON for GPU

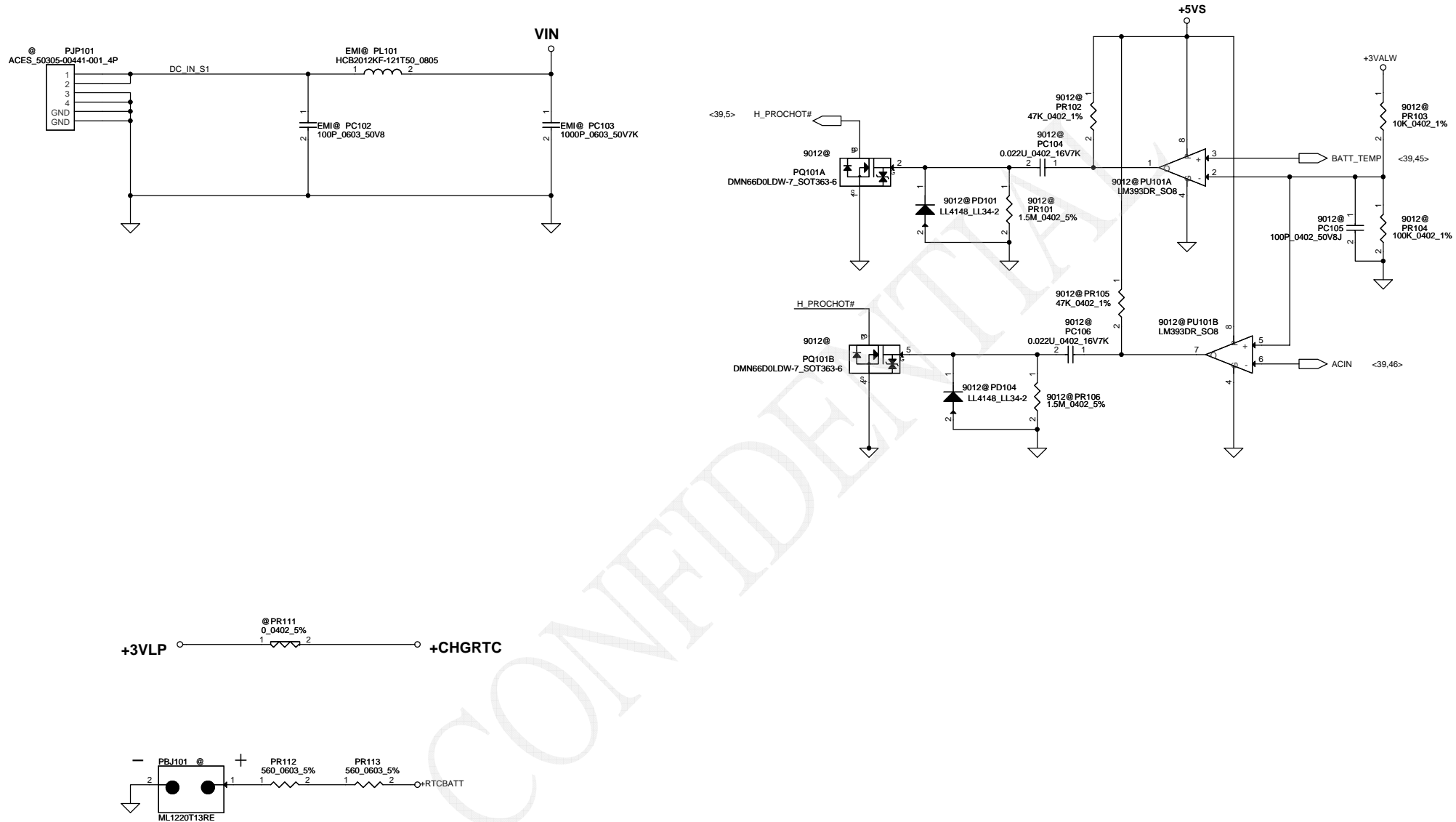


+3VS to +3VSDGPU_MAIN for GC6-2.0

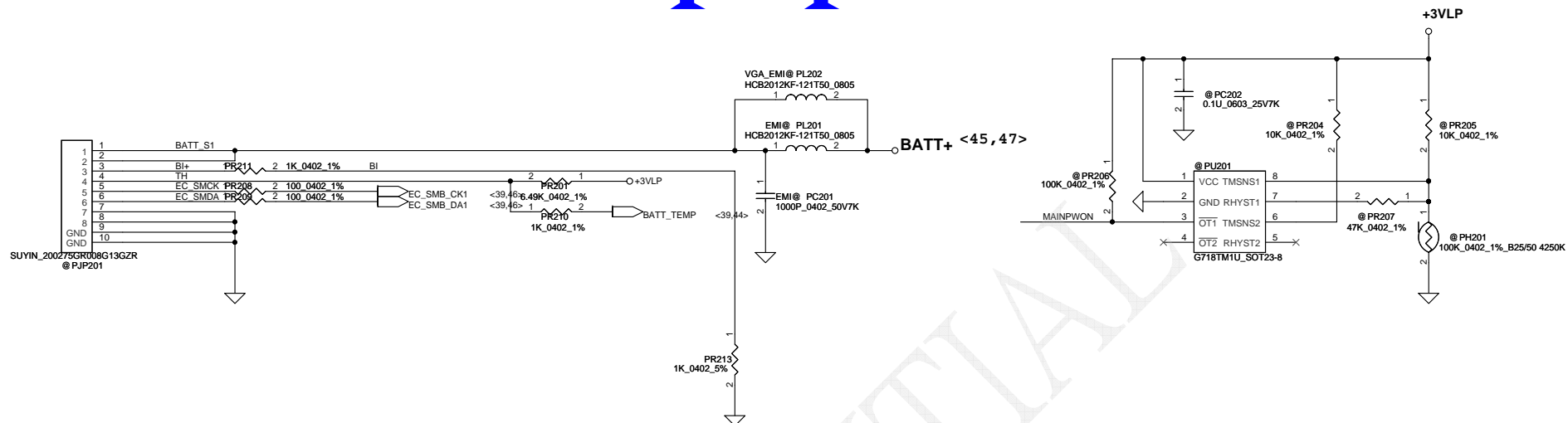


3VSDGPU_MAIN_EN From GPU

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				Customer	0.2
				25WAW M/B LA-B702	
				Date: Tuesday, May 27, 2014	Sheet 43 of 56



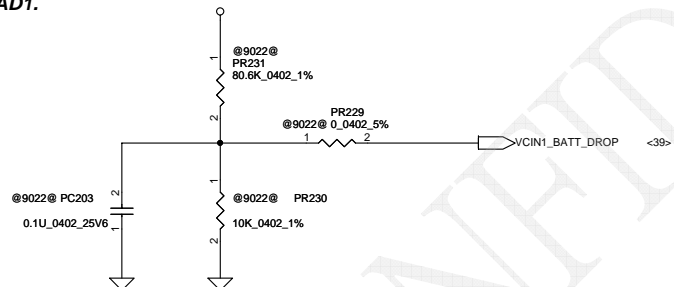
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2013/10/02

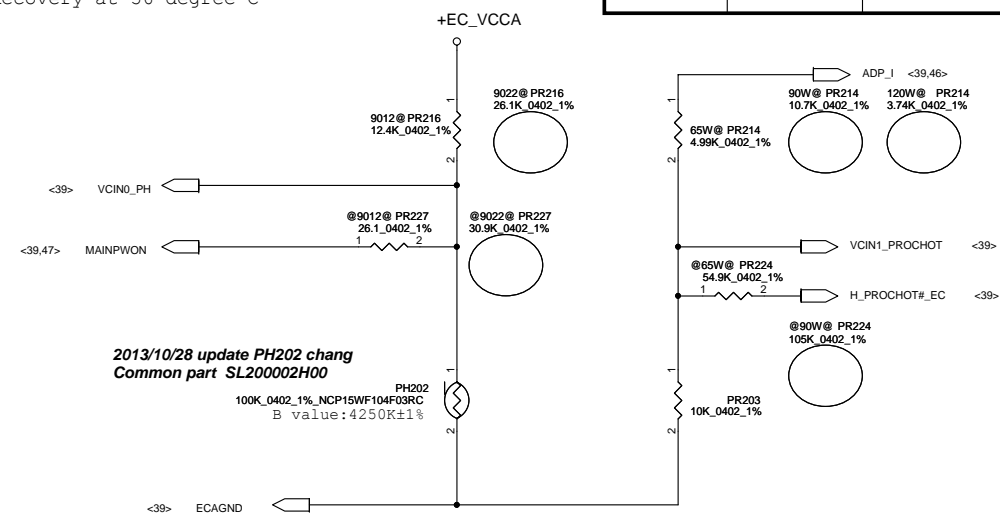
Add for ENE9022 Battery Voltage drop detection. B+
Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.
B+=9V



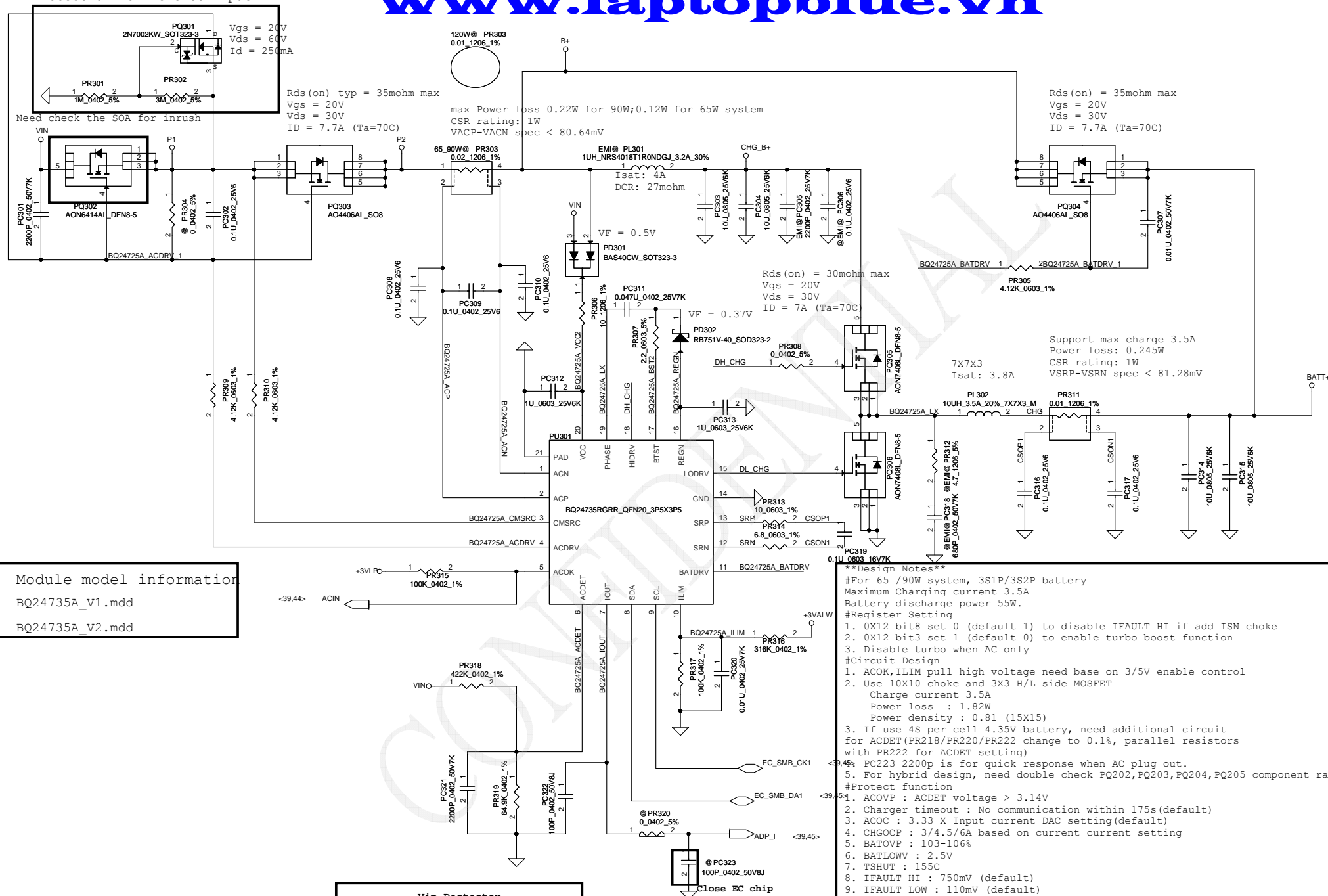
PH202 under CPU bottom side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C

For KB9012 sense 20ms	Active	Recovery
65W	85W, 1.2V	65W, 0.913V
90W	117W, 1.2V	90W, 0.915V
120W	156W, 1.2V	120W, 0.919V



2013/10/28 update PH202 chang
Common part SL200002H00

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2013/12/26				2014/12/26				Title			
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Security Classification

Compal Secret Data

Issued Date

2013/12/26

Deciphered Date

2014/12/26

Compal Electronics, Inc.

CHARGER

Document Number

Common Circuit

Rev

0.1

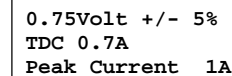
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				Date:	Tuesdays, May 27, 2014	
				Sheet	47	of 56

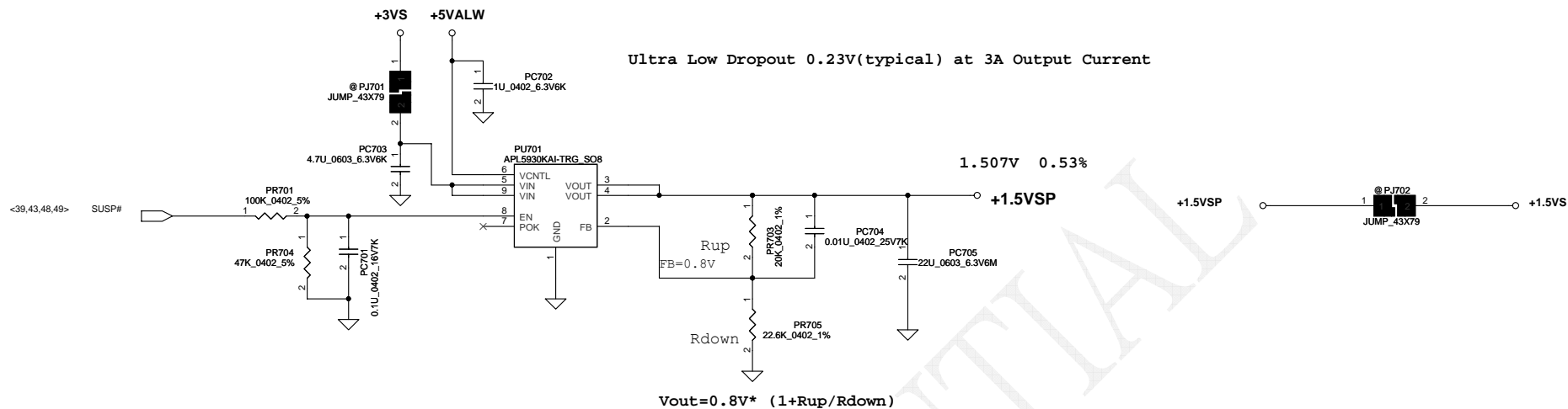


Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET footprint: SIS412DN

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				Date:	Tuesday, May 27, 2014	Sheet 48 of 56

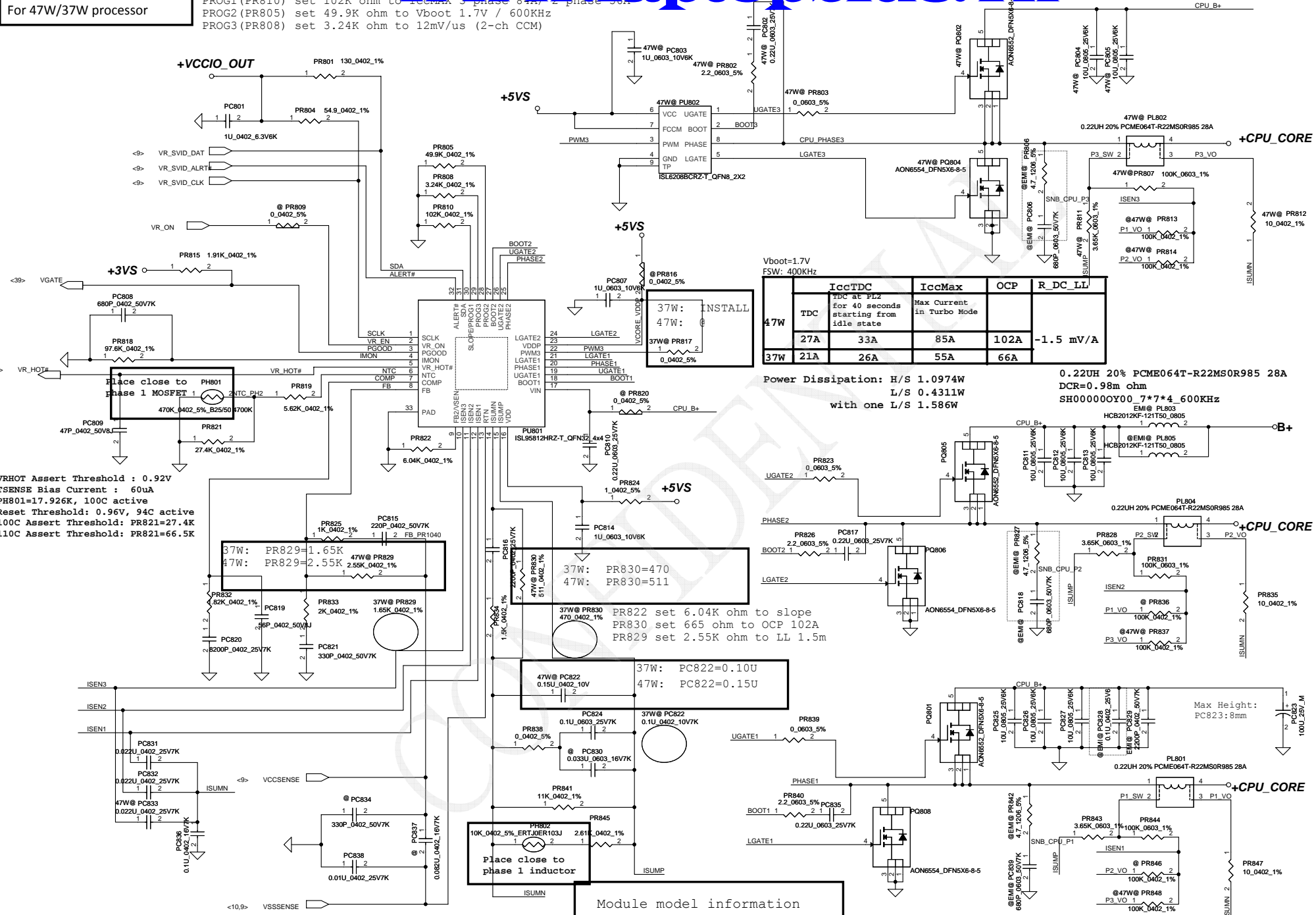


Ultra Low Dropout 0.23V(typical) at 3A Output Current

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Module design of ISL95812 VR
For 47W/37W processor

PROG1 (PR810) set 102K ohm to IccMax 3 phase 84W / 2 phase 36W
PROG2 (PR805) set 49.9K ohm to Vboot 1.7V / 600KHz
PROG3 (PR808) set 3.24K ohm to 12mV/us (2-ch CCM)



VRHOT Assert Threshold : 0.92V
TSense Bias Current : 60uA
PH801=17.926K, 100C active
Reset Threshold: 0.96V, 94C active
100C Assert Threshold: PR821=27.4K
110C Assert Threshold: PR821=66.5K

		IccTDC	IccMax	OCP	R_DC_LL
47W	TDC	TDC at PL2 for 40 seconds starting from idle state	Max Current in Turbo Mode		
	27A	33A	85A	102A	-1.5 mV/A
37W	21A	26A	55A	66A	

Power Dissipation: H/S 1.0974W
L/S 0.4311W
with one L/S 1.586W

0.22uH 20% PCME064T-R22MS0R985 28A
DCR=0.98m ohm
SH000000Y00_7*7*4_600KHz

37W: PR829=1.65K
47W: PR829=2.55K

37W: PR830=470
47W: PR830=511

37W: PC822=0.10u
47W: PC822=0.15u

Place close to phase 1 inductor

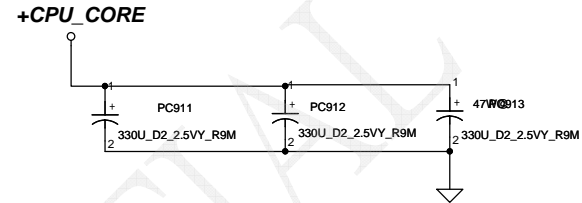
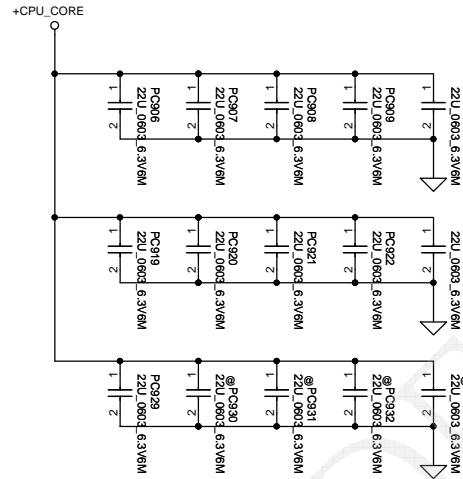
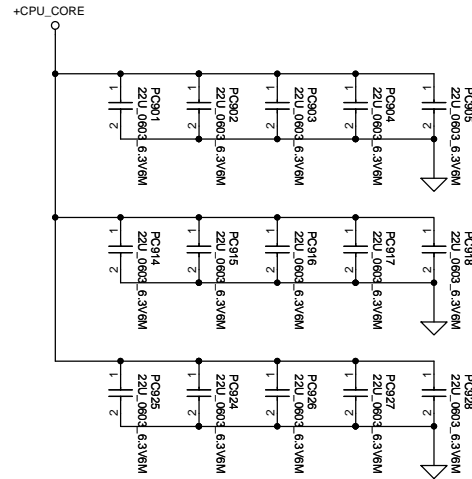
Module model information
ISL95812_V1A.mdd for IC portion
ISL95812_V1B.mdd for SW portion

Local sense put on HW site

3 X 330u/9m (47W)
2 X 330u/9m (37W)
24 pcs 22uF and reserve 4 pcs
2013/08/16

2 X 330u/9m (47W)
26 pcs 22uF
2013/08/28

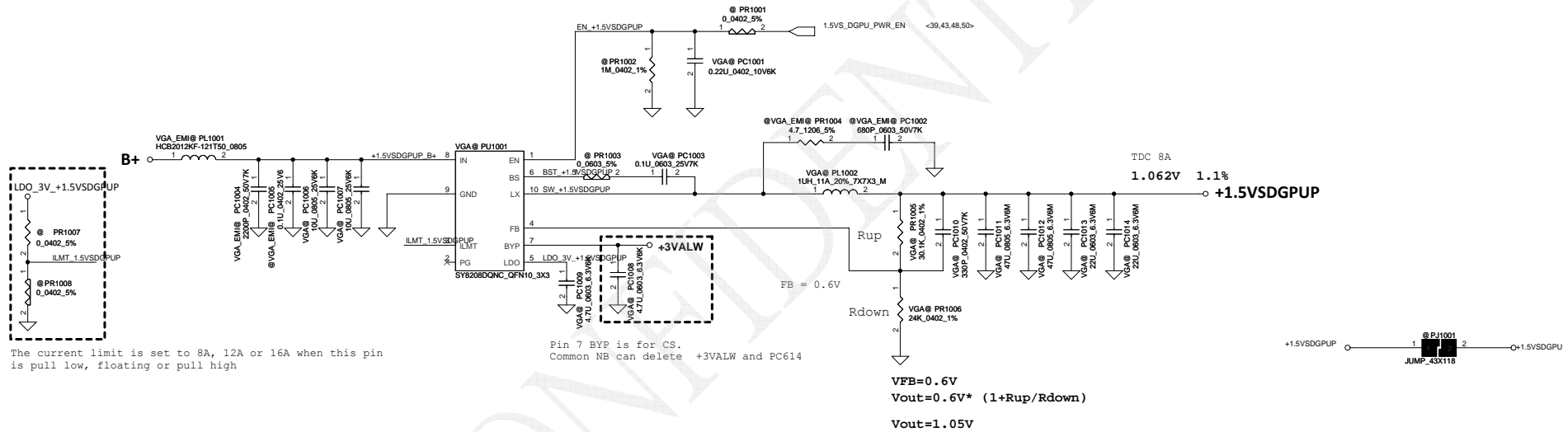
PWR Rule
需確認最新SPEC.
Modify 8/6.



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								Size		Document Number				Rev	
								Custom						0.1	
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Module model information
SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR1002



Module model information: RT8813A_V1A for IC module RT8813A_V1B for SW module

Vboot=Vvref*Ref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Ref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Ref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

PWM-VID Spec and component Values

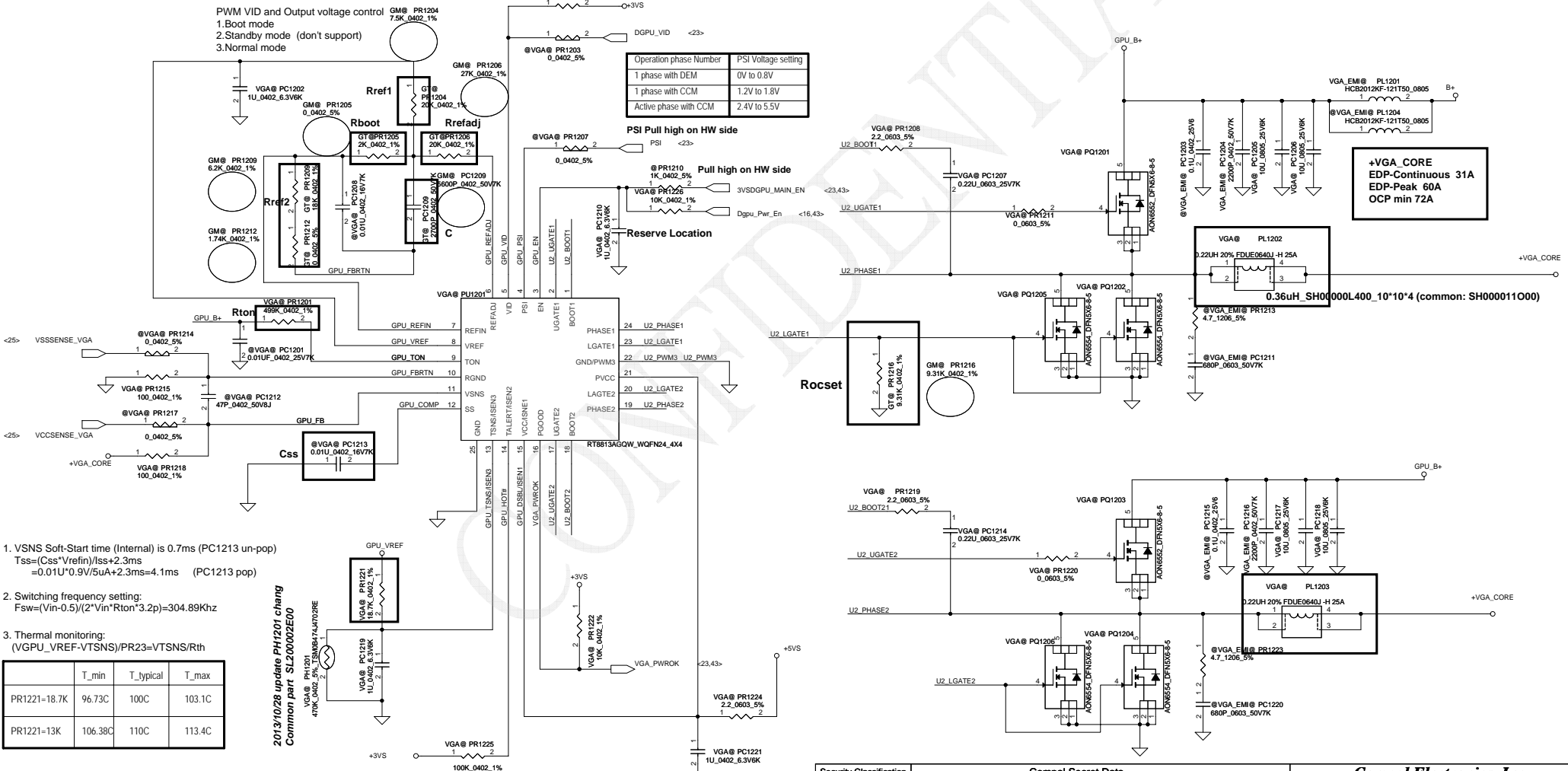
PWM-VID Spec	Config A	Config B	Config C	Config D
Vmin	0.6V	0.6V	0.65V	0.9V
Vmax	1.2V	1.2V	1.15V	1.15V
Vboot	0.875V	0.9V	0.9V	1.028V
Voltage step	6.25mV	6.25mV	25mV	12.5mV
N of Voltage level	96	96	20	20
PWM Frequency	1.125	1.125	0.676	0.676
Rrefadj	PR1206 39K	20K	39K	27K
Rref1	PR1204 39K	20K	30K	7.5K
Rboot	PR1205 1.5K	2K	3K	0
Rref2=PR1209+PR1212	PR1209 30K	18K	24K	6.2K
	PR1212 1.5K	0	3K	1.74K
C	PC1209 1.5nf	2.7nf	1.8nf	5.6nf

H-side MOS:AON6552 L-side MOS:AON6554
Rds(on): 5.6mohm@Vgs=10V 3.2mohm@Vgs=10V
6.7mohm@Vgs=4.5V 3-3.8mohm@Vgs=4.5V
Id :20A@Ta=25 degC Id :85A@Ta=25 degC

Choke: 0.36uH (Size:10*10*4)
Rdc=0.82mohm +-5%
Heat Rating Current=37A
Saturation Current=40A
C=3*330uF (9mohm)=990uF
Vripple=Iripple*ESR(min)=7.811A*3mohm=23.4mV

www.laptopblue.vn

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT	N15S-GT	N15V-GM
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config D
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W	18W	18.16W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W	25W	24.72W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A	31A	29.2A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A	60A	44.3A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A		
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A	72A	54A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K	13K	10.2K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L	2phase 1H1L	2phase 1H1L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)		
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL	GT@	GM@

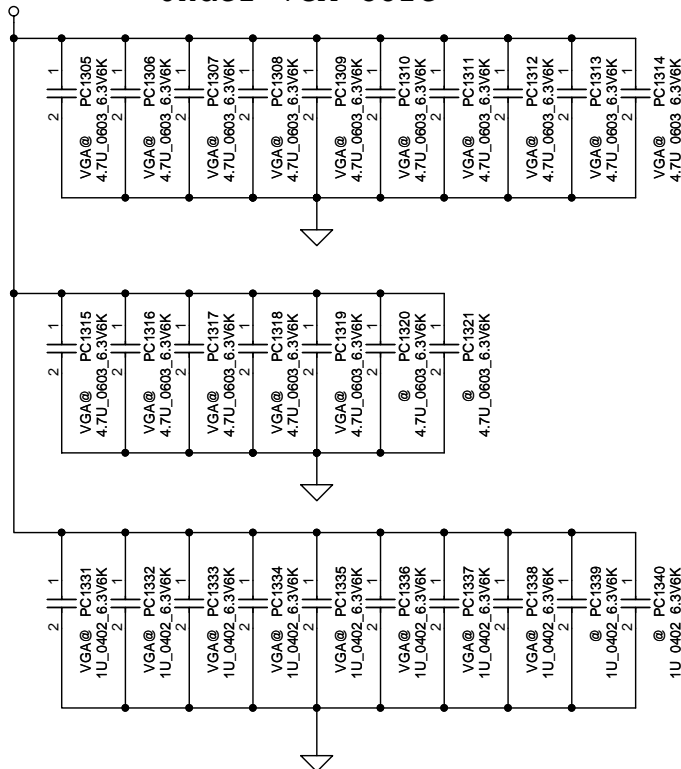


- VSNS Soft-Start time (Internal) is 0.7ms (PC1213 un-pop)
Tss=(Ccs*Vrefin)/Iss+2.3ms
=0.01u*0.9V/5uA+2.3ms=4.1ms (PC1213 pop)
- Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=304.89KHz
- Thermal monitoring:
(VGPU_VREF-VTSNS)/PR23=VTSNS/Rth

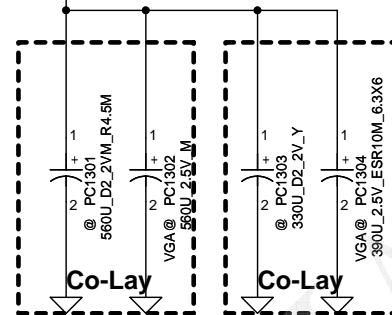
	T_min	T_typical	T_max
PR1221=18.7K	96.73C	100C	103.1C
PR1221=13K	106.38C	110C	113.4C

2013/10/28 update PH1201 change
Common part SL20002E00

+VGA_CORE Under VGA Core



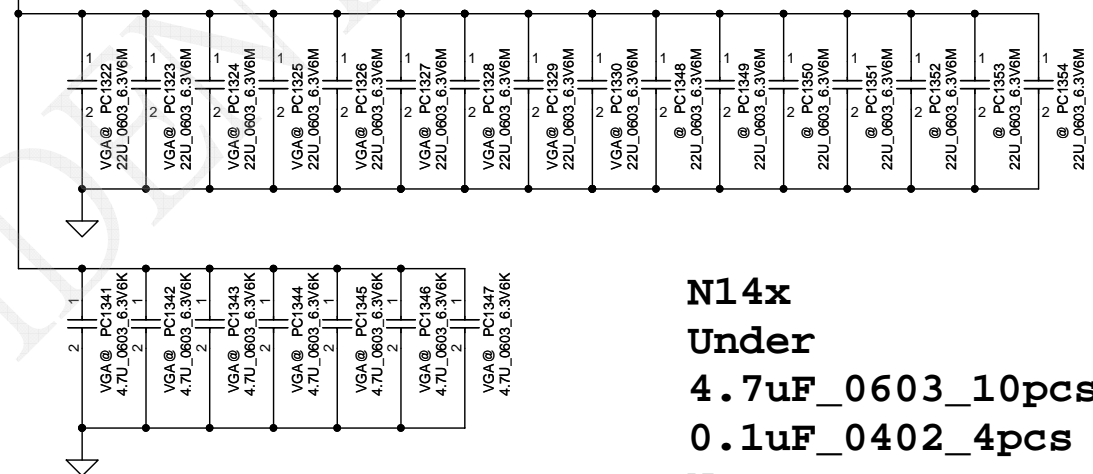
+VGA_CORE



N15x
Under
4.7uF_0603_15pcs stuff 2
1uF_0402_8pcs stuff 2
Near
47uF_0805_0pcs
22uF_0805_14pcs stuff 7
4.7uF_0805_5pcs stuff 2

+VGA_CORE

Near VGA Core



N14x
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1		Reduce 0 ohm count		Change PR510, PR602, PR607, PR809, PR816, PR820 to R-short	4/1	DVT
2	HW request	Change VRAM voltage to raise VRAM sequence	53	Change PR1006 to SD034240280	4/1	DVT
3		Improve CPU transient	51	Change PR818 to SD034976280	4/1	DVT
4		Reduce 0 ohm count		Change PR601, PR1001, PR1003, PR1008 to R-short	5/2	PVT
5		Component PN from M0 to 80	51	Change PC820 PN from SE0000006M0 to SE000000680	5/5	PVT
6		CPU low-side MOS selete	51	PQ804, PQ806, PQ808 from AON6414 change to AON6508	5/5	PVT
7		CPU TAT show VR thermal Alrt	51	change PR819 from 3.42K to 5.62K (active from 96'C to 106'C)	5/12	PVT
8		slewrate from ULV change to SV	51	PR808 from 16.9K to 3.24K (from 53mV/us to 12mV/us)	5/12	PVT
9		CPU low-side MOS selete	51	PQ804, PQ806, PQ808 from AON6508 change to AON6554	5/15	PVT MEMO
10		Thermal team change PH1 setting	45	PR216 from 16.9K to 26.1K (92'C active change to 85'C active)	5/15	PVT MEMO
12						
13						
14						
15						
16						
17						

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