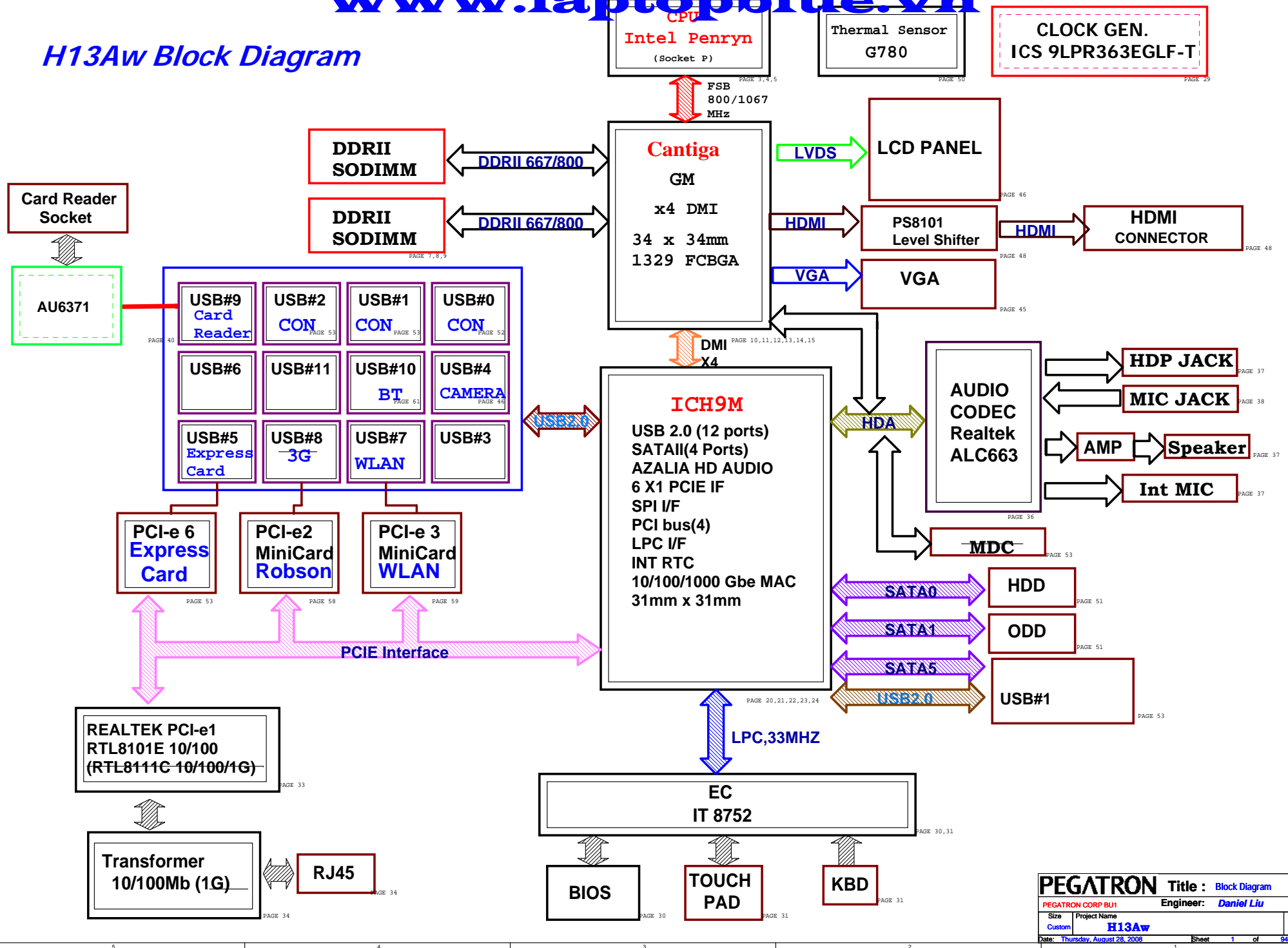
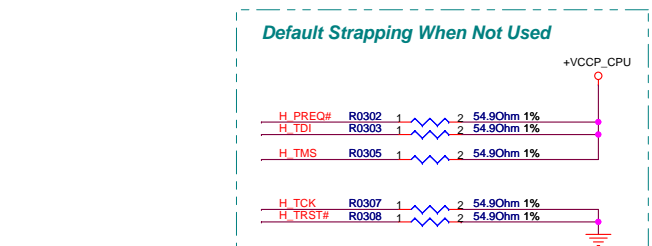
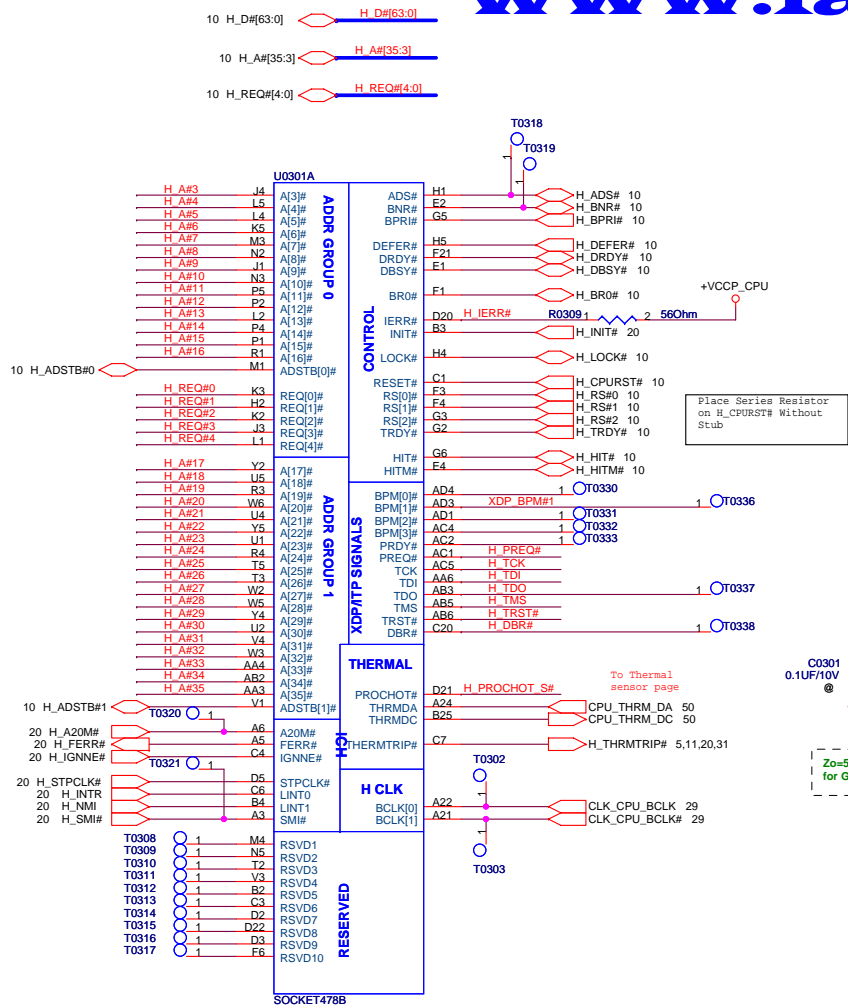
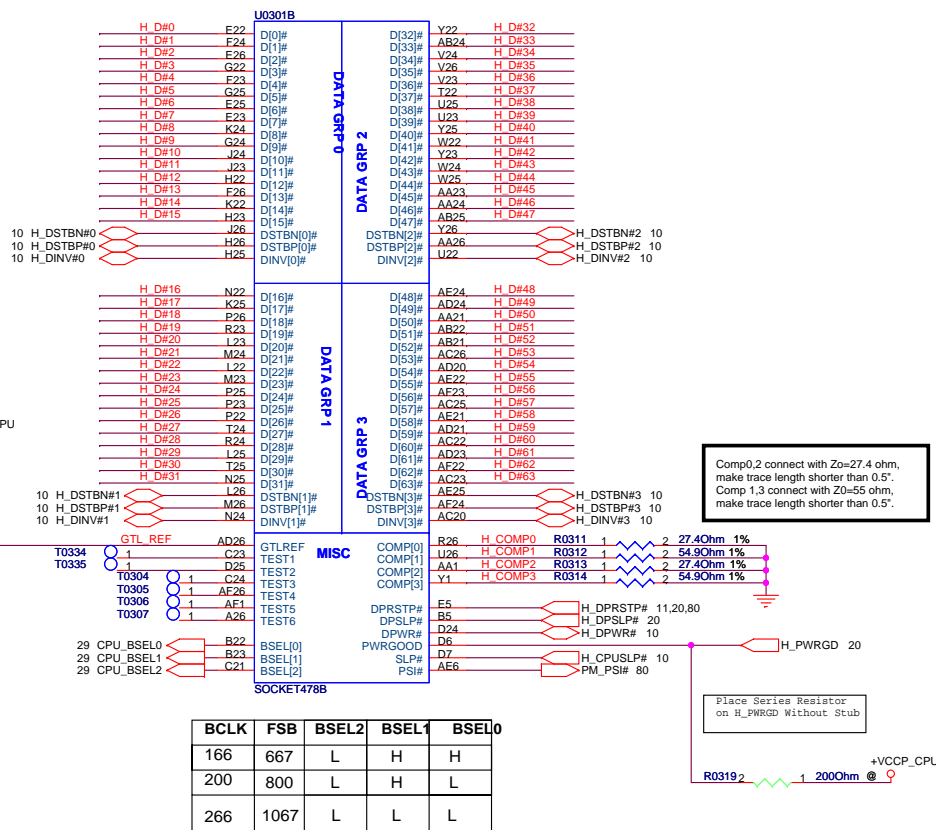


H13Aw Block Diagram

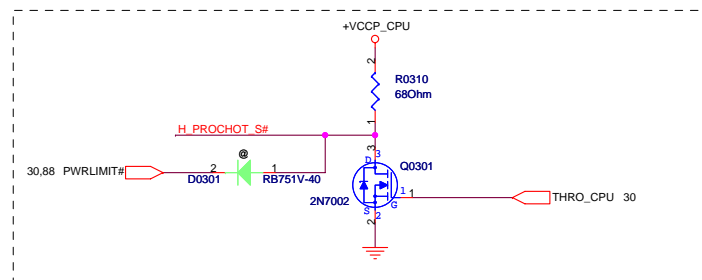


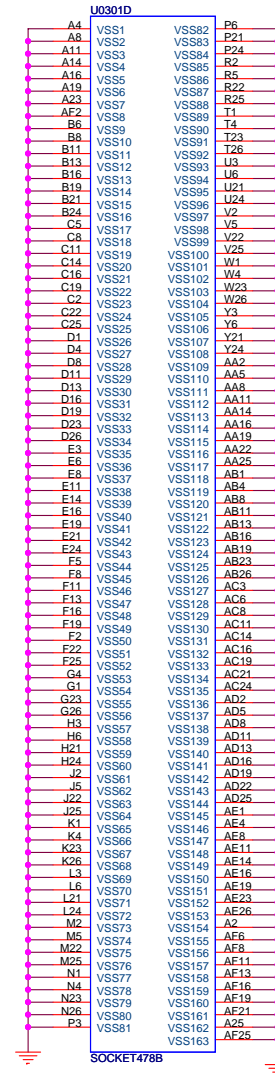
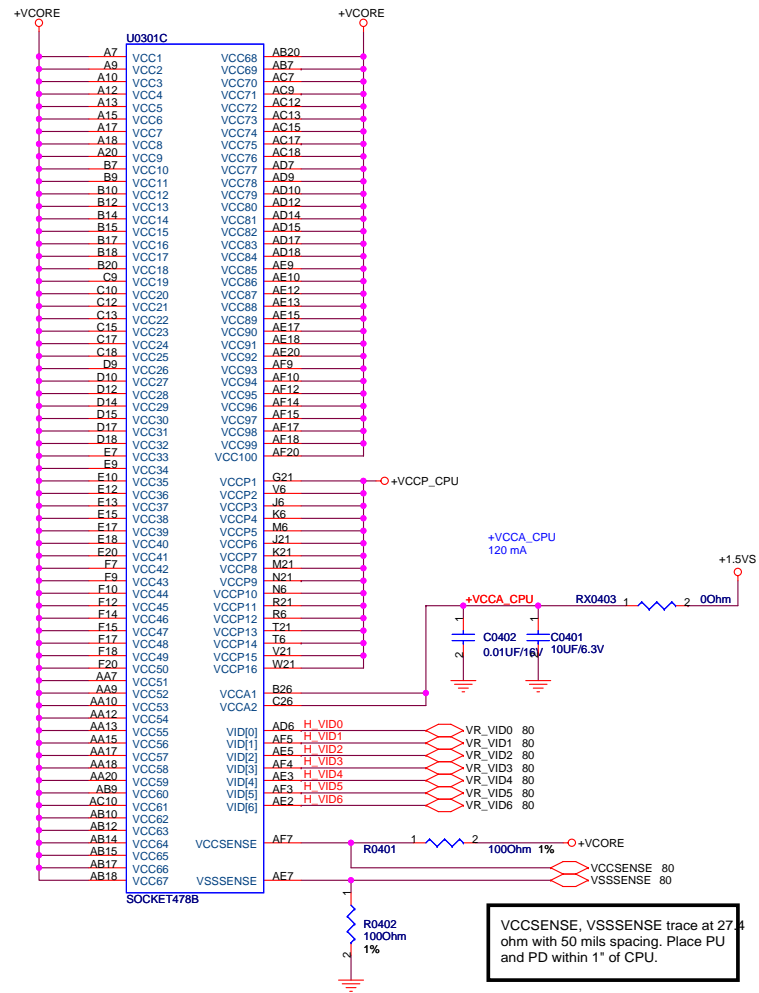


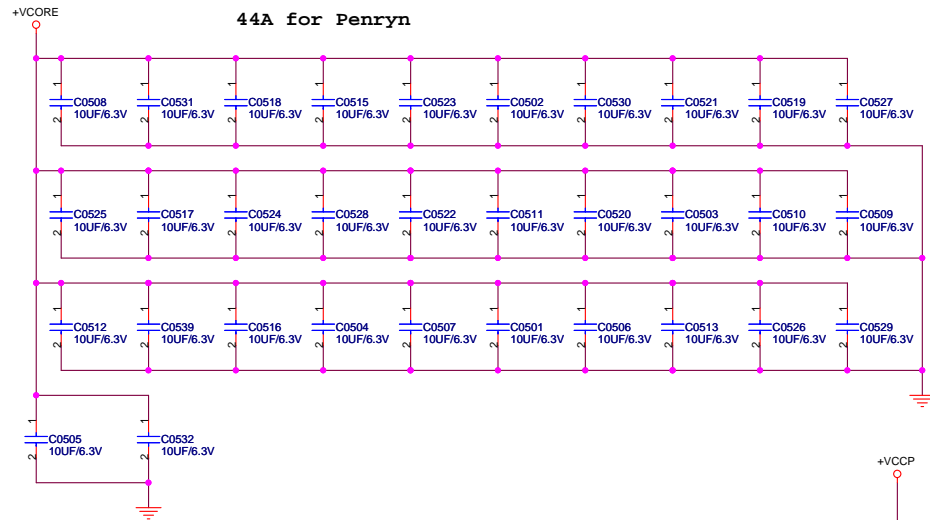
Place R0304 & R0306 for XDP function



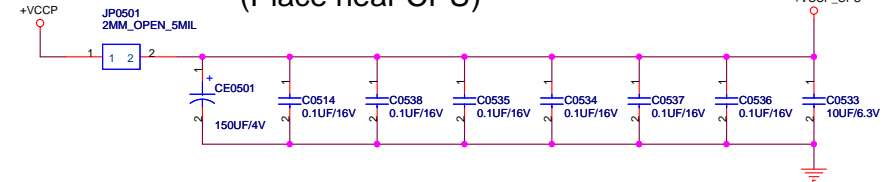
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L





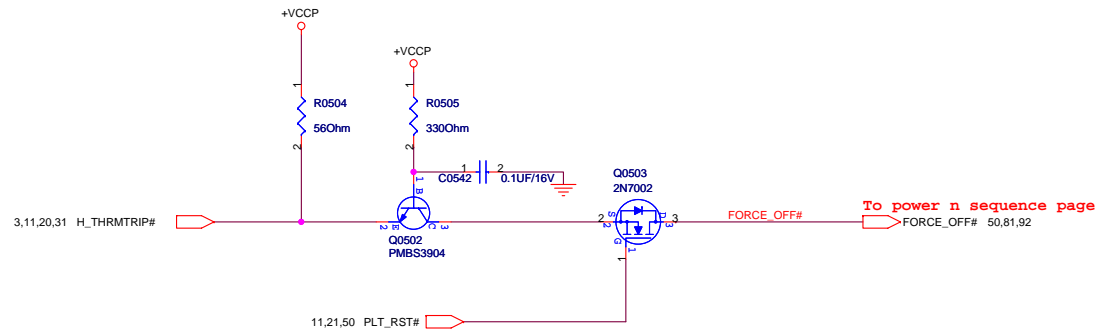


+VCCP Decoupling Capacitor (Place near CPU)



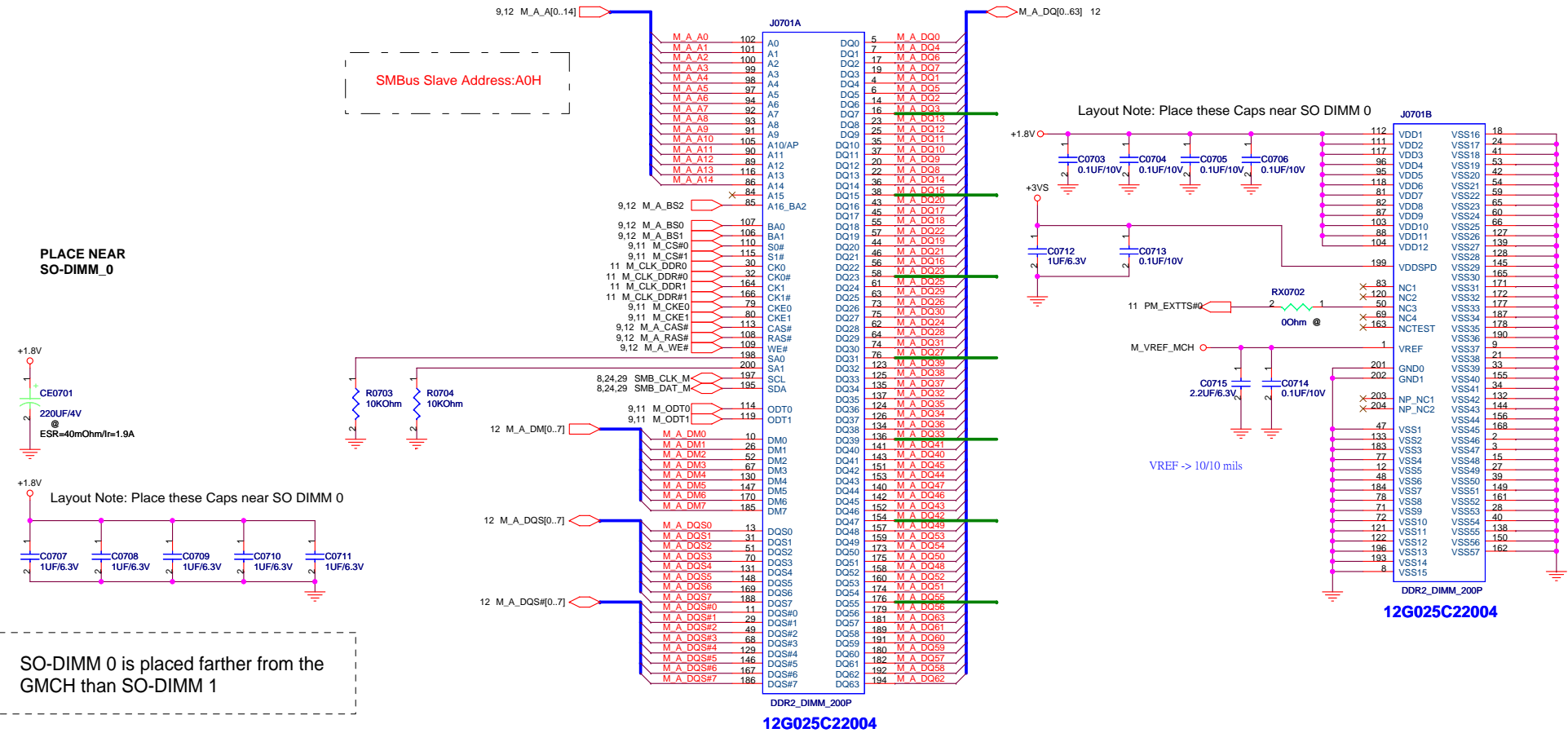
Decoupling guide from INTEL

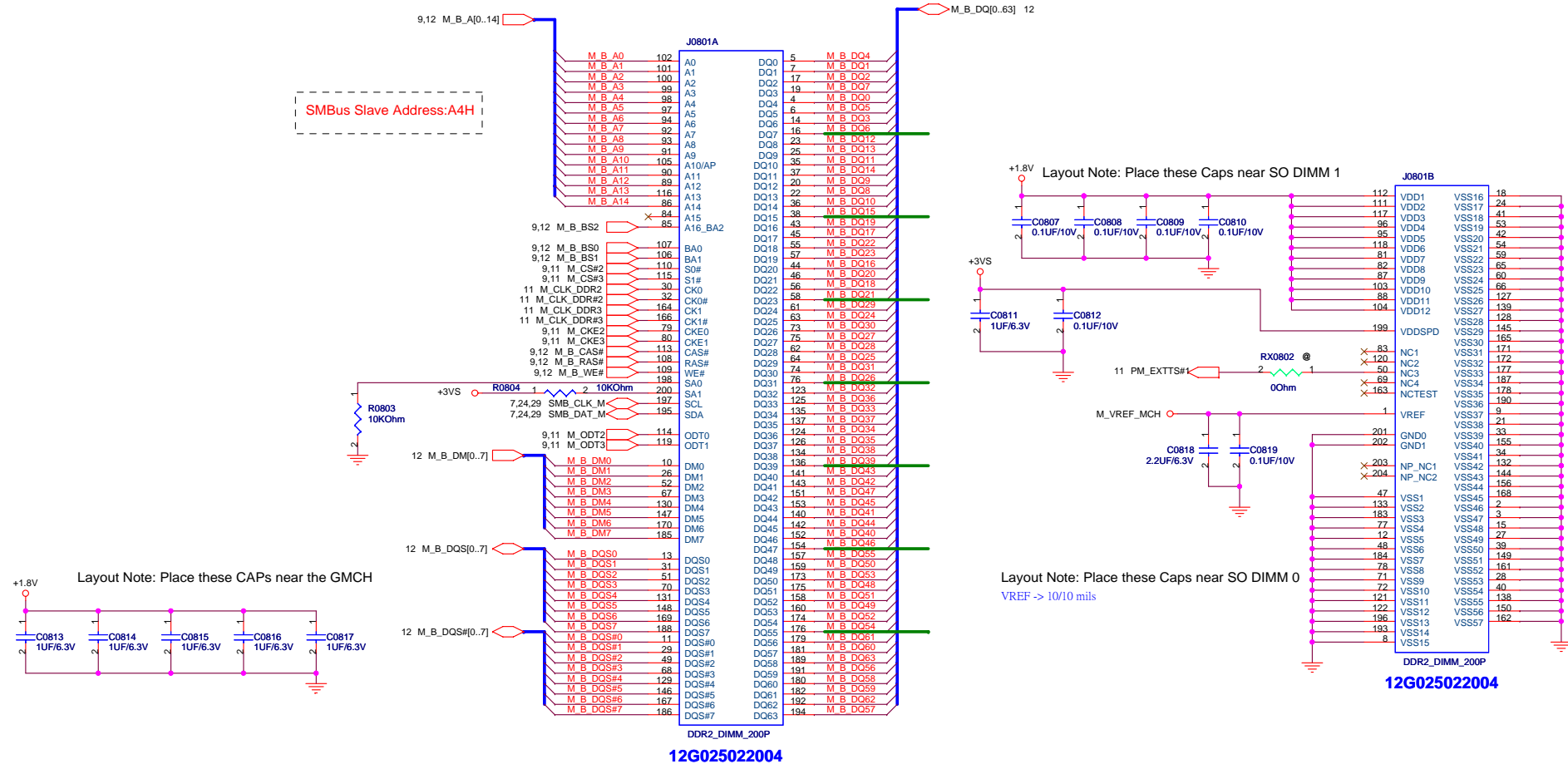
VCORE	22uF/10V or 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

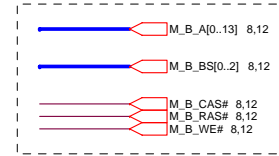
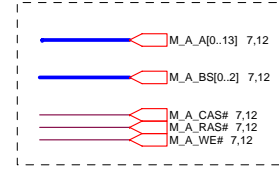
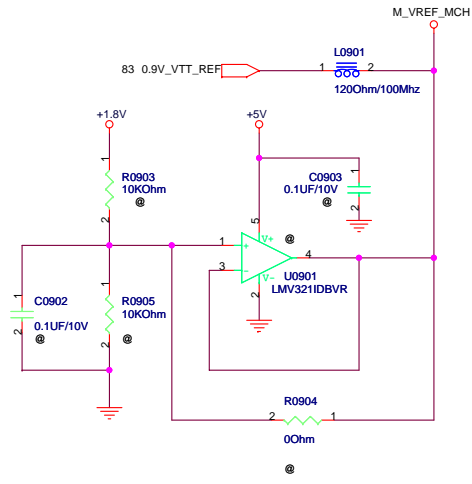


Thermal Trip signal(From CPU to ICH-9M and sequence)

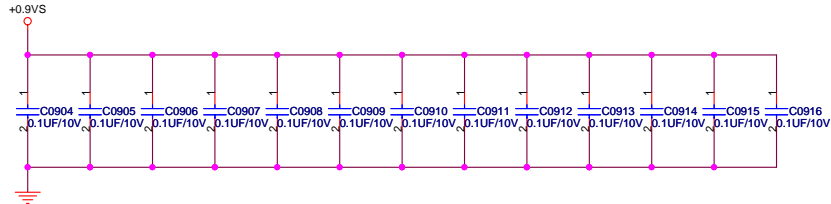
PEGATRON		Title :	
PEGATRON CORP BU1		Engineer: Daniel Liu	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: Thursday, August 28, 2008		Sheet	6 of 94



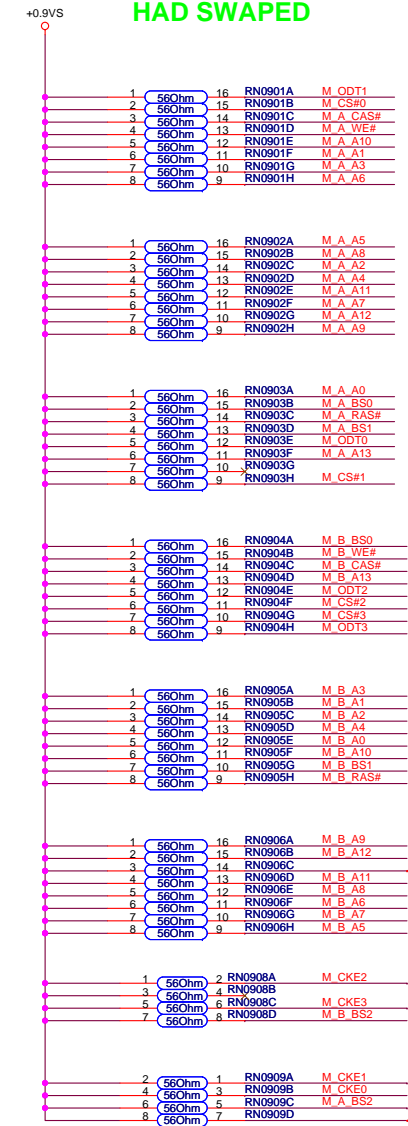
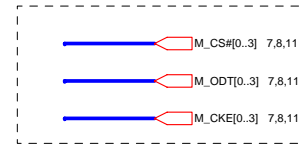
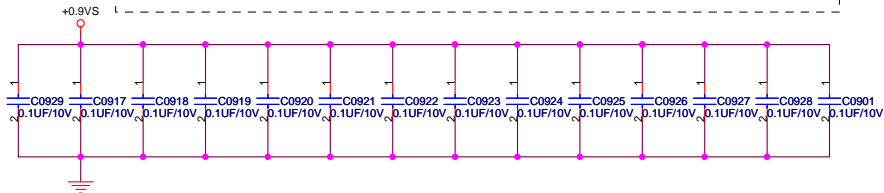


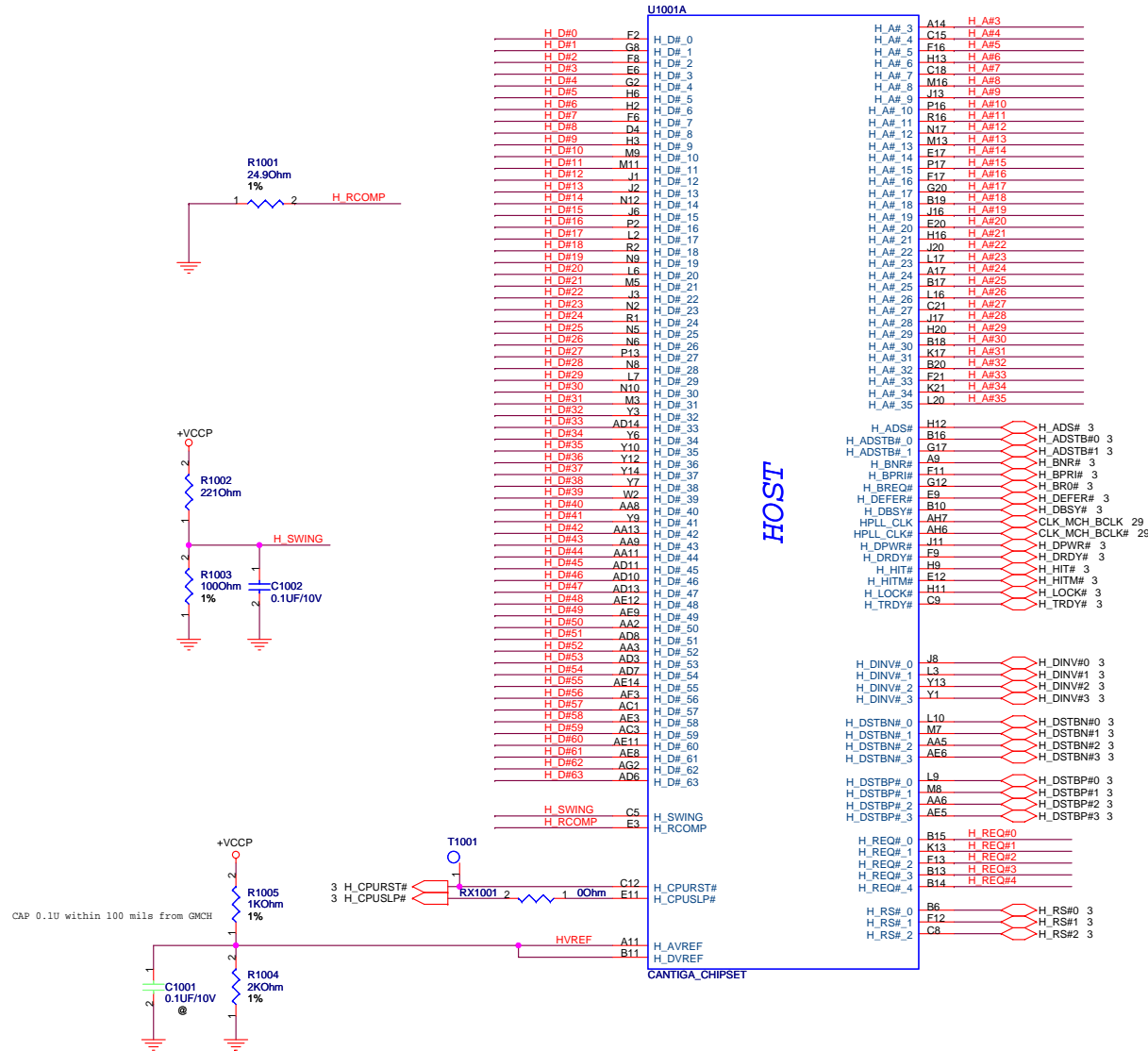


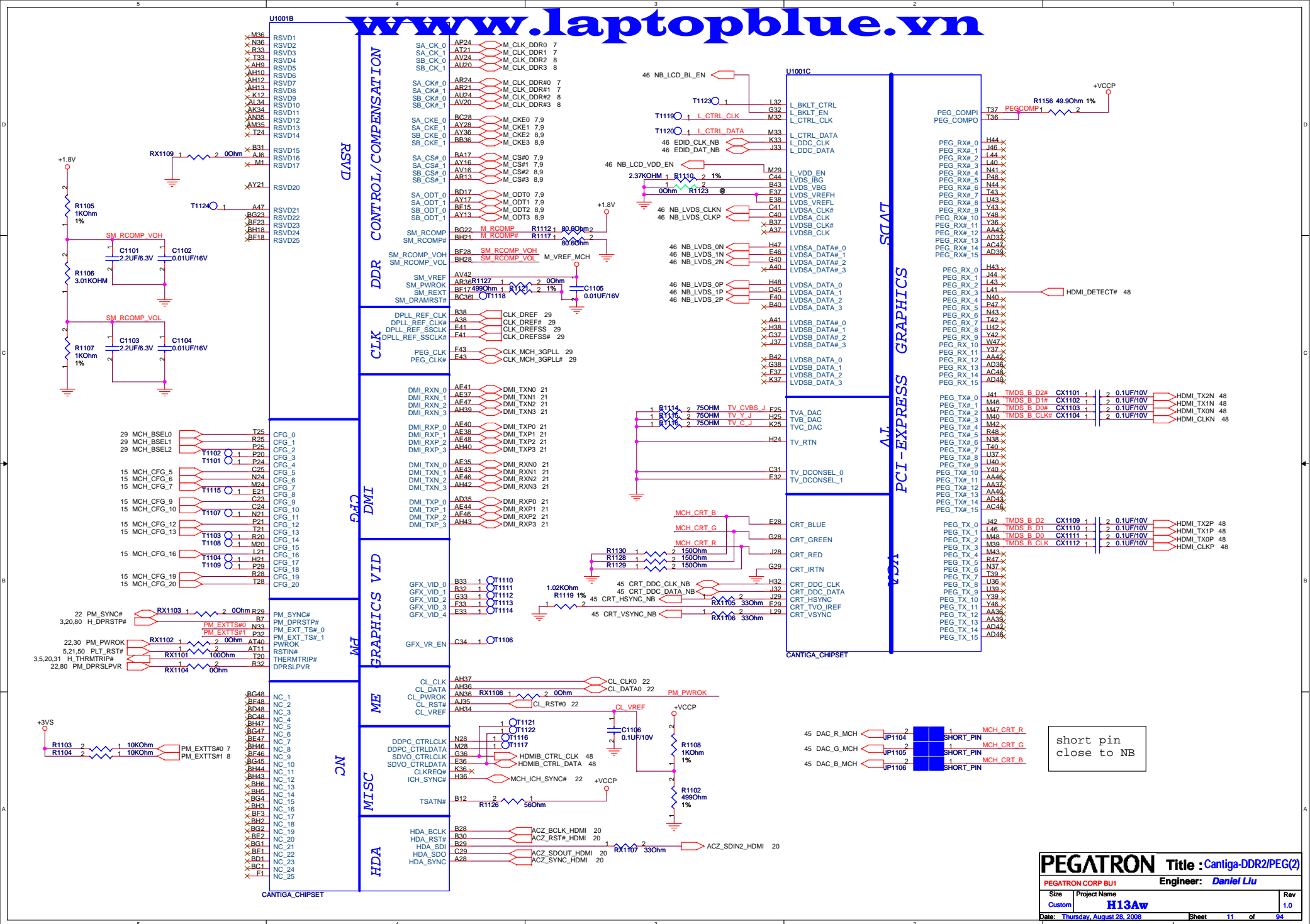
If system doesn't support iAMT, termination power rail should be +0.9VS.

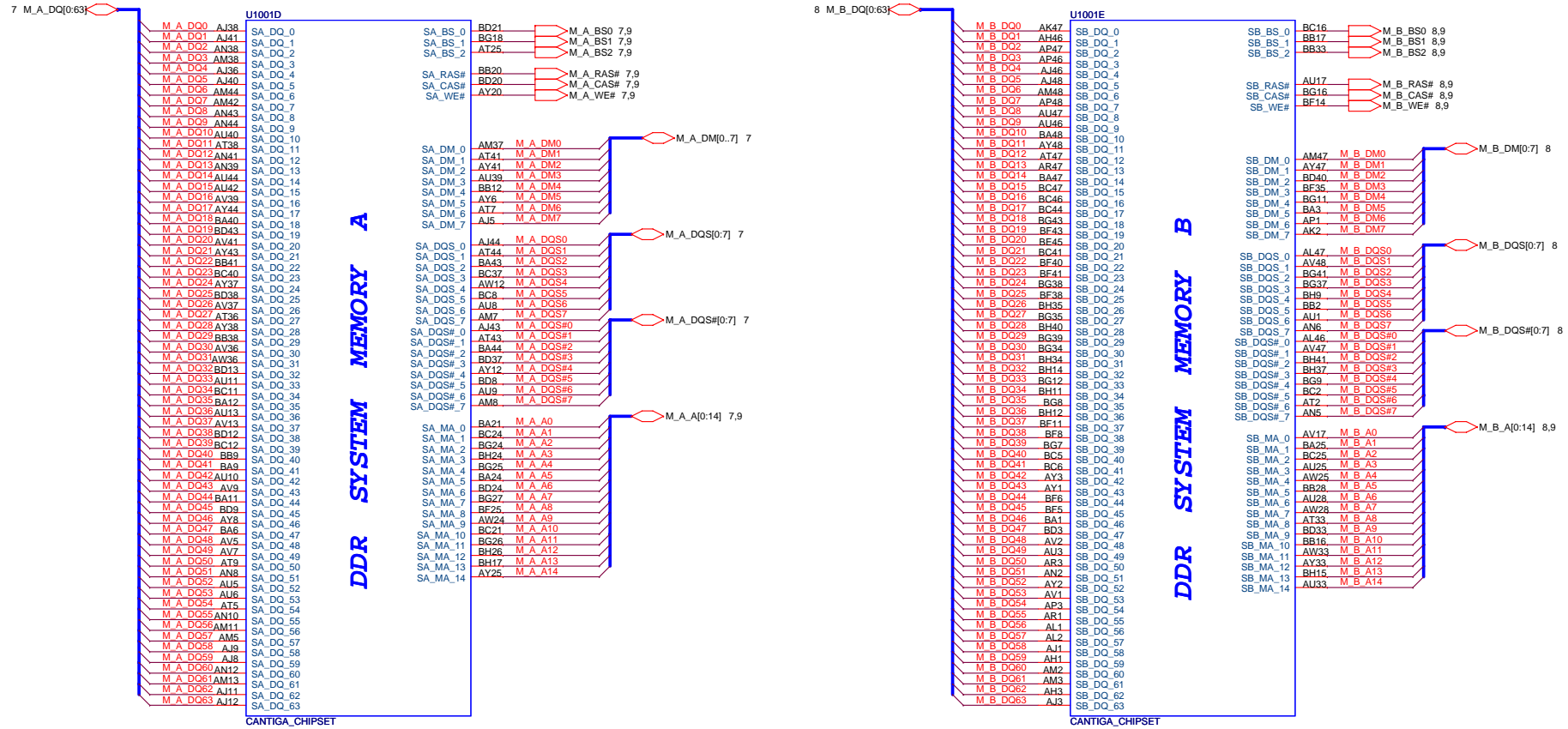


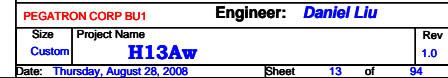
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

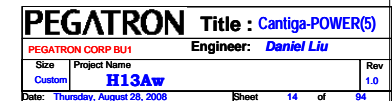


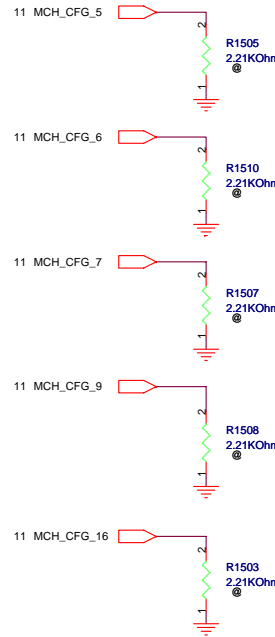
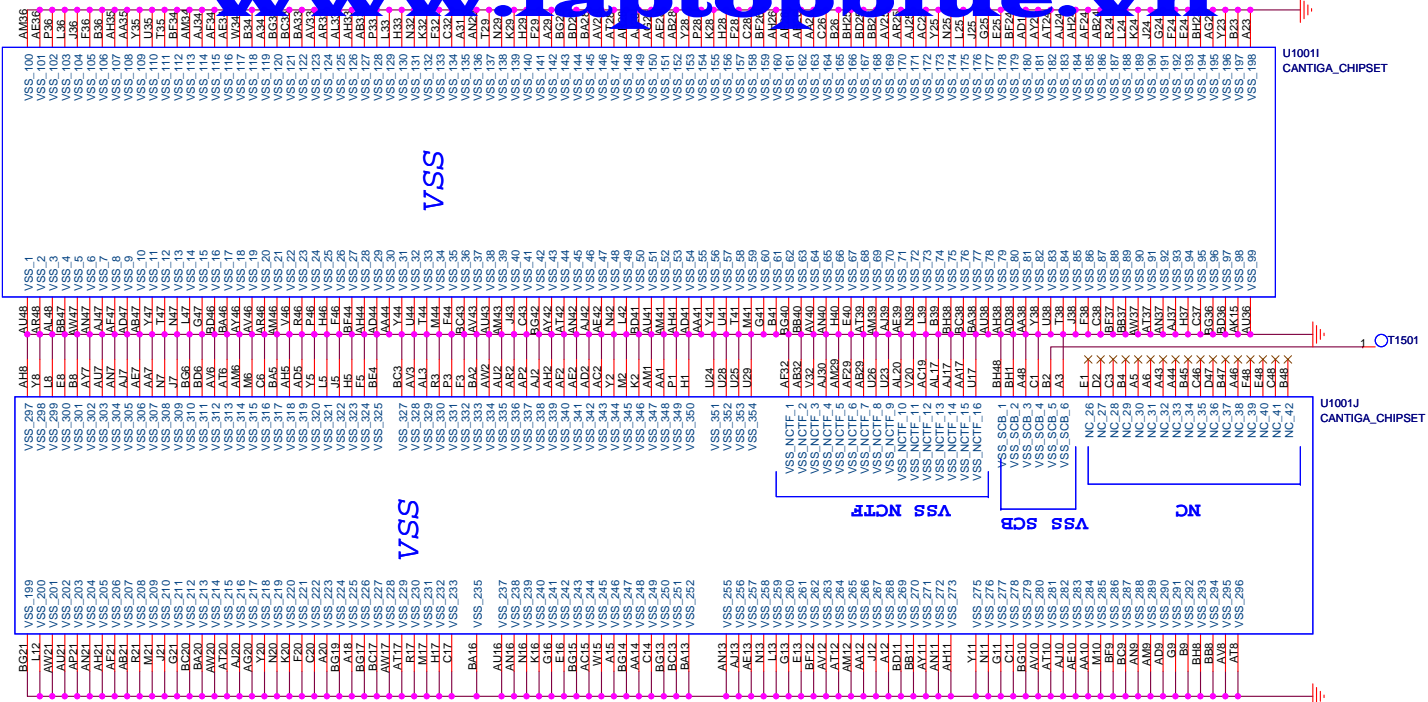












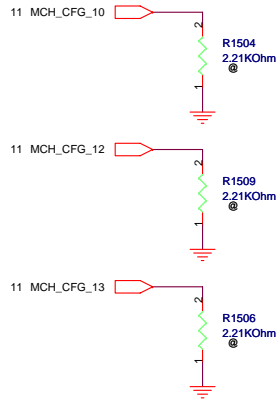
CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality

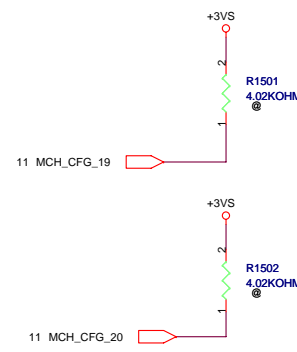
CFG9 : PCIE GRAPHIC LANE
LOW = Reverse Lanes
HIGH = Normal Operation (Default)

CFG16 : FSB Dynamic ODT
HIGH = Enable (Default)
LOW = Disable



CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)



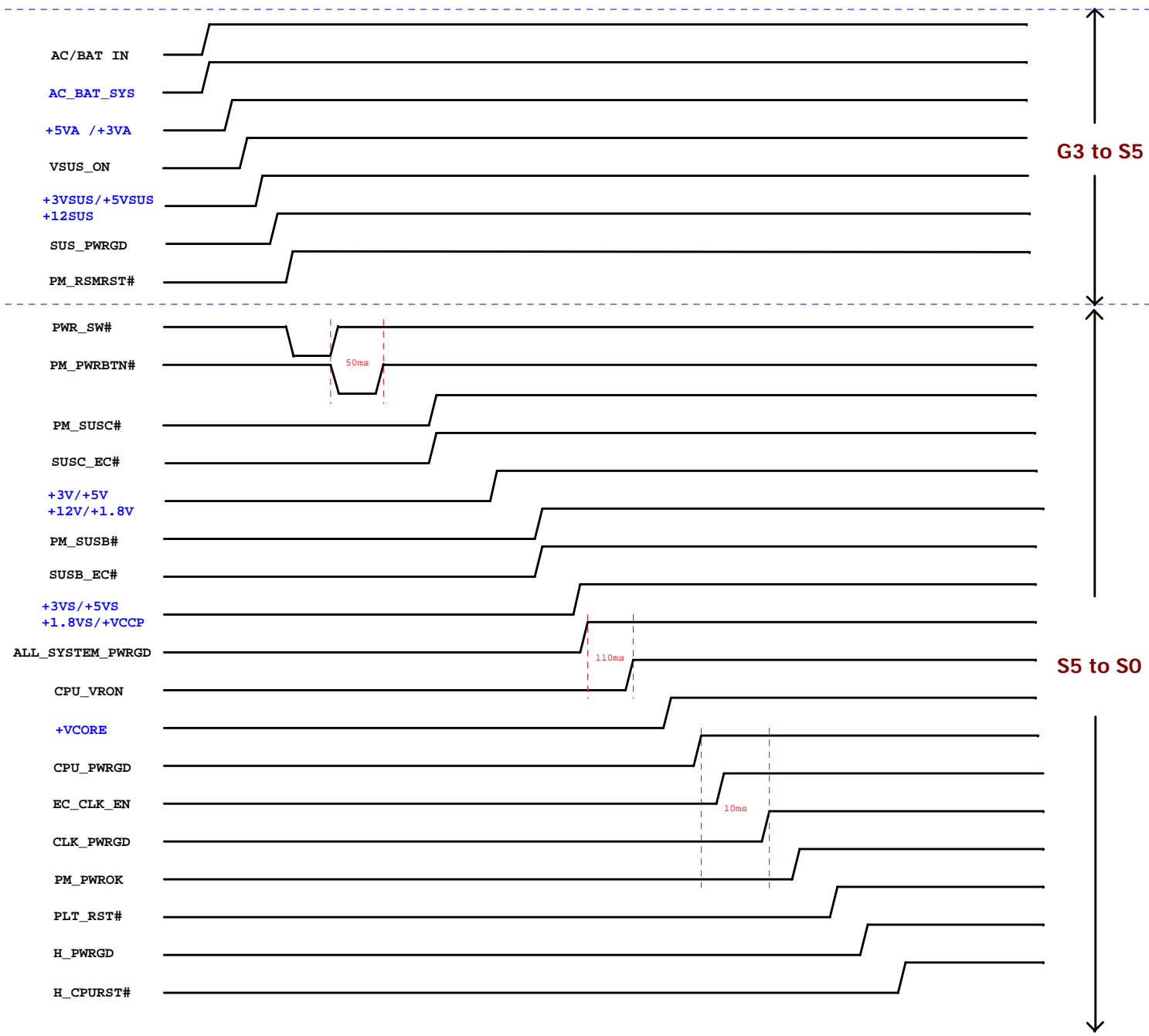
CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes

CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

PEGATRON		Title :	
PEGATRON CORP BU1		Engineer: <i>Daniel Liu</i>	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: <i>Thursday, August 28, 2008</i>		Sheet	16 of 94

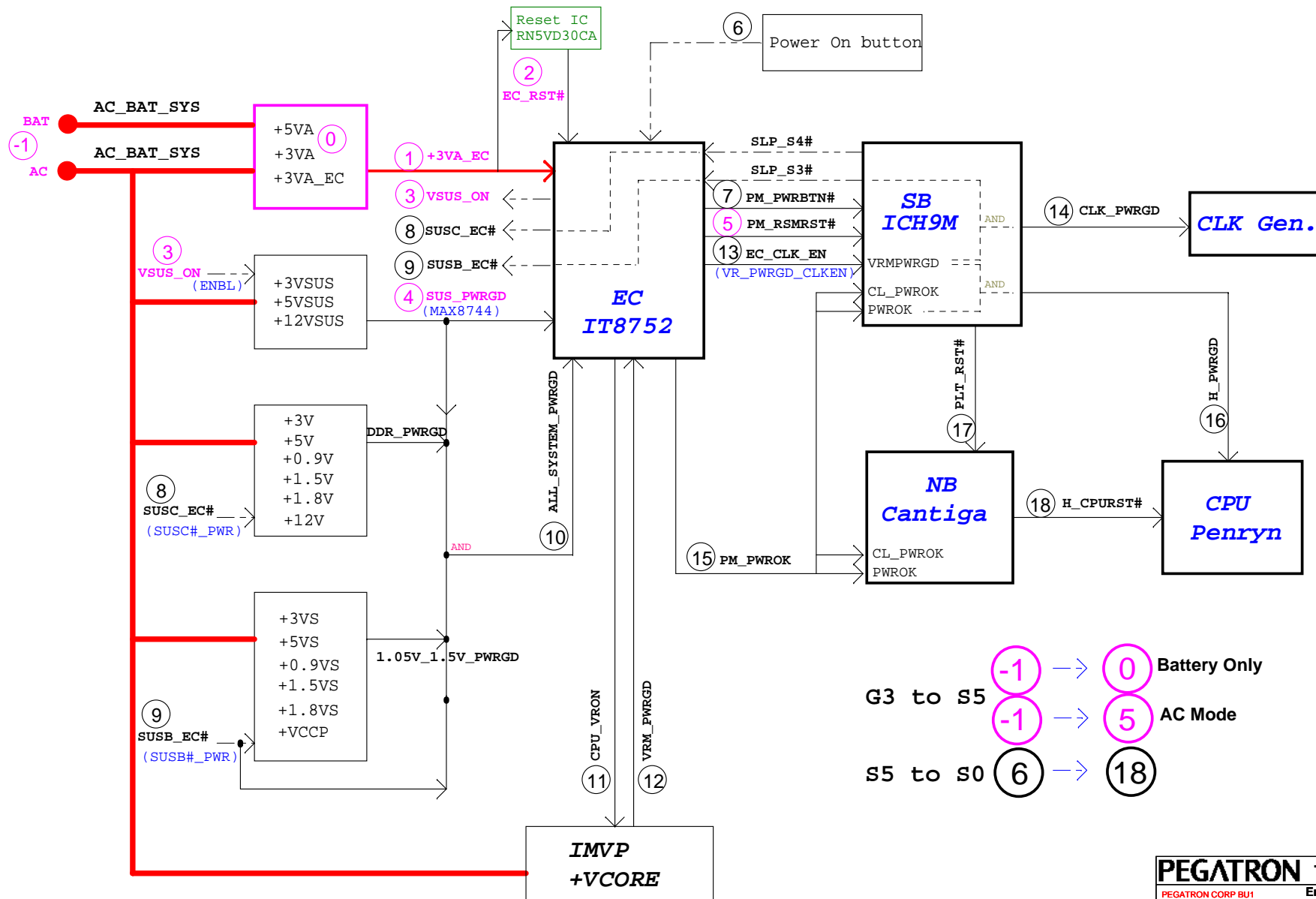
PEGATRON		Title :	
PEGATRON CORP BU1		Engineer: <i>Daniel Liu</i>	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: <i>Thursday, August 28, 2008</i>		Sheet	17 of 94

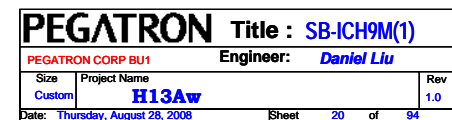
Power On Sequence

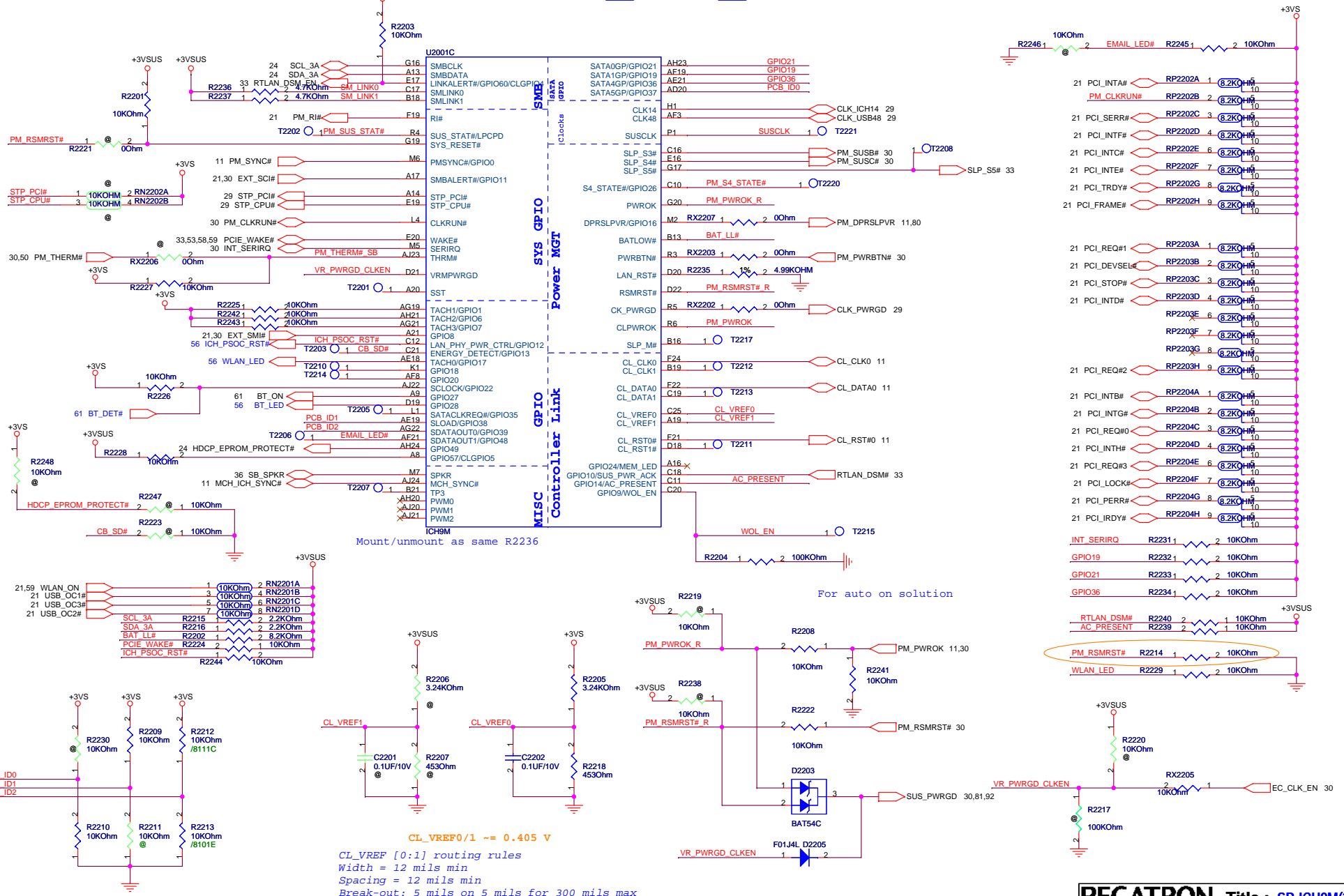


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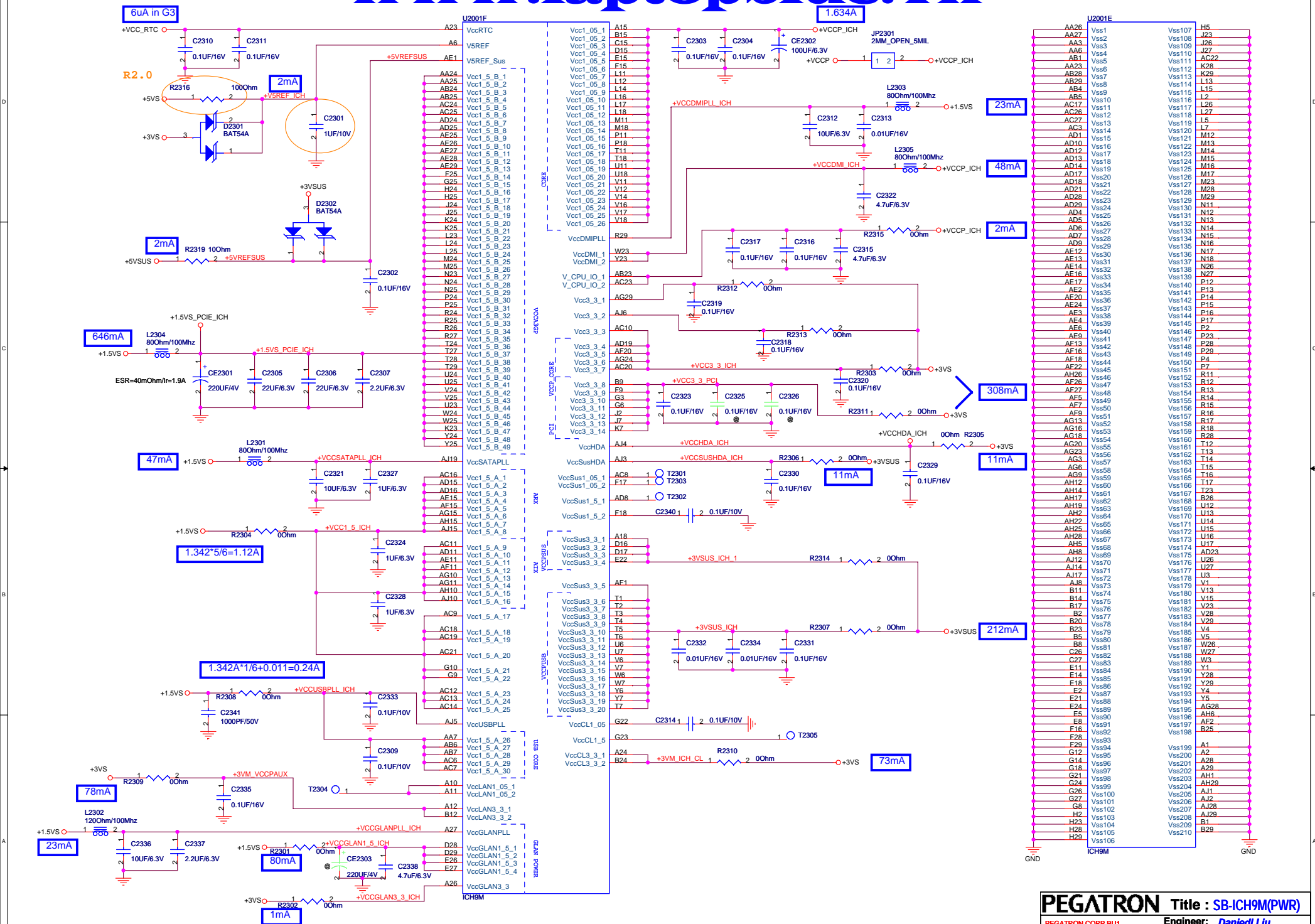
Power On Sequence



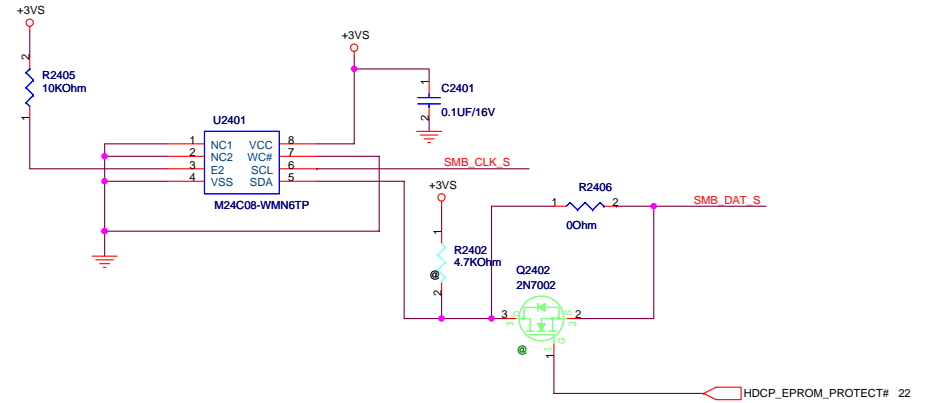
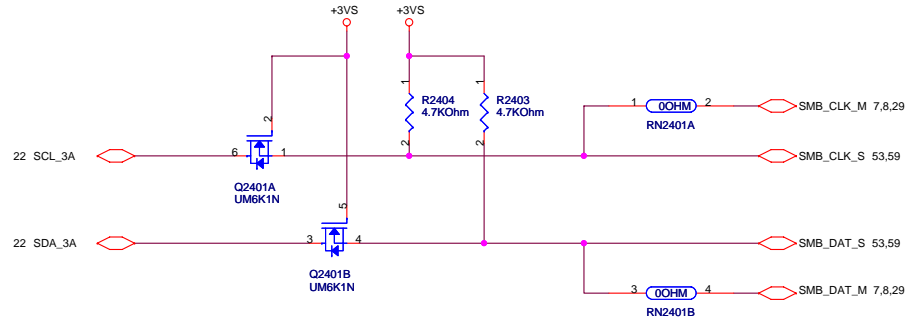




Giga Lan ->GPIO39 :1, GPIO38:1
;10/100 Lan->GPIO39:0,
GPIO38:1(03/31/2008)



ICH9-M



EC

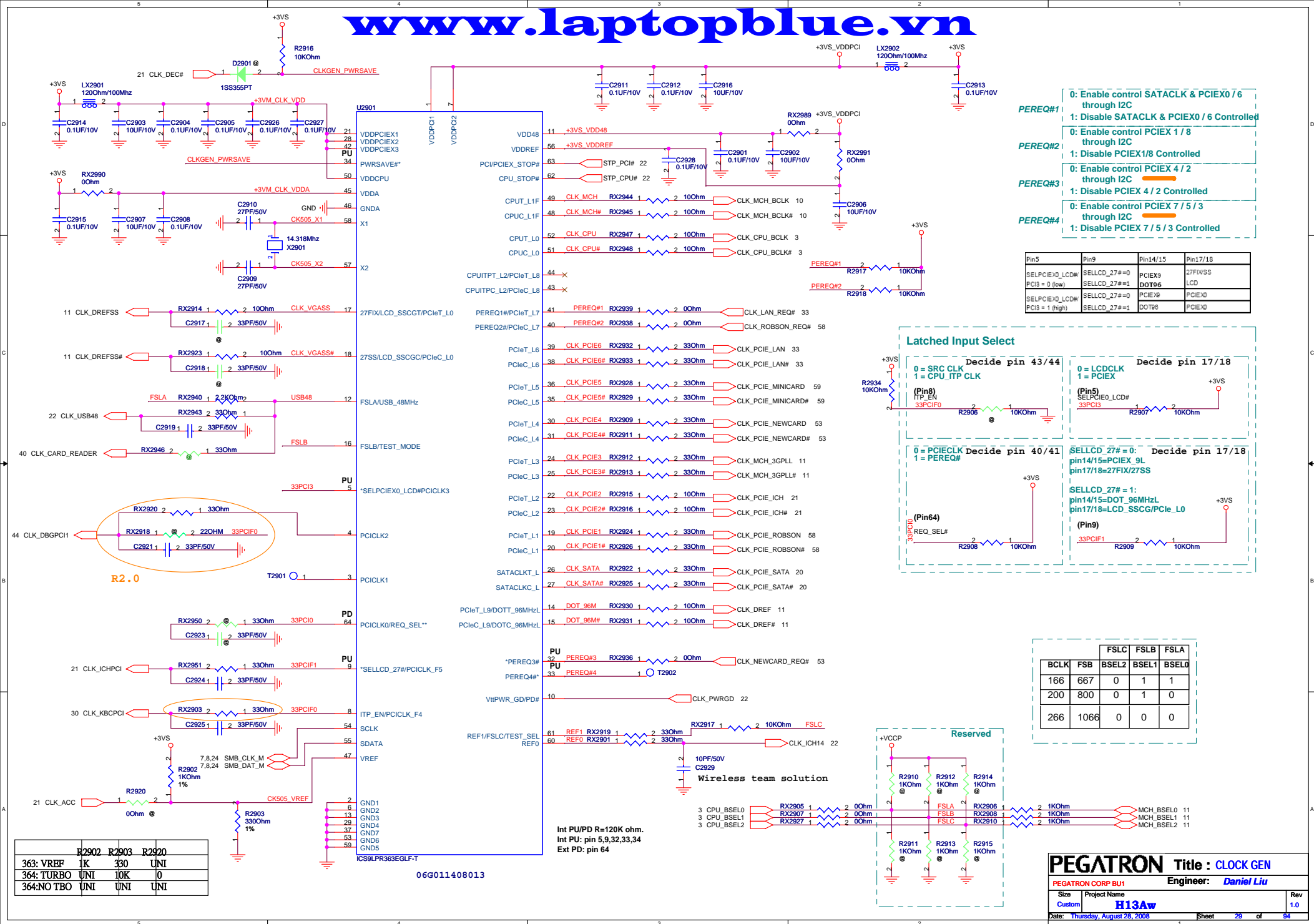
Master	Slave
SCL_3A SDA_3A (ICH9M)	A. SMB_CLK_S → WLAN Card ; New Card ; SMB_DAT_S → HDPC B. SMB_CLK_M → SO-DIMM0; SO-DIMM1; SMB_DAT_M → CLK Generator
SMB0_CLK SMB0_DAT (EC)	BATTERY
SMB1_CLK SMB1_DAT (EC)	A:Thermal Sensor Address: 98h (CPU) B:Volume Bar

PEGATRON		Title : SPI ROM	
PEGATRON CORP BU1		Engineer: Daniel Liu	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: Thursday, August 28, 2008		Sheet	25 of 94

PEGATRON		Title :	
PEGATRON CORP BU1		Engineer: <i>Daniel Liu</i>	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: <i>Thursday, August 28, 2008</i>		Sheet	26 of 94

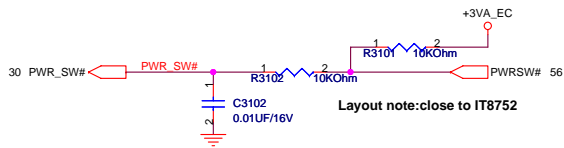
PEGATRON		Title :	
PEGATRON CORP BU1		Engineer: Daniel Liu	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: Thursday, August 28, 2008		Sheet	27 of 94

PEGATRON		Title :	
PEGATRON CORP BU1		Engineer: Daniel Liu	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: Thursday, August 28, 2008		Sheet	28 of 94

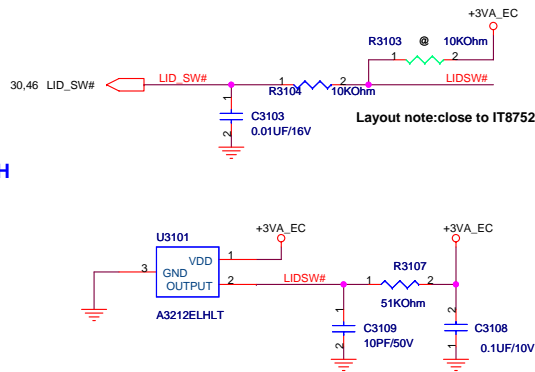


T/P

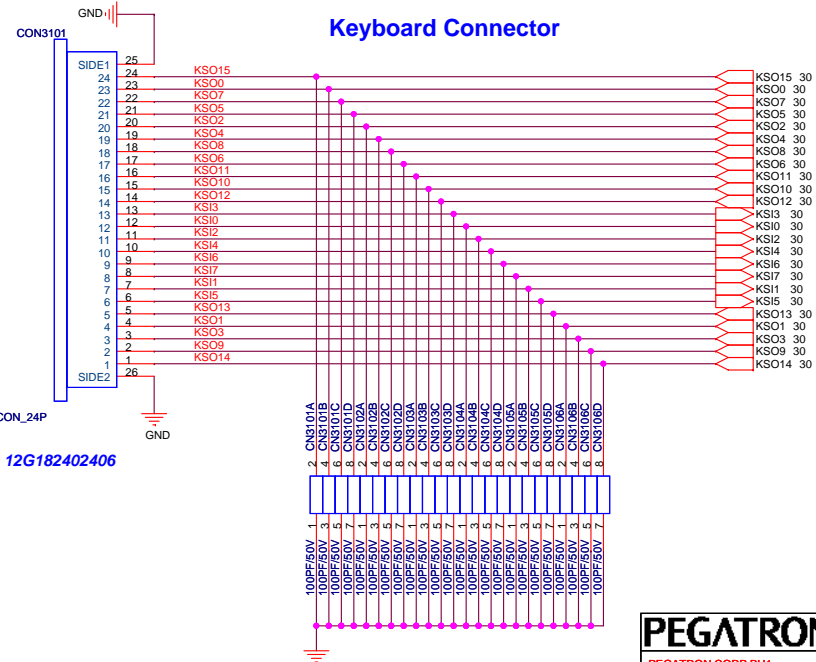
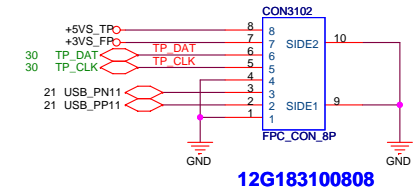
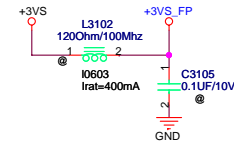
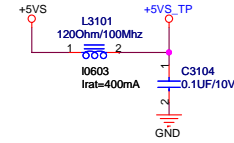
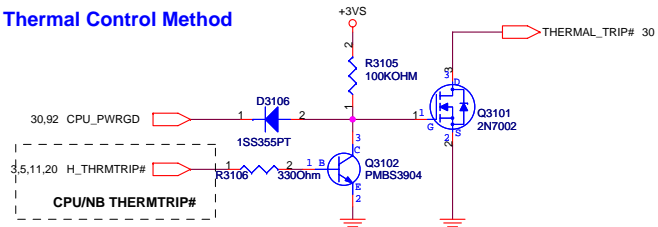
PWR SWITCH

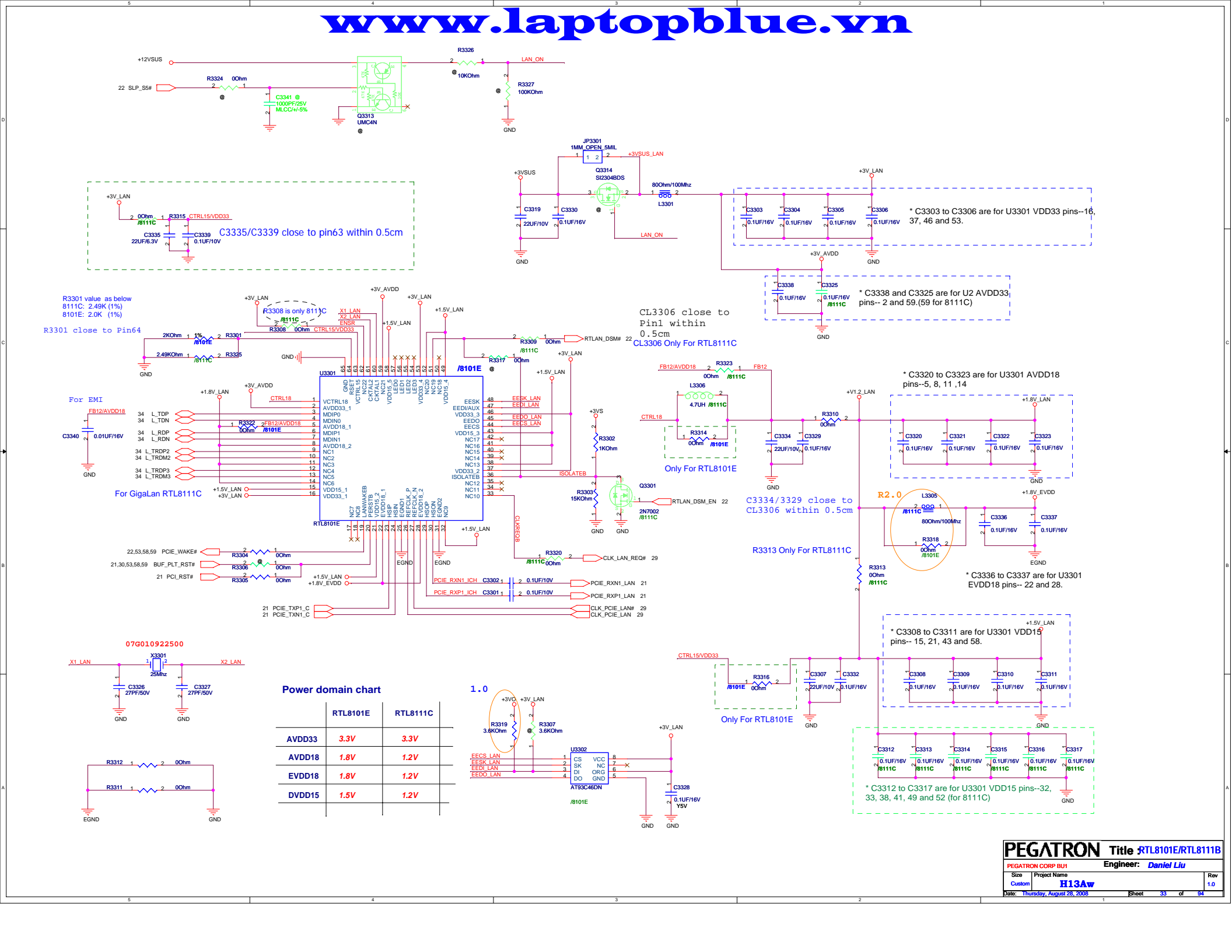


LID SWITCH



For Thermal Control Method





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12V_{SUS}

22 SLP_55#

R3324 00hm

R3341 1000PF/25V MLCC±4%±5%

Q3313 UMICAN

R3326 10KOhm

R3327 100KOhm

LAN_ON

3V_{LAN}

R3315 CTRL15/VDD33

R3316 00hm

C3335 22UF/16V

C3339 0.1UF/10V

C3335/C3339 close to pin63 within 0.5cm

3V_{SUS}

JP3301 1MM_OPEN_5MIL

Q3314 SI2304BDS

800hm/100Mhz

L3301

3V_{LAN}

C3319 22UF/10V

C3330 0.1UF/16V

LAN_ON

3V_{LAN}

C3303 0.1UF/16V

C3304 0.1UF/16V

C3305 0.1UF/16V

C3306 0.1UF/16V

* C3303 to C3306 are for U3301 VDD33 pins--16, 37, 46 and 53.

3V_{AVDD}

C3338 0.1UF/16V

C3325 0.1UF/16V

* C3338 and C3325 are for U2 AVDD33 pins-- 2 and 59.(59 for 8111C)

CL3306 close to Pin1 within 0.5cm

CL3306 Only For RTL8111C

R3301 close to Pin64

R3301 value as below

8111C: 2.49K (1%)

8101E: 2.0K (1%)

2KOhm 1% /8101E

2.49KOhm /8111C

R3301

3V_{LAN}

R3308 00hm

R3309 00hm

R3310 00hm

R3311 00hm

R3312 00hm

R3313 00hm

R3314 00hm

R3315 00hm

R3316 00hm

R3317 00hm

R3318 00hm

R3319 00hm

R3320 00hm

R3321 00hm

R3322 00hm

R3323 00hm

R3324 00hm

R3325 00hm

R3326 00hm

R3327 00hm

R3328 00hm

R3329 00hm

R3330 00hm

R3331 00hm

R3332 00hm

R3333 00hm

R3334 00hm

R3335 00hm

R3336 00hm

R3337 00hm

R3338 00hm

R3339 00hm

R3340 00hm

R3341 00hm

R3342 00hm

R3343 00hm

R3344 00hm

R3345 00hm

R3346 00hm

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R3355 00hm

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R3365 00hm

R3366 00hm

R3367 00hm

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R3369 00hm

R3370 00hm

R3371 00hm

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R3373 00hm

R3374 00hm

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R3377 00hm

R3378 00hm

R3379 00hm

R3380 00hm

R3381 00hm

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R3386 00hm

R3387 00hm

R3388 00hm

R3389 00hm

R3390 00hm

R3391 00hm

R3392 00hm

R3393 00hm

R3394 00hm

R3395 00hm

R3396 00hm

R3397 00hm

R3398 00hm

R3399 00hm

R3400 00hm

R3401 00hm

R3402 00hm

R3403 00hm

R3404 00hm

R3405 00hm

R3406 00hm

R3407 00hm

R3408 00hm

R3409 00hm

R3410 00hm

R3411 00hm

R3412 00hm

R3413 00hm

R3414 00hm

R3415 00hm

R3416 00hm

R3417 00hm

R3418 00hm

R3419 00hm

R3420 00hm

R3421 00hm

R3422 00hm

R3423 00hm

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R3425 00hm

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R3434 00hm

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R3500 00hm

R3501 00hm

R3502 00hm

R3503 00hm

R3504 00hm

R3505 00hm

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R3540 00hm

R3541 00hm

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R3548 00hm

R3549 00hm

R3550 00hm

R3551 00hm

R3552 00hm

R3553 00hm

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R3557 00hm

R3558 00hm

R3559 00hm

R3560 00hm

R3561 00hm

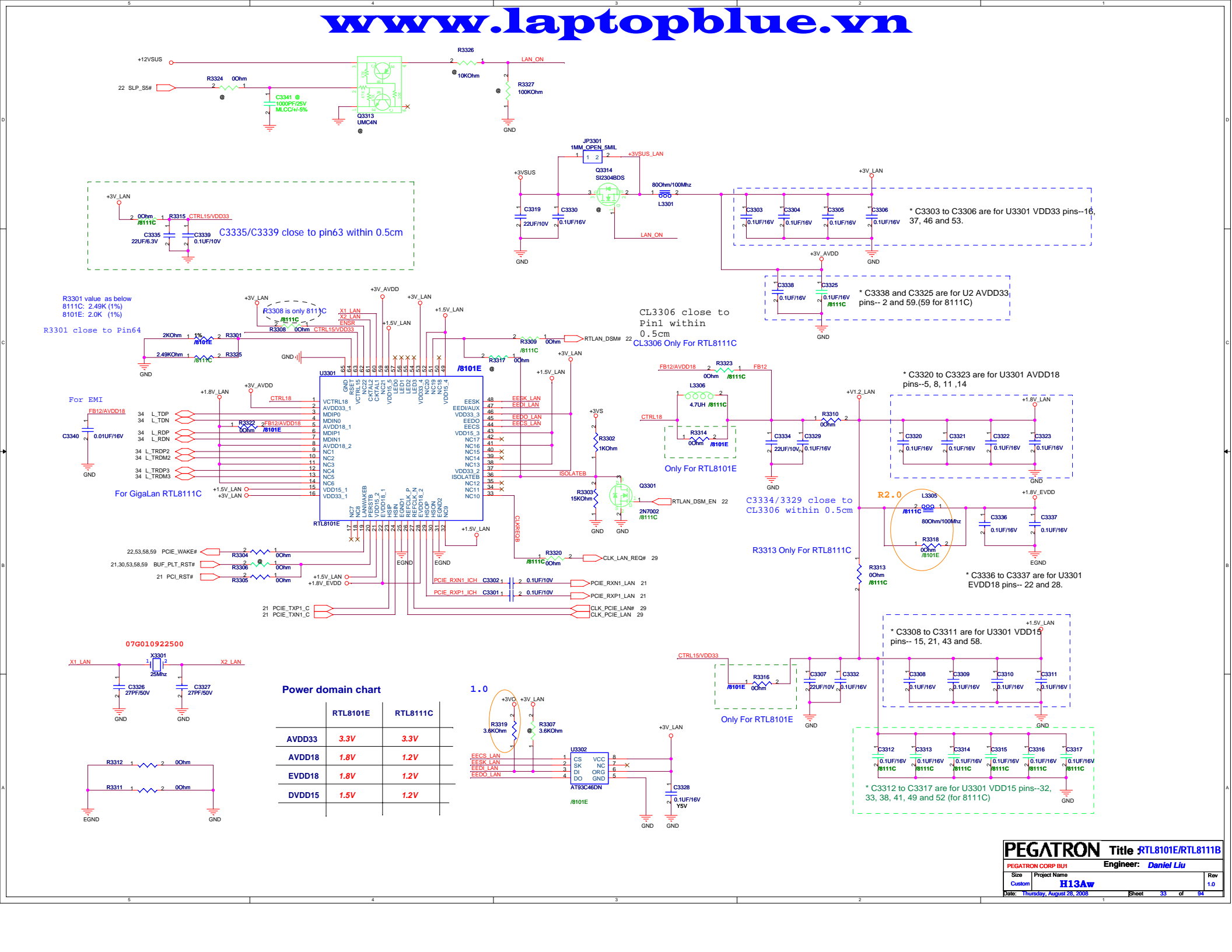
R3562 00hm

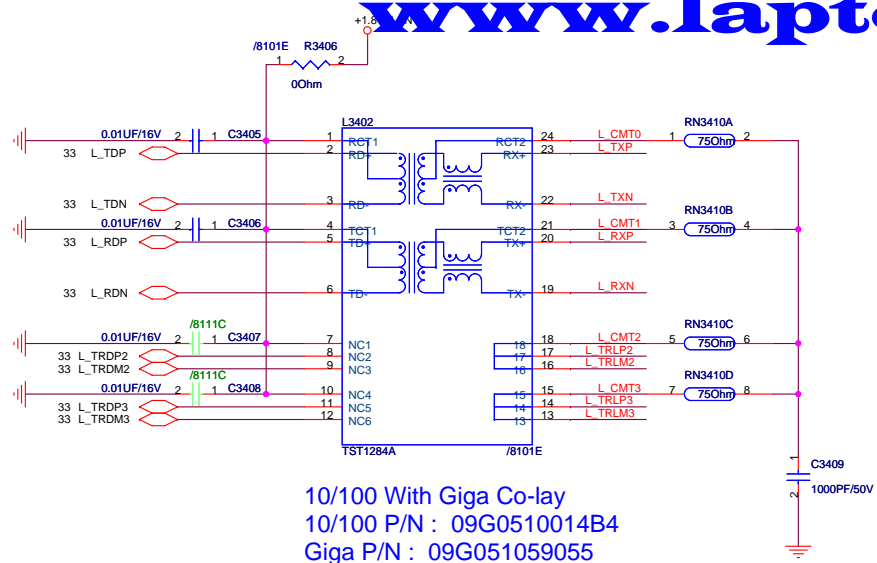
R3563 00hm

R3564 00hm

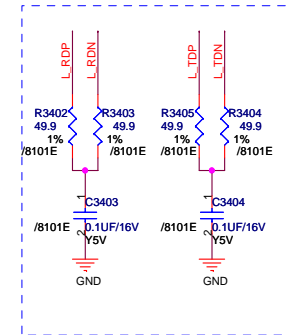
R3565 00hm

R356

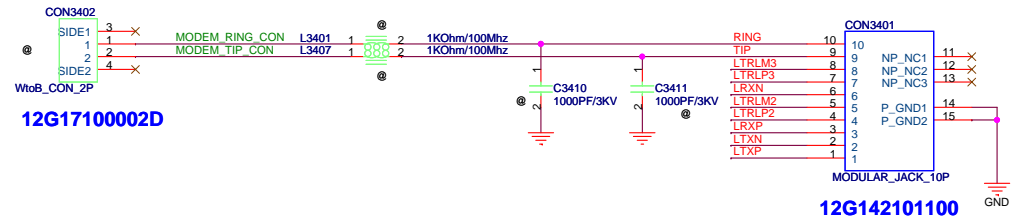
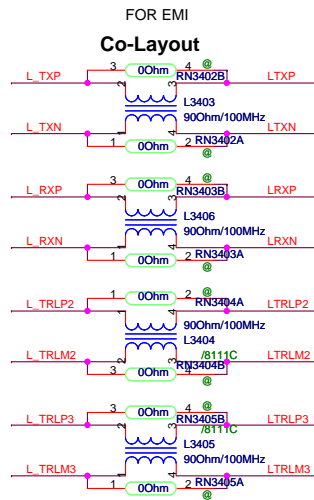
[illegible]



Only used in the
RTL8101E circuitry.



RJ45/RJ11

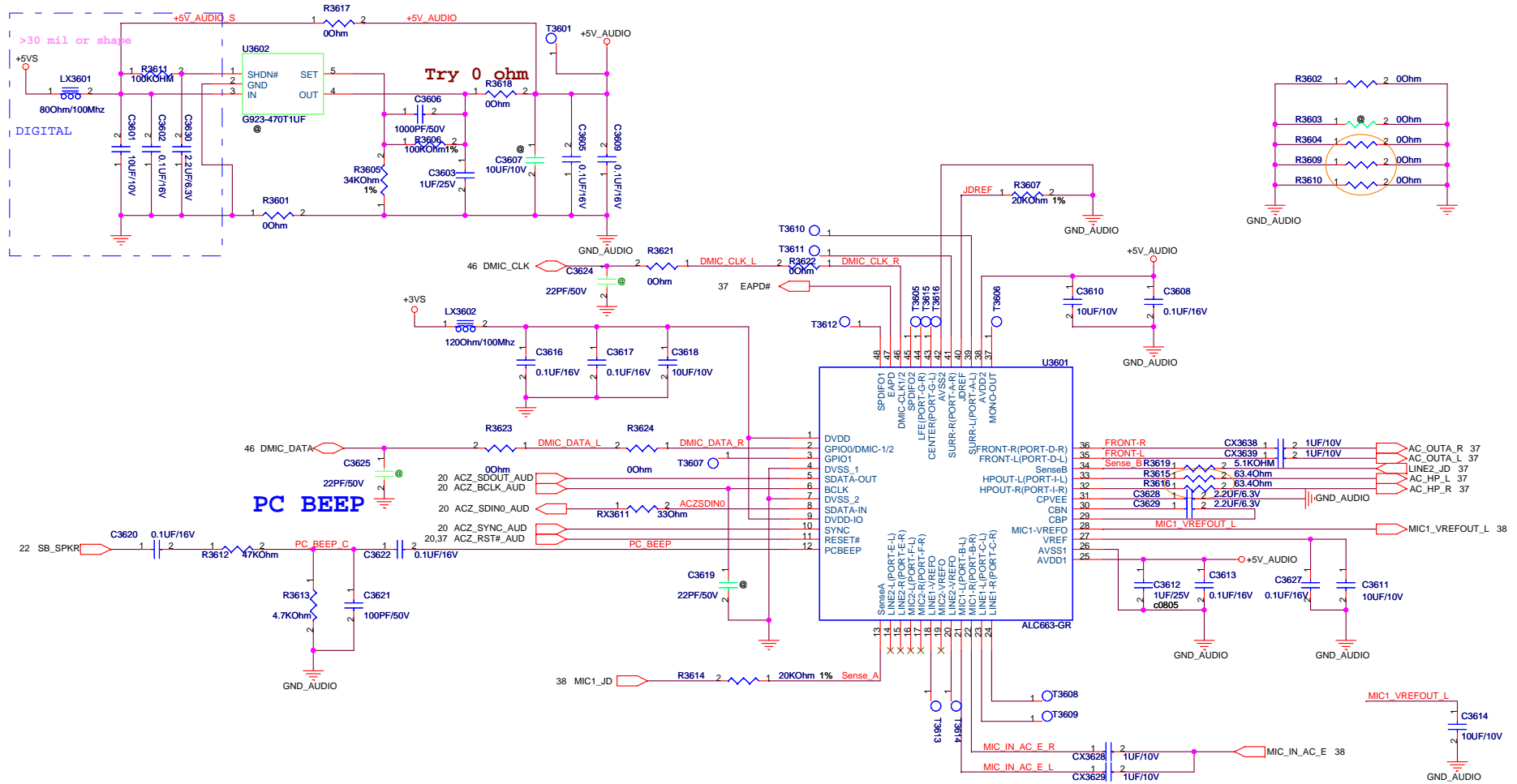


Audio Power

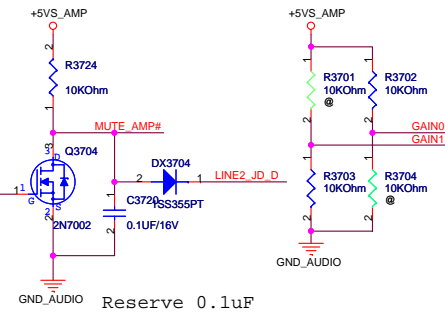
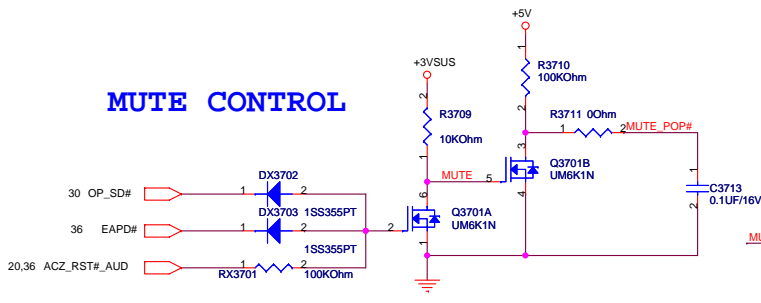
FOR ADJUST MODE:

$$V_o = 1.25 * (1 + R_{3606} / R_{3605})$$

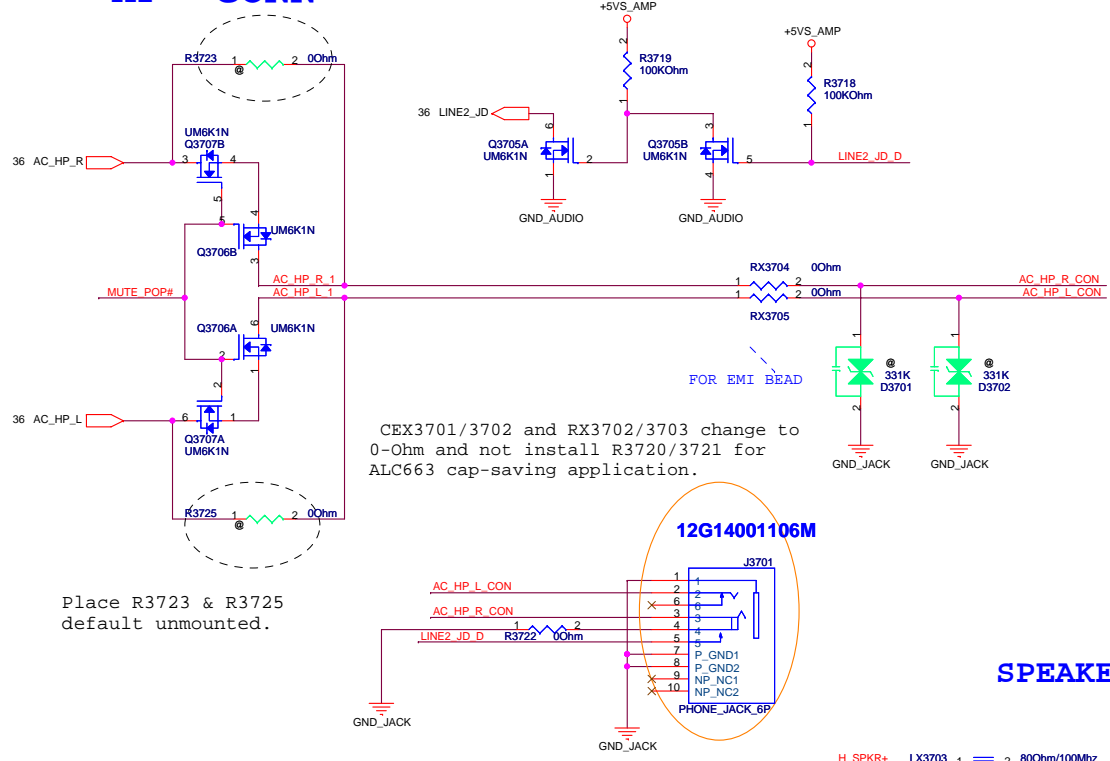
$$= 1.25 * (1 + 100K / 34K) = 4.926V$$



MUTE CONTROL

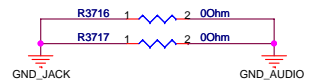


HP CONN

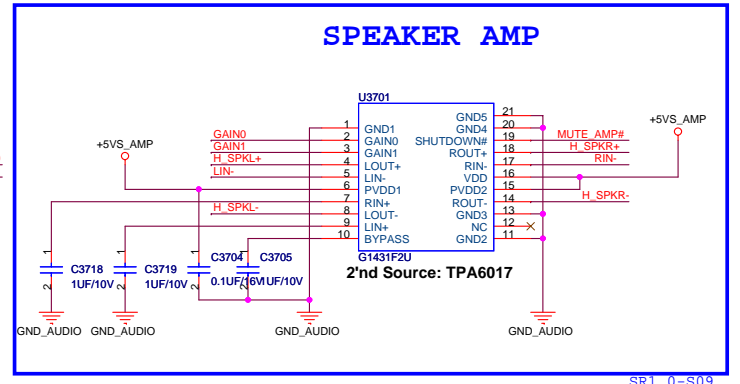


Place R3723 & R3725 default unmounted.

JACK GND

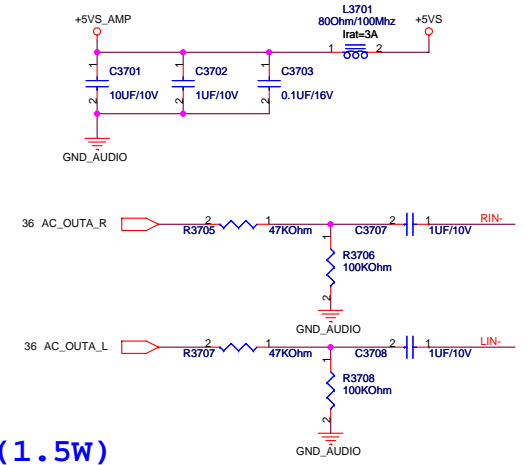


SPEAKER AMP

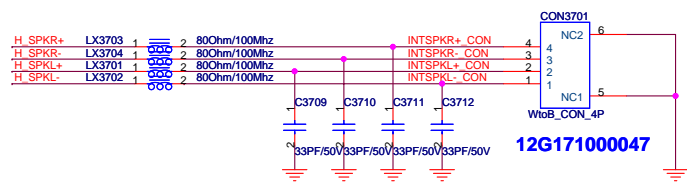


GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

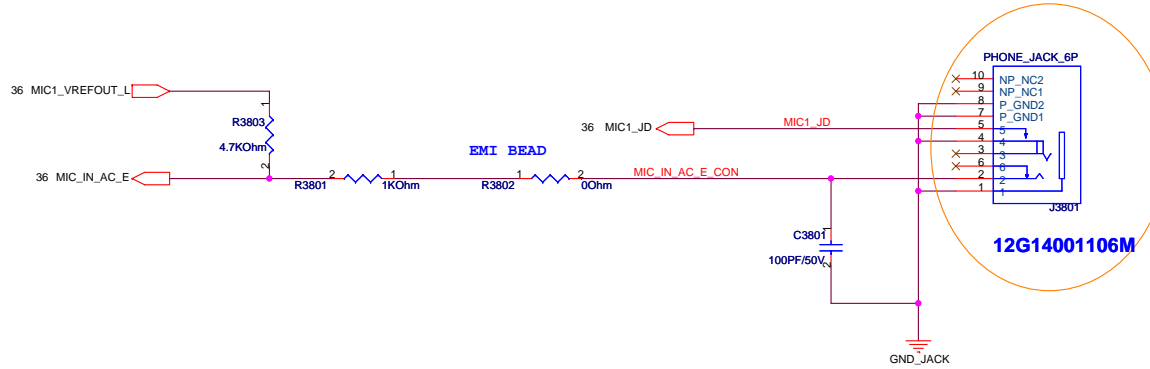
AMP POWER

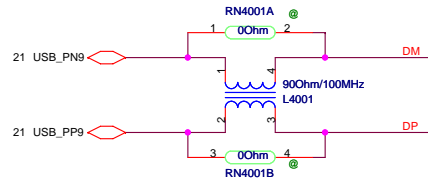
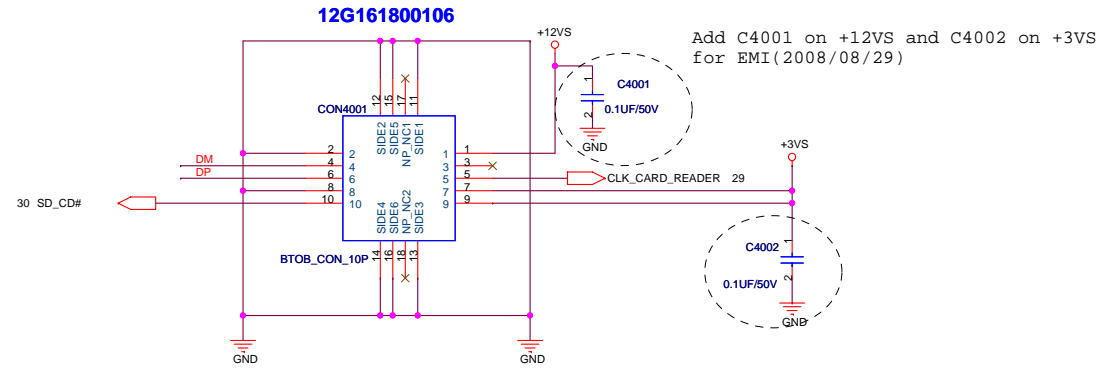


SPEAKER CONNECTOR (1.5W)



EXTERNAL MICROPHONE

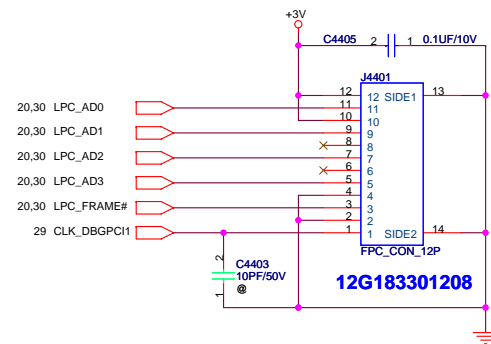


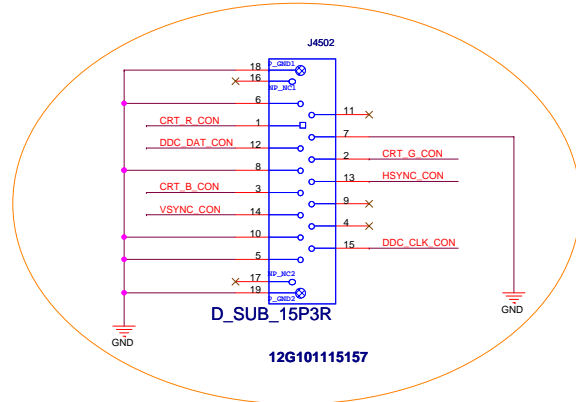


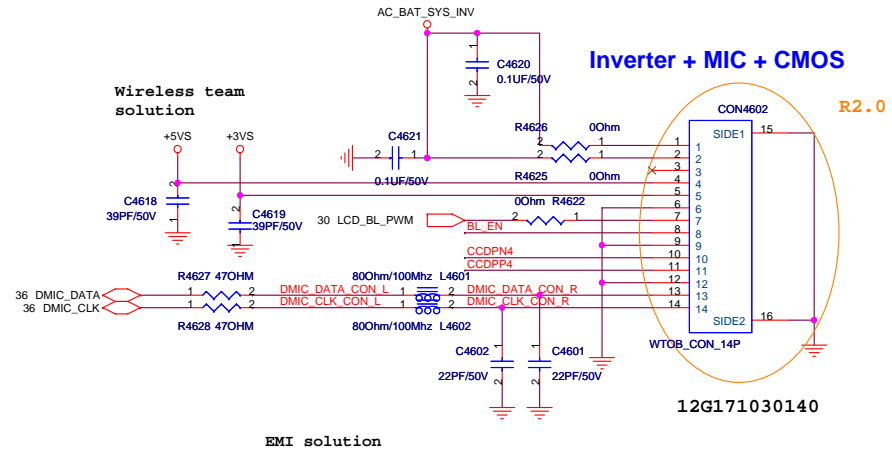
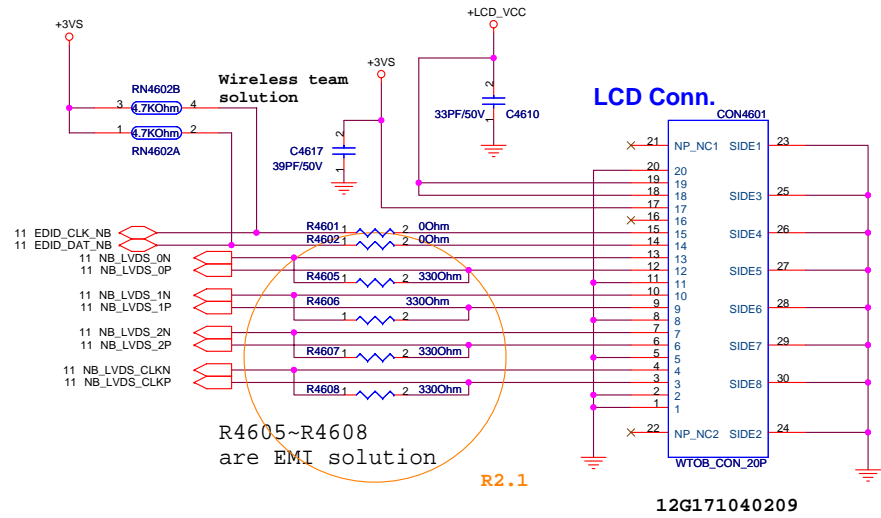
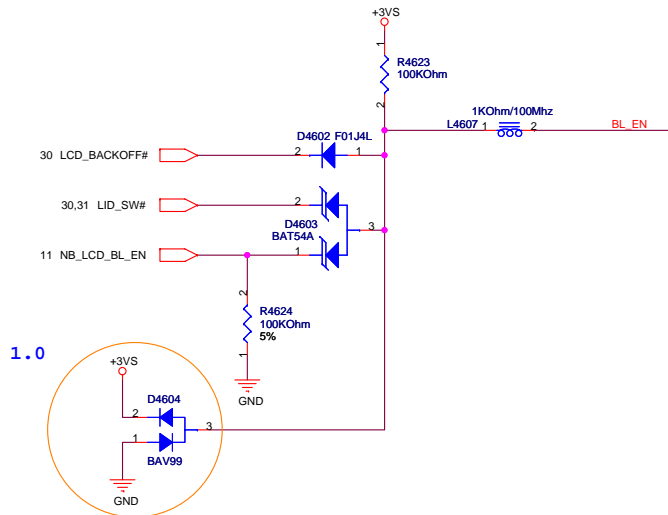
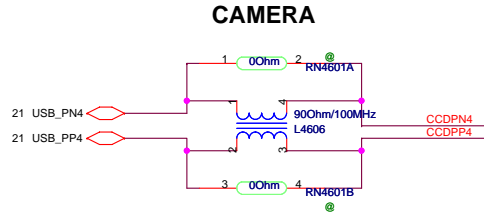
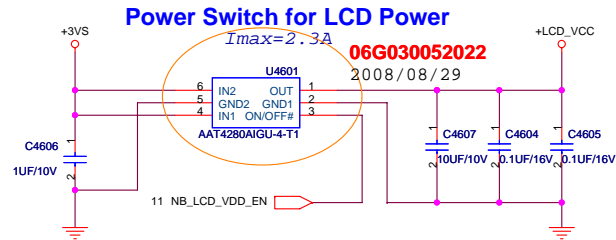
PEGATRON		Title :CARDBUS R5C833 (2)	
PEGATRON CORP BU1		Engineer: Daniel Liu	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: Thursday, August 28, 2008		Sheet	41 of 94

PEGATRON		Title : 1394&CardReader CON	
PEGATRON CORP BU1		Engineer: Daniel Liu	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: Thursday, August 28, 2008		Sheet	42 of 94

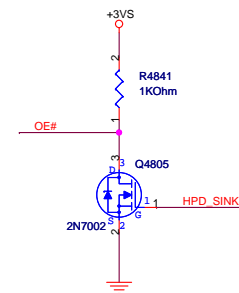
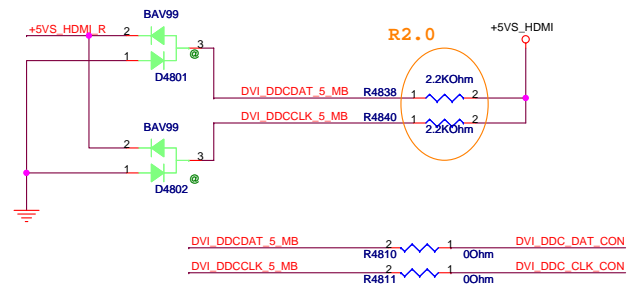
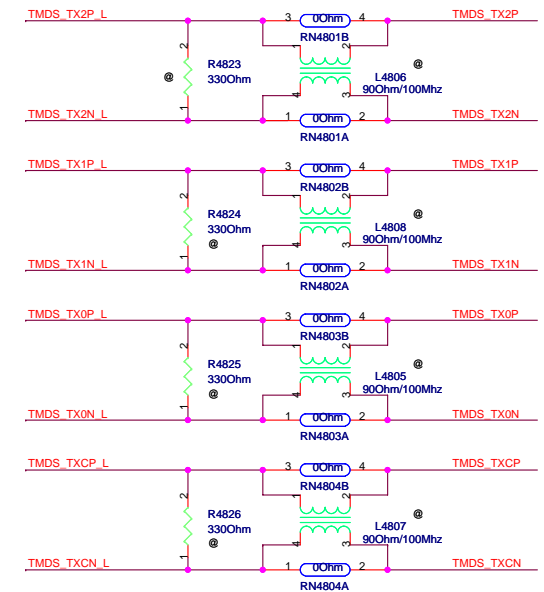
PEGATRON		Title : NEW CARD	
PEGATRON CORP BU1		Engineer: Daniel Liu	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: Thursday, August 28, 2008		Sheet	43 of 94



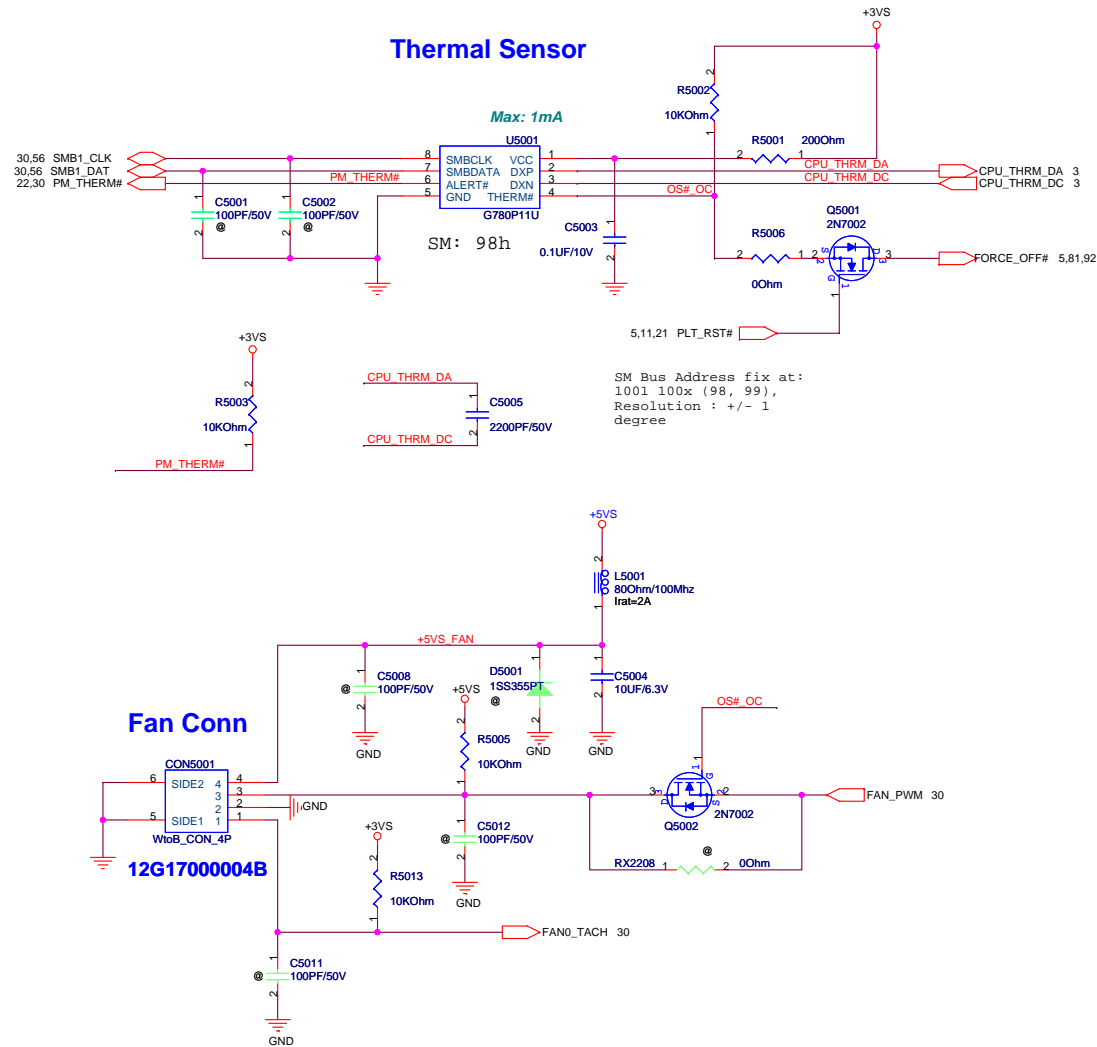
[illegible]



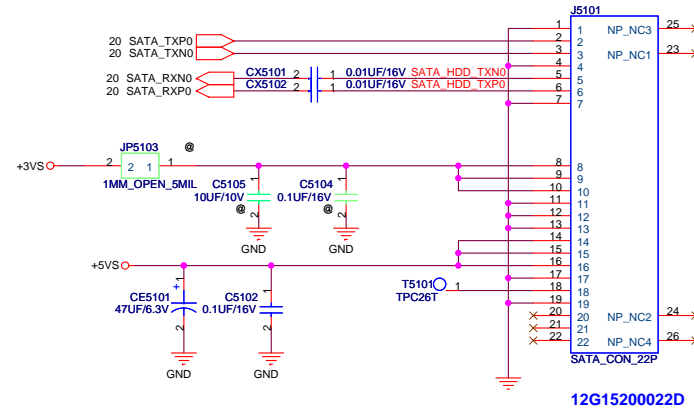
PEGATRON		Title : Hybrid-Switch	
PEGATRON CORP BU1		Engineer: Daniel Liu	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: Thursday, August 28, 2008		Sheet	47 of 94



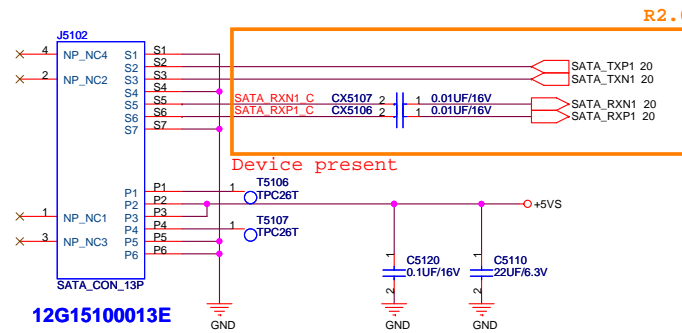
PEGATRON		Title :	HDMI
PEGATRON CORP BU1		Engineer:	Daniel Liu
Size Custom	Project Name H13Aw		Rev 1.0
Date: Thursday, August 28, 2008		Sheet	48 of 94

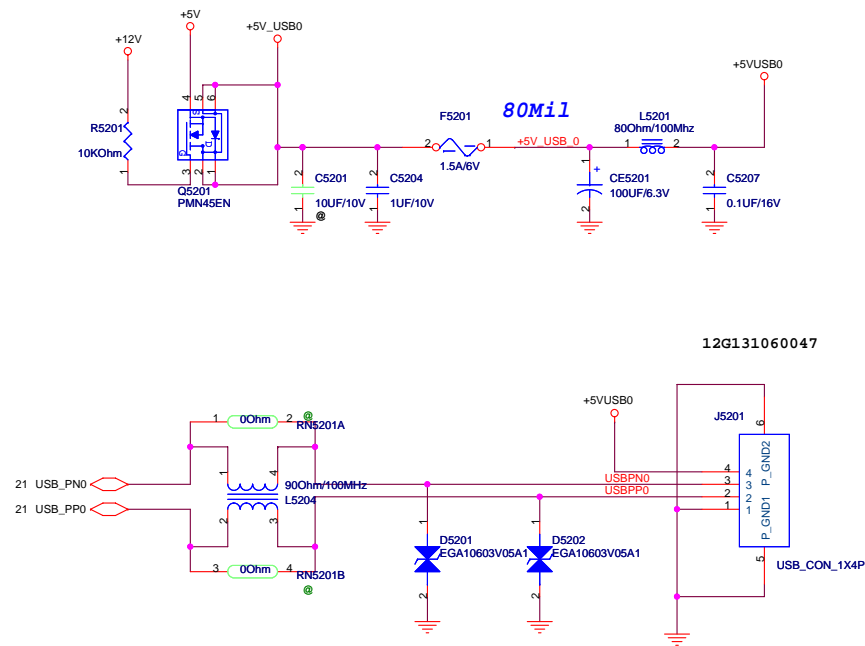


SATA HDD CON

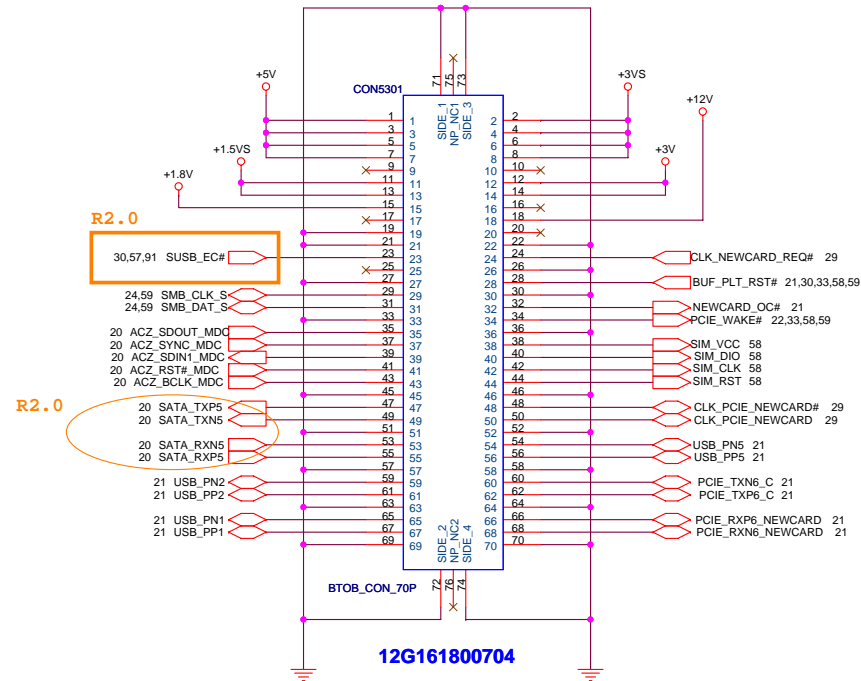


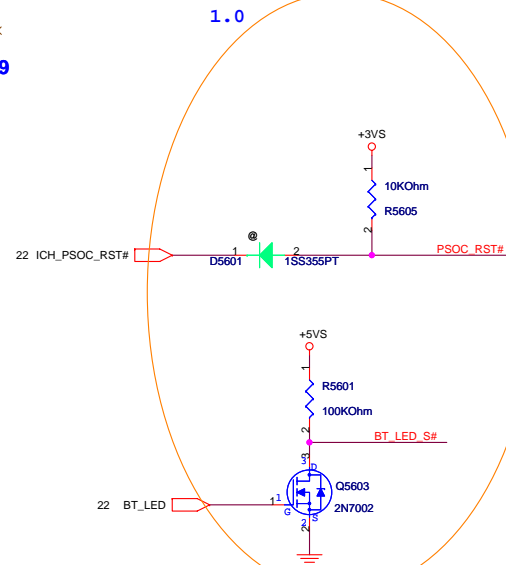
SATA ODD CON

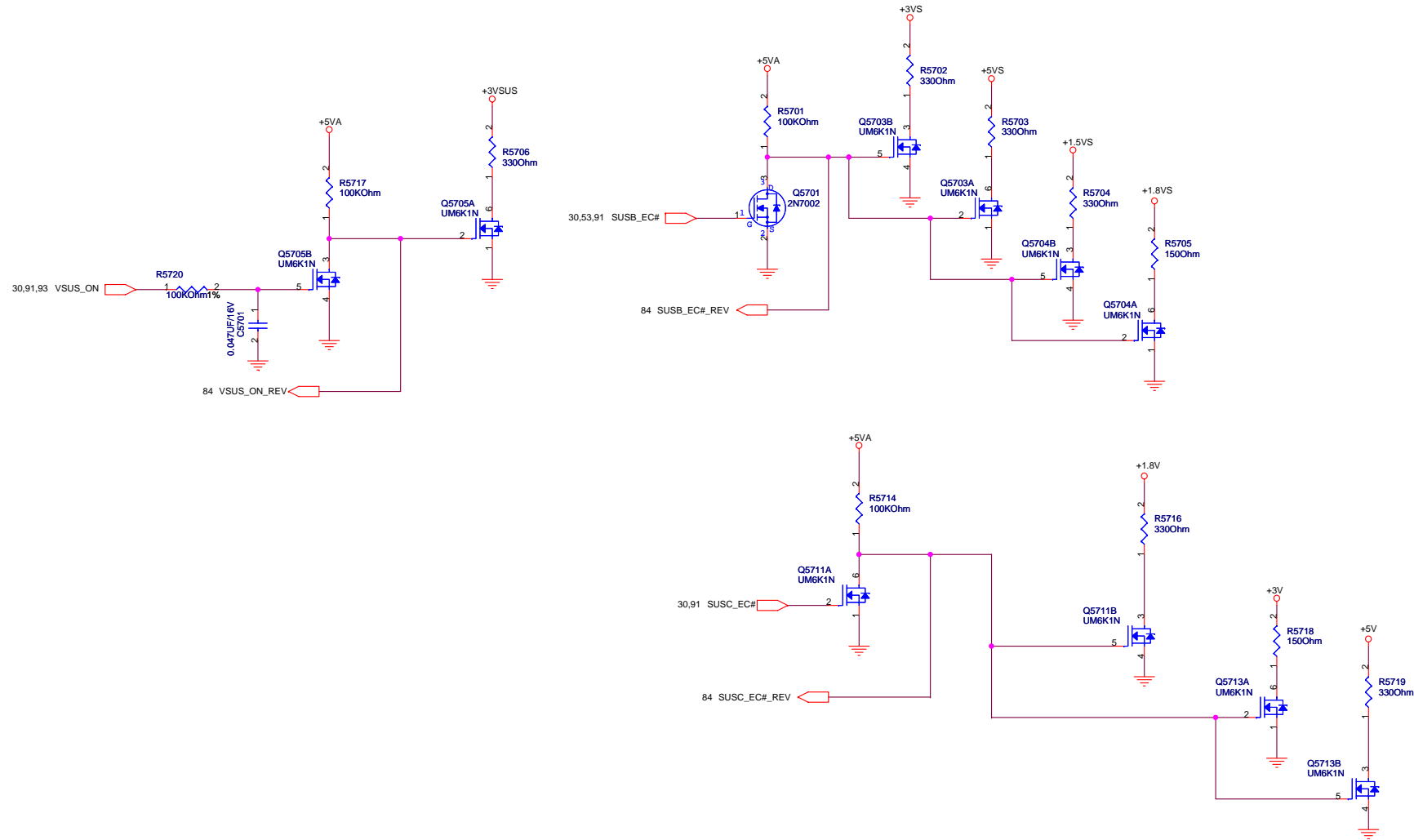


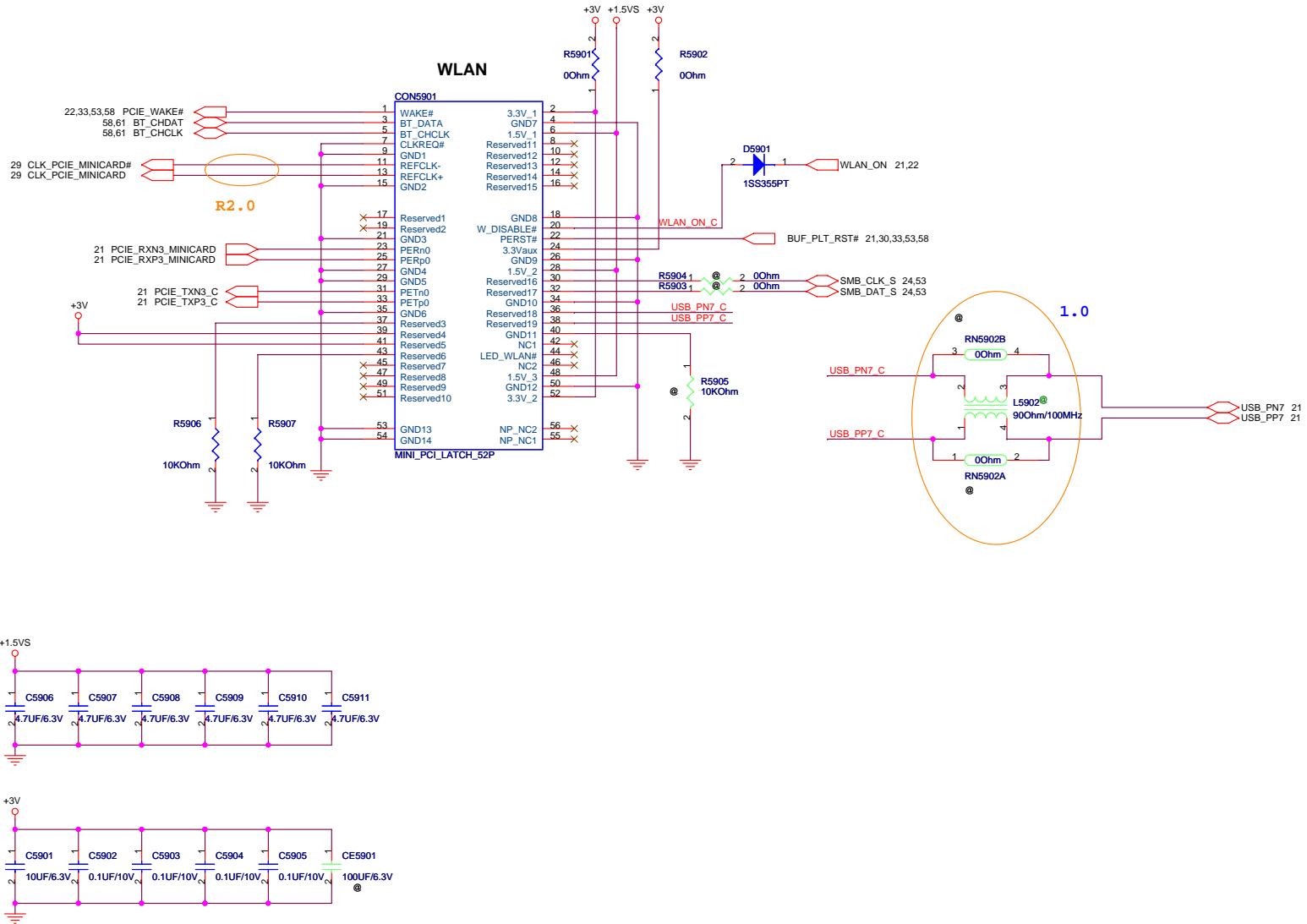


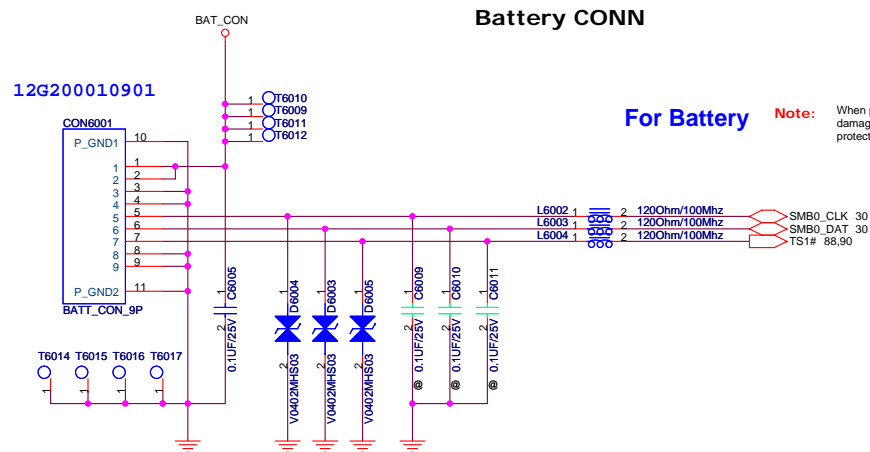
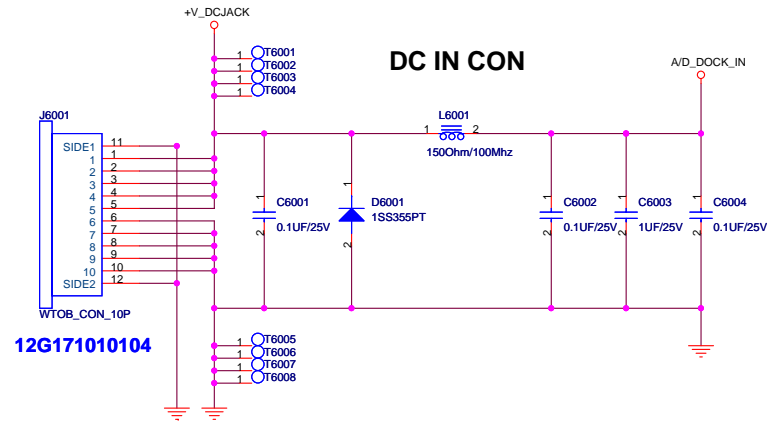
12G131060047

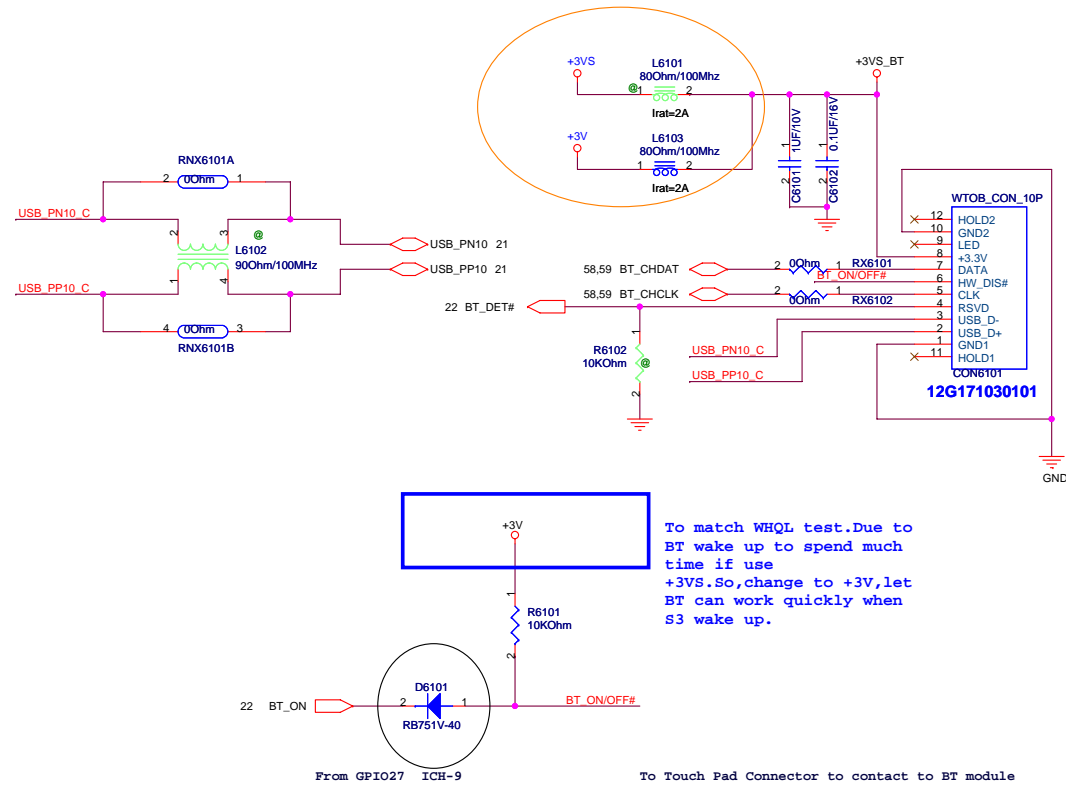












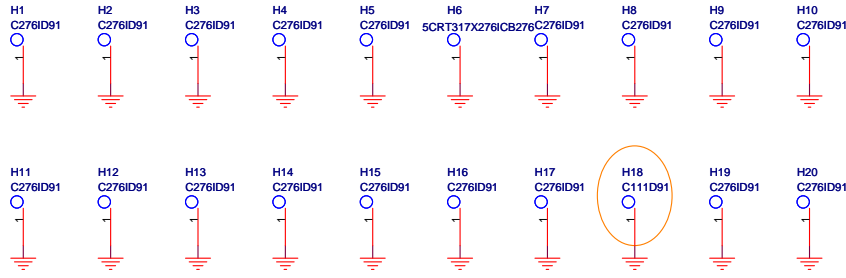
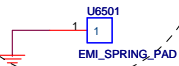
PEGATRON		Title : TPM	
PEGATRON CORP BU1		Engineer: Daniel Liu	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: Thursday, August 28, 2008		Sheet	62 of 94

PEGATRON		Title : Finger Printer	
PEGATRON CORP BU1		Engineer: Daniel Liu	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: Thursday, August 28, 2008		Sheet	63 of 94

R2.0

s03670

R2.0 Add U6501 EMI SPRING
for EMI(2008/06/02)



H18 change to PN:s03821(07/29/2008)

機構定位孔,N-PTH(2008/04/01)

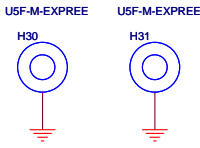
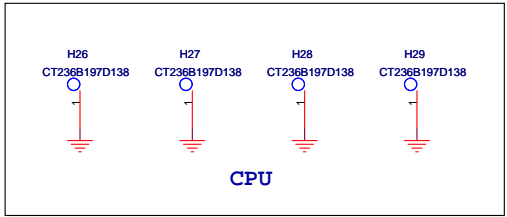
s01724
H34
O138x98DO138x98N

temp_5262_gh15
H35
C98D98N

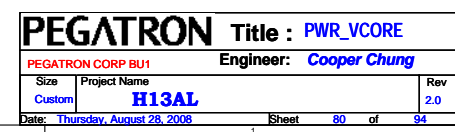


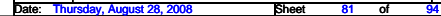
H24 change from PN:S03668 to 13GNQP10T040-1(04/01/2008)

Add Thermal Module NUT(04/01/2008)

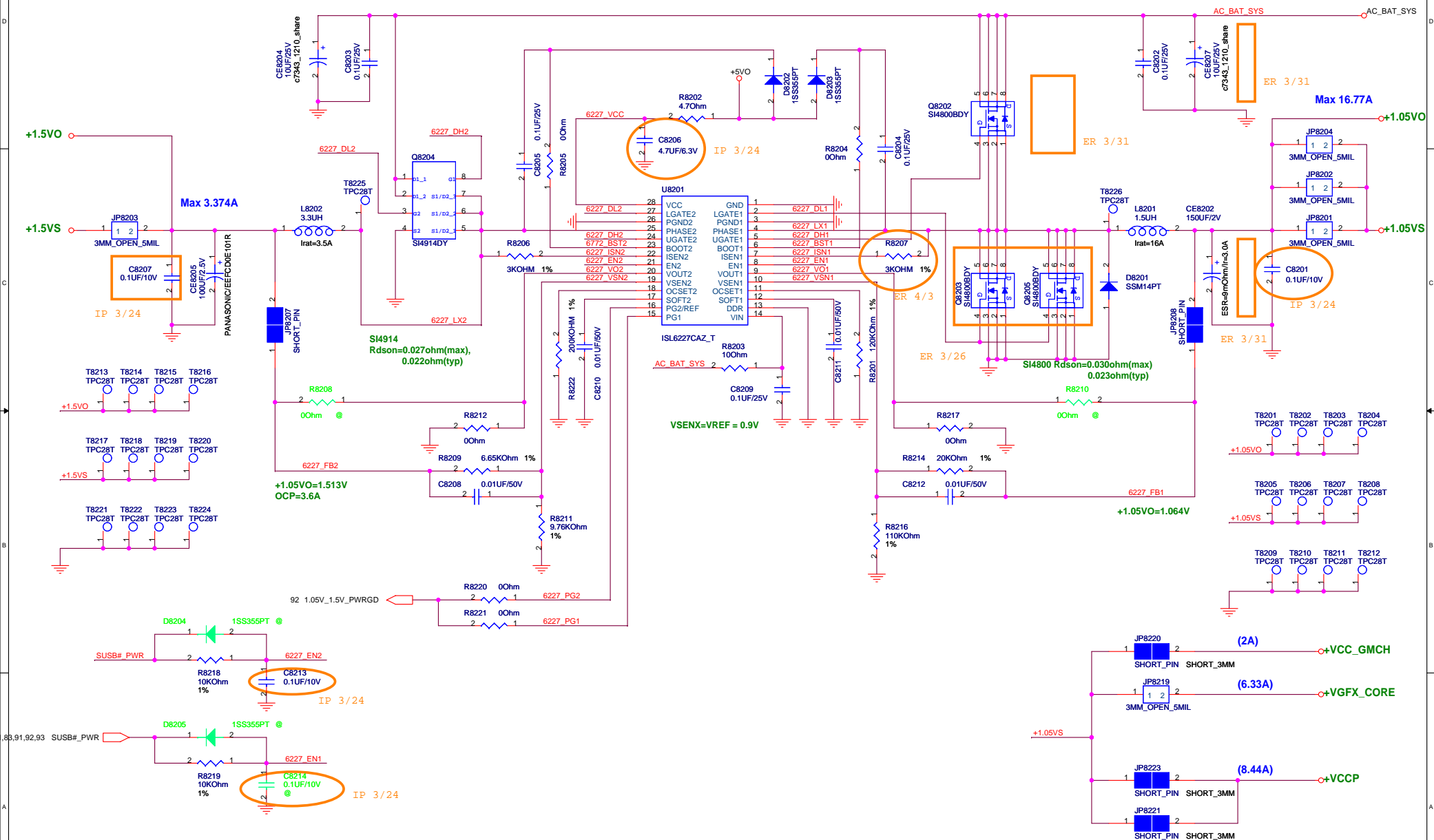


PEGATRON		Title :	
PEGATRON CORP BU1		Engineer: <i>Daniel Liu</i>	
Size	Project Name		Rev
Custom	H13Aw		1.0
Date: <i>Thursday, August 28, 2008</i>		Sheet	69 of 94



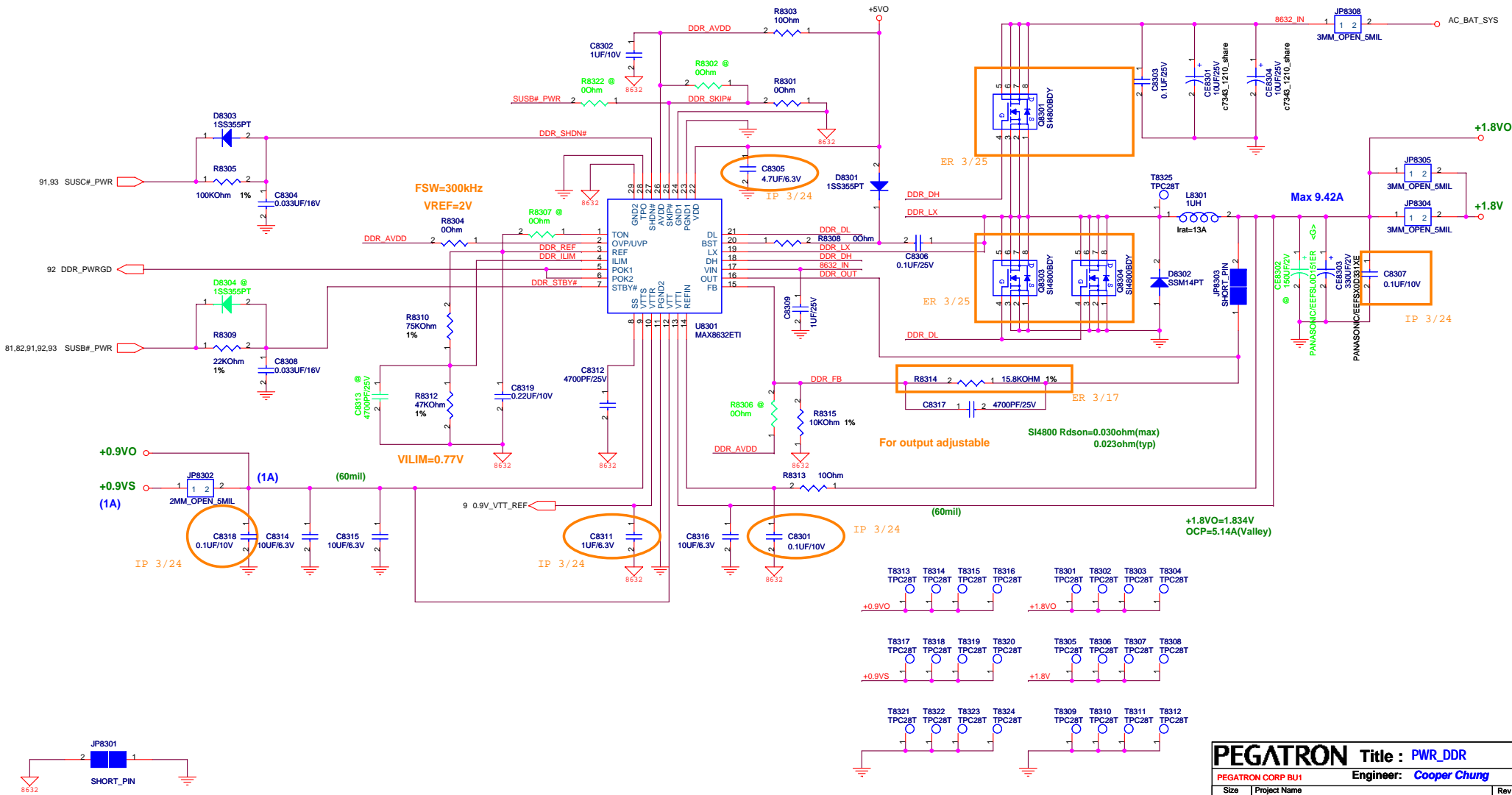


Change PN of CE8204, CE8207
to only 11G234210612320 in BOM

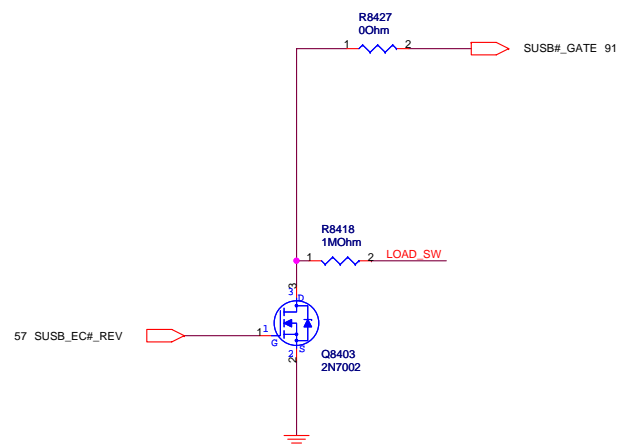
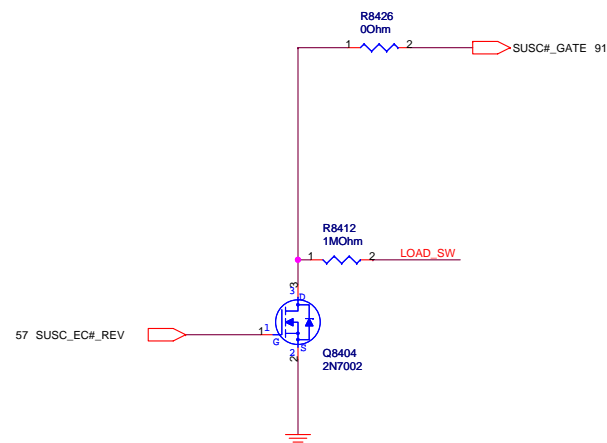


PEGATRON		Title : PWR_I/O	
PEGATRON CORP BU1		Engineer: Cooper Chung	
Size	Project Name	Rev	
Custom	H13AL	2.0	
Date: Thursday, August 28, 2008		Sheet 82 of 94	

Change PN of CE8301, CE8304
to only 11G234210612320 in BOM



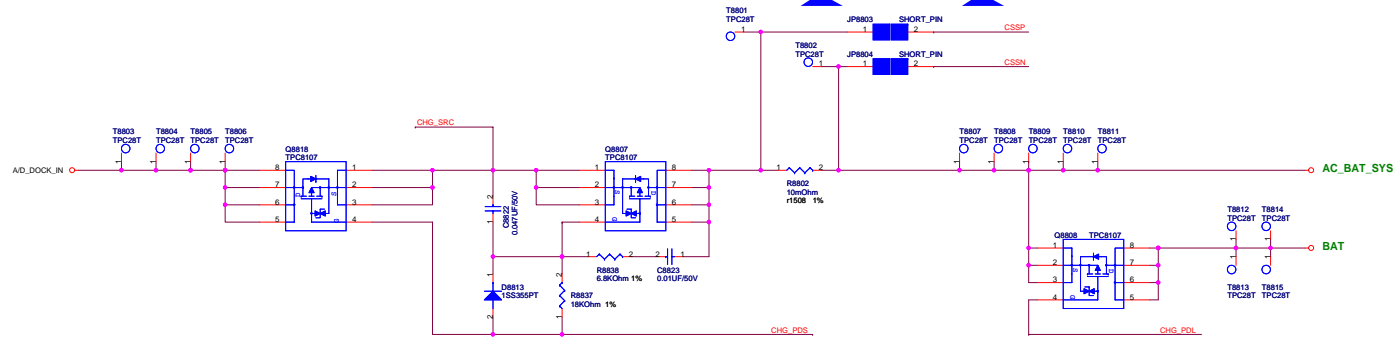
SUSB#_PWR Load SW



PEGATRON		Title : PWR_****	
PEGATRON CORP BU1		Engineer: Cooper Chung	
Size	Project Name		Rev
Custom	H13AL		2.0
Date: Thursday, August 28, 2008		Sheet	85 of 84

PEGATRON		Title : PWR_****	
PEGATRON CORP BU1		Engineer: Cooper Chung	
Size	Project Name		Rev
Custom	H13AL		2.0
Date: Thursday, August 28, 2008		Sheet 86 of 94	

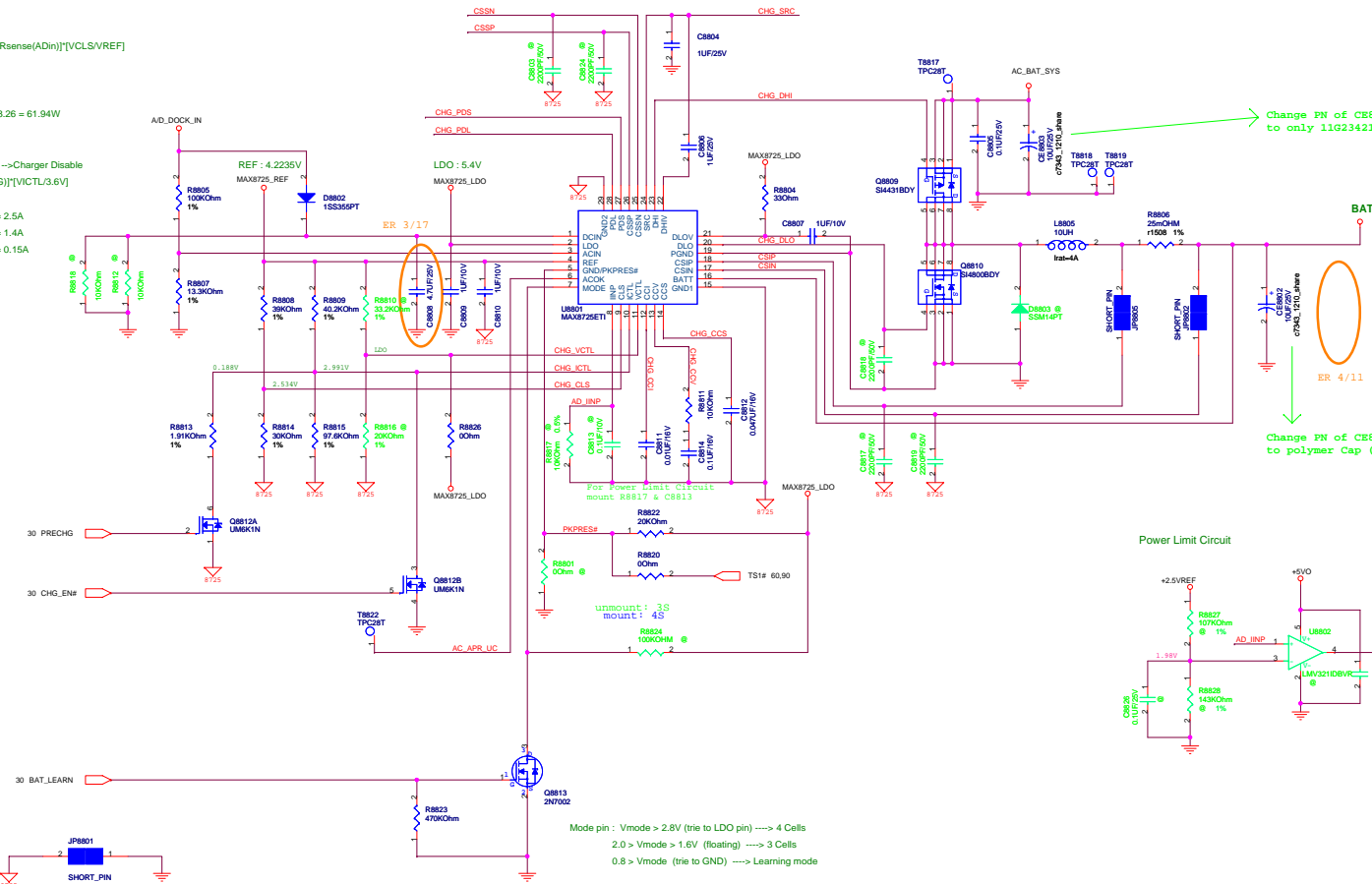
PEGATRON		Title : PWR_****	
PEGATRON CORP BU1		Engineer: Cooper Chung	
Size	Project Name		Rev
Custom	H13AL		2.0
Date: Thursday, August 28, 2008		Sheet 87 of 94	



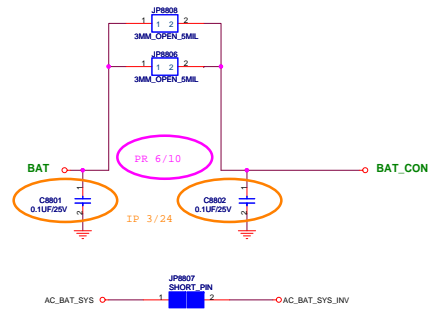
AC_IN Threshold 2.048V
=> A/D_DOCK_IN > 17.44V active

Adapter $I_{in(max)} = [0.075V/R_{sense(ADIN)}][V_{CLS}/V_{REF}]$
 $R_{sense(ADIN)} = 0.010\Omega$
 $V_{CLS} = 1.836V$
=> $I_{in(max)} = 3.26A$
=> Constant Power = $19 \times 3.26 = 61.94W$

$I_{CTL} < 0.06V$ or $DCIN < 7V$ -> Charger Disable
 $I_{chg} = [0.075V/R_{sense(CHG)}][V_{ICTL}/3.6V]$
 $R_{sense(CHG)} = 0.025\Omega$
 $V_{ICTL} = 2.991V$ => $I_{chg} = 2.5A$
 $V_{ICTL} = 1.68V$ => $I_{chg} = 1.4A$
 $V_{ICTL} = 0.188V$ => $I_{chg} = 0.15A$
 $V_{CTL} = MAX8725_LDO$
=> $V_{batt} = Cell \times 4.2V$



Mode pin : $V_{mode} > 2.8V$ (tie to LDO pin) -> 4 Cells
 $2.0 > V_{mode} > 1.6V$ (floating) -> 3 Cells
 $0.8 > V_{mode}$ (tie to GND) -> Learning mode

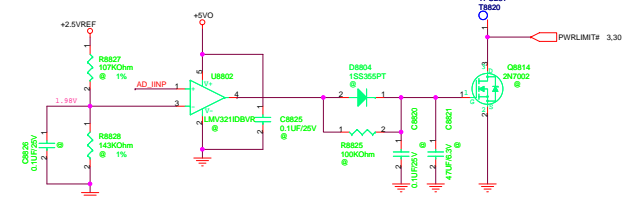


AC_BAT_SYS_INV to Inverter connect,
Power trace = 60mil(min),
Put JP8807 close to Q8808

Change PN of C8803
to only 11G234210612320 in BOM

Change PN of C8802
to polymer Cap (11G08D215620) in BOM

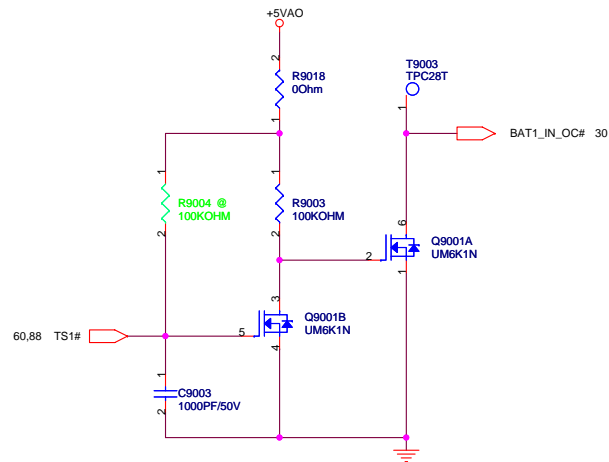
Power Limit Circuit



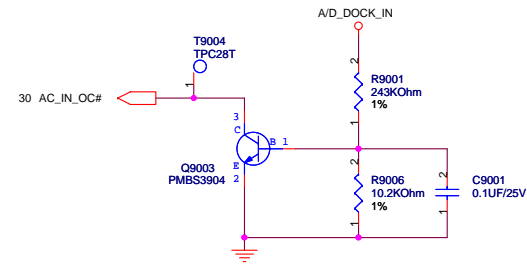
PEGATRON Title : PWR_CHARGER	
PEGATRON CORP BUY	Engineer: Cooper Chung
Rev: 1	Project Name: H13AL
Custom: H13AL	Rev: 2.0
Date: Thursday, August 28, 2008	Sheet: 88 of 94

PEGATRON		Title : PWR_****	
PEGATRON CORP BU1		Engineer: Cooper Chung	
Size	Project Name		Rev
Custom	H13AL		2.0
Date: Thursday, August 28, 2008		Sheet	89 of 94

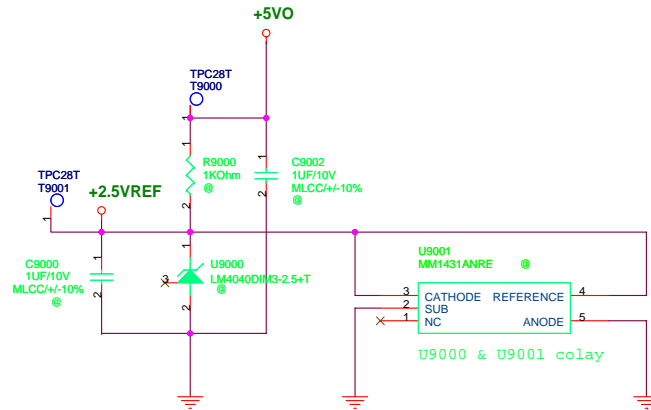
BATTERY IN DETECT



ADAPTER IN DETECT



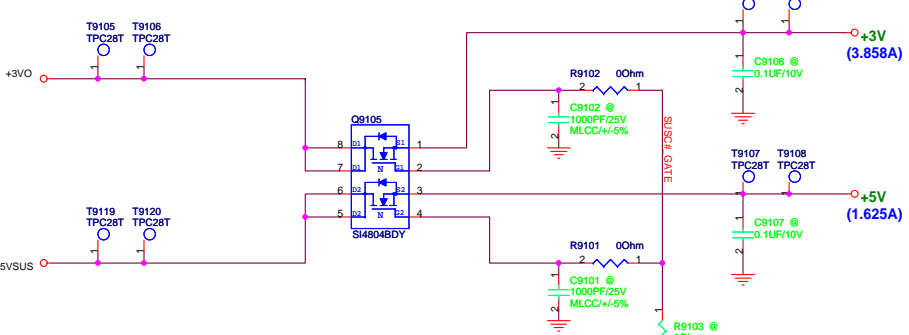
+2.5VREF



U9001 Main source change to 06G006002414(tolerance:1%).
Add second source 06G006002610 (tolerance:1%),
06G006002412 (tolerance:0.2%) and
06G006002020(tolerance:0.2%)

PEGATRON		Title : PWR_DETECT	
PEGATRON CORP BU1		Engineer: Cooper Chung	
Size A3	Project Name H13AL		Rev 2.0
Date: Thursday, August 28, 2008		Sheet 90	of 94

SUSC#_P_R Load SW



12V SUS

T9109
TPC28T

T9125
TPC28T

SUSC# PWR

Q9111
UMC4N

T9110
TPC28T

T9111
TPC28T

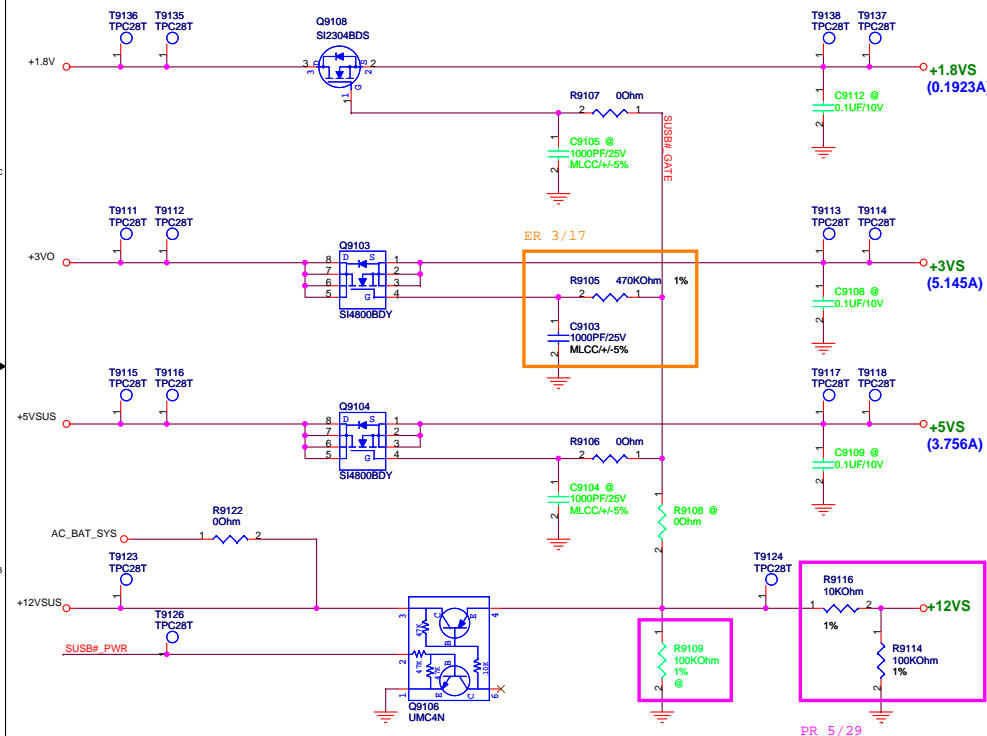
R9104
100KOhm
1%
⊕

R9120
10KOhm

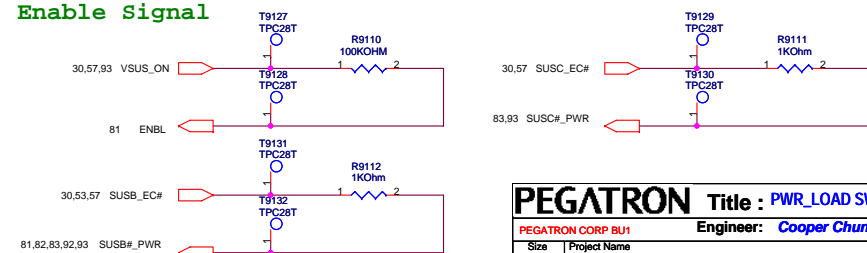
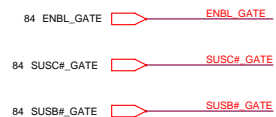
R9113
100KOhm
1%

+12V

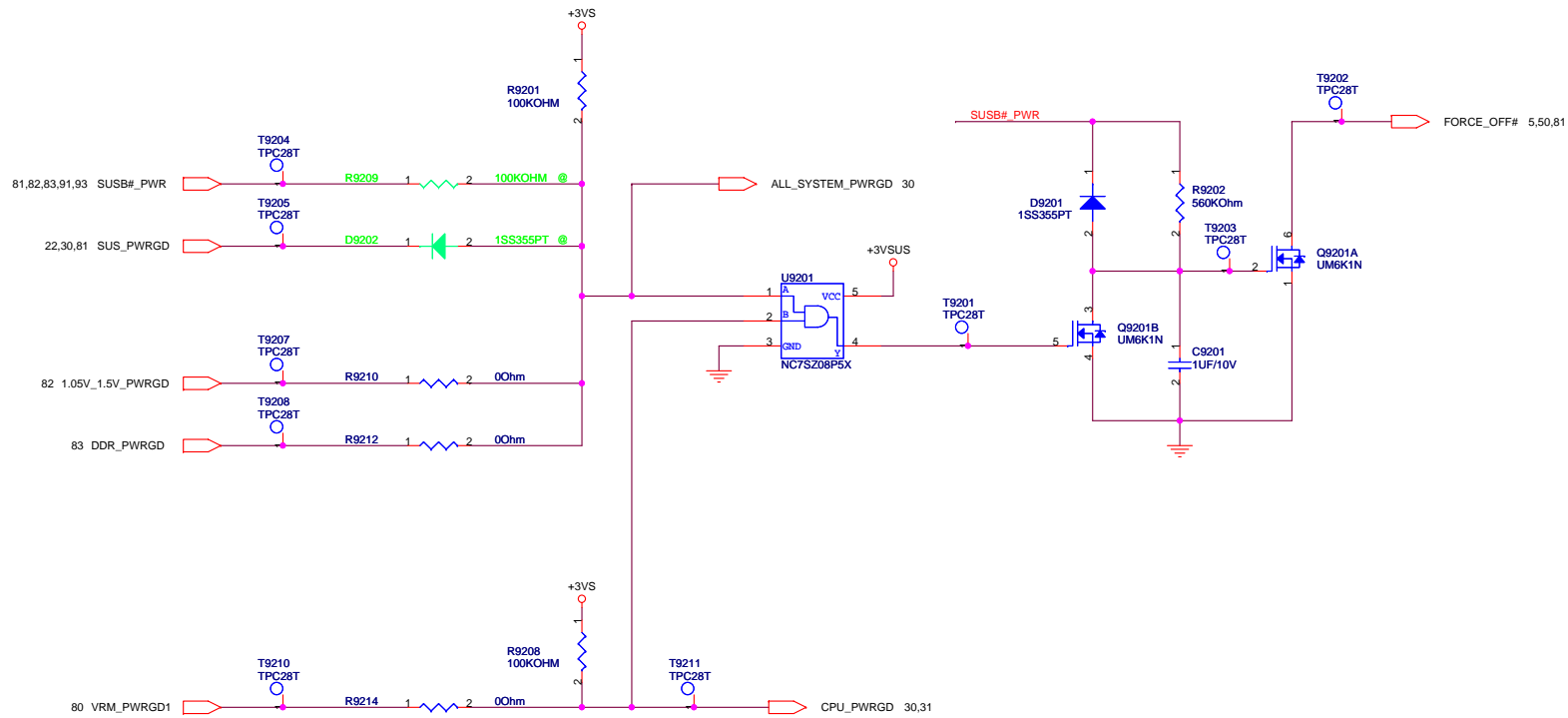
PR 5/29

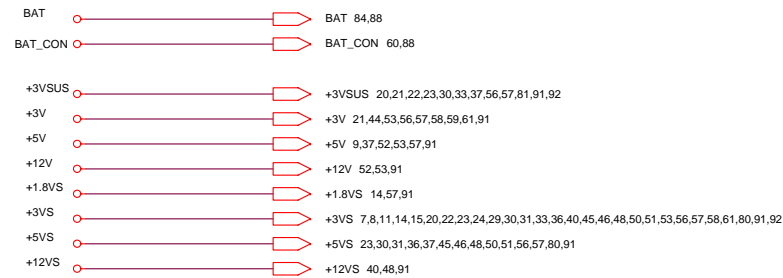
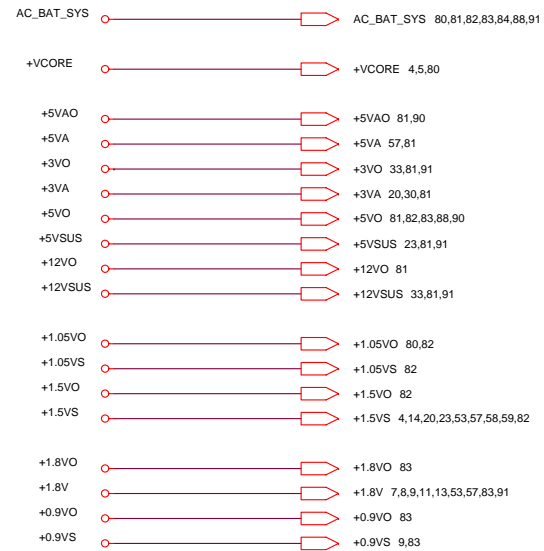


Enable Signal



POWER GOOD DETECTOR





FOR POWER TEST

