

Model Name :

File Name :

Compal Confidential

ULC UMA M/B LA-A994P Schematics Document

Intel Bay Trail M VC

Project Code : ZSO50

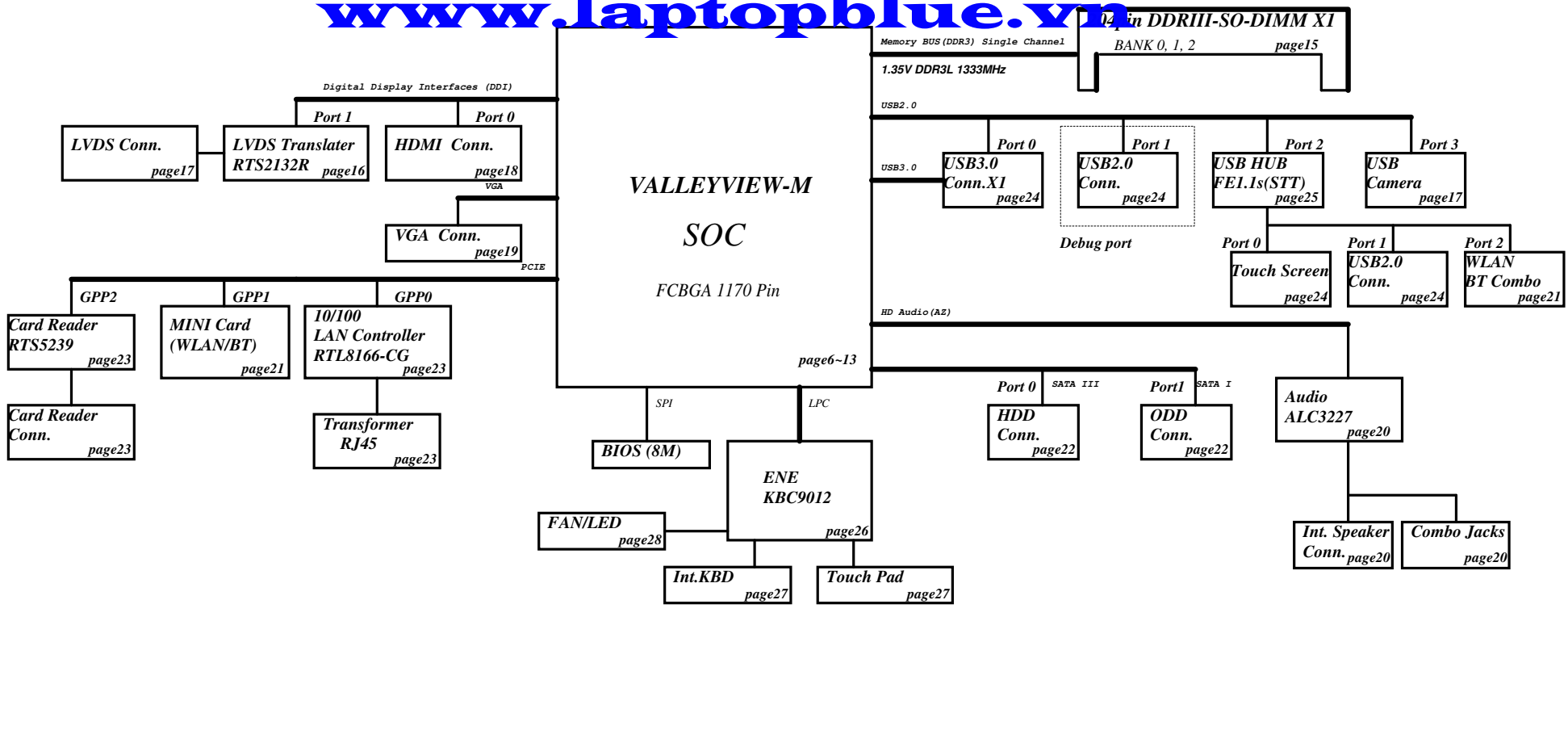
2014/02/05

MV Rev. 1.0

DAX ZSO50 BayTrail-M

Part Number	Description
DAZ14Z00200	PCB 14Z LA-A994P REV0 M/B 4

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Issued Date	2012/12/01	Deciphered Date	2013/07/10	Title	Cover Page
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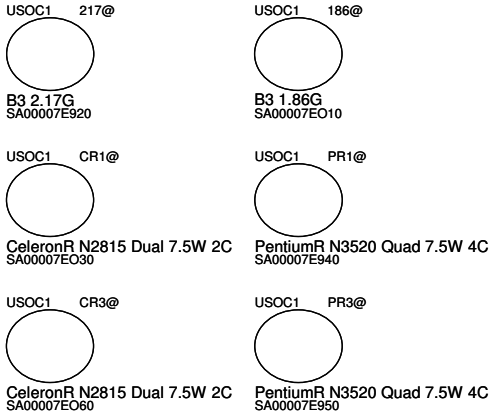
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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.2VALW	+1.2v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

Board ID	PCB Revision
DB	0.1
SI	0.2
PV	0.3
MV	1.0

BOM Option Table	
BTO Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMI requirement	EMI@
EMI requirement unpop	@EMI@
ESD requirement	ESD@
ESD requirement unpop	@ESD@
8161 LAN controller	8161@
8166 LAN controller	8166@
LVDS	LVDS@
LVDS LDO mode	LVDSLDO@
LVDS SWR mode	LVDSSWR@
Translator RTS2132S	2132S@
Translator RTS2132R	2132R@
Short Pad	RS@
Clean CMOS	CMOS@
Jump	JP@



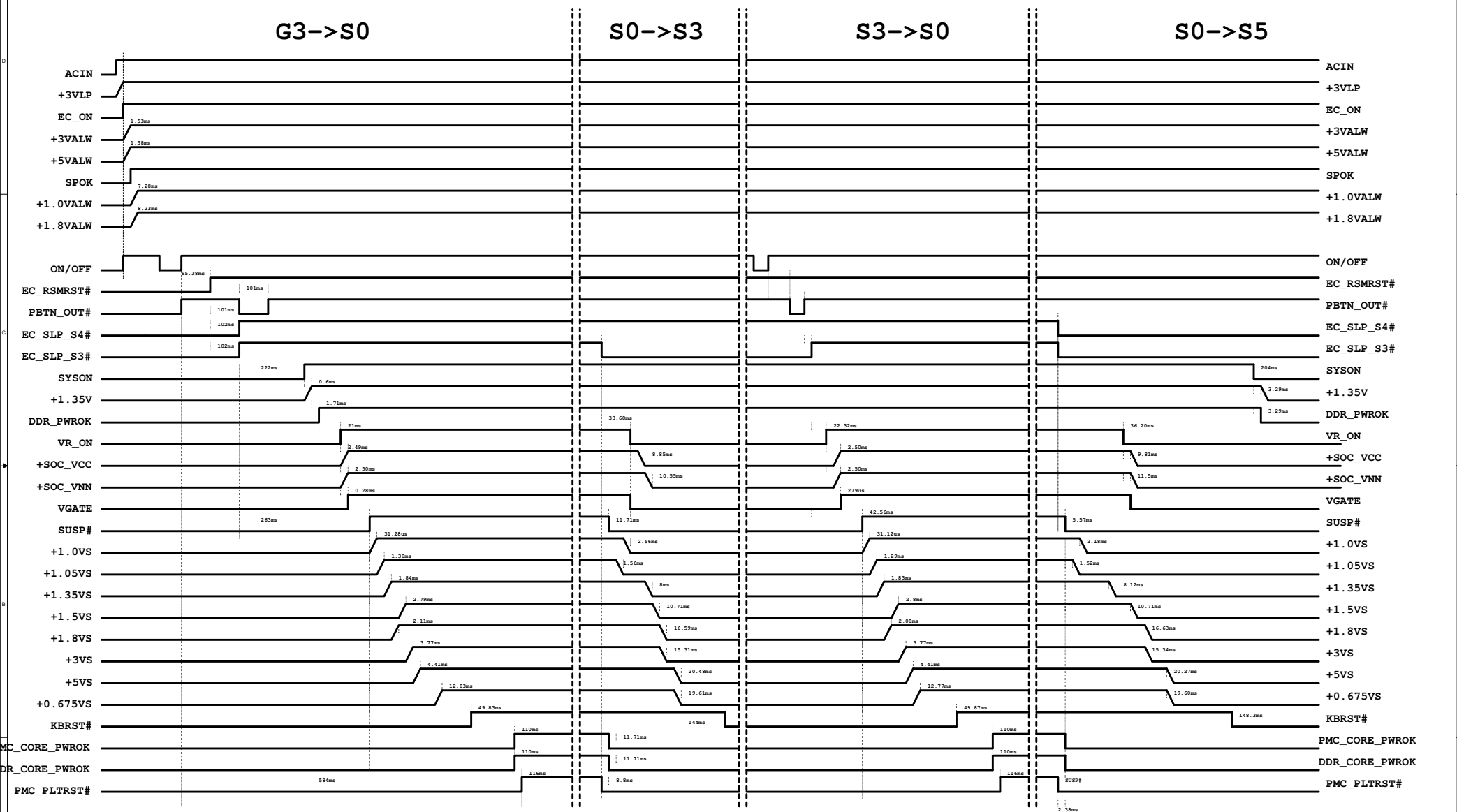
EC SM Bus1 address		EC SM Bus2 address	
Device	Address	Device	Address
Smart Battery	0001 011X b		
SOC SM Bus address			
Device	Address		
ChannelA DIMM0 A0	1010 000X	JDIMM1(SPD)	

43 level BOM table

43 Level	Description	BOM Structure
4319P6BOL01	SMT MB AA231 V1UE3 HDMI	

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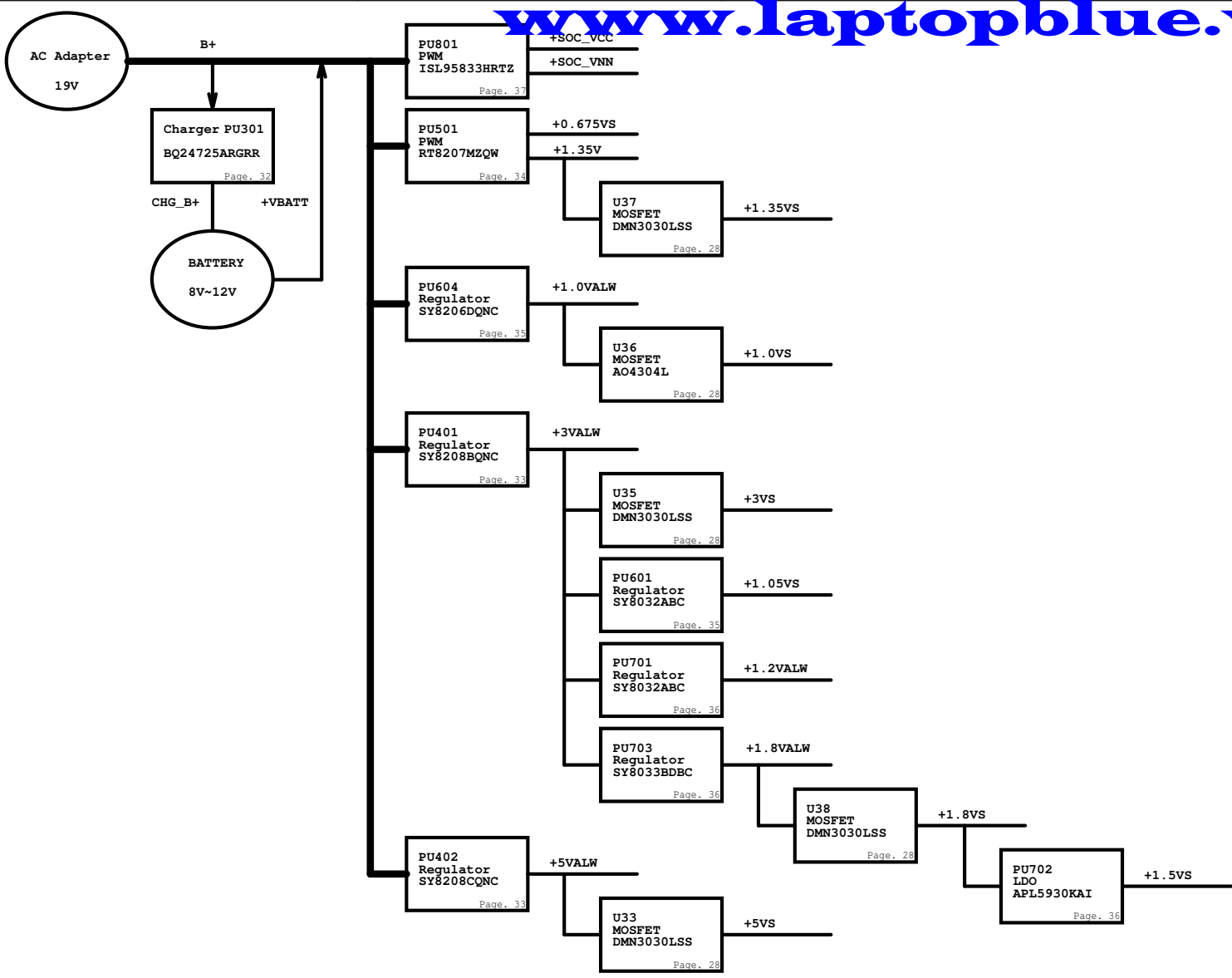


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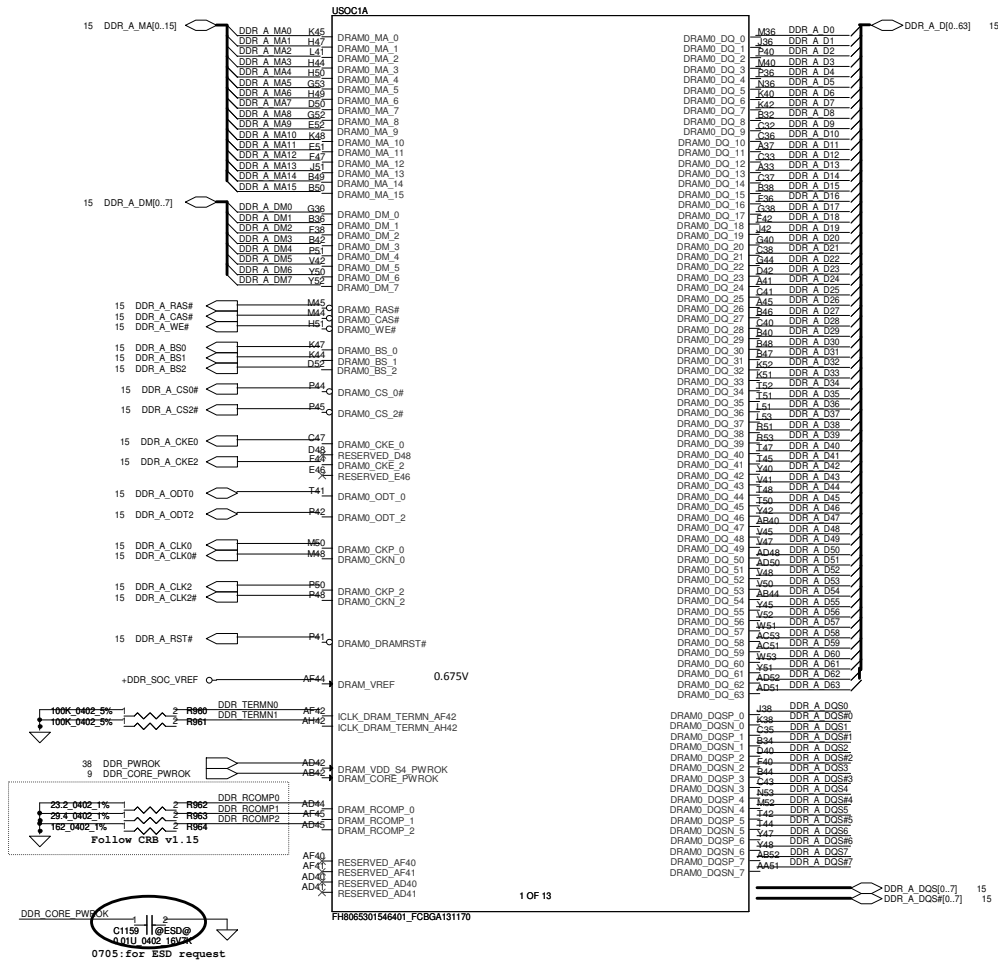
1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

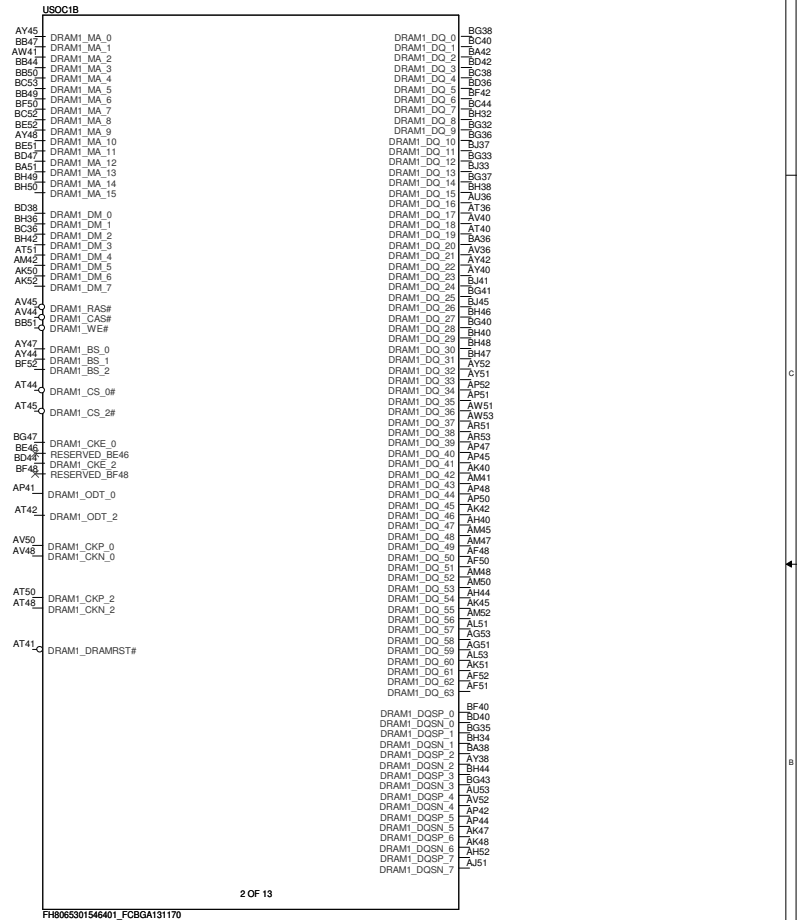
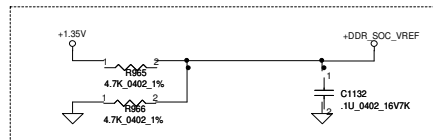
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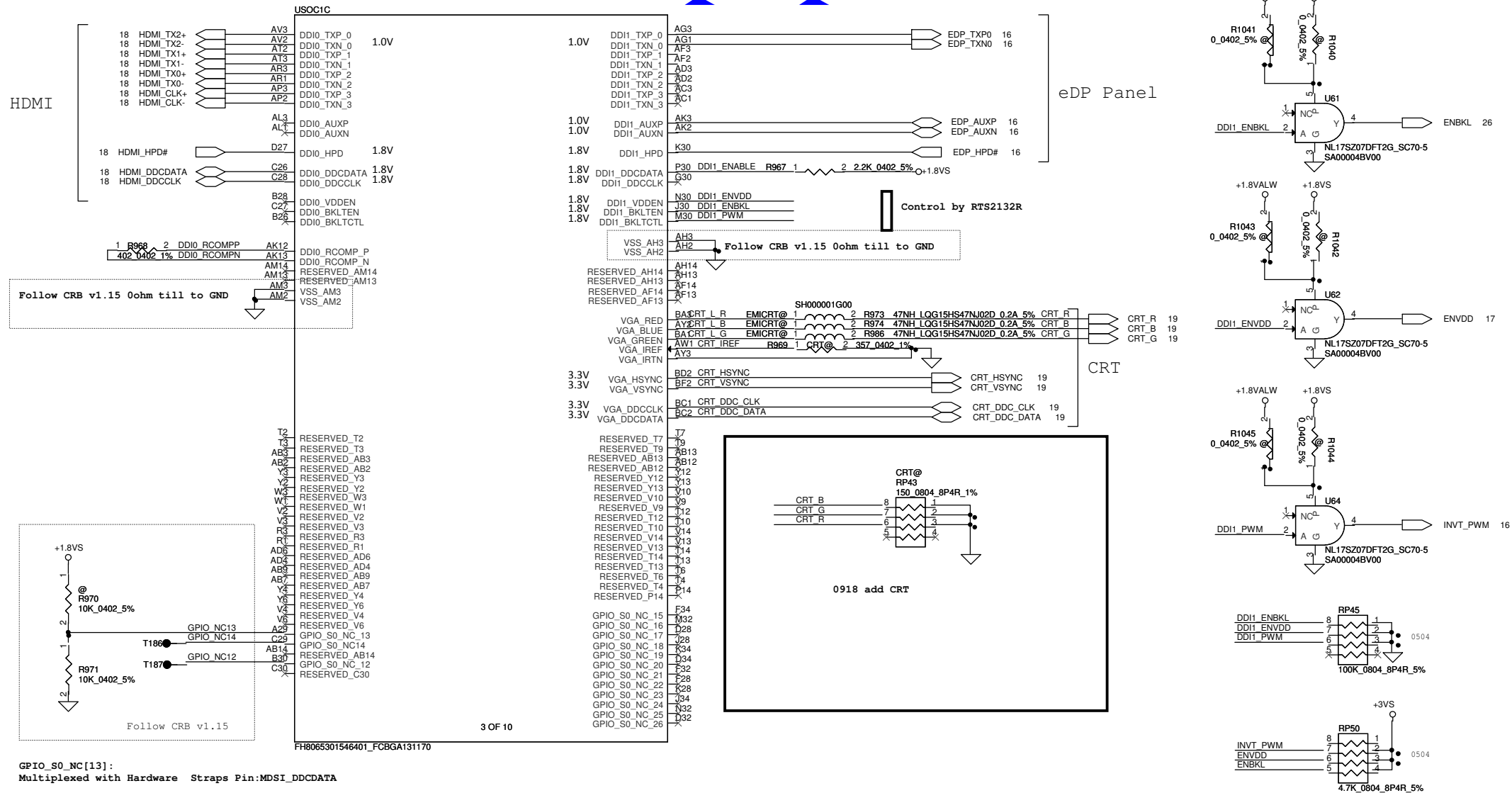


Close To SOC Pin

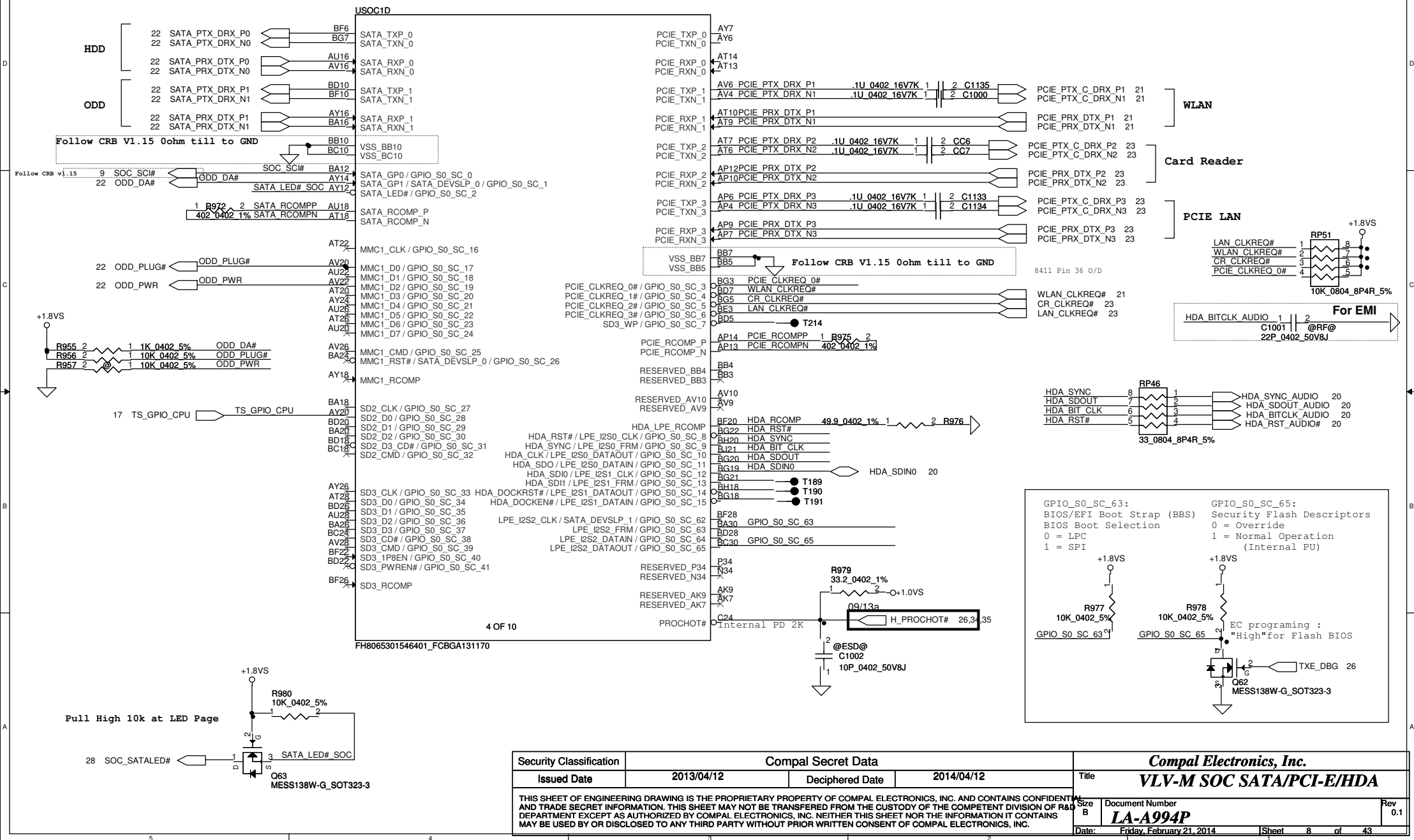


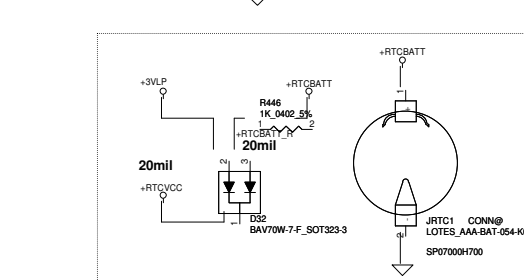
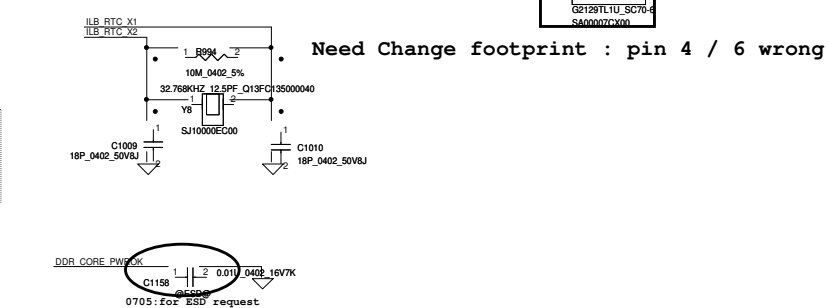
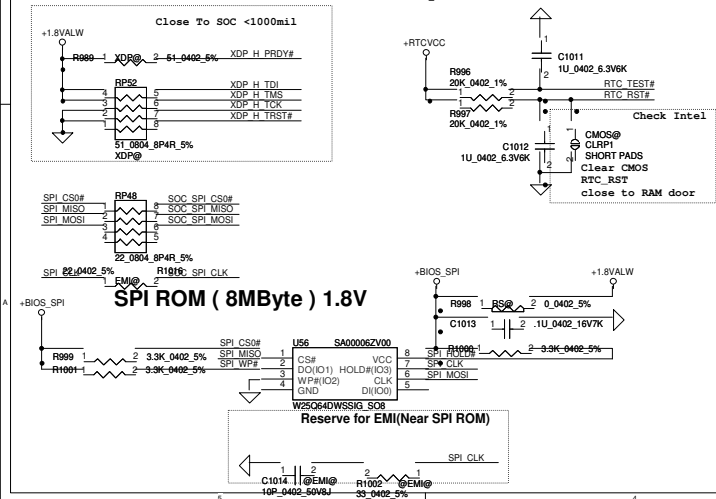
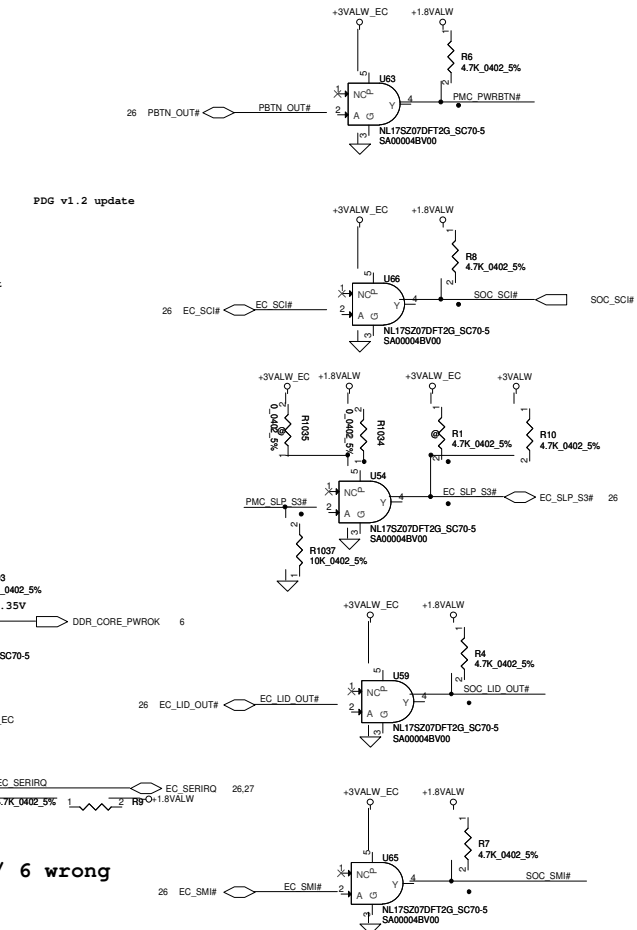
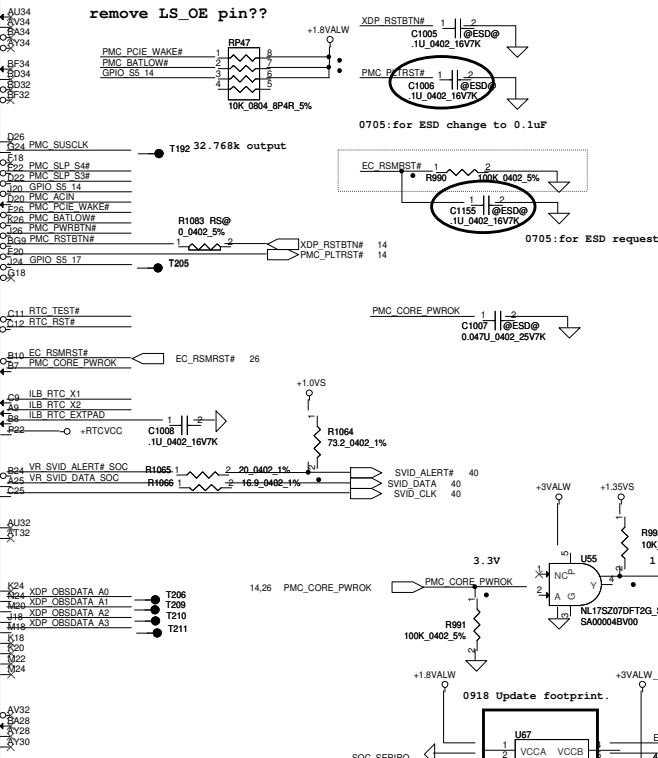
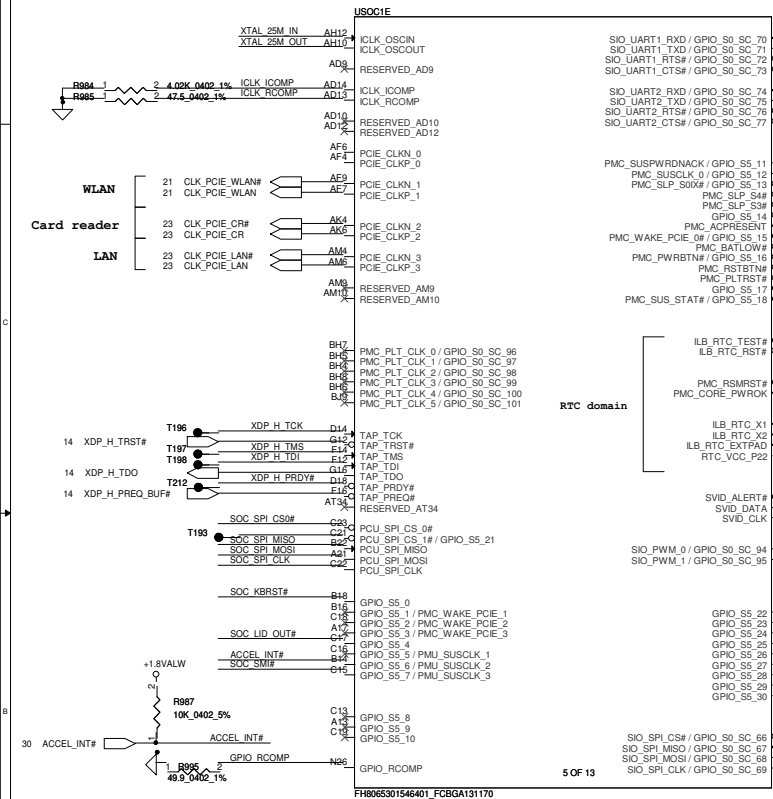
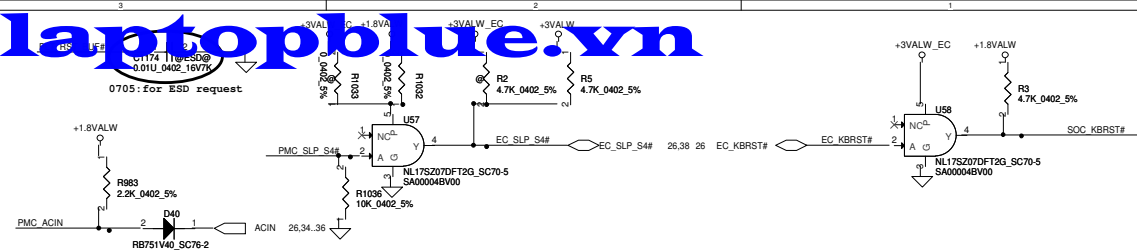
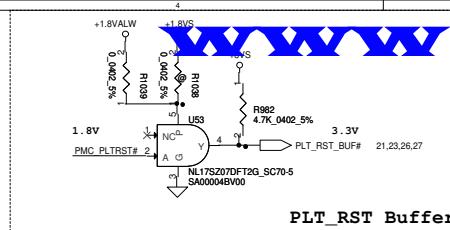
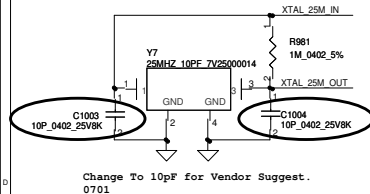
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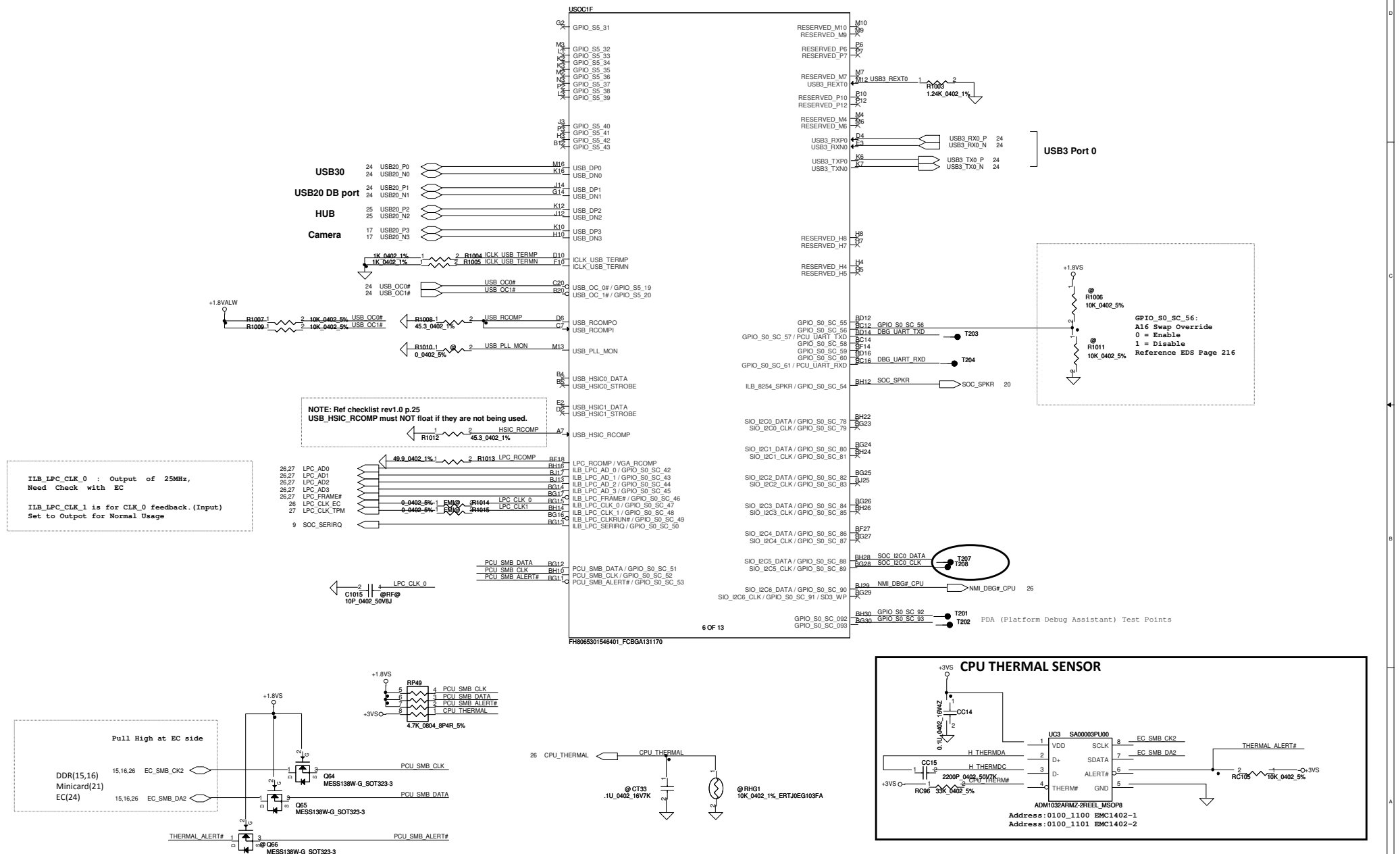


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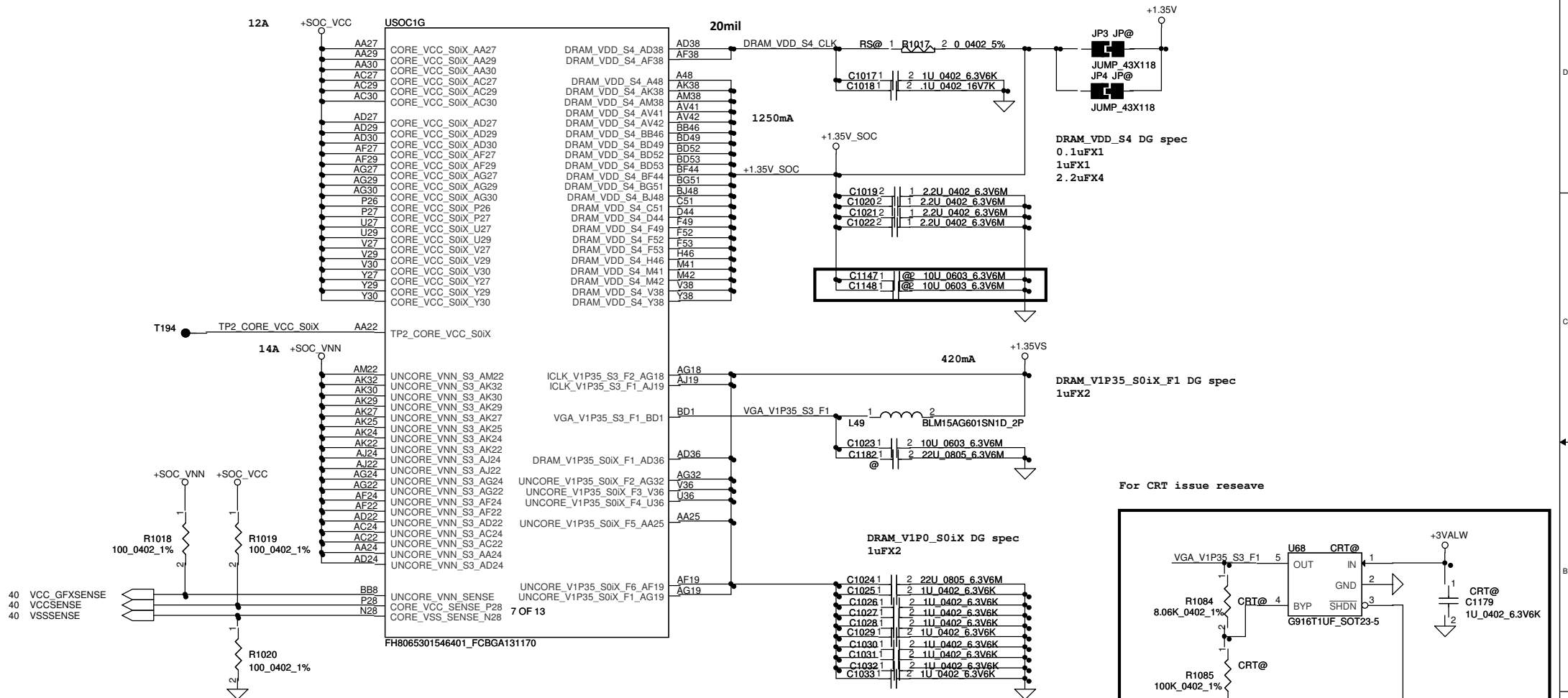




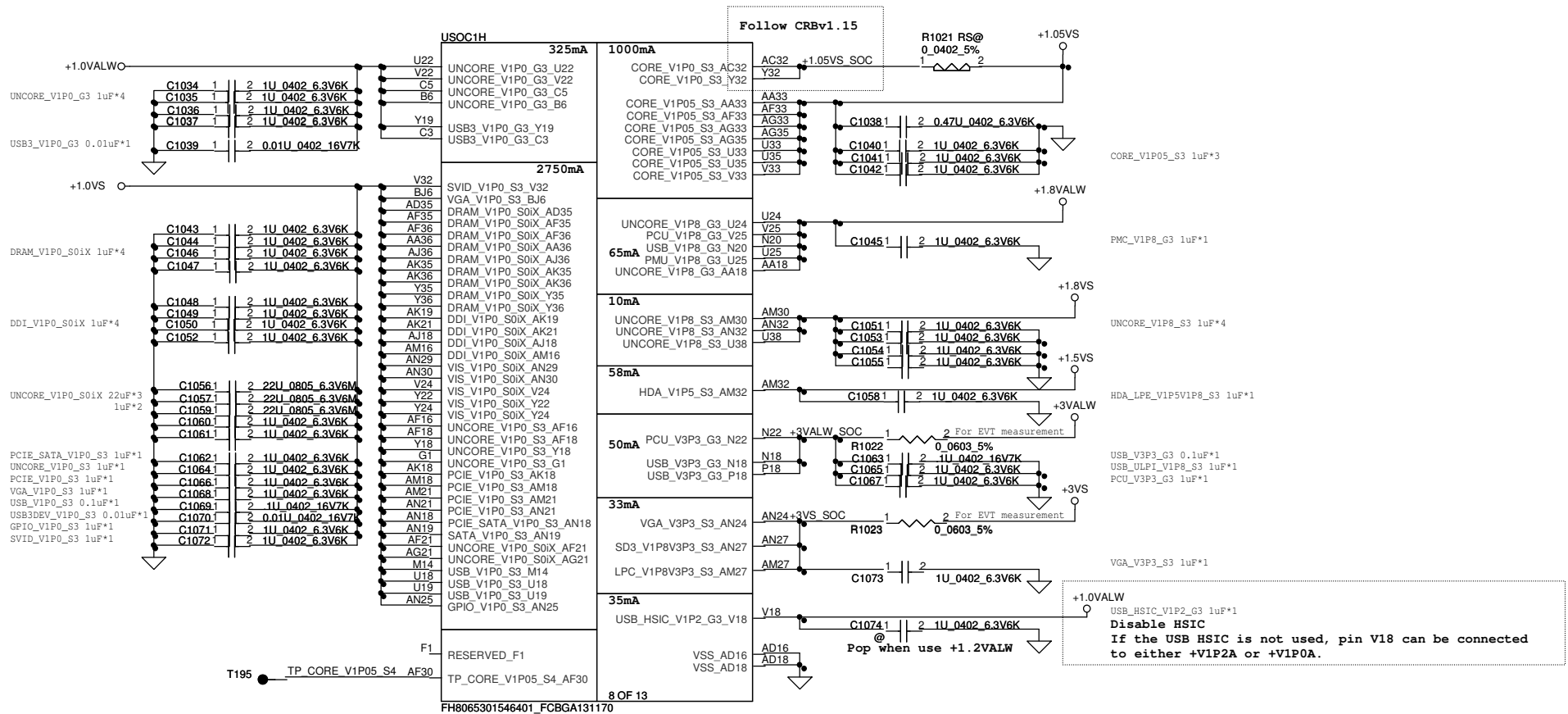
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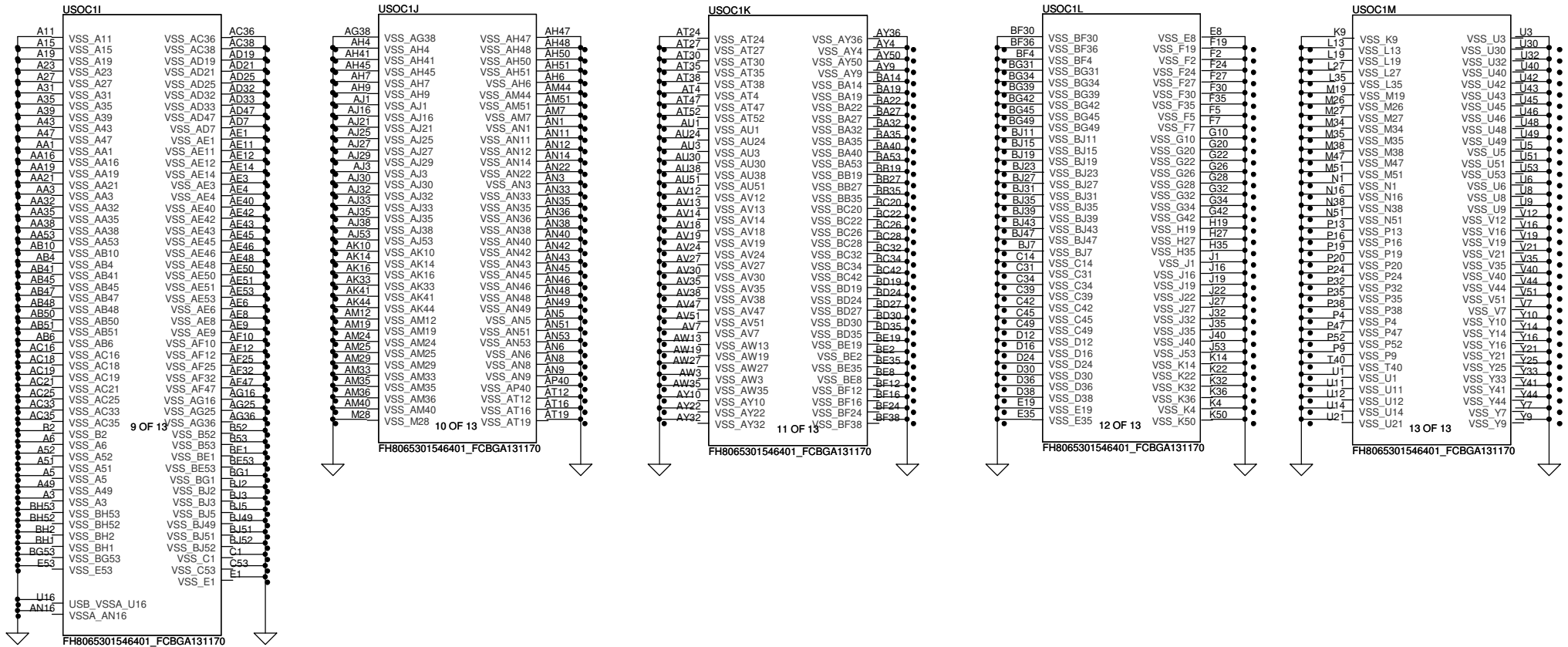
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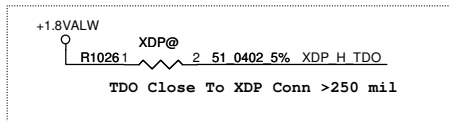
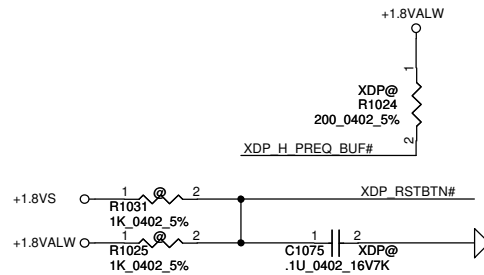
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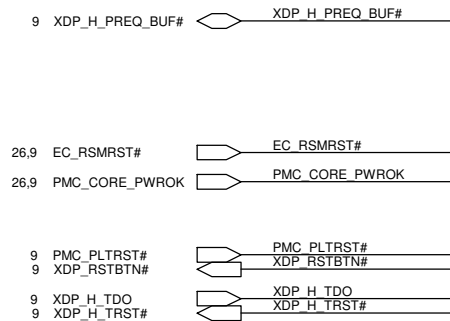
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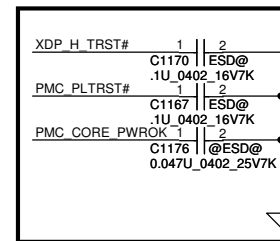
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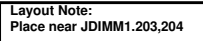
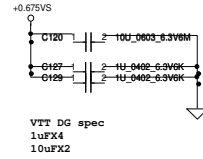
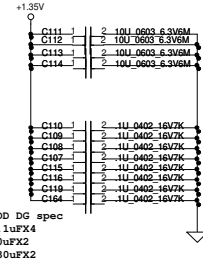
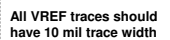
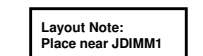
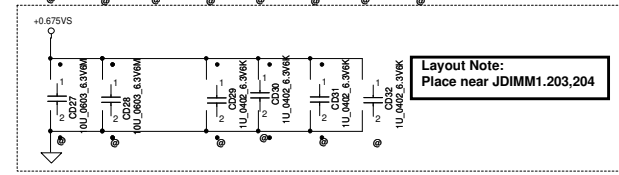
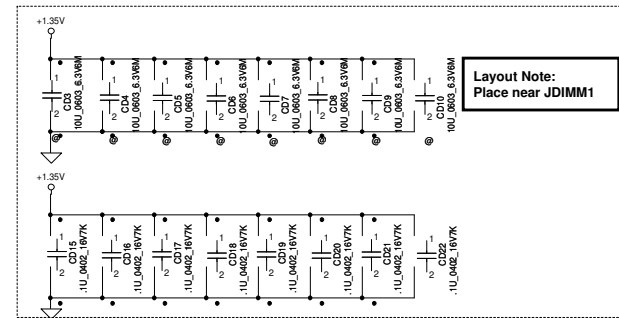
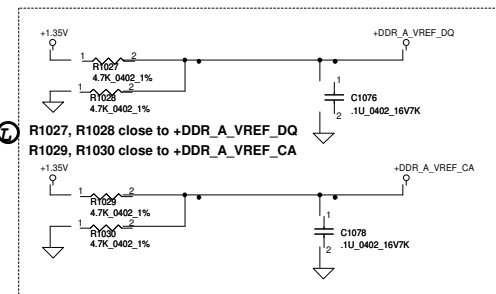
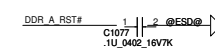
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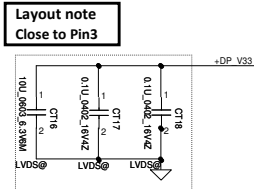
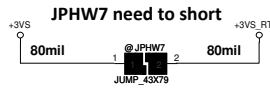
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Channel A

DIMM_1 STD H:4mm

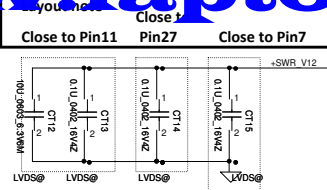
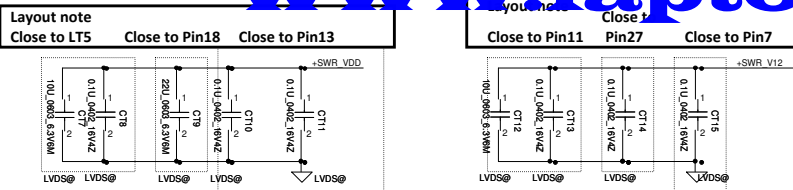
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SWR / LDO Mode select

	LDO	SWR
2132S	Do not support	mount LT7
2132R	Use 0 ohm	mount LT7

* If use 2132R, please select LDO mode as default.

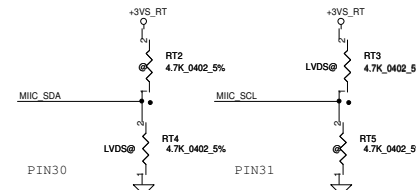


*ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.

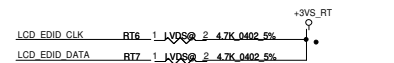
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.

EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

(*Default mode)



<CONN>



<CONN>
<CPU>

	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

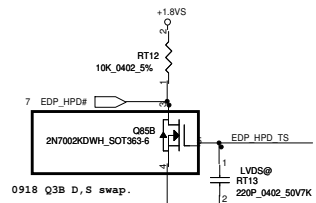
	PIN16	Accept voltage input (high level)
2132S		3.3V
2132R		1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform

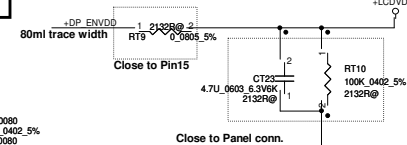
Different between 2132S and 2132R

2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

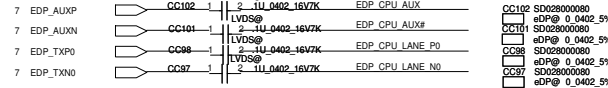
<CPU 1.8V level>



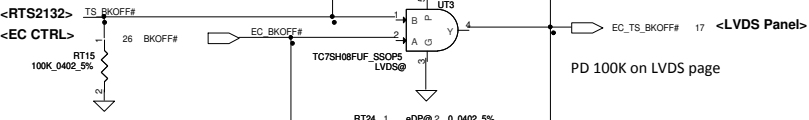
Layout note
Close to Pin8



<CPU>



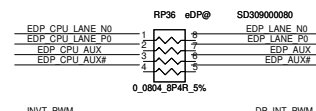
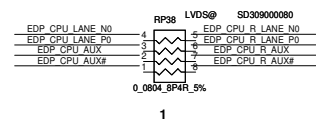
<SI> Update UT3 footprint (As UV11) 10/09



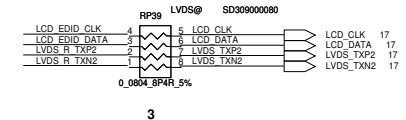
131111 add RT15 for power sequence

<LVDS panel> ==>

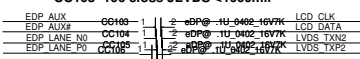
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<Translator to Conn>

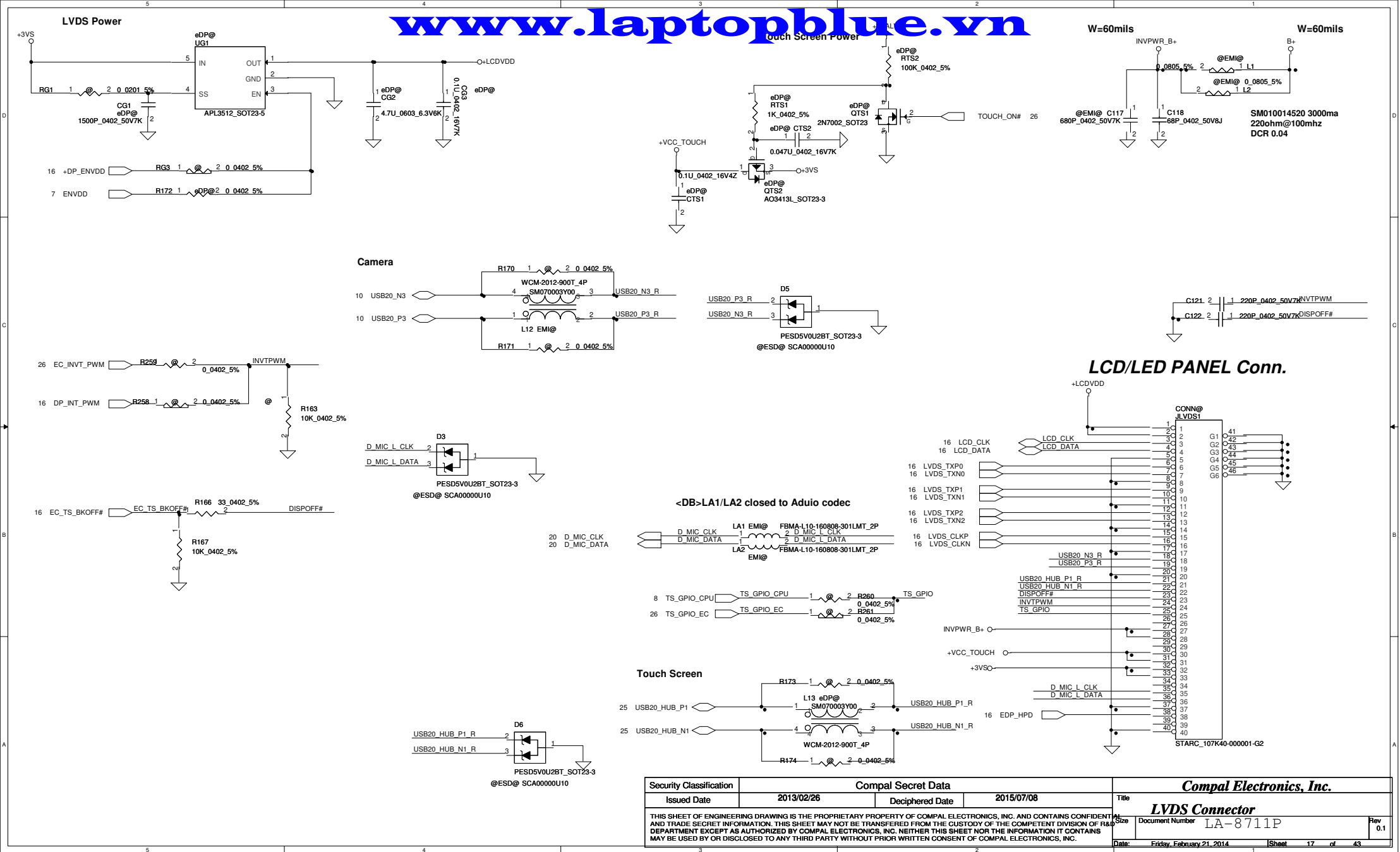


CC103~106 close JLVDS <1000mil

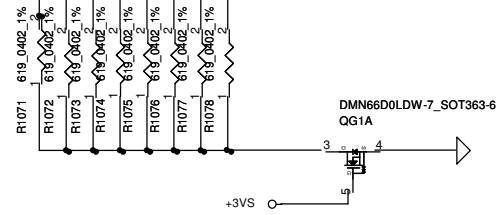
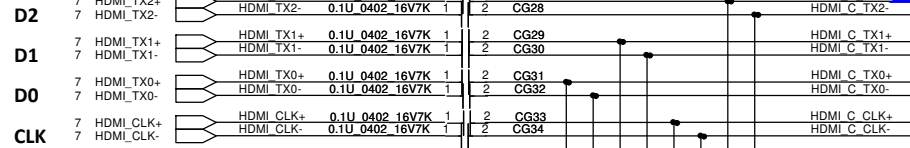


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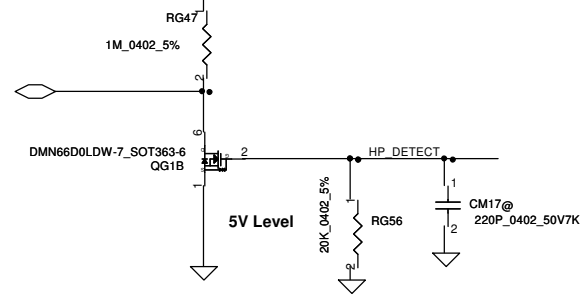
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/3/1	Deciphered Date	2015/3/1	Title	LVDS Translator-RTD2132R
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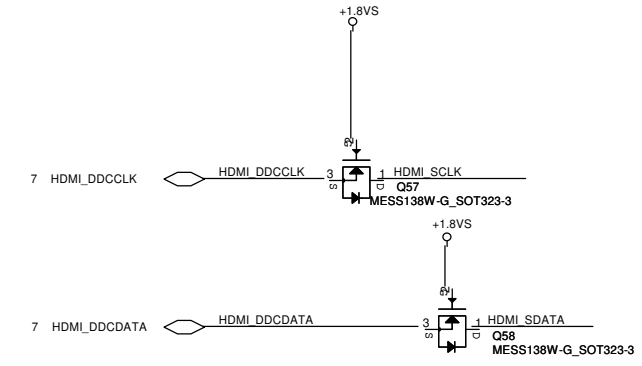
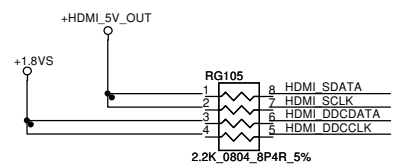
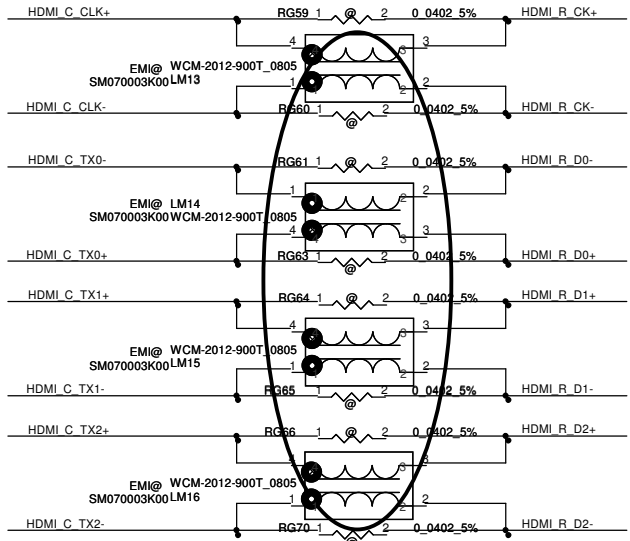
<CPU>



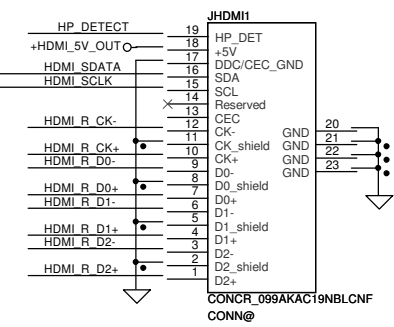
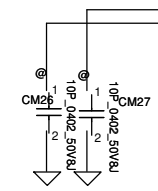
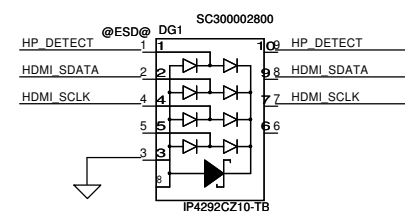
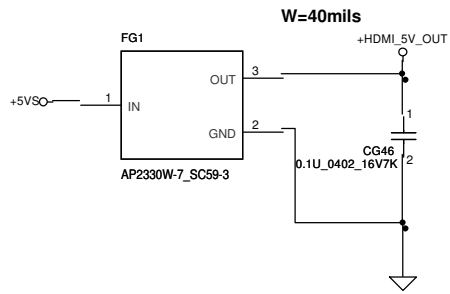
7 HDMI_HPD#



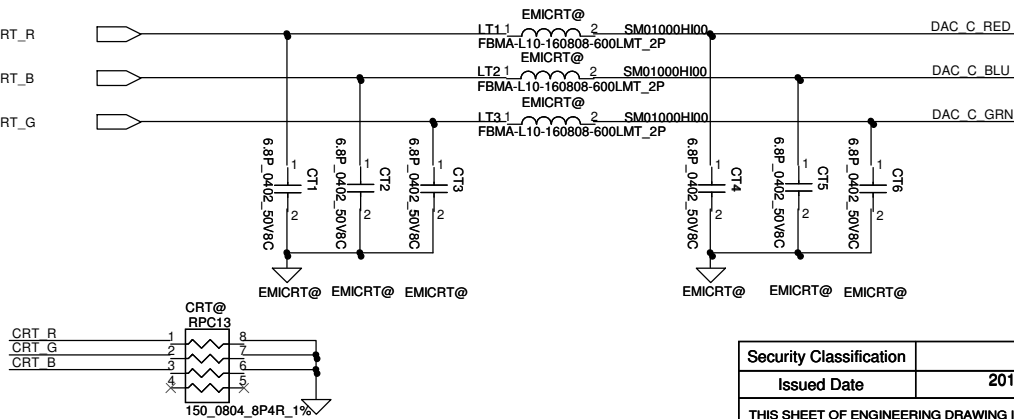
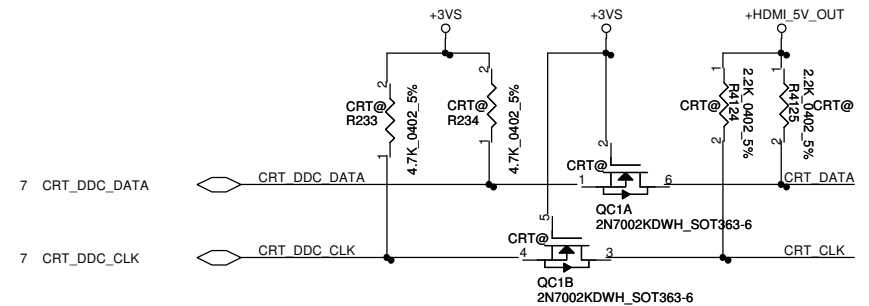
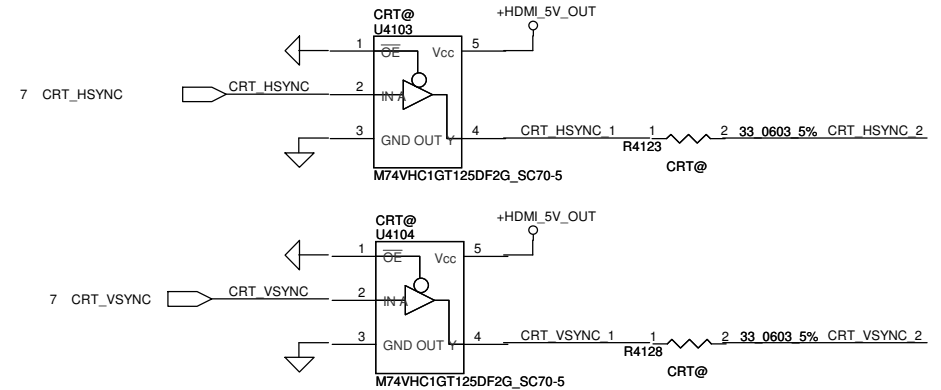
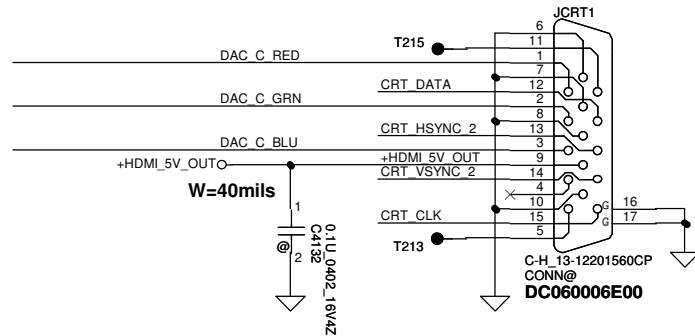
10/21 BOM change SM070003K00



HDMI Conn.

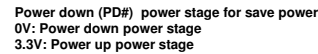


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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	
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Size		Document Number		Rev	
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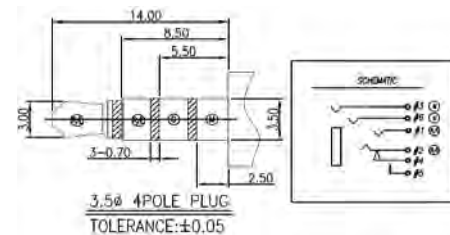


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2013/02/26		Deciphered Date		2015/07/08		Title	
										CRT Connector	
										Document Number	
										LA-A994P	
										Rev	
										0.1	
										Date: Friday, February 21, 2014	
										Sheet 19 of 43	

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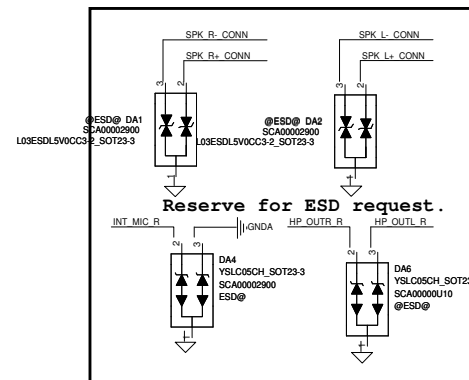


Close to Codec pin12

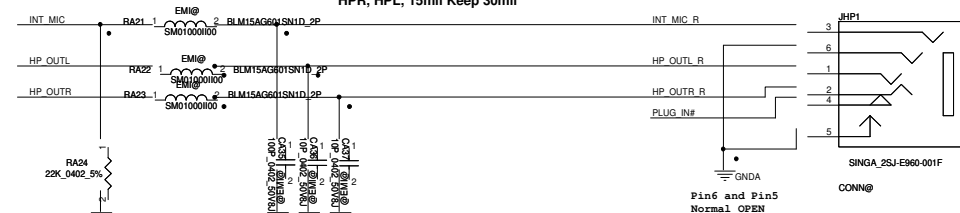


<DB>KELACE KA13/KA14/KA15/KA16 CLOSE TO OAL

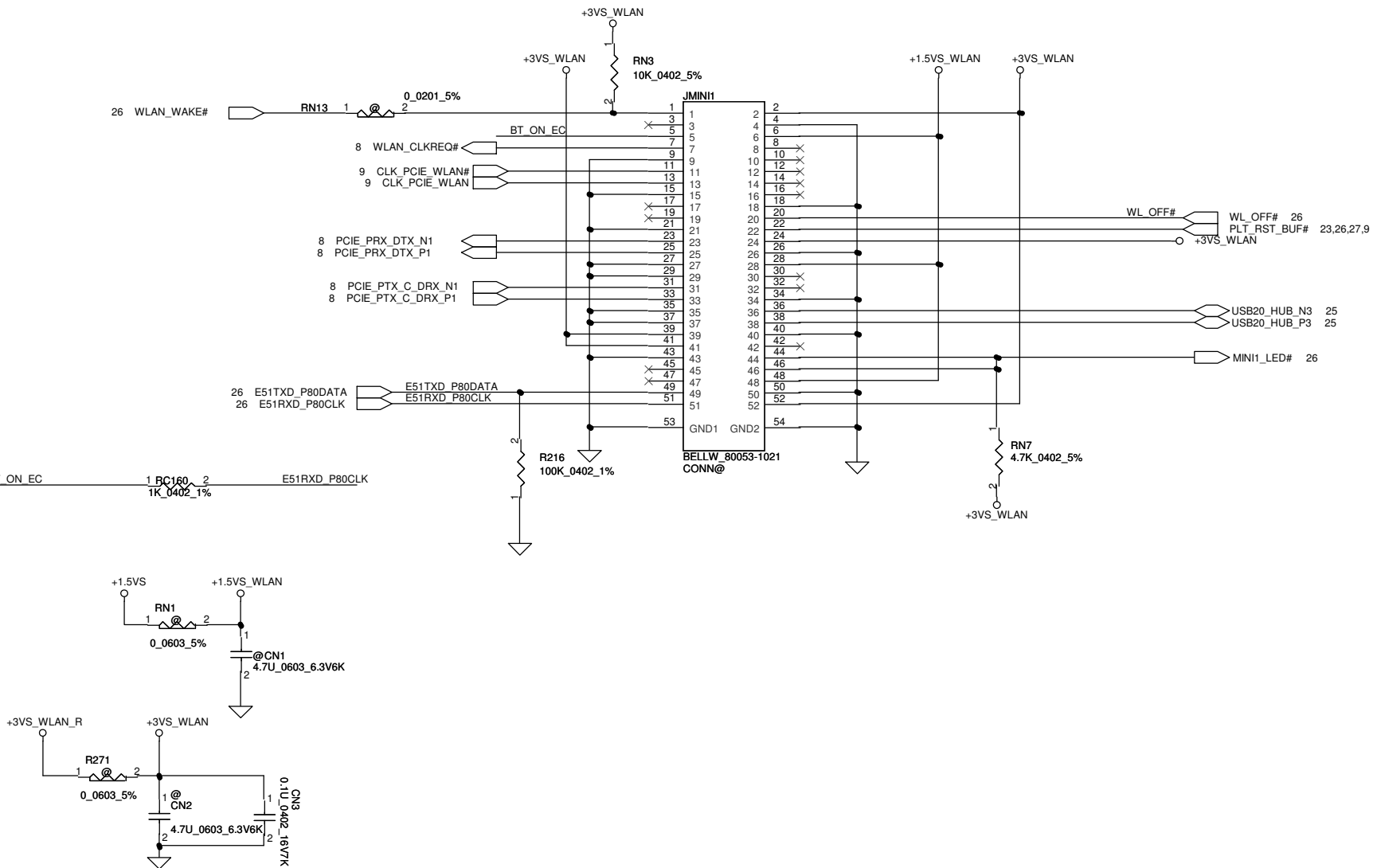
wide 40 MIL Delete ESD Diode



HPR, HPL, 15mil Keep 30mil

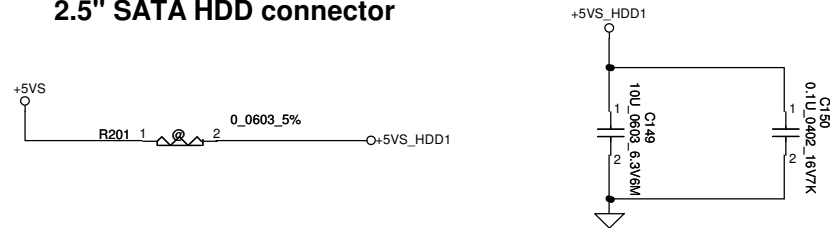


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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		Deciphered Date		2015/01/04	
				AUDIO ALC259-VC2-CG	
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				Document Number	
				LA-A992P	
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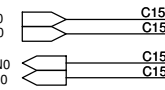


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	WLAN
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2.5" SATA HDD connector



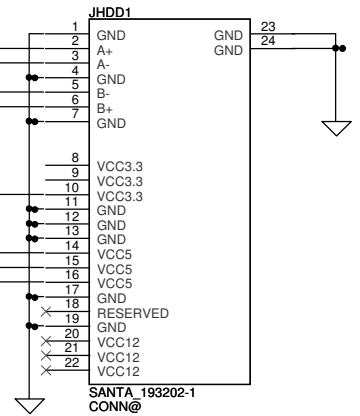
8 SATA_PTX_DRX_P0
8 SATA_PTX_DRX_N0



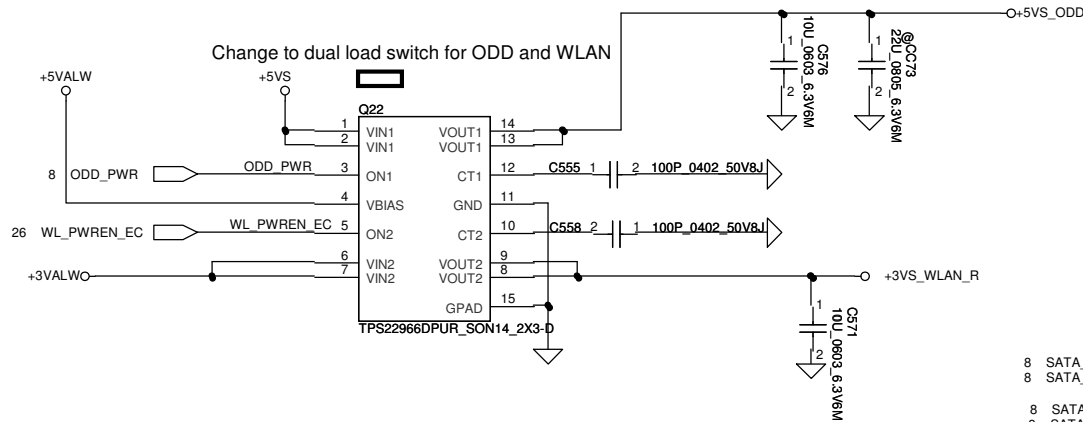
10/22 RS11 Change to un pop

+3VS RS11 1 2 0.0402 5% JHDD P10

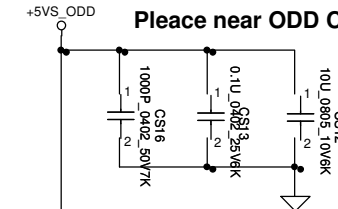
+5VS_HDD1C



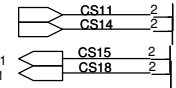
Change to dual load switch for ODD and WLAN



Place near ODD Connector

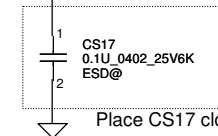


8 SATA_PTX_DRX_P1
8 SATA_PTX_DRX_N1
8 SATA_PRX_DTX_N1
8 SATA_PRX_DTX_P1

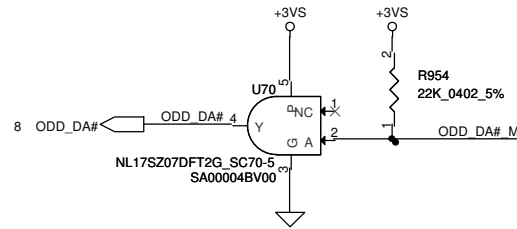
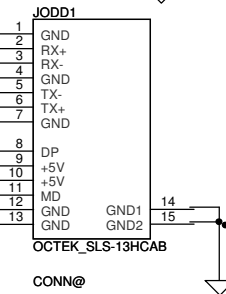


8 ODD_PLUG#

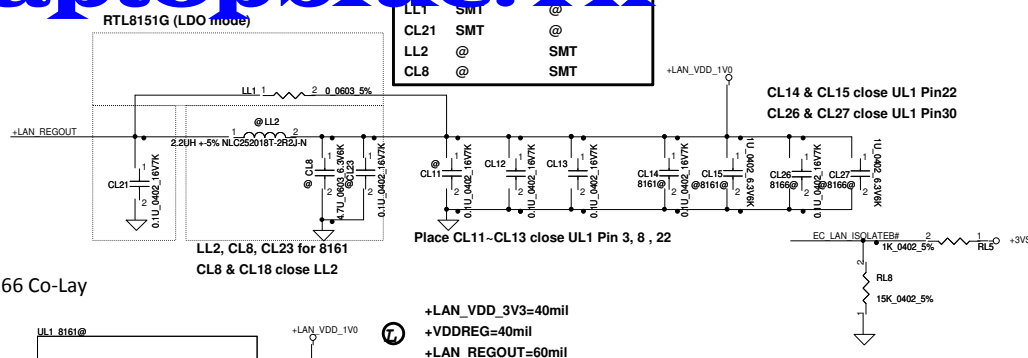
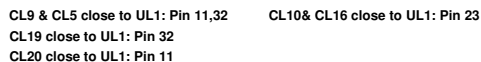
ODD DA# M



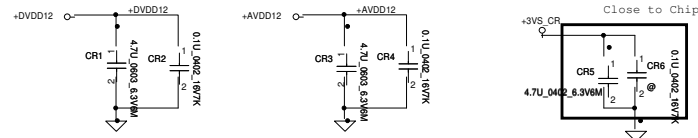
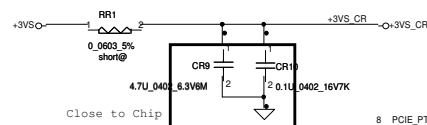
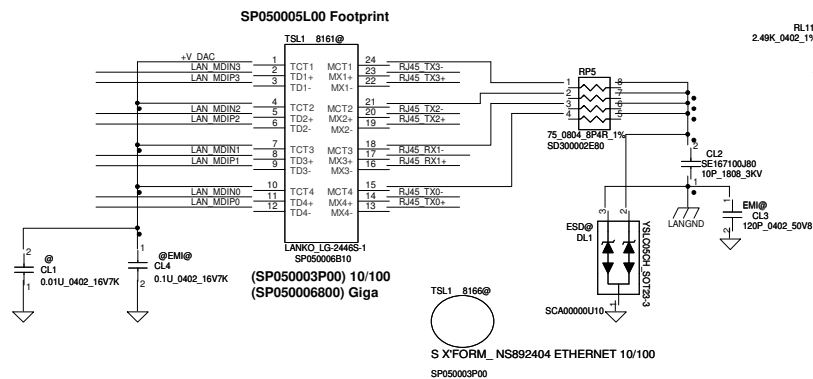
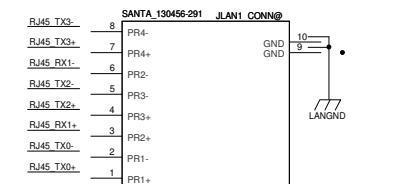
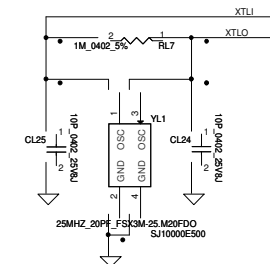
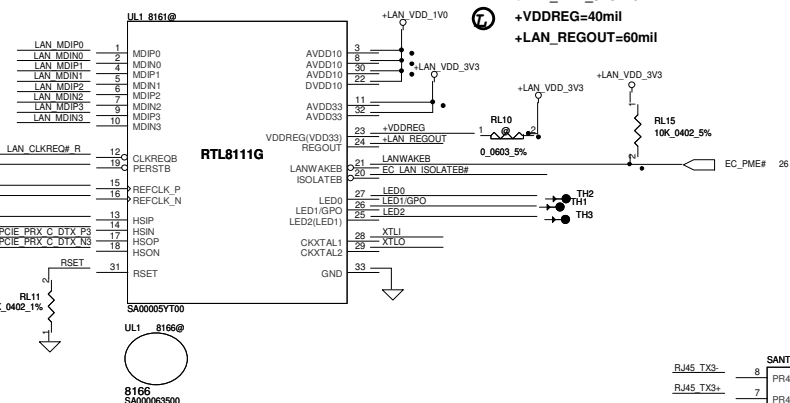
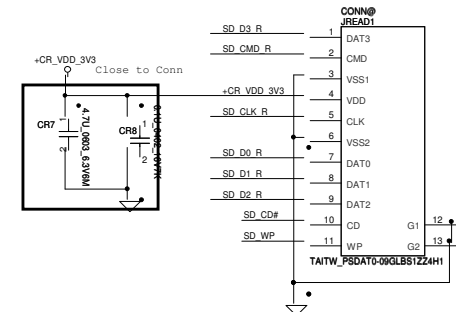
Place CS17 close to JODD



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				Date:	Friday, February 21, 2014
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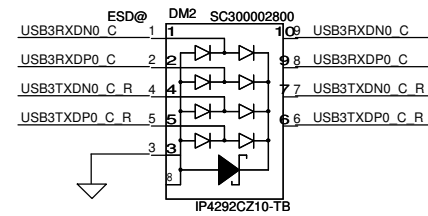
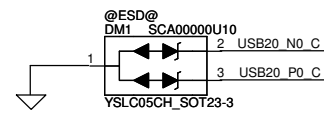
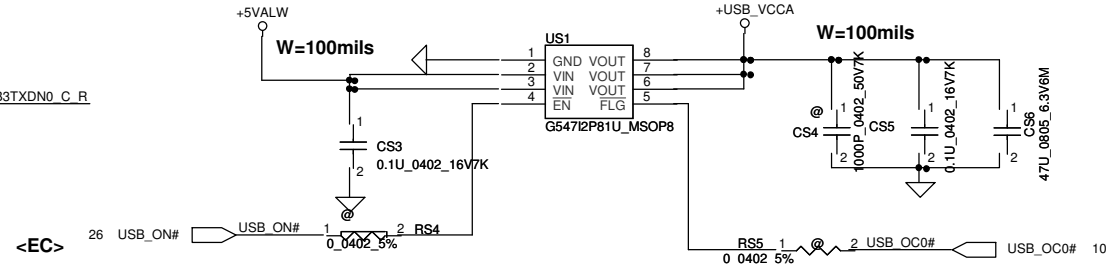
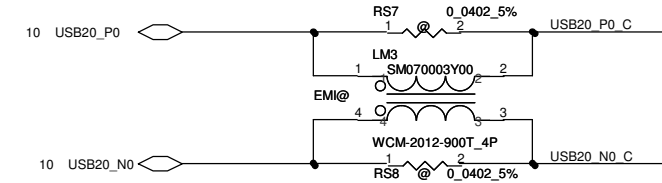
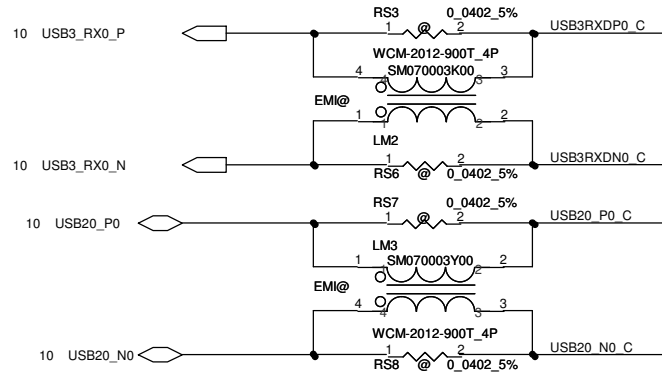
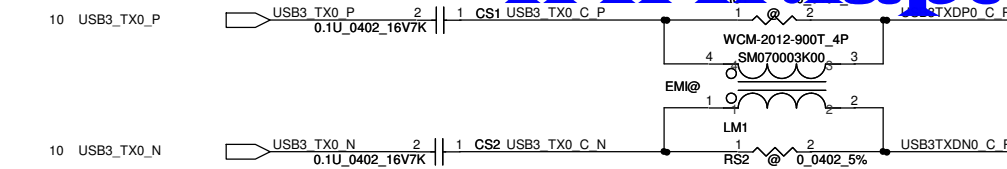


8151/8166 Co-Lay

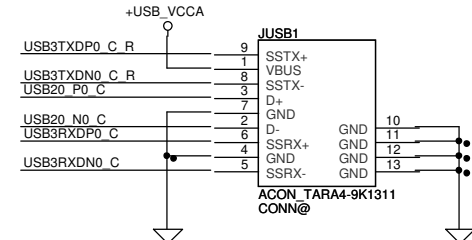
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					LA-A992P	0.
				Date:	Friday, February 21, 2014	Sheet 23 of 43

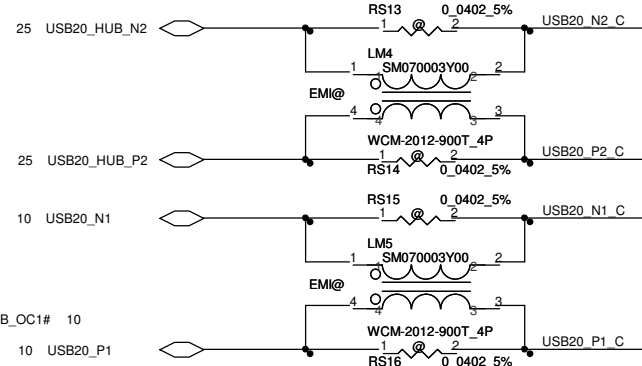
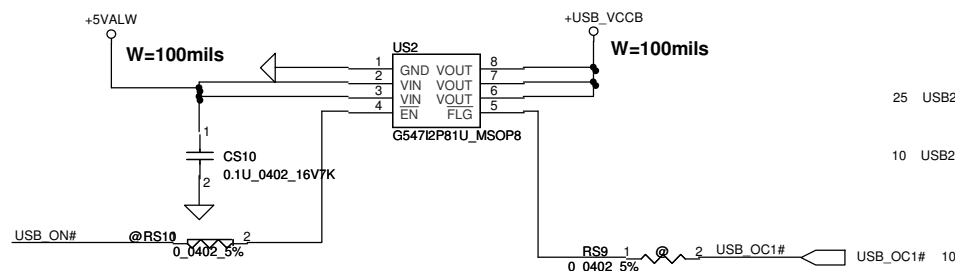
USB 3.0 support 2.5A
change USB PWR SW SA00003TV00
low active



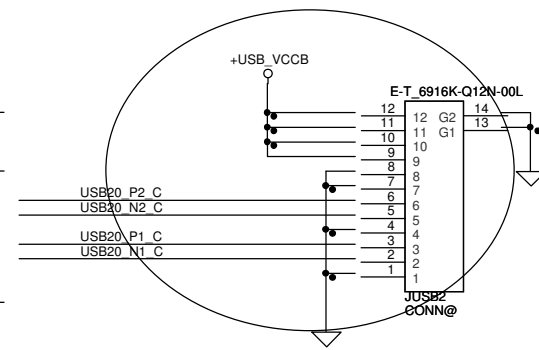
USB2.0/USB3.0 port 1



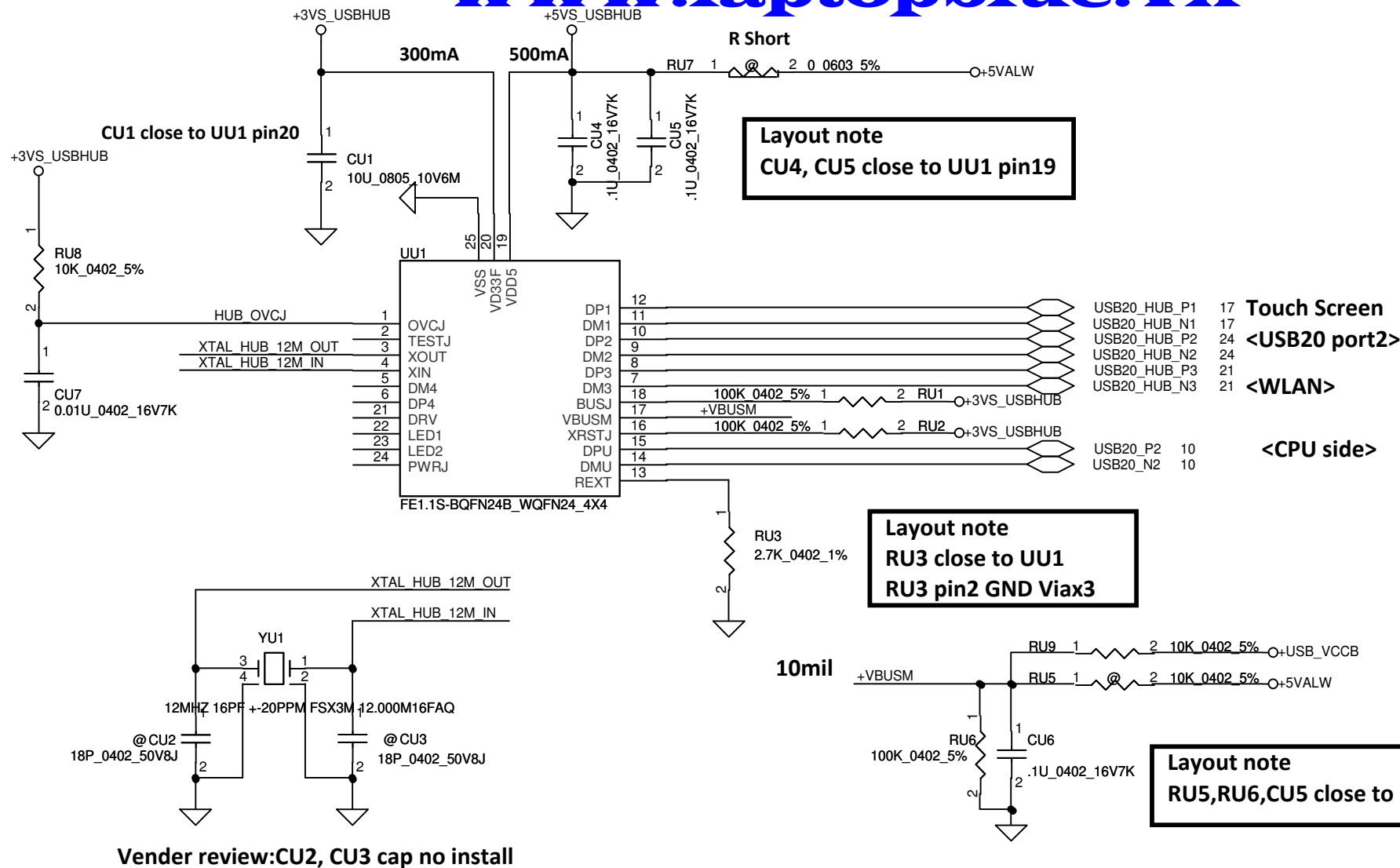
USB2.0 port x 2



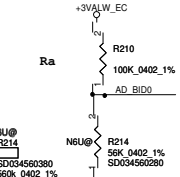
131109 Follow 15" Haswell LA-A992PR02



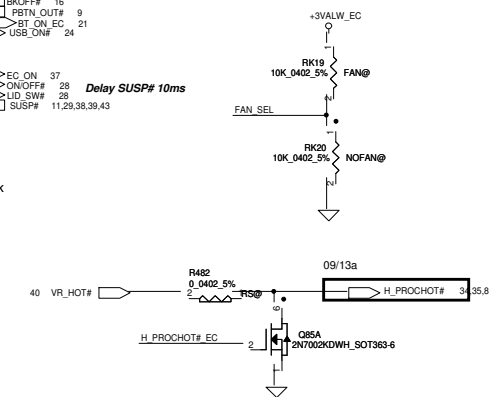
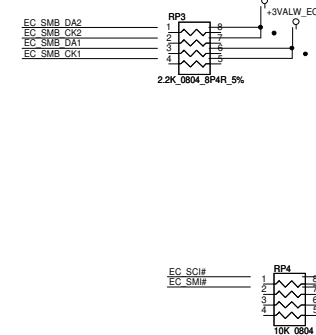
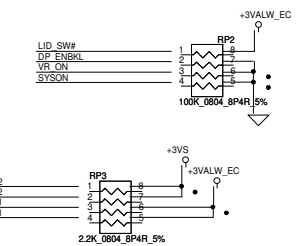
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	
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		LA-A994P			0.1
Date:		Friday, February 21, 2014		Sheet	25 of 43

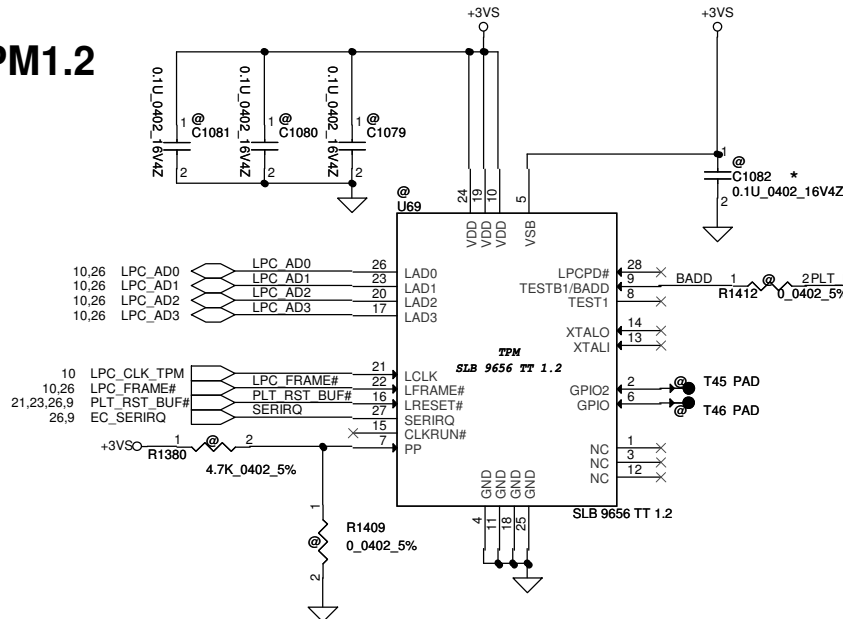


15" 6U	DB	SI	PV	MV
Board ID R214	NA	NA	330K ohm	560K ohm
Project ID R210	NA	NA	100k ohm	100k ohm

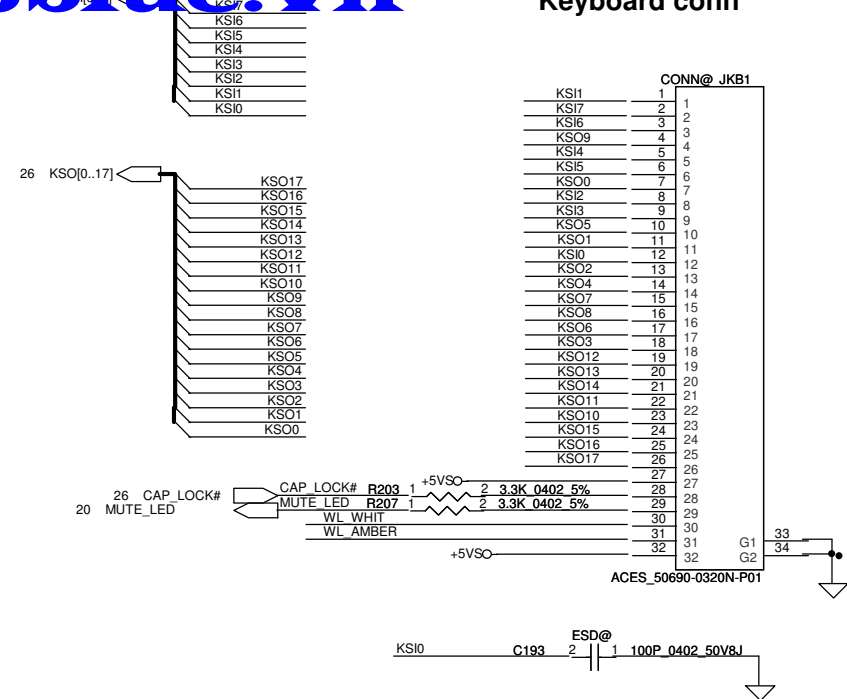


TP CLK
TP DATA 4.7K 0402 5%
4.7K 0402 5%
+3VALW
R244
R245

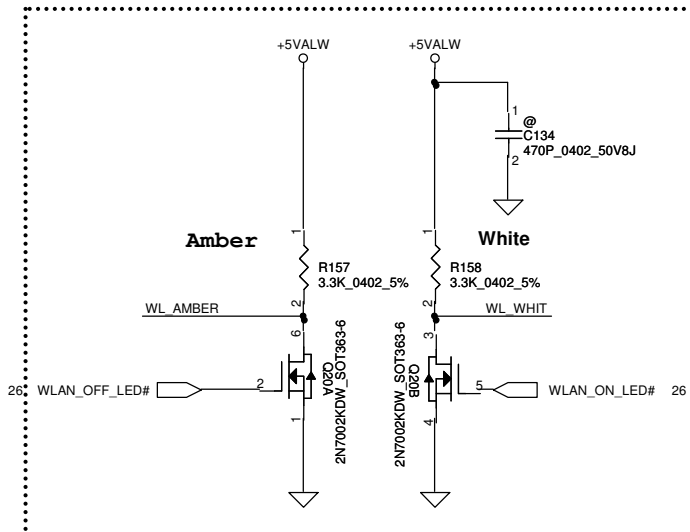
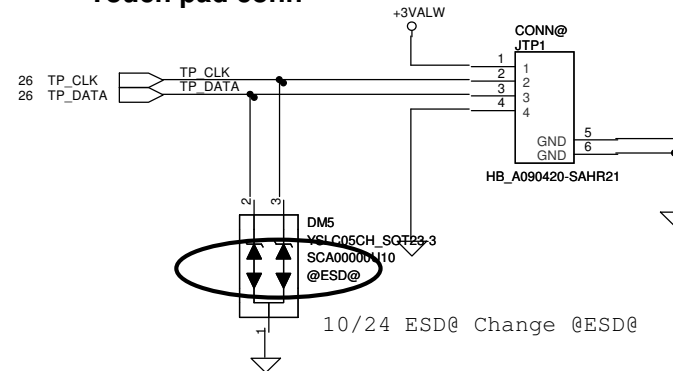
TPM1.2



Keyboard conn

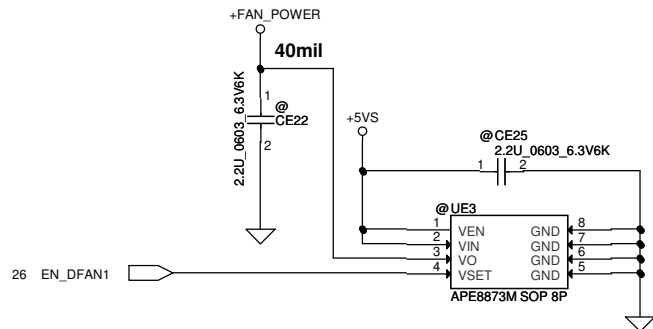
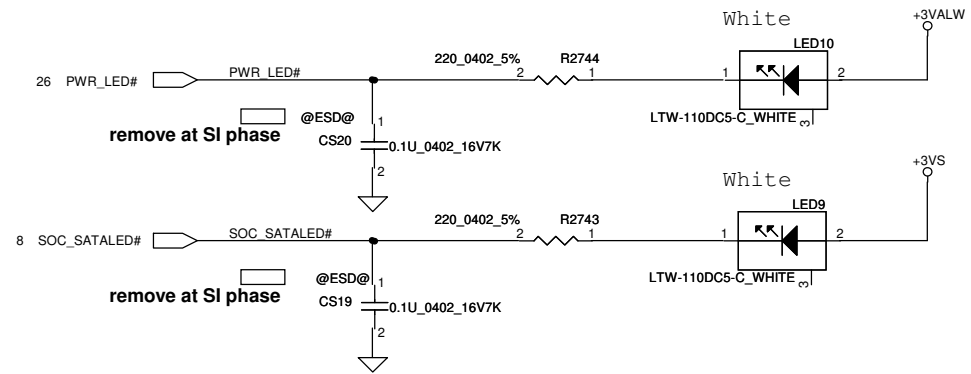
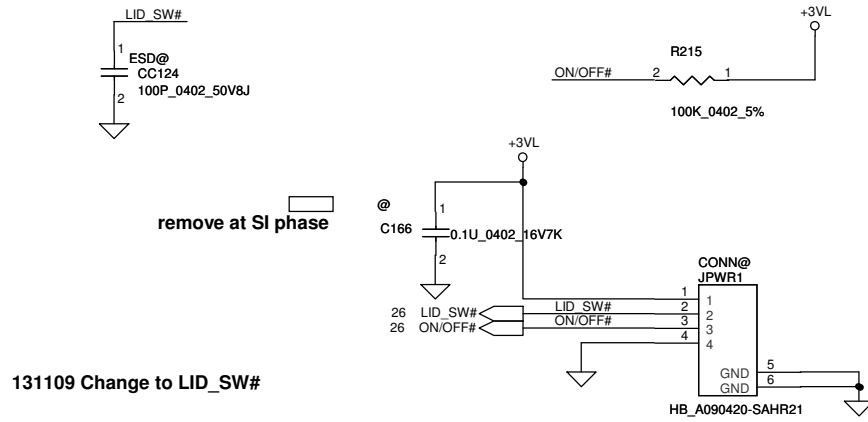


Touch pad conn

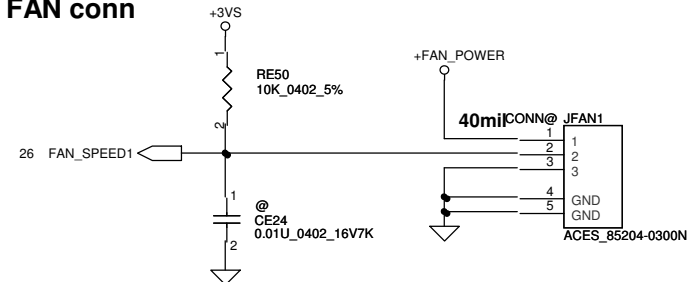


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Power Button Connector

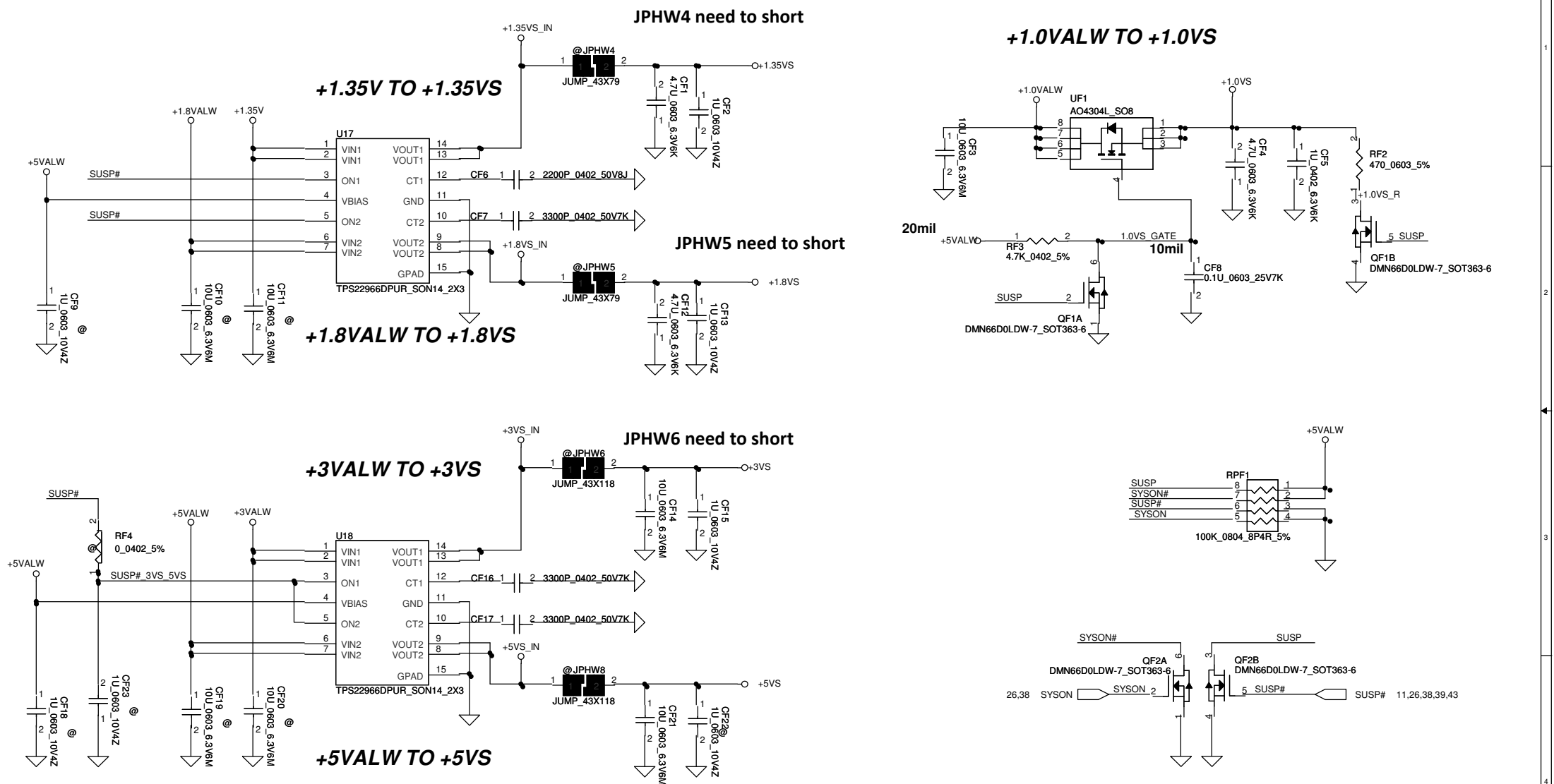


FAN conn



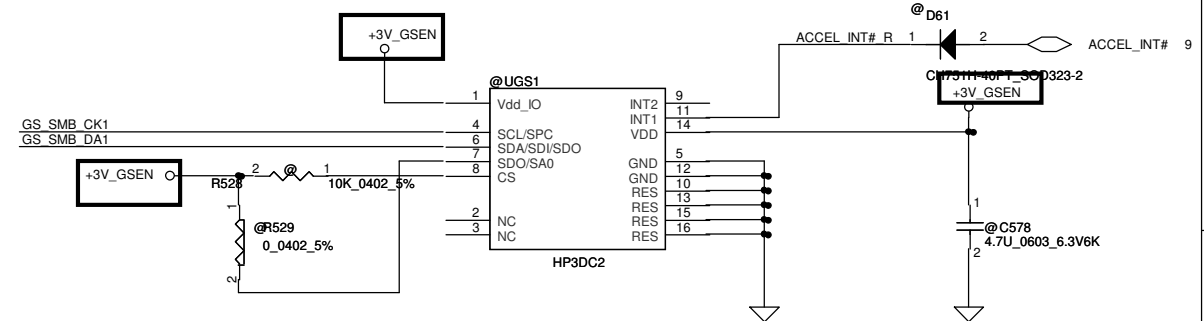
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					Date:	Friday, March 14, 2014	Sheet 28 of 43

Bay trail M new power up sequence

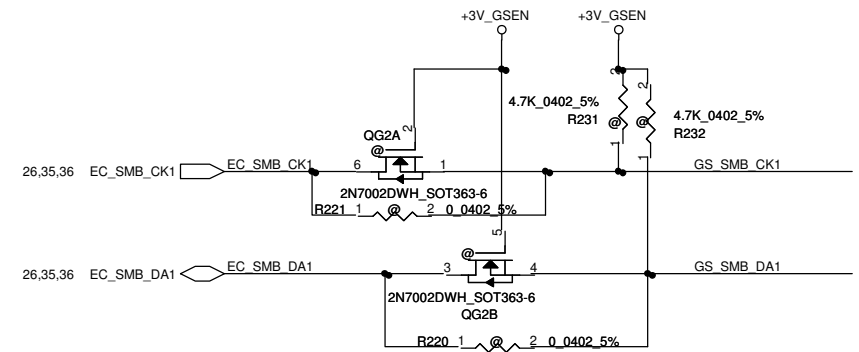


10/21 +3VALW Change +3VL

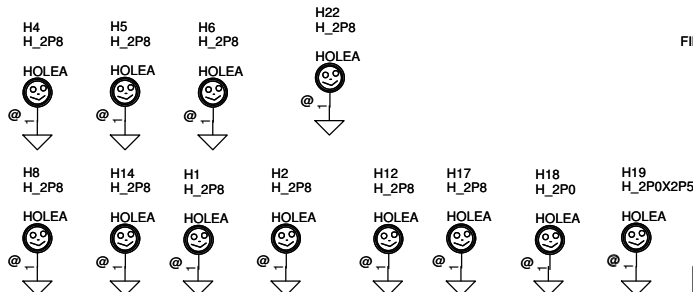
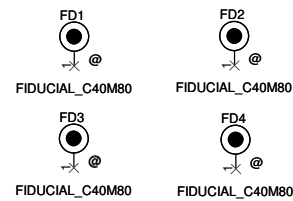
ACCELEROMETER



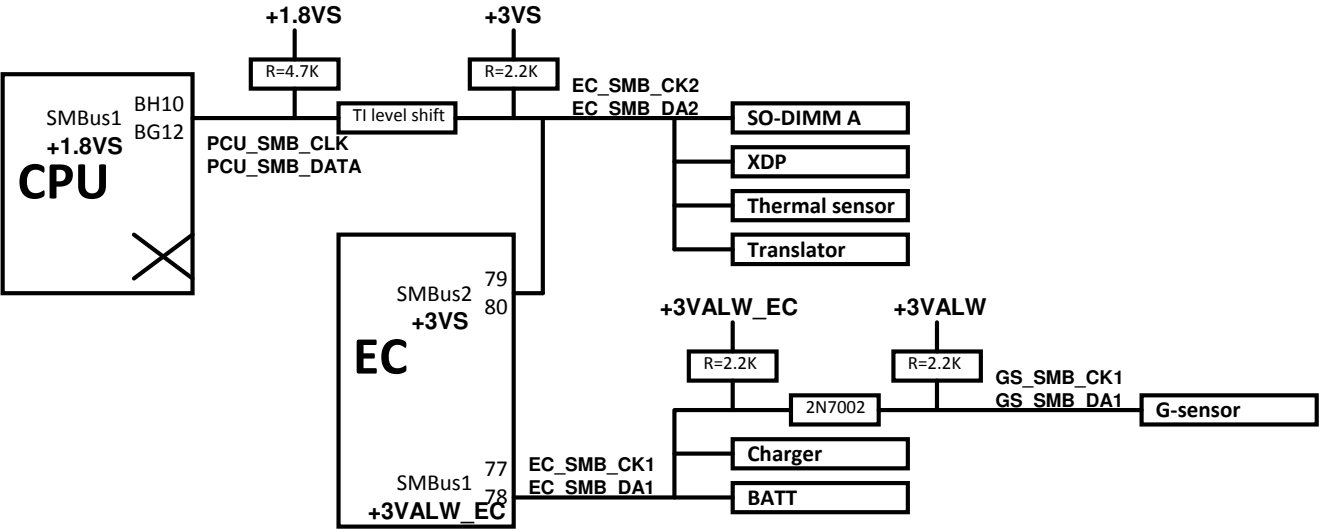
(L) Must be placed in the center of the system.



Reserve MOS for power leakage



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USB2.0	USB3.0	Function	Note
0	X	Left port (USB2.0)	
1	0	Right port-1 (USB2.0/3.0)	
2	X	Right port-2 (USB2.0)	
3	X	WLAN	USB2.0x4 Hub
4	X	Touch screen	USB2.0x4 Hub
5	X	Camera	USB2.0x4 Hub
6	X	NC	USB2.0x4 Hub

<PCI-E port>

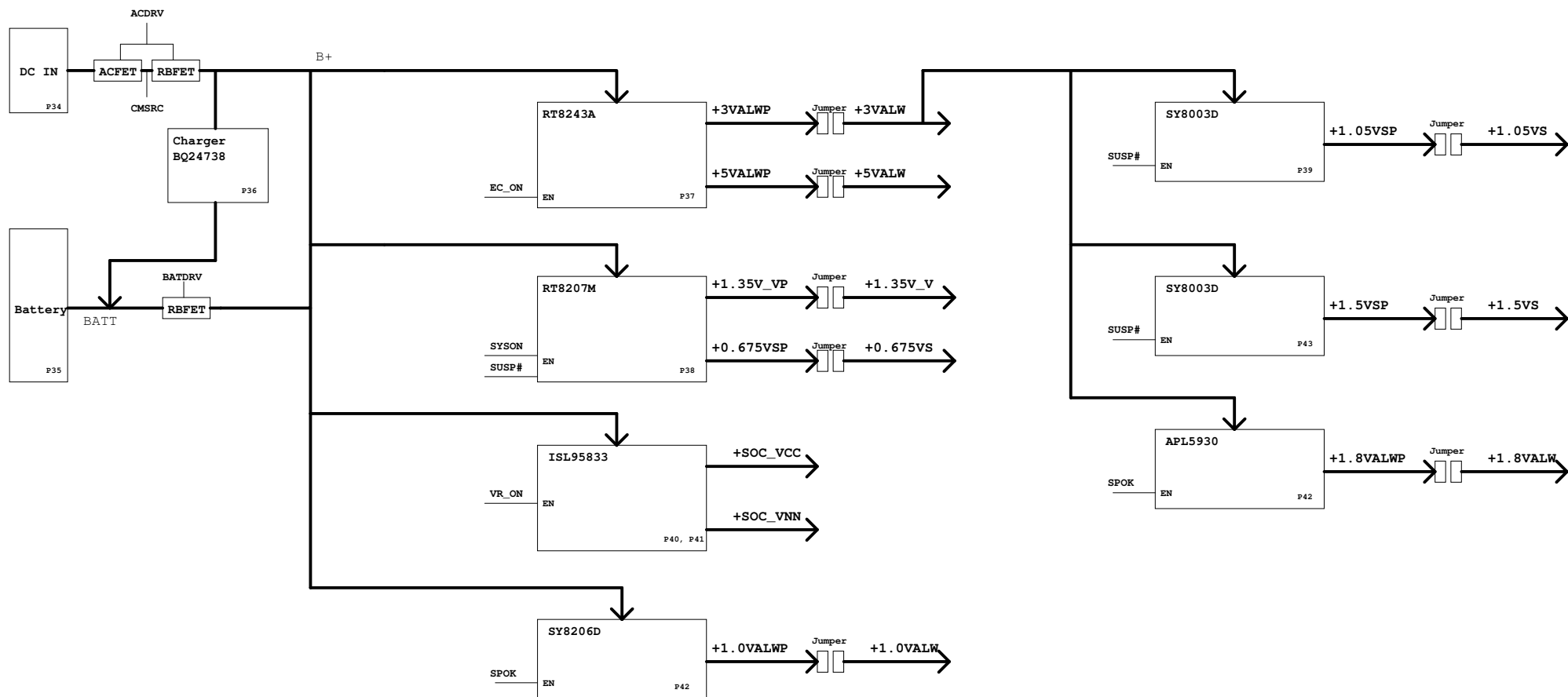
PCI-E	Function	Note
0	LAN	
1	WLAN	
2	Card reader	
3	NC	

<SATA port>

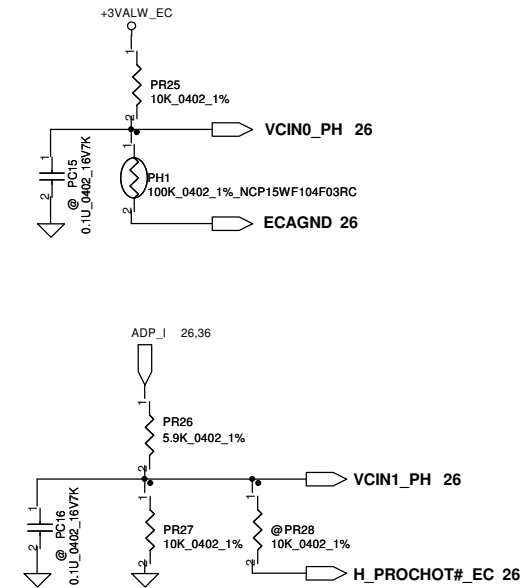
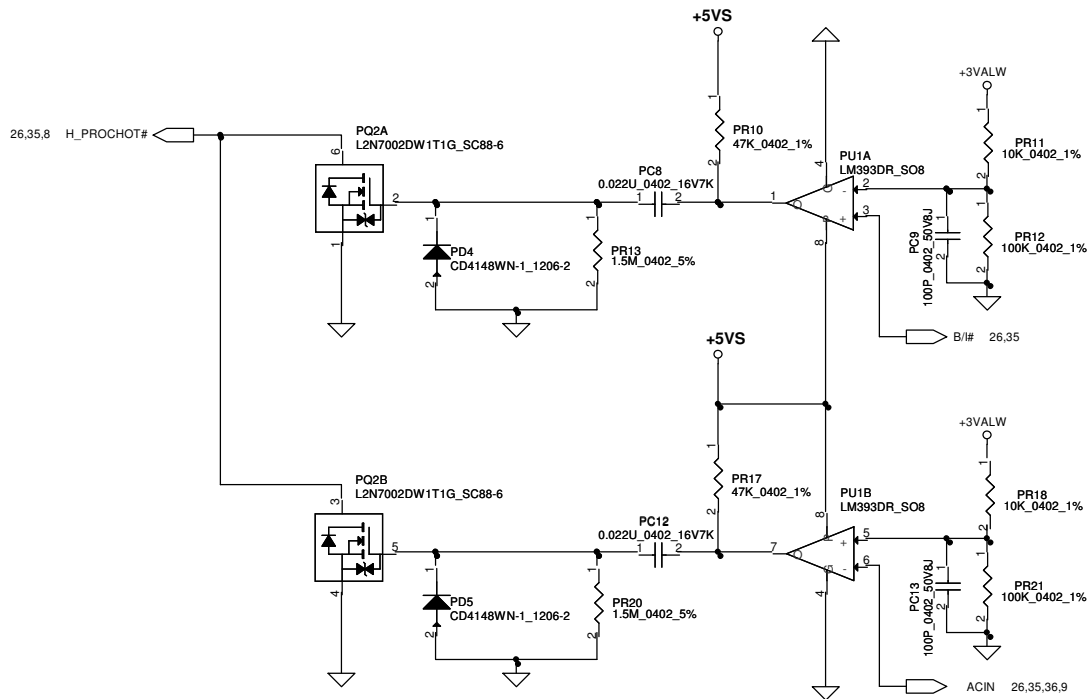
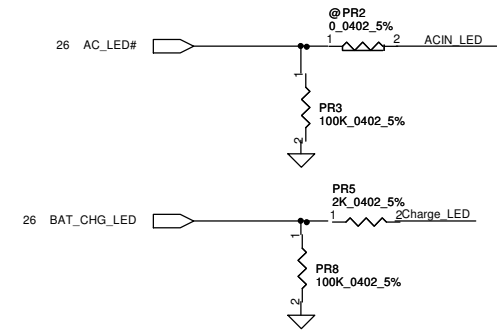
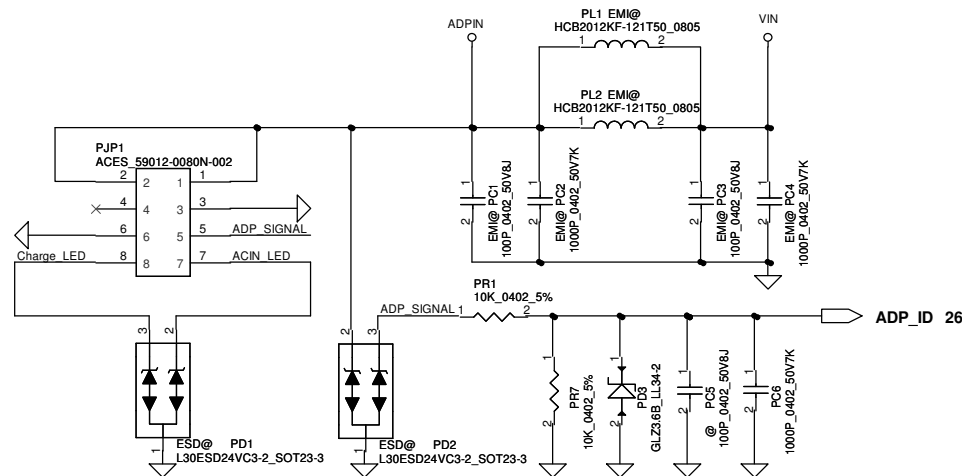
PCI-E	Function	Note
0	HDD	
1	NC	

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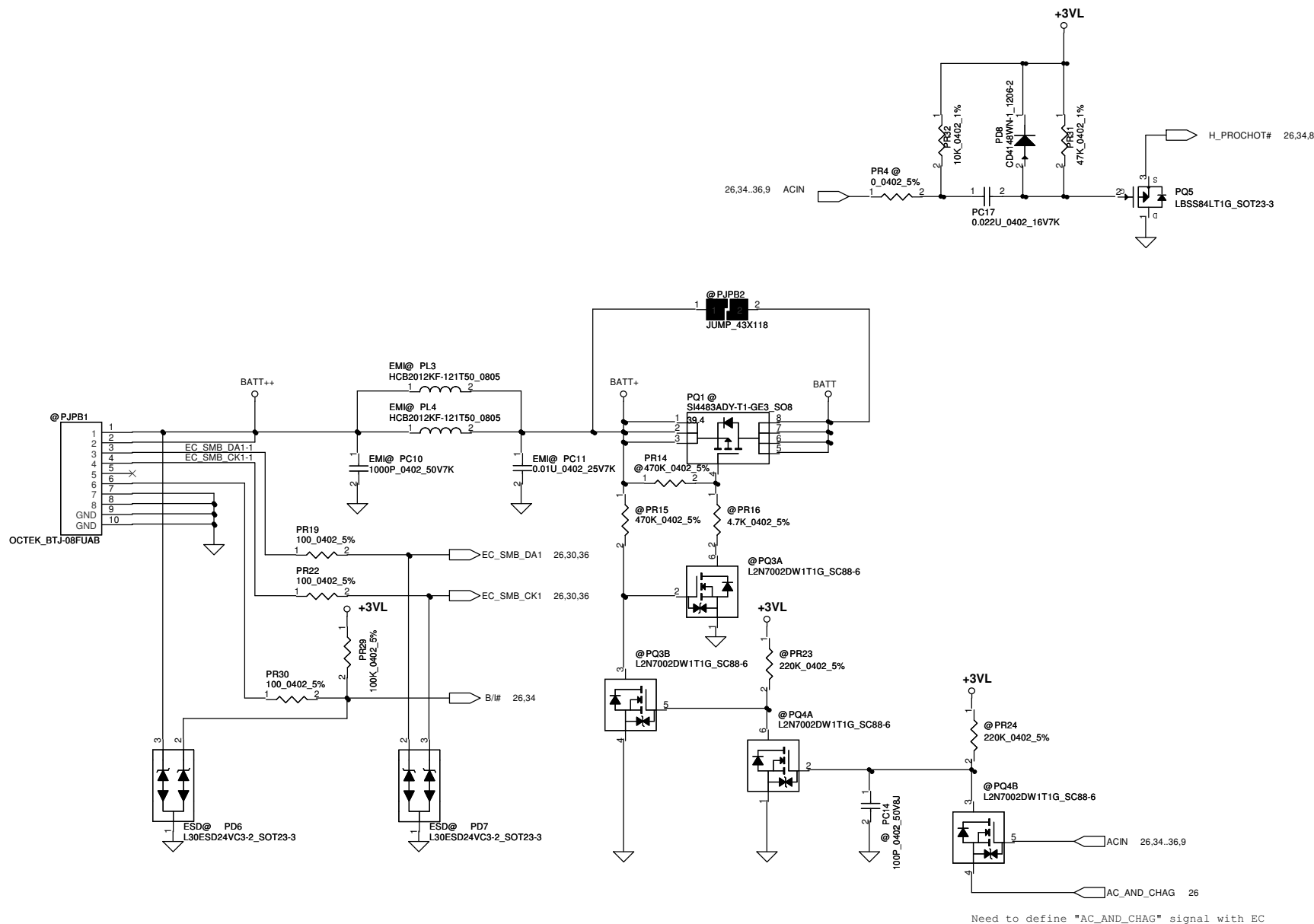
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29		131107		1.Change PN of RPF1 from SD302100380 to SD309100380		
2	28		131109		1.Change Control pin of LID from NEW_LID_SW(R218) to LID_SW#(R219)		
3	24		131109		1.Follow 14" Haswell LA-A993PRO2's USB2 Conn.		
4	16		131111		1.Update UT3 footprint follow Haswell platform		
5	22		131111		1.Delete R954 ,Q84 for ODD_DA# 2.unpop RS11		
6	18		131111		1.Change PN of LM13,LM14,LM15 & LM16 from SM070001V00 to SM070003K00		
7	30		131111		1.Change Power Rail of G sensor from +3VALW to +3VL & unpop QG2		
8	30		131111		1.pop DM5		
9	26		131111		1.change Board ID to SI phase		
10	16		131111		1.add PD 100K RT15K for power sequence		



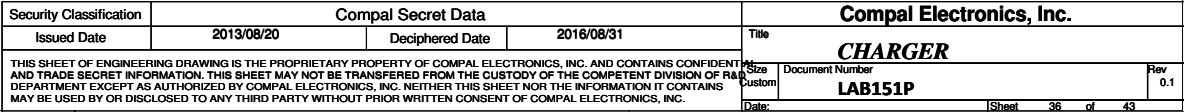
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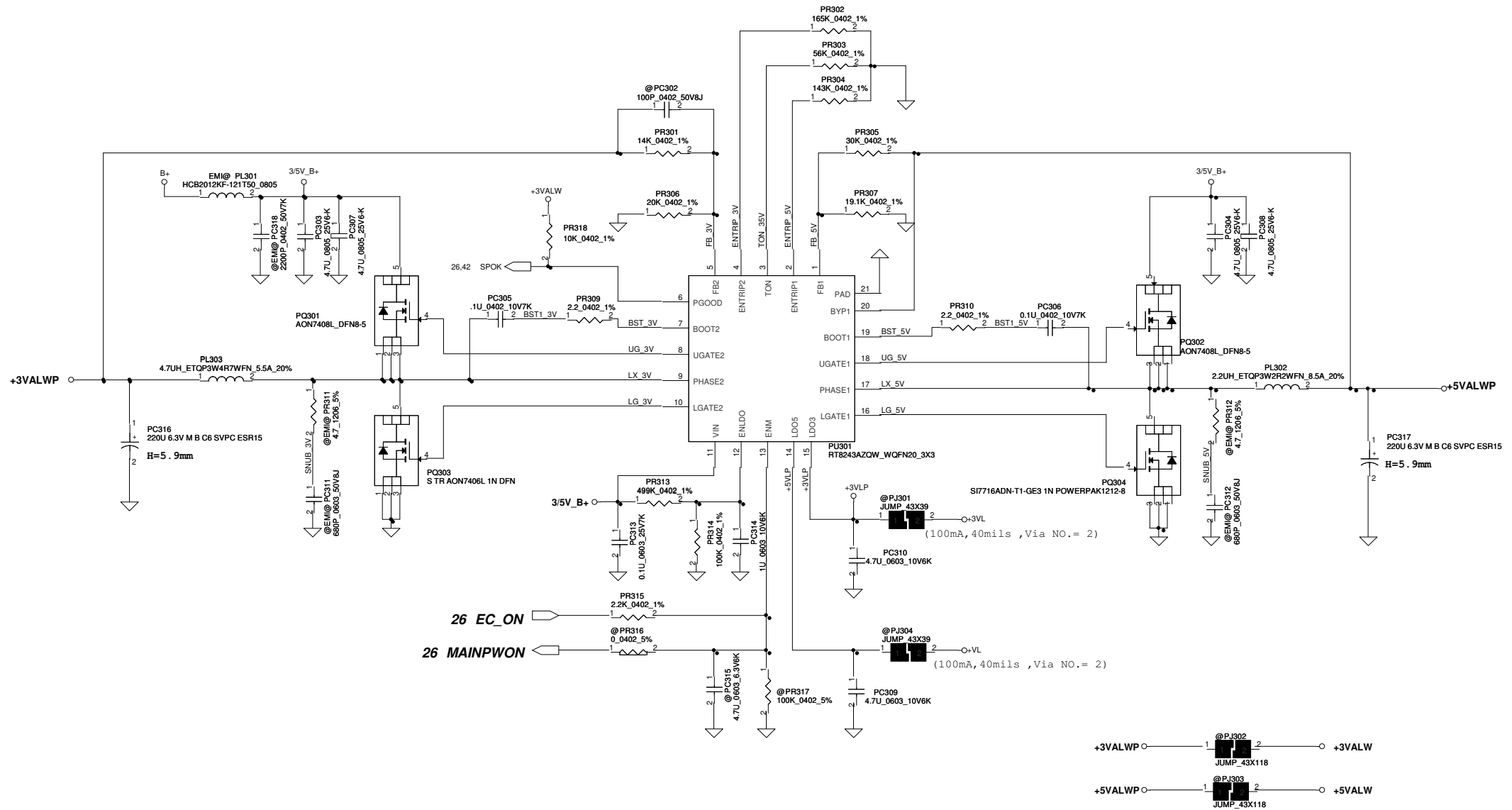


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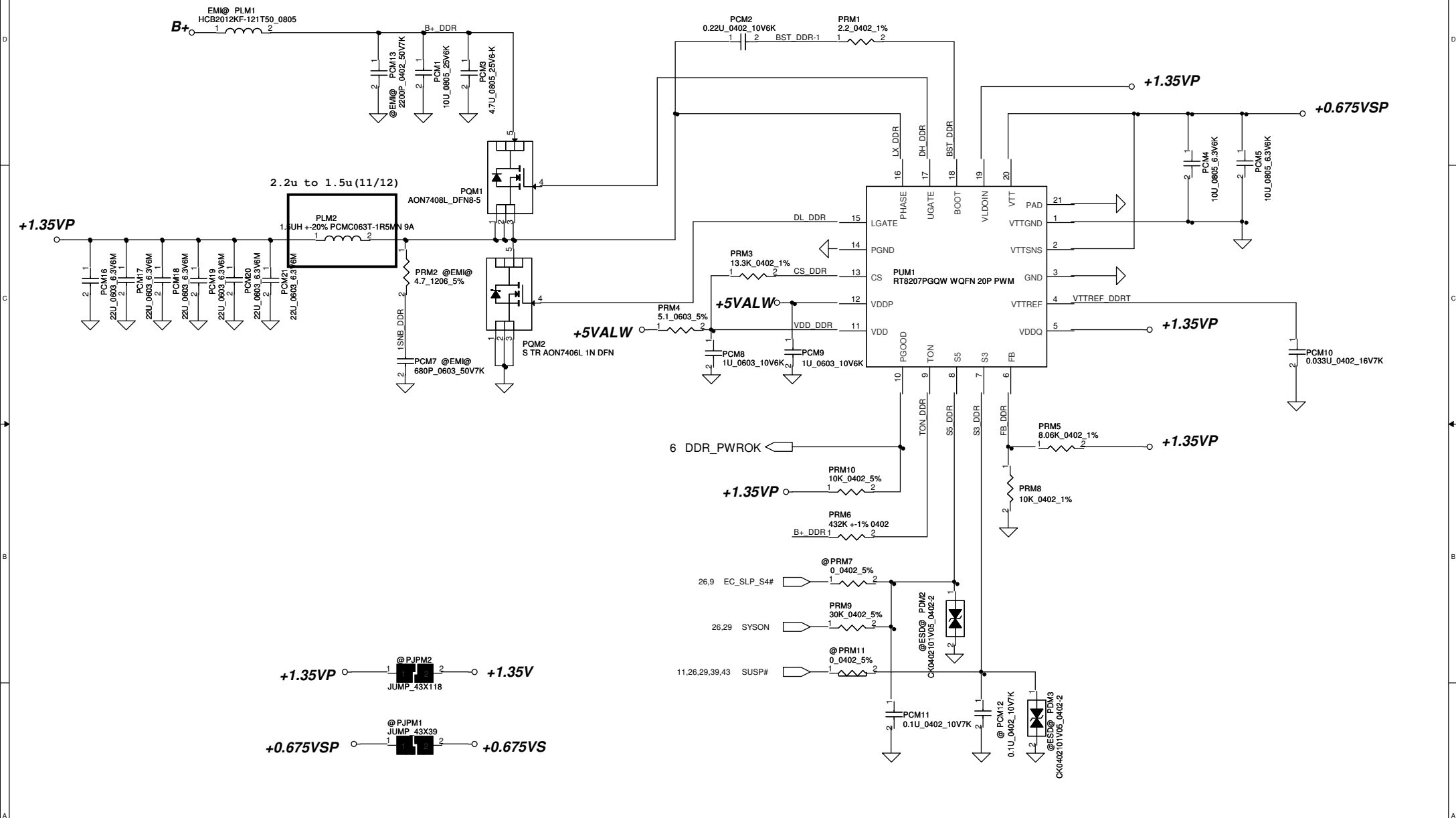


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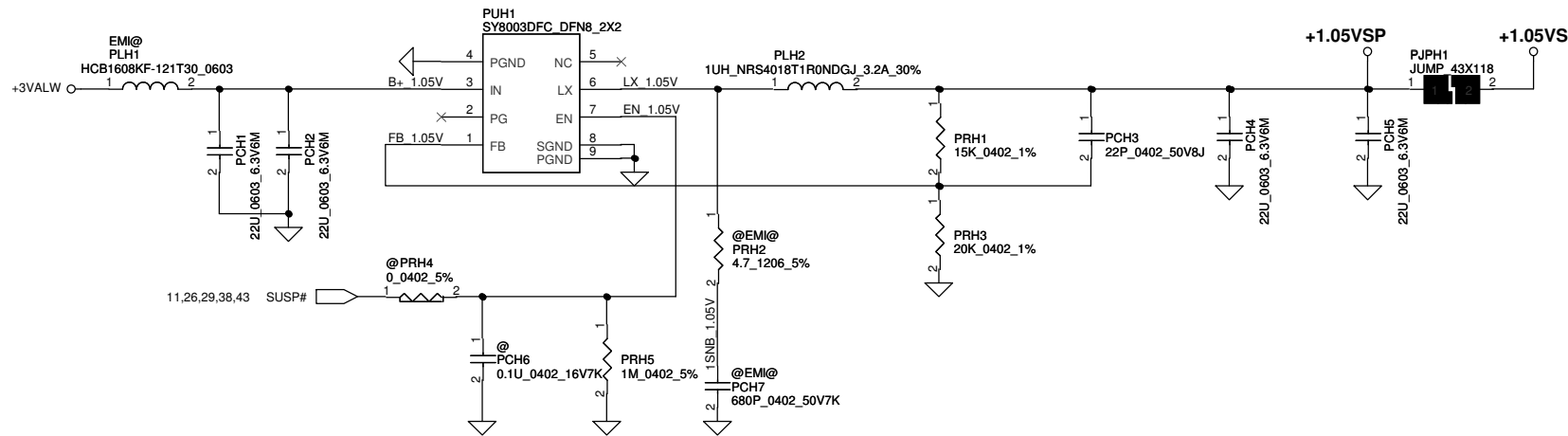




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Design Note
This circuit is for ULC 1+1 7.5W.
CPU: Icc=12A
Loadline: -5.9 m V/A
GFX(GT2): Icc=14A
Loadline: -5.9 m V/A

For VR_HOT#, already
pull high at power side.

PR18 and PR30
27.4K ohm for 100 degree
61.9K ohm for 110 degree

Layout Note
SVID routing
1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.
2. SVID spacing requirement is 18mils(0.475mm)/VSSSENSE
3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).
4. The SVID bus must be ground reference, It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.
5. Avoid routing under noisy circuit, e.g. switch node, Gate driver, B+, Vin, high speed signal.
6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.

Close GFX choke

Close GFX L/S MOS

Close CPU L/S MOS

$C_n = L / ((R_{ntcnet} * R_{sum}) / (R_{ntcnet} + R_{sum})) * DCR$
If C_n is correctly selected, when the load current has a square change, the output voltage also has a square response.

Layout Note
Reduce Acoustic Noise
1. The AL bulk capacitor of B+ should be very close to CPU_CORE MOSFET.
2. Input ceramic caps must place on symmetry same location on top side and bottom side.

MDV1525 Vds=30V
Rds(on)=11.5-14m ohm@Vgs=4.5V

MDU1511 Vds=30V
Rds(on)=2.7-3.3m ohm@Vgs=4.5V

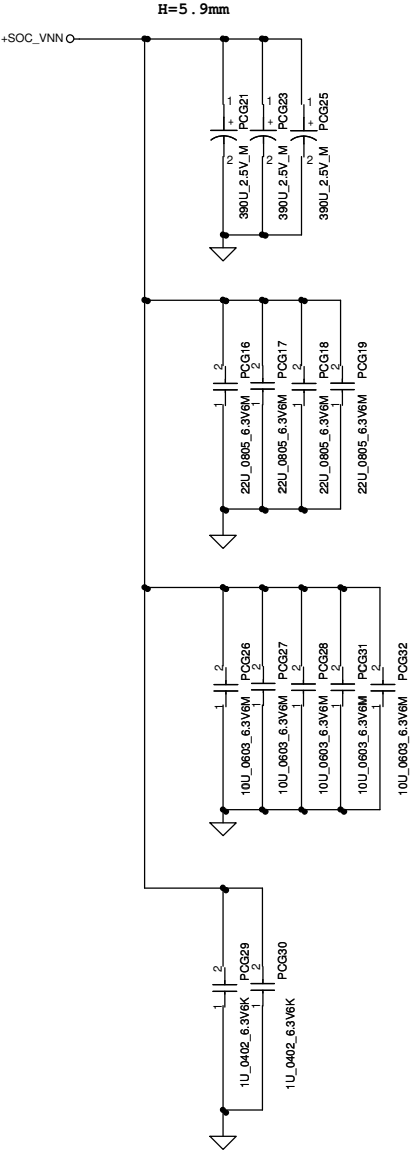
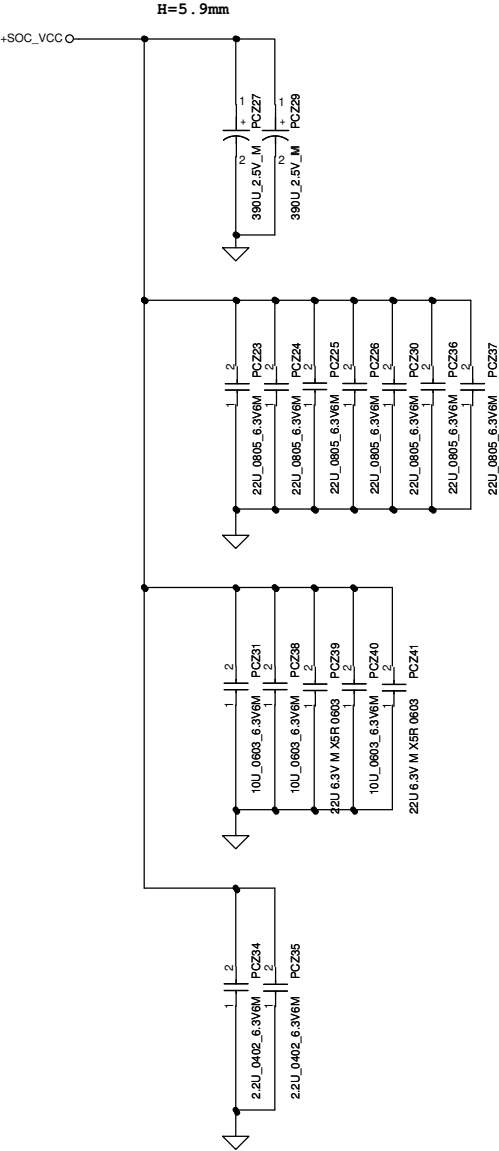
MDV1525 Vds=30V
Rds(on)=11.5-14m ohm@Vgs=4.5V

MDU1511 Vds=30V
Rds(on)=2.7-3.3m ohm@Vgs=4.5V

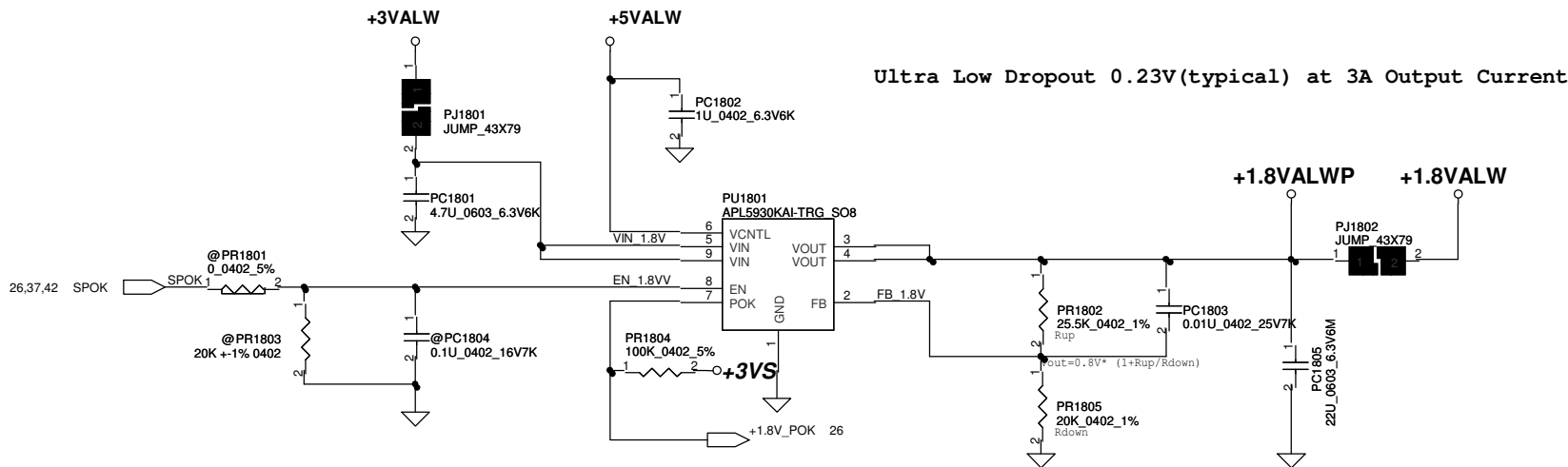
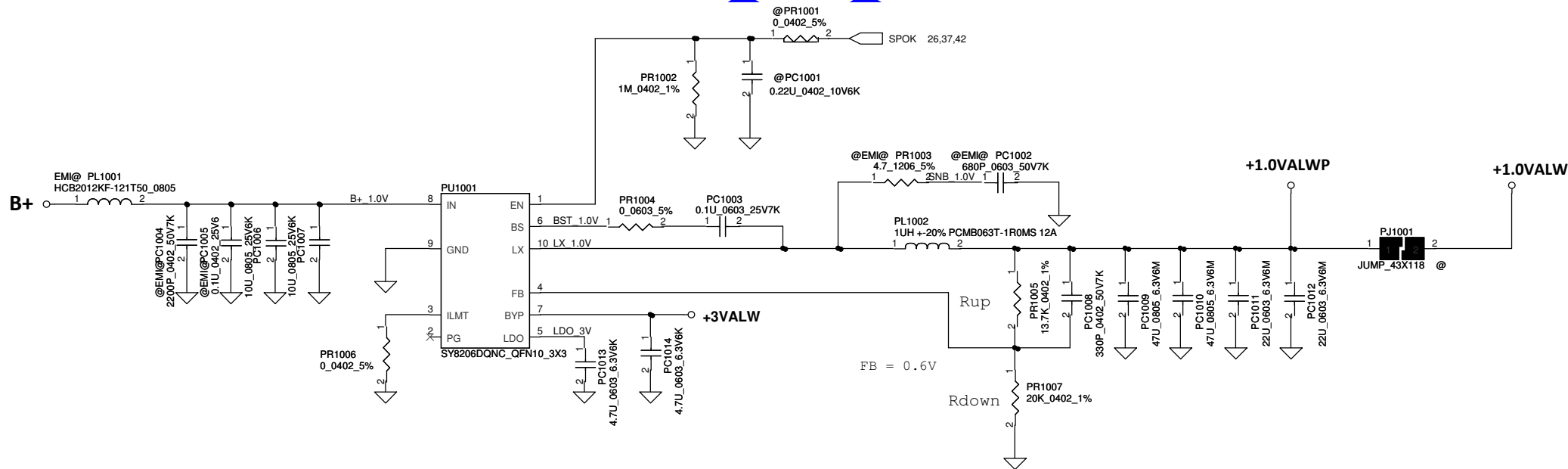
OCP setting=-20A

OCP setting=-18A

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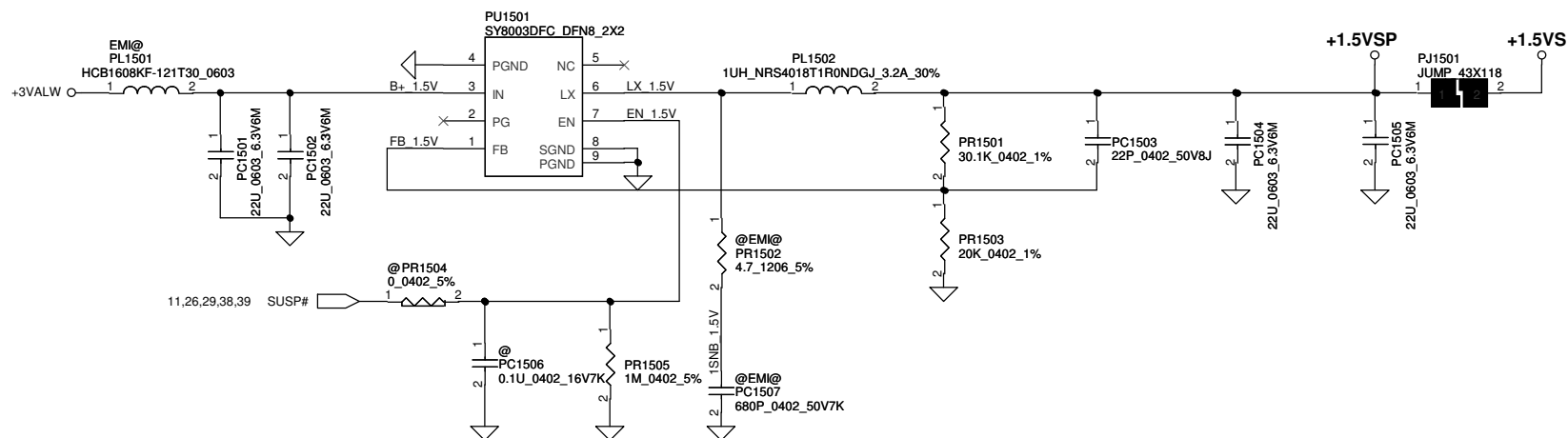


Ultra Low Dropout 0.23V(typical) at 3A Output Current

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