MK-2.0/DU-1.0 Block Diagram -- AMD Nile

PCB STACK UP 8L

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT

FAN/Thermal Sensor
Environment
PG 31

Thermal Sensor
PG 6

Sideport Memory
PG 13

11.6" HD (1366x768) LCD
PG 20

CRT
PG 21

HDMI
PG 21

AMD ASB2 CPU
Geneva
TPD~15W
27mmX27mm 812pin BGA
PG 4,5,6,7

Max 4GB

DDR3 SO-DIMM 1
(CH-A,RVS)
PG 8

DDR3 SO-DIMM 2
(CH-B,STD)
PG 9

14.318MHZ

Clock Gengerator
ICS9LPRS478
PG 3

Hyper Transport Link 16x16(HT_LINK)

NORTH BRIDGE
RS880M
21mmX21mm, 528pin BGA
TPD~7.5W
PG 10,11,12,13,14

LVDS

RGB

HDMI

PCI-e/USB

Mini PCIe Slot
PG 27

WLAN Module
PG 27

PCI-e/USB

Mini PCIe Slot
PG28

WWAN Module
PG 28

SIM Card
PG 28

PCI-e

10/100/1G Ethernet
Realtek RTL8111DL
PG 22

RJ-45
PG 22

32.768KHz 25MHz

PCIE 4X(A_LINK)

HP/Mic Audio Jack
PG22

HDA CODEC
CX20582-11Z
PG 23

HD Audio

SOUTH BRIDGE
SB820
TPD~4W
21mmX21mm, 528pin BGA
PG 15,16,17,18,19

SATA

2.5" HDD /SSD Module
(Option)
PG 24

12 MHz

USB

Card Reader
Realtek
RTS5159
PG 26

3 in 1 Socket
MS/MS Pro/SD/MMC
PG 26

Internal MIC
PG 23

Internal SPK
PG 23

32.768KHz

LPC BUS

USB

USB PORT X 3
PG 25

USB

Camera Conn
PG 20

Camera Module
PG 20

USB

Bluetooth
(BDC-2)
PG 30

ITE8502E
PG 33

SPI Flash
PG 33

Accelerometer
(APS)
PG 30

Int. KB
PG 29

T/P
PG 29

Battery
PG 35

Charger
PG 35

POWER

DC/DC 3VPCU, 5VPCU, +15V	PG 36
REGULATOR (DDR3) 1.5VSUS, +0.75V_DDR_VTT	PG 37
REGULATOR +1.1V/+1.1VS5/+1.8V	PG 38
REGULATOR +1.8V	PG 39
REGULATOR +NB_CORE/+0.9V/+2.5V	PG 40
CPU Core	PG 41
RUN POWER SW 3VSUS, 5VSUS, 3V_S5, 5V_S5 +3V, +5V	PG 42
Discharge	PG 42

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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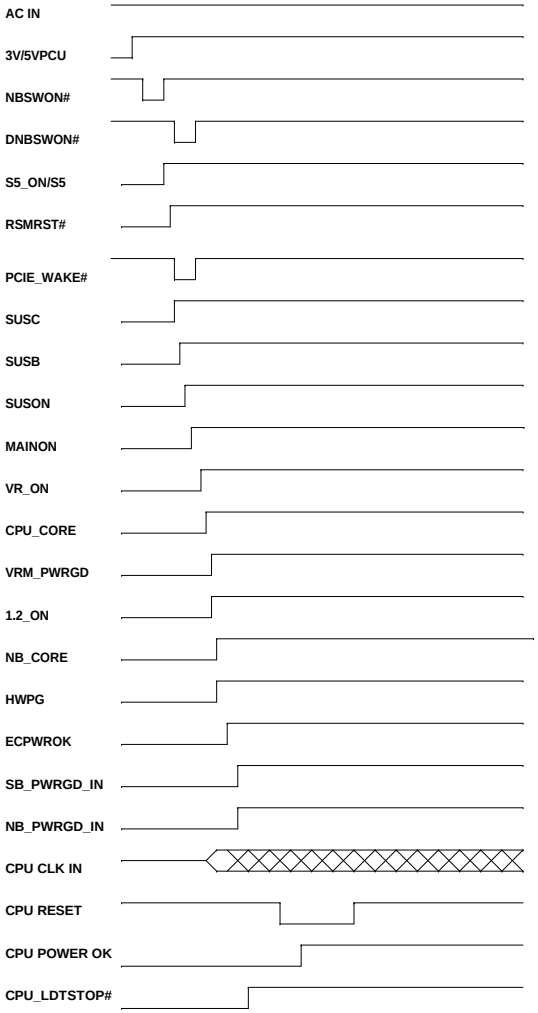
Power Sequence



RS880 DAC/I2C/DDC BUS

RS880 BUS	Pin NO.	BUS Function Define
INT_DDCCLK INT_DDCDAT (+5V)	F8 E8	CRT
INT_EDIDCLK INT_EDIDDAT (+5V)	B9 A9	LVDS
INT_HDMI_SCL INT_HDMI_SDA	B7 A7	not support HDMI port

SB820 SM BUS

SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID / CLOCK GEN
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM INFORMATION	1A

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+3V [6,8,9,12,14,15,16,17,18,19,20,21,22,23,24,26,27,28,30,31,32,33,34,36,38,40,41,42]
+1.1V [7,11,12,13,14,18,38,42]

3.3V(250mA)

+3V L27 HCB1608KF-601T10_6 +3V_CLK_VDD

ECA04: C331 10U/6.3V/X5R_8; C353 22U/6.3V/X5R_8; C384 0.1U/10V/X5R_4; C347 2200P/50V/X7R_4; C345 0.1U/10V/X5R_4; C351 0.1U/10V/X5R_4; C381 0.1U/10V/X5R_4; C541 0.1U/10V/X5R_4; C419 0.1U/10V/X5R_4

+1.1V_CLK_VDDIO(53mA)

+1.1V L28 BLM18AG601SN1D_6 +1.1V_CLK_VDDIO

ECA12: C370 *47P/50V/NPO_4; C382 22U/6.3V/X5R_8; C424 2200P/50V/X7R_4; C540 2200P/50V/X7R_4; C388 0.1U/10V/X5R_4; C357 0.1U/10V/X5R_4; C346 0.1U/10V/X5R_4

ICS9LPRS480 P/N : ALPRS480000

RTM880N-796-VB-GRT P/N : AL000880001

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN

Place within 0.5" of CLKGEN

+3V_CLK_VDD

U24 ICS9LPRS480AKLFT QFN64

VDDDOT VDDSRC VDDATIG VDDSB_SRC VDDSATA VDDCPU VDDHTT VDDREF VDD48

VDDSRC_IO0 VDDSRC_IO1 VDDATIG_IO VDDSB_SRC_IO VDDCPU_IO

GND48 GNDDOT GNDSRC0 GNDSRC1 GNDATIG GNDSB_SRC GNDSATA GNDCPU GNDHTT GNDREF

3.3V(53mA) +3V_CLK_48 +3V L33 BLM18AG601SN1D_6

ECA12: C411 *47P/50V/NPO_4; C421 2.2U/6.3V/X5R_6

+1.1V_CLK_VDDIO

EC_B20: C407 33P/50V/NPO_4; Y4 14.318MHZ; C406 33P/50V/NPO_4; CG_XIN; CG_XOUT

CG_XIN CG_XOUT X1 X2

[8,9,16,32] PCLK_SMB SMBCLK
[8,9,16,32] PDAT_SMB SMBDAT

+3V_CLK_VDD R245 8.2K_4 CLK_PD# PD#

T72 CLKREQ0# CLKREQ0#
T53 CLKREQ1# CLKREQ1#
T59 CLKREQ2# CLKREQ2#
T55 CLKREQ3# CLKREQ3#
T54 CLKREQ4# CLKREQ4#

TGND0 TGND1 TGND2 TGND3 TGND4 TGND5 TGND6 TGND7 TGND8 TGND9

CPUK8_0T CPUK8_0C: CLK_CPUP_R CLK_CPUN_R RP10 0_4P2R_4 → CPUCLKP [6] CPUCLKN [6] → To CPU Diff 200MHz

R210 *261/F_4

RP7 *0_4P2R_4 → CPUCLKP_L [15] CPUCLKN_L [15] → To NB Diff 100MHz

ATIG0T ATIG0C ATIG1T ATIG1C: CLK_NBGFXP_R T63; CLK_NBGFXN_R T65

SB_SRC0T SB_SRC0C SB_SRC1T SB_SRC1C: CLK_SBSRCP_R CLK_SBSRCN_R RP11 0_4P2R_4 → CLK_SBREFP_R [15] CLK_SBREFN_R [15] CLK_SBSRCP [15] CLK_SBSRCN [15] → To NB Diff 100MHz, To SB Diff 100MHz

SRC0T SRC0C SRC1T SRC1C: NBGPP_CLKP_R T71; NBGPP_CLKN_R T70; CLK_PCIE_NEW_R T74; CLK_PCIE_NEW#_R T73

SRC2T SRC2C SRC3T SRC3C SRC4T SRC4C: CLK_PCIE_LANP_R CLK_PCIE_LANN_R RP13 0_4P2R_4 → CLK_PCIE_WLANP_R [15] CLK_PCIE_WLANN_R [15] CLK_PCIE_WANP_R [15] CLK_PCIE_WANN_R [15] CLK_PCIE_LANP [22] CLK_PCIE_LANN [22] → To Mini PCIE Slot (WLAN), To Mini PCIE Slot (WWAN), To LAN Controller

RP6 *0_4P2R_4 → CLK_PCIE_LANP_L [15] CLK_PCIE_LANN_L [15]

SRC6T/SATAT SRC6C/SATAC SRC7T/27M_SS SRC7C/27M_NS: T51; T50; T106; T105

HTT0T/66M HTT0C/66M: NBHT_REFCLKP_R NBHT_REFCLKN_R → NBHT_REFCLKP_R [15] NBHT_REFCLKN_R [15] → To NB Diff 100MHz

48MHz_0: CLK_48M_USB_R R307 47_4 R300 *22_4 CLK_48M_USB_CR → CLK_48M_USB [16] CLK_48M_USB_CR [26] → To SB 48MHz, To RTS5159 48MHz

REF0/SEL_HTT66 REF1/SEL_SATA REF2/SEL_27: SEL_HTT66 SEL_SATA SEL_27; T69; EXT_NB_OSC [12] → To SB 14.318MHz, To NB 14.318MHz

CLK_48M_USB CLK_48M_USB_CR

C431 *12P/50V/C0G_4; C426 *12P/50V/C0G_4

ECA12

R279 158/F_4
R271 90.9/F_4

R4004/R4005 (value may change)

	NB_OSC
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

RES CHIP 82.5 1/16W +-1%(0402) --> CS08252FB11
RES CHIP 130 1/16W +-1%(0402)L-F --> CS11302FB15
RES CHIP 158 1/16W +-1%(0402) --> CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) --> CS09092FB15

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

ECA05 +3V R212 8.2K_4 → [16,22] PCIE_REQ_LAN# R211 0_4 CLKREQ4#

ECA05 +3V R214 8.2K_4 → [16,28] PCIE_REQ_WWAN# R213 0_4 CLKREQ3#

ECA05 +3V R216 8.2K_4 → [16,27] PCIE_REQ_WLAN# R215 0_4 CLKREQ2#

+3V_CLK_VDD R283 *8.2K_4

SEL_SATA SEL_HTT66 SEL_27

R289 8.2K_4 R292 8.2K_4 R286 *8.2K_4

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0 *	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

CLK_48M_USB_R C415 *10P/50V/C0G_4
SEL_SATA C401 10P/50V/C0G_4
SEL_27 C398 10P/50V/C0G_4

EMI Cap placement close IC

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLK GEN	1A

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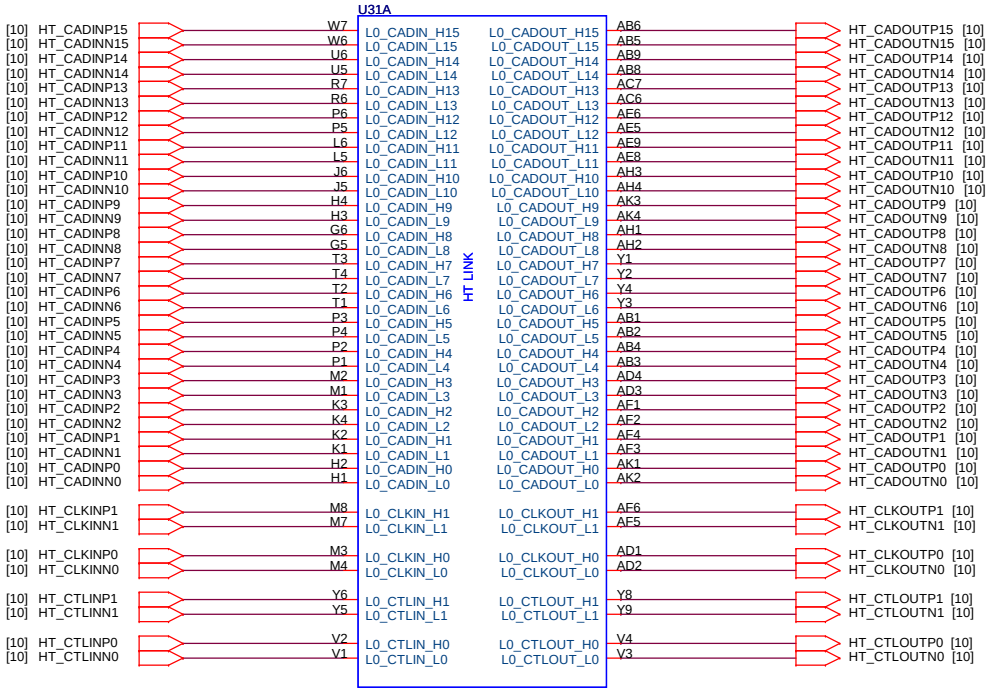
AMD Processor HT Interface



PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
B	AMD ASB2 CPU(HT)	1A

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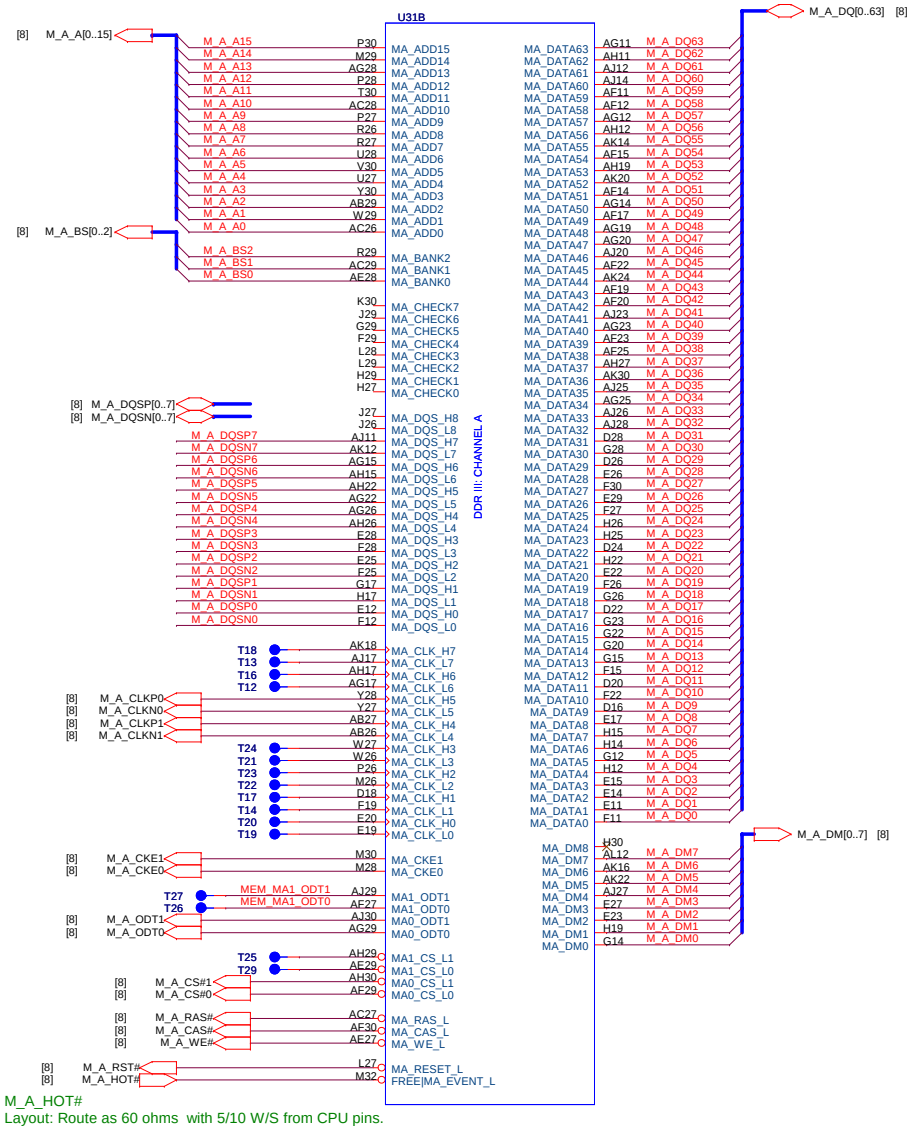
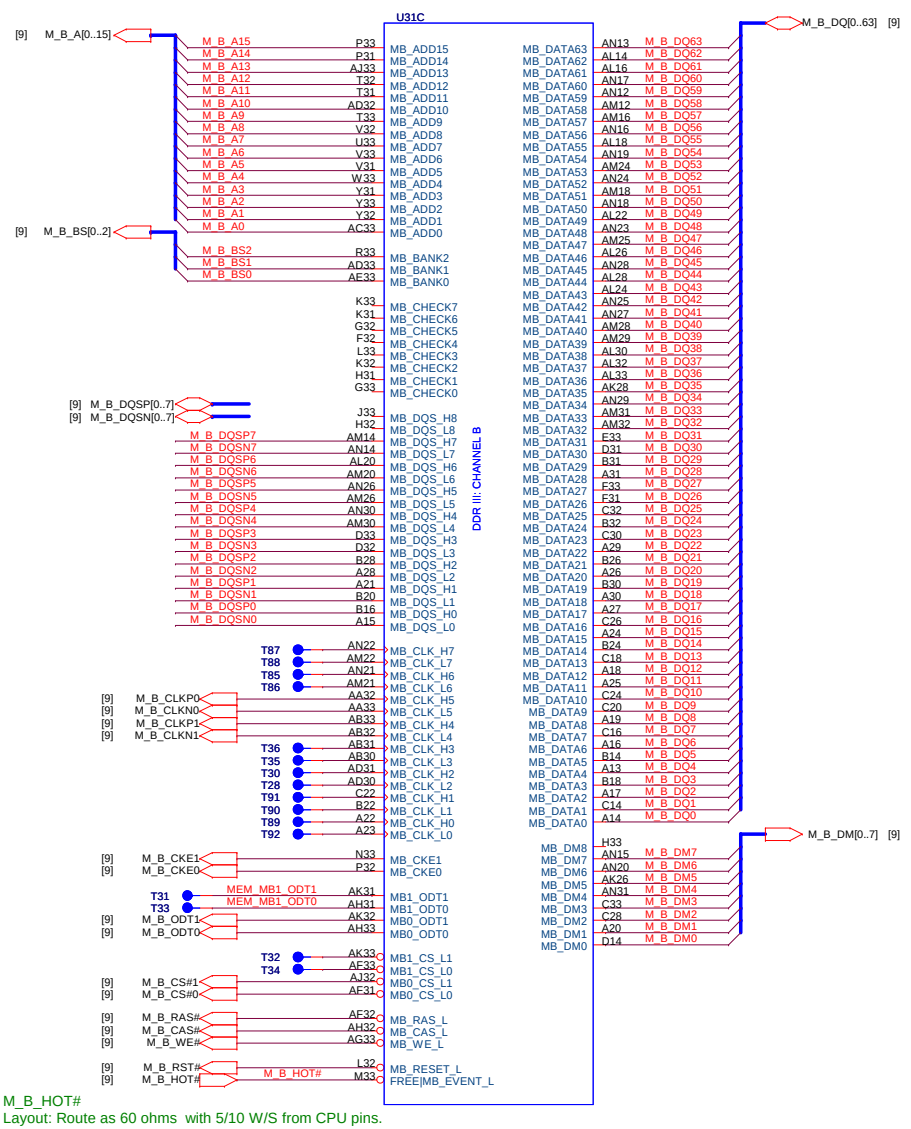
Channel-A to SODIMM Connector

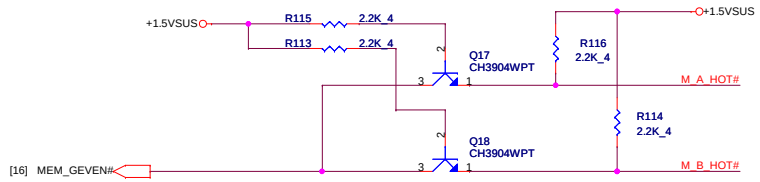


M_A_HOT#
Layout: Route as 60 ohms with 5/10 W/S from CPU pins.

Channel-B to SODIMM Connector



M_B_HOT#
Layout: Route as 60 ohms with 5/10 W/S from CPU pins.



PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMD ASB2 CPU(DDR3)	1A

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+1.5VSUS [5,7,8,9,12,34,37,40,41,42]
+1.5V [14,16,27,28,42]
+2.5V [34,40,42]
+3V [3,8,9,12,14,15,16,17,18,19,20,21,22,23,24,26,27,28,30,31,32,33,34,36,38,40,41,42]
+CPU_VLDT [7]
+3V [3,8,9,12,14,15,16,17,18,19,20,21,22,23,24,26,27,28,30,31,32,33,34,36,38,40,41,42]
+3VS5 [15,16,17,18,19,25,27,30,32,42]

CPU CLK

Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"

Thermdc and Thermda should be routed away to VRM, crystal, etc. Customer should follow the MBDG. However, Bimini is using TSI so this does not applies to Bimini.

W/S= 15 mil/20mil

+2.5V L38 BLM21PG221SN1D +CPUVDDA
C492 4.7U/6.3V/X5R_6
C491 *22U/6.3V/X5R_8
C490 4.7U/6.3V/X5R_6
C488 0.22U/6.3V/X5R_4
C487 3300P/50V/X7R_4

U31D
MISC
VDDA_1 A8
VDDA_2 B8
CLKIN_H A6
CLKIN_L A7
PWROK
LDTSTOP_L
RESET_L
RSVD|CORE_TYPE M31 CPU_CORE_TYPE T93
SVC C1 CPU_SVC_R
SVD B2 CPU_SVD_R
SIC AN4 CPU_SIC
SID AN5 CPU_SID
RSVD_SA0 AM2
ALERT_L AN3 CPU_ALERT
THERMDC AL6 H_THRMDC
THERMDA AM5 H_THRMDA
THERMTRIP_L AK6 CPU_THERMTRIP#_R
PROCHOT_L AN6 CPU_PROCHOT#_R
TDO AN7 CPU_TDO
TDI AM8 CPU_TDI
TRST_L AL8 CPU_TRST#
TCK AK8 CPU_TCK
TMS AN8 CPU_TMS
DBREQ_L G9 CPU_DBREQ#
DBRDY H9 CPU_DBRDY
VSS_SENSE D2 CPU_VDD0_RUN_FB_L
VLDT_SENSE E2 CPU_VLDT_SENSE
VDD_SENSE E1 CPU_VDD0_RUN_FB_H
VDDNB_SENSE D1 CPU_VDDNB_RUN_FB_H
VDDIO_SENSE D3 CPU_VDDIO_SUS_FB_H
VDDR_SENSE C2 CPU_VDDR_SENSE
M_VREF A11
M_ZN_H AM9
M_ZN_L AN9
RSVD3 AM6 RSVD3
CPU_PRESENT_L AJ9 CPU_PRESENT_L
HTREF1 V10 CPU_HTREF1
HTREF0 V9 CPU_HTREF0
BYPASSCLK_H A9 CPU_TEST25_H_BYPASSCLK_H
BYPASSCLK_L B9 CPU_TEST25_L_BYPASSCLK_L
PLLTEST0 A5 CPU_TEST19_PLLTEST0
PLLTEST1 B6 CPU_TEST18_PLLTEST1
ANALOGIN G8 CPU_TEST9_ANALOGIN
BP3 F8 CPU_TEST17_BP3
BP2 C8 CPU_TEST16_BP2
BP1 D9 CPU_TEST15_BP1
BP0 E8 CPU_TEST14_BP0
ANALOG_T C6 CPU_TEST7_ANALOG_T
DIECRACKMON AH7 CPU_TEST6_DIECRACKMON
GATE0 AK5 CPU_TEST3
DRAIN0 AJ7 CPU_TEST2
FBCLKOUT_H B10 CPU_TEST29_H_FBCLKOUT_P
FBCLKOUT_L A10 CPU_TEST29_L_FBCLKOUT_N
SCANCLK1 AK7 CPU_TEST24_SCANCLK1
TSTUPD AG8 CPU_TEST23_TSTUPD
SCANSHIFTEN AK9 CPU_TEST22_SCANSHIFTEN
SCANEN AH9 CPU_TEST21_SCANEN
SCANCLK2 AM7 CPU_TEST20_SCANCLK2
PLLCHRZ_H G11 CPU_TEST28_H_PLLCHRZ_P
PLLCHRZ_L H11 CPU_TEST28_L_PLLCHRZ_N
SINGLECHAIN AJ8 CPU_TEST27_SINGLECHAIN
BURNIN_L AM4 CPU_TEST26_BURNIN_L
ANALOGOUT D7 CPU_TEST10_ANALOGOUT
DIG_T B5 CPU_TEST8_DIG_T
M_TEST AG9

[3] CPUCLKP C462 3900P/25V/X7R_4
[3] CPUCLKN C461 3900P/25V/X7R_4
R375 169/F_4
CPUCLKIN
CPUCLKIN#
[15] CPU_PWR_GD
[12,15] CPU_LDT_STOP#
[15] CPU_LDT_RST#
CPU_LDT_RST# L
+1.5V R97 300_4
+1.5VSUS
R58 1K/F_4
M_VREF
R55 1K/F_4
C93 0.1U/10V/X5R_4
C105 1000P/50V/X7R_4
[41] CPU_VDD0_RUN_FB_L
T2
[41] CPU_VDD0_RUN_FB_H
[41] CPU_VDDNB_RUN_FB_H
[37] CPU_VDDIO_SUS_FB_H
[40] CPU_VDDR_SENSE
R497 *0_4
0.01U/16V/X7R_4 C469
R384 39.2/F_4
M_ZP
M_ZN
PLACE THEM CLOSE TO CPU WITHIN 1"
+1.5VSUS
R52 510/F_4
R47 510/F_4
R43 *Short_4
T8 T82 T4 T7 T5 T9
R44 1K_4
place within 1.5"
R30 44.2/F_4
R45 44.2/F_4
+CPU_VLDT
R379 80.6/F_4
Route as 80ohm, diff
route as differential as short as possible testpoint under package
R31 *300/J_4 +CPU_VLDT
R147 is installed ONLY when SCAN is enabled
R215, R185 internal ONLY

+1.5VSUS
R381 10K/F_4
R380 1K_4
Q33 CH3904WPT
Q34 CH3904WPT
R385 0_4
R386 *0_4
SYS_SHDN# [31,36,42]
CPU_THERMTRIP# [16]
CPU_PROCHOT# [15]
R378 *0_4
R388 300_4
R387 10K/F_4
Q32 *CH3904WPT
CPU_PROCHOT#_EC [33]
R376 *300/J_4
+1.5VSUS

CPU THERM

Symbol		Max	Units
Tshutdown	THERMTRIP shutdown temperature	125	℃
Tsd_delay	Maximun allowed time from TSHUTDOWN detection to VDD shutdown to prevent thermal damage to the processor	500	ms

+3V
R73 *200_4
R61 *10K_4
R59 *10K_4
Q7 *RHU002N06
MBCLK_THRM [31,33]
*0.1U/10V/X5R_4 C124 +3V_THERM
U1
H_THRMDA
C96 *1000P/50V/X7R_4
H_THRMDC
VCC SCLK
DXP SDA
DXN ALERT#
GND OVERT#
*ADM1032
MSOP
LM86_SMC
LM86_SMD
SMBALERT#
Q8 *RHU002N06
MBDATA_THRM [31,33]
R57 *10K_4
*0_4 R54
PM_THERM# [17]
+3VS5
ECA96

ADDRESS: 98H

AL001032001 / IC OTHER(8P) ADM1032ARMZ-1RL(MSOP)
AL000786000 / IC OTHER(8P) G786P81U(MSOP)

CPU H/W MONITOR

+3V
R63 *10K_4
R74 *330_4
Q9 *CH3904WPT
THERM_SHD#
SYS_SHDN# R
C127 *1U/16V/X5R_6

+1.5VSUS R96 *10K/F_4 CNTR_VREF
+3V
R88 *1K/F_4
Q16 *MMBT3904
CPU_LDT_RST#
CPU_LDT_RST_HTPA#
Can remove on MP------>LX

+1.5VSUS
R371 1K/F_4 CPU_TEST26_BURNIN_L
R40 300_4 CPU_DBREQ#
R69 1K/F_4 CPU_TEST27_SINGLECHAIN
CPU_TEST21_SCANEN R49 300_4
CPU_TEST20_SCANCLK2 R383 300_4
CPU_TEST24_SCANCLK1 R382 1K/F_4
CPU_TEST22_SCANSHIFTEN R50 1K/F_4
CPU_TEST15_BP1 R42 *300/J_4
CPU_TEST14_BP0 R41 *300/J_4
CPU_DBRDY R46 *300/J_4
CPU_TEST18_PLLTEST1 R39 1K/F_4
CPU_TEST19_PLLTEST0 R373 1K/F_4
CPU_TEST23_TSTUPD R53 1K/F_4

HDT Connector

+1.5VSUS
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
C89 *0.1U/10V_4
KEY
CN4 *HDT CONN
CPU_LDT_RST_HTPA#

VID Override Circuit

Note:
To override VID,
Remove R192, R194, R196,
install R165
set VID via SW100

SVC	SVD	BOOT VOLTAGE(VDD) (CPUVRM_PRO# = VCC/GND)	(CPUVRM_PRO# = OPEN)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

VID OVERIDE TABLE (VDD)

+1.5VSUS R365 1K_4
+1.5V R27 1K_4 R370 *1K_4 R24 300_4
CPU_SVC_R R363 *Short_4
CPU_SVD_R R367 *Short_4
CPU_PWR_GD R25 *Short_4
R28 *220/J_4
R372 *220/J_4
R23 *220/J_4
To CPU VRM
CPU_SVC [41]
CPU_SVD [41]
CPU_PWRGD_SVID_REG [41]

OVERT# Check EC Setting Degree

+1.5VSUS
+3V
R366 1K/F_4
R19 390_4
R18 390_4
R369 *2K/F_4
R21 2K/F_4
R15 2K/F_4
CPU_SIC
Q4 BSS138_NL/SOT23
MBCLK_THRM [31,33]
CPU_SID
Q6 BSS138_NL/SOT23
MBDATA_THRM [31,33]
EC_B14
CPU_ALERT
Q31 *BSS138_NL/SOT23
THERM_SHD#

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE
Quanta Computer Inc.
Size Custom
Document Number AMD ASB2 CPU(CLK,THM,CTRL)
Rev 1A
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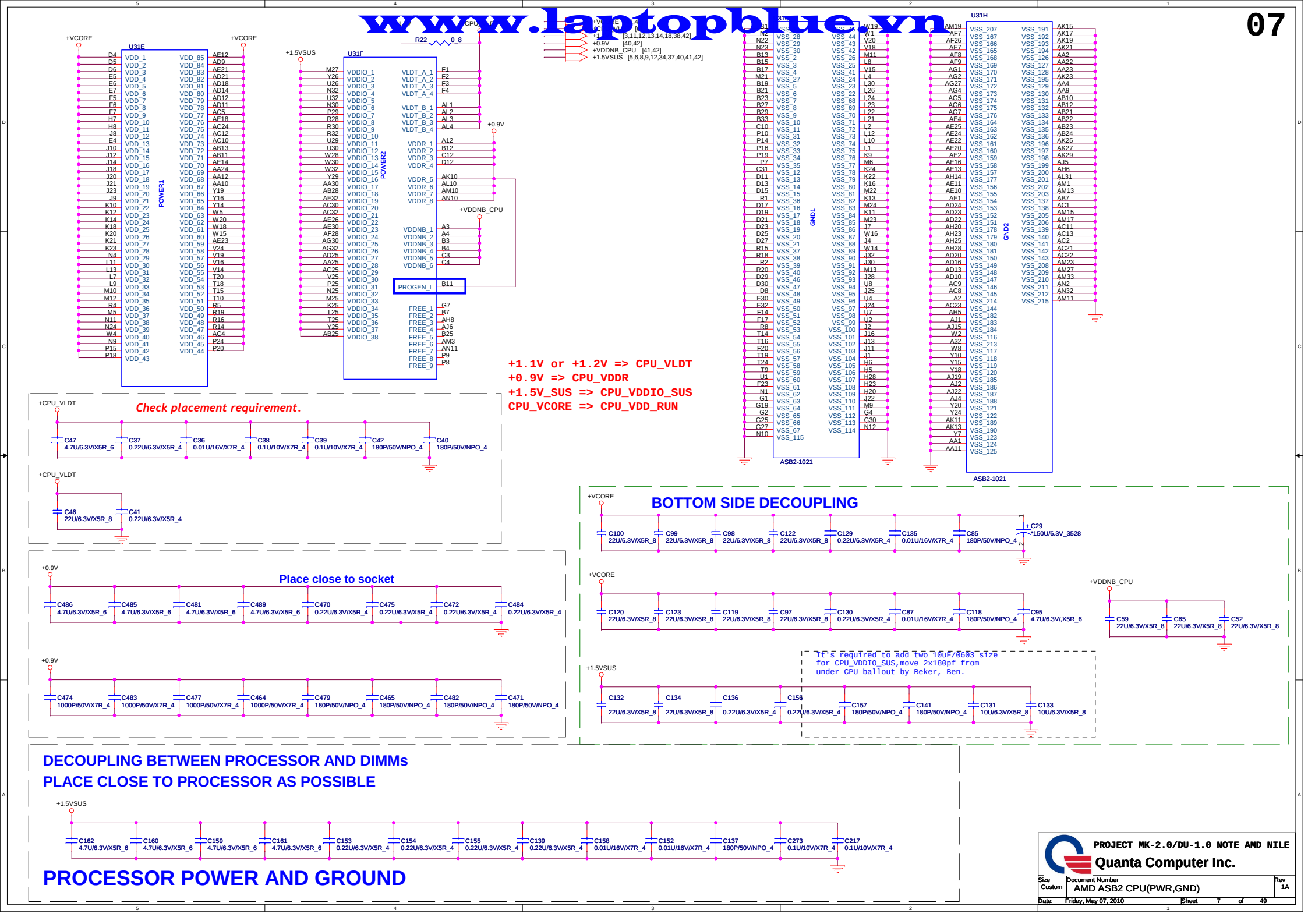

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMD ASB2 CPU(PWR,GND)	1A

Date: Friday, May 07, 2010 Sheet 7 of 49

+5VS [5,6,7,9,12,34,37,40,41,42]
+DDR_VREF_DIMM [37]
+0.75V_DDR_VTT [9,37,42]
+3V [3,6,9,12,14,15,16,17,18,19,20,21,22,23,24,26,27,28,30,31,32,33,34,36,38,40,41,42]

CN17A

[5] M_A_A[0..15]
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14 M_A_A15

[5] M_A_BS[0..2]
M_A_BS0 M_A_BS1 M_A_BS2

[5] M_A_CS#0
[5] M_A_CS#1
[5] M_A_CLKP0
[5] M_A_CLKN0
[5] M_A_CLKP1
[5] M_A_CLKN1
[5] M_A_CKE0
[5] M_A_CKE1
[5] M_A_CAS#
[5] M_A_RAS#
[5] M_A_WE#
R122 10K/F_4 DIMM0_SA0
R121 10K/F_4 DIMM0_SA1
[3,9,16,32] PCLK_SMB
[3,9,16,32] PDAT_SMB

[5] M_A_ODT0
[5] M_A_ODT1
[5] M_A_DM[0..7]
M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7

[5] M_A_DQSP[7:0]
M_A_DQSP0 M_A_DQSP1 M_A_DQSP2 M_A_DQSP3 M_A_DQSP4 M_A_DQSP5 M_A_DQSP6 M_A_DQSP7

[5] M_A_DQSN[7:0]
M_A_DQSN0 M_A_DQSN1 M_A_DQSN2 M_A_DQSN3 M_A_DQSN4 M_A_DQSN5 M_A_DQSN6 M_A_DQSN7

PC2100 DDR3 SDRAM SO-DIMM (204P)

CONN_DDR3_RVS

BUS1_A2

M_A_DQ[0..63] [5]
M_A_DQ0 M_A_DQ1 M_A_DQ7 M_A_DQ3 M_A_DQ4 M_A_DQ5 M_A_DQ6 M_A_DQ2 M_A_DQ8 M_A_DQ9 M_A_DQ14 M_A_DQ11 M_A_DQ13 M_A_DQ12 M_A_DQ10 M_A_DQ15 M_A_DQ20 M_A_DQ17 M_A_DQ22 M_A_DQ23 M_A_DQ21 M_A_DQ16 M_A_DQ18 M_A_DQ19 M_A_DQ24 M_A_DQ29 M_A_DQ27 M_A_DQ26 M_A_DQ28 M_A_DQ25 M_A_DQ31 M_A_DQ30 M_A_DQ36 M_A_DQ37 M_A_DQ39 M_A_DQ34 M_A_DQ32 M_A_DQ33 M_A_DQ38 M_A_DQ35 M_A_DQ40 M_A_DQ45 M_A_DQ43 M_A_DQ42 M_A_DQ44 M_A_DQ41 M_A_DQ46 M_A_DQ47 M_A_DQ48 M_A_DQ52 M_A_DQ54 M_A_DQ50 M_A_DQ53 M_A_DQ49 M_A_DQ51 M_A_DQ55 M_A_DQ60 M_A_DQ61 M_A_DQ63 M_A_DQ62 M_A_DQ56 M_A_DQ57 M_A_DQ58 M_A_DQ59

SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

+1.5VSUS

CN17B

PC2100 DDR3 SDRAM SO-DIMM (204P)

CONN_DDR3_RVS

[5] M_A_HOT#
[5] M_A_RST#
R124 *0/short_4 MEM_A_HOT#

[9] +DDR_VREF
C183 0.1U/10V/X7R_4

+3V

ECA10

C319 *0.1U/10V_4
R173 *10K_4
U16
+3V
PDAT_SMB
PCLK_SMB
*DS75U+T&R
MEMHOT_DIMM# R183 *0_4 CPU_MEMHOT# [16]

ADDRESS: 92H Close DDR3 socket CN7016,CN7017

600mA
+0.75V_DDR_VTT
C188 4.7U/6.3V/X5R_6
C184 0.1U/10V/X7R_4
C186 4.7U/6.3V/X5R_6

3mA
+DDR_VREF_DIMM
[37] +DDR_VREF_DIMM
R161 0_6
R163 *10K/F_4
R123 *10K/F_4

C176 C187 C196 C189 C175 0.1U/10V/X7R_4

C198 C199 C173 C174 C180 C192 C195
4.7U/6.3V/X5R_6 4.7U/6.3V/X5R_6 2.2U/6.3V/X5R_6 2.2U/6.3V/X5R_6 1U/6.3V/X5R_4 1U/6.3V/X5R_4 1U/6.3V/X5R_4

C181 C182 C179 C178 C177 C194 C193 C191 C190 0.1U/10V/X7R_4

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 SO-DIMM (CH-A,RVS)	1A

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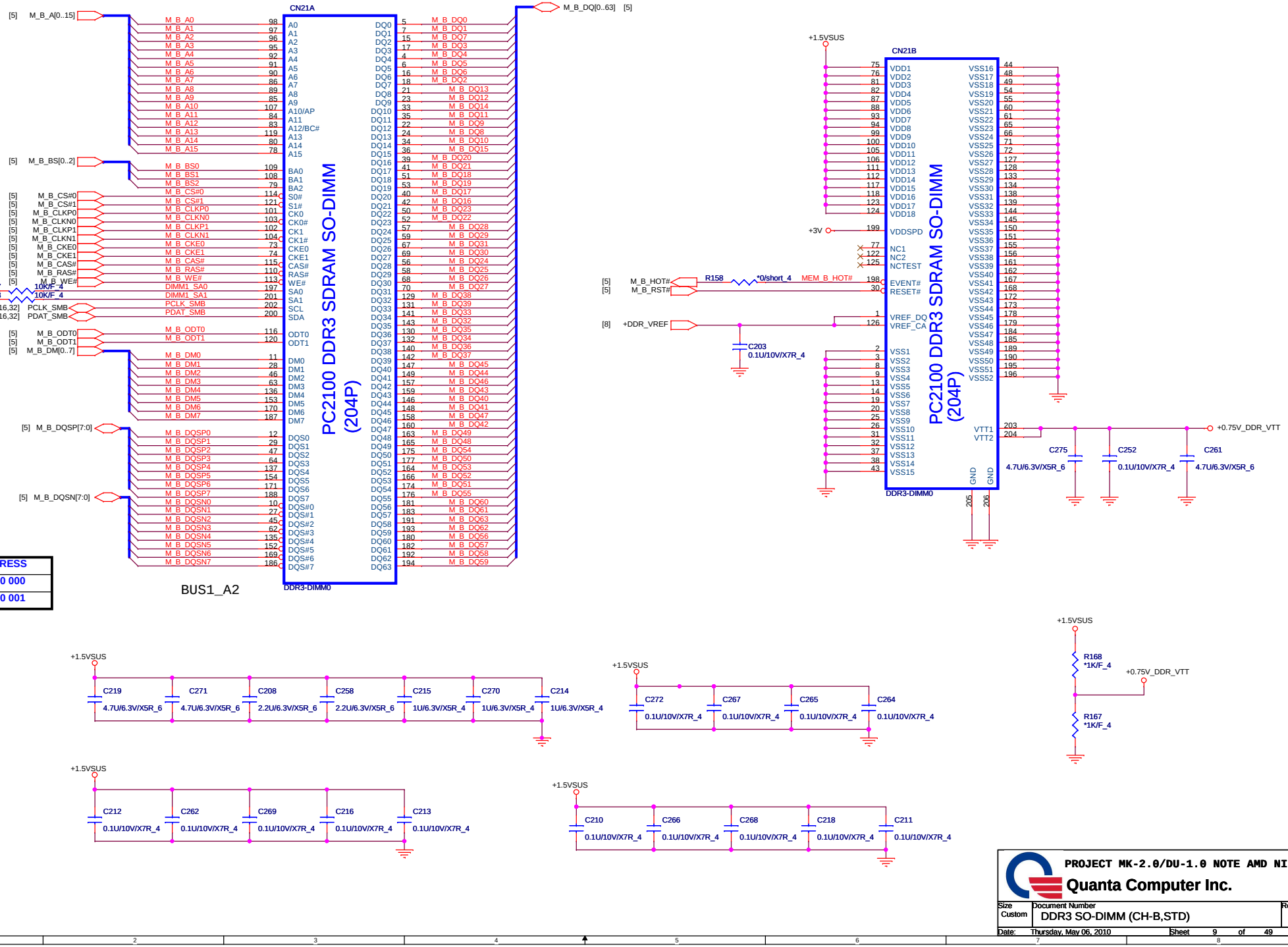
+1.5VSUS [5,6,7,8,12,34,37,40,41,42]
+0.75V_DDR_VTT [8,37,42]
+3V [3,6,8,12,14,15,16,17,18,19,20,21,22,23,24,26,27,28,30,31,32,33,34,36,38,40,41,42]



SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 SO-DIMM (CH-B,STD)	1A

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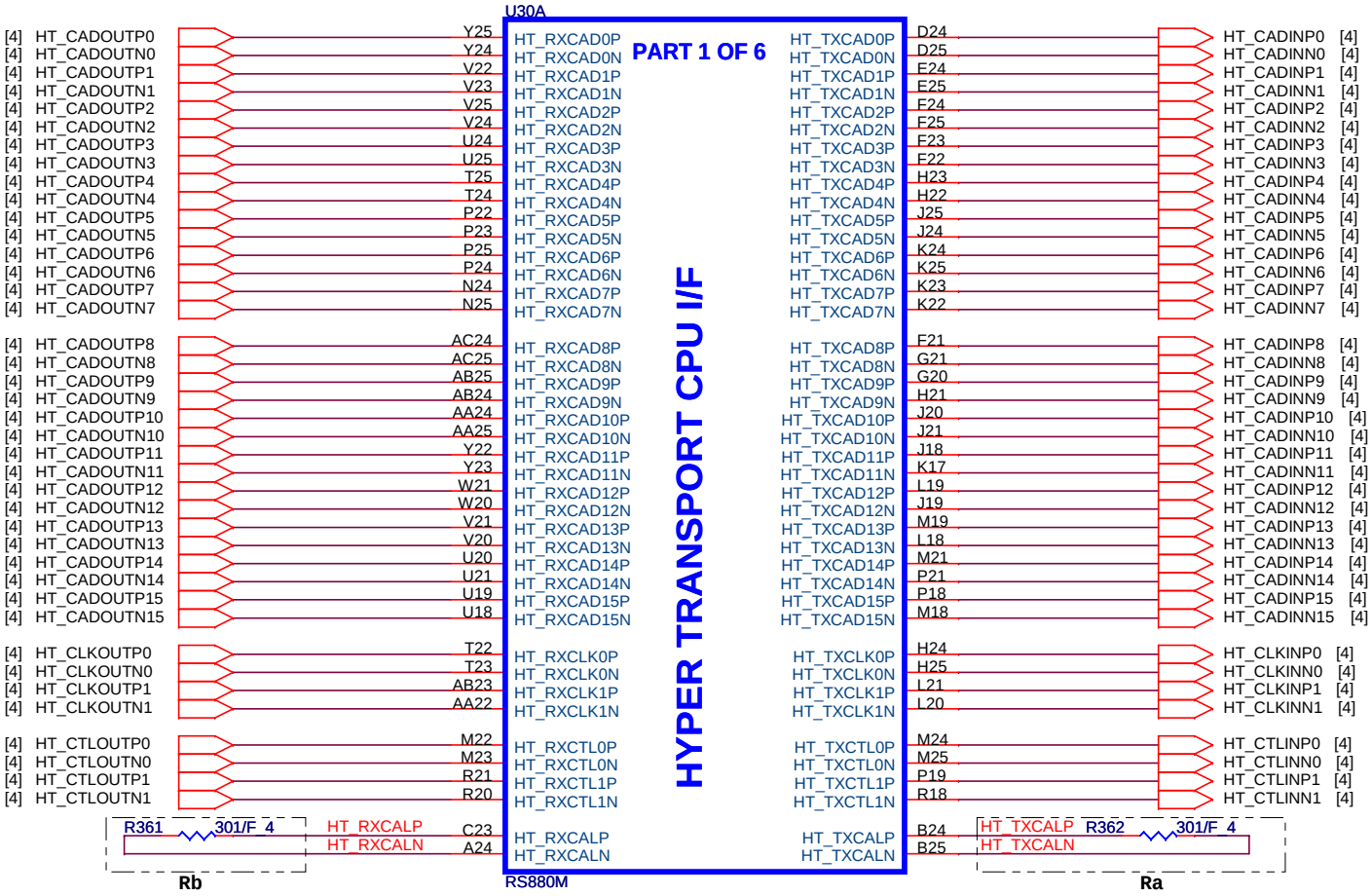


1. Support 16-bit up/down Hyper Transport (HT) 3.0 interface up to 4.4 GT/s
2. Support 200, 400, 600, 800, and 1000 MHz HT1 frequences
3. Support 1.6, 1.8,2.0, and 2.2 GHz HT3 frequences
4. Single chip solution in 55nm, 1.1V low power CMOS technology
5. 528-FCBGA package, 21mmx21mm

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

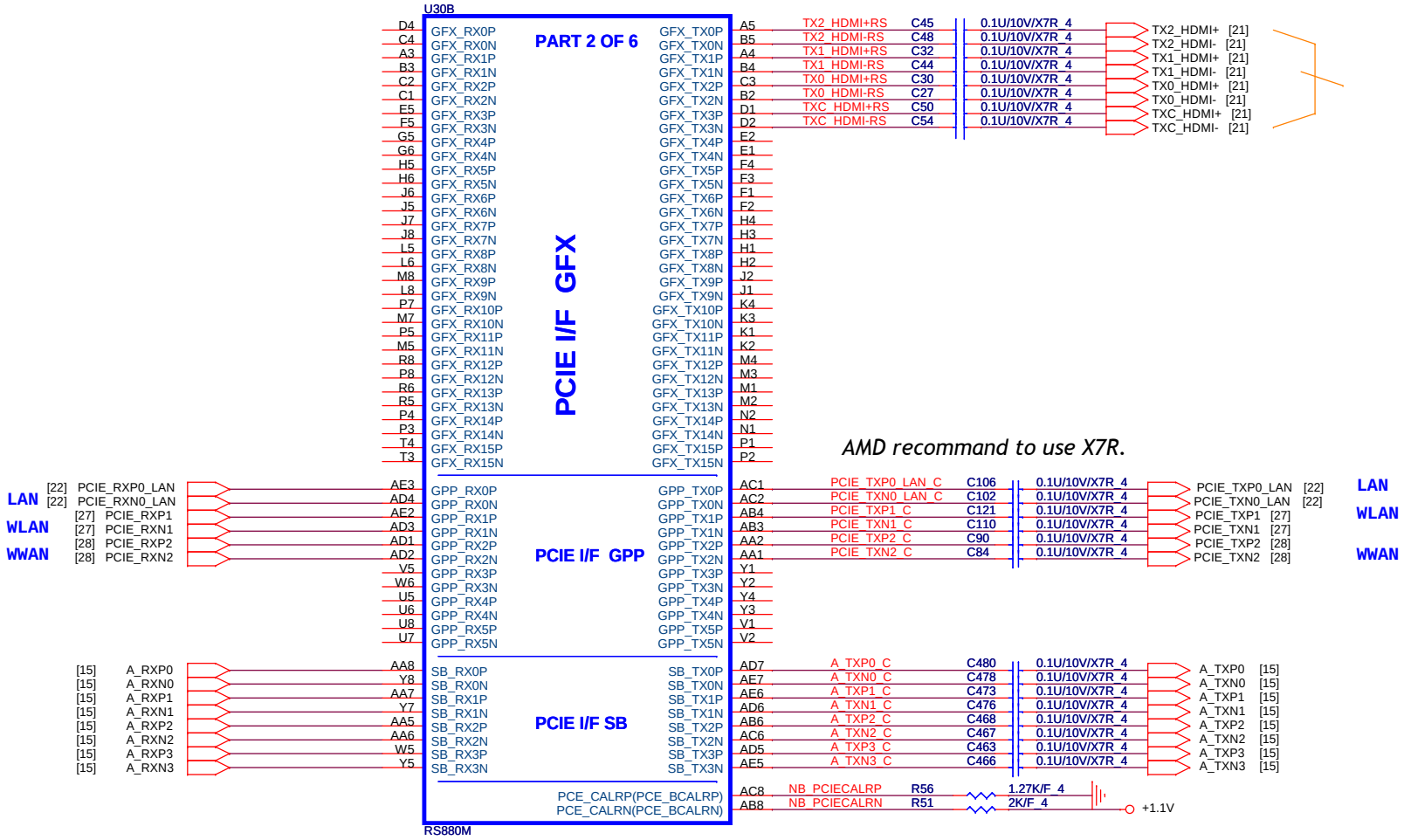
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880M (HT)	1A

Date: Thursday, May 06, 2010 Sheet 10 of 49

Support PCIe Gen2 (Version 2.0)

AMD recommand to use X7R.



105-A75631_00F_HDMI.pdf

TMDS_DATA2+	<>	PETp0
TMDS_DATA2-	<>	PETn0
TMDS_DATA1+	<>	PETp1
TMDS_DATA1-	<>	PETn1
TMDS_DATA0+	<>	PETp2
TMDS_DATA0-	<>	PETn2
TMDS_CLK+	<>	PETp3
TMDS_CLK-	<>	PETn3

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880M (PCIE*4)	1A
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RS880M --- ADD

AVDD-DAC Analog
not applicable to RS880

+3V — BLM18PG181SN1D(180,1.5A)_6 — +3V_AVDD_NB — 110mA
C31 2.2U/6.3V/X5R_6

AVDDI-DAC Digital
not applicable to RS880

+1.8V — R16 0_6 — +1.8V_AVDDI_NB — 20mA
C23 0.1U/10V/X7R_4

AVDDQ-DAC Bandgap
Reference
not applicable to RS880

L6 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_AVDDQ_NB — 4mA
C26 2.2U/6.3V/X5R_6

PLLVDD - Graphics PLL
not applicable to
RS880

+1.1V — L37 BLM18PG181SN1D(180,1.5A)_6 — +1.1V_PLLVDD — 65mA
C459 2.2U/6.3V/X5R_6

PLLVDD18 - Graphics PLL
not applicable to RS880

+1.8V — L8 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_PLLVDD18 — 20mA
C19 10U/6.3V/X5R_8
C35 2.2U/6.3V/X5R_6

VDDA18PCIEPLL -PCIE PLL

+1.8V — 20mils width — L5 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_VDDA18PCIEPLL — 120mA
C25 2.2U/6.3V/X5R_6

VDDA18HTPLL -HT LINK PLL

20mils width — L9 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_VDDA18HTPLL — 20mA
C43 2.2U/6.3V/X5R_6

U30C

RS880M

PART 3 OF 6

CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.

+3V_AVDD_NB — F12 AVDD1(NC)
E12 AVDD2(NC)
+1.8V_AVDDDI_NB — F14 AVDDDI(NC)
G15 AVSSDI(NC)
+1.8V_AVDDQ_NB — H15 AVDDQ(NC)
H14 AVSSQ(NC)

E17 C_Pr(DFT_GPIO5)
F17 Y(DFT_GPIO2)
F15 COMP_Pb(DFT_GPIO4)

[21] INT_CRT_RED — R32 140/F_4 — INT_CRT_RED — G18 RED(DFT_GPIO0)
[21] INT_CRT_GRE — R29 150/F_4 — INT_CRT_GRE — G17 REDb(NC)
[21] INT_CRT_BLU — R26 150/F_4 — INT_CRT_BLU — E18 GREEN(DFT_GPIO1)
F18 GREENb(NC)
E19 BLUE(DFT_GPIO3)
F19 BLUEb(NC)

[21] INT_CRT_HSYNC — INT_CRT_HSYNC — A11 DAC_HSYNC(PWM_GPIO4)
[21] INT_CRT_VSYNC — INT_CRT_VSYNC — B11 DAC_VSYNC(PWM_GPIO6)
[21] INT_DDCDAT — E8 DAC_SDA(PCE_TCALRN)
[21] INT_DDCCLK — F8 DAC_SCL(PCE_RCALRN)

R35 715/F_4 — DAC_RSET_NB — G14 DAC_RSET(PWM_GPIO1)

+1.1V_PLLVDD — A12 PLLVDD(NC)
+1.8V_PLLVDD18 — D14 PLLVDD18(NC)
B12 PLLVSS(NC)

+1.8V_VDDA18HTPLL — H17 VDDA18HTPLL

+1.8V_VDDA18PCIEPLL — D7 VDDA18PCIEPLL1
E7 VDDA18PCIEPLL2

[15] NB_PLTRST# — D8 SYSRESETb
[16] NB_PWRGD_IN — A10 POWERGOOD
NB_LDT_STOP# — C10 LDTSTOPb
NB_ALLOW_LDTSTOP — C12 ALLOW_LDTSTOP

[15] CLK_REFCLKP — C25 HT_REFCLKP
[15] CLK_REFCLKN — C24 HT_REFCLKN

[15] CLK_HT_REFCLKP — E11 REFCLK_P/OSCIN(OSCIN)
[15] CLK_HT_REFCLKN — F11 REFCLK_N(PWM_GPIO3)

[3] EXT_NB_OSC — RP1 0_4P2R_4 — External CLK
+1.1V — R33 4.7K_4 — R34 4.7K_4

R368 4.7K_4 — CLK_NBGFXP — T2 GFX_REFCLKP
R374 4.7K_4 — CLK_NBGFXN — T1 GFX_REFCLKN

T80 — CLK_GPP_REFCLKP — U1 GPP_REFCLKP
T81 — CLK_GPP_REFCLKN — U2 GPP_REFCLKN

[15] CLK_SBLINKP — V4 GPPSB_REFCLKP(SB_REFCLKP)
[15] CLK_SBLINKN — V3 GPPSB_REFCLKN(SB_REFCLKN)

+3V — R353 4.7K_4 — R354 4.7K_4

[20] INT_EDIDDAT — INT_EDIDDAT — A9 I2C_DATA
[20] INT_EDIDCLK — INT_EDIDCLK — B9 I2C_CLK
LX_PE_GPIO2 — T79 — B8 DDC_DATA/AUX0N(NC)
A8 DDC_CLK/AUX0P(NC)

[21] INT_HDMI_SCL — B7 DDC_CLK1/AUX1P(NC)
[21] INT_HDMI_SDA — A7 DDC_DATA1A/AUX1N(NC)

[40] DYN_PWR_EN — DYN_PWR_EN — B10 STRP_DATA

G11 RSVD

RS880_AUX_CAL — C8 AUX_CAL(NC)
R352 150/F_4

NB CORE POWER

+3V — [3,6,8,9,14,15,16,17,18,19,20,21,22,23,24,26,27,28,30,31,32,33,34,36,38,40,41,42]
+1.8V — [13,14,16,38,39,42]
+1.1V — [3,7,11,13,14,18,38,42]

TXOUT_L0P(NC) — A22 — INT_TXLOUTP0 [20]
TXOUT_L0N(NC) — B22 — INT_TXLOUTN0 [20]
TXOUT_L1P(NC) — A21 — INT_TXLOUTP1 [20]
TXOUT_L1N(NC) — B21 — INT_TXLOUTN1 [20]
TXOUT_L2P(NC) — B20 — INT_TXLOUTP2 [20]
TXOUT_L2N(DBG_GPIO0) — A20 — INT_TXLOUTN2 [20]
TXOUT_L3P(NC) — A19
TXOUT_L3N(DBG_GPIO2) — B19

TXOUT_U0P(NC) — B18
TXOUT_U0N(NC) — A18
TXOUT_U1P(PCIE_RESET_GPIO3) — A17
TXOUT_U1N(PCIE_RESET_GPIO2) — B17
TXOUT_U2P(NC) — D20
TXOUT_U2N(NC) — D21
TXOUT_U3P(PCIE_RESET_GPIO5) — D18
TXOUT_U3N(NC) — D19

TXCLK_LP(DBG_GPIO1) — B16 — INT_TXLCLKOUTP [20]
TXCLK_LN(DBG_GPIO3) — A16 — INT_TXLCLKOUTN [20]
TXCLK_UP(PCIE_RESET_GPIO4) — D16
TXCLK_UN(PCIE_RESET_GPIO1) — D17

VDDLTP18(NC) — A13 — +1.8V_VDDLTP18_NB
VSSLTP18(NC) — B13
VDDLT18_1(NC) — A15 — +1.8V_VDDLT_18_NB
VDDLT18_2(NC) — B15
VDDLT33_1(NC) — A14
VDDLT33_2(NC) — B14

VSSLT1(VSS) — C14
VSSLT2(VSS) — D15
VSSLT3(VSS) — C16
VSSLT4(VSS) — C18
VSSLT5(VSS) — C20
VSSLT6(VSS) — E20
VSSLT7(VSS) — C22

LVDS_DIGON(PCE_TCALRP) — E9 — INT_LVDS_VDDEN [20]
LVDS_BLON(PCE_RCALRP) — E7 — INT_LVDS_BRIGHT [20]
LVDS_ENA_BL(PWM_GPIO2) — G12 — INT_LVDS_BLON [20]

R499 4.7K/J_4

HDMI PLUG DET

TMDS_HPD(NC) — D9 — INT_HDMI_HPD [21]
HPD(NC) — D10 — T78
SUS_STAT#(PWM_GPIO5) — D12 — SUS_STAT#_NB — R12 *Short_4 — SUS_STAT# [16]

THERMALDIODE_P — AE8 — RS880_THRMDA — T83
THERMALDIODE_N — AD8 — RS880_THRMDC — T84

TESTMODE — D13 — TEST_EN
R351 1.82K/F_4

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M
1 Disable
0 Enable

INT_CRT_VSYNC — R358 3K_4 — +3V

RS880M: Enables Side port memory

RS880M:INT_HSYNC_COM

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

DAC_HSYNC	
PULLED DOWN	Side-Port / Enable
PULLED UP	Side-Port / Disable

INT_CRT_HSYNC — R356 *3K/J_4 — +3V
R357 3K_4

For extrnal EEPROM Debug only **RS880**

DYN_PWR_EN — R355 2K/F_4

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

+1.8V

15mA — +1.8V_VDDLTP18_NB — L36 BLM18PG181SN1D(180,1.5A)_6
C458 2.2U/6.3V/X5R_6

VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RS880

300mA — +1.8V_VDDLT_18_NB — L4 BLM21PG221SN1D(220,100M,2A)_8
C460 0.1U/10V/X7R_4
C17 4.7U/6.3V/X5R_6

VDDLT18 - LVDS or DVI/HDMI digital not applicable to RS880

+1.5VSUS — R89 300_4
+1.5VSUS — R90 2K_4
+1.8V — R77 4.7K_4
Q11 MMBT3904_NL(40V,0.2A)

[6,15] CPU_LDT_STOP# — R78 *Short_4 — NB_LDT_STOP#

ECA09

+1.8V — R359 1K_4

[15] ALLOW_LDTSTOP — R360 *0/short_4 — NB_ALLOW_LDTSTOP

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880M (CLK,DISP,PLL)	1A

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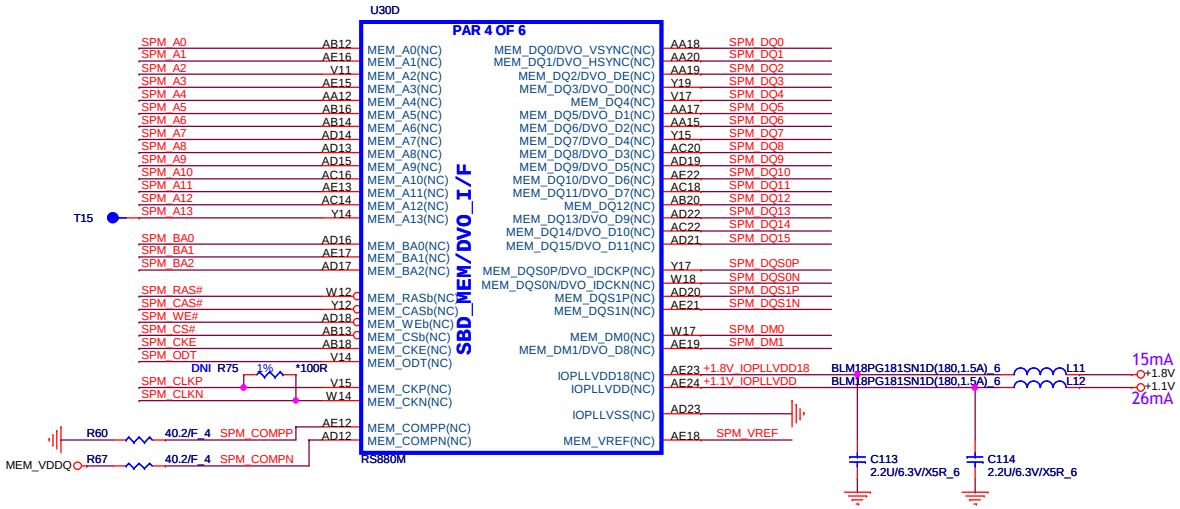
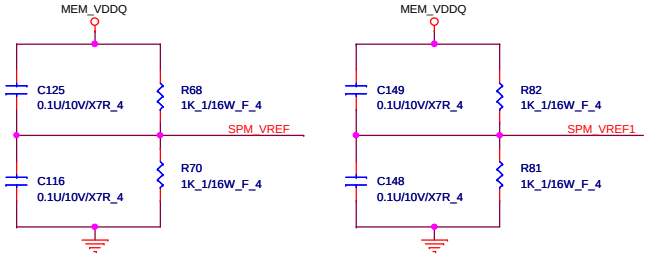
Support an optional dedicated local frame buffer (side-port) up to 32MB through a 16-bit interface. Note however, that the memory interface is optimized for a 64MB local frame buffer. As such, the system BIOS will downsize the side-port size if a 128MB memory device is populated.

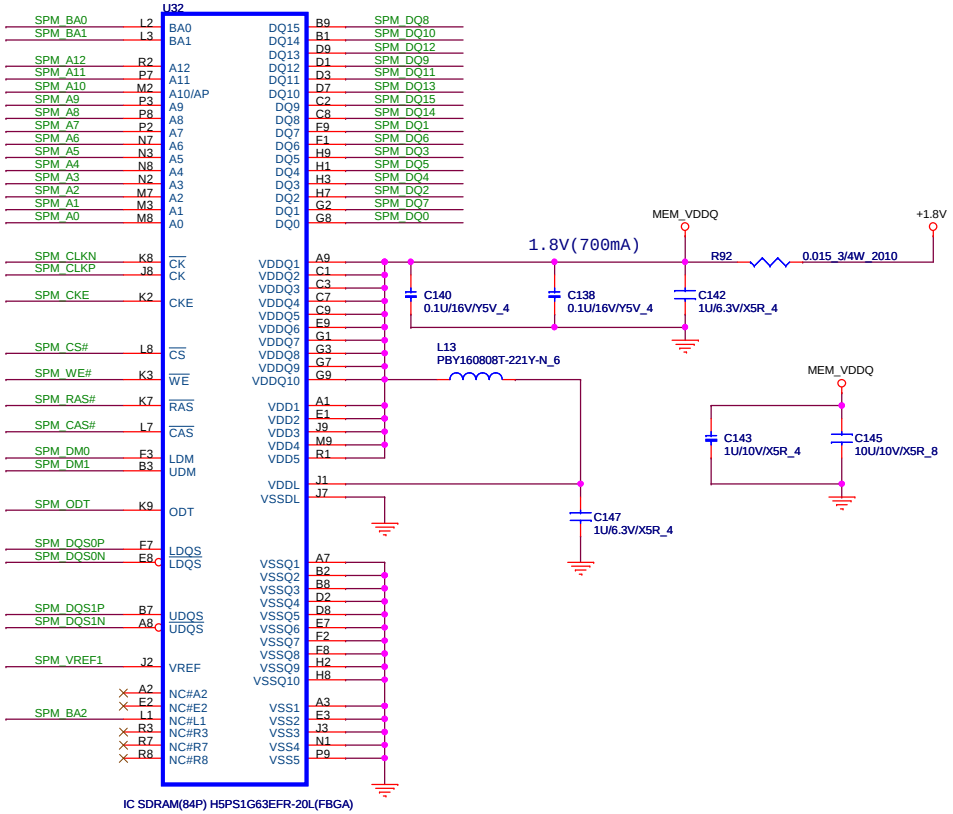
+1.8V [12,14,16,38,39,42]
+1.1V [3,7,11,12,14,18,38,42]

This block is for UMA only , DIS can remove all component





Side Port / VRAM --> DDR2



PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880M (SIDEPORT,VRAM)	1A

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+1.1V_DYN [40,42]
[3,6,8,9,12,15,16,17,18,19,20,21,22,23,24,26,27,28,30,31,32,33,34,36,38,40,41,42]
+1.1V [3,7,11,12,13,18,38,42]
+1.8V [12,13,16,38,39,42]

U30F RS880M

PART 6/6

GROUND

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

+1.1V 2A for RS880M

VDDHT - HT LINK digital I/O for RS880
VDDHT plane cut with a width 35 mils

VDDHTRX - HT LINK RX I/O for RS880
(at least 40 mils with area fills under ASIC)

VDDHTTX - HT LINK TX I/O for RS880
thick trace (at least 20 mils with area fills under ASIC)

+1.1V 2A for RS880M

For Geneva ASB2 CPU, please design 1.1V for VDDHTTX.

600mA +1.1V
R37 0_8 C55 4.7U/6.3V/X5R_6
+1.1V_VDDHT
C73 0.1U/10V/X7R_4 C64 0.1U/10V/X7R_4 C69 0.1U/10V/X7R_4

700mA
R20 0_8 C49 4.7U/6.3V/X5R_6
+1.1V_VDDHTRX
C56 0.1U/10V/X7R_4 C34 0.1U/10V/X7R_4 C53 0.1U/10V/X7R_4

500mA +1.1V
R48 0_8 C76 4.7U/6.3V/X5R_6
+1.1V_VDDHTTX
C103 0.1U/10V/X7R_4 C109 0.1U/10V/X7R_4 C78 0.1U/10V/X7R_4 C74 0.1U/10V/X7R_4

U30E

PART 5/6

POWER

J17 VDDHT_1	A6 VDDPCIE_1
K16 VDDHT_2	B6 VDDPCIE_2
L16 VDDHT_3	C6 VDDPCIE_3
M16 VDDHT_4	D6 VDDPCIE_4
P16 VDDHT_5	E6 VDDPCIE_5
R16 VDDHT_6	F6 VDDPCIE_6
T16 VDDHT_7	G7 VDDPCIE_7
	H8 VDDPCIE_8
	J9 VDDPCIE_9
H18 VDDHTRX_1	K9 VDDPCIE_10
G19 VDDHTRX_2	M9 VDDPCIE_11
F20 VDDHTRX_3	L9 VDDPCIE_12
E21 VDDHTRX_4	P9 VDDPCIE_13
D22 VDDHTRX_5	R9 VDDPCIE_14
B23 VDDHTRX_6	T9 VDDPCIE_15
A23 VDDHTRX_7	V9 VDDPCIE_16
	U9 VDDPCIE_17
AE25 VDDHTTX_1	K12 VDDC_1
AD24 VDDHTTX_2	J14 VDDC_2
AC23 VDDHTTX_3	U16 VDDC_3
AB22 VDDHTTX_4	J11 VDDC_4
AA21 VDDHTTX_5	K15 VDDC_5
Y20 VDDHTTX_6	M12 VDDC_6
W19 VDDHTTX_7	L14 VDDC_7
V18 VDDHTTX_8	L11 VDDC_8
U17 VDDHTTX_9	M13 VDDC_9
T17 VDDHTTX_10	M15 VDDC_10
R17 VDDHTTX_11	N12 VDDC_11
P17 VDDHTTX_12	N14 VDDC_12
M17 VDDHTTX_13	P11 VDDC_13
	P13 VDDC_14
J10 VDDA18PCIE_1	P14 VDDC_15
P10 VDDA18PCIE_2	R12 VDDC_16
K10 VDDA18PCIE_3	R15 VDDC_17
M10 VDDA18PCIE_4	T11 VDDC_18
L10 VDDA18PCIE_5	T15 VDDC_19
W9 VDDA18PCIE_6	U12 VDDC_20
H9 VDDA18PCIE_7	T14 VDDC_21
T10 VDDA18PCIE_8	J16 VDDC_22
R10 VDDA18PCIE_9	
Y9 VDDA18PCIE_10	AE10 VDD_MEM1(NC)
AA9 VDDA18PCIE_11	AA11 VDD_MEM2(NC)
AB9 VDDA18PCIE_12	Y11 VDD_MEM3(NC)
AD9 VDDA18PCIE_13	AD10 VDD_MEM4(NC)
AE9 VDDA18PCIE_14	AB10 VDD_MEM5(NC)
U10 VDDA18PCIE_15	AC10 VDD_MEM6(NC)
F9 VDDG18_1(VDD18_1)	H11 VDDG33_1(NC)
G9 VDDG18_2(VDD18_2)	H12 VDDG33_2(NC)
AE11 VDD18_MEM1(NC)	
AD11 VDD18_MEM2(NC)	

RS880M

+1.8V 1A for RS880M+SB820

700mA +1.8V
L10 BLM21PG221SN1D(220,100M,2A)_8
+1.8V_VDDA18PCIE
C62 4.7U/6.3V/X5R_6
C66 4.7U/6.3V/X5R_6 C83 0.1U/10V/X7R_4 C80 0.1U/10V/X7R_4 C77 0.1U/10V/X7R_4 C67 0.1U/10V/X7R_4

VDDA18PCIE - PCIE TX stage I/O for RS880

VDD18 - RS880 I/O transform

25mA +1.8V
R17 0_6 10mA
+1.8V_VDDG18_NB
C28 1U/10V/X5R_4

25mA +1.8V
R65 0_6
+1.8_MEM
C126 1U/10V/X5R_4
R66 *0/J_6

VDDPCIE - PCIE-E Main power

2.5A
+1.1V_VDD_PCIE
C58 0.1U/10V/X7R_4 C72 0.1U/10V/X7R_4 C51 1U/10V/X5R_4 C33 1U/10V/X5R_4 C60 4.7U/6.3V/X5R_6
R36 0_8 +1.1V

AMD suggest customer to implement voltage scaling(0.95V/1.1V) as per PowerPlay functional.

VDDC - Core Logic power
12A
+1.1V_DYN
C68 0.1U/10V/X7R_4 C57 0.1U/10V/X7R_4 C79 0.1U/10V/X7R_4 C61 0.1U/10V/X7R_4 C82 10U/6.3V/X5R_8
C70 0.1U/10V/X7R_4 C71 0.1U/10V/X7R_4 C63 0.1U/10V/X7R_4 C81 10U/6.3V/X5R_8

1.8V is for DDR3 800MHz and lower.
1.5V is for DDR3 1066 and above

100mA
R64 0/J_6 +1.8V
R71 *0_6 +1.5V
R62 *0/J_6
+1.5V_VDD_MBM
C111 0.1U/10V/X7R_4 C92 0.1U/10V/X7R_4 C115 1U/6.3V/X5R_4 C108 1U/6.3V/X5R_8 C101 10U/6.3V/X5R_8 C112 10U/6.3V/X5R_8
RS880

+3V_VDDG33
R11 0_6 +3V 60mA,15mil
C21 0.1U/10V/X7R_4 C24 0.1U/10V/X7R_4

VDD33 - 3.3V I/O
Not applicable to RX780

If the side-port memory interface is not used:
- The memory interface I/O power (VDD_MEM) is connected to GND.
- The memory interface I/O transform power (VDD18_MEM) is connected to GND plane

(preferred) or connected to 1.8 V.

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880M (PWR,GND)	1A
Date: Thursday, May 06, 2010	Sheet 14 of 49	

+1.1V_PCIE_VDDR [18]
+3VS [6,16,17,18,19,25,27,30,32,42]
3VPCU [20,21,22,25,32,33,35,36,38,40,42]
+3V [3,6,8,9,12,14,16,17,18,19,20,21,22,23,24,26,27,28,30,31,32,33,34,36,38,40,41,42]

Add AND gate to reset all PCIE devices by AMD recommand

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U7017

To RS880

SB820 Part 1 of 5

PCI EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

PCI CLKS

LPC

CPU

RTC

STRAP Function To EC

Debug STRAPs

All the PCI bus has build-in Pull-UP/Down resistors

To RS880M

To RS880M

CPU_CLK

To WLAN Connector

To LAN Controller

To WWAN Connector

To STRAPs Page

RTC_CLK must ready refore RSMRST#

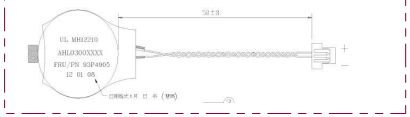
INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

RTC

20mils 20mils 20mils 20mils 20mils

D5 RB500V-40
D4 RB500V-40
R94 510/F_6
C166 1U/6.3V/X5R_4
R87 1K_4
G1 *SHORT_PAD1
BT1 RTC_CON

RTC P/N: AHL03002009 (CR2025)
Don't support chargeable Battery



PROJECT MK-2.0/DU-1.0 NOTE AMD NILE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820 PCIE/LPC/CPU IF	1A

Date: Friday, May 07, 2010 Sheet 15 of 49

+3V [3,6,8,9,12,14,15,17,18,19,20,21,22,23,24,26,27,28,30,31,32,33,34,36,38,40,41,42]
+3VS5 [6,15,17,18,19,25,27,30,32,42]
+1.8V [12,13,14,38,39,42]

SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R144 2.2K_4 PCLK_SMB
R149 2.2K_4 PDAT_SMB

Clock gen/Robson/TV tuner
/DDR3/DDR3 thermal/Accelerometer

+1.8V
R413 300_4
[12] NB_PWRGD_IN
R414 *Short_4 WD_PWRGD

NB POWERGOOD / VDD18
SB/ PWR_GOOD / VDDIO_33_S

SB800
SB_TEST0,SB_TEST1,SB_TEST2
has internal 10K PD.

[22,27] PCIE_WAKE#
C334 100P/50V/X7R_4

+3VS5 R267 10K/F_4 SYS_RST#
+3V R406 *10K/F_4 GATEA20
By AMD confirm

+3VS5 R446 2.2K_4 DNBSWON#
+3V R229 4.7K_4 SUS_STAT#

+3VS5 R202 *10K/F_4 CPU_THERMTRIP#

Add SB_GPIO_RST# form AMD recommand

SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it

+3VS5 R265 10K/F_4 R262 10K/F_4
+3V R415 *10K/F_4

To Azalia
HD audio interface is 3.3S5 voltage

[23] ACZ_BITCLK_AUDIO
[19] ACZ_SDOUT
[23] ACZ_SDOUT_AUDIO
[23] ACZ_SDIN0
[23] ACZ_SYNC_AUDIO
[23] ACZ_RST#_AUDIO
C376 10P/50V/C0G_4
C368 *10P/50V/C0G_4
C375 *10P/50V/C0G_4
C350 *10P/50V/C0G_4
R242 33_4
R244 33_4
R241 *10K_4
R243 *10K_4
R246 *10K_4
R240 33_4
R225 33_4
ACZ_BITCLK_R
ACZ_SDOUT
ACZ_SYNC_R
ACZ_RST#_R

+3VS5 R220 10K/F_4 SB_PWRGD_IN
C356 *2.2U/6.3V/X5R_6
[41] DELAY_VR_PWRGOOD
[33] ECPWROK
D11 BAT54A
NB/SB POWER GOOD CIRCUIT

U33D
SB820
Part 4 of 5
SB800 A11

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC
GPIO
USB 2.0
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL

[5] MEM_GEVEN#
T102 RI#
T67 SPI_CS3#
[33] PM_SLP_S3#
[33] PM_SLP_S4#
[33] DNBSWON#
DNBSWON#
SB_PWRGD_IN
[12] SUS_STAT#
SUS_STAT#
T64 SB_TEST0
T60 SB_TEST1
T56 SB_TEST2
[33] GATEA20
[33] RCIN#
[33] SCI#
[33] KBSMI#
T103
SYS_RST#
[6] CPU_THERMTRIP#
CPU_THERMTRIP#
WD_PWRGD
[33] ICH_RSMRST#
R419 *0_4
[3,28] PCIE_REQ_WWAN#
T44
[15] SB_GPIO_RST#
[3,22] PCIE_REQ_LAN#
R418 *0_4
T97
T43
[23] ACZ_SPKR
[3,8,9,32] PCLK_SMB
[3,8,9,32] PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1
[3,27] PCIE_REQ_WLAN#
R417 *0_4
LX_VGA_REQ_R
ACCLED_EN
T62
[20] LCD_BK_OFF
SP_DDR3_RST#
+1.5V R268 *10K/F_4
T45
[8] CPU_MEMHOT#
D10 *CH500V-40PT
CPU_MEMHOT#_IN
R261 *10K_4
T58
[25] USBOC2#
[25] USBOC1#
[25] USBOC0#
T42
T96
R247 *10K_4

USBCLK/14M_25M_48M_OSC
USB_RCOMP
CLK_48M_USB [3]
T66
R156 11.8K/F_4
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USBP8+ T47
USBP8- T46
USBP7+ [20]
USBP7- [20] CCD
USBP6+ [26]
USBP6- [26] 4 IN 1 CARD READER (MMC)
USBP5+ [27]
USBP5- [27] Min-Card(WLAN)
USBP4+ [28]
USBP4- [28] Min-Card(WWAN)
USBP3+ [30]
USBP3- [30] BLUETOOTH
USBP2+ [25]
USBP2- [25] USB3 Connector (FB SIDE)
USBP1+ [25]
USBP1- [25] USB2 Connector (FB SIDE)
USBP0+ [25]
USBP0- [25] USB1 Connector (MB SIDE)

SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
SB_SCLK2 R412 10K/F_4 +3VS5
SB_SDATA2 R136 10K/F_4
SB_SCLK3 R407 10K/F_4 +3VS5
SB_SDATA3 R405 10K/F_4
SB_GPIO199 R153 *10K/F_4 +3VS5
SB_GPIO200 R416 2.2K_4

GPIO200	GPIO199
H,H = Reserved	
H,L = SPI ROM	
L,H = LPC ROM (Default)	
L,L = FWH ROM	

SB_SCLK2 R411 *2.2K_4
SB_SDATA2 R137 *2.2K_4
SB_SCLK3 R409 *2.2K_4
SB_SDATA3 R404 *2.2K_4
SB_SMBCLK1 R266 *2.2K_4
SB_SMBDATA1 R263 *2.2K_4

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE
Quanta Computer Inc.
Size: Custom
Document Number: SB820 ACPI/GPIO/USB
Rev: 1A
Date: Friday, May 07, 2010
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SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB820

SATA HDD

[24] SATA_TXP0 — C519 0.01U/16V/X7R_4 SATA_TXP0_C — AH9 SATA_TX0P
[24] SATA_TXN0 — C517 0.01U/16V/X7R_4 SATA_TXN0_C — AJ9 SATA_TX0N
[24] SATA_RXN0 — C520 0.01U/16V/X7R_4 SATA_RXN0_C — AJ8 SATA_RX0N
[24] SATA_RXP0 — C521 0.01U/16V/X7R_4 SATA_RXP0_C — AH8 SATA_RX0P

U33B

SB820
Part 2 of 5

AH10 SATA_TX1P
AJ10 SATA_TX1N
AG10 SATA_RX1N
AF10 SATA_RX1P
AG12 SATA_TX2P
AF12 SATA_TX2N
AJ12 SATA_RX2N
AH12 SATA_RX2P
AH14 SATA_TX3P
AJ14 SATA_TX3N
AG14 SATA_RX3N
AF14 SATA_RX3P
AG17 SATA_TX4P
AF17 SATA_TX4N
AJ17 SATA_RX4N
AH17 SATA_RX4P
AJ18 SATA_TX5P
AH18 SATA_TX5N
AH19 SATA_RX5N
AJ19 SATA_RX5P

SERIAL ATA

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820

XTLVDD_SATA-- SATA crystal power

PLVDD_SATA-- SATA PLL POWER

+1.1V_AVDD_SATA — R171 1K/F_4 SATA_CALRP — AB14 SATA_CALRP
R170 931/F_4 SATA_CALRN — AA14 SATA_CALRN

+3V — R184 10K/F_4 — AD11 SATA_ACT#/GPIO67

C289 *22P/50V/NPO_4 — SATA_X1 AD16 SATA_X1
Y1 *25MHZ
R178 *1M/F_4
C311 *22P/50V/NPO_4 — SATA_X2 AC16 SATA_X2

T61 — ROM_RST# — G2 ROM_RST#/GPIO161

J5 SPI_DI/GPIO164
E2 SPI_DO/GPIO163
K4 SPI_CLK/GPIO162
K9 SPI_CS1#/GPIO165

SPI ROM

SB800 A11

FC_CLK AH28
FC_FBCLKOUT AG28
FC_FBCLKIN AF26

FC_OE#/GPIOD145 AF28
FC_AVD#/GPIOD146 AG29
FC_WE#/GPIOD148 AG26
FC_CE1#/GPIOD149 AF27
FC_CE2#/GPIOD150 AE29
FC_INT1/GPIOD144 AF29
FC_INT2/GPIOD147 AH27

FC_ADQ0/GPIOD128 AJ27
FC_ADQ1/GPIOD129 AJ26
FC_ADQ2/GPIOD130 AH25
FC_ADQ3/GPIOD131 AH24
FC_ADQ4/GPIOD132 AG23
FC_ADQ5/GPIOD133 AH23
FC_ADQ6/GPIOD134 AJ22
FC_ADQ7/GPIOD135 AG21
FC_ADQ8/GPIOD136 AF21
FC_ADQ9/GPIOD137 AH22
FC_ADQ10/GPIOD138 AJ23
FC_ADQ11/GPIOD139 AF23
FC_ADQ12/GPIOD140 AJ24
FC_ADQ13/GPIOD141 AJ25
FC_ADQ14/GPIOD142 AG25
FC_ADQ15/GPIOD143 AH26

FLASH

NC1 G27
NC2 Y2

FANOUT0/GPIO52 W5 — CCD_ON [20]
FANOUT1/GPIO53 W6 — BT_ON [27,30]
FANOUT2/GPIO54 Y9 — WLAN_OFF# [27]

FANIN0/GPIO56 W7 — BT_DET# [30]
FANIN1/GPIO57 V9 — WWAN_OFF# [28]
FANIN2/GPIO58 W8

TEMPIN0/GPIO171 B6 TEMPIN0
TEMPIN1/GPIO172 A6 TEMPIN1
TEMPIN2/GPIO173 A5 TEMPIN2
TEMPIN3/TALERT#/GPIO174 B5 PM_THERM# — PM_THERM# [6]
TEMP_COMM C7

R217 10K/F_4 — +3VS5

VIN0/GPIO175 A3 CPU_TYPE
VIN1/GPIO176 B4 SB_HOLE_TIME
VIN2/GPIO177 A4 CPU_SENSOR
VIN3/GPIO178 C5 SIDE_PORT
VIN4/GPIO179 A7 BOARD_ID0
VIN5/GPIO180 B7 BOARD_ID1
VIN6/GBE_STAT3/GPIO181 B8 BOARD_ID2
VIN7/GBE_LED3/GPIO182 A8 BOARD_ID3

HW MONITOR

AMD recommand : TEMPIN0 / TEMPIN1 / TEMPIN2 can not maintain on floating stages when without usage. Do not care pull high or pull down.

TEMPIN2 — R232 10K_4
TEMPIN1 — R231 10K_4
TEMPIN0 — R236 10K_4

SIDE_PORT	GPIO178
W/SIDE_PORT	1
WO/SIDE_PORT	0

CPU THERMAL	GPIO179
External	1
SB-TSI	0

SB8XX Hold Time	GPIO180
1.2V	1
1.1V	0

DU1/MK2	GPIO181
DU1.0 AMD	0
MK2.0 AMD	1

MB ID

+3VS5

R426 10K_4 BOARD_ID0 R427 *10K_4
R430 *10K_4 BOARD_ID1 R429 10K_4
R433 *10K_4 BOARD_ID2 R432 10K_4
R423 10K_4 BOARD_ID3 R422 *10K_4

+3VS5 R500 *10K/F_4 CPU_TYPE R501 10K/F_4
+3VS5 R440 10K/F_4 SIDE_PORT R438 *10K/F_4
+3VS5 R431 *10K/F_4 CPU_SENSOR R436 10K/F_4
+3VS5 R496 *10K/F_4 SB_HOLE_TIME R495 10K/F_4

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820 SATA/BIDs	1A

Date: Thursday, May 06, 2010 Sheet 17 of 49

+3V [3,6,8,9,12,14,15,16,17,19,20,21,22,23,24,26,27,28,30,31,32,33,34,36,38,40,41,42]
+1.1V [7,11,12,13,14,38,42]
+3VS5 [6,15,16,17,19,25,27,30,32,42]
+1.1VS5 [38,42]

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDDIO_18_FC is for IDE/Flash IO power. In mobile platform, SB820M does not support this function. It only implement in SB800.

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

U33C SB820 Part 3 of 5

POWER

VDDQ--3.3V I/O power 131mA
VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power 71mA
AMD recommand remove +1.8v
PCIE_VDDR--PCIE I/O power 600mA
AVDD_SATA--SATA phy power 567mA
AVDDTX--USB Phy Analog I/O power 658mA
93mA,15 mil
43mA
TBDmA
For support USB wakeup-->3V_S5

VDD-- S/B CORE power 790mA
CKVDD_1.1V--Internal clock Generator I/O power 382mA
S5_3.3--3.3v standby power
S5_1.1V--1.1V standby power
39mA
115mA
15 mA
197mA
47mA
62mA
17mA
5mA
32mA

U33E SB820 Part 5 of 5

GROUND

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE
Quanta Computer Inc.
Size: Custom | Document Number: SB820 PWR/GND | Rev: 1A
Date: Thursday, May 06, 2010 | Sheet 18 of 49

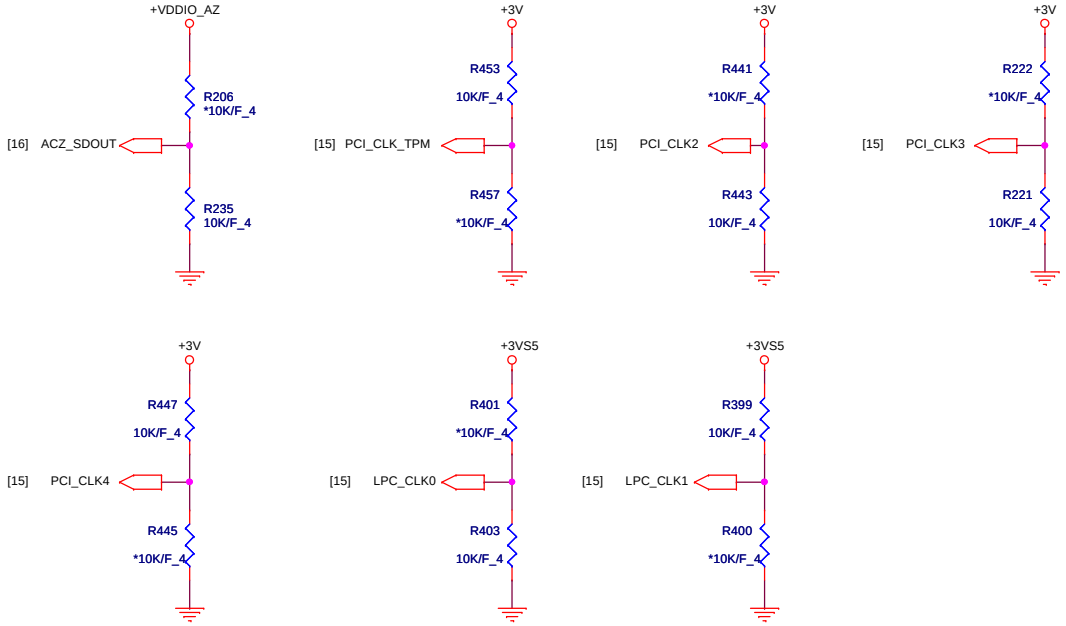
SB800 A11

+VDDIO_AZ [18]
+3V [3,6,8,9,12,14,15,16,17,18,20,21,22,23,24,26,27,28,30,31,32,33,34,36,38,40,41,42]
+3VS5 [6,15,16,17,18,25,27,30,32,42]

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need

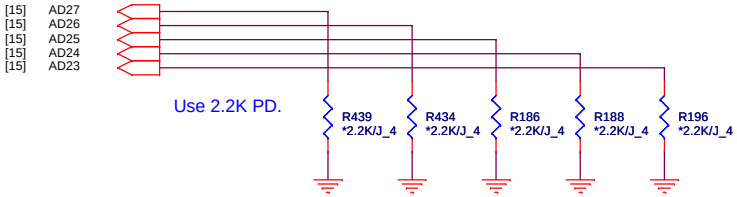
REQUIRED STRAPS



PCI_CLK4 CPU/NB HT Clock Selection
0 V – Reserved.
3.3 V – Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

DEBUG STRAPS

SB820 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

REQUIRED STRAPS

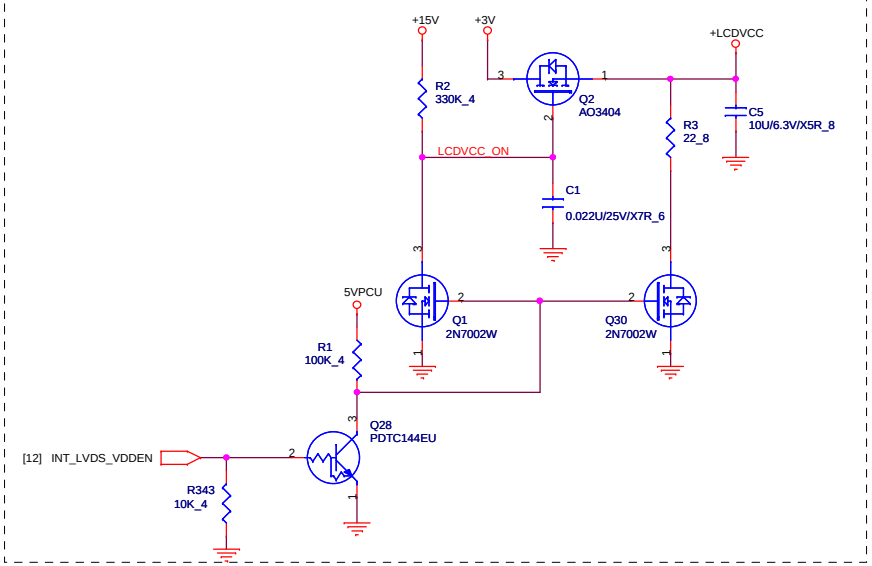
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

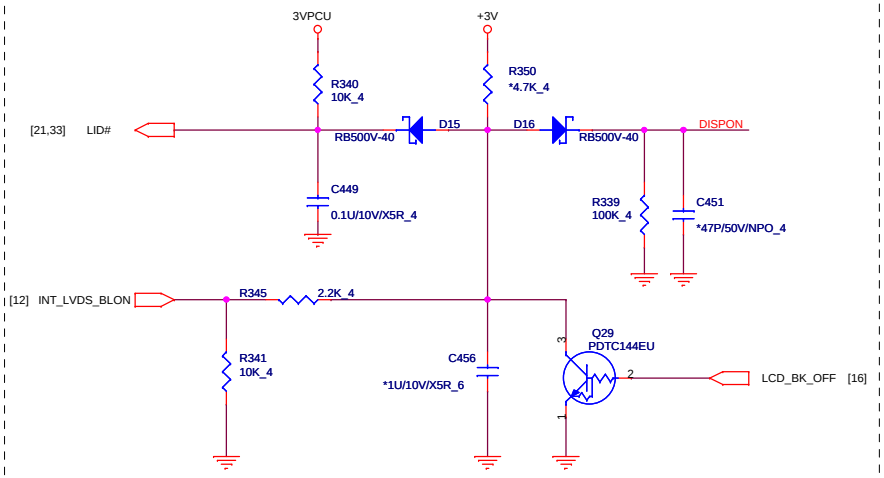
Quanta Computer Inc.

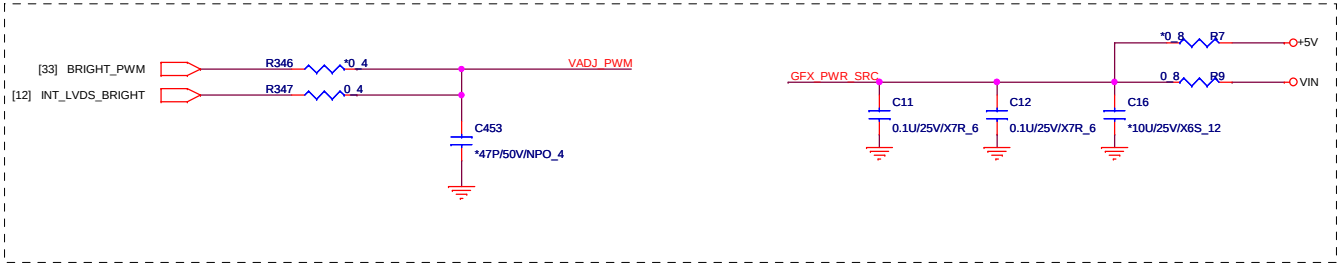
Size	Document Number	Rev
Custom	SB820 STRAPS/PWRGD	1A
Date: Thursday, May 06, 2010	Sheet 19 of 49	

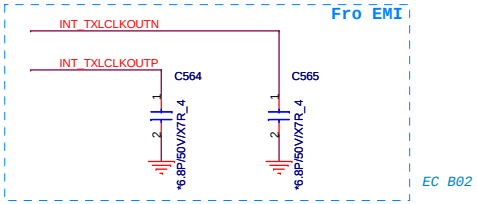
LCDVCC

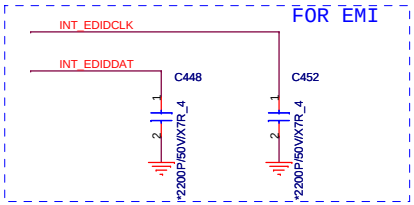


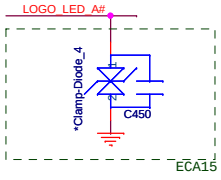
Back light

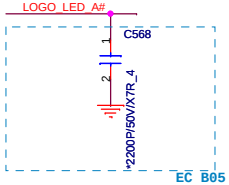


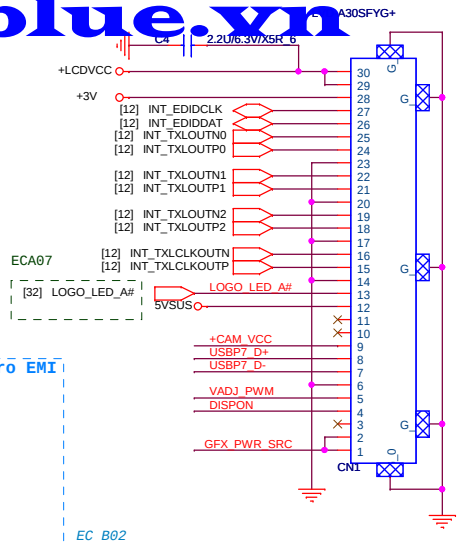


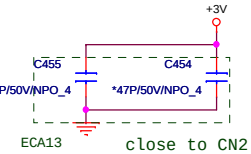






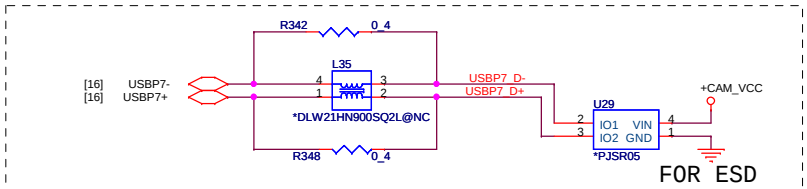


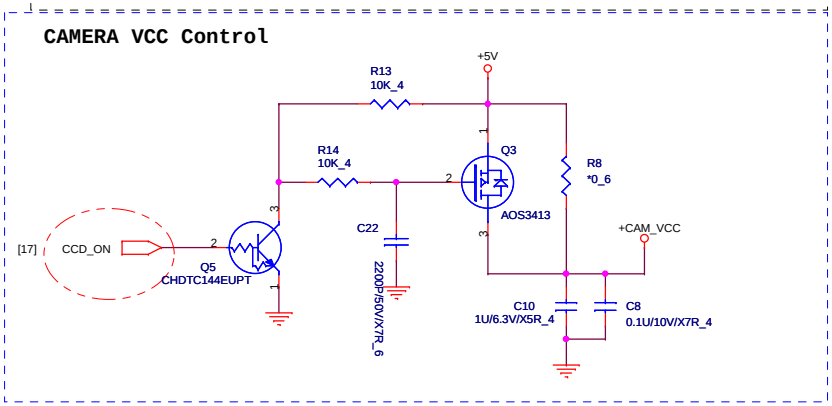




LVDS (11.6") (1024x600, 1366x768)

+3V	[3,6,8,9,12,14,15,16,17,18,19,21,22,23,24,26,27,28,30,31,32,33,34,36,38,40,41,42]
3VPCU	[15,21,22,25,32,33,35,36,38,40,42]
+15V	[30,36,42]
+5V	[21,23,24,29,31,33,34,42]
VIN	[35,36,37,38,40,41,42]
5VSUS	[32,38,40,41,42]





PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD/CAMERA	1A

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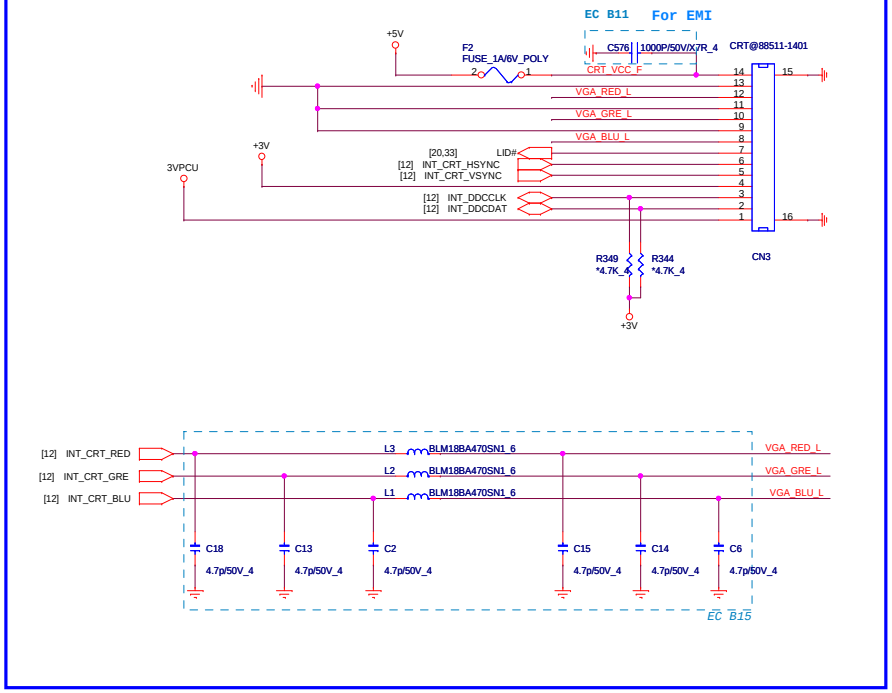
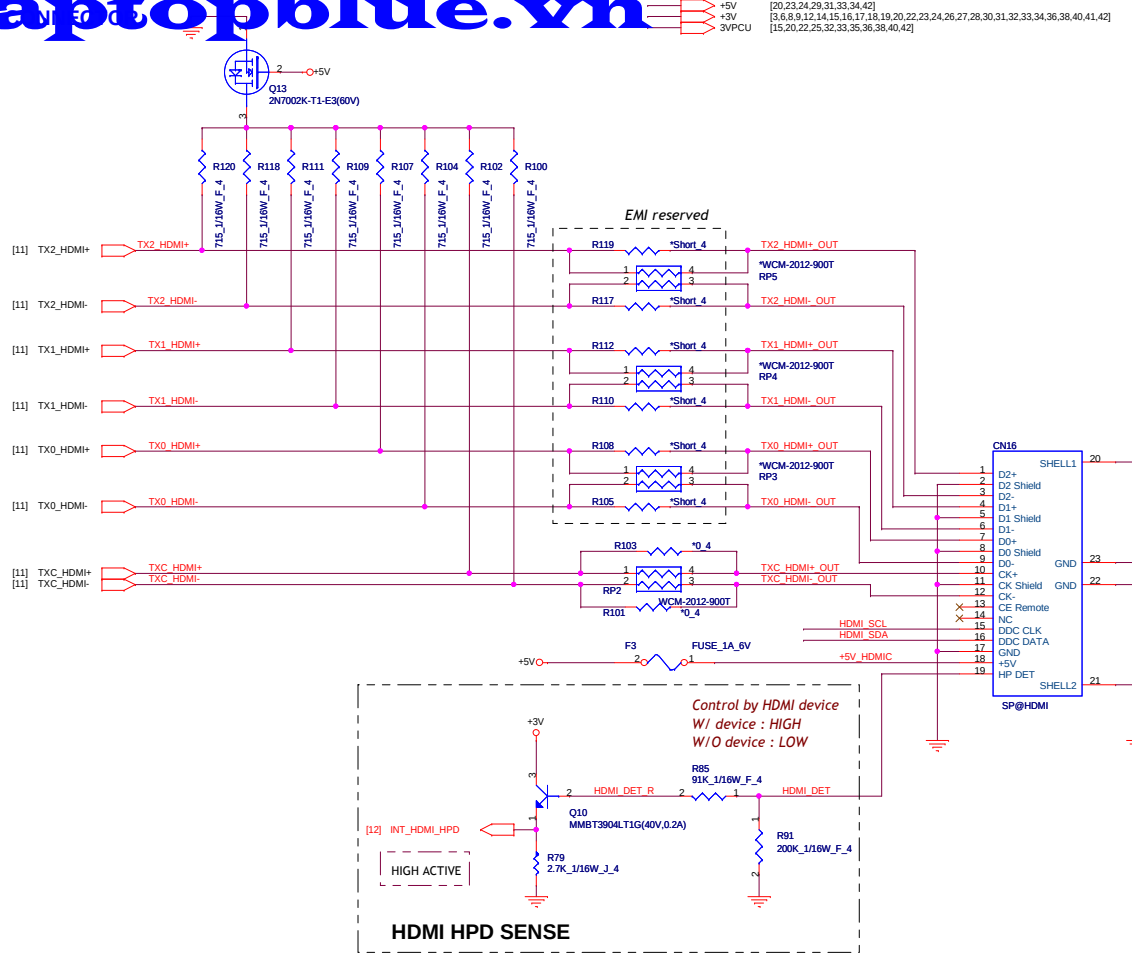
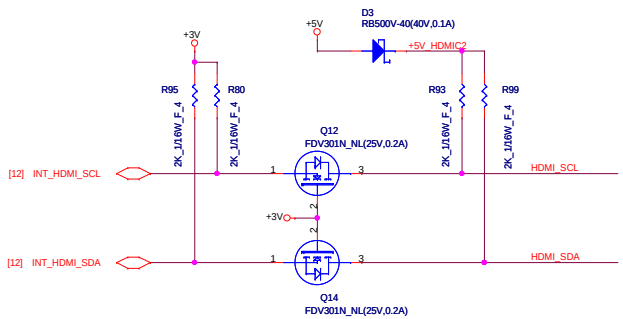
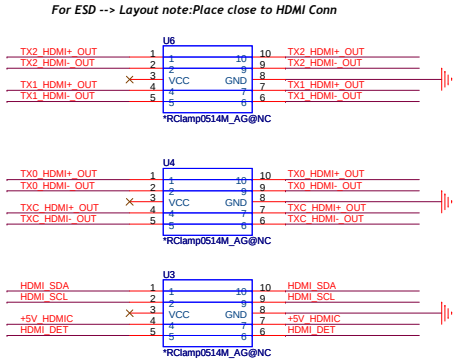
CRT FFC CONNECTOR









PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT CONN	1A

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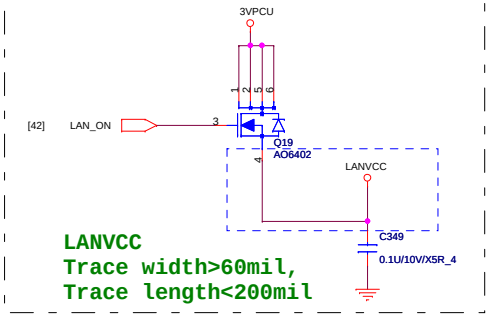
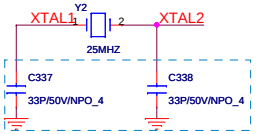
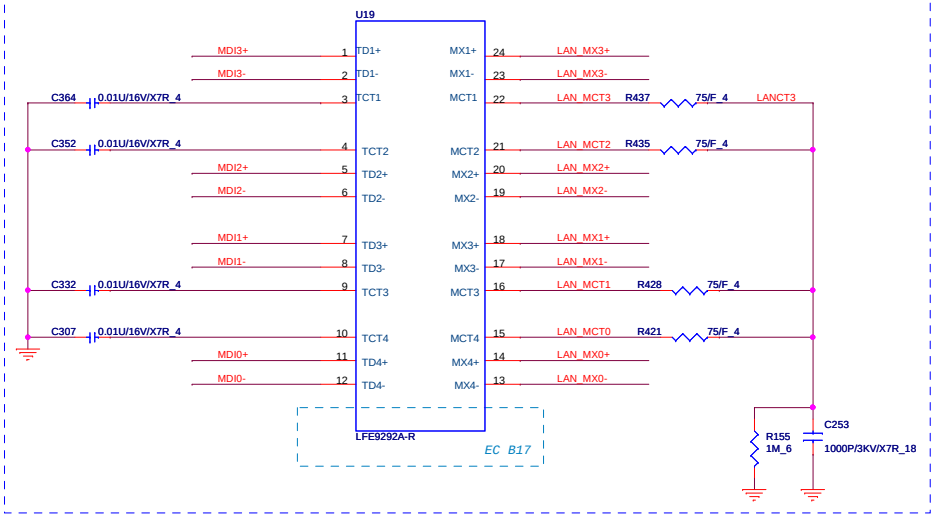
LANVCC

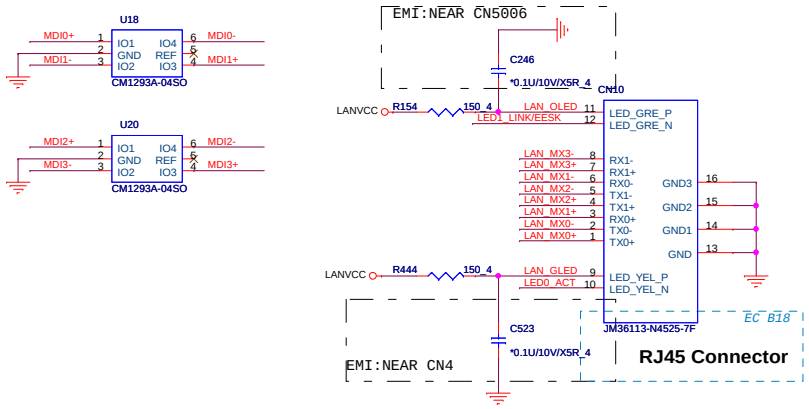




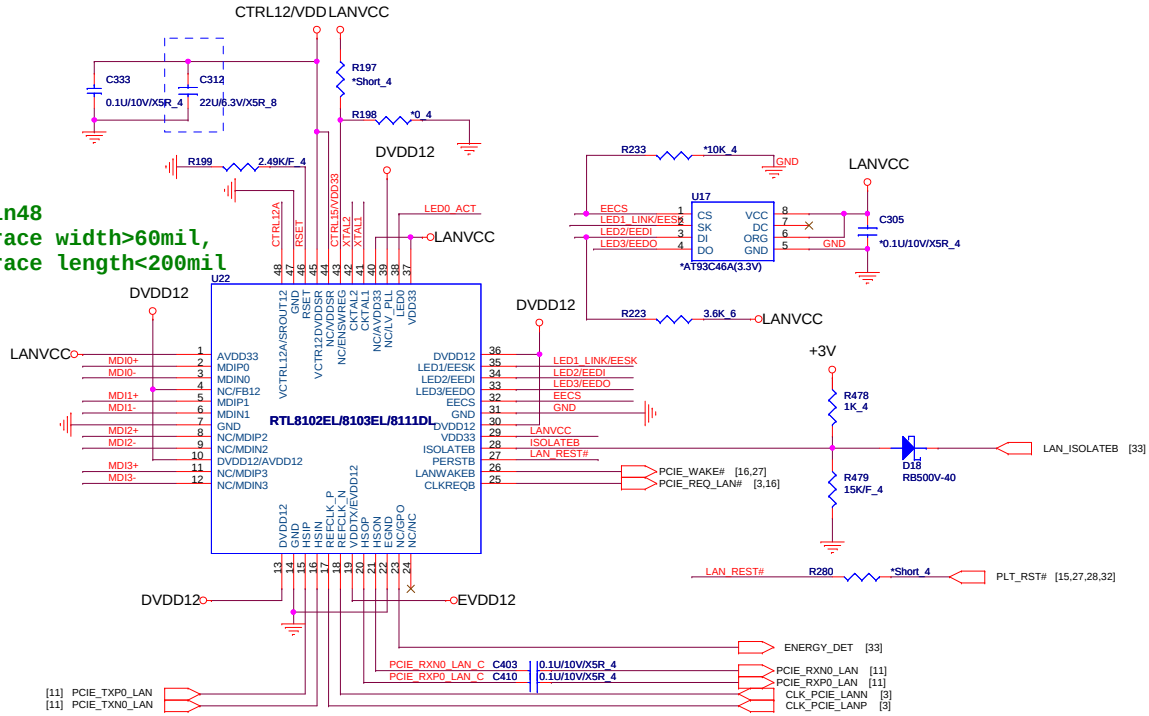
Tramsformer



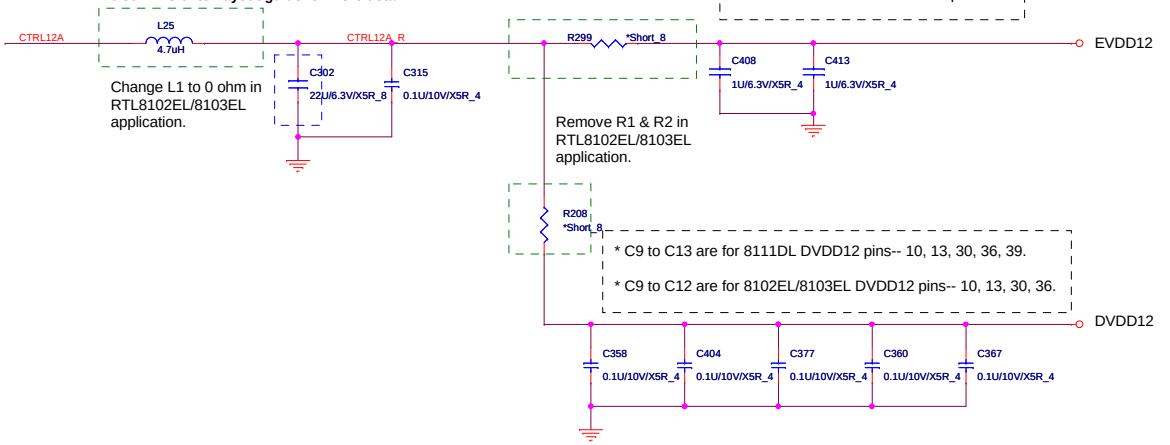
RJ45 Connector



Pin48
Trace width>60mil,
Trace length<200mil



Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.



PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN(RTL8103EL/8111DL)	1A

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Note:
To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.

+3V [3,6,8,9,12,14,15,16,17,18,19,20,21,22,24,26,27,28,30,31,32,33,34,36,38,40,41,42]
+5V [20,21,24,29,31,33,34,42]

HD Audio Bus

DIGITAL_MIC

INT Speaker

PC BEEP CONTROL

Internal MIC

EMI Reserved

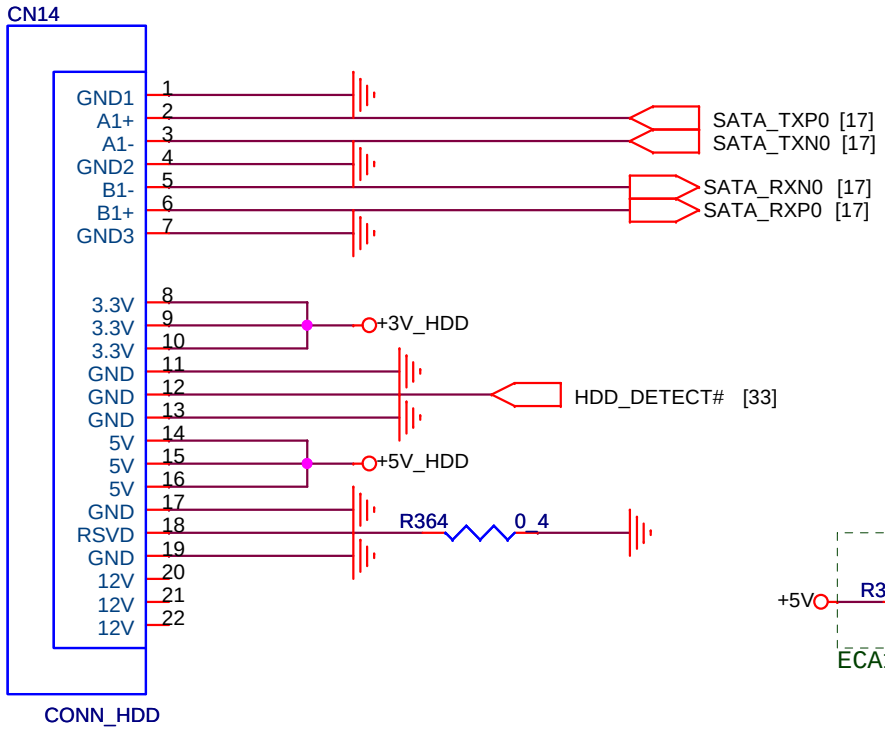
Sense For MIC/ Headphone out combo

External MIC/ Headphone out combo

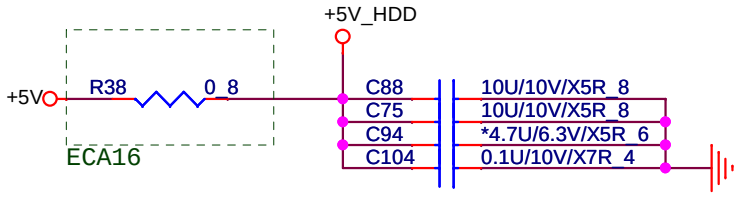
PROJECT	MK-2.0/DU-1.0 NOTE AMD NILE
Quanta Computer Inc.	
Size: Custom	Document Number: AUDIO (CX20582, SPK)
Rev: 1A	
Date: Monday, May 10, 2010	Sheet 23 of 49

HDD

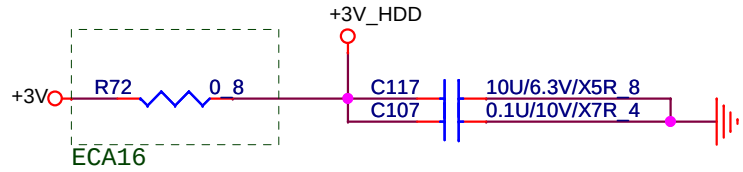
+3V [3,6,8,9,12,14,15,16,17,18,19,20,21,22,23,26,27,28,30,31,32,33,34,36,38,40,41,42]
+5V [20,21,23,29,31,33,34,42]



DC Current rating: 2 A (MAX)



DC Current rating: 3 A (MAX)



PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

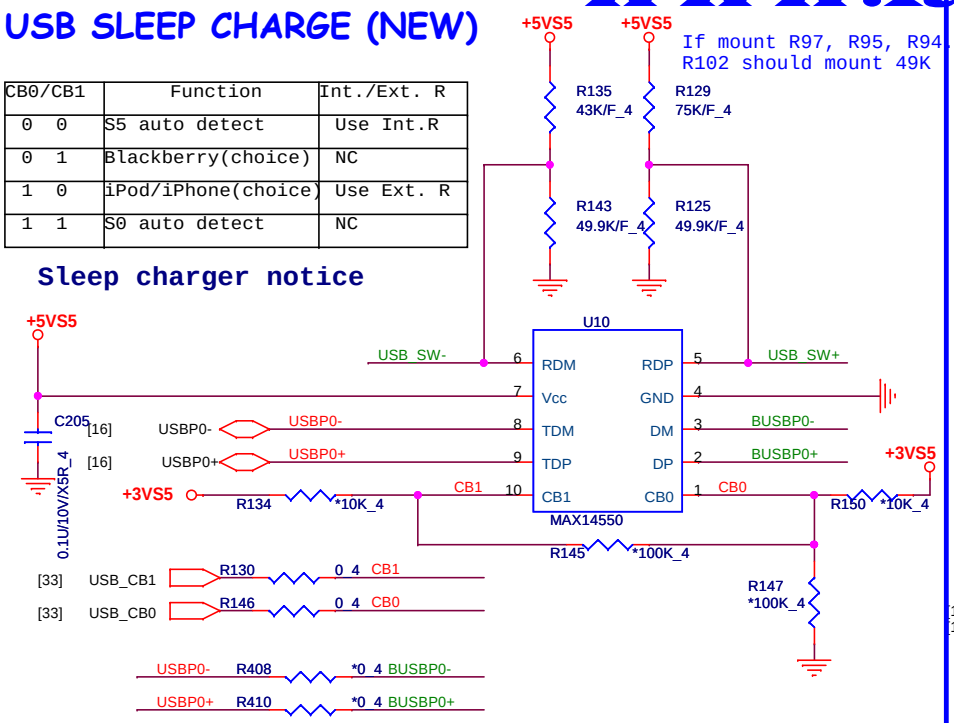
Size	Document Number	Rev
Custom	SATA	1A
Date: Thursday, May 06, 2010	Sheet 24 of 49	

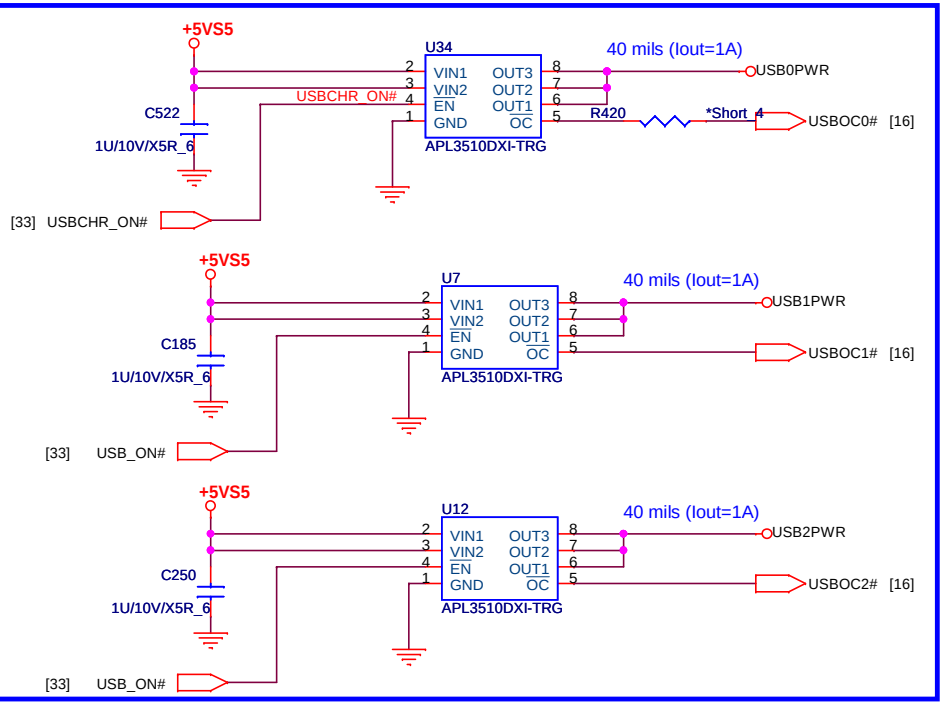
USB SLEEP CHARGE (NEW)

CB0/CB1	Function	Int./Ext. R
0 0	S5 auto detect	Use Int.R
0 1	Blackberry(choice)	NC
1 0	iPod/iPhone(choice)	Use Ext. R
1 1	S0 auto detect	NC

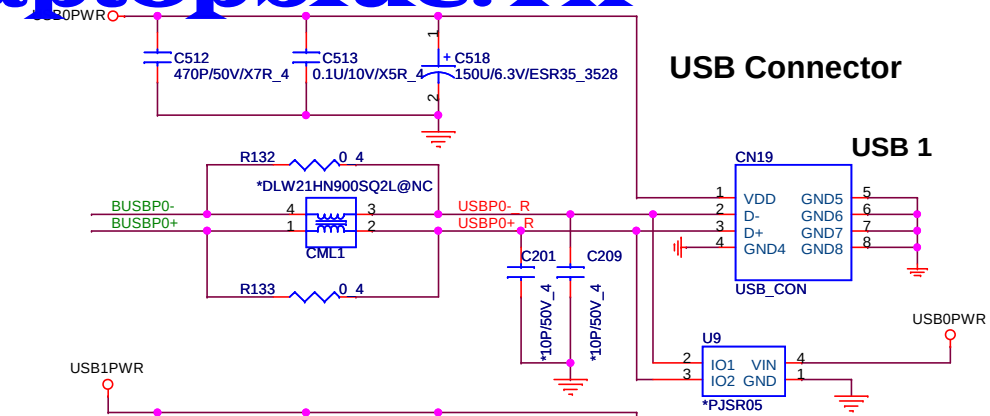
If mount R97, R95, R94
R102 should mount 49K

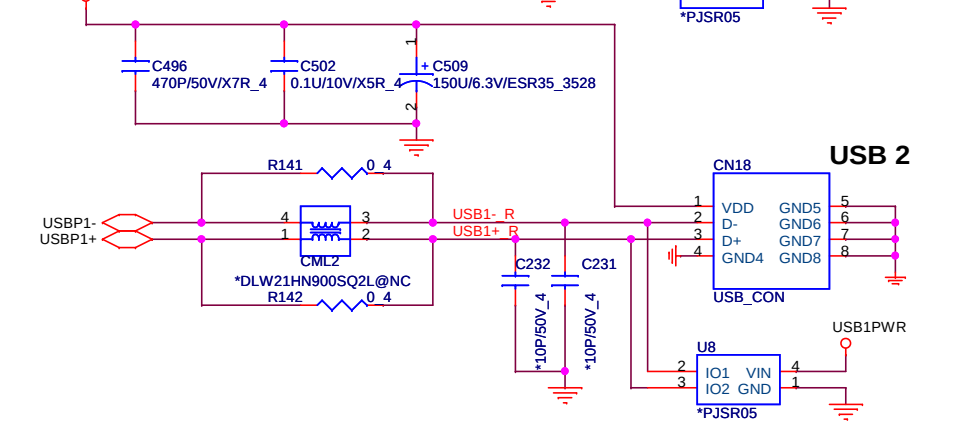
Sleep charger notice



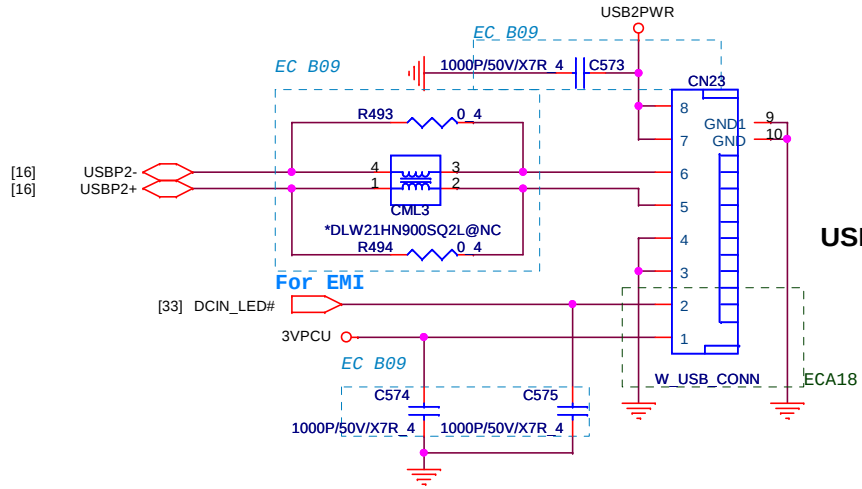


USB Connector





USB BTB connector



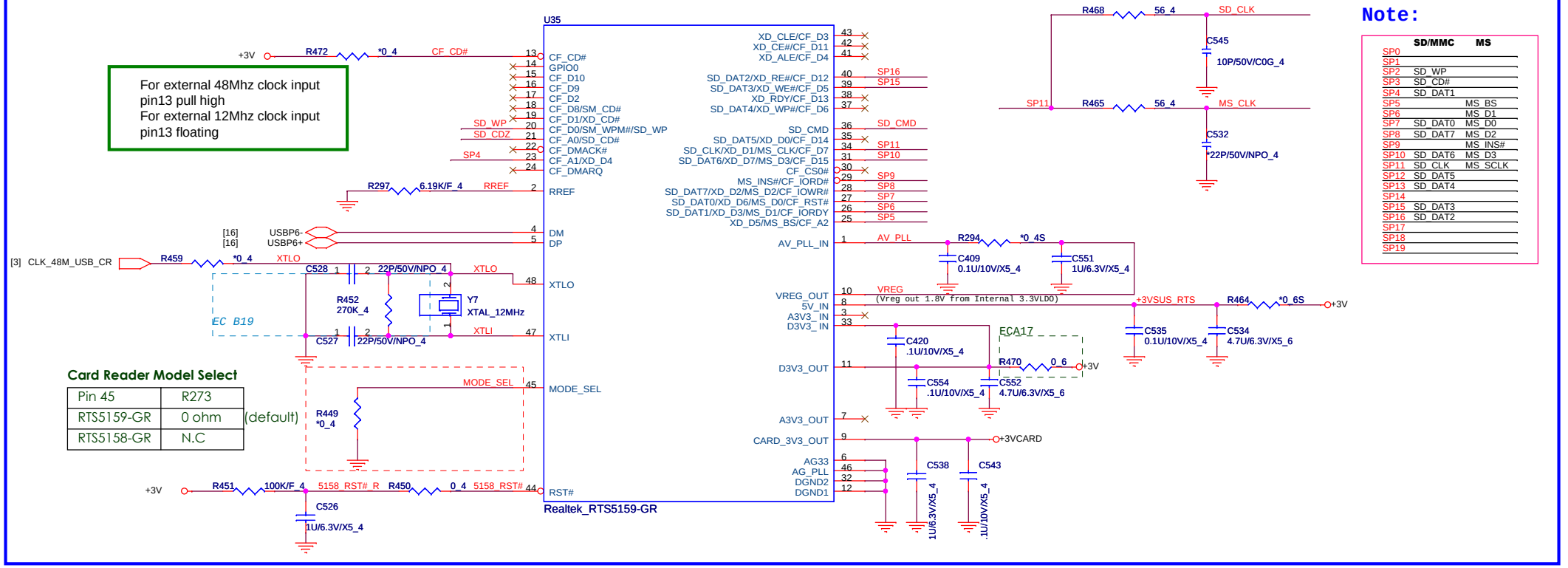
+5VS5 [42]
+3VS5 [6,15,16,17,18,19,27,30,32,42]
5VSUS [20,32,38,40,41,42]
3VPCU [15,20,21,22,32,33,35,36,38,40,42]

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

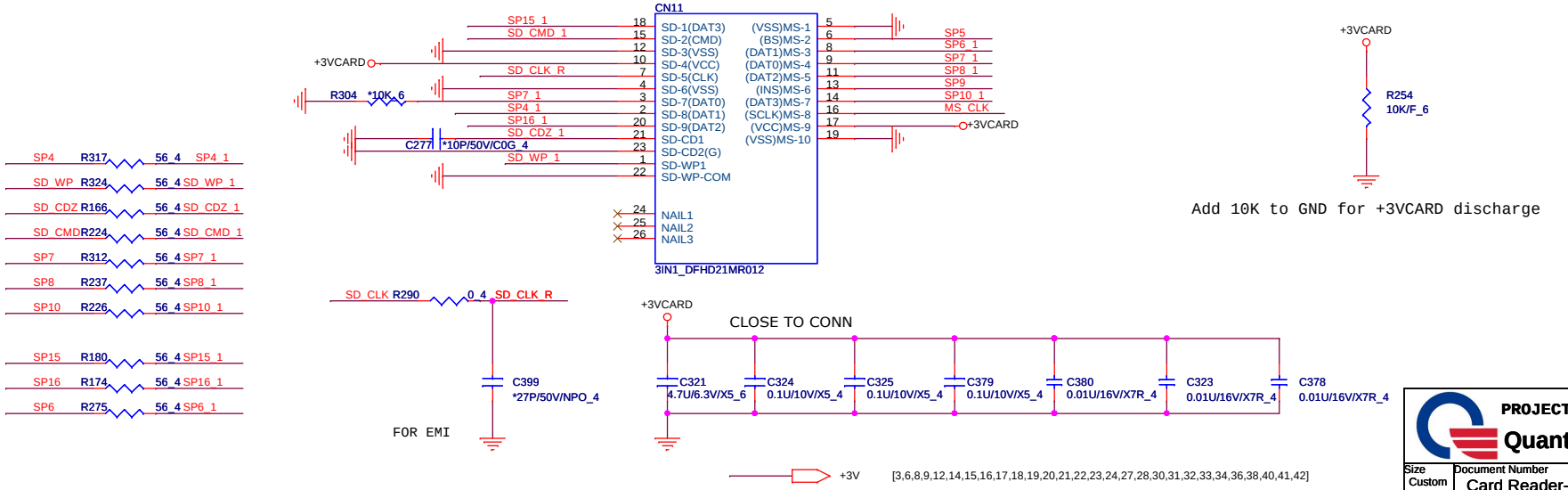
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB x 3	1A
Date: Monday, May 10, 2010	Sheet 25 of 49	

RTL5159



3 IN 1 CARD READER



PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Card Reader-RTL5159	1A

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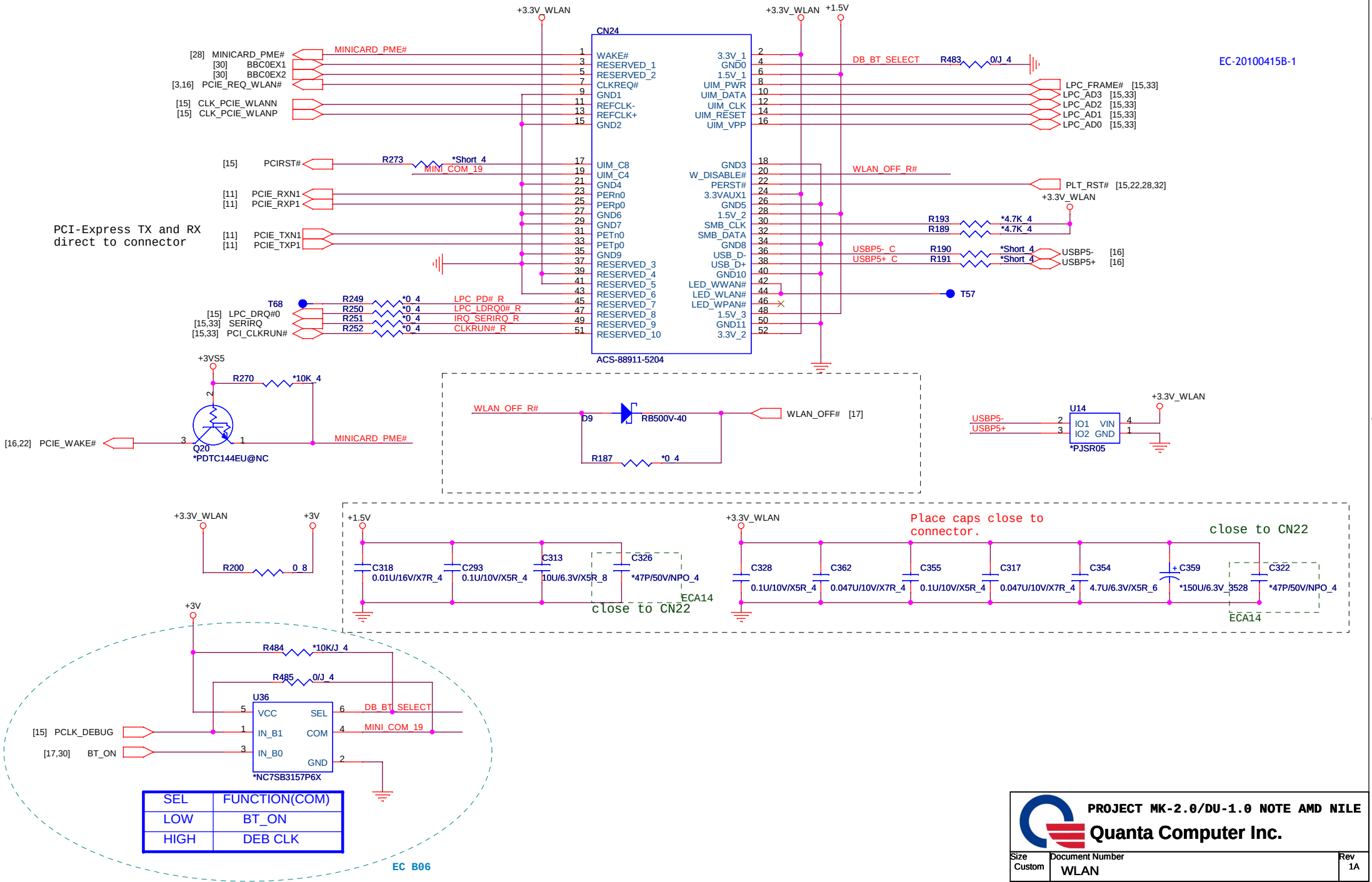
Minicard WLAN connector

+3.3V [2,3,8,9,12,14,15,16,17,18,19,20,21,22,23,24,26,28,30,31,32,33,34,36,38,40,41,42]
+1.5V [6,14,16,28,42]
+3VS5 [6,15,16,17,18,19,25,30,32,42]



SEL	FUNCTION(COM)
LOW	BT_ON
HIGH	DEB CLK

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	WLAN	1A

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SIM Card CONN

+3V [3,6,8,9,12,14,15,16,17,18,19,20,21,22,23,24,26,29,30,31,32,33,34,36,38,41,42]
+1.5V [6,14,16,27,42]

CN20
UIM_PWR 1 VCC
UIM_RESET 2 RST
UIM_CLK 3 CLK
GND 4
VPP 5 UIM_VPP
DATA 6 UIM_DATA
2WM610C1C-DS-7F

Layout Note:
UIM_RESET,UIM_CLK,UIM_DATA routting as short as possible

U13
UIM_RESET 1
UIM_CLK 2
3
1 6
2 5
3 4
CM1293A-04SO
6 UIM_VPP
5 UIM_PWR
4 UIM_DATA
C239 33P/50V/NPO_4
C238 33P/50V/NPO_4
C287 33P/50V/NPO_4
C290 1U/10V/X5R_6
C286 33P/50V/NPO_4

MiniCard WWAN connector

CN22
[27] MINICARD_PME# 1 WAKE#
3 RESERVED_1
5 RESERVED_2
[3,16] PCIE_REQ_WWAN# 7 CLKREQ#
9 GND1
[15] CLK_PCIE_WANN 11 REFCLK-
[15] CLK_PCIE_WANP 13 REFCLK+
15 GND2
17 UIM_C8
19 UIM_C4
21 GND4
[11] PCIE_RXN2 23 PERn0
[11] PCIE_RXP2 25 PERp0
27 GND6
29 GND7
[11] PCIE_TXN2 31 PETn0
[11] PCIE_TXP2 33 PETp0
35 GND9
37 RESERVED_3
39 RESERVED_4
41 RESERVED_5
43 RESERVED_6
45 RESERVED_7
47 RESERVED_8
49 RESERVED_9
51 RESERVED_10
2 3.3V_1
4 GND0
6 1.5V_1
8 UIM_PWR
10 UIM_DATA
12 UIM_CLK
14 UIM_RESET
16 UIM_VPP
18 GND3
20 W_DISABLE#
22 PERST#
24 3.3VAUX1
26 GND5
28 1.5V_2
30 SMB_CLK
32 SMB_DATA
34 GND8
36 USB_D-
38 USB_D+
40 GND10
42 LED_WWAN#
44 LED_WLAN#
46 LED_WPAN#
48 1.5V_3
50 GND11
52 3.3V_2
ACS-88911-5204

PCI-Express TX and RX
direct to connector

UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP

R176 *Short_4 WWAN_OFF# [17]
PLT_RST# [15,22,27,32]
R159 *4.7K_4
R157 *4.7K_4
USBP4-_C R151 *Short_4 USBP4- [16]
USBP4+_C R148 *Short_4 USBP4+ [16]
T39

U11
USBP4-_C 2 IO1 VIN 4
USBP4+_C 3 IO2 GND 1
*PJSR05

Place caps close to connector.

C221 0.047U/10V/X7R_4
C248 33P/50V/NPO_4
C254 *47P/50V/NPO_4
ECA14
close to CN21

C206 33P/50V/NPO_4
C233 0.047U/10V/X7R_4
C202 33P/50V/NPO_4
C241 0.047U/10V/X7R_4
C291 *150U/6.3V_3528
C257 *47P/50V/NPO_4
ECA14
close to CN21

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	WWAN	1A

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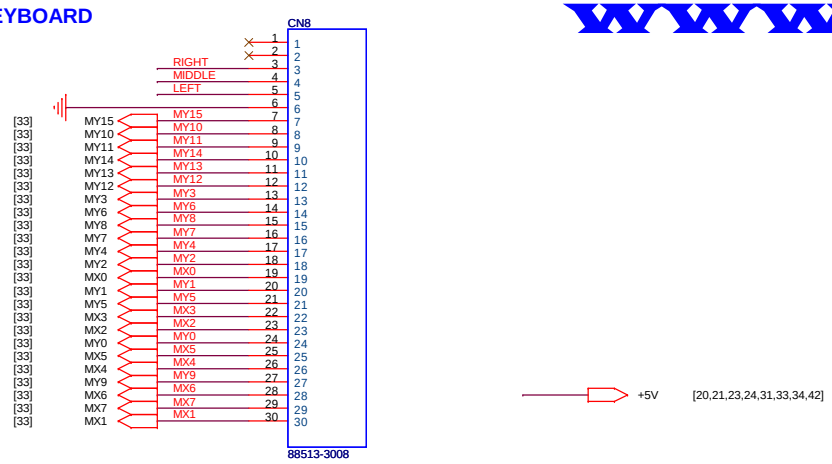
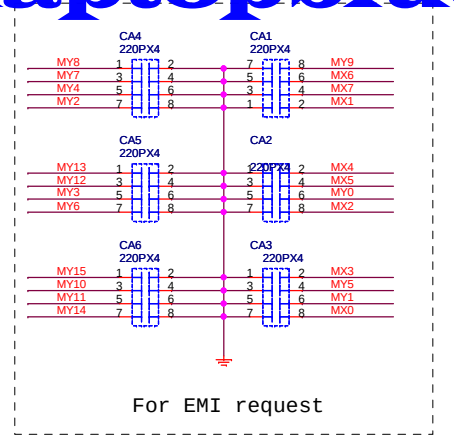
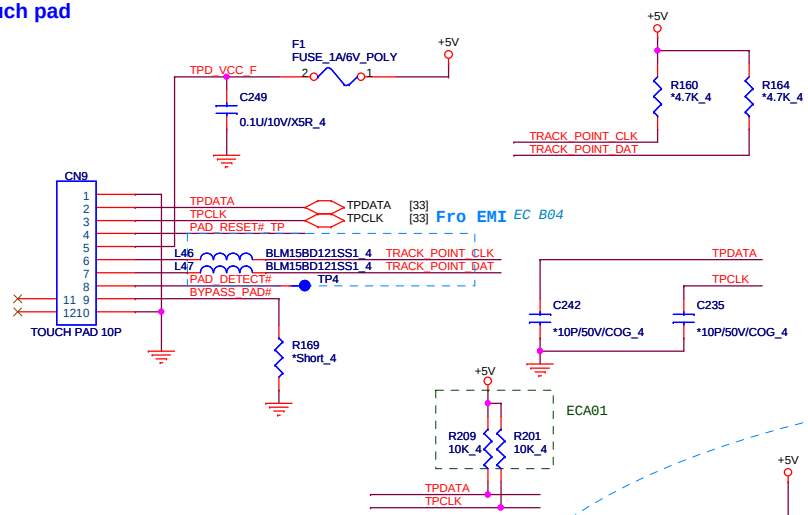
KEYBOARD



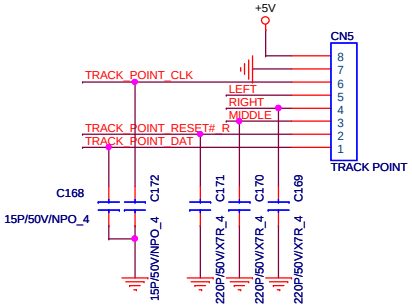
+5V [20,21,23,24,31,33,34,42]

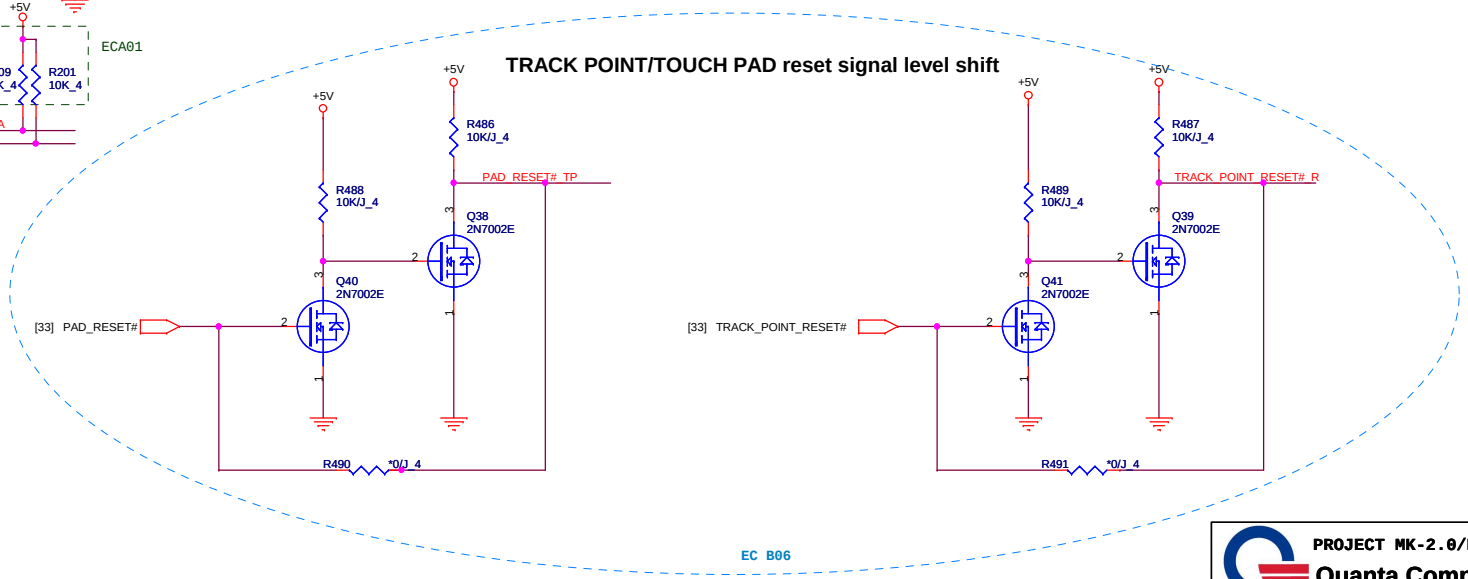


Touch pad



TRACK POINT





PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

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Custom	KB/TP	1A

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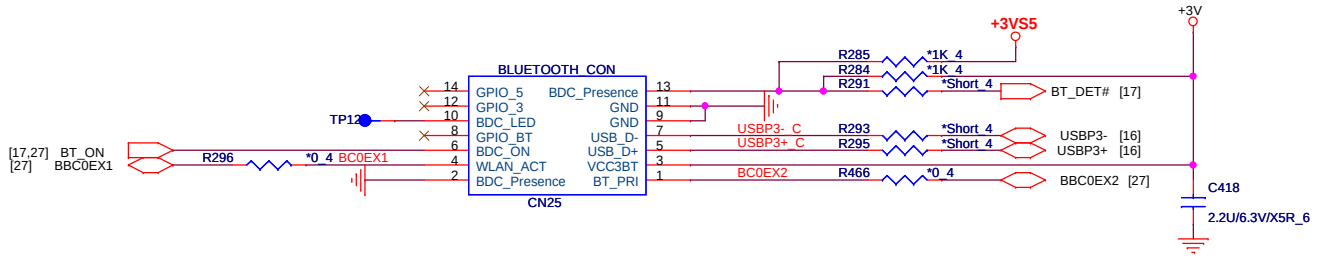
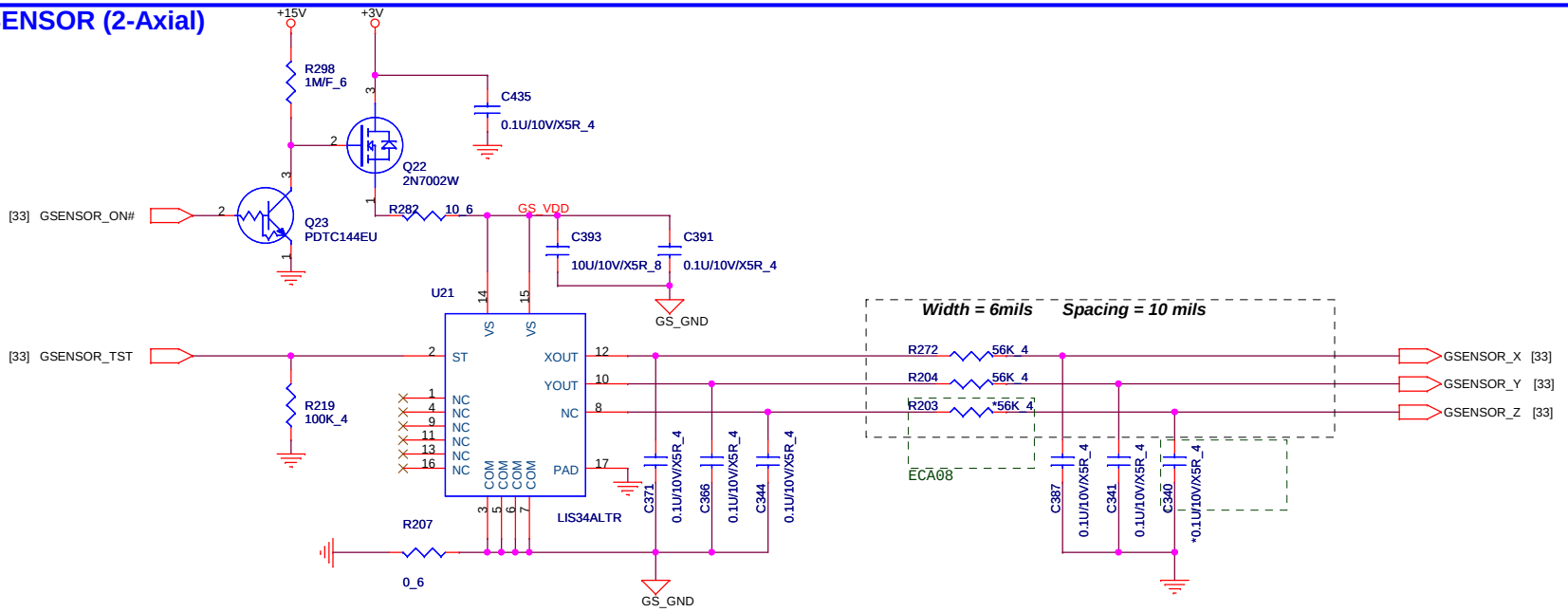
BLUETOOTH



G-SENSOR (2-Axial)



+3V	[3,6,8,9,12,14,15,16,17,18,19,20,21,22,23,24,26,27,28,31,32,33,34,36,38,40,41,42]
+15V	[20,36,42]
+3VS5	[6,15,16,17,18,19,25,27,32,42]

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/G-SENSOR	1A

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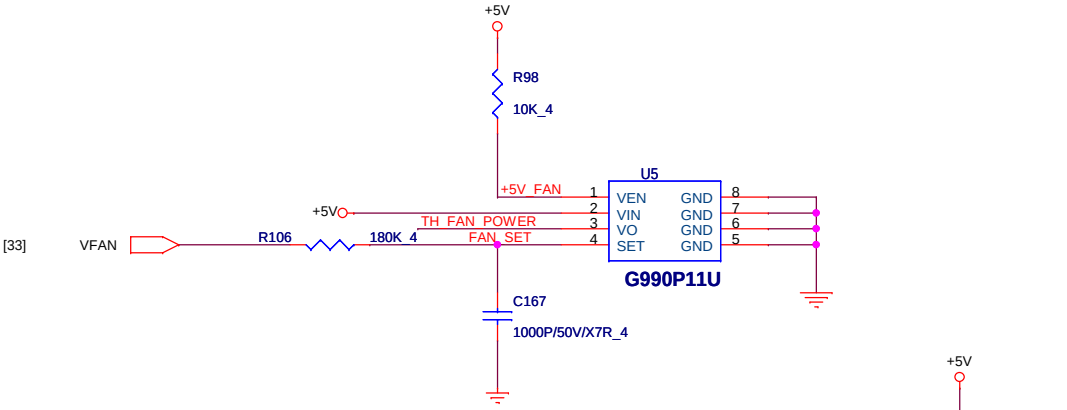
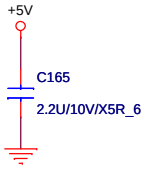
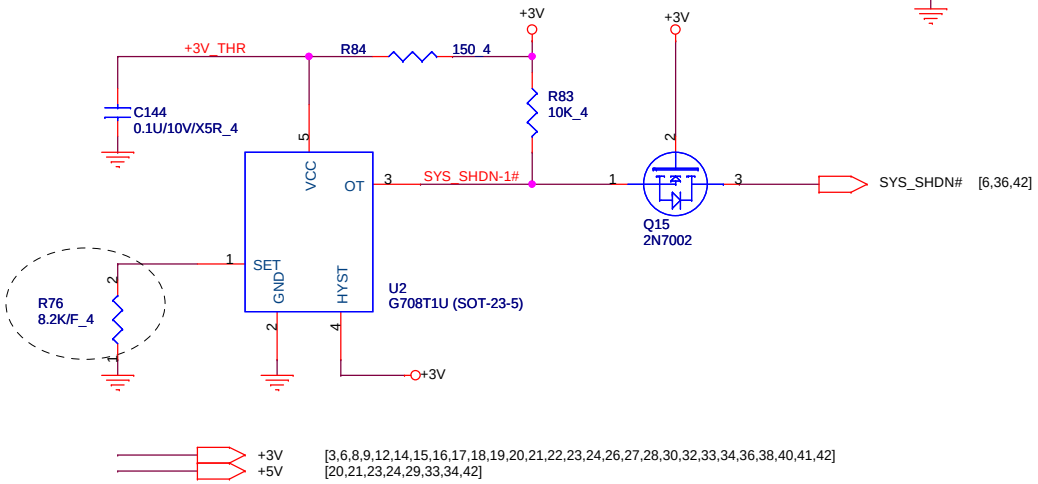
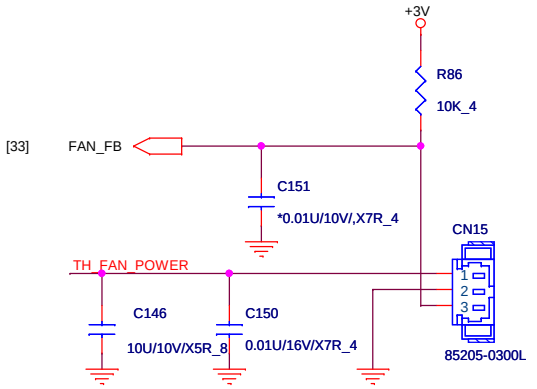
FANPWR = 1.6*VSET

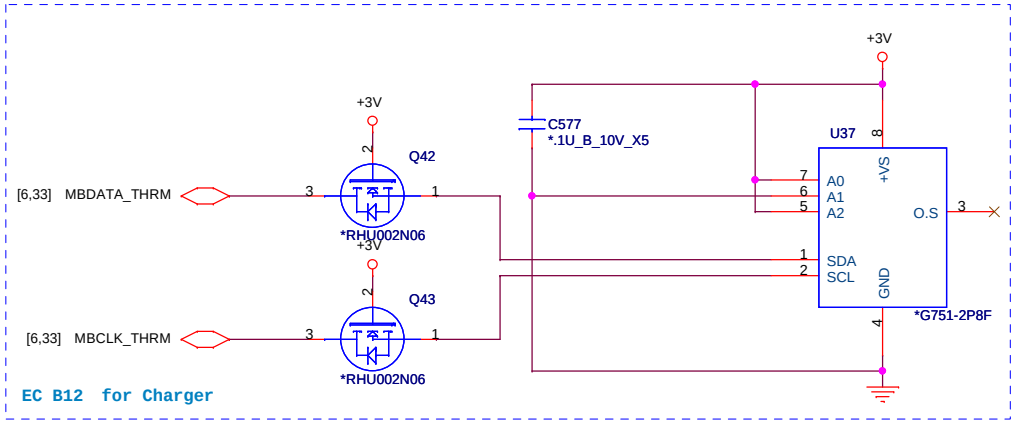






+3V [3,6,8,9,12,14,15,16,17,18,19,20,21,22,23,24,26,27,28,30,32,33,34,36,38,40,41,42]
+5V [20,21,23,24,29,33,34,42]





ADDRESS: 9AH

ADDRESS

1	0	0	1	A2	A1	A0	0

MSB LSB

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

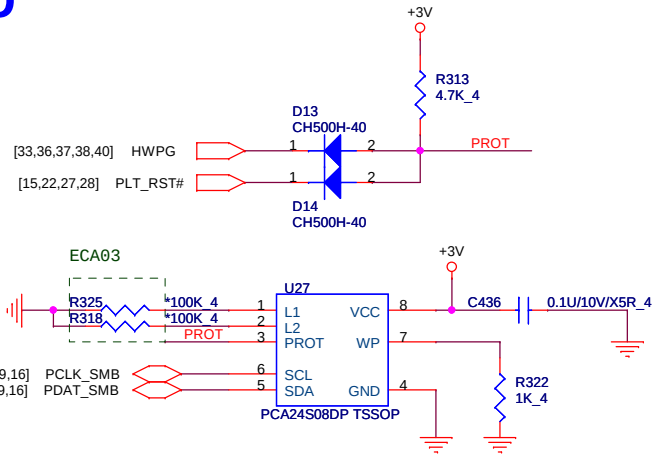
Quanta Computer Inc.

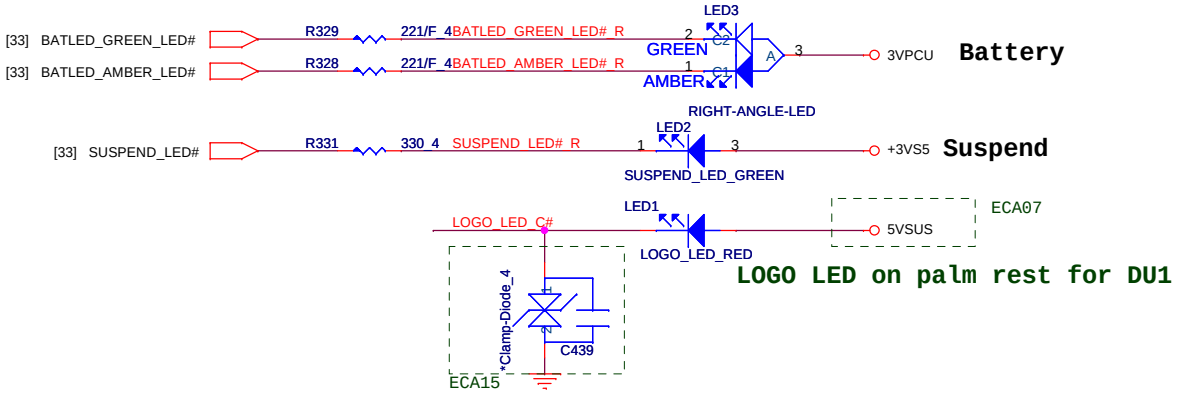
Size	Document Number	Rev
Custom	FAN/Thermal	1A

Date: Thursday, May 06, 2010 Sheet 31 of 49

3V [3,6,8,11,14,15,16,17,18,19,20,21,22,23,24,26,27,28,30,31,33,34,36,38,40,41,42]
3VPCU [15,20,21,22,25,33,35,36,38,40,42]
+3VS5 [6,15,16,17,18,19,25,27,30,42]
5VSUS [20,38,40,41,42]

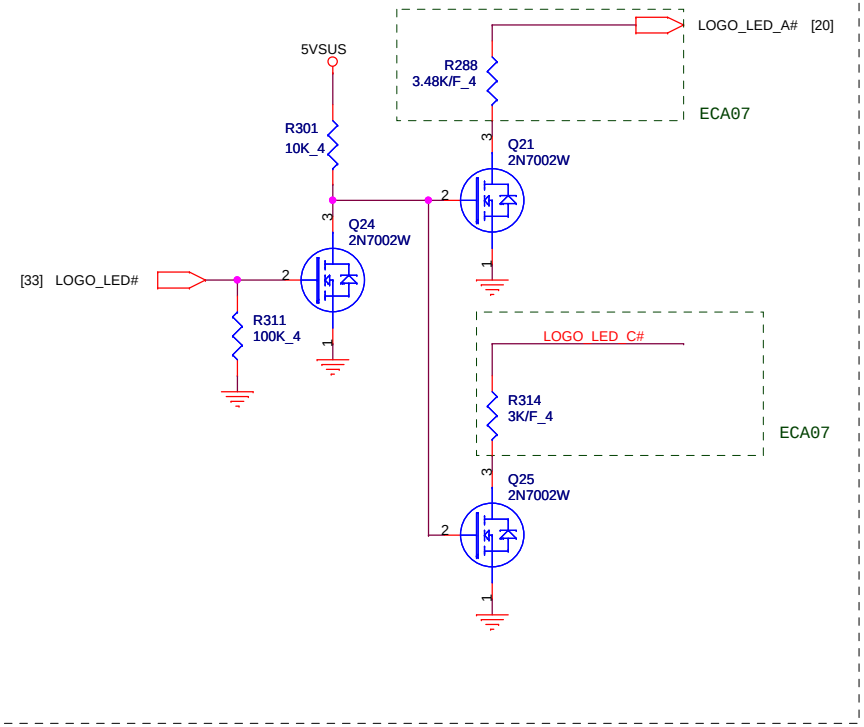
RFID



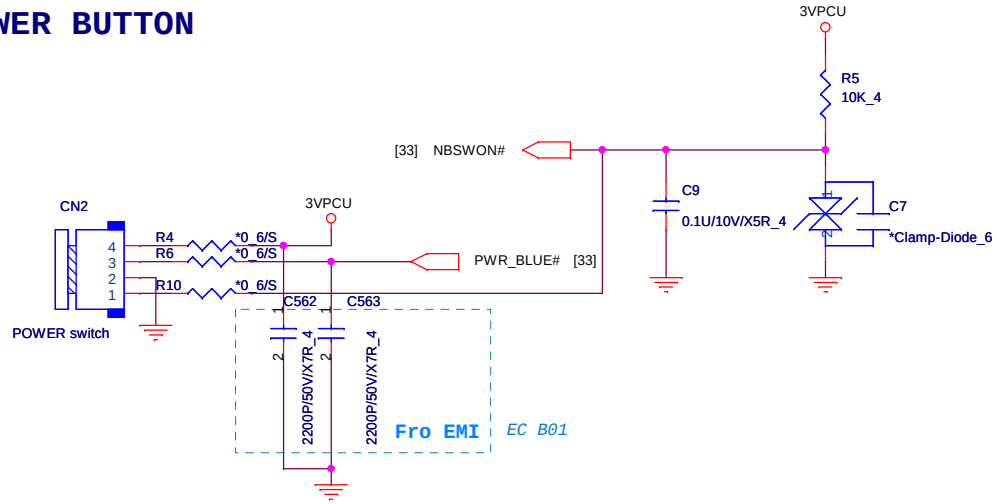


LED Driver

LOGO LED on panel cover for DU1



POWER BUTTON



PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SW/LED/RFID_EEPROM	1A
Date: Thursday, May 06, 2010	Sheet 32 of 49	

IT8502E

(For PLL Power)

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function
Enable
Disable

R609	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

16Mbit (2M Byte), SPI

Winbond	AKE32ZP0N00
SST	AKE28FP0K07
MX	AKE37FP0Z13

To avoid glitch during bootup

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBC IT8502E	1A

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Hole for CPU support

HOLE2 *H-T146B197D146PB

HOLE3 *H-T146B197D146PB

MiniCard WLAN

HOLE15 h-c197d118p2

MiniCard WLAN

HOLE14 h-c197d35p2

HOLE13 h-c197d102p2

BLUETOOTH

HOLE16 h-c197d59p2

CRT

Spad1 *Spad1

Keyboard

HOLE6 *o-mk-note-1

Boundary Hole

HOLE1 *H-C236D91P2

HOLE4 *H-C259D209P2

HOLE5 *H-C47D47N

HOLE7 *h-c197d91p2

HOLE8 *H-O102X91D102X91N

HOLE9 *hg-c276d91p2

Boundary Hole

HOLE10 *h-tc236bc276d91p2

HOLE11 *h-tc236bc197d91p2

HOLE12 *h-c256d91p2

EMI

+1.5VSUS

C91 C86 C164 C494 C309 C425 C361

2200P/50V/X7R_4

+3V

C457 C20 C128 C412 C432 C200 C400 C163

2200P/50V/X7R_4

+5V

C3 C204 C227 C437 C416 C493

2200P/50V/X7R_4

Fro EMI

+2.5V

C579 C580

2200P/50V/X7R_4

EC B03

Fro EMI

5VPCU

C572 C566 C567

1000P/50V/X7R_4 1U/6.3V/X5R_4 1U/6.3V/X5R_4

EC B03

+3V [3,6,8,9,12,14,15,16,17,18,19,20,21,22,23,24,26,27,28,30,31,32,33,36,38,40,41,42]

+5V [20,21,23,24,29,31,33,42]

+1.5VSUS [5,6,7,8,9,12,37,40,41,42]

5VPCU [20,35,36,37,38,39,40,42]

PROJECT MK-2.0/DU-1.0 NOTE AMD NILE

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Screw Hole/EMI	1A

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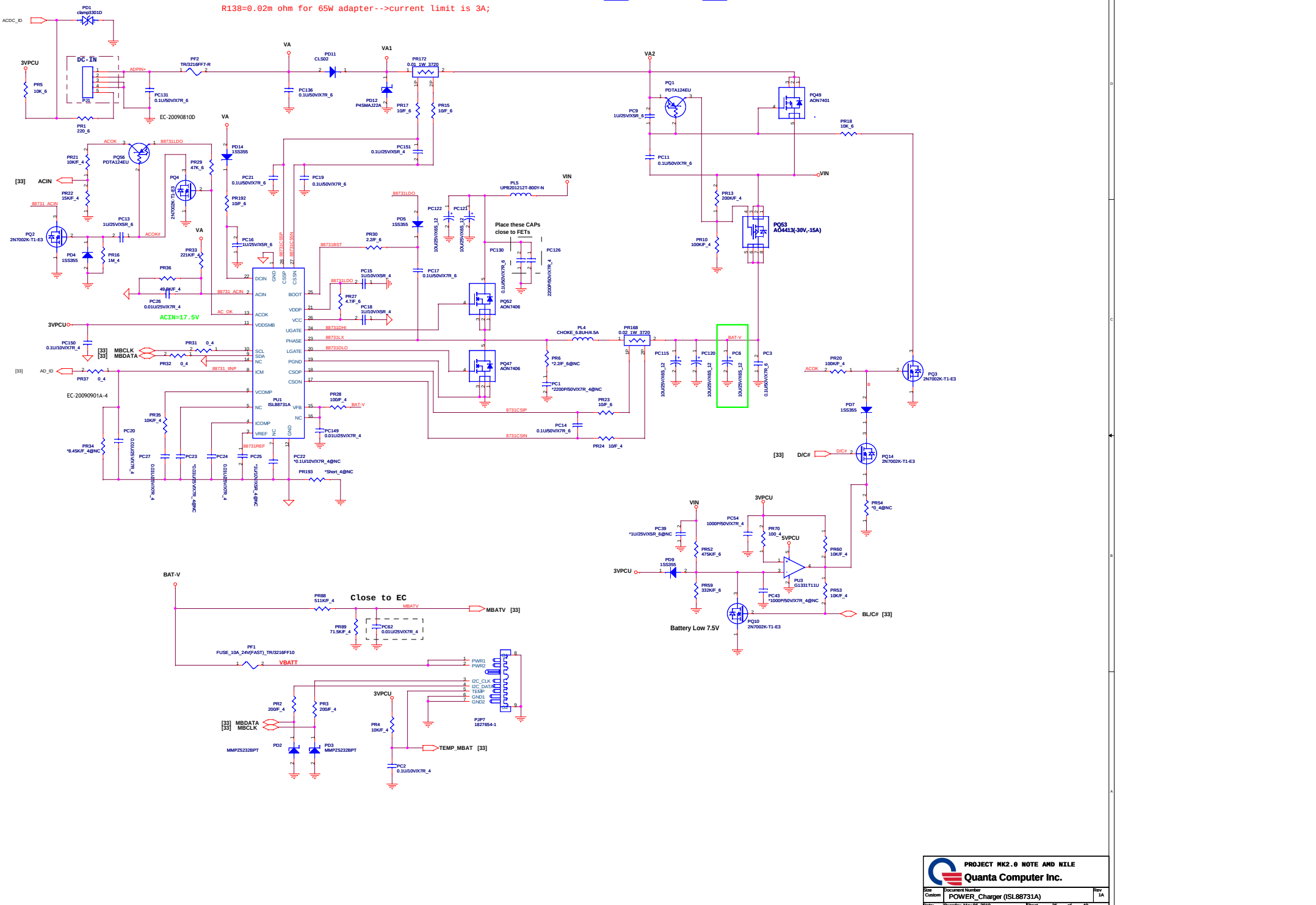
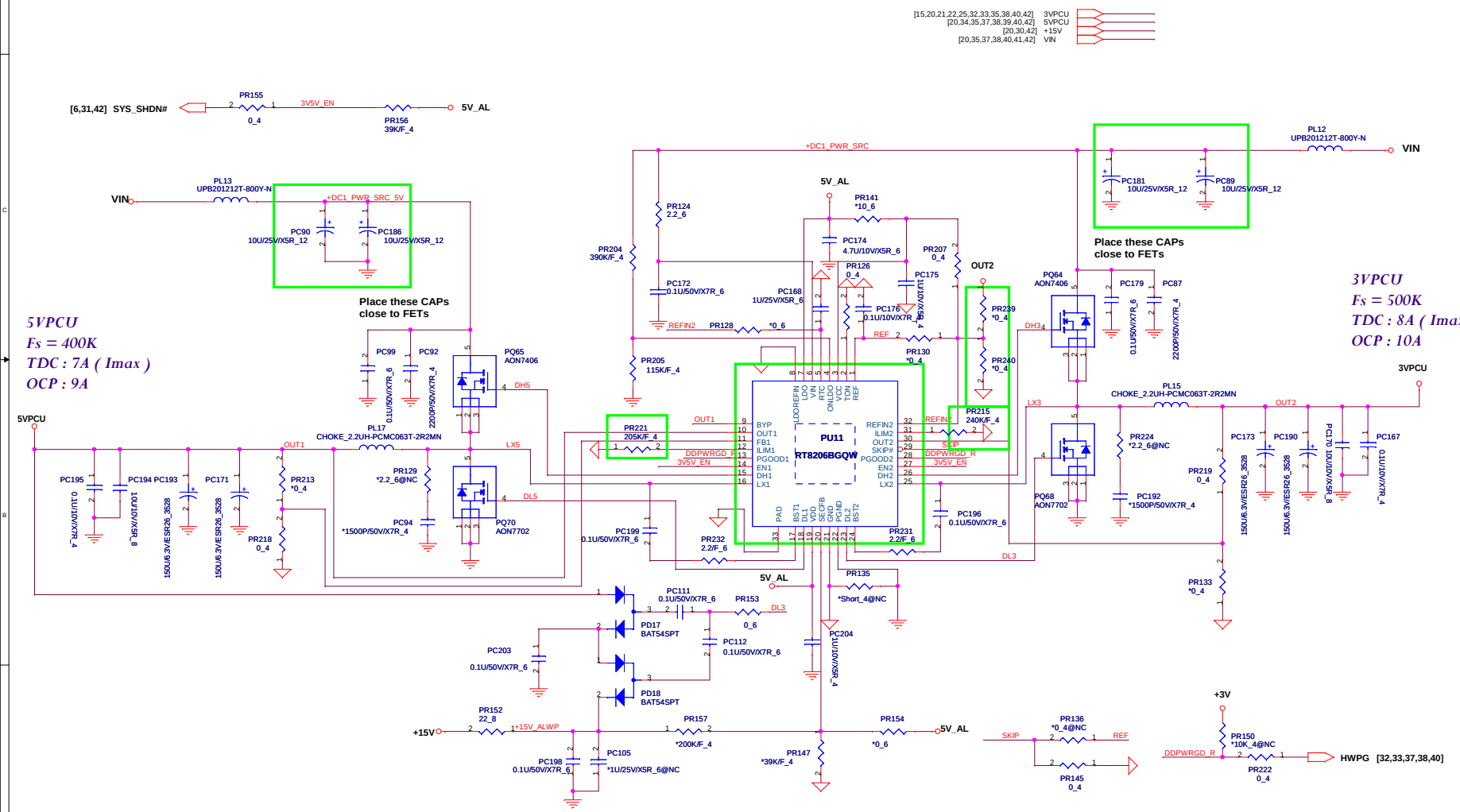
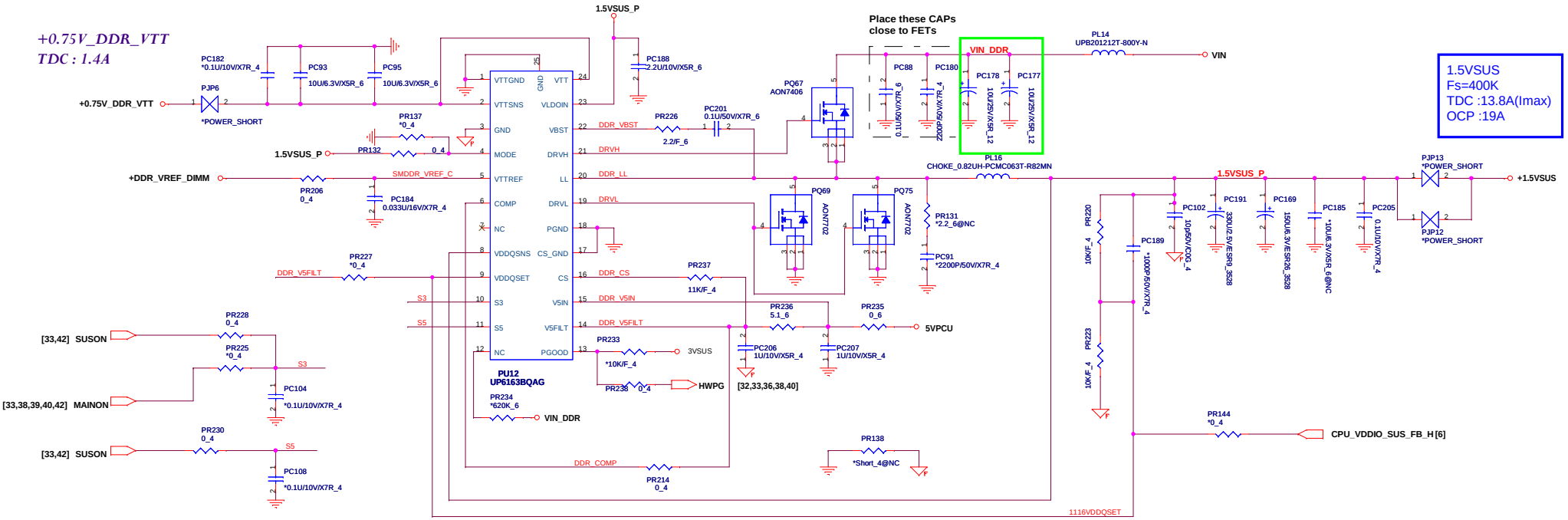
R138=0.02m ohm for 65W adapter-->current limit is 3A;

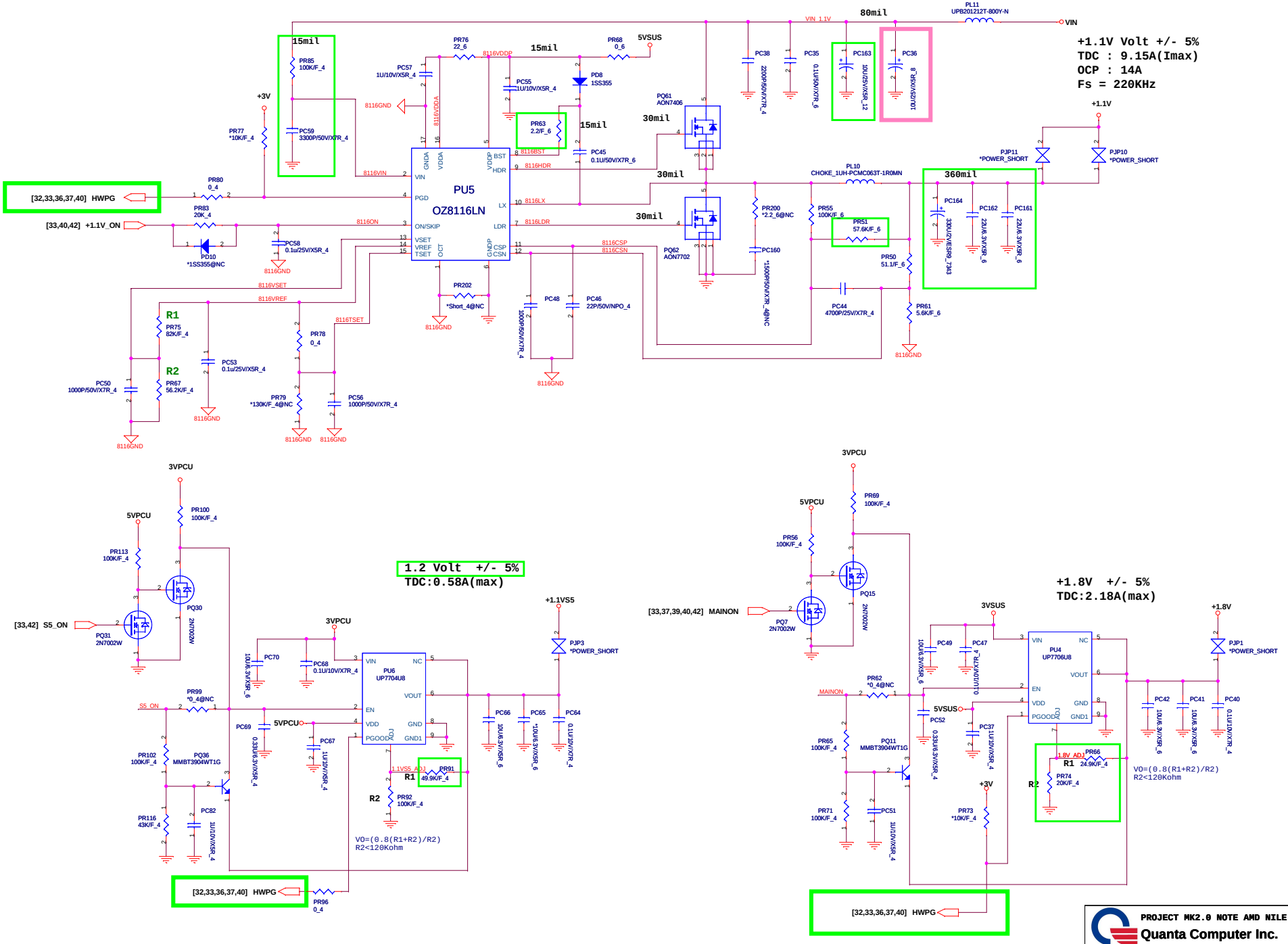


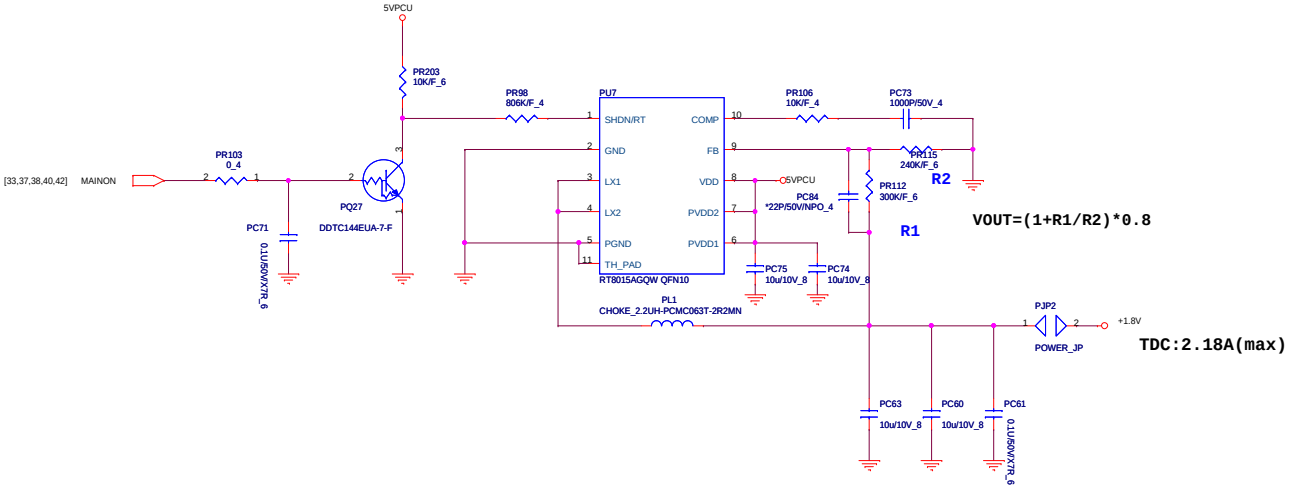


PROJECT MK2.0 NOTE AMD NILE			
Quanta Computer Inc.			
Size: Custom	Document Number: 3V/5V (RT8206BGQW)		Rev: 1A
Date: Thursday, May 06, 2010		Sheet 36 of 49	



PROJECT MK2.0 NOTE AMD NILE			
Quanta Computer Inc.			
Size: Custom	Document Number: DDR3(UP6163AQAG)		Rev: 1A
Date: Thursday, May 06, 2010	Sheet 37 of 49		



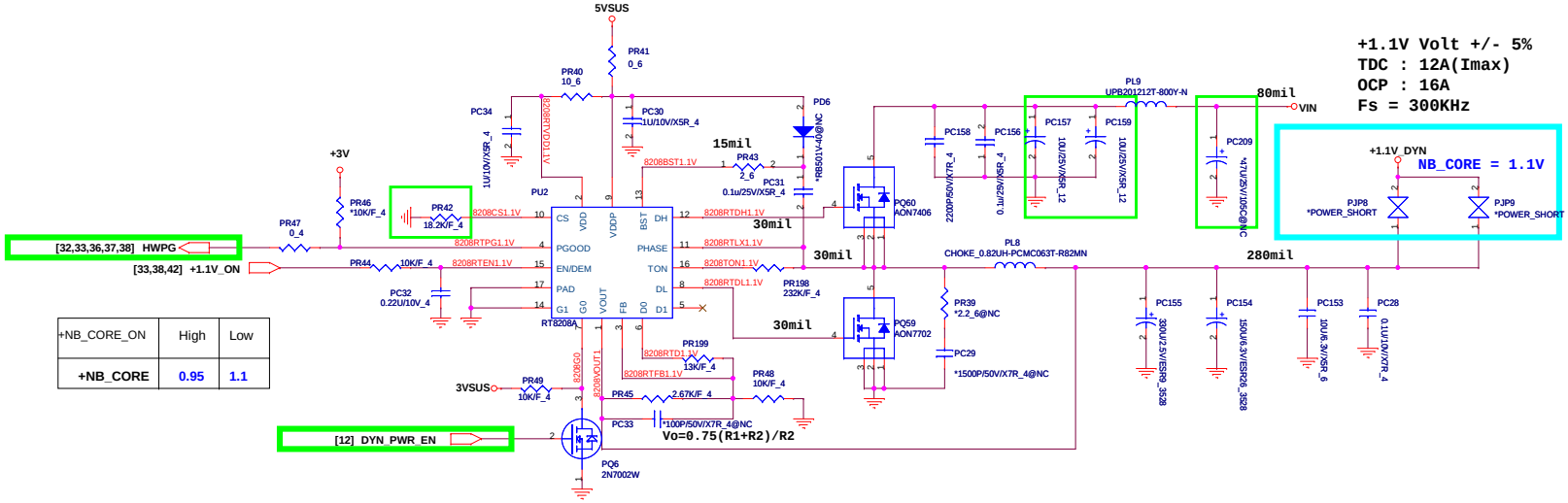


PROJECT MK2.0 NOTE AMD NILE

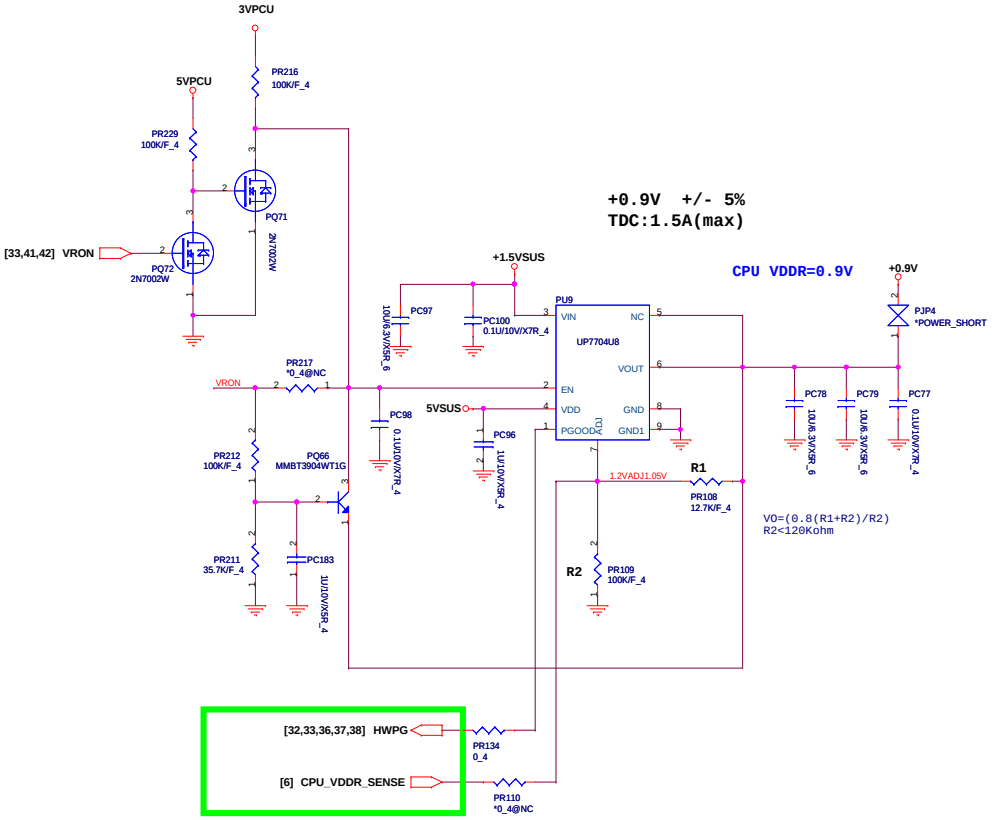
Quanta Computer Inc.

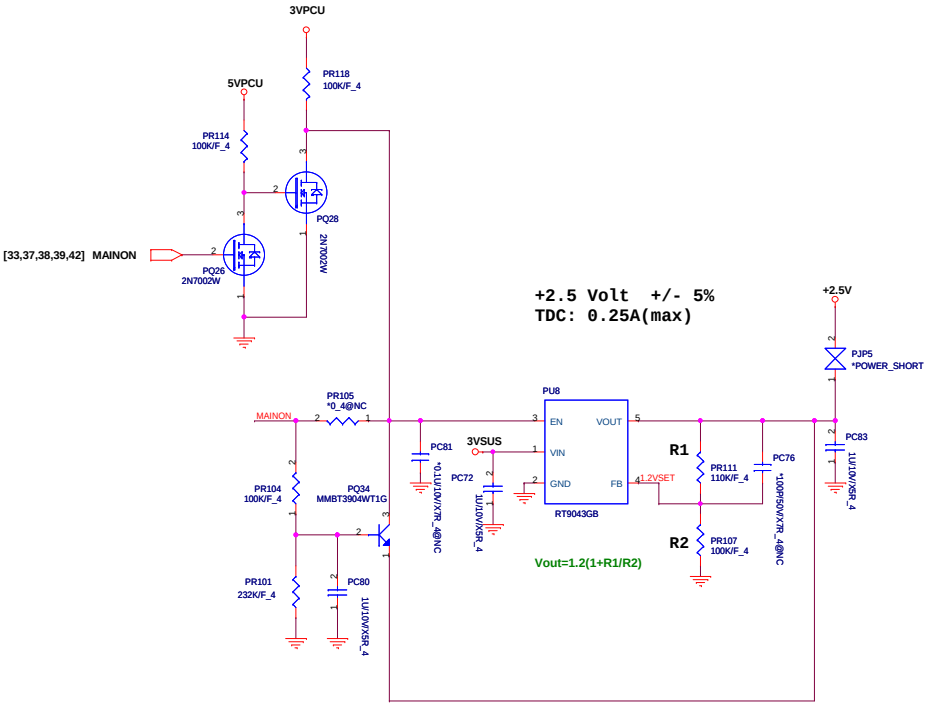
Size	Document Number	Rev
C	+1.8V RT8015A	1A

Date: Friday, May 07, 2010 Sheet 39 of 49



+NB_CORE_ON	High	Low
+NB_CORE	0.95	1.1





PROJECT MK2.0 NOTE AMD NILE
Quanta Computer Inc.

Size	Document Number	Rev
C	+NB_CORE/+0.9V/+2.5V 8208	1A

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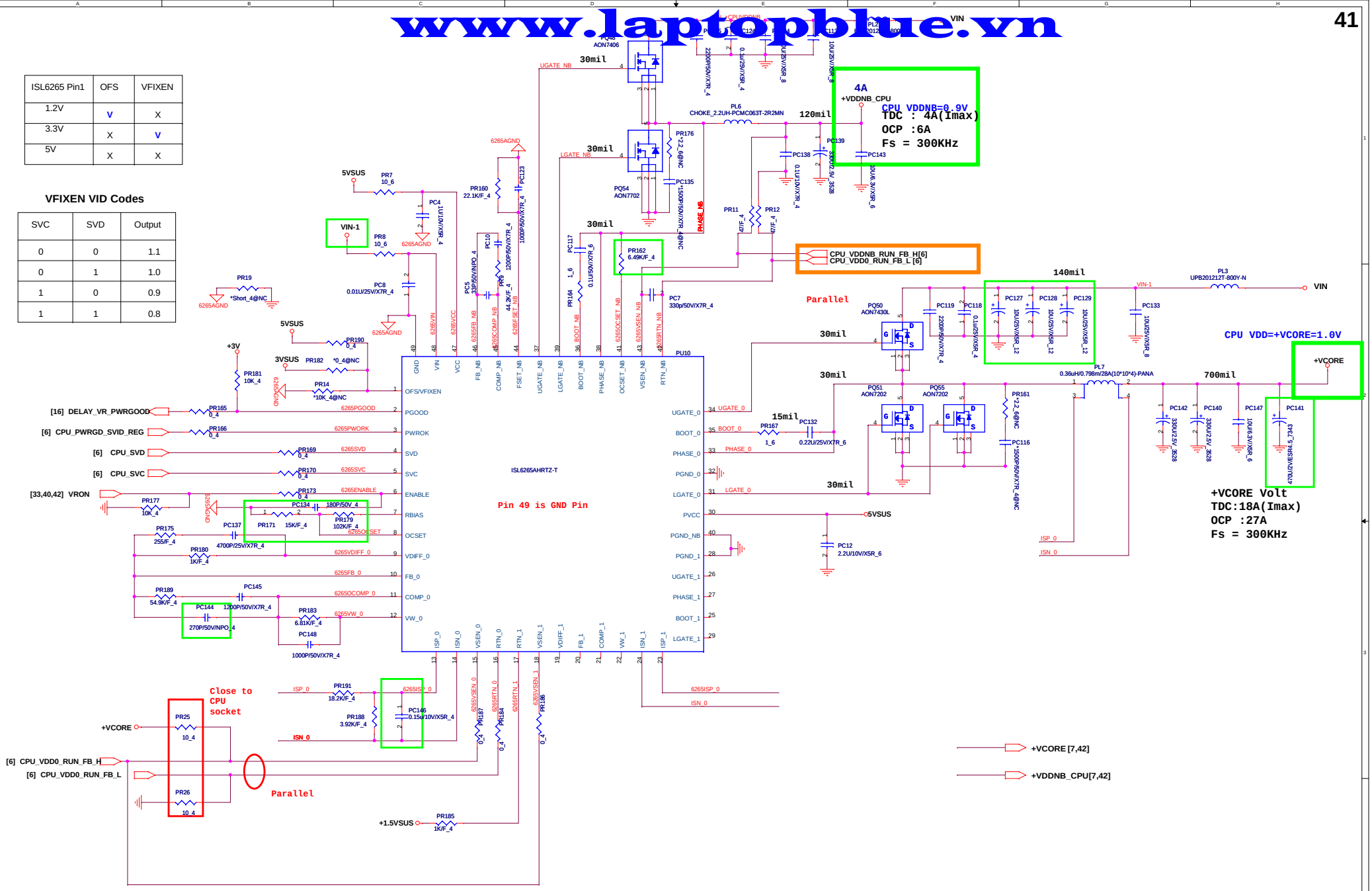
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



PROJECT MK2.0 NOTE AMD NILE
Quanta Computer Inc.

Size	Document Number	Rev
C	+CPU_CORE (ISL6265C)	1A

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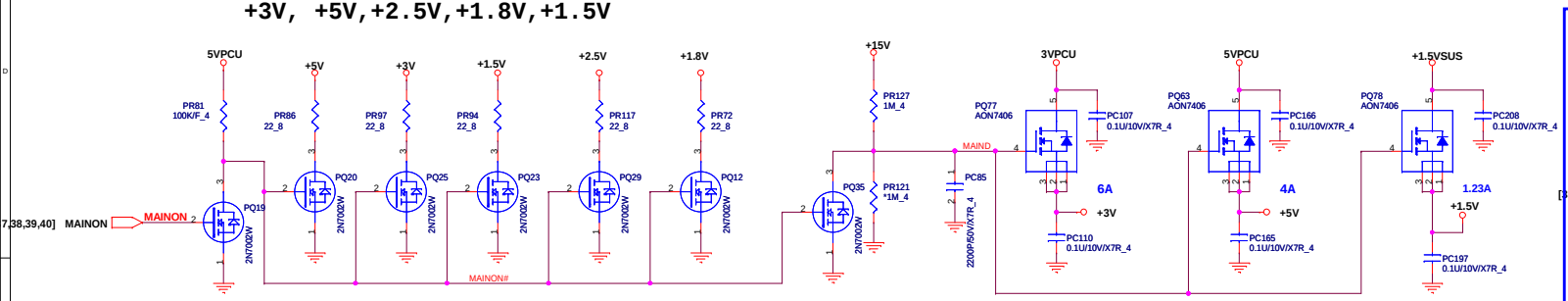
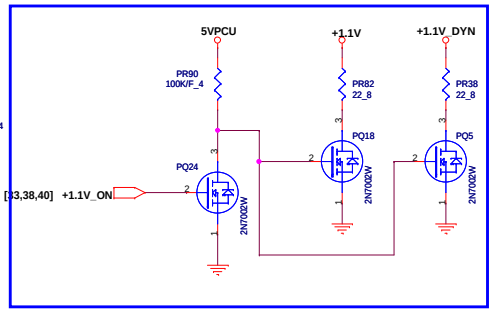
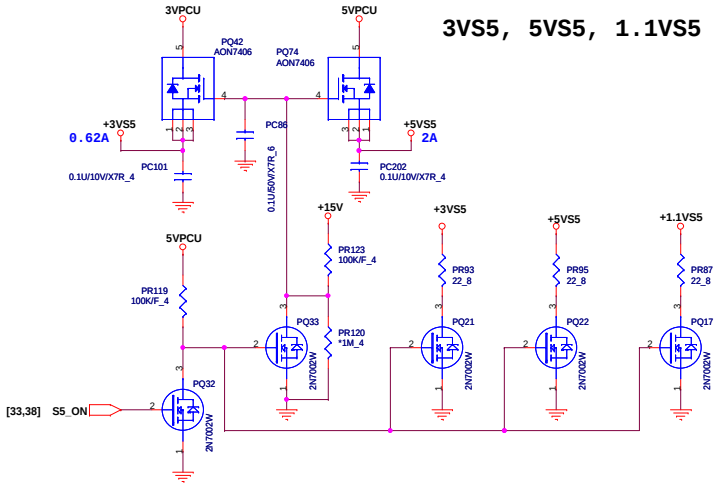
DISCHARGE

+3V, +5V,+2.5V,+1.8V,+1.5V

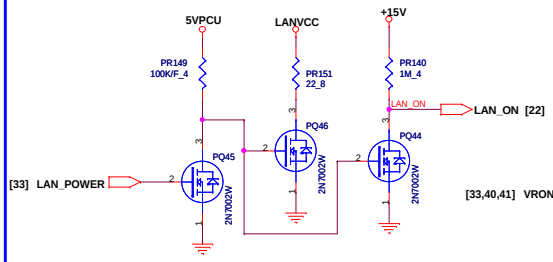




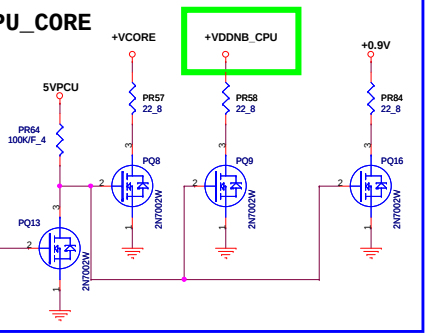
3VS5, 5VS5, 1.1VS5



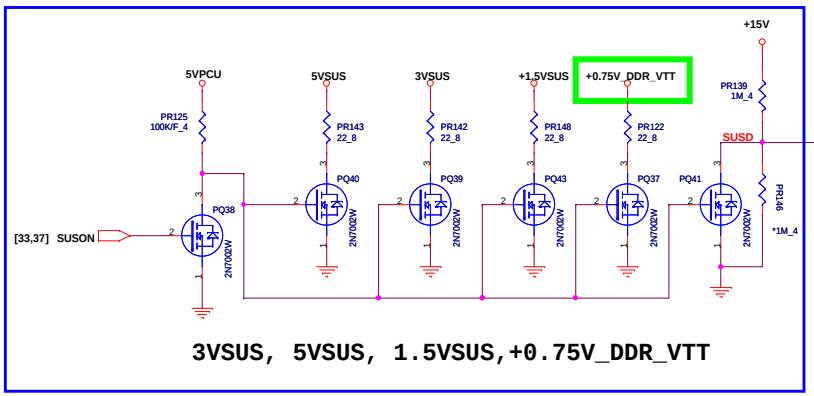
LANVCC

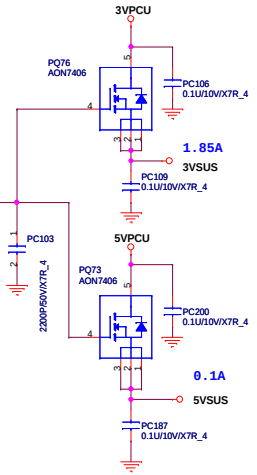


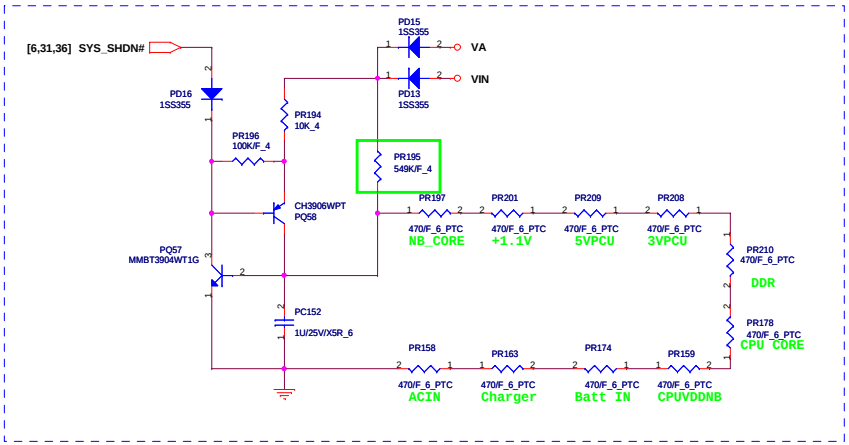
CPU_CORE



3VSUS, 5VSUS, 1.5VSUS,+0.75V_DDR_VTT







PROJECT MK2.0 NOTE AMD NILE
Quanta Computer Inc.

Size	Document Number	Rev
C	Discharge	1A

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