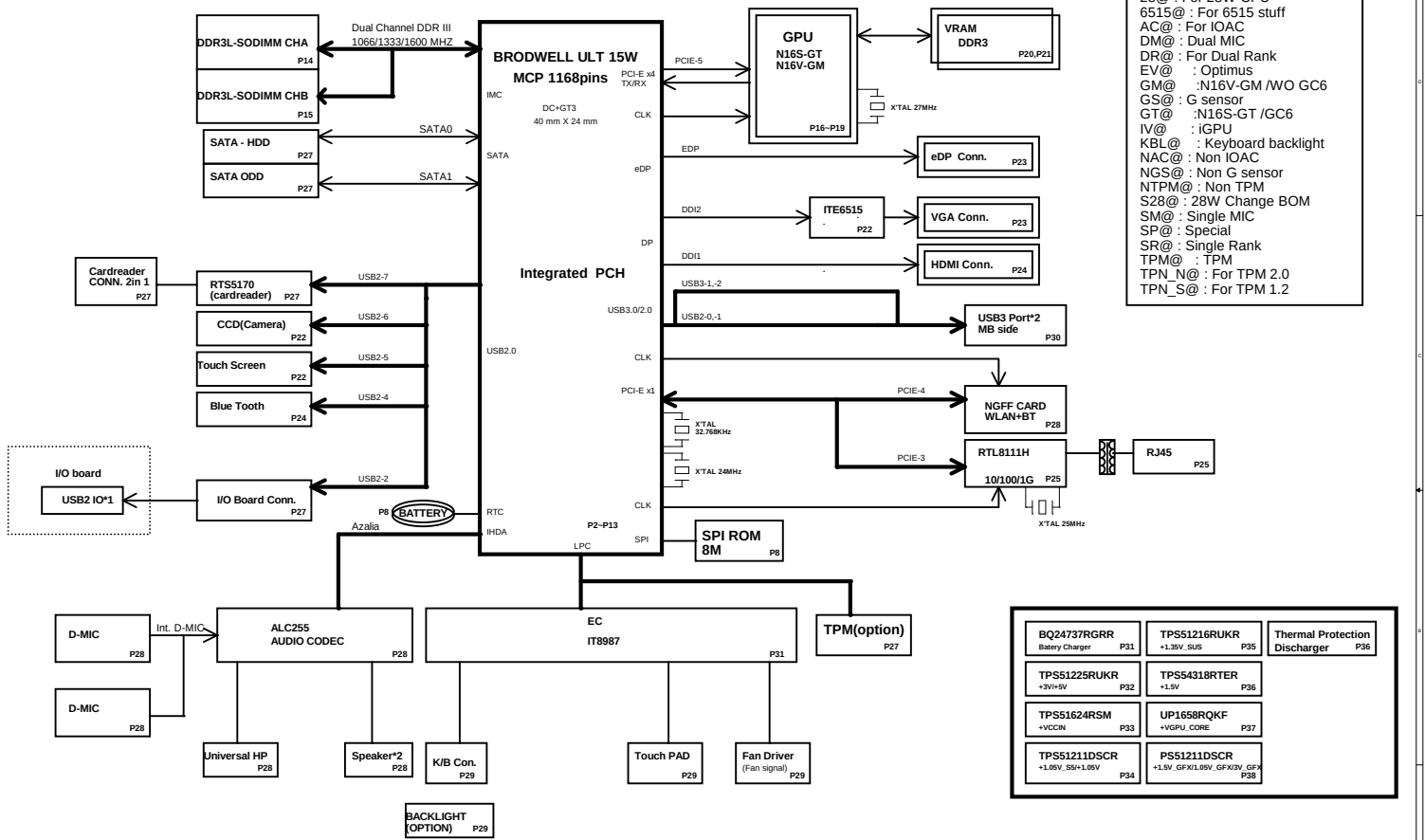


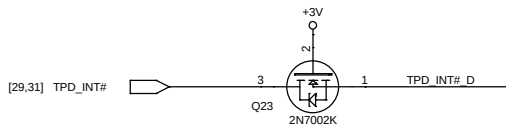
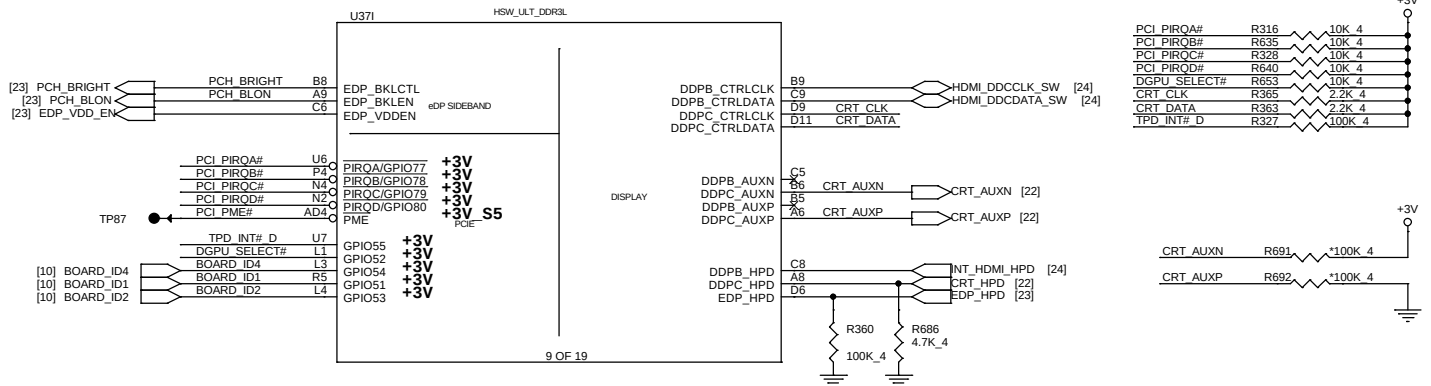
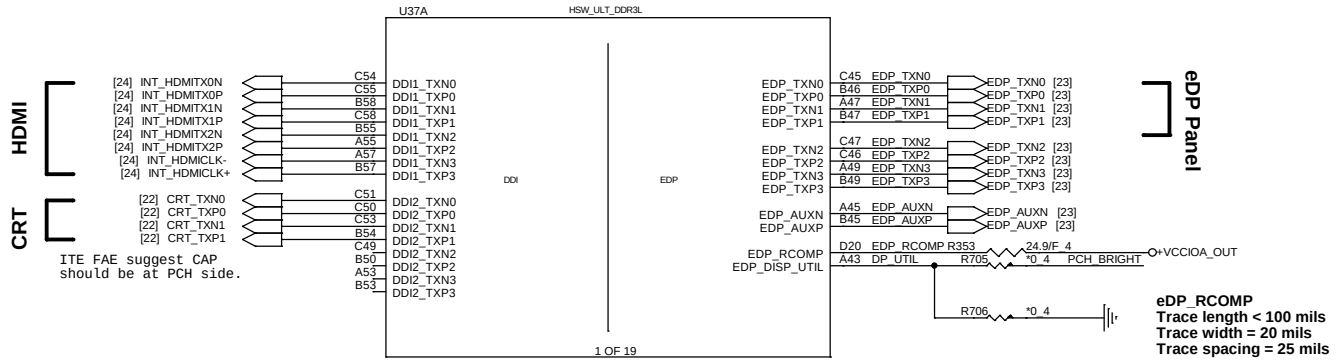
ZRT/ZRTA GDDR3 BWD Laptop System Block Diagram



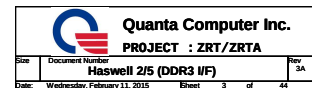
BOM

15@ : For 15W CPU
28@ : For 28W CPU
6515@ : For 6515 stuff
AC@ : For IOAC
DM@ : Dual MIC
DR@ : For Dual Rank
EV@ : Optimus
GM@ : N16V-GM /WO GC6
GS@ : G sensor
GT@ : N16S-GT /GC6
IV@ : iGPU
KBL@ : Keyboard backlight
NAC@ : Non IOAC
NGS@ : Non G sensor
NTPM@ : Non TPM
S28@ : 28W Change BOM
SM@ : Single MIC
SP@ : Special
SR@ : Single Rank
TPM@ : TPM
TPN_N@ : For TPM 2.0
TPN_S@ : For TPM 1.2

Haswell ULT (DISPLAY, eDP)



Haswell Processor (DDR3)

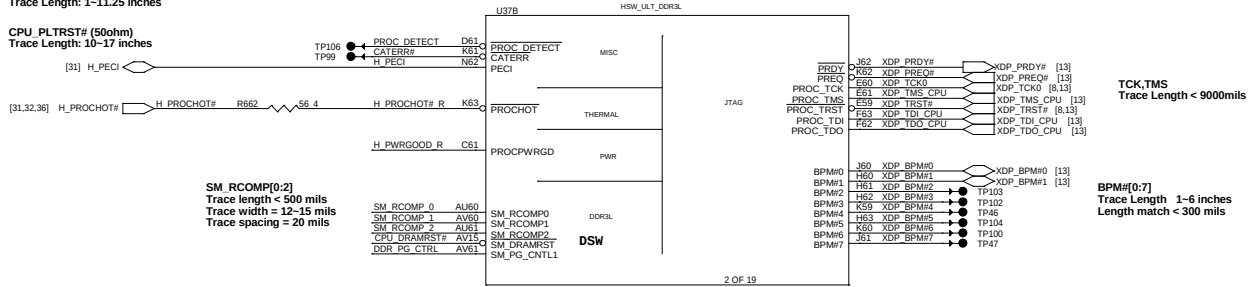


Haswell ULT (SIDE BAND)

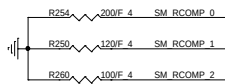
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

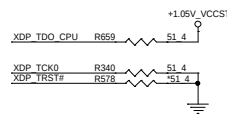
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



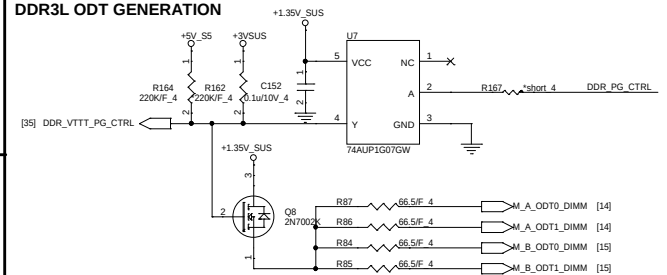
DRAM COMP



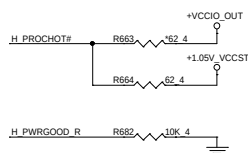
XDP PU/PD



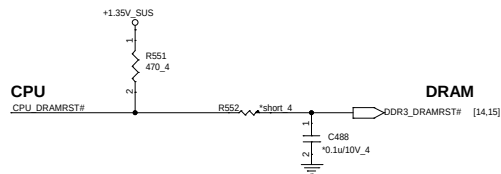
DDR3L ODT GENERATION



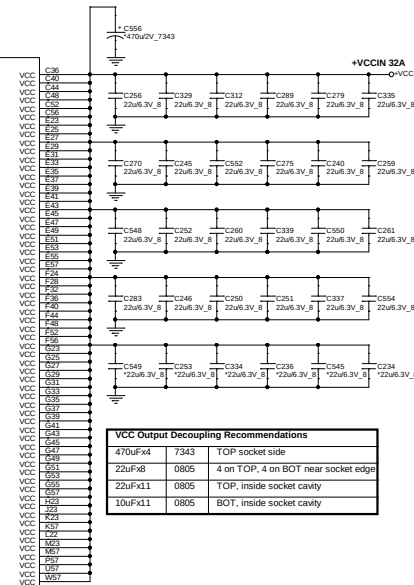
PU/PD of CPU



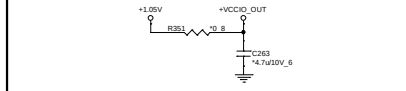
DRAMRST



Laptopblue



470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

[illegible]

SVID

Layout note: need routing together and ALERT need between CLK and DATA.

+VCCIO_OUT +1.05V_VCCST

R651 130F_4 R652 130F_4 R653 130F_4

H_CPU_SVIDDAT +VCCIO_OUT 100F_4 +VCCIO_ALERT2 [36]

Place PU resistor close to CPU

H_CPU_SVIDDAT2 +1.05V_VCCST +VCCIO_OUT

R637 75_4 R636 75_4

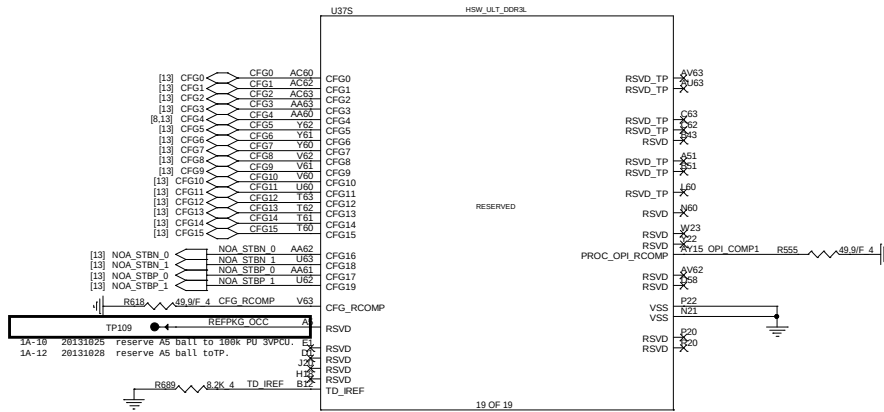
H_CPU_SVIDDAT2 100F_4 +VCCIO_ALERT2 [36]

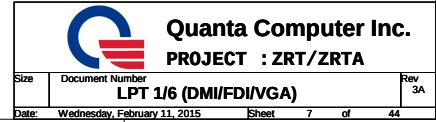
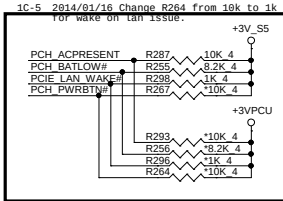
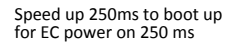
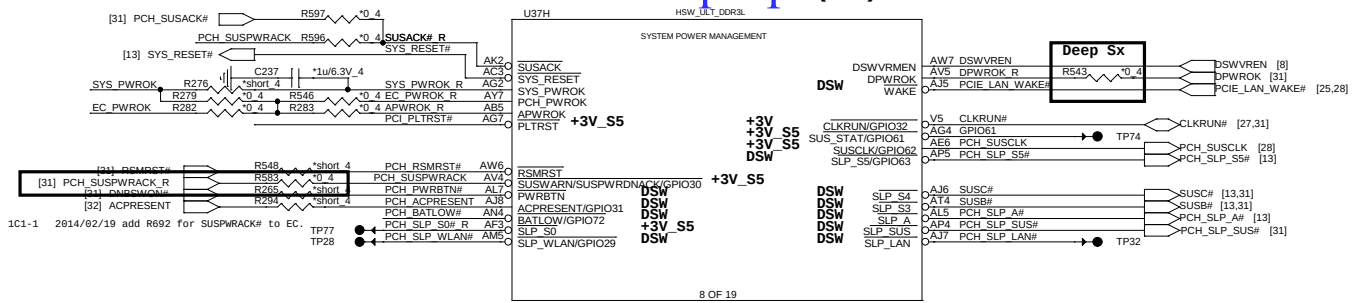
Place PU resistor close to CPU

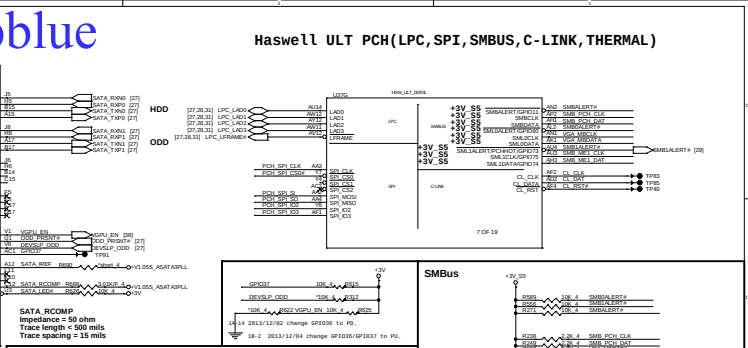
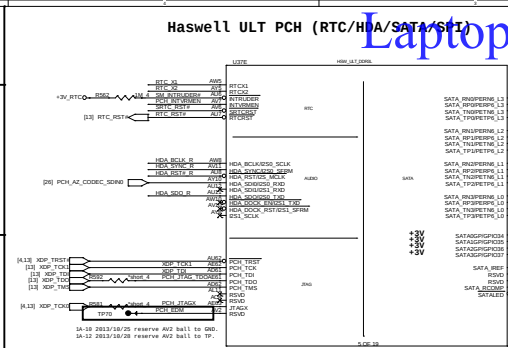
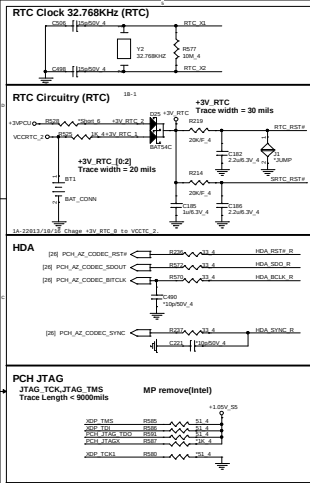
H_CPU_SVIDCLK 100F_4 +VCCIO_ALERT2 [36]

 Quanta Computer Inc. PROJECT : ZRT/ZRTA		Rev	3A
Size	Document Number	Haswell 4/5 (POWER)	
Date:	Wednesday, February 11, 2015	Sheet	5 of 44

Haswell Laptop (CF9, RSV)

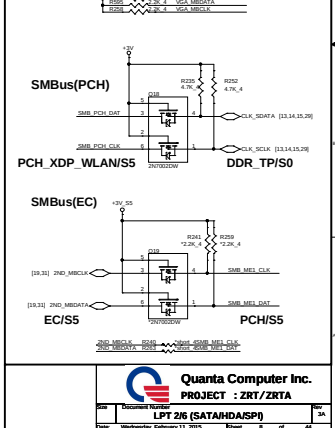
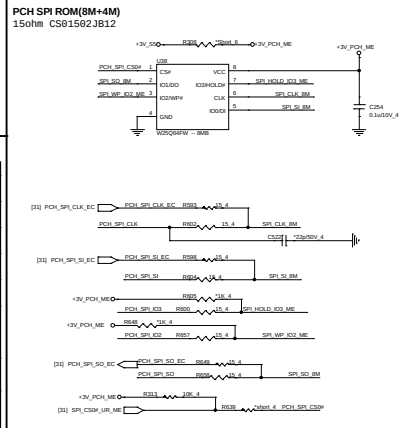


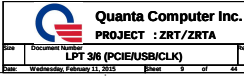




ULT Strapping Table

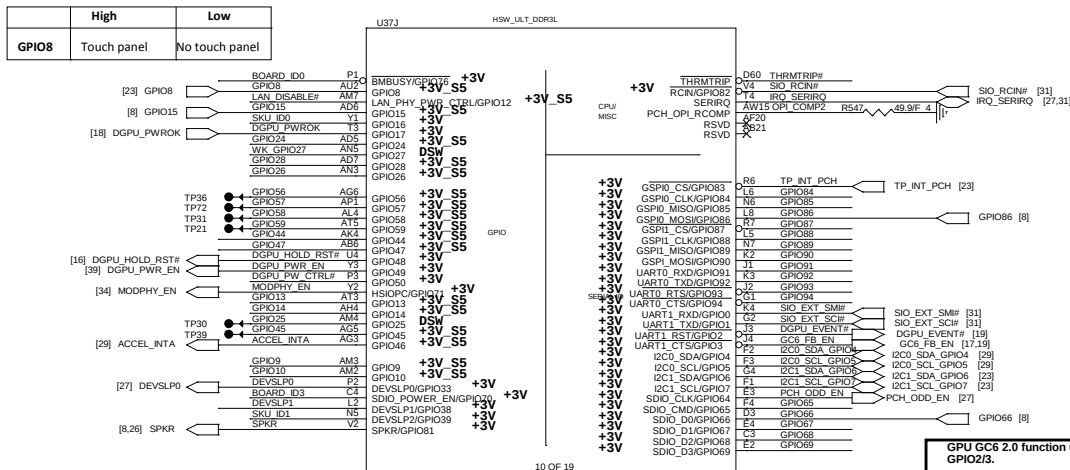
Pin Name	Strap description	Sampled	Configuration	note
GPIO01(SPKR)	No reboot on TCO Timer expiration	PWR0K	0 = Default enable (IPD 20K) 1 = Disable: No-Reboot mode	[10.1] GPIO01
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWR0K	0 = Default can program ME (IPD 20K) 1 = can't program ME	HDA_SDO
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	
GPIO06	Top-Block Swap override		0 = Default enable (IPD 20K) 1 = Enable TBS function	
GPIO08	Boot BIOS Strap Bit		0 = Default enable (IPD 20K) 1 = LPC	
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(IPD 20K) 1 = Default enable with confidentiality	
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 = disable	[11.1] CFG4
DSWVREN	Deep Sx well on die VR enable		1=Should be always pull-up	



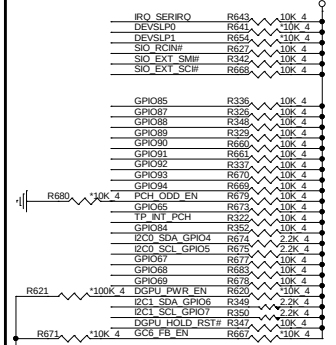


Haswell ULT PCH (GPIO,CPU/MISC,NTF)

	High	Low
GPIO8	Touch panel	No touch panel

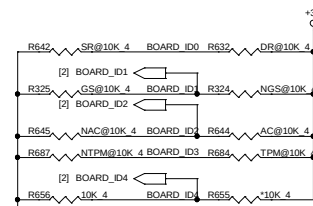


PCH GPIO PU/PD



1A-1 20131815 For GC6 NV DG GC6_FB_EN PD.
1A-8 20131822 Change GPIO83/84 GPU GC6 pin to GPIO2/3.
1A-12 20131829 Change GPIO45 to PU S5, change GPIO58 one is GPIO56.

Board ID



	Low	High
BOARD_ID0	single rank SKU	Dual rank SKU
BOARD_ID1	Reserved (Default)	Reserve
BOARD_ID2	No IOAC	IOAC
BOARD_ID3	No TPM	TPM
BOARD_ID4	Non-Dolly (Default)	Dolly

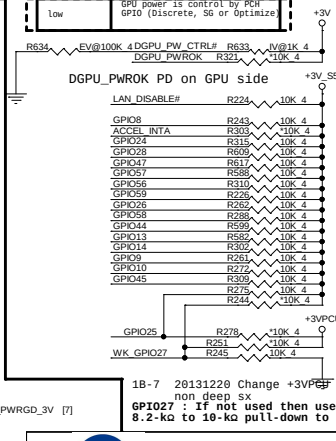
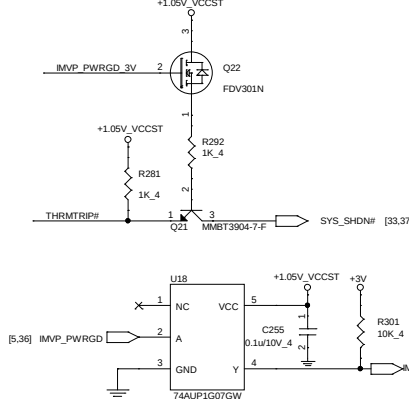
RAM ID



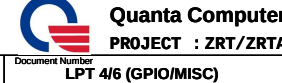
SKU ID

	SKU_ID1	SKU_ID0	VGA H/V Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

CPU thermal trip



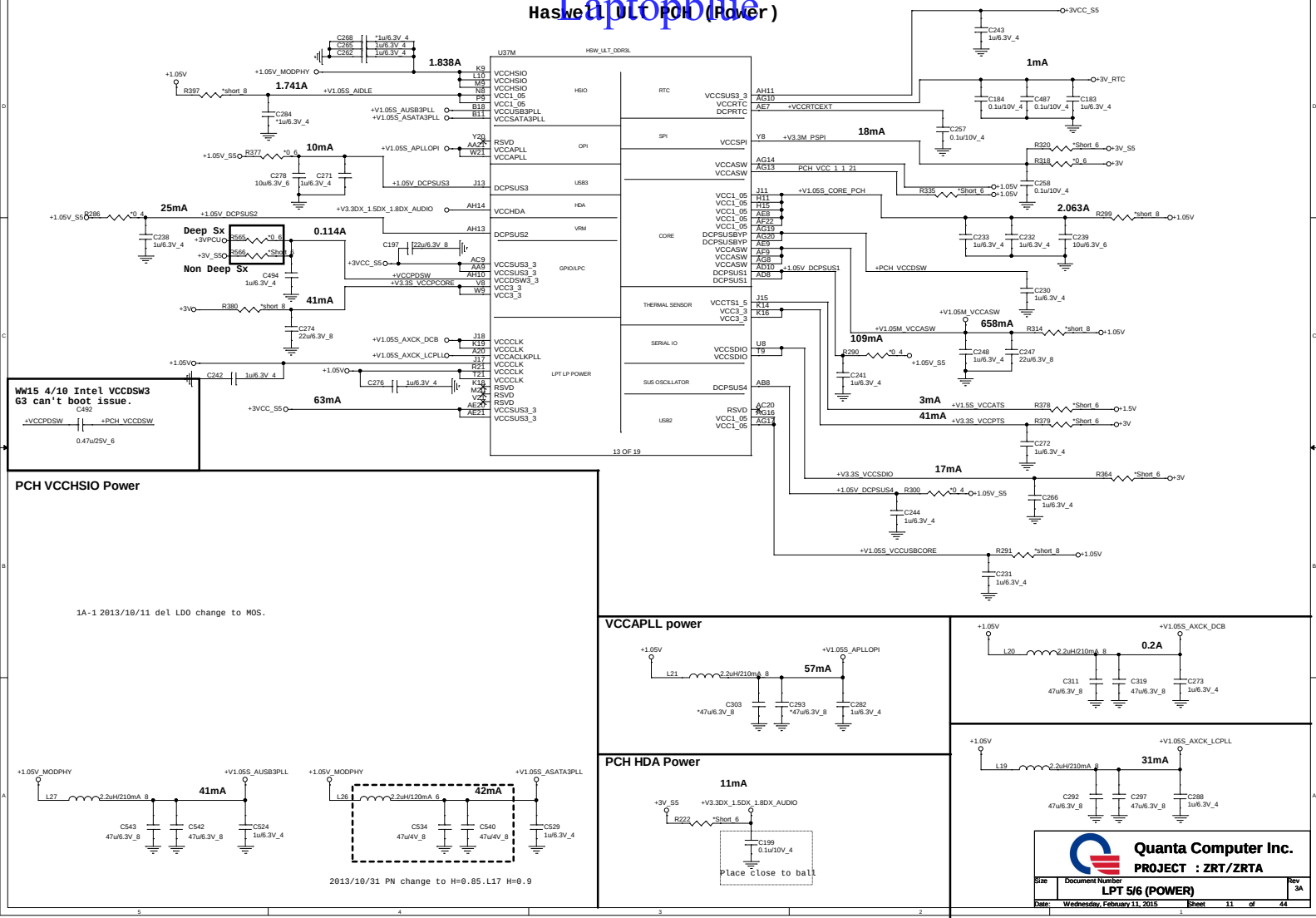
1B-7 20131228 Change +3V_P5 to +3V_S5 non deep sx
GPIO27 : if not used then use 8.2-kΩ to 10-kΩ pull-down to GND.



Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	3A

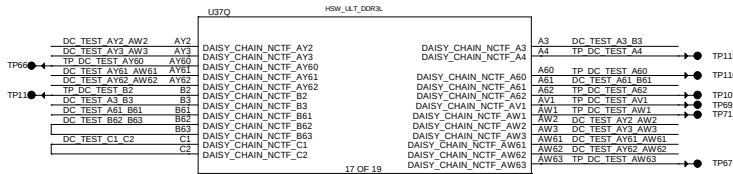
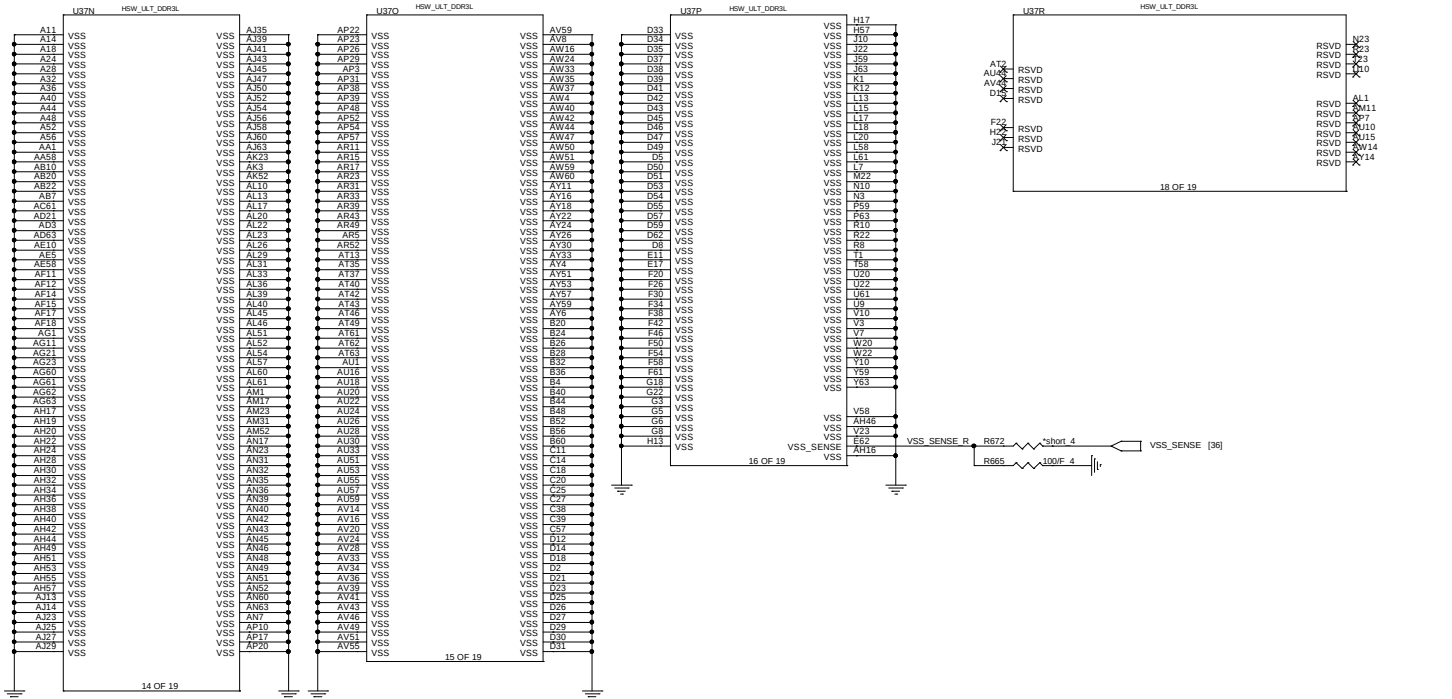
Date: Wednesday, February 11, 2015 Sheet 10 of 44

Haswell ULT PCH (Power)



Haswell ULT (GND)

Laptopblue

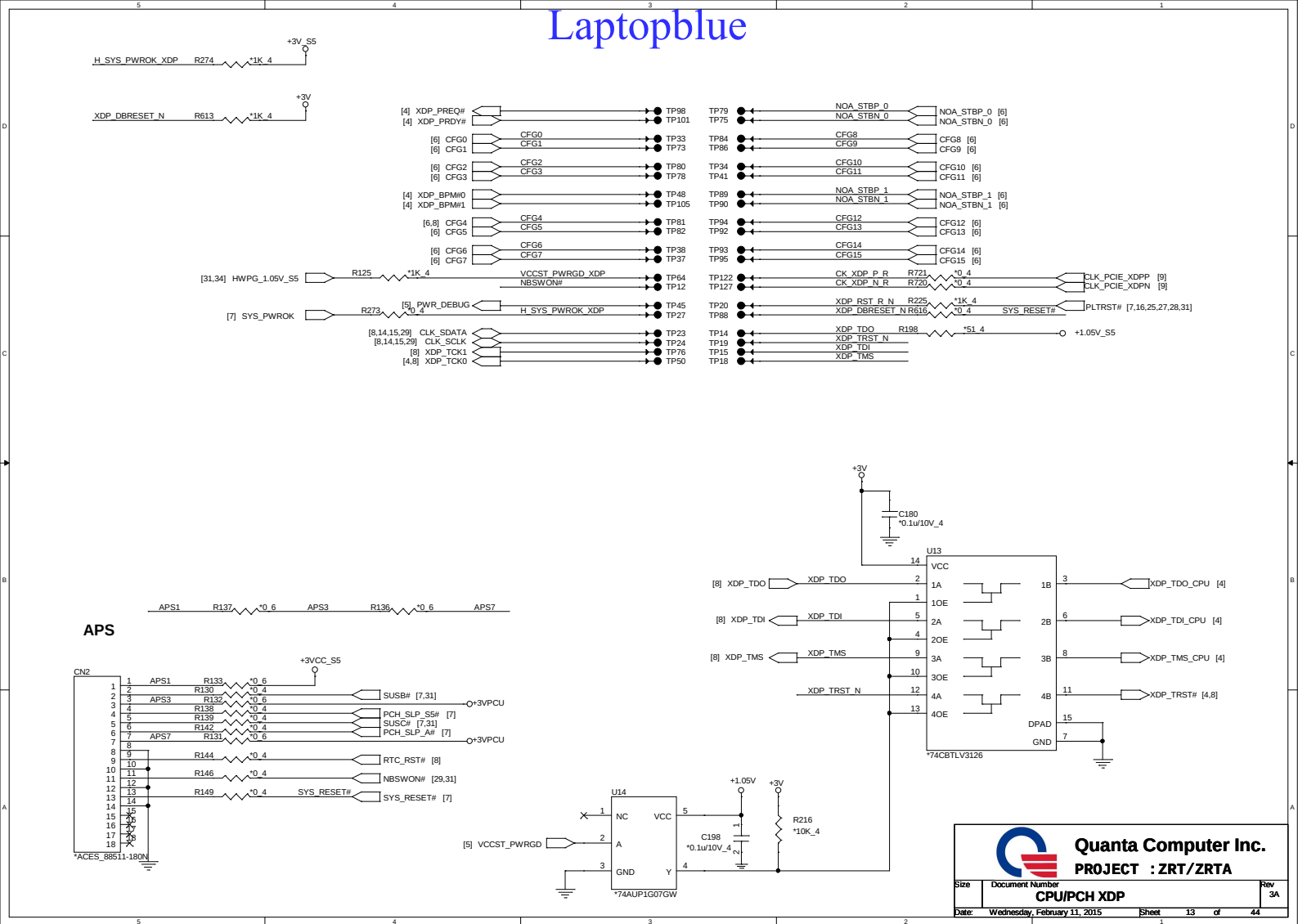


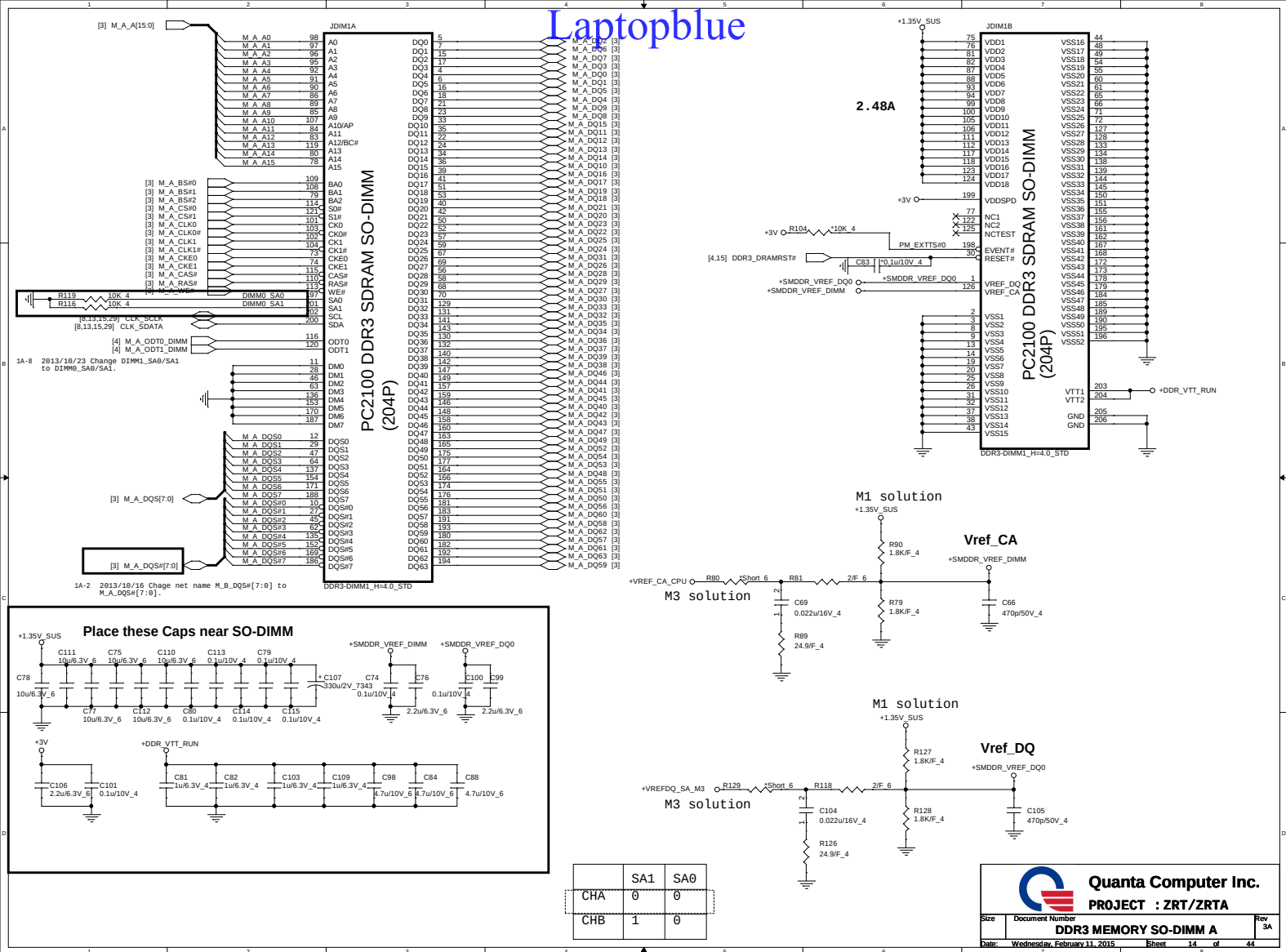


Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	LPT 6/6 (GND)	3A
Date	Wednesday, February 11, 2015	Sheet 12 of 44

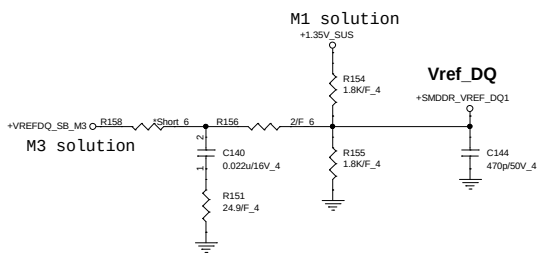
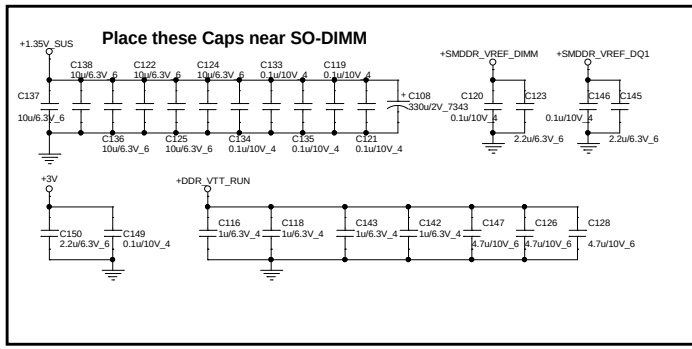
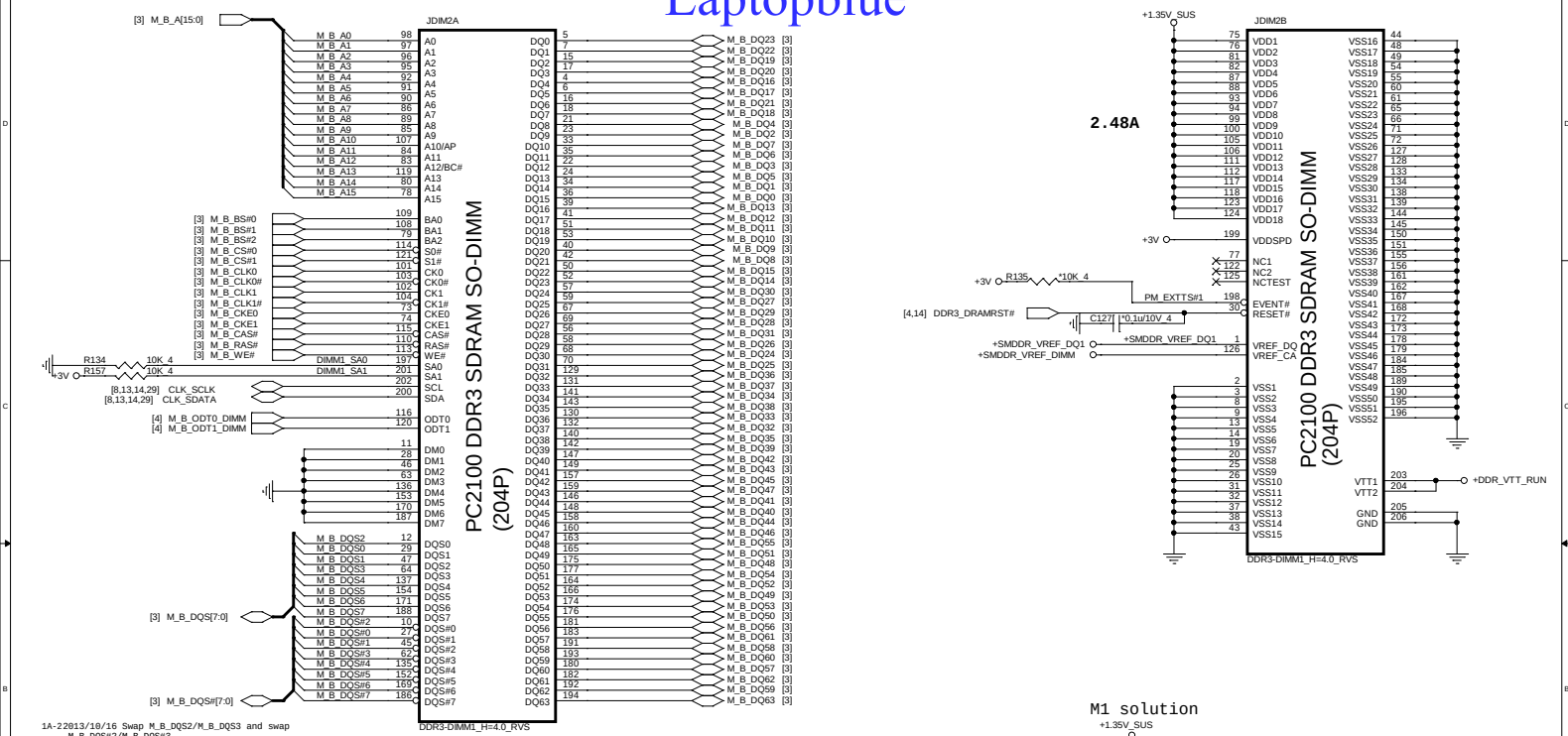
Laptopblue





	SA1	SA0
CHA	0	0
CHB	1	0

Laptopblue



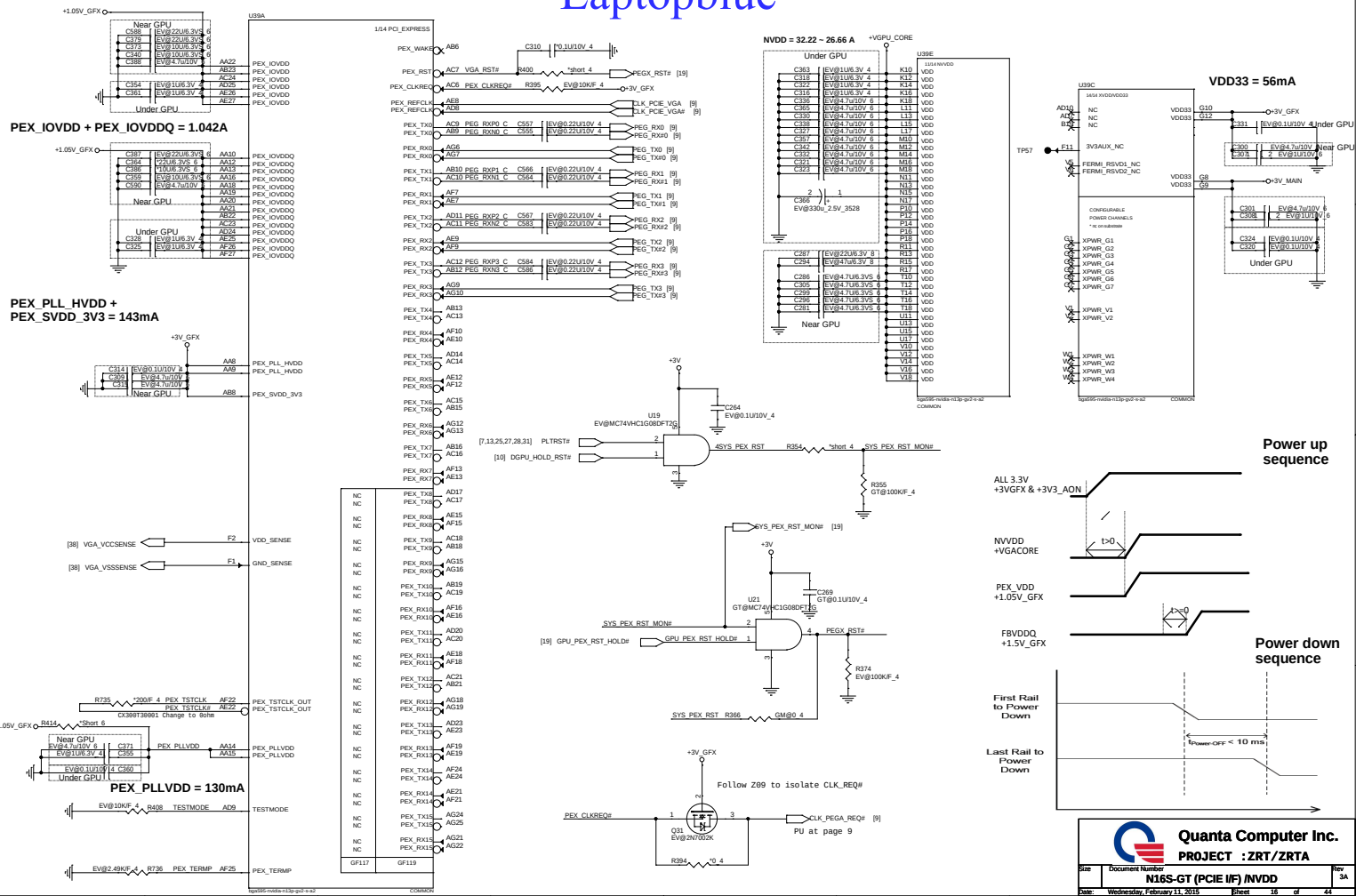
	SA1	SA0
CHA	0	0
CHB	1	0

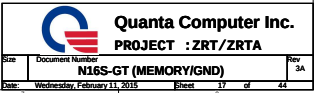
Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size Document Number
DDRIII Memory SO-DIMM B

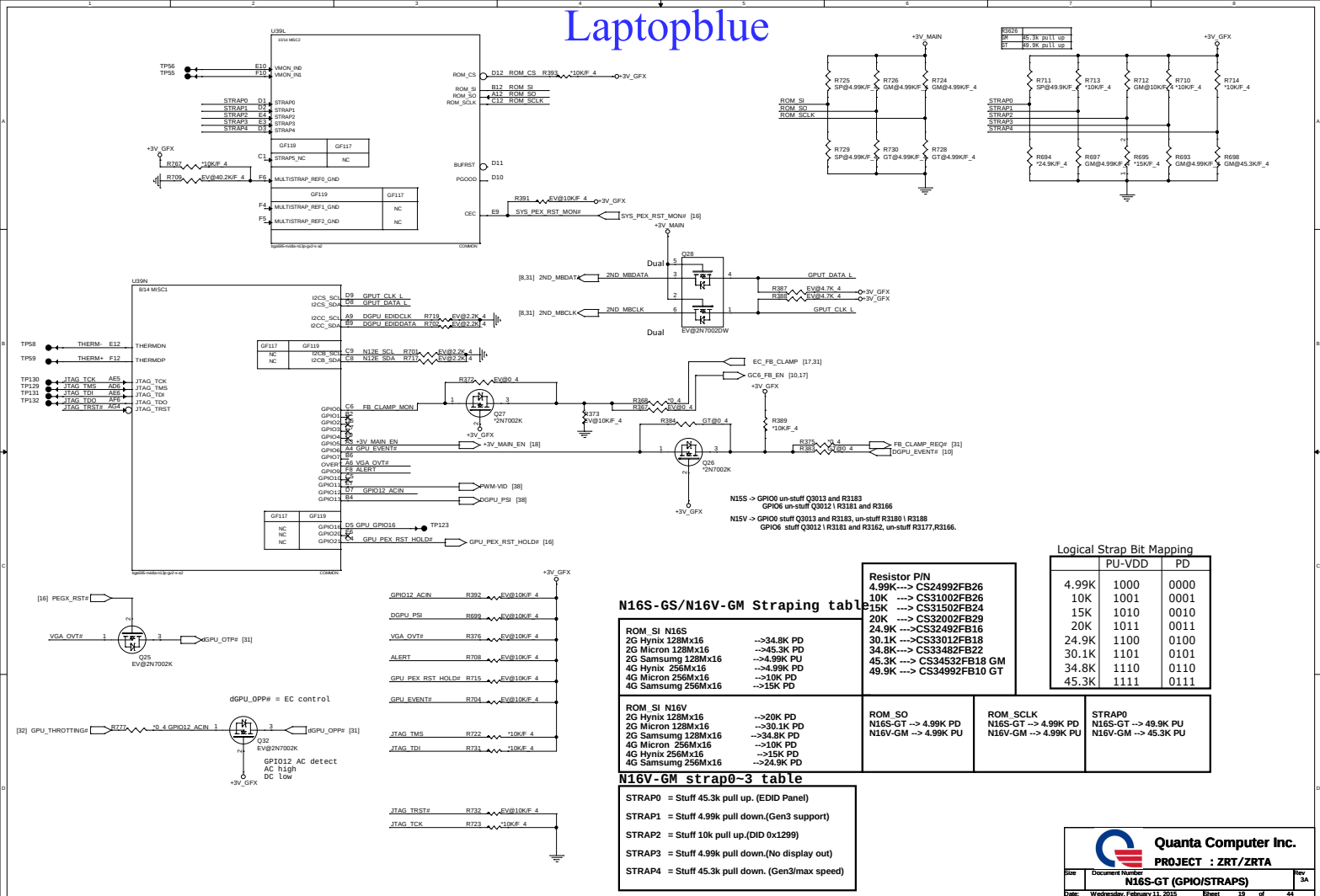
Date: Wednesday, February 11, 2015 Sheet 15 of 44 Rev 3A

Laptopblue



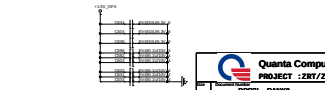
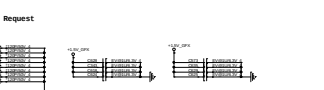
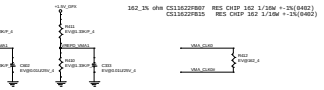
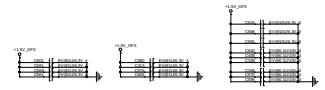
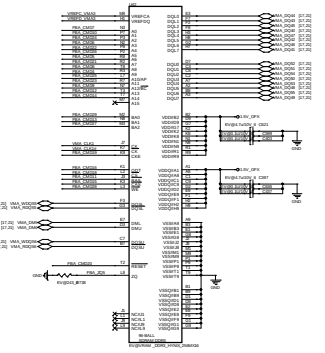
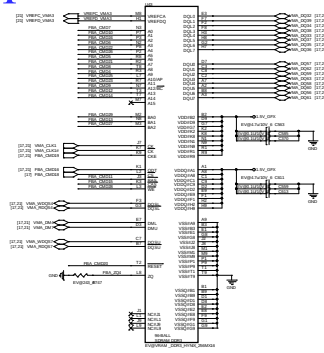
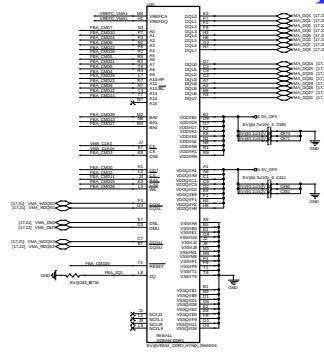
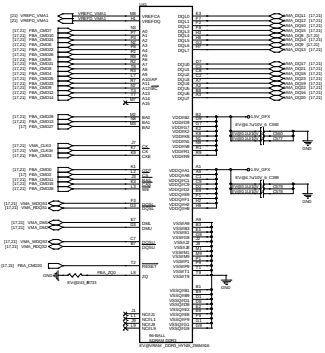


Laptopblue

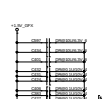
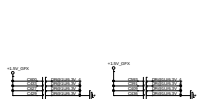
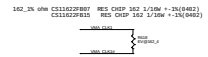
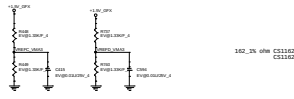
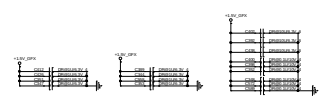
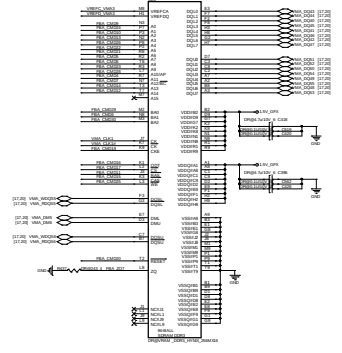
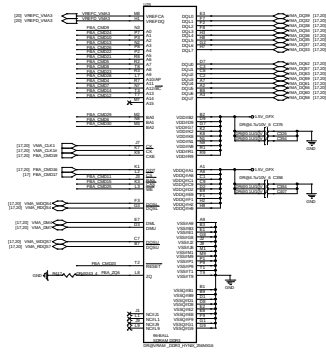
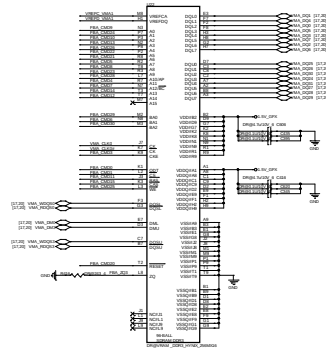
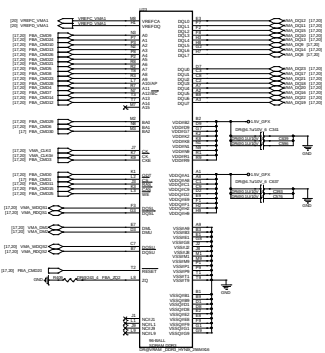


Laptopblue

WU 2509416, H5C462346F-11C QOC PR : ARSPT07MB...TSP 8/5 PR : ARSPT07MB
H5C 2509416, H5C462346F-11C QOC PR : ARSPT07MB...TSP 8/5 PR : ARSPT07MB
SAP 2509416, H5C462346F-11C QOC PR : ARSPT07MB...TSP 8/5 PR : ARSPT07MB

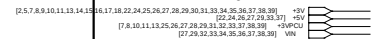
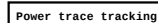
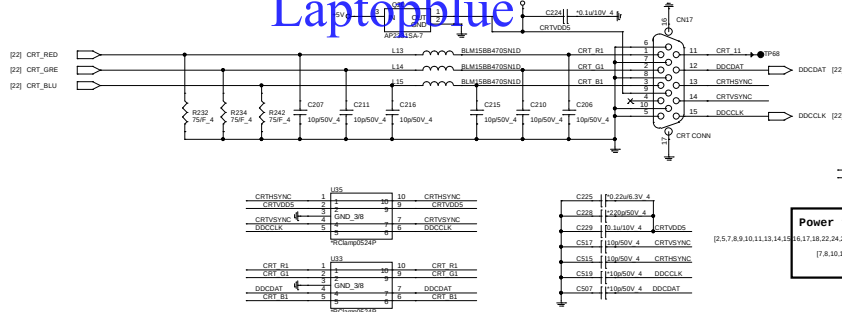


Laptopblue

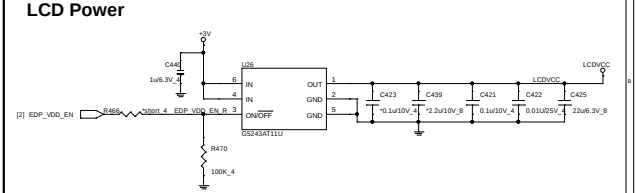
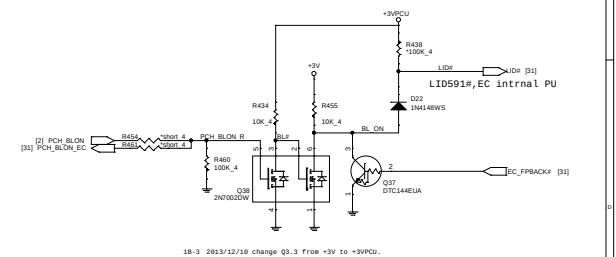


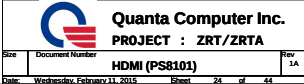


Laptopblue

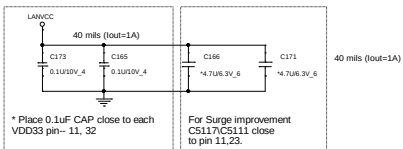


LCD Power

[illegible]



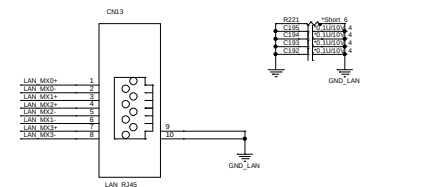
Laptopblue



* Place 0.1uF CAP close to each VDD10 pin-- 3, 8, 22, 30

The diagram shows a section of a PCB layout for the VDD10 power plane. A horizontal bus line is labeled "40 mils (Iout=1A)". Below this bus, several decoupling capacitors are placed: C460 (0.1uF, V4_4), C476 (0.1uF, V4_4), C478 (0.1uF, V4_4), C481 (0.1uF, V4_4), C477 (1uF, V4_4), and C478 (0.1uF, V4_4). A ground symbol is shown below the bus line. A VDD10 pin is shown on the right, connected to the bus line.

RJ45 Connector

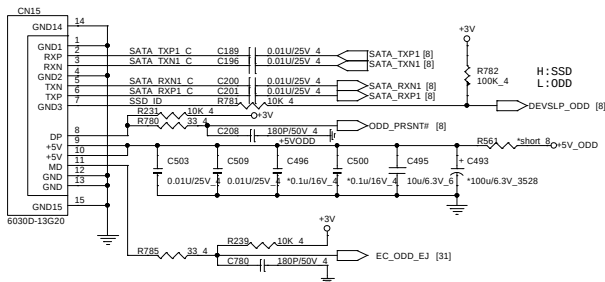

$$\begin{array}{l} [2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,26,27,28,29,30,31,33,34,35,36,37,38,39] \\ [5,7,8,9,10,11,13,27,29,31,33,36,38] \\ [7,8,10,11,13,23,26,27,28,29,31,32,33,37,38,39] + \end{array}$$


Quanta Computer Inc.

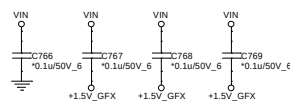
PROJECT : 2

Size	Document Number	REV
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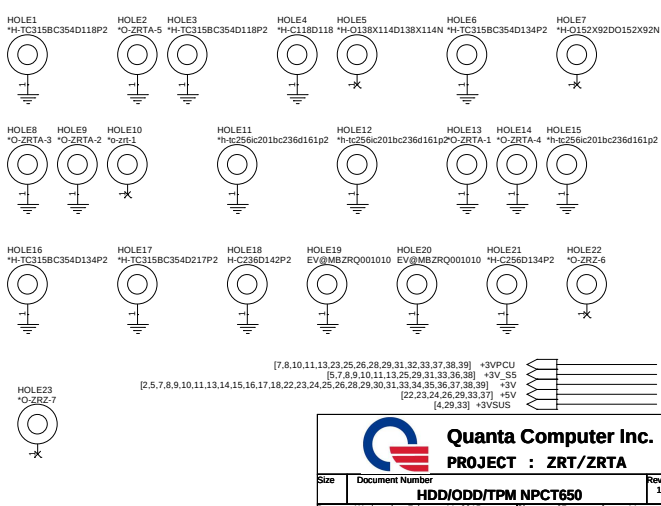
SATA ODD Connector(ODD)

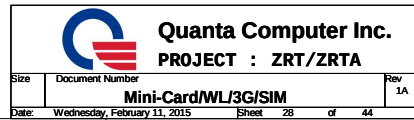


EMI

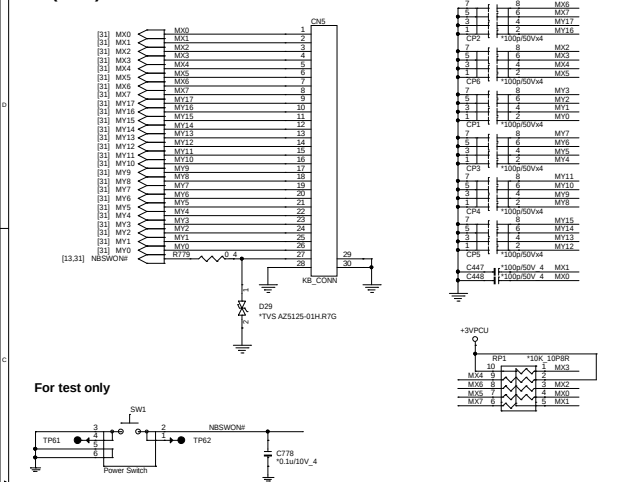


HOLE1	HOLE2	HOLE3	HOLE4	HOLE5	HOLE6	HOLE7
*H.TC315RC354D118P2	*O.ZPTA.5	*H.TC315RC354D118P2	*H.C118D118	*H.O138Y114D138Y114N	*H.TC315RC354D134P2	*H.O152X92D0152X92

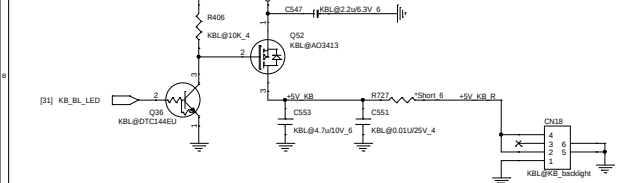




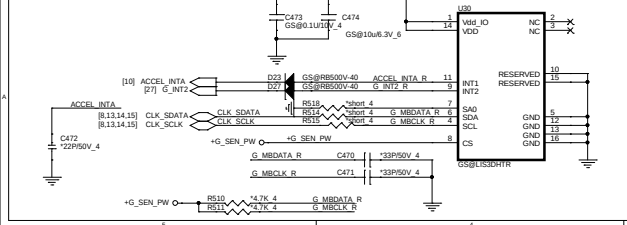
K/B (KBC)



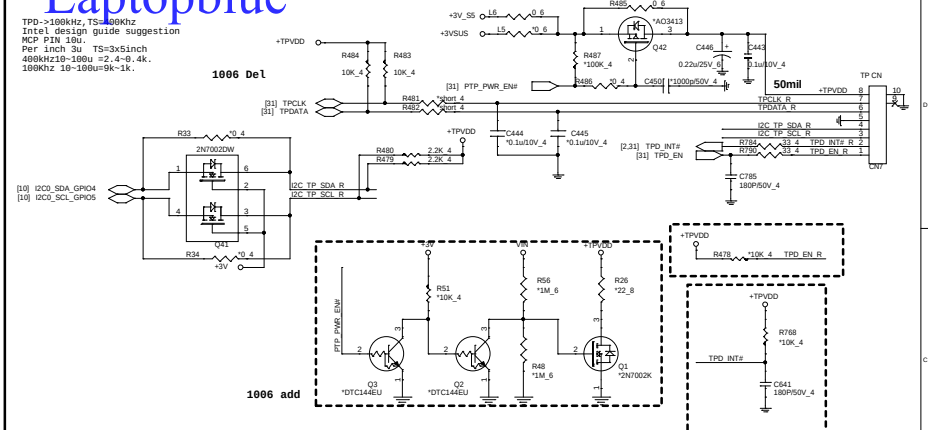
KB_BL LED (KBL)



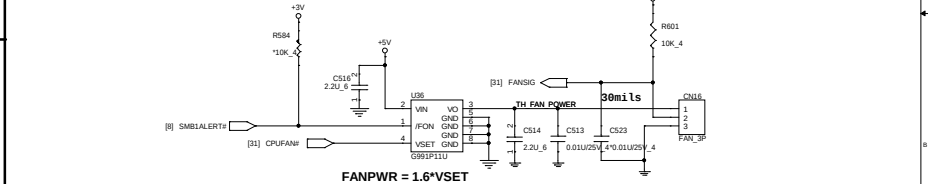
G-sensor(ACS)



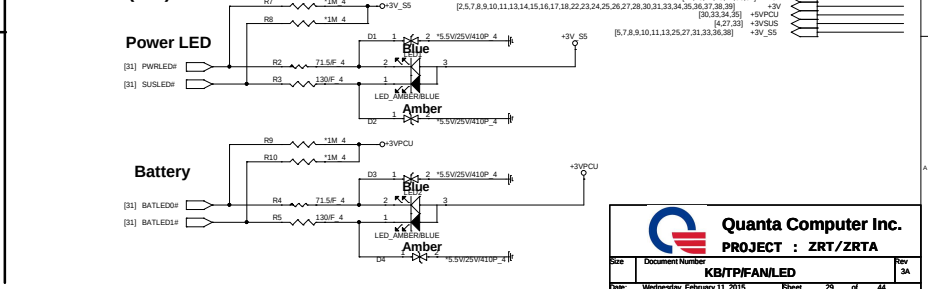
3	
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)	



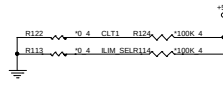
CPU FAN (THM)



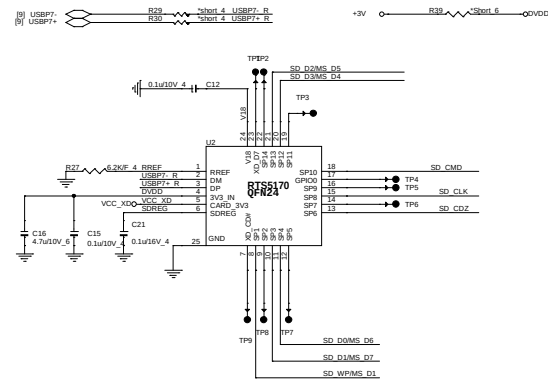
POWER LED(UIF)



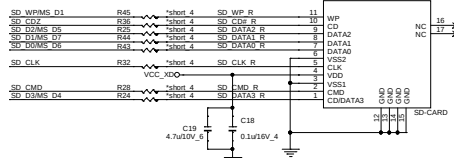
USB Charger for USB3.0 Port0 (UBC)

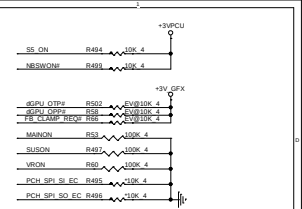
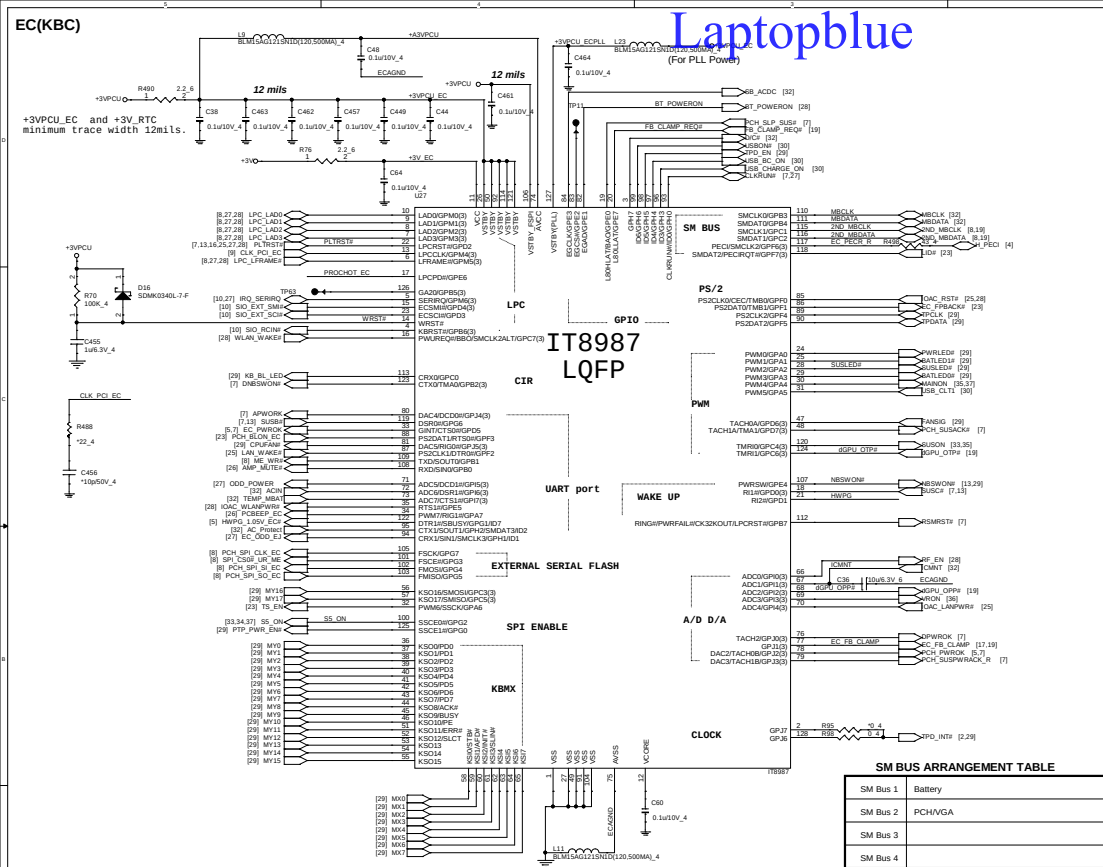
[illegible]

Card Reader (CRD)

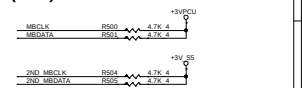


SD/MMC CARD READER (CRD)

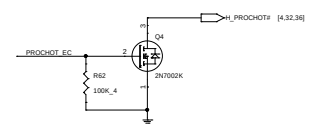
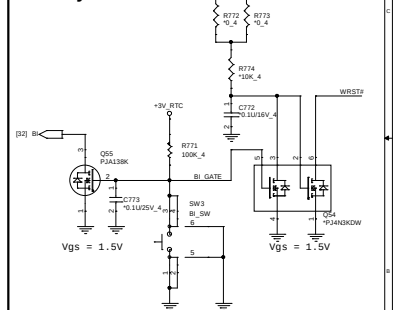




SM BUS PU(KBC)

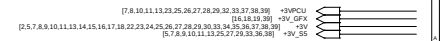
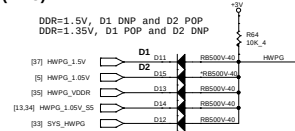


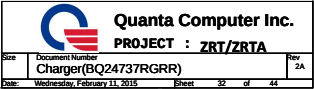
Battery B/I SW

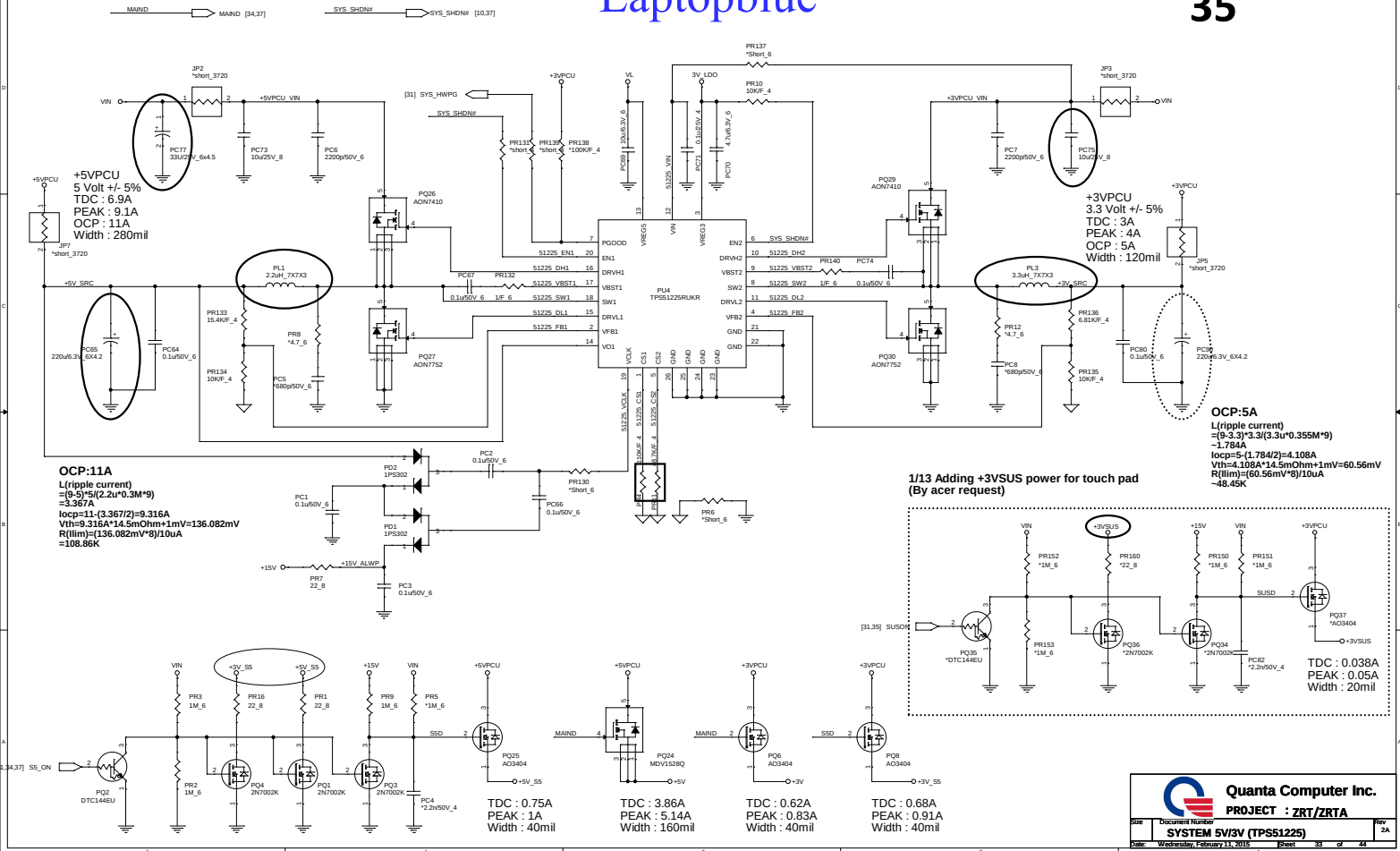


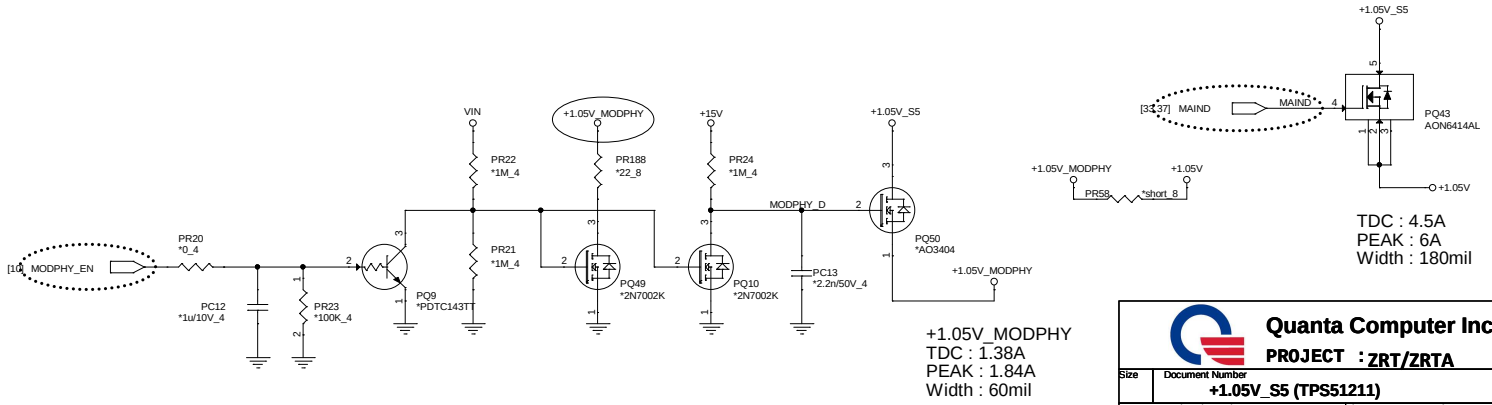
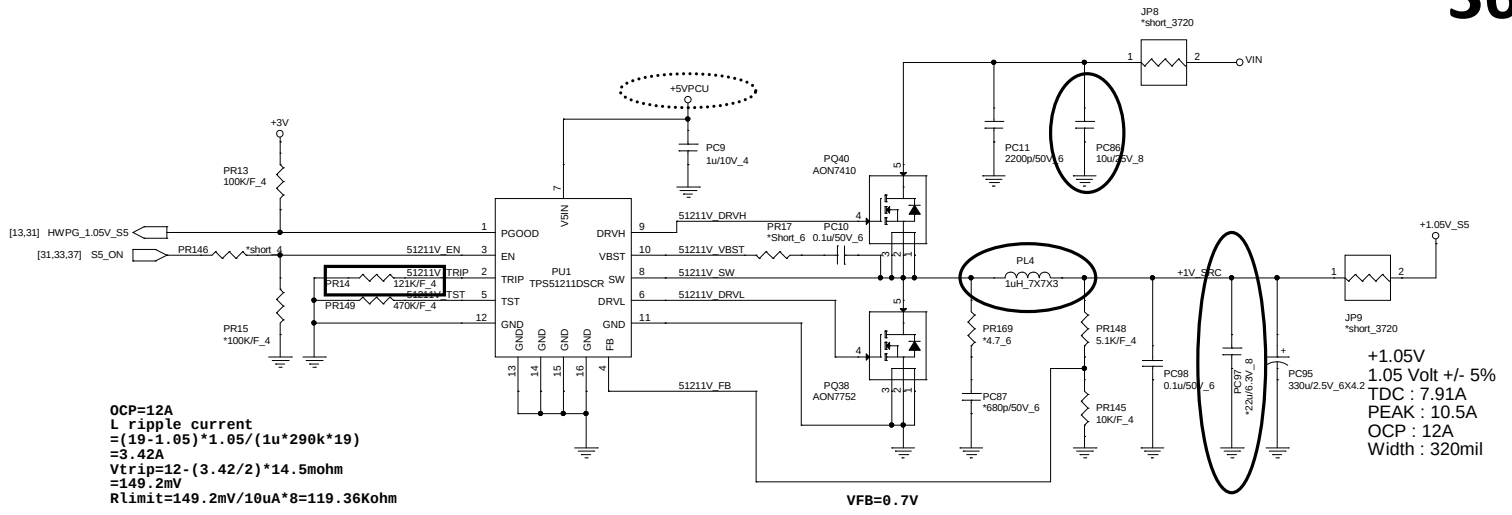
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

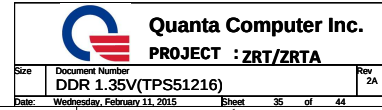
HWPG(KBC)

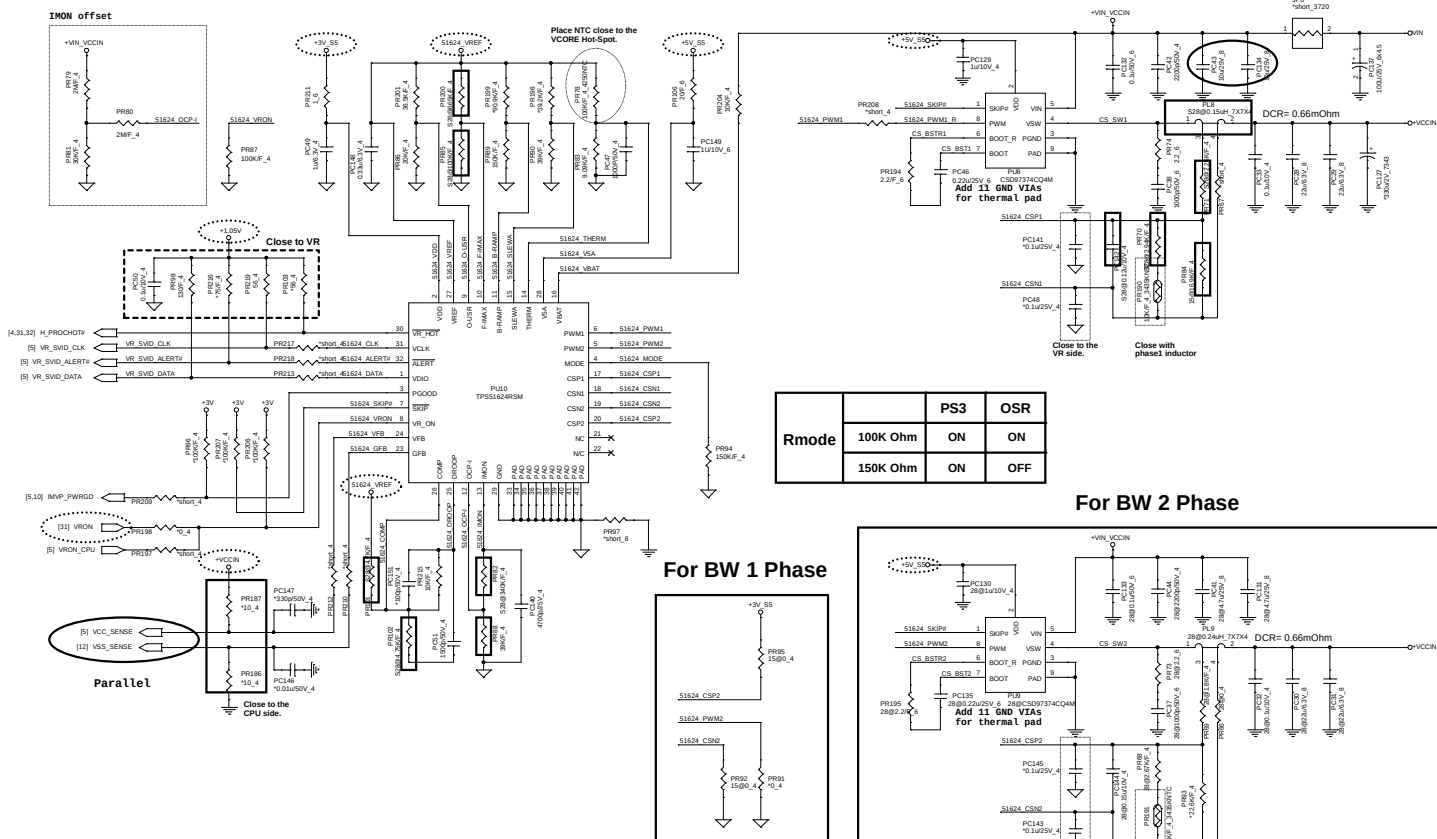










**BW-U 15W (1 phase)**

Icc TDC PL2 : 14A
 Icc Max : 32A
 OCP : 37A
 Fsw : 1.2MHz

VCORE L/L :

R_DC_LL : - 2.0mV/A
 R_AC_LL : - 7.0mV/A

BW-U 28W (1 phase)

Icc TDC PL2 : 19A
 Icc Max : 40A
 OCP : 47A
 Fsw : 800KHz

VCORE L/L :

R_DC_LL : - 2.0mV/A
 R_AC_LL : - 7.0mV/A

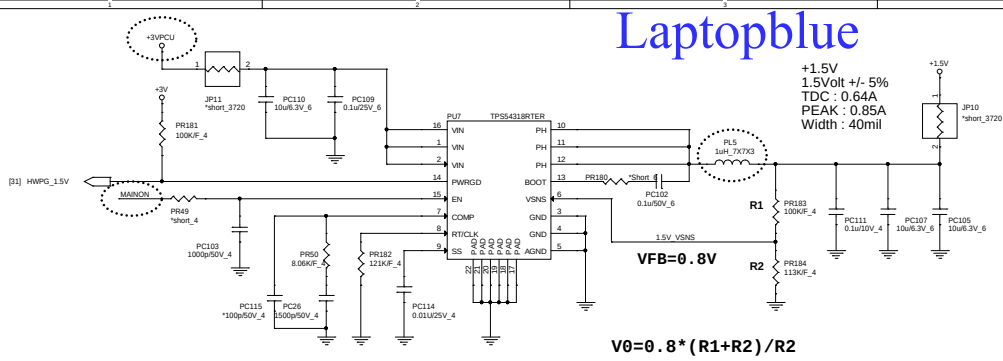
S28@**BW-U 28W 2 phase**

Location	Value	Location	Value
PL8	CV+24P0MZ00	PR85	CS35622FB10
PR71	CS21622FB14	PR101	CS22372FB11
PR82	CS41502FB18	PR102	CS31002FB26
PR70	CS22672FB12	PR200	CS42942FB13
PC142	CH4152K9B02		
Block 1.	Stuff		

PL9 0.24uH_7X7X4
 PR84 - PR93 *22.6K/F_4
 PR92 - PR95 *0_4
 PC143 - PC145 *0.1u/25V_4

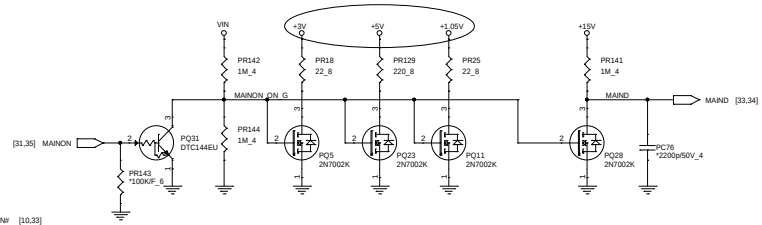
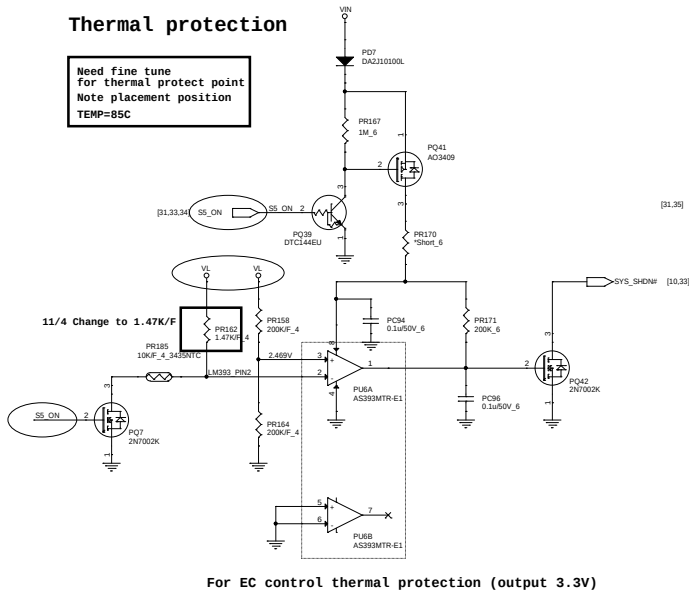
Quanta Computer Inc.
PROJECT : ZRT/ZRTA

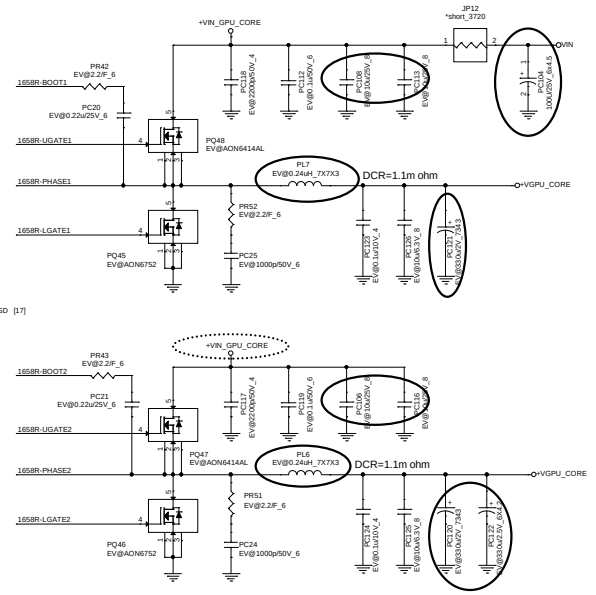
Doc: **TPS51624**
 Date: **Wednesday, February 13, 2015** **Page: 38 of 44**



Thermal protection

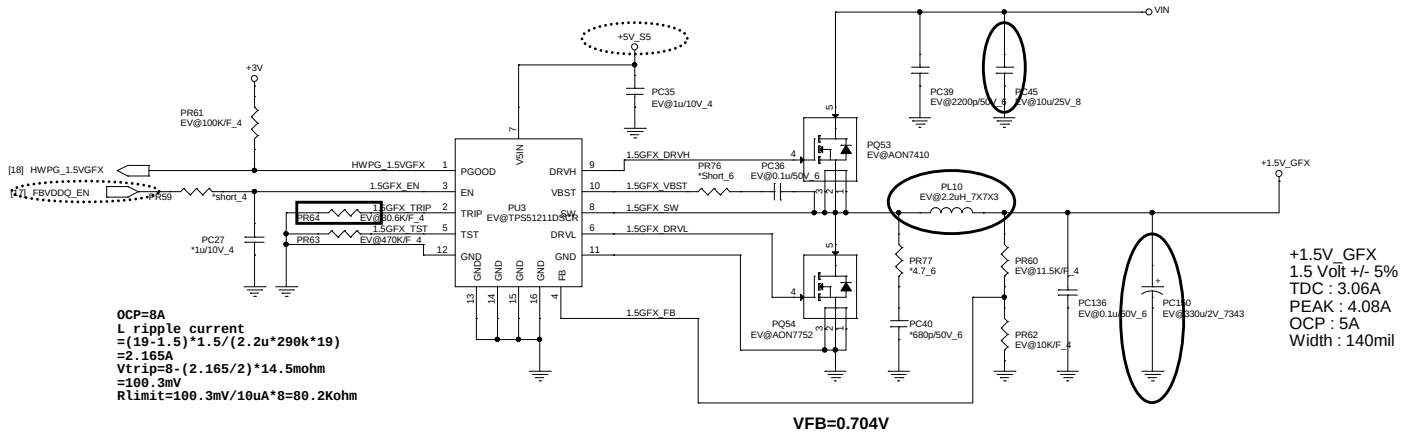
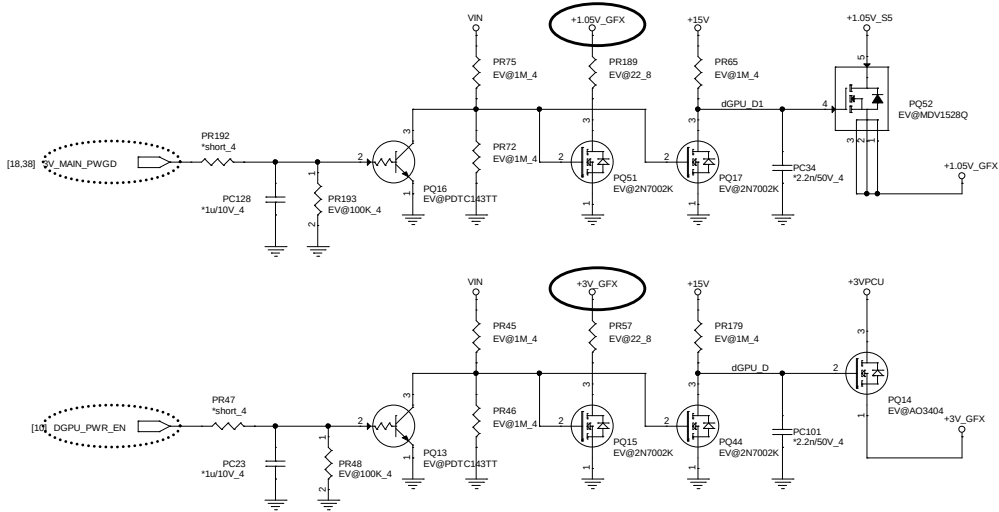
Need fine tune
for thermal protect point
Note placement position
TEMP=85C

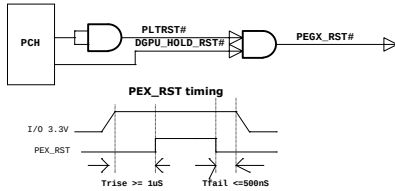
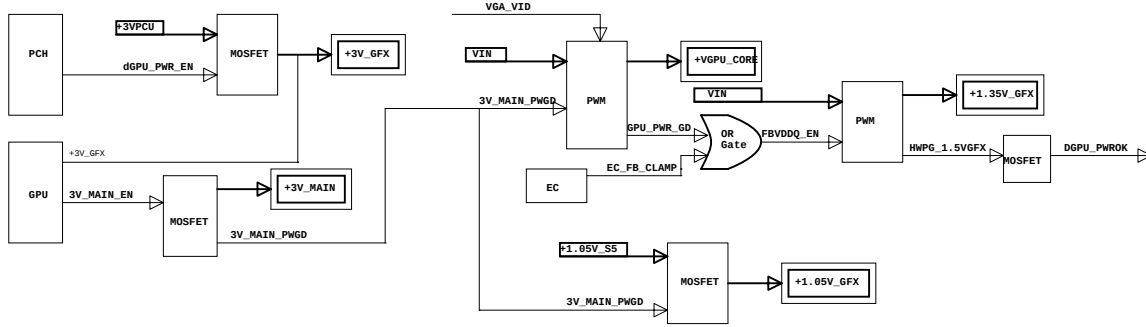




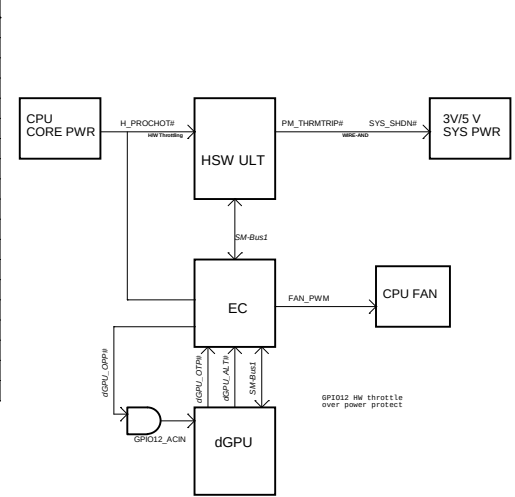
+VGPU_CORE
Countinue current:26A
Peak current:51A
OCP:A
FSW:300KHz
L/L=0mV/A

[16,17,18] +1.05V_GFX
[17,20,21,27] +1.5V_GFX
[16,18,19,31] +3V_GFX

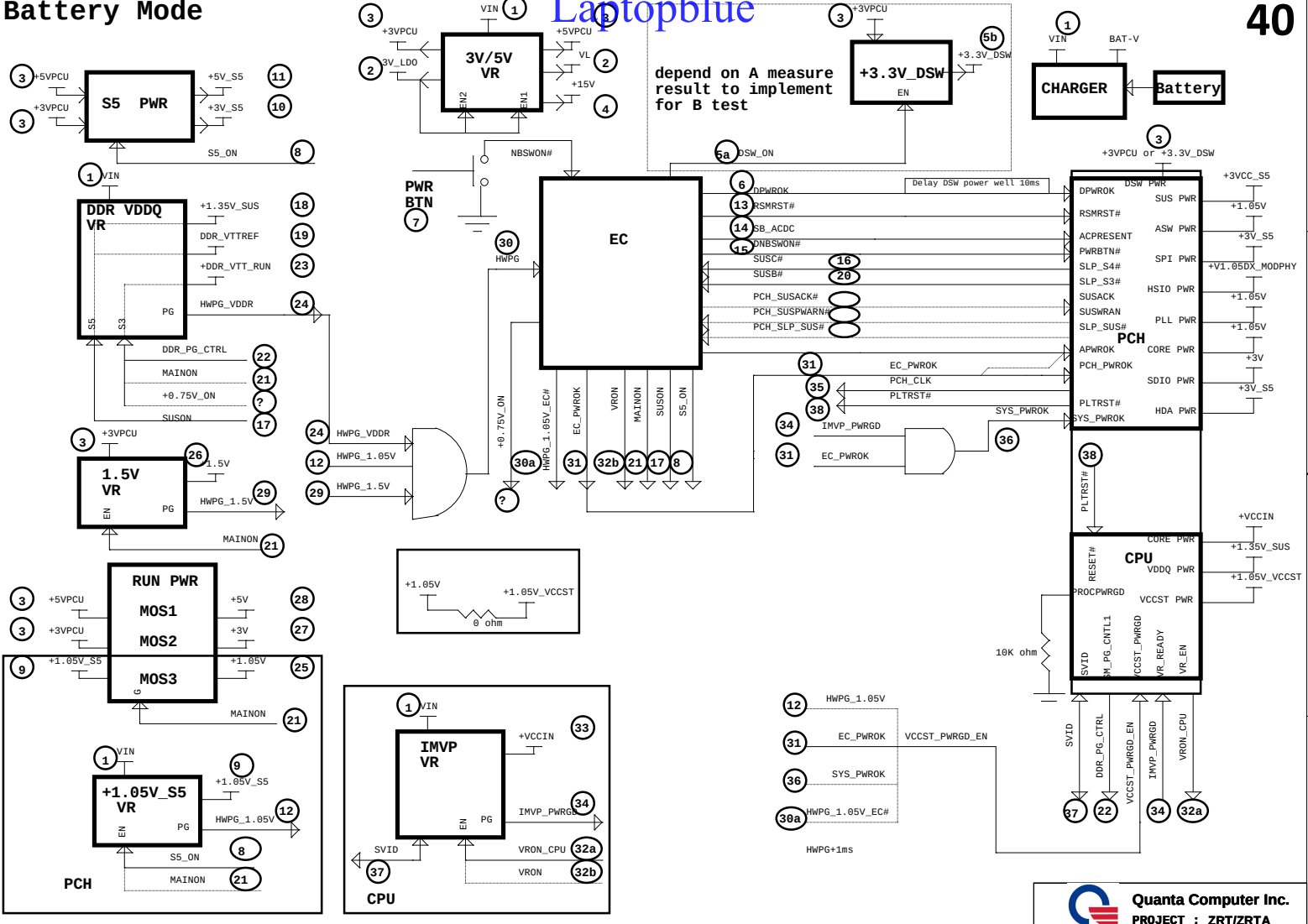


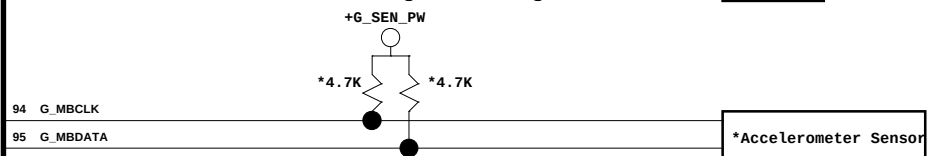
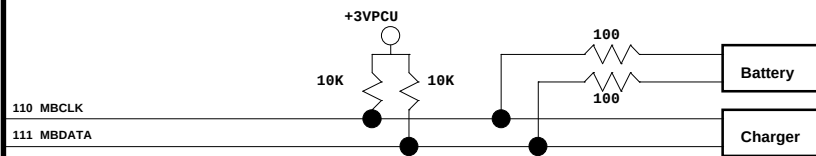
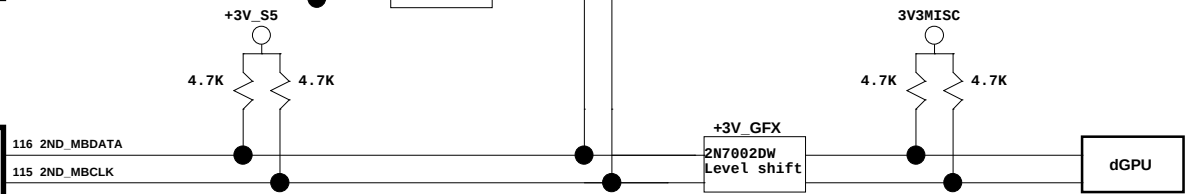
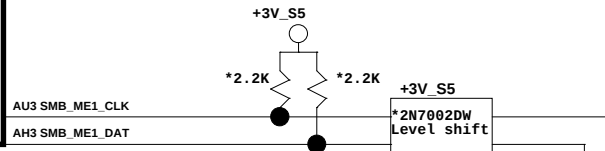
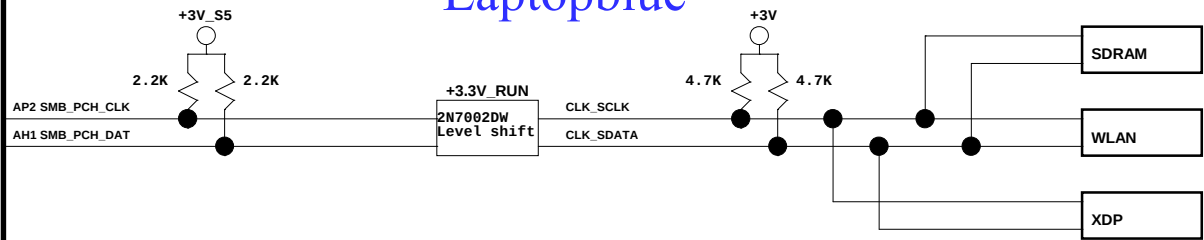


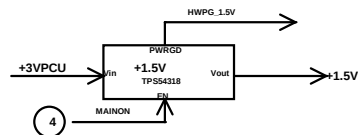
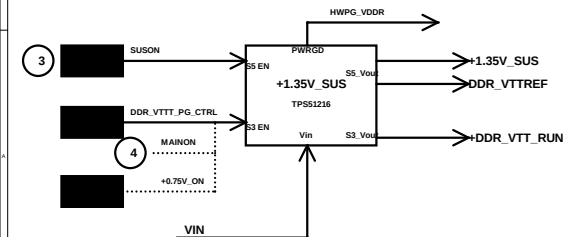
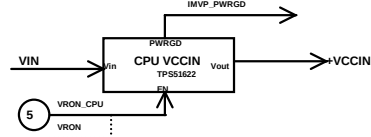
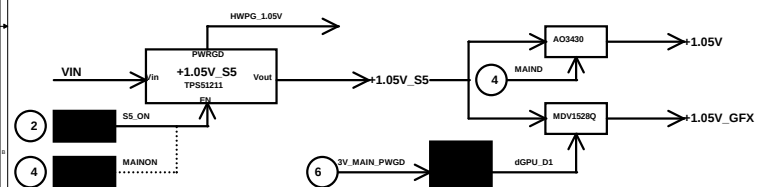
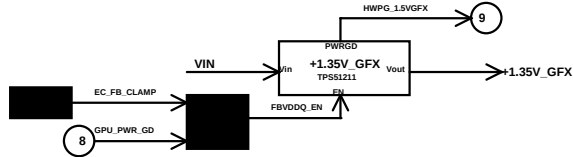
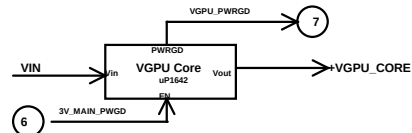
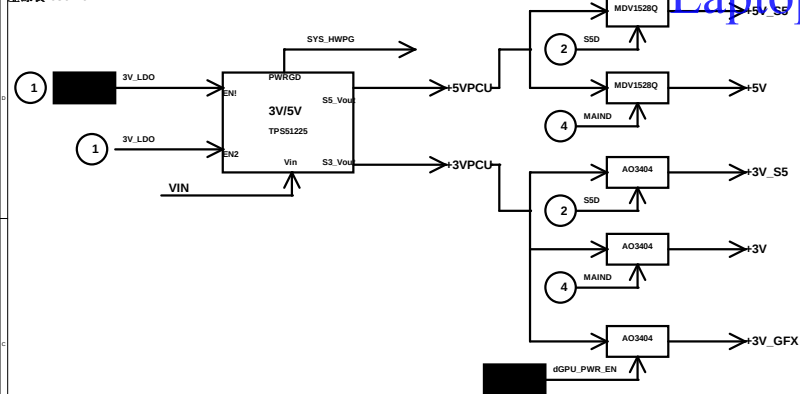
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V→+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V→+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LANBT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V_H	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PC/HGPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCD_VTT	+3.3V	LCD POWER	LVDS_VDDON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+3V_GFX	variation	External GPU POWER	DGPU_PWR_EN	S0
+1.05V_GFX	+3.3V	External GPU POWER	3V_MAIN_EN	S0
+VGPU_CORE	+1.35V	External GPU POWER	3V_MAIN_EN	S0
+1.35V_GFX	+1.05V	External GPU POWER	FBVDDQ_EN	S0



```
dGPU_OPP# EC notify HW throttle over power protect
dGPU_OTP#  VGA thntrip# => inform EC over temperature protect
```



Brodwell
ULTSIO
ITE8987



Laptopblue

[illegible]