1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,X425

08/06/2014 PROTO1A

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00330	1	SCHEM,MLB,X305	SCH	CRITICAL	
820-00138	1	PCBF,MLB,X305	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Wed Aug 6 13:00:04 2014

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00039	COMMON PARTS,MLB,X425	X425_COMMON
985-00043	DEV,MLB,X425	X425_DEVEL:ENG
639-00534	PCBA,MLB,CTO,16G-HYN,X425	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1866
639-00535	PCBA,MLB,CTO,16G-MIC,X425	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1866

X425 BOM Groups

BOM GROUP	BOM OPTIONS
X425_COMMON	ALTERNATE,COMMON,X425_COMMON1,X425_COMMON2,X425_PROGPARTS
X425_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CPUPEG:X8X8,S2_PWR:S0,SMC_SUSACK:YES
X425_COMMON2	EDP:YES,XDP,SSD_PWR_EN:GPIO,CAM_WAKE:NO,SAMCONN,APCLKRQ:ISOL,DDRREG_PGD:N,CRW_SPRT,WLAN_SW:SIL
X425_PVT	BKLT:PROD,SENSOR_NONPROD:N
X425_PROGPARTS	SMC_PROG:BASE,BOOTROM_PROG:PROTO1A,TBTROM:PROG
X425_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,X249:BOOST
X425_DEVEL:DVT	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,DBGLED
X425_DEVEL:PVT	XDP_DEBUG
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00057	1	CRW,SR1ZW,PRQ,C0,2.2,47W,4+3E,1.2,6M,BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S00058	1	CRW,SR1ZX,PRQ,C0,2.5,47W,4+3E,1.2,6M,BGA	U0500	CRITICAL	CPU_CRW:BEST
337S00059	1	CRW,SR1ZY,PRQ,C0,2.8,47W,4+3E,1.2,6M,BGA	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,QEWV,LPT-M,HM87,C2,SR199,PRQ,FCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1264	1	IC,BCM15700A2,S2 PCIE CMRA,8X8,208FCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GEMMA,96B FBGA	U4000	CRITICAL	
333S0802	16	IC,SDRAM,25NM,512MX8,DDR3L-1866,78B FBGA		CRITICAL	HYNIX_1866_S
333S0719	16	IC,SDRAM,4GBIT,DDR3-1866,V80A,78B,FBGA		CRITICAL	MICRON_1866_S
333S0802	32	IC,SDRAM,25NM,512MX8,DDR3L-1866,78B FBGA		CRITICAL	HYNIX_1866
333S0719	32	IC,SDRAM,4GBIT,DDR3-1866,V80A,78B,FBGA		CRITICAL	MICRON_1866

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1866_S	HYNIX_1866_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:MICRON_1866_S	MICRON_1866_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM:HYNIX_1866	HYNIX_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:MICRON_1866	MICRON_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00039	1	COMMON PARTS,MLB,X425	BASE	CRITICAL	BASE_BOM
985-00043	1	DEV,MLB,X425	DEVEL	CRITICAL	DEVEL_BOM

SYNC_MASTER=CLEAN_X305 SYNC_DATE=05/30/2014

PAGE TITLE
BOM Configuration

Apple Inc.

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Programmables - All builds

335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK
341S00133	1	T29,FALCON RIDGE(VXXXX)PROTO 1A,X425	U2890	CRITICAL	TBTROM:PROG

SMC

338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BLANK
341S00125	1	IC,SMC-B1,EXT (V2.24A31) PROTO 1A,X425	U5000	CRITICAL	SMC_PROG:BASE

EFI ROM

335S00007	1	IC,SERIAL FLASH,64MB,3V,WSON,6X5MM	U6100	CRITICAL	BOOTROM_BLANK:WIN
335S00006	1	IC,SERIAL FLASH,64MB,3V,WSON,6X5MM	U6100	CRITICAL	BOOTROM_BLANK:MAC
341S00131	1	IC,EFI ROM (VXXXX) PROTO 1A,X425	U6100	CRITICAL	BOOTROM_PROG:PROTO1A

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Epson
371S0713	371S0558		ALL	DDS alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S00008		ALL	Panasonic alt to TDK
376S1217	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NXP alt to Diodes
376S1089	376S1128		ALL	NXP alt to Diodes
128S0371	128S0376		ALL	Kemet alt to Sanyo
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohm alt to Vishay
138S0732	138S0715		ALL	Rohm alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX
311S0649	311S0541		ALL	ON alt to Toshiba
376S00014	376S0761		ALL	Toshiba alt to Vishay
740S00003	740S0135		ALL	AEM alt to Tyco
377S0155	377S00011		ALL	On Semi alt to Infineon
377S0184	377S00011		ALL	Infineon alt to Infineon

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

BOM Configuration

Apple Inc.

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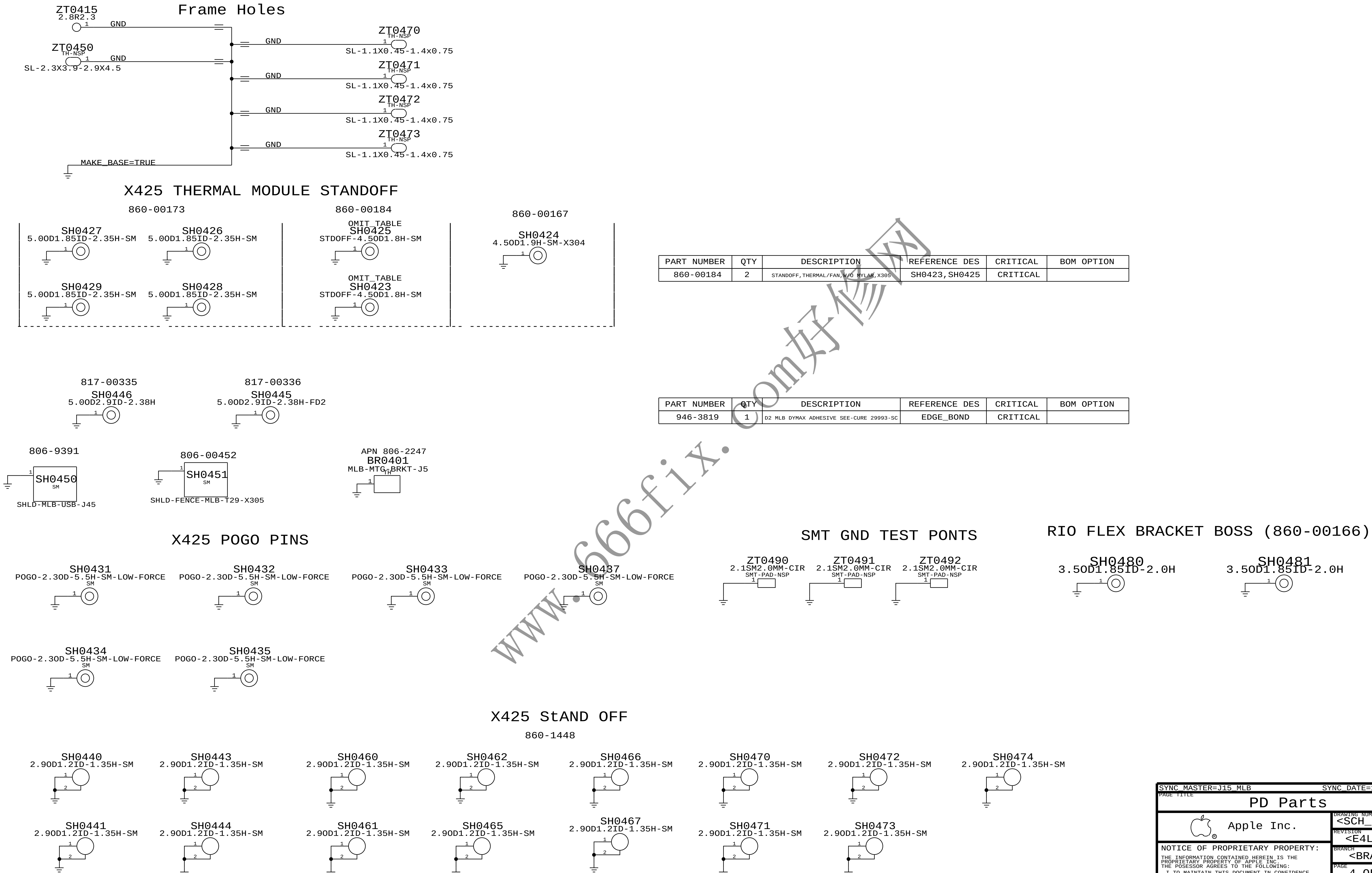

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-00184	2	STANDOFF,THERMAL/FAN,W/O MYLAR,X305	SH0423,SH0425	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

PD Parts

Apple Inc.

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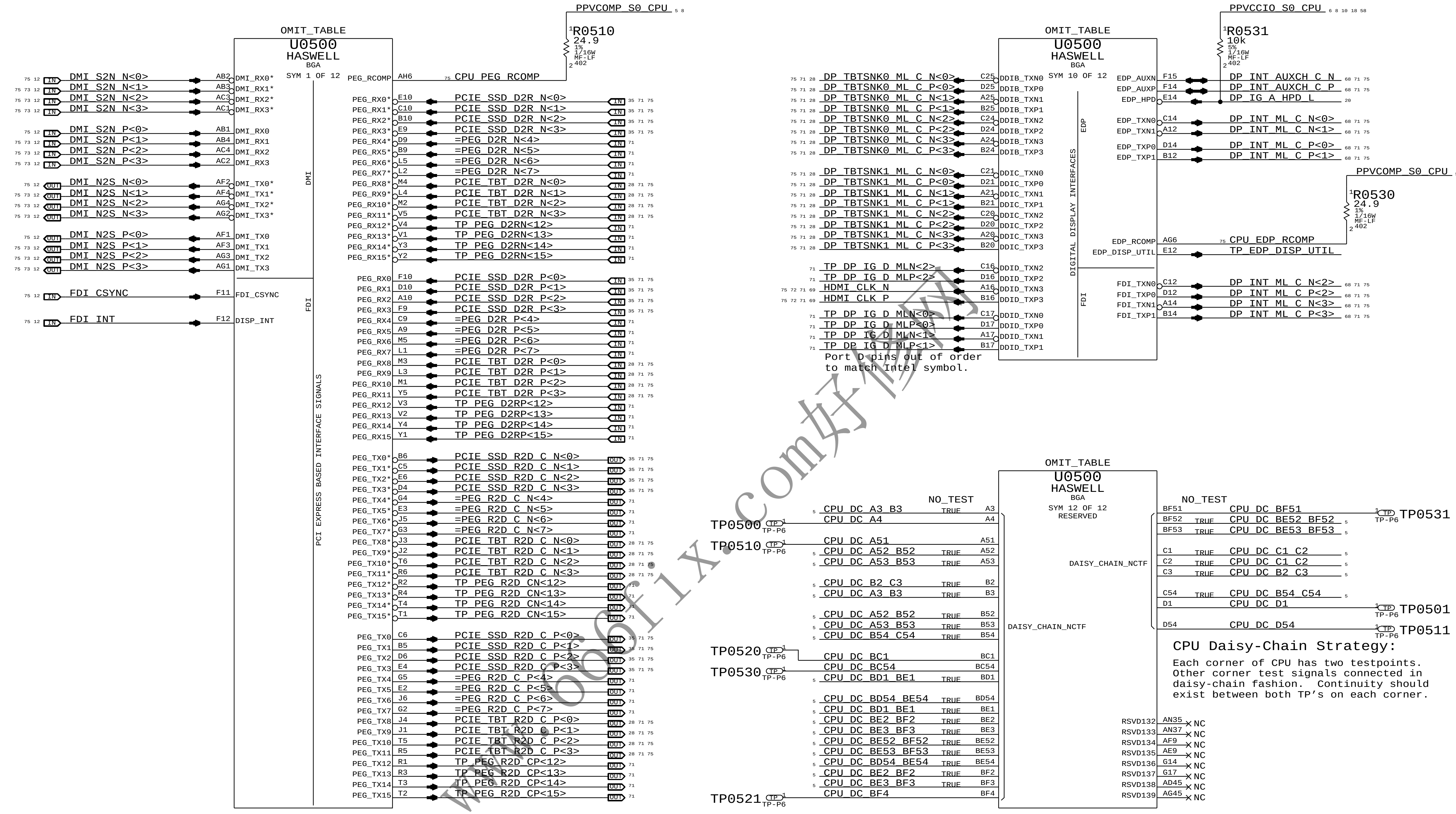
Laptopblue



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PAGE TITLE

CPU DMI/PEG/FDI/RSVD

Apple Inc.

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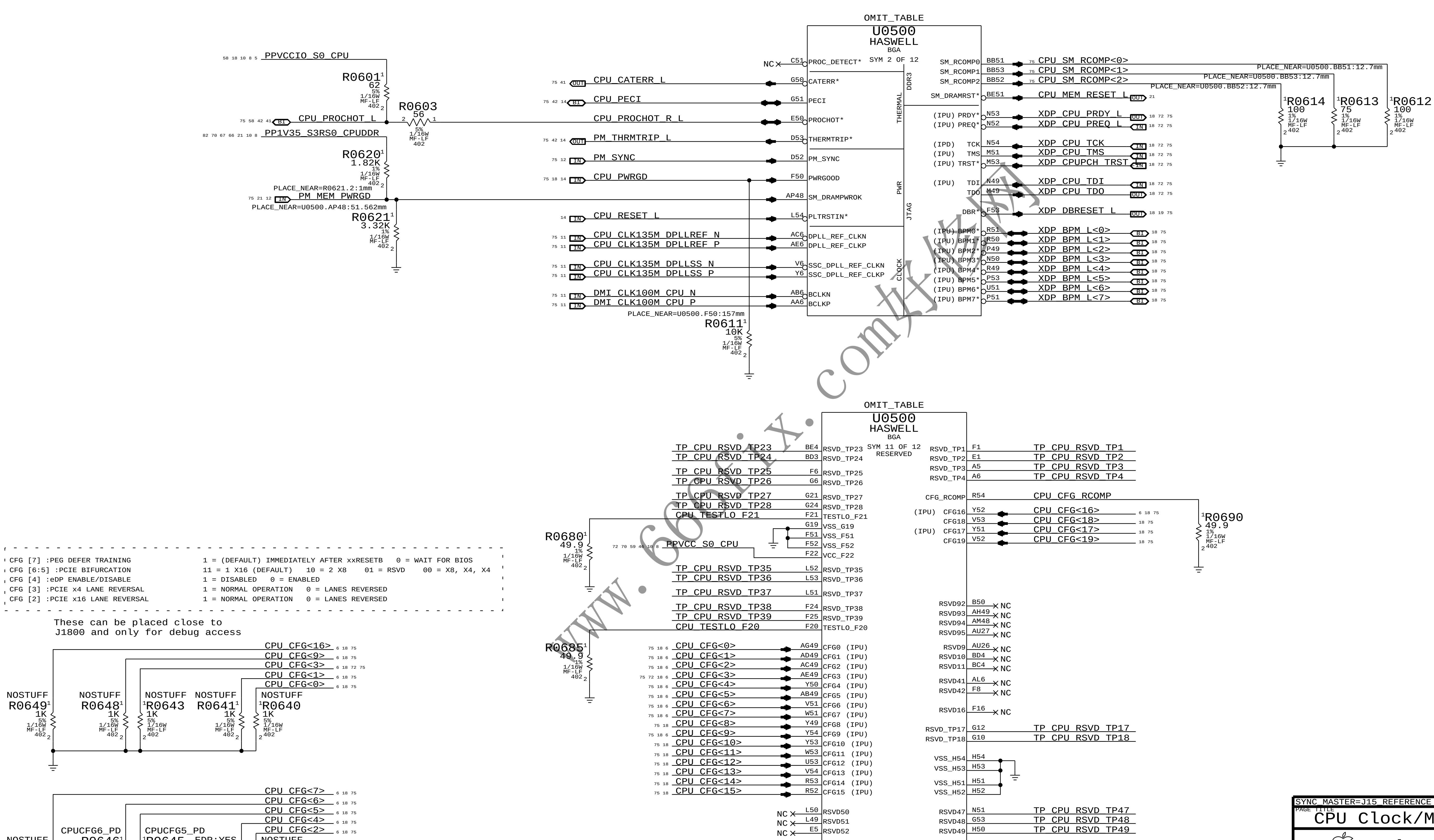

CFG [7] :PEG DEFER TRAINING — 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION — 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE — 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL — 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL — 1 = NORMAL OPERATION 0 = LANES REVERSED

These can be placed close to
J1800 and only for debug access

BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE
CPU Clock/Misc/JTAG/CFG

Apple Inc.

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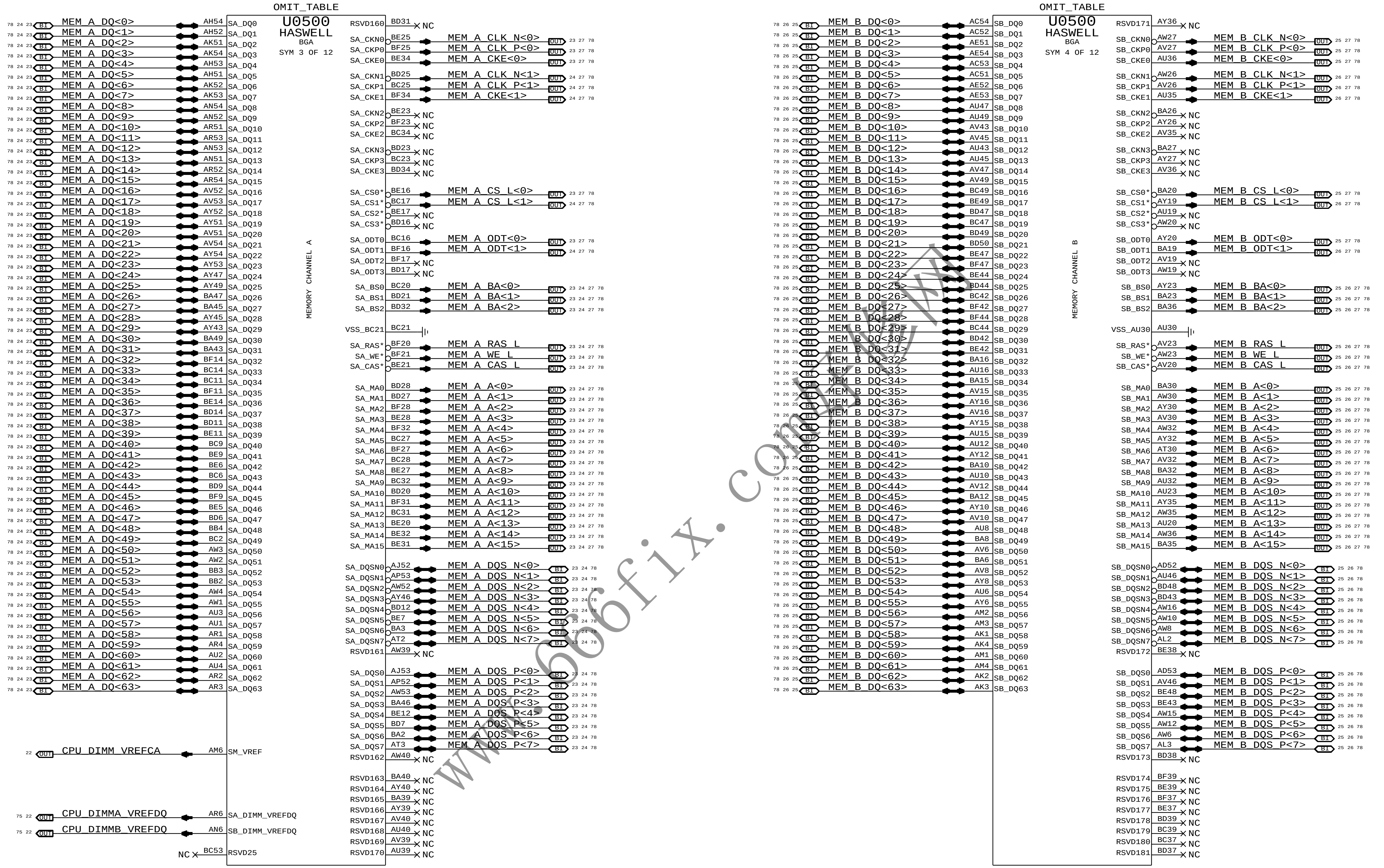

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PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

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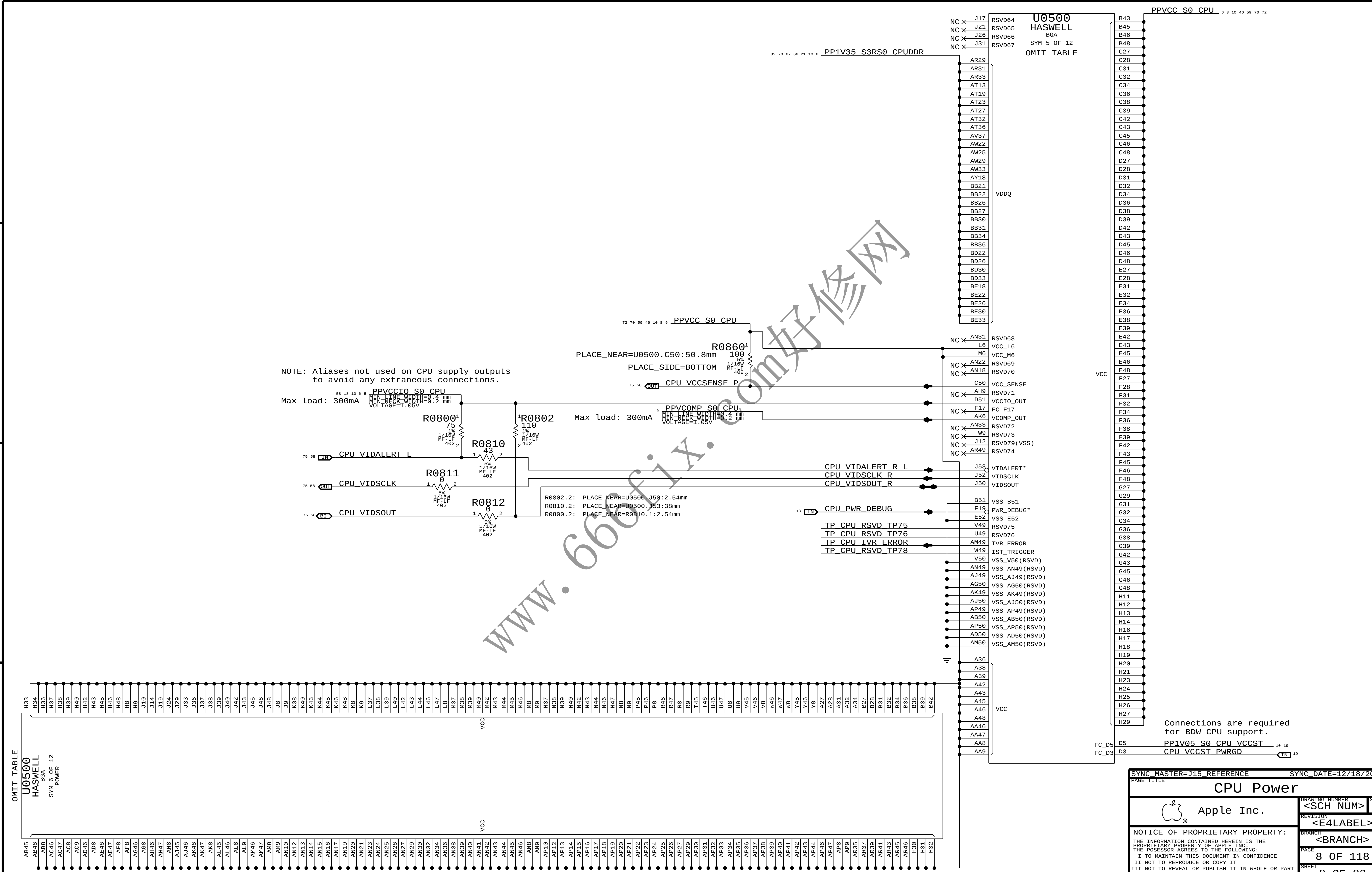

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PAGE TITLE

CPU Power

Apple Inc.

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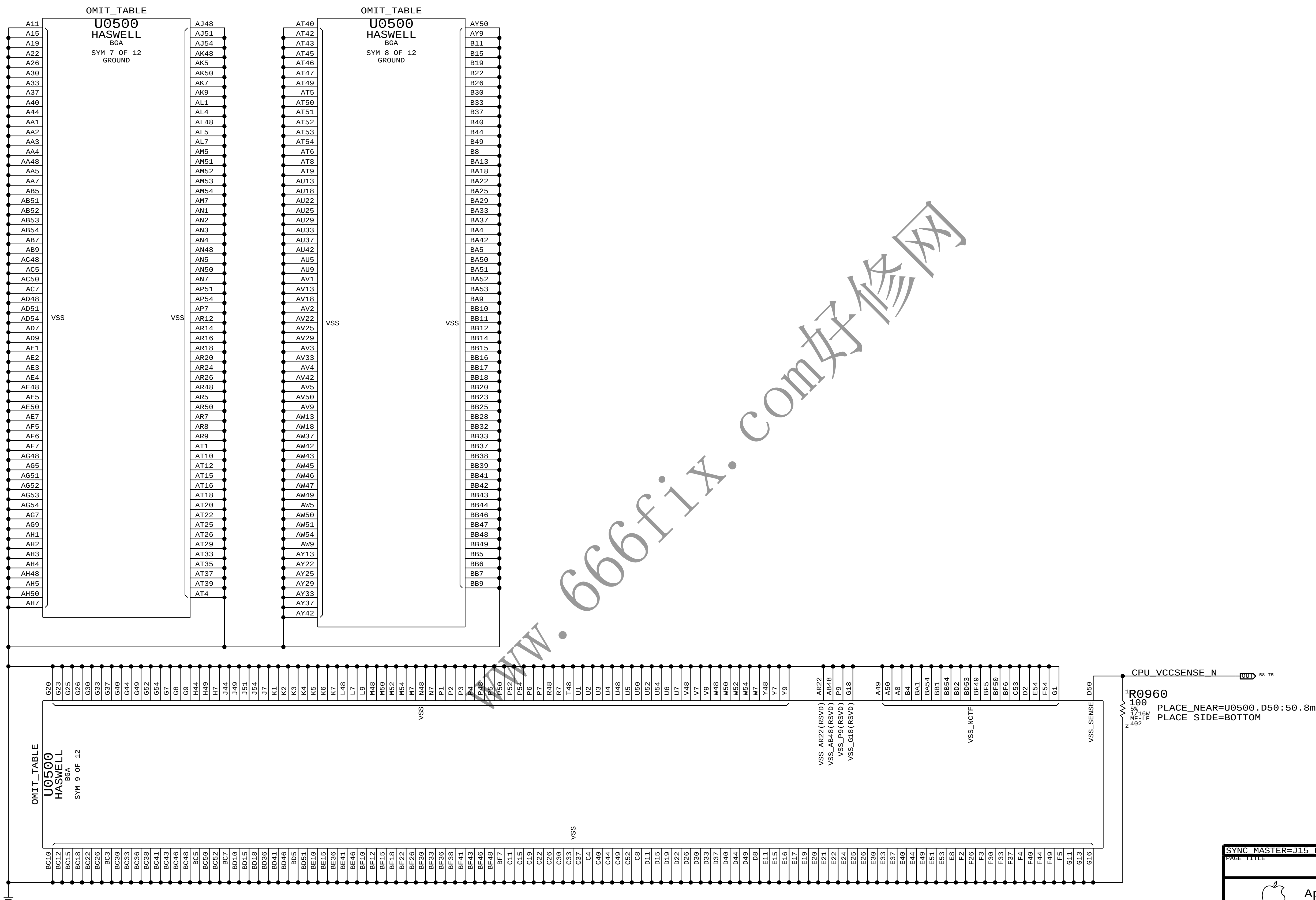

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PAGE TITLE

CPU Ground

Apple Inc.

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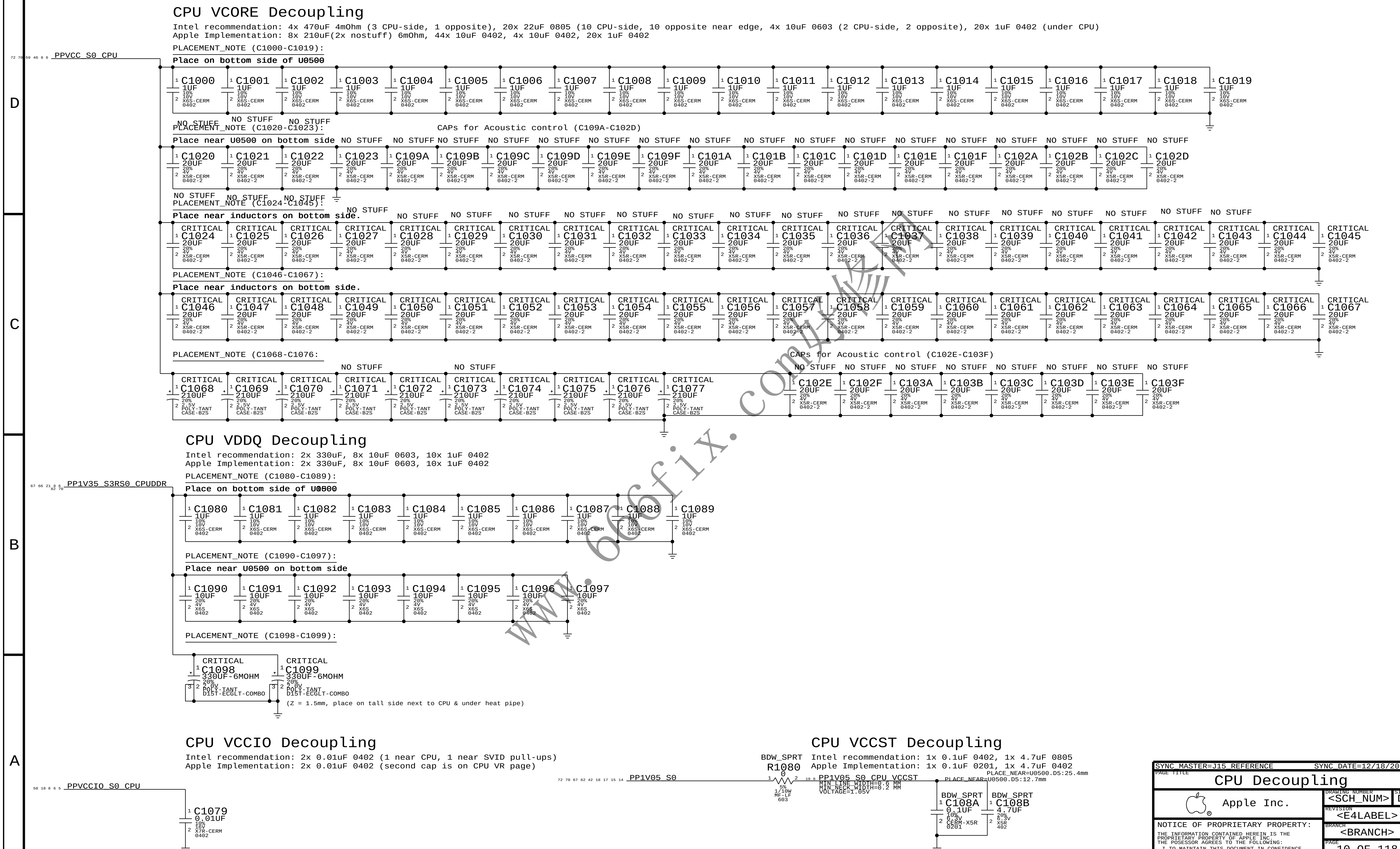

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: CPU Decoupling

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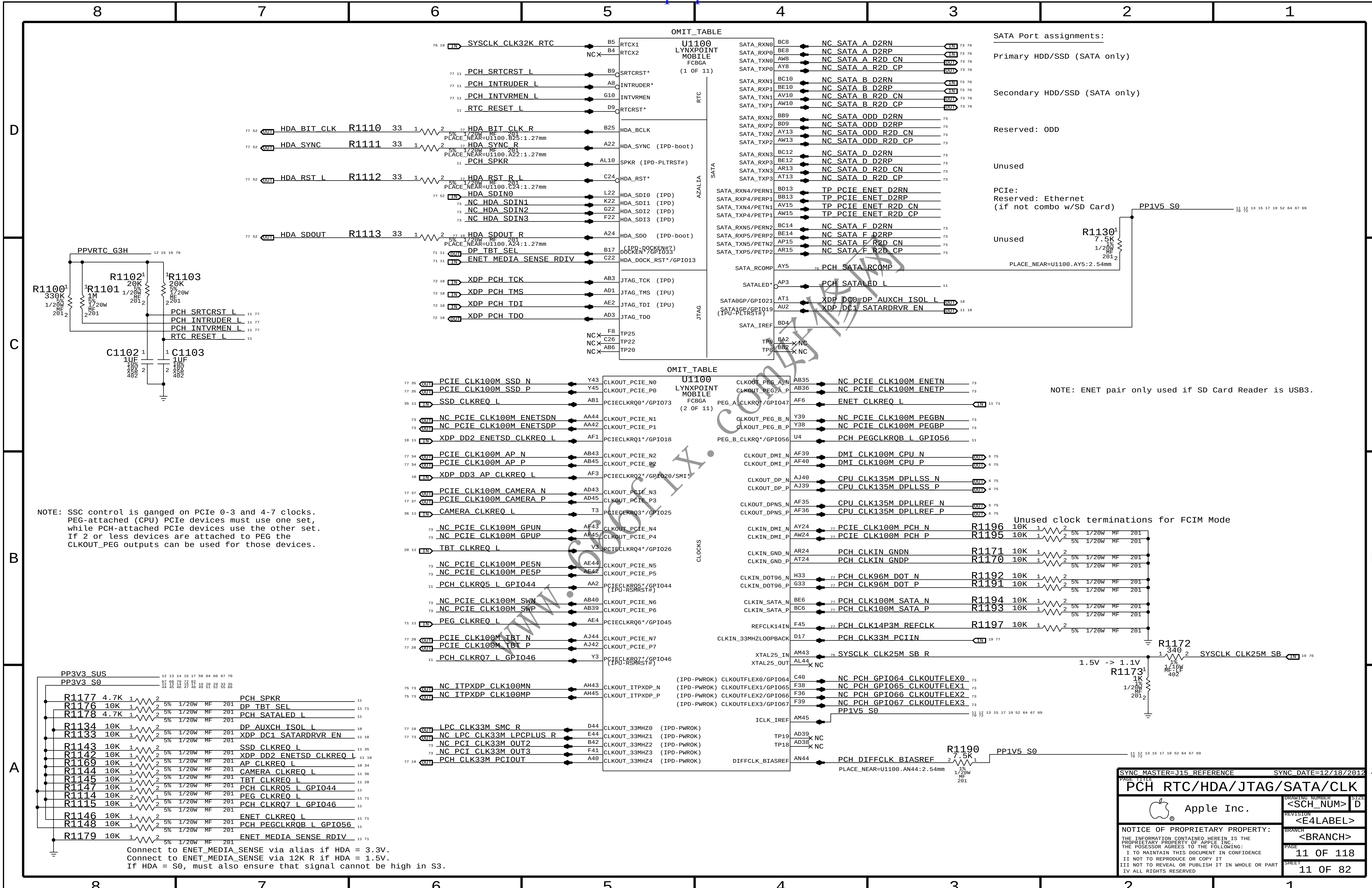
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(1 OF 11)
RTC
AZALIA
SATA
JTAG
SYSCLK_CLK32K_RTC
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
HDA_BIT_CLK
HDA_SYNC
HDA_RST_L
HDA_SDOUT
R1110 33
R1111 33
R1112 33
R1113 33
HDA_BIT_CLK_R
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
NC_HDA_SDIN1
NC_HDA_SDIN2
NC_HDA_SDIN3
HDA_SDOUT_R
DP_TBT_SEL
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
PPVRTC_G3H
R1100 330K
R1101 1M
R1102 20K
R1103 20K
C1102 1UF
C1103 1UF
NC_SATA_A_D2RN
NC_SATA_A_D2RP
NC_SATA_A_R2D_CN
NC_SATA_A_R2D_CP
NC_SATA_B_D2RN
NC_SATA_B_D2RP
NC_SATA_B_R2D_CN
NC_SATA_B_R2D_CP
NC_SATA_ODD_D2RN
NC_SATA_ODD_D2RP
NC_SATA_ODD_R2D_CN
NC_SATA_ODD_R2D_CP
NC_SATA_D_D2RN
NC_SATA_D_D2RP
NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP
TP_PCIE_ENET_D2RN
TP_PCIE_ENET_D2RP
TP_PCIE_ENET_R2D_CN
TP_PCIE_ENET_R2D_CP
NC_SATA_F_D2RN
NC_SATA_F_D2RP
NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP
PCH_SATA_RCOMP
PCH_SATALED_L
XDP_DC0_DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN
SATA Port assignments:
Primary HDD/SSD (SATA only)
Secondary HDD/SSD (SATA only)
Reserved: ODD
Unused
PCIe:
Reserved: Ethernet
(if not combo w/SD Card)
Unused
PP1V5_S0
R1130 7.5K
PLACE_NEAR=U1100.AY5:2.54mm
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(2 OF 11)
CLOCKS
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
SSD_CLKREQ_L
NC_PCIE_CLK100M_ENETSDN
NC_PCIE_CLK100M_ENETSDP
XDP_DD2_ENETSD_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
XDP_DD3_AP_CLKREQ_L
PCIE_CLK100M_CAMERA_N
PCIE_CLK100M_CAMERA_P
CAMERA_CLKREQ_L
NC_PCIE_CLK100M_GPUN
NC_PCIE_CLK100M_GPUP
TBT_CLKREQ_L
NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P
PCH_CLKRQ5_L_GPIO44
NC_PCIE_CLK100M_SWN
NC_PCIE_CLK100M_SWP
PEG_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
PCH_CLKRQ7_L_GPIO46
NC_ITPXDP_CLK100MN
NC_ITPXDP_CLK100MP
LPC_CLK33M_SMC_R
NC_LPC_CLK33M_LPCPLUS_R
NC_PCI_CLK33M_OUT2
NC_PCI_CLK33M_OUT3
PCH_CLK33M_PCIOUT
NC_PCIE_CLK100M_ENETN
NC_PCIE_CLK100M_ENETP
ENET_CLKREQ_L
NC_PCIE_CLK100M_PEGBN
NC_PCIE_CLK100M_PEGBP
PCH_PEGCLKRQB_L_GPIO56
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
CPU_CLK135M_DPLLSS_N
CPU_CLK135M_DPLLSS_P
CPU_CLK135M_DPLLREF_N
CPU_CLK135M_DPLLREF_P
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
PCH_CLKIN_GNDN
PCH_CLKIN_GNDP
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
SYSCLK_CLK25M_SB_R
NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3
PP1V5_S0
PCH_DIFFCLK_BIASREF
R1190 7.5K
PLACE_NEAR=U1100.AN44:2.54mm
NOTE: ENET pair only used if SD Card Reader is USB3.
Unused clock terminations for FCIM Mode
R1196 10K
R1195 10K
R1171 10K
R1170 10K
R1192 10K
R1191 10K
R1194 10K
R1193 10K
R1197 10K
R1172 340
SYSCLK_CLK25M_SB
1.5V -> 1.1V
R1173 1K
NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.
PP3V3_SUS
PP3V3_S0
R1177 4.7K PCH_SPKR
R1176 10K DP_TBT_SEL
R1178 4.7K PCH_SATALED_L
R1134 10K DP_AUXCH_ISOL_L
R1133 10K XDP_DC1_SATARDRVR_EN
R1143 10K SSD_CLKREQ_L
R1142 10K XDP_DD2_ENETSD_CLKREQ_L
R1169 10K AP_CLKREQ_L
R1144 10K CAMERA_CLKREQ_L
R1145 10K TBT_CLKREQ_L
R1147 10K PCH_CLKRQ5_L_GPIO44
R1114 10K PEG_CLKREQ_L
R1115 10K PCH_CLKRQ7_L_GPIO46
R1146 10K ENET_CLKREQ_L
R1148 10K PCH_PEGCLKRQB_L_GPIO56
R1179 10K ENET_MEDIA_SENSE_RDIV
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
SYNC_MASTER=J15_REFERENCE
SYNC_DATE=12/18/2012
PCH RTC/HDA/JTAG/SATA/CLK
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<SCH_NUM>
D
<E4LABEL>
<BRANCH>
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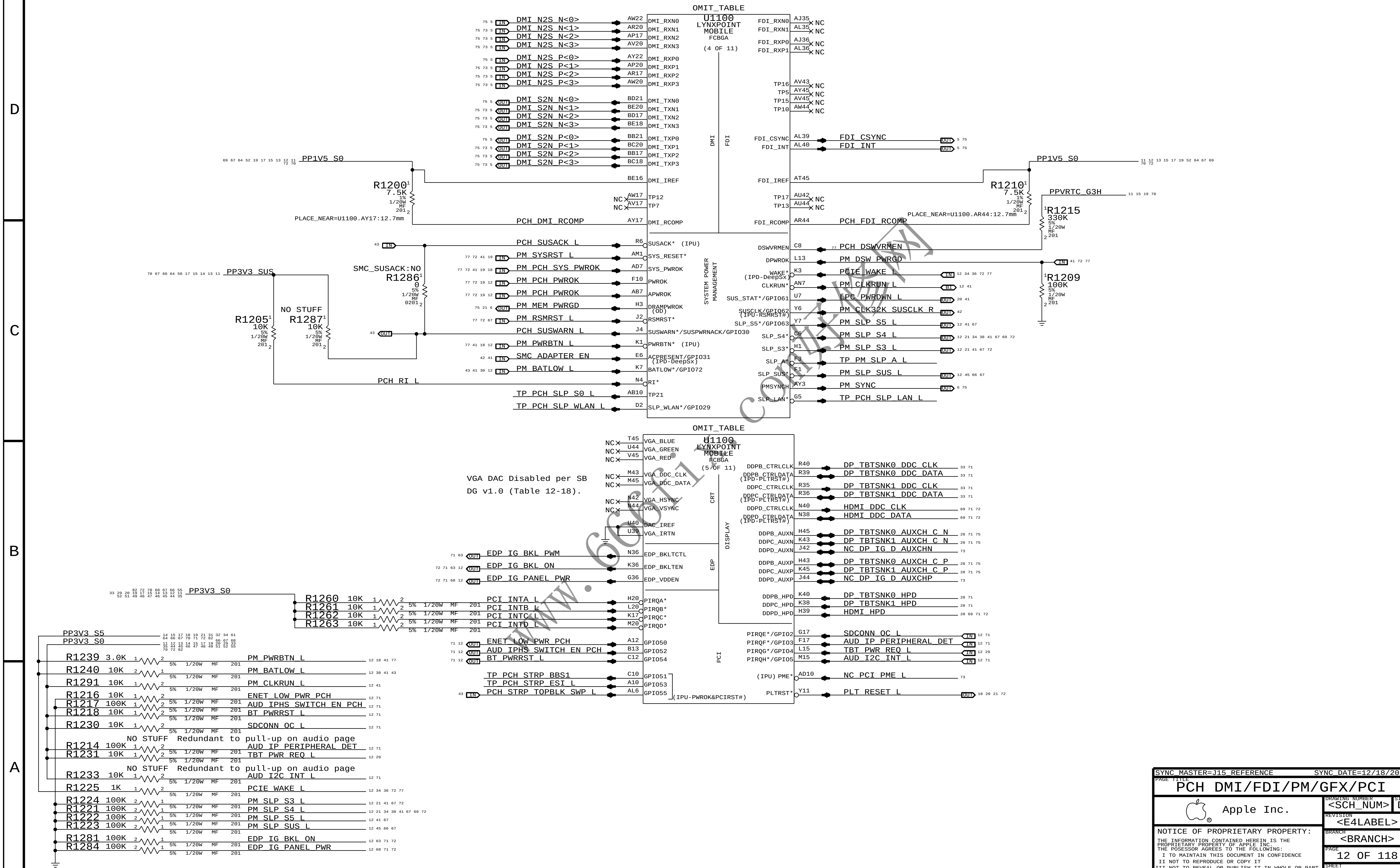

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PAGE TITLE

PCH DMI/FDI/PM/GFX/PCI

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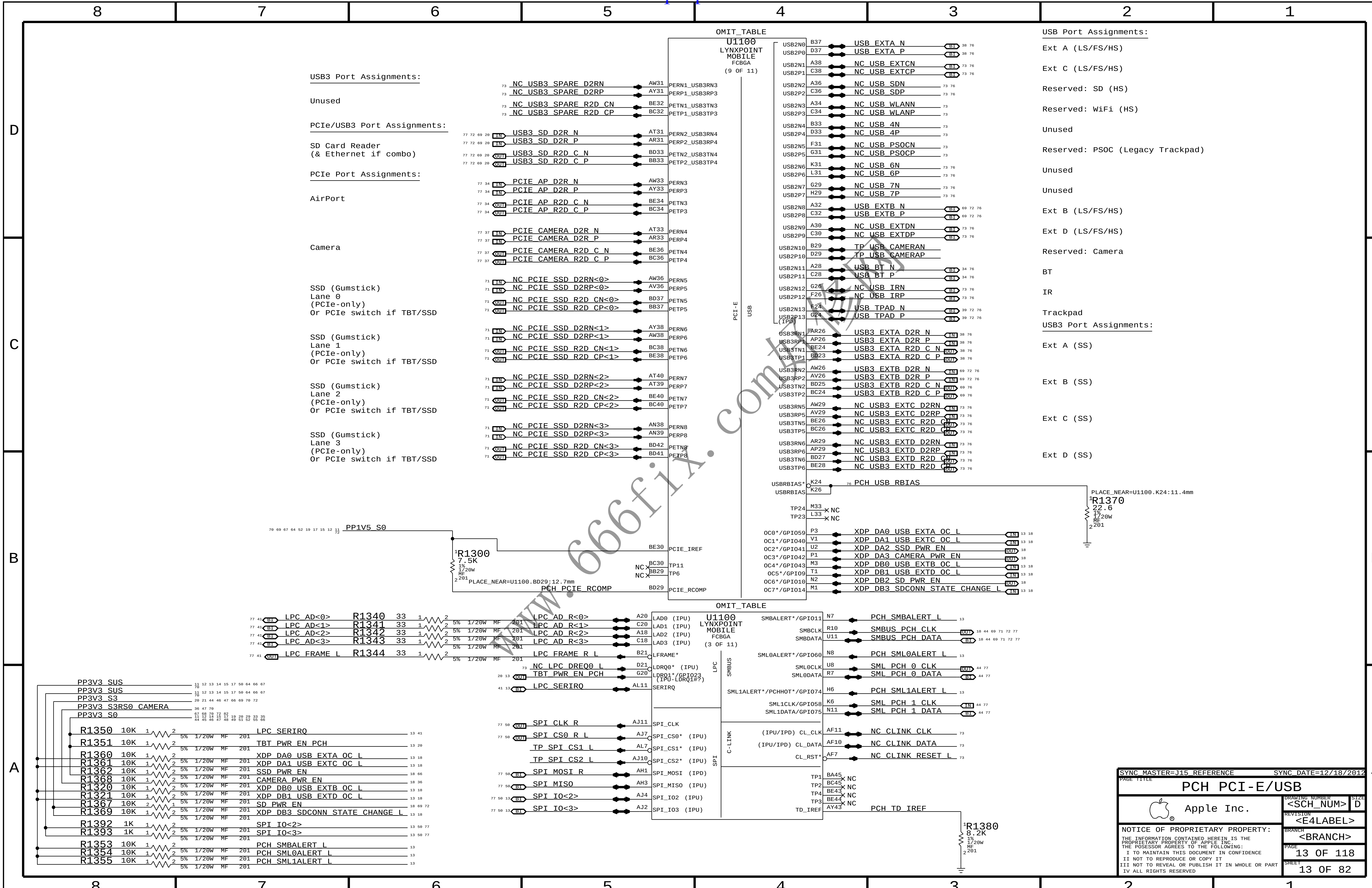
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D C B A
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(9 OF 11)
PCI-E
USB
USB3 Port Assignments:
Unused
PCIe/USB3 Port Assignments:
SD Card Reader
(& Ethernet if combo)
PCIe Port Assignments:
AirPort
Camera
SSD (Gumstick)
Lane 0
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 1
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 2
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 3
(PCIe-only)
Or PCIe switch if TBT/SSD
NC_USB3_SPARE_D2RN AW31 PERN1_USB3RN3
NC_USB3_SPARE_D2RP AY31 PERP1_USB3RP3
NC_USB3_SPARE_R2D_CN BE32 PETN1_USB3TN3
NC_USB3_SPARE_R2D_CP BC32 PETP1_USB3TP3
USB3_SD_D2R_N AT31 PERN2_USB3RN4
USB3_SD_D2R_P AR31 PERP2_USB3RP4
USB3_SD_R2D_C_N BD33 PETN2_USB3TN4
USB3_SD_R2D_C_P BB33 PETP2_USB3TP4
PCIE_AP_D2R_N AW33 PERN3
PCIE_AP_D2R_P AY33 PERP3
PCIE_AP_R2D_C_N BE34 PETN3
PCIE_AP_R2D_C_P BC34 PETP3
PCIE_CAMERA_D2R_N AT33 PERN4
PCIE_CAMERA_D2R_P AR33 PERP4
PCIE_CAMERA_R2D_C_N BE36 PETN4
PCIE_CAMERA_R2D_C_P BC36 PETP4
NC_PCIE_SSD_D2RN<0> AW36 PERN5
NC_PCIE_SSD_D2RP<0> AV36 PERP5
NC_PCIE_SSD_R2D_CN<0> BD37 PETN5
NC_PCIE_SSD_R2D_CP<0> BB37 PETP5
NC_PCIE_SSD_D2RN<1> AY38 PERN6
NC_PCIE_SSD_D2RP<1> AW38 PERP6
NC_PCIE_SSD_R2D_CN<1> BC38 PETN6
NC_PCIE_SSD_R2D_CP<1> BE38 PETP6
NC_PCIE_SSD_D2RN<2> AT40 PERN7
NC_PCIE_SSD_D2RP<2> AT39 PERP7
NC_PCIE_SSD_R2D_CN<2> BE40 PETN7
NC_PCIE_SSD_R2D_CP<2> BC40 PETP7
NC_PCIE_SSD_D2RN<3> AN38 PERN8
NC_PCIE_SSD_D2RP<3> AN39 PERP8
NC_PCIE_SSD_R2D_CN<3> BD42 PETN8
NC_PCIE_SSD_R2D_CP<3> BD41 PETP8
PP1V5_S0
R1300 7.5K 1% 1/20W MF 201
PLACE_NEAR=U1100.BD29:12.7mm
PCH_PCIE_RCOMP BD29 PCIE_RCOMP
BE30 PCIE_IREF
NC BC30 TP11
NC BB29 TP6
USB2N0 B37 USB_EXTA_N
USB2P0 D37 USB_EXTA_P
USB2N1 A38 NC_USB_EXTCN
USB2P1 C38 NC_USB_EXTCP
USB2N2 A36 NC_USB_SDN
USB2P2 C36 NC_USB_SDP
USB2N3 A34 NC_USB_WLANN
USB2P3 C34 NC_USB_WLANP
USB2N4 B33 NC_USB_4N
USB2P4 D33 NC_USB_4P
USB2N5 F31 NC_USB_PSOCN
USB2P5 G31 NC_USB_PSOCP
USB2N6 K31 NC_USB_6N
USB2P6 L31 NC_USB_6P
USB2N7 G29 NC_USB_7N
USB2P7 H29 NC_USB_7P
USB2N8 A32 USB_EXTB_N
USB2P8 C32 USB_EXTB_P
USB2N9 A30 NC_USB_EXTDN
USB2P9 C30 NC_USB_EXTDP
USB2N10 B29 TP_USB_CAMERAN
USB2P10 D29 TP_USB_CAMERAP
USB2N11 A28 USB_BT_N
USB2P11 C28 USB_BT_P
USB2N12 G26 NC_USB_IRN
USB2P12 F26 NC_USB_IRP
USB2N13 F24 USB_TPAD_N
USB2P13 G24 USB_TPAD_P
(IPD)
USB3RN1 AR26 USB3_EXTA_D2R_N
USB3RP1 AP26 USB3_EXTA_D2R_P
USB3TN1 BE24 USB3_EXTA_R2D_C_N
USB3TP1 BD23 USB3_EXTA_R2D_C_P
USB3RN2 AW26 USB3_EXTB_D2R_N
USB3RP2 AV26 USB3_EXTB_D2R_P
USB3TN2 BD25 USB3_EXTB_R2D_C_N
USB3TP2 BC24 USB3_EXTB_R2D_C_P
USB3RN5 AW29 NC_USB3_EXTC_D2RN
USB3RP5 AV29 NC_USB3_EXTC_D2RP
USB3TN5 BE26 NC_USB3_EXTC_R2D_CN
USB3TP5 BC26 NC_USB3_EXTC_R2D_CP
USB3RN6 AR29 NC_USB3_EXTD_D2RN
USB3RP6 AP29 NC_USB3_EXTD_D2RP
USB3TN6 BD27 NC_USB3_EXTD_R2D_CN
USB3TP6 BE28 NC_USB3_EXTD_R2D_CP
USBRBIAS* K24 PCH_USB_RBIAS
USBRBIAS K26
TP24 M33 NC
TP23 L33 NC
PLACE_NEAR=U1100.K24:11.4mm
R1370 22.6 1% 1/20W MF 201
OC0*/GPIO59 P3 XDP_DA0_USB_EXTA_OC_L
OC1*/GPIO40 V1 XDP_DA1_USB_EXTC_OC_L
OC2*/GPIO41 U2 XDP_DA2_SSD_PWR_EN
OC3*/GPIO42 P1 XDP_DA3_CAMERA_PWR_EN
OC4*/GPIO43 M3 XDP_DB0_USB_EXTB_OC_L
OC5*/GPIO9 T1 XDP_DB1_USB_EXTD_OC_L
OC6*/GPIO10 N2 XDP_DB2_SD_PWR_EN
OC7*/GPIO14 M1 XDP_DB3_SDCONN_STATE_CHANGE_L
USB Port Assignments:
Ext A (LS/FS/HS)
Ext C (LS/FS/HS)
Reserved: SD (HS)
Reserved: WiFi (HS)
Unused
Reserved: PSOC (Legacy Trackpad)
Unused
Unused
Ext B (LS/FS/HS)
Ext D (LS/FS/HS)
Reserved: Camera
BT
IR
Trackpad
USB3 Port Assignments:
Ext A (SS)
Ext B (SS)
Ext C (SS)
Ext D (SS)
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(3 OF 11)
LPC SMBUS C-LINK SPI
LPC_AD<0> R1340 33 5% 1/20W MF 201 LPC_AD_R<0> A20 LAD0 (IPU)
LPC_AD<1> R1341 33 5% 1/20W MF 201 LPC_AD_R<1> C20 LAD1 (IPU)
LPC_AD<2> R1342 33 5% 1/20W MF 201 LPC_AD_R<2> A18 LAD2 (IPU)
LPC_AD<3> R1343 33 5% 1/20W MF 201 LPC_AD_R<3> C18 LAD3 (IPU)
LPC_FRAME_L R1344 33 5% 1/20W MF 201 LPC_FRAME_R_L B21 LFRAME*
NC_LPC_DREQ0_L D21 LDRQ0* (IPU)
TBT_PWR_EN_PCH G20 LDRQ1*/GPIO23 (IPU-LDRQ1#?)
LPC_SERIRQ AL11 SERIRQ
SPI_CLK_R AJ11 SPI_CLK
SPI_CS0_R_L AJ7 SPI_CS0* (IPU)
TP_SPI_CS1_L AL7 SPI_CS1* (IPU)
TP_SPI_CS2_L AJ10 SPI_CS2* (IPU)
SPI_MOSI_R AH1 SPI_MOSI (IPD)
SPI_MISO AH3 SPI_MISO (IPU)
SPI_IO<2> AJ4 SPI_IO2 (IPU)
SPI_IO<3> AJ2 SPI_IO3 (IPU)
SMBALERT*/GPIO11 N7 PCH_SMBALERT_L
SMBCLK R10 SMBUS_PCH_CLK
SMBDATA U11 SMBUS_PCH_DATA
SML0ALERT*/GPIO60 N8 PCH_SML0ALERT_L
SML0CLK U8 SML_PCH_0_CLK
SML0DATA R7 SML_PCH_0_DATA
SML1ALERT*/PCHHOT*/GPIO74 H6 PCH_SML1ALERT_L
SML1CLK/GPIO58 K6 SML_PCH_1_CLK
SML1DATA/GPIO75 N11 SML_PCH_1_DATA
(IPU/IPD) CL_CLK AF11 NC_CLINK_CLK
(IPU/IPD) CL_DATA AF10 NC_CLINK_DATA
CL_RST* AF7 NC_CLINK_RESET_L
TP1 BA45 NC
TP2 BC45 NC
TP4 BE43 NC
TP3 BE44 NC
TD_IREF AY43 PCH_TD_IREF
R1380 8.2K 1% 1/20W MF 201
PP3V3_SUS
PP3V3_SUS
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0
R1350 10K 5% 1/20W MF 201 LPC_SERIRQ
R1351 10K 5% 1/20W MF 201 TBT_PWR_EN_PCH
R1360 10K 5% 1/20W MF 201 XDP_DA0_USB_EXTA_OC_L
R1361 10K 5% 1/20W MF 201 XDP_DA1_USB_EXTC_OC_L
R1362 10K 5% 1/20W MF 201 SSD_PWR_EN
R1368 10K 5% 1/20W MF 201 CAMERA_PWR_EN
R1320 10K 5% 1/20W MF 201 XDP_DB0_USB_EXTB_OC_L
R1321 10K 5% 1/20W MF 201 XDP_DB1_USB_EXTD_OC_L
R1367 10K 5% 1/20W MF 201 SD_PWR_EN
R1369 10K 5% 1/20W MF 201 XDP_DB3_SDCONN_STATE_CHANGE_L
R1392 1K 5% 1/20W MF 201 SPI_IO<2>
R1393 1K 5% 1/20W MF 201 SPI_IO<3>
R1353 10K 5% 1/20W MF 201 PCH_SMBALERT_L
R1354 10K 5% 1/20W MF 201 PCH_SML0ALERT_L
R1355 10K 5% 1/20W MF 201 PCH_SML1ALERT_L
SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012
PAGE TITLE
PCH PCI-E/USB
DRAWING NUMBER <SCH_NUM> SIZE D
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BRANCH <BRANCH>
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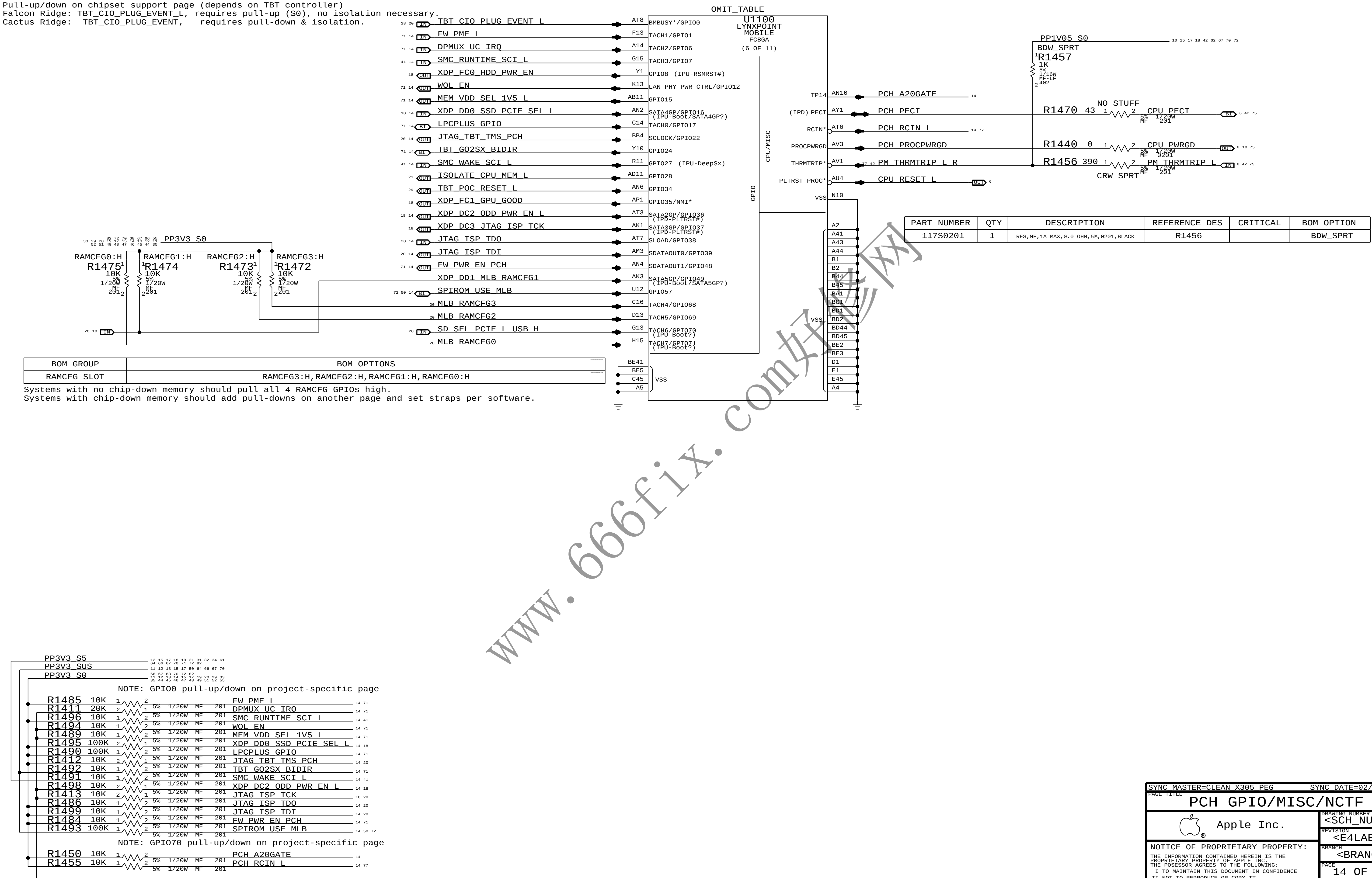
Pull-up/down on chipset support page (depends on TBT controller)
Falcon Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	R1456		BDW_SPRT

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE
PCH GPIO/MISC/NCTF

Apple Inc.

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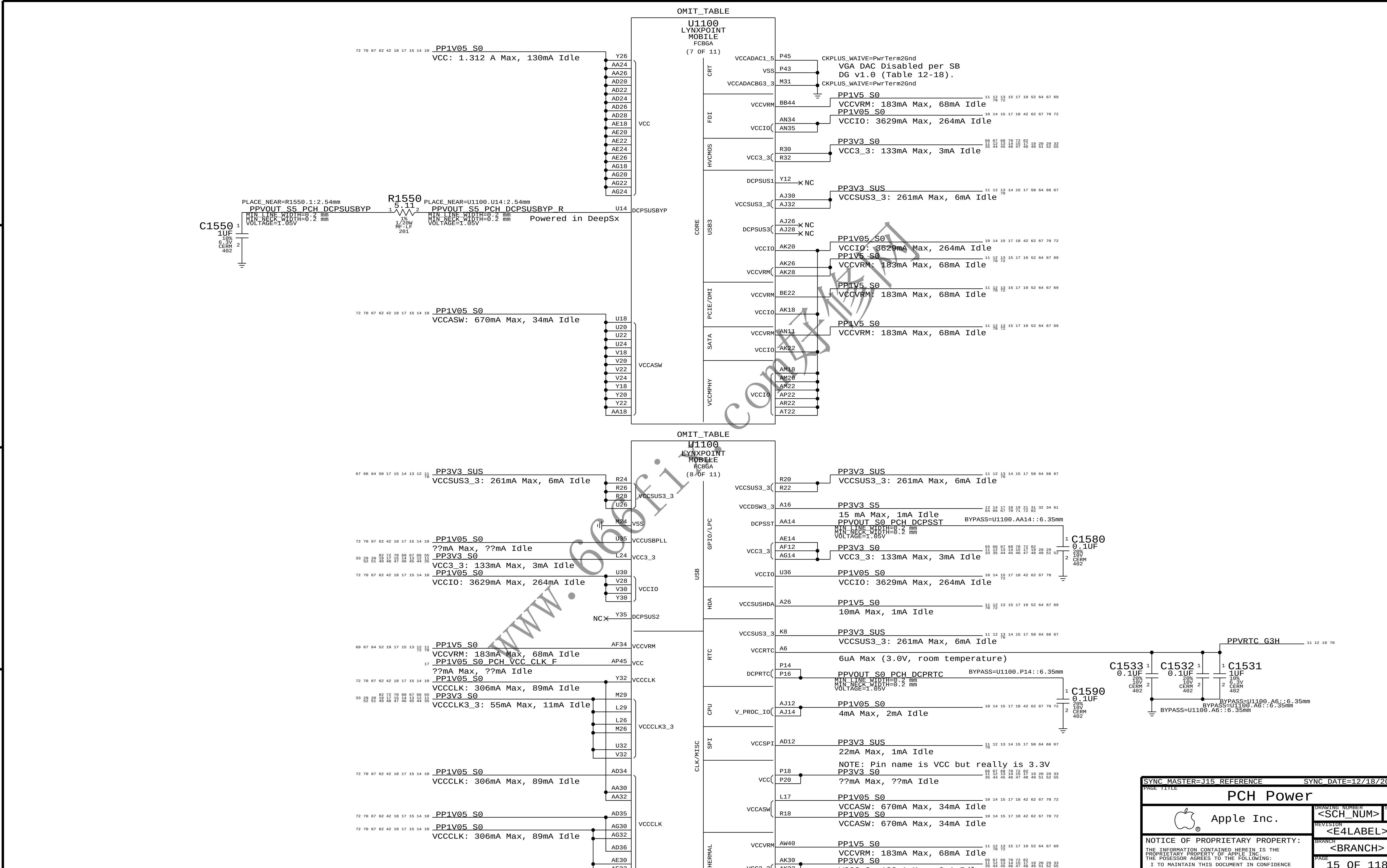

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

PCH Power

DRAWING NUMBER <SCH_NUM> SIZE D

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REVISION <E4LABEL>

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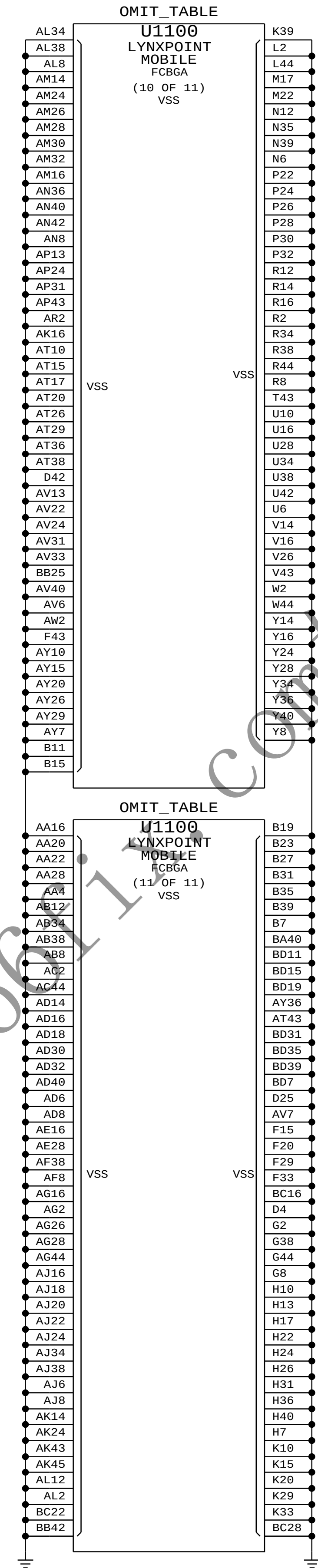

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

PCH Grounds

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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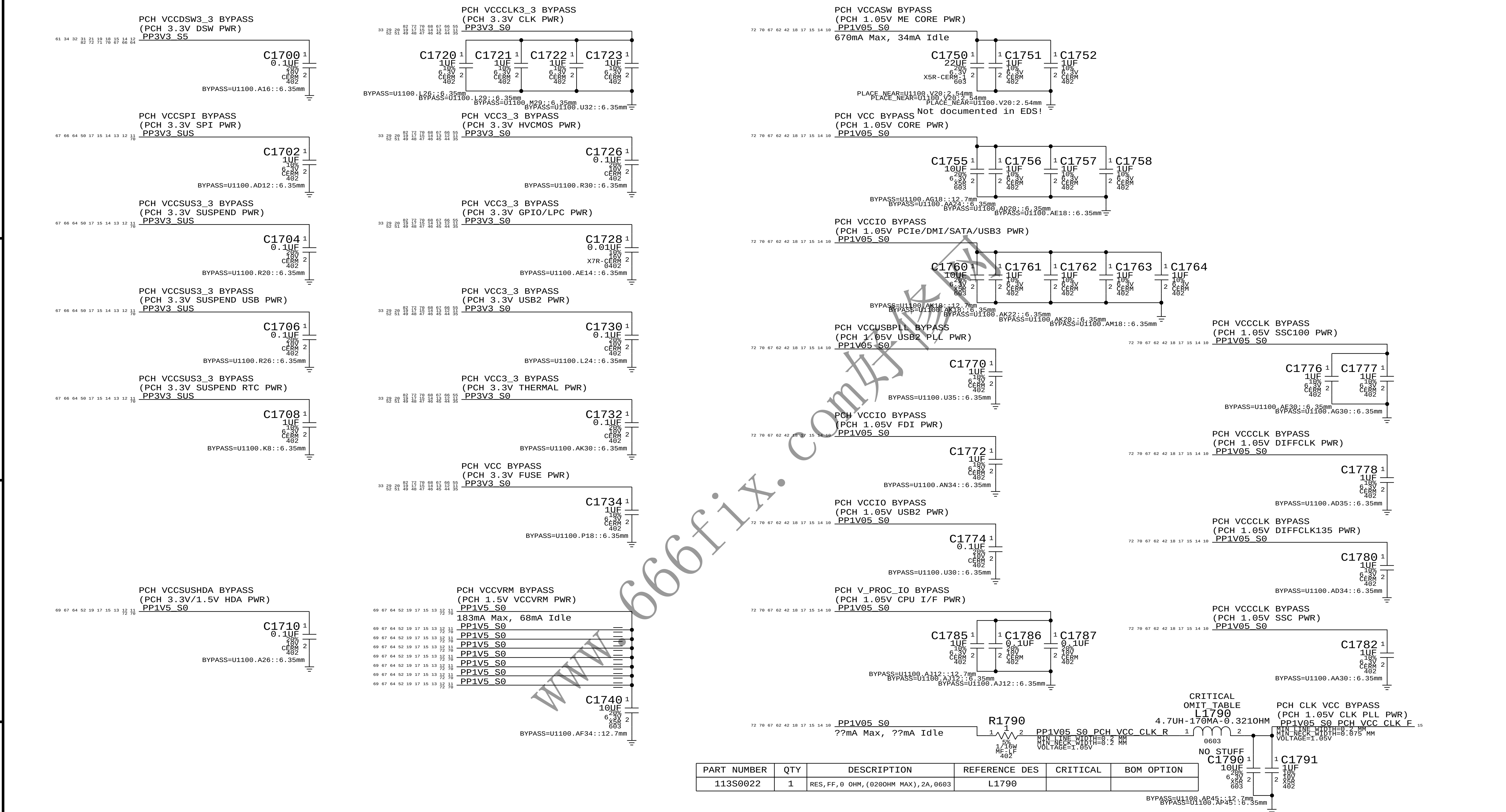

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020HM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

PCH DECOUPLING

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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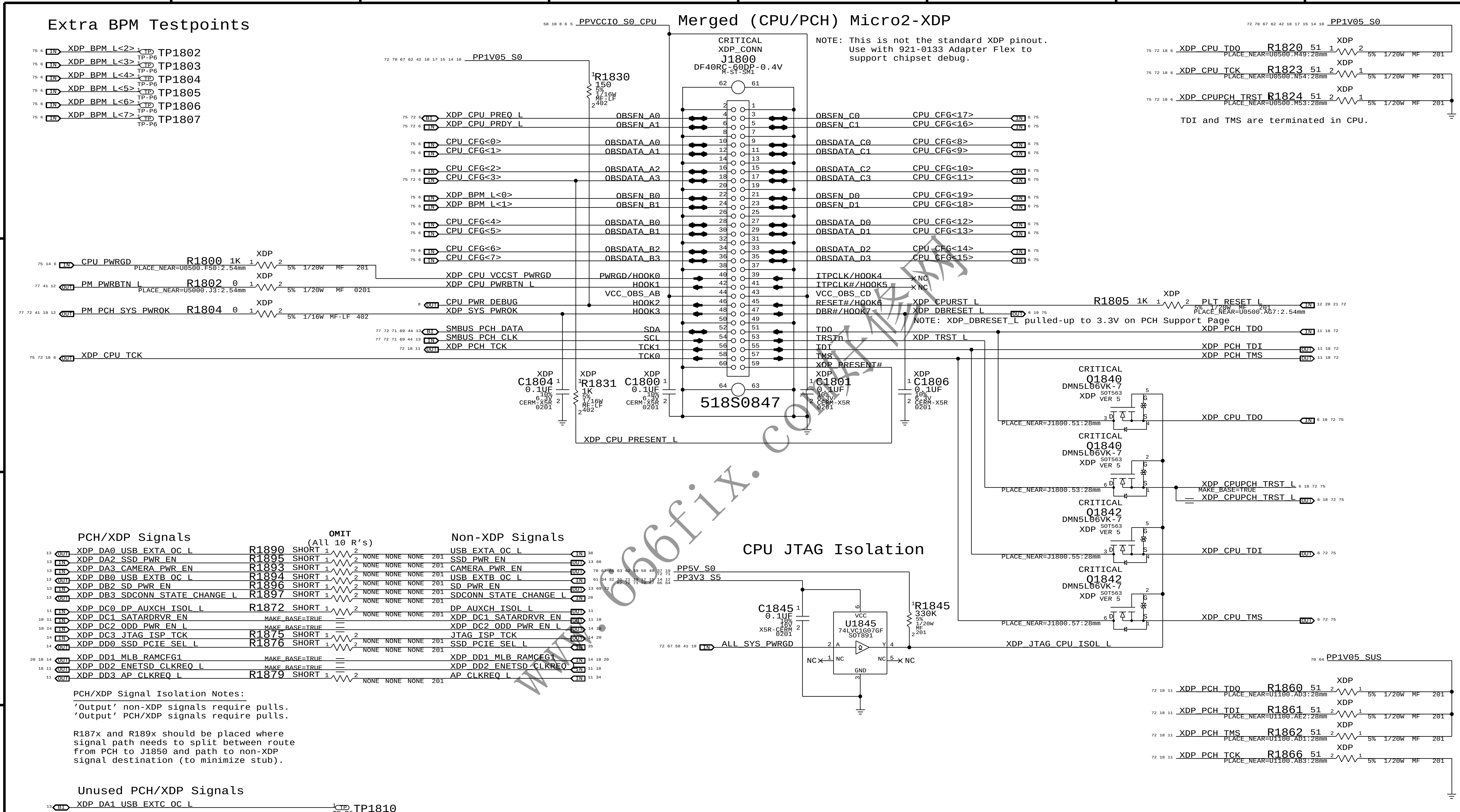


SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: CPU & PCH XDP

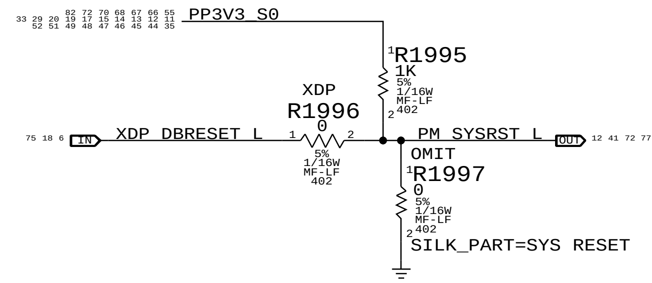
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

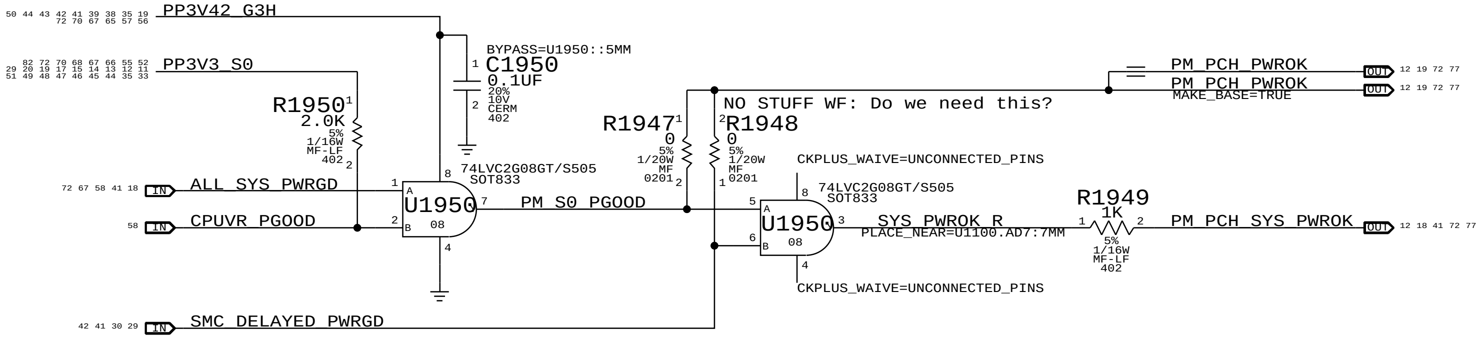
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PCH Reset Button

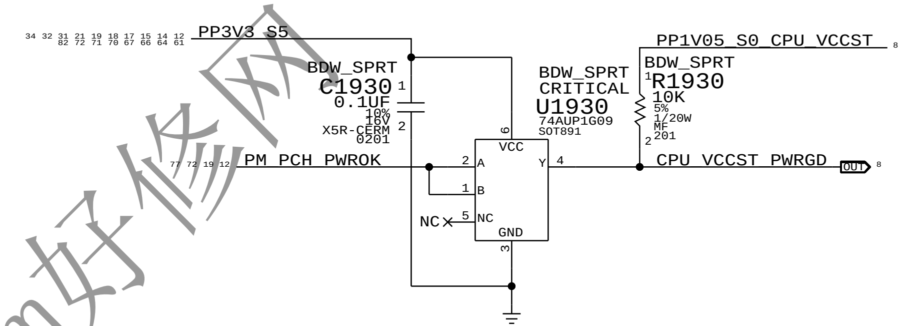


PCH PWROK Generation

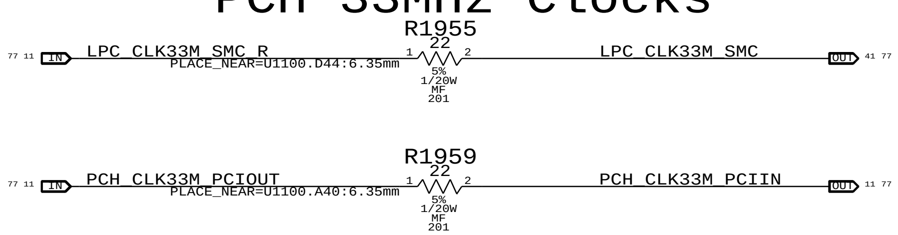


NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

VCCST (1.05V S0) PWRGD

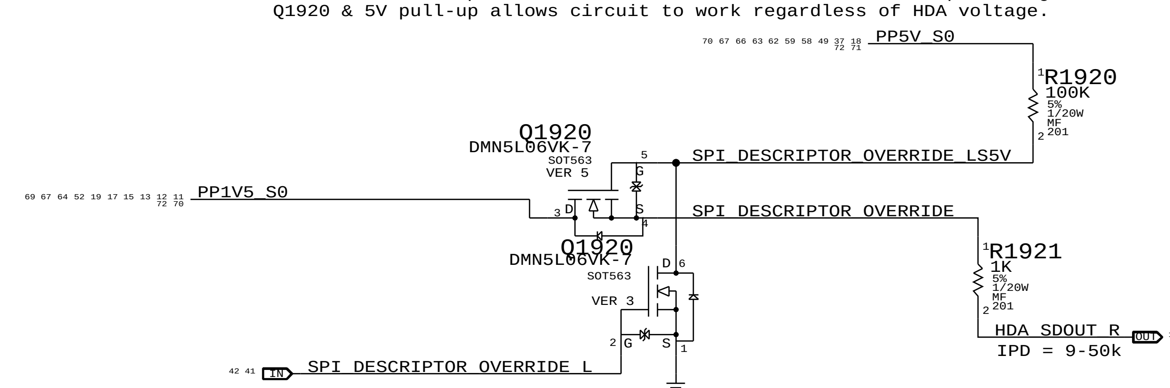


PCH 33MHz Clocks



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

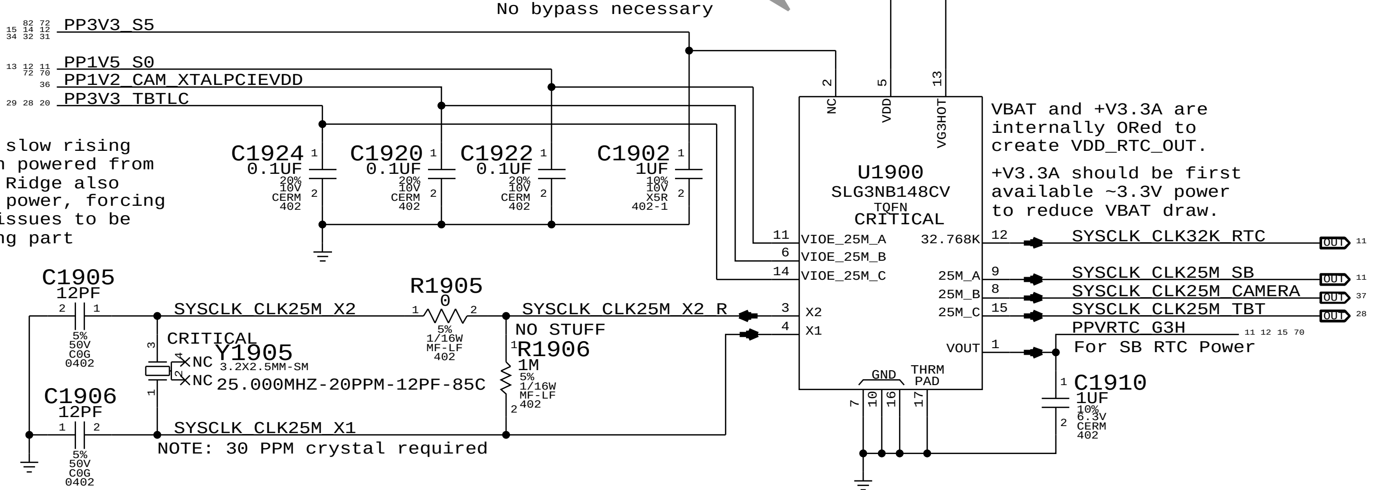
PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary

NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Falcon Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).

VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.



NOTE: 30 PPM crystal required

SYNC_MASTER=J15_REFERENCE	SYNC_DATE=12/18/2012
PAGE TITLE	Chipset Support
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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	BRANCH <BRANCH>
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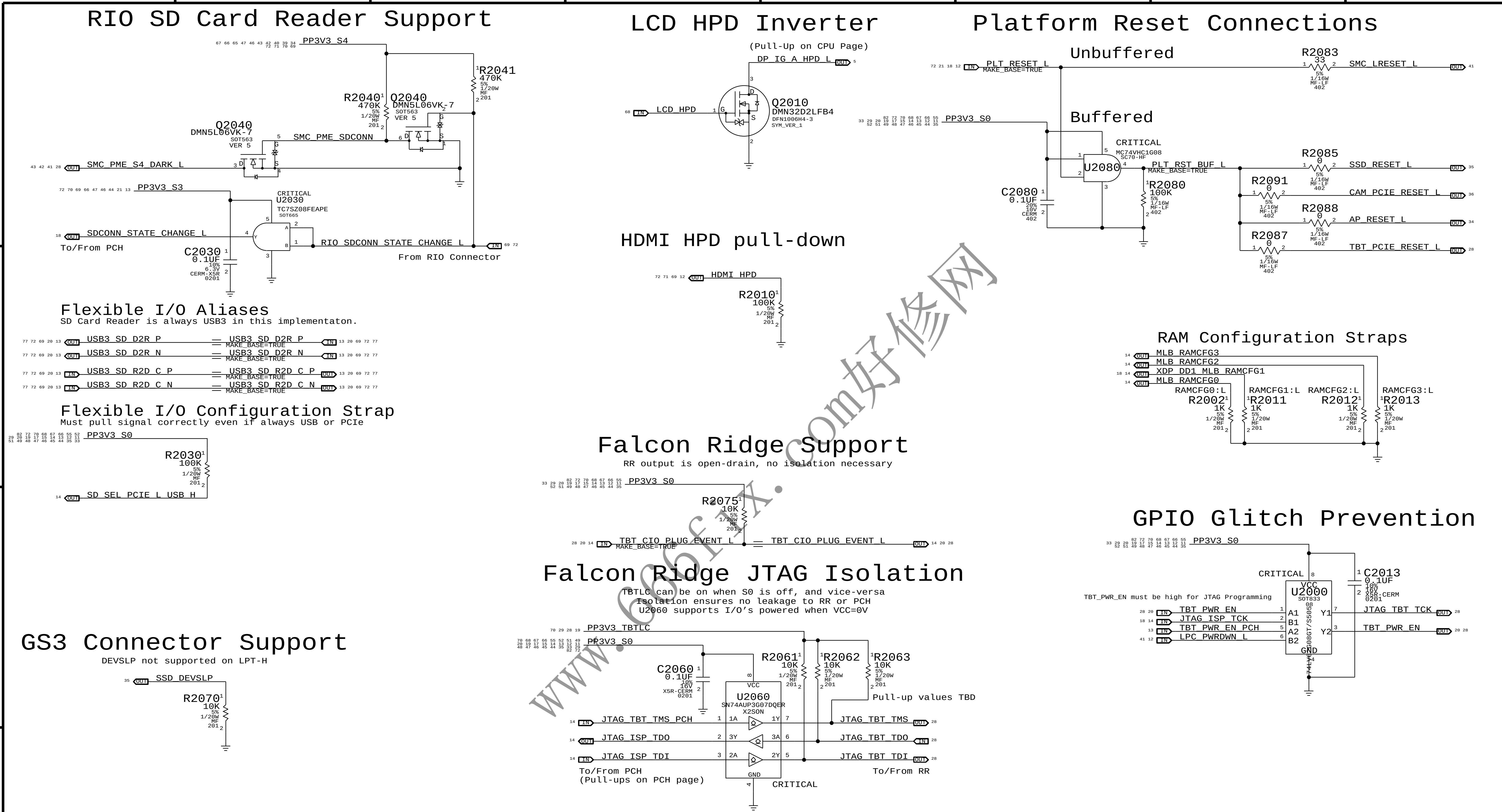

SYNC_MASTER=J15_REFERENCE SYNC_DATE=01/14/2013

PAGE TITLE: Project Chipset Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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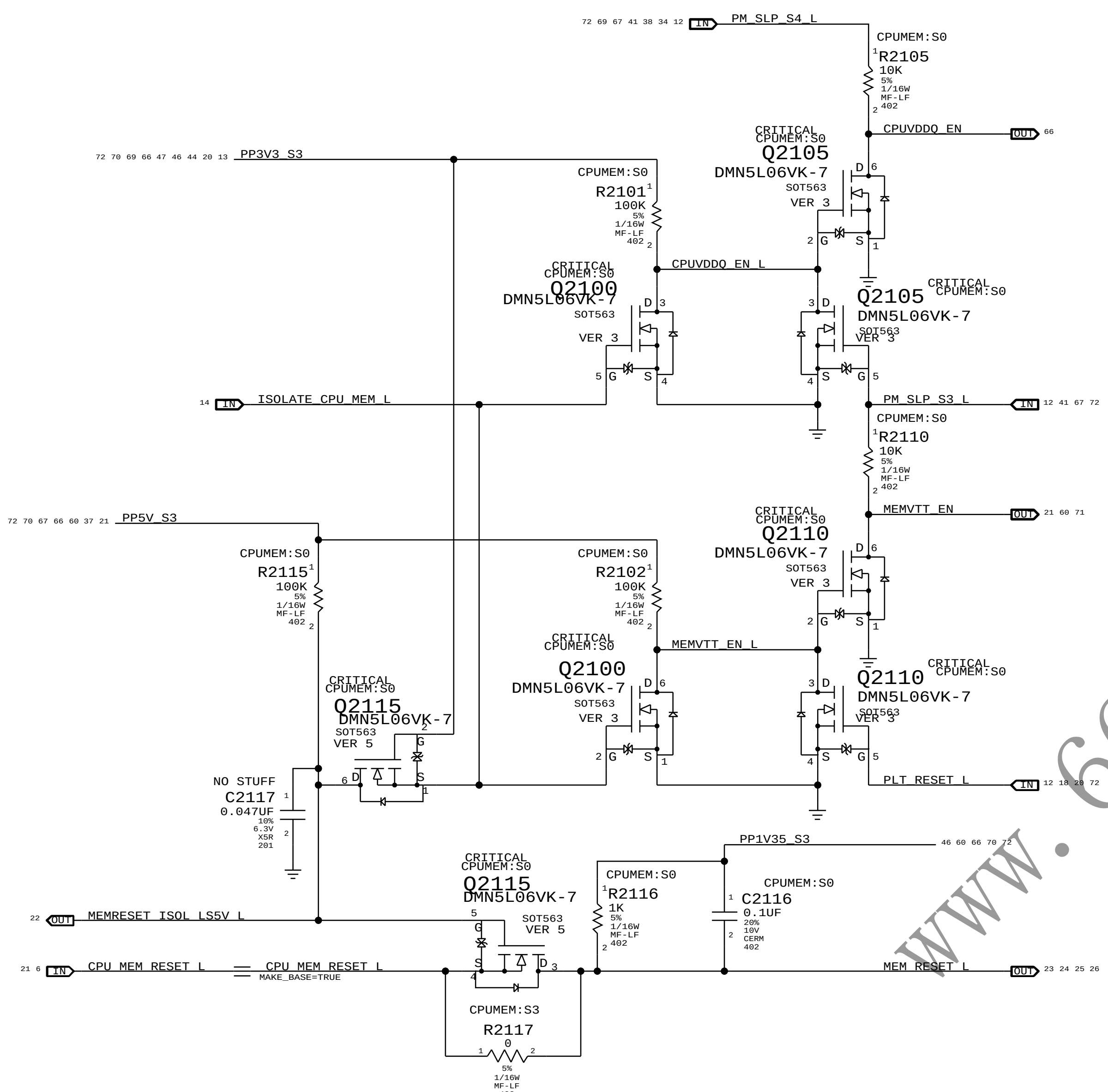
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

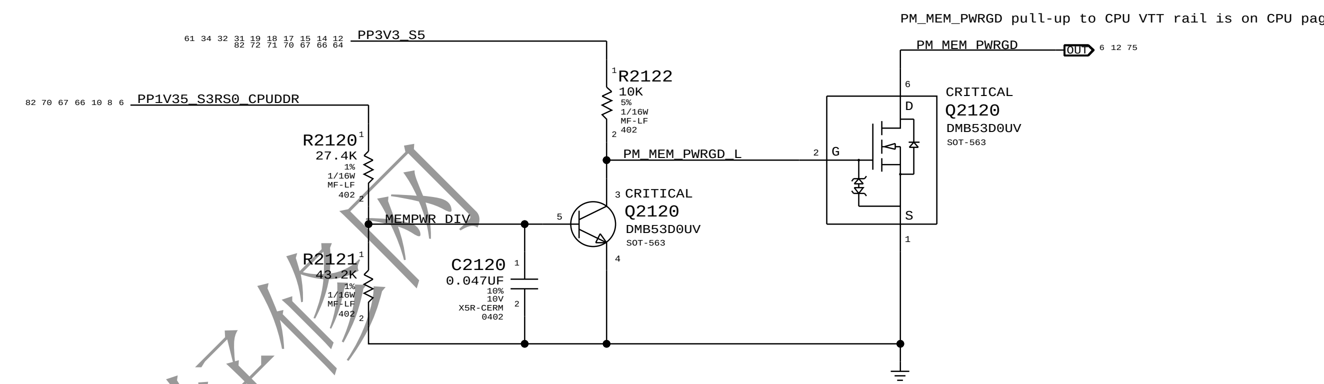
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



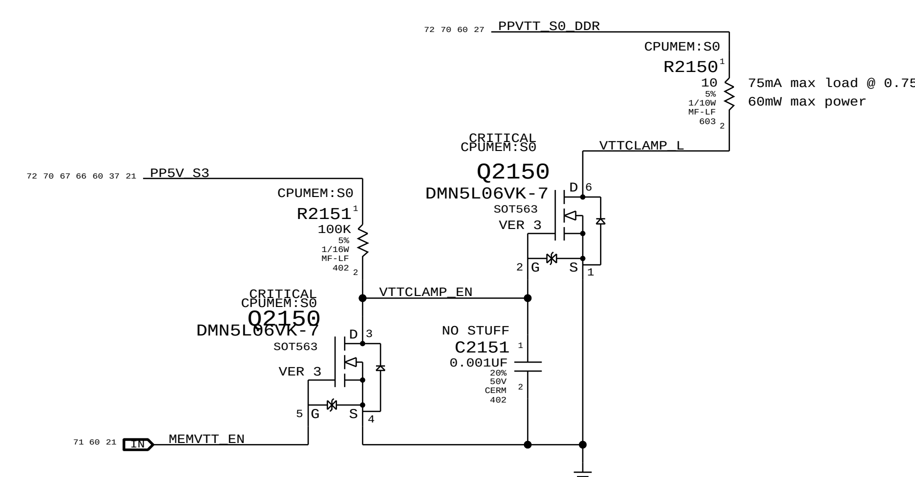
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
	2	0	0	1	1	1	1	0	1
S3	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=CLEAN_X305G SYNC_DATE=07/01/2014
PAGE TITLE
CPU Memory S3 Support
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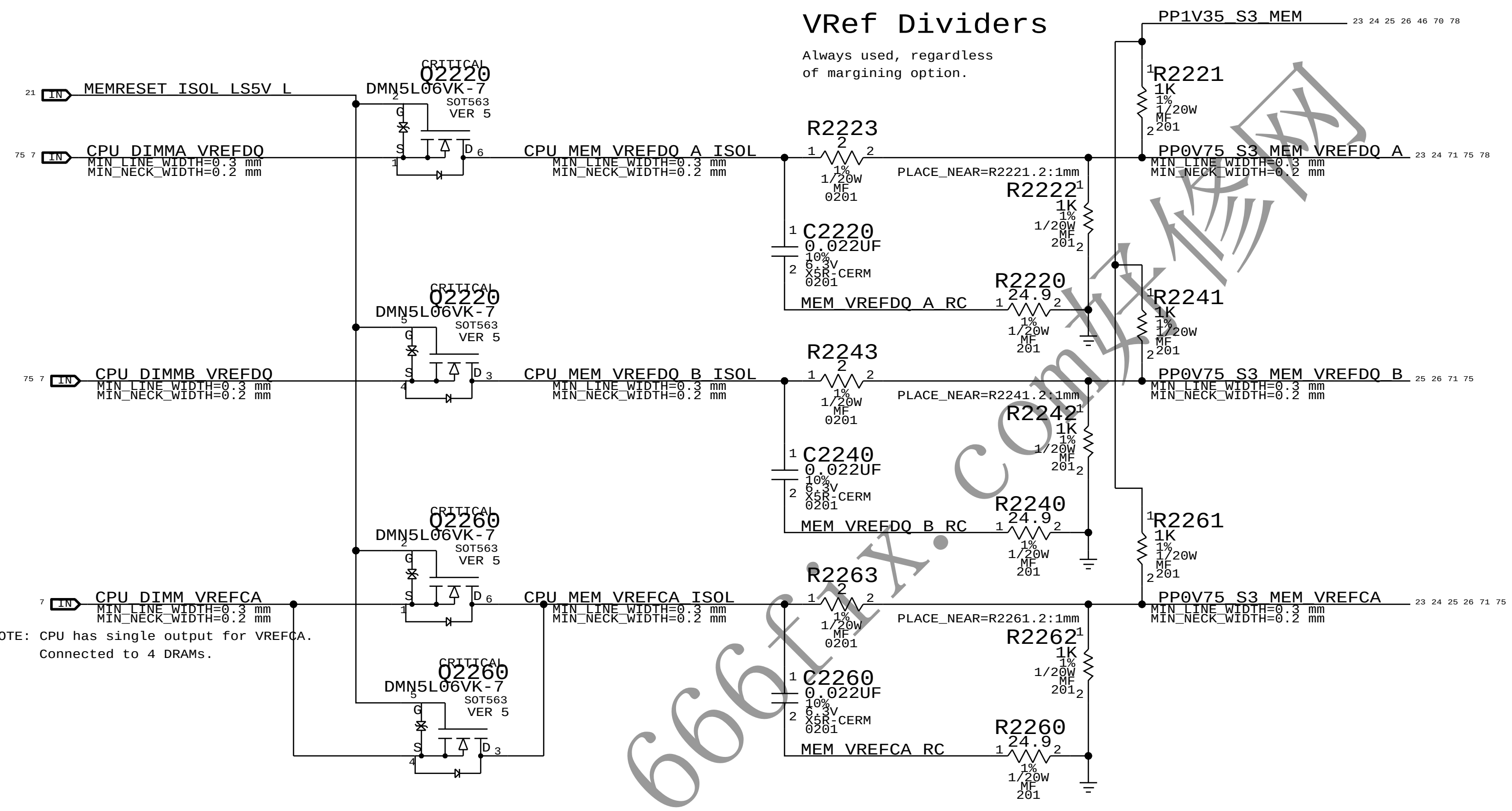
Apple Inc.
REVISION <E4LABEL>
BRANCH <BRANCH>

CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

VRef Dividers

Always used, regardless of margining option.



NOTE: CPU has single output for VREFCA.
Connected to 4 DRAMs.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5

	LPDDR3 (1.2V)	DDR3L (1.35V)	LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)	0.675V (DAC: 0x34)	1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)	0.337V - 1.013V (+/- 337.5mV)	0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)	0.000V - 1.354V (0x00 - 0x69)	0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)	+82uA - -82uA (- = sourced)	+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output	6.36mV / step @ output	4.28mV / step @ output	3.53mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/14/2014

PAGE TITLE: DDR3 VREF MARGINING

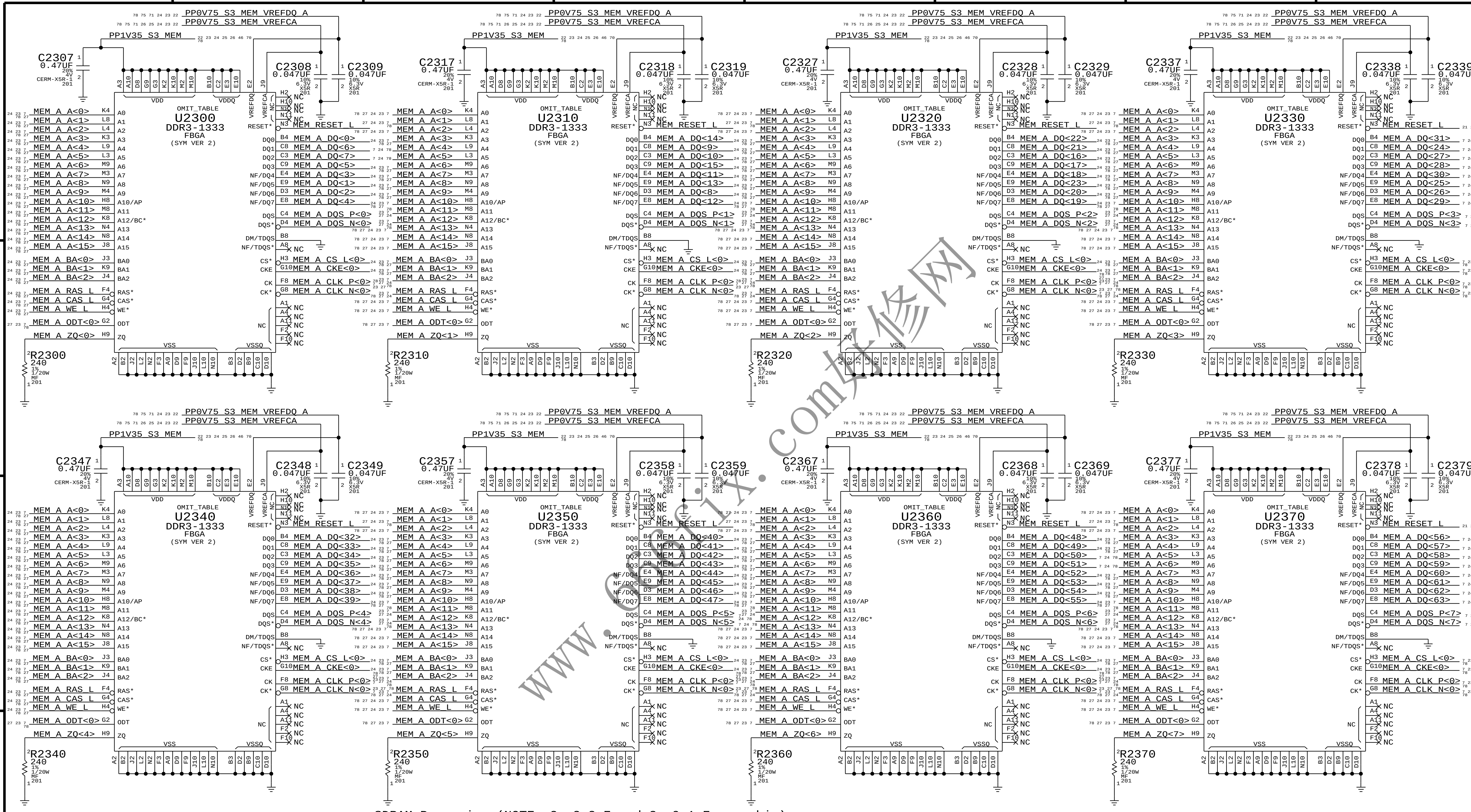
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

8 7 6 5 4 3 2 1



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

DDR3 SDRAM Bank A (1 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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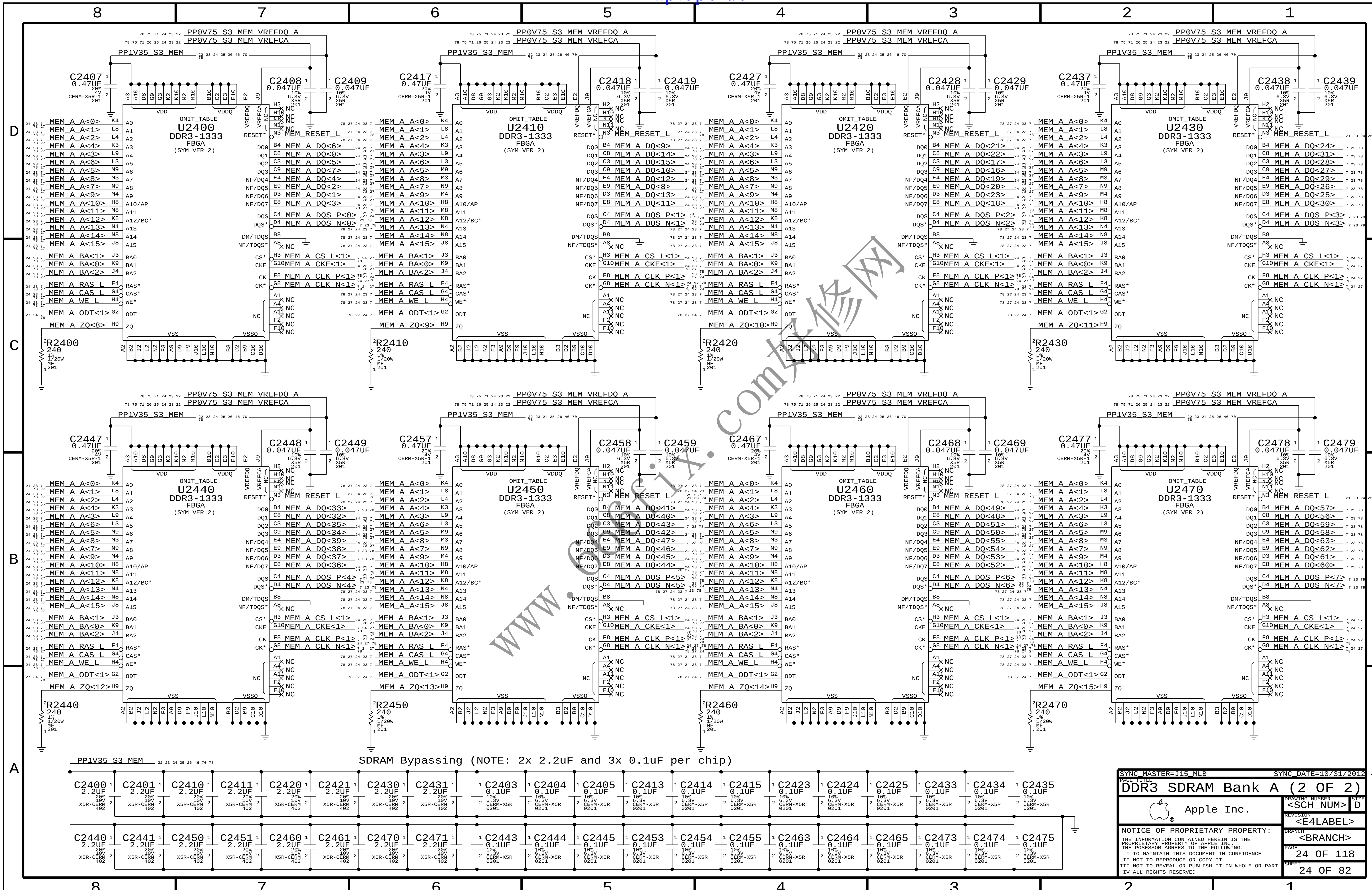
8 7 6 5 4 3 2 1



8 7 6 5 4 3 2 1
D C B A
PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA
PP1V35_S3_MEM
C2407 0.47UF
C2408 0.047UF
C2409 0.047UF
OMIT_TABLE
U2400
DDR3-1333
FBGA
(SYM VER 2)
R2400 240
C2417 0.47UF
C2418 0.047UF
C2419 0.047UF
U2410
DDR3-1333
FBGA
R2410 240
C2427 0.47UF
C2428 0.047UF
C2429 0.047UF
U2420
DDR3-1333
FBGA
R2420 240
C2437 0.47UF
C2438 0.047UF
C2439 0.047UF
U2430
DDR3-1333
FBGA
R2430 240
C2447 0.47UF
C2448 0.047UF
C2449 0.047UF
U2440
DDR3-1333
FBGA
R2440 240
C2457 0.47UF
C2458 0.047UF
C2459 0.047UF
U2450
DDR3-1333
FBGA
R2450 240
C2467 0.47UF
C2468 0.047UF
C2469 0.047UF
U2460
DDR3-1333
FBGA
R2460 240
C2477 0.47UF
C2478 0.047UF
C2479 0.047UF
U2470
DDR3-1333
FBGA
R2470 240
MEM_A_RESET_L
MEM_A_CS_L<1>
MEM_A_CKE<1>
MEM_A_CLK_P<1>
MEM_A_CLK_N<1>
MEM_A_RAS_L
MEM_A_CAS_L
MEM_A_WE_L
MEM_A_ODT<1>
SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
C2400 2.2UF C2401 2.2UF C2410 2.2UF C2411 2.2UF C2420 2.2UF C2421 2.2UF C2430 2.2UF C2431 2.2UF
C2403 0.1UF C2404 0.1UF C2405 0.1UF C2413 0.1UF C2414 0.1UF C2415 0.1UF C2423 0.1UF C2424 0.1UF C2425 0.1UF C2433 0.1UF C2434 0.1UF C2435 0.1UF
C2440 2.2UF C2441 2.2UF C2450 2.2UF C2451 2.2UF C2460 2.2UF C2461 2.2UF C2470 2.2UF C2471 2.2UF
C2443 0.1UF C2444 0.1UF C2445 0.1UF C2453 0.1UF C2454 0.1UF C2455 0.1UF C2463 0.1UF C2464 0.1UF C2465 0.1UF C2473 0.1UF C2474 0.1UF C2475 0.1UF
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012
DDR3 SDRAM Bank A (2 OF 2)
Apple Inc.
<SCH_NUM>
D
<E4LABEL>
<BRANCH>
24 OF 118
24 OF 82
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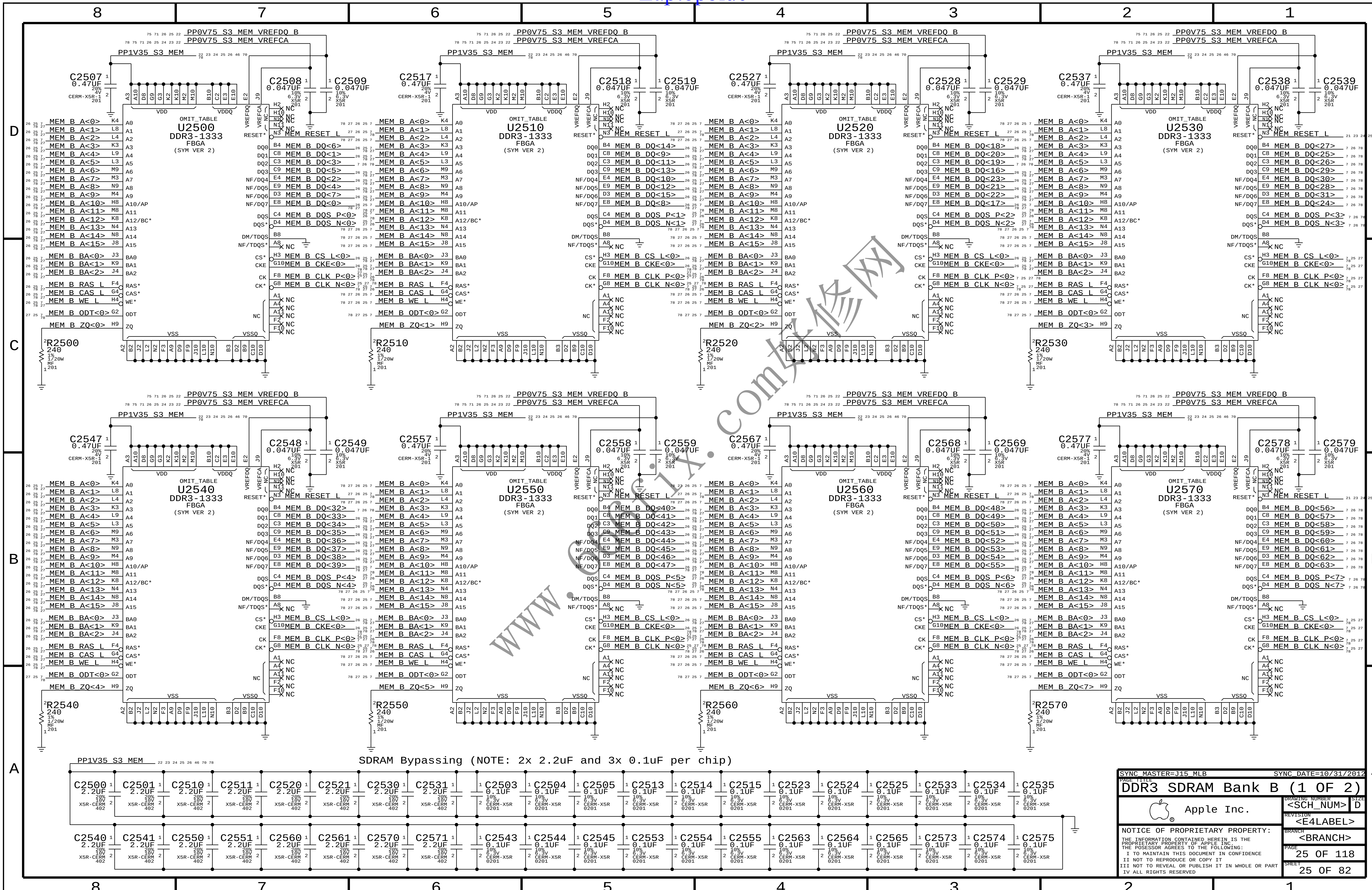

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

DDR3 SDRAM Bank B (1 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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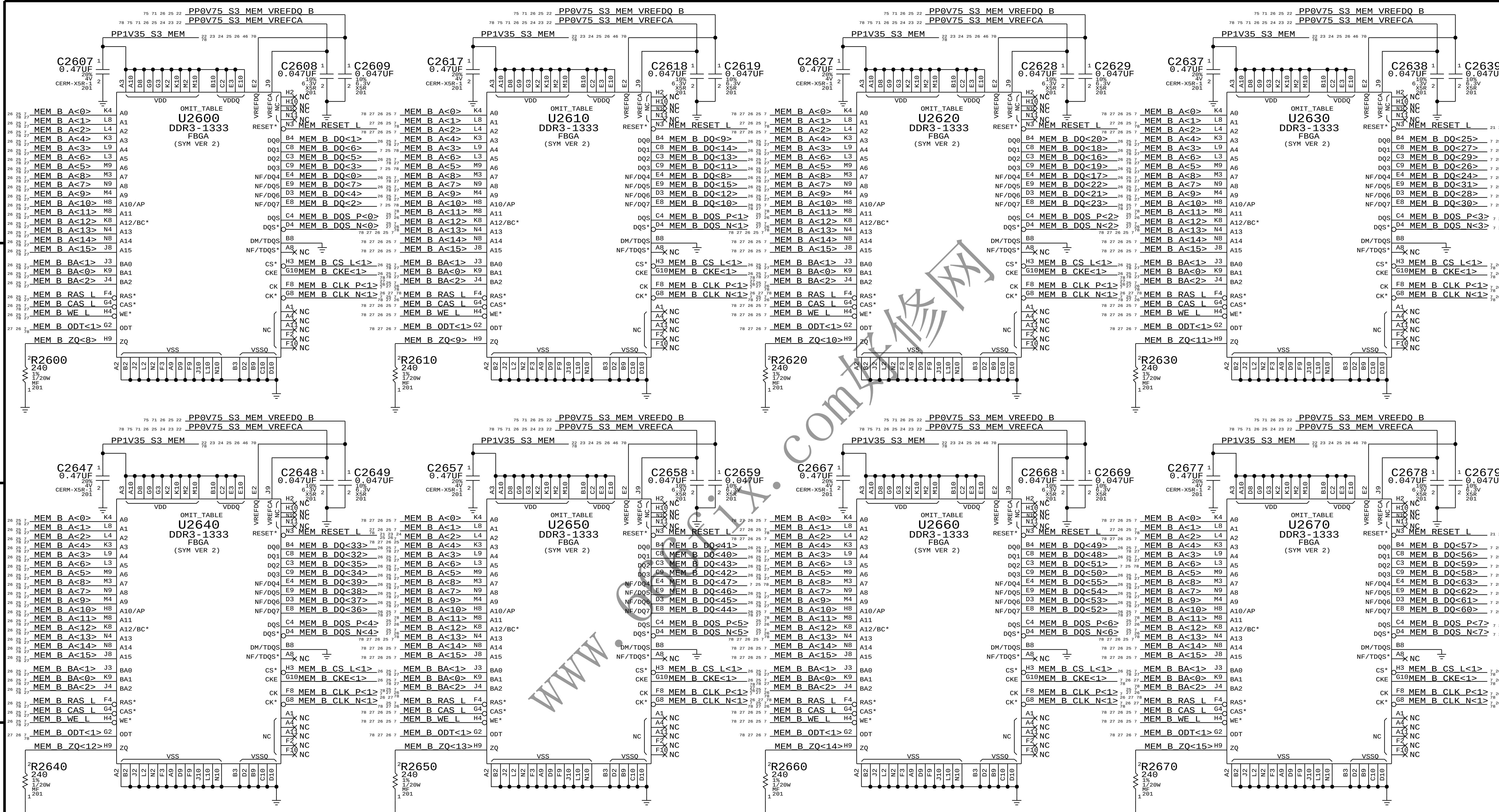
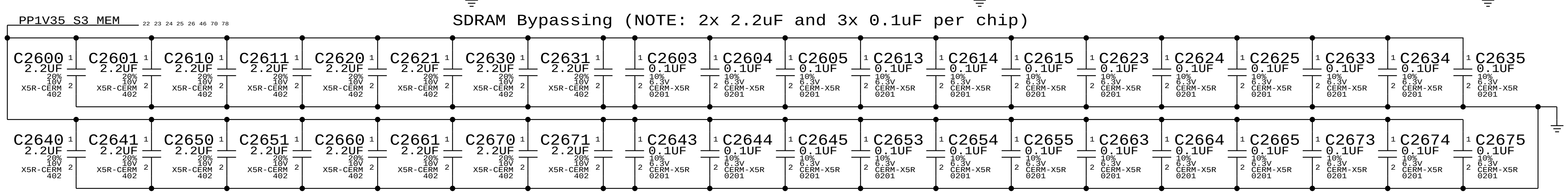


SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)



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DDR3 SDRAM Bank B (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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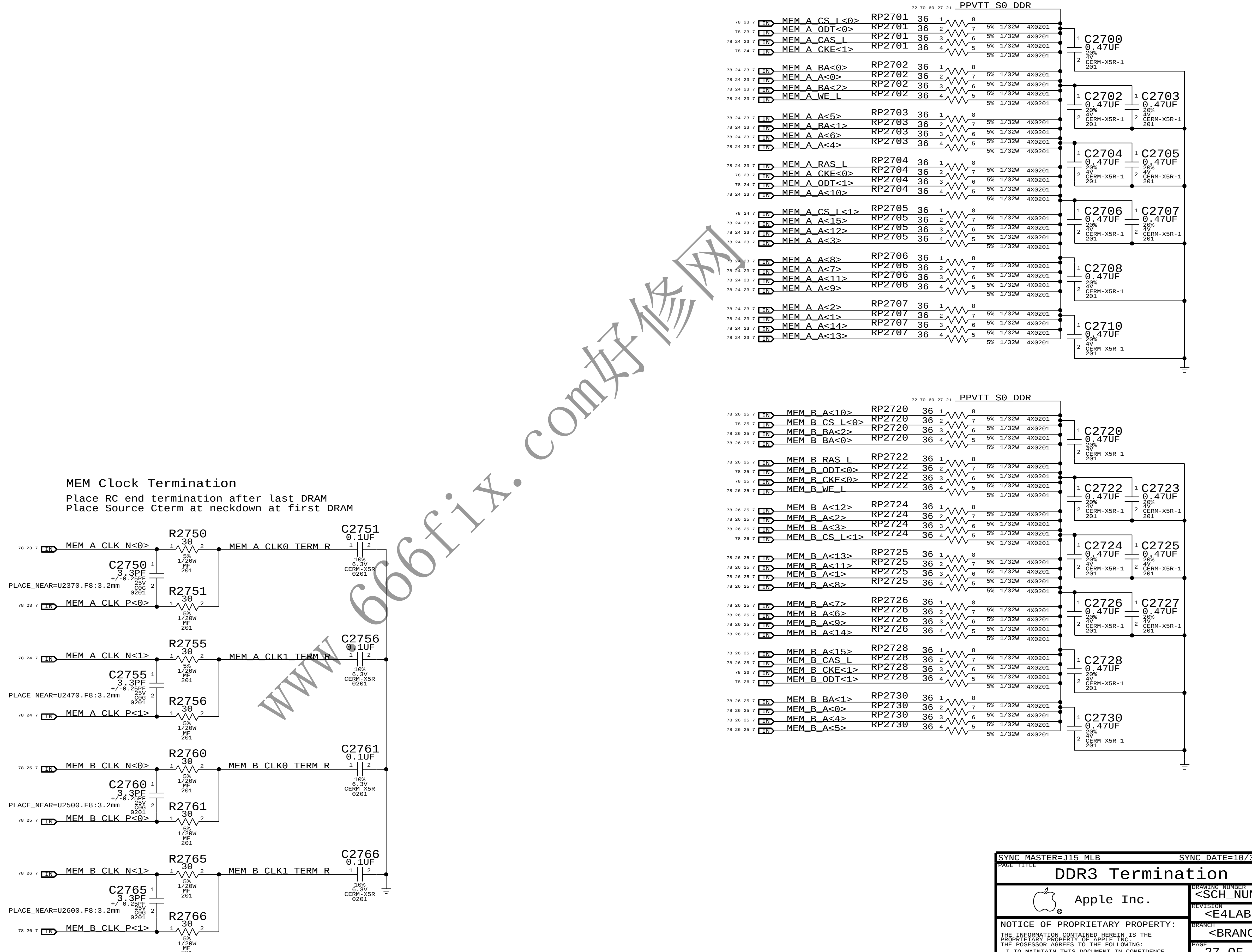
SHEET 26 OF 82

JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



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PAGE TITLE

DDR3 Termination

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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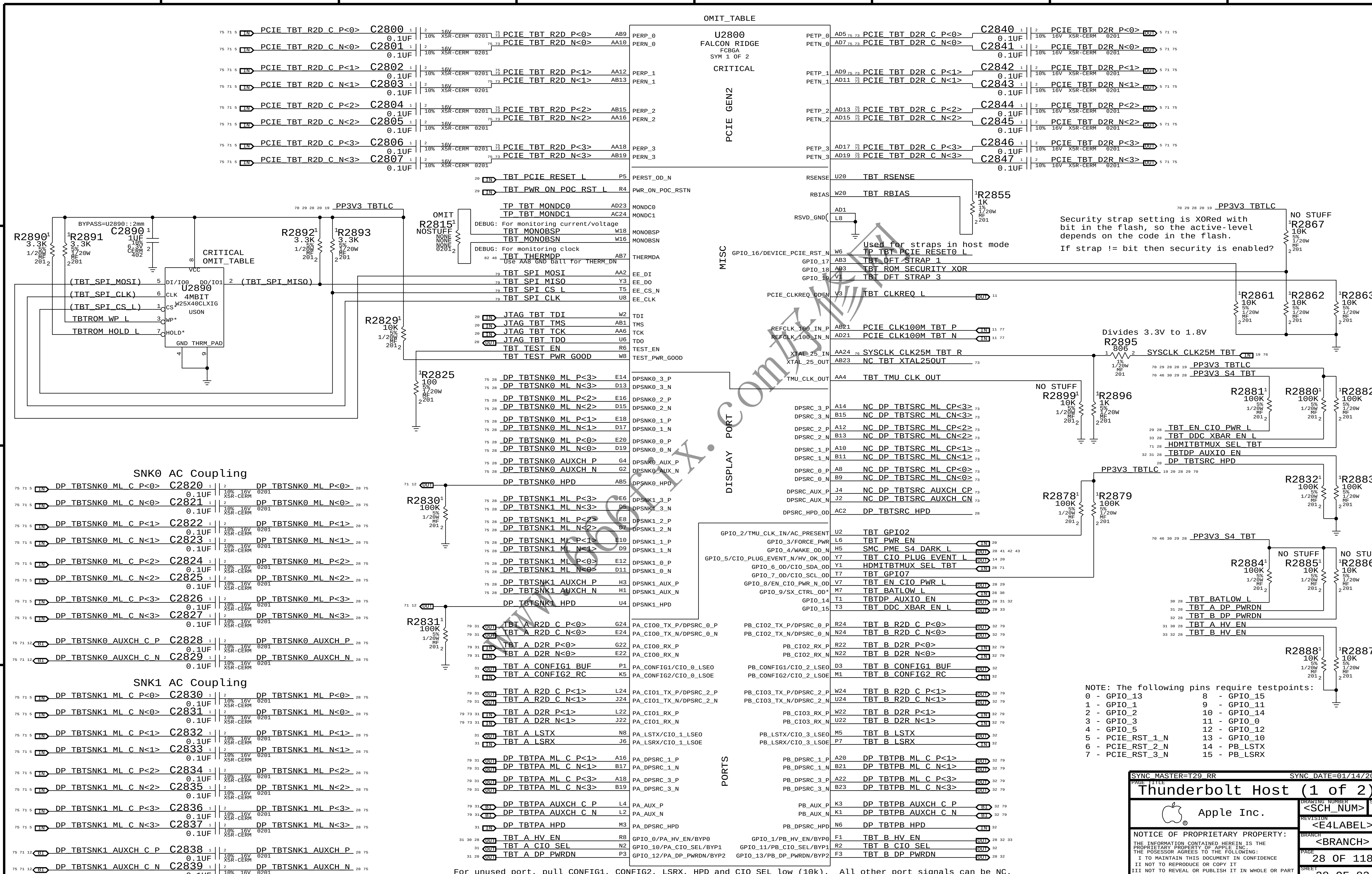
OMIT_TABLE
U2800
FALCON RIDGE
FCBGA
SYM 1 OF 2
CRITICAL
PCIE GEN2
MISC
DISPLAY PORT
PORTS
U2890
4MBIT
W25X40CLXIG
USON
CRITICAL
OMIT_TABLE
BYPASS=U2890::2mm
PP3V3_TBTLC
PP3V3_S4_TBT
DEBUG: For monitoring current/voltage
DEBUG: For monitoring clock
Use AA8 GND ball for THERM_DN
Used for straps in host mode
Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.
If strap != bit then security is enabled?
Divides 3.3V to 1.8V
SNK0 AC Coupling
SNK1 AC Coupling
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=T29_RR
SYNC_DATE=01/14/2013
Thunderbolt Host (1 of 2)
Apple Inc.
<SCH_NUM>
D
<E4LABEL>
<BRANCH>
28 OF 118
28 OF 82
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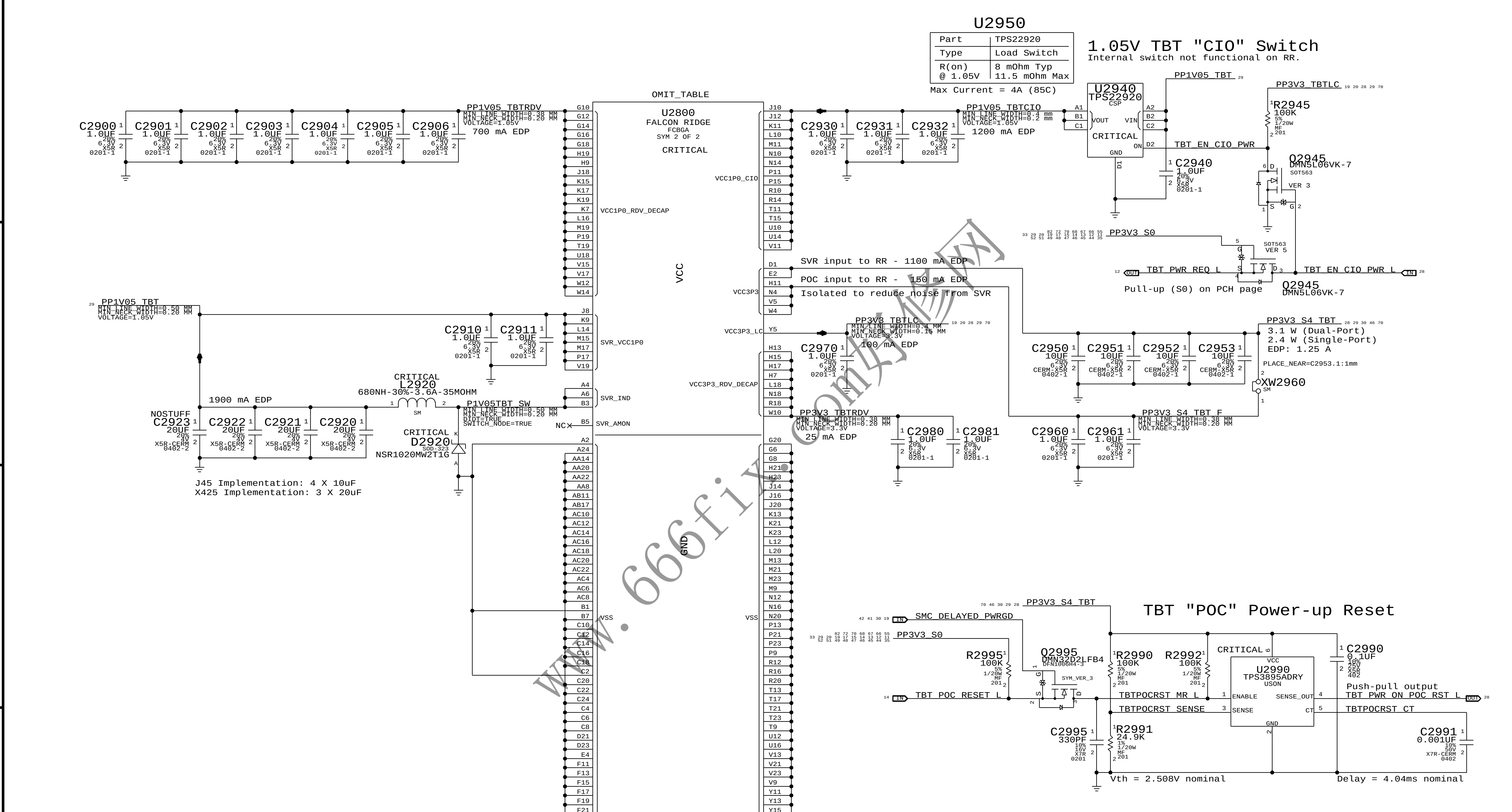


EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC_MASTER=T29_RR SYNC_DATE=01/14/2013

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

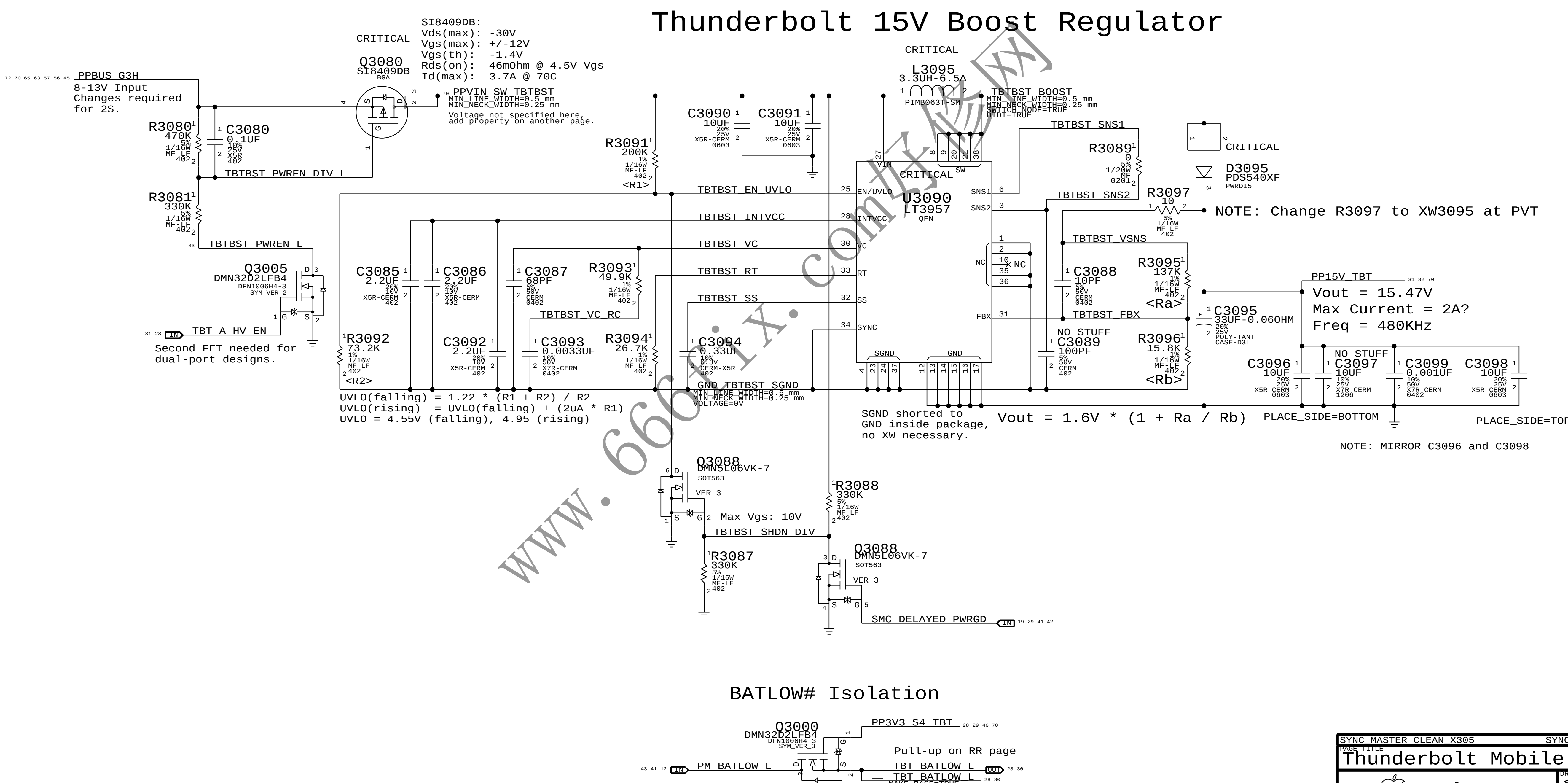
BRANCH: <BRANCH>

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE: Thunderbolt Mobile Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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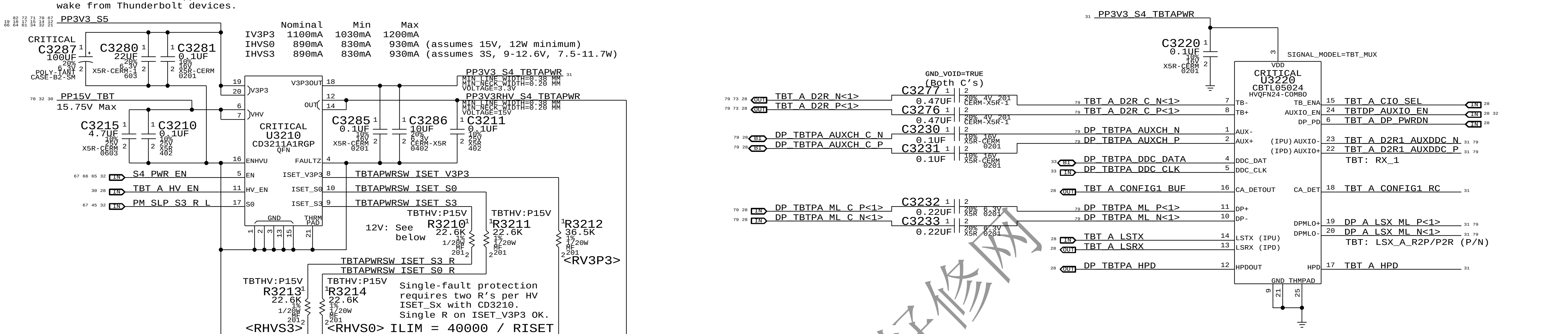
3.3V/HV Power MUX

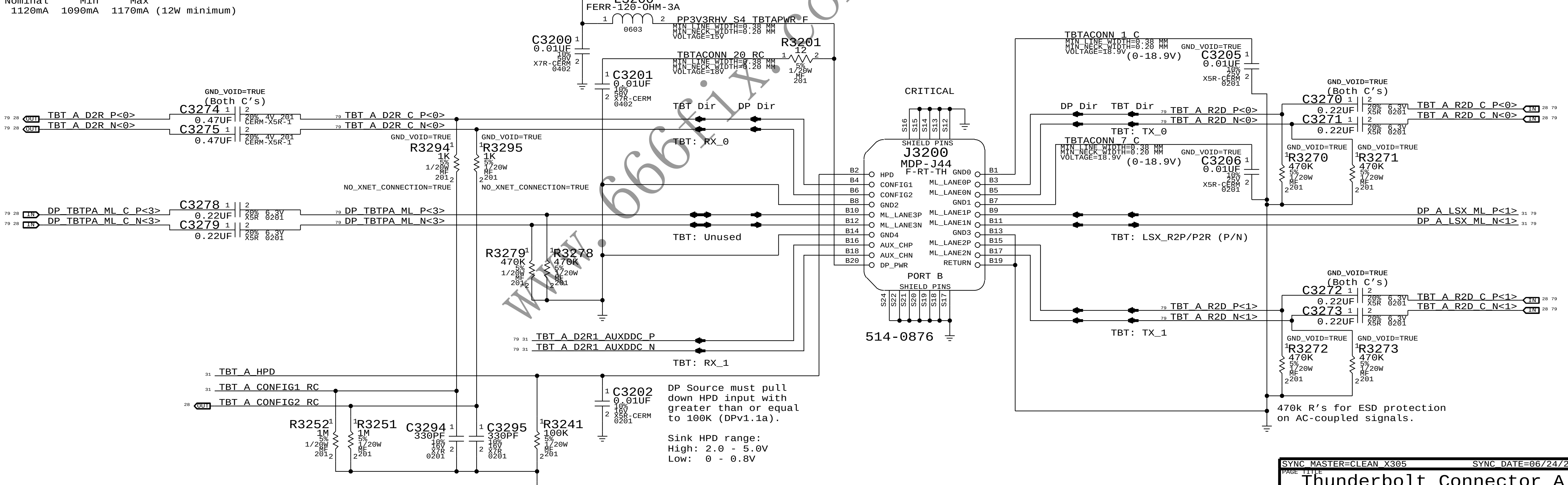


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)

Thunderbolt Connector A



SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE
Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

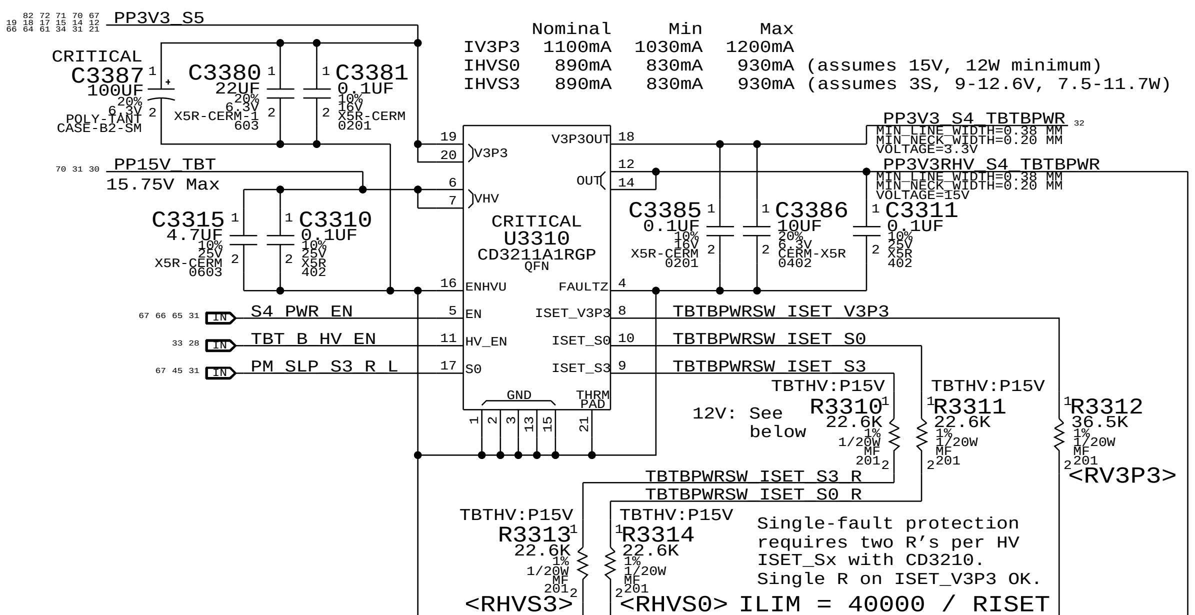
REVISION <E4LABEL>

BRANCH <BRANCH>

3.3V/HV Power MUX

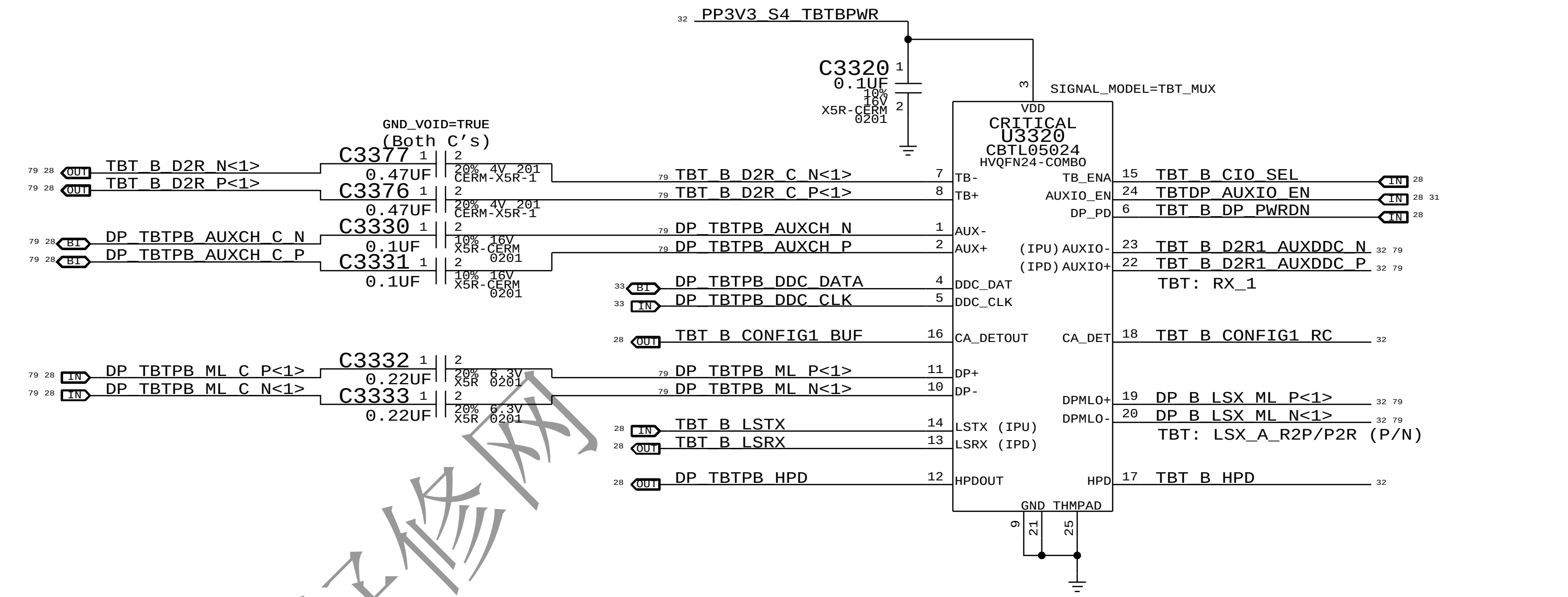
V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)



Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

<RHVS3> <RHVS0> ILIM = 40000 / RISET

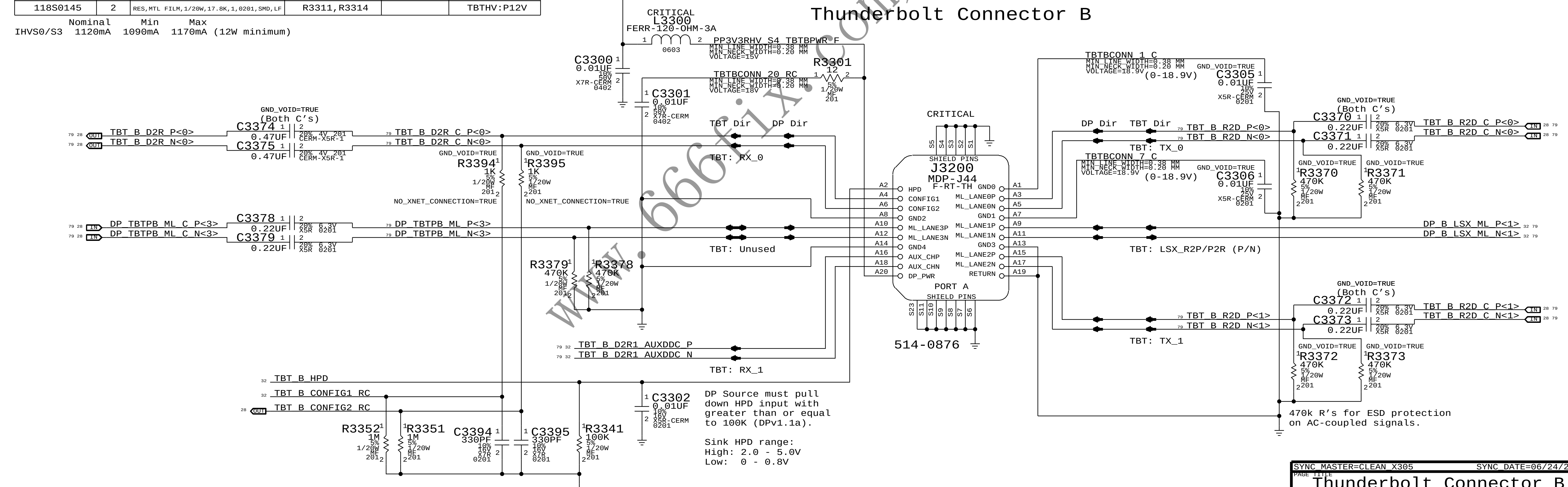


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector B



DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

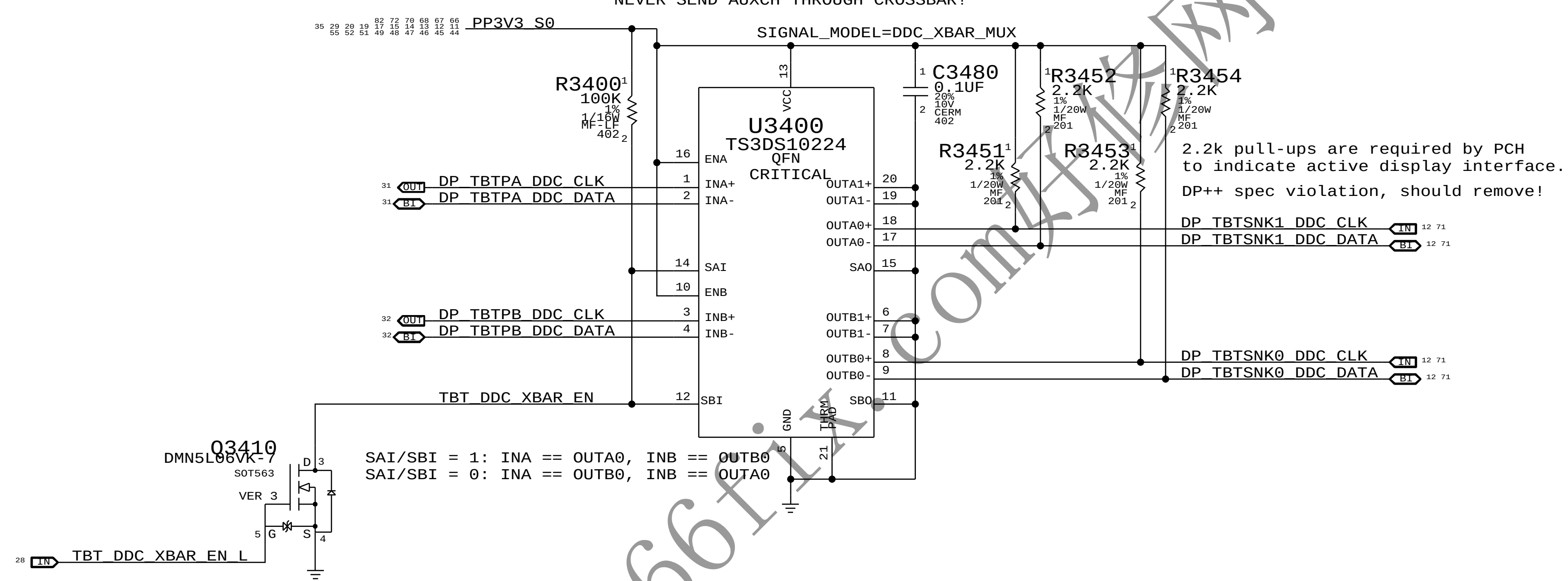
DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

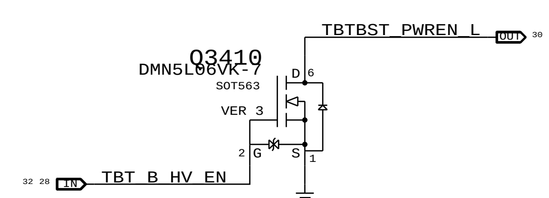
BRANCH: <BRANCH>

DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!



Second TBT Port HV Boost Enable



SYNC_MASTER=J15_REFERENCE SYNC_DATE=11/16/2012

PAGE TITLE: DDC Crossbar

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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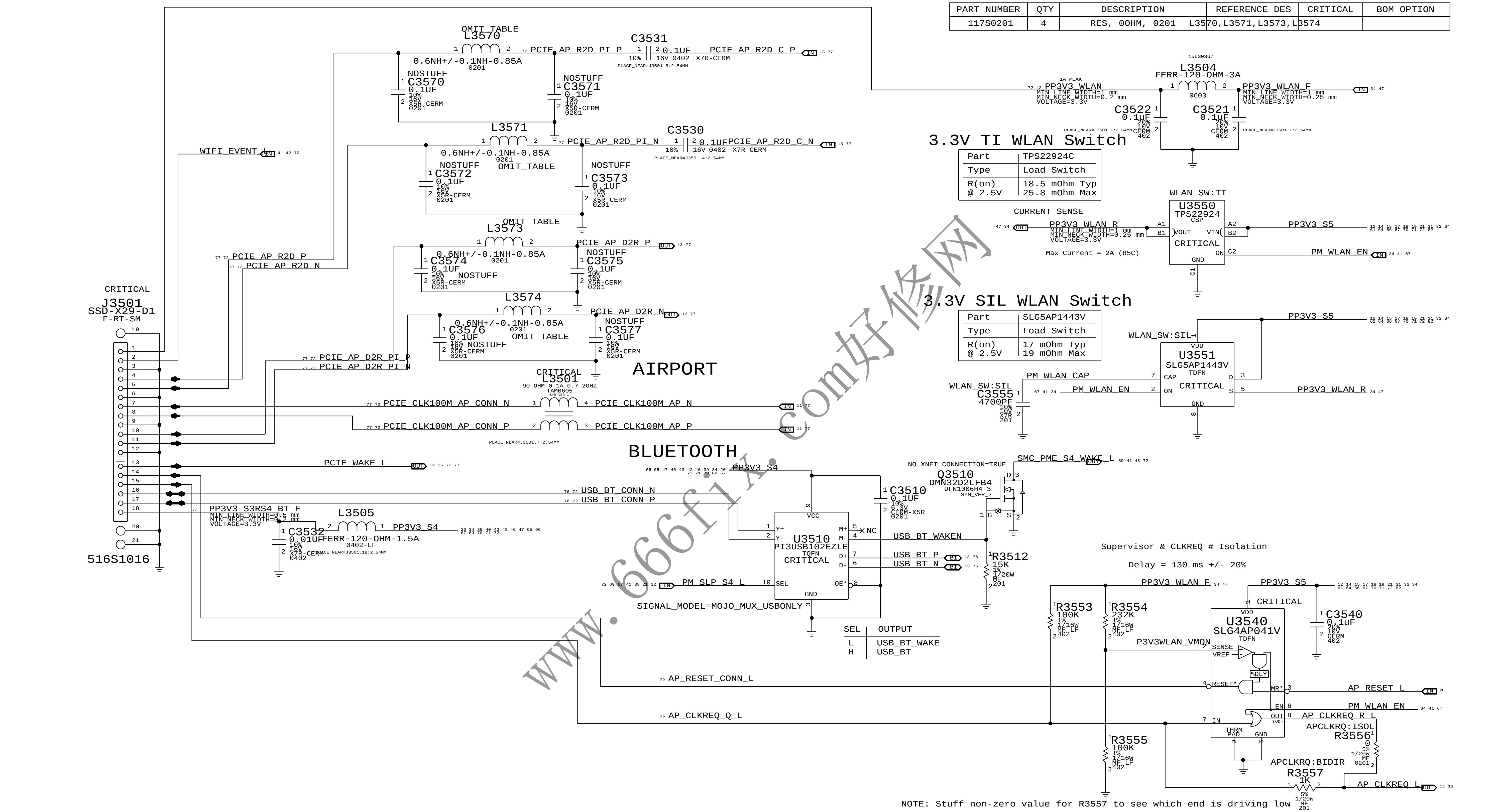
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 0OHM, 0201	L3570,L3571,L3573,L3574		



SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/15/2014

PAGE TITLE: X87 CONNECTOR

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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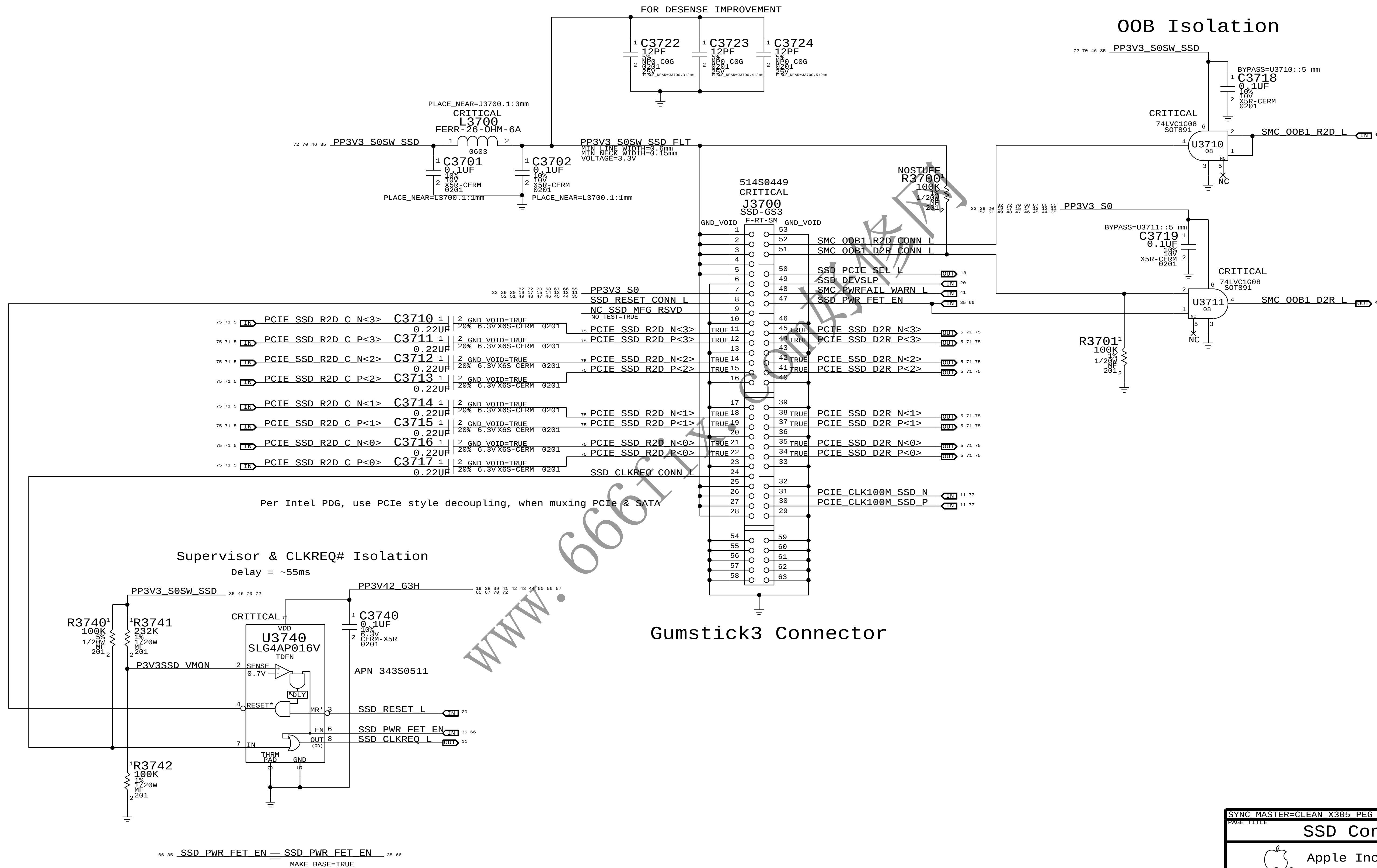

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE

SSD Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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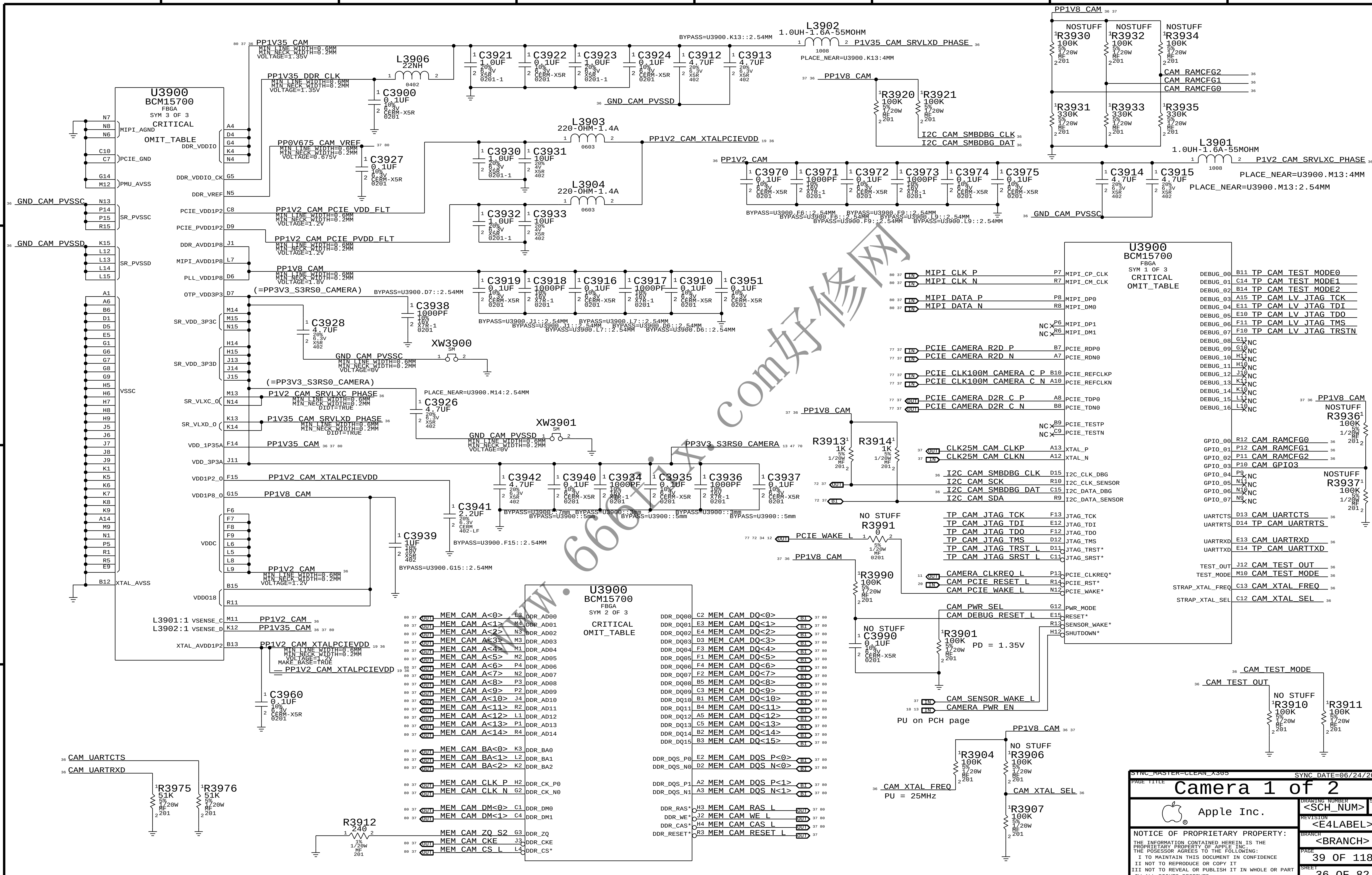
U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE
U3900
BCM15700
FBGA
SYM 1 OF 3
CRITICAL
OMIT_TABLE
U3900
BCM15700
FBGA
SYM 2 OF 3
CRITICAL
OMIT_TABLE
PP1V35_CAM
PP1V35_DDR_CLK
PP0V675_CAM_VREF
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PCIE_PVDD_FLT
PP1V8_CAM
PP1V2_CAM_XTALPCIEVDD
PP1V35_CAM_SRVLXD_PHASE
PP1V2_CAM_SRVLXC_PHASE
PP3V3_S3RS0_CAMERA
GND_CAM_PVSSC
GND_CAM_PVSSD
L3901
1.0UH-1.6A-55MOHM
L3902
1.0UH-1.6A-55MOHM
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
L3906
22NH
XW3900
XW3901
MIPI_CLK_P
MIPI_CLK_N
MIPI_DATA_P
MIPI_DATA_N
PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_N
PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
CLK25M_CAM_CLKP
CLK25M_CAM_CLKN
I2C_CAM_SMBDBG_CLK
I2C_CAM_SCK
I2C_CAM_SMBDBG_DAT
I2C_CAM_SDA
TP_CAM_JTAG_TCK
TP_CAM_JTAG_TDI
TP_CAM_JTAG_TDO
TP_CAM_JTAG_TMS
TP_CAM_JTAG_TRST_L
TP_CAM_JTAG_SRST_L
CAMERA_CLKREQ_L
CAM_PCIE_RESET_L
CAM_PCIE_WAKE_L
PCIE_WAKE_L
CAM_PWR_SEL
CAM_DEBUG_RESET_L
CAM_SENSOR_WAKE_L
CAMERA_PWR_EN
PU on PCH page
PD = 1.35V
TP_CAM_TEST_MODE0
TP_CAM_TEST_MODE1
TP_CAM_TEST_MODE2
TP_CAM_LV_JTAG_TCK
TP_CAM_LV_JTAG_TDI
TP_CAM_LV_JTAG_TDO
TP_CAM_LV_JTAG_TMS
TP_CAM_LV_JTAG_TRSTN
CAM_RAMCFG0
CAM_RAMCFG1
CAM_RAMCFG2
CAM_GPIO3
CAM_UARTCTS
TP_CAM_UARTRTS
CAM_UARTRXD
TP_CAM_UARTTXD
CAM_TEST_OUT
CAM_TEST_MODE
CAM_XTAL_FREQ
CAM_XTAL_SEL
PU = 25MHz
MEM_CAM_A<0> … MEM_CAM_A<14>
MEM_CAM_BA<0> … MEM_CAM_BA<2>
MEM_CAM_CLK_P
MEM_CAM_CLK_N
MEM_CAM_DM<0>
MEM_CAM_DM<1>
MEM_CAM_ZQ_S2
MEM_CAM_CKE
MEM_CAM_CS_L
MEM_CAM_DQ<0> … MEM_CAM_DQ<15>
MEM_CAM_DQS_P<0>
MEM_CAM_DQS_N<0>
MEM_CAM_DQS_P<1>
MEM_CAM_DQS_N<1>
MEM_CAM_RAS_L
MEM_CAM_WE_L
MEM_CAM_CAS_L
MEM_CAM_RESET_L
L3901:1 VSENSE_C
L3902:1 VSENSE_D
SYNC_MASTER=CLEAN_X305
SYNC_DATE=06/24/2014
PAGE TITLE
Camera 1 of 2
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
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REVISION
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BRANCH
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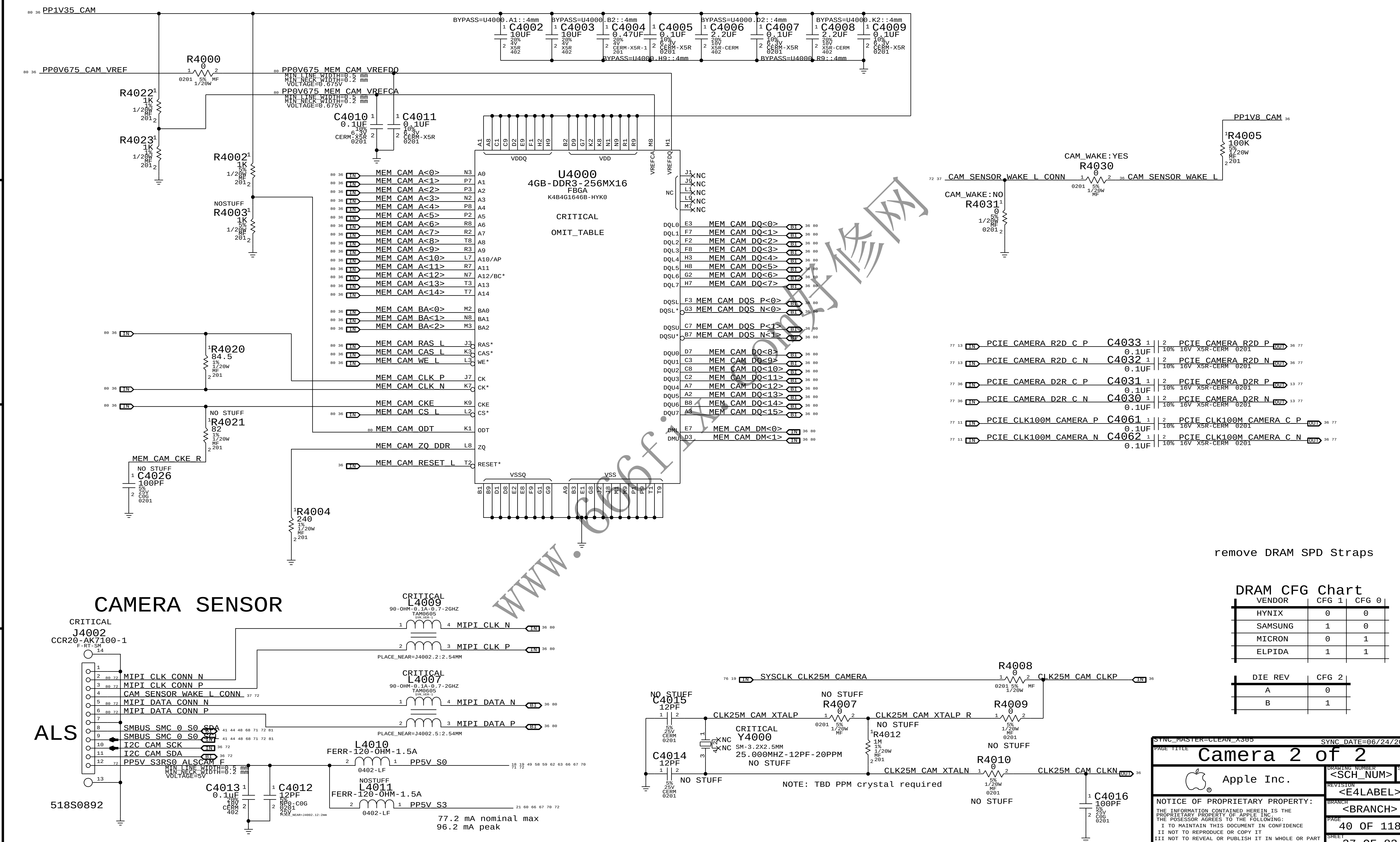

DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE: Camera 2 of 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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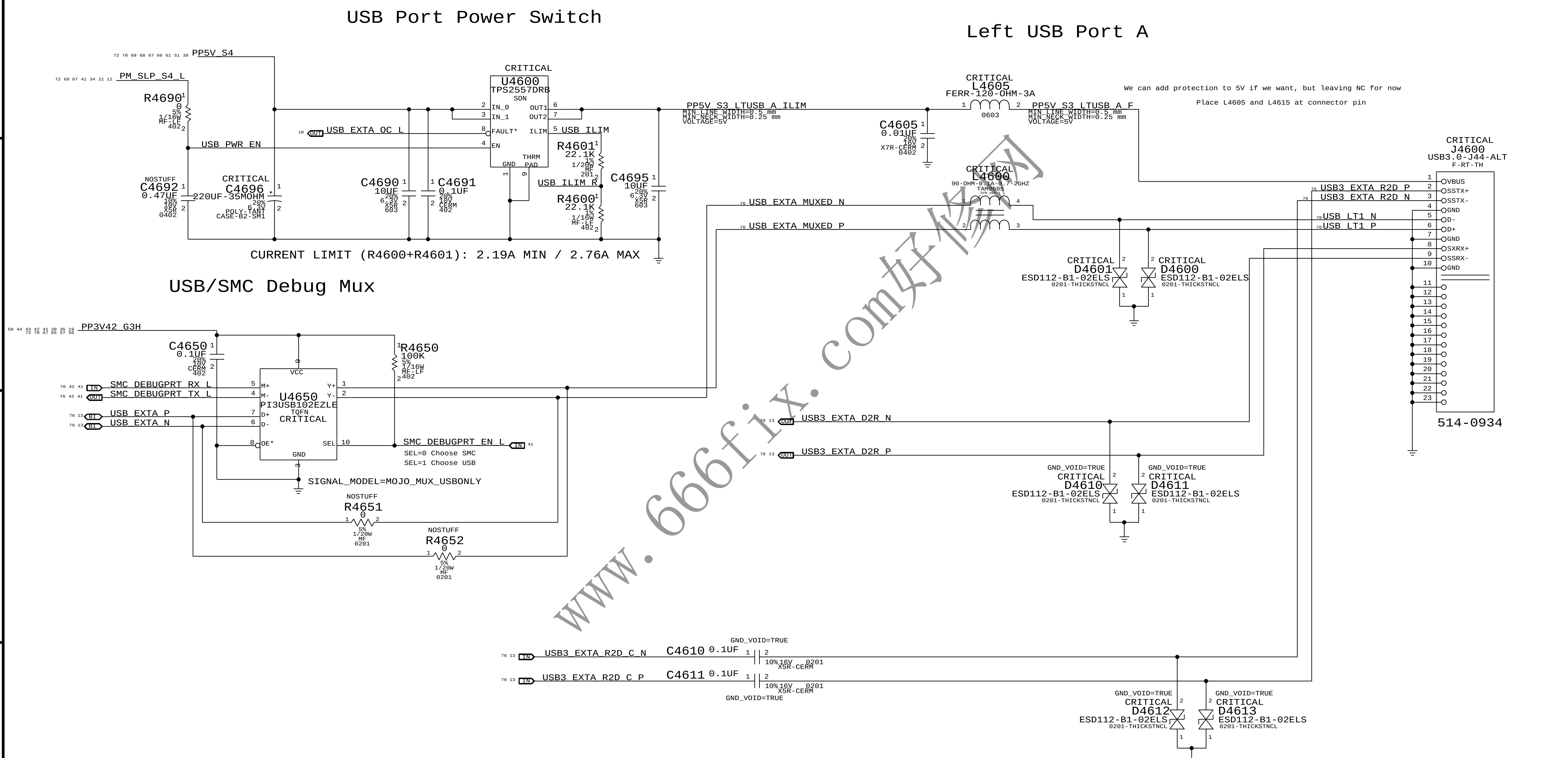

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PAGE TITLE

USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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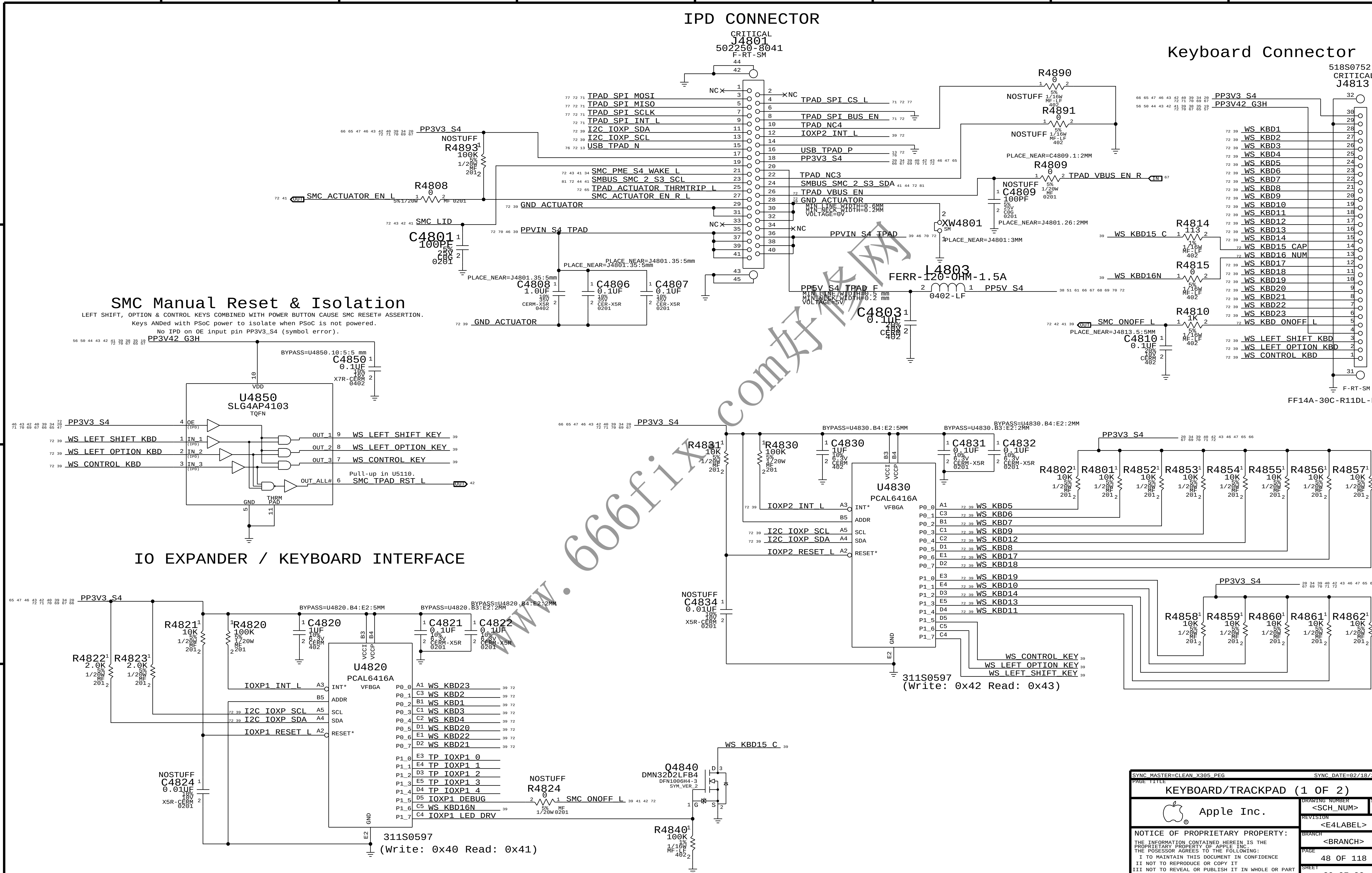

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE

KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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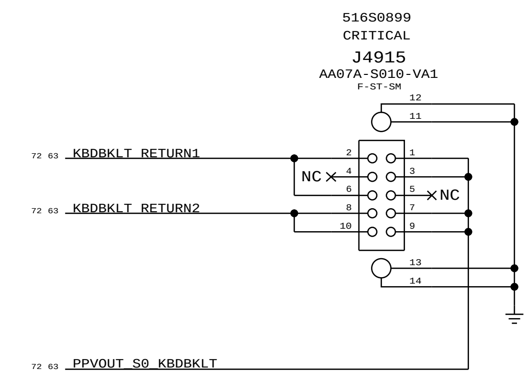
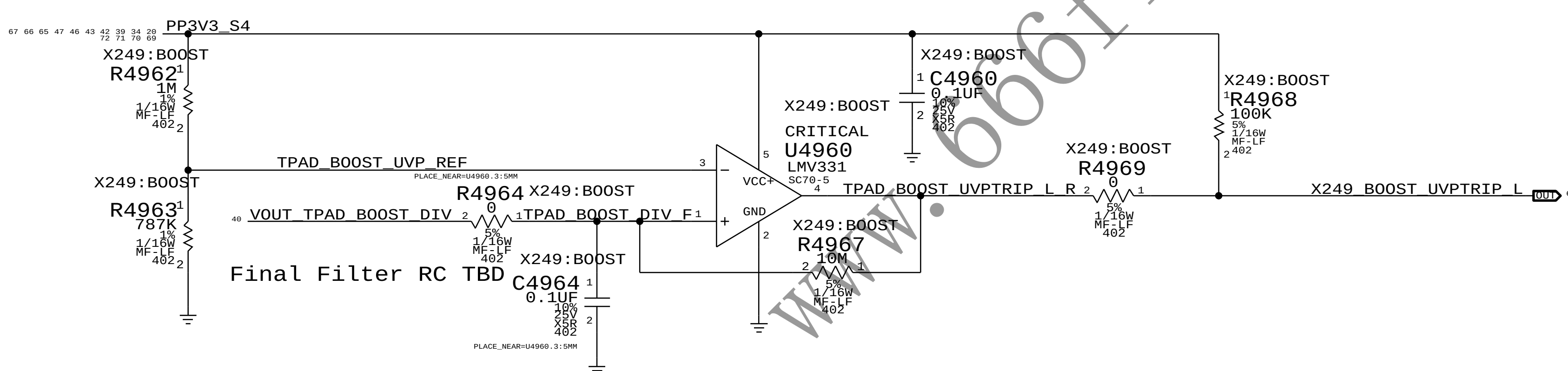
Keyboard Backlight Connector

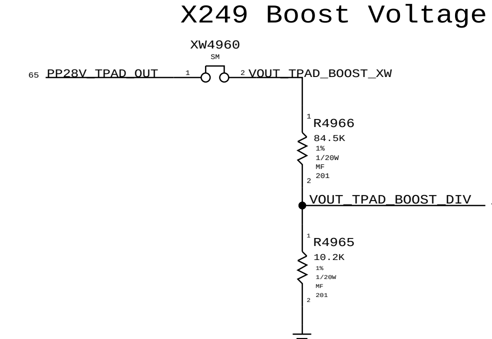


X249 BOOST UVP TRIP



Trip set at 13.5V (divider set for 1.45V)

X249 Boost Voltage Sense



SYNC_MASTER=CLEAN_X305 SYNC_DATE=05/30/2014

PAGE TITLE: KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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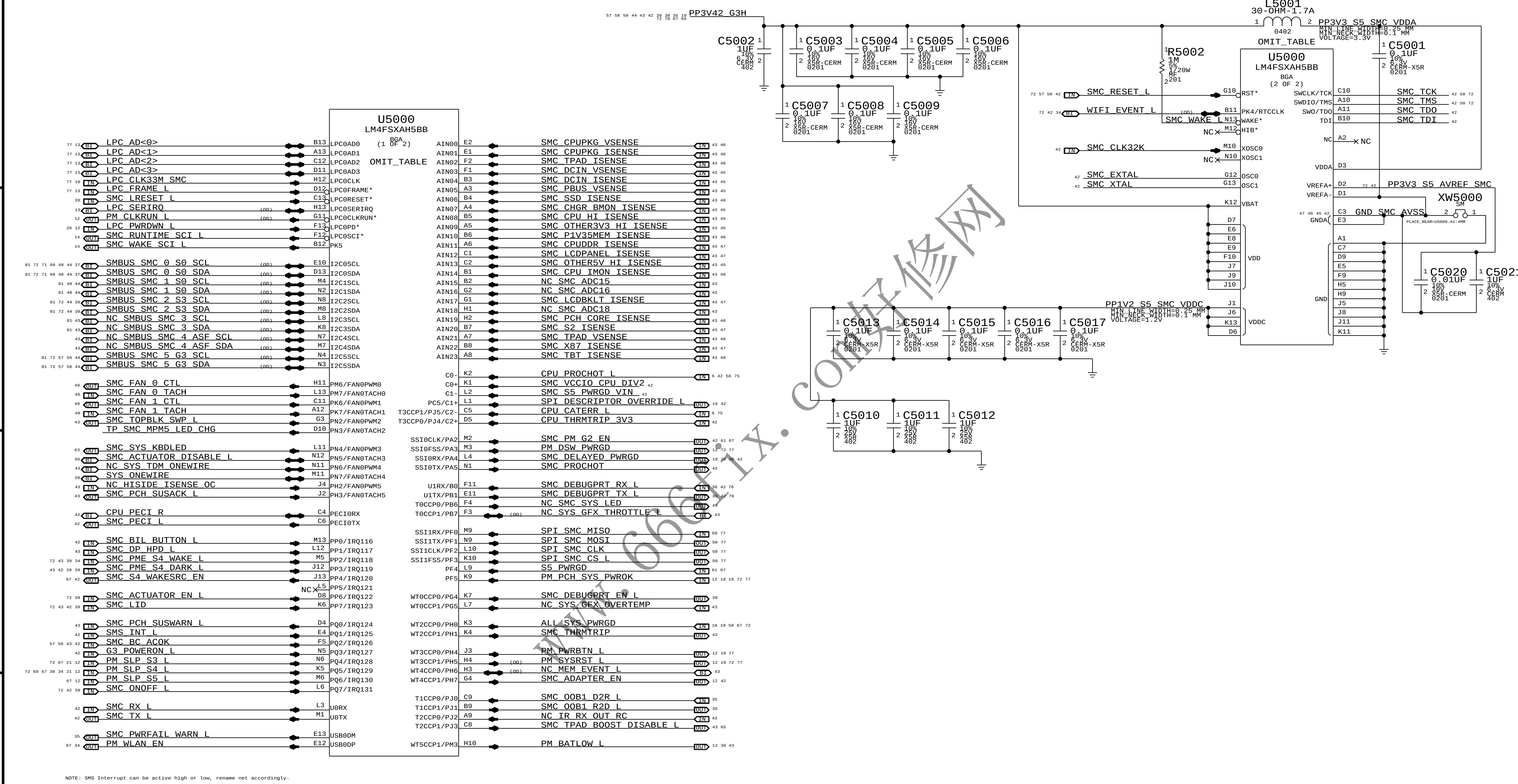
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/15/2014

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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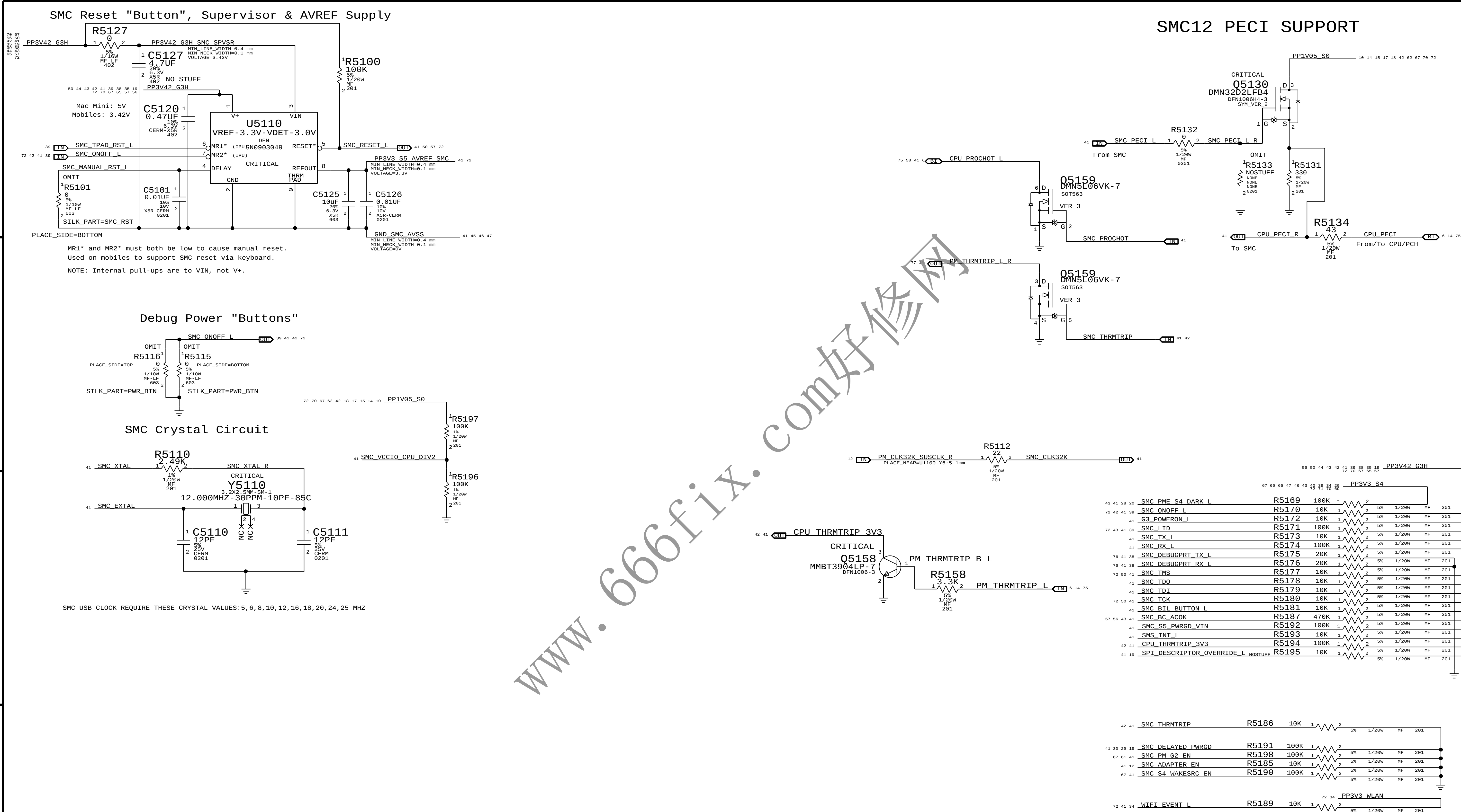

SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE

SMC Shared Support

Apple Inc.

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REVISION <E4LABEL>

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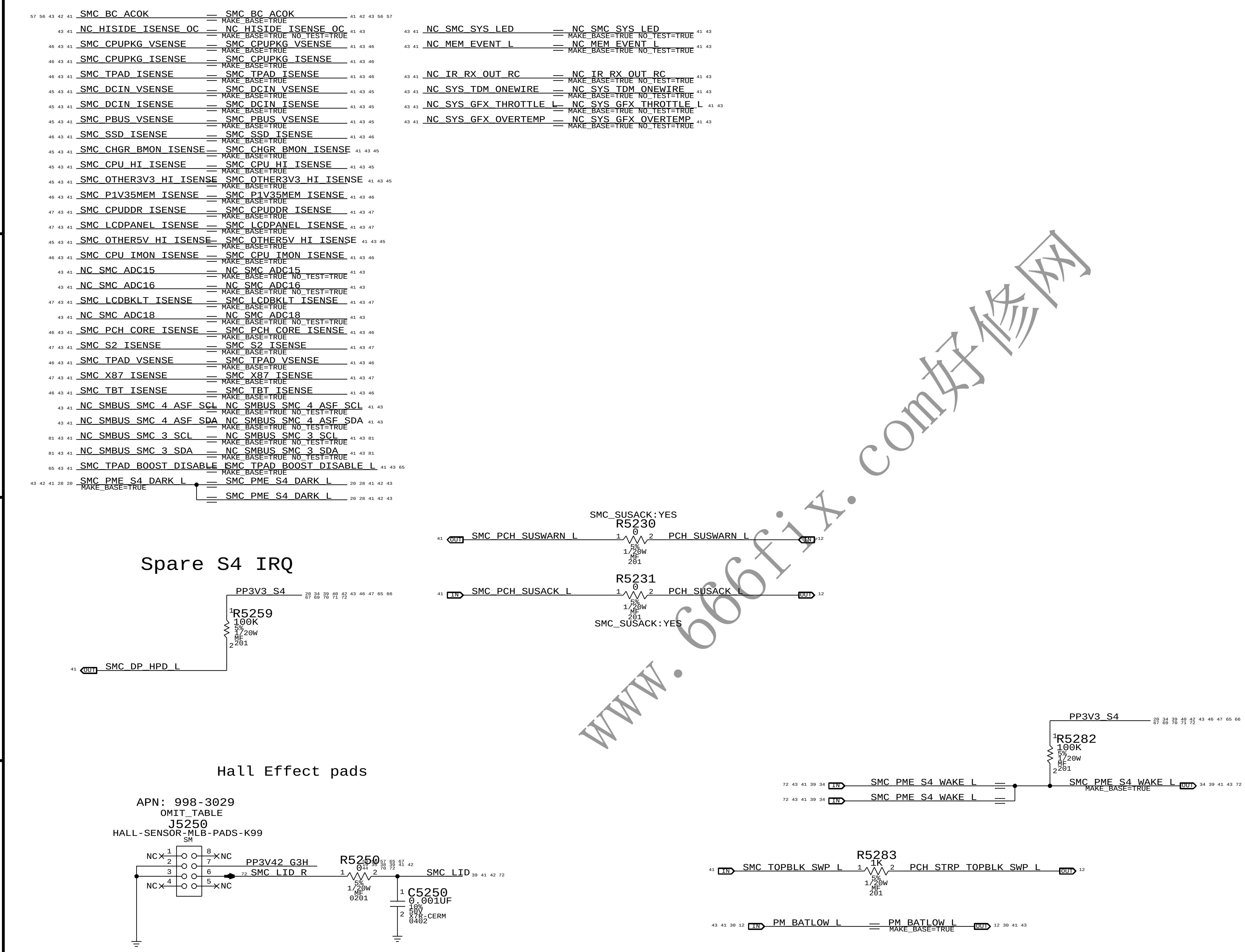

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	

PAGE TITLE
SMC Project Support

Apple Inc.

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REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 52 OF 118
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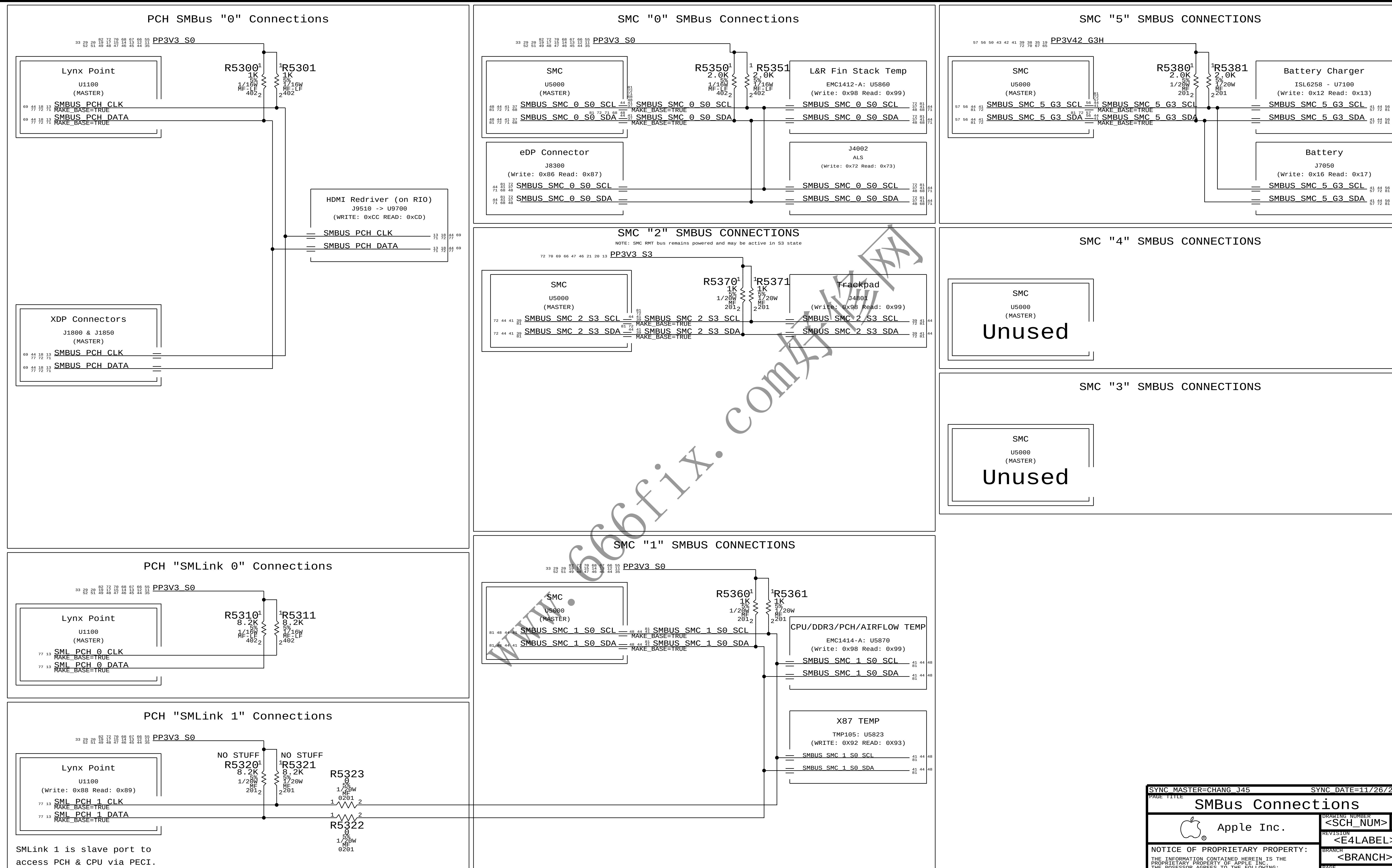

SYNC_MASTER=CHANG_J45 SYNC_DATE=11/26/2012

PAGE TITLE
SMBus Connections

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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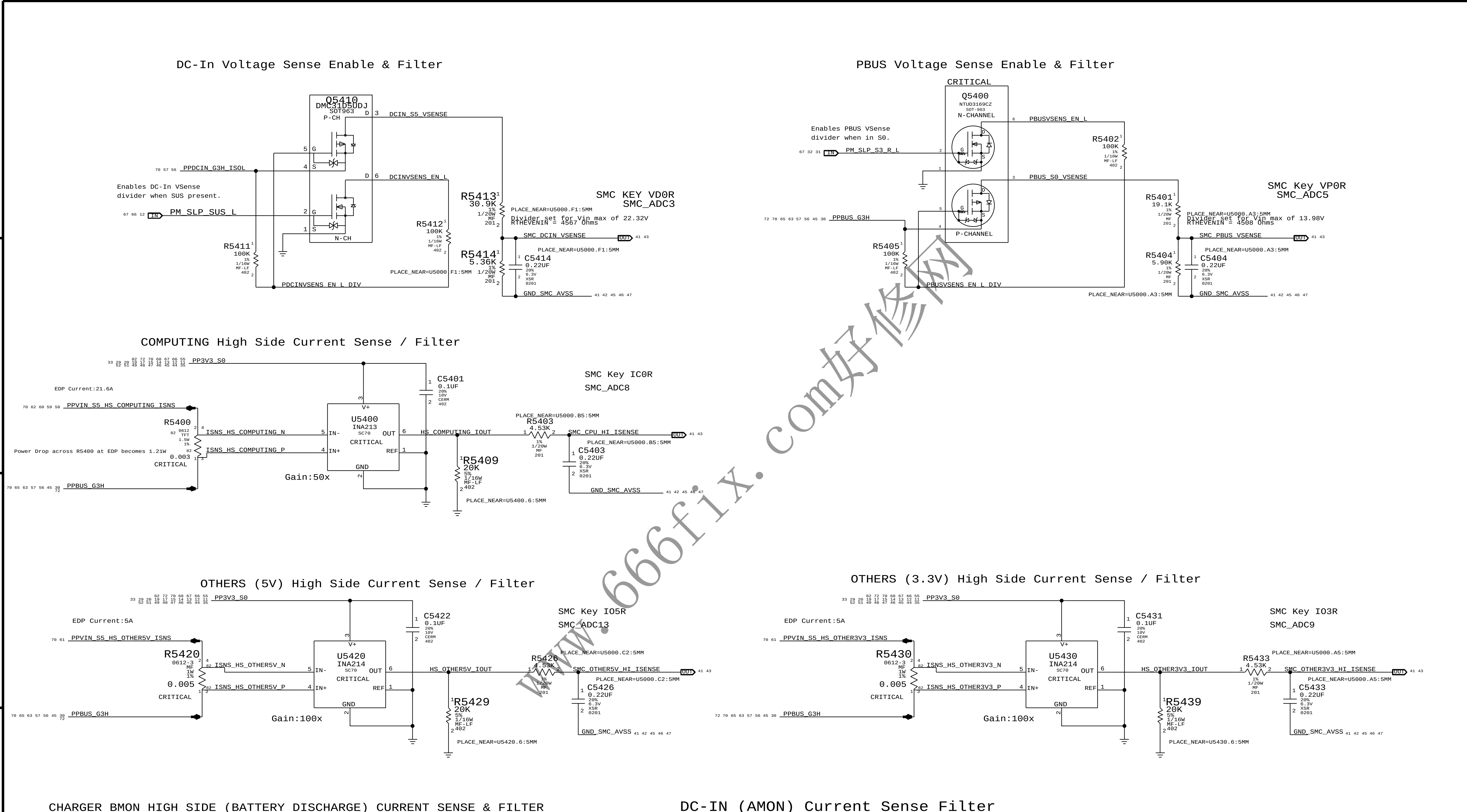


SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

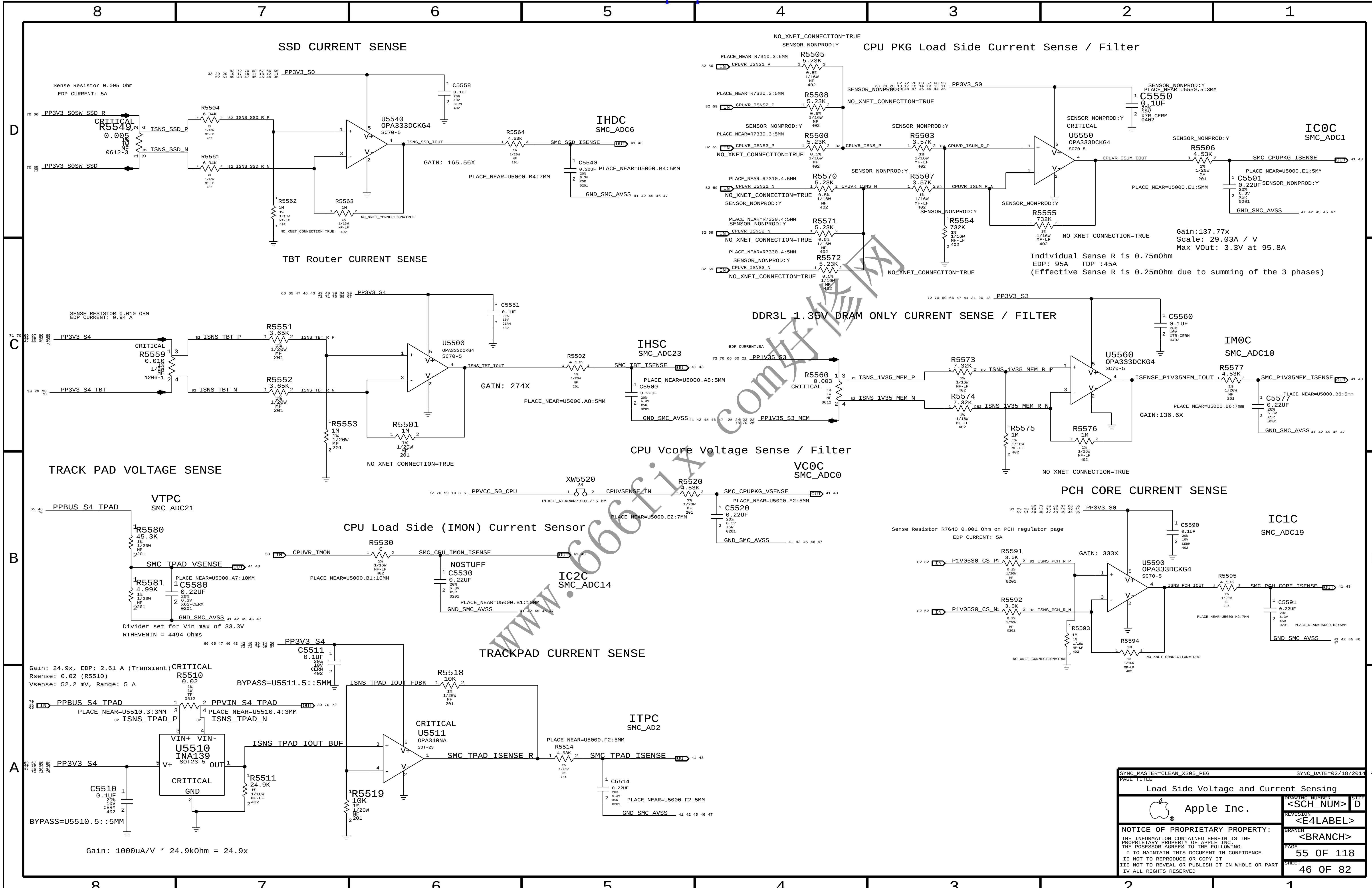
PAGE TITLE
High Side Voltage and Current Sensing

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>



SSD CURRENT SENSE
Sense Resistor 0.005 Ohm
EDP CURRENT: 5A
PP3V3_S0SW_SSD_R
PP3V3_S0SW_SSD
CRITICAL
R5549
0.005
ISNS_SSD_P
ISNS_SSD_N
R5504
R5561
6.04K
PP3V3_S0
C5558
0.1UF
U5540
OPA333DCKG4
SC70-5
ISNS_SSD_IOUT
R5564
4.53K
SMC_SSD_ISENSE
IHDC
SMC_ADC6
GAIN: 165.56X
C5540
0.22UF
PLACE_NEAR=U5000.B4:7MM
PLACE_NEAR=U5000.B4:5MM
GND_SMC_AVSS
R5562
1M
R5563
1M
NO_XNET_CONNECTION=TRUE
TBT Router CURRENT SENSE
SENSE RESISTOR 0.010 OHM
EDP CURRENT: 0.94 A
PP3V3_S4
CRITICAL
R5559
0.010
PP3V3_S4_TBT
R5551
3.65K
ISNS_TBT_P
R5552
3.65K
ISNS_TBT_N
C5551
0.1UF
U5500
OPA333DCKG4
SC70-5
ISNS_TBT_IOUT
R5502
4.53K
SMC_TBT_ISENSE
IHSC
SMC_ADC23
GAIN: 274X
C5500
0.22UF
PLACE_NEAR=U5000.A8:5MM
PLACE_NEAR=U5000.A8:5MM
R5553
1M
R5501
1M
NO_XNET_CONNECTION=TRUE
TRACK PAD VOLTAGE SENSE
PPBUS_S4_TPAD
VTPC
SMC_ADC21
R5580
45.3K
SMC_TPAD_VSENSE
R5581
4.99K
C5580
0.22UF
PLACE_NEAR=U5000.A7:10MM
GND_SMC_AVSS
Divider set for Vin max of 33.3V
RTHEVENIN = 4494 Ohms
CPU Load Side (IMON) Current Sensor
CPUVR_IMON
R5530
0
SMC_CPU_IMON_ISENSE
NOSTUFF
C5530
0.22UF
IC2C
SMC_ADC14
PLACE_NEAR=U5000.B1:10MM
PLACE_NEAR=U5000.B1:10MM
TRACKPAD CURRENT SENSE
Gain: 24.9x, EDP: 2.61 A (Transient)
Rsense: 0.02 (R5510)
Vsense: 52.2 mV, Range: 5 A
CRITICAL
R5510
0.02
PPBUS_S4_TPAD
PPVIN_S4_TPAD
PLACE_NEAR=U5510.3:3MM
PLACE_NEAR=U5510.4:3MM
ISNS_TPAD_P
ISNS_TPAD_N
C5511
0.1UF
BYPASS=U5511.5::5MM
ISNS_TPAD_IOUT_FDBK
R5518
10K
U5510
INA139
SOT23-5
CRITICAL
ISNS_TPAD_IOUT_BUF
CRITICAL
U5511
OPA340NA
SOT-23
SMC_TPAD_ISENSE_R
R5514
4.53K
SMC_TPAD_ISENSE
ITPC
SMC_AD2
PLACE_NEAR=U5000.F2:5MM
C5514
0.22UF
PLACE_NEAR=U5000.F2:5MM
C5510
0.1UF
BYPASS=U5510.5::5MM
R5511
24.9K
R5519
10K
Gain: 1000uA/V * 24.9kOhm = 24.9x
CPU PKG Load Side Current Sense / Filter
NO_XNET_CONNECTION=TRUE
SENSOR_NONPROD:Y
CPUVR_ISNS1_P
CPUVR_ISNS2_P
CPUVR_ISNS3_P
CPUVR_ISNS1_N
CPUVR_ISNS2_N
CPUVR_ISNS3_N
R5505
R5508
R5500
R5570
R5571
R5572
5.23K
CPUVR_ISNS_P
CPUVR_ISNS_N
R5503
R5507
3.57K
CPUVR_ISUM_R_P
CPUVR_ISUM_R_N
C5550
0.1UF
U5550
OPA333DCKG4
SC70-5
CPUVR_ISUM_IOUT
R5506
4.53K
SMC_CPUPKG_ISENSE
IC0C
SMC_ADC1
C5501
0.22UF
PLACE_NEAR=U5000.E1:5MM
R5554
732K
R5555
732K
Gain:137.77x
Scale: 29.03A / V
Max VOut: 3.3V at 95.8A
Individual Sense R is 0.75mOhm
EDP: 95A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 phases)
DDR3L 1.35V DRAM ONLY CURRENT SENSE / FILTER
PP3V3_S3
C5560
0.1UF
EDP CURRENT:8A
PP1V35_S3
R5560
0.003
CRITICAL
PP1V35_S3_MEM
R5573
7.32K
ISNS_1V35_MEM_P
R5574
7.32K
ISNS_1V35_MEM_N
U5560
OPA333DCKG4
SC70-5
ISENSE_P1V35MEM_IOUT
R5577
4.53K
SMC_P1V35MEM_ISENSE
IM0C
SMC_ADC10
C5577
0.22UF
PLACE_NEAR=U5000.B6:7mm
PLACE_NEAR=U5000.B6:5mm
GAIN:136.6X
R5575
1M
R5576
1M
CPU Vcore Voltage Sense / Filter
PPVCC_S0_CPU
XW5520
SM
PLACE_NEAR=R7310.2:5 MM
CPUVSENSE_IN
R5520
4.53K
SMC_CPUPKG_VSENSE
VC0C
SMC_ADC0
C5520
0.22UF
PLACE_NEAR=U5000.E2:5MM
PLACE_NEAR=U5000.E2:7MM
PCH CORE CURRENT SENSE
PP3V3_S0
C5590
0.1UF
Sense Resistor R7640 0.001 Ohm on PCH regulator page
EDP CURRENT: 5A
GAIN: 333X
IC1C
SMC_ADC19
P1V05S0_CS_P
P1V05S0_CS_N
R5591
3.0K
R5592
3.0K
ISNS_PCH_R_P
ISNS_PCH_R_N
U5590
OPA333DCKG4
SC70-5
ISNS_PCH_IOUT
R5595
4.53K
SMC_PCH_CORE_ISENSE
C5591
0.22UF
R5593
1M
R5594
1M
SYNC_MASTER=CLEAN_X305_PEG
SYNC_DATE=02/18/2014
PAGE TITLE
Load Side Voltage and Current Sensing
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
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REVISION
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<BRANCH>
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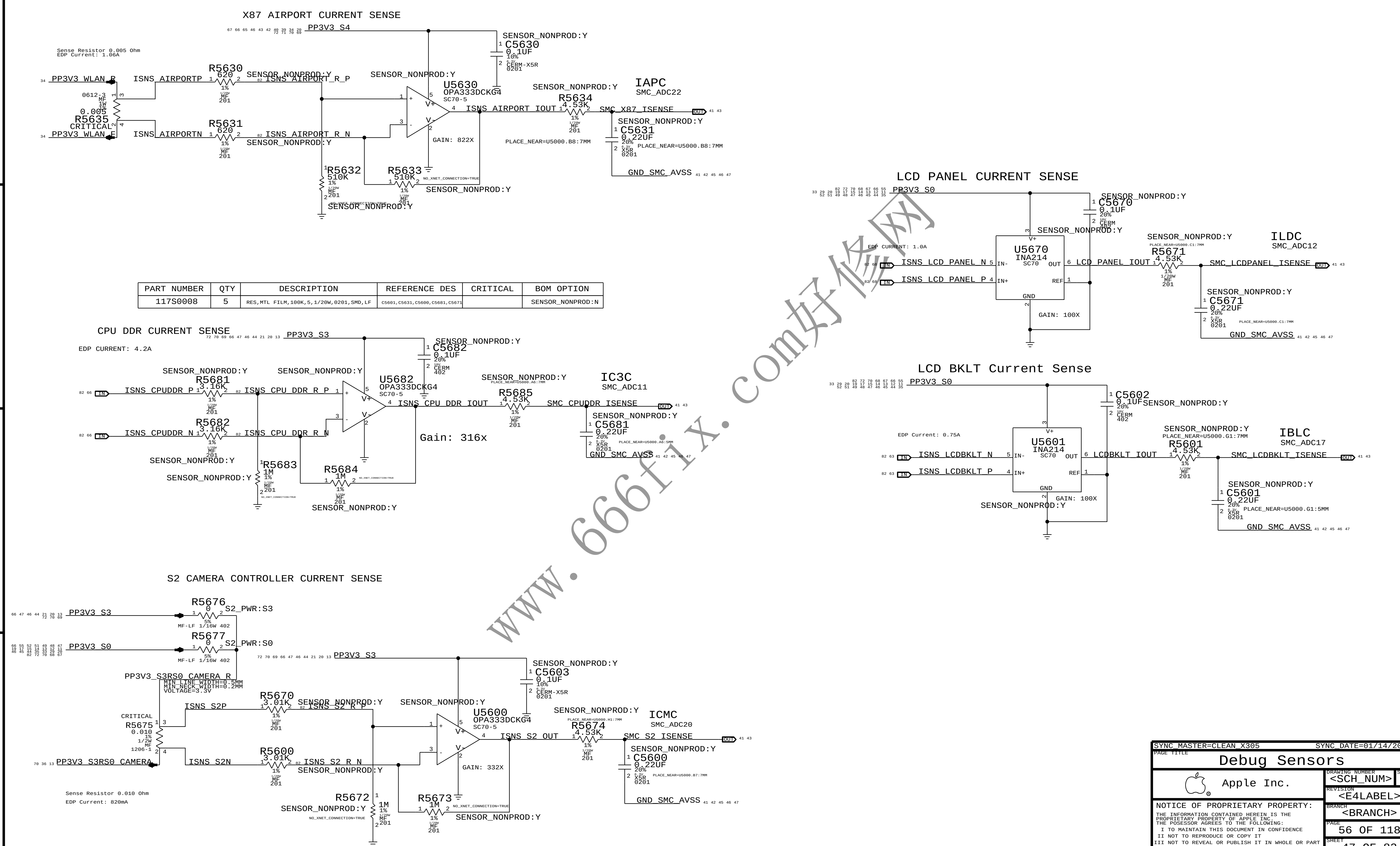

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF	C5601,C5631,C5600,C5681,C5671		SENSOR_NONPROD:N

SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/14/2014

PAGE TITLE

Debug Sensors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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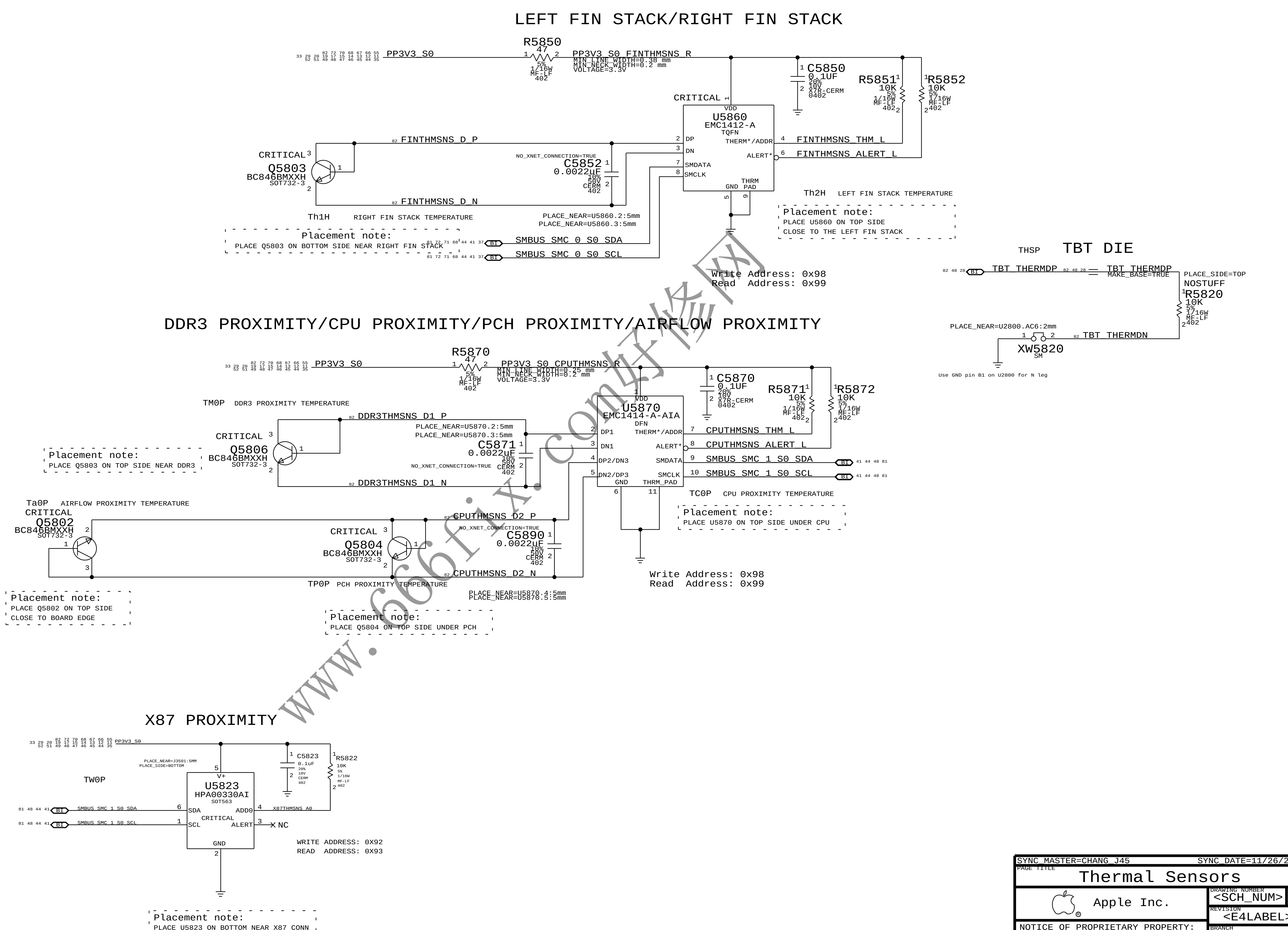
8 7 6 5 4 3 2 1



SYNC_MASTER=CHANG_J45 SYNC_DATE=11/26/2012

PAGE TITLE

Thermal Sensors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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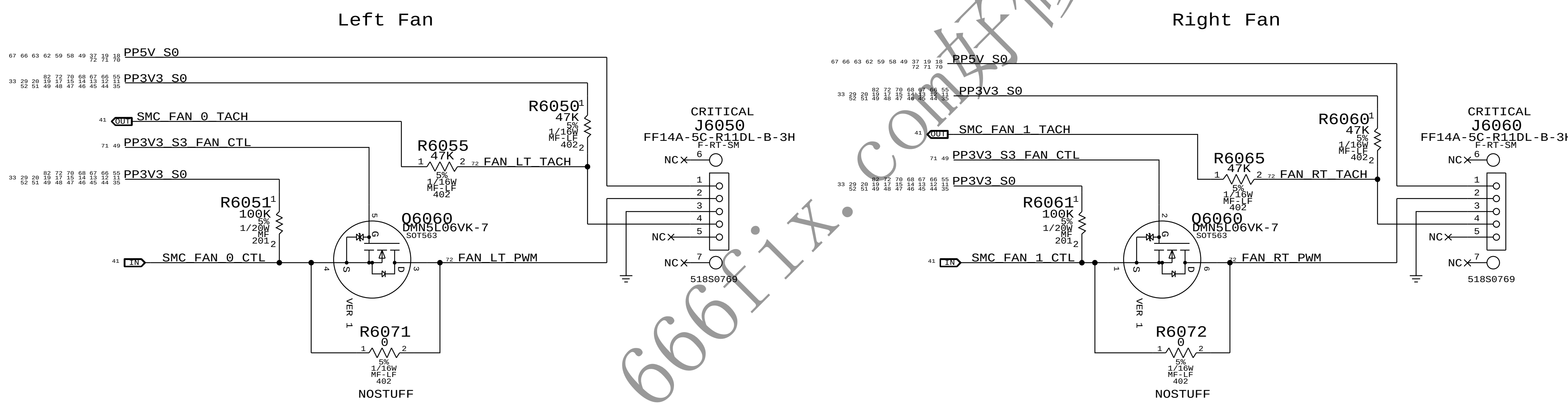

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PAGE TITLE

Fan Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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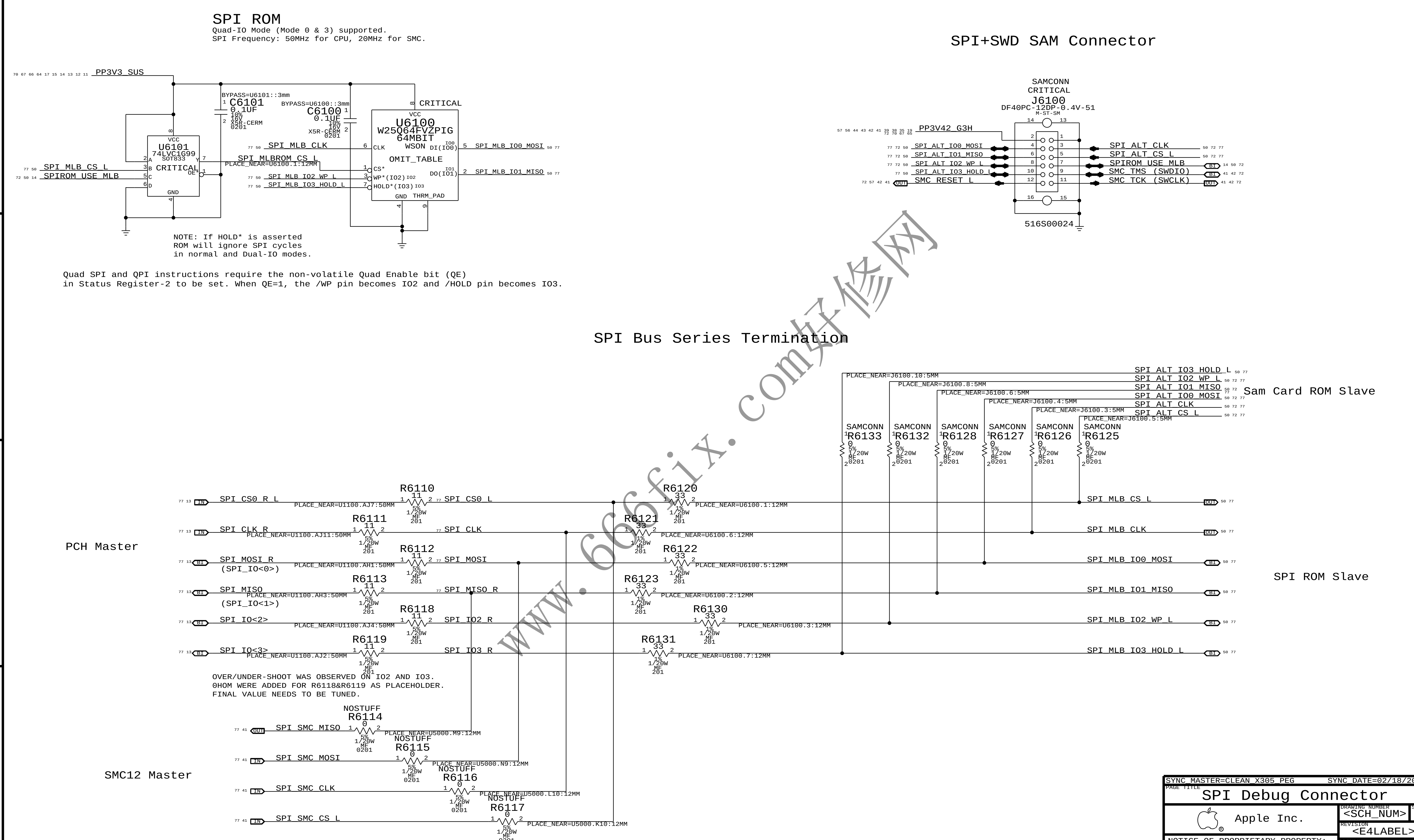

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE

SPI Debug Connector

Apple Inc.

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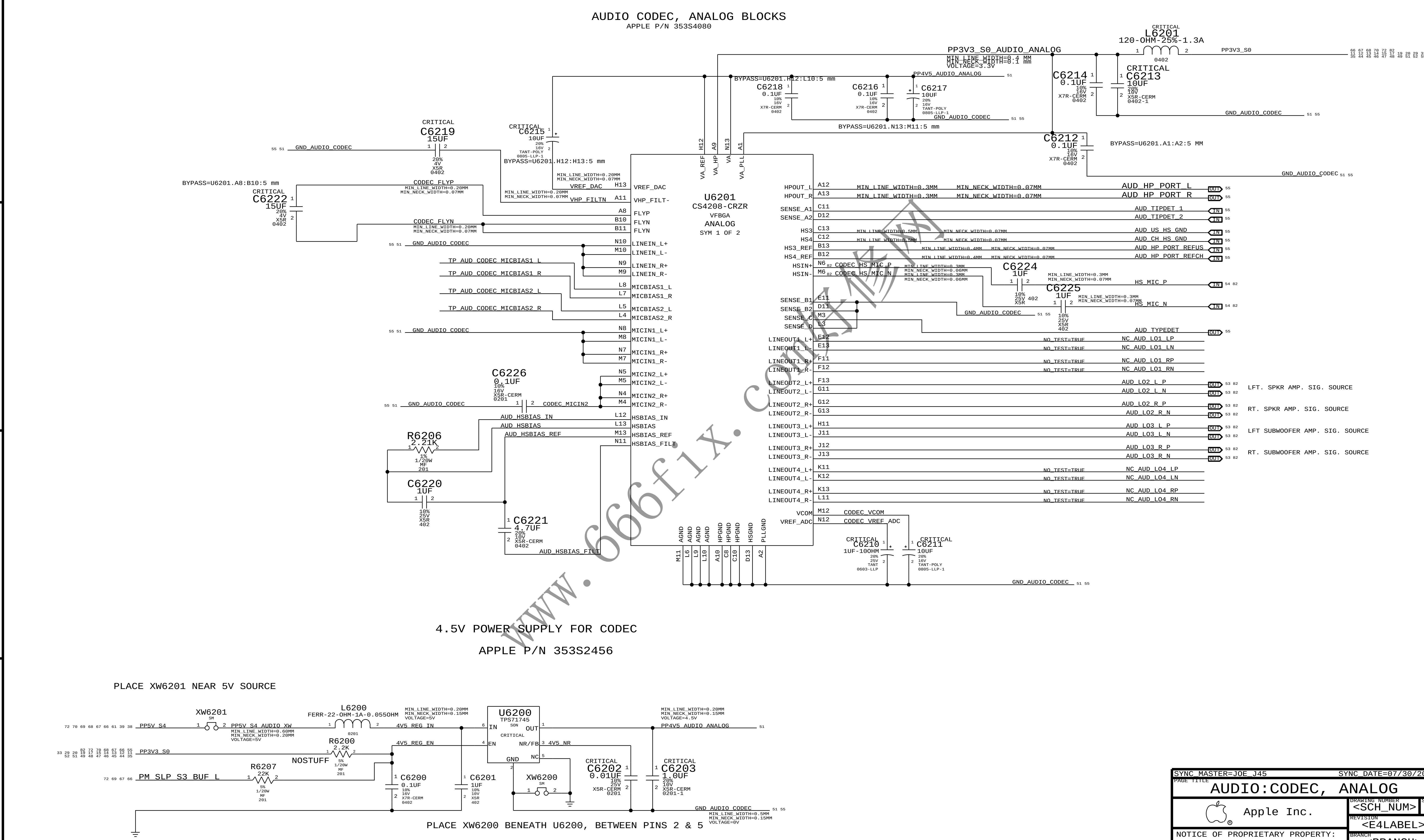
AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080



SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE

AUDIO:CODEC, ANALOG

Apple Inc.

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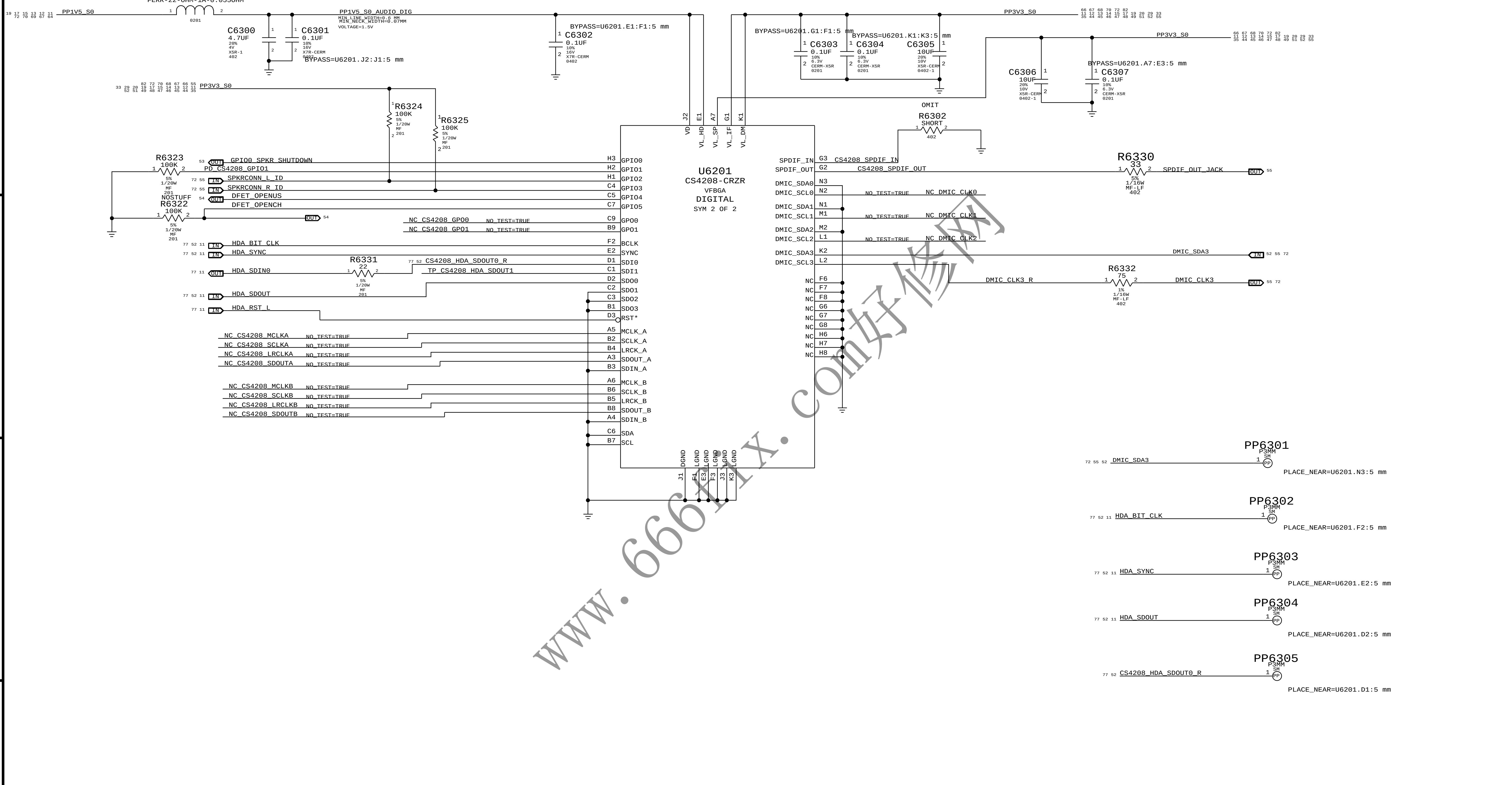
AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080



SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE

AUDIO:CODEC, DIGITAL

Apple Inc.

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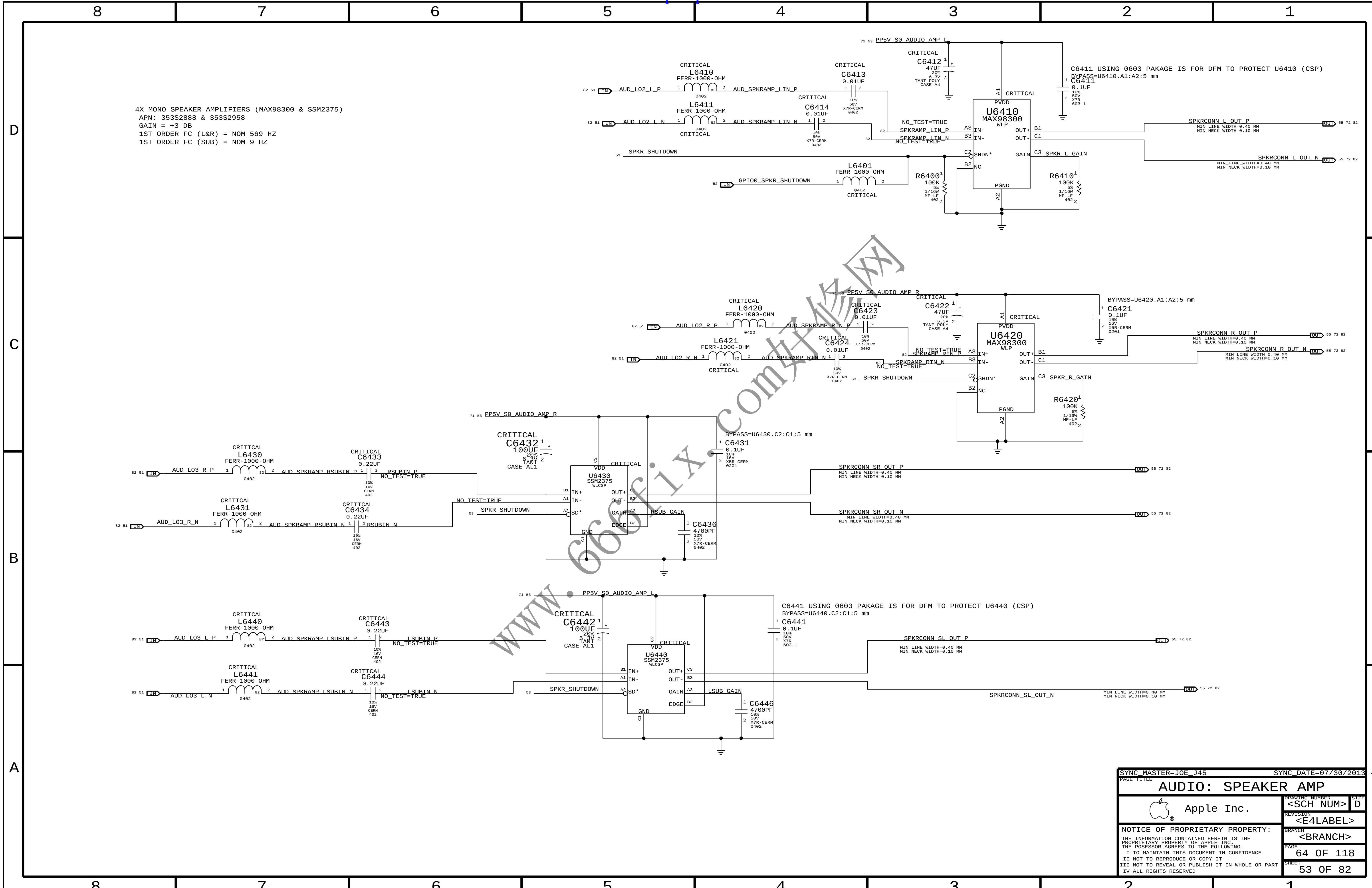
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ
PP5V_S0_AUDIO_AMP_L
C6411 USING 0603 PAKAGE IS FOR DFM TO PROTECT U6410 (CSP)
BYPASS=U6410.A1:A2:5 mm
CRITICAL
L6410
FERR-1000-OHM
AUD_LO2_L_P
AUD_SPKRAMP_LIN_P
L6411
AUD_LO2_L_N
AUD_SPKRAMP_LIN_N
C6413
0.01UF
C6414
0.01UF
C6412
47UF
C6411
0.1UF
U6410
MAX98300
WLP
NO_TEST=TRUE
SPKRAMP_LIN_P
SPKRAMP_LIN_N
SPKR_SHUTDOWN
L6401
GPIO0_SPKR_SHUTDOWN
R6400
100K
R6410
100K
SPKR_L_GAIN
SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
MIN_LINE_WIDTH=0.40 MM
MIN_NECK_WIDTH=0.10 MM
PP5V_S0_AUDIO_AMP_R
BYPASS=U6420.A1:A2:5 mm
L6420
AUD_LO2_R_P
AUD_SPKRAMP_RIN_P
L6421
AUD_LO2_R_N
AUD_SPKRAMP_RIN_N
C6422
47UF
C6423
0.01UF
C6424
0.01UF
C6421
0.1UF
U6420
MAX98300
SPKRAMP_RIN_P
SPKRAMP_RIN_N
SPKR_R_GAIN
R6420
100K
SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
BYPASS=U6430.C2:C1:5 mm
C6432
100UF
C6431
0.1UF
L6430
AUD_LO3_R_P
AUD_SPKRAMP_RSUBIN_P
C6433
0.22UF
RSUBIN_P
L6431
AUD_LO3_R_N
AUD_SPKRAMP_RSUBIN_N
C6434
0.22UF
RSUBIN_N
U6430
SSM2375
WLCSP
RSUB_GAIN
C6436
4700PF
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N
PP5V_S0_AUDIO_AMP_L
C6441 USING 0603 PAKAGE IS FOR DFM TO PROTECT U6440 (CSP)
BYPASS=U6440.C2:C1:5 mm
C6442
100UF
C6441
0.1UF
L6440
AUD_LO3_L_P
AUD_SPKRAMP_LSUBIN_P
C6443
0.22UF
LSUBIN_P
L6441
AUD_LO3_L_N
AUD_SPKRAMP_LSUBIN_N
C6444
0.22UF
LSUBIN_N
U6440
SSM2375
LSUB_GAIN
C6446
4700PF
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N
SYNC_MASTER=JOE_J45
SYNC_DATE=07/30/2013
AUDIO: SPEAKER AMP
Apple Inc.
<SCH_NUM>
D
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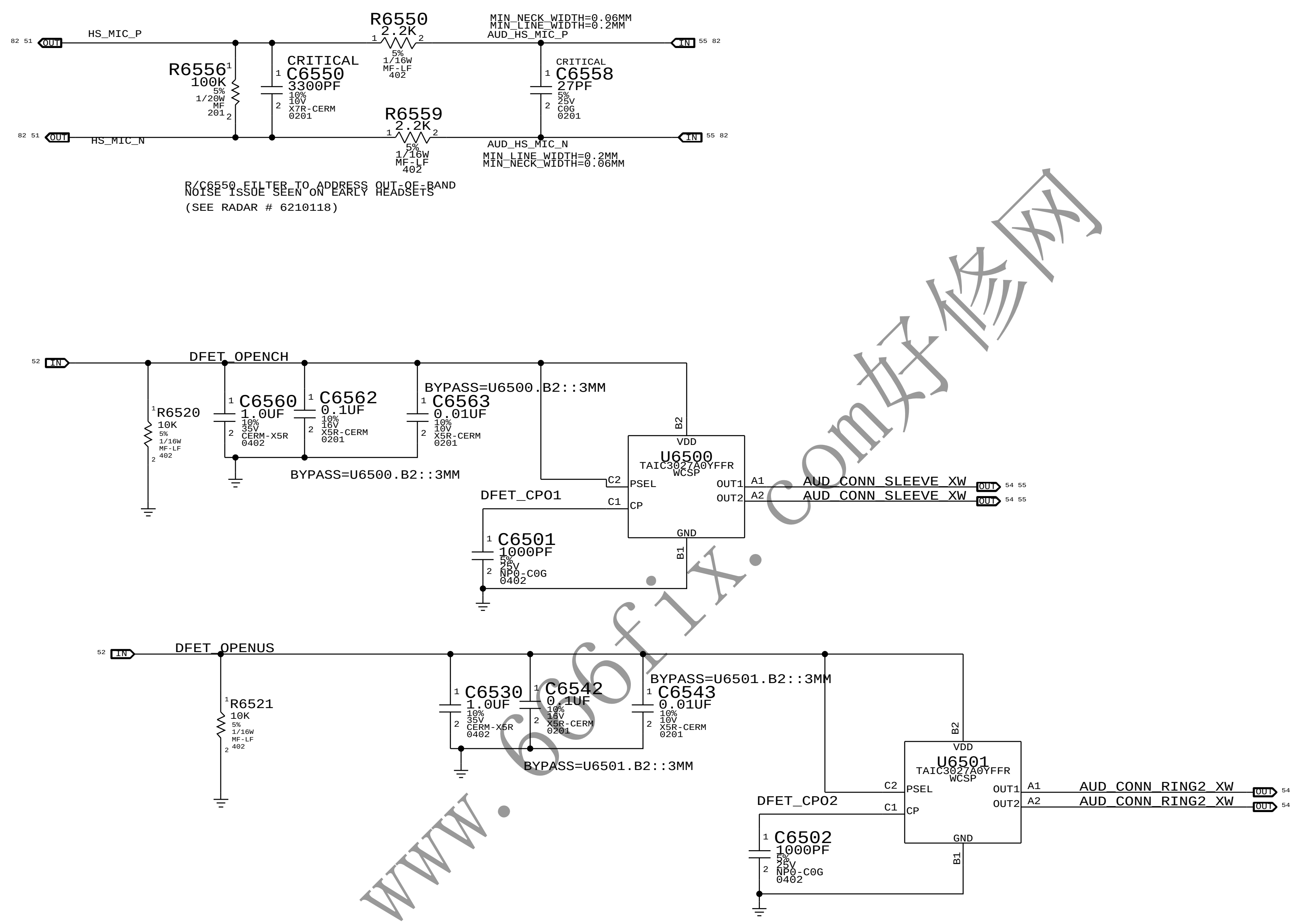

SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE

AUDIO: JACK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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CODEC OUTPUT SIGNAL PATHS

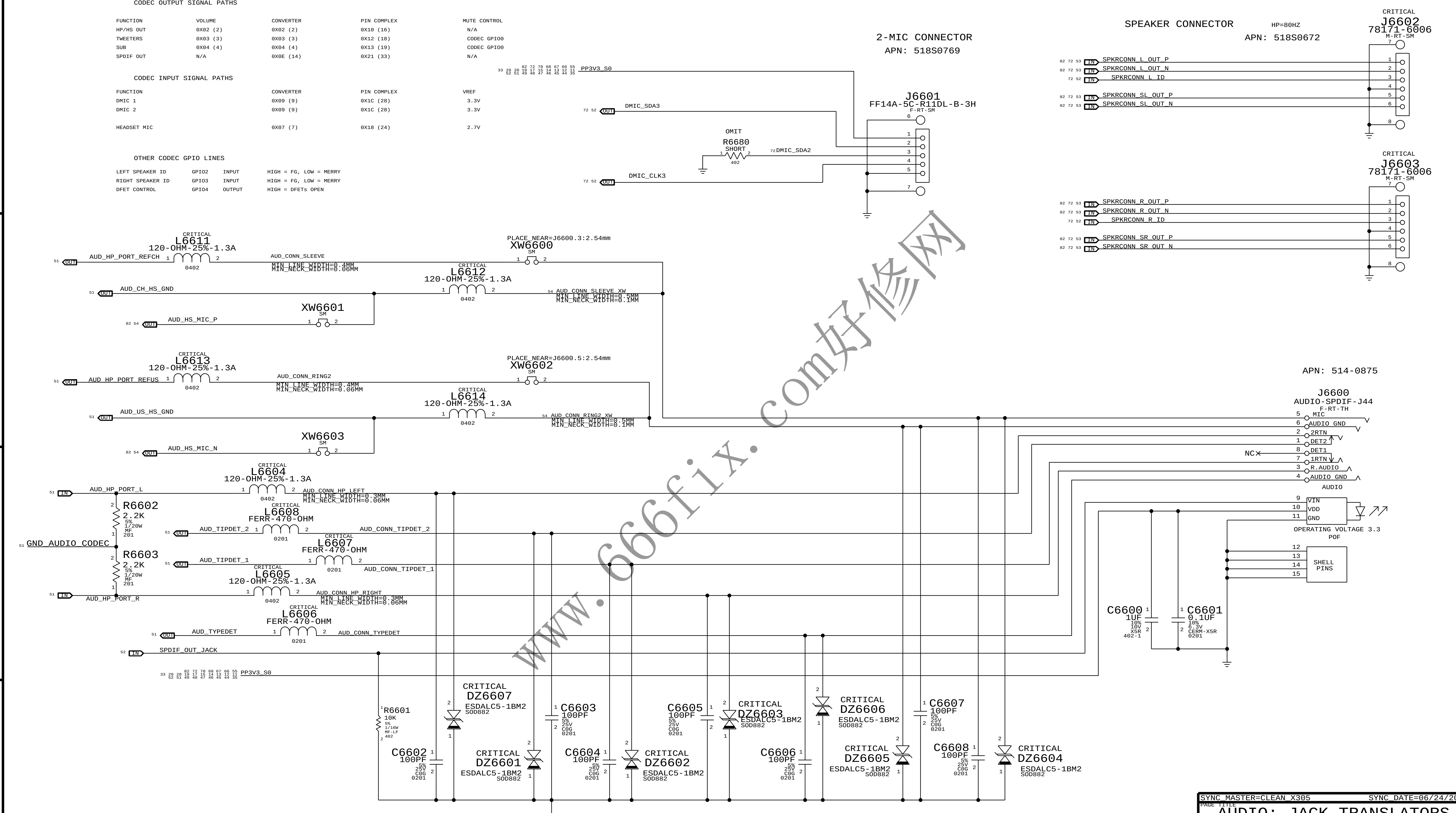
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN



SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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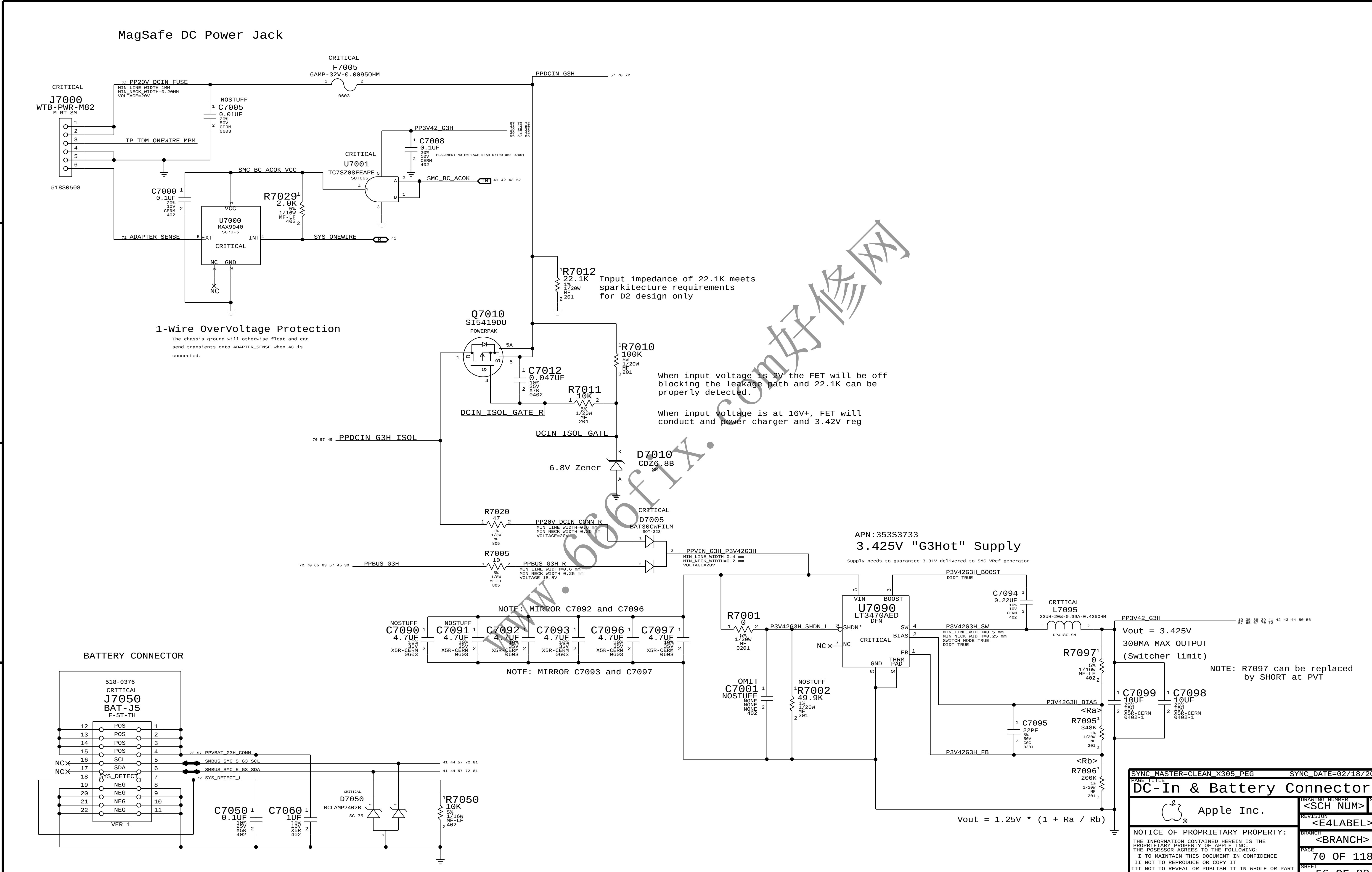

MagSafe DC Power Jack
CRITICAL
J7000
WTB-PWR-M82
M-RT-SM
518S0508
PP20V_DCIN_FUSE
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=20V
CRITICAL
F7005
6AMP-32V-0.0095OHM
0603
PPDCIN_G3H
NOSTUFF
C7005
0.01UF
20%
50V
CERM
0603
TP_TDM_ONEWIRE_MPM
PP3V42_G3H
C7008
0.1UF
20%
10V
CERM
402
PLACEMENT_NOTE=PLACE NEAR U7100 and U7001
CRITICAL
U7001
TC7SZ08FEAPE
SOT665
SMC_BC_ACOK
SMC_BC_ACOK_VCC
C7000
0.1UF
20%
10V
CERM
402
R7029
2.0K
5%
1/16W
MF-LF
402
U7000
MAX9940
SC70-5
VCC
EXT
INT
CRITICAL
NC
GND
ADAPTER_SENSE
SYS_ONEWIRE
1-Wire OverVoltage Protection
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.
R7012
22.1K
1%
1/20W
MF
201
Input impedance of 22.1K meets sparkitecture requirements for D2 design only
Q7010
SI5419DU
POWERPAK
R7010
100K
5%
1/20W
MF
201
C7012
0.047UF
10%
25V
X7R
0402
R7011
10K
5%
1/20W
MF
201
DCIN_ISOL_GATE_R
DCIN_ISOL_GATE
When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.
When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg
PPDCIN_G3H_ISOL
D7010
CDZ6.8B
SM
6.8V Zener
R7020
47
1%
1/3W
MF
805
PP20V_DCIN_CONN_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=20V
CRITICAL
D7005
BAT30CWFILM
SOT-323
PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=20V
R7005
10
5%
1/8W
MF-LF
805
PPBUS_G3H
PPBUS_G3H_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V
APN:353S3733
3.425V "G3Hot" Supply
Supply needs to guarantee 3.31V delivered to SMC VRef generator
NOTE: MIRROR C7092 and C7096
C7090 C7091 C7092 C7093 C7096 C7097
4.7UF
10%
35V
X5R-CERM
0603
NOTE: MIRROR C7093 and C7097
R7001
0
5%
1/20W
MF
0201
P3V42G3H_SHDN_L
U7090
LT3470AED
DFN
VIN
BOOST
SHDN*
NC
SW
BIAS
FB
CRITICAL
GND
THRM PAD
P3V42G3H_BOOST
DIDT=TRUE
C7094
0.22UF
10%
10V
CERM
402
CRITICAL
L7095
33UH-20%-0.39A-0.435OHM
DP418C-SM
P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE
PP3V42_G3H
Vout = 3.425V
300MA MAX OUTPUT
(Switcher limit)
R7097
0
5%
1/16W
MF-LF
402
NOTE: R7097 can be replaced by SHORT at PVT
OMIT
C7001
NOSTUFF
NONE
402
NOSTUFF
R7002
49.9K
1%
1/20W
MF
201
C7099
10UF
20%
10V
X5R-CERM
0402-1
C7098
10UF
20%
10V
X5R-CERM
0402-1
P3V42G3H_BIAS
<Ra>
R7095
348K
1%
1/20W
MF
201
C7095
22PF
5%
50V
C0G
0201
P3V42G3H_FB
<Rb>
R7096
200K
1%
1/20W
MF
201
Vout = 1.25V * (1 + Ra / Rb)
BATTERY CONNECTOR
518-0376
CRITICAL
J7050
BAT-J5
F-ST-TH
POS
SCL
SDA
SYS_DETECT
NEG
VER 1
PPVBAT_G3H_CONN
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
SYS_DETECT_L
C7050
0.1UF
10%
25V
X5R
402
C7060
1UF
10%
16V
X5R
402
CRITICAL
D7050
RCLAMP2402B
SC-75
R7050
10K
5%
1/16W
MF-LF
402
SYNC_MASTER=CLEAN_X305_PEG
SYNC_DATE=02/18/2014
PAGE TITLE
DC-In & Battery Connectors
Apple Inc.
DRAWING NUMBER
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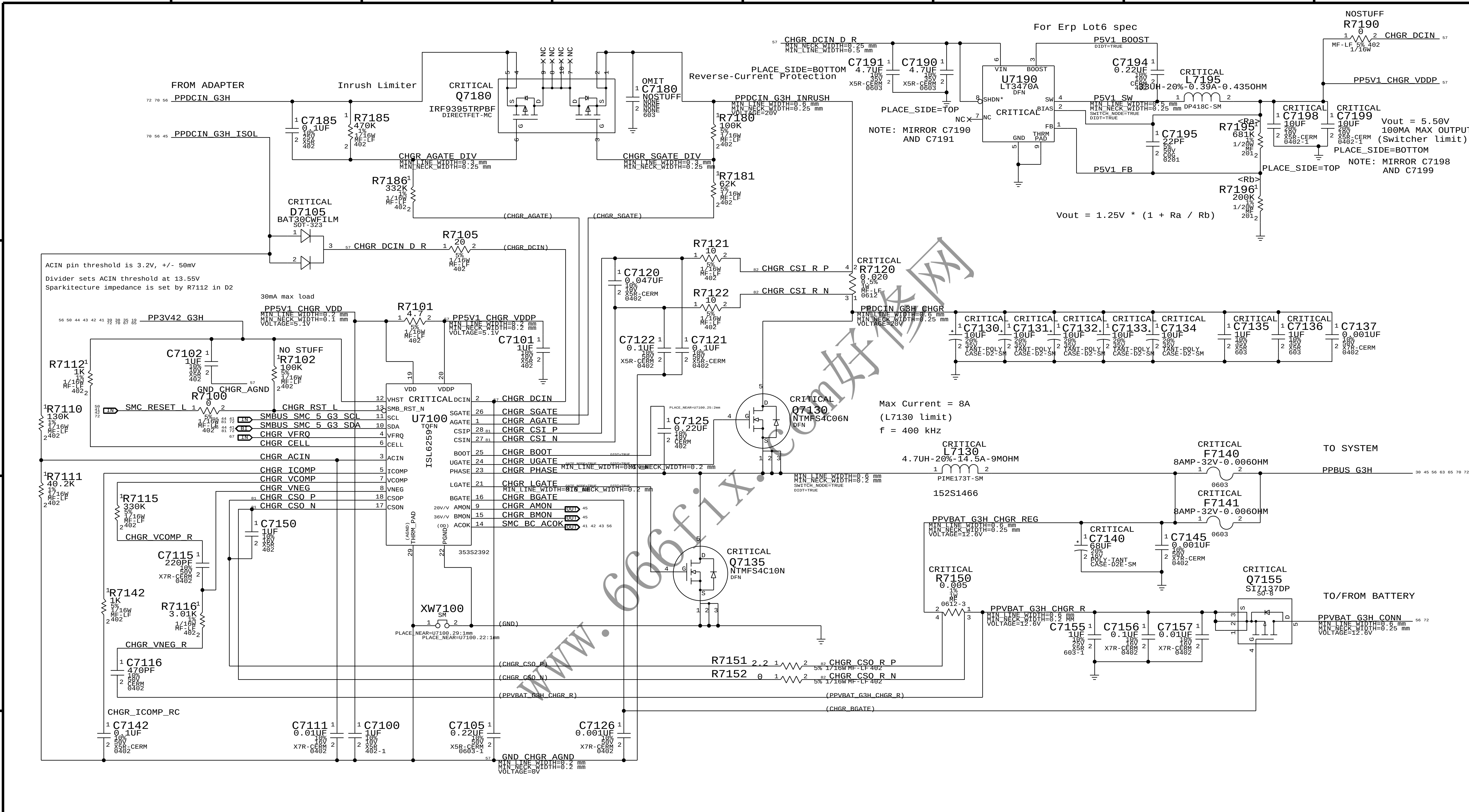

SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/15/2014

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

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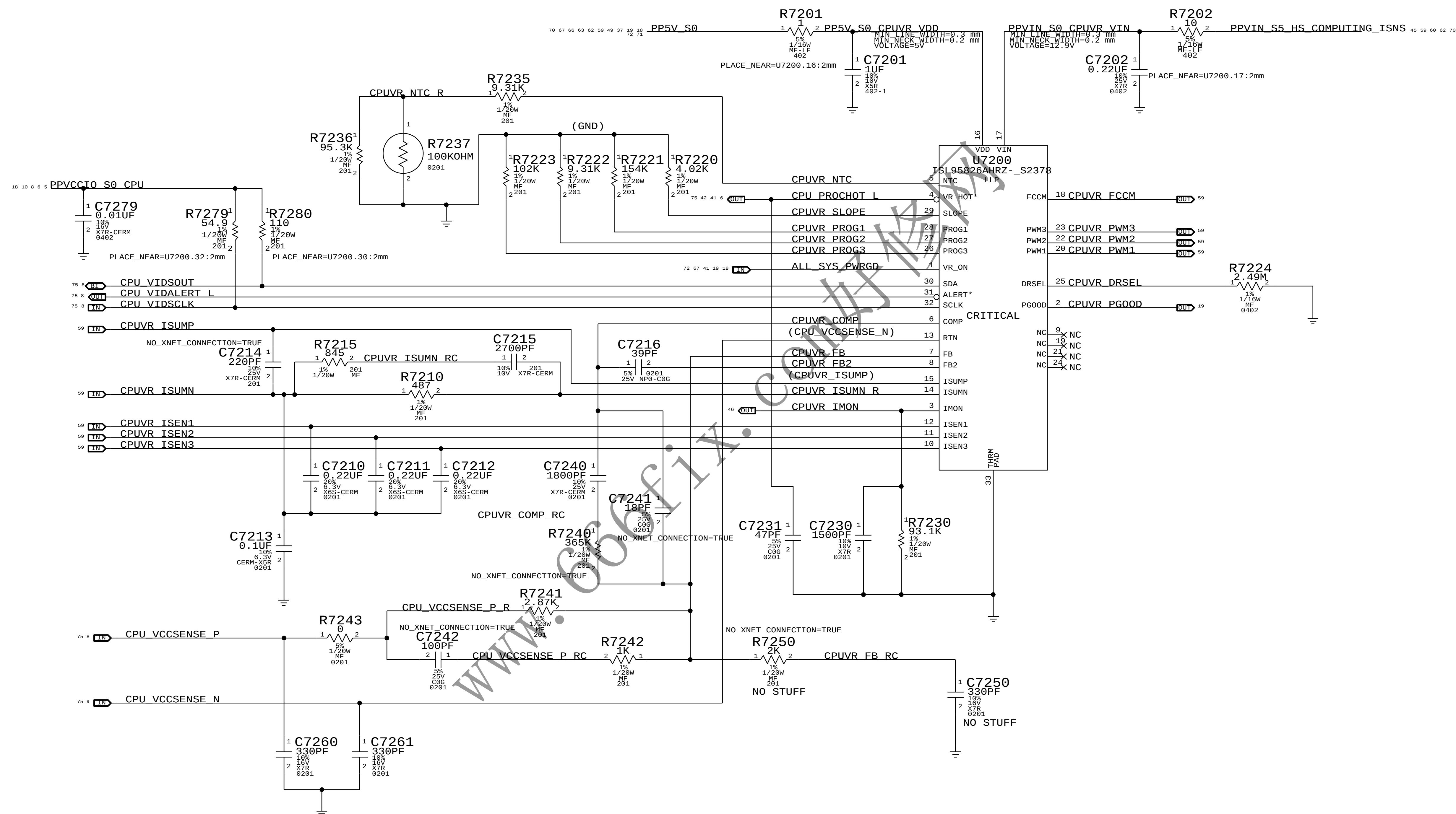
Laptopblue



SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/24/2014

PAGE TITLE

CPU VR12.5 VCC Regulator IC

DRAWING NUMBER <SCH_NUM> SIZE D

Apple Inc.

REVISION <E4LABEL>

BRANCH <BRANCH>

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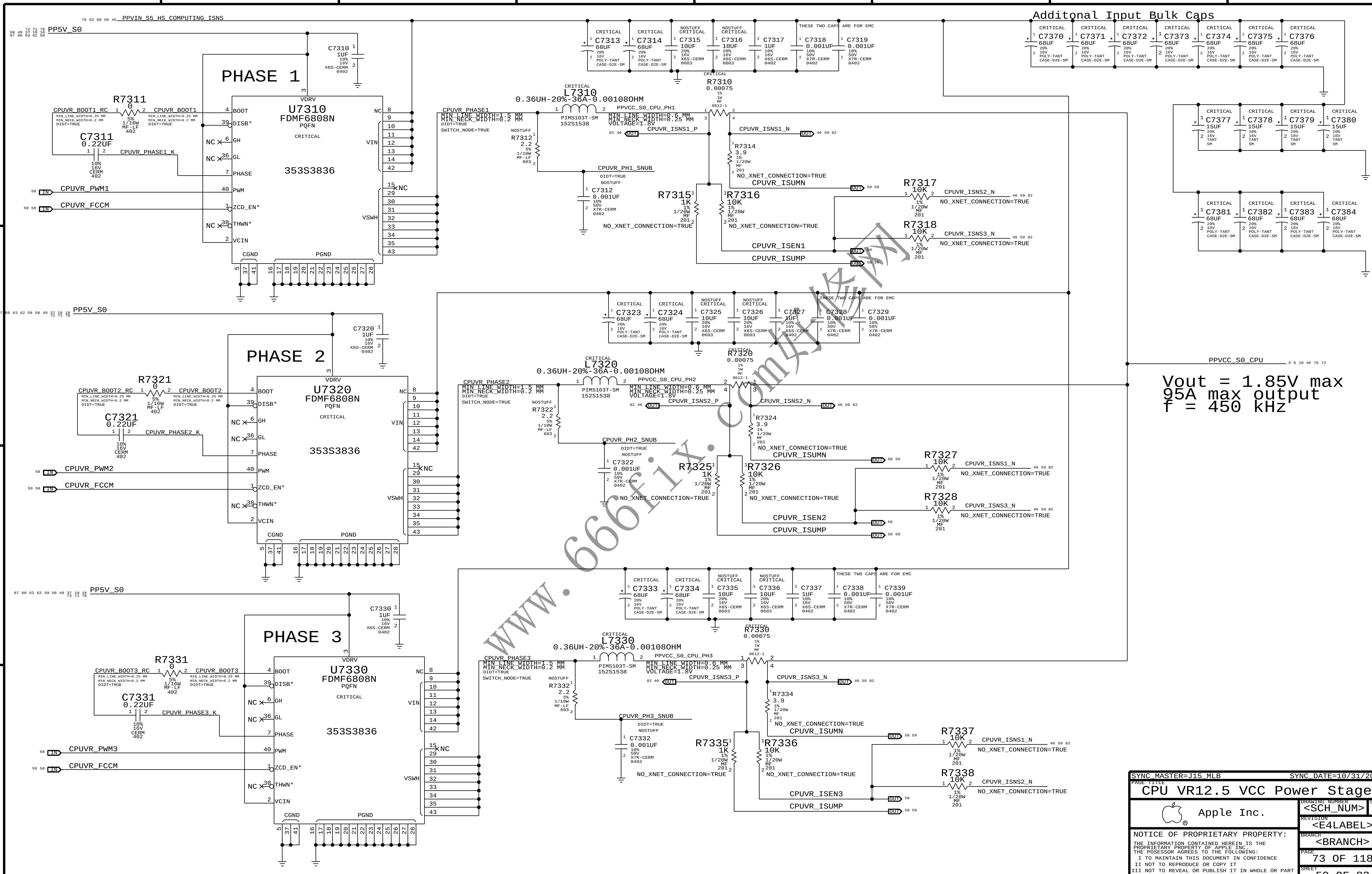
SHEET 58 OF 82



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

CPU VR12.5 VCC Power Stage

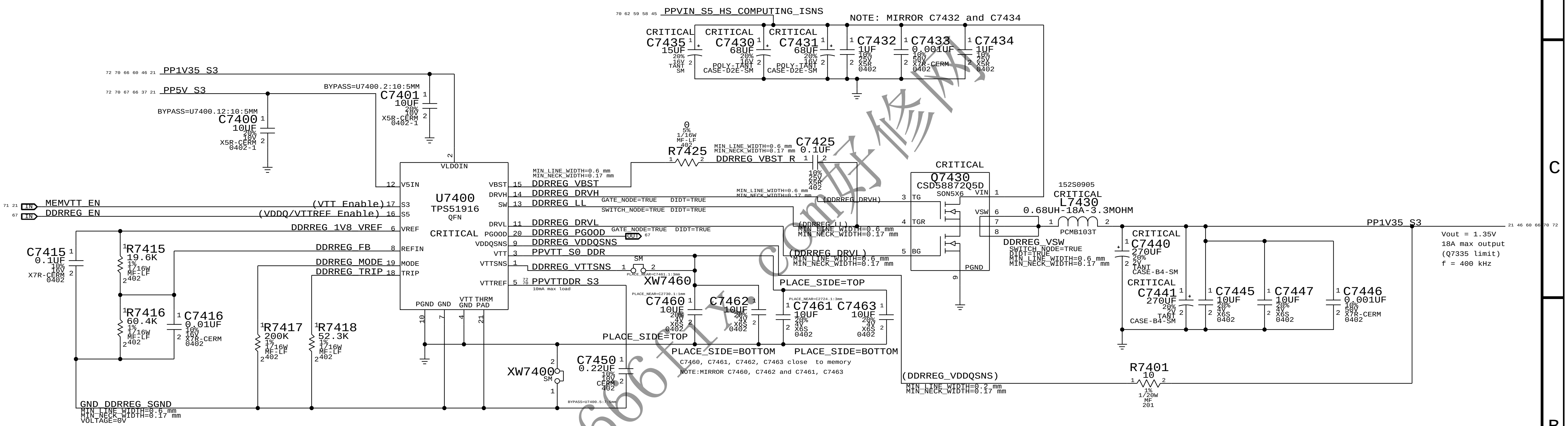
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

DDR3L (1V35 S3) REGULATOR



SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/15/2014

PAGE TITLE

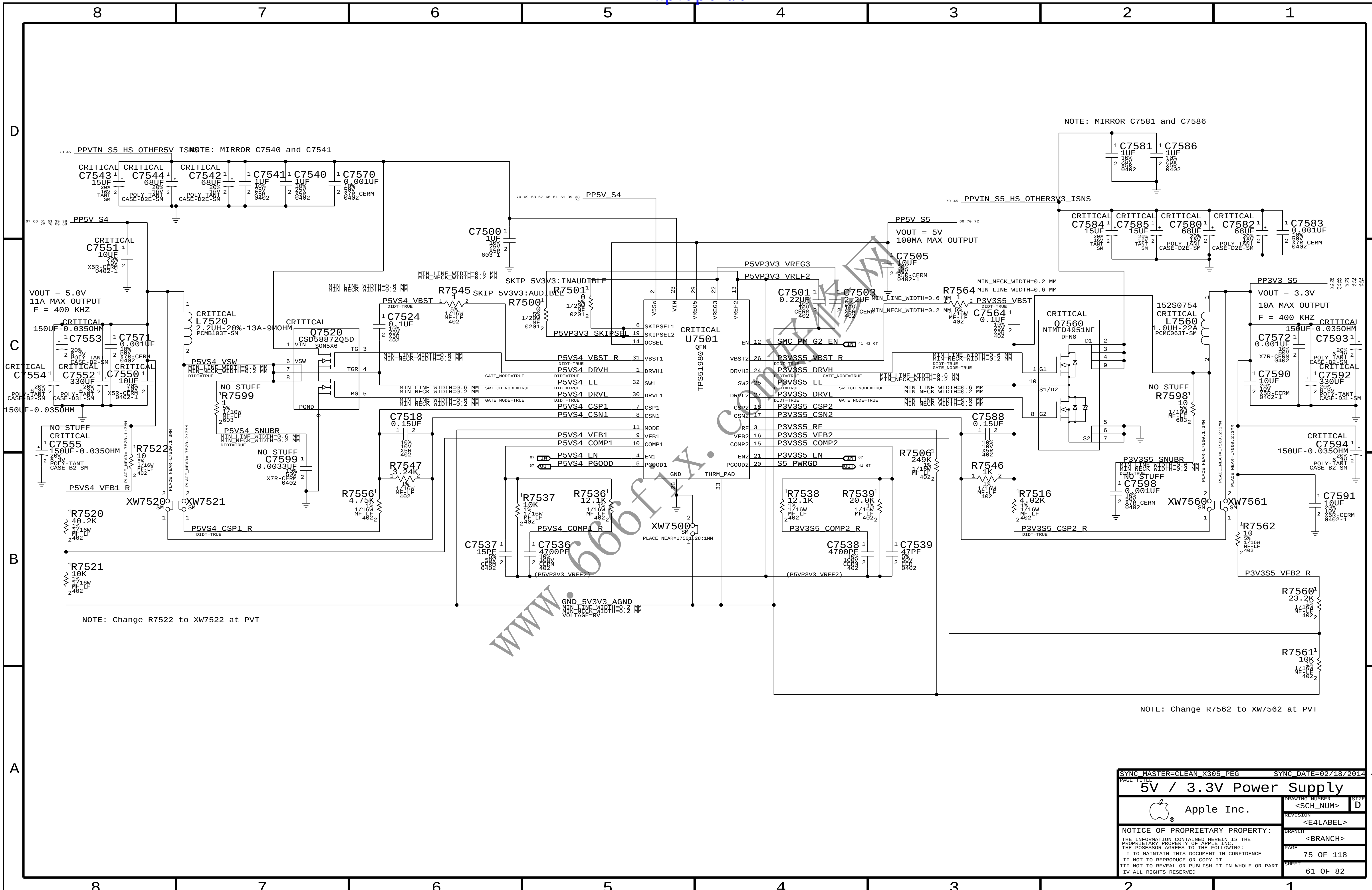
1.35V DDR3L SUPPLY

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>



NOTE: MIRROR C7540 and C7541
PPVIN_S5_HS_OTHER5V_ISNS
PP5V_S4
VOUT = 5.0V
11A MAX OUTPUT
F = 400 KHZ
CRITICAL
C7543 15UF
C7544 68UF
C7542 68UF
C7541 1UF
C7540 1UF
C7570 0.001UF
C7551 10UF
C7553 150UF-0.035OHM
C7571 0.001UF
C7554 150UF-0.035OHM
C7552 330UF
C7550 10UF
C7555 150UF-0.035OHM
NO STUFF
L7520 2.2UH-20%-13A-9MOHM
PCMB103T-SM
Q7520 CSD58872Q5D
SON5X6
P5VS4_VSW
R7599 1
P5VS4_SNUBR
C7599 0.0033UF
R7522 10
XW7520
XW7521
P5VS4_VFB1_R
R7520 40.2K
R7521 10K
P5VS4_CSP1_R
NOTE: Change R7522 to XW7522 at PVT
C7500 1UF
P5VS4_VBST
R7545 1
C7524 0.1UF
SKIP_5V3V3:INAUDIBLE
SKIP_5V3V3:AUDIBLE
R7501 0
R7500 0
P5VP3V3_SKIPSEL
P5VS4_VBST_R
P5VS4_DRVH
P5VS4_LL
P5VS4_DRVL
P5VS4_CSP1
P5VS4_CSN1
C7518 0.15UF
R7547 3.24K
R7556 4.75K
P5VS4_VFB1
P5VS4_COMP1
P5VS4_EN
P5VS4_PGOOD
R7537 10K
R7536 12.1K
P5VS4_COMP1_R
C7537 15PF
C7536 4700PF
(P5VP3V3_VREF2)
GND_5V3V3_AGND
VOLTAGE=0V
CRITICAL
U7501
TPS51980
QFN
XW7500
PLACE_NEAR=U7501.28:1MM
P5VP3V3_VREG3
P5VP3V3_VREF2
PP5V_S5
VOUT = 5V
100MA MAX OUTPUT
C7505 10UF
C7501 0.22UF
C7503 2.2UF
SMC_PM_G2_EN
P3V3S5_VBST_R
P3V3S5_DRVH
P3V3S5_LL
P3V3S5_DRVL
P3V3S5_CSP2
P3V3S5_CSN2
P3V3S5_RF
P3V3S5_VFB2
P3V3S5_COMP2
P3V3S5_EN
S5_PWRGD
R7538 12.1K
R7539 20.0K
P3V3S5_COMP2_R
C7538 4700PF
C7539 47PF
R7506 249K
R7564 1
P3V3S5_VBST
C7564 0.1UF
C7588 0.15UF
R7546 1K
R7516 4.02K
P3V3S5_CSP2_R
Q7560
NTMFD4951NF
DFN8
NOTE: MIRROR C7581 and C7586
C7581 1UF
C7586 1UF
PPVIN_S5_HS_OTHER3V3_ISNS
C7584 15UF
C7585 15UF
C7580 68UF
C7582 68UF
C7583 0.001UF
152S0754
L7560 1.0UH-22A
PCMC063T-SM
PP3V3_S5
VOUT = 3.3V
10A MAX OUTPUT
F = 400 KHZ
C7572 0.001UF
C7593 150UF-0.035OHM
C7590 10UF
C7592 330UF
R7598 10
P3V3S5_SNUBR
C7598 0.001UF
XW7560
XW7561
C7594 150UF-0.035OHM
C7591 10UF
R7562 10
P3V3S5_VFB2_R
R7560 23.2K
R7561 10K
NOTE: Change R7562 to XW7562 at PVT
SYNC_MASTER=CLEAN_X305_PEG
SYNC_DATE=02/18/2014
PAGE TITLE
5V / 3.3V Power Supply
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
75 OF 118
SHEET
61 OF 82
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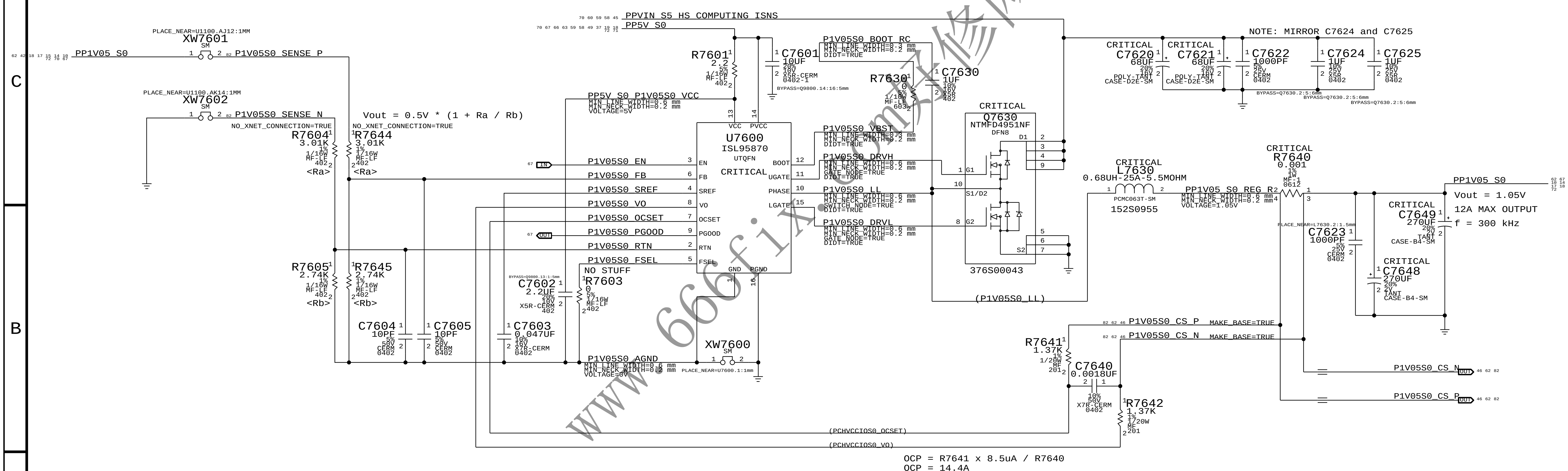
1V05 S0 REGULATOR



SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE
1V05V POWER SUPPLY

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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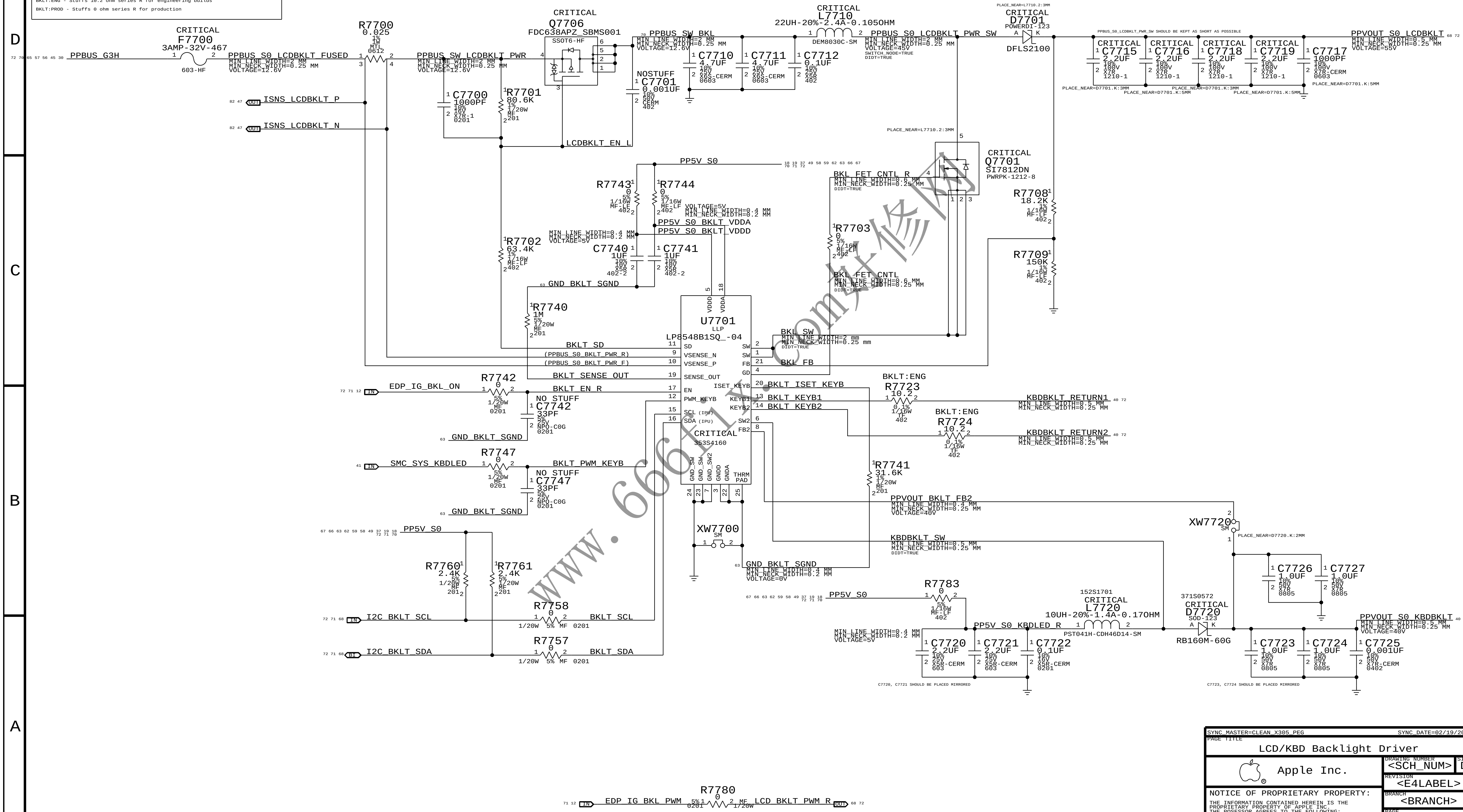
SHEET 62 OF 82

Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7723,R7724		BKLT:PROD



SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/19/2014

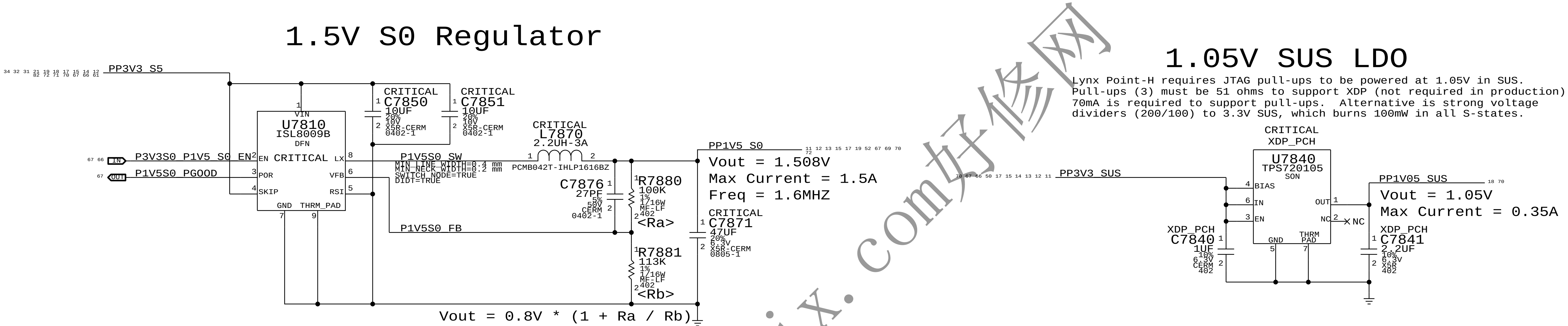
PAGE TITLE: LCD/KBD Backlight Driver

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>



SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/15/2014

PAGE TITLE

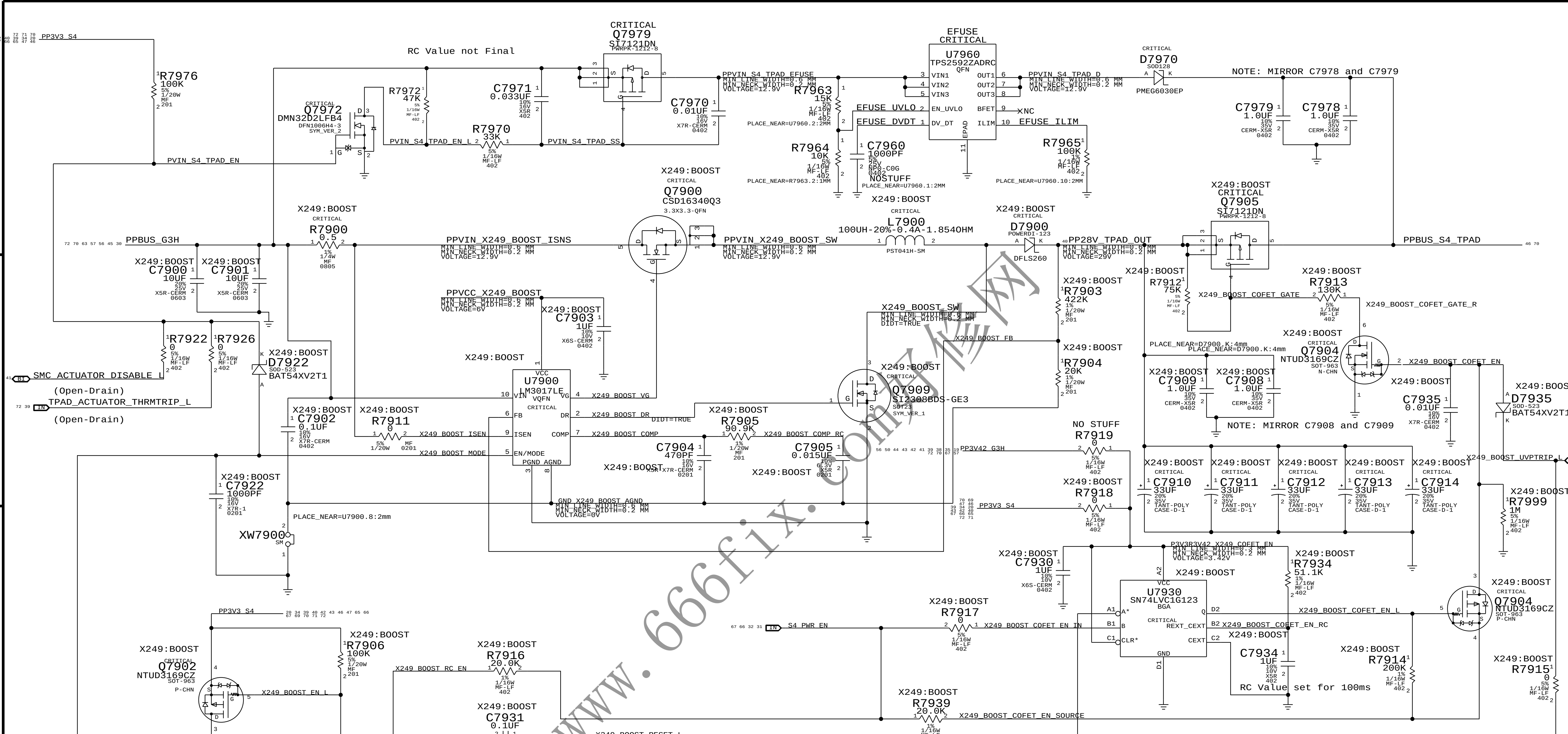
Misc Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>



BOOST CONTROL INPUTS (X249:BOOST BOM OPTION)

SYSTEM STATE	=X249_BOOST_EN (PM_SLP_S*_L)	SMC_ACTUATOR_DISABLE_L	TPAD_ACTUATOR_THRMTRIP_L	X249_BOOST_MODE	BOOST OUTPUT	X249 POWER
G3H, S5	0 V	X	X	0 V	0 V (OFF)	0 V
S4, S3, S0	0 V	Hi-Z	Hi-Z	0 V	0 V (OFF)	PBUS
S4, S3, S0	3.3 V	Hi-Z	Hi-Z	1.8 V	28 V (BOOST)	28 V
S4, S3, S0	X	0 V	X	0 V	0 V (OFF)	0 V
S4, S3, S0	X	X	0 V	0 V	0 V (OFF)	0 V

PBUS ONLY CONTROL INPUTS

SYSTEM STATE	SMC_ACTUATOR_DISABLE_L	TPAD_ACTUATOR_THRMTRIP_L	X249 POWER
G3H, S5	X	X	0 V
S4, S3, S0	Hi-Z	Hi-Z	PBUS
S4, S3, S0	0 V	X	0 V
S4, S3, S0	X	0 V	0 V

SYNC_MASTER=CLEAN_X305 SYNC_DATE=05/30/2014

PAGE TITLE
X249 Boost Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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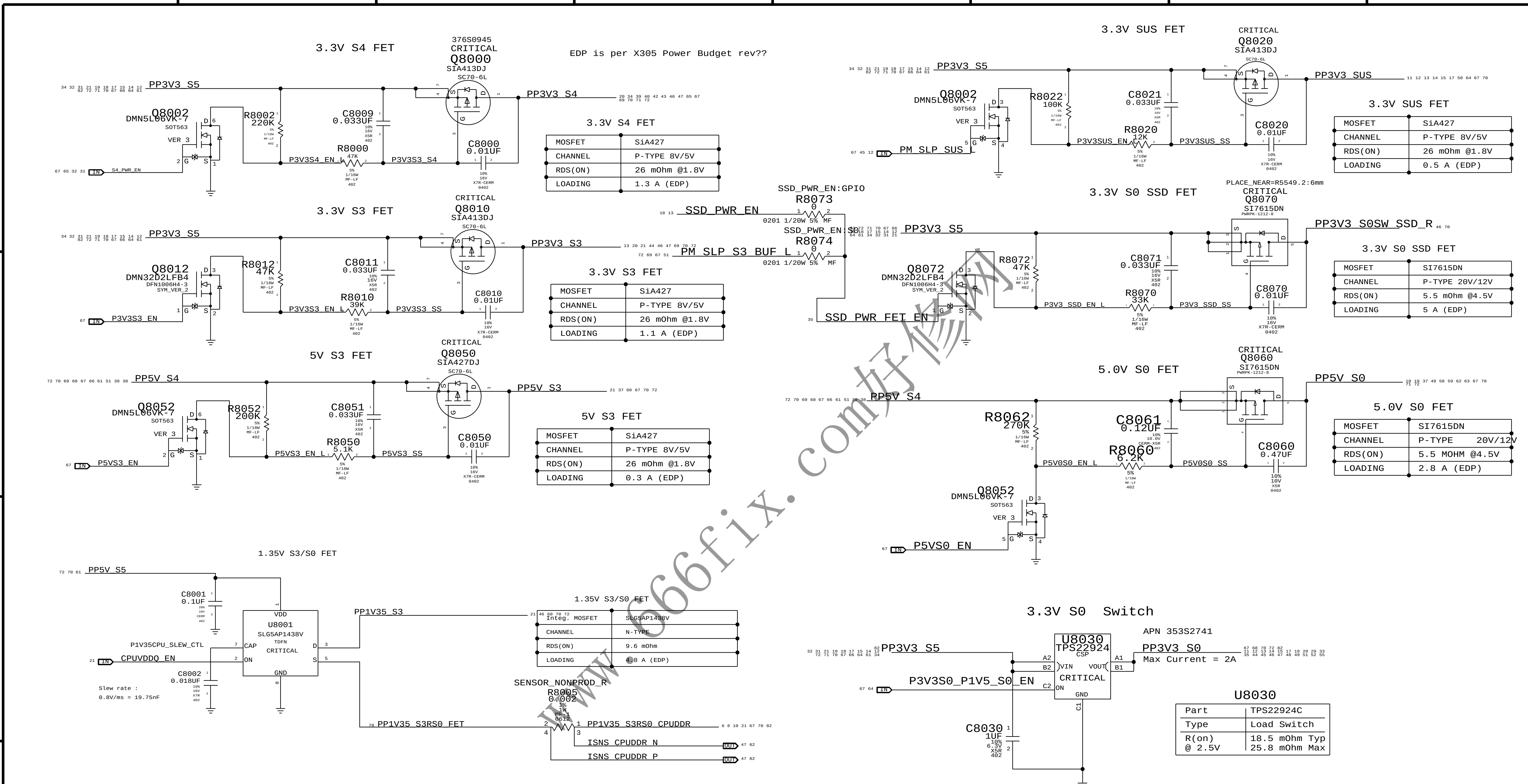


3.3V S4 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

5V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

1.35V S3/S0 FET

Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

3.3V S0 SSD FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: Power FETs

Apple Inc.

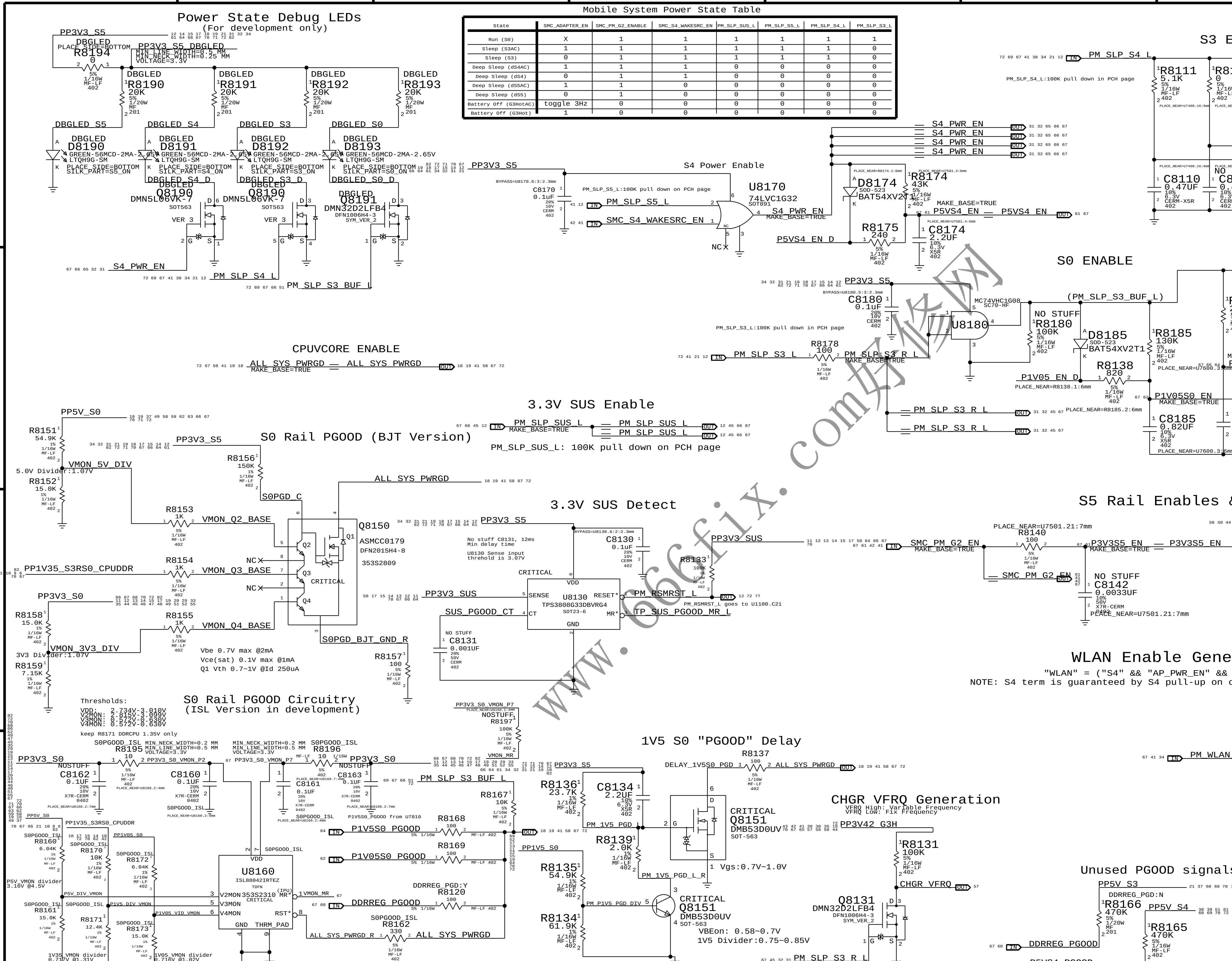
DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0



SYNC_MASTER=CLEAN_X305 SYNC_DATE=05/30/2014

PAGE TITLE: Power Control 1/ENABLE

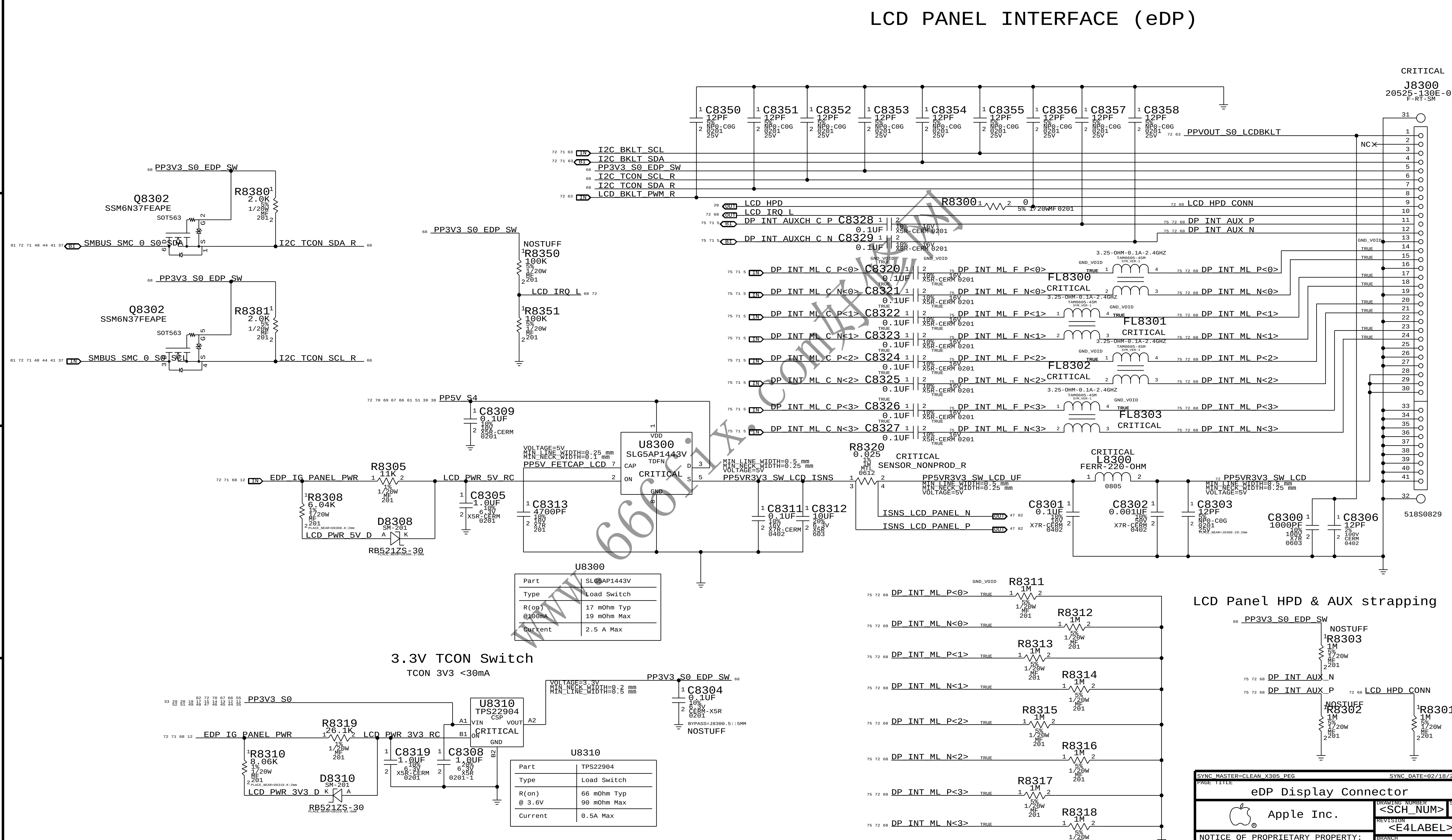
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

LCD PANEL INTERFACE (eDP)



U8300

Part	SLG5AP1443V
Type	Load Switch
R(on) @100mA	17 mOhm Typ 19 mOhm Max
Current	2.5 A Max

U8310

Part	TPS22904
Type	Load Switch
R(on) @ 3.6V	66 mOhm Typ 90 mOhm Max
Current	0.5A Max

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

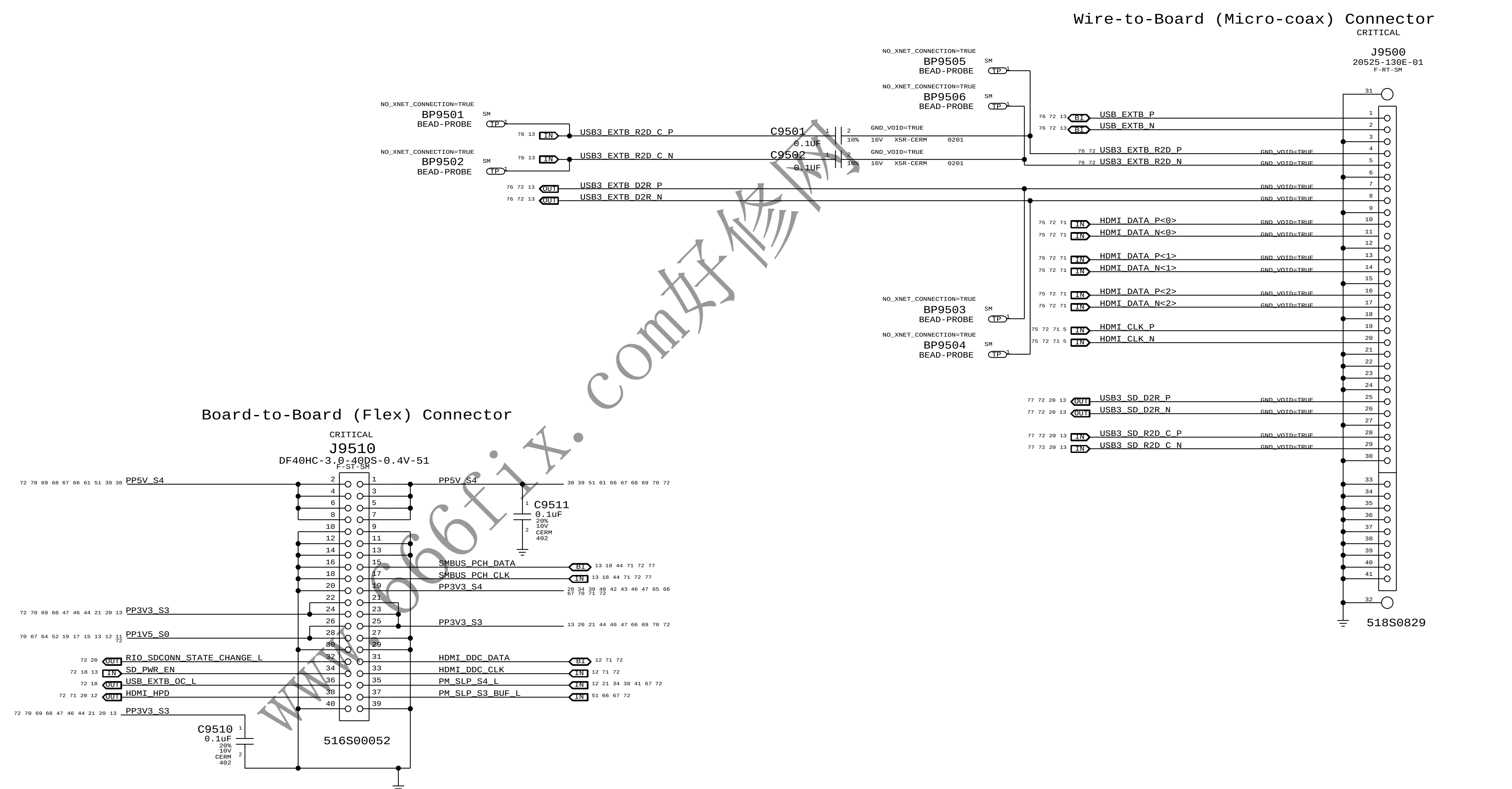
PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>



SYNC_MASTER=CLEAN_X305G SYNC_DATE=01/14/2014

PAGE TITLE

RIO Connectors

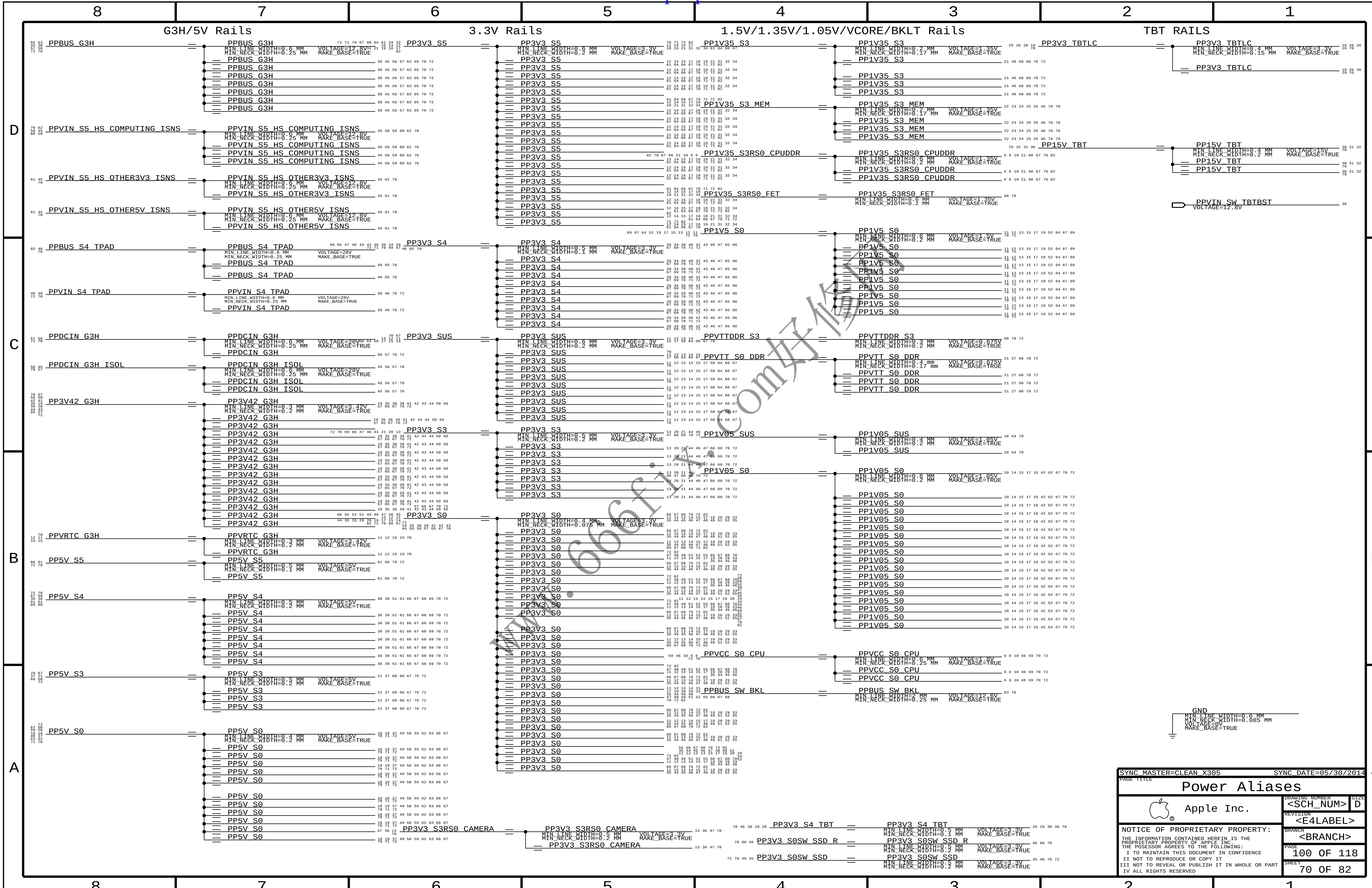
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

Laptopblue


G3H/5V Rails
3.3V Rails
1.5V/1.35V/1.05V/VCORE/BKLT Rails
TBT RAILS
PPBUS_G3H
PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_OTHER3V3_ISNS
PPVIN_S5_HS_OTHER5V_ISNS
PPBUS_S4_TPAD
PPVIN_S4_TPAD
PPDCIN_G3H
PPDCIN_G3H_ISOL
PP3V42_G3H
PPVRTC_G3H
PP5V_S5
PP5V_S4
PP5V_S3
PP5V_S0
PP3V3_S5
PP3V3_S4
PP3V3_SUS
PP3V3_S3
PP3V3_S0
PP3V3_S3RS0_CAMERA
PP1V35_S3
PP1V35_S3_MEM
PP1V35_S3RS0_CPUDDR
PP1V35_S3RS0_FET
PP1V5_S0
PPVTTDDR_S3
PPVTT_S0_DDR
PP1V05_SUS
PP1V05_S0
PPVCC_S0_CPU
PPBUS_SW_BKL
PP3V3_S4_TBT
PP3V3_S0SW_SSD_R
PP3V3_S0SW_SSD
PP3V3_TBTLC
PP15V_TBT
PPVIN_SW_TBTBST
VOLTAGE=12.8V
GND
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.085 MM
VOLTAGE=0V
MAKE_BASE=TRUE
SYNC_MASTER=CLEAN_X305
SYNC_DATE=05/30/2014
PAGE TITLE
Power Aliases
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
100 OF 118
SHEET
70 OF 82
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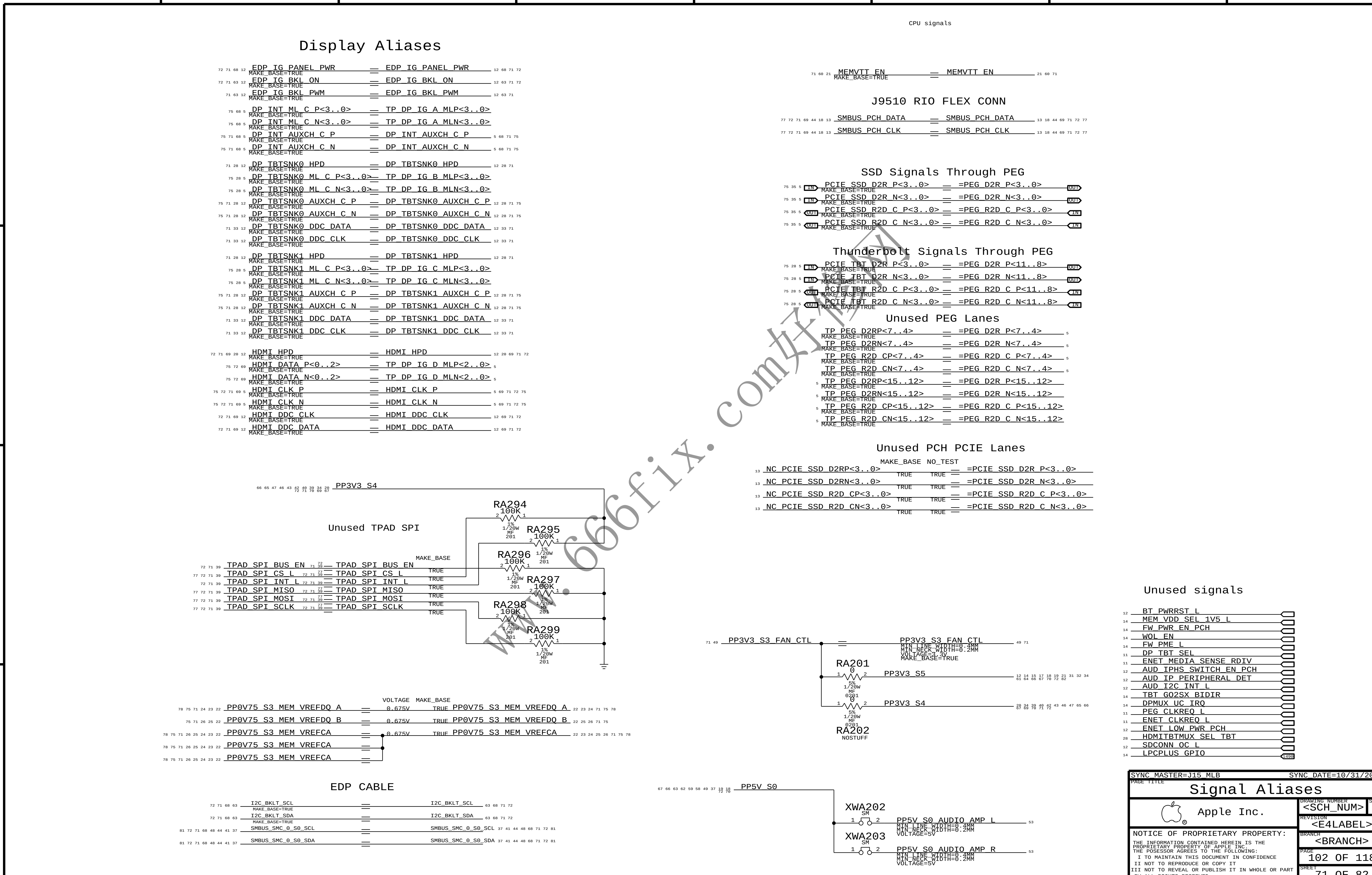
Display Aliases
EDP_IG_PANEL_PWR = EDP_IG_PANEL_PWR
EDP_IG_BKL_ON = EDP_IG_BKL_ON
EDP_IG_BKL_PWM = EDP_IG_BKL_PWM
DP_INT_ML_C_P<3..0> = TP_DP_IG_A_MLP<3..0>
DP_INT_ML_C_N<3..0> = TP_DP_IG_A_MLN<3..0>
DP_INT_AUXCH_C_P = DP_INT_AUXCH_C_P
DP_INT_AUXCH_C_N = DP_INT_AUXCH_C_N
DP_TBTSNK0_HPD = DP_TBTSNK0_HPD
DP_TBTSNK0_ML_C_P<3..0> = TP_DP_IG_B_MLP<3..0>
DP_TBTSNK0_ML_C_N<3..0> = TP_DP_IG_B_MLN<3..0>
DP_TBTSNK0_AUXCH_C_P = DP_TBTSNK0_AUXCH_C_P
DP_TBTSNK0_AUXCH_C_N = DP_TBTSNK0_AUXCH_C_N
DP_TBTSNK0_DDC_DATA = DP_TBTSNK0_DDC_DATA
DP_TBTSNK0_DDC_CLK = DP_TBTSNK0_DDC_CLK
DP_TBTSNK1_HPD = DP_TBTSNK1_HPD
DP_TBTSNK1_ML_C_P<3..0> = TP_DP_IG_C_MLP<3..0>
DP_TBTSNK1_ML_C_N<3..0> = TP_DP_IG_C_MLN<3..0>
DP_TBTSNK1_AUXCH_C_P = DP_TBTSNK1_AUXCH_C_P
DP_TBTSNK1_AUXCH_C_N = DP_TBTSNK1_AUXCH_C_N
DP_TBTSNK1_DDC_DATA = DP_TBTSNK1_DDC_DATA
DP_TBTSNK1_DDC_CLK = DP_TBTSNK1_DDC_CLK
HDMI_HPD = HDMI_HPD
HDMI_DATA_P<0..2> = TP_DP_IG_D_MLP<2..0>
HDMI_DATA_N<0..2> = TP_DP_IG_D_MLN<2..0>
HDMI_CLK_P = HDMI_CLK_P
HDMI_CLK_N = HDMI_CLK_N
HDMI_DDC_CLK = HDMI_DDC_CLK
HDMI_DDC_DATA = HDMI_DDC_DATA
MAKE_BASE=TRUE
CPU signals
MEMVTT_EN = MEMVTT_EN
J9510 RIO FLEX CONN
SMBUS_PCH_DATA = SMBUS_PCH_DATA
SMBUS_PCH_CLK = SMBUS_PCH_CLK
SSD Signals Through PEG
PCIE_SSD_D2R_P<3..0> = =PEG_D2R_P<3..0>
PCIE_SSD_D2R_N<3..0> = =PEG_D2R_N<3..0>
PCIE_SSD_R2D_C_P<3..0> = =PEG_R2D_C_P<3..0>
PCIE_SSD_R2D_C_N<3..0> = =PEG_R2D_C_N<3..0>
Thunderbolt Signals Through PEG
PCIE_TBT_D2R_P<3..0> = =PEG_D2R_P<11..8>
PCIE_TBT_D2R_N<3..0> = =PEG_D2R_N<11..8>
PCIE_TBT_R2D_C_P<3..0> = =PEG_R2D_C_P<11..8>
PCIE_TBT_R2D_C_N<3..0> = =PEG_R2D_C_N<11..8>
Unused PEG Lanes
TP_PEG_D2RP<7..4> = =PEG_D2R_P<7..4>
TP_PEG_D2RN<7..4> = =PEG_D2R_N<7..4>
TP_PEG_R2D_CP<7..4> = =PEG_R2D_C_P<7..4>
TP_PEG_R2D_CN<7..4> = =PEG_R2D_C_N<7..4>
TP_PEG_D2RP<15..12> = =PEG_D2R_P<15..12>
TP_PEG_D2RN<15..12> = =PEG_D2R_N<15..12>
TP_PEG_R2D_CP<15..12> = =PEG_R2D_C_P<15..12>
TP_PEG_R2D_CN<15..12> = =PEG_R2D_C_N<15..12>
Unused PCH PCIE Lanes
MAKE_BASE NO_TEST
NC_PCIE_SSD_D2RP<3..0> TRUE TRUE = =PCIE_SSD_D2R_P<3..0>
NC_PCIE_SSD_D2RN<3..0> TRUE TRUE = =PCIE_SSD_D2R_N<3..0>
NC_PCIE_SSD_R2D_CP<3..0> TRUE TRUE = =PCIE_SSD_R2D_C_P<3..0>
NC_PCIE_SSD_R2D_CN<3..0> TRUE TRUE = =PCIE_SSD_R2D_C_N<3..0>
PP3V3_S4
Unused TPAD SPI
MAKE_BASE
TPAD_SPI_BUS_EN = TPAD_SPI_BUS_EN TRUE
TPAD_SPI_CS_L = TPAD_SPI_CS_L TRUE
TPAD_SPI_INT_L = TPAD_SPI_INT_L TRUE
TPAD_SPI_MISO = TPAD_SPI_MISO TRUE
TPAD_SPI_MOSI = TPAD_SPI_MOSI TRUE
TPAD_SPI_SCLK = TPAD_SPI_SCLK TRUE
RA294 100K 1% 1/20W MF 201
RA295 100K 1% 1/20W MF 201
RA296 100K 1% 1/20W MF 201
RA297 100K 1% 1/20W MF 201
RA298 100K 1% 1/20W MF 201
RA299 100K 1% 1/20W MF 201
VOLTAGE MAKE_BASE
PP0V75_S3_MEM_VREFDQ_A = 0.675V TRUE PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFDQ_B = 0.675V TRUE PP0V75_S3_MEM_VREFDQ_B
PP0V75_S3_MEM_VREFCA = 0.675V TRUE PP0V75_S3_MEM_VREFCA
PP0V75_S3_MEM_VREFCA
PP0V75_S3_MEM_VREFCA
EDP CABLE
I2C_BKLT_SCL = I2C_BKLT_SCL
I2C_BKLT_SDA = I2C_BKLT_SDA
SMBUS_SMC_0_S0_SCL = SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA = SMBUS_SMC_0_S0_SDA
PP3V3_S3_FAN_CTL = PP3V3_S3_FAN_CTL
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
RA201 0 5% 1/20W MF 0201 PP3V3_S5
RA202 0 5% 1/20W MF 0201 PP3V3_S4 NOSTUFF
PP5V_S0
XWA202 SM PP5V_S0_AUDIO_AMP_L
XWA203 SM PP5V_S0_AUDIO_AMP_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
Unused signals
BT_PWRRST_L
MEM_VDD_SEL_1V5_L
FW_PWR_EN_PCH
WOL_EN
FW_PME_L
DP_TBT_SEL
ENET_MEDIA_SENSE_RDIV
AUD_IPHS_SWITCH_EN_PCH
AUD_IP_PERIPHERAL_DET
AUD_I2C_INT_L
TBT_GO2SX_BIDIR
DPMUX_UC_IRQ
PEG_CLKREQ_L
ENET_CLKREQ_L
ENET_LOW_PWR_PCH
HDMITBTMUX_SEL_TBT
SDCONN_OC_L
LPCPLUS_GPIO
SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012
PAGE TITLE
Signal Aliases
Apple Inc.
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REVISION <E4LABEL>
BRANCH <BRANCH>
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Functional Test Points

J3501 - airport

FUNC_TEST

- AP_CLKREQ_Q_L
- AP_RESET_CONN_L
- PCIE_AP_D2R_PI_N
- PCIE_AP_D2R_PI_P
- PCIE_AP_R2D_N
- PCIE_AP_R2D_P
- PCIE_CLK100M_AP_CONN_N
- PCIE_CLK100M_AP_CONN_P
- PCIE_WAKE_L
- PP3V3_S3RS4_BT_F
- PP3V3_WLAN
- USB_BT_CONN_N
- USB_BT_CONN_P
- WIFI_EVENT_L
- GND 4X

J4002 - Camera

- MIPI_CLK_CONN_N
- MIPI_CLK_CONN_P
- CAM_SENSOR_WAKE_L_CONN
- MIPI_DATA_CONN_N
- MIPI_DATA_CONN_P
- SMBUS_SMC_0_S0_SDA
- SMBUS_SMC_0_S0_SCL
- I2C_CAM_SCK
- I2C_CAM_SDA
- PP5V_S3RS0_ALSCAM_F
- GND

J9500 - rio coax

- HDMI_CLK_N
- HDMI_CLK_P
- HDMI_DATA_N<0>
- HDMI_DATA_N<1>
- HDMI_DATA_N<2>
- HDMI_DATA_P<0>
- HDMI_DATA_P<1>
- HDMI_DATA_P<2>
- USB3_SD_D2R_N
- USB3_SD_D2R_P
- USB3_SD_R2D_C_N
- USB3_SD_R2D_C_P
- USB3_EXTB_D2R_N
- USB3_EXTB_D2R_P
- USB3_EXTB_R2D_N
- USB3_EXTB_R2D_P
- USB_EXTB_N
- USB_EXTB_P
- GND 19X

J9510 - rio flex

- SD_PWR_EN
- HDMI_DDC_CLK
- HDMI_DDC_DATA
- HDMI_HPD
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA
- PM_SLP_S3_BUF_L
- PM_SLP_S4_L
- PP3V3_S3 3X
- PP3V3_S4
- PP5V_S4 5X
- RIO_SDCONN_STATE_CHANGE_L
- USB_EXTB_OC_L
- GND 10X

J5150 - hall effect

- PP3V42_G3H
- SMC_LID_R
- GND

J6050 - left fan

- FAN_LT_PWM
- FAN_LT_TACH
- PP5V_S0 3X
- GND 5X

J6060 - right fan

- FAN_RT_PWM
- FAN_RT_TACH
- PP5V_S0 3X
- GND 5X

J6100 - spi

FUNC_TEST

- PP3V42_G3H
- SMC_RESET_L
- SMC_TCK
- SMC_TMS
- SPIROM_USE_MLB
- SPI_ALT_CLK
- SPI_ALT_CS_L
- SPI_ALT_IO0_MOSI
- SPI_ALT_IO1_MISO
- SPI_ALT_IO2_WP_L
- SPI_ALT_IO1_HOLD_L
- GND 2X

J4801 - ipd flex

- TPAD_SPI_INT_L
- TPAD_SPI_CS_L
- TPAD_SPI_MOSI
- TPAD_SPI_MISO
- TPAD_SPI_SCLK
- TPAD_SPI_BUS_EN
- USB_TPAD_N
- USB_TPAD_P
- IOXP2_INT_L
- I2C_IOXP_SCL
- I2C_IOXP_SDA
- SMC_PME_S4_WAKE_L
- TPAD_ACTUATOR_THRMTRIP_L
- TPAD_VBUS_EN
- SMBUS_SMC_2_S3_SCL
- SMBUS_SMC_2_S3_SDA
- SMC_LID
- SMC_ACTUATOR_EN_L
- PPVIN_S4_TPAD 4X
- GND_ACTUATOR 4X
- PP3V3_S4
- PP5V_S4
- GND 2X

J4813 - keyboard

- PP3V3_S4
- PP3V42_G3H
- WS_CONTROL_KBD
- WS_KBD1
- WS_KBD10
- WS_KBD11
- WS_KBD12
- WS_KBD13
- WS_KBD14
- WS_KBD15_CAP
- WS_KBD16_NUM
- WS_KBD17
- WS_KBD18
- WS_KBD19
- WS_KBD2
- WS_KBD20
- WS_KBD21
- WS_KBD22
- WS_KBD23
- WS_KBD3
- WS_KBD4
- WS_KBD5
- WS_KBD6
- WS_KBD7
- WS_KBD8
- WS_KBD9
- WS_KBD_ONOFF_L
- WS_LEFT_OPTION_KBD
- WS_LEFT_SHIFT_KBD
- GND 2X

J4915 - kbd bklt

- KBDBKLT_RETURN1 2X
- KBDBKLT_RETURN2 2X
- PPVOUT_S0_KBDBKLT
- GND 4X

J6601 - mic

- DMIC_CLK3
- PP3V3_S0
- DMIC_SDA2
- DMIC_SDA3
- GND

J6602 - L speaker

- SPKRCONN_L_ID
- SPKRCONN_L_OUT_N
- SPKRCONN_L_OUT_P
- SPKRCONN_SL_OUT_N
- SPKRCONN_SL_OUT_P
- GND

J6603 - R speaker

- SPKRCONN_R_ID
- SPKRCONN_R_OUT_N
- SPKRCONN_R_OUT_P
- SPKRCONN_SR_OUT_N
- SPKRCONN_SR_OUT_P
- GND

J7000 - DC PWR

- ADAPTER_SENSE
- PP20V_DCIN_FUSE 2X
- GND 2X

J7050 - battery

- PPVBAT_G3H_CONN 8X
- SMBUS_SMC_5_G3_SCL
- SMBUS_SMC_5_G3_SDA
- SYS_DETECT_L
- GND 8X

J8300 - eDP

- DP_INT_AUX_N
- DP_INT_AUX_P
- DP_INT_ML_N<0>
- DP_INT_ML_N<1>
- DP_INT_ML_N<2>
- DP_INT_ML_N<3>
- DP_INT_ML_P<0>
- DP_INT_ML_P<1>
- DP_INT_ML_P<2>
- DP_INT_ML_P<3>
- LCD_IRQ_L
- LCD_HPD_CONN
- LCD_BKLT_PWM_R
- SMBUS_SMC_0_S0_SDA
- SMBUS_SMC_0_S0_SCL
- I2C_BKLT_SDA
- I2C_BKLT_SCL
- PP5VR3V3_SW_LCD 3X
- PPVOUT_S0_LCDBKLT
- GND 16X

Power Rails

- PM_SLP_S3_L
- PPVTT_S0_DDR
- PP3V3_S0
- PP3V3_S3
- PP3V3_S5
- PP3V3_S5_AVREF_SMC
- PP3V42_G3H
- PP5V_S0
- PP5V_S3
- PP5V_S5
- PPBUS_G3H
- PPDCIN_G3H
- PPVCC_S0_CPU
- PPVTTDDR_S3
- PP3V3_S0SW_SSD
- PP1V5_S0
- PP1V35_S3

XDP

FUNC_TEST

- XDP_CPU_TCK
- XDP_PCH_TCK
- XDP_CPU_TDI
- XDP_CPU_TDO
- XDP_CPUPCH_TRST_L
- XDP_CPU_TMS
- XDP_PCH_TMS
- XDP_PCH_TDI
- XDP_PCH_TDO
- XDP_CPU_PREQ_L
- XDP_CPU_PRDY_L
- PM_RSMRST_L
- PM_PCH_PWROK
- PM_SYSRST_L
- CPU_CFG<3>
- PP1V05_S0
- GND 2X GND

Power Sequence

FUNC_TEST

- SMC_ONOFF_L
- PM_DSW_PWRGD
- ALL_SYS_PWRGD
- PM_PCH_SYS_PWROK
- PLT_RESET_L
- EDP_IG_PANEL_PWR
- EDP_IG_BKL_ON

SYNC_MASTER=J15_MLB	SYNC_DATE=10/31/2012
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NC NO_TESTs

PCH

Net	NO_TEST	MAKE_BASE	Net
NC_USB3_SPARE_D2RN	TRUE	TRUE	NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP	TRUE	TRUE	NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
NC_USB3_EXTC_D2RN	TRUE	TRUE	NC_USB3_EXTC_D2RN
NC_USB3_EXTC_D2RP	TRUE	TRUE	NC_USB3_EXTC_D2RP
NC_USB3_EXTC_R2D_CN	TRUE	TRUE	NC_USB3_EXTC_R2D_CN
NC_USB3_EXTC_R2D_CP	TRUE	TRUE	NC_USB3_EXTC_R2D_CP
NC_USB3_EXTD_D2RN	TRUE	TRUE	NC_USB3_EXTD_D2RN
NC_USB3_EXTD_D2RP	TRUE	TRUE	NC_USB3_EXTD_D2RP
NC_USB3_EXTD_R2D_CN	TRUE	TRUE	NC_USB3_EXTD_R2D_CN
NC_USB3_EXTD_R2D_CP	TRUE	TRUE	NC_USB3_EXTD_R2D_CP
NC_PCIE_ENET_D2RN	TRUE	TRUE	NC_PCIE_ENET_D2RN
NC_PCIE_ENET_D2RP	TRUE	TRUE	NC_PCIE_ENET_D2RP
NC_PCIE_ENET_R2D_CN	TRUE	TRUE	NC_PCIE_ENET_R2D_CN
NC_PCIE_ENET_R2D_CP	TRUE	TRUE	NC_PCIE_ENET_R2D_CP
NC_SATA_A_D2RN	TRUE	TRUE	NC_SATA_A_D2RN
NC_SATA_A_D2RP	TRUE	TRUE	NC_SATA_A_D2RP
NC_SATA_A_R2D_CN	TRUE	TRUE	NC_SATA_A_R2D_CN
NC_SATA_A_R2D_CP	TRUE	TRUE	NC_SATA_A_R2D_CP
NC_SATA_B_D2RN	TRUE	TRUE	NC_SATA_B_D2RN
NC_SATA_B_D2RP	TRUE	TRUE	NC_SATA_B_D2RP
NC_SATA_B_R2D_CN	TRUE	TRUE	NC_SATA_B_R2D_CN
NC_SATA_B_R2D_CP	TRUE	TRUE	NC_SATA_B_R2D_CP
NC_SATA_ODD_D2RN	TRUE	TRUE	NC_SATA_ODD_D2RN
NC_SATA_ODD_D2RP	TRUE	TRUE	NC_SATA_ODD_D2RP
NC_SATA_ODD_R2D_CN	TRUE	TRUE	NC_SATA_ODD_R2D_CN
NC_SATA_ODD_R2D_CP	TRUE	TRUE	NC_SATA_ODD_R2D_CP
NC_SATA_D_D2RN	TRUE	TRUE	NC_SATA_D_D2RN
NC_SATA_D_D2RP	TRUE	TRUE	NC_SATA_D_D2RP
NC_SATA_D_R2D_CN	TRUE	TRUE	NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP	TRUE	TRUE	NC_SATA_D_R2D_CP
NC_SATA_F_D2RN	TRUE	TRUE	NC_SATA_F_D2RN
NC_SATA_F_D2RP	TRUE	TRUE	NC_SATA_F_D2RP
NC_SATA_F_R2D_CN	TRUE	TRUE	NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP	TRUE	TRUE	NC_SATA_F_R2D_CP
NC_USB_EXTCN	TRUE	TRUE	NC_USB_EXTCN
NC_USB_EXTCP	TRUE	TRUE	NC_USB_EXTCP
NC_USB_SDN	TRUE	TRUE	NC_USB_SDN
NC_USB_SDP	TRUE	TRUE	NC_USB_SDP
NC_USB_WLANN	TRUE	TRUE	NC_USB_WLANN
NC_USB_WLANP	TRUE	TRUE	NC_USB_WLANP
NC_USB_6N	TRUE	TRUE	NC_USB_6N
NC_USB_6P	TRUE	TRUE	NC_USB_6P
NC_USB_7N	TRUE	TRUE	NC_USB_7N
NC_USB_7P	TRUE	TRUE	NC_USB_7P
NC_USB_EXTDN	TRUE	TRUE	NC_USB_EXTDN
NC_USB_EXTDP	TRUE	TRUE	NC_USB_EXTDP
NC_USB_PSOCN	TRUE	TRUE	NC_USB_PSOCN
NC_USB_PSOCP	TRUE	TRUE	NC_USB_PSOCP
NC_USB_IRN	TRUE	TRUE	NC_USB_IRN
NC_USB_IRP	TRUE	TRUE	NC_USB_IRP
NC_ITPXDP_CLK100MN	TRUE	TRUE	NC_ITPXDP_CLK100MN
NC_ITPXDP_CLK100MP	TRUE	TRUE	NC_ITPXDP_CLK100MP
NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L
NC_PCI_CLK33M_OUT2	TRUE	TRUE	NC_PCI_CLK33M_OUT2
NC_PCI_CLK33M_OUT3	TRUE	TRUE	NC_PCI_CLK33M_OUT3
NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1
NC_HDA_SDIN2	TRUE	TRUE	NC_HDA_SDIN2
NC_HDA_SDIN3	TRUE	TRUE	NC_HDA_SDIN3
NC_LPC_DREQ0_L	TRUE	TRUE	NC_LPC_DREQ0_L
NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK
NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA
NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L
NC_LPC_CLK33M_LPCPLUS_R	TRUE	TRUE	NC_LPC_CLK33M_LPCPLUS_R
NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP
NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN
NC_SMC_INTERFACE_2	TRUE	TRUE	NC_SMC_INTERFACE_2

Thunderbolt

Net	NO_TEST	MAKE_BASE	Net
NC_TBT_XTAL25OUT	TRUE	TRUE	NC_TBT_XTAL25OUT
TP_DP_TBTSRC_ML_CP<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
TP_DP_TBTSRC_ML_CN<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN
NC_DP_IG_D_AUXCHN	TRUE	TRUE	NC_DP_IG_D_AUXCHN
NC_DP_IG_D_AUXCHP	TRUE	TRUE	NC_DP_IG_D_AUXCHP
NC_PCIE_CLK100M_GPUN	TRUE	TRUE	NC_PCIE_CLK100M_GPUN
NC_PCIE_CLK100M_GPUP	TRUE	TRUE	NC_PCIE_CLK100M_GPUP
NC_PCIE_CLK100M_PE5N	TRUE	TRUE	NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P	TRUE	TRUE	NC_PCIE_CLK100M_PE5P
NC_PCIE_CLK100M_ENETSDN	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
NC_PCIE_CLK100M_ENETSDP	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
NC_PCIE_CLK100M_ENETN	TRUE	TRUE	NC_PCIE_CLK100M_ENETN
NC_PCIE_CLK100M_ENETP	TRUE	TRUE	NC_PCIE_CLK100M_ENETP
NC_PCIE_CLK100M_PEGBN	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
NC_PCIE_CLK100M_PEGBP	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
NC_PCIE_CLK100M_SWN	TRUE	TRUE	NC_PCIE_CLK100M_SWN
NC_PCIE_CLK100M_SWP	TRUE	TRUE	NC_PCIE_CLK100M_SWP
NC_PCH_GPIO64_CLKOUTFLEX0	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3
NC_USB_4N	TRUE	TRUE	NC_USB_4N
NC_USB_4P	TRUE	TRUE	NC_USB_4P

NO_TEST	Net
TRUE	PCIE_TBT_R2D_P<3..0>
TRUE	PCIE_TBT_R2D_N<3..0>
TRUE	PCIE_TBT_D2R_C_P<3..0>
TRUE	PCIE_TBT_D2R_C_N<3..0>
TRUE	DMI_S2N_P<3..1>
TRUE	DMI_S2N_N<3..1>
TRUE	DMI_N2S_P<3..1>
TRUE	DMI_N2S_N<3..1>

PLACEABLE BEAD-PROBES FOR TBT

Net	Part	Ref	Property
TBT_A_D2R_P<1>	TP SM BEAD-PROBE	BPA531	NO_XNET_CONNECTION=TRUE
TBT_A_D2R_N<1>	TP SM BEAD-PROBE	BPA532	NO_XNET_CONNECTION=TRUE

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: NC & No Test

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

8 7 6 5 4 3 2 1

X425 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

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PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG3_2SAME	*	=4X_DIELECTRIC	?
PEG3_TXRX	*	=8X_DIELECTRIC	?
PEG3_2OTHER	*	=5X_DIELECTRIC	?
PEG3_2CLK	*	=8X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG3_2SAME	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG3_TXRX	TOP,BOTTOM	=12X_DIELECTRIC	?
PEG3_2OTHER	TOP,BOTTOM	=8X_DIELECTRIC	?
PEG3_2CLK	TOP,BOTTOM	=12X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG3_*	=SAME	*	PEG3_2SAME
PEG3_R2D	PEG3_D2R	*	PEG3_TXRX
PEG3_*	*	*	PEG3_2OTHER
PEG3_*	CLK_*	*	PEG3_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_P<3:0>	5 12 73
	DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_N<3:0>	5 12 73
	DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_P<3:0>	5 12 73
	DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_N<3:0>	5 12 73
	FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
	FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC	5 12
I125	DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P	6 11
I126	DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N	6 11
	CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
	CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
I151	CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
	CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11
I132	CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
I130	CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
I133	CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 72
	XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MP	11 73
	XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MN	11 73
	XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 72
	XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 72
	XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 72
	XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 72
	XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 18 72
	XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	6 18
	XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	6 18
I134	XDP_BDRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
I135	XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 72
I136	XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 72
	CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 41
	CPU_PECI	CPU_45S	CPU_VID	CPU_PECI	6 14 42
	CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 41 42 58
I150	CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 14 18
	PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	6 14 42
	PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	6 12 21
	PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	6 12
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
	CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT	8 58
	CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK	8 58
	CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L	8 58
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 58
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 58
I140	CPU_MEM_VREF		MEM_12MIL	CPU_DIMMA_VREFDQ	7 22
I141	CPU_MEM_VREF		MEM_12MIL	CPU_DIMMB_VREFDQ	7 22
I255	CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 71 78
I256	CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	22 25 26 71
I254	CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 71 75 78
I253	CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 71 75 78
I252	PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE_SSD_D2R_P<3..0>	5 35 71
I251	PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE_SSD_D2R_N<3..0>	5 35 71
I250	PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_C_P<3..0>	5 35 71
I249	PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_C_N<3..0>	5 35 71
I248		CPU_85D	PEG3_R2D	PCIE_SSD_R2D_P<3..0>	35
I247		CPU_85D	PEG3_R2D	PCIE_SSD_R2D_N<3..0>	35
I153	PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0>	5 28 71
I152	PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0>	5 28 71
I154		CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>	28 73
I155		CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>	28 73
I156	PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0>	28 73
I158	PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0>	28 73
I157		CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>	5 28 71
I159		CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>	5 28 71

DP AUX NET PROPERTIES

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I243	DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	5 68 71
I244	DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	5 68 71
I166		DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	68 72 75
I167		DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	68 72 75
I231		DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	68
I232		DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	68
I234		DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	68 72 75
I233		DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	68 72 75
I246	DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	5 68 71
I245	DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	5 68 71
I171	DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	68 72
I170	DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	68 72

DP / HDMI NET PROPERTIES

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I211	HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_P<2..0>	69 71 72
I210	HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_N<2..0>	69 71 72
I213	HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_P	5 69 71 72
I212	HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_N	5 69 71 72
I235	DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	5 28 71
I236	DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	5 28 71
I237		DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28
I238		DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28
I239	DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	5 28 71
I240	DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	5 28 71
I241		DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28
I242		DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28
I223	TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28
I224	TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28
I228		DP_85D		DP_TBTSNK0_AUXCH_C_P	12 28 71
I229		DP_85D		DP_TBTSNK0_AUXCH_C_N	12 28 71
I227	TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	28
I226	TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	28
I225		DP_85D		DP_TBTSNK1_AUXCH_C_P	12 28 71
I230		DP_85D		DP_TBTSNK1_AUXCH_C_N	12 28 71

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

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CPU Constraints

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	11 73
		SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	11 73
I272		SATA_85D	SATA_D2R	NC_SATA_A_D2RP	11 73
I271		SATA_85D	SATA_D2R	NC_SATA_A_D2RN	11 73
I299		SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	11 73
I298		SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	11 73
I300		SATA_85D	SATA_D2R	NC_SATA_B_D2RP	11 73
I301		SATA_85D	SATA_D2R	NC_SATA_B_D2RN	11 73
I213	PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
	USB_EXTA	USB_85D	USB	USB_EXTA_P	13 38
	USB_EXTA	USB_85D	USB	USB_EXTA_N	13 38
I245	USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	38
I244	USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_N	38
I248	USB_EXTA	USB_85D	USB	USB_LT1_P	38
I249	USB_EXTA	USB_85D	USB	USB_LT1_N	38
	USB_NC	USB_85D	USB	NC_USB_EXTCP	13 73
	USB_NC	USB_85D	USB	NC_USB_EXTCN	13 73
I238	USB_NC	USB_85D	USB	NC_USB_SDP	13 73
I239	USB_NC	USB_85D	USB	NC_USB_SDN	13 73
I273		CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	38 41 42
I274		CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	38 41 42
	USB_SMC	USB_85D	USB	NC_USB_SMCP	73
	USB_SMC	USB_85D	USB	NC_USB_SMCN	73
I281	USB_NC	USB_85D	USB	NC_USB_6P	13 73
I282	USB_NC	USB_85D	USB	NC_USB_6N	13 73
I283	USB_NC	USB_85D	USB	NC_USB_7P	13 73
I284	USB_NC	USB_85D	USB	NC_USB_7N	13 73
	USB_EXTB	USB_85D	USB	USB_EXTB_P	13 69 72
	USB_EXTB	USB_85D	USB	USB_EXTB_N	13 69 72
I260	USB_NC	USB_85D	USB	NC_USB_EXTDP	13 73
I259	USB_NC	USB_85D	USB	NC_USB_EXTDN	13 73
	USB_BT	USB_85D	USB	USB_BT_P	13 34
	USB_BT	USB_85D	USB	USB_BT_N	13 34
		USB_85D	USB	USB_BT_CONN_P	34 72
		USB_85D	USB	USB_BT_CONN_N	34 72
I285	USB_NC	USB_85D	USB	NC_USB_IRP	13 73
I286	USB_NC	USB_85D	USB	NC_USB_IRN	13 73
I288	USB_TPAD	USB_85D	USB	USB_TPAD_P	13 39 72
I287	USB_TPAD	USB_85D	USB	USB_TPAD_N	13 39 72
I302		USB_85D	USB	USB_TPAD_R_P	
I303		USB_85D	USB	USB_TPAD_R_N	
	PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
I228	USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 38
I231	USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 38
I267		USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
I265		USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
I230	USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	38
I229	USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	38
I268		USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 38
I266		USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 38
I222	USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 69 72
I223	USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 69 72
I264		USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
I262		USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
I220	USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	69 72
I221	USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	69 72
I261		USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 69
I263		USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 69
I290	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	13 73
I291	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	13 73
I293		USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	13 73
I292		USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	13 73
I295	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	13 73
I294	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	13 73
I296		USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	13 73
I297		USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	13 73

Clock Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I256	SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
I255	SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
I254		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
I253	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 37
I251	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
I250		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

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REVISION: <E4LABEL>

BRANCH: <BRANCH>

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?
SPI3X	*	=3x_DIELECTRIC	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	13 41
	LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	13 41
	SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	13 18 44 69 71 72
	SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	13 18 44 69 71 72
	SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	13 44
	SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	13 44
	SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK	13 44
	SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA	13 44
	HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	11 52
		HDA_45S	HDA	HDA_BIT_CLK_R	11
	HDA_SYNC	HDA_45S	HDA	HDA_SYNC	11 52
		HDA_45S	HDA	HDA_SYNC_R	11
		HDA_45S	HDA	HDA_RST_R_L	11
	HDA_RST_L	HDA_45S	HDA	HDA_RST_L	11 52
	HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	11 52
	HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	52
	HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	11 52
		HDA_45S	HDA	HDA_SDOUT_R	11 19
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	13 20 69 72
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	13 20 69 72
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P	13 20 69 72
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N	13 20 69 72
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	34 72
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	34 72
		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 34
I304		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 34
		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	34
I303		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	34
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 34
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 34
I275		PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	34 72
I276		PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	34 72
I325	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	36 37
I326	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	36 37
I327		PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 37
I328		PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 37
I329	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 37
I330	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 37
I331		PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	36 37
I332		PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	36 37
		CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	11 19
	PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	19 41
I293		CLK_LPC_45S	CLK_LPC	NC_LPC_CLK33M_LPCPLUS_R	11 73
I298	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN	11 19
I258	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
I260	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT	11 19
I253	PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
I254	PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
I262	PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
I261	PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
I255	PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
I257	PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
I256	PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
I259	PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
	PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_P	
	PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_N	
	PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 34
	PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 34
I300		PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	34 72
I299		PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	34 72
	PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 37
	PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 37
I333		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	36 37
I334		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	36 37
I281	PCIE_CLK100M_FW	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 35
I282		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 35

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I313	PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L	11
I314	PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L	11
I315	PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN	12
I316	PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L	11
I308	PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L	12 67 72
I307	PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L	12 19 41 72
I318	PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 72 77
I317	PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 72 77
I320	PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD	12 41 72
I319	PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK	12 18 19 41 72
I321	PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L	12 18 41
I322	PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R	14 42
I323	PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L	12 34 36 72
I324	PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L	14
I386	SPI_MLB	SPI_45S	SPI3X	SPI_ALT_CLK	50 72
I369	SPI_MLB	SPI_45S	SPI	SPI_CLK	50
I368	SPI_MLB	SPI_45S	SPI	SPI_CLK_R	13 50
I383	SPI_MLB	SPI_45S	SPI3X	SPI_MLB_CLK	50
I382	SPI_MLB	SPI_45S	SPI3X	SPI_SMC_CLK	41 50
I395	SPI_MLB	SPI_45S	SPI3X	SPI_ALT_CS_L	50 72
I364	SPI_MLB	SPI_45S	SPI	SPI_CS0_L	50
I363	SPI_MLB	SPI_45S	SPI	SPI_CS0_R_L	13 50
I392	SPI_MLB	SPI_45S	SPI3X	SPI_MLB_CS_L	50
I391	SPI_MLB	SPI_45S	SPI3X	SPI_SMC_CS_L	41 50
I390	SPI_MLB	SPI_45S	SPI3X	SPI_ALT_IO1_MISO	50 72
I359	SPI_MLB	SPI_45S	SPI	SPI_MISO	13 50
I358	SPI_MLB	SPI_45S	SPI	SPI_MISO_R	50
I387	SPI_MLB	SPI_45S	SPI3X	SPI_MLB_IO1_MISO	50
I381	SPI_MLB	SPI_45S	SPI3X	SPI_SMC_MISO	41 50
I380	SPI_MLB	SPI_45S	SPI3X	SPI_ALT_IO0_MOSI	50 72
I354	SPI_MLB	SPI_45S	SPI	SPI_MOSI	50
I353	SPI_MLB	SPI_45S	SPI	SPI_MOSI_R	13 50
I377	SPI_MLB	SPI_45S	SPI3X	SPI_MLB_IO0_MOSI	50
I376	SPI_MLB	SPI_45S	SPI3X	SPI_SMC_MOSI	41 50
I375	SPI_MLB_IO2	SPI_45S	SPI3X	SPI_IO<2>	13 50
I374	SPI_MLB_IO2	SPI_45S	SPI3X	SPI_MLB_IO2_WP_L	50
I371	SPI_MLB_IO2	SPI_45S	SPI3X	SPI_ALT_IO2_WP_L	50 72
I373	SPI_MLB_IO3	SPI_45S	SPI3X	SPI_IO<3>	13 50
I372	SPI_MLB_IO3	SPI_45S	SPI3X	SPI_MLB_IO3_HOLD_L	50
I370	SPI_MLB_IO3	SPI_45S	SPI3X	SPI_ALT_IO3_HOLD_L	50
I344	SPI_TPAD	SPI_45S	SPI	TPAD_SPI_SCLK	39 71 72
I343	SPI_TPAD_CS	SPI_45S	SPI	TPAD_SPI_CS_L	39 71 72
I342	SPI_TPAD	SPI_45S	SPI	TPAD_SPI_MISO	39 71 72
I341	SPI_TPAD	SPI_45S	SPI	TPAD_SPI_MOSI	39 71 72

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PAGE TITLE
PCH Constraints 2

Apple Inc.

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BRANCH <BRANCH>

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0>	7 23 27
	MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0>	7 23 27
I130	MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1>	7 24 27
I129	MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1>	7 24 27
	MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0>	7 23 27
I124	MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1>	7 24 27
I125	MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0>	7 23 27
I101	MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1>	7 24 27
I126	MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0>	7 23 27
I103	MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1>	7 24 27
	MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	7 23 24 27
	MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	7 23 24 27
	MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	7 23 24 27
	MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	7 23 24 27
	MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	7 23 24 27
	MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0>	7 23 24
	MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8>	7 23 24
	MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16>	7 23 24
	MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24>	7 23 24
	MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32>	7 23 24
	MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40>	7 23 24
	MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48>	7 23 24
I105	MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56>	7 23 24
I106	MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 23 24
	MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 23 24
	MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 23 24
	MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 23 24
	MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 23 24
	MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 23 24
	MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 23 24
	MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 23 24
	MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 23 24
	MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 23 24
	MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 23 24
	MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 23 24
I117	MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 23 24
I118	MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 23 24
I116	MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 23 24
I119	MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 23 24
	MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0>	7 25 27
	MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0>	7 25 27
I127	MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1>	7 26 27
I128	MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1>	7 26 27
	MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0>	7 25 27
I120	MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1>	7 26 27
I121	MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0>	7 25 27
I122	MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1>	7 26 27
I123	MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0>	7 25 27
	MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1>	7 26 27
I108	MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	7 25 26 27
	MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	7 25 26 27
	MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	7 25 26 27
	MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	7 25 26 27
	MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	7 25 26 27
	MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0>	7 25 26
	MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8>	7 25 26
	MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16>	7 25 26
	MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24>	7 25 26
	MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32>	7 25 26
	MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40>	7 25 26
	MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48>	7 25 26
	MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56>	7 25 26
	MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 25 26
	MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 25 26
	MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 25 26
	MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 25 26
	MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 25 26
	MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 25 26
	MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 25 26
	MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 25 26
	MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 25 26
	MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 25 26
	MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 25 26
	MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 25 26
I113	MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 25 26
I112	MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 25 26
I115	MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 25 26
I114	MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 25 26
I110			MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 71 75
I109			MEM_PWR	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 71 75
I111			MEM_PWR	PP1V35_S3_MEM	22 23 24 25 26 46 70

SYNC_MASTER=SIDLE_J45	SYNC_DATE=12/10/2012
PAGE TITLE	Memory Constraints
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	Net	Pages
	TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0>	28 31
	TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0>	28 31
	TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0>	31
	TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0>	31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	28 31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	28 31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	31
I308	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	28 31
I310	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	28 31
I311	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	31
I309	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	31
	TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0>	31
	TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0>	31
	TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0>	28 31
	TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0>	28 31
I312	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1>	31
I313	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1>	31
I314	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1>	28 31 73
I315	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1>	28 31 73
	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P	31
	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N	31
	TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P	28 31
	TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N	28 31
	TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P	31
	TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N	31
I316	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0>	28 32
I317	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0>	28 32
I318	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0>	32
I319	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0>	32
I321	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	28 32
I322	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	28 32
I320	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	32
I324	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	32
I325	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	32
I323	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	32
I327	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	28 32
I326	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	28 32
I328	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	32
I329	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	32
I331	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0>	32
I332	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0>	32
I330	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0>	28 32
I334	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0>	28 32
I333	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1>	32
I336	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1>	32
I337	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1>	28 32
I335	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1>	28 32
I339	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P	32
I338	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N	32
I341	TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P	28 32
I340	TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N	28 32
I342	TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P	32
I343	TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N	32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	Net	Pages
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	28

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Thunderbolt Constraints

Apple Inc.

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BRANCH: <BRANCH>

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	36 37
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	36 37
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	36 37
I101	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	36 37
I102		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	37
I103	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	36 37
I104	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	36 37
I106	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	36 37
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	36 37
I108	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	36 37
I107	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	36 37
I109	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	36 37
I110	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	36 37
I147	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	36 37
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	36 37
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	36 37
I127	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	36 37
I128	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	36 37
I129		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	37 72
I130		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	37 72
I134	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	36 37
I133	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	36 37
I132		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	37 72
I131		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	37 72
I145			S2_MEM_PWR	PP1V35_CAM	36 37
I146			S2_MEM_PWR	PP0V675_CAM_VREF	36 37
I148			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	37
I149			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	37

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	Net	Pages
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	39 41 44 72
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	39 41 44 72
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	41 44 48
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	41 44 48
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	37 41 44 48 68 71 72
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	37 41 44 48 68 71 72
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_g3_SCL	41 44 56 57 72
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	41 44 56 57 72
SMBUS_SMC_3_SCL	SMB_45S	SMB	NC_SMBUS_SMC_3_SCL	41 43
SMBUS_SMC_3_SDA	SMB_45S	SMB	NC_SMBUS_SMC_3_SDA	41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	Net	Pages
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
	1TO1_DIFFPAIR		CHGR_CSO_N	57

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SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE

SMC Constraints

Apple Inc.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

X425 Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I426	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P	47 66
I425	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N	47 66
I421		THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P	47
I423		THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N	47
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P	48
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N	48
I422	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_P	47 68 82
I424	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_N	47 68 82
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P	48
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N	48
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_P	48
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_N	48
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P	46
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N	46
I419		SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P	46
I420		SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N	46
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	
		SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P	47
		SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N	47
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	47 63
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	47 63
I533	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_N	47 68 82
I532	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_P	47 68 82
I524	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PCH_P	
I525	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PCH_N	
I523		SENSE_1TO1_45S	SENSE	ISNS_PCH_R_P	46
I521		SENSE_1TO1_45S	SENSE	ISNS_PCH_R_N	46
I522	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_TPAD_P	46
I520	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_TPAD_N	46
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P	45
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N	45
I514	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P	45
I515	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N	45
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	45
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	45
		SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P	46
		SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N	46
I510	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	
I511	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	

DIFFERENTIAL_PAIR

I530	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1	CPUVR_ISNS1_P	46 59
I531	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1	CPUVR_ISNS1_N	46 59
I528	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2	CPUVR_ISNS2_P	46 59
I529	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2	CPUVR_ISNS2_N	46 59
I527	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3	CPUVR_ISNS3_P	46 59
I526	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3	CPUVR_ISNS3_N	46 59

I432	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P	46
I436	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N	46
I498	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	82
I499	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	82
I502	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	82
I503	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	82
I405	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	46
I406	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P	46
I407		AUDIODIFF	AUDIO	ISNS_TBT_R_N	46
I408		AUDIODIFF	AUDIO	ISNS_TBT_R_P	46
I446	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P	46
I445		THERM_1TO1_45S	THERM	ISNS_SSD_N	46
I447	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P	46
I448		THERM_1TO1_45S	THERM	ISNS_SSD_R_N	46
I449	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P	46 62
I450		THERM_1TO1_45S	THERM	P1V05S0_CS_N	46 62

DIFFERENTIAL_PAIR

I451	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE P1V05S0_SENSE_P	62
I452		THERM_1TO1_45S	THERM	P1V05S0_SENSE P1V05S0_SENSE_N	62
I453	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMDP	28 48
I454		THERM_1TO1_45S	THERM	TBT_THERMDN	48
I455	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P	57
I456		AUDIODIFF	AUDIO	CHGR_CSI_R_N	57
I457	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P	57
I458		AUDIODIFF	AUDIO	CHGR_CSO_R_N	57
I517	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_P	
I516	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_N	
I519	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_P	47
I518	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_N	47

X425 Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I361		AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
I362		AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
		AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
		AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
I459		AUDIODIFF	AUDIO	RSUBIN_P	53
I440		AUDIODIFF	AUDIO	RSUBIN_N	53
I441		AUDIODIFF	AUDIO	LSUBIN_P	53
I442		AUDIODIFF	AUDIO	LSUBIN_N	53
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
		AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
		AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
		AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
		AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
I461		AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
I462		AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
I460		AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
I463		AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
I358	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	53 55 72
I357	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	53 55 72
I360	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	53 55 72
I359	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	53 55 72
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	53 55 72
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	53 55 72
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	53 55 72
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	53 55 72
I480	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P	
I481	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N	
I482	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P	51
I483	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N	51
I484	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P	
I485		DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N	
I486		DIFFPAIR	AUDIO	AUD_HS_MIC_P	54 55
I487		DIFFPAIR	AUDIO	AUD_HS_MIC_N	54 55
I489		DIFFPAIR	AUDIO	HS_MIC_P	51 54
I488		DIFFPAIR	AUDIO	HS_MIC_N	51 54
I490		DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P	
I491		DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N	
I494	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	51 53
I495	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N	51 53
I493	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	51 53
I492	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N	51 53
			SB_POWER	PP3V3_S5	12 14 15 17 18 19 21 31 32 34 61 64 66 67 70 71 72
			SB_POWER	PP3V3_S0	66 67 68 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55 70 72
			SB_POWER	PP1V35_S3RS0_CPUDDR	6 8 10 21 66 67 70
			GND	GND	

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