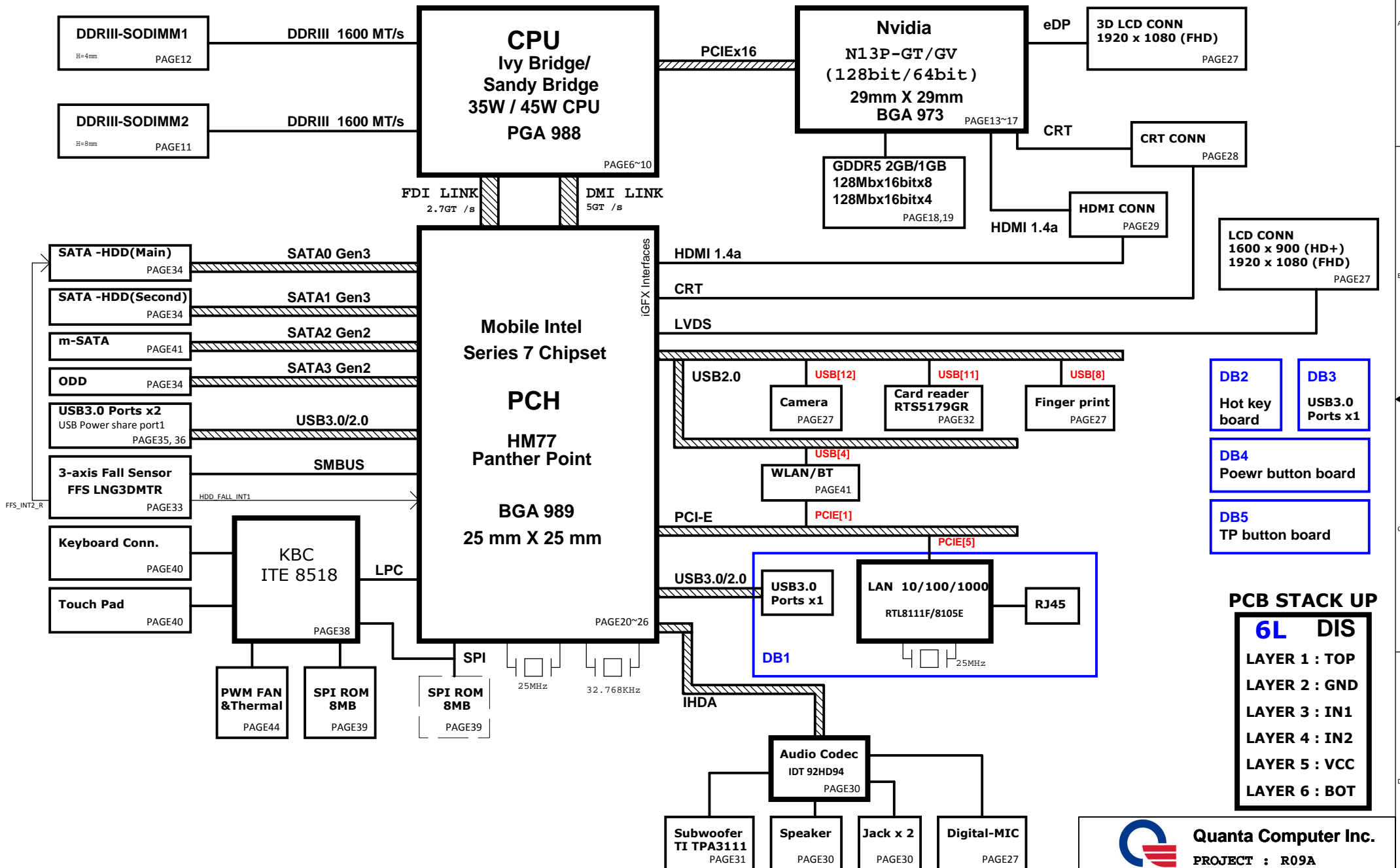
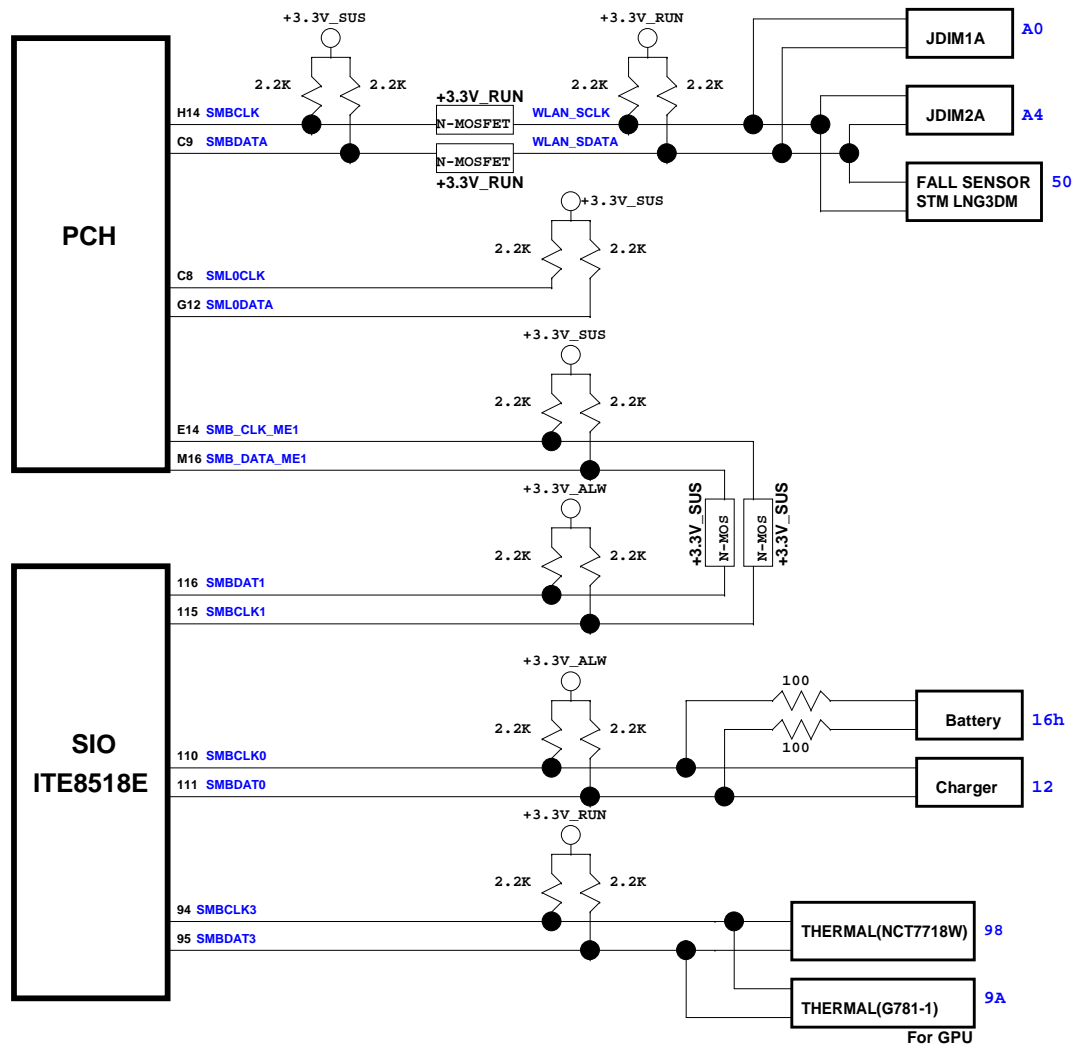


R09/A 17" OPT BLOCK DIAGRAM



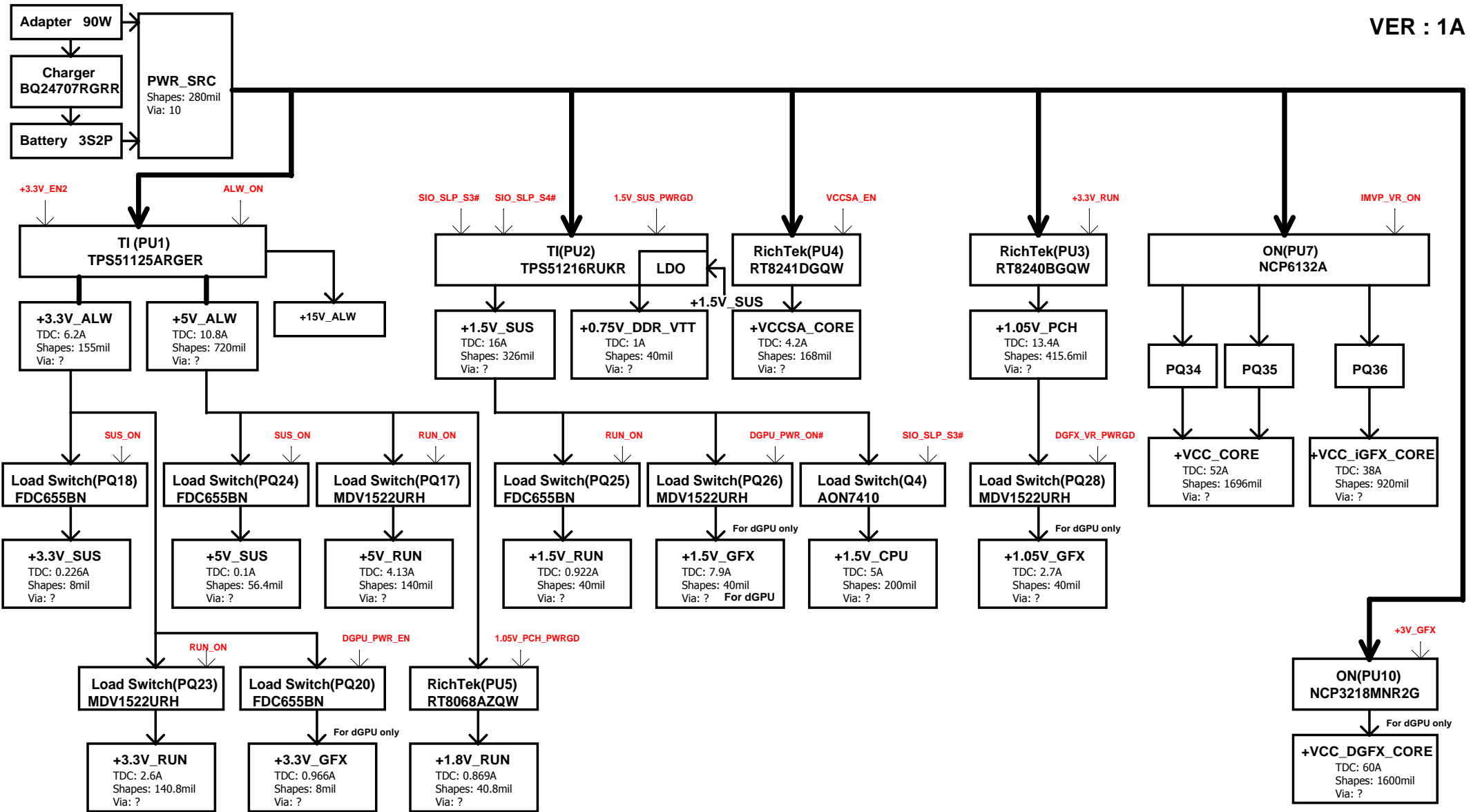


Function	IC	SMBus Address
DDR3	JDIM1A	A0
	JDIM2A	A4
Thermal IC	G781-1P8	1001101xb (9Ah)
	EMC1422	1001100xb (98h)
Charge IC	BQ24707ARGRR	0b00010010 (0x12)
Battery	Battery	16h
Fall Sensor	LNG3DM	01010000 (50h)

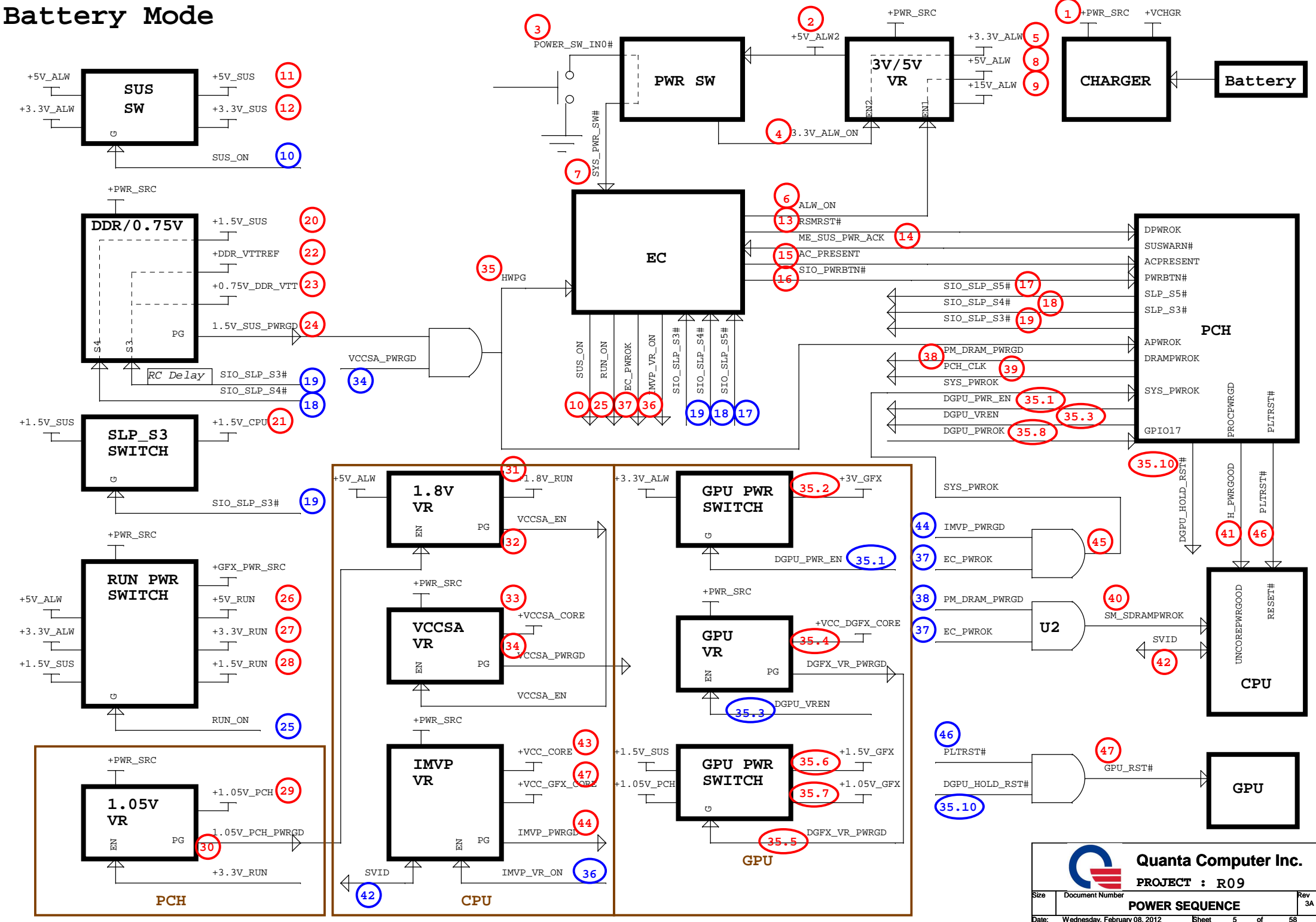
USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0 / Power share)
USB2	External port#3 (USB3.0)
USB3	External port#4 (USB3.0)
USB4	MiniCard 1 (WLAN/BT/WiMAX)
USB5	NC
USB6	X(FOR HM77)
USB7	X(FOR HM77)
USB8	Fingerprint
USB9	NC
USB10	Card Reader
USB11	Express Card
USB12	Camera
USB13	NC

SATA Master	Port Assignment
SATA0	HDD Main
SATA1	HDD Second
SATA2	mSATA
SATA3	ODD
SATA4	NC
SATA5	NC

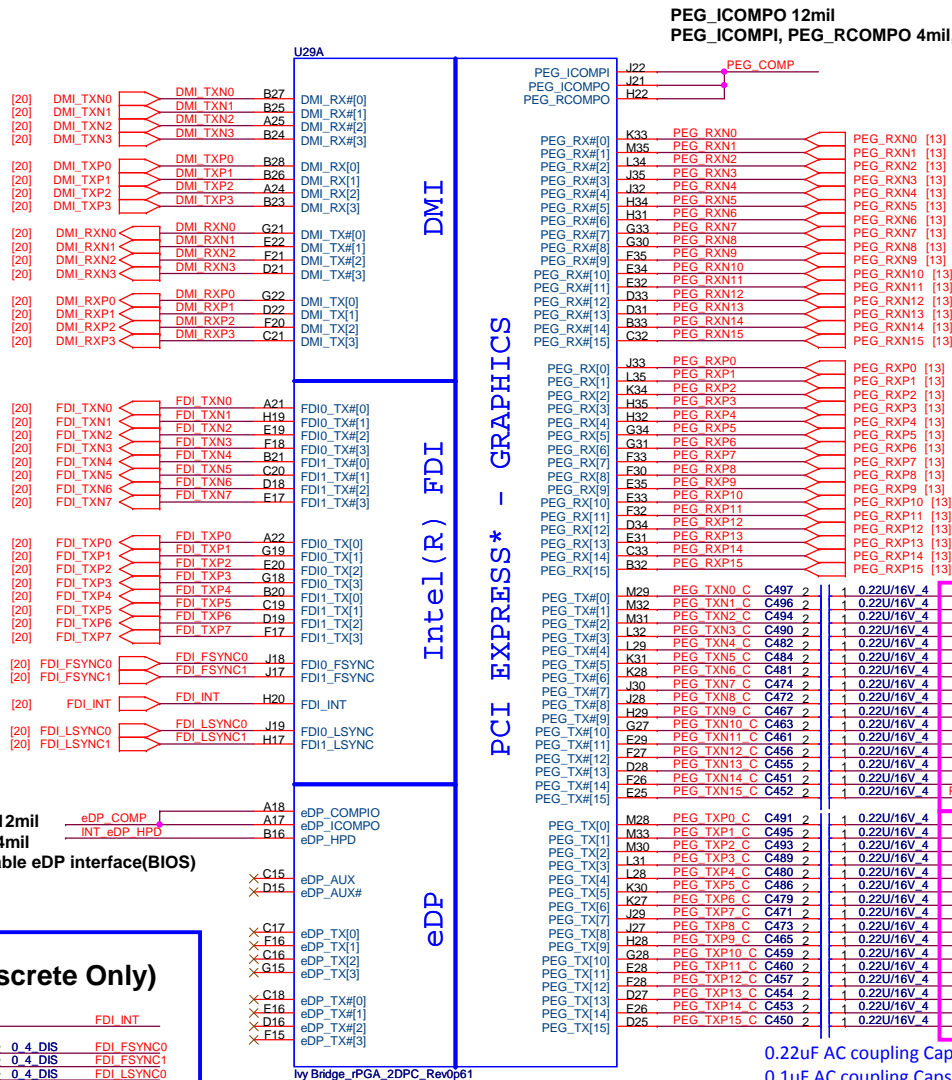
PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	NC
PCIE 3	NC
PCIE 4	NC
PCIE 5	LAN
PCIE 6	NC
PCIE 7	NC
PCIE 8	NC



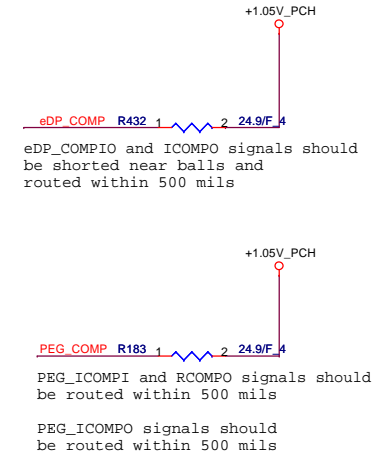
Battery Mode



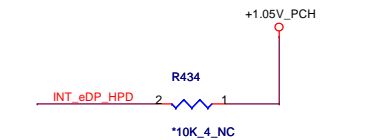
Ivy Bridge Processor (RESERVED, CFG)



DP & PEG Compensation



eDP Hot-plug (Disable)



CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

VGA (U3)	AC coupling Cap	PN	TX location	RX location (page13)
N13P-GV	0.1uF CAP CHIP 0.1U 16V(10%,X7R,0402)	CH4103K1B08	C452,C451,C455, C456,C461,C463, C467,C472,C450, C453,C454,C457, C460,C459,C465, C473	C125,C126,C147 C145,C123,C124 C152,C153,C121 C122,C151,C150 C119,C120,C149 C148
N13P-GT	0.22uF CAP CHIP 0.22U 16V(10%,X7R,0402)	CH4223K1B00	ALL	ALL

Ivy Bridge Processor (CLK,MISC,JTAG)

SNB_IVB# N.A at SNB EDS #27637 0.7v1

[23] H_SNB_IVB# ← H_SNB_IVB# C26 PROC_SELECT#
[38] H_CPUDET# ← H_CPUDET# AN34 SKTOCC#

TP1 CATERR# AL33 CATERR#

[38] PECI_EC ← PECI_EC R159 2 43 4 PECI_EC R AN33 PECI

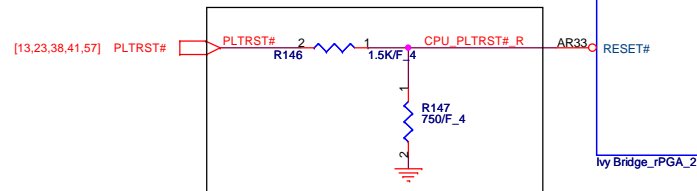
[38,53,55] IMVP7_PROCHOT# ← IMVP7_PROCHOT# R151 2 56 4 H_PROCHOT# AL32 PROCHOT#

Over 130 degree C will drive low
[25] PM_THRMTRIP# ← PM_THRMTRIP# AN32 THERMTRIP#

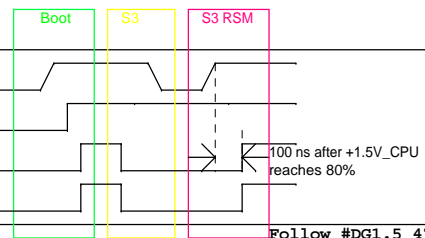
[20] H_PM_SYNC ← H_PM_SYNC AM34 PM_SYNC

[25] H_PWRGOOD ← H_PWRGOOD AP33 UNCOREPWRGOOD

10K 4 2 1 R136 SM_DRAMPWROK V8 SM_DRAMPWROK

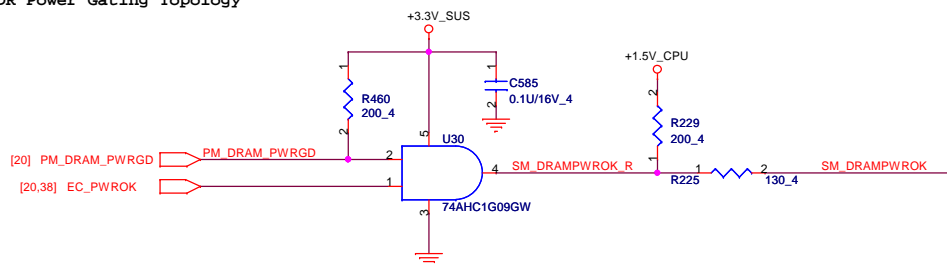


Intel spec VinH min =VCCIO X 0.7

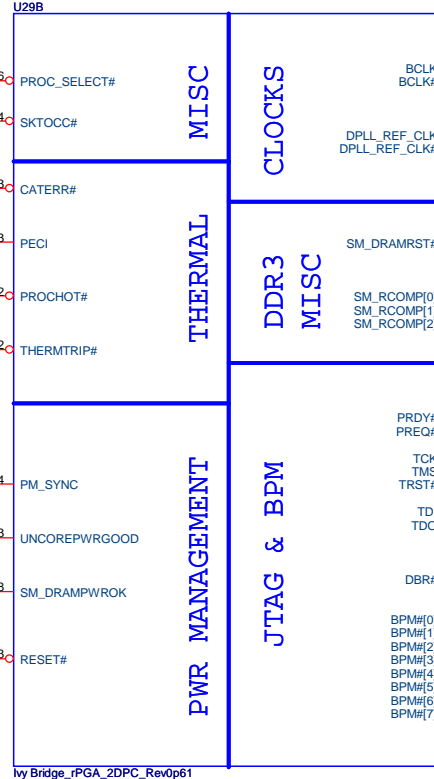


Follow #DG1.5 471984 P119

Follow #DG1.5 471984 P128
DDR Power Gating Topology



when 1,2 is high, 4 is high-impedance OFF-state



Ivy Bridge_rPGA_2DPC_Rev0p61

BCLK BCLK#
A28 CLK_CPU_BCLKP [24]
A27 CLK_CPU_BCLKN [24]

A16 CLK_DP_P_R R439 2 1K_4
A15 CLK_DP_N_R R439 2 1K_4 +1.05V_PCH

For internal eDP (Disable)

R8 CPU_DRAMRST#
AK1 SM_RCOMP_0 R236 1 2 140F_4
A5 SM_RCOMP_1 R231 1 2 25.5F_4
A4 SM_RCOMP_2 R230 1 2 200F_4

SM_RCOMP_0, SM_RCOMP_1 20mil / SM_RCOMP_2 15mil.

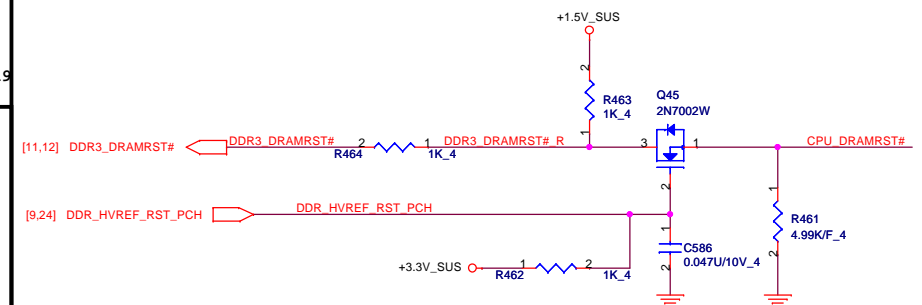
AP29 XDP_TCLK P3
AP27 XDP_TMS P5
AP30 XDP_TRST# P7
AR28 XDP_TDI P6
AP26 XDP_TDO P4

AL35 XDP_DBRST# R152 2 1K_4 +3.3V_RUN

BPM#0 AT28
BPM#1 AR29
BPM#2 AR30
BPM#3 AT33
BPM#4 AP32
BPM#5 AR31
BPM#6 AT35
BPM#7 AR33

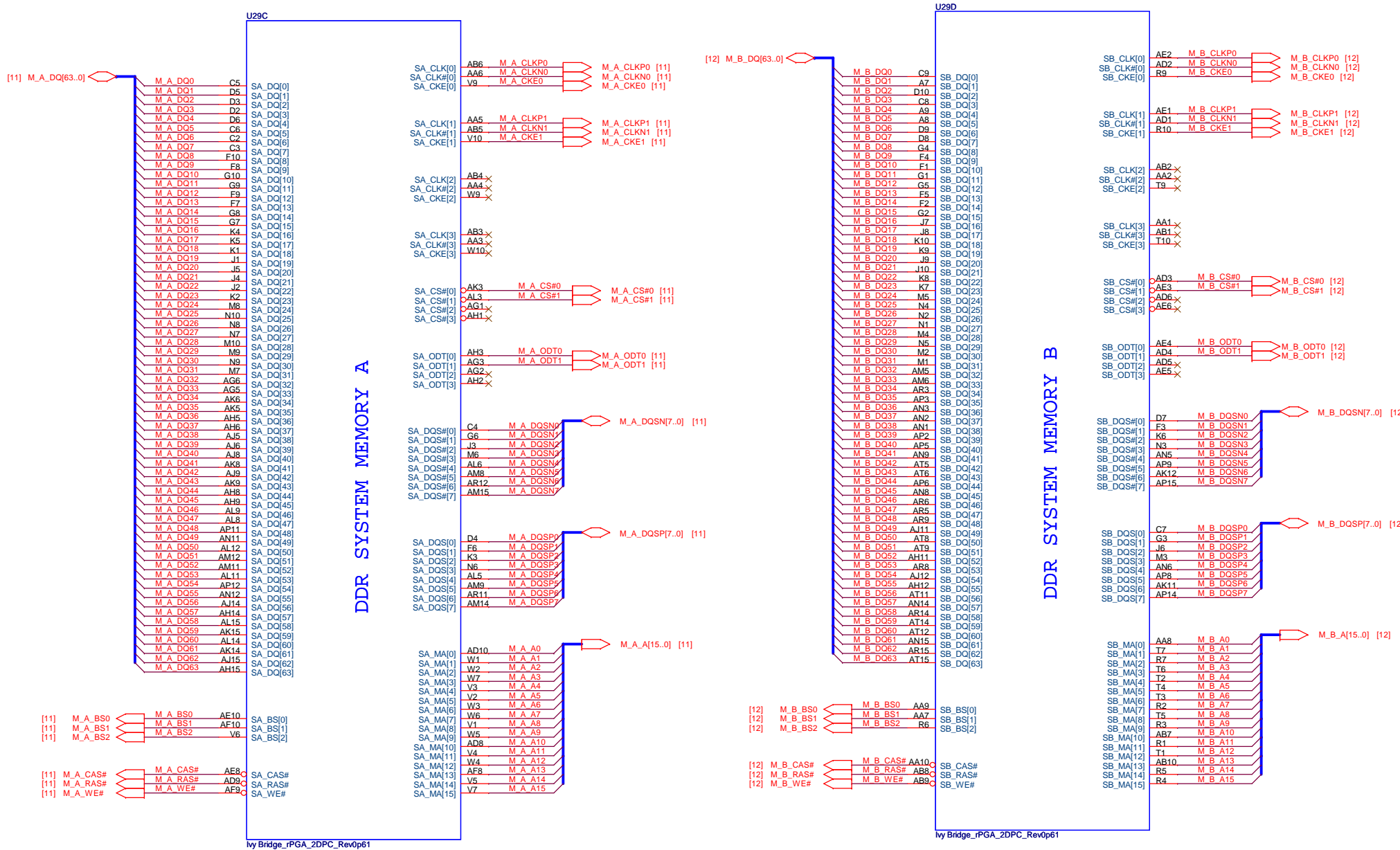
+1.05V_PCH
XDP_TMS R142 2 1 *51_4 NC
XDP_TDI R143 2 1 *51_4 NC
XDP_TDO R141 2 1 *51_4 NC
IMVP7_PROCHOT# R139 2 1 62_4
XDP_TCLK R129 1 2 *51_4 NC
XDP_TRST# R144 1 2 *51_4 NC

Follow #DG1.5 471984 P130
DRAMRST# Routing Illustration



Quanta Computer Inc.
PROJECT : R09A

Ivy Bridge Processor (DDR3)



Ivy Bridge Processor (GRAPHIC POWER)

35W	16pcs
45W	24pcs

CPU Core Power
 IVY, SNB: 35W ~ 53A
 IVY, SNB: 45W ~ 94A
 10F x24

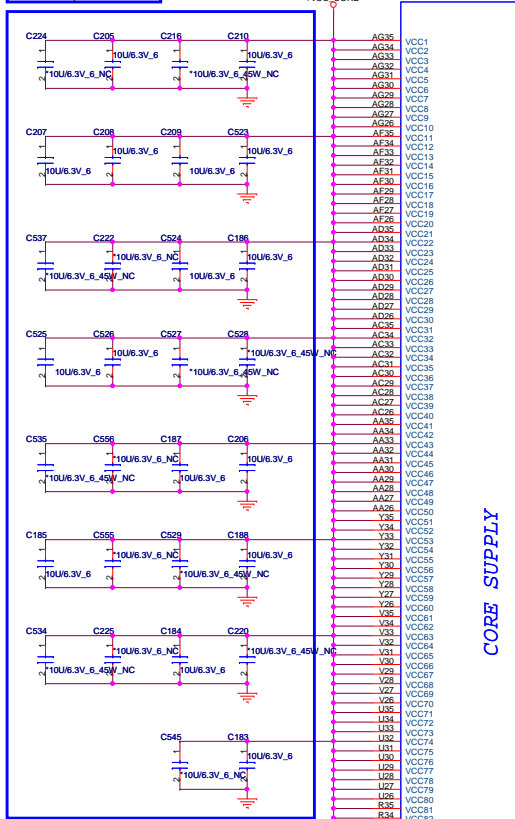
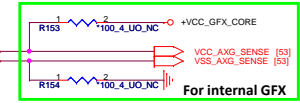
POWER

1.05V_PCH
 SNB: 8.5A
 IVY: 8.5A
 10F x12

CPU VGT
 SNB: 33A
 IVY: 33A
 10uF x 12

POWER

OTP/UMA: POP
DIS: NC

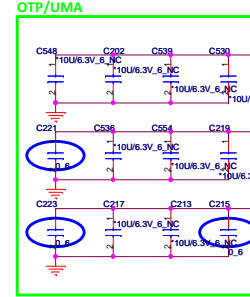


PEG AND DDR

SVID

SENSE LINES

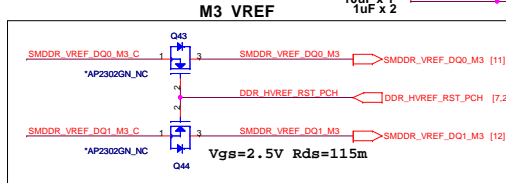
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	100Ω	27-33Ω	<25 mils
VCCAXG_SENSE / VSSAXG_SENSE	100Ω		
VCCIO_SENSE / VSS_SENSE_VCCIO	10Ω	55Ω	
VCCSA	100Ω		



DIS 0 ohm C221,C223,C215
RESISTOR CHIP 0 1/10W+5%(0603)

UMA/OTP C548,C202,C539,C530,C221,C536,C554,C219,C223,C217,C213,C215
10uF
CH6101M9905
CAP CHIP 10U 6.3V(+20%,X5R,0603)

CPU VCCPL
 SNB: 1.2A
 IVY: 1.2A
 10uF x 1
 1uF x 2



M3 VREF

Vgs=2.5V Rds=115m

GRAPHICS

1.8V RAIL

SENSE LINES

VREF

DDR3 - 1.5V RAILS

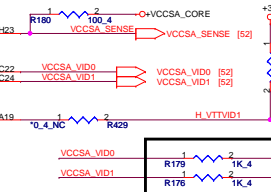
SA RAIL

MISC

CAD Note: +VDDR_REF_CPU should have 10 mil trace width
SMDR_VREF_DQ0 M3 C
SMDR_VREF_DQ1 M3 C

CPU MCH
 SNB: 5A
 IVY: 5A
 10uF x 6

CPU SA
 SNB: 6A
 IVY: 6A
 10uF x 3



R34 and R36 pull-down 1K
 Spec: This will ensure the VID is 00 prior to VCCIO stability.

5V ALW

PS_S3CNTRL

SIO_SLP_S3M

1.5V_CPU

1.5V_CPU

1.5V_CPU

1.5V_CPU

1.5V_CPU

1.5V_CPU

1.5V_CPU

S3 Power reduce

5A

1.5V_CPU

1.5V_CPU

1.5V_CPU

1.5V_CPU

1.5V_CPU

1.5V_CPU

1.5V_CPU

1.5V_CPU

1.5V_CPU

Take care Q20 Vgs(MAX)=2.5

+1.5V_CPU +VDDR_REF_CPU

+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

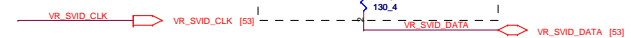
+1.5V_CPU

+1.5V_CPU

+1.5V_CPU

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK



Place PU resistor close to CPU

+1.05V_PCH

SVID DATA

VR_SVID_DATA [53]

VR_SVID_DATA [53]

VR_SVID_DATA [53]

VR_SVID_DATA [53]

VR_SVID_DATA [53]

VR_SVID_DATA [53]

VR_SVID_DATA [53]

VR_SVID_DATA [53]

Place PU resistor close to CPU

+1.05V_PCH

SVID ALERT

H_CPU_SVIDALRTM [53]

VR_SVID_ALERTM [53]

VR_SVID_ALERTM [53]

VR_SVID_ALERTM [53]

VR_SVID_ALERTM [53]

VR_SVID_ALERTM [53]

VR_SVID_ALERTM [53]

VR_SVID_ALERTM [53]

Quanta Computer Inc.
PROJECT :R09A

Ivy Bridge 4/5

Size Document Number

Date: Monday, March 06, 2012

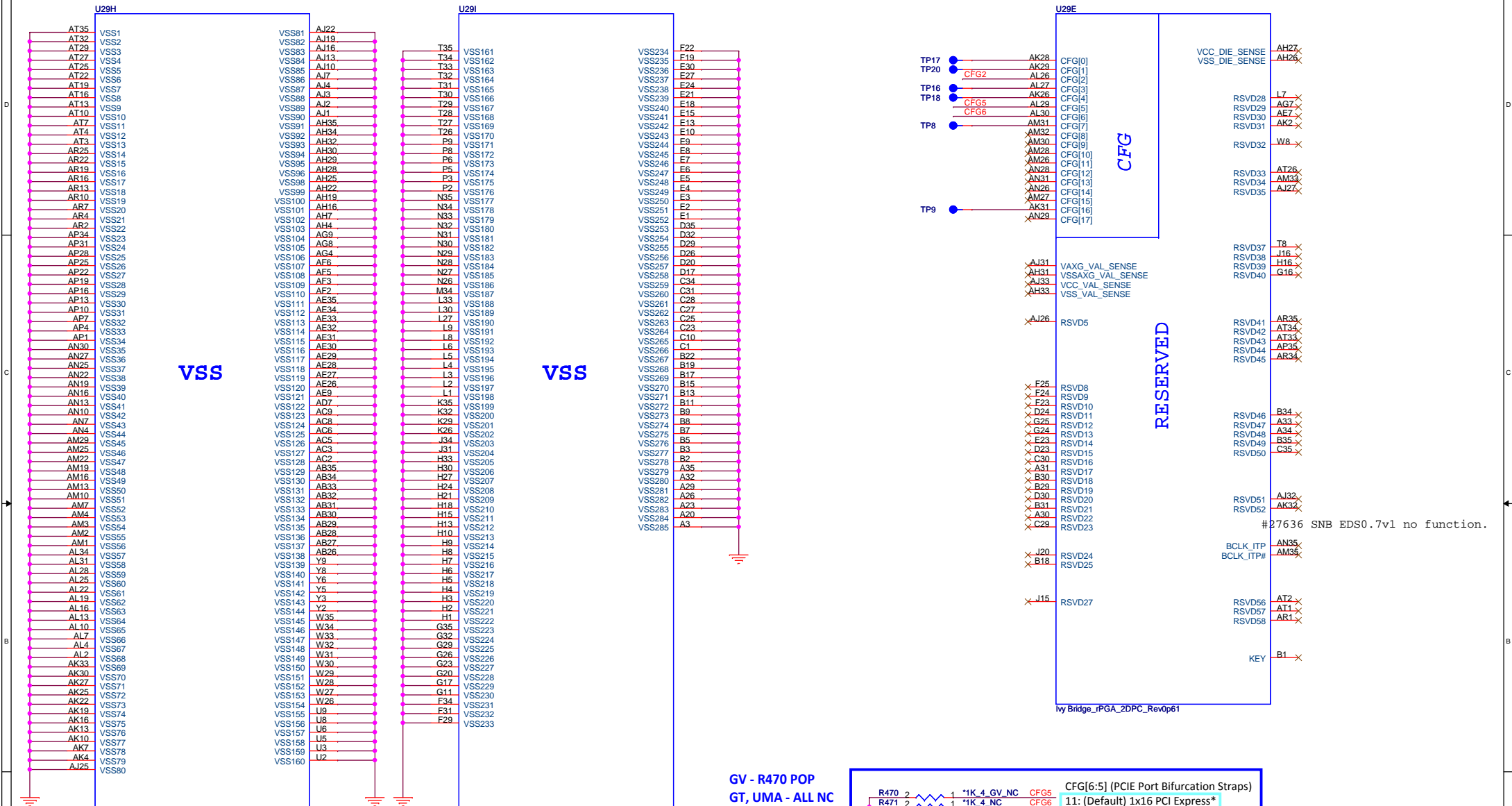
Sheet 9 of 58

Rev 3A

Rev 3A

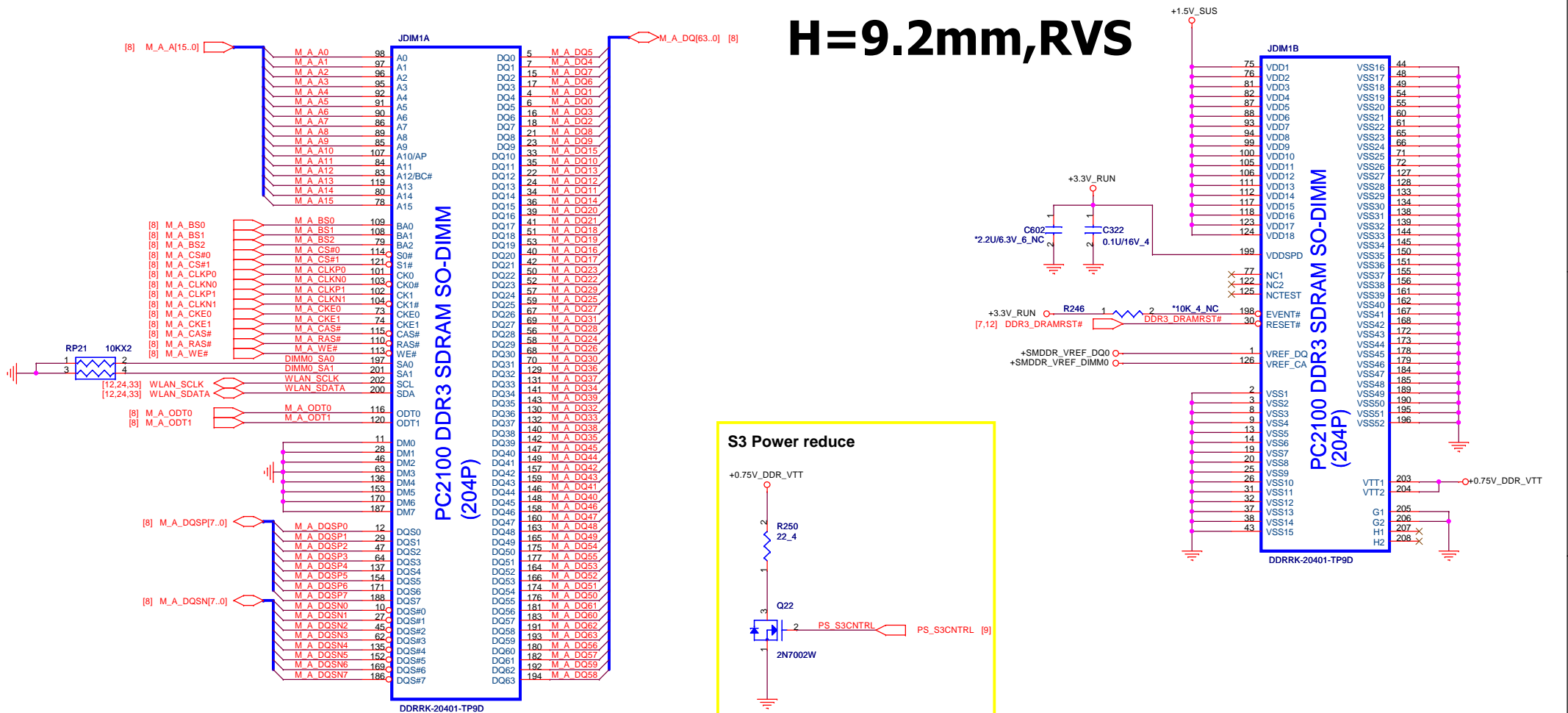
Ivy Bridge Processor (GND)

Ivy Bridge Processor (RESERVED, CFG)

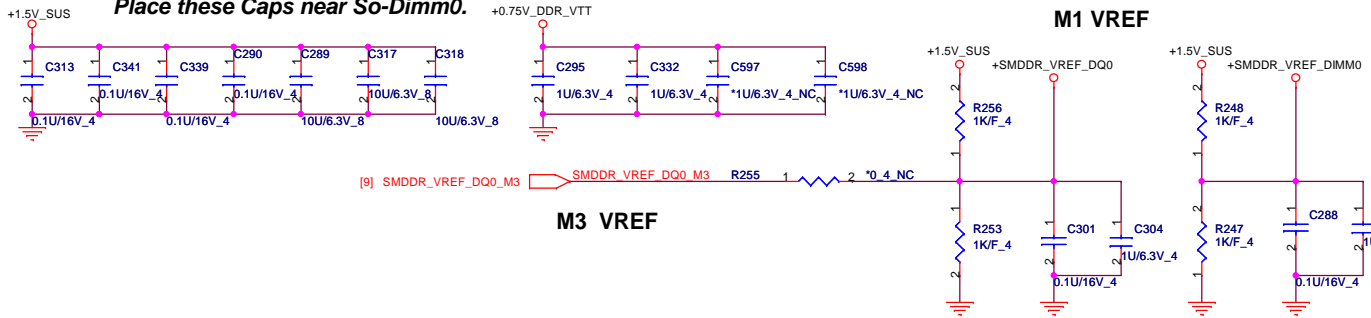


	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

H=9.2mm,RVS



Place these Caps near So-Dimm0.



H=5.2mm,RVS

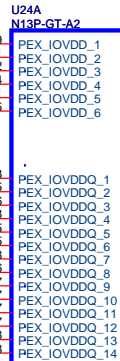
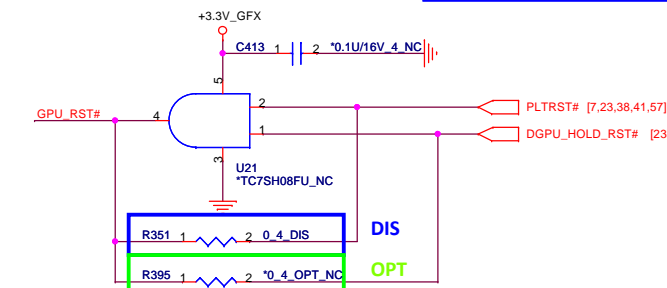
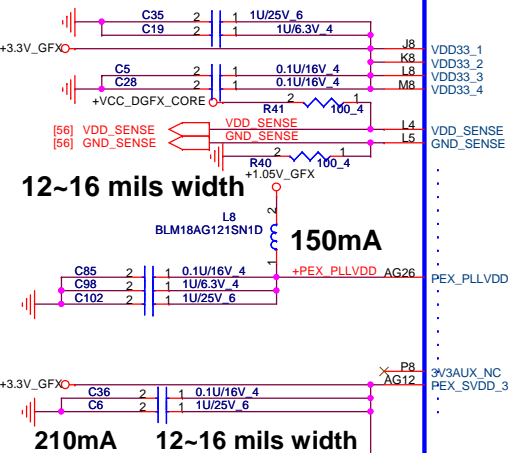
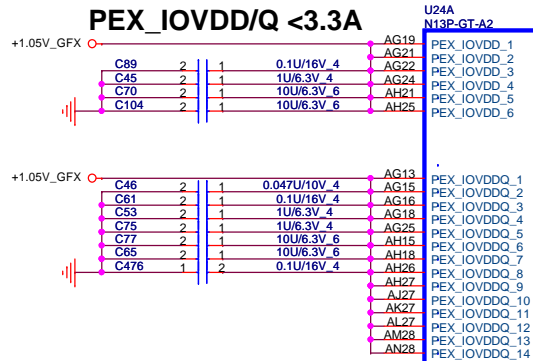
PC2100 DDR3 SDRAM SO-DIMM (204P)

PC2100 DDR3 SDRAM SO-DIMM (204P)

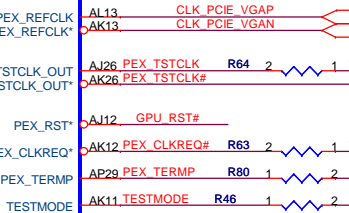
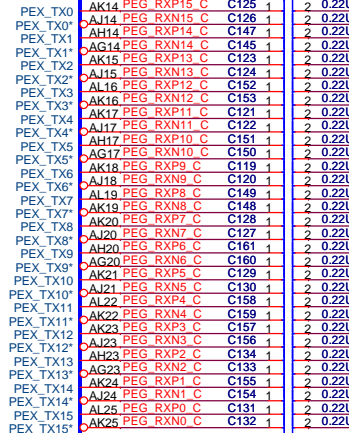
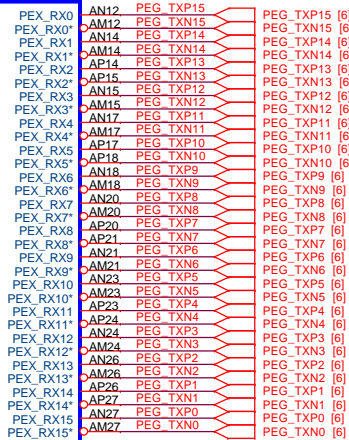
Place these Caps near So-Dimm1.

M1 VREF

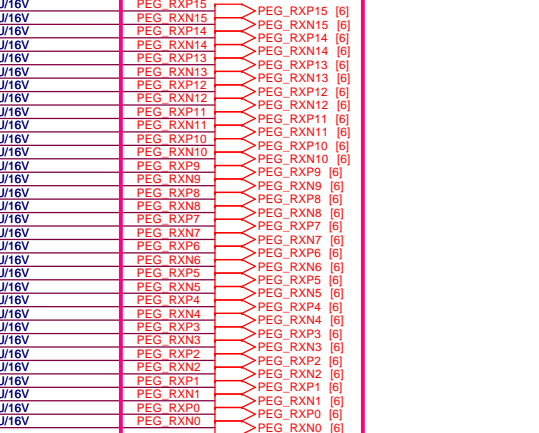
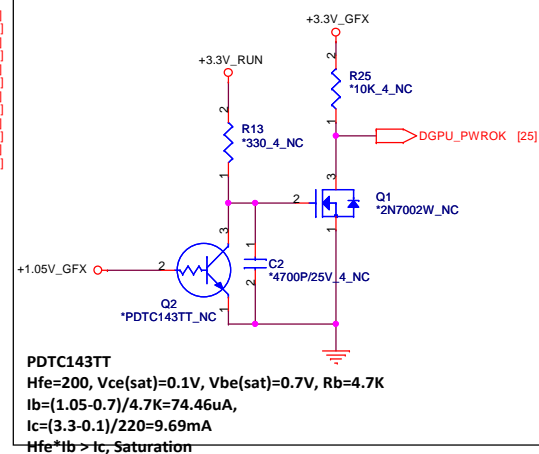
M3 REF



GB4-128 PCI EXPRESS

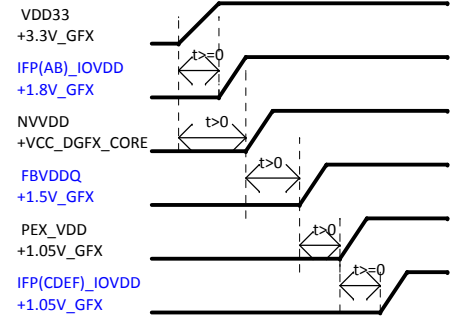


GPU all PWROK

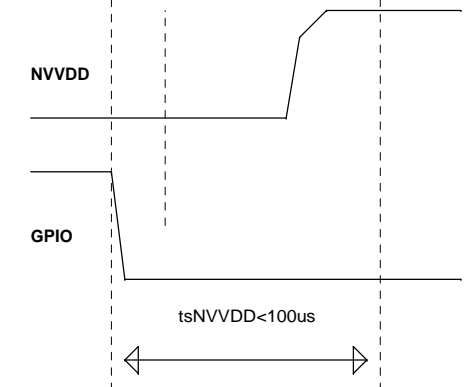


0.22uF AC coupling Caps for PCIE GEN1/2/3
0.1uF AC coupling Caps for PCIE GEN1/2

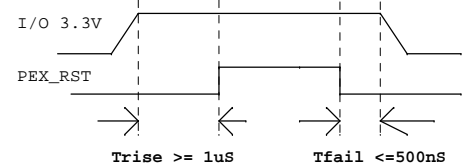
Power up sequence



NVVDD Maximum Settling Time



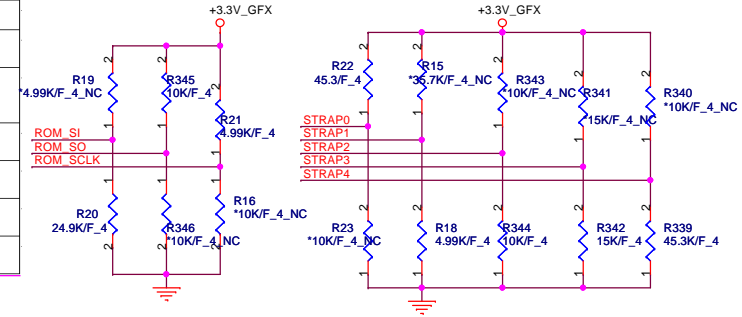
PEX_RST timing



Quanta Computer Inc.
PROJECT : R09A

N13P-GT

	N13P-GT-OPT	N13P-GT-DIS
ROM_SCLK	5K-PU	5K-PU
ROM_SO	10K-PU	10K-PU
ROM_SI	GDDR5	GDDR5
	Hynix-128MX16 ⁶ 25K-PD	Hynix-128MX16 ⁶ 25K-PD
	Samsung-128Mx16-30K-PD	Samsung-128Mx16-30K-PD
STRAP-1	5K-PD	5K-PD
STRAP-2	10K-PD	10K-PD
STRAP-3	5K-PD	15K-PD
STRAP-4	45K-PD	45K-PD



N13P-GV

For N13P-GV-B-A2, the h/w strap setting must be modified as below

ROM_SO PD 10K
ROM_SI PD 10K
ROM_SCLK PD 10K
Strap 4 PD 10K

For Hynix 128MX16 GDDR5
Strap 3 PD 10K
Strap 2 PU 10K
Strap 1 PD 10K
Strap 0 PD 10K

For Samsung 128MX16 GDDR5
Strap 3 PD 10K
Strap 2 PU 10K
Strap 1 PD 10K
Strap 0 PD 10K

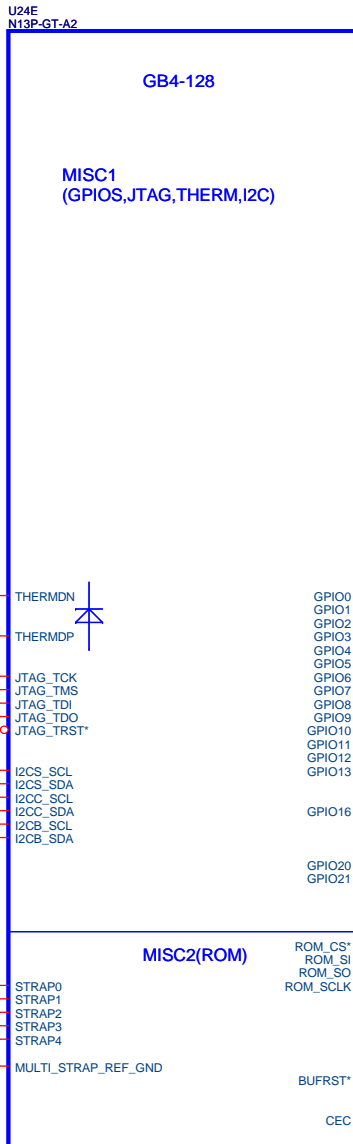
Default: Hynix VRAM (0100) VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Quanta P/N	Vendor P/N	ROM_SI
0100	GDDR5 128Mx16, 2500MHz	Hynix	AKG5MWUTW14	H5GQ2H24MFR-T2C	PD 25K
0101	GDDR5 128Mx16, 2500MHz	Samsung	AKG5MWDT509	K4G20325FD-F	PD 30K

SOR_EXPOSED[3:0]		STRAP3
0000	Optimus	PD 5K
0010	Discret only	PD 15K

Display conifauration table

GPIO	I/O	ACTIVE	USAGE
0	OUT	N/A	NVDD VID4
1	OUT	N/A	NVDD VID3
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID1
6	OUT	N/A	NVDD VID2
7	OUT	N/A	3D VERSION LEFT/RIGHT SIGNAL
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	MEMORY VREF CONTROL
11	OUT	N/A	NVDD VID0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	NVDD VID5



	Output	VID0	VID1	VID2	VID3	VID4	VID5
N13P-GV (QS)	0.875V	0	1	0	0	1	1
N13P-GT (QS)	0.9V	0	0	0	0	1	1

+VCC_DGFX_CORE

U24F
N13P-GT-A2

GB4-128
NVVDD

AA12	VDD_001	VDD_057	V18
AA14	VDD_002	VDD_058	AB18
AA16	VDD_003	VDD_059	V20
AA19	VDD_004	VDD_060	V22
AA21	VDD_005	VDD_061	W12
AA23	VDD_006	VDD_062	W14
AB13	VDD_007	VDD_063	W16
AB15	VDD_008	VDD_064	W19
AB17	VDD_009	VDD_065	W21
AB20	VDD_010	VDD_066	W23
AB22	VDD_011	VDD_067	Y15
AC12	VDD_012	VDD_068	Y17
AC14	VDD_013	VDD_069	Y18
AC16	VDD_014	VDD_070	Y20
AC19	VDD_015	VDD_071	Y22
AC21	VDD_016	VDD_072	U1
AC23	VDD_017	XVDD_01	U2
M12	VDD_018	XVDD_02	U3
M14	VDD_019	VDD_03	U4
M16	VDD_020	XVDD_04	U5
M19	VDD_021	XVDD_05	U6
M21	VDD_022	XVDD_06	U7
M23	VDD_023	XVDD_07	U8
N13	VDD_024	XVDD_08	V1
N15	VDD_025	XVDD_09	V2
N17	VDD_026	XVDD_10	V3
N18	VDD_027	XVDD_11	V4
N20	VDD_028	XVDD_12	V5
N22	VDD_029	XVDD_13	V6
P12	VDD_030	XVDD_14	V7
P14	VDD_031	XVDD_15	V8
P16	VDD_032	XVDD_16	W2
P19	VDD_033	XVDD_17	W3
P21	VDD_034	XVDD_18	W4
P23	VDD_035	XVDD_19	W5
R13	VDD_036	XVDD_20	W7
R15	VDD_037	XVDD_21	W8
R17	VDD_038	XVDD_22	Y1
R18	VDD_039	XVDD_23	Y2
R20	VDD_040	XVDD_24	Y3
R22	VDD_041	XVDD_25	Y4
T12	VDD_042	XVDD_26	Y5
T14	VDD_043	XVDD_27	Y6
T16	VDD_044	XVDD_28	Y7
T19	VDD_045	XVDD_29	Y8
T21	VDD_046	XVDD_30	AA1
T23	VDD_047	XVDD_31	AA2
U13	VDD_048	XVDD_32	AA3
U15	VDD_049	XVDD_33	AA4
U17	VDD_050	XVDD_34	AA5
U18	VDD_051	XVDD_35	AA6
U20	VDD_052	XVDD_36	AA7
U22	VDD_053	XVDD_37	AA8
V13	VDD_054	XVDD_38	.
V15	VDD_055	.	.
V17	VDD_056	.	.

+VCC_DGFX_CORE

GT: 60A all POP

GV: 42A NC C34,C38,C72

NVVDD Decoupling

+VCC_DGFX_CORE

C34	1	2	0.01U/25V 4 GT
C73	1	2	0.01U/25V 4
C83	1	2	0.01U/25V 4
C74	1	2	0.01U/25V 4
C69	1	2	0.01U/25V 4
C81	1	2	0.01U/25V 4
C84	1	2	0.01U/25V 4
C50	1	2	0.01U/25V 4
C38	1	2	0.01U/25V 4 GT
C51	1	2	0.01U/25V 4
C39	1	2	0.01U/25V 4
C66	1	2	0.1U/16V 4
C72	1	2	0.1U/16V 4 GT
C48	1	2	0.1U/16V 4
C80	1	2	0.1U/16V 4
C40	1	2	0.1U/16V 4
C52	1	2	1U/6.3V 4
C68	1	2	1U/6.3V 4
C82	1	2	1U/6.3V 4
C67	1	2	1U/6.3V 4
C60	1	2	1U/25V 6
C59	1	2	10U/6.3V 6
C43	1	2	10U/6.3V 6
C58	1	2	10U/6.3V 6
C26	1	2	10U/6.3V 6

330uF*2 at power plane

U24G
N13P-GT-A2

GB4-128
GROUND

A2	GND_1	E22
A33	GND_2	E10
AA13	GND_3	D33
AA15	GND_4	E25
AA17	GND_5	E5
AA18	GND_6	E7
AA20	GND_7	E28
AA22	GND_8	F7
AB12	GND_9	G10
AB14	GND_10	G11
AB16	GND_11	G12
AB19	GND_12	G13
AB2	GND_13	G19
AB21	GND_14	G2
AB23	GND_15	G22
AB28	GND_16	G25
AB30	GND_17	G28
AB32	GND_18	G3
AB5	GND_19	G30
AB7	GND_20	G32
AC13	GND_21	G33
AC15	GND_22	G5
AC17	GND_23	G7
AC18	GND_24	K2
AC20	GND_25	K28
AC22	GND_26	K30
AE2	GND_27	K32
AE28	GND_28	K33
AE30	GND_29	K5
AE32	GND_30	K7
AE33	GND_31	M13
AE5	GND_32	M15
AE7	GND_33	M17
AH10	GND_34	M18
AH13	GND_35	M20
AH16	GND_36	M22
AH19	GND_37	N12
AH2	GND_38	N14
AH22	GND_39	N16
AH24	GND_40	N19
AH28	GND_41	N2
AH29	GND_42	N21
AH30	GND_43	N23
AH32	GND_44	N28
AH33	GND_45	N30
AH5	GND_46	N32
AH7	GND_47	N33
A17	GND_48	N5
AK10	GND_49	N7
AK7	GND_50	P13
AL12	GND_51	P15
AL14	GND_52	P17
AL15	GND_53	P18
AL17	GND_54	P20
AL18	GND_55	P22
AL2	GND_56	R12
AL20	GND_57	R14
AL21	GND_58	R16
AL23	GND_59	R19
AL24	GND_60	R21
AL26	GND_61	R23
AL28	GND_62	T13
AL30	GND_63	T15
AL32	GND_64	T17
AL33	GND_65	T18
AL5	GND_66	T2
AM13	GND_67	T20
AM16	GND_68	T22
AM19	GND_69	AG11
AM22	GND_70	T28
AN1	GND_71	T32
AN10	GND_72	T5
AN13	GND_73	T7
AN16	GND_74	U12
AN19	GND_75	U14
AN22	GND_76	U16
AN25	GND_77	U19
AN30	GND_78	U21
AN34	GND_79	U23
AN4	GND_80	V12
AN7	GND_81	V14
AP2	GND_82	V16
AP33	GND_83	V19
B1	GND_84	V21
B10	GND_85	V23
B22	GND_86	W13
B25	GND_87	W15
B28	GND_88	W17
B31	GND_89	W18
B34	GND_90	W20
B4	GND_91	W22
B7	GND_92	W28
C10	GND_93	Y12
C13	GND_94	Y14
C19	GND_95	Y16
C22	GND_96	Y19
C25	GND_97	Y21
C28	GND_98	Y23
C7	GND_99	AH11
D2	GND_100	C16
D31	GND_101	W32
	GND_102	



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Size Document Number 17 of 58

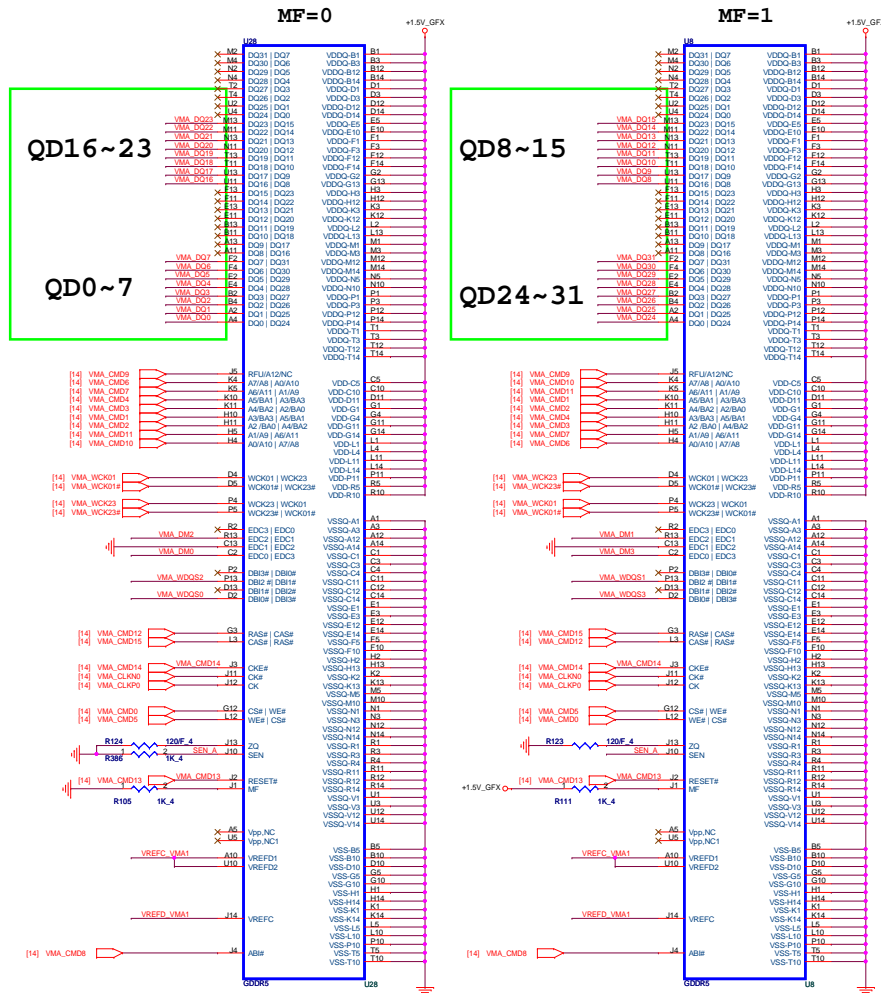
N13P-GS (POWER & GND) 5/5

Date: Saturday, March 03, 2012

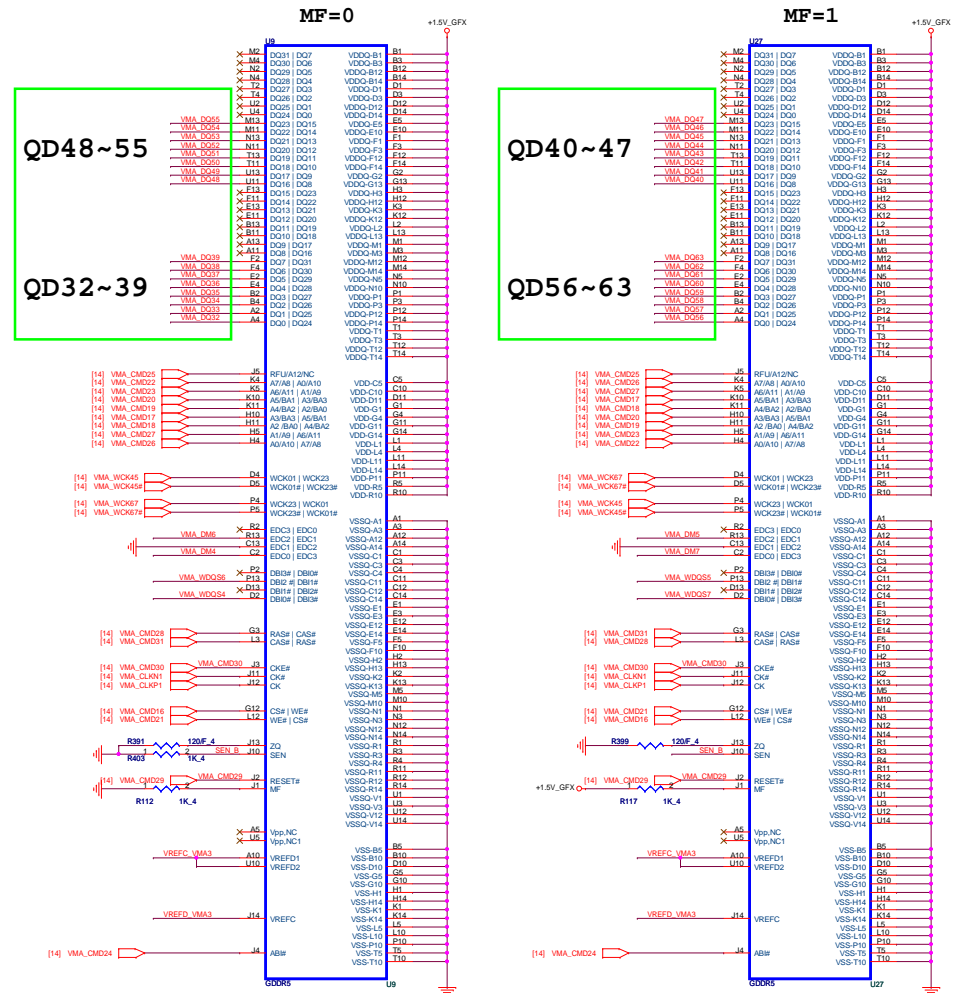
Sheet 17 of 58

Rev 3A

LOWER HALF



UPPER HALF



GDDR5 Mode H Mapping		
< 0-31	> 32-63	Memory
CM0	CM16	CS*
CM1	CM17	A1_BA3
CM2	CM18	A2_BA0
CM3	CM19	A4_BA2
CM4	CM20	A5_BA1
CM5	CM21	WE*
CM6	CM22	A7_BA
CM7	CM23	A6_A11
CM8	CM24	AB*
CM9	CM25	A12_RFU
CM10	CM26	A0_A10
CM11	CM27	A1_A9
CM12	CM28	RAS*
CM13	CM29	RST*
CM14	CM30	CE*
CM15	CM31	CAS*

CHANNEL B: 1024MB GDDR5

LOWER HALF

UPPER HALF

MF=0

MF=1

MF=0

MF=1

QD16~23

QD0~7

QD8~15

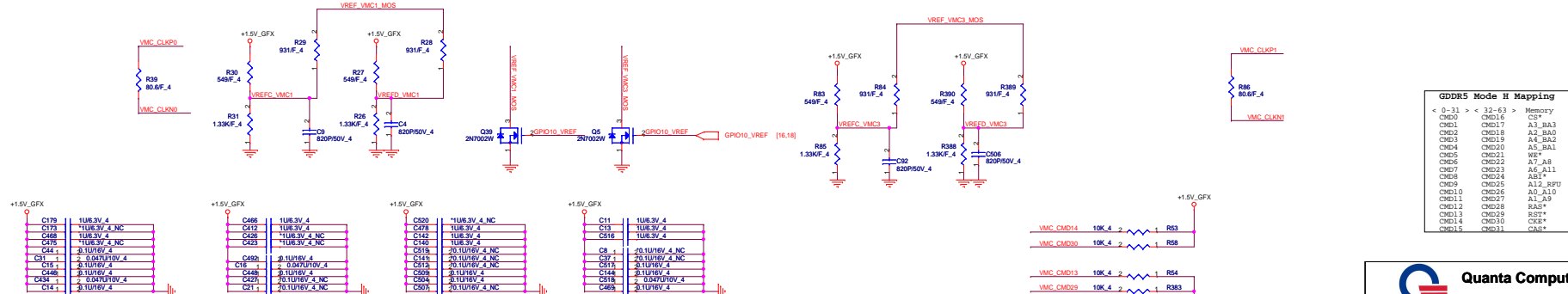
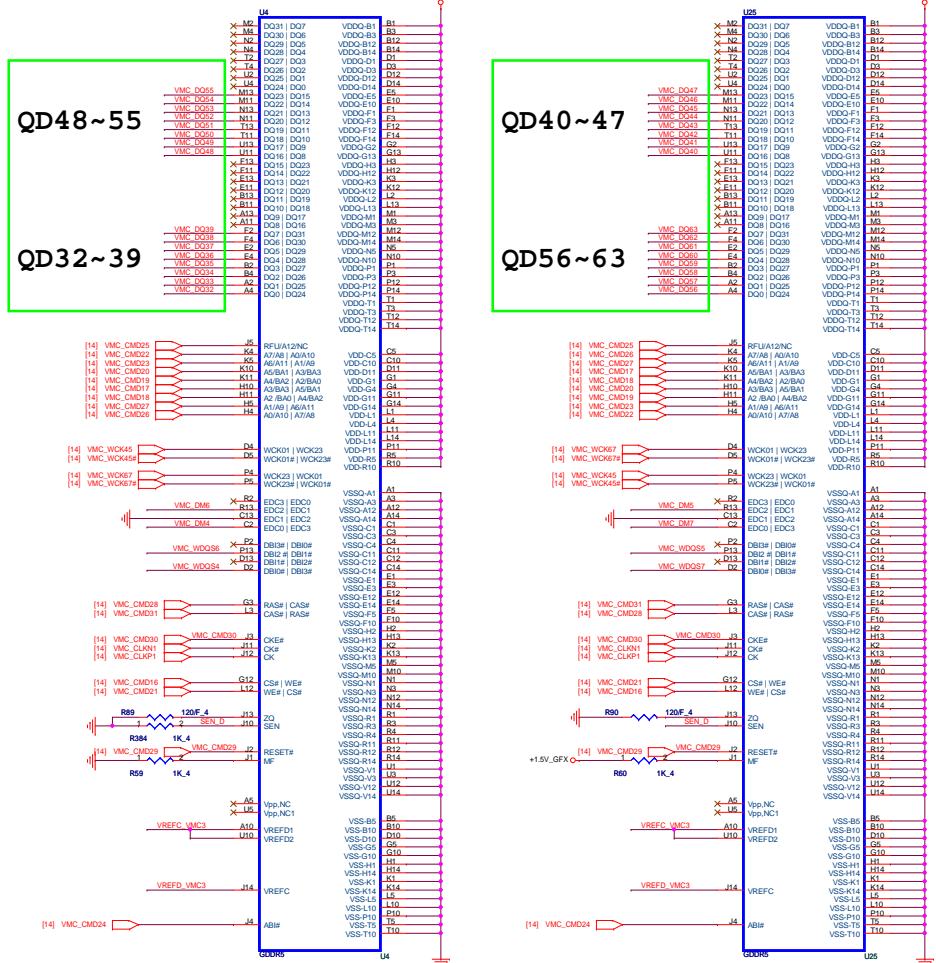
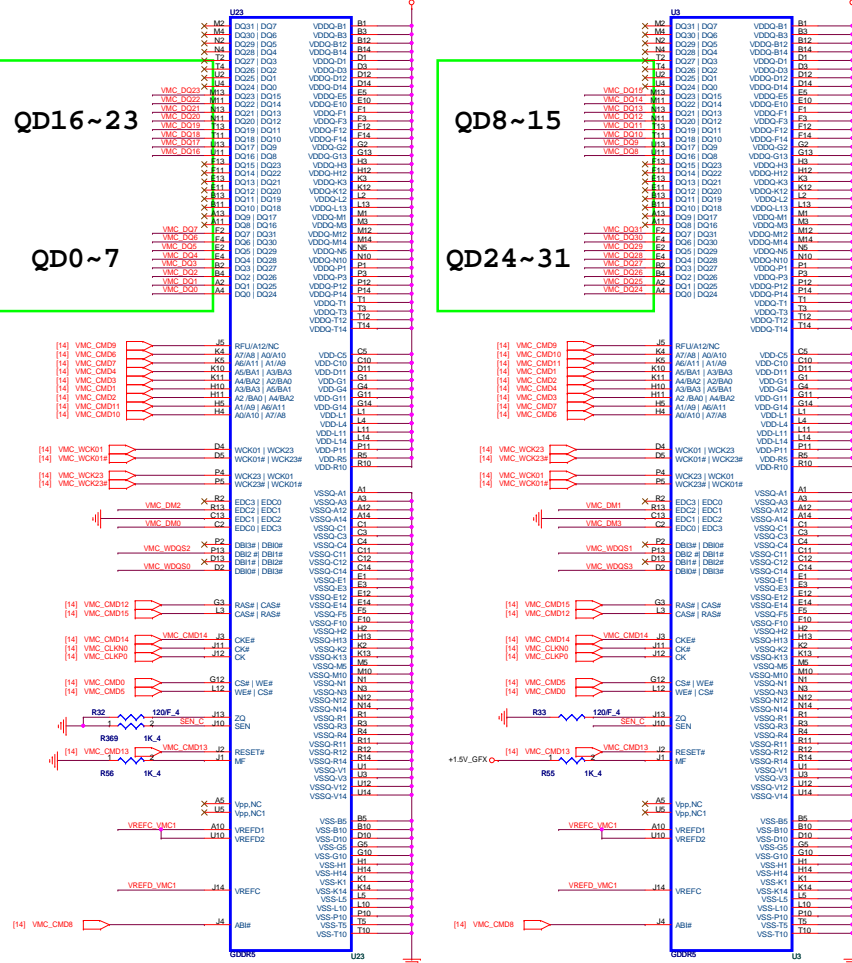
QD24~31

QD48~55

QD32~39

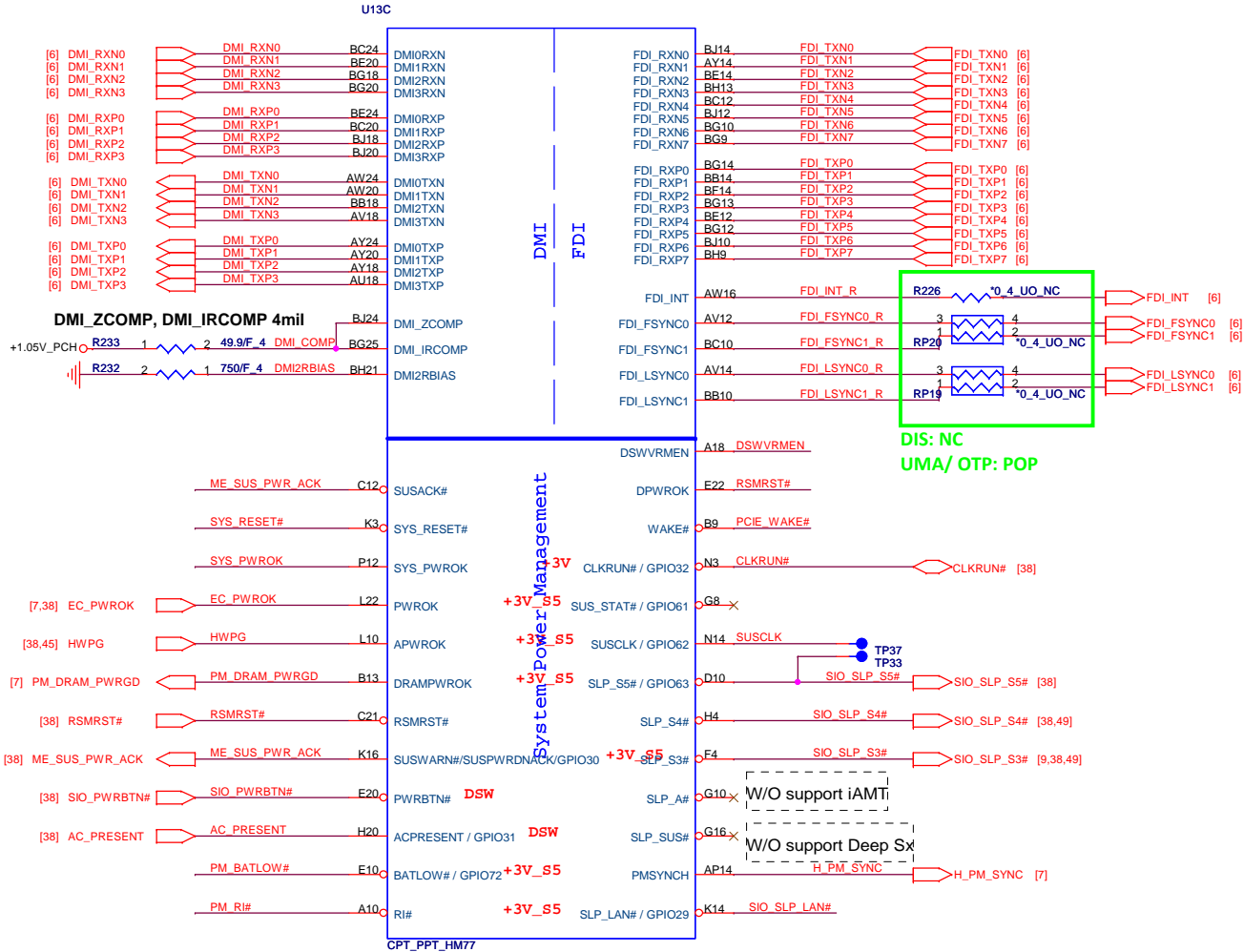
QD40~47

QD56~63

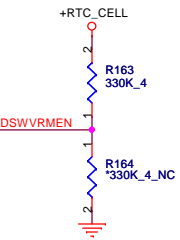
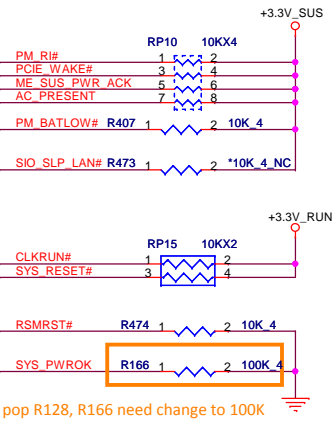


GDDR5 Mode H Mapping	
< 0-31 >	< 32-63 >
QD16	QD32
QD17	QD33
QD18	QD34
QD19	QD35
QD20	QD36
QD21	QD37
QD22	QD38
QD23	QD39
QD24	QD40
QD25	QD41
QD26	QD42
QD27	QD43
QD28	QD44
QD29	QD45
QD30	QD46
QD31	QD47
QD32	QD48
QD33	QD49
QD34	QD50
QD35	QD51
QD36	QD52
QD37	QD53
QD38	QD54
QD39	QD55
QD40	QD56
QD41	QD57
QD42	QD58
QD43	QD59
QD44	QD60
QD45	QD61
QD46	QD62
QD47	QD63

Cougar Point/Panther Point (DMI,FDI,PM)



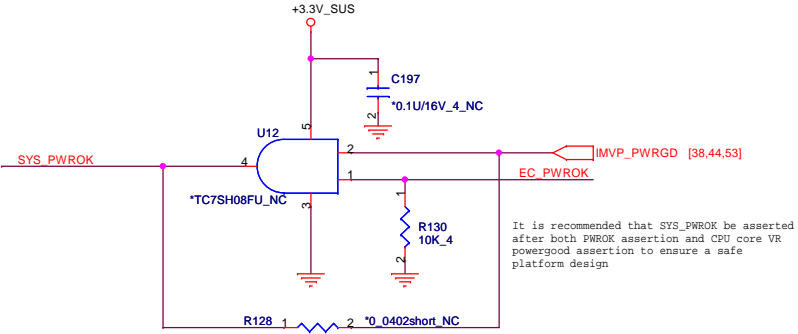
PCH Pull-high/low(CLG)



On Die DSW VR Enable

High = Enable (Default)

Low = Disable



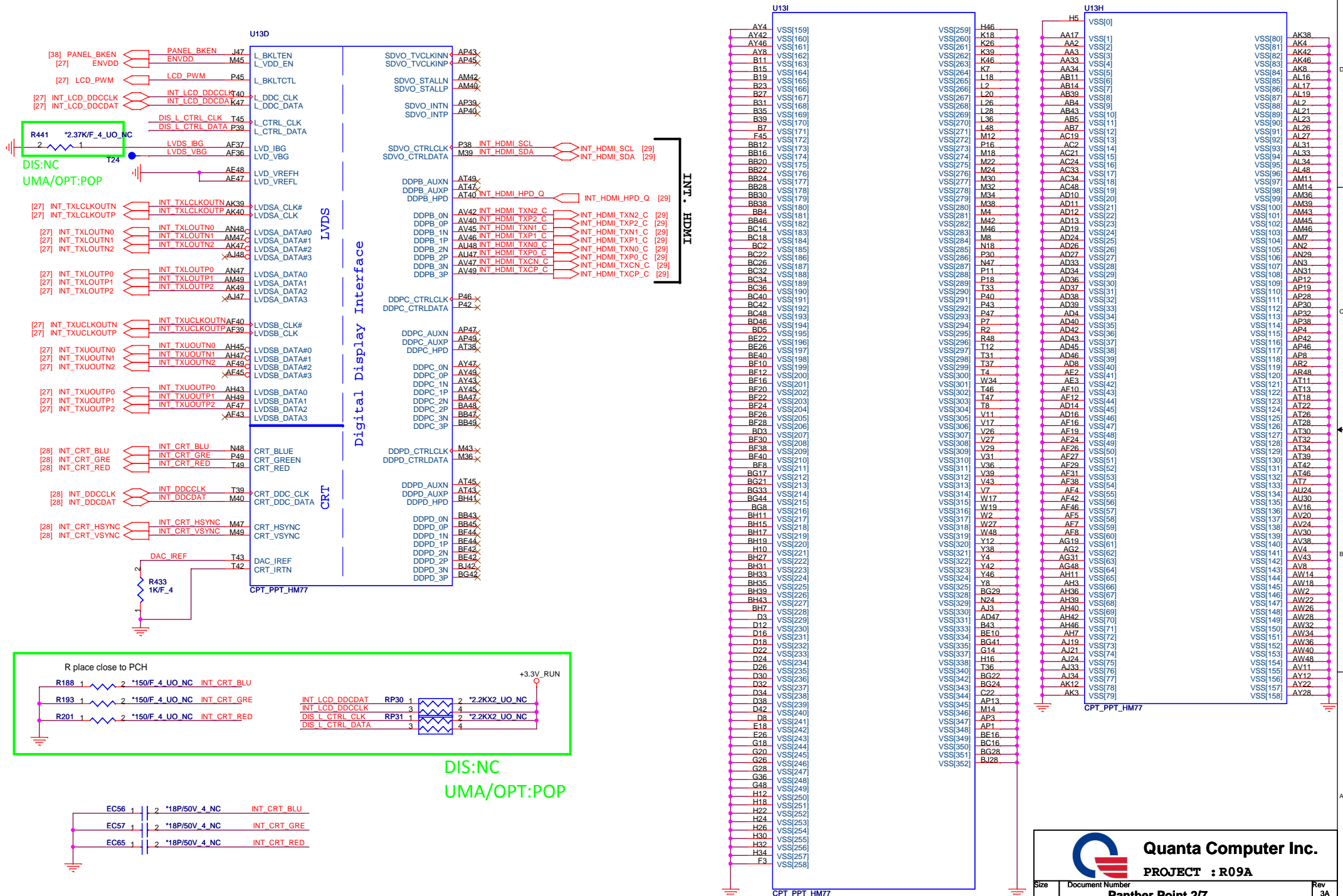
It is recommended that SYS_PWROK be asserted after both PWROK assertion and CPU core VR powergood assertion to ensure a safe platform design



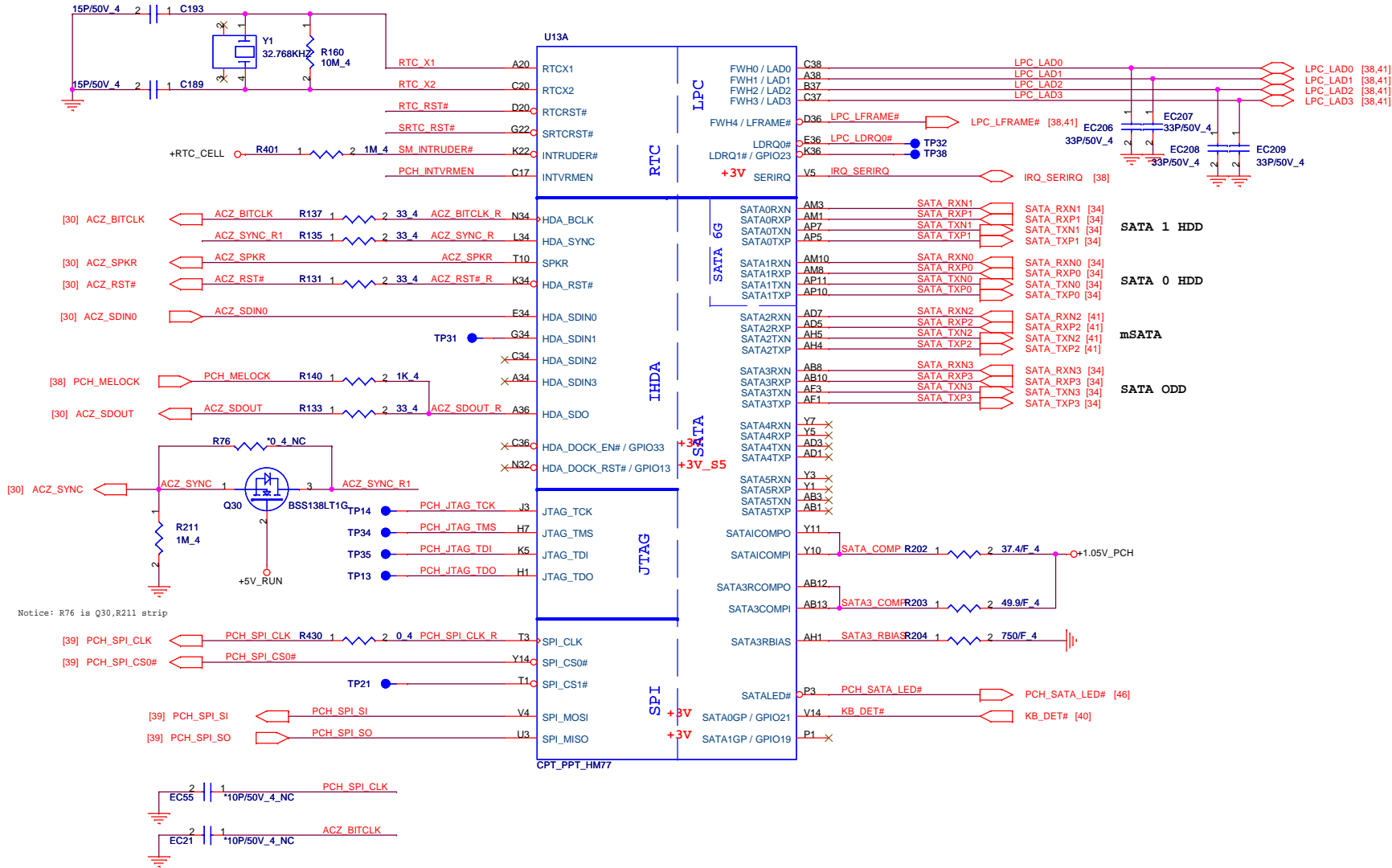
Quanta Computer Inc.

PROJECT : R09A

Cougar Point/Panther Point (GND)

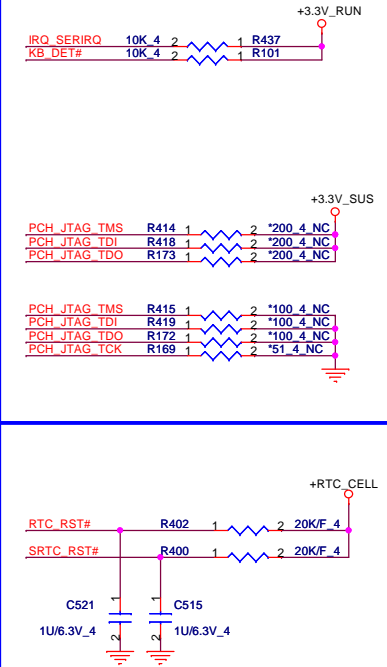


Cougar Point/Panther Point (HDA,JTAG,SATA)

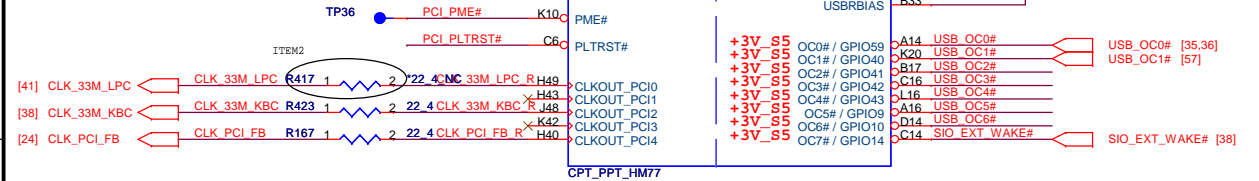
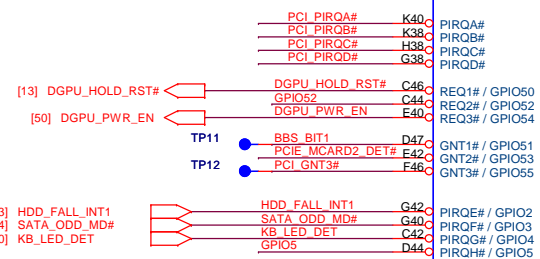
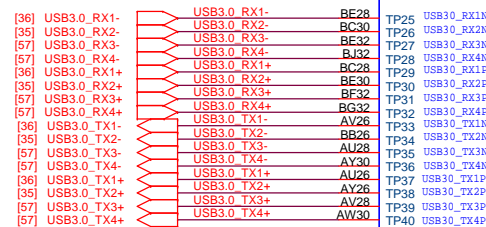
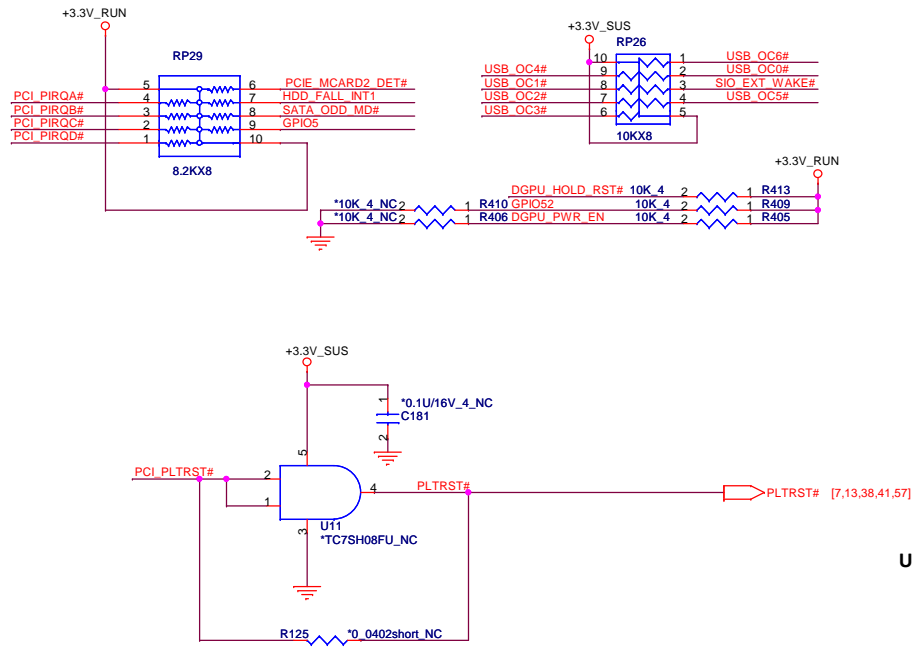


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	NC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	NC
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL ○ R162 1 2 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS ○ R134 1 2 1K 4 ACZ_SYNC R



Cougar Point-M/Panther Point (PCI,USB,NVRAM)



Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>Bit 0</th><th>Bit 1</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										

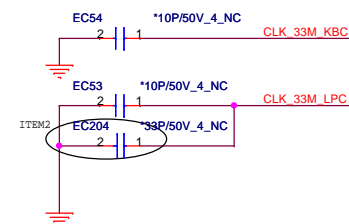
Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm
--------	---------------------------------------	-------	-----------------------

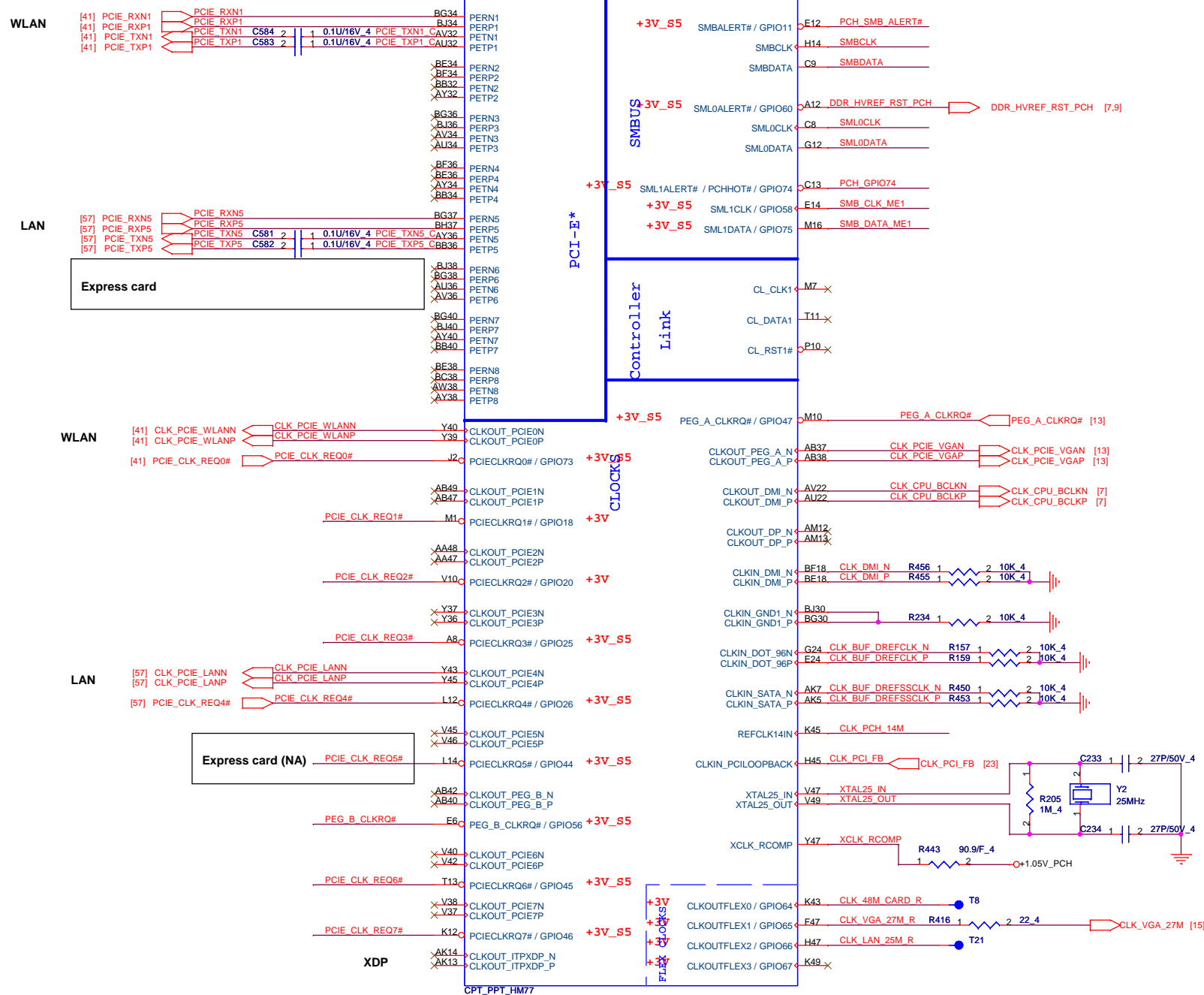
R216 2.2K 4 0+1.8V_RUN

R214 1K 4 DF_TVS [25]

H_SNB_IVB# [7]

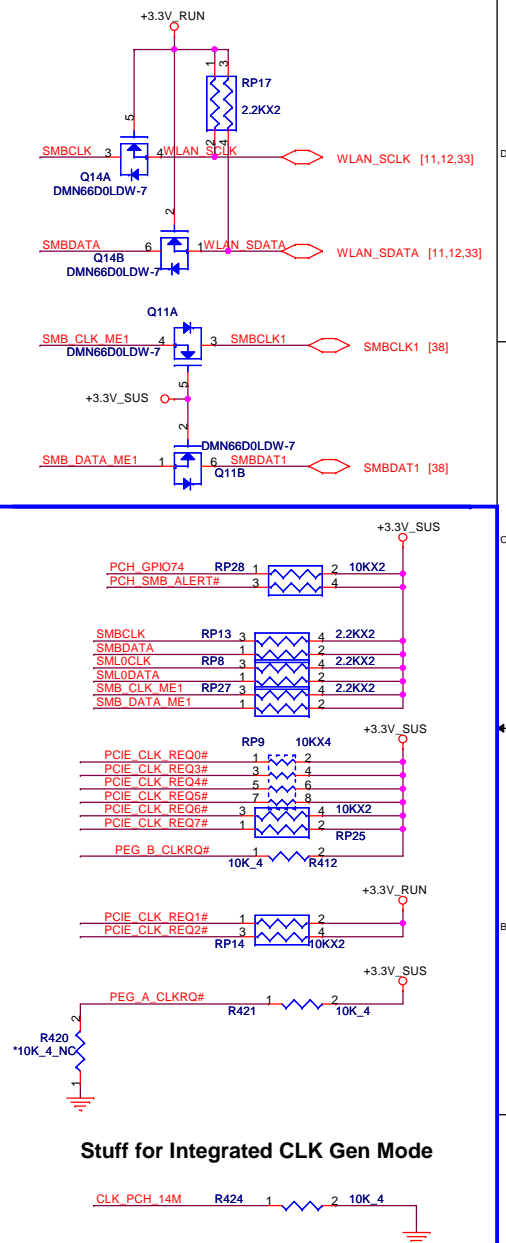


U13B Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 /GPIO64	• 33 /27 /48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 /GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX2 /GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 /GPIO67	• 27/14.318 output to SIO / 48/24 MHz (Default)

SMBus/Pull-up(CLG)



Stuff for Integrated CLK Gen Mode



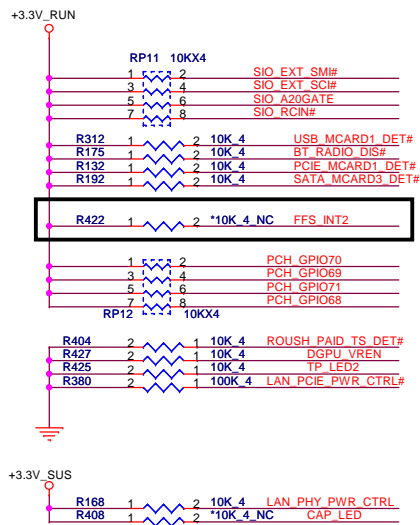
Quanta Computer Inc.

PROJECT : R09A

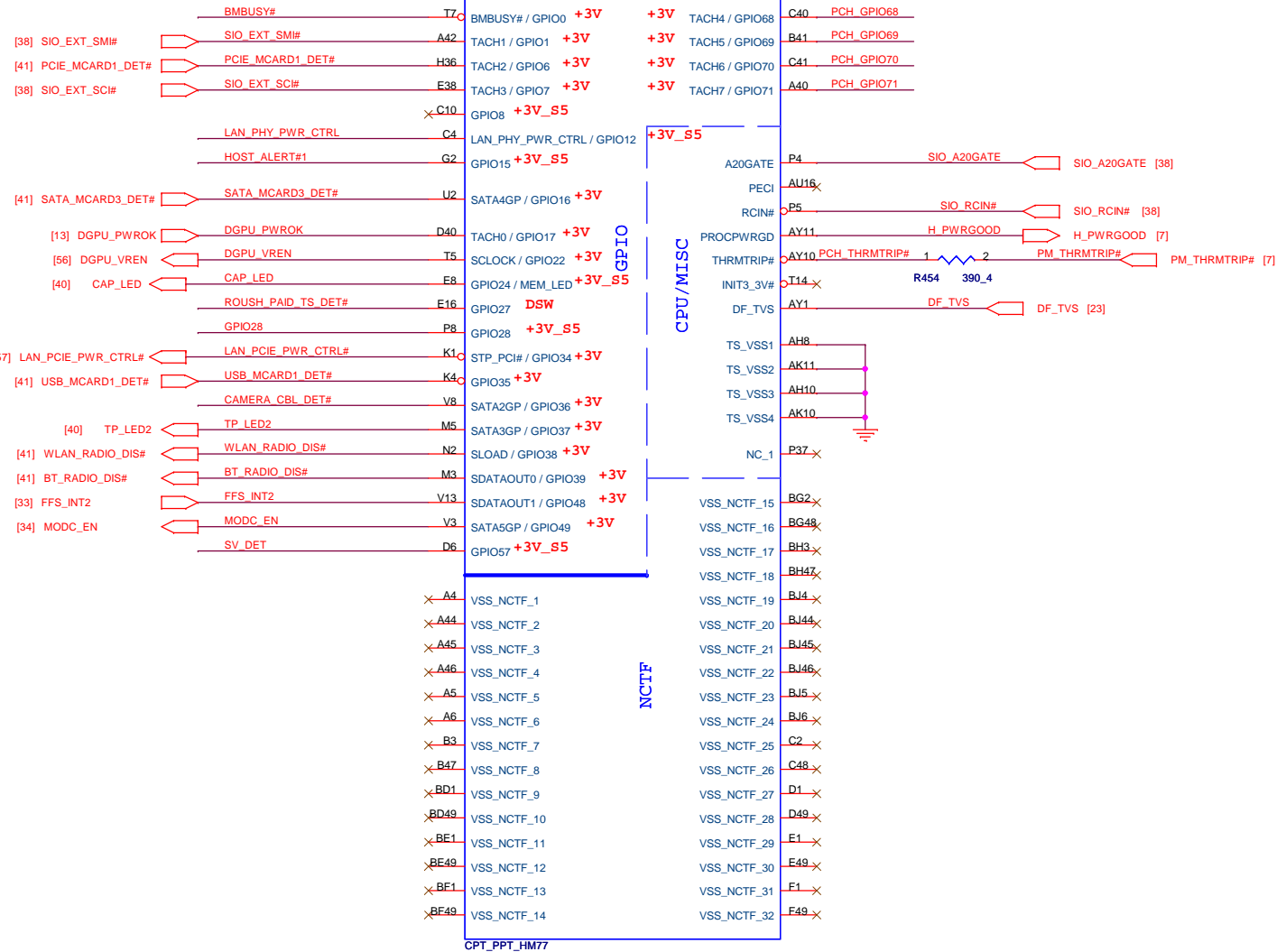
Panther Point 5/7

Size	Document Number	Rev
	Panther Point 5/7	3A
Date:	Wednesday, February 08, 2012	Sheet 24 of 58

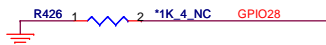
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



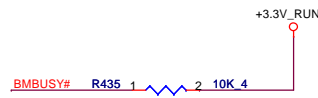
Vostro POP - NA



Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)



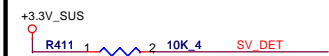
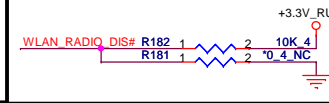
CHECK LIST:
When Unused as GPIO or SATA*GP - Use 8.2K-10K pull-down to ground.



BMBUSY#:
If not used, require a weak pull-up
(8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and
100 ohm on this net for validation purpose.

Intel ME Crypto Transport Layer
Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

MFG-TEST

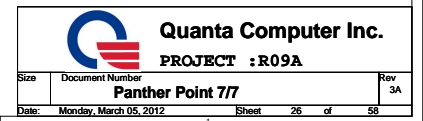


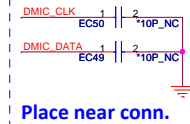
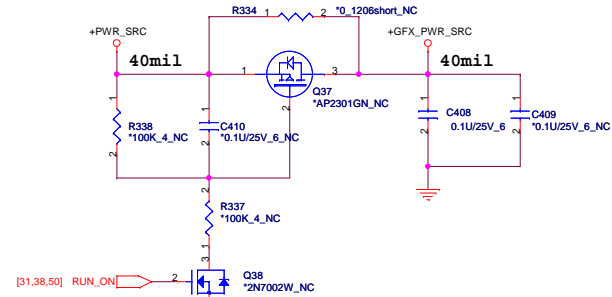
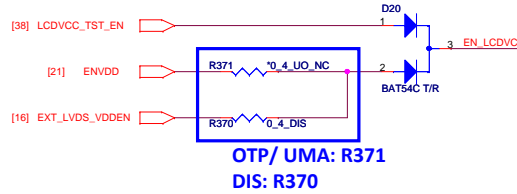
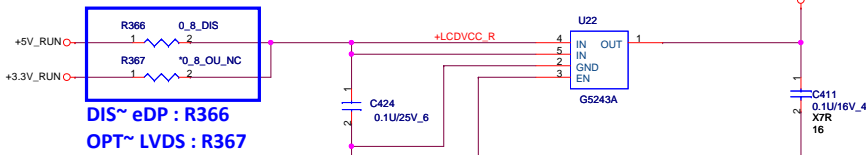
Quanta Computer Inc.
PROJECT : R09A

Size	Document Number	Rev
1	Panther Point 6/7	3A

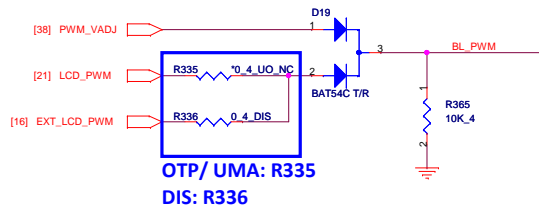
Date: Wednesday, February 08, 2012 Sheet 25 of 58

Cougar Point/Panther Point (POWER)

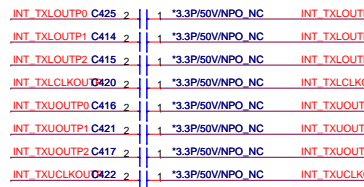




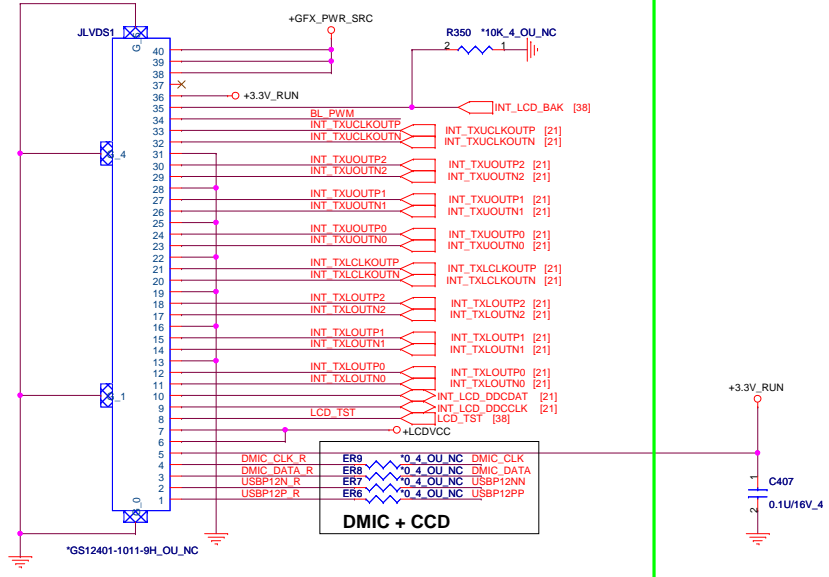
Backlight Control



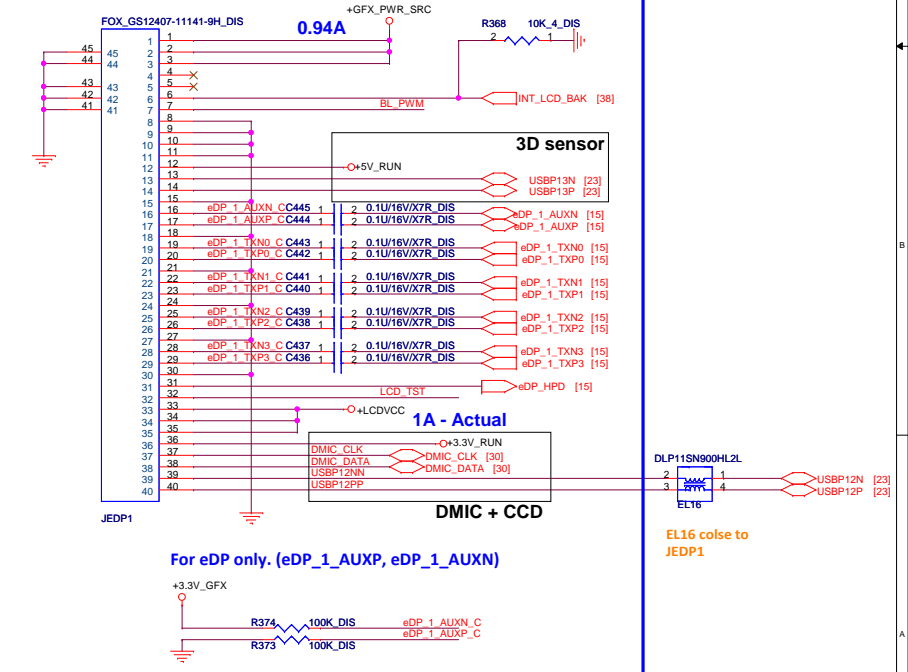
EMC Reserve



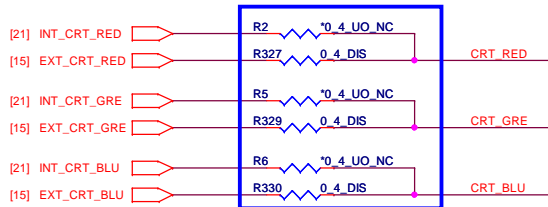
Normal Panel - 40pin



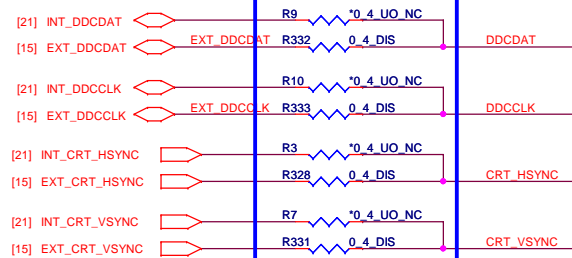
3D Panel - DIS turbo - 40pin



VGA

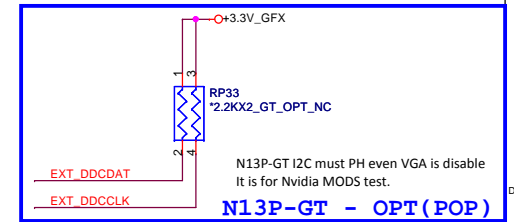
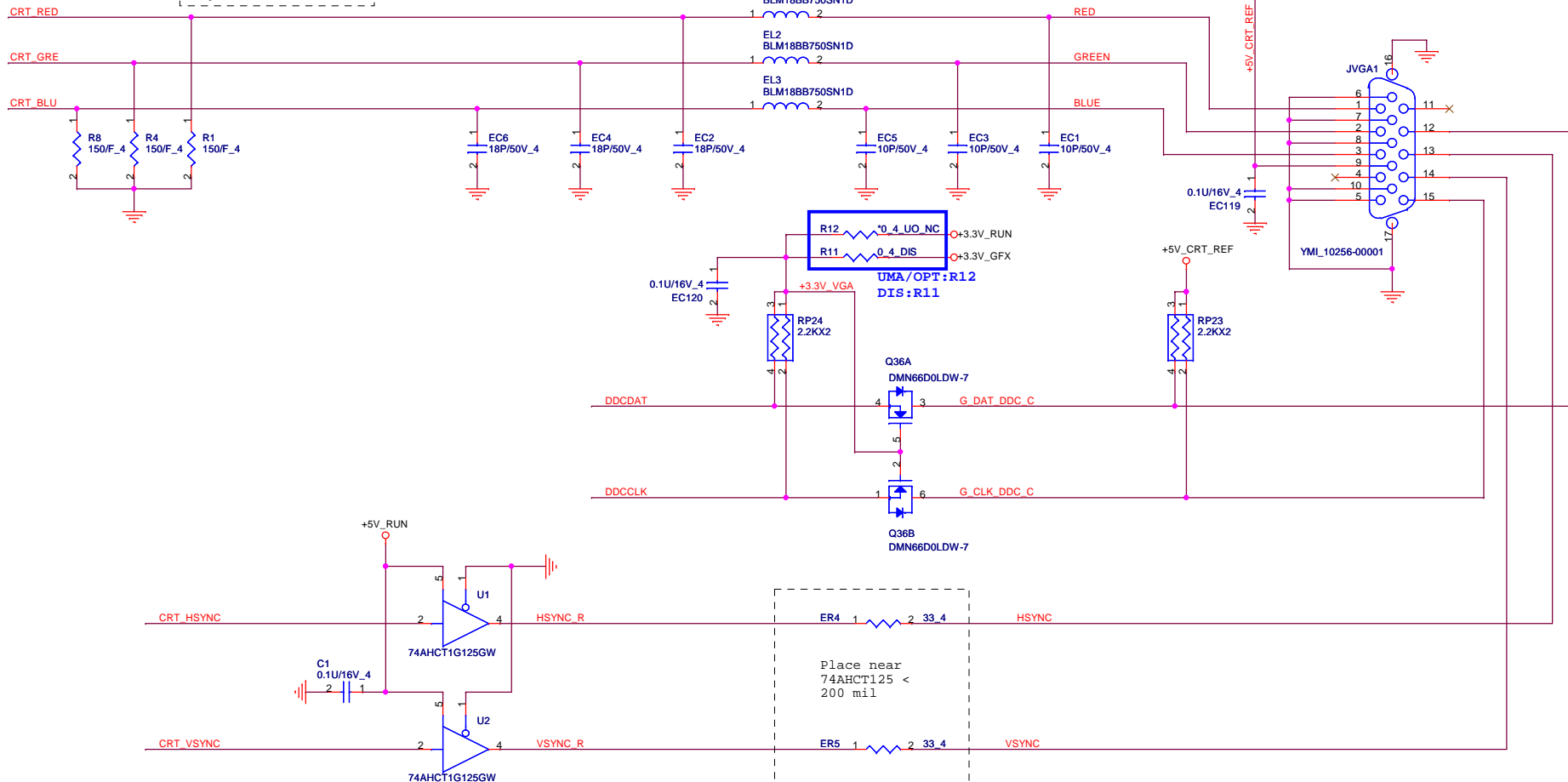


DIS: EXT POP
UMA/OPT: INT POP



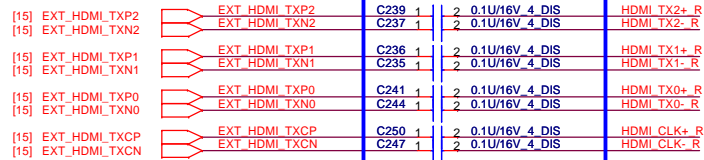
DIS: EXT POP
UMA/OPT: INT POP

Layout Note:
Setting R,G,B treac
impedance to 50 ohm.

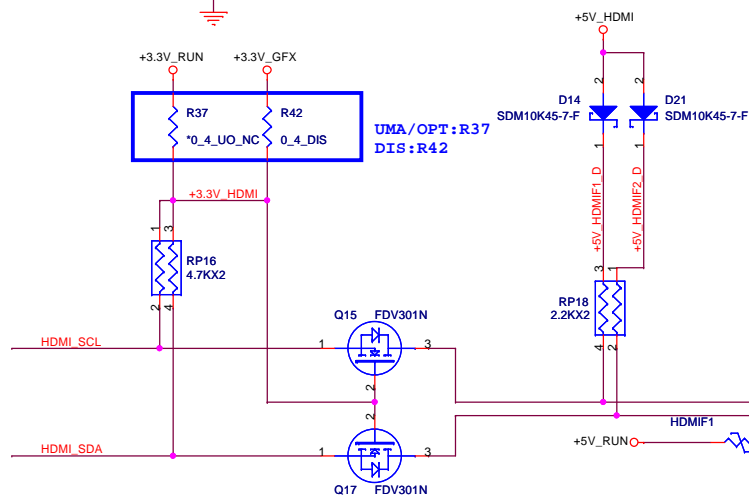
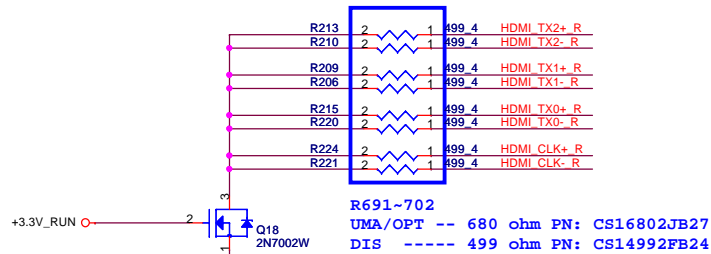
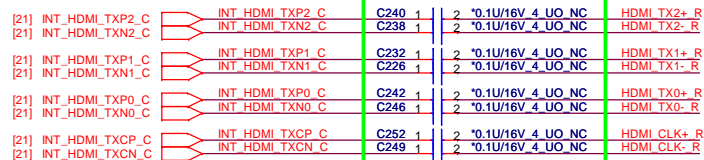


HDMI W/O Re-driver

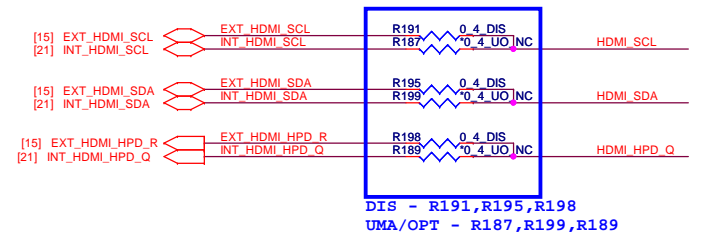
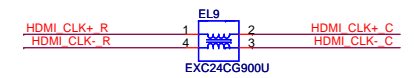
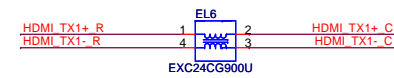
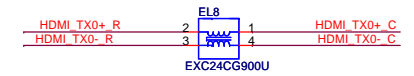
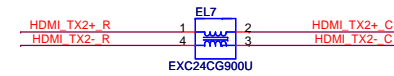
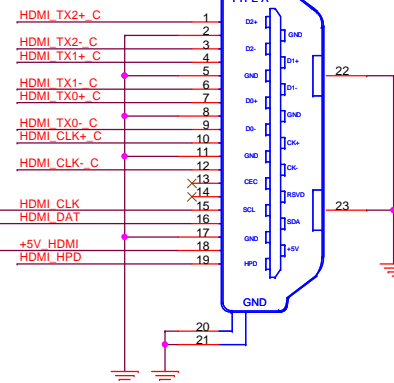
DIS HDMI



OTP/UMA HDMI

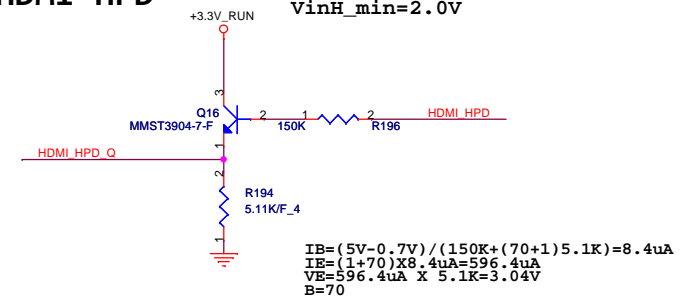


HDMI Conn.



HDMI HPD

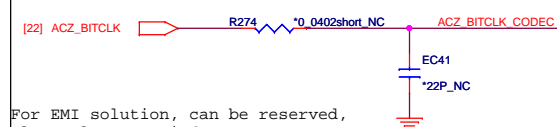
HDMI_HPD spec
VinH_min=2.0V



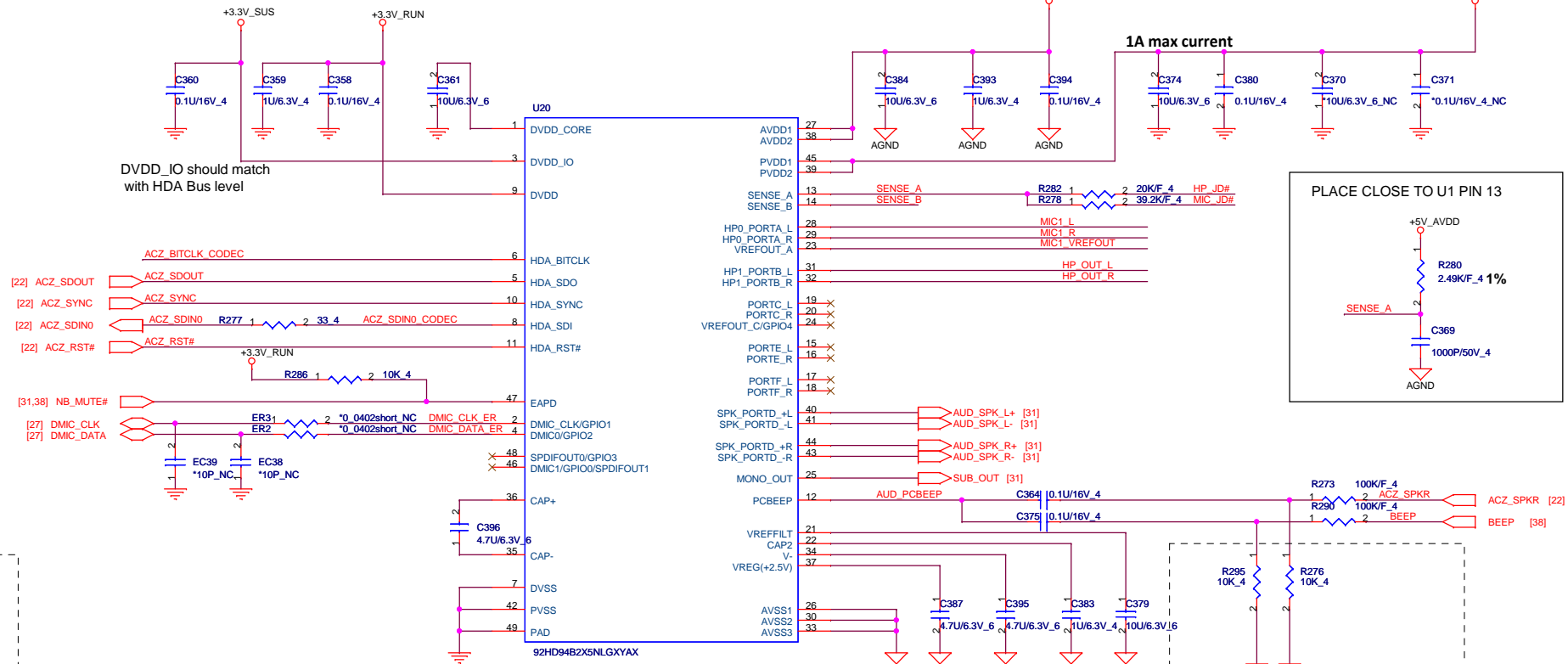
Quanta Computer Inc.

PROJECT : R09A

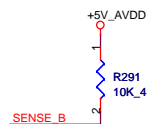
CODEC



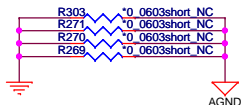
For EMI solution, can be reserved,
place close to pin6



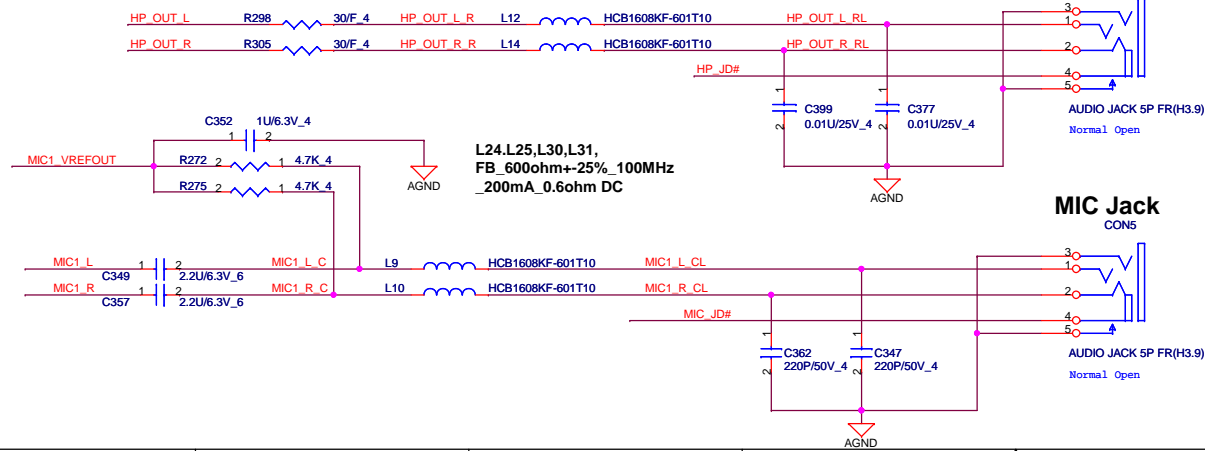
PLACE CLOSE TO U1 PIN 14



If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor



**Tied at one point only under the 92HD94 or near it.
QT change to short pad**



HP Jack

Place C14~C17 close to Codec

Recommend to divide the amplitude of BEEP signal before input to PCBEEP pin. R20,R21 are optional.

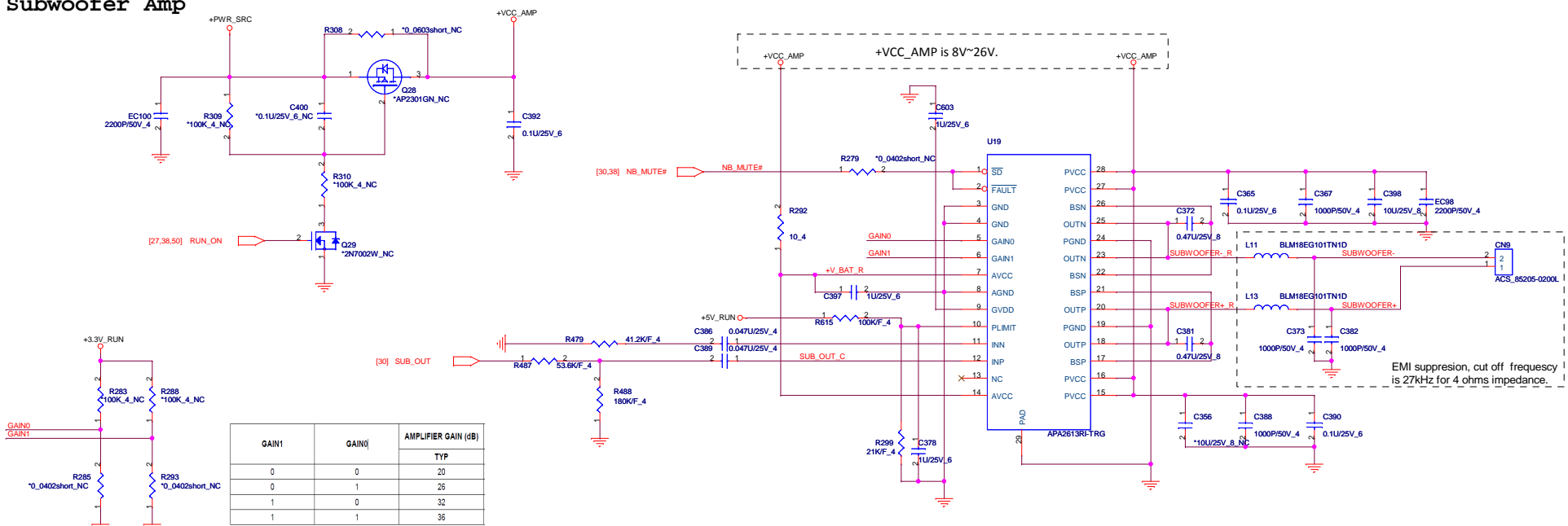
MIC Jack

**Quanta Computer Inc.**

PROJECT : R09A

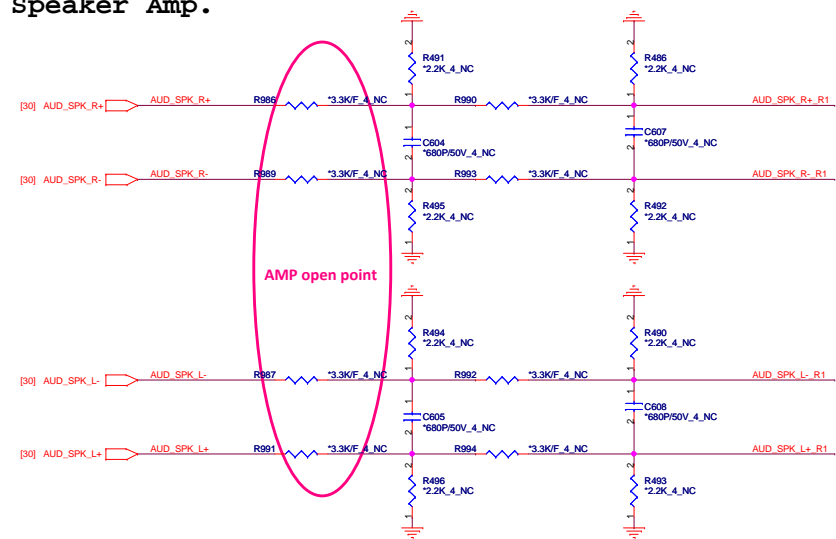
Size	Document Number CODEC	Rev 3A
Date:	Friday, March 02, 2012	Sheet 30 of 58

Subwoofer Amp

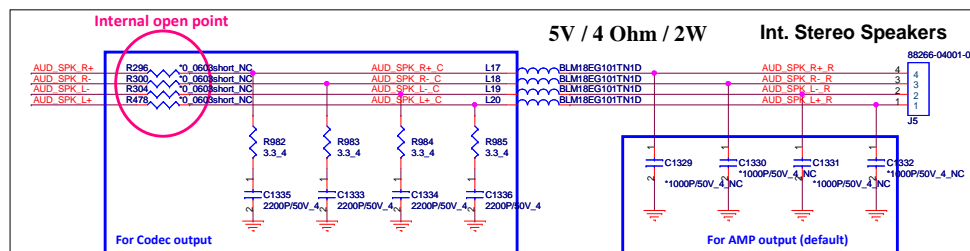
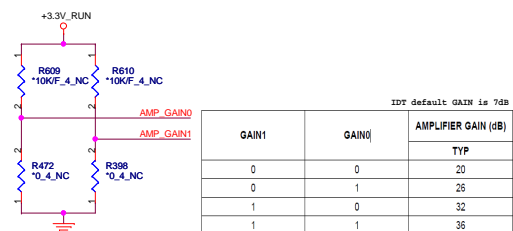
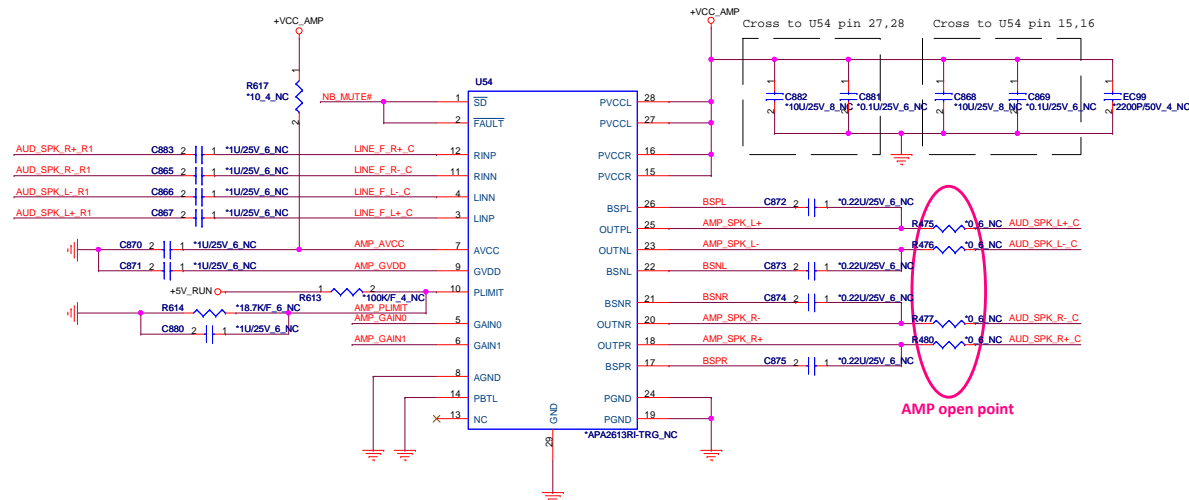


Speaker Amp.

R491,R495,R494,R496 default NC

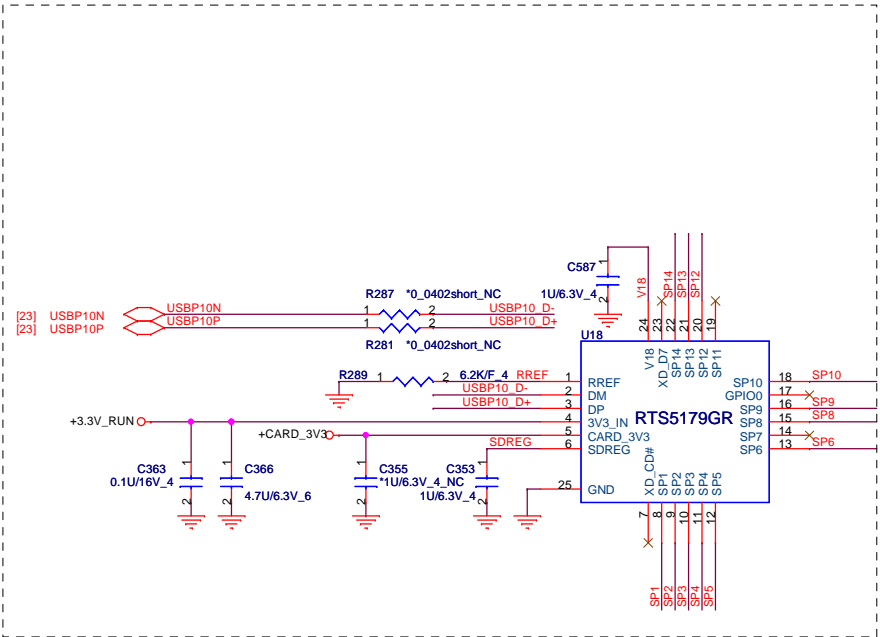
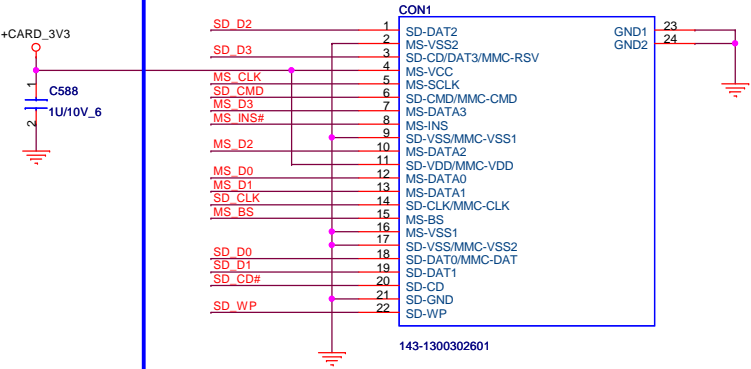


APA2613 is P2P to TI TPA3113

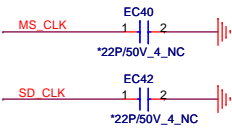
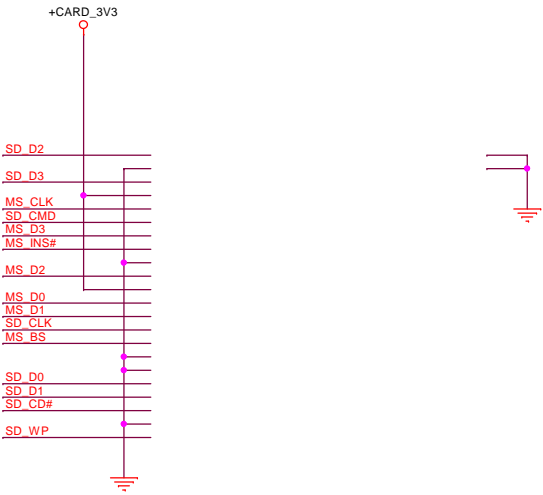


Cardreader (RTS5179GR) Support SD3.0 USH50

For INSPIRON Placement (R09,R09A,R09T)



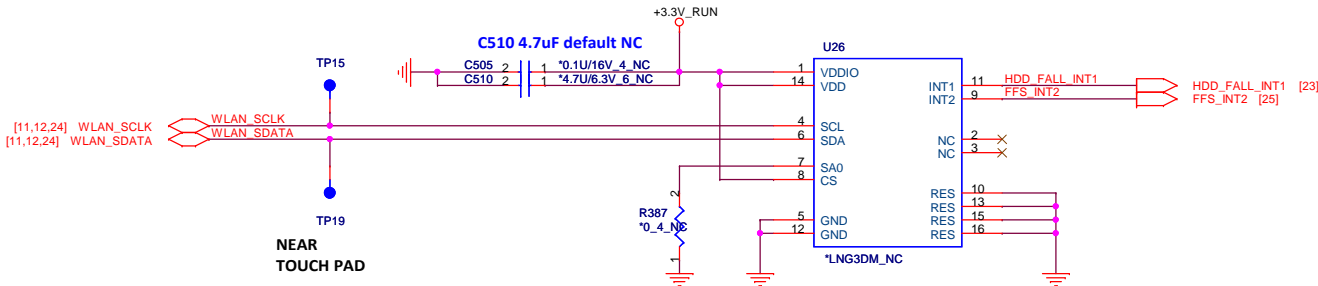
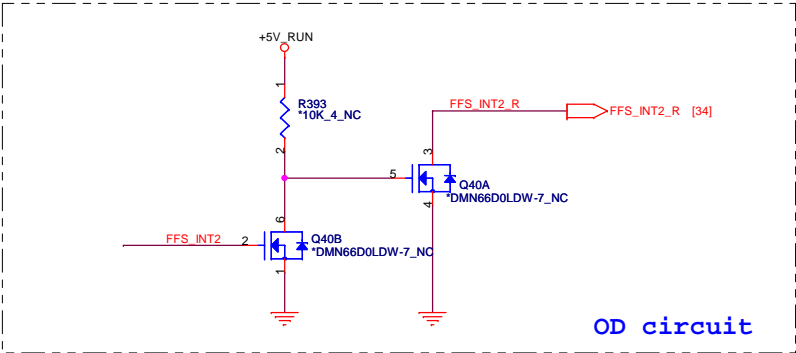
NA



SP1	SD_WP	MS_CLK
SP2	SD_D1	MS_INS#
SP3	SD_D0	MS_D7
SP4	SD_D7	MS_D3
SP5	SD_CD#	MS_D0
SP6	SD_CLK	MS_D2
SP8	SD_D5	MS_D0
SP9	SD_CMD	MS_D1
SP10	SD_D3	MS_D5
SP12	SD_D2	MS_BS
SP13		
SP14		

Share Pin

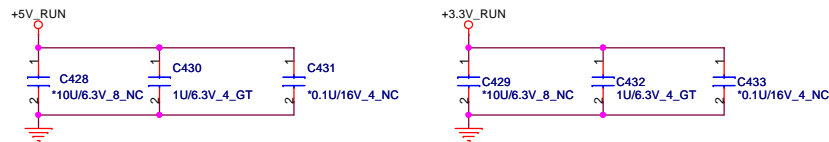
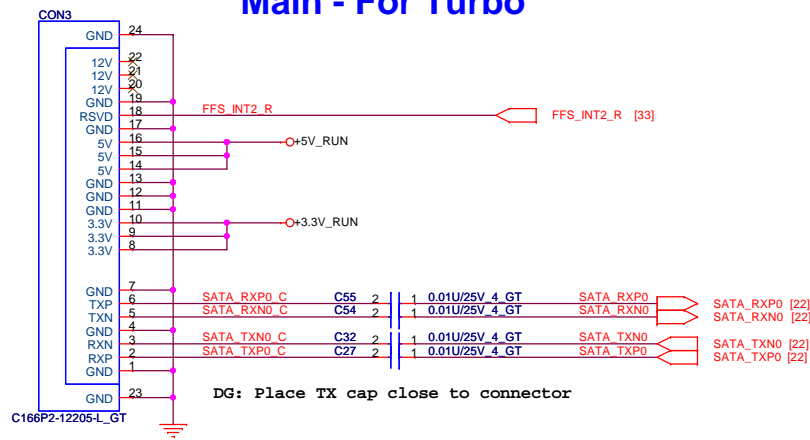
3-axis Fall Sensor - NC



SA0 is low: I2C device address is 00110000 (30h)
SA0 is high: I2C device address is 00110010 (32h)

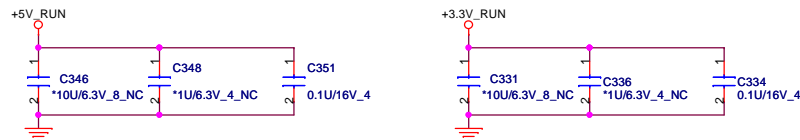
HDDX2

Main - For Turbo

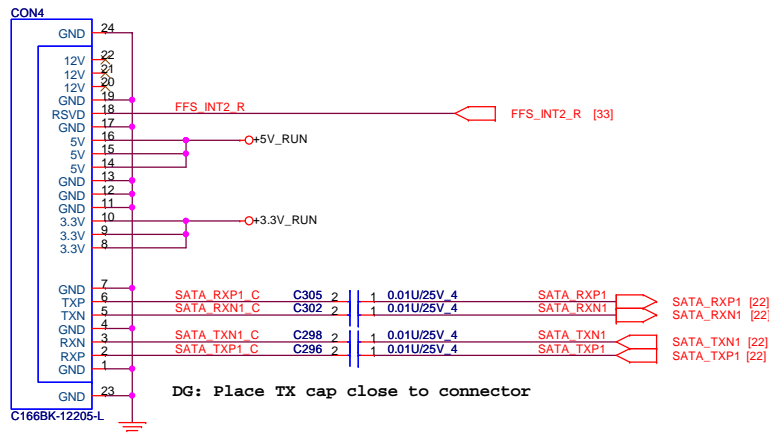


Default C351, C430 POP

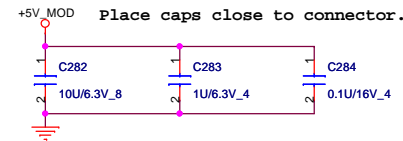
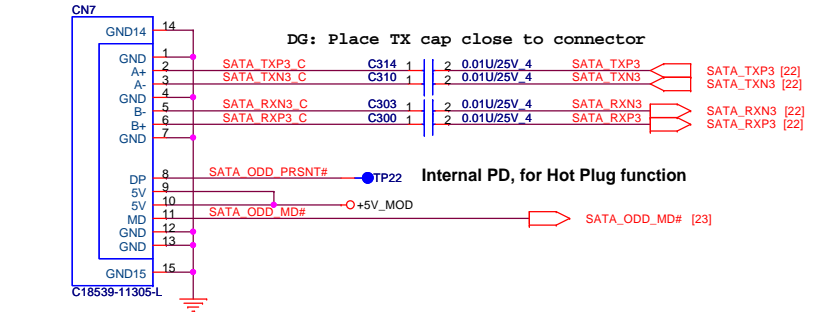
Default C334, C432 POP



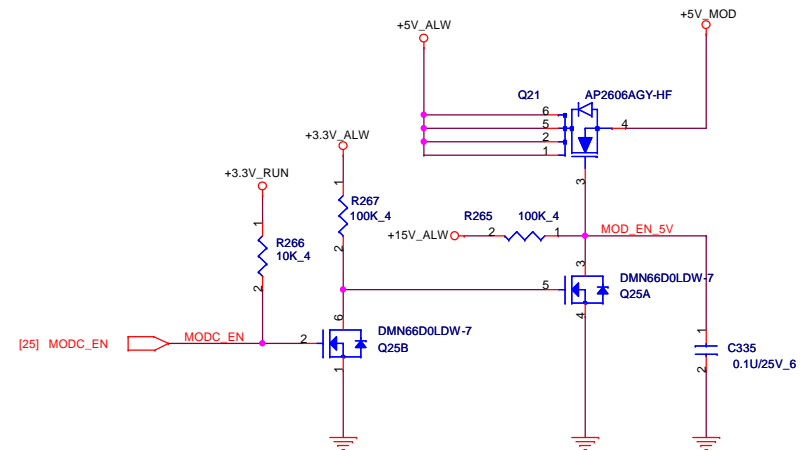
Second - For Inspiron



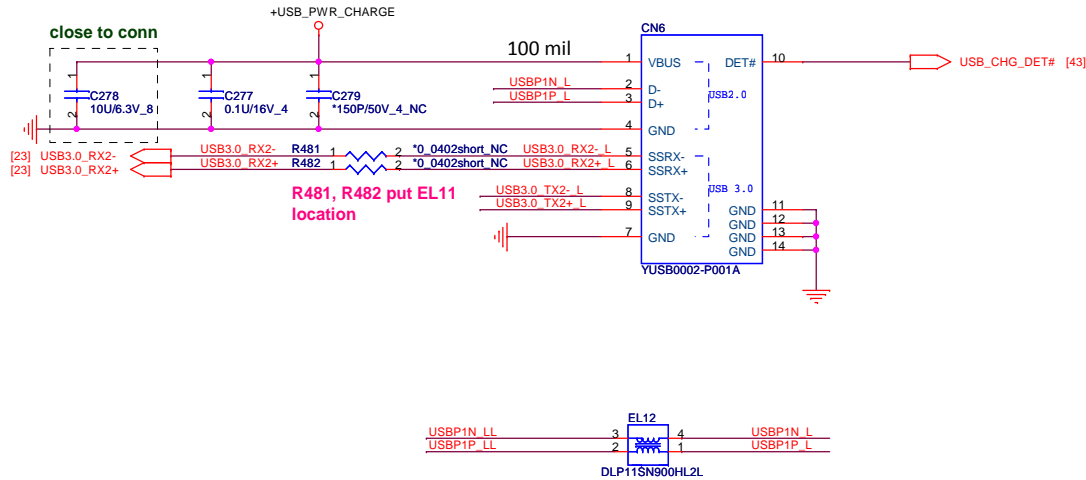
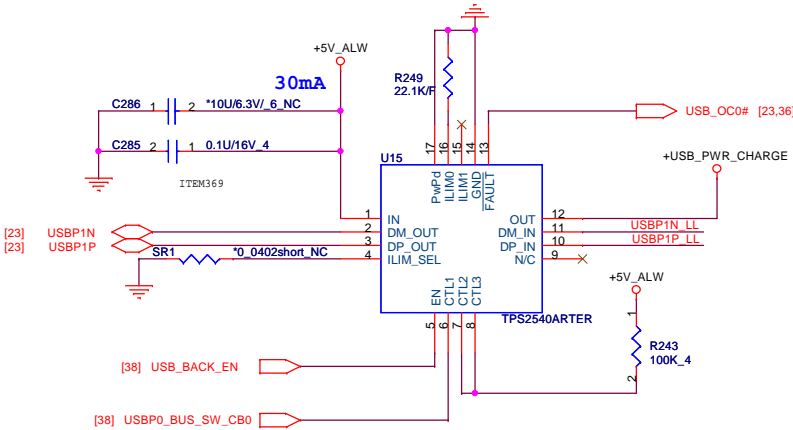
ODD



Support Zero power ODD



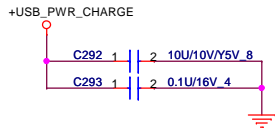
USB3.0x1 with Power share



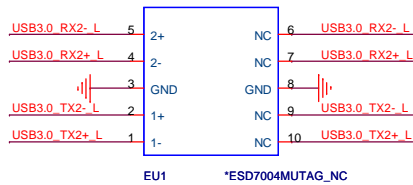
	R249	mA
OC limitation	100k ohm	480
	22.1k ohm	2171

Applied Now

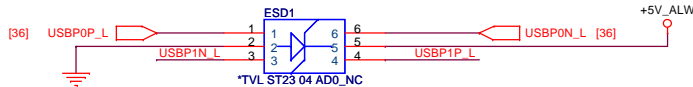
USBP0_BUS_SW_CB0	Mode	Operating at
Low	DCP, Auto-detect	S3/S4/S5, 1.5 A
High	CDP, BC Spec 1.1	S0, 1.5 A



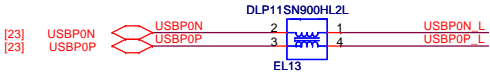
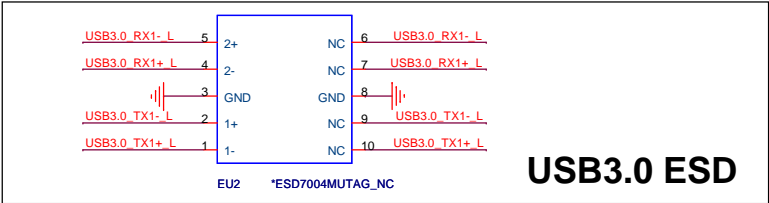
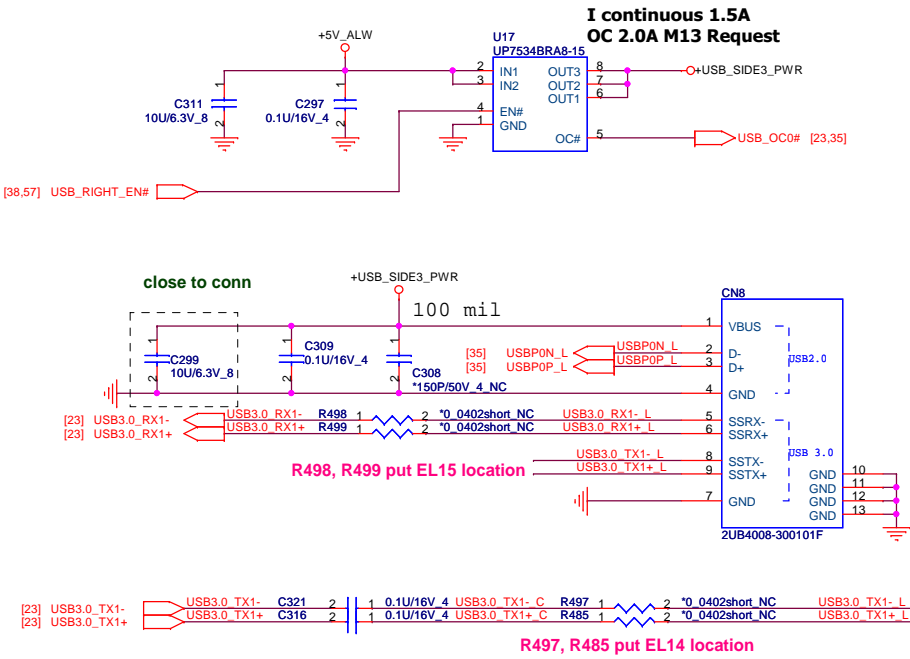
USB 3.0 ESD



USB 2.0 ESD



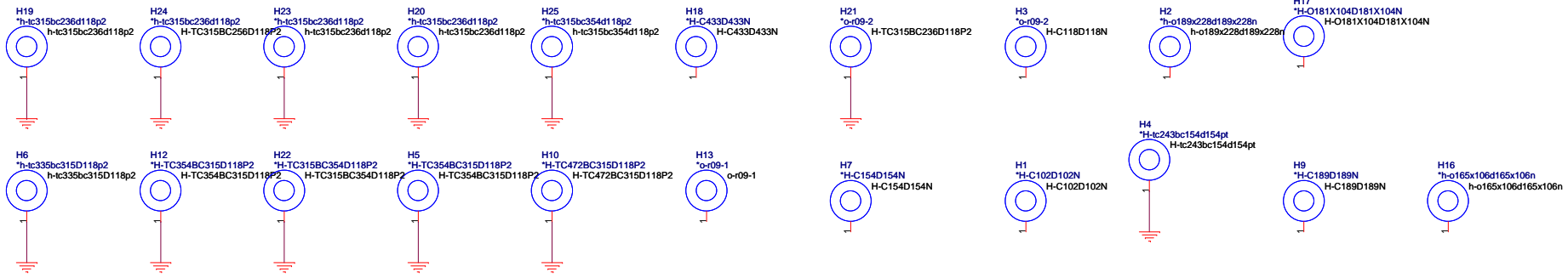
USB3.0x1

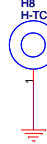


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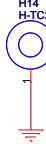
PROJECT : R09A

USB 3.0 port

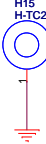




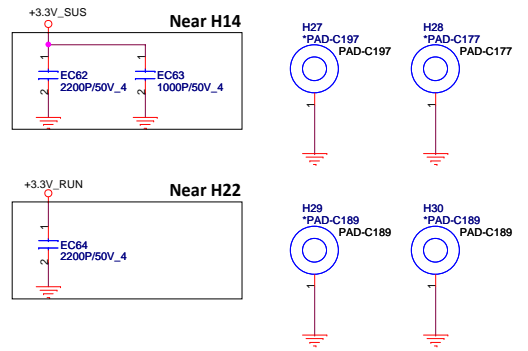
CPU NUT
MBIM3001010



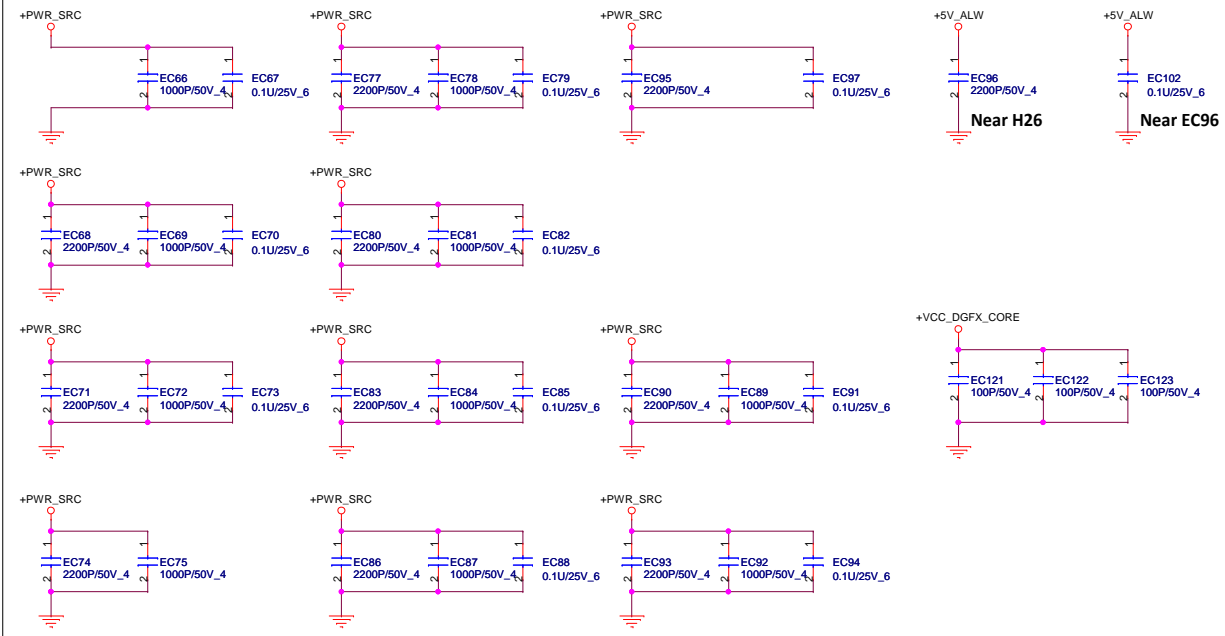
mSATA NUT
MBIM3001010



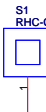
WLAN NUT
FBFM8001010




Near
C423/ESD2/H8/PR204/PR235/pq20/PL5/PC121/H10/R334/PL7/EC45



Spring



S1
RHC-CP-55B01
SPAD-RE167X98



S2
RHC-CP-25L03
SPAD-RE110X79

L5.6*W2.5*H5.5

L3.5*W2.0*H2.5

AOI label

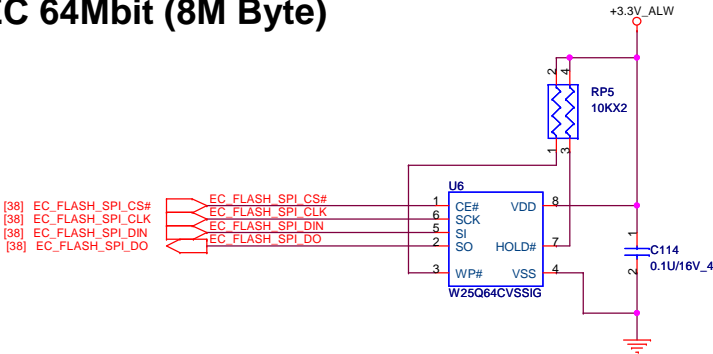
AOI LABEL on 31 header

PPID label

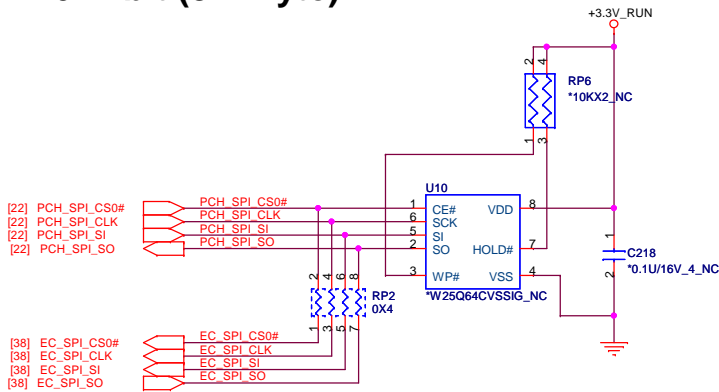
PPID LABEL on 31 header

FLASH / RTC

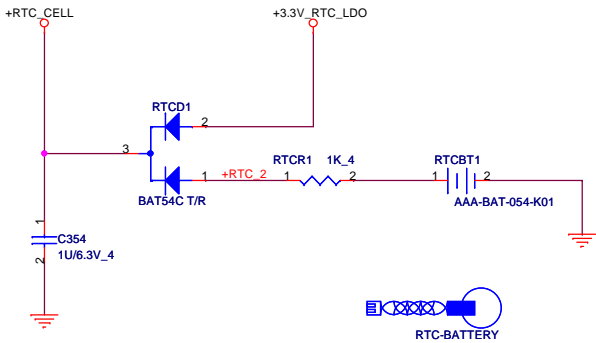
For EC 64Mbit (8M Byte)



For PCH 64Mbit (8M Byte)

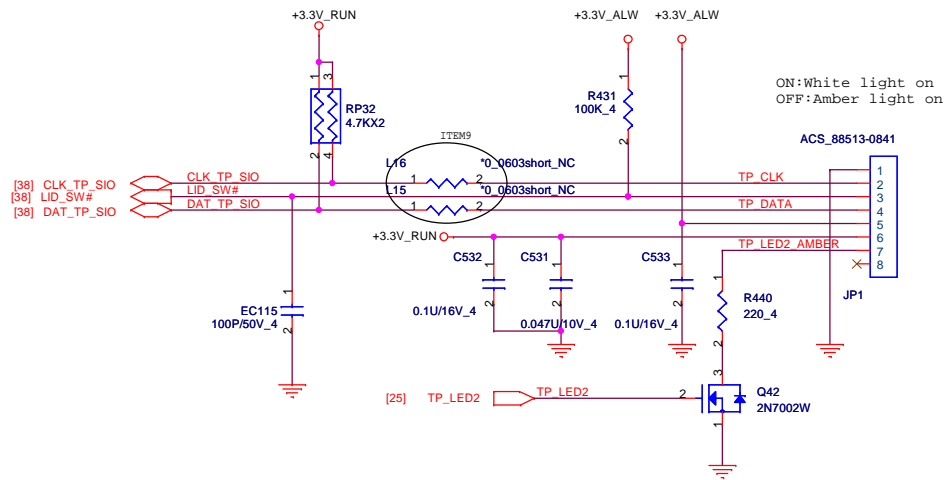


RTC

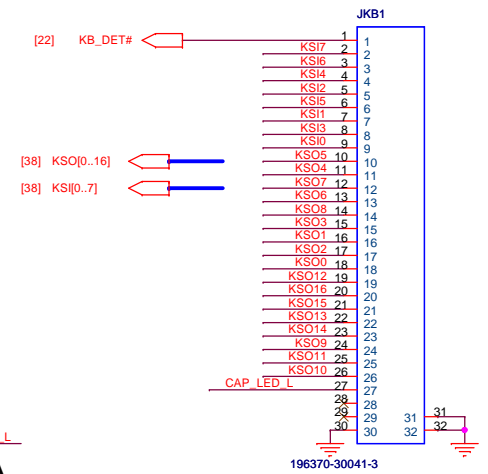
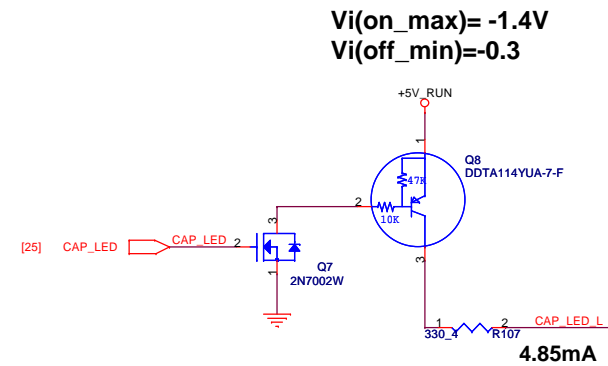


Double, 25°C, Vf=0.4V, If=25mA
one, 25°C, Vf=0.35V, If=15.8mA

Touch Pad CONNECTOR

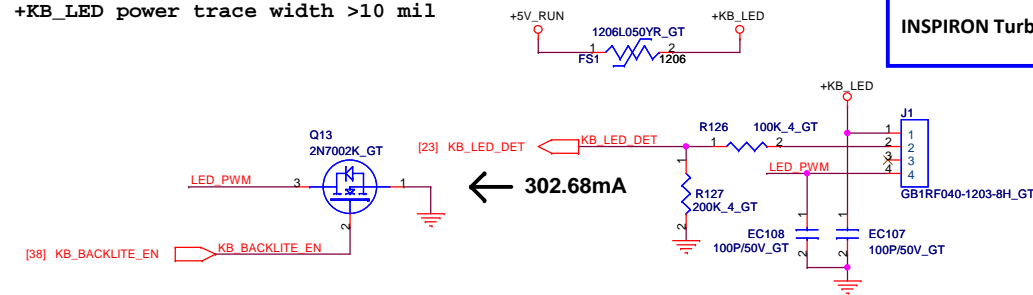


KEYBOARD CONNECTOR

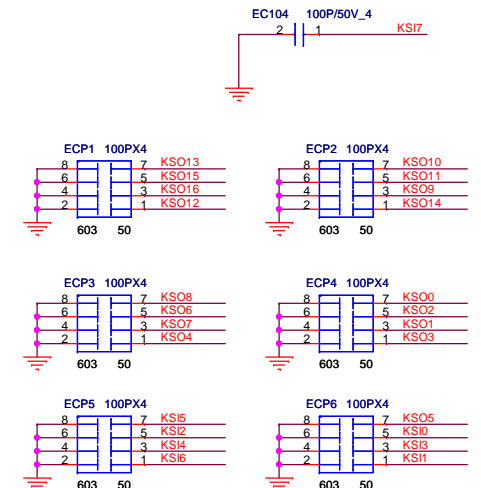


Key board illumination

+KB_LED power trace width >10 mil



INSPIRON	NC
INSPIRON Turbo	POP



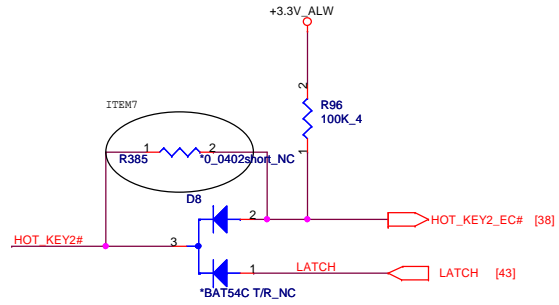
Layout Note: 100P CAPS CLOSE TO JKB1



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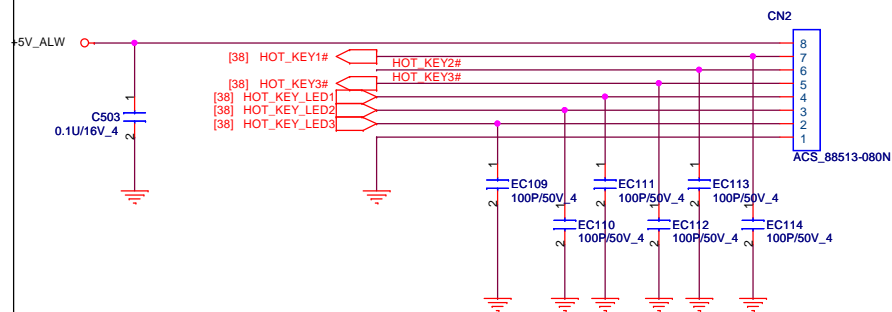
Size	Document Number	Rev
	TP / KB	3A
Date:	Saturday, March 03, 2012	Sheet 40 of 58

HOT_KEY2 support Pre-Boot Recovery



INSPIRON: R385 pop, D8 NC

Hot key BOARD



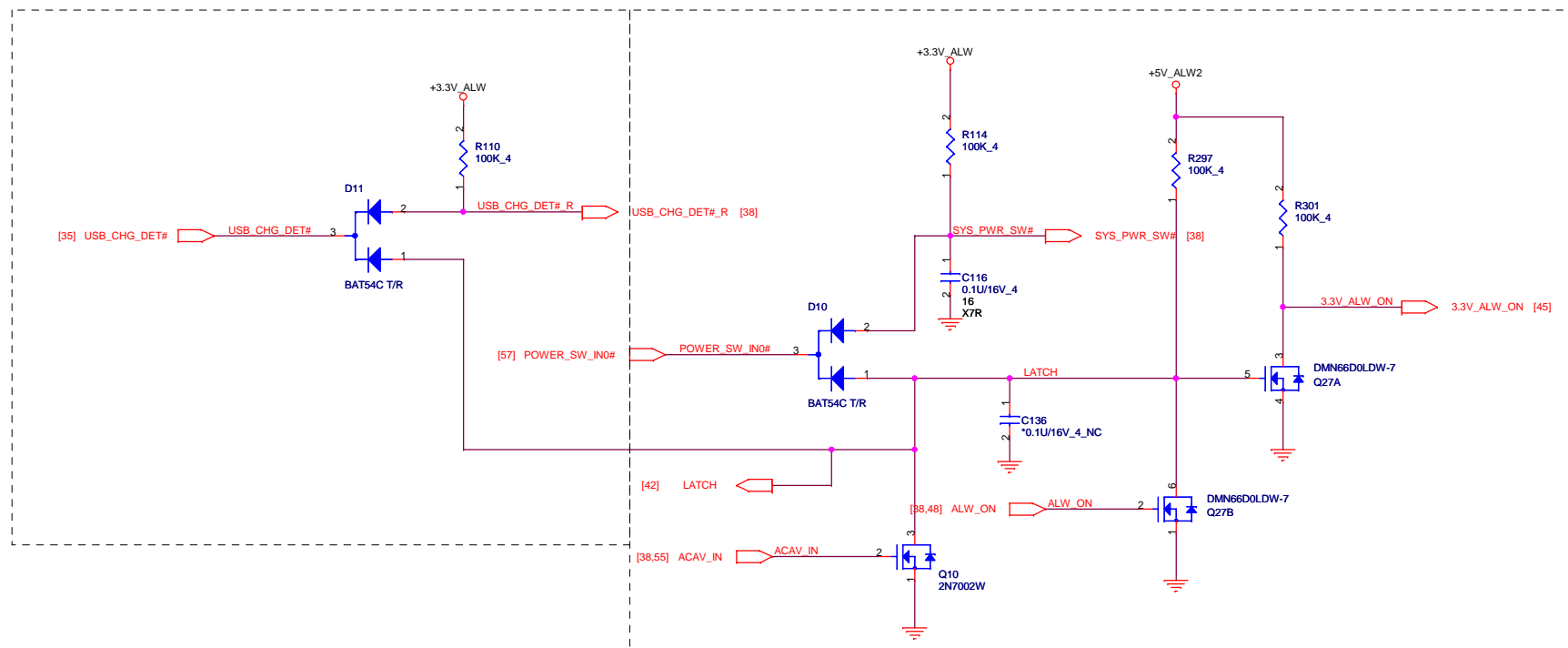
Quanta Computer Inc.

PROJECT : R09A

Size	Document Number	Rev
		3A
Date:	Wednesday, February 08, 2012	Sheet 42 of 58

HOT KEY

3V ALW ON POWER LOGIC

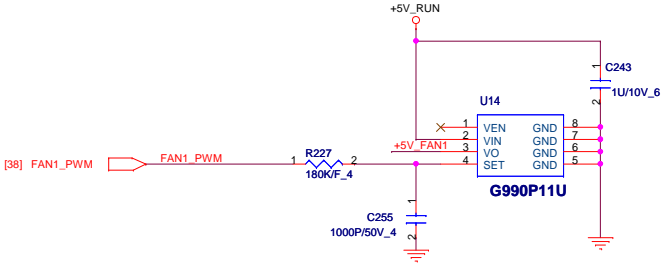
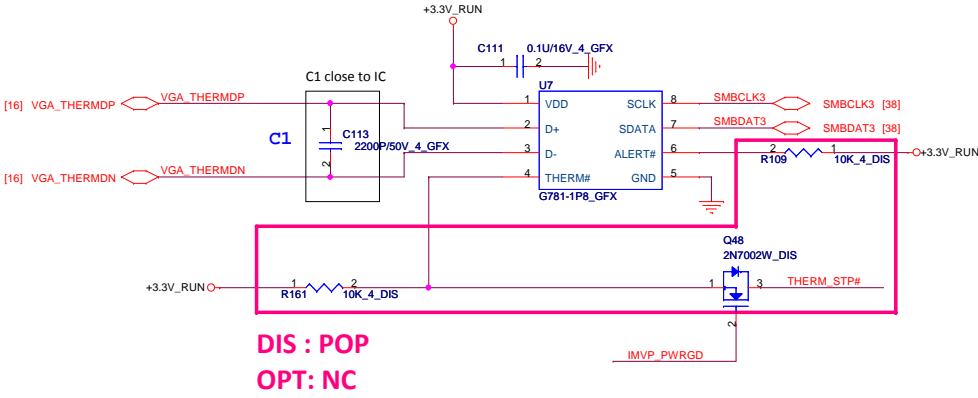


THERMAL IC

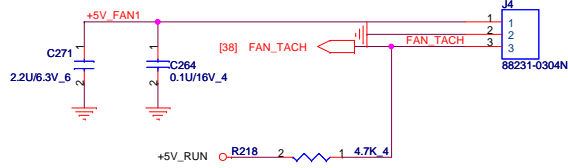
For GPU use

G781-1P8
 SMBus address is 1001101xb (9Ah) (x is R/W bit).

DIS/OPT:POP
 UMA:NC

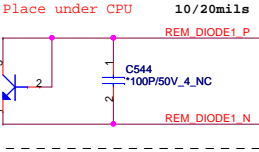


FAN CONN



For CPU use

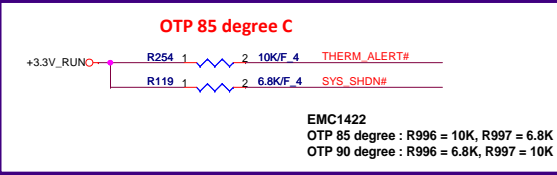
Closed to CPU



Low cost
 EMC1422 pin to pin NCT7718W
 NCT7718W
 Quanta PN: AL007718000

- 1.Place C1340 close to NCT7718W
- 2.Place C1339 close to Q81
- Total capacitance between D+/D- is 2200pF(max)
- if use 2200pF for C1340, then C1339 should be dummy

[20,38,53] IMVP_PWRGD

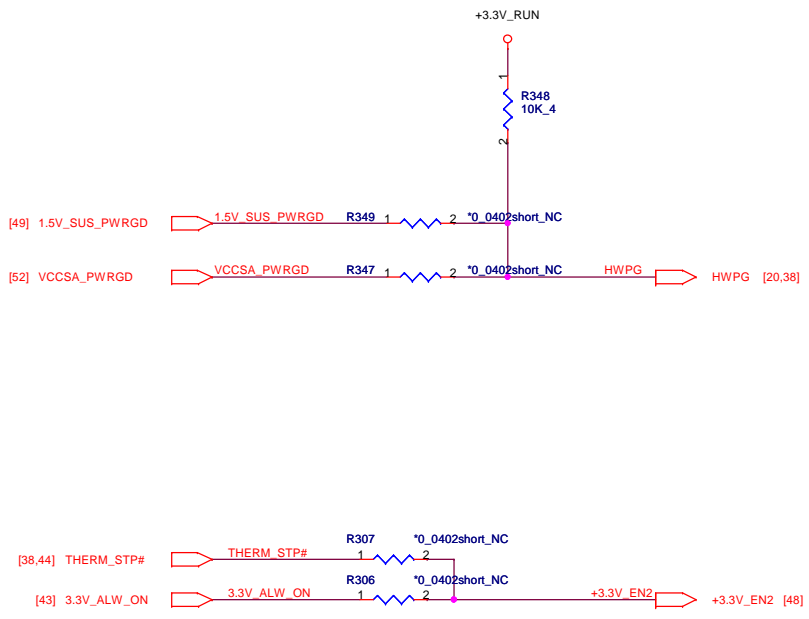


NCT7718W SMBus address is 1001100xb (98h) (x is R/W bit).

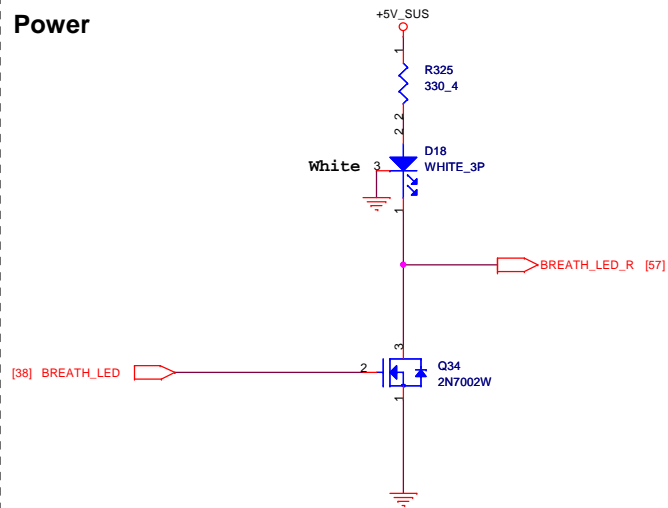
SYS_SHD#	2K	7.5K	10.5K	14K	18.7K
ALERT#	77'C	87'C	97'C	107'C	117'C
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C

EMC1422 SMBus address is 1001_100xb (98h) (x is R/W bit).

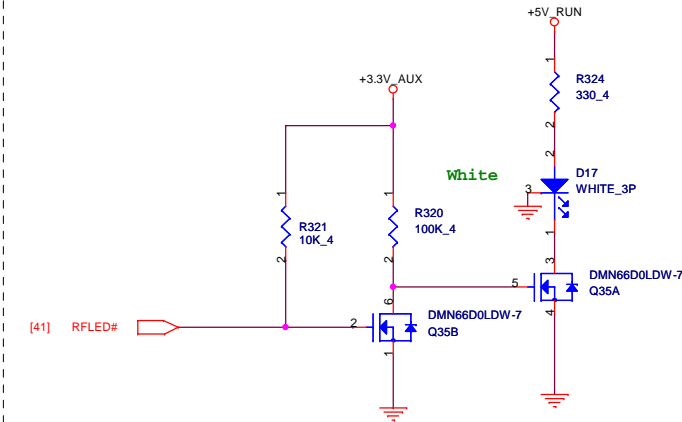
SYS_SHD#	4.7K	6.8K	10K	15K	22K	33K
ALERT#	77'C	83'C	89'C	95'C	101'C	107'C
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C



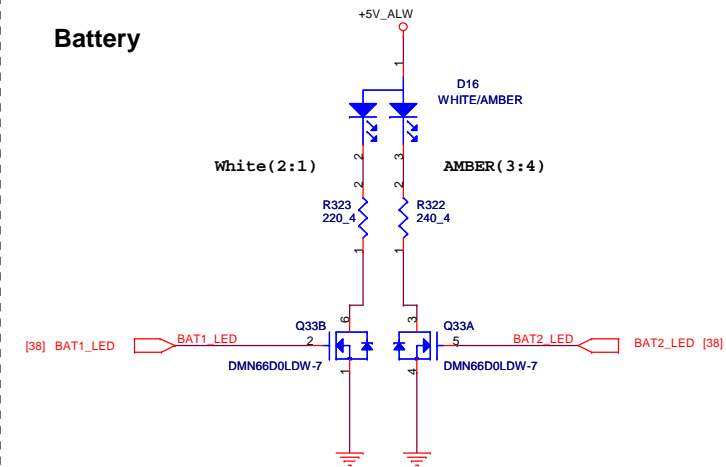
Power



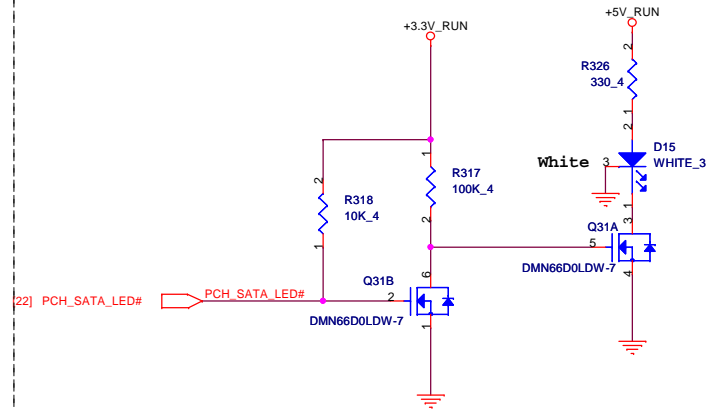
Bluetooth / WLAN on/off LED

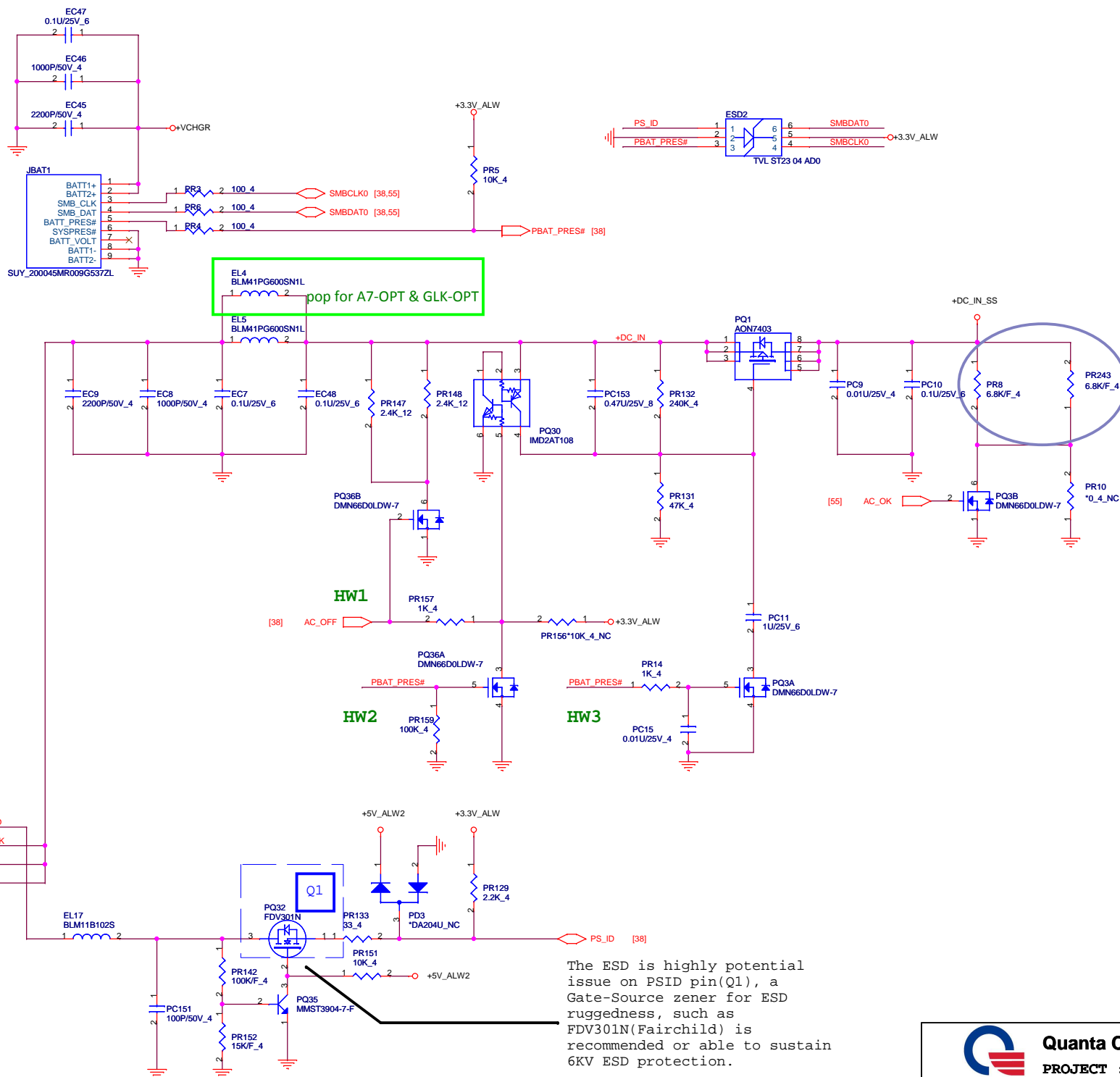


Battery

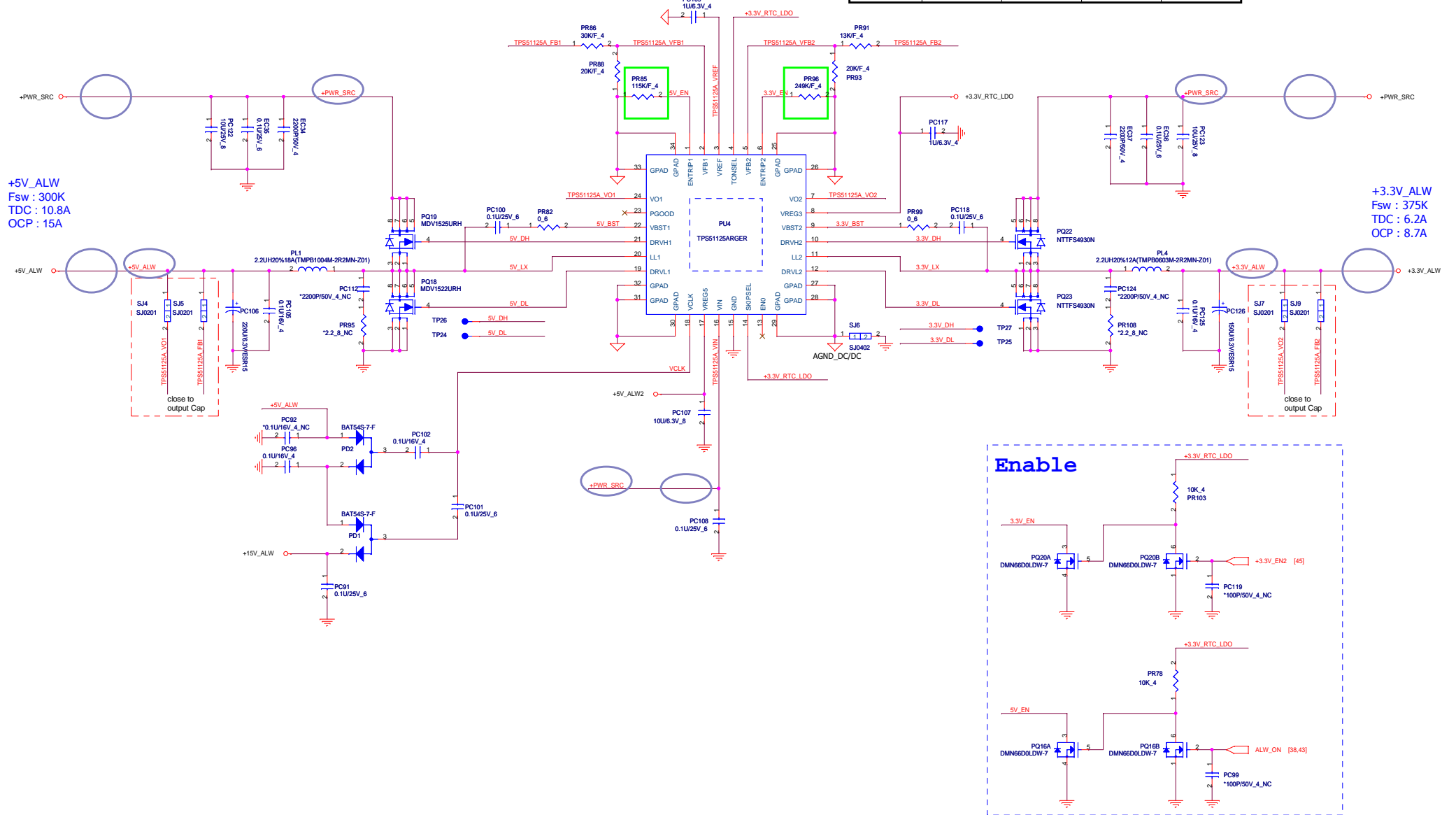


HDD activity LED.

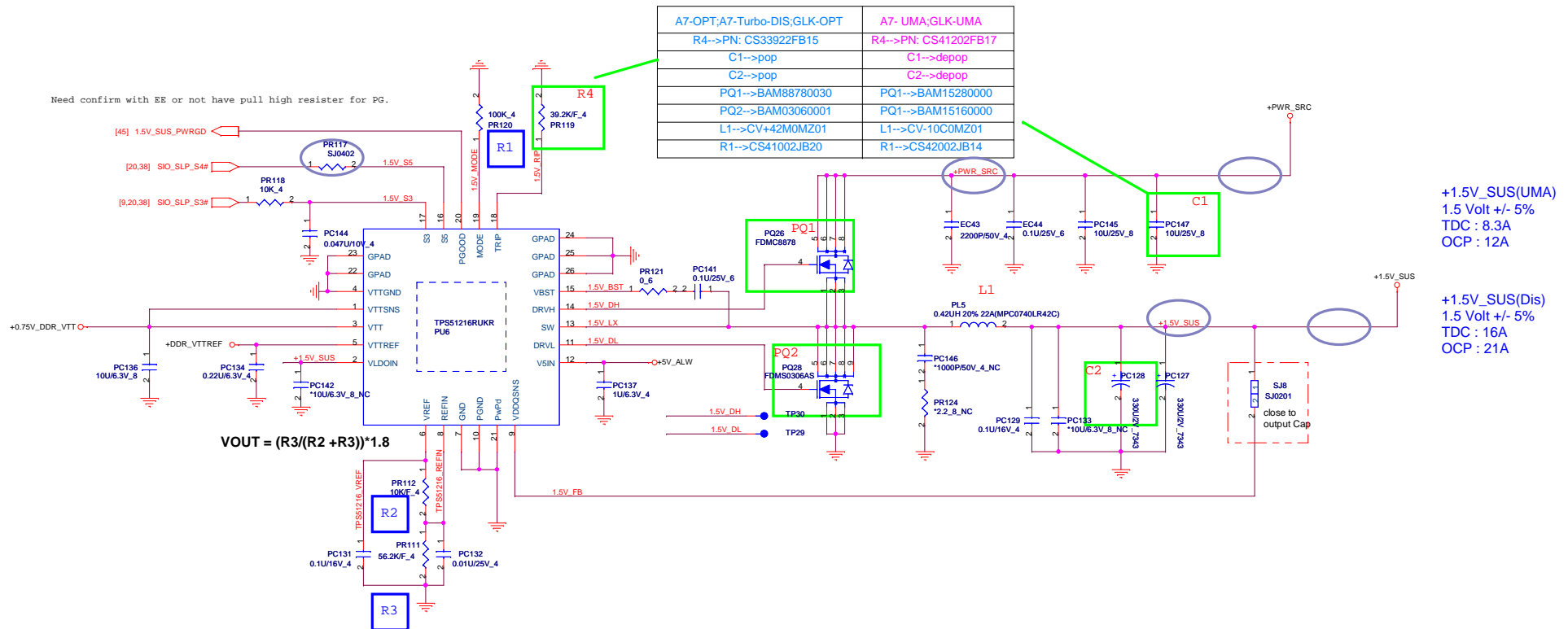




TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz



Need confirm with EE or not have pull high resistor for PG.



+1.5V_SUS(UMA)
1.5 Volt +/- 5%
TDC : 8.3A
OCP : 12A

+1.5V_SUS(Dis)
1.5 Volt +/- 5%
TDC : 16A
OCP : 21A

MODE Selection			
	Resistance between MODE and GND	Frequency	Discharge Mode
R1	200K_4	CS42002JB14	400k Hz
R1	100K_4	CS41002JB20	300k Hz
R1	68K_4	CS36802JB12	300k Hz
R1	47K_4	CS34702JB21	400k Hz

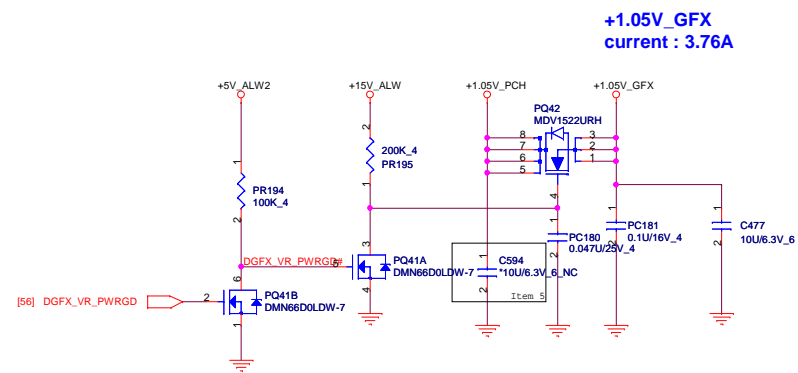
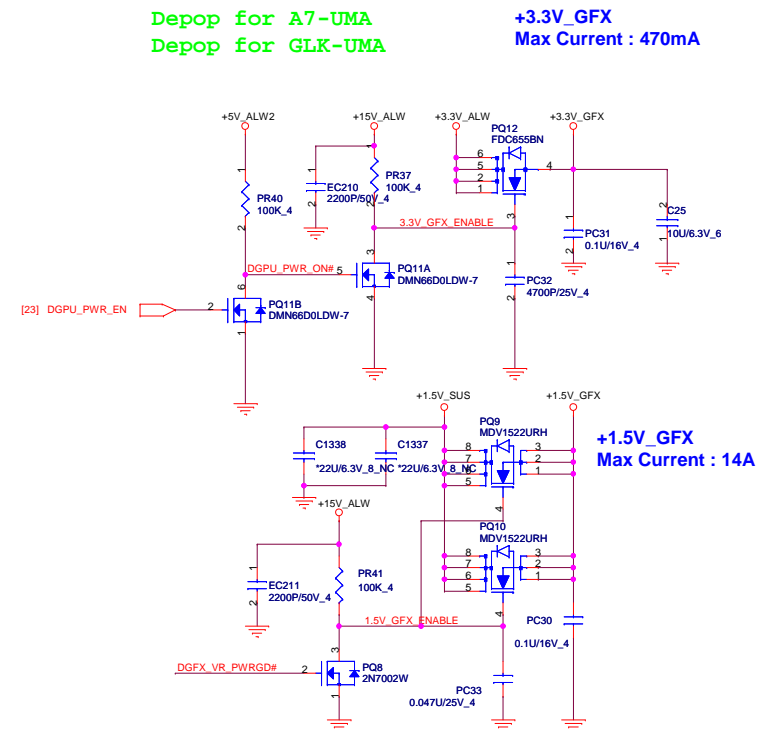
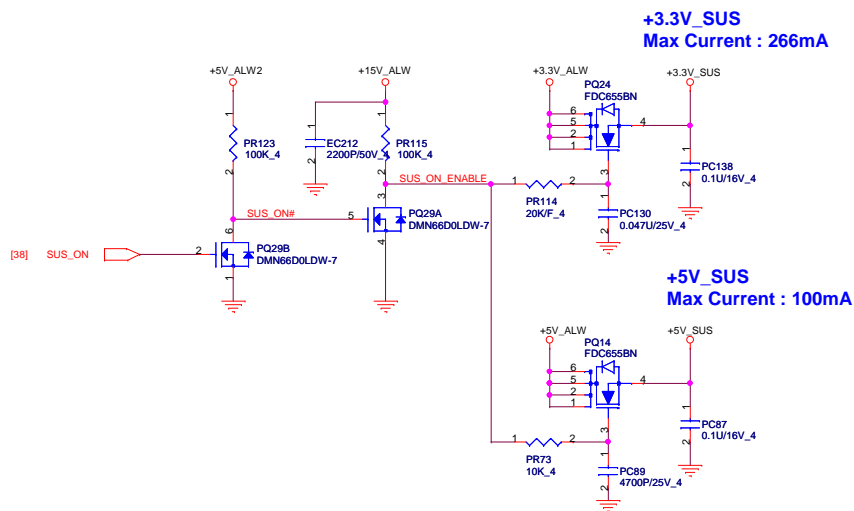
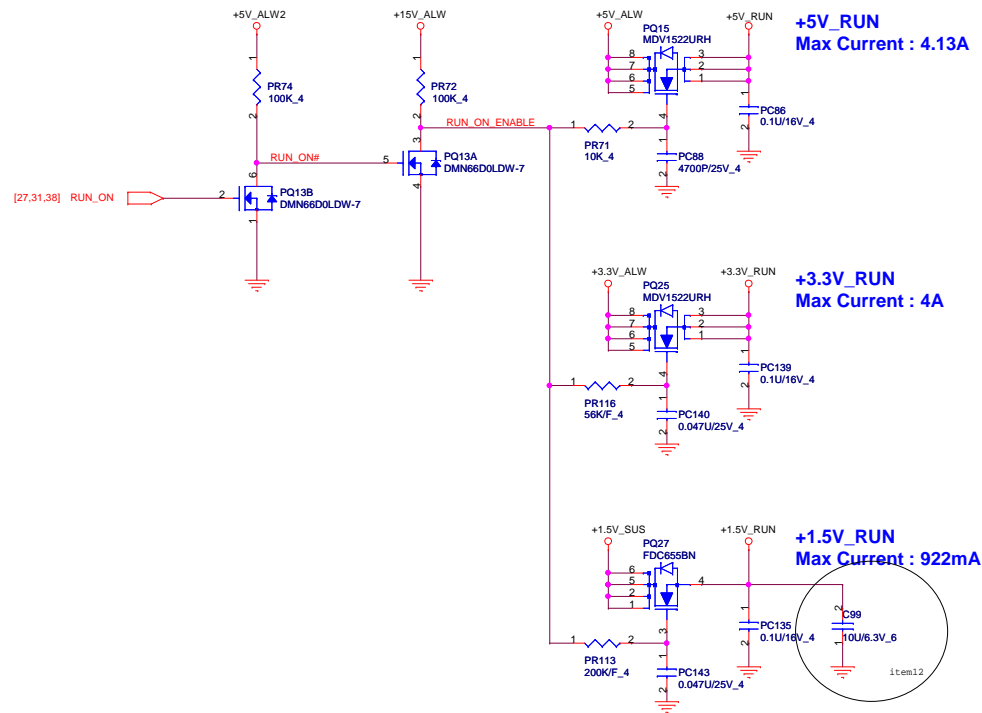
Outputs Management by S3, S5 control

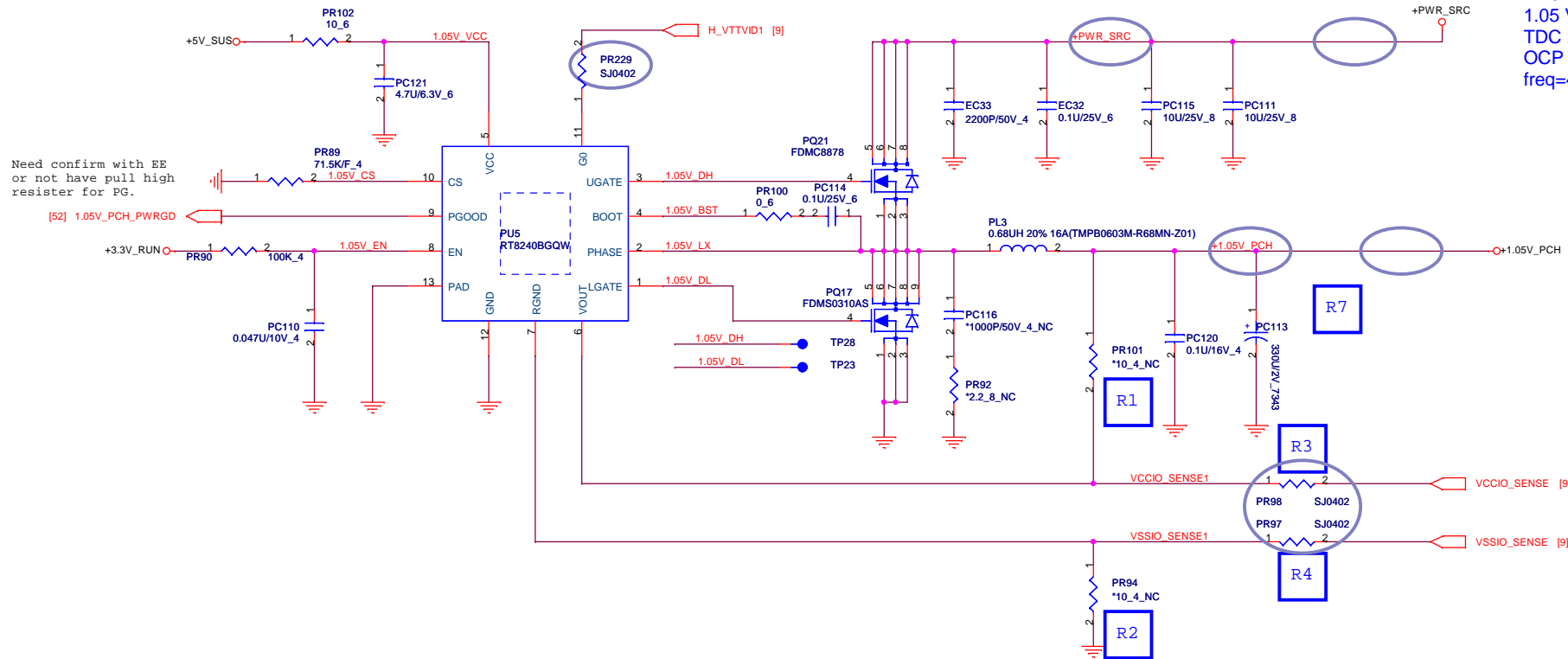
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)



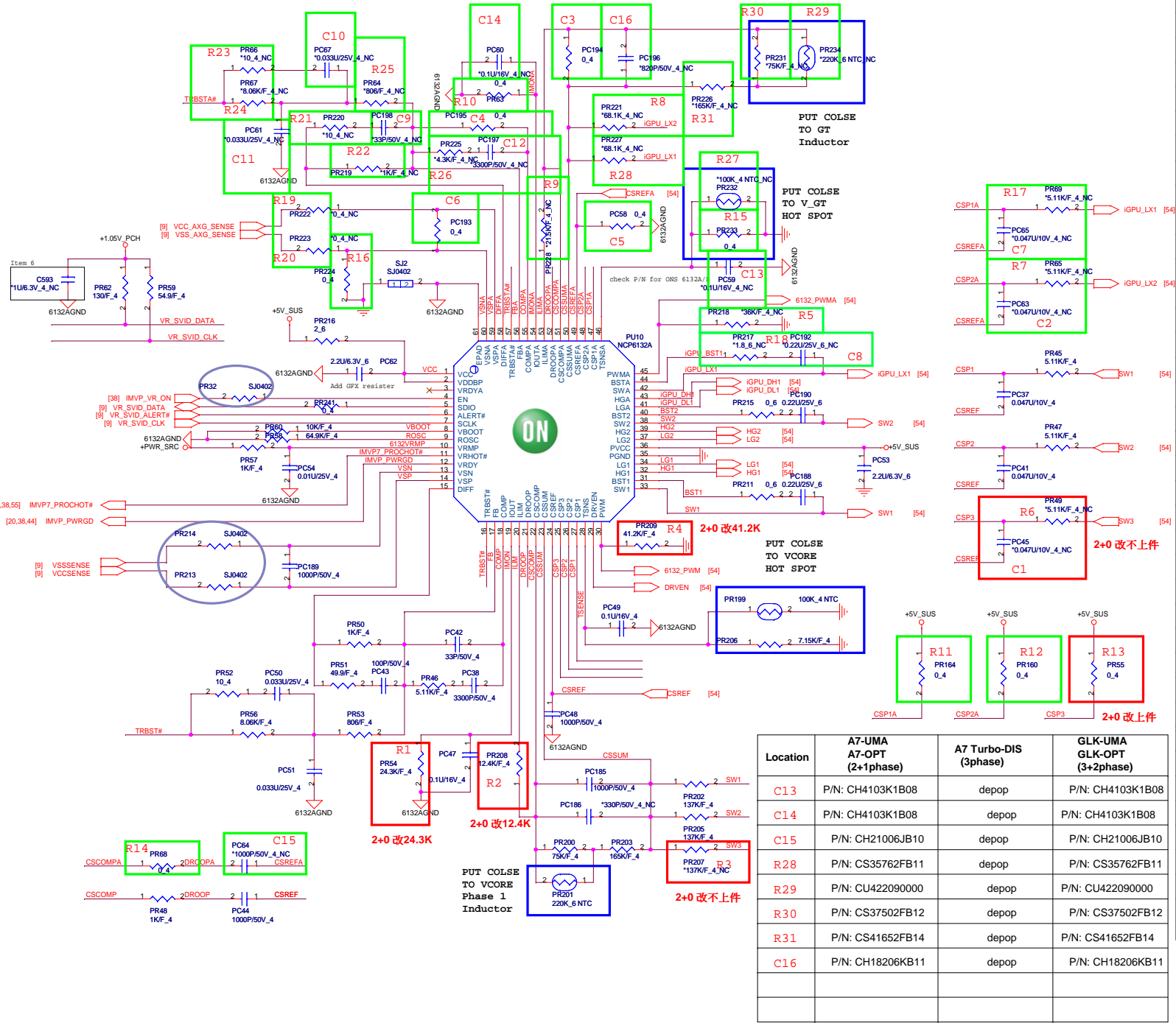
Quanta Computer Inc.
PROJECT : R09

Size: 1.5 SUS/0.75 DDR VTT (TPS51216RUKR) Rev: 1A
Date: Monday, March 05, 2012 Sheet: 49 of 57



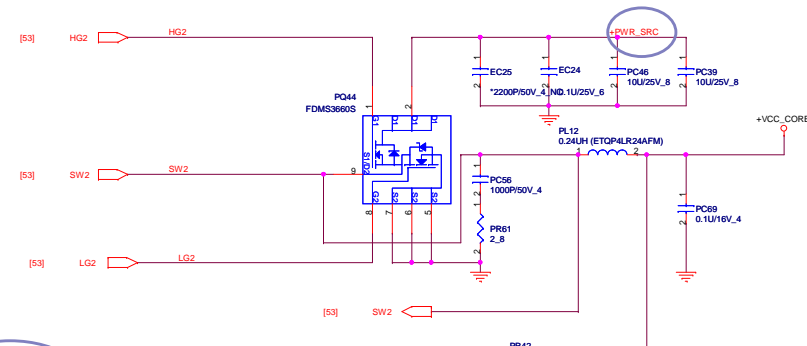
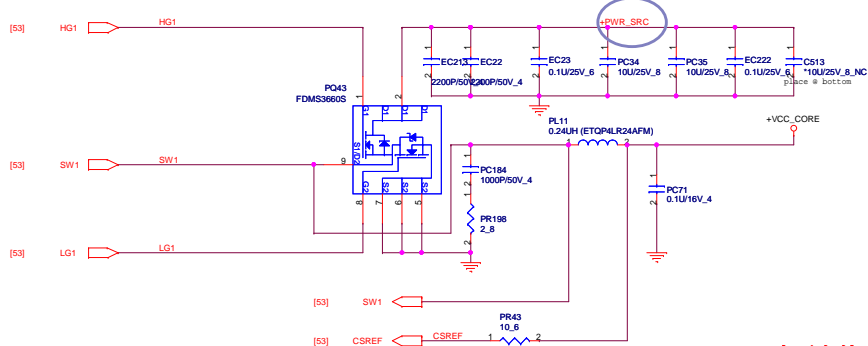


For EA test	
R1	10_4
R2	10_4
R3	NC
R4	NC
R5	NC
R6	NC
R7	NC



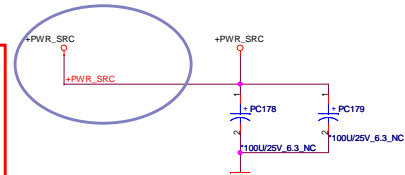
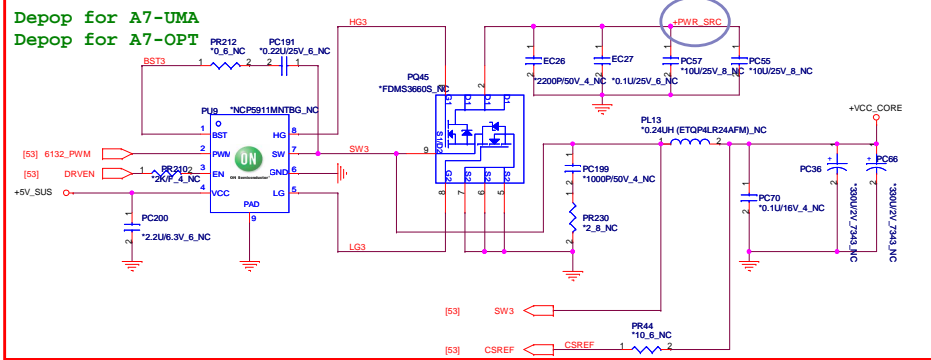
Location	A7-UMA A7-OPT (2+1phase)	A7 Turbo-DIS (3phase)	GLK-UMA GLK-OPT (3+2phase)
R1	P/N: CS32432FB01	P/N: CS32372FB05	P/N: CS32372FB05
R2	P/N: CS31242FB05	P/N: CS32102FB14	P/N: CS32102FB14
R3	depop	P/N: CS41302FB01	P/N: CS41302FB01
R4	P/N: CS34122FB19	P/N: CS37322FB14	P/N: CS37322FB14
R5	P/N: CS32552FB03	depop	P/N: CS33602FB07
R6	depop	P/N: CS25112FB15	P/N: CS25112FB15
C1	depop	P/N: CH34702KB10	P/N: CH34702KB10
R7	depop	depop	P/N: CS25112FB15
C2	depop	depop	P/N: CH34702KB10
R8	depop	depop	P/N: CS35762FB11
R9	P/N: CS31582FB12	depop	P/N: CS32152B00
R10	P/N: CS32432FB01	P/N: CS00002JB38	P/N: CS32402FB15
R11	depop	P/N: CS00002JB38	depop
R12	P/N: CS00002JB38	P/N: CS00002JB38	depop
R13	P/N: CS00002JB38	depop	depop
C3	P/N: CH21006JB10	P/N: CS00002JB38	P/N: CH21006JB10
C4	P/N: CH01006JB08	P/N: CS00002JB38	P/N: CH01006JB08
C5	P/N: CH21006JB10	P/N: CS00002JB38	P/N: CH21006JB10
R14	P/N: CS15102FB19	P/N: CS00002JB38	P/N: CS15102FB19
C6	P/N: CH21006JB10	P/N: CS00002JB38	P/N: CH21006JB10
R15	P/N: CS28252FB15	P/N: CS00002JB38	P/N: CS28252FB15
R16	depop	P/N: CS00002JB38	depop
R17	P/N: CS25112FB15	depop	P/N: CS25112FB15
C7	P/N: CH34702KB10	depop	P/N: CH34702KB10
R18	P/N: CS00003J951	depop	P/N: CS00003J951
C8	P/N: CH4224K9904	depop	P/N: CH4224K9904
R19	P/N: CS00002JB38	depop	P/N: CS00002JB38
R20	P/N: CS00002JB38	depop	P/N: CS00002JB38
R21	P/N: CS01002JB22	depop	P/N: CS01002JB22
R22	P/N: CS21002FB24	depop	P/N: CS21002FB24
C9	P/N: CH03306JB04	depop	P/N: CH03306JB04
R23	P/N: CS01002JB22	depop	P/N: CS01002JB22
R24	P/N: CS22002FB19	depop	P/N: CS22002FB19
C10	P/N: CH16806KB17	depop	P/N: CH16806KB17
C11	P/N: CH24704KB19	depop	P/N: CH24704KB19
R25	P/N: CS31072FB10	depop	P/N: CS31072FB10
R26	P/N: CS24302FB07	depop	P/N: CS24302FB07
C12	P/N: CH23306JB16	depop	P/N: CH23306JB16
R27	P/N: CU4100B0000	depop	P/N: CU4100B0000

CPU Power

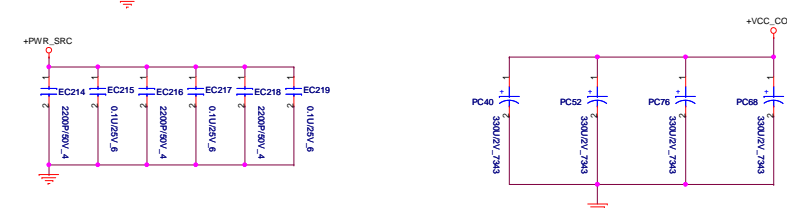


2+0 改不上件

Depop for A7-UMA
Depop for A7-OPT

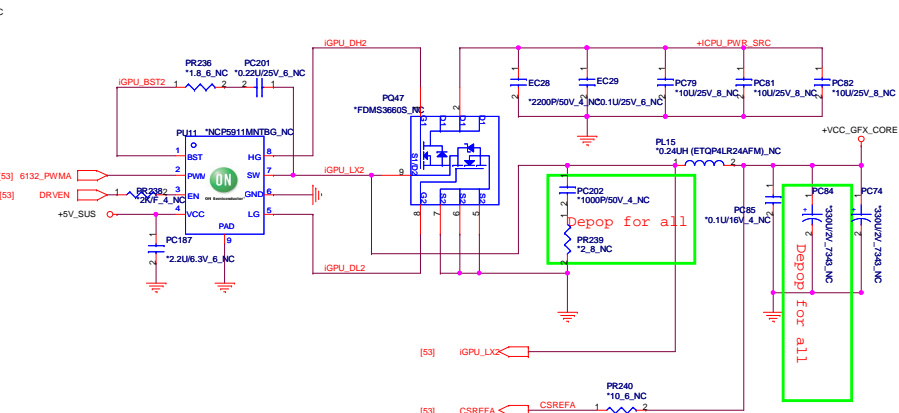
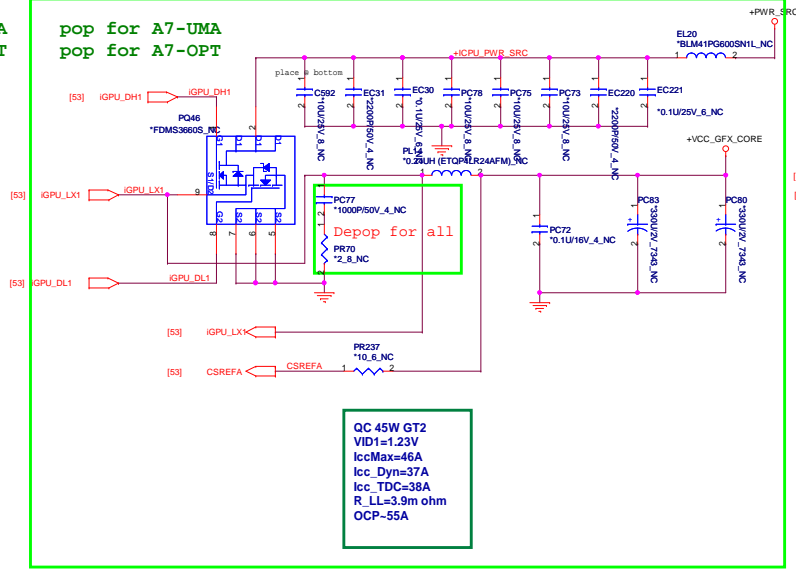


QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP=110A

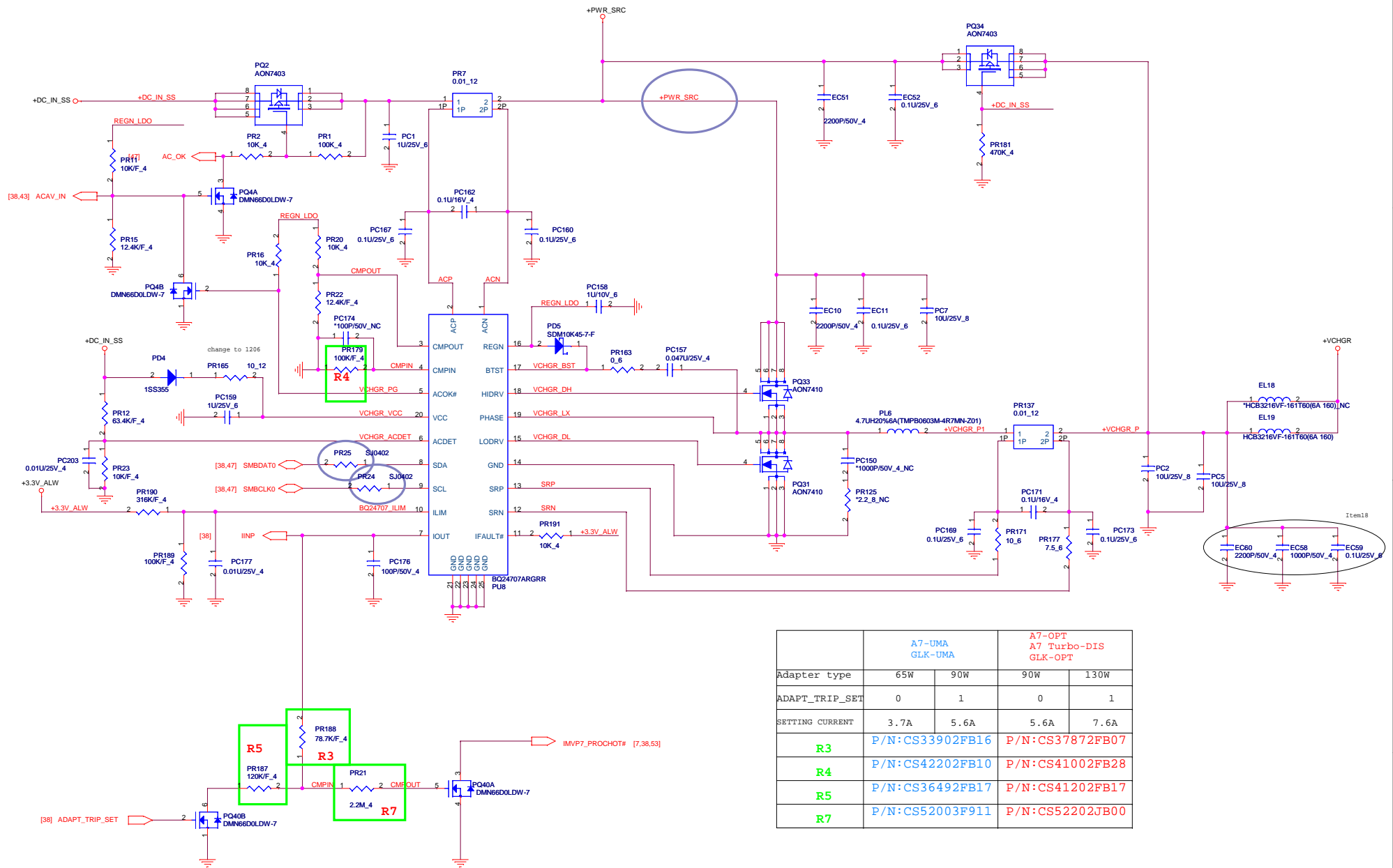


pop for GLK UMA
pop for GLK OPT

pop for A7-UMA
pop for A7-OPT



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP=55A



	A7-UMA GLK-UMA		A7-OPT A7 Turbo-DIS GLK-OPT	
Adapter type	65W	90W	90W	130W
ADAPT_TRIP_SET	0	1	0	1
SETTING CURRENT	3.7A	5.6A	5.6A	7.6A
R3	P/N:CS33902FB16		P/N:CS37872FB07	
R4	P/N:CS42202FB10		P/N:CS41002FB28	
R5	P/N:CS36492FB17		P/N:CS41202FB17	
R7	P/N:CS52003F911		P/N:CS52202JB00	

Depop for A7-UMA
Depop for GLK-UMA

N13XXX2

	DGPU_VID3	DGPU_VID2	DGPU_VID1
0.85V	1	0	1
0.95V	0	1	1
1.0V	0	1	0

N13XXX1

	DGPU_VID3	DGPU_VID2	DGPU_VID1
0.825V	1	0	1
0.975V	0	1	0
1.0V	0	0	1

+VCC_GFX_CORE
F_s=400K
Dis =30A
Turbo OC=42A
Dis OC=42A
Turbo OC=60A

PR130 pop; PR135,PR242 depop
for Nvidia OS sample

[D5] DGPU_VREN 2 PR130 10.4_M
+3.3V_GFX 1 PR135 1.0K_4
PR242

Need confirm with EE
or not have pull high
resistor for PG.

[D6] DGPU_VR_PWRGD
PR150 110K_4

PC149 150P950V_4
PC155 150P950V_4
PR141 1.65K_4

3215_FB
PC156 33P950V_4
PR158 33P950V_4
PR172 7.33K_4

VGA_PWR_LEVEL_R
PR174 220K_6 NTC
PR175 220K_6 NTC
PR176 220K_6 NTC

+VCC_GFX_CORE
VDD_SENS1
GND_SENS1

PR17 100.4_NC
PR126 100.4_NC
PR18 100.4_NC
PR19 100.4_NC

For EA test
R1 100.4
R2 100.4
R3 NC
R4 NC

PR174 220K_6 NTC
PR175 220K_6 NTC
PR176 220K_6 NTC

PR177 220K_6 NTC
PR178 220K_6 NTC
PR179 220K_6 NTC

PR180 220K_6 NTC
PR181 220K_6 NTC
PR182 220K_6 NTC

PR183 220K_6 NTC
PR184 220K_6 NTC
PR185 220K_6 NTC

PR186 220K_6 NTC
PR187 220K_6 NTC
PR188 220K_6 NTC

PR189 220K_6 NTC
PR190 220K_6 NTC
PR191 220K_6 NTC

PR192 220K_6 NTC
PR193 220K_6 NTC
PR194 220K_6 NTC

PR195 220K_6 NTC
PR196 220K_6 NTC
PR197 220K_6 NTC

PR198 220K_6 NTC
PR199 220K_6 NTC
PR200 220K_6 NTC

PR201 220K_6 NTC
PR202 220K_6 NTC
PR203 220K_6 NTC

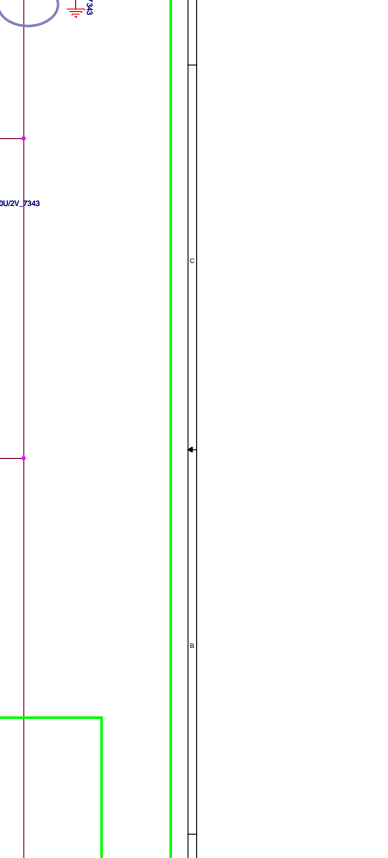
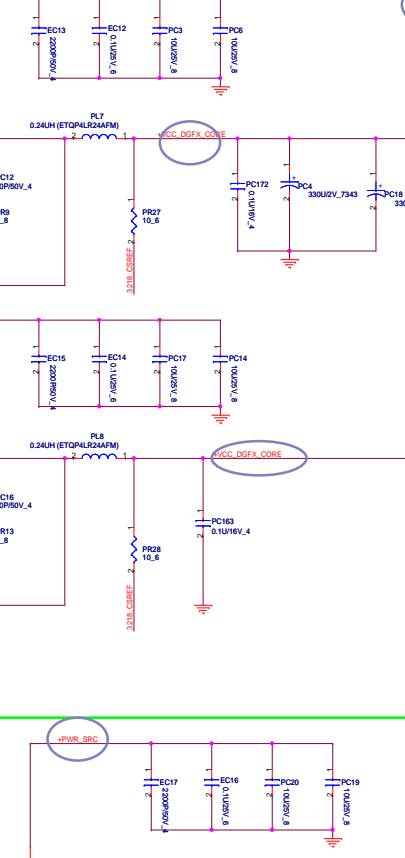
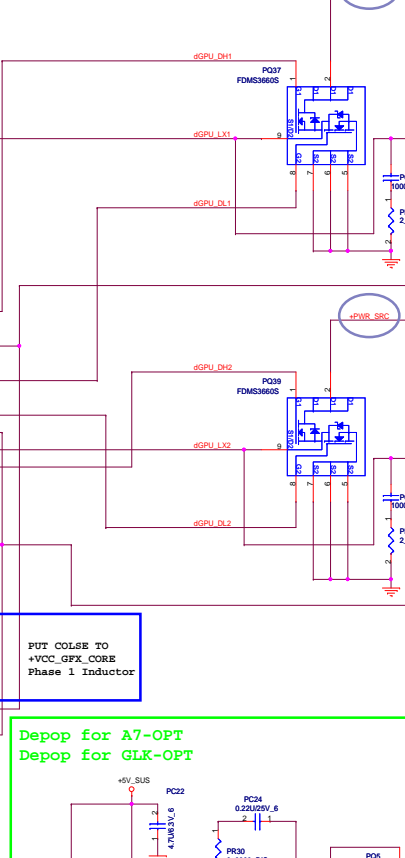
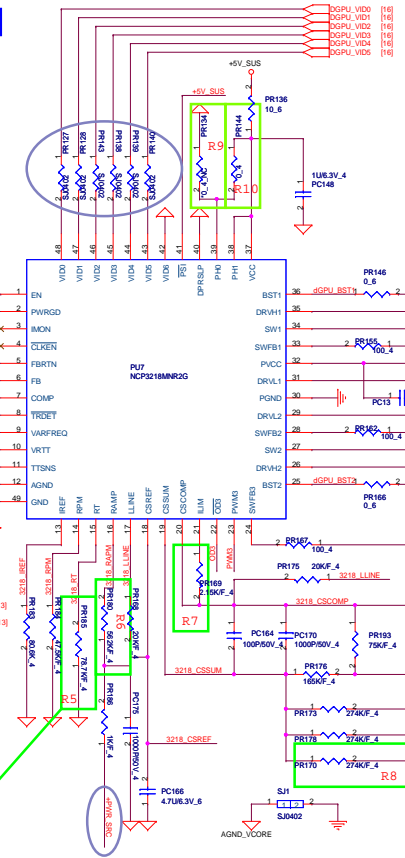
PR204 220K_6 NTC
PR205 220K_6 NTC
PR206 220K_6 NTC

PR207 220K_6 NTC
PR208 220K_6 NTC
PR209 220K_6 NTC

PR210 220K_6 NTC
PR211 220K_6 NTC
PR212 220K_6 NTC

PR213 220K_6 NTC
PR214 220K_6 NTC
PR215 220K_6 NTC

PR216 220K_6 NTC
PR217 220K_6 NTC
PR218 220K_6 NTC



Depop for A7-OPT
Depop for GLK-OPT

PUT COLSE TO
+VCC_GFX_CORE
Phase 1 Inductor

PR174 220K_6 NTC
PR175 220K_6 NTC
PR176 220K_6 NTC

PR177 220K_6 NTC
PR178 220K_6 NTC
PR179 220K_6 NTC

PR180 220K_6 NTC
PR181 220K_6 NTC
PR182 220K_6 NTC

PR183 220K_6 NTC
PR184 220K_6 NTC
PR185 220K_6 NTC

PR186 220K_6 NTC
PR187 220K_6 NTC
PR188 220K_6 NTC

PR189 220K_6 NTC
PR190 220K_6 NTC
PR191 220K_6 NTC

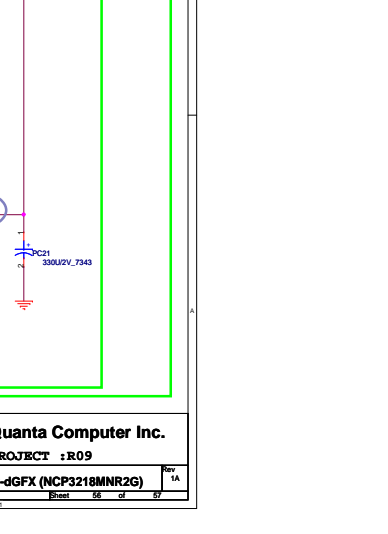
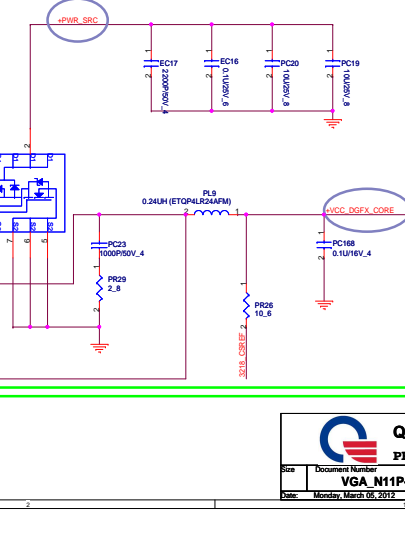
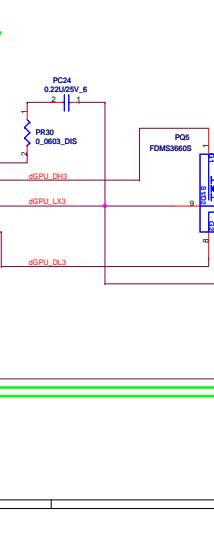
PR192 220K_6 NTC
PR193 220K_6 NTC
PR194 220K_6 NTC

PR195 220K_6 NTC
PR196 220K_6 NTC
PR197 220K_6 NTC

PR198 220K_6 NTC
PR199 220K_6 NTC
PR200 220K_6 NTC

PR201 220K_6 NTC
PR202 220K_6 NTC
PR203 220K_6 NTC

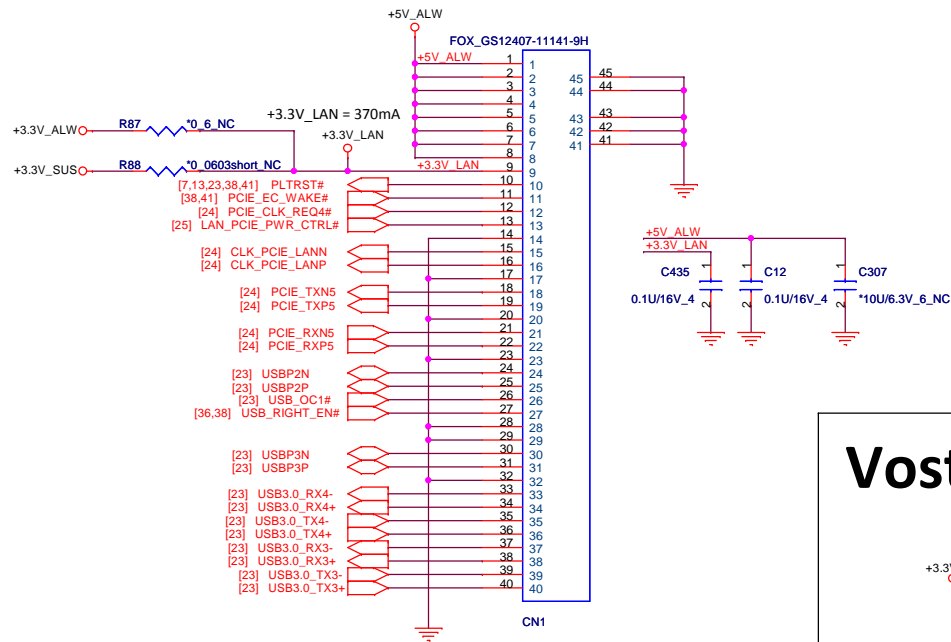
PR204 220K_6 NTC
PR205 220K_6 NTC
PR206 220K_6 NTC



Location	A7-OPT GLK-OPT (2phase)	A7 Turbo-DIS (3phase)
R5	P/N: CS41202FB17	P/N: CS3782FB15
R6	P/N: CS46492FB00	P/N: CS45622FB11
R7	P/N: CS21402FB02	P/N: CS22152FB07
R8	Depop	P/N: CS42742FB00
R9	P/N: CS00002JB38	Depop
R10	Depop	P/N: CS00002JB38

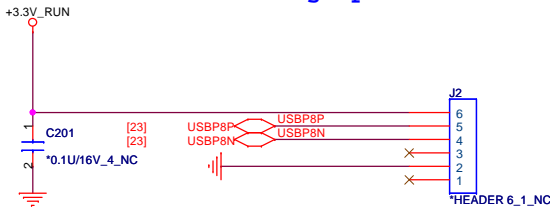
DB CONNECTOR

RJ45 + USB 3.0* 2



Vostro - NA

Fingerprint



Power button board

