1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC,Folsten_MBP17

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
B		738810	Production Release	6/19/09	6/19/09

06/15/09

DIMENSIONS ARE IN MILLIMETERS

XX ± _____

X.XX ± _____

X.XXX ± _____

ANGLES ± _____

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

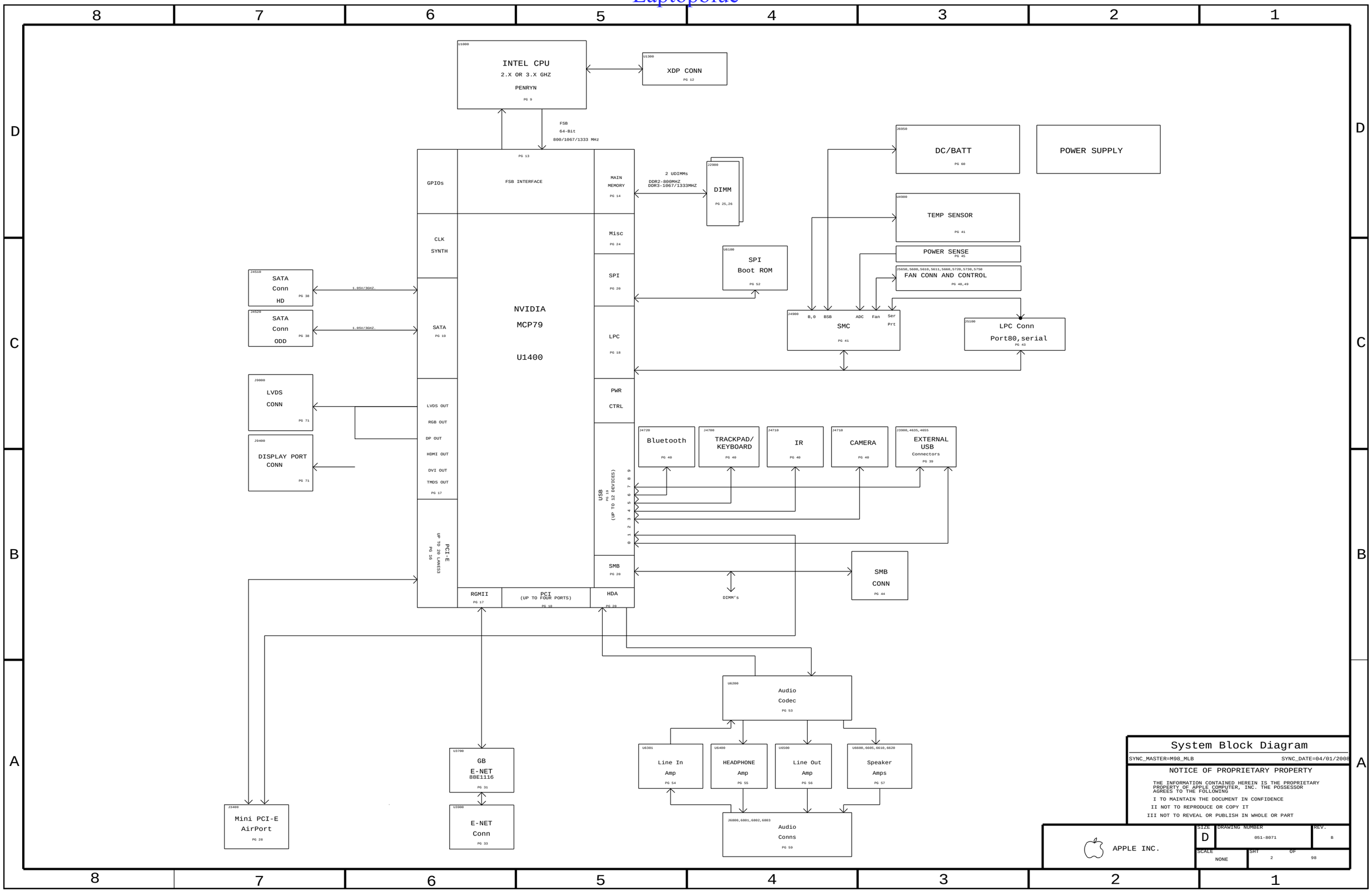
SIZE D

APPLE INC.

TITLE: SCHEM,Folsten,MBP17

DRAWING NUMBER: 051-8071 REV. B

SHT 1 OF 98



System Block Diagram

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B

SCALE	SHT	OF
NONE	2	98

"Folsten" POWER SYSTEM ARCHITECTURE

Power Block Diagram

SYNC_MASTER=RXU_K20 SYNC_DATE=07/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 3 OF 98	

PVT:

03/24/09
csa.5: Project copied from K20 mlb_pvt.
Changed CPU APNs for 2.8 and 3.06GHz CPUs.
Changed BOM and EEE codes for K20A.
csa.45: Connected =PP1V5_EXP_S0 to J4501.13 for SATA redriver on flex.
03/25/09
csa.9: Added PBUS VS 5V voltage selection resistors for keyboard backlight driver.
03/27/09
csa.90: Added 1000pF cap to the backlight power pin for EMI baseline noise.
03/30/09
csa.5: Changed the bom option to KBDLED_5V per radar# 6723272.
03/31/09
csa.1: Changed rev to 1.0.0
04/09/09
csa.70: No stuff C7099 per radar# 6772695.
04/29/09
Production Release Fab to rev A
csa.5: Changed K20A EFI ROM APN 341S2507 (BOM change only)
05/05/09
Added 128S0264 (SANYO) as alternate to 128S0257 (KEMET ELEC) per Radar# 6656624.
06/15/09
Added 107S0136 (DALE/VISHAY) as alternate to 107S0132 (CYNTEC) per Radar# 6971400.
For U7871 P/N 353S2718 is made primary. P/N 353S2310 is added back as alternate.
For U6100 Locked Bootrom P/N 341S2506 replaces existing Unlock Bootrom P/N 341S2507.

Revision History

SYNC_MASTER=NA SYNC_DATE=NA

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	4	98

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0172	PCBA,BEST,2.8,512SAM_VRAM,K20A	K20A_COMMON,EEE_9EH,CPU_2_80GHZ,FB_512_SAMSUNG
639-0173	PCBA,BEST,3.06,512SAM_VRAM,K20A	K20A_COMMON,EEE_9EK,CPU_3_06GHZ,FB_512_SAMSUNG
639-0174	PCBA,BEST,2.8,512HYN_VRAM,K20A	K20A_COMMON,EEE_9EL,CPU_2_80GHZ,FB_512_HYNIX
639-0175	PCBA,BEST,3.06,512HYN_VRAM,K20A	K20A_COMMON,EEE_9EM,CPU_3_06GHZ,FB_512_HYNIX

Folsten BOM GROUPS

BOM GROUP	BOM OPTIONS
K20A_COMMON	ALTERNATE,COMMON,K20A_COMMON1,K20A_COMMON2,K20A_DEBUG,K20A_PROGPARTS
K20A_COMMON1	ONEWIRE_PU,ISL6258,MEMRESET_HW,MEMRESET_MCP,MCP_B03,MCP_PROD,MCPSEQ_SMC,BMON_PROD,MCP_CS1_NO,FW_LVG_NEW,PROD_DIGSMS,TPDT_DEBOUNCE,KBDLED_5V
K20A_COMMON2	BOOT_MODE_USER,GPUVID_1P00V,MUXGFX,DPMUX_EN_S0,DP_ESD,EG_PWRSEQ_GMUX,DP_CA_DET_EG_PLD,BKLT_PLL_NOT,GMUX_1V8
K20A_DEBUG	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K20A_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_1024_SAMSUNG	VRAM8,VRAM_1024_SAMSUNG
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM4,VRAM_512_HYNIX

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung
152S0684	152S0368		ALL	Maglayers alt to Dale/Vishay
104S0023	104S0018		ALL	Cyntec alt to sense resistor
104S0024	104S0017		ALL	Panasonic alt to FW resistor
341S2367	341S2366		ALL	Macronix alt to SST
152S0876	152S0782		ALL	Maglayer alt to Delta
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
514-0612	514-0607		ALL	FOXLINK ALT TO FOXCONN XCVR
514-0613	514-0608		ALL	FOXLINK ALT TO FOXCONN RCVR
152S0684	152S0421		ALL	MAG LAYERS ALT TO VISHAY
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
152S0915	152S0796		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
128S0264	128S0257		ALL	SANYO ALT TO KEMET ELEC.
107S0136	107S0132		ALL	DALE/VISHAY ALT TO CYNTEC.
353S2310	353S2718		ALL	INTERSIL.COMMON TO K24/K19

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9EH]	CRITICAL	EEE_9EH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9EK]	CRITICAL	EEE_9EK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9EL]	CRITICAL	EEE_9EL
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9EM]	CRITICAL	EEE_9EM

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0737	1	IC,ASSP,GPU,NV G96-GS,VLOWLKG,BGA969,LF	U8000	CRITICAL	
338S0694	1	IC,RTL8251CA-VB-GR,GIGE TRANSCEIVER,48P LQFP	U3700	CRITICAL	
338S0654	1	IC,FW643-E,1394B PHY/DHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0710	1	IC,MCP79XT-B3,35X35MM,BGA1437	U1400	CRITICAL	MCP_B03
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2355	1	IC,SMC,DEVELOPMENT,K20	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2506	1	IC,LOCKED EFI ROM,K20A	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
341S2383	1	IC,PSOC +W/USB,56PIN,MLF,M98	U5701	CRITICAL	TPAD_PROG
337S3744	1	IC,PDC,SLGKH,PMQ,3.06,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_3_06GHZ
337S3682	1	IC,PDC,SLGEM,PMQ,2.80,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_80GHZ
333S0481	4	IC,SGRAM,GDDR3,32MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0481	8	IC,SGRAM,GDDR3,32MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550,U9100,U9150,U9300,U9250	CRITICAL	VRAM_1024_SAMSUNG
333S0506	4	IC,SDRAM,GDDR3,32MX32,900MHZ,TIVA,HF	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX

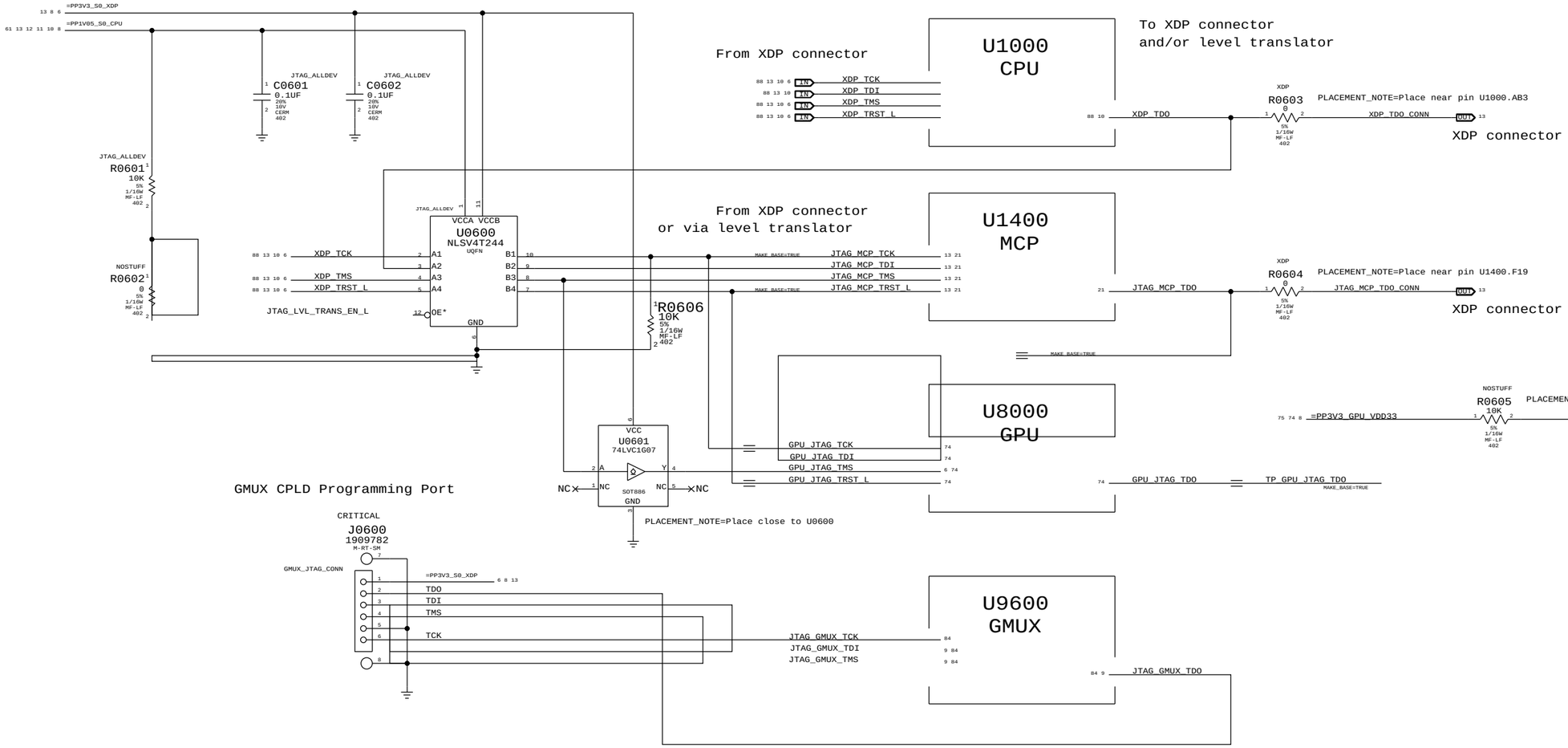
BOM Configuration

SYNC_MASTER=K20A_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 5 OF 98	

1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)



JTAG Scan Chain

SYNC_MASTER=BEN_K20 SYNC_DATE=07/11/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 6 OF 98	

Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	8 48	3 TPs per Fan
TRUE	FAN_LT_PWM	48	
TRUE	FAN_LT_TACH	48	

J5660 (RIGHT FAN CONN)

TRUE	FAN_RT_PWM	48	
TRUE	FAN_RT_TACH	48	5 TPs per Fan
TRUE	GND		

J6780 (MIC CONN)

TRUE	BI_MIC_LO	57 58	
TRUE	BI_MIC_SHIELD	57 58	
TRUE	BI_MIC_HI	57 58	

J6781 (LEFT SPEAKER)

TRUE	SPKRAMP_L1_OUT_P	56 57 96	
TRUE	SPKRAMP_L1_OUT_N	56 57 96	
TRUE	SPKRAMP_L2_OUT_P	56 57 96	
TRUE	SPKRAMP_L2_OUT_N	56 57 96	

J6782 (RIGHT & SUB SPEAKER)

TRUE	SPKRAMP_LFE_OUT_P	56 57 96	
TRUE	SPKRAMP_LFE_OUT_N	56 57 96	
TRUE	SPKRAMP_R1_OUT_P	56 57 96	
TRUE	SPKRAMP_R1_OUT_N	56 57 96	
TRUE	SPKRAMP_R2_OUT_P	56 57 96	
TRUE	SPKRAMP_R2_OUT_N	56 57 96	

J9000 (LVDS CONN)

TRUE	BKL_SYNC	78 85	
TRUE	PP3V3_SW_LCD	78	
TRUE	=PP3V3_S0_DDC_LCD	8 75 78	
TRUE	PPVOUT_S0_LCDBKLT	78 85	2 TP needed
TRUE	LVDS_DDC_CLK	78 81	
TRUE	LVDS_DDC_DATA	78 81	
TRUE	LVDS_CONN_A_DATA_P<0>	78 81 95	
TRUE	LVDS_CONN_A_DATA_N<0>	78 81 95	
TRUE	LVDS_CONN_A_DATA_P<1>	78 81 95	
TRUE	LVDS_CONN_A_DATA_N<1>	78 81 95	
TRUE	LVDS_CONN_A_DATA_P<2>	78 81 95	
TRUE	LVDS_CONN_A_DATA_N<2>	78 81 95	
TRUE	LVDS_CONN_A_CLK_F_P	78 95	
TRUE	LVDS_CONN_A_CLK_F_N	78 95	
TRUE	LVDS_CONN_B_DATA_P<0>	78 81 95	
TRUE	LVDS_CONN_B_DATA_N<0>	78 81 95	
TRUE	LVDS_CONN_B_DATA_P<1>	78 81 95	
TRUE	LVDS_CONN_B_DATA_N<1>	78 81 95	
TRUE	LVDS_CONN_B_DATA_P<2>	78 81 95	
TRUE	LVDS_CONN_B_DATA_N<2>	78 81 95	
TRUE	LVDS_CONN_B_CLK_F_P	78 95	
TRUE	LVDS_CONN_B_CLK_F_N	78 95	
TRUE	LED_RETURN_1	78 85	
TRUE	LED_RETURN_2	78 85	
TRUE	LED_RETURN_3	78 85	
TRUE	LED_RETURN_4	78 85	
TRUE	LED_RETURN_5	78 85	
TRUE	LED_RETURN_6	78 85	
TRUE	GND		4 TPs

J4500 (SATA ODD CONN)

TRUE	PP5V_SW_ODD	38	
TRUE	SMC_ODD_DETECT	38 41	
TRUE	SATA_ODD_D2R_C_P	38 90	
TRUE	SATA_ODD_D2R_C_N	38 90	
TRUE	SATA_ODD_R2D_P	38 90	
TRUE	SATA_ODD_R2D_N	38 90	
TRUE	GND		3 TPs

J4501 (SATA HDD CONN)

TRUE	PP5V_S0_HDD_FLT	38	
TRUE	SATA_HDD_R2D_P	38 90	
TRUE	SATA_HDD_R2D_N	38 90	
TRUE	SATA_HDD_D2R_C_N	38 90	
TRUE	SATA_HDD_D2R_C_P	38 90	
TRUE	GND		5 TPs

J5815 (KBD BACKLIGHT CONN)

TRUE	KBDLED_ANODE	50	
TRUE	SMC_KDBLED_PRESENT_L	50	
TRUE	GND		

FUNC_TEST

TRUE	GND	
TRUE	GND	6 TPs

USB PORTS

TRUE	PP5V_S3_RTUSB_A_F	39	
TRUE	USB2_LT1_N	39 96	
TRUE	USB2_LT1_P	39 96	
TRUE	GND		
TRUE	PP5V_S3_RTUSB_B_F	39	
TRUE	USB_LT2_N	39 96	
TRUE	USB_LT2_P	39 96	
TRUE	GND		
TRUE	PP5V_S3_RTUSB_C_F	98	
TRUE	USB_LT3_N	96 98	
TRUE	USB_LT3_P	96 98	
TRUE	GND		

J3401 (AIRPORT/BT/CAMERA CONN)

TRUE	PCIE_MINI_D2R_P	17 30 90	
TRUE	PCIE_MINI_D2R_N	17 30 90	
TRUE	PCIE_MINI_R2D_P	30 90	
TRUE	PCIE_MINI_R2D_N	30 90	
TRUE	PCIE_CLK100M_MINI_CONN_P	30 96	
TRUE	PCIE_CLK100M_MINI_CONN_N	30 96	
TRUE	MINI_CLKREQ_Q_L	30	
TRUE	PCIE_WAKE_L	7 17 30 31	
TRUE	MINI_RESET_CONN_L	30	
TRUE	PP5V_WLAN	30	
TRUE	PP5V_S3_BTCAMERA_F	30	
TRUE	SMBUS_SMC_A_S3_SDA	7 44 94	
TRUE	SMBUS_SMC_A_S3_SCL	7 44 94	
TRUE	USB_CAMERA_CONN_P	30 96	
TRUE	USB_CAMERA_CONN_N	30 96	
TRUE	CONN_USB2_BT_P	30 96	
TRUE	CONN_USB2_BT_N	30 96	

J3500 (EXPRESS CARD CONN)

TRUE	PP1V5_S0_EXCARD_SWITCH	31	
TRUE	PCIE_WAKE_L	7 17 30 31	
TRUE	SMBUS_MCP_0_CLK	13 21 44 91	
TRUE	SMBUS_MCP_0_DATA	13 21 44 91	
TRUE	PP3V3_S0_EXCARD_SWITCH	31	
TRUE	PP3V3_S3_EXCARD_SWITCH	31	
TRUE	USB2_EXCARD_CONN_N	31 96	
TRUE	USB2_EXCARD_CONN_P	31 96	
TRUE	EXCARD_CPUSB_L	31	
TRUE	EXCARD_CLKREQ_CONN_L	31	
TRUE	EXCARD_CPPE_L	31	
TRUE	PLT_RESET_SWITCH_L	31	
TRUE	PCIE_EXCARD_D2R_P	17 31 90	
TRUE	PCIE_EXCARD_D2R_N	17 31 90	
TRUE	PCIE_EXCARD_R2D_P	31 90	
TRUE	PCIE_EXCARD_R2D_N	31 90	
TRUE	PCIE_CLK100M_EXCARD_CONN_P	31 96	
TRUE	PCIE_CLK100M_EXCARD_CONN_N	31 96	

J5800 (IPD FLEX CONN)

TRUE	PP3V3_S3_LDO	50	
TRUE	PP18V5_S3	7 50	
TRUE	TPAD_GND_F	50	
TRUE	Z2_CS_L	49 50	
TRUE	Z2_DEBUG3	49 50	
TRUE	Z2_MISO	49 50	
TRUE	Z2_BOOST_EN	50	
TRUE	Z2_BOOT_CFG1	49 50	
TRUE	Z2_CLKIN	49 50	
TRUE	Z2_KEY_ACT_L	49 50	
TRUE	Z2_RESET	49 50	
TRUE	PSOC_F_CS_L	49 50	
TRUE	PICKB_L	49 50	
TRUE	PSOC_MISO	49 50	
TRUE	PSOC_MOSI	49 50	
TRUE	PSOC_SCLK	49 50	
TRUE	SMBUS_SMC_A_S3_SCL	7 44 94	
TRUE	SMBUS_SMC_A_S3_SDA	7 44 94	

J6900 (DC POWER CONN)

TRUE	ADAPTER_SENSE	59	
TRUE	PP18V5_DCIN_FUSE	59	
TRUE	GND		

J6950 (MAIN BATT CONN)

TRUE	PPVBAT_G3H_CONN_F	59	
TRUE	SMBUS_SMC_BSA_SCL	7 44 94	
TRUE	SMBUS_SMC_BSA_SDA	7 44 94	
TRUE	SMC_BS_ALRT_L	41 42 59	
TRUE	GND		

J6995 (BAT LED CONN)

TRUE	PP3V42_G3H	7 8 42	
TRUE	SMBUS_SMC_BSA_SDA	7 44 94	
TRUE	SMBUS_SMC_BSA_SCL	7 44 94	
TRUE	SMC_BIL_BUTTON_DB_L	42 59	
TRUE	GND		

J5713 (KEY BOARD CONN)

TRUE	PP3V3_S3	7 8	
TRUE	PP3V42_G3H	7 8 42	
TRUE	WS_KBD1	49	
TRUE	WS_KBD2	49	
TRUE	WS_KBD3	49	
TRUE	WS_KBD4	49	
TRUE	WS_KBD5	49	
TRUE	WS_KBD6	49	
TRUE	WS_KBD7	49	
TRUE	WS_KBD8	49	
TRUE	WS_KBD9	49	
TRUE	WS_KBD10	49	
TRUE	WS_KBD11	49	
TRUE	WS_KBD12	49	
TRUE	WS_KBD13	49	
TRUE	WS_KBD14	49	
TRUE	WS_KBD15_CAP	49	
TRUE	WS_KBD16_NUM	49	
TRUE	WS_KBD17	49	
TRUE	WS_KBD18	49	
TRUE	WS_KBD19	49	
TRUE	WS_KBD20	49	
TRUE	WS_KBD21	49	
TRUE	WS_KBD22	49	
TRUE	WS_KBD23	49	
TRUE	WS_KBD_ONOFF_L	49	
TRUE	WS_LEFT_SHIFT_KBD	49	
TRUE	WS_LEFT_OPTION_KBD	49	
TRUE	WS_CONTROL_KBD	49	

J4800 (FRONT CABLE CONN)

TRUE	PP3V42_G3H_LIDSWITCH_R	40	
TRUE	PP5V_S3_IR_R	40	
TRUE	SMC_LID_R	40	
TRUE	IR_RX_OUT	40	
TRUE	SYS_LED_ANODE	40 42	
TRUE	GND		

J5502 (SENSOR CONN)

TRUE	MCPTHMSNS_D_P	47 96	
TRUE	MCPTHMSNS_D_N	47 96	

POWER RAILS

FUNC_TEST

TRUE	PM_SLP_S3_L	21 33 36 41 67 82 84	
TRUE	PPBUS_G3H	8 45	
TRUE	PPBUS_CPU_IMVP_ISNS	8	
TRUE	PP3V42_G3H	7 8 42	
TRUE	PP5V_S3	8	
TRUE	PP5V_S0	8	
TRUE	PPVCORE_S0_CPU	8	
TRUE	PPVCORE_S0_MCP	7 8	
TRUE	PP3V3_S5	8 96	
TRUE	PP3V3_S3	7 8	
TRUE	PP3V3_S0	8 9 96	
TRUE	PP2V5_S0	8	
TRUE	PP1V2_S0	8	
TRUE	PP1V8_S0	8	
TRUE	PP1VBR1V5_S3	8	
TRUE	PP1VBR1V5_S0	8	
TRUE	PPMCPDDR_ISNS	7 8	
TRUE	PP1V05_S0	8	
TRUE	PP1V2R1V05_S5	8	
TRUE	PPCPUVTT_S0	8	
TRUE	PP0V9R0V75_S0_DDRVTT	8	
TRUE	PP1V2R1V05_ENET	8	
TRUE	PP3V3_ENET_PHY	8	
TRUE	PPVP_FW	8	
TRUE	PP1V0_FW	8	
TRUE	PP3V3_S0GPU	8	
TRUE	PP1V1_S0GPU	8	
TRUE	PP1V8_S0GPU_ISNS	8	
TRUE	PPVCORE_GPU	8	
TRUE	PP1V8_S0GPU_ISNS_R	8	
TRUE	PP3V3_S5_AVREF_SMC	41 42	
TRUE	PP18V5_S3	7 50	
TRUE	PPDCIN_G3H	8	
TRUE	PPVCORE_S0_MCP	7 8	
TRUE	PPMCPDDR_ISNS	7 8	
TRUE	PPVTTDDR_S3	8	
TRUE	PP1V8_GPUIFPX	8	

FUNC_TEST

TRUE	SYS_LED_ANODE_R	40	
TRUE	LPC_CLK33M_LPCPLUS	25 43 91	
TRUE	LPC_AD<0..3>	19 41 43 84 91	
TRUE	SPI_ALT_MOSI	43	
TRUE	SPI_ALT_MISO	43	
TRUE	LPC_FRAME_L	19 41 43 84 91	
TRUE	PM_CLKRUN_L	19 41 43	
TRUE	SMC_TMS	41 42 43	
TRUE	DEBUG_RESET_L	25 43	
TRUE	SMC_TDO	41 42 43	
TRUE	SMC_TRST_L	41 43	
TRUE	SMC_MD1	41 43	
TRUE	SMC_TX_L	39 41 42 43	
TRUE	SPIROM_USE_MLB	43	
TRUE	SPI_ALT_CLK	43	
TRUE	SPI_ALT_CS_L	43	
TRUE	LPC_SERIRQ	19 41 43	
TRUE	LPC_PWRDWN_L	19 41 43	
TRUE	SMC_TDI	41 42 43	
TRUE	SMC_TCK	41 42 43	
TRUE	SMC_RESET_L	41 42 43	
TRUE	SMC_NMI	41 43	
TRUE	SMC_RX_L	39 41 42 43	
TRUE	LPCPLUS_GPIO	18 43	
TRUE	TISSP_SCLK_P1_1	49	
TRUE	TISSP_SDATA_P1_0	49	
TRUE	SMC_ONOFF_L	41 42 49	
TRUE	PM_SYSRST_L	25 41	
TRUE	BKL_FB		
TRUE	BKL_GD		
TRUE	BKL_SW		
TRUE	BKLT_EN	85	
TRUE	BKL_SCL		
TRUE	BKL_SDA		
TRUE	LCD_BKLT_PWM	84 85	

ICT Test Points

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	10 14 88	
TRUE	FSB_ADS_L	10 14 88	
TRUE	FSB_ADSTB_L<1..0>	10 14 88	
TRUE	FSB_D_L<63..0>	10 14 88	
TRUE	FSB_DBSY_L	10 14 88	
TRUE	FSB_DINV_L<3..0>	10 14 88	
TRUE	FSB_DRDY_L	10 14 88	
TRUE	FSB_DSTB_L_N<3..0>	10 14 88	
TRUE	FSB_DSTB_L_P<3..0>	10 14 88	
TRUE	FSB_HIT_L	10 14 88	
TRUE	FSB_HITM_L	10 14 88	
TRUE	FSB_LOCK_L	10 14 88	
TRUE	FSB_REQ_L<4..0>	10 14 88	

FB NO_TESTs

NO_TEST

TRUE	FB_A_DQ<63..0>	71 72 79 95	
TRUE	FB_B_DQ<63..0>	71 73 80 95	
TRUE	FB_B_BA<1>	71 73 80 95	
TRUE	FB_B_CAS_L	71 73 80 95	
TRUE	FB_B_CS0_L	71 73 95	
TRUE	FB_B_MA<11>	71 73 80 95	

LVDS NO_TESTs

NO_TEST

TRUE	LVDS_A_DATA_N<0>	81 84 95	
TRUE	LVDS_A_DATA_P<0>	81 84 95	
TRUE	LVDS_B_CLK_P	81 84 95	
TRUE	LVDS_B_DATA_N<0>	81 84 95	
TRUE	LVDS_B_DATA_P<0>	81 84 95	
TRUE	LVDS_EG_A_DATA_N<2>	76 84 95	

NC NO_TESTs

NO_TEST

TRUE	NC_SMC_FAN_3_TACH	42	
TRUE	NC_SMC_FAN_3_CTL	42	
TRUE	NC_SMC_FAN_2_TACH	42	
TRUE	NC_SMC_FAN_2_CTL	42	
TRUE	NC_FW2_TPBP	37	
TRUE	NC_FW2_TPBN	37	
TRUE	NC_FW2_TPBPIAS	37	
TRUE	NC_FW2_TPAP	37	
TRUE	NC_FW2_TPAN	37	
TRUE	NC_FW0_TPBP	37	
TRUE	NC_FW0_TPBN	37	
TRUE	NC_FW0_TPAP	37	
TRUE	NC_ESTARLDO_EN	42	
TRUE	NC_ALS_GAIN	42	

NC NO_TESTs

NO_TEST

TRUE	TP_CPU_PECI_MCP	MAKE_BASE=TRUE	NC_CPU_PECI_MCP
TRUE	TP_CPU_TEST3	MAKE_BASE=TRUE	NC_CPU_TEST3
TRUE	TP_ENET_INTR_L	MAKE_BASE=TRUE	NC_ENET_INTR_L
TRUE	TP_ENET_PWRDWN_L	MAKE_BASE=TRUE	NC_ENET_PWRDWN_L
TRUE	TP_FW643_AVREG	MAKE_BASE=TRUE	NC_FW643_AVREG
TRUE	TP_FW643_TDI	MAKE_BASE=TRUE	NC_FW643_TDI
TRUE	TP_MEM_A_A<15>	MAKE_BASE=TRUE	NC_MEM_A_A<15>
TRUE	TP_MEM_A_CKE<2>	MAKE_BASE=TRUE	NC_MEM_A_CKE<2>
TRUE	TP_MEM_A_CKE<3>	MAKE_BASE=TRUE	NC_MEM_A_CKE<3>
TRUE	TP_MEM_A_CLK2N	MAKE_BASE=TRUE	NC_MEM_A_CLK2N
TRUE	TP_MEM_A_CLK2P	MAKE_BASE=TRUE	NC_MEM_A_CLK2P
TRUE	TP_MEM_A_CLK3N	MAKE_BASE=TRUE	NC_MEM_A_CLK3N
TRUE	TP_MEM_A_CLK3P	MAKE_BASE=TRUE	NC_MEM_A_CLK3P
TRUE	TP_MEM_A_CLK4N	MAKE_BASE=TRUE	NC_MEM_A_CLK4N
TRUE	TP_MEM_A_CLK4P	MAKE_BASE=TRUE	NC_MEM_A_CLK4P
TRUE	TP_MEM_A_CLK5N	MAKE_BASE=TRUE	NC_MEM_A_CLK5N
TRUE	TP_MEM_A_CLK5P	MAKE_BASE=TRUE	NC_MEM_A_CLK5P
TRUE	TP_MEM_A_CS_L<2>	MAKE_BASE=TRUE	NC_MEM_A_CS_L<2>
TRUE	TP_MEM_A_CS_L<3>	MAKE_BASE=TRUE	NC_MEM_A_CS_L<3>
TRUE	TP_MEM_A_ODT<2>	MAKE_BASE=TRUE	NC_MEM_A_ODT<2>
TRUE	TP_MEM_A_ODT<3>	MAKE_BASE=TRUE	NC_MEM_A_ODT<3>
TRUE	TP_MEM_B_A<15>	MAKE_BASE=TRUE	NC_MEM_B_A<15>
TRUE	TP_MEM_B_CKE<2>	MAKE_BASE=TRUE	NC_MEM_B_CKE<2>
TRUE	TP_MEM_B_CLK2P	MAKE_BASE=TRUE	NC_MEM_B_CLK2P
TRUE	TP_MEM_B_CLK3N	MAKE_BASE=TRUE	NC_MEM_B_CLK3N
TRUE	TP_MEM_B_CLK3P	MAKE_BASE=TRUE	NC_MEM_B_CLK3P
TRUE	TP_MEM_B_CLK4N	MAKE_BASE=TRUE	NC_MEM_B_CLK4N
TRUE	TP_MEM_B_CLK4P	MAKE_BASE=TRUE	NC_MEM_B_CLK4P
TRUE	TP_MEM_B_CLK5N	MAKE_BASE=TRUE	NC_MEM_B_CLK5N
TRUE	TP_MEM_B_CLK5P	MAKE_BASE=TRUE	NC_MEM_B_CLK5P
TRUE	TP_MEM_B_CS_L<2>	MAKE_BASE=TRUE	NC_MEM_B_CS_L<2>
TRUE	TP_MEM_B_CS_L<3>	MAKE_BASE=TRUE	NC_MEM_B_CS_L<3>
TRUE	TP_MEM_B_ODT<2>	MAKE_BASE=TRUE	NC_MEM_B_ODT<2>
TRUE	TP_MEM_B_ODT<3>	MAKE_BASE=TRUE	NC_MEM_B_ODT<3>
TRUE	TP_MLB_RAM_SIZE	MAKE_BASE=TRUE	NC_MLB_RAM_SIZE
TRUE	TP_MLB_RAM_VENDOR	MAKE_BASE=TRUE	NC_MLB_RAM_VENDOR
TRUE	TP_GPU_BUFRST_L	MAKE_BASE=TRUE	NC_GPU_BUFRST_L
TRUE	TP_GPU_GSTATE<0>	MAKE_BASE=TRUE	NC_GPU_GSTATE<0>
TRUE	TP_GPU_GSTATE<1>	MAKE_BASE=TRUE	NC_GPU_GSTATE<1>
TRUE	TP_GPU_MIOA_D<9..0>	MAKE_BASE=TRUE	NC_GPU_MIOA_D<9..0>
TRUE	TP_GPU_MIOA_DE	MAKE_BASE=TRUE	NC_GPU_MIOA_DE
TRUE	TP_GPU_PGOOD_OUT_L	MAKE_BASE=TRUE	NC_GPU_PGOOD_OUT_L
TRUE	TP_GPU_VCORE_VID3	MAKE_BASE=TRUE	NC_GPU_VCORE_VID3
TRUE	TP_LPC_DRQ0_L	MAKE_BASE=TRUE	NC_LPC_DRQ0_L
TRUE	TP_LVDS_EG_B_CLK_N	MAKE_BASE=TRUE	NC_LVDS_EG_B_CLK_N
TRUE	TP_LVDS_EG_B_CLK_P	MAKE_BASE=TRUE	NC_LVDS_EG_B_CLK_P
TRUE	TP_LVDS_EG_BKL_PWM	MAKE_BASE=TRUE	NC_LVDS_EG_BKL_PWM
TRUE	TP_LVDS_IG_B_CLKN	MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKN
TRUE	TP_LVDS_IG_B_CLKP	MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP
TRUE	TP_LVDS_IG_BKL_PWM	MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM
TRUE	TP_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE	NC_MCP_BUF_SIO_CLK
TRUE	TP_MCP_GPIO_18	MAKE_BASE=TRUE	NC_MCP_GPIO_18
TRUE	TP_MCP_KBDRSTIN_L	MAKE_BASE=TRUE	NC_MCP_KBDRSTIN_L
TRUE	TP_MCP_SATALED_L	MAKE_BASE=TRUE	NC_MCP_SATALED_L

NC NO_TESTs

NO_TEST

TRUE	TP_PCI_AD<31..8>	MAKE_BASE=TRUE	NC_PCI_AD<31..8>
TRUE	TP_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE	NC_PCI_C_BE_L<3..0>
TRUE	TP_PCI_CLK0	MAKE_BASE=TRUE	NC_PCI_CLK0
TRUE	TP_PCI_CLK1	MAKE_BASE=TRUE	NC_PCI_CLK1
TRUE	TP_PCI_DEVSEL_L	MAKE_BASE=TRUE	NC_PCI_DEVSEL_L
TRUE	TP_PCI_FRAME_L	MAKE_BASE=TRUE	NC_PCI_FRAME_L
TRUE	TP_PCI_GNT0_L	MAKE_BASE=TRUE	NC_PCI_GNT0_L
TRUE	TP_PCI_GNT1_L	MAKE_BASE=TRUE	NC_PCI_GNT1_L
TRUE	TP_PCI_INTW_L	MAKE_BASE=TRUE	NC_PCI_INTW_L
TRUE	TP_PCI_INTX_L	MAKE_BASE=TRUE	NC_PCI_INTX_L
TRUE	TP_PCI_INTY_L	MAKE_BASE=TRUE	NC_PCI_INTY_L
TRUE	TP_PCI_INTZ_L	MAKE_BASE=TRUE	NC_PCI_INTZ_L
TRUE	TP_PCI_IRDY_L	MAKE_BASE=TRUE	NC_PCI_IRDY_L
TRUE	TP_PCI_PAR	MAKE_BASE=TRUE	NC_PCI_PAR
TRUE	TP_PCI_PERR_L	MAKE_BASE=TRUE	NC_PCI_PERR_L
TRUE	TP_PCI_RESET1_L	MAKE_BASE=TRUE	NC_PCI_RESET1_L
TRUE	TP_PCI_SERR_L	MAKE_BASE=TRUE	NC_PCI_SERR_L
TRUE	TP_PCI_STOP_L	MAKE_BASE=TRUE	NC_PCI_STOP_L
TRUE	TP_PCI_TRDY_L	MAKE_BASE=TRUE	NC_PCI_TRDY_L
TRUE	TP_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P
TRUE	TP_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N
TRUE	TP_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P
TRUE	TP_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N
TRUE	TP_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P
TRUE	TP_PCIE_PE4_D2RN	MAKE_BASE=TRUE	NC_PCIE_PE4_D2RN
TRUE	TP_PCIE_PE4_D2RP	MAKE_BASE=TRUE	NC_PCIE_PE4_D2RP
TRUE	TP_PE4_CLKREQ_L	MAKE_BASE=TRUE	NC_PE4_CLKREQ_L
TRUE	TP_PEX_CLKREQ_L	MAKE_BASE=TRUE	NC_PEX_CLKREQ_L
TRUE	TP_PSOC_P1_3	MAKE_BASE=TRUE	NC_PSOC_P1_3
TRUE	TP_SATA_C_D2RN	MAKE_BASE=TRUE	NC_SATA_C_D2RN
TRUE	TP_SATA_C_D2RP	MAKE_BASE=TRUE	NC_SATA_C_D2RP
TRUE	TP_SATA_C_R2D_CN	MAKE_BASE=TRUE	NC_SATA_C_R2D_CN
TRUE	TP_SATA_C_R2D_CP	MAKE_BASE=TRUE	NC_SATA_C_R2D_CP
TRUE	TP_SATA_D_D2RN	MAKE_BASE=TRUE	NC_SATA_D_D2RN
TRUE	TP_SATA_D_D2RP	MAKE_BASE=TRUE	NC_SATA_D_D2RP
TRUE	TP_SATA_D_R2D_CN	MAKE_BASE=TRUE	NC_SATA_D_R2D_CN
TRUE	TP_SATA_D_R2D_CP	MAKE_BASE=TRUE	NC_SATA_D_R2D_CP
TRUE	TP_SATA_E_D2RN	MAKE_BASE=TRUE	NC_SATA_E_D2RN
TRUE	TP_SATA_E_D2RP	MAKE_BASE=TRUE	NC_SATA_E_D2RP
TRUE	TP_SATA_E_R2D_CN	MAKE_BASE=TRUE	NC_SATA_E_R2D_CN
TRUE	TP_SATA_E_R2D_CP	MAKE_BASE=TRUE	NC_SATA_E_R2D_CP
TRUE	TP_SATA_F_D2RN	MAKE_BASE=TRUE	NC_SATA_F_D2RN
TRUE	TP_SATA_F_D2RP	MAKE_BASE=TRUE	NC_SATA_F_D2RP
TRUE	TP_SATA_F_R2D_CN	MAKE_BASE=TRUE	NC_SATA_F_R2D_CN
TRUE	TP_SATA_F_R2D_CP	MAKE_BASE=TRUE	NC_SATA_F_R2D_CP
TRUE	TP_SB_A20GATE	MAKE_BASE=TRUE	NC_SB_A20GATE
TRUE	TP_SMC_P41	MAKE_BASE=TRUE	NC_SMC_P41
TRUE	TP_USB_10P	MAKE_BASE=TRUE	NC_USB_10P
TRUE	TP_USB_11N	MAKE_BASE=TRUE	NC_USB_11N
TRUE	TP_USB_11P	MAKE_BASE=TRUE	NC_USB_11P
TRUE	TP_USB_EXTDN	MAKE_BASE=TRUE	NC_USB_EXTDN
TRUE	TP_USB_EXTDP	MAKE_BASE=TRUE	NC_USB_EXTDP
TRUE	TP_USB_MININ	MAKE_BASE=TRUE	NC_USB_MININ
TRUE	TP_USB_MINIP	MAKE_BASE=TRUE	NC_USB_MINIP
TRUE	TP_XDP_OBSDATA_B2	MAKE_BASE=TRUE	NC_XDP_OBSDATA_B2
TRUE	TP_XDP_OBSDATA_B3	MAKE_BASE=TRUE	NC_XDP_OBSDATA_B3

Functional / ICT Test

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 7 OF 98	

"G3Hot" (Always-Present) Rails

60 =PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=6V
MAKE_BASE=TRUE
=PPVIN_S5_P5VP3V3 62
=PPVIN_S0_CPUVTTS0 65
=PPBUS_S0_LCDBKLT 86
=PPVIN_GPU_GPUVCORE 77
=PPVIN_S5_CPU_IMVP_ISNS_R 45
=PPVIN_S0_P5VRTS0_MCPCORE 64
=PPVIN_S3_DDRREG 63
=PPVIN_S0GPU_P1V8P1V1 83
=PPVBAT_G3H_P3V42G3H 59
=PPVIN_S0_P1V05S5 66
=PPVIN_PBUS_KBDLED 9
=PPVIN_S5_FWPWRSW 36
=PPVIN_S5_BKL

45 =PPVIN_S5_CPU_IMVP_ISNS
PPBUS_CPU_IMVP_ISNS 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=6V
MAKE_BASE=TRUE
=PPVIN_S5_CPU_IMVP 61

59 =PP18V5_DCIN_CONN
PPDCIN_G3H 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPDCIN_S5_CHGR 60

59 =PP3V42_G3H_REG
PP3V42_G3H 7 42
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PP3V42_G3H_SMCUSBMUX 39
=PP3V42_G3H_SMBUS_SMC_BSA 44
=PP3V42_G3H_LIDSWITCH 40
=PP3V3_S5_SMC 41 42 51
=PP3V3_S5_LPCPLUS 43
=PPVIN_S5_SMCVREF 42
=PP3V42_G3H_PWRCTL 67
=PP3V42_G3H_CHGR 60
=PP3V3_S5_RTC_D 25
=PP3V42_G3H_BATT 59
=PP3V42_G3H_TPAD 49
=PP3V42_G3H_BMON_ISNS 45
=PP3V42_G3H_CPUCOREISNS 45

5V Rails

62 =PP5V_S3_REG
PP5V_S3 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_SYSLED 42
=PP5V_S3_BTCAMERA 30
=PP5V_S3_WLAN 30
=PP5V_S3_IR 40
=PP5V_S3_DDRREG 63
=PP5V_S3_GPUVCORE 77
=PP5V_S3_RTUSB 39 98
=PP5V_S3_TPAD 50
=PP5V_S3_P1V05S0FET 68
=PP5V_S3_MCPDDRFET 68
=PP5V_S3_VTTCLAMP 68
=PP5V_S3_AUDIO_PWR 9

64 =PP5V_S0_REG
PP5V_S0 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_FAN_LT 7 48
=PP5V_S0_FAN_RT 48
=PP5V_S0_CPU_IMVP 61
=PP5V_S0_CPUVTTS0 65
=PP5V_S0GPU_P1V1P1V8_GPU 83
=PP5V_S0_LPCPLUS 43
=PP5V_S0_ODD 38
=PP5V_S0_HDD 38
=PPVIN_PP5V_KBDLED 9

Chipset "VCore" Rails

61 =PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU 11 12 45

64 =PPMCPCORE_S0_REG
PPVCORE_S0_MCP 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP 22 23 45

3.3V-2.5V Rails

62 =PP3V3_S5_REG
PP3V3_S5 7 96
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_ROM 43 52
=PP3V3_S5_MEMRESET 29
=PP3V3_S3_P3V3S3FET 68
=PP3V3_S0_LCD 78
=PP3V3_S0_P3V3S0FET 68
=PP3V3_GPU_P3V3GPUFET 68
=PP3V3_S5_PWRCTL 67
=PP3V3_S5_P1V05FET 68
=PP3V3_S5_MCP 22 23
=PP3V3_S5_MCP_GPIO 18 20
=PP3V3_FW_LATEVG_ACTIVE 36
=PP3V3_S5_MCPPWRGD 25
=PP3V3_FW_LATEVG 37
=PP3V3_S5_P1V05ENETFET 33
=PP3V3_S5_P3V3ENETFET 33
=PP3V3_S5_DP_PORT_PWR 82

68 =PP3V3_S3_FET
PP3V3_S3 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_GMUX 84
=PP3V3_S3_BT 30
=PP3V3_S3_P1V8S0 66
=PP3V3_S3_SMBUS_SMC_A_S3 44
=PP3V3_S3_SMS 8 51
=PP3V3_S3_TPAD 49
=PP3V3_S3_SMS 8 51
=PP3V3_S3_WLAN 30
=PP3V3_S3_MCP_GPIO 21
=PP3V3_S3_VREFMRGN 26
=PP3V3_S3_SMBUS_SMC_MGMT 44
=PP3V3_S3_EXCARD 31
=PP3V3_S3_P1V5EXPS0 66

68 =PP3V3_S0_FET
PP3V3_S0 7 9 96
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_LPCPLUS 43
=PP3V3_S0_SMC 42
=PP3V3_S0_SMBUS_SMC_B_S0 44
=PP3V3_S0_MCPDDRISNS 46
=PP3V3_S0_GPU1V8ISNS 46
=PP3V3_S0_CPUTHMSNS 47
=PP3V3_S0_GPUTHMSNS 47
=PP3V3_S0_FAN_LT 48
=PP3V3_S0_FAN_RT 48
=PP3V3_S0_IMVP 61
=PP3V3_S0_PWRCTL 67
=PP3V3_S0_DDC_LCD 7 75 78
=PP3V3_S0_XDP 6 8 13
=PP3V3_S0_MCPCOREISNS 46
=PP3V3_S0_XDP 6 8 13
=PPSPD_S0_MEM_A 27
=PPSPD_S0_MEM_B 28
=PP3V3_S0_SMBUS_MCP_0 44
=PP3V3_S0_GMUX 84
=PP3V3_S0_DPMUX 81
=PP3V3_S0_DPCONN 82
=PP3V3_S0_P1V2P2V5 87
=PP3V3_S0_MCP_GPIO 18 19 21
=PP3V3_S0_HDCPROM 24
=PP3V3R1V5_S0_MCP_HDA 21 23
=PP3V3_S0_MCP_PLL_UF 23
=PP3V3_S0_MCP_VPLL_UF 24
=PP3V3_S0_MCP_DAC_UF 24
=PP3V3_S0_MCP 21 22 23
=PP3V3_S0_AUDIO 53 57 58
=PP3V3_S0_ODD 38
=PP3V3_S0_VMON 67
=PP3V3_S0_SMBUS_MCP_1 44
=PP3V3_S0_REMTHMSNS 47
=PP3V3_S0_EXCARD 31
=PP3V3_S0_LVDSDDCMUX 81
=PP3V3_S0_BATTCHARGERTMPSNSR 47
=PP3V3_GPU_SMBUS_SMC_0_S0 44
=PP3V3_S0_TPAD 50
=PP3V3_S0_MCP_PLL_VLDO 66
=PP3V3_FW_FWPHY 35 37
=PP3V3_FW_P1V0FW 66

87 =PP2V5_S0_REG
PP2V5_S0 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=2.5V
MAKE_BASE=TRUE
=PP2V5_S0_GMUX 84

87 =PP1V2_S0_REG
PP1V2_S0 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE
=PP1V2_S0_GMUX 84

1.8V/DDR 1.5V Rails

66 =PP1V8_S0_REG
500 mA max supply
PP1V8_S0 7
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
190 mA =PP3V3R1V8_S0_MCP_IFP_VDD 18 24
=PP1V8_S0_MCP_PLL_VLDO 66

63 =PPDDR_S3_REG
PP1V8R1V5_S3 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V8R1V5_S0_MCP_FET 68
=PPVIN_S0_DDRREG_LDO 63
=PP1V5_S3_MEM_A 27
=PP1V5_S3_MEM_B 28
=PP1V5_S3_MEMRESET 29

68 =PP1V8R1V5_S0_FET
PP1V8R1V5_S0 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
4771 mA =PPMCPDDR_ISNS_R 46
130 mA =PP1V5_S0_CPU 11 12
500 mA =PP1V5_S0_VMON 67

66 38 =PP1V5_EXP_S0
PP1V5_EXP_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_EXCARD 31

23 16 =PP1V8R1V5_S0_MCP_MEM
PPMCPDDR_ISNS 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_MEM_A 27
=PP1V5_S0_MEM_B 28
=PPMCPDDR_ISNS 46

68 66 =PP1V05_S0_FET
PP1V05_S0 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
1034 mA
=PP1V05_S0_MCP_AVDD_UF 23
=PP1V05_S0_MCP_PEX_DVDD 8 23
=PP1V05_S0_MCP_SATA_DVDD 8 23
=PP1V05_S0_MCP_HDMI_VDD 18 24
=PP1V05_S0_VMON 67
=PP1V05_S0_MCP_PLL_PEX_UF 23

PP1V05_S0_MCP_PLL_UF
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
=PP1V05_S0_MCP_PLL_UF 23 66

23 8 =PP1V05_S0_MCP_PEX_DVDD
=PP1V05_S0_MCP_PEX_DVDD0 17
=PP1V05_S0_MCP_PEX_DVDD1 17

23 PP1V05_S0_MCP_PEX_AVDD
MAKE_BASE=TRUE
=PP1V05_S0_MCP_PEX_AVDD0 17
=PP1V05_S0_MCP_PEX_AVDD1 17

23 8 =PP1V05_S0_MCP_SATA_DVDD
=PP1V05_S0_MCP_SATA_DVDD0 20

23 PP1V05_S0_MCP_SATA_AVDD
MAKE_BASE=TRUE
=PP1V05_S0_MCP_SATA_AVDD0 20

(1.1V for A01)
66 =PP1V05_S5_MCP
PP1V2R1V05_S5 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
241 mA max load
105 mA/241 mA =PP1V05_S5_MCP_VDD_AUXC 22 23
139 mA/ 0 mA =PP1V05_ENET_P1V05ENETFET 33
=PP1V05_S5_P1V05S0FET 68

65 =PPCPUVTT_S0_REG
PPCPUVTT_S0 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
5300 mA
4500 mA =PP1V05_S0_CPU 6 10 11 12 13 61
=PP1V05_S0_SMC_LS 42
1182 mA =PP1V05_S0_MCP_FSB 9 14 22 23

63 26 =PPVTT_S3_DDR_BUF
PPVTTDDR_S3 7
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

63 =PPVTT_S0_DDR_LDO
PP0V9R0V75_S0_DDRVTT 7
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V75_S0_MEM_VTT_A 27
=PP0V75_S0_MEM_VTT_B 28
=PPVTT_S0_VTTCLAMP 68
OR 0.75V

ENET Rails

33 =PP1V05_ENET_FET
PP1V2R1V05_ENET 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_ENET_MCP_PLL_MAC 23
=PP1V05_ENET_MCP_RMGT 18 23
=PP1V05_ENET_PHY 32

33 =PP3V3_ENET_FET
PP3V3_ENET_PHY 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_MCP_RMGT 18 23
=PP3V3_ENET_PHY 32

"FW" (FireWire) Rails

36 =PPVOUT_FW_FWPWRSW
PPBUS_FW_FWBOOST
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=6V
MAKE_BASE=TRUE
=PPVIN_PFWBOOST 66

66 =PFWBOOST_REG
PP10V_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=10V
MAKE_BASE=TRUE
=PPBOOST_FW_FWPWRSW_F 36

36 =PPBOOST_S5_FW_FET
PPVP_FW 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=10V
MAKE_BASE=TRUE
=PPVP_FW_PORT1 37
=PPVP_FW_PHY_CPS_FET 37

66 =PP1V0_FW_REG
PP1V0_FW 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
MAKE_BASE=TRUE
=PP1V0_FW_FWPHY 35

"GPU" Rails

68 =PP3V3_S0GPU_FET
PP3V3_S0GPU 7
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_VDD33 6 74 75
=PP3V3_GPU_MIO 74 75
=PP3V3_GPU_LVDS_DDC 81
=PP3V3_GPU_PWRCTL 67
=PP3V3_GPU_VCORELOGIC 77
=PP3V3_GPU_P1V8S0 66

83 =PP1V1_S0GPU_REG
PP1V1_S0GPU 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.1V
MAKE_BASE=TRUE
=PP1V1_GPU_PEX_IOVDDQ 69
=PP1V1_GPU_PEX_IOVDD 69
=PP1V1_GPU_PEX_PLLXVDD 69
=PP1V1_GPU_PLLVDD 74
=PP1V1_GPU_H_PLLVDD 74
=PP1V1_GPU_VID_PLLVDD 74
=PP1V1_GPU_FBPLLAVDD 71
=PP1V1_GPU_IFPCD_IOVDD 76

66 =PP1V8_GPUIFPX_REG
PP1V8_GPUIFPX 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_GPU_IFPX 76

46 =PP1V8_S0GPU_ISNS
PP1V8_S0GPU_ISNS 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_GPU_FB_VDD 72 73 79 80
=PP1V8_GPU_FB_VDDQ 9 72 73 79 80
=PP1V8_GPU_FBVDDQ 70
=PP1V8_GPU_FBIO 71

77 45 =PPVCORE_GPU_REG
PPVCORE_GPU 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE
=PPVCORE_GPU 70

83 =PP1V8_GPU_REG
PP1V8_S0GPU_ISNS_R 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PP1V8_S0GPU_ISNS_R 46

Power Aliases

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

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SCALE: NONE	SHT 8 OF 98	

Thermal Module Holes

ZT0982 STDOFF-4.50D.98H-1.1-3.48-TH — Left CPU TM Hole
ZT0983 STDOFF-4.50D.98H-1.1-3.48-TH — Right CPU TM Hole
ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH — Top GPU Right TM Hole
ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH — Bottom Left GPU TM Hole
ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0985 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0986 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND_BATT_CHGND
ZT0945 3R2P5 — GND_CHASSIS_USB
ZT0932 3R2P5 — GND_CHASSIS_RIGHTHS
ZT0960 3R2P5 — GND_CHASSIS_SATA
ZT0971 3R2P5 — GND_CHASSIS_TPAD
ZT0965 3R2P5 — GND_CHASSIS_CLUTCH
ZT0940 3R2P5 — GND_CHASSIS_LVDS
ZT0970 3R2P5 — GND_CHASSIS_DIMM

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa

=PP1V05_S0_MCP_FSB
R0950 220 5% 1/16W MF-LF 402 — NO STUFF
R0960 62 5% 1/16W MF-LF 402 — NO STUFF
R0970 200 5% 1/16W MF-LF 402 — NO STUFF
R0980 150 1% 1/16W MF-LF 402 — NO STUFF
R0990 150 1% 1/16W MF-LF 402 — NO STUFF
CPU_DPRSTP_L
FSB_BREQ0_L
FSB_CPURST_L
CPU_INTR
CPU_NMI

Bosses for Flex Protector Bracket

ZT0931 STDOFF-4.0OD3.0H-SM
ZT0934 STDOFF-4.0OD3.0H-SM
ZT0957 4.0OD1.65H-M1.6X0.35
ZT0958 4.0OD1.65H-M1.6X0.35
ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH

R0900 10 1% 1/16W MF-LF 402
R0901 10 1% 1/16W MF-LF 402
=PP1V8_GPU_FB_VDDQ
GPU_FB_A_VREF_DIV — =PP1V8_GPU_FB_VREF_A
GPU_FB_B_VREF_DIV — =PP1V8_GPU_FB_VREF_B

KBDLED_PBUS
R0998 0 5% 1/10W MF-LF 603
=PPVIN_PBUS_KBDLED — PP5VR8V4_KBDLED (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=8.4V, MAKE_BASE=TRUE) — =PPVIN_S0_KBDLED
KBDLED_5V
R0999 0 5% 1/10W MF-LF 603
=PPVIN_PP5V_KBDLED

SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0901 2.0DIA-TALL-EMI-MLB-M97-M98
SH0920 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0923 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0924 2.0DIA-TALL-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98
SH0917 2.0DIA-TALL-EMI-MLB-M97-M98
SH0918 2.0DIA-TALL-EMI-MLB-M97-M98
SH0919 2.0DIA-TALL-EMI-MLB-M97-M98
SH0930 2.0DIA-TALL-EMI-MLB-M97-M98
SH0921 2.0DIA-TALL-EMI-MLB-M97-M98
SH0931 2.0DIA-TALL-EMI-MLB-M97-M98
SH0922 2.0DIA-TALL-EMI-MLB-M97-M98
SH0932 2.0DIA-TALL-EMI-MLB-M97-M98
SH0934 2.0DIA-TALL-EMI-MLB-M97-M98
SH0933 2.0DIA-TALL-EMI-MLB-M97-M98
SH0935 2.0DIA-TALL-EMI-MLB-M97-M98

CPU signals

TP_IMVP6_CLKEN_L — VR_PWRGD_CLKEN_L
CPU_VID<0..6> — IMVP6_VID<0..6>
CPU_BSEL<0..2> — =MCP_BSEL<0..2>
MEM_VTT_EN — =DDRVTT_EN
TP_SPI_CS1_R_L_USE_MLB — =SPI_CS1_R_L_USE_MLB

GPU signals

PEG_D2R_P<0..15> — =PEG_D2R_P<0..15>
PEG_D2R_N<0..15> — =PEG_D2R_N<0..15>
PEG_R2D_C_P<0..15> — =PEG_R2D_C_P<0..15>
PEG_R2D_C_N<0..15> — =PEG_R2D_C_N<0..15>

LCD_BKLT_EN — LVDS_BKL_ON
DP_IG_ML_P<3> — =MCP_HDMI_TXC_P
DP_IG_ML_N<3> — =MCP_HDMI_TXC_N
DP_IG_ML_P<2..0> — =MCP_HDMI_TXD_P<0..2>
DP_IG_ML_N<2..0> — =MCP_HDMI_TXD_N<0..2>
DP_IG_DDC_CLK — =MCP_HDMI_DDC_CLK
DP_IG_DDC_DATA — =MCP_HDMI_DDC_DATA
DP_IG_HPD — =MCP_HDMI_HPD

GMUX ALIASES

PM_ALL_GPU_PGOOD — ALL_EG_PGOOD
TP_LVDS_MUX_SEL_EG — LVDS_MUX_SEL_EG
EG_RESET_L — GPU_RESET_L
JTAG_GMUX_TDI — GMUX_JTAG_TDI
JTAG_GMUX_TMS — GMUX_JTAG_TMS
JTAG_GMUX_TDO — GMUX_JTAG_TDO
GMUX_INT — =DVI_HPD_GMUX_INT
LVDS_IG_BKL_ON — IG_BKLT_EN
LVDS_IG_PANEL_PWR — IG_LCD_PWR_EN

=PP1V05_S0_MCP_SATA_DVDD1
=PP1V05_S0_MCP_SATA_AVDD1

=P1V5_EXP_S0_EN — PP3V3_S0

MCP_MII_PD
R0930 47K 5% 1/16W MF-LF 402
=MCP_MII_RXER
=MCP_MII_CRS
=MCP_MII_COL

Digital Ground
GND (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=0V)

TP_USB_EXTDP — USB_EXTD_P
TP_USB_EXTDN — USB_EXTD_N
TP_USB_MINIP — USB_MINI_P
TP_USB_MININ — USB_MINI_N
TP_MEM_A_A<15> — MEM_A_A<15>
TP_MEM_B_A<15> — MEM_B_A<15>
TP_CPU_PECI_MCP — CPU_PECI_MCP
TP_LVDS_IG_B_CLKP — LVDS_IG_B_CLK_P
TP_LVDS_IG_B_CLKN — LVDS_IG_B_CLK_N
TP_LVDS_IG_BKL_PWM — LVDS_IG_BKL_PWM

NC_LVDS_IG_A_DATAP<3> — LVDS_IG_A_DATA_P<3>
NC_LVDS_IG_A_DATAN<3> — LVDS_IG_A_DATA_N<3>
NC_LVDS_IG_B_DATAP<3> — LVDS_IG_B_DATA_P<3>
NC_LVDS_IG_B_DATAN<3> — LVDS_IG_B_DATA_N<3>

AUDIO ALIASES

HDA_BITCLK — HDA_BIT_CLK
XW0900 PP5V_S3_AUDIO (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)
=PP5V_S3_AUDIO_PWR
XW0901 PP5V_S3_AUDIO_AMP (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)
R0902 10K 5% 1/16W MF-LF 402 — AUD_IPHS_SWITCH_EN
R0903 0 5% 1/16W MF-LF 402 — MCP_SPKR — SMC_MCP_SAFE_MODE

ETHERNET ALIASES

=P3V3ENET_EN — PM_SLP_RMGT_L
=P1V05ENET_EN
=PP3V3_ENET_PHY_VDDREG — TP_PP3V3_ENET_PHY_VDDREG
=RTL8211_REGOUT — NC_RTL8211_REGOUT
=RTL8211_ENSWREG

MCP79 PCIe PRSNT# Straps

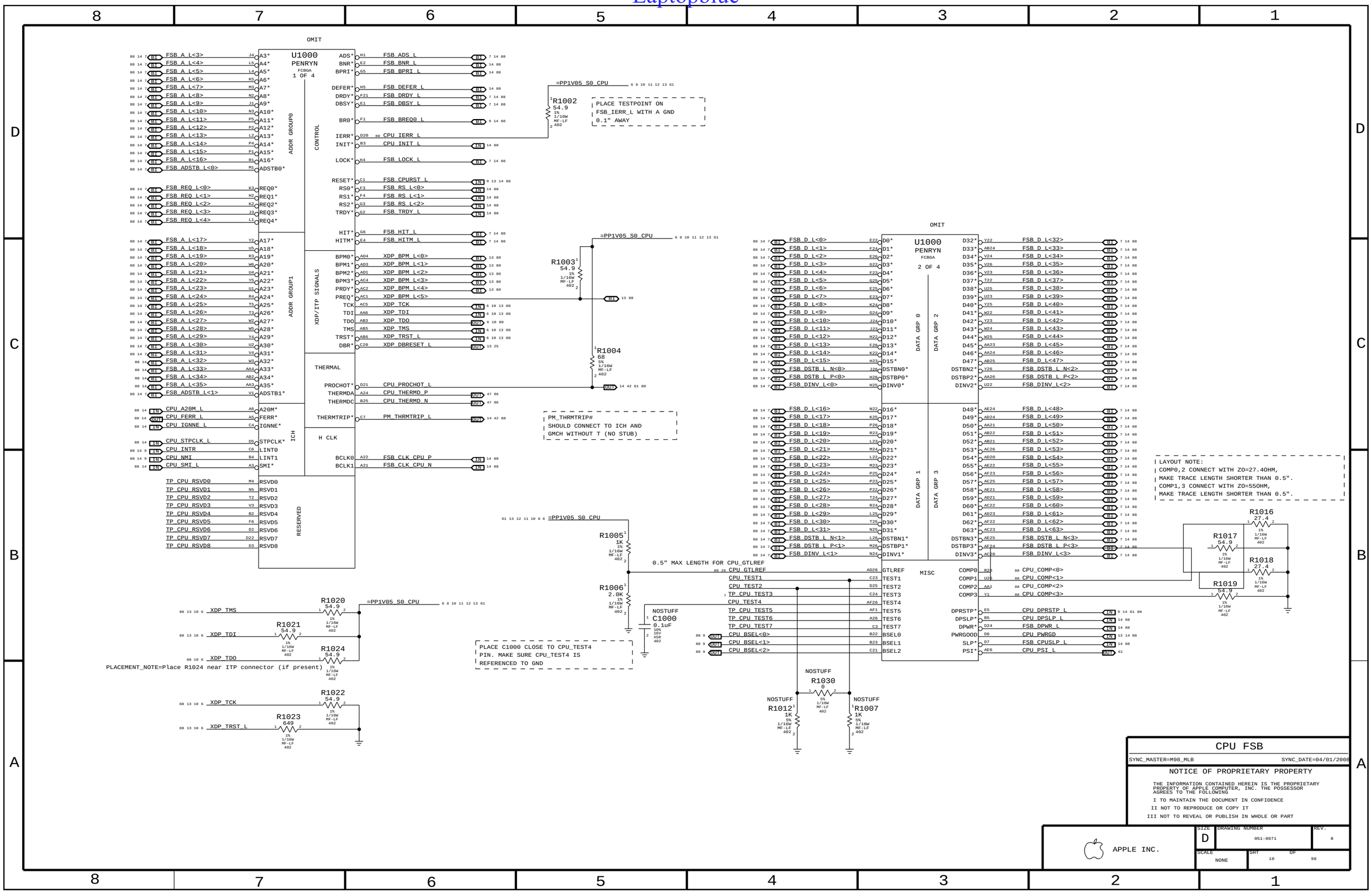
R0925 0 5% 1/16W MF-LF 402 — PCIE_FW_PRSNT_L (MAKE_BASE=TRUE) — OUT
NO STUFF
R0927 0 5% 1/16W MF-LF 402 — PEG_PRSNT_L (MAKE_BASE=TRUE) — OUT
R0926 0 5% 1/16W MF-LF 402 — EG_CLKREQ_OUT_L — IN

Signal Aliases

SYNC_MASTER=K20_MLB — SYNC_DATE=09/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 9 OF 98	



CPU FSB

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 10 OF 98	

(CPU CORE POWER)

=PPVCORE_S0_CPU 8 11 12 45

Standard Voltage:

44.0 A (Design Target)

41.0 A (HFM)
30.4 A (LFM)
25.5 A (SuperLFM)

27.4 A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)

27.4 A (Sleep HFM)
16.8 A (Sleep SuperLFM)

25.0 A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)

11.5 A (Deeper Sleep)

9.4 A (Enhanced Deeper Sleep)

Low Voltage:

23.0 A (Design Target)

21.0 A (HFM)
18.7 A (LFM)
TBD A (SuperLFM)

TBD A (Auto-Halt/Stop-Grant HFM)
TBD A (Auto-Halt/Stop-Grant SuperLFM)

TBD A (Sleep HFM)
TBD A (Sleep SuperLFM)

TBD A (Deep Sleep HFM)
TBD A (Deep Sleep SuperLFM)

TBD A (Deeper Sleep)

TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

17.0 A (Design Target)

TBD A (HFM)
TBD A (LFM)

TBD A (Auto-Halt/Stop-Grant HFM)
TBD A (Auto-Halt/Stop-Grant LFM)

TBD A (Sleep HFM)
TBD A (Sleep LFM)

TBD A (Deep Sleep HFM)
TBD A (Deep Sleep LFM)

TBD A (Deeper Sleep)

TBD A (Enhanced Deeper Sleep)

OMIT
U1000
PENRYN
FCBGA
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VCC: A7, A9, A10, A12, A13, A15, A17, A18, A20, B7, B9, B10, B12, B14, B15, B17, B18, B20, C9, C10, C12, C13, C15, C17, C18, D9, D10, D12, D14, D15, D17, D18, E7, E9, E10, E12, E13, E15, E17, E18, E20, F7, F9, F10, F12, F14, F15, F17, F18, F20, AA7, AA9, AA10, AA12, AA13, AA15, AA17, AA18, AA20, AB9, AC10, AB10, AB12, AB14, AB15, AB17, AB18

VCC: AB20, AB7, AC7, AC9, AC12, AC13, AC15, AC17, AC18, AD7, AD9, AD10, AD12, AD14, AD15, AD17, AD18, AE9, AE10, AE12, AE13, AE15, AE17, AE18, AE20, AF9, AF10, AF12, AF14, AF15, AF17, AF18, AF20

(CPU IO POWER 1.05V)

=PP1V05_S0_CPU 6 8 10 12 13 61

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21, V6, J6, K6, M6, J21, K21, M21, N21, N6, R21, R6, T21, T6, V21, W21

(CPU INTERNAL PLL POWER 1.5V)

=PP1V5_S0_CPU 8 12

130 mA

VCCA: B26, C26

VID0	AD6	CPU_VID<0>	OUT 9 88
VID1	AF5	CPU_VID<1>	OUT 9 88
VID2	AE5	CPU_VID<2>	OUT 9 88
VID3	AF4	CPU_VID<3>	OUT 9 88
VID4	AE3	CPU_VID<4>	OUT 9 88
VID5	AF3	CPU_VID<5>	OUT 9 88
VID6	AE2	CPU_VID<6>	OUT 9 88

VCCSENSE AF7 CPU_VCCSENSE_P OUT 61 88

VSSSENSE AE7 CPU_VCCSENSE_N OUT 61 88

=PPVCORE_S0_CPU 8 11 12 45

R1100
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
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VSS: A4, A8, A11, A14, A16, A19, A23, AF2, B6, B8, B11, B13, B16, B19, B21, B24, C5, C8, C11, C14, C16, C19, C2, C22, C25, D1, D4, D8, D11, D13, D16, D19, D23, D26, E3, E6, E8, E11, E14, E16, E19, E21, E24, F5, F8, F11, F13, F16, F19, F2, F22, F25, G4, G1, G23, G26, H3, H6, H21, H24, J2, J5, J22, J25, K1, K4, K23, K26, L3, L6, L21, L24, M2, M5, M22, M25, N1, N4, N23, N26, P3, B1

VSS: P6, P21, P24, R2, R5, R22, R25, T1, T4, T23, T26, U3, U6, U21, U24, V2, V5, V22, V25, W1, W4, W23, W26, Y3, Y6, Y21, Y24, AA2, AA5, AA8, AA11, AA14, AA16, AA19, AA22, AA25, AB1, AB4, AB8, AB11, AB13, AB16, AB19, AB23, AB26, AC3, AC6, AC8, AC11, AC14, AC16, AC19, AC21, AC24, AD2, AD5, AD8, AD11, AD13, AD16, AD19, AD22, AD25, AE1, AE4, AE8, AE11, AE14, AE16, AE19, AE23, AE26, A2, AF6, AF8, AF11, AF13, AF16, AF19, AF21, A25, AF25

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

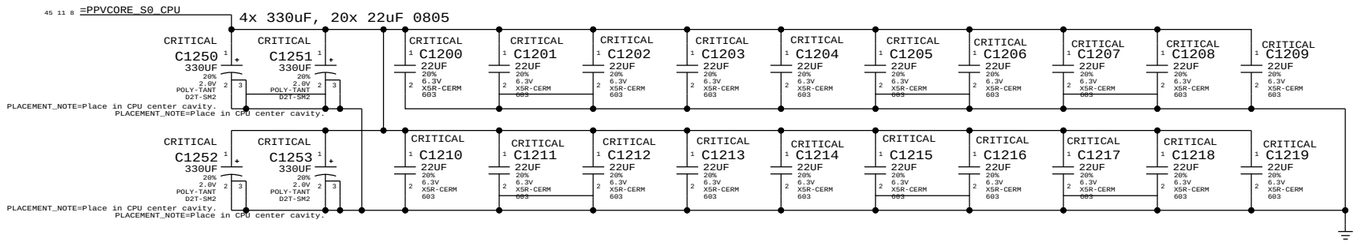
CPU Power & Ground

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

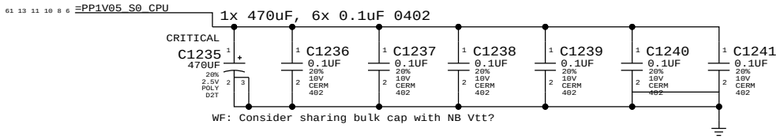
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 11 OF 98	

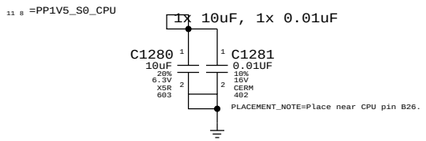
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

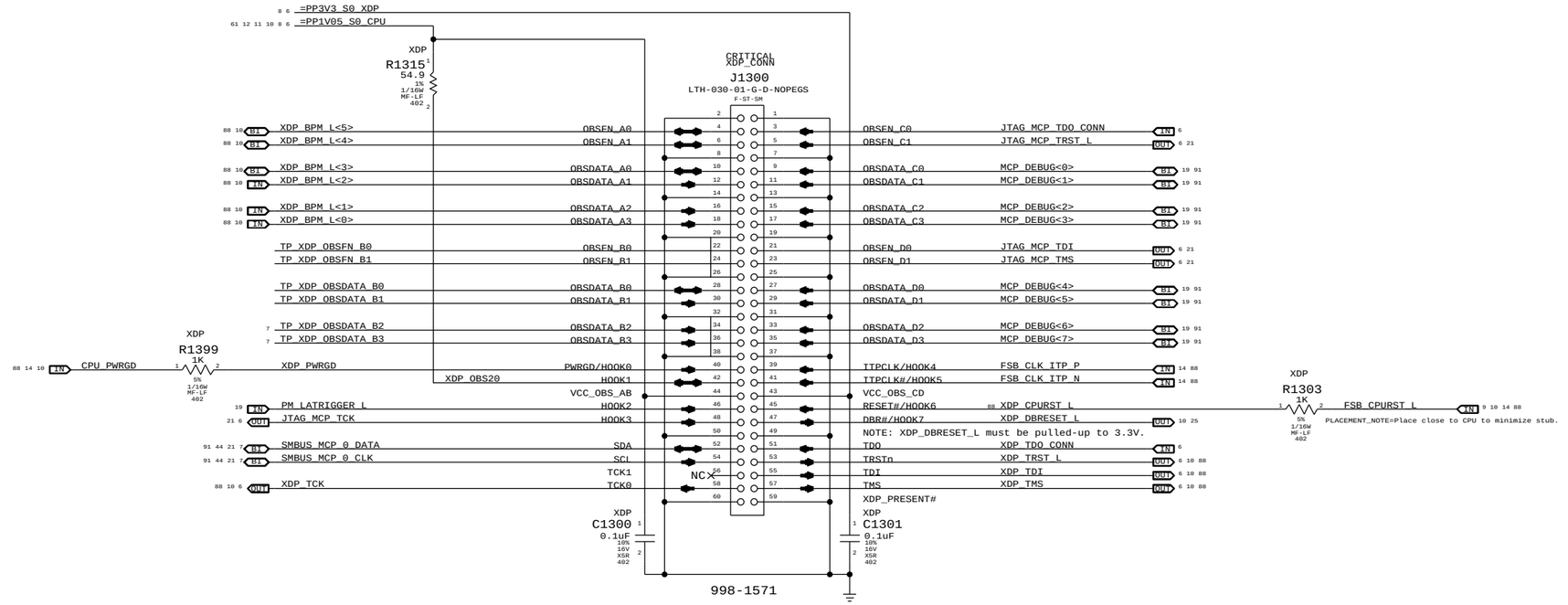
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 12 OF 98	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port(MiniXDP)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 13 OF 98	

OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#	
FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#	
FSB_DINV_L<0>	V41	CPU_DBI0#	
FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#	
FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#	
FSB_DINV_L<1>	V35	CPU_DBI1#	
FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#	
FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#	
FSB_DINV_L<2>	N35	CPU_DBI2#	
FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#	
FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#	
FSB_DINV_L<3>	J41	CPU_DBI3#	
FSB_A_L<3>	AC34	CPU_A3#	
FSB_A_L<4>	AE38	CPU_A4#	
FSB_A_L<5>	AE34	CPU_A5#	
FSB_A_L<6>	AC37	CPU_A6#	
FSB_A_L<7>	AE37	CPU_A7#	
FSB_A_L<8>	AE35	CPU_A8#	
FSB_A_L<9>	AB35	CPU_A9#	
FSB_A_L<10>	AF35	CPU_A10#	
FSB_A_L<11>	AG35	CPU_A11#	
FSB_A_L<12>	AG39	CPU_A12#	
FSB_A_L<13>	AE33	CPU_A13#	
FSB_A_L<14>	AG37	CPU_A14#	
FSB_A_L<15>	AG38	CPU_A15#	
FSB_A_L<16>	AG34	CPU_A16#	
FSB_A_L<17>	AN38	CPU_A17#	
FSB_A_L<18>	AL39	CPU_A18#	
FSB_A_L<19>	AG33	CPU_A19#	
FSB_A_L<20>	AL33	CPU_A20#	
FSB_A_L<21>	AJ33	CPU_A21#	
FSB_A_L<22>	AN36	CPU_A22#	
FSB_A_L<23>	AJ35	CPU_A23#	
FSB_A_L<24>	AJ37	CPU_A24#	
FSB_A_L<25>	AJ36	CPU_A25#	
FSB_A_L<26>	AJ38	CPU_A26#	
FSB_A_L<27>	AL37	CPU_A27#	
FSB_A_L<28>	AL34	CPU_A28#	
FSB_A_L<29>	AN37	CPU_A29#	
FSB_A_L<30>	AJ34	CPU_A30#	
FSB_A_L<31>	AL38	CPU_A31#	
FSB_A_L<32>	AL35	CPU_A32#	
FSB_A_L<33>	AN34	CPU_A33#	
FSB_A_L<34>	AR39	CPU_A34#	
FSB_A_L<35>	AN35	CPU_A35#	
FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#	
FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#	
FSB_REQ_L<0>	AC38	CPU_REQ0#	
FSB_REQ_L<1>	AA33	CPU_REQ1#	
FSB_REQ_L<2>	AC39	CPU_REQ2#	
FSB_REQ_L<3>	AC33	CPU_REQ3#	
FSB_REQ_L<4>	AC35	CPU_REQ4#	
FSB_ADS_L	AD42	CPU_ADS#	
FSB_BNR_L	AD43	CPU_BNR#	
FSB_BREQ0_L	AE40	CPU_BR0#	
FSB_BREQ1_L	AL32	CPU_BR1#	
FSB_DBSY_L	AD39	CPU_DBSY#	
FSB_DRDY_L	AD41	CPU_DRDY#	
FSB_HIT_L	AB42	CPU_HIT#	
FSB_HITM_L	AD40	CPU_HITM#	
FSB_LOCK_L	AC43	CPU_LOCK#	
FSB_TRDY_L	AE41	CPU_TRDY#	
CPU_PECI_MCP	E41	CPU_PECI	
CPU_PROCHOT_L	AJ41	CPU_PROCHOT#	
	AG43	CPU_THERMTRIP#	
	AH40	CPU_FERR#	
(MCP_BSEL<2>)	F42	CPU_BSEL2	
(MCP_BSEL<1>)	D42	CPU_BSEL1	
(MCP_BSEL<0>)	F41	CPU_BSEL0	
FSB_RS_L<0>	AC41	CPU_RS0#	
FSB_RS_L<1>	AB41	CPU_RS1#	
FSB_RS_L<2>	AC42	CPU_RS2#	
PP1V05_S0_MCP_PLL_FSB	AG27	+V_DLL_DLCELL_AVDD	206 mA
	AH27	+V_PLL_MCLK	20 mA
	AG28	+V_PLL_FSB	29 mA
	AH28	+V_PLL_CPU	15 mA
MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AM42	CPU_COMP_GND	

PP1V05_S0_MCP_PLL_FSB: 270 mA (A01)

CPU_D0#	Y43	FSB_D_L<0>	
CPU_D1#	W42	FSB_D_L<1>	
CPU_D2#	Y40	FSB_D_L<2>	
CPU_D3#	W41	FSB_D_L<3>	
CPU_D4#	Y39	FSB_D_L<4>	
CPU_D5#	V42	FSB_D_L<5>	
CPU_D6#	Y41	FSB_D_L<6>	
CPU_D7#	Y42	FSB_D_L<7>	
CPU_D8#	P42	FSB_D_L<8>	
CPU_D9#	U41	FSB_D_L<9>	
CPU_D10#	R42	FSB_D_L<10>	
CPU_D11#	T39	FSB_D_L<11>	
CPU_D12#	T42	FSB_D_L<12>	
CPU_D13#	T41	FSB_D_L<13>	
CPU_D14#	R41	FSB_D_L<14>	
CPU_D15#	T43	FSB_D_L<15>	
CPU_D16#	W35	FSB_D_L<16>	
CPU_D17#	AA37	FSB_D_L<17>	
CPU_D18#	W33	FSB_D_L<18>	
CPU_D19#	W34	FSB_D_L<19>	
CPU_D20#	AA36	FSB_D_L<20>	
CPU_D21#	AA34	FSB_D_L<21>	
CPU_D22#	AA38	FSB_D_L<22>	
CPU_D23#	AA35	FSB_D_L<23>	
CPU_D24#	U38	FSB_D_L<24>	
CPU_D25#	U36	FSB_D_L<25>	
CPU_D26#	U35	FSB_D_L<26>	
CPU_D27#	U33	FSB_D_L<27>	
CPU_D28#	U34	FSB_D_L<28>	
CPU_D29#	W38	FSB_D_L<29>	
CPU_D30#	R33	FSB_D_L<30>	
CPU_D31#	U37	FSB_D_L<31>	
CPU_D32#	N34	FSB_D_L<32>	
CPU_D33#	N33	FSB_D_L<33>	
CPU_D34#	R34	FSB_D_L<34>	
CPU_D35#	R35	FSB_D_L<35>	
CPU_D36#	P35	FSB_D_L<36>	
CPU_D37#	R39	FSB_D_L<37>	
CPU_D38#	R37	FSB_D_L<38>	
CPU_D39#	R38	FSB_D_L<39>	
CPU_D40#	L37	FSB_D_L<40>	
CPU_D41#	L39	FSB_D_L<41>	
CPU_D42#	L38	FSB_D_L<42>	
CPU_D43#	N36	FSB_D_L<43>	
CPU_D44#	N38	FSB_D_L<44>	
CPU_D45#	J39	FSB_D_L<45>	
CPU_D46#	J38	FSB_D_L<46>	
CPU_D47#	J37	FSB_D_L<47>	
CPU_D48#	L42	FSB_D_L<48>	
CPU_D49#	M42	FSB_D_L<49>	
CPU_D50#	P41	FSB_D_L<50>	
CPU_D51#	N41	FSB_D_L<51>	
CPU_D52#	N40	FSB_D_L<52>	
CPU_D53#	M40	FSB_D_L<53>	
CPU_D54#	H40	FSB_D_L<54>	
CPU_D55#	K42	FSB_D_L<55>	
CPU_D56#	H41	FSB_D_L<56>	
CPU_D57#	L41	FSB_D_L<57>	
CPU_D58#	H43	FSB_D_L<58>	
CPU_D59#	H42	FSB_D_L<59>	
CPU_D60#	K41	FSB_D_L<60>	
CPU_D61#	J40	FSB_D_L<61>	
CPU_D62#	H39	FSB_D_L<62>	
CPU_D63#	M43	FSB_D_L<63>	
CPU_BPRI#	AA41	FSB_BPRI_L	
CPU_DEFER#	AA40	FSB_DEFER_L	
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P	
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N	
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P	
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N	
BCLK_OUT_NB_P	AL41	FSB_CLK_MCP_P	
BCLK_OUT_NB_N	AK42	FSB_CLK_MCP_N	
BCLK_IN_N	AK41		
BCLK_IN_P	AJ40		
CPU_A20M#	AF41	CPU_A20M_L	
CPU_IGNNE#	AH39	CPU_IGNNE_L	
CPU_INIT#	AH42	CPU_INIT_L	
CPU_INTR	AF42	CPU_INTR	
CPU_NMI	AG41	CPU_NMI	
CPU_SMI#	AH41	CPU_SMI_L	
CPU_PWRGD	AH43	CPU_PWRGD	
CPU_RESET#	H38	FSB_CPURST_L	
CPU_SLP#	AM33	FSB_CPUSLP_L	
CPU_DPSLP#	AN33	CPU_DPSLP_L	
CPU_DPWR#	AM32	FSB_DPWR_L	
CPU_STPCLK#	AG42	CPU_STPCLK_L	
CPU_DPRSTP#	AN32	CPU_DPRSTP_L	

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB
R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402
PM_THRMTRIP_L
CPU_FERR_L
NO STUFF R1420 1K 5% 1/16W MF-LF 402
NO STUFF R1421 1K 5% 1/16W MF-LF 402
NO STUFF R1422 1K 5% 1/16W MF-LF 402
=MCP_BSEL<2>
=MCP_BSEL<1>
=MCP_BSEL<0>
R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402
=PP1V05_S0_MCP_FSB
NO STUFF R1440 150 5% 1/16W MF-LF 402

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MCP CPU Interface

SYNC_MASTER=T18_MLB
SYNC_DATE=06/06/2008

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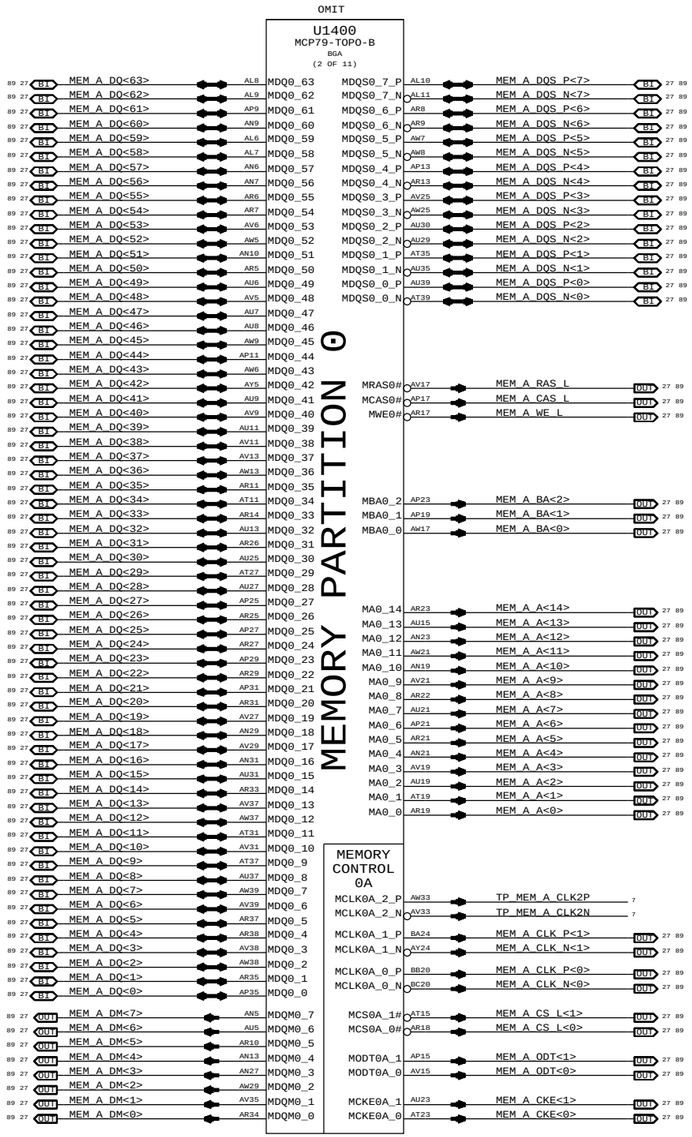
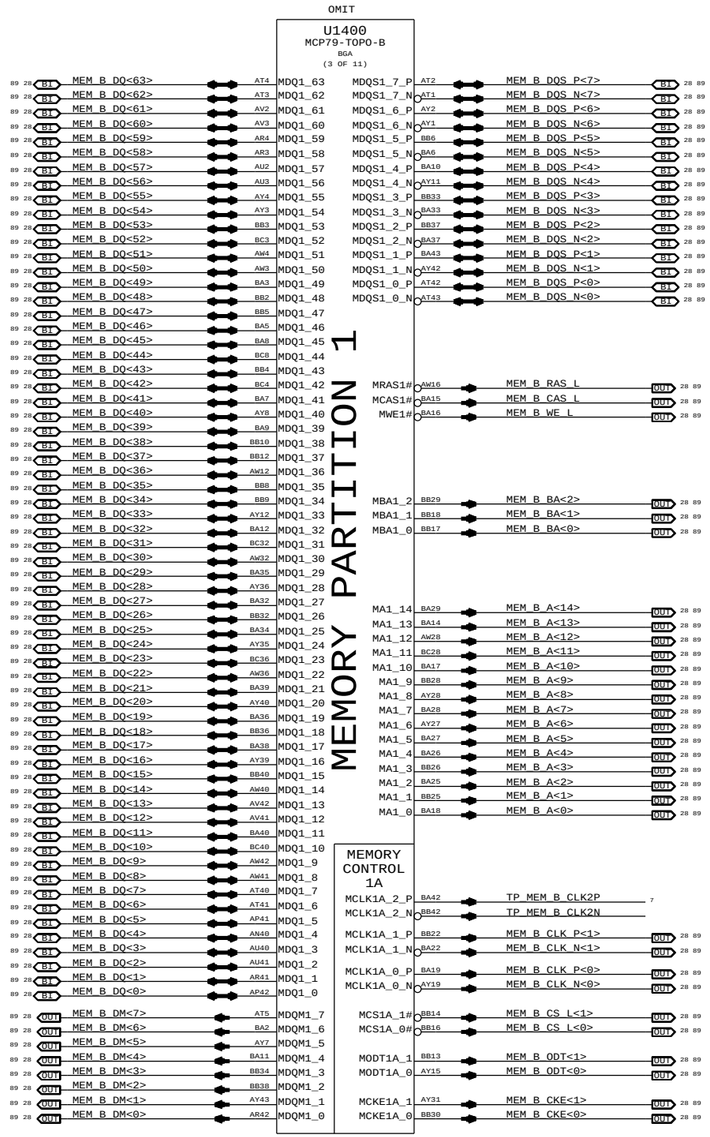
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 14 OF 98	





MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 15 OF 98	

OMIT

U1400
MCP79-TOPO-B
BGA
(4 OF 11)

MEMORY CONTROL 0B

TP_MEM_A_CLK5P	AU33	MCLK0B_2_P	
TP_MEM_A_CLK5N	AU32	MCLK0B_2_N	
TP_MEM_A_CLK4P	BB24	MCLK0B_1_P	
TP_MEM_A_CLK4N	BC24	MCLK0B_1_N	
TP_MEM_A_CLK3P	BA21	MCLK0B_0_P	
TP_MEM_A_CLK3N	BB21	MCLK0B_0_N	
TP_MEM_A_CS_L<2>	AU17	MCS0B_0#	
TP_MEM_A_CS_L<3>	AR17	MCS0B_1#	
TP_MEM_A_ODT<2>	AN17	MODT0B_0	
TP_MEM_A_ODT<3>	AN15	MODT0B_1	
TP_MEM_A_CKE<2>	AV23	MCKE0B_0	
TP_MEM_A_CKE<3>	AN25	MCKE0B_1	

MEMORY CONTROL 1B

		MCLK1B_2_P	BA41
		MCLK1B_2_N	BB41
		MCLK1B_1_P	AY23
		MCLK1B_1_N	BA23
		MCLK1B_0_P	BA20
		MCLK1B_0_N	AY20
		MCS1B_0#	BC16
		MCS1B_1#	BA13
		MODT1B_0	AY16
		MODT1B_1	BC13
		MCKE1B_0	BA30
		MCKE1B_1	BA31
		MRESET0#	AY32

TP_MEM_B_CLK5P			
TP_MEM_B_CLK5N			
TP_MEM_B_CLK4P			
TP_MEM_B_CLK4N			
TP_MEM_B_CLK3P			
TP_MEM_B_CLK3N			
TP_MEM_B_CS_L<2>			
TP_MEM_B_CS_L<3>			
TP_MEM_B_ODT<2>			
TP_MEM_B_ODT<3>			
TP_MEM_B_CKE<2>			
TP_MEM_B_CKE<3>			
MCP_MEM_RESET_L			

TP or NC for DDR2.

PP1V05_S0_MCP_PLL_CORE
87 mA (A01)

17 mA	T27	+V_PLL_XREF_XS	
12 mA	U28	+V_PLL_DP	
19 mA	U27	+V_PLL_CORE	
39 mA	T28	+V_VPLL	

=PP1V8R1V5_S0_MCP_MEM

R1610 40.2 1% 1/16W MF-LF 402

R1611 40.2 1% 1/16W MF-LF 402

MCP_MEM_COMP_VDD	AN41	MEM_COMP_VDD	
MCP_MEM_COMP_GND	AM41	MEM_COMP_GND	

=PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

		+VDD_MEM1	AM17
		+VDD_MEM2	AM19
		+VDD_MEM3	AM21
		+VDD_MEM4	AM23
		+VDD_MEM5	AM25
		+VDD_MEM6	AM27
		+VDD_MEM7	AM29
		+VDD_MEM8	AN16
		+VDD_MEM9	BC29
		+VDD_MEM10	AN20
		+VDD_MEM11	AN24
		+VDD_MEM12	AT17
		+VDD_MEM13	AP16
		+VDD_MEM14	AN22
		+VDD_MEM15	AP20
		+VDD_MEM16	AP24
		+VDD_MEM17	AV16
		+VDD_MEM18	AR16
		+VDD_MEM19	AR20
		+VDD_MEM20	AR24
		+VDD_MEM21	AW15
		+VDD_MEM22	AP22
		+VDD_MEM23	AP18
		+VDD_MEM24	AU16
		+VDD_MEM25	AN18
		+VDD_MEM26	AU24
		+VDD_MEM27	AT21
		+VDD_MEM28	AY29
		+VDD_MEM29	AV24
		+VDD_MEM30	AU20
		+VDD_MEM31	AU22
		+VDD_MEM32	AW27
		+VDD_MEM33	BC17
		+VDD_MEM34	AV20
		+VDD_MEM35	AY17
		+VDD_MEM36	AY18
		+VDD_MEM37	AM15
		+VDD_MEM38	AU18
		+VDD_MEM39	AY25
		+VDD_MEM40	AY26
		+VDD_MEM41	AW19
		+VDD_MEM42	AW24
		+VDD_MEM43	BC25
		+VDD_MEM44	AL30
		+VDD_MEM45	AM31

		GND55	T33
		GND56	T34
		GND57	T35
		GND58	T37
		GND59	T38
		GND60	T7
		GND61	T9
		GND62	U18
		GND63	U20
		GND64	U22

AA22	GND1		
AP12	GND2		
G30	GND3		
P10	GND4		
T10	GND5		
T6	GND6		
V10	GND7		
V34	GND8		
W5	GND9		
AA39	GND10		
AB22	GND11		
AB7	GND12		
AD22	GND13		
AE20	GND14		
AF24	GND15		
AG24	GND16		
AH35	GND17		
AK7	GND18		
AM28	GND19		
AT25	GND20		
AP30	GND21		
AR36	GND22		
AU10	GND23		
F28	GND24		
BC21	GND25		
AY9	GND26		
BC9	GND27		
D34	GND28		
F24	GND29		
G32	GND30		
H31	GND31		
K7	GND32		
M38	GND33		
M5	GND34		
M6	GND35		
M7	GND36		
M9	GND37		
N39	GND38		
N8	GND39		
P33	GND40		
P34	GND41		
P37	GND42		
P4	GND43		
P40	GND44		
P7	GND45		
R36	GND46		
R40	GND47		
R43	GND48		
R5	GND49		
T18	GND50		
T20	GND51		
AK11	GND52		
T24	GND53		
T26	GND54		

MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B

SCALE	SHT	OF
NONE	16	98

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS

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MINI_CLKREQ_L	D5	PEB_CLKREQ#/GPIO_49 Int PU	PE0_REFCLK_P	E11
PCIE_MINI_PRSNT_L	D9	PEB_PRSNT# Int PU	PE0_REFCLK_N	D11
FW_CLKREQ_L	E8	PEC_CLKREQ#/GPIO_50 Int PU	PE1_REFCLK_P	G11
PCIE_FW_PRSNT_L	C10	PEC_PRSNT# Int PU	PE1_REFCLK_N	F11
EXCARD_CLKREQ_L	M15	PED_CLKREQ#/GPIO_51 Int PU	PE2_REFCLK_P	J11
PCIE_EXCARD_PRSNT_L	B10	PED_PRSNT# Int PU	PE2_REFCLK_N	J10
TP_PE4_CLKREQ_L	L16	PEE_CLKREQ#/GPIO_16 Int PU	PE3_REFCLK_P	G13
TP_PE4_PRSNT_L	L18	PEE_PRSNT#/GPIO_46 Int PU	PE3_REFCLK_N	F13
AUD_IP_PERIPHERAL_DET	M16	PEF_CLKREQ#/GPIO_17 Int PU	PE4_REFCLK_P	J13
GMUX_JTAG_TCK_L	M18	PEF_PRSNT#/GPIO_47 Int PU	PE4_REFCLK_N	H13
TP_MCP_GPIO_18	M17	PEG_CLKREQ#/GPIO_18 Int PU	PE5_REFCLK_P	L14
GMUX_JTAG_TDO	M19	PEG_PRSNT#/GPIO_48 Int PU	PE5_REFCLK_N	K14
PCIE_WAKE_L	F17	PE_WAKE# Int PU (S5)	PE6_REFCLK_P	N14
			PE6_REFCLK_N	M14
			PEX_RST0#	K11

PCIE_MINI_D2R_P	K9	PE1_RX0_P	PE1_TX0_P	D8
PCIE_MINI_D2R_N	J9	PE1_RX0_N	PE1_TX0_N	C8
PCIE_FW_D2R_P	H9	PE1_RX1_P	PE1_TX1_P	B8
PCIE_FW_D2R_N	G9	PE1_RX1_N	PE1_TX1_N	A8
PCIE_EXCARD_D2R_P	F9	PE1_RX2_P	PE1_TX2_P	A7
PCIE_EXCARD_D2R_N	E9	PE1_RX2_N	PE1_TX2_N	B7
TP_PCIE_PE4_D2RP	H7	PE1_RX3_P	PE1_TX3_P	B6
TP_PCIE_PE4_D2RN	G7	PE1_RX3_N	PE1_TX3_N	C6

=PP1V05_S0_MCP_PEX_DVDD0			=PP1V05_S0_MCP_PEX_AVDD0	
57 mA (A01, DVDD0 & 1)	T17	+DVDD0_PEX1	+AVDD0_PEX1	Y12
	W19	+DVDD0_PEX2	+AVDD0_PEX2	AA12
	U17	+DVDD0_PEX3	+AVDD0_PEX3	AB12
	V19	+DVDD0_PEX4	+AVDD0_PEX4	M12
	W16	+DVDD0_PEX5	+AVDD0_PEX5	P12
	W17	+DVDD0_PEX6	+AVDD0_PEX6	R12
	W18	+DVDD0_PEX7	+AVDD0_PEX7	N12
	U16	+DVDD0_PEX8	+AVDD0_PEX8	T12
			+AVDD0_PEX9	U12
=PP1V05_S0_MCP_PEX_DVDD1			+AVDD0_PEX10	AC12
	T19	+DVDD1_PEX1	+AVDD0_PEX11	AD12
	U19	+DVDD1_PEX2	+AVDD0_PEX12	V12
			+AVDD0_PEX13	W12
PP1V05_S0_MCP_PLL_PEX	T16	+V_PLL_PEX	=PP1V05_S0_MCP_PEX_AVDD1	
84 mA (A01)			+AVDD1_PEX1	M13
			+AVDD1_PEX2	N13
MCP_PEX_CLK_COMP	A11	PEX_CLK_COMP	+AVDD1_PEX3	P13

Minimum 1.025V for Gen2 support

206 mA (A01, AVDD0 & 1)

Minimum 1.025V for Gen2 support

NO STUFF
R1710
2.37K
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 12.7mm of U1400

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

MCP PCIe Interfaces

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 17 OF 98	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
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LAN

DACS

FLAT PANEL

RGB ONLY

TV / Component
C / Pr
Y / Y
Comp / Pb

(See below)

=PP3V3_ENET_MCP_RMGT
23 18 8

R1810 49.9 1% 1/16W MF-LF 402

R1811 49.9 1% 1/16W MF-LF 402

=PP3V3_S5_MCP_GPIO
20 8

R1820 47K 5% 1/16W MF-LF 402

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP not used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

R1850 10K 5% 1/16W MF-LF 402

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

R1860 100K 5% 1/16W MF-LF 402
R1861 100K 5% 1/16W MF-LF 402

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE: NONE SHT 18 OF 98

OMIT

U1400
MCP79-TOPO-B
BGA
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PCI

91 19	PCI_REQ0_L	T2	PCI_REQ0#		
91 19	PCI_REQ1_L	V9	PCI_REQ1#/FANRPM2		
19	OUT CRTMUX_SEL_TV_L	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	PCI_GNT0# R3	TP_PCI_GNT0_L 7
58 9	OUT AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#	PCI_GNT1#/FANCTL2 U10	TP_PCI_GNT1_L 7
19	IN MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	PCI_GNT2#/GPIO_41/RS232_DTR# R4	GMUX_JTAG_TMS OUT 9
				PCI_GNT3#/GPIO_39/RS232_RTS# U11	GMUX_JTAG_TDI OUT 9
				PCI_GNT4#/GPIO_53/RS232_SOUT# P3	MCP_RS232_SOUT_L OUT 19
91 13	BI MCP_DEBUG<0>	AC3	PCI_AD0	PCI_CBE0# AA3	TP_PCI_C_BE_L<0> 7
91 13	BI MCP_DEBUG<1>	AE10	PCI_AD1	PCI_CBE1# AA6	TP_PCI_C_BE_L<1> 7
91 13	BI MCP_DEBUG<2>	AC4	PCI_AD2	PCI_CBE2# AA11	TP_PCI_C_BE_L<2> 7
91 13	BI MCP_DEBUG<3>	AE11	PCI_AD3	PCI_CBE3# W10	TP_PCI_C_BE_L<3> 7
91 13	BI MCP_DEBUG<4>	AB3	PCI_AD4		
91 13	BI MCP_DEBUG<5>	AC6	PCI_AD5	PCI_DEVSEL# AA9	TP_PCI_DEVSEL_L 7
91 13	BI MCP_DEBUG<6>	AB2	PCI_AD6	PCI_FRAME# Y4	TP_PCI_FRAME_L 7
91 13	BI MCP_DEBUG<7>	AC7	PCI_AD7	PCI_IRDY# AA10	TP_PCI_IRDY_L 7
7	TP_PCI_AD<8>	AC8	PCI_AD8	PCI_PAR Y1	TP_PCI_PAR 7
7	TP_PCI_AD<9>	AA2	PCI_AD9	PCI_PERR#/GPIO_43/RS232_DCD# AB9	TP_PCI_PERR_L 7
7	TP_PCI_AD<10>	AC9	PCI_AD10	PCI_SERR# AA7	TP_PCI_SERR_L 7
7	TP_PCI_AD<11>	AC10	PCI_AD11	PCI_STOP# Y2	TP_PCI_STOP_L 7
7	TP_PCI_AD<12>	AC11	PCI_AD12	PCI_PME#/GPIO_30 T1	PM_LATRIGGER_L OUT 13
7	TP_PCI_AD<13>	AA1	PCI_AD13	Int PU (S5)	
7	TP_PCI_AD<14>	AA5	PCI_AD14		
7	TP_PCI_AD<15>	Y5	PCI_AD15	PCI_RESET0# R10	MEM_VTT_EN_R OUT 25
7	TP_PCI_AD<16>	W3	PCI_AD16	PCI_RESET1# R11	TP_PCI_RESET1_L 7
7	TP_PCI_AD<17>	W6	PCI_AD17		
7	TP_PCI_AD<18>	W4	PCI_AD18		
7	TP_PCI_AD<19>	W7	PCI_AD19		
7	TP_PCI_AD<20>	V3	PCI_AD20	PCI_CLK0 R6	TP_PCI_CLK0 7
7	TP_PCI_AD<21>	W8	PCI_AD21	PCI_CLK1 R7	TP_PCI_CLK1 7
7	TP_PCI_AD<22>	V2	PCI_AD22	PCI_CLK2 R8	91 PCI_CLK33M_MCP_R
7	TP_PCI_AD<23>	W9	PCI_AD23		
7	TP_PCI_AD<24>	U3	PCI_AD24		
7	TP_PCI_AD<25>	W11	PCI_AD25		
7	TP_PCI_AD<26>	U2	PCI_AD26		
7	TP_PCI_AD<27>	U5	PCI_AD27		
7	TP_PCI_AD<28>	U1	PCI_AD28		
7	TP_PCI_AD<29>	U6	PCI_AD29		
7	TP_PCI_AD<30>	T5	PCI_AD30		
7	TP_PCI_AD<31>	U7	PCI_AD31		
7	TP_PCI_INTW_L	P2	PCI_INTW#		
7	TP_PCI_INTX_L	N3	PCI_INTX#		
7	TP_PCI_INTY_L	N2	PCI_INTY#		
7	TP_PCI_INTZ_L	N1	PCI_INTZ#		
7	TP_PCI_TRDY_L	Y3	PCI_TRDY#		
43 41 7	IN PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42	PCI_CLKIN R9	91 PCI_CLK33M_MCP
35	IN FW_PME_L	AE2	LPC_DRQ1#/GPIO_19 Int PU		
7	TP_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU		
43 41 7	BI LPC_SERIRQ	AE6	LPC_SERIRQ Int PU		

R1910 22 5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

LPC

LPC_FRAME#	AD4	43	LPC_FRAME_R_L	R1960 22 5% 1/16W MF-LF 402	LPC_FRAME_L OUT 7 41 43 84 91
LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12		LPC_PWRDWN_L		OUT 7 41 43
LPC_RESET0#	AE5		LPC_RESET_L		OUT 25 84 91
LPC_AD0	AD3		LPC_AD_R<0>	R1950 22 5% 1/16W MF-LF 402	LPC_AD<0> BI 7 41 43 84 91
LPC_AD1	AD2		LPC_AD_R<1>	R1951 22 5% 1/16W MF-LF 402	LPC_AD<1> BI 7 41 43 84 91
LPC_AD2	AD1		LPC_AD_R<2>	R1952 22 5% 1/16W MF-LF 402	LPC_AD<2> BI 7 41 43 84 91
LPC_AD3	AD5		LPC_AD_R<3>	R1953 22 5% 1/16W MF-LF 402	LPC_AD<3> BI 7 41 43 84 91
LPC_CLK0	AE9		LPC_CLK33M_SMC_R		OUT 25 91

R1961 10K 5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

U24	GND65	GND98	Y26
U26	GND66	GND99	Y27
U39	GND67	GND100	AB18
U4	GND68	GND101	H34
U8	GND69	GND102	AB20
V16	GND70	GND103	AB21
V17	GND71	GND104	AB23
V18	GND72	GND105	AB24
V20	GND73	GND106	AB25
V22	GND74	GND107	AB26
V24	GND75	GND108	AB27
V26	GND76	GND109	AB28
V27	GND77	GND110	AB34
V28	GND78	GND111	AB37
V33	GND79	GND112	AB4
V37	GND80	GND113	AB40
V4	GND81	GND114	AC22
V40	GND82	GND115	AC36
V7	GND83	GND116	AC40
W20	GND84	GND117	AB33
W22	GND85	GND118	AC5
W24	GND86	GND119	AD16
W36	GND87	GND120	AD17
W40	GND88	GND121	AD18
W43	GND89	GND122	AD19
Y16	GND90	GND123	AD20
Y17	GND91	GND124	AD24
Y18	GND92	GND125	AD25
Y19	GND93	GND126	AD26
Y20	GND94	GND127	AD27
Y22	GND95	GND128	AD28
Y24	GND96	GND129	AD33
Y25	GND97	GND130	AD34

21 18 8 =PP3V3_S0_MCP_GPIO

19	MCP_RS232_SOUT_L	R1989	8.2K	5% 1/16W MF-LF 402
91 19	PCI_REQ0_L	R1990	8.2K	5% 1/16W MF-LF 402
91 19	PCI_REQ1_L	R1991	8.2K	5% 1/16W MF-LF 402
19	CRTMUX_SEL_TV_L	R1992	8.2K	5% 1/16W MF-LF 402
19	MCP_RS232_SIN_L	R1994	8.2K	5% 1/16W MF-LF 402

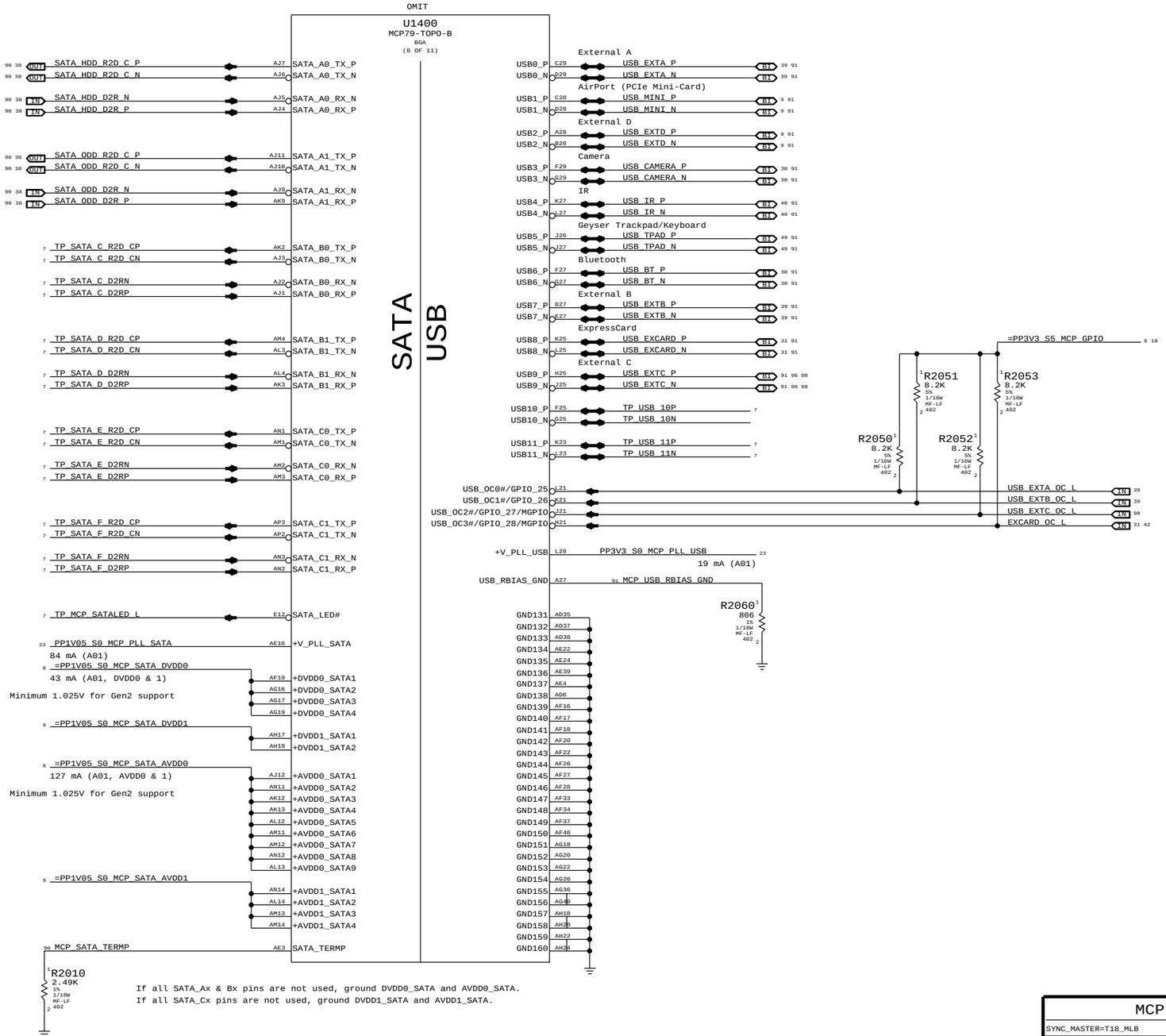
MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B

SCALE	SHT	OF
NONE	19	98



If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP SATA & USB

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 20 OF 98	

OMIT

U1400
MCP79-TOPO-B
BGA
(9 OF 11)

HDA

HDA_SDIN0 — G15 HDA_SDATA_IN0 (Int PD)
TP_MLB_RAM_SIZE — J14 HDA_SDATA_IN1_GPIO_2/PS2_KB_CLK (Int PD)
TP_MLB_RAM_VENDOR (MXM_OK for MXM systems) — J15 HDA_SDATA_IN2_GPIO_3/PS2_KB_DATA (Int PD)

=PP3V3R1V5_S0_MCP_HDA — R2110 49.9 1% 1/10W MF-LF 402 — MCP_HDA_PULLDN_COMP — A15 HDA_PULLDN_COMP

PP1V05_S0_MCP_PLL_NV — 37 mA (A01) — 20 mA / 17 mA — AE18 +V_PLL_NV_H, AE17 +V_PLL_SP_SPREF

=PP3V3R1V5_S0_MCP_HDA — 7 mA (A01) — R2160 8.2K 5% 1/10W MF-LF 402 — +V_DUAL_HDA1 J16, +V_DUAL_HDA2 K16

HDA_SDATA_OUT	F15	HDA_SDOUT_R	R2170 22 5% 1/16W MF-LF 402	HDA_SDOUT
HDA_BITCLK	E15	HDA_BIT_CLK_R	R2171 22 5% 1/16W MF-LF 402	HDA_BIT_CLK
HDA_RESET*	K15	HDA_RST_R_L	R2172 22 5% 1/16W MF-LF 402	HDA_RST_L
HDA_SYNC	L15	HDA_SYNC_R	R2173 22 5% 1/16W MF-LF 402	HDA_SYNC

MISC

SMC_ADAPTER_EN	L26	GPIO_12_SUS_STAT_ACCLMTR_EXT_TRIG_L	
=SPI_CS1_R_L_USE_MLB	L24	GPIO_1/PWRDN_OK/SPI_CS1	
TP_SB_A20GATE	K13	A20GATE	Int PU
TP_MCP_KBDRSTIN_L	L13	KBRDRSTIN*	Int PU
SMC_WAKE_SCI_L	C19	SIO_PME*	Int PU (S5)
SMC_RUNTIME_SCI_L	C18	EXT_SMI/GPIO_32*	Int PU (S5)
SM_INTRUDER_L	B20	INTRUDER*	
TP_MCP_LID_L	M25	LID*	Int PU (S5)
PM_BATLOW_L	M24	LLB*	Int PU (S5)
PM_DPRSLPVR	M22	CPU_DPRSLPVR	
PM_PWRBTN_L	C16	PWRBTN*	Int PU (S5)
PM_SYSRST_DEBOUNCE_L	D16	RSTBTN*	Int PU
RTC_RST_L	C20	RTC_RST*	
PM_RSMRST_L	D20	PWRGD_SB	
MCP_PS_PWRGD	E20	PS_PWRGD	
MCP_CPU_VLD	C17	CPU_VLD	
JTAG_MCP_TDI	E19	JTAG_TDI	Int PU
JTAG_MCP_TDO	F19	JTAG_TDO	
JTAG_MCP_TMS	J19	JTAG_TMS	Int PU
JTAG_MCP_TRST_L	J18	JTAG_TRST*	
JTAG_MCP_TCK	G19	JTAG_TCK	
MCP_CLK25M_XTALIN	A16	XTALIN	
MCP_CLK25M_XTALOUT	B16	XTALOUT	
RTC_CLK32K_XTALIN	A19	XTALIN_RTC	
RTC_CLK32K_XTALOUT	B19	XTALOUT_RTC	

PP3V3_G3_RTC — R2120 49.9K 1% 1/16W MF-LF 402 — R2121 49.9K 1% 1/16W MF-LF 402

R2150 10K 5% 1/16W MF-LF 402 — R2151 100K 5% 1/16W MF-LF 402

HDA_DOCK_EN*_GPIO_4/PS2_MS_CLK	K17	MCP_GPIO_4	21
HDA_DOCK_RST*_GPIO_5/PS2_MS_DATA	L17	AUD_I2C_INT_L	IN 21 58
SLP_S3*	G17	PM_SLP_S3_L	OUT 7 33 36 41 67 82 84
SLP_RMGT*	J17	PM_SLP_RMGT_L	OUT 8
SLP_S5*	M17	PM_SLP_S4_L	OUT 39 41 42 67
THERM_DIODE_P	B11	MCP_THMDIODE_P	OUT 47 96
THERM_DIODE_N	C11	MCP_THMDIODE_N	OUT 47 96
MCP_VID0/GPIO_13	L20	MCP_VID<0>	OUT 21 64
MCP_VID1/GPIO_14	M20	MCP_VID<1>	OUT 21 64
MCP_VID2/GPIO_15	M21	MCP_VID<2>	OUT 21 64
SPKR	C13	MCP_SPKR	
SMB_CLK0	L19	SMBUS_MCP_0_CLK	OUT 7 13 44 91
SMB_DATA0	K19	SMBUS_MCP_0_DATA	BI 7 13 44 91
SMB_CLK1/MSMB_CLK	G21	SMBUS_MCP_1_CLK	OUT 44 91
SMB_DATA1/MSMB_DATA	F21	SMBUS_MCP_1_DATA	BI 44 91
SMB_ALERT*/GPIO_64	M23	AP_PWR_EN	OUT 21 30 33
(MGPIO2) FANRPM0/GPIO_60	B12	MEM_EVENT_L	IN 21 27 28 41
FANCTL0/GPIO_61	A12	ODD_PWR_EN_L	OUT 38
(MGPIO3) FANRPM1/GPIO_63	D12	SMC_IG_THROTTLE_L	IN 21 42
FANCTL1/GPIO_62	C12	ARB_DETECT	21
CPUVDD_EN	D17	MCP_CPUVDD_EN	OUT 25
SPI_CS0/GPIO_10	C14	SPI_CS0_R_L	OUT 43 91
SPI_CLK/GPIO_11	D13	SPI_CLK_R	OUT 43 91
SPI_DI/GPIO_8	C15	SPI_MISO	IN 43 91
SPI_DO/GPIO_9	B14	SPI_MOSI_R	OUT 43 91
SUS_CLK/GPIO_34	B18	PM_CLK32K_SUSCLK_R	OUT 25 91
BUF_SIO_CLK	AE7	TP_MCP_BUF_SIO_CLK	7
TEST_MODE_EN	K22	MCP_TEST_MODE_EN	
PKG_TEST	L22		

R2163 10K 5% 1/16W MF-LF 402 — R2190 1K 1% 1/16W MF-LF 402

=PP3V3_S0_MCP — BOOT_MODE_SAFE — R2180 10K 5% 1/16W MF-LF 402 — OUT 9 BOOT_MODE_USER — R2181 10K 5% 1/16W MF-LF 402

USER mode: Normal
SAFE mode: For ROMSIP recovery

Connects to SMC for automatic recovery.

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R 21 91 — C2170 10PF 5% 50V CERM 402
HDA_BIT_CLK_R 21 91
HDA_RST_R_L 21 91 — C2172 10PF 5% 50V CERM 402
HDA_SYNC_R 21 91 — C2171 10PF 5% 50V CERM 402 — C2173 10PF 5% 50V CERM 402

=PP3V3_S0_MCP_GPIO 8 18 19 — R2140 10K, R2141 10K, R2142 10K, R2143 10K (5% 1/16W MF-LF 402)

MCP_GPIO_4	21
AUD_I2C_INT_L	21 58
MEM_EVENT_L	21 27 28 41
SMC_IG_THROTTLE_L	21 42
ARB_DETECT	21

R2147 100K 5% 1/16W MF-LF 402

=PP3V3_S3_MCP_GPIO 8 — R2154 100K 5% 1/16W MF-LF 402 — AP_PWR_EN 21 30 33

MCP_VID<0> 21 64 — R2155 22K 5% 1/16W MF-LF 402
MCP_VID<1> 21 64 — R2156 22K 5% 1/16W MF-LF 402
MCP_VID<2> 21 64 — R2157 22K 5% 1/16W MF-LF 402

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MCP HDA & MISC

SYNC_MASTER=T18_MLB — SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE: NONE — SHT 21 OF 98

OMIT

U1400
MCP79-TOPO-B
BGA
(11 OF 11)

GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

45 23 8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

AA25	+VDD_CORE1	+VTT_CPU1	R32	=PP1V05_S0_MCP_FSB 8 9 14 23
AC23	+VDD_CORE2	+VTT_CPU2	AC32	1139 mA 1182 mA (A01)
U25	+VDD_CORE3	+VTT_CPU3	E40	
AH12	+VDD_CORE4	+VTT_CPU4	J36	
AG10	+VDD_CORE5	+VTT_CPU5	N32	
AG5	+VDD_CORE6	+VTT_CPU6	T32	
Y21	+VDD_CORE7	+VTT_CPU7	U32	
Y23	+VDD_CORE8	+VTT_CPU8	V32	
AA16	+VDD_CORE9	+VTT_CPU9	W32	
AA26	+VDD_CORE10	+VTT_CPU10	P31	
AA27	+VDD_CORE11	+VTT_CPU11	AF32	
AA28	+VDD_CORE12	+VTT_CPU12	AE32	
AC16	+VDD_CORE13	+VTT_CPU13	AH32	
AC17	+VDD_CORE14	+VTT_CPU14	AJ32	
AC18	+VDD_CORE15	+VTT_CPU15	AK31	
AC19	+VDD_CORE16	+VTT_CPU16	AK32	
AC20	+VDD_CORE17	+VTT_CPU17	AD32	
AC21	+VDD_CORE18	+VTT_CPU18	AL31	
AA17	+VDD_CORE19	+VTT_CPU19	AB32	
AC24	+VDD_CORE20	+VTT_CPU20	B41	
AC25	+VDD_CORE21	+VTT_CPU21	B42	
AC26	+VDD_CORE22	+VTT_CPU22	C40	
AC27	+VDD_CORE23	+VTT_CPU23	C41	
AC28	+VDD_CORE24	+VTT_CPU24	C42	
AD21	+VDD_CORE25	+VTT_CPU25	D39	
AD23	+VDD_CORE26	+VTT_CPU26	D40	
W27	+VDD_CORE27	+VTT_CPU27	D41	
V25	+VDD_CORE28	+VTT_CPU28	E38	
AA18	+VDD_CORE29	+VTT_CPU29	E39	
AE19	+VDD_CORE30	+VTT_CPU30	F37	
AE21	+VDD_CORE31	+VTT_CPU31	F38	
AE23	+VDD_CORE32	+VTT_CPU32	F39	
AE25	+VDD_CORE33	+VTT_CPU33	G36	
AE26	+VDD_CORE34	+VTT_CPU34	G37	
AE27	+VDD_CORE35	+VTT_CPU35	G38	
AE28	+VDD_CORE36	+VTT_CPU36	H35	
AF10	+VDD_CORE37	+VTT_CPU37	H37	
AF11	+VDD_CORE38	+VTT_CPU38	J34	
AA19	+VDD_CORE39	+VTT_CPU39	J35	
AF2	+VDD_CORE40	+VTT_CPU40	K33	
AF21	+VDD_CORE41	+VTT_CPU41	K34	
AF23	+VDD_CORE42	+VTT_CPU42	K35	
AF25	+VDD_CORE43	+VTT_CPU43	L32	
AF3	+VDD_CORE44	+VTT_CPU44	L33	
AF4	+VDD_CORE45	+VTT_CPU45	L34	
AF7	+VDD_CORE46	+VTT_CPU46	M31	
AH23	+VDD_CORE47	+VTT_CPU47	M32	
AF9	+VDD_CORE48	+VTT_CPU48	M33	
AA20	+VDD_CORE49	+VTT_CPU49	N31	
AG11	+VDD_CORE50	+VTT_CPU50	P32	
AG12	+VDD_CORE51	+VTT_CPU51	Y32	
AG21	+VDD_CORE52	+VTT_CPU52	AA32	
AG23	+VDD_CORE53			
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32	43 mA
AG3	+VDD_CORE55			
AG4	+VDD_CORE56			
AA21	+VDD_CORE57			
AG6	+VDD_CORE58			=PP3V3_S0_MCP 8 21 23
AG7	+VDD_CORE59	+3.3V_1	AD10	450 mA (A01)
AG8	+VDD_CORE60	+3.3V_2	AE8	
AG9	+VDD_CORE61	+3.3V_3	AB10	
AH1	+VDD_CORE62	+3.3V_4	AD9	
AH10	+VDD_CORE63	+3.3V_5	Y10	
AH11	+VDD_CORE64	+3.3V_6	AB11	
W26	+VDD_CORE65	+3.3V_7	AA8	
AH2	+VDD_CORE66	+3.3V_8	Y9	
AA23	+VDD_CORE67			
W28	+VDD_CORE68			
AH25	+VDD_CORE69			=PP3V3_S5_MCP 8 23
AH21	+VDD_CORE70	+3.3V_DUAL1	G18	16 mA 266 mA (A01)
AH3	+VDD_CORE71	+3.3V_DUAL2	H19	
AH4	+VDD_CORE72	+3.3V_DUAL3	J20	
AH5	+VDD_CORE73	+3.3V_DUAL4	K20	
AH6	+VDD_CORE74			
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26	250 mA
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27	
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28	
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28	
W23	+VDD_CORE79			
W25	+VDD_CORE80			
AF12	+VDD_CORE81			
		+VDD_AUXC1	T21	=PP1V05_S5_MCP_VDD_AUXC 8 23
		+VDD_AUXC2	U21	105 mA (A01)
A20	+VBAT	+VDD_AUXC3	V21	

25 21 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	22	98

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Core Power
=PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)
NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)
C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power
=PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)
C2515 4.7UF 20% 4V X5R 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power
=PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)
C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

=PP1V05_S0_MCP_AVDD_UF
333 mA (A01)
L2570 30-OHM-5A 0603
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)
C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF
PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)

MCP 1.05V AUX Power
=PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)
C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power
=PP1V05_ENET_MCP_RMGT
131 mA (A01)
C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

L2575 30-OHM-5A 0603
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)
C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF
PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)

MCP FSB (VTT) Power
=PP1V05_S0_MCP_FSB
1182 mA (A01)
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)
C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_S0_MCP_PLL_PEX_UF
L2582 30-OHM-1.7A 0402
C2582 4.7UF 20% 4V X5R 402
C2583 2.2UF 20% 6.3V CERM 402-LF
PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

MCP Memory Power
=PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)
C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

=PP1V05_S0_MCP_PLL_UF
562 mA (A01)
R2580 0.2 1% 1/5W MF 402-HF
C2580 4.7UF 20% 4V X5R 402
C2581 2.2UF 10% 16V X5R 603
PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)

MCP 3.3V Power
=PP3V3_S0_MCP
450 mA (A01)
NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)
C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

=PP3V3_S0_MCP_PLL_UF
19 mA (A01)
L2555 30-OHM-1.7A 0402
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2555 2.2UF 20% 6.3V CERM 402-LF
PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)

L2584 30-OHM-1.7A 0402
C2584 4.7UF 20% 4V X5R 402
C2585 2.2UF 20% 6.3V CERM 402-LF
PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

MCP 3.3V AUX/USB Power
=PP3V3_S5_MCP
266 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power
=PP3V3_ENET_MCP_RMGT
83 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2564 2.2UF 20% 6.3V CERM 402-LF

L2586 30-OHM-1.7A 0402
C2586 4.7UF 20% 4V X5R 402
C2587 2.2UF 20% 6.3V CERM 402-LF
PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)

MCP 3.3V/1.5V HDA Power
=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2562 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef
=PP3V3_ENET_MCP_RMGT
R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402
MCP_MII_VREF
C2591 0.1UF 20% 10V CERM 402

=PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)
L2595 30-OHM-1.7A 0402
C2595 4.7UF 20% 4V X5R 402
C2596 2.2UF 20% 6.3V CERM 402-LF
PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)

L2588 30-OHM-1.7A 0402
C2588 4.7UF 20% 4V X5R 402
C2589 2.2UF 20% 6.3V CERM 402-LF
C2590 0.1UF 20% 10V CERM 402
PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling
SYNC_MASTER=M98_MLB
SYNC_DATE=04/01/2008

APPLE INC.
SIZE D
DRAWING NUMBER 051-8071
REV. 8
SCALE NONE
SHT 23 OF 98

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

8 =PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)

C2610 2.2UF 20% 6.3V CERM 402-LF

8 =PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)

C2615 4.7UF 20% 4V X5R 402
C2616 2.2UF 20% 6.3V CERM 402-LF

90 18 MCP_HDMI_RSET
90 18 MCP_HDMI_VPROBE

NO STUFF C2620 0.1UF 20% 10V CERM 402
R2620 1K 1% 1/16W MF-LF 402

90 18 MCP_IFPAB_RSET
90 18 MCP_IFPAB_VPROBE

NO STUFF C2630 0.1UF 20% 10V CERM 402
NO STUFF R2630 1K 1% 1/16W MF-LF 402

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???

8 =PP3V3_S0_MCP_VPLL_UF
16 mA (A01)

L2640 30-OHM-1.7A 0402

PP3V3_S0_MCP_VPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
16 mA (A01)

C2640 4.7UF 20% 6.3V CERM 603
C2641 2.2UF 20% 6.3V CERM 402-LF

8 =PP3V3_S0_MCP_DAC_UF
206 mA (A01)

NO STUFF L2650 30-OHM-1.7A 0402

NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

PP3V3_S0_MCP_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
206 mA (A01)

NO STUFF C2650 2.2UF 20% 6.3V CERM 402-LF
R2651 0 5% 1/10W MF-LF 402

18	TP_MCP_RGB_RED		NC_MCP_RGB_RED
18	TP_MCP_RGB_GREEN		NC_MCP_RGB_GREEN
18	TP_MCP_RGB_BLUE		NC_MCP_RGB_BLUE
18	TP_MCP_RGB_HSYNC		NC_MCP_RGB_HSYNC
18	TP_MCP_RGB_VSYNC		NC_MCP_RGB_VSYNC
90 18	CRT_IG_R_C_PR		NC_CRT_IG_R_C_PR
90 18	CRT_IG_G_Y_Y		NC_CRT_IG_G_Y_Y
90 18	CRT_IG_B_COMP_PB		NC_CRT_IG_B_COMP_PB
90 18	CRT_IG_HSYNC		NC_CRT_IG_HSYNC
90 18	CRT_IG_VSYNC		NC_CRT_IG_VSYNC
18	TP_MCP_RGB_DAC_RSET		NC_MCP_RGB_DAC_RSET
18	TP_MCP_RGB_DAC_VREF		NC_MCP_RGB_DAC_VREF
90 18	MCP_TV_DAC_RSET		NC_MCP_TV_DAC_RSET
90 18	MCP_TV_DAC_VREF		NC_MCP_TV_DAC_VREF
18	MCP_CLK27M_XTALIN		NC_MCP_CLK27M_XTALIN
18	MCP_CLK27M_XTALOUT		NC_MCP_CLK27M_XTALOUT

(MAKE_BASE=TRUE, NO_TEST=TRUE)

HDCP ROM

WF: Open question on which packge option(s) nVidia can support.

8 =PP3V3_S0_HDCPROM

C2690 0.1UF 20% 10V CERM 402
NO STUFN
NO STUFF
R2690 10K 5% 1/16W MF-LF 402
NO STUFF

U2695 AT24C08 SOIC
VCC
A0
A1
A2
SDA =I2C_HDCPROM_SDA (IO 44)
SCL =I2C_HDCPROM_SCL (IN 44)
WP HDCPROM_WP
GND

Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

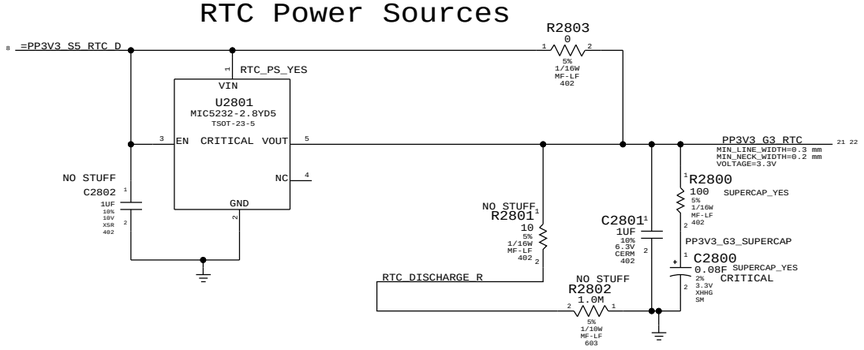
MCP Graphics Support

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

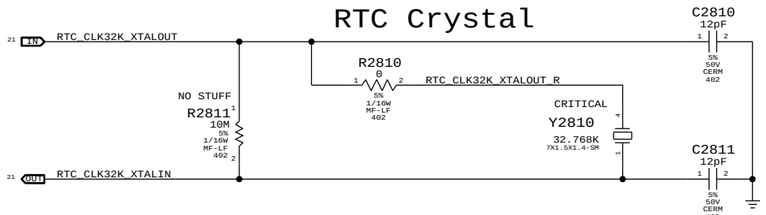
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 24 OF 98	

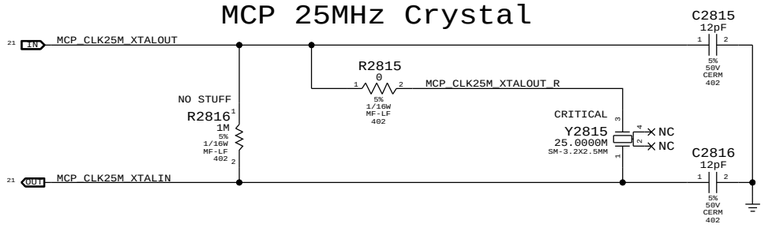
RTC Power Sources



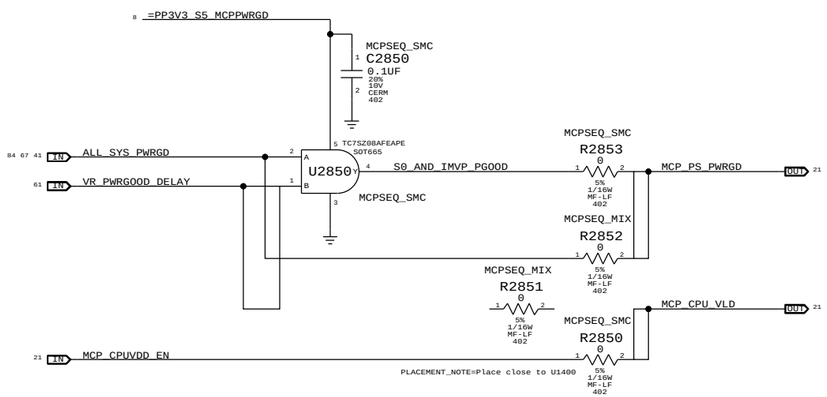
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 ‘MLB’ power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

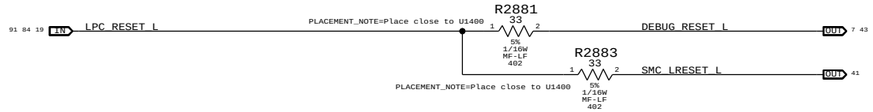
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

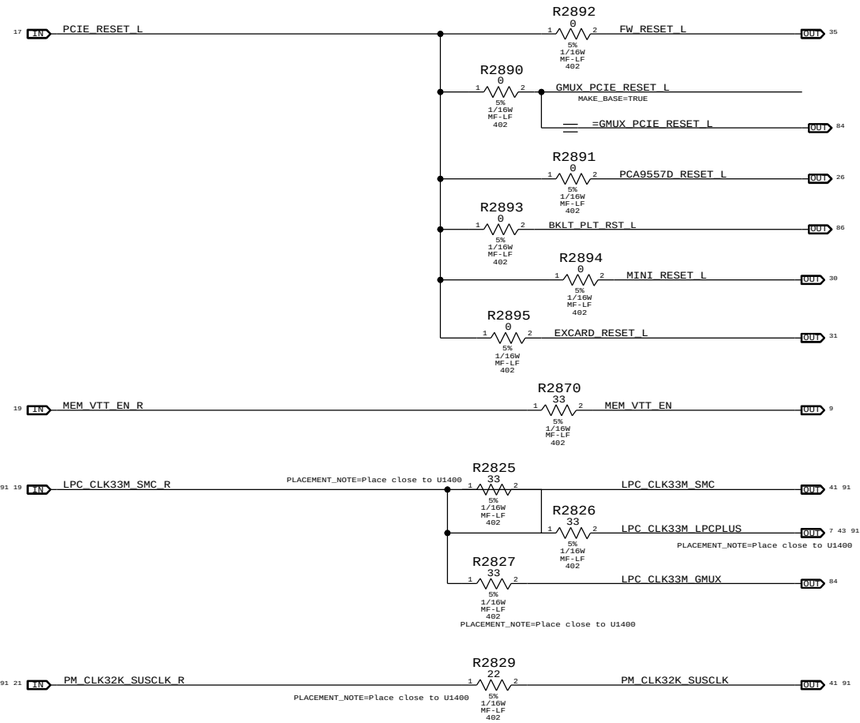
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Platform Reset Connections

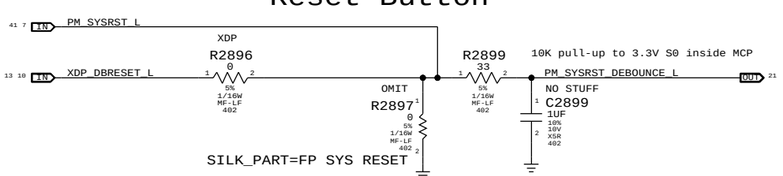
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



SB Misc	
SYNC_MASTER=M98_MLB	SYNC_DATE=05/01/2008

APPLE INC.	SIZE D	DRAWING NUMBER 051-8071	REV. B
	SCALE NONE	SHT 25 OF 98	

Page Notes

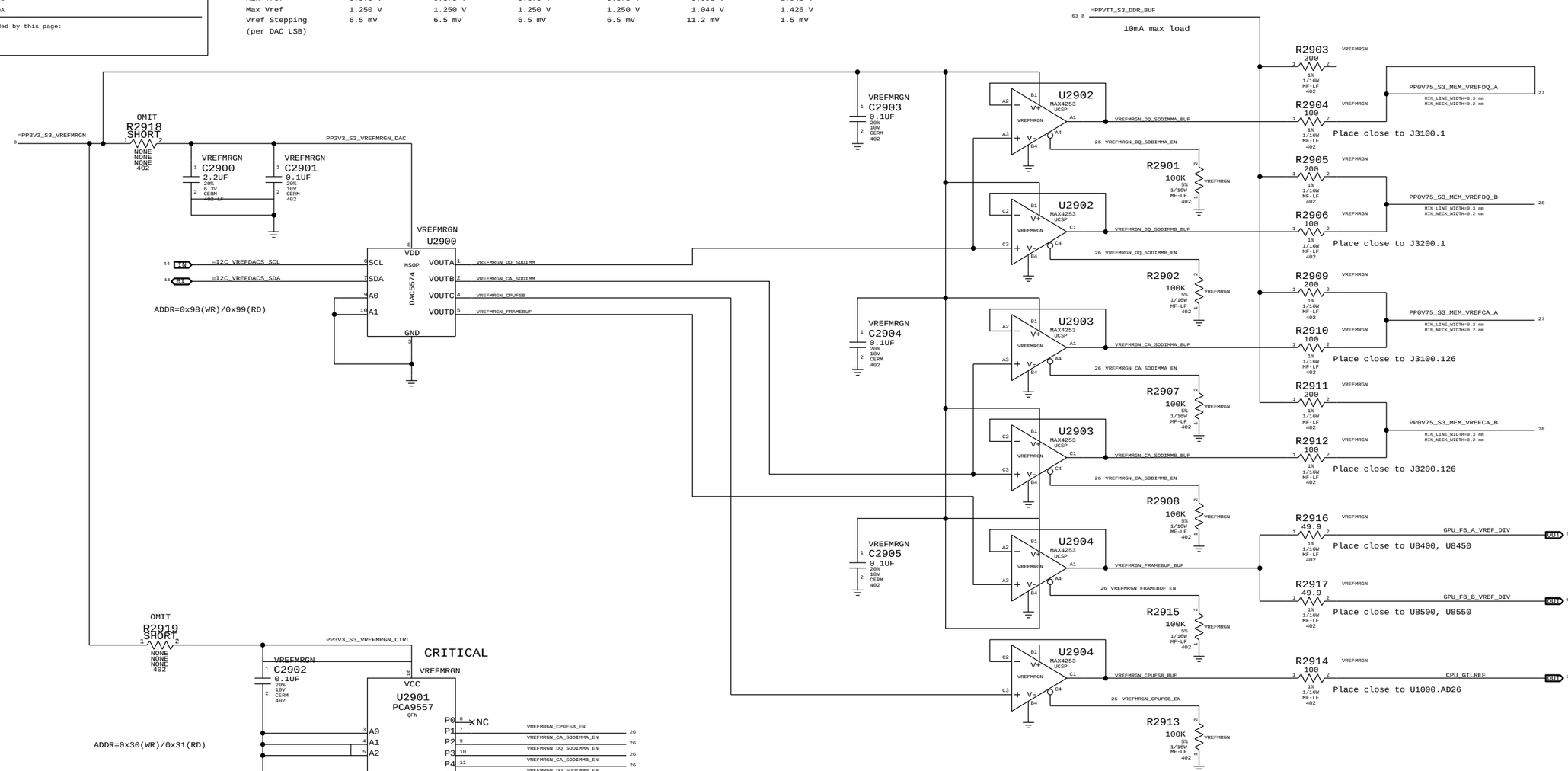
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ A	MEM A VREF CA B	MEM B VREF DQ A	MEM B VREF CA B	CPU FSB VREF C	FRAME BUFFER VREF D
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55	0xFF
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 26 OF 98	

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

8 =PP1V5_S0_MEM_A

8 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603

C3101 10UF 20% 6.3V X5R 603

C3110 C3111 C3112 C3113 C3114 C3115 C3116 C3117 C3118 C3119 C3120 C3121 C3122 C3123 0.1UF 20% 10V CERM 402

26 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF

C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-THB (SYMBOL 2 OF 2)

DDR3-SODIMM-DUAL-M97-3

KEY

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204

NC

NC

NC

516-0201

SPD ADDR=0xA0(WR)/0xA1(RD)

J3100 F-RT-THB (SYMBOL 1 OF 2)

DDR3-SODIMM-DUAL-M97-3

CRITICAL

KEY

1	VREFDQ	VSS	2
3	VSS	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS	8
9	VSS	DQS0*	10
11	DM0	DQS0	12
13	VSS	VSS	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS	VSS	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS	VSS	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS	VSS	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS	VSS	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS	VSS	44
45	DQS2*	DM2	46
47	DQS2	VSS	48
49	VSS	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS	54
55	VSS	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS	60
61	VSS	DQS3*	62
63	DM3	DQS3	64
65	VSS	VSS	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS	VSS	72

516-0201

PP0V75_S3_MEM_VREFCA_A 26

C3135 2.2UF 20% 6.3V CERM 402-LF

C3136 0.1UF 20% 10V CERM 402

=PP0V75_S0_MEM_VTT_A 8

C3140 2.2UF 20% 6.3V CERM 402-LF

R3140 10K 5% 1/16W MF-LF 402

R3141 10K 5% 1/16W MF-LF 402

8 =PPSPD_S0_MEM_A

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=BEN_K20 SYNC_DATE=06/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 27 OF 98	

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

8 =PP1V5_S0_MEM_B
8 =PP1V5_S3_MEM_B

C3210 C3211 C3212 C3213 C3214 C3215 C3216 C3217 C3218 C3219 C3220 C3221 C3222 C3223
0.1UF 20% 10V CERM 402

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603

26 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 DDR3-SODIMM (2 OF 2) F-RT-BGA3

KEY

		73	CKE0	CKE1	74
		75	VDD	VDD	76
		77	NC	A15	78
89 15 IN	MEM_B_BA<2>	79	BA2	A14	80
		81	VDD	VDD	82
89 15 IN	MEM_B_A<12>	83	A12/BC*	A11	84
89 15 IN	MEM_B_A<9>	85	A9	A7	86
		87	VDD	VDD	88
89 15 IN	MEM_B_A<8>	89	A8	A6	90
89 15 IN	MEM_B_A<5>	91	A5	A4	92
		93	VDD	VDD	94
89 15 IN	MEM_B_A<3>	95	A3	A2	96
89 15 IN	MEM_B_A<1>	97	A1	A0	98
		99	VDD	VDD	100
89 15 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102
89 15 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104
		105	VDD	VDD	106
89 15 IN	MEM_B_A<10>	107	A10/AP	BA1	108
89 15 IN	MEM_B_BA<0>	109	BA0	RAS*	110
		111	VDD	VDD	112
89 15 IN	MEM_B_WE_L	113	WE*	S0*	114
89 15 IN	MEM_B_CAS_L	115	CAS*	ODT0	116
		117	VDD	VDD	118
89 15 IN	MEM_B_A<13>	119	A13	ODT1	120
89 15 IN	MEM_B_CS_L<1>	121	S1*	NC	122
		123	VDD	VDD	124
		125	TEST	VREFCA	126
		127	VSS	VSS	128
89 15 BI	MEM_B_DQ<32>	129	DQ32	DQ36	130
89 15 BI	MEM_B_DQ<37>	131	DQ33	DQ37	132
		133	VSS	VSS	134
89 15 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136
89 15 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138
		139	VSS	DQ38	140
89 15 BI	MEM_B_DQ<34>	141	DQ34	DQ39	142
89 15 BI	MEM_B_DQ<35>	143	DQ35	VSS	144
		145	VSS	DQ44	146
89 15 BI	MEM_B_DQ<41>	147	DQ40	DQ45	148
89 15 BI	MEM_B_DQ<40>	149	DQ41	VSS	150
		151	VSS	DQS5*	152
89 15 IN	MEM_B_DM<5>	153	DM5	DQS5	154
		155	VSS	VSS	156
89 15 BI	MEM_B_DQ<43>	157	DQ42	DQ46	158
89 15 BI	MEM_B_DQ<42>	159	DQ43	DQ47	160
		161	VSS	VSS	162
89 15 BI	MEM_B_DQ<55>	163	DQ48	DQ52	164
89 15 BI	MEM_B_DQ<49>	165	DQ49	DQ53	166
		167	VSS	VSS	168
89 15 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170
89 15 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172
		173	VSS	DQ54	174
89 15 BI	MEM_B_DQ<52>	175	DQ50	DQ55	176
89 15 BI	MEM_B_DQ<51>	177	DQ51	VSS	178
		179	VSS	DQ60	180
89 15 BI	MEM_B_DQ<56>	181	DQ56	DQ61	182
89 15 BI	MEM_B_DQ<57>	183	DQ57	VSS	184
		185	VSS	DQS7*	186
89 15 IN	MEM_B_DM<7>	187	DM7	DQS7	188
		189	VSS	VSS	190
89 15 BI	MEM_B_DQ<63>	191	DQ58	DQ62	192
89 15 BI	MEM_B_DQ<59>	193	DQ59	DQ63	194
		195	VSS	VSS	196
	MEM_B_SA<0>	197	SA0	EVENT*	198
		199	VDDSPD	SDA	200
	MEM_B_SA<1>	201	SA1	SCL	202
		203	VTT	VTT	204
		205	MTG PIN	MTG PIN	206
		207	MTG PIN	MTG PIN	208
		209	MTG PIN	MTG PIN	210
		211	MTG PIN	MTG PIN	212

MTG PINS

MEM_B_CKE<0> MEM_B_CKE<1>
MEM_B_BA<2> MEM_B_A<15> (IN 9) MEM_B_A<14>
MEM_B_A<12> MEM_B_A<11>
MEM_B_A<9> MEM_B_A<7>
MEM_B_A<8> MEM_B_A<6>
MEM_B_A<5> MEM_B_A<4>
MEM_B_A<3> MEM_B_A<2>
MEM_B_A<1> MEM_B_A<0>
MEM_B_CLK_P<0> MEM_B_CLK_P<1>
MEM_B_CLK_N<0> MEM_B_CLK_N<1>
MEM_B_A<10> MEM_B_BA<1>
MEM_B_BA<0> MEM_B_RAS_L
MEM_B_WE_L MEM_B_CS_L<0>
MEM_B_CAS_L MEM_B_ODT<0>
MEM_B_A<13> MEM_B_ODT<1>
MEM_B_CS_L<1>
MEM_B_DQ<32> MEM_B_DQ<33>
MEM_B_DQ<37> MEM_B_DQ<36>
MEM_B_DQS_N<4> MEM_B_DM<4>
MEM_B_DQS_P<4>
MEM_B_DQ<34> MEM_B_DQ<38>
MEM_B_DQ<35> MEM_B_DQ<39>
MEM_B_DQ<41> MEM_B_DQ<44>
MEM_B_DQ<40> MEM_B_DQ<45>
MEM_B_DM<5>
MEM_B_DQ<43> MEM_B_DQ<47>
MEM_B_DQ<42> MEM_B_DQ<46>
MEM_B_DQ<55> MEM_B_DQ<48>
MEM_B_DQ<49> MEM_B_DQ<54>
MEM_B_DQS_N<6> MEM_B_DM<6>
MEM_B_DQS_P<6>
MEM_B_DQ<52> MEM_B_DQ<53>
MEM_B_DQ<51> MEM_B_DQ<50>
MEM_B_DQ<56> MEM_B_DQ<60>
MEM_B_DQ<57> MEM_B_DQ<61>
MEM_B_DM<7> MEM_B_DQS_N<7>
MEM_B_DQS_P<7>
MEM_B_DQ<63> MEM_B_DQ<58>
MEM_B_DQ<59> MEM_B_DQ<62>
MEM_EVENT_L (OUT 21 27 41)
=I2C_SODIMMB_SDA (BI 44)
=I2C_SODIMMB_SCL (IN 44)
=PP0V75_S0_MEM_VTT_B (8)

516s0706

SPD ADDR=0xA2(WR)/0xA3(RD)

R3240 10K 5% 1/16W MF-LF 402
R3241 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF

8 =PPSPD_S0_MEM_B

J3200 DDR3-SODIMM (1 OF 2) F-RT-BGA3 CRITICAL

KEY

		1	VREFDQ	VSS	2
		3	VSS	DQ4	4
89 15 BI	MEM_B_DQ<0>	5	DQ0	DQ5	6
89 15 BI	MEM_B_DQ<1>	7	DQ1	VSS	8
		9	VSS	DQS0*	10
89 15 IN	MEM_B_DM<0>	11	DM0	DQS0	12
		13	VSS	VSS	14
89 15 BI	MEM_B_DQ<2>	15	DQ2	DQ6	16
89 15 BI	MEM_B_DQ<3>	17	DQ3	DQ7	18
		19	VSS	VSS	20
89 15 BI	MEM_B_DQ<28>	21	DQ8	DQ12	22
89 15 BI	MEM_B_DQ<24>	23	DQ9	DQ13	24
		25	VSS	VSS	26
89 15 BI	MEM_B_DQS_N<3>	27	DQS1*	DM1	28
89 15 BI	MEM_B_DQS_P<3>	29	DQS1	RESET*	30
		31	VSS	VSS	32
89 15 BI	MEM_B_DQ<31>	33	DQ10	DQ14	34
89 15 BI	MEM_B_DQ<30>	35	DQ11	DQ15	36
		37	VSS	VSS	38
89 15 BI	MEM_B_DQ<9>	39	DQ16	DQ20	40
89 15 BI	MEM_B_DQ<8>	41	DQ17	DQ21	42
		43	VSS	VSS	44
89 15 BI	MEM_B_DQS_N<1>	45	DQS2*	DM2	46
89 15 BI	MEM_B_DQS_P<1>	47	DQS2	VSS	48
		49	VSS	DQ22	50
89 15 BI	MEM_B_DQ<15>	51	DQ18	DQ23	52
89 15 BI	MEM_B_DQ<10>	53	DQ19	VSS	54
		55	VSS	DQ28	56
89 15 BI	MEM_B_DQ<21>	57	DQ24	DQ29	58
89 15 BI	MEM_B_DQ<17>	59	DQ25	VSS	60
		61	VSS	DQS3*	62
89 15 IN	MEM_B_DM<2>	63	DM3	DQS3	64
		65	VSS	VSS	66
89 15 BI	MEM_B_DQ<18>	67	DQ26	DQ30	68
89 15 BI	MEM_B_DQ<22>	69	DQ27	DQ31	70
		71	VSS	VSS	72

MEM_B_DQ<4> MEM_B_DQ<5>
MEM_B_DQS_N<0> MEM_B_DQS_P<0>
MEM_B_DQ<6> MEM_B_DQ<7>
MEM_B_DQ<29> MEM_B_DQ<25>
MEM_B_DM<3> MEM_RESET_L (IN 27 29)
MEM_B_DQ<26> MEM_B_DQ<27>
MEM_B_DQ<13> MEM_B_DQ<12>
MEM_B_DM<1>
MEM_B_DQ<14> MEM_B_DQ<11>
MEM_B_DQ<20> MEM_B_DQ<16>
MEM_B_DQS_N<2> MEM_B_DQS_P<2>
MEM_B_DQ<19> MEM_B_DQ<23>

516s0706

PP0V75_S3_MEM_VREFCA_B (26)

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

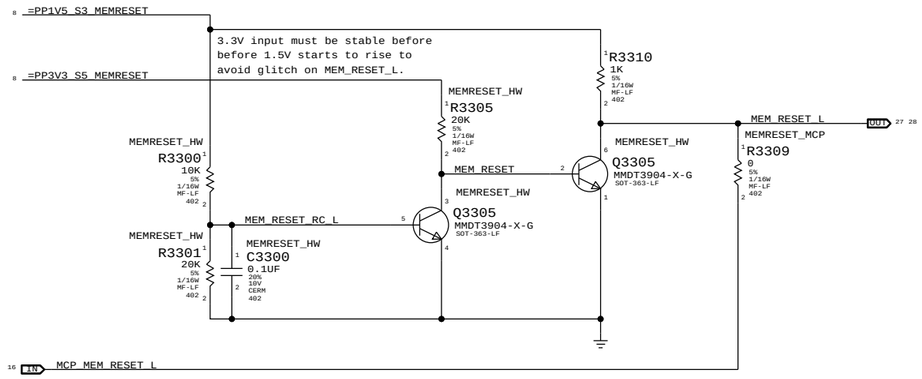
SYNC_MASTER=BEN_K20 SYNC_DATE=07/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 28 OF 98	

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support			
SYNC_MASTER=M98_MLB	SYNC_DATE=04/01/2008		
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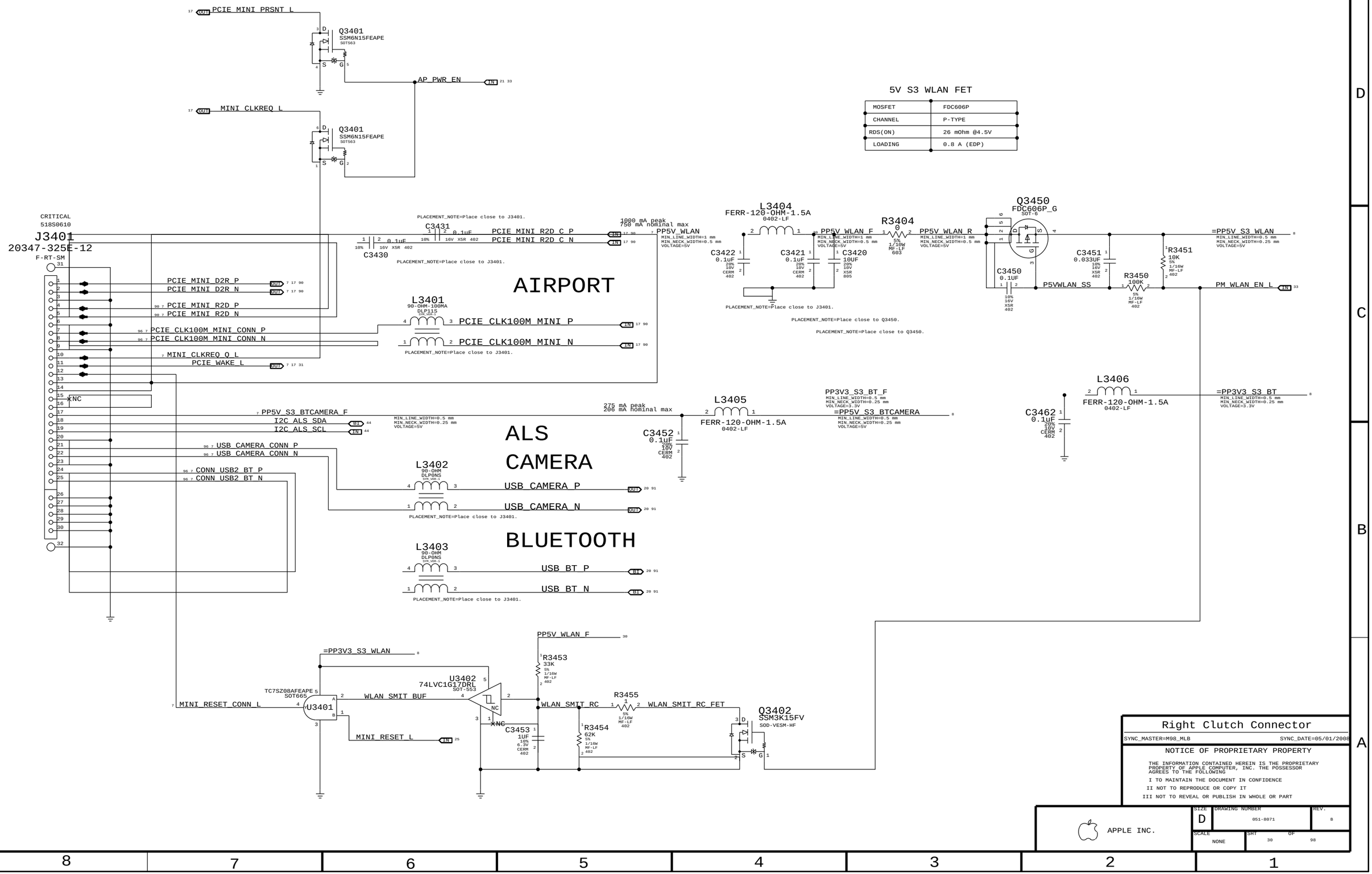
APPLE INC.	SIZE D	DRAWING NUMBER 051-8071	REV. 8
	SCALE NONE	SHT 29 OF 98	


PCIE MINI PRSNT L
Q3401
SSM6N15FEAPE
SOT563
AP PWR EN
MINI CLKREQ L
Q3401
SSM6N15FEAPE
SOT563
5V S3 WLAN FET
MOSFET | FDC606P
CHANNEL | P-TYPE
RDS(ON) | 26 mOhm @4.5V
LOADING | 0.8 A (EDP)
CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM
PCIE MINI D2R P
PCIE MINI D2R N
PCIE MINI R2D P
PCIE MINI R2D N
PCIE CLK100M MINI CONN P
PCIE CLK100M MINI CONN N
MINI CLKREQ O L
PCIE WAKE L
NC
USB CAMERA CONN P
USB CAMERA CONN N
CONN USB2 BT P
CONN USB2 BT N
PLACEMENT_NOTE=Place close to J3401.
C3431
0.1uF
C3430
0.1uF
PCIE MINI R2D C P
PCIE MINI R2D C N
1000 mA peak
750 mA nominal max
PP5V_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V
AIRPORT
L3401
90-OHM-100MA
DLP11S
PCIE CLK100M MINI P
PCIE CLK100M MINI N
L3404
FERR-120-OHM-1.5A
0402-LF
C3422
0.1uF
C3421
0.1uF
C3420
10UF
R3404
0
1/10W
MF-LF
603
PP5V_WLAN_F
PP5V_WLAN_R
PLACEMENT_NOTE=Place close to Q3450.
Q3450
FDC606P_G
SOT-6
C3450
0.1UF
C3451
0.033UF
R3450
100K
R3451
10K
P5VWLAN_SS
=PP5V_S3_WLAN
PM_WLAN_EN_L
ALS
CAMERA
L3402
90-OHM
DLP0NS
USB_CAMERA_P
USB_CAMERA_N
BLUETOOTH
L3403
90-OHM
DLP0NS
USB_BT_P
USB_BT_N
L3405
FERR-120-OHM-1.5A
0402-LF
275 mA peak
206 mA nominal max
PP3V3_S3_BT_F
=PP5V_S3_BTCAMERA
C3452
0.1uF
PP5V_S3_BTCAMERA_F
I2C_ALS_SDA
I2C_ALS_SCL
L3406
FERR-120-OHM-1.5A
0402-LF
=PP3V3_S3_BT
C3462
0.1uF
=PP3V3_S3_WLAN
PP5V_WLAN_F
U3402
74LVC1G17DRL
SOT-353
TC7SZ08AFEAPE
SOT665
U3401
MINI_RESET_CONN_L
WLAN_SMIT_BUF
MINI_RESET_L
R3453
33K
R3454
62K
R3455
1
C3453
1UF
WLAN_SMIT_RC
WLAN_SMIT_RC_FET
Q3402
SSM3K15FV
SOD-VESM-HF
Right Clutch Connector
SYNC_MASTER=M98_MLB
SYNC_DATE=05/01/2008
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REV. 8
SCALE NONE
SHT 30 OF 98

EXPRESSCARD/34 FLEX CONNECTOR

INPUT DECOUPLING

31 8 =PP3V3_S3_EXCARD
- C3530 0.1uF 20% 10V CERM 402
- C3531 10uF 20% 6.3V X5R 603

31 8 =PP1V5_S0_EXCARD
- C3534 0.1uF 20% 10V CERM 402
- C3535 10uF 20% 6.3V X5R 603

OMIT
- R3504 SHORT (31 8 =PP3V3_S3_EXCARD) NONE NONE NONE NONE 402
- R3503 SHORT (31 8 =PP3V3_S0_EXCARD) NONE NONE NONE NONE 402
- R3502 SHORT (31 8 =PP1V5_S0_EXCARD) NONE NONE NONE 402

L3502
90-OHM DLP0NS SYM_VER-1

91 29 BI USB_EXCARD_N — 4 — 3 — USB2_EXCARD_CONN_N 7 31 96

91 29 BI USB_EXCARD_P — 1 — 2 — USB2_EXCARD_CONN_P 7 31 96

PLACEMENT_NOTE=Place close to J3500

L3503
90-OHM-100MA DLP11S SYM_VER-1

90 17 IN PCIE_CLK100M_EXCARD_N — 4 — 3 — PCIE_CLK100M_EXCARD_CONN_N 7 31 96

90 17 IN PCIE_CLK100M_EXCARD_P — 1 — 2 — PCIE_CLK100M_EXCARD_CONN_P 7 31 96

PLACEMENT_NOTE=Place close to J3500

PLACEMENT_NOTE=Place close to J3500

C3571 / C3570
90 17 IN PCIE_EXCARD_R2D_C_N — C3571 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_N 7 31 90

90 17 IN PCIE_EXCARD_R2D_C_P — C3570 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_P 7 31 90

PLACEMENT_NOTE=Place close to J3500

CRITICAL J3500 502250-0627
FCI-SSF

		29	
90 31 7	PCIE_EXCARD_R2D_N	24	25 PCIE_EXCARD_R2D_P 7 31 90
90 17 7 OUT	PCIE_EXCARD_D2R_P	22	23 PCIE_EXCARD_D2R_N OUT 7 17 90
		20	21 PCIE_CLK100M_EXCARD_CONN_P 7 31 96
96 31 7	PCIE_CLK100M_EXCARD_CONN_N	18	19 EXCARD_CPPE_L 7 31
31 7	EXCARD_CLKREQ_CONN_L	16	17 PP3V3_S0_EXCARD_SWITCH 7 31
31 7	PP3V3_S0_EXCARD_SWITCH	14	15 PLT_RESET_SWITCH_L 7 31
31 7	PP3V3_S3_EXCARD_SWITCH	12	13 PCIE_WAKE_L OUT 7 17 30
31 7	PP1V5_S0_EXCARD_SWITCH	10	11 PP1V5_S0_EXCARD_SWITCH 7 31
44 BI	=SMBUS_EXCARD_SDA	8	9 =SMBUS_EXCARD_SCL BI 44
NC		6	7
31 7	EXCARD_CPUSB_L	4	5 NC
96 31 7	USB2_EXCARD_CONN_N	2	3 USB2_EXCARD_CONN_P 7 31 96
			1
		28	

518S0647

R3501
31 7 EXCARD_CPPE_L — R3501 0 MF-LF 402 5% 1/10W — PCIE_EXCARD_PRSNT_L 17

OUTPUT DECOUPLING

CRITICAL U3500 TPS2231 QFN

PP3V3_S3_EXCARD_R	17 AUXIN	AUXOUT 15	PP3V3_S3_EXCARD_SWITCH 7 31
PP3V3_S0_EXCARD_R	2 VIN3P3	VOUT3P3 3	
PP1V5_S0_EXCARD_R	12 VIN1P5	VOUT1P5 11	PP3V3_S0_EXCARD_SWITCH 7 31
		PERST* 8	PP1V5_S0_EXCARD_SWITCH 7 31
		CPPE* 10	PLT_RESET_SWITCH_L 7 31
		CPUSB* 9	EXCARD_CPPE_L 7 31
			EXCARD_CPUSB_L 7 31
NC	4 NC0	RCLKEN 18	EXCARD_RCLKEN 31
NC	5 NC1		
NC	13 NC2		
NC	14 NC3		
NC	16 NC4	THRML_PAD 21	
		GND	

VOLTAGE=3.3V — C3500 0.1uF 20% 10V CERM 402 — C3503 10uF 20% 6.3V X5R 603

VOLTAGE=3.3V — C3501 0.1uF 10% 16V X5R 402 — C3504 10uF 20% 6.3V X5R 603

VOLTAGE=1.5V — C3502 0.1uF 10% 16V X5R 402 — C3505 10uF 20% 6.3V X5R 603

41 IN SMC_EXCARD_PWR_EN — R3500 0 MF-LF 402 5% 1/10W — EXCARD_SHDN_L_R 28 SHDN*

TP_EXCARD_STBY_L 1 STBY*

25 IN EXCARD_RESET_L 6 SYSRST*

42 28 IN EXCARD_OC_L 13 OC*

U3551
31 8 =PP3V3_S3_EXCARD

31 7 EXCARD_CPUSB_L → 1

31 7 EXCARD_CPPE_L → 2

74HC1G00GWDG SC70-5 — 5 VCC, 4 SMC_EXCARD_CP OUT 41 42, 3 GND

C3550 0.1uF 20% 10V CERM 402

U3560 / U3561
31 8 =PP3V3_S0_EXCARD

R3561 100K 1% 1/10W MF-LF 402

31 EXCARD_RCLKEN → U3560 1

EXCARD_CLKREQ_CONN → U3560 2

U3560 74HC1G00GWDG SC70-5 — 5 VCC, 3 EXCARD_CLKREQ_L OUT 17

31 7 EXCARD_CLKREQ_CONN_L → U3561 B1

U3561 SN74LVC1G04YZPR BGA — A2 VCC, C2 Y, C1 GND

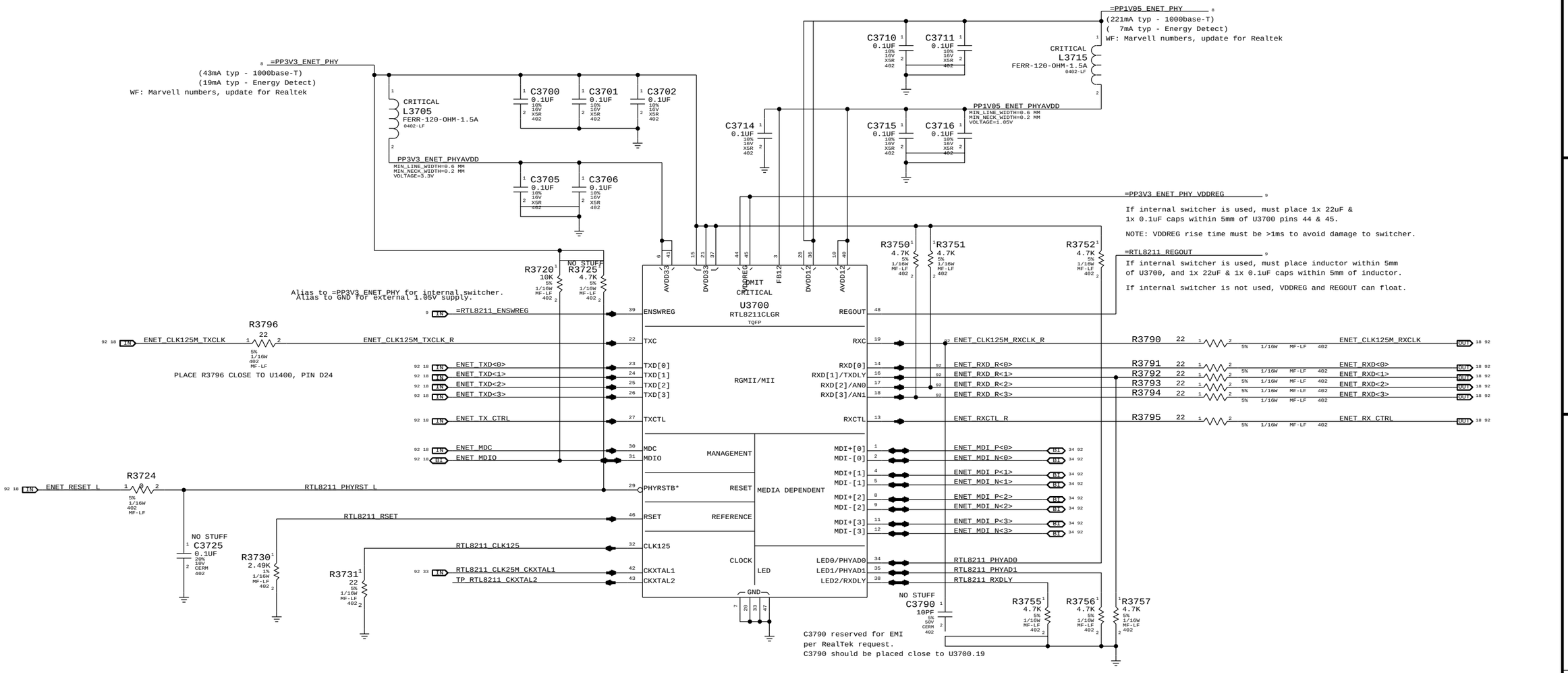
C3560 0.1uF 20% 10V CERM 402

ExpressCard Connector

SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 31 OF 98	



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

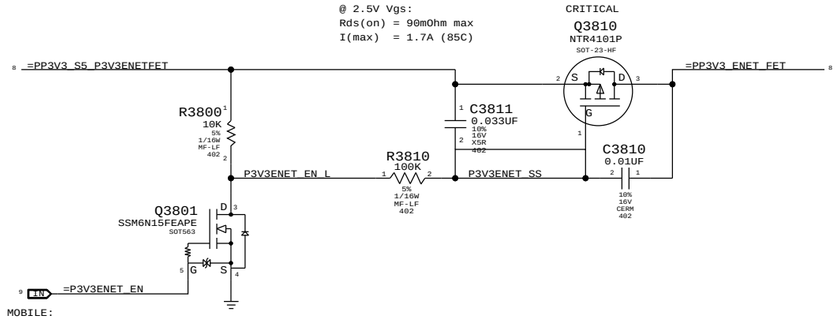
Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 32 OF 98	

3.3V ENET FET



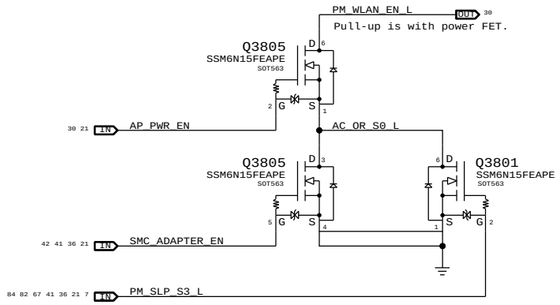
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

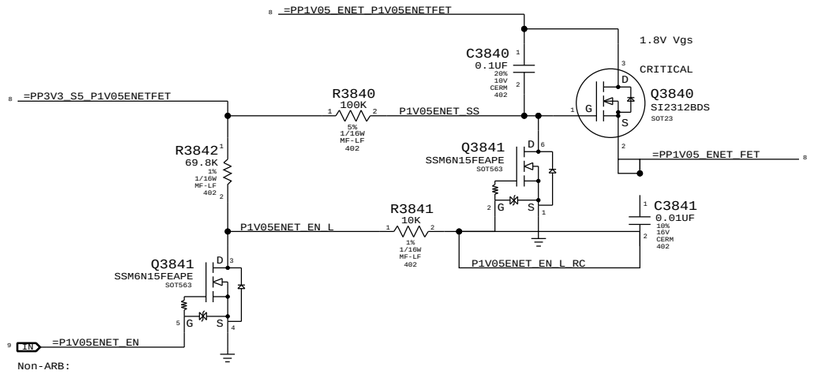
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET

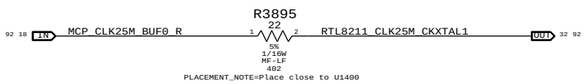


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



Ethernet & AirPort Support

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

APPLE INC.

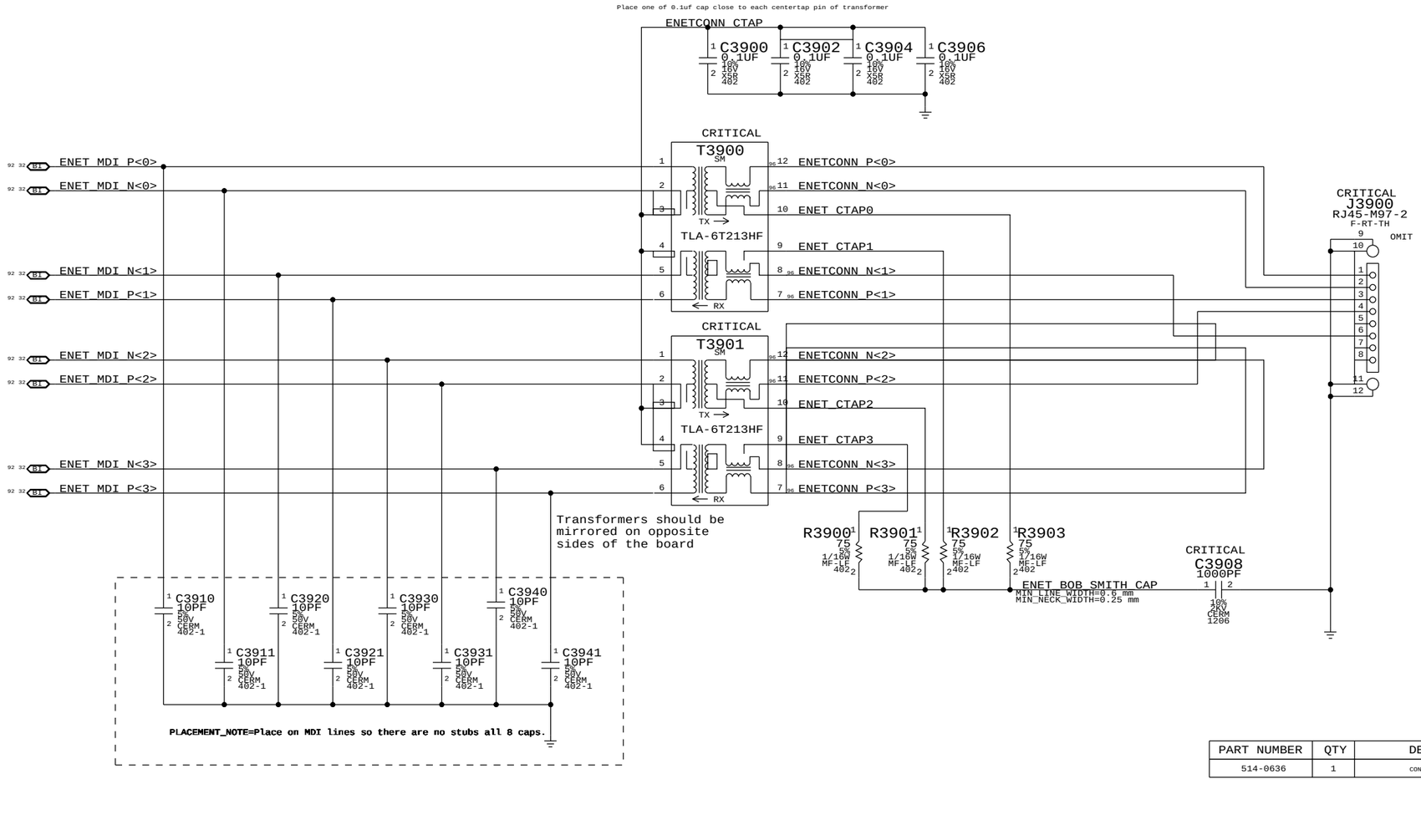
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 33 OF 98	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



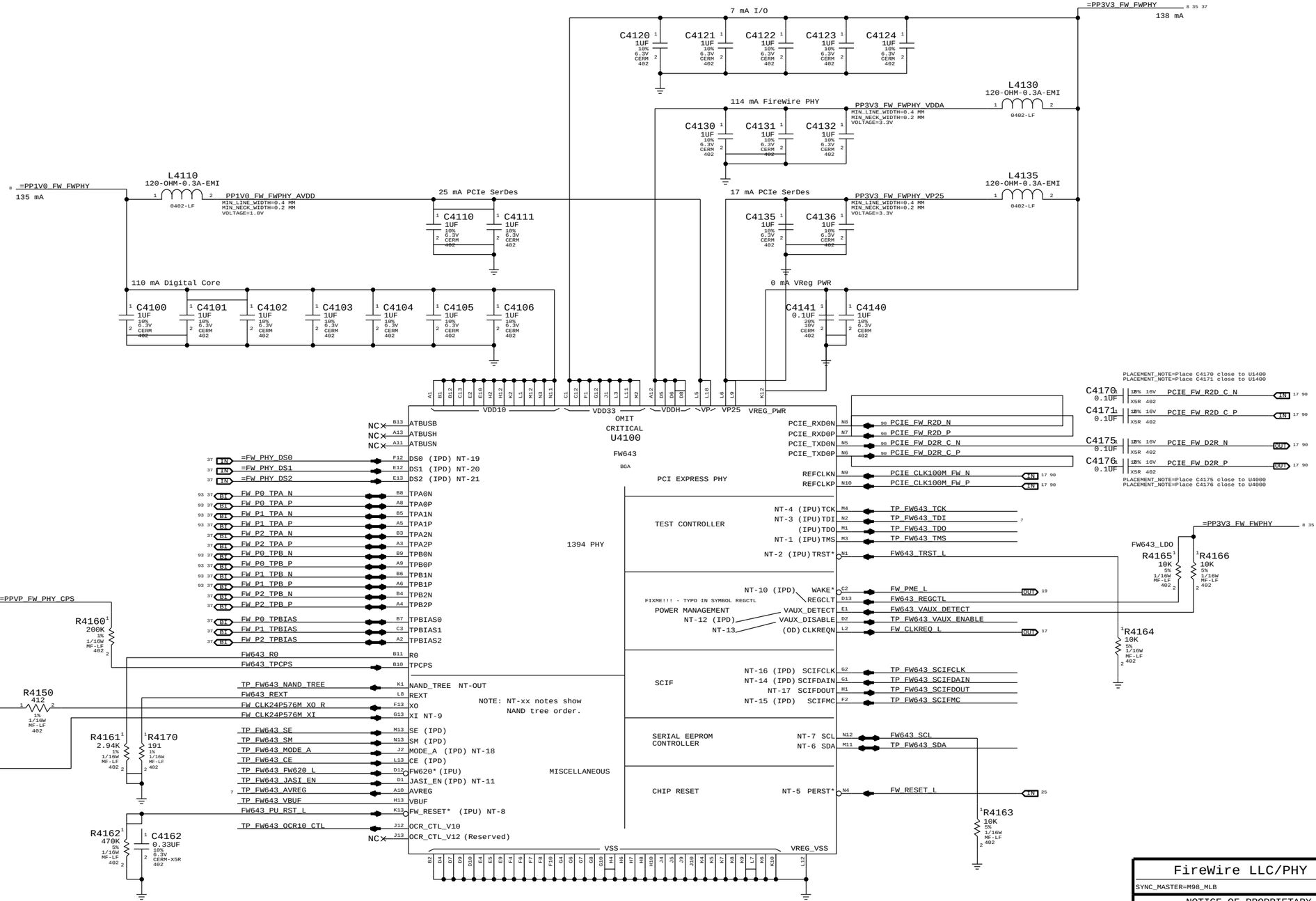
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0636	1	CONN,RJ45,HB,10/100TX	J3900	CRITICAL	

Ethernet Connector

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 34 OF 98	



FireWire LLC/PHY (FW643)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 35 OF 98	

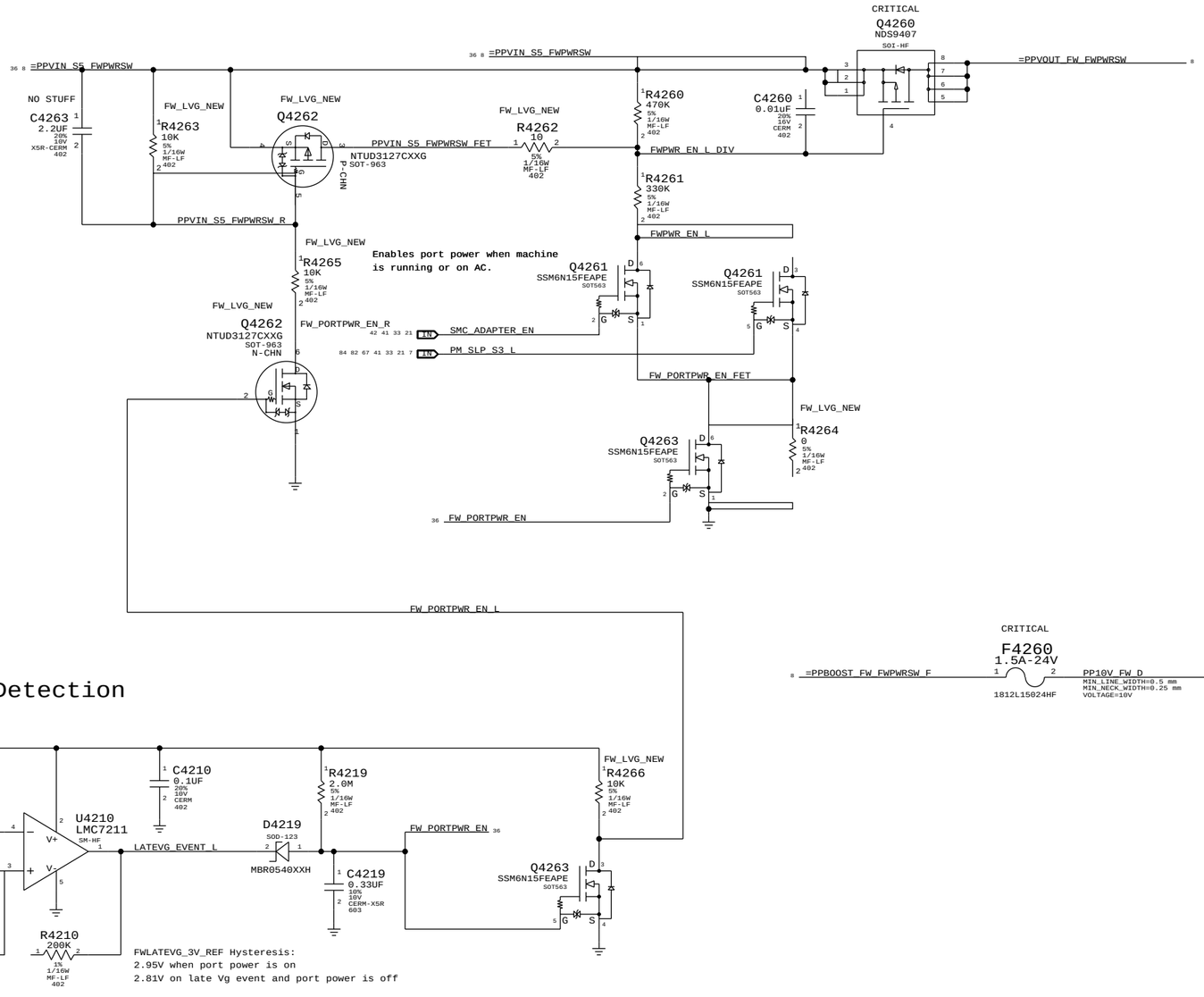
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection

FireWire Port Power

SYNC_MASTER=YWU_K20 SYNC_DATE=05/28/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	36	98

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

37 35 8 =PP3V3_FW_FWPHY

R4382 10K 1% 1/16W MF-LF 402
R4380 10K 1% 1/16W MF-LF 402
R4381 10K 1% 1/16W MF-LF 402

FWPHY_DS0 (MAKE_BASE=TRUE) = =FW_PHY_DS0 (35)
FWPHY_DS2 (MAKE_BASE=TRUE) = =FW_PHY_DS2 (35)
FWPHY_DS1 (MAKE_BASE=TRUE) = =FW_PHY_DS1 (35)

35 FW_P0_TPBIAS = NC_FW0_TPBIAS (MAKE_BASE=TRUE)
35 FW_P2_TPBIAS = NC_FW2_TPBIAS (MAKE_BASE=TRUE) 7
93 35 FW_P0_TPA_N = NC_FW0_TPAN (MAKE_BASE=TRUE)
93 35 FW_P0_TPA_P = NC_FW0_TPAP (MAKE_BASE=TRUE) 7
35 FW_P2_TPA_N = NC_FW2_TPAN (MAKE_BASE=TRUE) 7
35 FW_P2_TPA_P = NC_FW2_TPAP (MAKE_BASE=TRUE) 7
93 35 FW_P0_TPB_N = NC_FW0_TPBN (MAKE_BASE=TRUE) 7
93 35 FW_P0_TPB_P = NC_FW0_TPBP (MAKE_BASE=TRUE) 7
35 FW_P2_TPB_N = NC_FW2_TPBN (MAKE_BASE=TRUE) 7
35 FW_P2_TPB_P = NC_FW2_TPBP (MAKE_BASE=TRUE) 7

Termination

Place close to FireWire PHY

35 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY
R4360 56.2 1% 1/16W MF-LF 402
R4361 56.2 1% 1/16W MF-LF 402

93 35 FW_P1_TPA_P = FW_PORT1_TPA_P (MAKE_BASE=TRUE) 37
93 35 FW_P1_TPA_N = FW_PORT1_TPA_N (MAKE_BASE=TRUE) 37
93 35 FW_P1_TPB_P = FW_PORT1_TPB_P (MAKE_BASE=TRUE) 37
93 35 FW_P1_TPB_N = FW_PORT1_TPB_N (MAKE_BASE=TRUE) 37

SIGNAL_MODEL=EMPTY
R4362 56.2 1% 1/16W MF-LF 402
R4363 56.2 1% 1/16W MF-LF 402

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402
R4364 4.99K 1% 1/16W MF-LF 402

8 =PPVP_FW_PHY_CPS_FET

Q4300 (SYM_VER_1) BSS8402DW

R4311 470K 5% 1/16W MF-LF 402

PPVP_FW_CPS (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=10V) (MAKE_BASE=TRUE) = =PPVP_FW_PHY_CPS (35)

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

Q4300 BSS8402DW SOT-363 (SYM-VER1)

37 35 8 =PP3V3_FW_FWPHY

"Snapback" & "Late VG" Protection

37 36 PP2V4_FW_LATEVG

DP4310 BAV99DW-X-G SOT-363
C4311 0.01uF 10% 50V X7R 402
DP4310 BAV99DW-X-G SOT-363
C4310 0.01uF 10% 50V X7R 402

37 FW_PORT1_TPB_N
37 FW_PORT1_TPB_P

DP4311 BAV99DW-X-G SOT-363
C4312 0.01uF 10% 50V X7R 402
DP4311 BAV99DW-X-G SOT-363
C4313 0.01uF 10% 50V X7R 402

37 FW_PORT1_TPA_N
37 FW_PORT1_TPA_P

C4319 0.1uF 10% 50V X7R 603-1
R4319 1M 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

Cable Power

8 =PPVP_FW_PORT1

CRITICAL
L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=33V)

C4314 0.01UF 10% 50V X7R 402

PORT 1

BILINGUAL

CRITICAL
J4310 1394B-M97 F-RT-TH

1	TPB-	TPB(R)	TPB-
9	TPB+	VP	TPB<R>
8			TPB+
7	NC	SC/NC	VP
6			NC
3	TPA-	VG	VG
5			TPA-
4	TPA+	TPA(R)	TPA<R>
10			TPA+
11	CHASSIS GND		
12			
13			

OUTPUT
INPUT

(FW_PORT1_BREF)
(GND_FW_PORT1_VG)
FW_PORT1_AREF

514S0605

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

Late-VG Protection Power

8 =PP3V3_FW_LATEVG

R4390 332 1% 1/16W MF-LF 402

PP2V4_FW_LATEVG (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.4V) 36 37

CRITICAL
D4390 MMBZ5227BLT1H SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

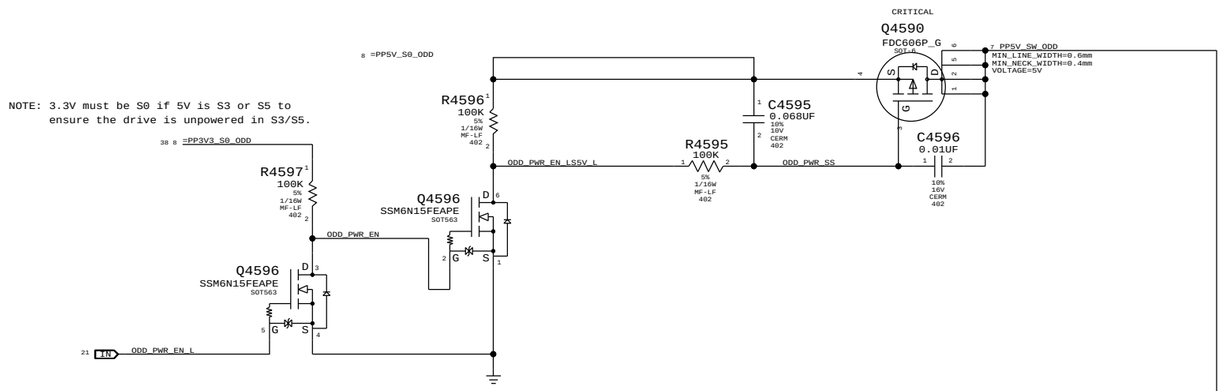
FireWire Ports

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

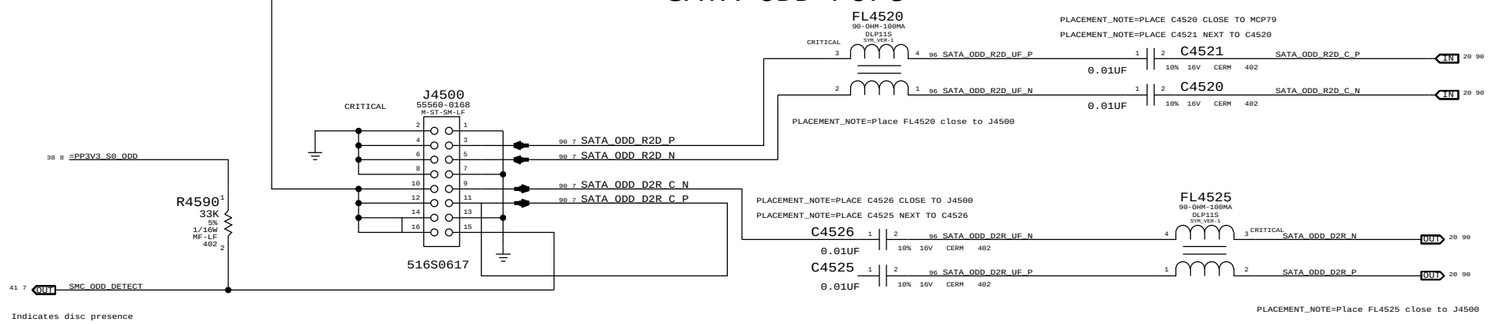
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 37 OF 98	

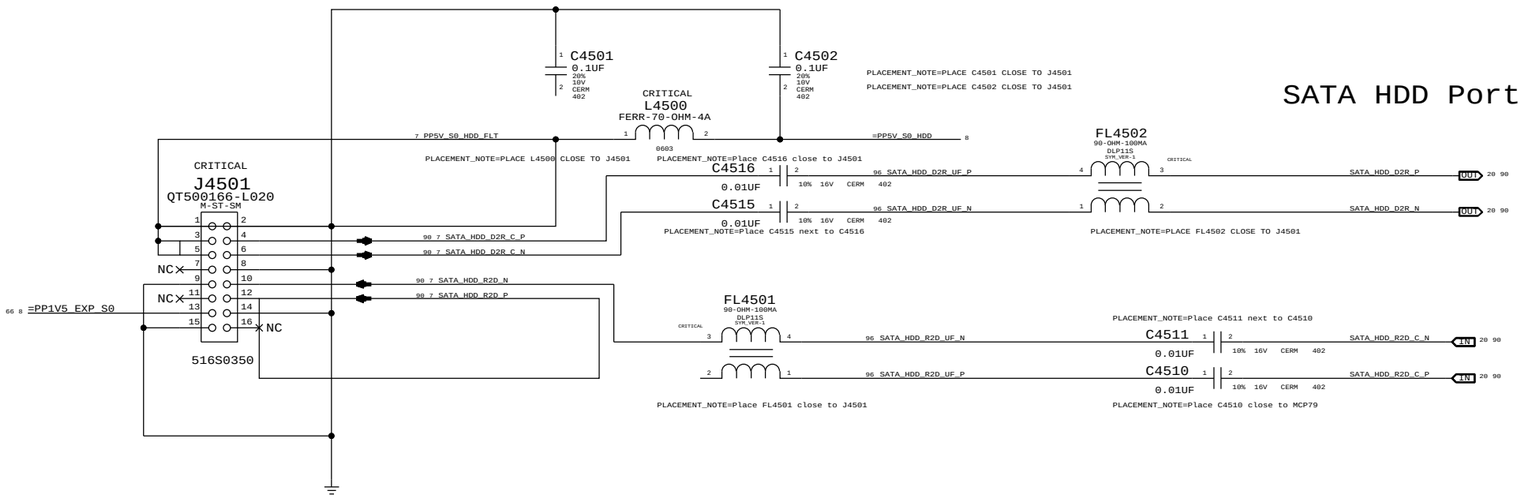
ODD Power Control



SATA ODD Port



SATA HDD Port



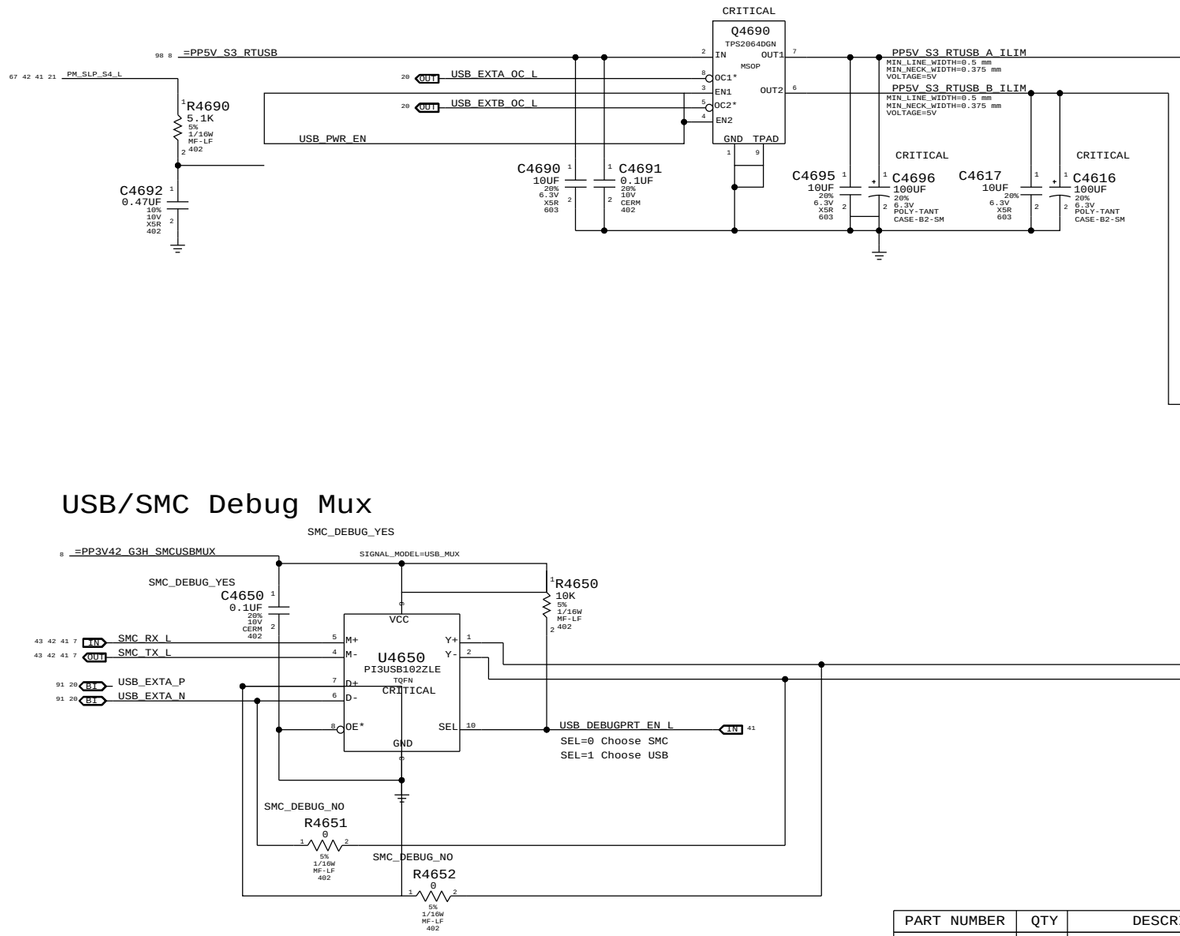
SATA Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

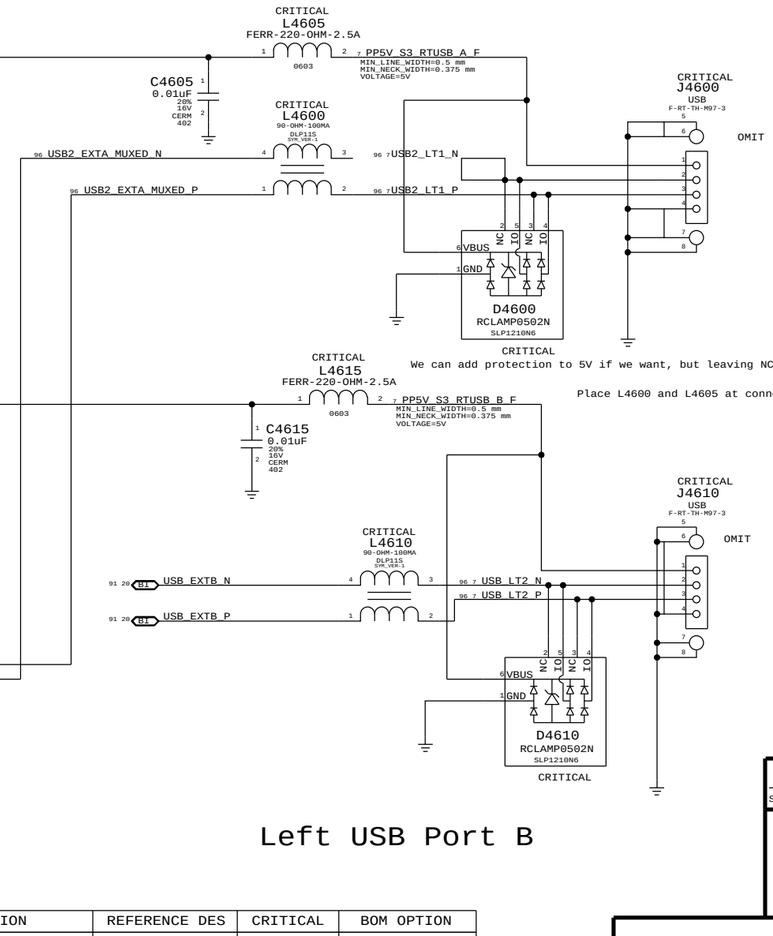
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	38	98

Port Power Switch



Left USB Port A



USB/SMC Debug Mux

Left USB Port B

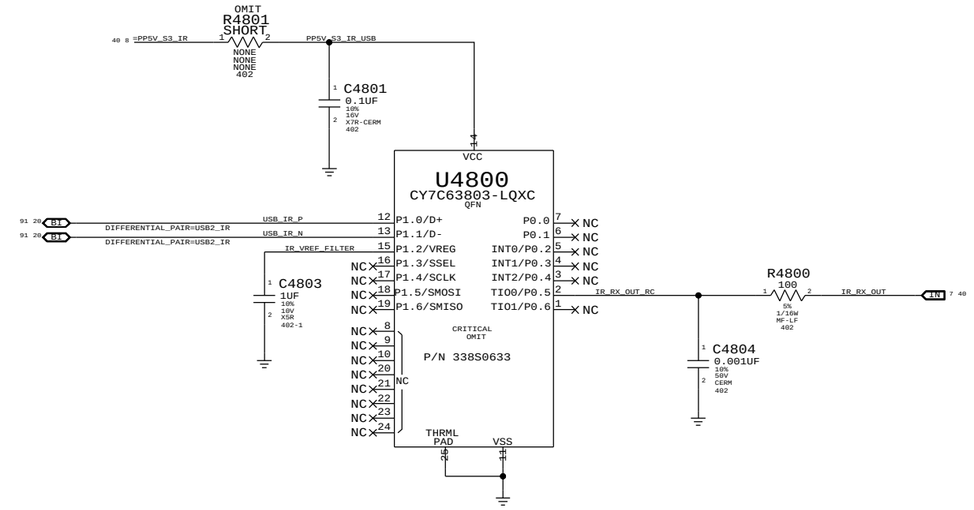
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	2	CONN,RCPT,USB,HB,4P	J4600, J4610	CRITICAL	

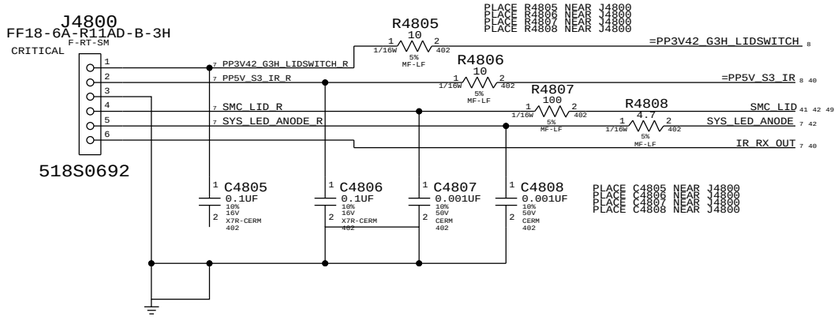
External USB Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 39 OF 98	





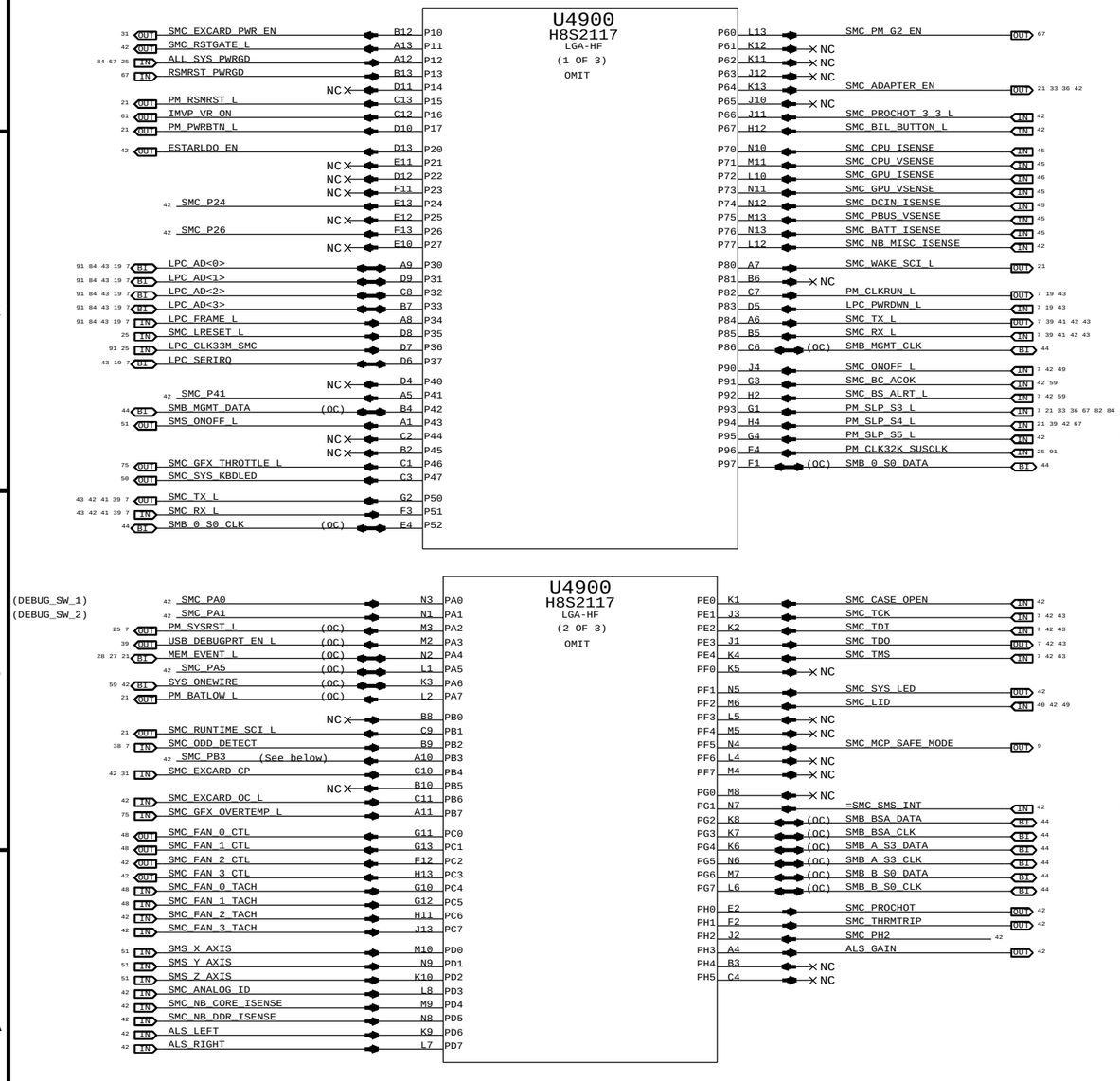
Front Flex Support

SYNC_MASTER=CHANG_K20 SYNC_DATE=07/18/2008

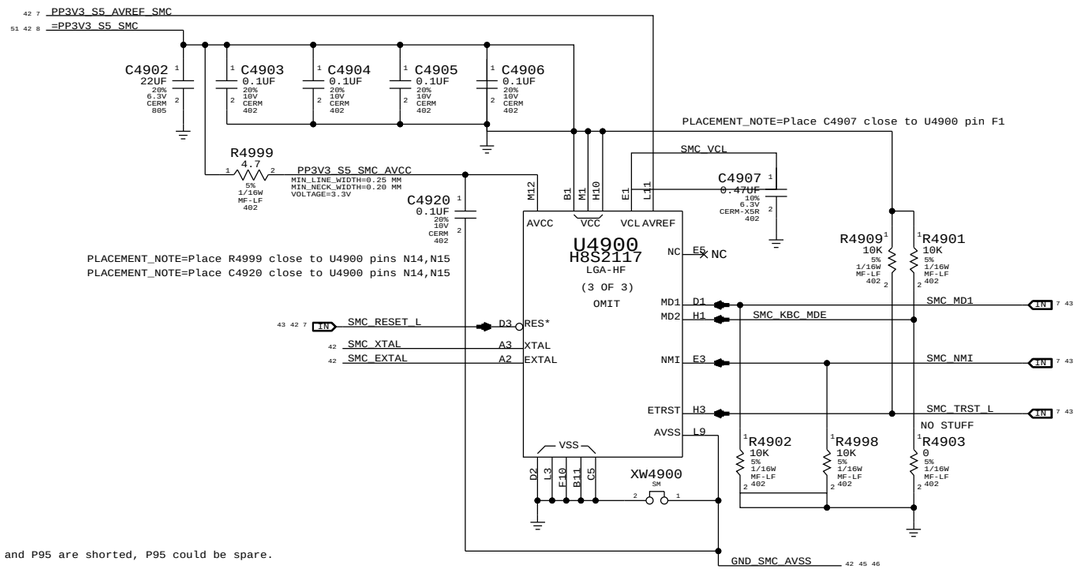
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	40	98

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted, P95 could be spare.



NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SMC		
SYNC_MASTER=T18_MLB	SYNC_DATE=06/06/2008	
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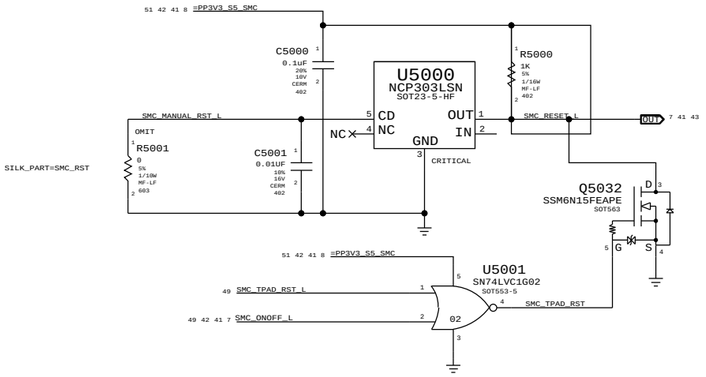
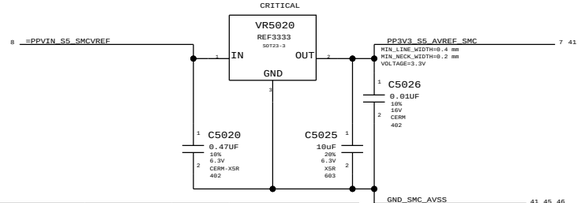
APPLE INC.	SIZE: D	DRAWING NUMBER: 051-8071
	REV: 8	
	SCALE: NONE	SHT: 41 OF 98

SMC Reset "Button" / Brownout Detect

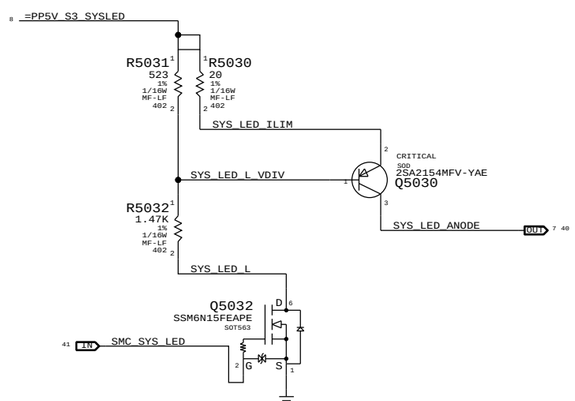


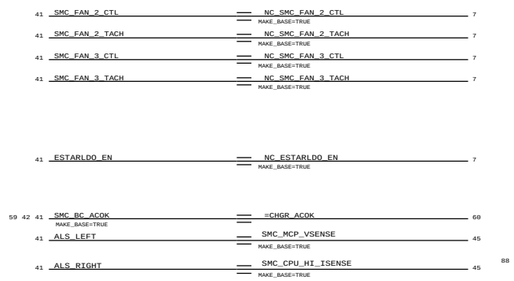
SMC AVREF Supply

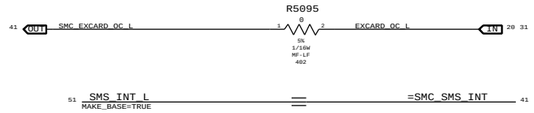


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

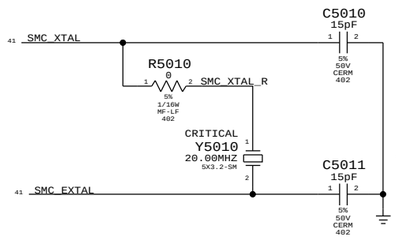
System (Sleep) LED Circuit



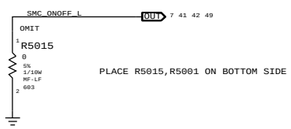




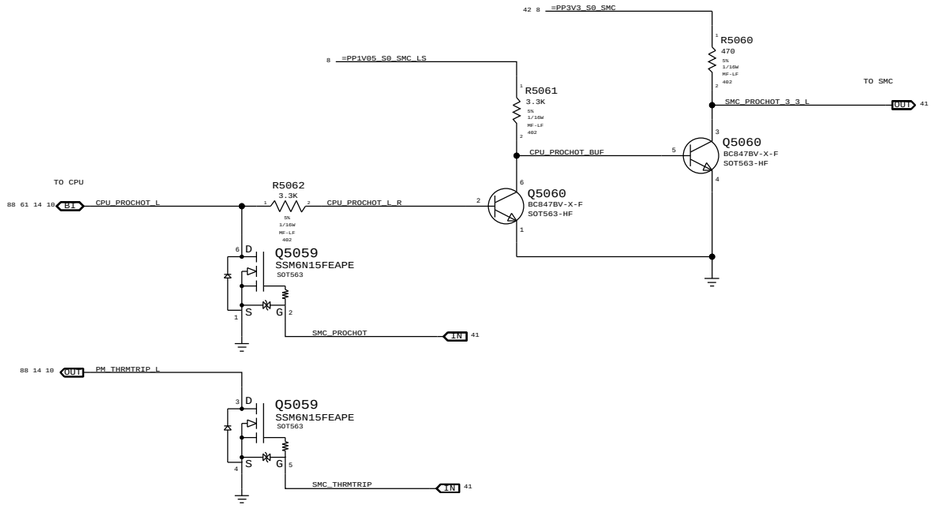
SMC Crystal Circuit

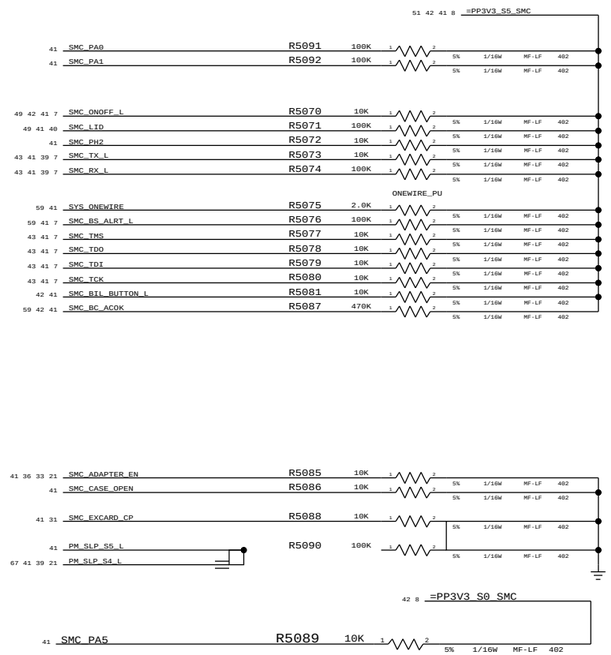


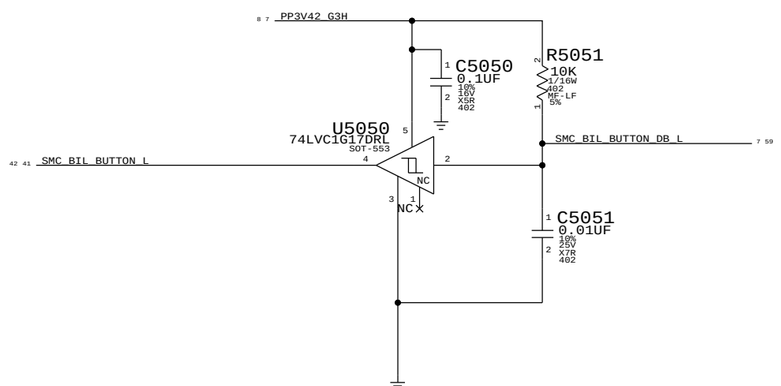
Debug Power "Button"



SMC FSB to 3.3V Level Shifting







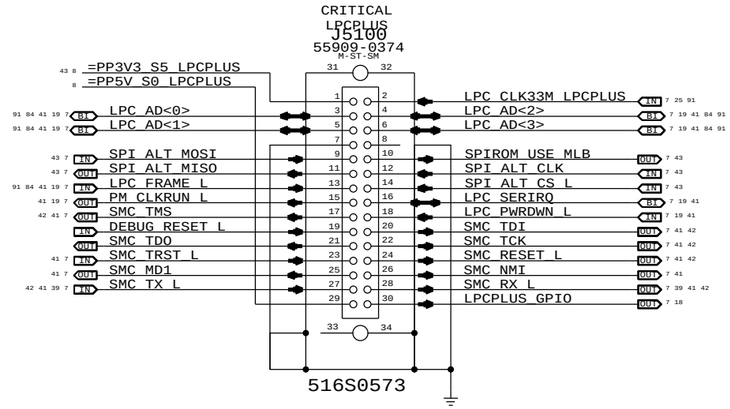
SMC Support

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

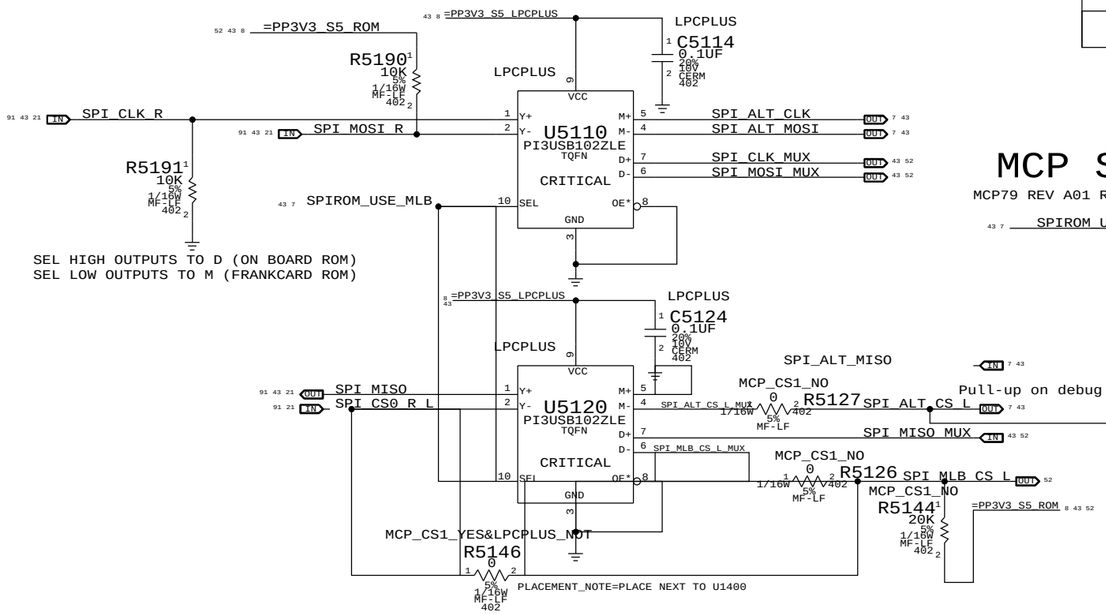
SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 42 OF 98	

LPC+SPI Connector



Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

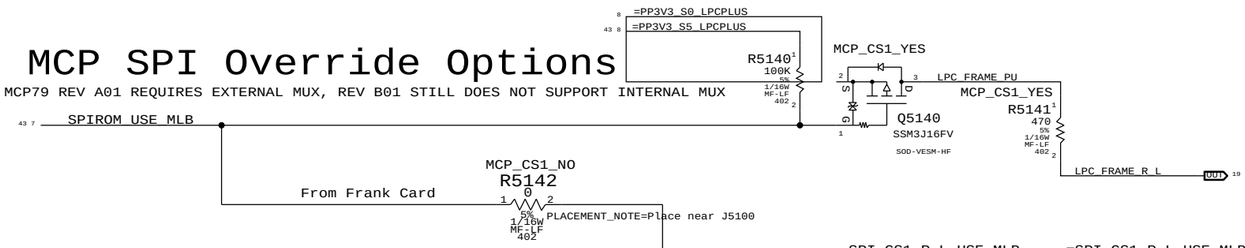


MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

MCP SPI Override Options

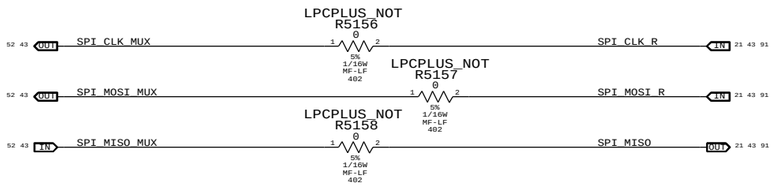
MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX



SPI_CS1_R_L_USE_MLB = =SPI_CS1_R_L_USE_MLB

MAKE_BASE=TRUE

SPI MUX BYPASS



LPC+SPI Debug Connector

SYNC_MASTER=CHANG_K20 SYNC_DATE=05/28/2008

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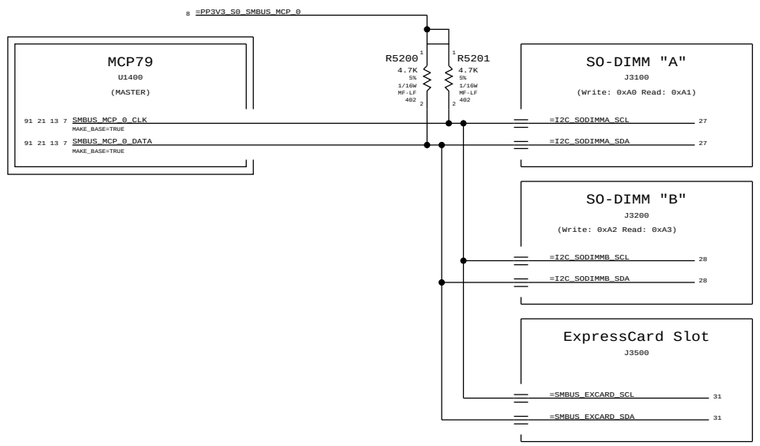
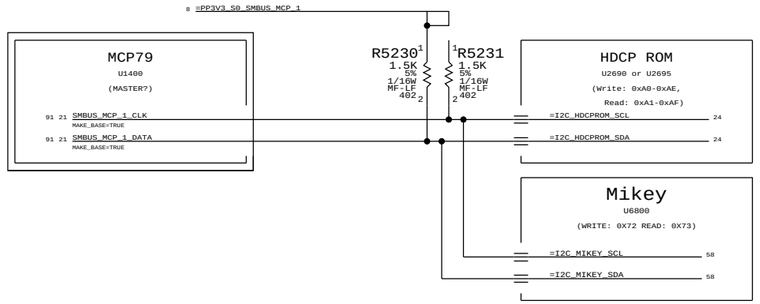
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 43 OF 98	

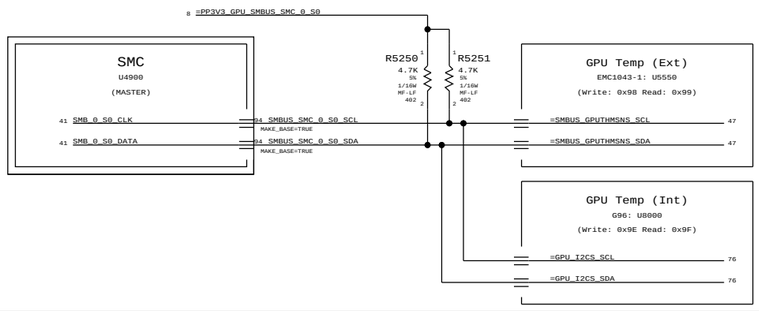
MCP79 SMBus "0" Connections



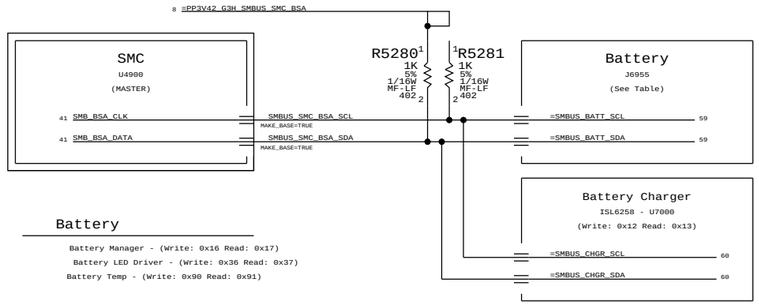
MCP79 SMBus "1" Connections



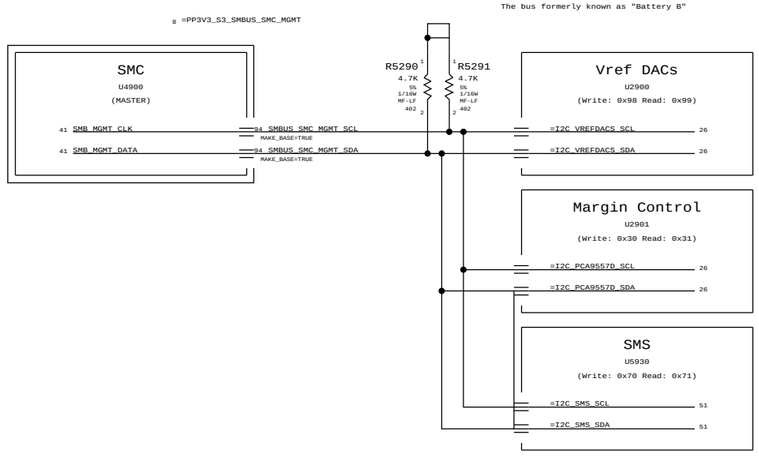
SMC "0" SMBus Connections



SMC "Battery A" SMBus Connections

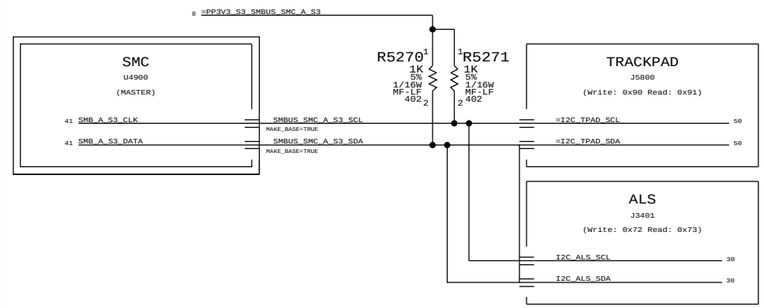


SMC "Management" SMBus Connections

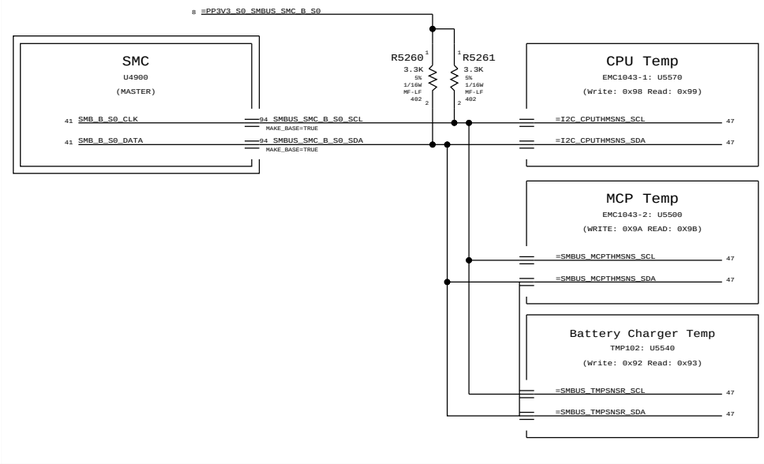


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "B" SMBus Connections

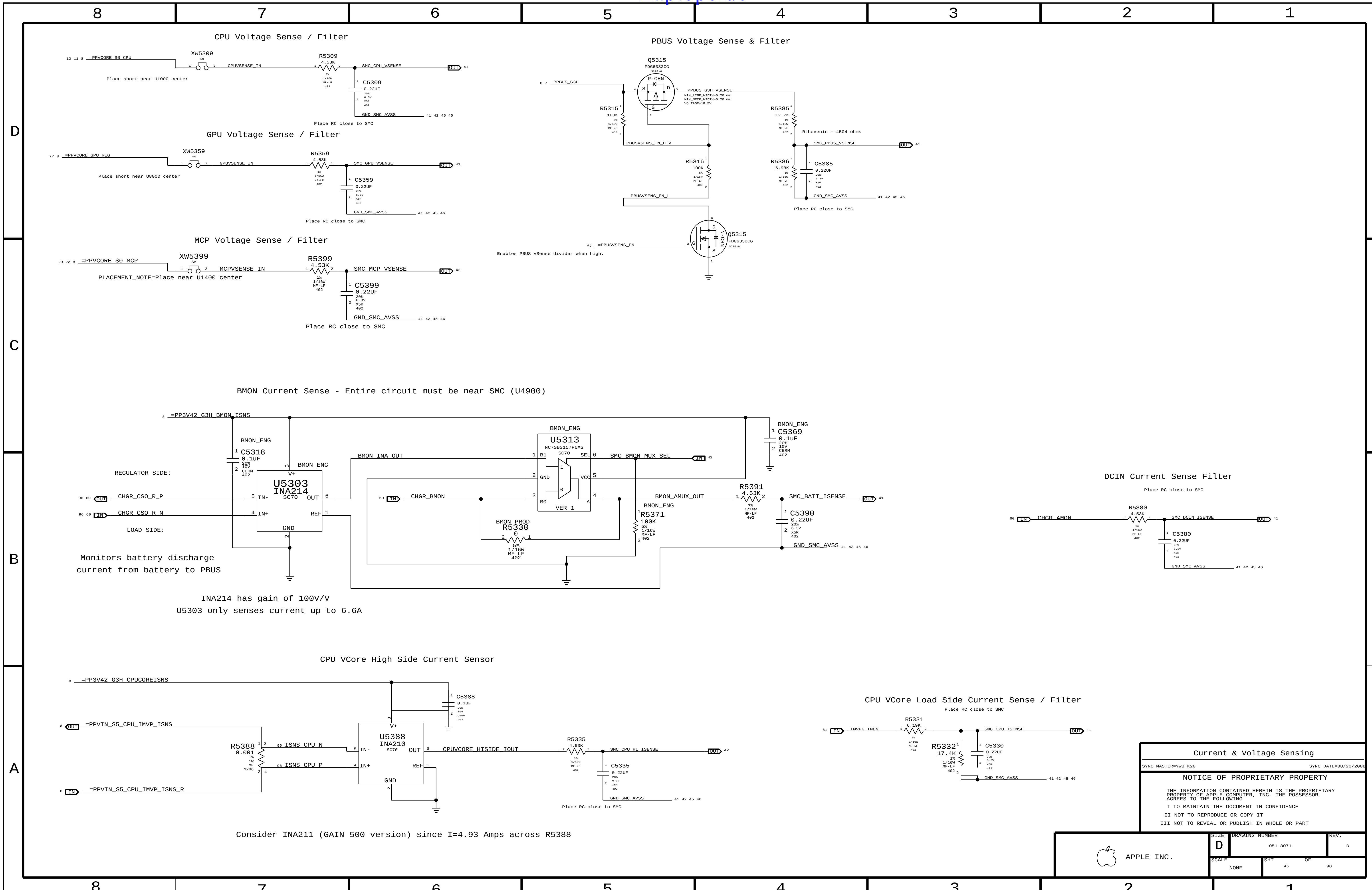


K20 SMBUS CONNECTIONS

SYNC_MASTER=BEN_K20 SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 44 OF 98	


CPU Voltage Sense / Filter
=PPVCORE_S0_CPU
XW5309
CPUVSENSE_IN
R5309
4.53K
SMC_CPU_VSENSE
OUT
C5309
0.22UF
GND_SMC_AVSS
Place short near U1000 center
Place RC close to SMC
GPU Voltage Sense / Filter
=PPVCORE_GPU_REG
XW5359
GPUVSENSE_IN
R5359
4.53K
SMC_GPU_VSENSE
C5359
0.22UF
Place short near U8000 center
MCP Voltage Sense / Filter
=PPVCORE_S0_MCP
XW5399
MCPVSENSE_IN
R5399
4.53K
SMC_MCP_VSENSE
C5399
0.22UF
PLACEMENT_NOTE=Place near U1400 center
PBUS Voltage Sense & Filter
Q5315
FDG6332CG
P-CHN
PPBUS_G3H
PPBUS_G3H_VSENSE
R5315
100K
R5385
12.7K
Rthevenin = 4504 ohms
PBUSVSENS_EN_DIV
SMC_PBUS_VSENSE
R5316
100K
R5386
6.98K
C5385
0.22UF
PBUSVSENS_EN_L
N-CHN
=PBUSVSENS_EN
Enables PBUS VSense divider when high.
BMON Current Sense - Entire circuit must be near SMC (U4900)
=PP3V42_G3H_BMON_ISNS
BMON_ENG
C5318
0.1UF
REGULATOR SIDE:
U5303
INA214
SC70
CHGR_CSO_R_P
CHGR_CSO_R_N
LOAD SIDE:
BMON_INA_OUT
U5313
NC7SB3157P6XG
SMC_BMON_MUX_SEL
CHGR_BMON
BMON_AMUX_OUT
BMON_PROD
R5330
0
R5371
100K
R5391
4.53K
SMC_BATT_ISENSE
C5390
0.22UF
C5369
0.1uF
Monitors battery discharge current from battery to PBUS
INA214 has gain of 100V/V
U5303 only senses current up to 6.6A
DCIN Current Sense Filter
Place RC close to SMC
CHGR_AMON
R5380
4.53K
SMC_DCIN_ISENSE
C5380
0.22UF
CPU VCore High Side Current Sensor
=PP3V42_G3H_CPUCOREISNS
C5388
0.1UF
=PPVIN_S5_CPU_IMVP_ISNS
R5388
0.001
ISNS_CPU_N
ISNS_CPU_P
U5388
INA210
CPUVCORE_HISIDE_IOUT
R5335
4.53K
SMC_CPU_HI_ISENSE
C5335
0.22UF
=PPVIN_S5_CPU_IMVP_ISNS_R
Consider INA211 (GAIN 500 version) since I=4.93 Amps across R5388
CPU VCore Load Side Current Sense / Filter
Place RC close to SMC
IMVP6_IMON
R5331
6.19K
SMC_CPU_ISENSE
R5332
17.4K
C5330
0.22UF
Current & Voltage Sensing
SYNC_MASTER=YWU_K20
SYNC_DATE=08/20/2008
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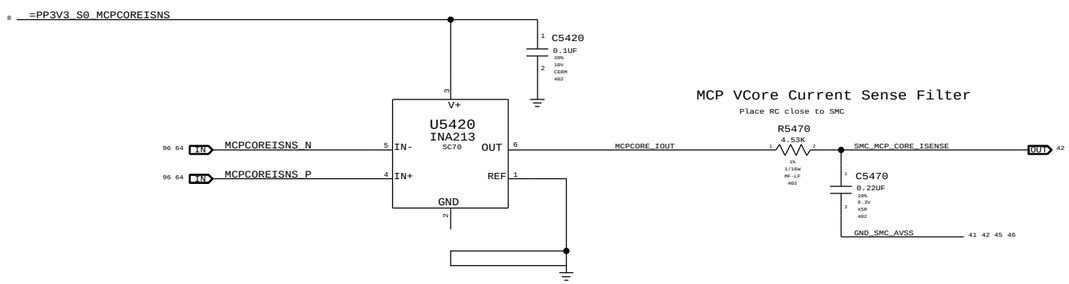
APPLE INC.
SIZE D
DRAWING NUMBER 051-8071
REV. 8
SCALE NONE
SHT 45 OF 98

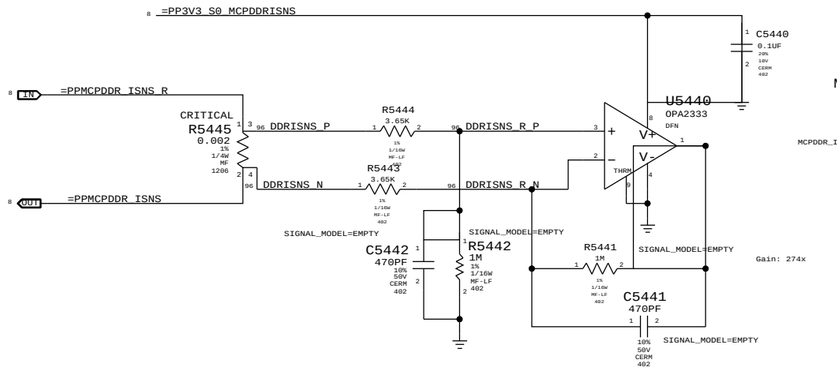
MCP VCore Current Sense



MCP VCore Current Sense Filter

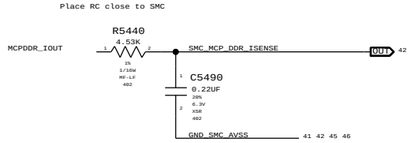
Place RC close to SMC

MCP MEM VDD Current Sense



MCP MEM VDD Current Sense Filter

Place RC close to SMC

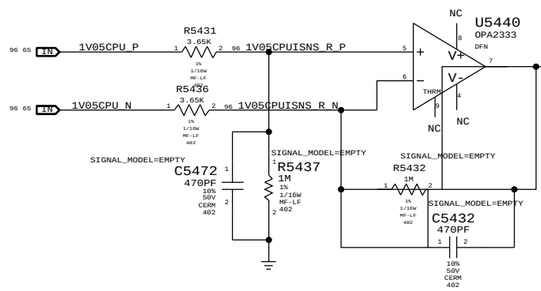


Gain: 274x

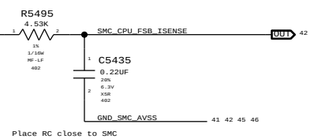
OPA2333s for proto are placeholders for OPA2330

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

CPU FSB 1.05V Current Sense



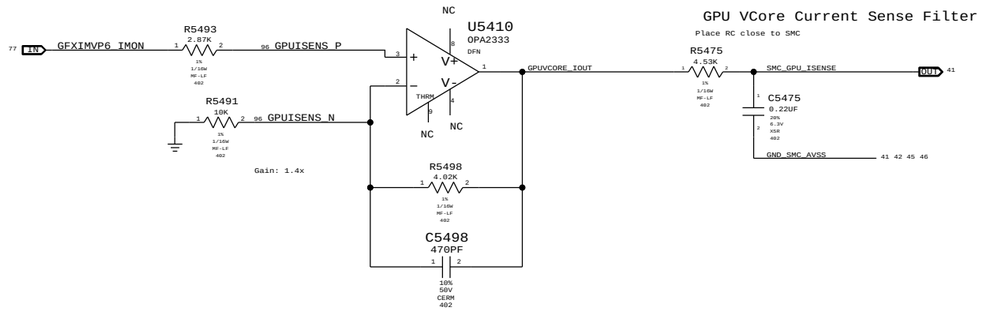
1.05V CPU Current Sense Filter



Place RC close to SMC

Gain: 274x

GPU VCore Current Sense



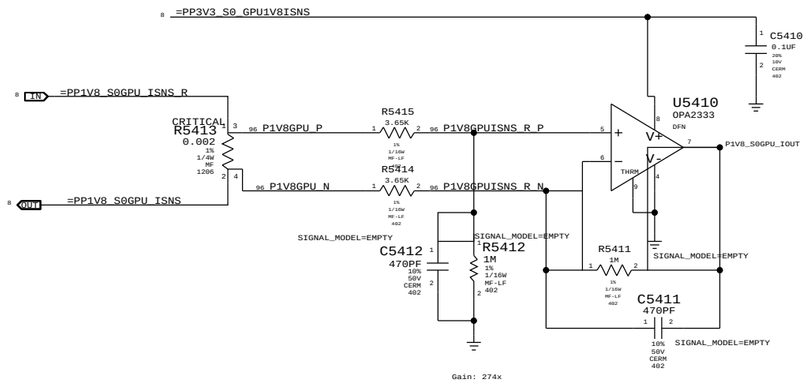
GPU VCore Current Sense Filter

Place RC close to SMC

Gain: 1.4x

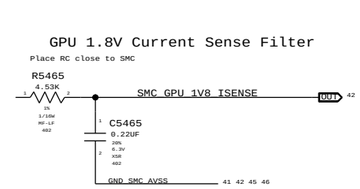
GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

GPU 1.8V Current Sense



GPU 1.8V Current Sense Filter

Place RC close to SMC



Gain: 274x

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

Current Sensing

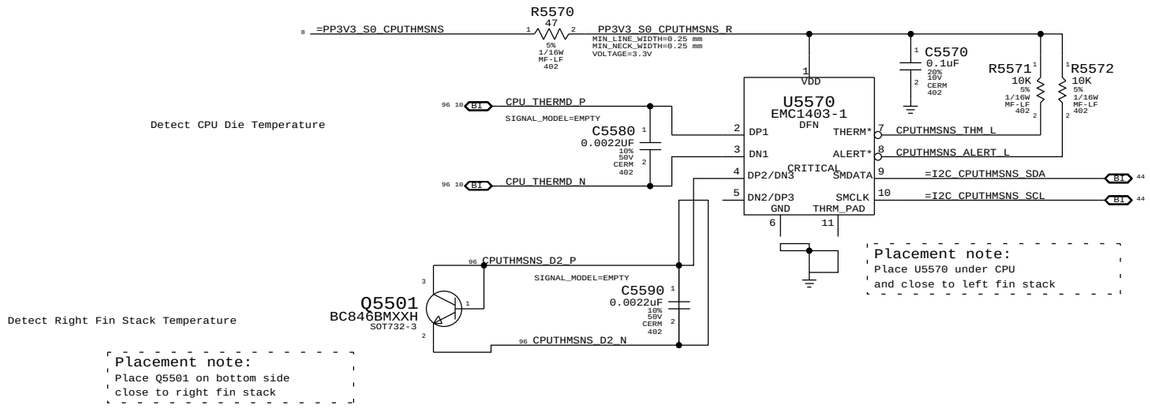
SYNC_MASTER=YWU_K20 SYNC_DATE=08/12/2008

NOTICE OF PROPRIETARY PROPERTY

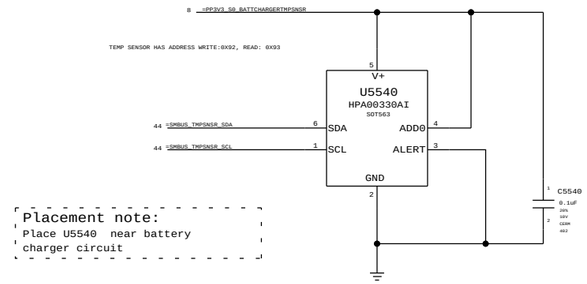
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	46	98

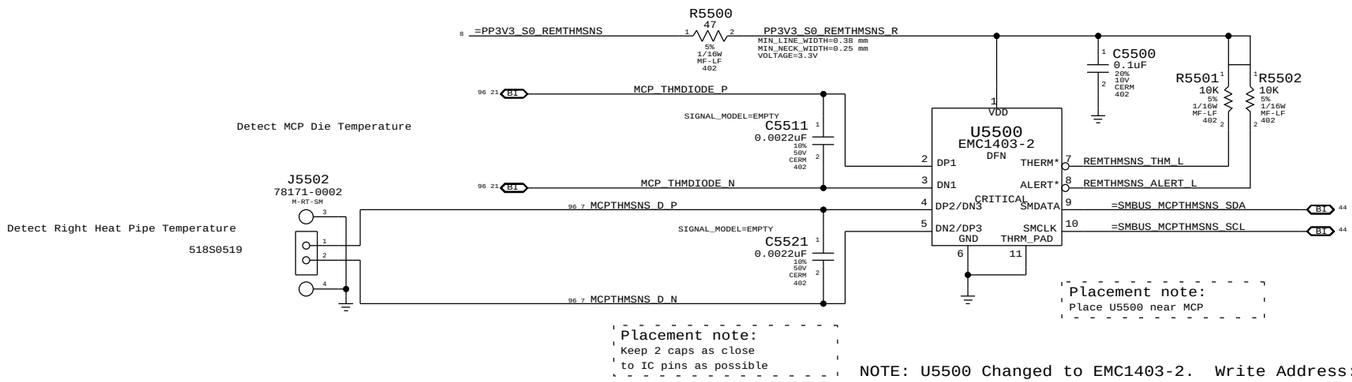
CPU Proximity/CPU Die/Right Fin Stack



Battery Charger Proximity



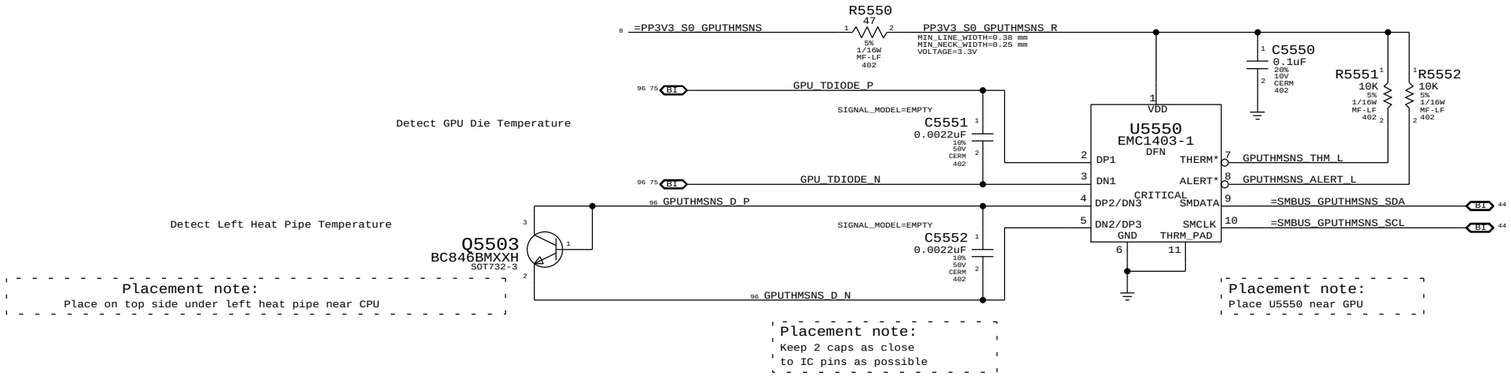
MCP Proximity/MCP Die/Right Heat Pipe



NOTE: U5500 Changed to EMC1403-2. Write Address: 0x9A

Note: EMC1403 can perform Beta
Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe



NOTE: U5550 Changed to EMC1403-1. Write Address: 0x98

Thermal Sensors		
SYNC_MASTER=YWU_K20	SYNC_DATE=05/28/2008	
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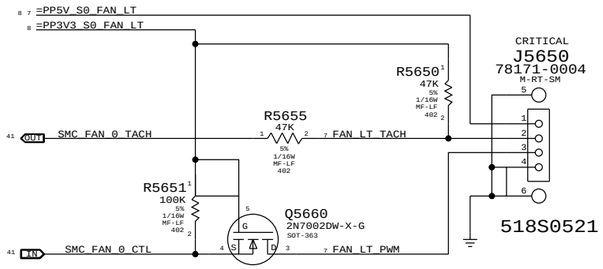
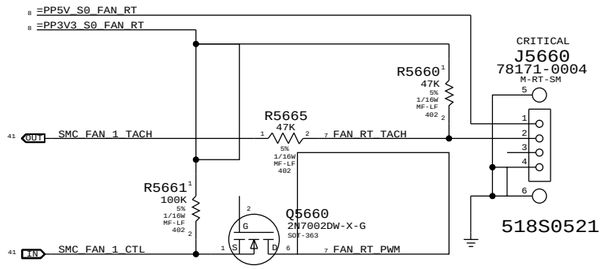
APPLE INC.	SIZE: D	DRAWING NUMBER: 051-8071
	REV: 8	
	SCALE: NONE	SHT 47 OF 98

Left Fan



Right Fan



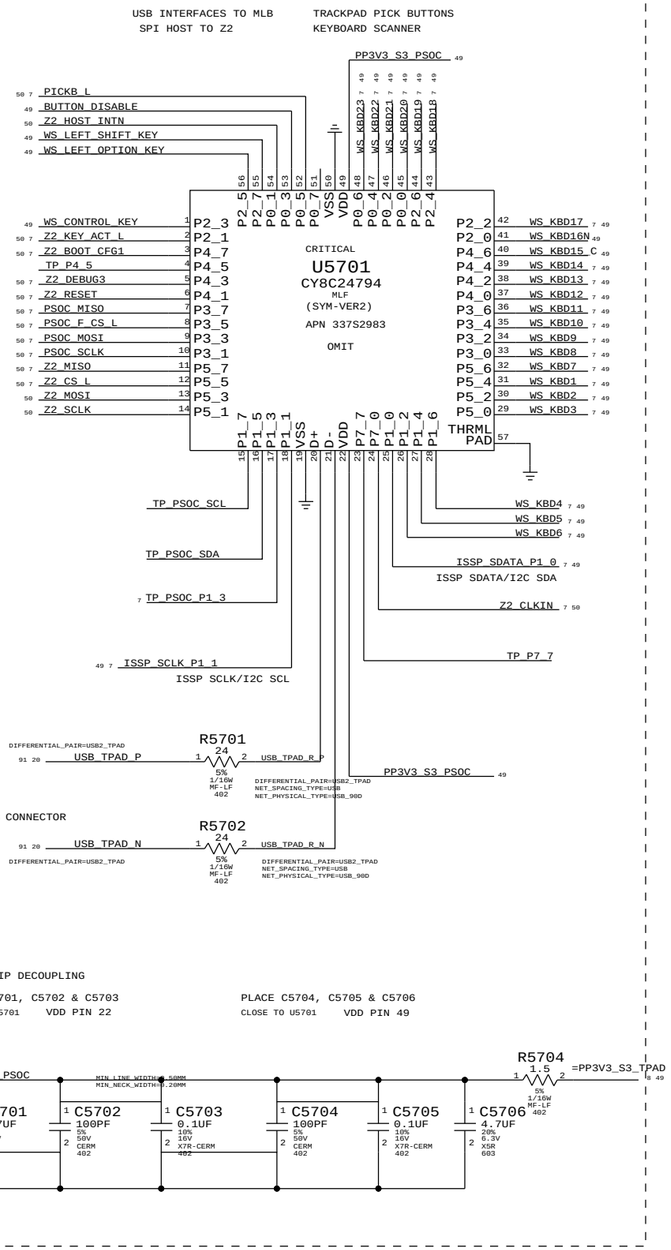
Fan Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 48 OF 98	

PSOC USB CONTROLLER



U5701 CHIP DECOUPLING

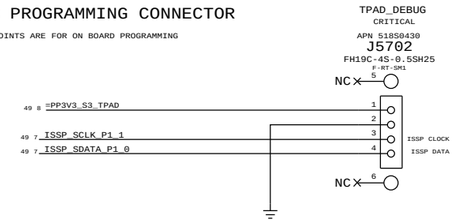
PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

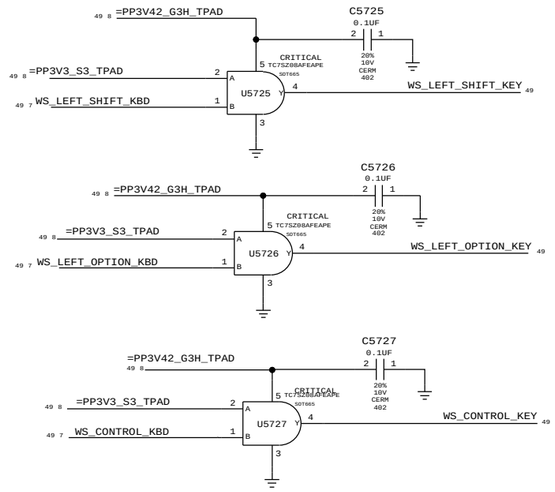
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

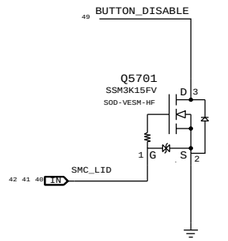
TEST POINTS ARE FOR ON BOARD PROGRAMMING



ISOLATION CIRCUIT



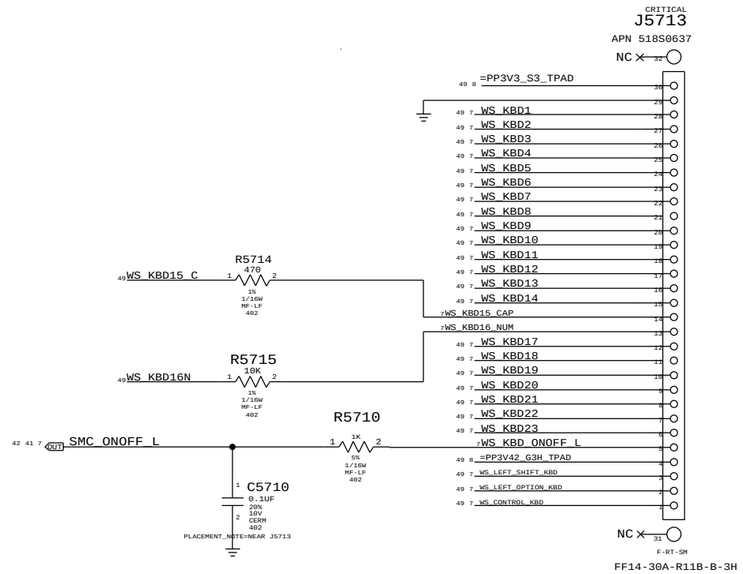
TPAD BUTTONS DISABLE



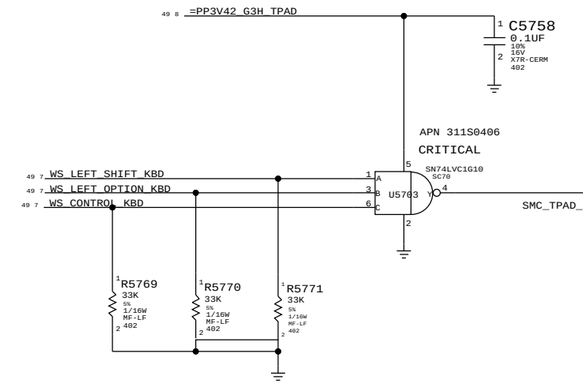
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC

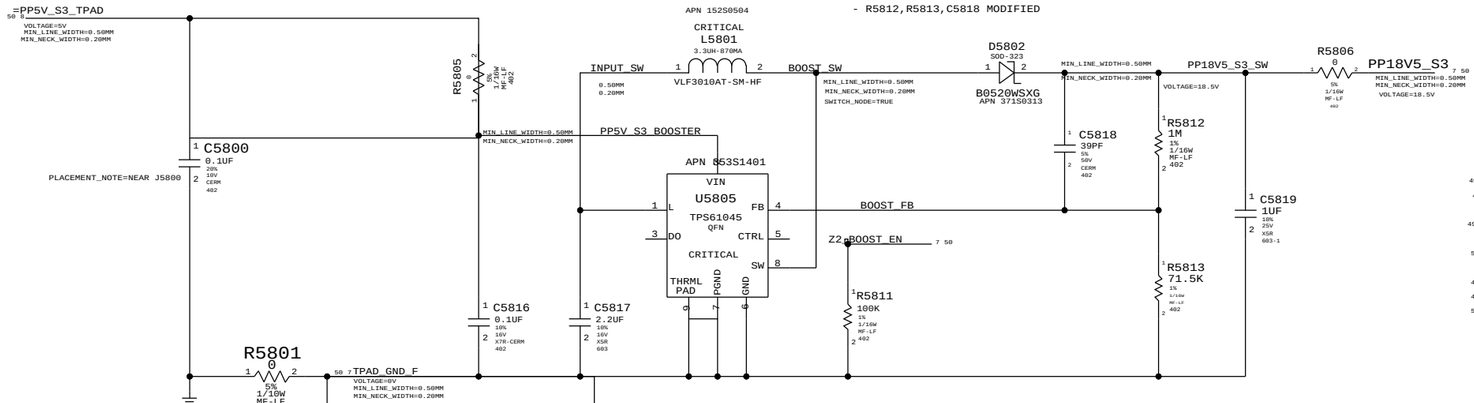


APPLE INC.

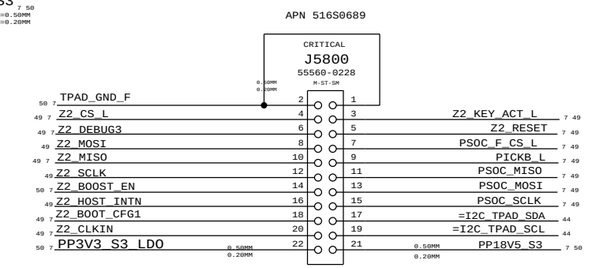
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 49 OF 98	

BOOSTER +18.5VDC FOR SENSORS

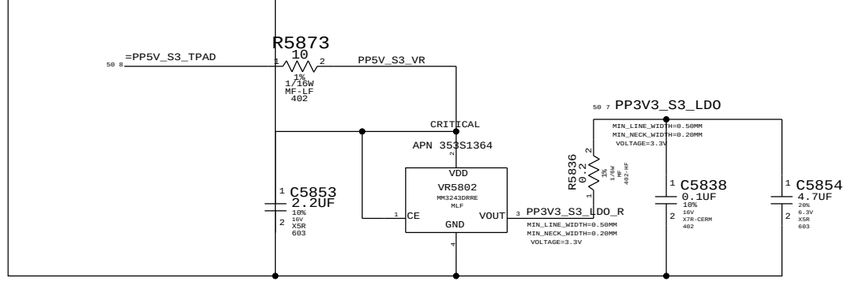
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD



Keyboard LED Driver

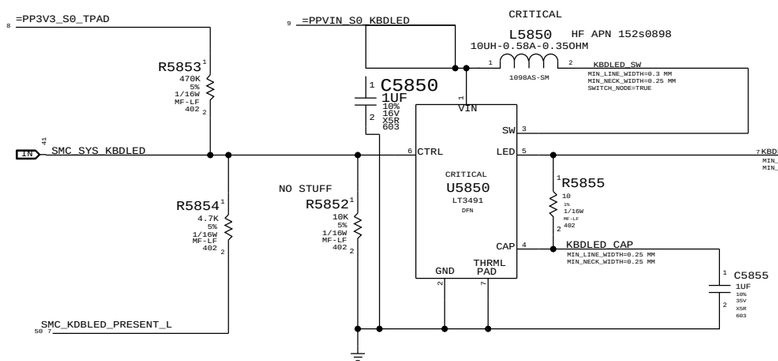
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

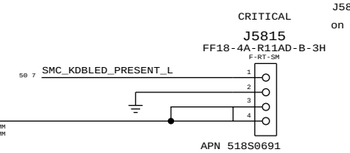
LOW = keyboard backlight present

HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT





J5815 pin 1 is grounded on keyboard backlight flex

KBD BACKLIGHT CONNECTOR

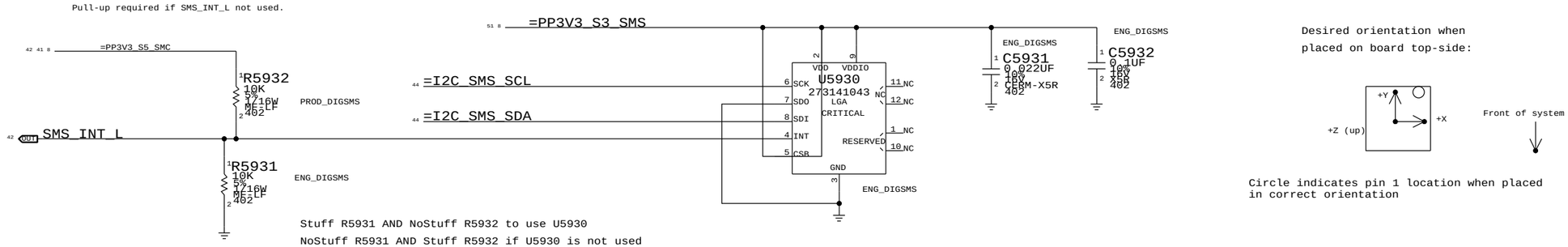
SYNC_MASTER=K20_MLB	SYNC_DATE=09/24/2008

WELLSPRING 2

APPLE INC.

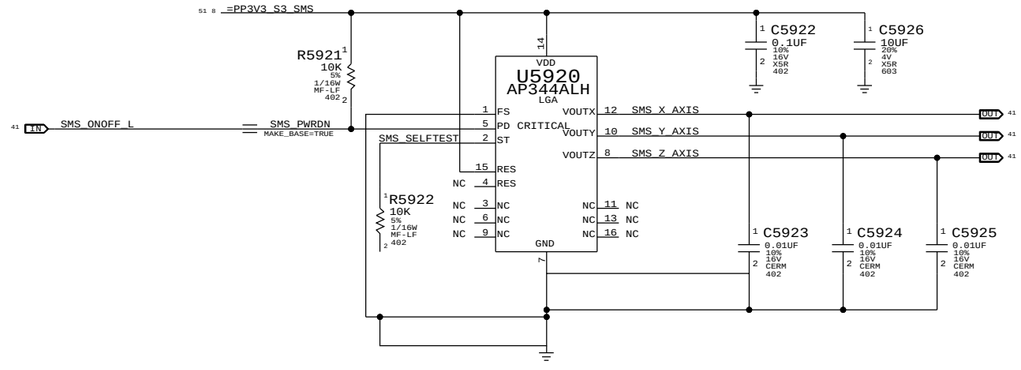
SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 50 OF 98	

Digital SMS



Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

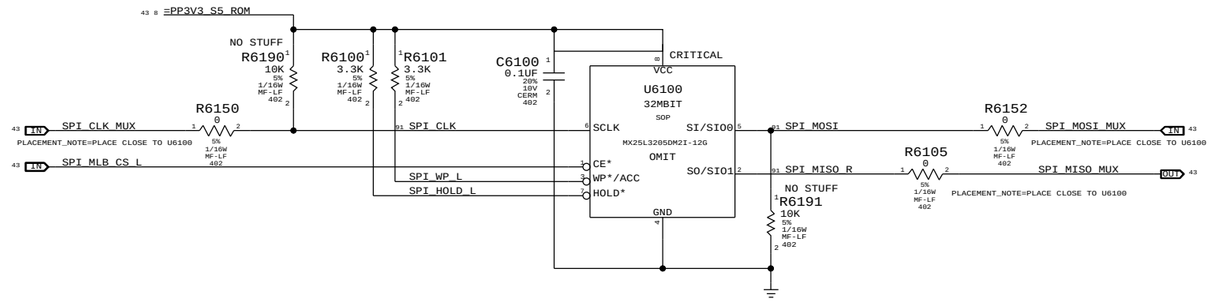


Sudden Motion Sensor (SMS)

SYNC_MASTER=YWU_K20 SYNC_DATE=06/17/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 51 OF 98	



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SPI ROM

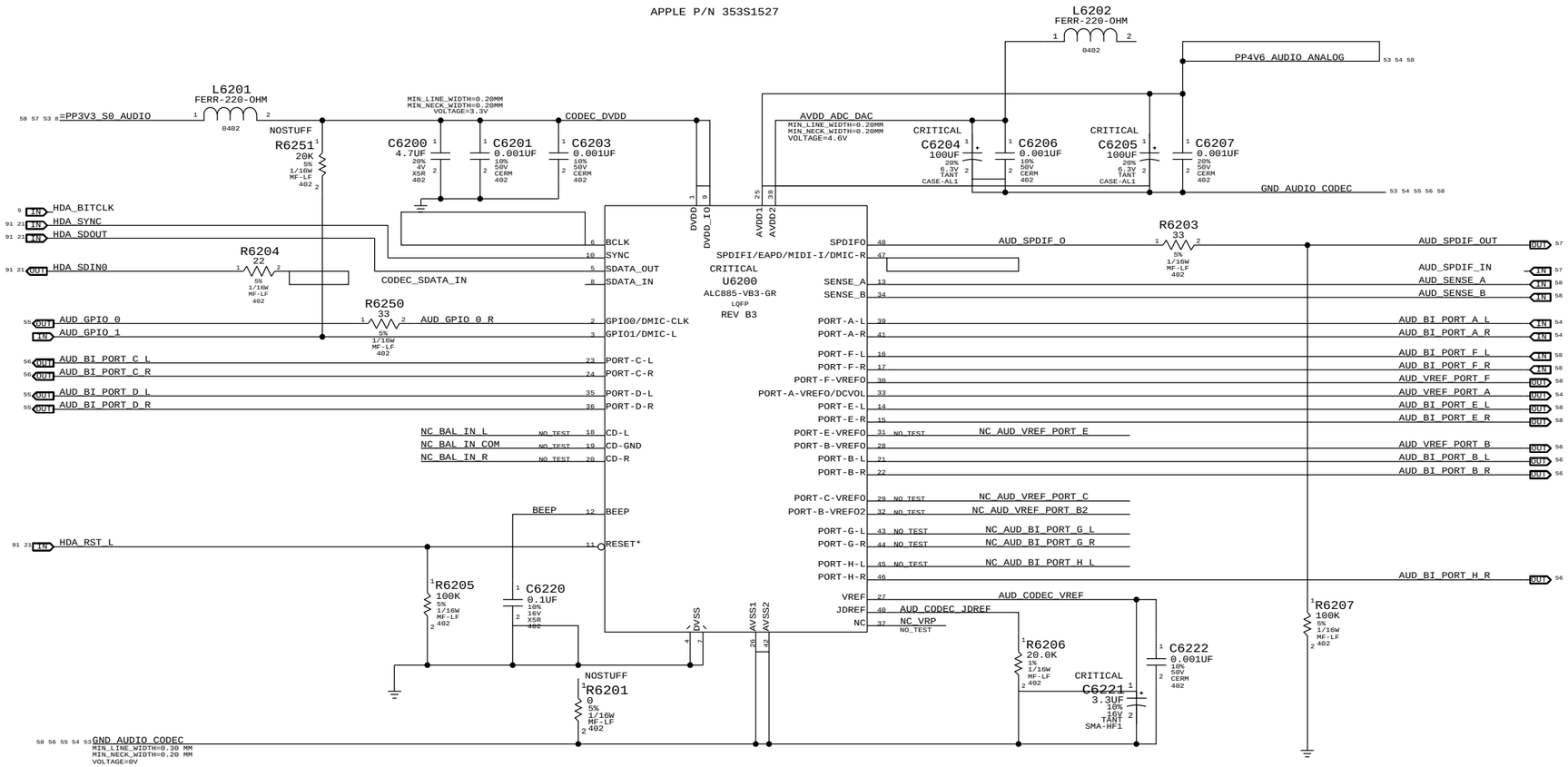
SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 52 OF 98	

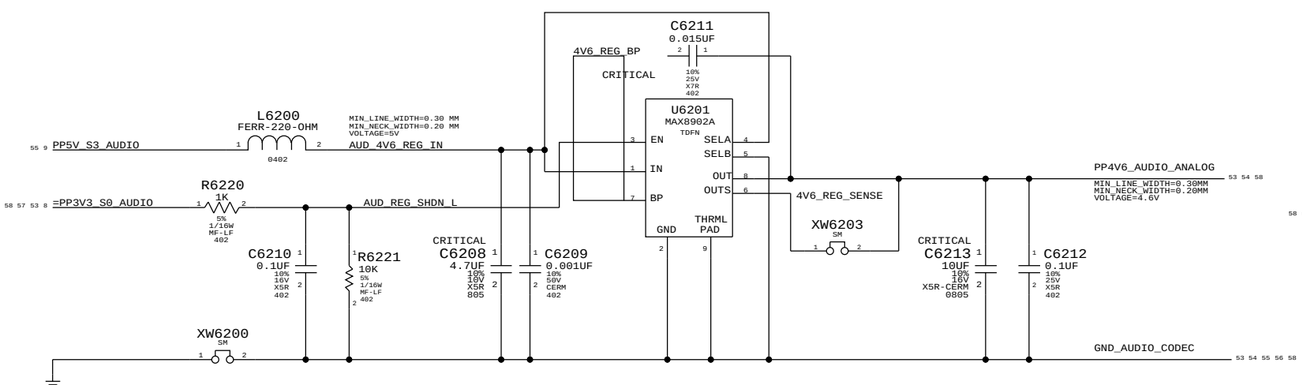
AUDIO CODEC

APPLE P/N 353S1527



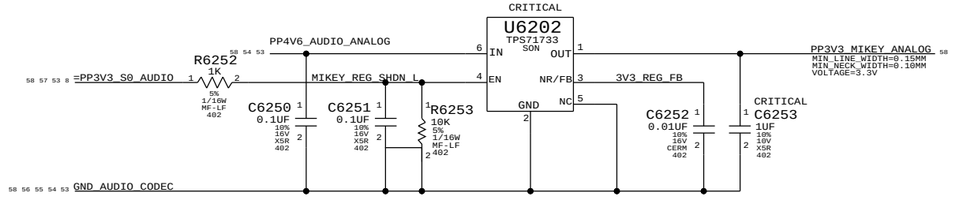
AUDIO 4.6 V REGULATOR

APPLE P/N 353S1897



MIKEY 3.3 V REGULATOR

APPLE P/N 353S1860



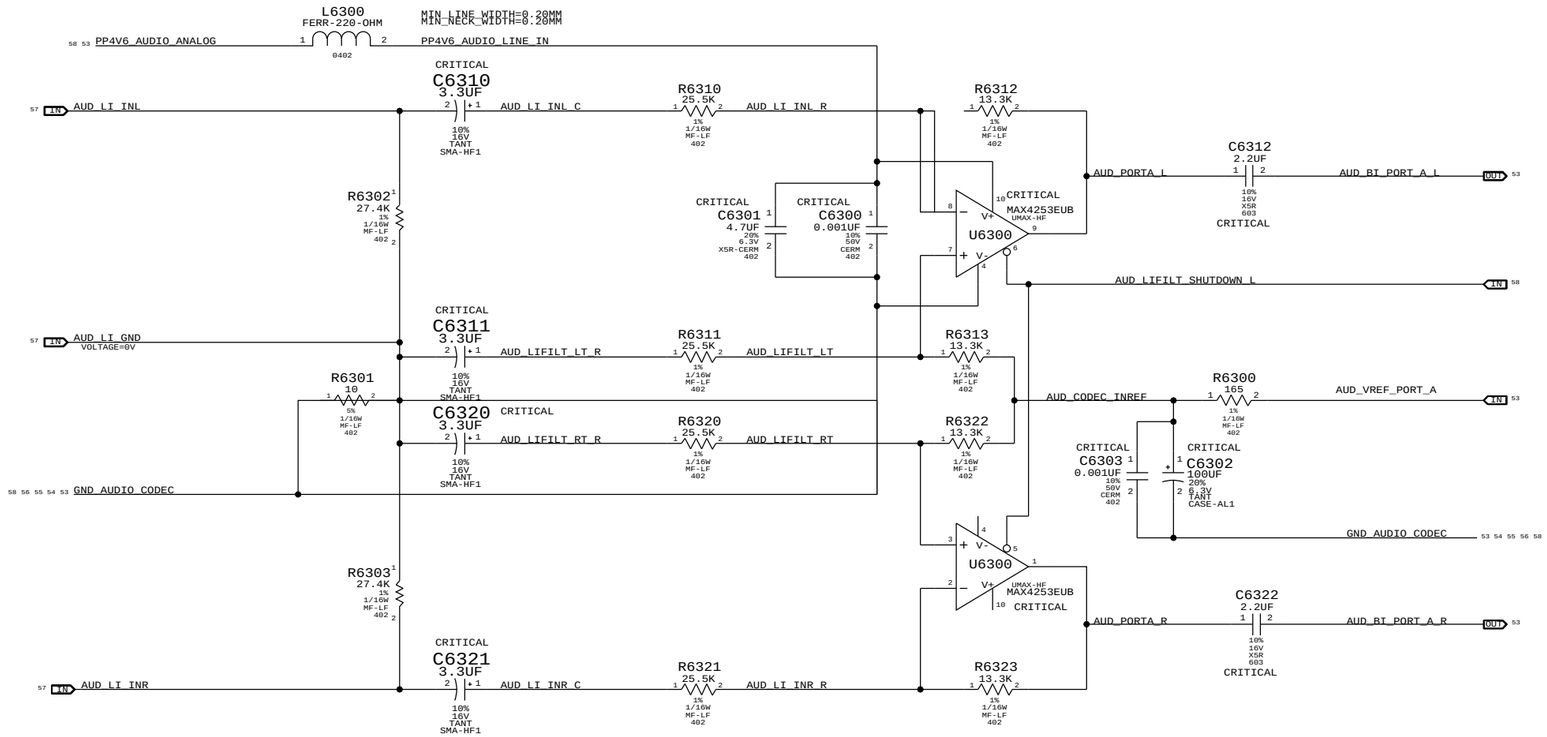
AUDIO:CODEC

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	53	98

Pseudo-Diff Line-In Filter
GAIN = -5.4 DB AV = 0.52
FC = 1.89 HZ



AUDIO: LINE IN

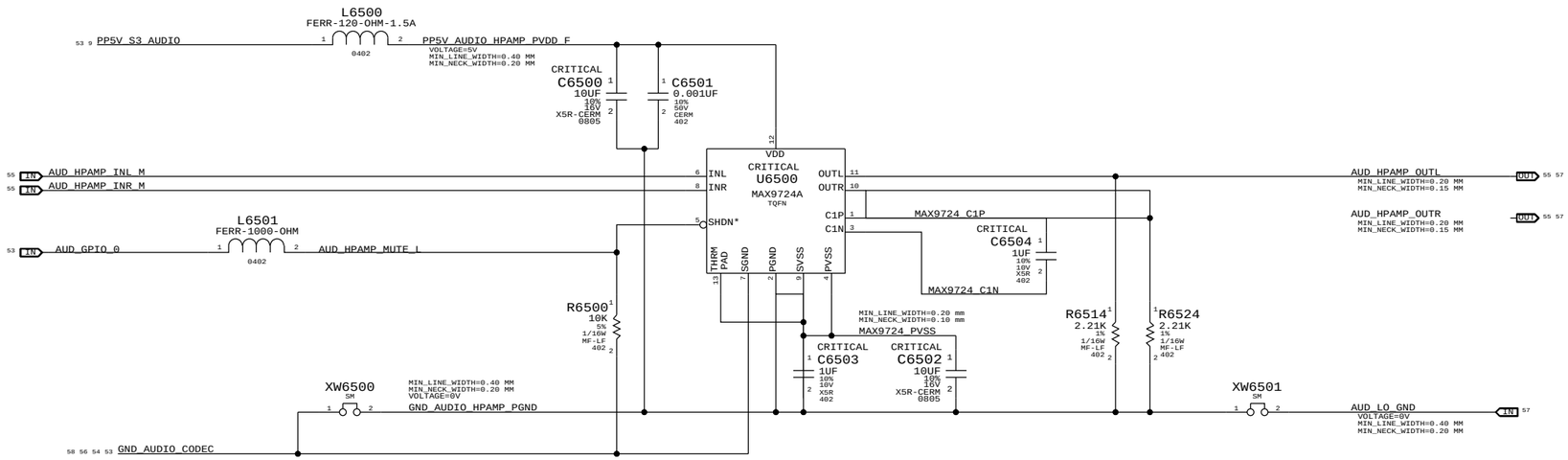
SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 54 OF 98	

Headphone Amplifier (MAX9724A)

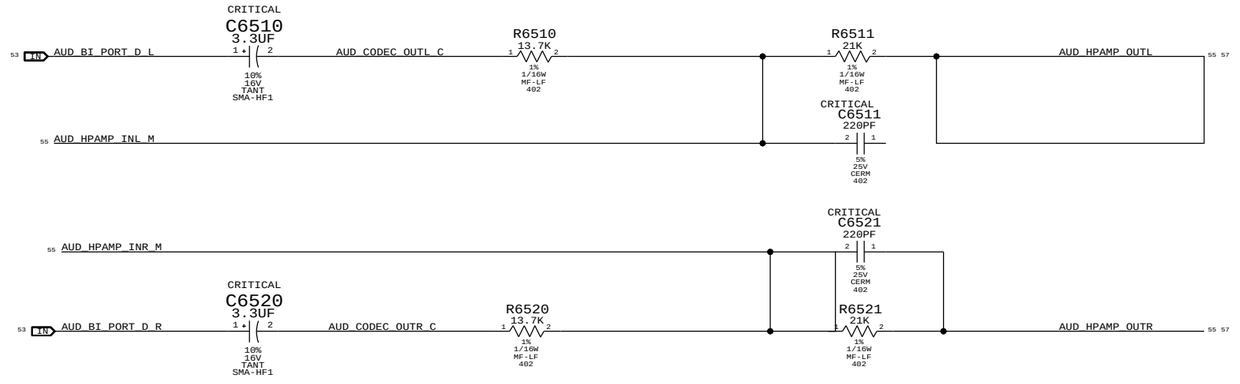
APN:353S1637



1st Order DAC Filter

HP:3.52 HZ LP:34 KHZ

VOLTAGE GAIN:1.53



AUDIO: HEADPHONE AMP

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

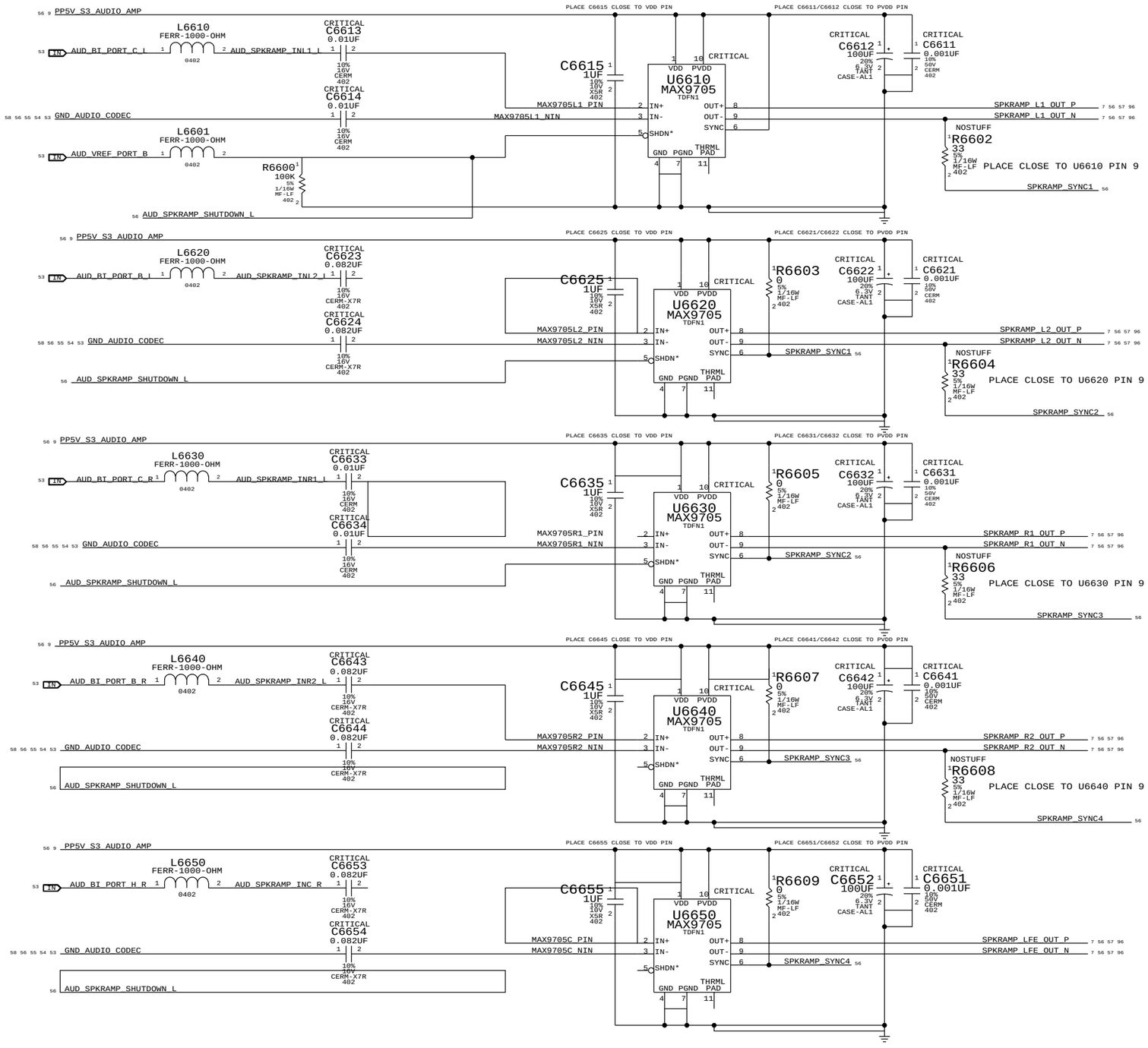
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 55 OF 98	

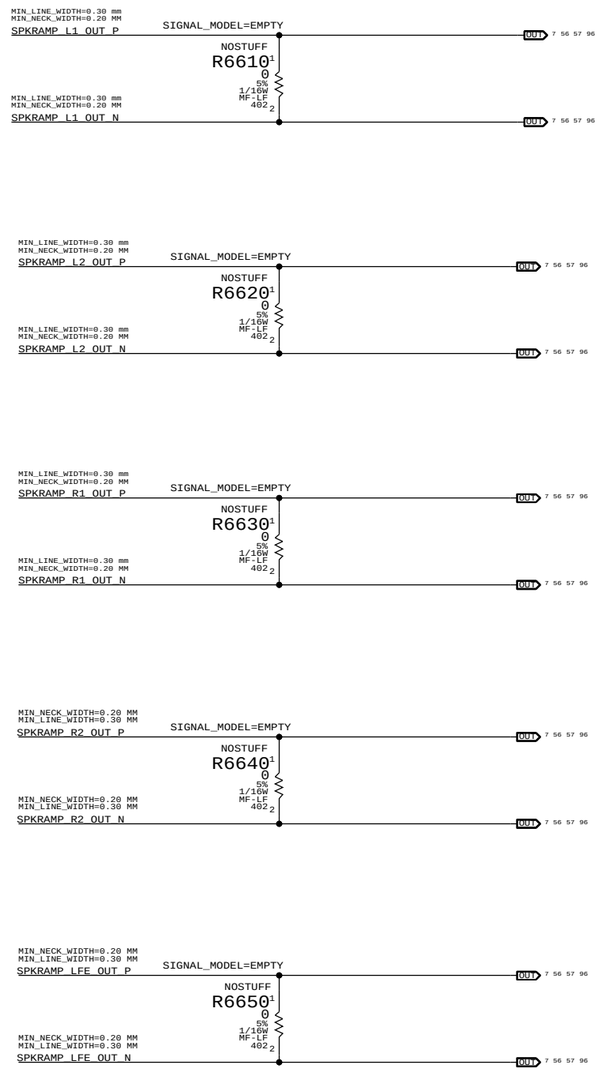
4X MONO SPEAKER AMPLIFIERS (MAX9705)

APN: 353S1595
GAIN = 12 DB

FC (SPEAKERS L1/R1) = ~796 HZ
FC (SPEAKERS L2/R2/LFE) = ~97 HZ



SPEAKER CHECKPOINTS



AUDIO:SPEAKER AMP

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 56 OF 98	

AUDIO JACK 1 LO/HP JACK, SPDIF TX

APN: 514-0632

CRITICAL J6700 SPDIF-TX-K20 F-RT-TH

MICROPHONE 6, DETECT FOR PT 5, SWITCH 2, LEFT 1, RIGHT 3, GROUND 4

AUDIO

A - VIN 7, B - VCC 8, C - GND 9

OPERATING VOLTAGE 3.3 POF

SHELL 10, SHIELD PINS 11 12 13

58 57 53 8 =PP3V3_S0_AUDIO

C6700 0.1UF 10% 16V X5R 402

C6701 2.2UF 20% 6.3V CERM 402-LF

CRITICAL DZ6700 6.8V-100PF 402

CRITICAL DZ6701 6.8V-100PF 402

CRITICAL DZ6702 6.8V-100PF 402

CRITICAL DZ6703 6.8V-100PF 402

CRITICAL DZ6704 6.8V-100PF 402

AUD_CONNJ1_SLEEVE2	R6713 0 5% 1/16W MF-LF 402	AUD_CONNJ1_SLEEVE2_F	L6703 FERR-1000-OHM 0402	HS_MIC_HI OUT 58
			L6702 FERR-1000-OHM 0402	HS_MIC_LO OUT 58
AUD_CONNJ1_SLEEVE (MIN_LINE_WIDTH=0.40 MM, MIN_NECK_WIDTH=0.20 MM)	R6711 0 5% 1/16W MF-LF 603	AUD_CONNJ1_SLEEVE_F (MIN_LINE_WIDTH=0.40 MM, MIN_NECK_WIDTH=0.20 MM)	L6701 CRITICAL FERR-220-OHM-2.5A 0603	AUD_LO_GND OUT 55
AUD_CONNJ1_RING (MIN_LINE_WIDTH=0.20 MM, MIN_NECK_WIDTH=0.15 MM)	R6714 0 5% 1/16W MF-LF 402	AUD_CONNJ1_RING_F (MIN_LINE_WIDTH=0.20 MM, MIN_NECK_WIDTH=0.15 MM)	L6704 CRITICAL FERR-220-OHM 0402	AUD_HPAMP_OUTR BI 55
AUD_CONNJ1_TIPDET	R6715 0 5% 1/16W MF-LF 402	AUD_CONNJ1_TIPDET_F	L6705 FERR-1000-OHM 0402	AUD_J1_TIPDET_R OUT 58
AUD_CONNJ1_TIP (MIN_LINE_WIDTH=0.20 MM, MIN_NECK_WIDTH=0.15 MM)	R6716 0 5% 1/16W MF-LF 402	AUD_CONNJ1_TIP_F (MIN_LINE_WIDTH=0.20 MM, MIN_NECK_WIDTH=0.15 MM)	L6706 CRITICAL FERR-220-OHM 0402	AUD_HPAMP_OUTL BI 55
AUD_CONNJ1_SLEEVEDET	R6710 0 5% 1/16W MF-LF 402	AUD_CONNJ1_SLEEVEDET_F	R6700 10K 5% 1/16W MF-LF 402	AUD_J1_SLEEVEDET_R OUT 58

AUD_SPDIF_OUT IN 53

NOSTUFF C6710 100PF 5% 50V CERM 402

NOSTUFF C6711 100PF 5% 50V CERM 402

NOSTUFF C6712 100PF 5% 50V CERM 402

C6713 100PF 5% 50V CERM 402

NOSTUFF C6714 100PF 5% 50V CERM 402

NOSTUFF C6715 100PF 5% 50V CERM 402

GND_CHASSIS_AUDIO_JACK 57

MIC CONNECTOR

APN: 518S0520

CRITICAL J6780 78171-0003 M-RT-SM

58 7 OUT BI_MIC_LO

58 7 OUT BI_MIC_SHIELD

58 7 OUT BI_MIC_HI

SPEAKER CONNECTORS

APN: 518S0521

CRITICAL J6781 78171-0004 M-RT-SM

96 56 7 IN SPKRAMP_L2_OUT_P

96 56 7 IN SPKRAMP_L2_OUT_N

96 56 7 IN SPKRAMP_L1_OUT_P

96 56 7 IN SPKRAMP_L1_OUT_N

NOSTUFF C6781 100PF 5% 50V CERM 402

NOSTUFF C6782 100PF 5% 50V CERM 402

NOSTUFF C6783 100PF 5% 50V CERM 402

NOSTUFF C6784 100PF 5% 50V CERM 402

APN: 518S0672

CRITICAL J6782 78171-6006 M-RT-SM

96 56 7 IN SPKRAMP_R2_OUT_P

96 56 7 IN SPKRAMP_R2_OUT_N

96 56 7 IN SPKRAMP_R1_OUT_P

96 56 7 IN SPKRAMP_R1_OUT_N

96 56 7 IN SPKRAMP_LFE_OUT_P

96 56 7 IN SPKRAMP_LFE_OUT_N

NOSTUFF C6785 100PF 5% 50V CERM 402

NOSTUFF C6786 100PF 5% 50V CERM 402

NOSTUFF C6787 100PF 5% 50V CERM 402

NOSTUFF C6788 100PF 5% 50V CERM 402

NOSTUFF C6789 100PF 5% 50V CERM 402

NOSTUFF C6790 100PF 5% 50V CERM 402

AUDIO JACK 2 LINE IN JACK, SPDIF RX

APN: 514-0633

CRITICAL J6750 SPDIF-RX-K20 F-RT-TH

DETECT FOR PT 5, SWITCH 2, LEFT 1, RIGHT 3, GROUND 4

AUDIO

A - VDD 6, B - GND 7, C - VOUT 8

OPERATING VOLTAGE 3.3 POF

SHELL 9, SHIELD PINS 10 11 12

58 57 53 8 =PP3V3_S0_AUDIO

C6750 0.1UF 10% 16V X5R 402

CRITICAL DZ6752 6.8V-100PF 402

CRITICAL DZ6753 6.8V-100PF 402

CRITICAL DZ6754 6.8V-100PF 402

CRITICAL DZ6755 6.8V-100PF 402

AUD_J2_OPT_OUT	R6749 10 5% 1/16W MF-LF 402			AUD_SPDIF_IN OUT 53
AUD_CONNJ2_SLEEVE	R6761 0 5% 1/16W MF-LF 402	AUD_CONNJ2_SLEEVE_F	L6751 FERR-220-OHM 0402	
AUD_CONNJ2_TIPDET	R6762 0 5% 1/16W MF-LF 402	AUD_CONNJ2_TIPDET_F	L6752 FERR-1000-OHM 0402	AUD_J2_TIPDET_R OUT 58
AUD_CONNJ2_RING	R6764 0 5% 1/16W MF-LF 402	AUD_CONNJ2_RING_F	L6754 FERR-1000-OHM 0402	AUD_LI_INR BI 54
AUD_CONNJ2_TIP	R6766 0 5% 1/16W MF-LF 402	AUD_CONNJ2_TIP_F	L6756 FERR-1000-OHM 0402	AUD_LI_INL BI 54
AUD_CONNJ2_SLEEVEDET	R6768 0 5% 1/16W MF-LF 402	AUD_CONNJ2_SLEEVEDET_F	L6758 FERR-220-OHM 0402	AUD_J2_COM XW6701 SM AUD_LI_GND 54

NOSTUFF C6761 100PF 5% 50V CERM 402

C6762 100PF 5% 50V CERM 402

NOSTUFF C6763 100PF 5% 50V CERM 402

NOSTUFF C6764 100PF 5% 50V CERM 402

NOSTUFF C6765 100PF 5% 50V CERM 402

GND_CHASSIS_AUDIO_JACK 57

RETURN FOR HF NOISE

57 GND_CHASSIS_AUDIO_JACK — R6701 0 5% 1/16W MF-LF 402

AUDIO: JACKS

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 57 OF 98	

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X0C (12)	0X02 (2)	0X0C (12)	0X14 (20,D)	GPIO_0	0X14 (20,D)
SPEAKERS L1/R1	0X0F (15)	0X05 (5)	0X0F (15)	0X1A (26,C)	VREF_B (100%)	N/A
SPEAKERS L2/R2	0X0D (13)	0X03 (3)	0X0D (13)	0X18 (24,B)	VREF_B (100%)	N/A
SPEAKER LFE	0X0E (14)	0X04 (4)	0X0E (14)	0X17 (23,H)	VREF_B (100%)	N/A
SPDIF OUT	N/A	0X06 (6)	N/A	0x1E (SPDIF OUT)	N/A	0X16 (22,G)

CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X15 (21,A)	VREF_A (50%)	0X15 (21,A)
SPDIF IN	N/A	0X0A (10)	0x1F (SPDIF IN)	N/A	N/A
MIC	0X24 (36)	0X07 (7)	0X19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	0X24 (36)	0X07 (7)	0X1B (27,E)	MIKEY	MIKEY

PORT D DETECT (Line-out)

PORT G DETECT (SPDIF DELEGATE)

PORT A DETECT (Line-in)

LINE_IN AMP SHUTDOWN CONTROL

PORT F (BUILT-IN MIC)

TIPDET DEBOUNCE CIRCUIT

PLACE L6800/C6800 CLOSE TO Q6800/01/02

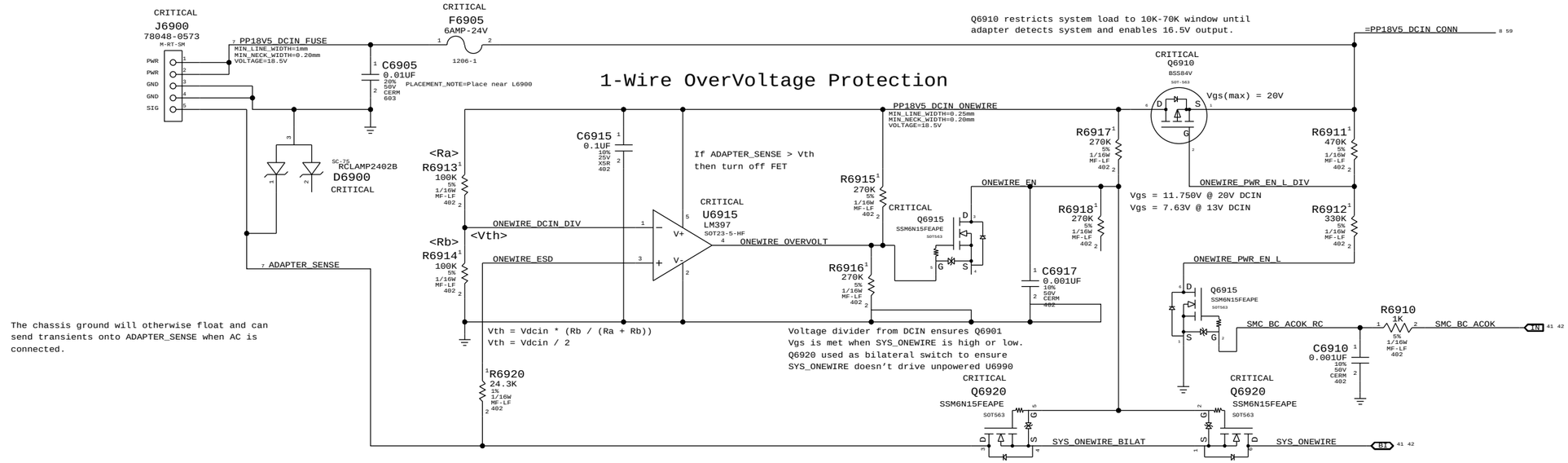
AUDIO: JACK TRANSLATORS	
SYNC_MASTER=AUDIO_K20	SYNC_DATE=09/29/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 58 OF 98	

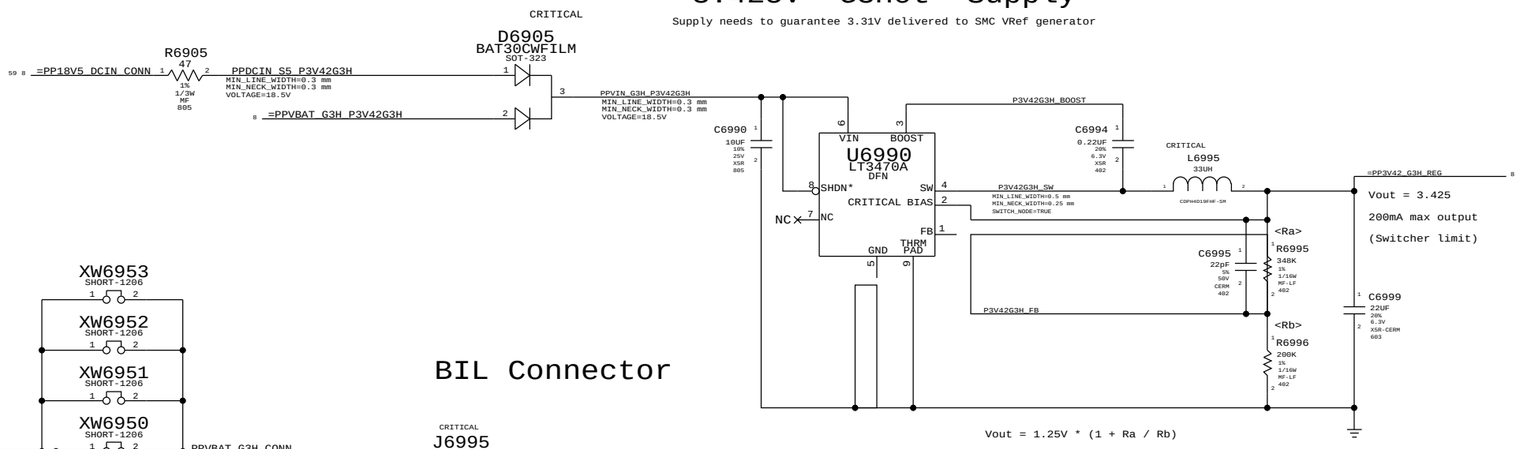
MagSafe DC Power Jack

1-Wire OverVoltage Protection

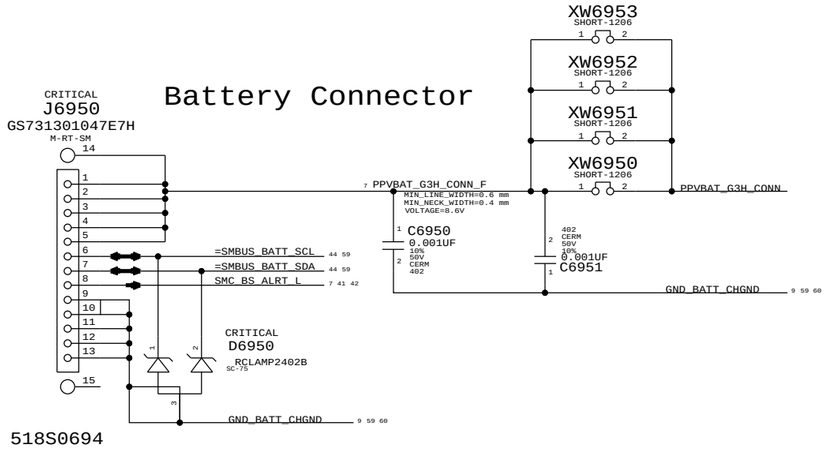


3.425V "G3Hot" Supply

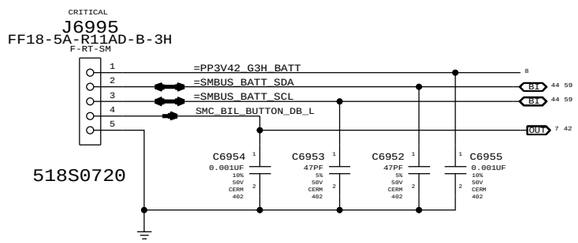
Supply needs to guarantee 3.31V delivered to SMC VRef generator



Battery Connector



BIL Connector



DC-In & Battery Connectors

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B

SCALE: NONE SHT 59 OF 98

FROM ADAPTER

=PPDCIN_S5_CHGR

Inrush Limiter

R7060 470K 1% 1/16W MF-LF 402

C7060 0.1UF 10% 25V X5R 402

CHGR_AGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

R7061 332K 1% 1/16W MF-LF 402

CRITICAL
Q7060
HAT1128R01
SO1

PPDCIN_S5_INRUSH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

Reverse-Current Protection

PPDCIN_S5_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

CRITICAL
Q7065
HAT1128R01
SO1

R7065 100K 5% 1/16W MF-LF 402

CHGR_SGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

R7066 62K 5% 1/16W MF-LF 402

CHGR_SGATE
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.25 mm

U7070 TL331 SOT23-5
VCC
GND
SGATE_P0V1_VREF

C7070 0.1uF 10% 16V X5R 402

R7070 57.6K 1% 1/16W MF-LF 402

R7071 1.82K 1% 1/16W MF-LF 402

Q7074 SSM6N15FEAPE SOT563
AMON_CLAMP

=PP3V42_G3H_CHGR

R7074 1M 5% 1/16W MF-LF 402

CHGR_AMON

R7075 clamps CHGR_AMON when charger is not powered to counter TL331 bias current.

Q7074 SSM6N15FEAPE SOT563

PP5V1_CHGR_VDD

(CHGR_AGATE)

(CHGR_DCIN)

CRITICAL
D7005
BAT30CWFILM
SOT-323

R7021 10 5% 1/16W MF-LF 402

R7022 10 5% 1/16W MF-LF 402

CHGR_CSI_R_P

CHGR_CSI_R_N

CRITICAL
R7020 0.02 0.5% 1W MF 0612

C7020 0.047UF 10% 10V CERM 402
SIGNAL_MODEL=EMPTY

=PP3V42_G3H_CHGR

ACIN pin threshold is 3.2V, +/- 50mV

Divider sets ACIN threshold at 13.07V

Input impedance of ~40K meets sparkitecture requirements

C7002 1UF 10% 10V X5R 402

PP5V1_CHGR_VDD
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

30mA max load

R7001 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

C7001 1UF 10% 10V X5R 402

C7022 0.1UF 10% 25V X5R 402

C7021 0.1UF 10% 25V X5R 402

C7035 0.22UF 10% 16V CERM 402

GND_CHGR_AGND

PPDCIN_S5_FET_CHGR
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

CRITICAL
Q7030
RJK0305DPB
LFPAK-HF

152S0542

CRITICAL
Q7031
RJK0305DPB
LFPAK-HF

152S0542

CRITICAL
C7030 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL
C7031 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL
C7036 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL
C7037 22UF 20% 25V POLY-TANT CASE-D2-SM

C7032 1UF 10% 25V X5R 603-1

C7033 1UF 10% 25V X5R 603-1

C7034 0.001UF 10% 50V X7R 402

CRITICAL
L7030
2.2UH-20A-5.5M-OHM
SM

CRITICAL
L7031
2.2UH-20A-5.5M-OHM
SM

PPVBAT_G3H_CHGR_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

PPVBAT_G3H_CHGR_REG_L
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

=PPBUS_G3H
TO SYSTEM

CRITICAL
F7040
8AMP-24V
1206

CRITICAL
F7041
8AMP-24V
1206

CRITICAL
C7043 33UF 20% 16V POLY-TANT CASED2E-SM

CRITICAL
C7040 33UF 20% 16V POLY-TANT CASED2E-SM

C7041 0.001UF 10% 50V X7R 402

R7010 30.1K 1% 1/16W MF-LF 402

R7011 9.31K 1% 1/16W MF-LF 402

R7015 56.2K 1% 1/16W MF-LF 402

CHGR_VCOMP_R

C7050 0.1uF 10% 16V X5R 402
SIGNAL_MODEL=EMPTY

C7015 0.001UF 10% 50V CERM 402

R7016 3.01K 1% 1/16W MF-LF 402

CHGR_VNEG_R

C7016 470PF 10% 50V CERM 402

=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA

VREF = 3.2V, < 300uA

CHGR_ACIN

CHGR_ICOMP

CHGR_VCOMP

CHGR_VNEG

CHGR_CSO_P

CHGR_CSO_N

CRITICAL
U7000
ISL6258A
QFN

VHST	AGATE	CHGR_AGATE
SCL	CSIP	CHGR_CSI_P
SDA	CSIN	CHGR_CSI_N
	BGATE	CHGR_BGATE
VREF	DCIN	CHGR_DCIN
ACIN	BOOT	CHGR_BOOT
ICOMP	UGATE	CHGR_UGATE
VCOMP	PHASE	CHGR_PHASE
VNEG	(OD) TRKL*	CHGR_LGATE
CSOP	20V/V AMON	CHGR_AMON
CSON	32V/V BMON	CHGR_BMON
	(OD) ACOK	=CHGR_ACOK

NC

OMIT

THRM_PAD

AGND

PGND

XW7000 SM

Max Current = 8.5A (L7030 limit)
f = 400 kHz

R7051 10 5% 1/16W MF-LF 402

R7052 10 5% 1/16W MF-LF 402

CHGR_CSO_R_P

CHGR_CSO_R_N

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

CRITICAL
R7050 0.005 1% 1W MF 0612

PPVBAT_G3H_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

C7055 1UF 10% 25V X5R 603-1

C7056 0.1UF 10% 16V X5R 402

C7057 0.01UF 10% 16V CERM 402

CRITICAL
HAT1127H
LFPAK-SM
Q7057

CRITICAL
HAT1127H
LFPAK-SM
Q7058

CRITICAL
HAT1127H
LFPAK-SM
Q7055

CRITICAL
HAT1127H
LFPAK-SM
Q7056

PPVBAT_G3H_FET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

PPVBAT_G3H_CONN
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

C7058 1UF 10% 16V X5R 402-1

BATT_POS_GATE

R7056 1M 5% MF-LF 402 1/16W

R7057 20K 5% MF-LF 402 1/16W

GND_BATT_CHGND

C7042 0.033UF 10% 16V X5R 402

C7000 1UF 10% 10V X5R 402

C7011 0.01UF 10% 16V CERM 402

C7005 0.1UF 10% 25V X5R 402

GND_CHGR_AGND
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

C7026 0.001UF 10% 50V CERM 402

M99 differences from last sync on 12/02/07 to T18 MLB:

1. L7030 changed from T18 MLB inductor to 152S0542.
2. Added Q7056, C7058,R7055,R7056..
3. U7000 Thermal Pad is now connected to GND, not through XW.
4. Q7060 and Q7065 changed to 376S0667.
5. Q7055 and Q7056 changed to 376S0666.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
353S1938	1	IC,ISL6258,BAT CHARGER,28P,4X4,QFN,L	U7000	CRITICAL	ISL6258	2S Battery Default
353S1832	1	IC,ISL6258A,BAT CHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6258A	3S Battery Default

PBus Supply & Battery Charger

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 60 OF 98	

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

These caps are for Q7100

These caps are for Q7102

Place R7131 Between L7100,L7101 and CPU

LAYOUT NOTE:
Place R7126 in hot spot of reg circuit.

IMVP6 CPU VCore Regulator

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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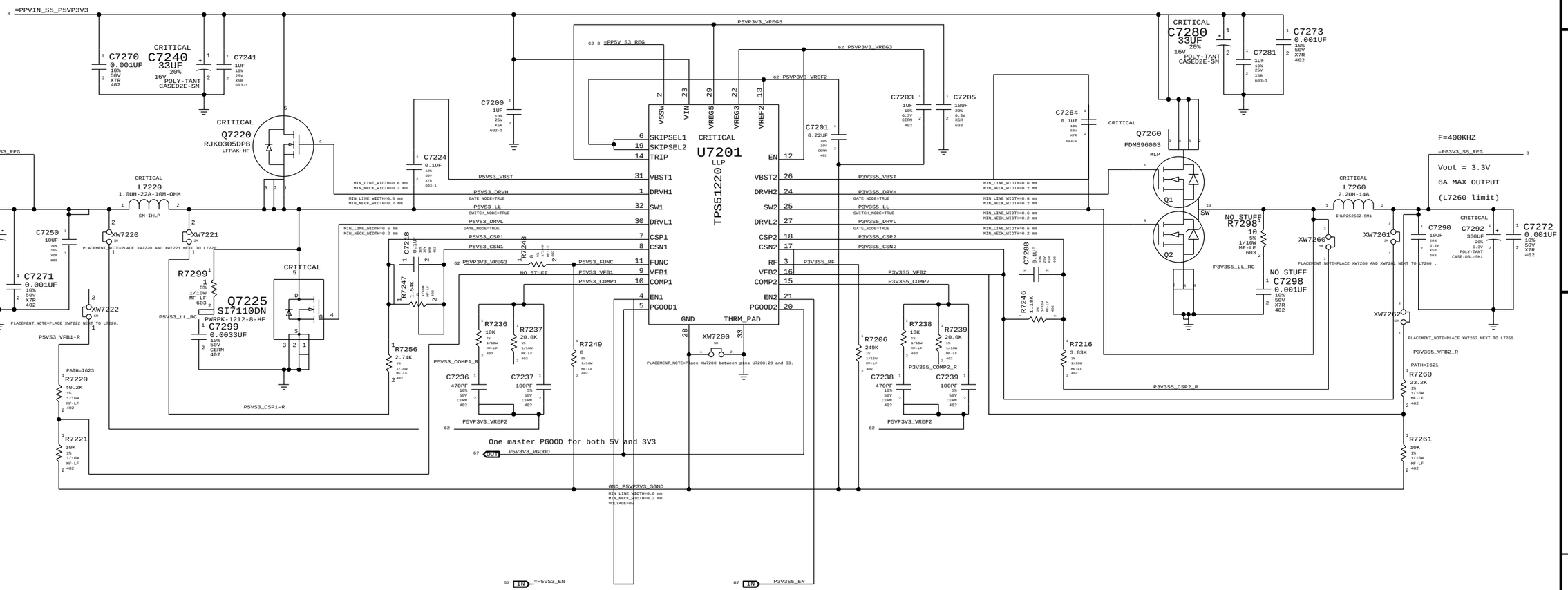
APPLE INC.

SIZE D | DRAWING NUMBER 051-8071 | REV. B

SCALE NONE | SHT 61 OF 98



5V / 3.3V Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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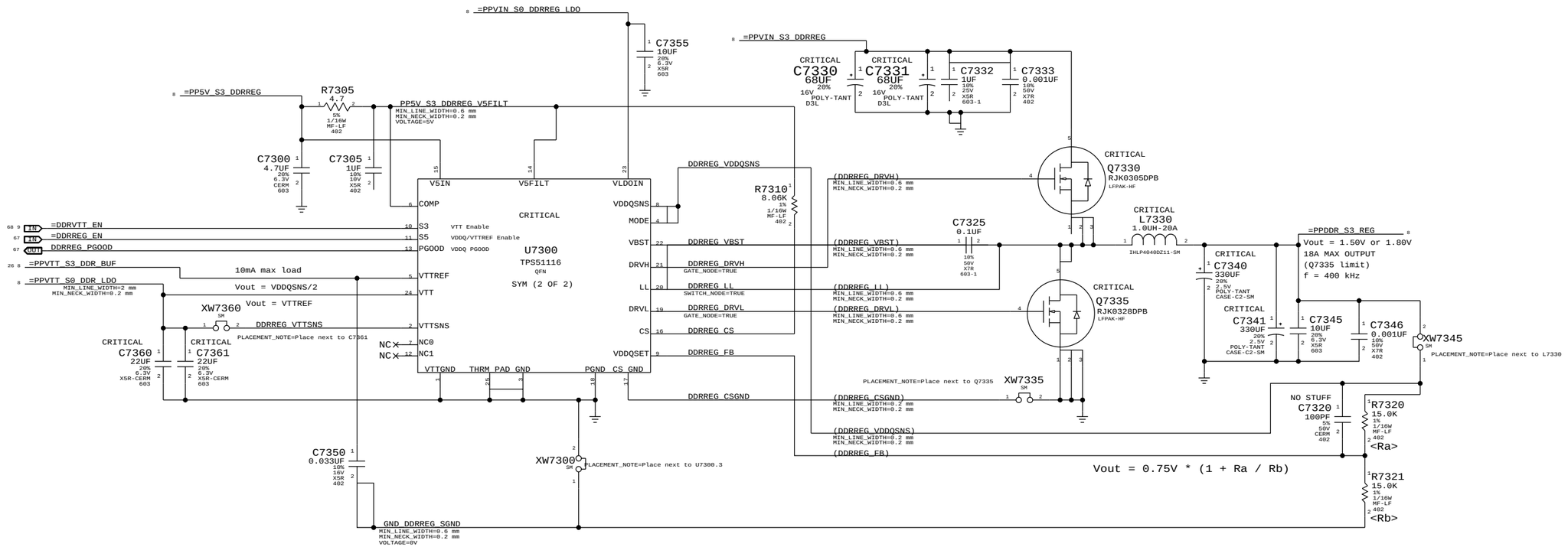
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 62 OF 98	

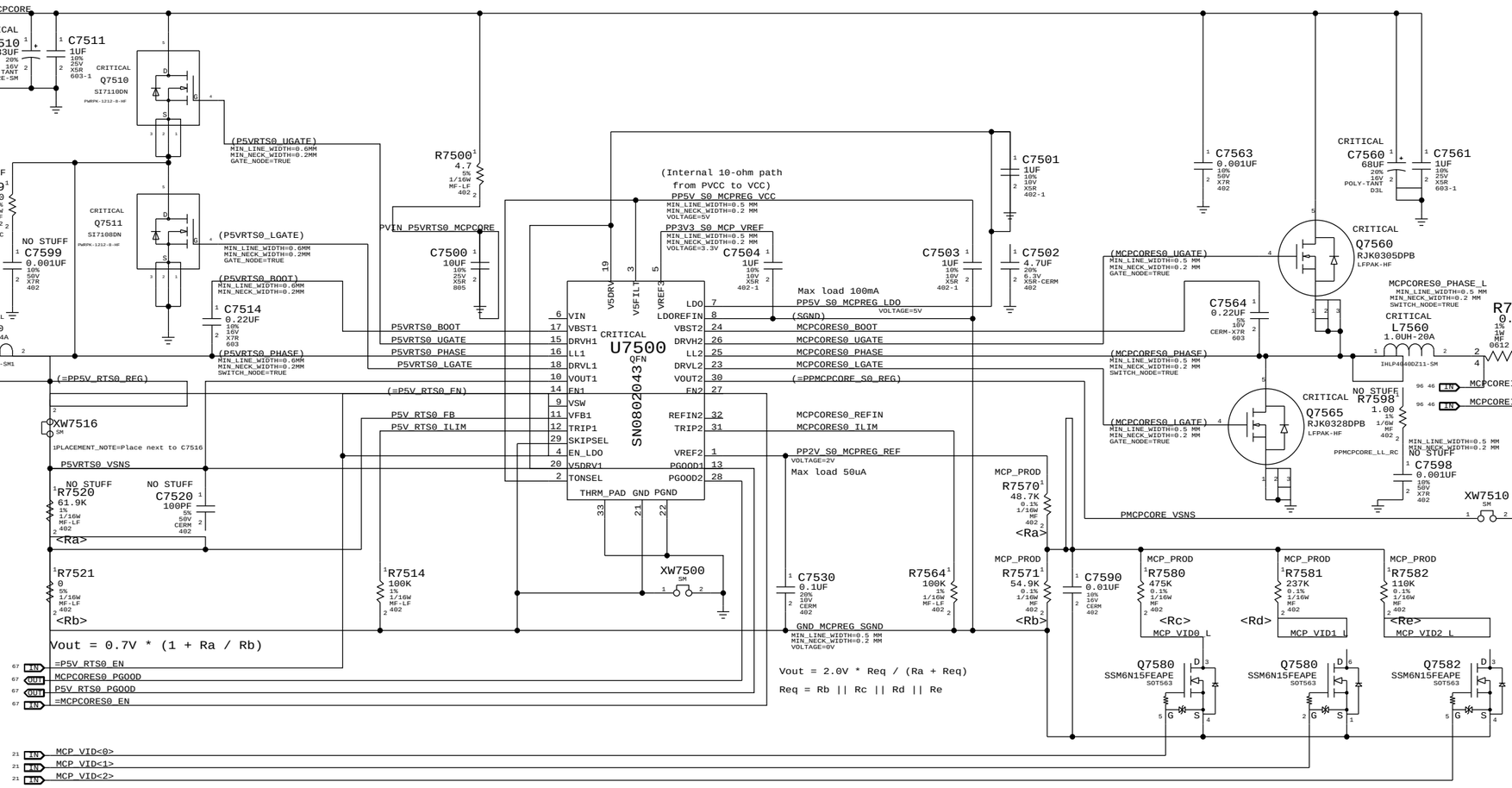


1.5V DDR3 Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 63 OF 98	



MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0382	1	RES,MTL FILM,1/16W,48.7K,1,0402,SMD,LF	R7570		MCP_A01
114S0400	1	RES,MTL FILM,1/16W,76.8K,1,0402,SMD,LF	R7571		MCP_A01
114S0482	1	RES,MTL FILM,1/16W,523K,1,0402,SMD,LF	R7580		MCP_A01
114S0453	1	RES,MTL FILM,1/16W,267K,1,0402,SMD,LF	R7581		MCP_A01
114S0422	1	RES,MTL FILM,1/16W,130K,1,0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1,0402,SMD,LF	R7570		MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1,0402,SMD,LF	R7571		MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1,0402,SMD,LF	R7580		MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R7581		MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7582		MCP_A01Q

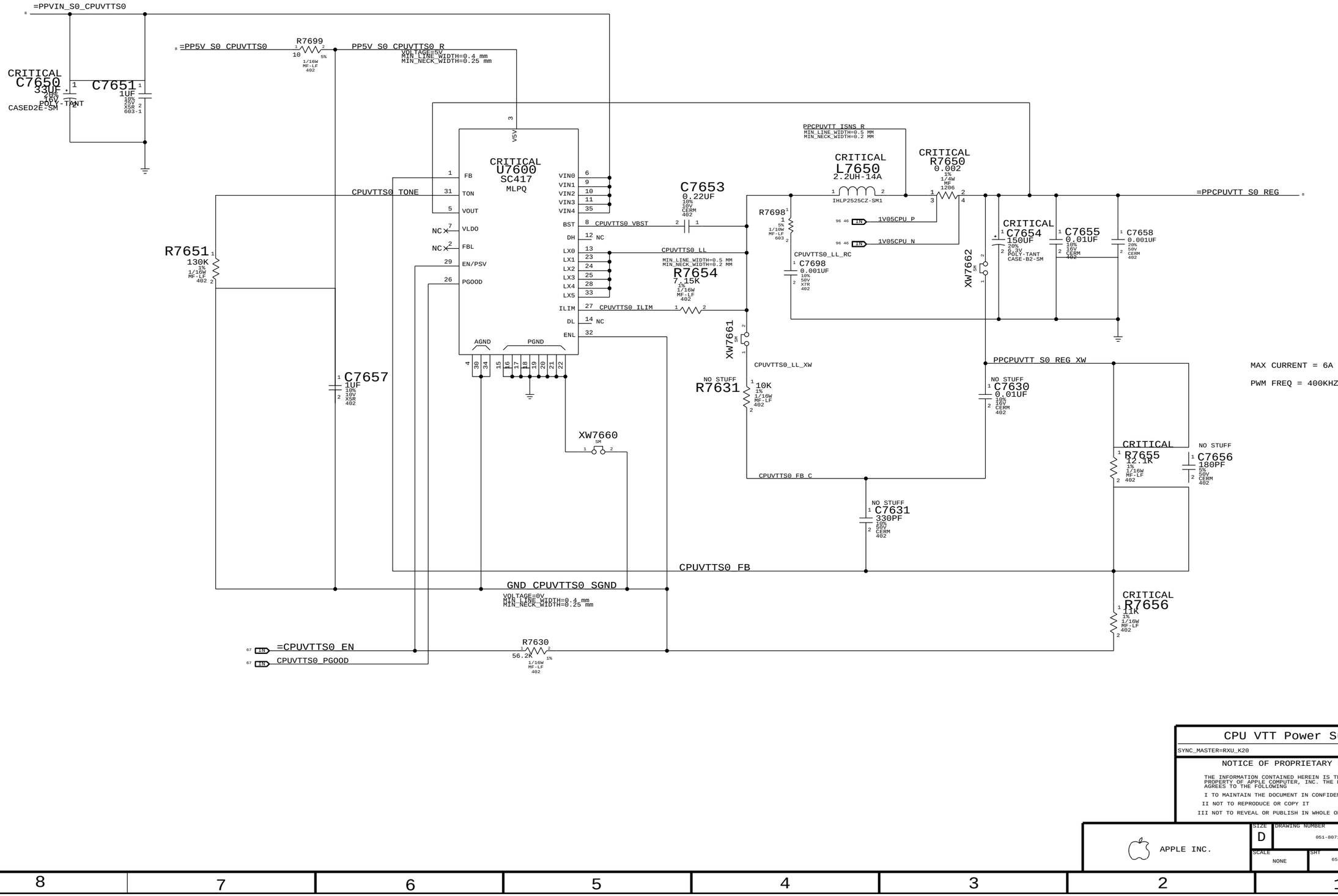
VID<2:0>	Rev A01 Voltage	Production Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

5V_S0 / MCP CORE REGULATOR

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 64 OF 98	



CPU VTT Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	65	98

1.8V S0 Switcher / 1.0VFW SWITCHER

S5 power required for output discharge feature

=PP3V3_S3_P1V8S0

C7700 2.2UF 20% 6.3V CERM 402-LF

P1V0FW_SW — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, SWITCH_NODE=TRUE

CRITICAL L7780 2.2UH-1.2A PCAA031B-SM

C7782 10PF 5% 50V CERM 402

<Ra> R7782 187K 1% 1/16W MF-LF 402

<Rb> R7783 280K 1% 1/16W MF-LF 402

=PP1V0_FW_REG

Vout = 1.001V
300mA max output
(Switcher limit)
f = 2.25 MHz

C7785 4.7UF 20% 4V X5R 402

P1V0FW_VFB

U7700 DFN-HF
VIN, SW1, SW2, VFB1, VFB2, RUN1, RUN2, THRML PAD, GND

P1V8S0_LX — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, SWITCH_NODE=TRUE

CRITICAL L7700 2.2UH-1.2A PCAA031B-SM

C7701 10PF 5% 50V CERM 402

<Ra> R7700 562K 1% 1/16W MF-LF 402

<Rb> R7701 280K 1% 1/16W MF-LF 402

=PP1V8_S0_REG

VOUT = 1.804V
0.3A max output
(Switcher limit)
F = 2.25 MHZ

C7705 4.7UF 20% 4V X5R 402

P1V8S0_VFB

=P1V8S0_EN

=PP3V3_FW_P1V0FW

Vout = 0.6V * (1 + Ra/Rb)

MCP79 PLL VLDO

=PP3V3_S0_MCP_PLL_VLDO

R7743 100 5% 1/16W MF-LF 402

C7740 1UF 10% 6.3V CERM 402

=PP1V8_S0_MCP_PLL_VLDO

U7740 LTC3025 DFN
BIAS CRITICAL, IN, SHDN*, OUT, ADJ, GND, THRML PAD

C7741 1UF 10% 6.3V CERM 402

=PP1V05_S0_FET

NO STUFF
R7742 0 5% 1/16W MF-LF 402

<Ra> R7740 66.5K 1% 1/16W MF-LF 402

<Rb> R7741 40.2K 1% 1/16W MF-LF 402

P1V05_S0_MCP_PLL_VLDO_ADJ

C7742 1UF 10% 6.3V CERM 402

MAX CURRENT = 300MA

=PP1V05_S0_MCP_PLL_VLDO

Vout = 1.052V

FW BOOST POWER

=PPVIN_PFWBOOST

R7790 0.02 0.5% 1W MF 0612

C7790 10UF 10% 16V X5R 1206

CRITICAL L7795 4.7UH-10A PCMC063T-SM

PFWBOOST_SW — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, SWITCH_NODE=TRUE

PFWBOOST_BOOST — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm

CRITICAL U7790 LTC1872 SOT23-6
VIN, ITH/RUN, SENSE-, VFB, GND, NGATE, PFWBOOST_SENSE

PFWBOOST_ITH

R7797 38.3K 1% 1/16W MF-LF 402

PFWBOOST_ITH_R

C7797 0.001UF 10% 50V CERM 402

CRITICAL D7790 D0222-SM STPS1L30MF

CRITICAL Q7790 SUPERSOT-8 FDC796NG

PFWBOOST_NGATE

PFWBOOST_FB

C7795 33PF 5% 50V CERM 402

<Ra> R7795 1.00M 1% 1/4W MF-LF 1206

<Rb> R7796 86.6K 1% 1/16W MF-LF 402

C7794 1UF 10% 16V X5R 402

=PFWBOOST_REG

VOUT = 10V
?MA MAX OUTPUT
F=550KHZ?

C7799 33UF 20% 16V POLY-TANT CASED2E-SM

C7798 33UF 20% 16V POLY-TANT CASED2E-SM

VOUT = 0.8V * (1 + RA / RB)

EXPRESSCARD 1.5V_S0 SUPPLY

=PP3V3_S3_P1V5EXPS0

R7712 1 5% 1/16W MF-LF 402

CRITICAL C7710 22UF 20% 6.3V CERM 805

P1V5EXPS0_AVIN

CRITICAL L7710 2.2UH-1.2A PCAA031B-SM

=P1V5_EXP_S0_EN

CRITICAL U7710 TPS62510
EN, OVT, MODE, BQA, AVIN, PVIN, SW, FB, PG, AGND, PGND, THRM_PAD

P1V5EXPS0_SW

P1V5EXPS0_FB

C7711 0.1UF 10% 16V CERM 402

C7712 22PF 5% 50V CERM 402

<Ra> R7710 150K 1% 1/16W MF-LF 402

<Rb> R7711 100K 1% 1/16W MF-LF 402

=PP1V5_EXP_S0

Vout = 1.5V
MAX Current = 1.2A
FREQ = 1Mhz

CRITICAL C7713 22UF 20% 6.3V CERM 805

TP_P1V5_EXP_S0_PGOOD

P1V5EXPS0_SGND

XW7710 SM

VOUT = 0.6V * (1 + Ra / Rb)

1.8V S0 Switcher

INPUT RAIL IS 3.3V S0

=PP3V3_GPU_P1V8S0

C7760 10uF 20% 6.3V X5R 603

U7760 TPS62202 SOT23-5
VI, FB, EN, GND, SW

=P1V8FB_EN

CRITICAL L7760 10UH-0.55A-330MOHM PCAA031B-SM

P1V8GPU_SW

MAX CURRENT = 300MA

=PP1V8_GPUIFPX_REG

C7762 10uF 20% 6.3V X5R 603

MCP 1.05V AUXC Supply

=PPVIN_S0_P1V05S5

C7775 1UF 10% 25V X5R 603-1

CRITICAL Q7770 SI7110DN PWRPK-1212-8-HF

CRITICAL Q7771 SI7108DN PWRPK-1212-8-HF

P5V_P1V05S5_V5FILT

R7751 4.7 5% 1/16W MF-LF 402

P5V_P1V05S5 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V

C7752 1UF 10% 25V X5R 603-1

C7751 4.7UF 20% 6.3V CERM 603

C7750 2.2UF 10% 16V X5R 603

P1V05S5_ISEN

R7779 2.0K 1% 1/16W MF-LF 402

U7750 ISL6269 QFN
VIN, FSET, EN, FCCM, PGOOD, COMP, FB, VO, PVCC, VCC, UG, BOOT, PHASE, ISEN, LG, PGND, THRML PAD

P1V05S5_DRVH — GATE_NODE=TRUE — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM

P1V05S5_VBST — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM

P1V05S5_LL — SWITCH_NODE=TRUE — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM

P1V05S5_DRVL — GATE_NODE=TRUE — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM

C7770 0.22UF 10% 10V CERM 402

CRITICAL L7770 2.2UH-8.0A PCMB065T-SM

PLACEMENT_NOTE=Place XW7775 next to C7775

=PP1V05_S5_MCP

Vout = 1.052V
5A max output
(L7770 limit)
f = 400 kHz

XW7775 SM

C7776 4.7UF 20% 6V X5R 402

CRITICAL C7771 330UF 20% 2.0V POLY-TANT B2-SM

P1V05S5_VSNS

<Ra> R7780 3.74K 1% 1/16W MF-LF 402

<Rb> R7781 4.42K 1% 1/16W MF-LF 402

P1V05S5_FSET

R7752 38.3K 1% 1/16W MF-LF 402

C7753 0.01UF 10% 16V CERM 402

=P1V05S5_EN

P1V05_S5_PGOOD

P1V05_S5_COMP

R7753 100K 1% 1/16W MF-LF 402

C7755 22PF 5% 50V CERM 402

P1V05S5_VFB

P1V05S5_COMP_R

C7754 470PF 10% 50V CERM 402

XW7750 SM

(GND)

GND_P1V05S5_SGND — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V

(P1V05S5_VFB)

(=PP1V05_S5_REG)

Vout = 0.6V * (1 + Ra / Rb)

Misc Power Supplies

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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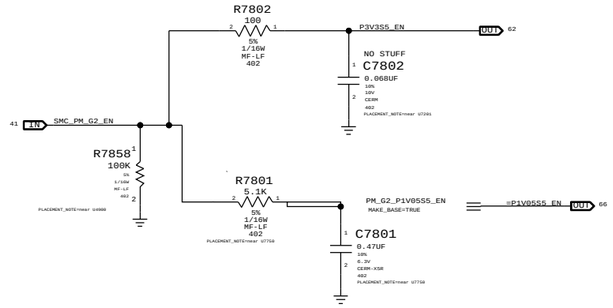
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

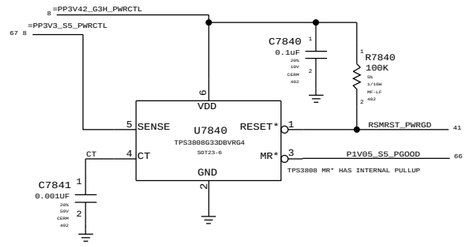
SCALE: NONE SHT 66 OF 98

3.3V 1,05V S5 ENABLE

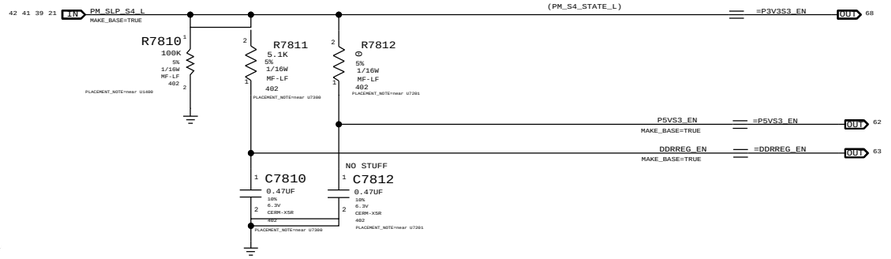


State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

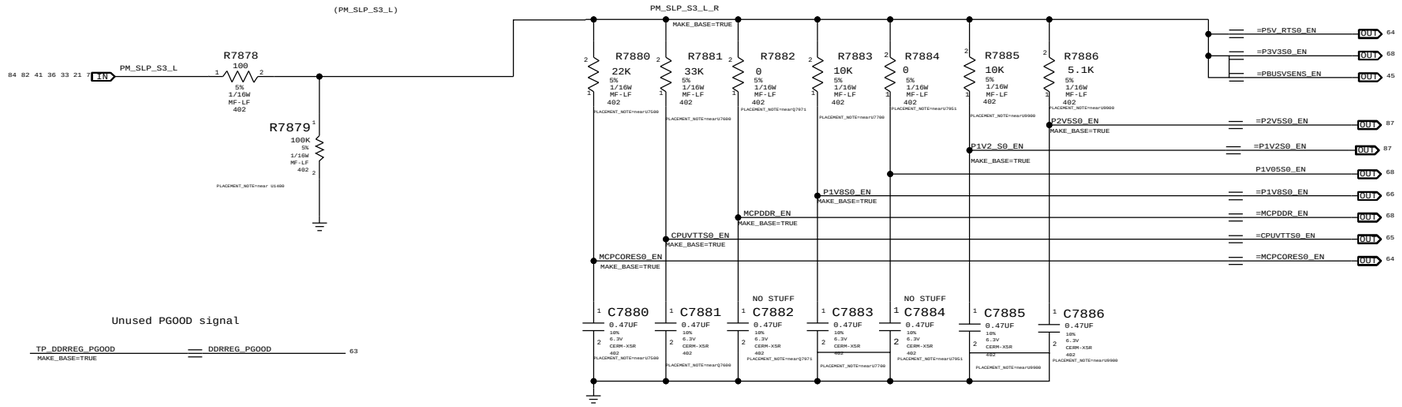
S5 rail PWRGD



3.3V,5V S3 ENABLE

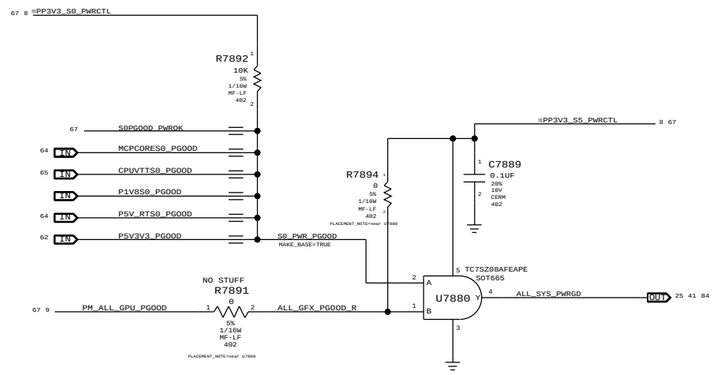


S0 ENABLE



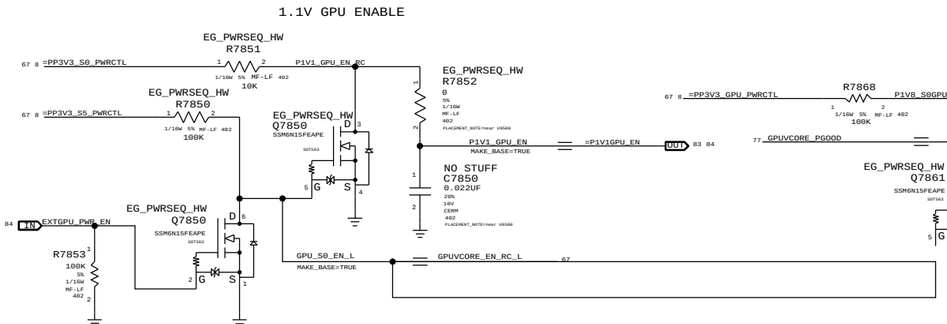
Other S0 RAILS

	PM_ALL_GFX_PGOOD
IG	high
EG	PM_ALL_GPU_PGOOD

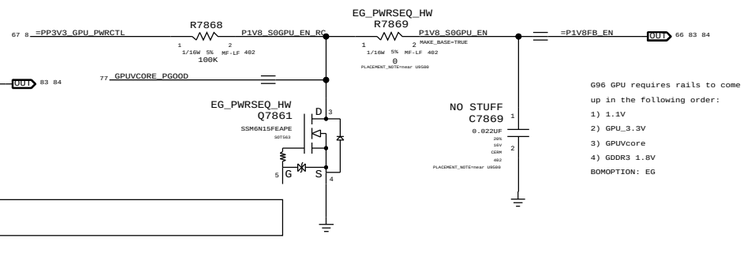


Unused PGOOD signal

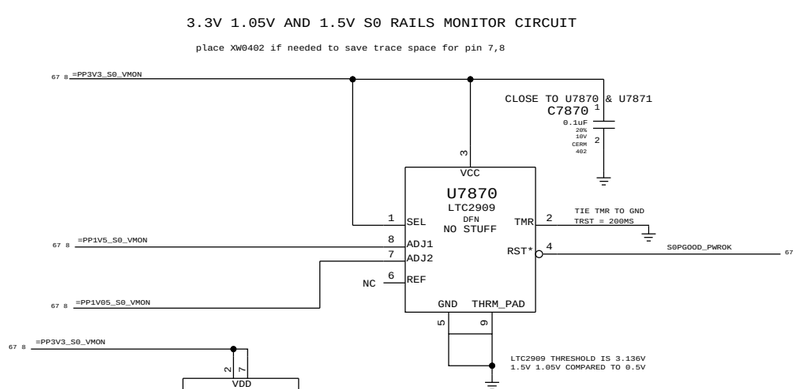
1.1V GPU ENABLE



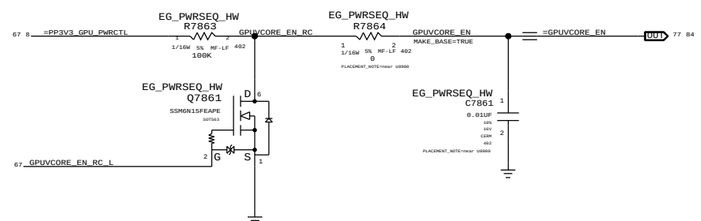
Graphic MEM ENABLE



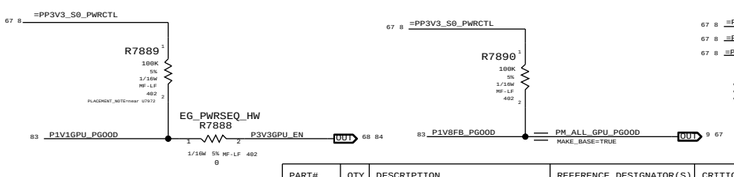
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



GPUVCORE ENABLE



EXT GPU PWRGD Pullup



U7871 IS TO REPLACE U7870

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2718	1	IC, QUAD VOLTAGE MONITOR	U7871	CRITICAL	

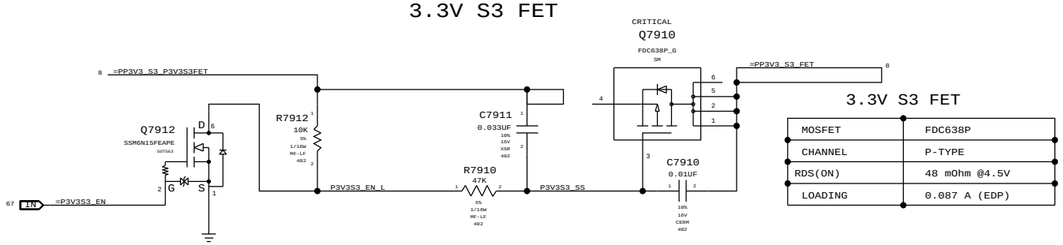
Power Control

SYNC_MASTER=YMA_K20 SYNC_DATE=09/09/2008

APPLE INC.

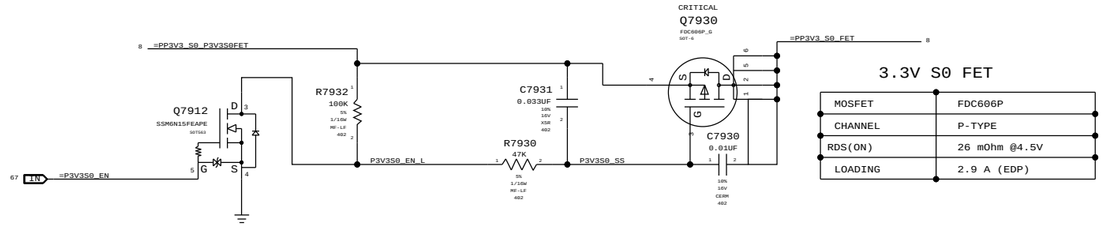
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 67 OF 98	

3.3V S3 FET



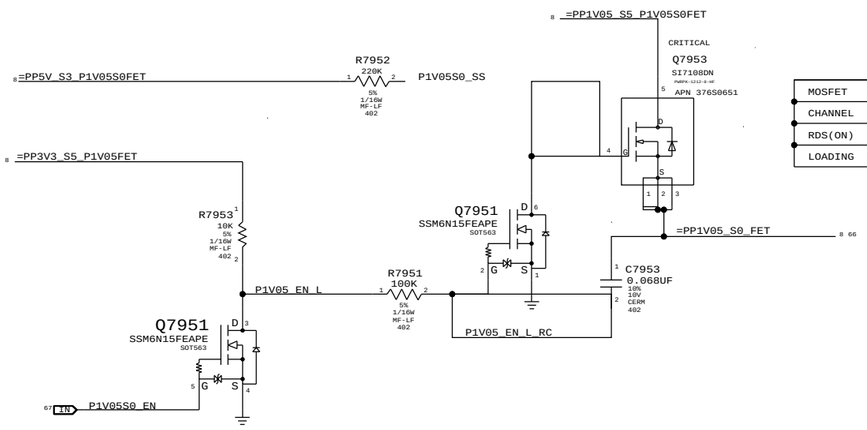
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

3.3V S0 FET



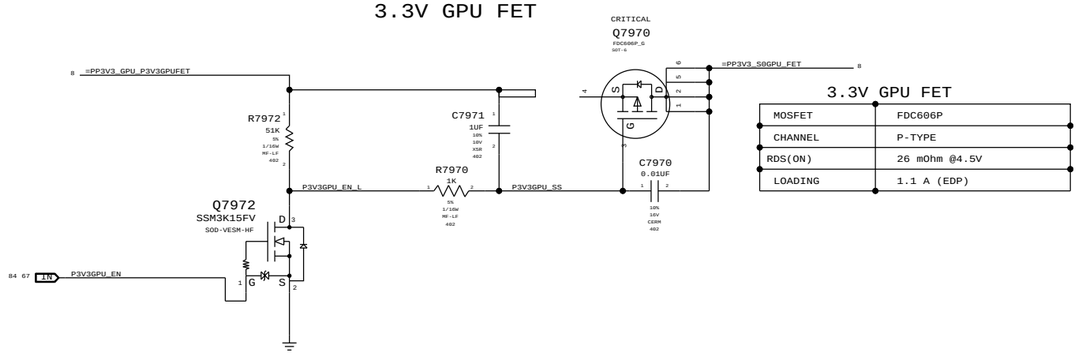
3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

1.05V S0 FET



1.05V S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.1 A (EDP)

3.3V GPU FET

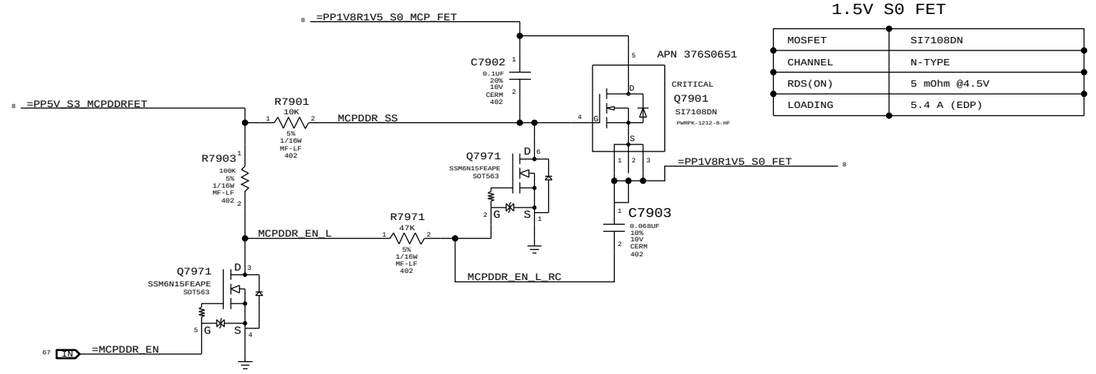


3.3V GPU FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)

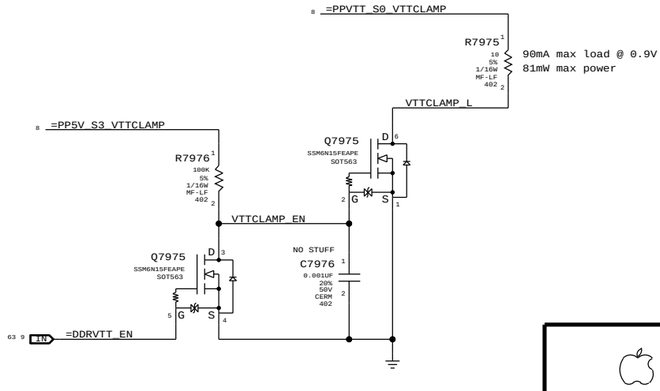
MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.

1.5V S0 FET



1.5V S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.4 A (EDP)



Power FETs	
SYNC_MASTER=YMA_K20	SYNC_DATE=05/19/2008

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-8071	B
	SCALE: NONE	SHT 68 OF 98	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

8 =PP1V1_GPU_PEX_PLLXVDD
8 =PP1V1_GPU_PEX_IOVDDQ
8 =PP1V1_GPU_PEX_IOVDD

PEX 1.1V Current = 2A

250mA

C8002 1UF 10% 6.3V CERM 402
C8001 4.7UF 20% 6.3V CERM 603
C8000 22UF 20% 6.3V CERM-X5R 805
C8003 1UF 10% 6.3V CERM 402
C8004 0.1UF 20% 10V CERM 402
C8005 0.1UF 20% 10V CERM 402

1500mA

C8008 1UF 10% 6.3V CERM 402
C8007 4.7UF 20% 6.3V CERM 603
C8006 22UF 20% 6.3V CERM-X5R 805
C8009 1UF 10% 6.3V CERM 402
C8010 0.1UF 20% 10V CERM 402
C8011 0.1UF 20% 10V CERM 402

180mA

L8015 10NH-600MA 0603

PP1V1_GPU_PEX_PLLVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V

C8017 0.1UF 20% 10V CERM 402
C8016 4.7UF 20% 6.3V CERM 603
C8015 4.7UF 20% 6.3V CERM 603

NC_GPU_DFM
NO_TEST=TRUE

OMIT

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NB9P-GS
BGA
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NC	A22	
NC	A7	
NC	P6	
	P7	PEX_IOVDD1 AK16
NC	R7	PEX_IOVDD2 AK17
	T7	PEX_IOVDD3 AK21
NC	V8	PEX_IOVDD4 AK24
NC	AB7	PEX_IOVDD5 AK27
NC	AD6	
NC	E25	
NC	G25	PEX_IOVDDQ1 AG11
NC	D25	PEX_IOVDDQ2 AG12
NC	K15	PEX_IOVDDQ3 AG13
NC	AL7	PEX_IOVDDQ4 AG15
NC	J7	PEX_IOVDDQ5 AG16
NC	E15	PEX_IOVDDQ6 AG17
NC	L7	PEX_IOVDDQ7 AG18
NC	A2	PEX_IOVDDQ8 AG22
		PEX_IOVDDQ9 AG23
		PEX_IOVDDQ10 AG24
		PEX_IOVDDQ11 AG25
		PEX_IOVDDQ12 AG26
		PEX_IOVDDQ13 AJ14
		PEX_IOVDDQ14 AJ15
		PEX_IOVDDQ15 AJ19
		PEX_IOVDDQ16 AJ21
		PEX_IOVDDQ17 AJ22
		PEX_IOVDDQ18 AJ24
		PEX_IOVDDQ19 AJ25
		PEX_IOVDDQ20 AJ27
		PEX_IOVDDQ21 AK18
		PEX_IOVDDQ22 AK20
		PEX_IOVDDQ23 AK23
		PEX_IOVDDQ24 AK26
		PEX_IOVDDQ25 AL16
		PEX_PLLVDD AG14
		VDD_SENSE AD20 GPU_VDD_SENSE 77
		GND_SENSE AD19 GPU_GND_SENSE 77

NC

OMIT

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BGA
SYMBOL 1 OF 9

90 9 IN	PEG_R2D_C_P<0>	C8020 0.1uF	AP17	PEX_RX0
90 9 IN	PEG_R2D_C_N<0>	C8021 0.1uF	AN17	PEX_RX0*
90 9 IN	PEG_R2D_C_P<1>	C8022 0.1uF	AN19	PEX_RX1
90 9 IN	PEG_R2D_C_N<1>	C8023 0.1uF	AP19	PEX_RX1*
90 9 IN	PEG_R2D_C_P<2>	C8024 0.1uF	AR19	PEX_RX2
90 9 IN	PEG_R2D_C_N<2>	C8025 0.1uF	AR20	PEX_RX2*
90 9 IN	PEG_R2D_C_P<3>	C8026 0.1uF	AP20	PEX_RX3
90 9 IN	PEG_R2D_C_N<3>	C8027 0.1uF	AN20	PEX_RX3*
90 9 IN	PEG_R2D_C_P<4>	C8028 0.1uF	AN22	PEX_RX4
90 9 IN	PEG_R2D_C_N<4>	C8029 0.1uF	AP22	PEX_RX4*
90 9 IN	PEG_R2D_C_P<5>	C8030 0.1uF	AR22	PEX_RX5
90 9 IN	PEG_R2D_C_N<5>	C8031 0.1uF	AR23	PEX_RX5*
90 9 IN	PEG_R2D_C_P<6>	C8032 0.1uF	AP23	PEX_RX6
90 9 IN	PEG_R2D_C_N<6>	C8033 0.1uF	AN23	PEX_RX6*
90 9 IN	PEG_R2D_C_P<7>	C8034 0.1uF	AN25	PEX_RX7
90 9 IN	PEG_R2D_C_N<7>	C8035 0.1uF	AP25	PEX_RX7*
90 9 IN	PEG_R2D_C_P<8>	C8036 0.1uF	AR25	PEX_RX8
90 9 IN	PEG_R2D_C_N<8>	C8037 0.1uF	AR26	PEX_RX8*
90 9 IN	PEG_R2D_C_P<9>	C8038 0.1uF	AP26	PEX_RX9
90 9 IN	PEG_R2D_C_N<9>	C8039 0.1uF	AN26	PEX_RX9*
90 9 IN	PEG_R2D_C_P<10>	C8040 0.1uF	AN28	PEX_RX10
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90 9 IN	PEG_R2D_C_P<11>	C8042 0.1uF	AR28	PEX_RX11
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90 9 IN	PEG_R2D_C_N<12>	C8045 0.1uF	AN29	PEX_RX12*
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90 9 IN	PEG_R2D_C_N<14>	C8049 0.1uF	AR32	PEX_RX14*
90 9 IN	PEG_R2D_C_P<15>	C8050 0.1uF	AR34	PEX_RX15
90 9 IN	PEG_R2D_C_N<15>	C8051 0.1uF	AP34	PEX_RX15*
90 17 IN	PEG_CLK100M_P		AR16	PEX_REFCLK
90 17 IN	PEG_CLK100M_N		AR17	PEX_REFCLK*
9 IN	GPU_RESET_L	R8020 0 5% 1/16W MF-LF 402	AM16	PEX_RST*
7	TP_PEX_CLKREQ_L		AR13	PEX_CLKREQ*

PEX_TX0	AL17	PEG_D2R_C_P<0>	C8055 0.1uF	PEG_D2R_P<0> OUT 9 90
PEX_TX0*	AM17	PEG_D2R_C_N<0>	C8056 0.1uF	PEG_D2R_N<0> OUT 9 90
PEX_TX1	AM18	PEG_D2R_C_P<1>	C8057 0.1uF	PEG_D2R_P<1> OUT 9 90
PEX_TX1*	AM19	PEG_D2R_C_N<1>	C8058 0.1uF	PEG_D2R_N<1> OUT 9 90
PEX_TX2	AL19	PEG_D2R_C_P<2>	C8059 0.1uF	PEG_D2R_P<2> OUT 9 90
PEX_TX2*	AK19	PEG_D2R_C_N<2>	C8060 0.1uF	PEG_D2R_N<2> OUT 9 90
PEX_TX3	AL20	PEG_D2R_C_P<3>	C8061 0.1uF	PEG_D2R_P<3> OUT 9 90
PEX_TX3*	AM20	PEG_D2R_C_N<3>	C8062 0.1uF	PEG_D2R_N<3> OUT 9 90
PEX_TX4	AM21	PEG_D2R_C_P<4>	C8063 0.1uF	PEG_D2R_P<4> OUT 9 90
PEX_TX4*	AM22	PEG_D2R_C_N<4>	C8064 0.1uF	PEG_D2R_N<4> OUT 9 90
PEX_TX5	AL22	PEG_D2R_C_P<5>	C8065 0.1uF	PEG_D2R_P<5> OUT 9 90
PEX_TX5*	AK22	PEG_D2R_C_N<5>	C8066 0.1uF	PEG_D2R_N<5> OUT 9 90
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PEX_TX6*	AM23	PEG_D2R_C_N<6>	C8068 0.1uF	PEG_D2R_N<6> OUT 9 90
PEX_TX7	AM24	PEG_D2R_C_P<7>	C8069 0.1uF	PEG_D2R_P<7> OUT 9 90
PEX_TX7*	AM25	PEG_D2R_C_N<7>	C8070 0.1uF	PEG_D2R_N<7> OUT 9 90
PEX_TX8	AL25	PEG_D2R_C_P<8>	C8071 0.1uF	PEG_D2R_P<8> OUT 9 90
PEX_TX8*	AK25	PEG_D2R_C_N<8>	C8072 0.1uF	PEG_D2R_N<8> OUT 9 90
PEX_TX9	AL26	PEG_D2R_C_P<9>	C8073 0.1uF	PEG_D2R_P<9> OUT 9 90
PEX_TX9*	AM26	PEG_D2R_C_N<9>	C8074 0.1uF	PEG_D2R_N<9> OUT 9 90
PEX_TX10	AM27	PEG_D2R_C_P<10>	C8075 0.1uF	PEG_D2R_P<10> OUT 9 90
PEX_TX10*	AM28	PEG_D2R_C_N<10>	C8076 0.1uF	PEG_D2R_N<10> OUT 9 90
PEX_TX11	AL28	PEG_D2R_C_P<11>	C8077 0.1uF	PEG_D2R_P<11> OUT 9 90
PEX_TX11*	AK28	PEG_D2R_C_N<11>	C8078 0.1uF	PEG_D2R_N<11> OUT 9 90
PEX_TX12	AK29	PEG_D2R_C_P<12>	C8079 0.1uF	PEG_D2R_P<12> OUT 9 90
PEX_TX12*	AL29	PEG_D2R_C_N<12>	C8080 0.1uF	PEG_D2R_N<12> OUT 9 90
PEX_TX13	AM29	PEG_D2R_C_P<13>	C8081 0.1uF	PEG_D2R_P<13> OUT 9 90
PEX_TX13*	AM30	PEG_D2R_C_N<13>	C8082 0.1uF	PEG_D2R_N<13> OUT 9 90
PEX_TX14	AM31	PEG_D2R_C_P<14>	C8083 0.1uF	PEG_D2R_P<14> OUT 9 90
PEX_TX14*	AM32	PEG_D2R_C_N<14>	C8084 0.1uF	PEG_D2R_N<14> OUT 9 90
PEX_TX15	AN32	PEG_D2R_C_P<15>	C8085 0.1uF	PEG_D2R_P<15> OUT 9 90
PEX_TX15*	AP32	PEG_D2R_C_N<15>	C8086 0.1uF	PEG_D2R_N<15> OUT 9 90
PEX_TSTCLK_OUT	AJ17	PEX_TSTCLK_P	R8060 200 1% 1/16W MF-LF 402	
PEX_TSTCLK_OUT*	AJ18	PEX_TSTCLK_N		
PEX_TERMP	AG21	PEX_TERMP_PD	R8050 2.49K 1% 1/16W MF-LF 402	
PEX_RFU1	AG19	NC		
PEX_RFU2	AG20	NC		

NV G96 PCI-E

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	69	98

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

B =PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 4.7UF 20% 6.3V X5R-CERM 402
C8101 4.7UF 20% 6.3V X5R-CERM 402
C8102 4.7UF 20% 6.3V X5R-CERM 402

C8103 0.47UF 10% 6.3V CERM-X5R 402
C8104 0.47UF 10% 6.3V CERM-X5R 402
C8105 0.47UF 10% 6.3V CERM-X5R 402
C8106 0.47UF 10% 6.3V CERM-X5R 402
C8107 0.47UF 10% 6.3V CERM-X5R 402

C8108 0.47UF 10% 6.3V CERM-X5R 402
C8109 0.47UF 10% 6.3V CERM-X5R 402
C8110 0.47UF 10% 6.3V CERM-X5R 402
C8111 0.47UF 10% 6.3V CERM-X5R 402
C8112 0.47UF 10% 6.3V CERM-X5R 402

C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402

C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

U8000
NB9P-GS
BGA
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OMIT

L11			V19
L12			V21
L13			V23
L14			V25
L15			W11
L16			W12
L17			W13
L18			W14
L19			W15
L20			W16
L21			W17
L22			W18
L23			W19
L24			AD24
L25			W21
M12			W22
M14			W23
M16			W24
M18			W25
M20			Y12
M22			Y14
M24			Y16
P11			Y18
P13			Y20
P15			Y22
P17			Y24
P19	VDD	VDD	AB11
P21			AB13
P23			AB15
P25			AB17
R11			AB19
R12			AB21
R13			AB23
R14			AB25
R15			AC11
R16			AC12
R17			AC13
R18			AC14
R19			AC15
R20			AC16
R21			AC17
R22			AC18
R23			AC19
R24			AC20
R25			AC21
T12			AC22
T14			AC23
T16			AC24
T18			AC25
T20			AD12
T22			AD14
T24			AD16
V11			AD18
V13			AD22
V15			W20
V17			

U8000
NB9P-GS
BGA
SYMBOL 8 OF 9

B3			V18
B6			V20
B9			V22
B12			V24
B15			V31
B21			Y11
B24			Y13
B27			Y15
B30			Y17
B33			Y19
C2			Y21
C34			Y23
E6			Y25
E9			AA2
E12			AA5
E15			AA11
E18			AA12
E24			AA13
E27			AA14
E30			AA15
F2			AA16
F5			AA17
F31			AA18
F34			AA19
J2			AA20
J5			AA21
J31			AA22
J34			AA23
L9			AA24
M2			AA25
M5			AA34
M11			AB12
M13			AB14
M15			AB16
M17			AB18
M19			AB20
M21			AB22
M23			AB24
M25			AC9
M31			AD2
M34			AD5
N11			AD11
N12			AD13
N13			AD15
N14			AD17
N15			AD21
N16			AD23
N17	GND	GND	AD25
N18			AD31
N19			AD34
N20			AE11
N21			AE12
N22			AE13
N23			AE14
N24			AE15
N25			AE16
P12			AE17
P14			AE18
P16			AE19
P18			AE20
P20			AE21
P22			AE22
P24			AE23
R2			AE24
R5			AE25
R31			AG2
R34			AG5
T11			AG31
T13			AG34
T15			AK2
T17			AK5
T19			AP33
T21			AK31
T23			AK34
T25			AL6
U11			AL9
U12			AL12
U13			AL15
U14			AL18
U15			AL21
U16			AL24
U17			AL27
U18			AL30
U19			AN2
U20			AN34
U21			AP3
U22			AP6
U23			AP9
U24			AP12
U25			AP15
V2			AP18
V5			AP21
V9			AP24
V12			AP27
V14			AP30
V16			

B =PP1V8_GPU_FBVDDQ

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603

C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402

C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402

C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

U8000
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OMIT

B18			J20
J17			J21
U27			J22
AB27			J24
AB29			J29
AC27			N27
AD27			P27
AE27			R27
AJ28			T27
E21	FBVDDQ	FBVDDQ	U29
G8			V27
G9			V29
G17			V34
G18			W27
G22			Y27
H29			AA27
J14			AA29
J15			AA31
J16			

NV G96 CORE/FB POWER

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	70	98

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT

U8000
NB9P-GS
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SYMBOL 3 OF 9

OMIT

U8000
NB9P-GS
BGA
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PLACEMENT_NOTE=Place close to U8000.

PLACEMENT_NOTE=Place close to U8000.

PLACEMENT_NOTE=Place close to U8000.

NO STUFF

NO STUFF

NO STUFF

GPU_FB_VREF_UNTERM_L
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

PP1V1_GPU_FBPLLAVDD_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.1V

CRITICAL

NV G96 FRAME BUFFER I/F

SYNC_MASTER=K20_MLB

SYNC_DATE=09/24/2008

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APPLE INC.

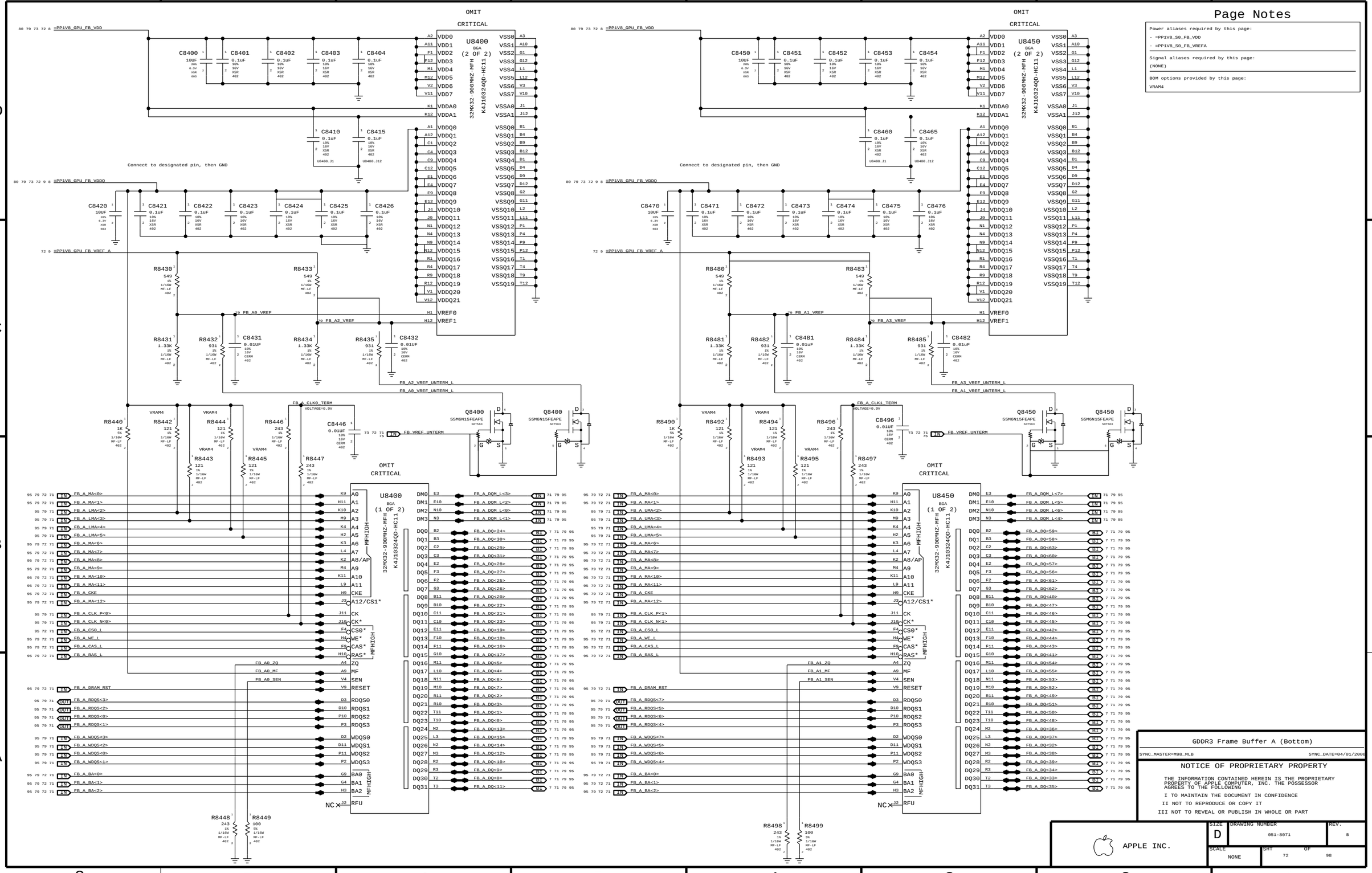
SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 71 OF 98	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4



GDDR3 Frame Buffer A (Bottom)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

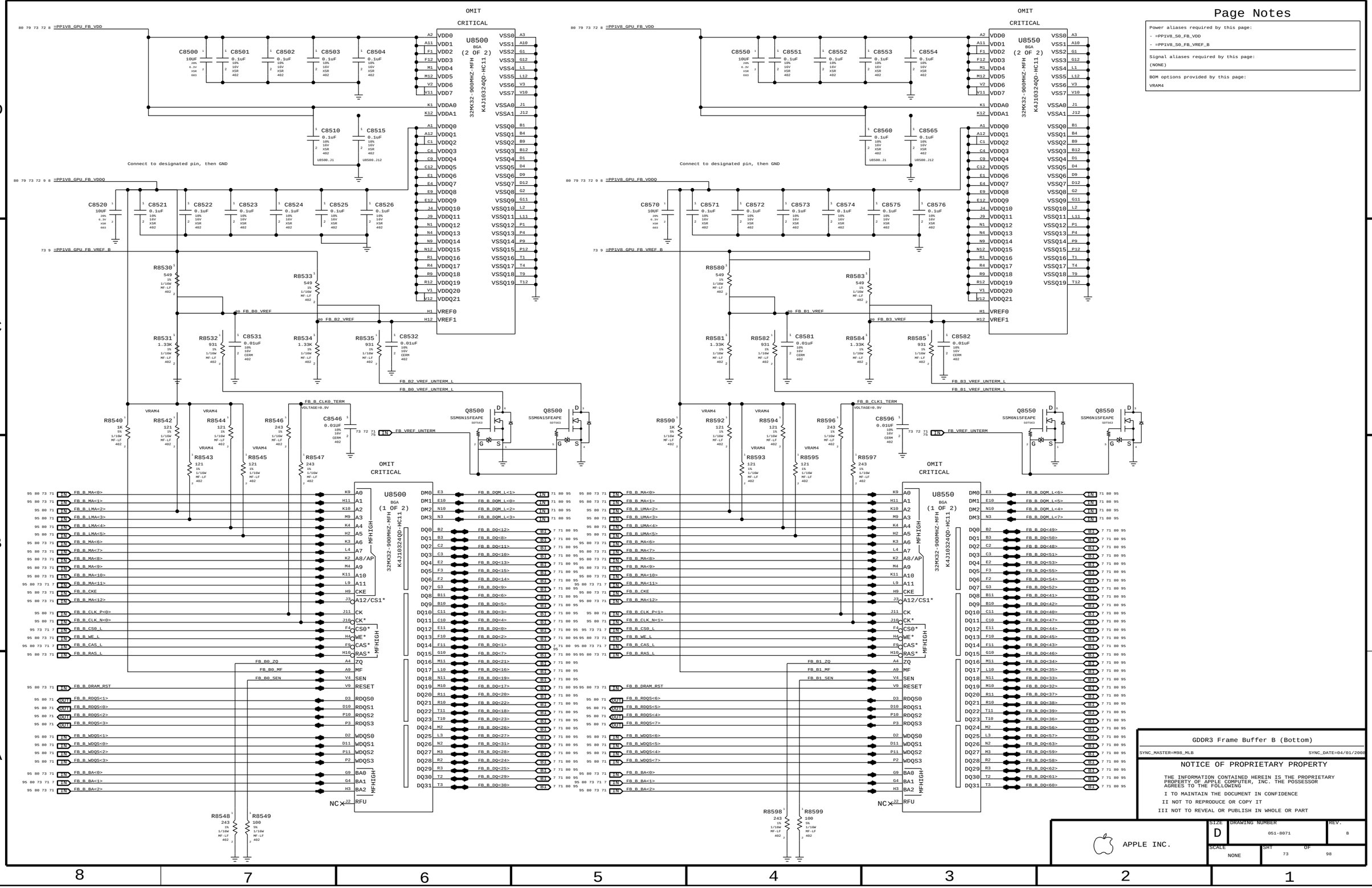
SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 72 OF 98	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4



GDDR3 Frame Buffer B (Bottom)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 73 OF 98	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

75 74 8 6 =PP3V3_GPU_VDD33 — 110mA

Typically <??mA

C8690 0.022UF 10% 16V CERM-X5R 402
C8692 0.022UF 10% 16V CERM-X5R 402
C8694 0.1UF 20% 10V CERM 402
C8696 0.47UF 10% 6.3V CERM-X5R 402
C8698 1UF 10% 6.3V CERM 402
C8691 0.022UF 10% 16V CERM-X5R 402
C8693 0.022UF 10% 16V CERM-X5R 402
C8695 0.1UF 20% 10V CERM 402
C8697 0.47UF 10% 6.3V CERM-X5R 402
C8600 0.47UF 10% 6.3V CERM-X5R 402
C8601 0.47UF 10% 6.3V CERM-X5R 402
C8602 0.47UF 10% 6.3V CERM-X5R 402

R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402

75 74 8 =PP3V3_GPU_MIO

R8620 49.9 1% 1/16W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
R8622 49.9 1% 1/16W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402
R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
R8619 10K 5% 1/16W MF-LF 402
R8660 10K 5% 1/16W MF-LF 402
C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402
C8617 0.1uF 10% 16V X5R 402
C8619 0.1uF 10% 16V X5R 402

CRITICAL
L8630 FERR-220-OHM 0402
8 =PP1V1_GPU_PLLVDD — PP1V1_GPU_PLLVDD_F — 65mA
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C8633 4.7UF 20% 6.3V CERM 603
C8630 4.7UF 20% 6.3V CERM 603
C8631 0.1uF 10% 16V X5R 402

CRITICAL
L8635 FERR-220-OHM 0402
8 =PP1V1_GPU_H_PLLVDD — PP1V1_GPU_H_PLLVDD_F — 25mA
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 0.1uF 10% 16V X5R 402

CRITICAL
L8640 FERR-220-OHM 0402
8 =PP1V1_GPU_VID_PLLVDD — PP1V1_GPU_VID_PLLVDD_F — 50mA
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 0.1uF 10% 16V X5R 402

OMIT

U8000
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J9	VDD33_1		
J10	VDD33_2		
J11	VDD33_3		
J12	VDD33_4		
J13	VDD33_5		
NC J25	RFU0		
NC J26	RFU1		
AK14	RFU0_GND		
K9	RFU1_GND		
75 GPU_ROM_CS_L — C3	ROM_CS*		
75 GPU_ROM_SCLK — D4	ROM_SCLK		
75 GPU_ROM_SI — D3	ROM_SI		
75 GPU_ROM_SO — C4	ROM_SO		
GPU_STRAP_REF_3V3_PD — N9	STRAP_REF_3V3		
GPU_STRAP_REF_MIOB_PD — M9	STRAP_REF_MIOB (IPD)		
P9	MIOA_VDDQ_1		
R9	MIOA_VDDQ_2		
T9	MIOA_VDDQ_3		
U9	MIOA_VDDQ_4		
AA9	MIOB_VDDQ_1		
AB9	MIOB_VDDQ_2		
W9	MIOB_VDDQ_3		
Y9	MIOB_VDDQ_4		
GPU_TESTMODE_PD — AP35	TESTMODE		
GPU_MIOA_VREF — N5	MIOA_VREF		
GPU_MIOB_VREF — AF1	MIOB_VREF		
74 GPU_MIOA_PD_VDDQ — U5	MIOA_CAL_PD_VDDQ		
74 GPU_MIOA_PU_GND — T5	MIOA_CAL_PU_GND		
74 GPU_MIOB_PD_VDDQ — AA7	MIOB_CAL_PD_VDDQ		
74 GPU_MIOB_PU_GND — AA6	MIOB_CAL_PU_GND		
AF9	SP_PLLVDD		
AE9	PLLVDD		
AD9	VID_PLLVDD		
75 IN GPU_XTALIN — B1	XTAL_IN		
75 OUT GPU_XTALOUT — B2	XTAL_OUT		
75 OUT GPU_XTALOUTBUFF — D1	XTAL_OUTBUFF		
75 IN GPU_XTALSSIN — D2	XTAL_SSIN		
GPIO0 K1	GPU_GPIO_0	BI	75
GPIO1 K2	GPU_GPIO_1	BI	75
GPIO2 K3	GPU_GPIO_2	BI	75
GPIO3 H3	GPU_GPIO_3	BI	75
GPIO4 H2	GPU_GPIO_4	BI	75
GPIO5 H1	GPU_GPIO_5	BI	75
GPIO6 H4	GPU_GPIO_6	BI	75
GPIO7 H5	GPU_GPIO_7	BI	75
GPIO8 H6	GPU_GPIO_8	BI	75
GPIO9 J7	GPU_GPIO_9	BI	75
GPIO10 K4	GPU_GPIO_10	BI	75
GPIO11 K5	GPU_GPIO_11	BI	75
GPIO12 H7	GPU_GPIO_12	BI	75
GPIO13 J4	GPU_GPIO_13	BI	75
GPIO14 J6	GPU_GPIO_14	BI	75
GPIO15 L1	GPU_GPIO_15	BI	75
GPIO16 L2	GPU_GPIO_16	BI	75
GPIO17 L4	GPU_GPIO_17	BI	75
GPIO18 M4	GPU_GPIO_18	BI	75
GPIO19 L7	GPU_GPIO_19	BI	75
GPIO20 L5	GPU_GPIO_20	BI	75
GPIO21 K6	GPU_GPIO_21	BI	75
GPIO22 L6	GPU_GPIO_22	BI	75
GPIO23 M6	GPU_GPIO_23	BI	75
HDA_SDI C7	GPU_HDA_SDI	OUT	75
HDA_SDO B7	GPU_HDA_SDO	OUT	75
HDA_SYNC A7	GPU_HDA_SYNC	OUT	75
HDA_BCLK D7	GPU_HDA_BCLK	OUT	75
HDA_RST* D6	GPU_HDA_RST_L	OUT	75
SPDIF A5	GPU_SPDIF	IN	75
BUFRST* A4	TP_GPU_BUFRST_L	OUT	7
JTAG_TCK AP14	GPU_JTAG_TCK	IN	6
JTAG_TDI AN14	GPU_JTAG_TDI	IN	6
JTAG_TDO AN16	GPU_JTAG_TDO	OUT	6
JTAG_TMS AR14	GPU_JTAG_TMS	IN	6
JTAG_TRST* AP16	GPU_JTAG_TRST_L	IN	6
MIOA_CLKIN N4	GPU_MIOA_CLKIN	IN	75
MIOA_CLKOUT R4	GPU_MIOA_CLKOUT_P	BI	75
MIOA_CLKOUT* T4	GPU_MIOA_CLKOUT_N	BI	75
MIOA_CTL3 P5	GPU_MIOA_CTL3	BI	75
MIOA_DE N2	GPU_MIOA_DE	BI	75
MIOA_D0 N1	GPU_MIOA_D<0>	BI	75
MIOA_D1 P4	GPU_MIOA_D<1>	BI	75
MIOA_D2 P1	GPU_MIOA_D<2>	BI	75
MIOA_D3 P2	GPU_MIOA_D<3>	BI	75
MIOA_D4 P3	GPU_MIOA_D<4>	BI	75
MIOA_D5 T3	GPU_MIOA_D<5>	BI	75
MIOA_D6 T2	GPU_MIOA_D<6>	BI	75
MIOA_D7 T1	GPU_MIOA_D<7>	BI	75
MIOA_D8 U4	GPU_MIOA_D<8>	BI	75
MIOA_D9 U1	GPU_MIOA_D<9>	BI	75
MIOA_D10 U2	GPU_MIOA_D<10>	BI	75
MIOA_D11 U3	GPU_MIOA_D<11>	BI	75
MIOA_D12 R6	GPU_MIOA_D<12>	BI	75
MIOA_D13 T6	GPU_MIOA_D<13>	BI	75
MIOA_D14 N6	GPU_MIOA_D<14>	BI	75
MIOA_HSYNC N3	GPU_MIOA_HSYNC	BI	75
MIOA_VSYNC L3	GPU_MIOA_VSYNC	BI	75
MIOB_CLKIN AE1	GPU_MIOB_CLKIN	IN	75
MIOB_CLKOUT V4	GPU_MIOB_CLKOUT_P	BI	75
MIOB_CLKOUT* W4	GPU_MIOB_CLKOUT_N	BI	75
MIOB_CTL3 W3	GPU_MIOB_CTL3	BI	75
MIOB_DE Y5	GPU_MIOB_DE	BI	75
MIOB_D0 Y1	GPU_MIOB_D<0>	BI	75
MIOB_D1 Y2	GPU_MIOB_D<1>	BI	75
MIOB_D2 Y3	GPU_MIOB_D<2>	BI	75
MIOB_D3 AB3	GPU_MIOB_D<3>	BI	75
MIOB_D4 AB2	GPU_MIOB_D<4>	BI	75
MIOB_D5 AB1	GPU_MIOB_D<5>	BI	75
MIOB_D6 AC4	GPU_MIOB_D<6>	BI	75
MIOB_D7 AC1	GPU_MIOB_D<7>	BI	75
MIOB_D8 AC2	GPU_MIOB_D<8>	BI	75
MIOB_D9 AC3	GPU_MIOB_D<9>	BI	75
MIOB_D10 AE3	GPU_MIOB_D<10>	BI	75
MIOB_D11 AE2	GPU_MIOB_D<11>	BI	75
MIOB_D12 U6	GPU_MIOB_D<12>	BI	75
MIOB_D13 W6	GPU_MIOB_D<13>	BI	75
MIOB_D14 Y6	GPU_MIOB_D<14>	BI	75
MIOB_D15 W5	GPU_STRAP<0>	BI	75
MIOB_D16 W7	GPU_STRAP<1>	BI	75
MIOB_D17 V7	GPU_STRAP<2>	BI	75
MIOB_HSYNC W1	GPU_MIOB_HSYNC	BI	75
MIOB_VSYNC W2	GPU_MIOB_VSYNC	BI	75
THERMDP B5	GPU_THERMD_P	IN	75
THERMDN B4	GPU_THERMD_N	OUT	75
PGOOD_OUT* C5	TP_GPU_PGOOD_OUT_L	OUT	7

NV G96 GPIO/MIO/MISC

SYNC_MASTER=K20_MLB — SYNC_DATE=09/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 74 OF 98	

GPIOs

Native Func		
GP	GPU_GPIO_0	NC_GPU_GPIO_0
HPDC	GPU_GPIO_1	DP_EG_HPD
LCD0_BL_PWM	GPU_GPIO_2	TP_LVDS_EG_BKL_PWM
LCD0_VDD	GPU_GPIO_3	EG_LCD_PWR_EN
LCD0_BL_EN	GPU_GPIO_4	EG_BKLT_EN
VID0	GPU_GPIO_5	TP_GPU_GSTATE<0>
VID1	GPU_GPIO_6	TP_GPU_GSTATE<1>
VID2/MEM_VID	GPU_GPIO_7	GPIO7_FBVDD_ALTVD
THERM	GPU_GPIO_8	SMC_GFX_OVERTEMP_R_L
FAN_PWM	GPU_GPIO_9	SMC_GFX_THROTTLE_R_L
MEM_VREF	GPU_GPIO_10	FB_VREF_UNTERM
SLI_SYNC	GPU_GPIO_11	GPU_VCORE_VID0
AC_DET	GPU_GPIO_12	GPU_VCORE_VID1
PWR_CTL0	GPU_GPIO_13	GPU_VCORE_VID2
PWR_CTL1	GPU_GPIO_14	TP_GPU_VCORE_VID3

GPIOs

Native Func		
HPDE	GPU_GPIO_15	NC_GPU_GPIO_15
DVI_MODE0	GPU_GPIO_16	EG_DP_CA_DET
HDMI_DETECT0	GPU_GPIO_17	NC_GPU_GPIO_17
DVI_MODE1	GPU_GPIO_18	NC_GPU_GPIO_18
HDMI_DETECT1	GPU_GPIO_19	NC_GPU_GPIO_19
HPDD	GPU_GPIO_20	NC_GPU_GPIO_20
HPDF	GPU_GPIO_21	NC_GPU_GPIO_21
SWAPRDY_A	GPU_GPIO_22	NC_GPU_GPIO_22
GP	GPU_GPIO_23	NC_GPU_GPIO_23

Renamed signals

GPU_XTALOUT — GPU_XTALOUT
GPU_CLK27M — GPU_XTALIN
GPU_CLK27M_SS — GPU_XTALSSIN
GPU_TDIODE_P — GPU_THERMD_P
GPU_TDIODE_N — GPU_THERMD_N
LVDS_EG_DDC_CLK — GPU_I2CA_SCL
LVDS_EG_DDC_DATA — GPU_I2CA_SDA
DP_EG_DDC_CLK — GPU_I2CB_SCL
DP_EG_DDC_DATA — GPU_I2CB_SDA

Unused I2C Buses

NC_GPU_I2CC_SCL — GPU_I2CC_SCL
NC_GPU_I2CC_SDA — GPU_I2CC_SDA
NC_GPU_I2CD_SCL — GPU_I2CD_SCL
NC_GPU_I2CD_SDA — GPU_I2CD_SDA
NC_GPU_I2CE_SCL — GPU_I2CE_SCL
NC_GPU_I2CE_SDA — GPU_I2CE_SDA
NC_GPU_I2CH_SCL — GPU_I2CH_SCL
NC_GPU_I2CH_SDA — GPU_I2CH_SDA

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

Unused signals

NC_GPU_SPDIF — GPU_SPDIF
NC_CPU_HDA_SDI — GPU_HDA_SDI
NC_CPU_HDA_SD0 — GPU_HDA_SDO
NC_CPU_HDA_SYNC — GPU_HDA_SYNC
NC_CPU_HDA_BCLK — GPU_HDA_BCLK
NC_CPU_HDA_RST_L — GPU_HDA_RST_L
NC_FBA_MA<13> — FB_A_MA<13>
NC_FBB_MA<13> — FB_B_MA<13>
NC_FBA_CMD28 — TP_FBA_CMD28
NC_FBC_CMD28 — TP_FBC_CMD28
NC_FBA_CMD29 — TP_FBA_CMD29
NC_FBC_CMD29 — TP_FBC_CMD29
NC_FBA_CMD30 — TP_FBA_CMD30
NC_FBC_CMD30 — TP_FBC_CMD30
NC_GPU_ROM_CS_L — GPU_ROM_CS_L

TP_LVDS_EG_B_CLK_P — LVDS_EG_B_CLK_P
TP_LVDS_EG_B_CLK_N — LVDS_EG_B_CLK_N
NC_LVDS_EG_A_DATA_P<3> — LVDS_EG_A_DATA_P<3>
NC_LVDS_EG_A_DATA_N<3> — LVDS_EG_A_DATA_N<3>
NC_LVDS_EG_B_DATA_P<3> — LVDS_EG_B_DATA_P<3>
NC_LVDS_EG_B_DATA_N<3> — LVDS_EG_B_DATA_N<3>

Config Straps

=PP3V3_GPU_MIO

OMIT: R8707 2.0K 5% 1/16W MF-LF 402
R8709 4.99K 1% 1/16W MF-LF 402
NO STUFF: R8711 4.99K 1% 1/16W MF-LF 402

GPU_ROM_SI (OUT)
GPU_ROM_SO (IN)
GPU_ROM_SCLK (IN)

OMIT: R8708 45.3K 1% 1/16W MF-LF 402
NO STUFF: R8710 2.0K 5% 1/16W MF-LF 402
R8712 15.0K 1% 1/16W MF-LF 402

Physical Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

Strap S1/S2 Bit[3:0] PU/PD Rval
0 0000 PD 5k
1 0001 PD 10k
2 0010 PD 15k
3 0011 PD 20k
4 0100 PD 25k
5 0101 PD 30k
6 0110 PD 35k
7 0111 PD 45k

Strap S1/S2 Bit[3:0] PU/PD Rval
8 1000 PU 5k
9 1001 PU 10k
A 1010 PU 15k
B 1011 PU 20k
C 1100 PU 25k
D 1101 PU 30k
E 1110 PU 35k
F 1111 PU 45k

=PP3V3_GPU_MIO

NO STUFF: R8701 45.3K 1% 1/16W MF-LF 402
NO STUFF: R8703 10K 1% 1/16W MF-LF 402
NO STUFF: R8705 10K 1% 1/16W MF-LF 402

GPU_STRAP<0> (BI)
GPU_STRAP<1> (BI)
GPU_STRAP<2> (BI)

NO STUFF: R8702 2.0K 5% 1/16W MF-LF 402
R8704 10K 1% 1/16W MF-LF 402
R8706 45.3K 1% 1/16W MF-LF 402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8707		VRAM_1024_SAMSUNG
114S0368	1	RES,MTL FILM,1/16W,35.7K,1,0402,SMD,LF	R8708		VRAM_512_HYNIX

=PP3V3_S0_DDC_LCD
=PP3V3_GPU_VDD33

R8750 4.7K 5% 1/16W MF-LF 402
R8751 4.7K 5% 1/16W MF-LF 402
R8752 4.7K 5% 1/16W MF-LF 402
R8753 4.7K 5% 1/16W MF-LF 402

DP_EG_DDC_CLK (IN)
DP_EG_DDC_DATA (BI)
DP_IG_DDC_CLK (IN)
DP_IG_DDC_DATA (BI)

=PP3V3_GPU_VDD33

DP_CA_DET_EG_FET
R8742 100K 1% 1/16W MF-LF 402
DP_CA_DET_EG_FET
Q8742
SOD-VESM-HF
SSM3K15FV

EG_DP_CA_DET — DP_CA_DET (IN)

R8743 0 5% 1/16W MF-LF 402
DP_CA_DET_EG (IN)
DP_CA_DET_EG_PLD

Isolation FETs for DP MUX inputs

GPU 27MHz Crystal

GPU_CLK27M (IN)
R8783 0 5% 1/16W MF-LF 402
GPU_CLK27M_XTALOUT_R
C8780 12pF 5% 50V CERM 402

NO STUFF: R8782 10M 5% 1/16W MF-LF 402
CRITICAL: Y8780 27MHZ SM-2 — NC / NC
C8781 12pF 5% 50V CERM 402
GPU_XTALOUT (OUT)

=PP3V3_GPU_VDD33

R8796 2.2K 5% 1/16W MF-LF 402
R8797 2.2K 5% 1/16W MF-LF 402

SMC_GFX_OVERTEMP_R_L — R8798 0 5% 1/16W MF-LF 402 — SMC_GFX_OVERTEMP_L (OUT)
SMC_GFX_THROTTLE_R_L — R8799 0 5% 1/16W MF-LF 402 — SMC_GFX_THROTTLE_L (OUT)

EG_LCD_PWR_EN (OUT)
EG_BKLT_EN (OUT)
GPIO7_FBVDD_ALTVD (OUT)
FB_VREF_UNTERM (OUT)

R8792 10K 5% 1/16W MF-LF 402
R8793 10K 5% 1/16W MF-LF 402
R8794 10K 5% 1/16W MF-LF 402
NO STUFF: R8795 10K 5% 1/16W MF-LF 402

G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

NC_GPU_MIOA_CLKOUT_P — GPU_MIOA_CLKOUT_P
NC_GPU_MIOA_CLKOUT_N — GPU_MIOA_CLKOUT_N
NC_GPU_MIOA_CTL3 — GPU_MIOA_CTL3
TP_GPU_MIOA_DE — GPU_MIOA_DE
TP_GPU_MIOA_D<9..0> — GPU_MIOA_D<9..0>
NC_GPU_MIOA_CLKIN — GPU_MIOA_CLKIN
NC_GPU_MIOA_D<14..10> — GPU_MIOA_D<14..10>
NC_GPU_MIOA_HSYNC — GPU_MIOA_HSYNC
NC_GPU_MIOA_VSYNC — GPU_MIOA_VSYNC

NC_GPU_MIOB_CLKIN — GPU_MIOB_CLKIN
NC_GPU_MIOB_CLKOUT_P — GPU_MIOB_CLKOUT_P
NC_GPU_MIOB_CLKOUT_N — GPU_MIOB_CLKOUT_N
NC_GPU_MIOB_CTL3 — GPU_MIOB_CTL3
NC_GPU_MIOB_DE — GPU_MIOB_DE
NC_GPU_MIOB_D<14..0> — GPU_MIOB_D<14..0>
NC_GPU_MIOB_VSYNC — GPU_MIOB_VSYNC
NC_GPU_MIOB_HSYNC — GPU_MIOB_HSYNC

Unused Clocks

GPU_XTALSSIN
GPU_XTALOUTBUFF
GPU_SS_INT

R8780 10K 5% 1/16W MF-LF 402
R8781 10K 5% 1/16W MF-LF 402

G96 GPIOs & Straps

SYNC_MASTER=M98_MLB
SYNC_DATE=05/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 75 OF 98	

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IFPX

CRITICAL
L8800
FERR-220-OHM
0402

?mA peak per diff pair
?mA peak for all pairs

C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402

Place at AG9
Place at AG10

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

CRITICAL
L8805
FERR-220-OHM
0402

80mA peak

C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPEF_RSET 76
GPU_IFPCD_RSET 76
GPU_IFPAB_RSET 76

R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402

=PP1V1_GPU_IFPCD_IOVDD

CRITICAL
L8810
FERR-220-OHM
0402

?mA peak per diff pair
?mA peak for all pairs

C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402

Place at AJ8
Place at AK8

PP1V1_GPU_IFPCD_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

CRITICAL
L8815
FERR-220-OHM
0402

160mA peak

C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPCD_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP1V1_GPU_IFPEF_IOVDD_F 76
PP1V8_GPU_IFPEF_PLLVDD_F 76

Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

OMIT

U8000
NB9P-GS
BGA
SYMBOL 5 OF 9

AG9	IFPA_IOVDD		
AG10	IFPB_IOVDD		
AJ8	IFPC_IOVDD		
AK8	IFPD_IOVDD		
AE7	IFPE_IOVDD		
AD7	IFPF_IOVDD		
AK9	IFPAB_PLLVDD		
AJ11	IFPAB_RSET		
AJ9	IFPCD_PLLVDD		
AK7	IFPCD_RSET		
AJ6	IFPEF_PLLVDD		
AL1	IFPEF_RSET		
G1	I2CA_SCL		
G4	I2CA_SDA		
E3	I2CC_SCL		
E4	I2CC_SDA		
E2	I2CS_SCL		
E1	I2CS_SDA		
F6	I2CH_SCL		
G6	I2CH_SDA		
G3	I2CB_SCL		
G2	I2CB_SDA		
F4	I2CD_SCL		
G5	I2CD_SDA		
D5	I2CE_SCL		
E5	I2CE_SDA		
AM11	IFPA_TXC	LVDS_EG_A_CLK_P	OUT 84 95
AM12	IFPA_TXC*	LVDS_EG_A_CLK_N	OUT 84 95
AM8	IFPA_TXD0	LVDS_EG_A_DATA_P<0>	OUT 84 95
AL8	IFPA_TXD0*	LVDS_EG_A_DATA_N<0>	OUT 84 95
AM10	IFPA_TXD1	LVDS_EG_A_DATA_P<1>	OUT 84 95
AM9	IFPA_TXD1*	LVDS_EG_A_DATA_N<1>	OUT 84 95
AK10	IFPA_TXD2	LVDS_EG_A_DATA_P<2>	OUT 84 95
AL10	IFPA_TXD2*	LVDS_EG_A_DATA_N<2>	OUT 7 84 95
AK11	IFPA_TXD3	LVDS_EG_A_DATA_P<3>	OUT 75
AL11	IFPA_TXD3*	LVDS_EG_A_DATA_N<3>	OUT 75
AP13	IFPB_TXC	LVDS_EG_B_CLK_P	OUT 75
AN13	IFPB_TXC*	LVDS_EG_B_CLK_N	OUT 75
AN8	IFPB_TXD4	LVDS_EG_B_DATA_P<0>	OUT 84 95
AP8	IFPB_TXD4*	LVDS_EG_B_DATA_N<0>	OUT 84 95
AP10	IFPB_TXD5	LVDS_EG_B_DATA_P<1>	OUT 84 95
AN10	IFPB_TXD5*	LVDS_EG_B_DATA_N<1>	OUT 84 95
AR11	IFPB_TXD6	LVDS_EG_B_DATA_P<2>	OUT 84 95
AR10	IFPB_TXD6*	LVDS_EG_B_DATA_N<2>	OUT 84 95
AN11	IFPB_TXD7	LVDS_EG_B_DATA_P<3>	OUT 75
AP11	IFPB_TXD7*	LVDS_EG_B_DATA_N<3>	OUT 75
AP2	IFPC_AUX	DP_EG_AUX_CH_P	OUT 81 95
AN3	IFPC_AUX*	DP_EG_AUX_CH_N	OUT 81 95
AM7	IFPC_L0	DP_EG_ML_P<0>	OUT 81 95
AM6	IFPC_L0*	DP_EG_ML_N<0>	OUT 81 95
AL5	IFPC_L1	DP_EG_ML_P<1>	OUT 81 95
AM5	IFPC_L1*	DP_EG_ML_N<1>	OUT 81 95
AM3	IFPC_L2	DP_EG_ML_P<2>	OUT 81 95
AM4	IFPC_L2*	DP_EG_ML_N<2>	OUT 81 95
AP1	IFPC_L3	DP_EG_ML_P<3>	OUT 81 95
AR2	IFPC_L3*	DP_EG_ML_N<3>	OUT 81 95
AP4	IFPD_AUX		NC
AN4	IFPD_AUX*		NC
AR6	IFPD_L0		NC
AP6	IFPD_L0*		NC
AL7	IFPD_L1		NC
AK7	IFPD_L1*		NC
AN5	IFPD_L2		NC
AP5	IFPD_L2*		NC
AR5	IFPD_L3		NC
AR4	IFPD_L3*		NC
AE4	IFPE_AUX		NC
AD4	IFPE_AUX*		NC
AH6	IFPE_L0		NC
AH5	IFPE_L0*		NC
AH4	IFPE_L1		NC
AG4	IFPE_L1*		NC
AF4	IFPE_L2		NC
AF5	IFPE_L2*		NC
AE6	IFPE_L3		NC
AE5	IFPE_L3*		NC
AF3	IFPF_AUX		NC
AF2	IFPF_AUX*		NC
AL2	IFPF_L0		NC
AL3	IFPF_L0*		NC
AJ3	IFPF_L1		NC
AJ4	IFPF_L1*		NC
AJ2	IFPF_L2		NC
AK2	IFPF_L2*		NC
AK3	IFPF_L3		NC
AK4	IFPF_L3*		NC
AJ12	DACA_VDD		
AK12	DACA_VREF		NC
AK13	DACA_RSET		NC
AC6	DACB_VDD		
AC5	DACB_VREF		NC
AD6	DACB_RSET		NC
AG7	DACC_VDD		
AK6	DACC_VREF		NC
AK7	DACC_RSET		NC
AM13	DACA_RED		NC
AM14	DACA_GREEN		NC
AL13	DACA_BLUE		NC
AM15	DACA_HSYNC		NC
AL15	DACA_VSYNC		NC
AA4	DACB_RED		NC
AB4	DACB_GREEN		NC
Y4	DACB_BLUE		NC
AB5	DACB_CSYNC		NC
AK4	DACC_RED		NC
AL4	DACC_GREEN		NC
AJ4	DACC_BLUE		NC
AM1	DACC_HSYNC		NC
AK1	DACC_VSYNC		NC

GPU_DACA_VDD
GPU_DACB_VDD
GPU_DACC_VDD

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

R8861 1K 5% 1/16W MF-LF 402
R8860 1K 5% 1/16W MF-LF 402
NO STUFF

NV G96 Video Interfaces

SYNC_MASTER=K20_MLB
SYNC_DATE=09/24/2008

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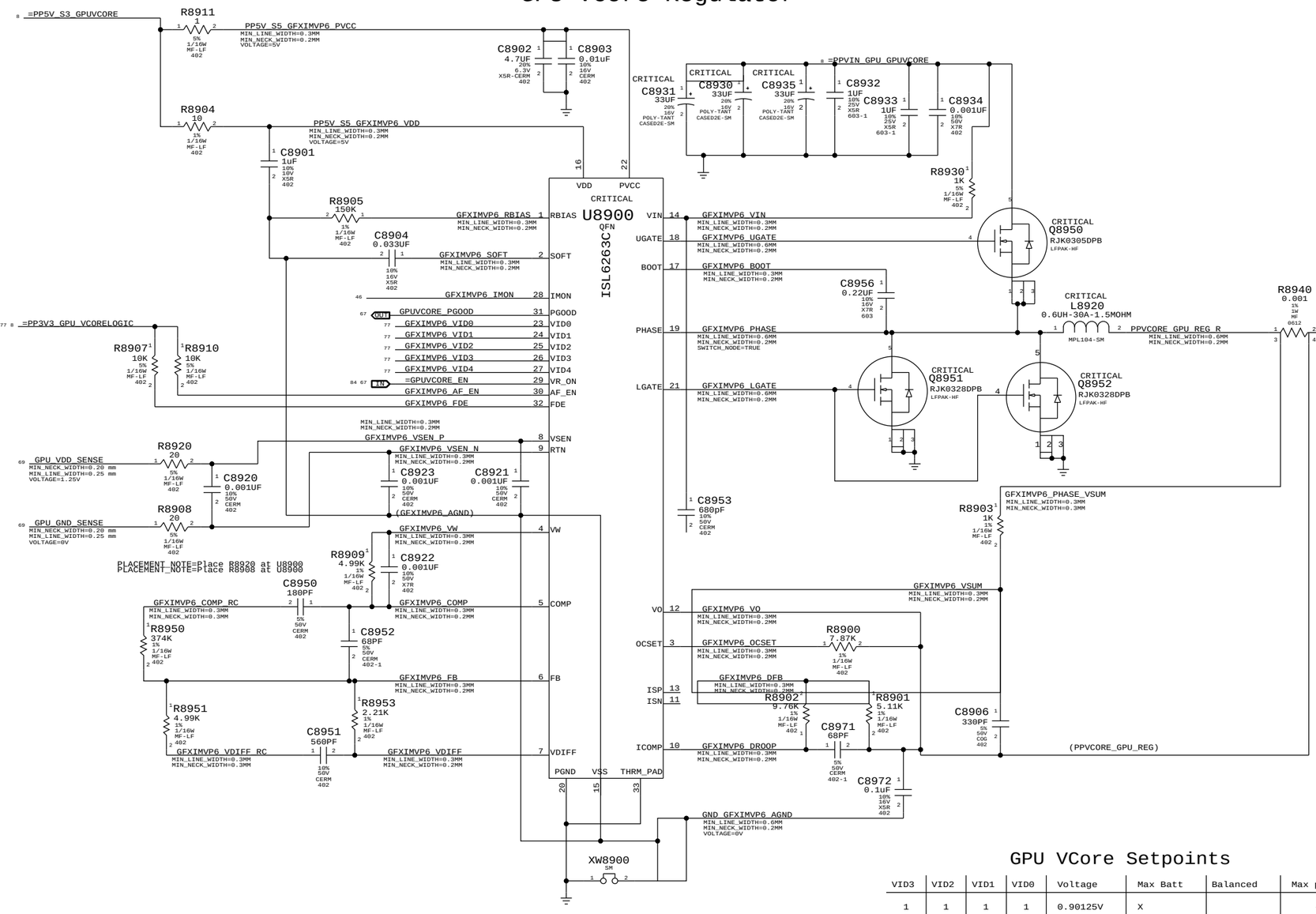
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 76 OF 98	

GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	X		-
1	1	1	0	0.92700V	-	X	-
1	0	1	1	1.00425V	-	-	X

Other VID states may not be valid

Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

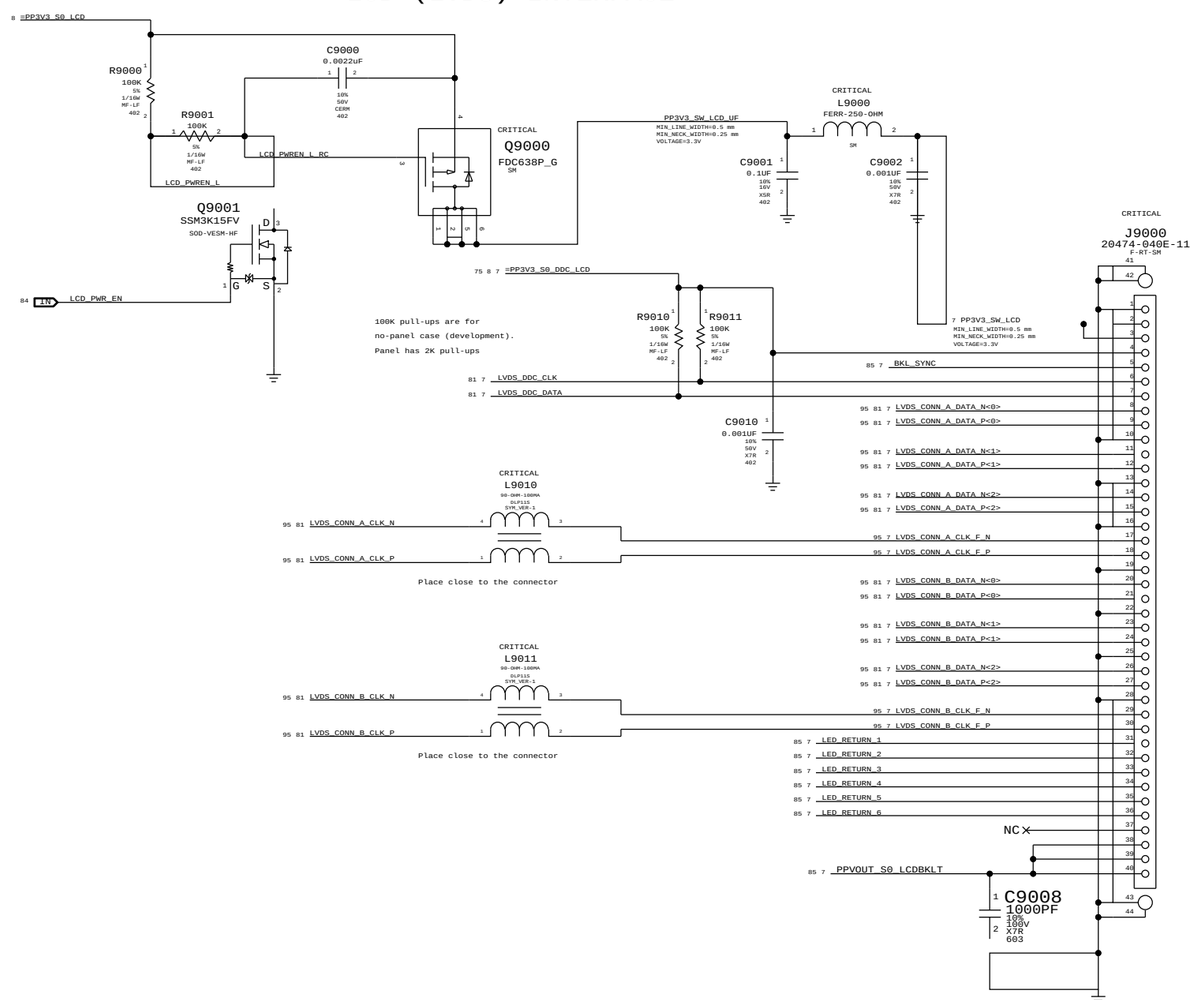
GPU (G96) CORE SUPPLY

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 77 OF 98	

LCD (LVDS) INTERFACE



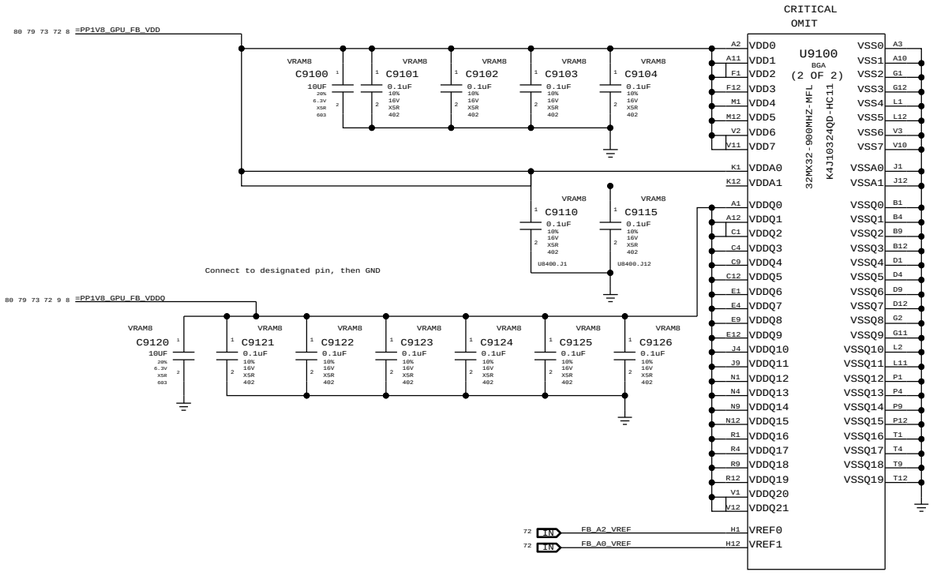
518S0651

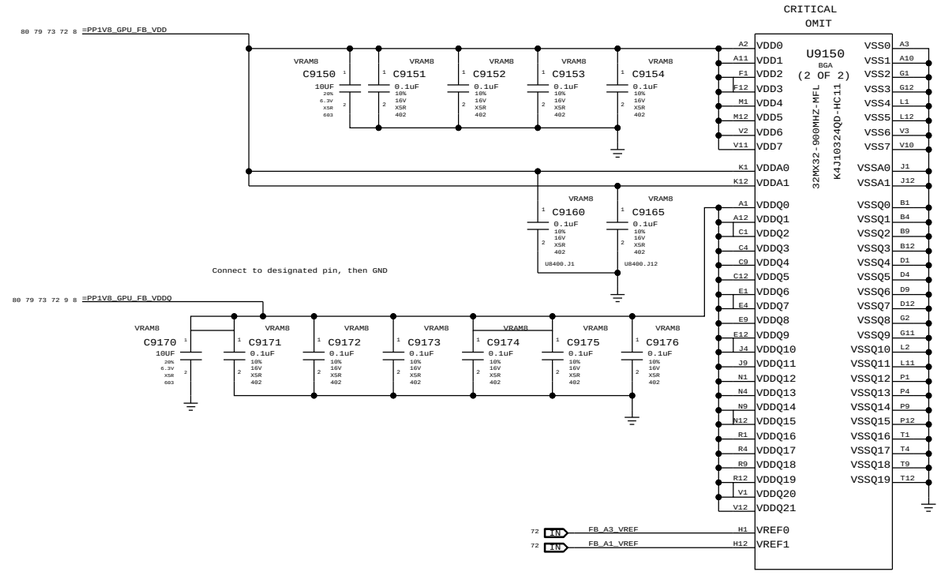
LVDS Display Connector

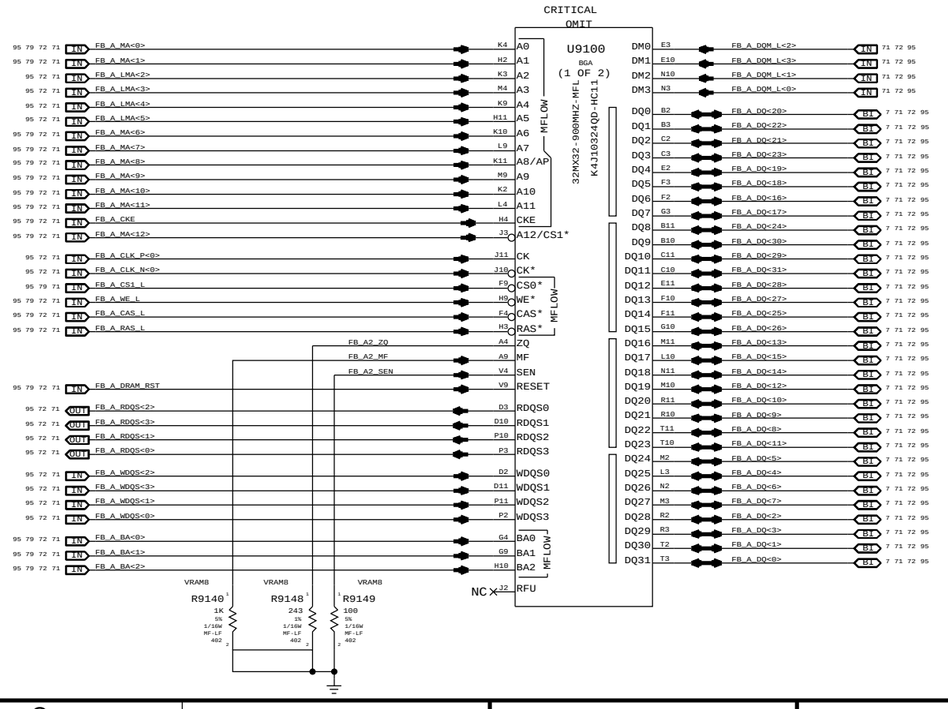
SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

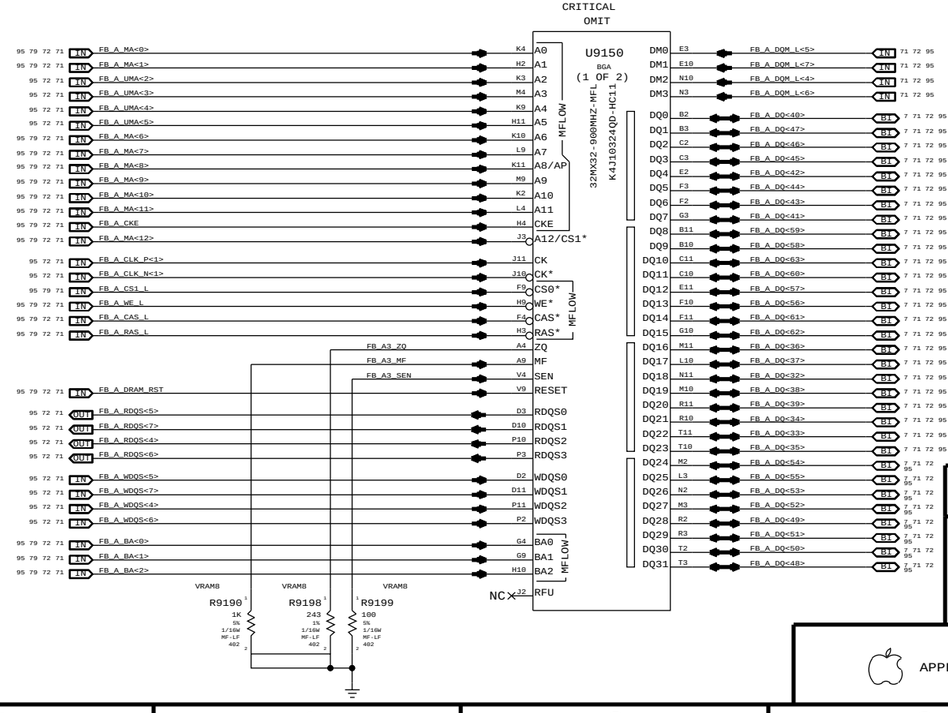
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	78	98









Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

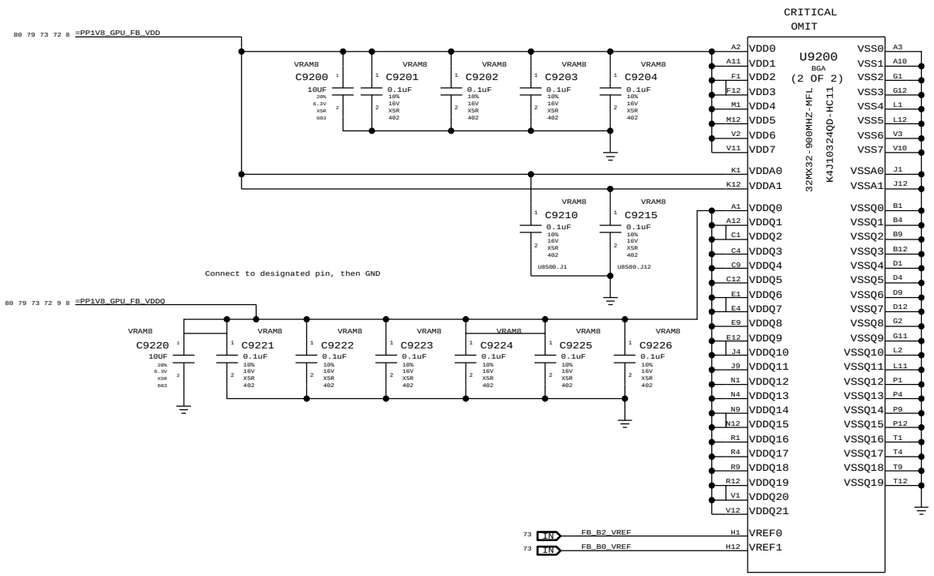
BOM options provided by this page:
VRAM8

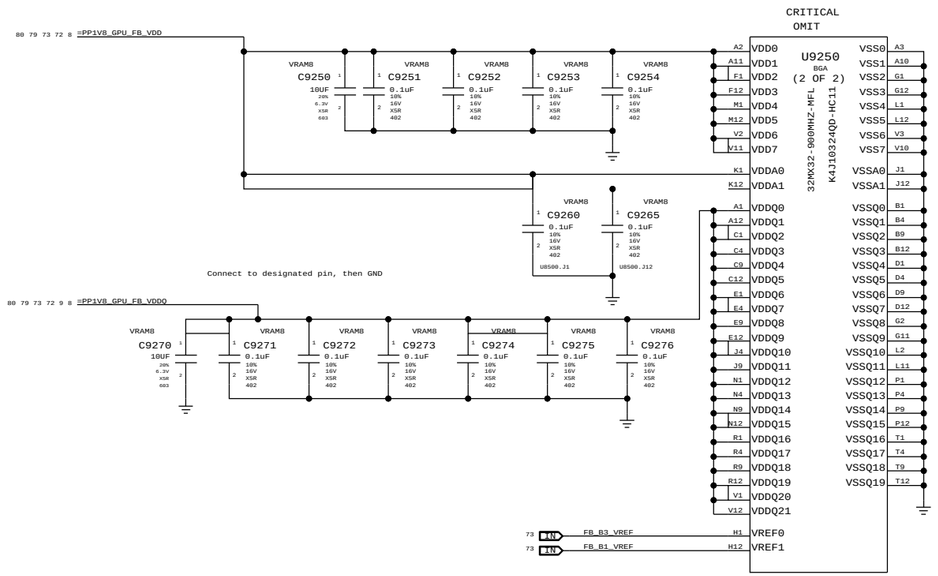
GDDR3 Frame Buffer A (Top)

SYNC_MASTER=M99_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 79 OF 98	





Page Notes

Power aliases required by this page:

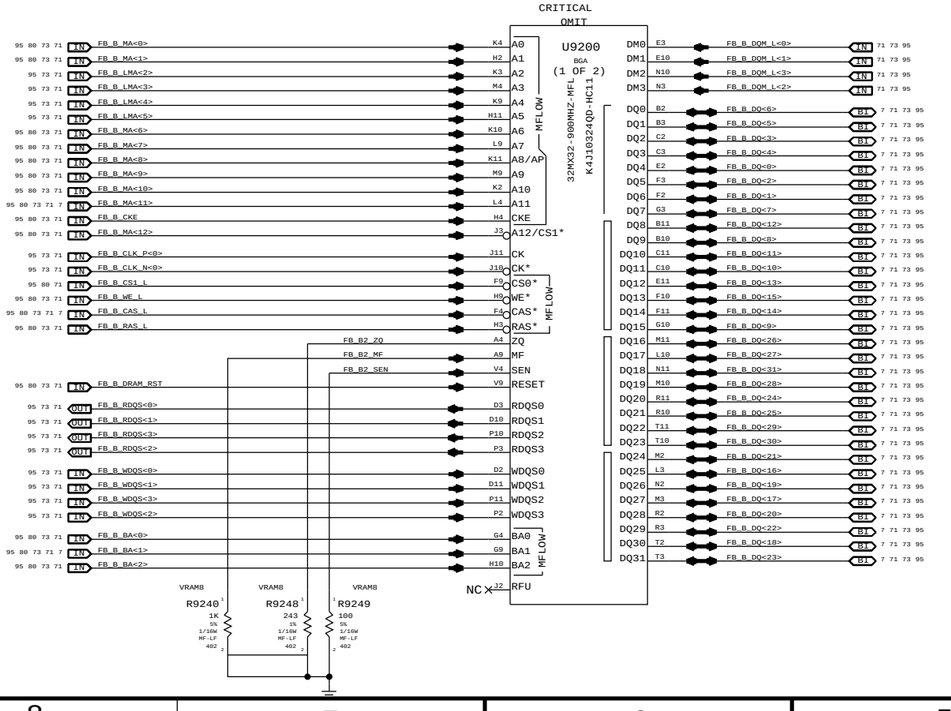
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

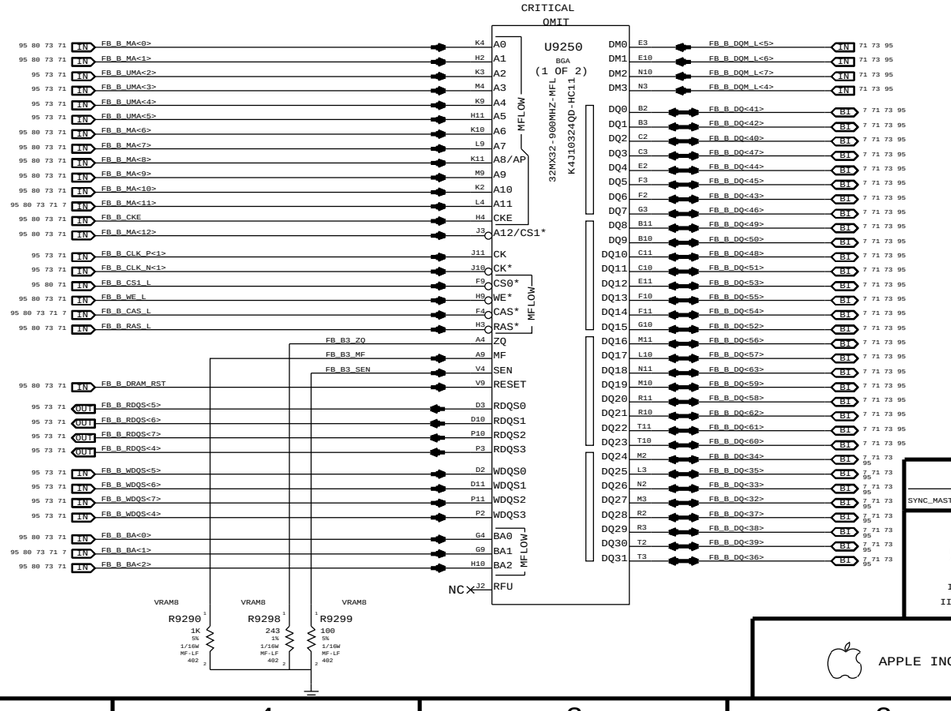
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM8





GDDR3 Frame Buffer B (Top)

SYNC_MASTER=M88_MLB SYNC_DATE=11/01/2007

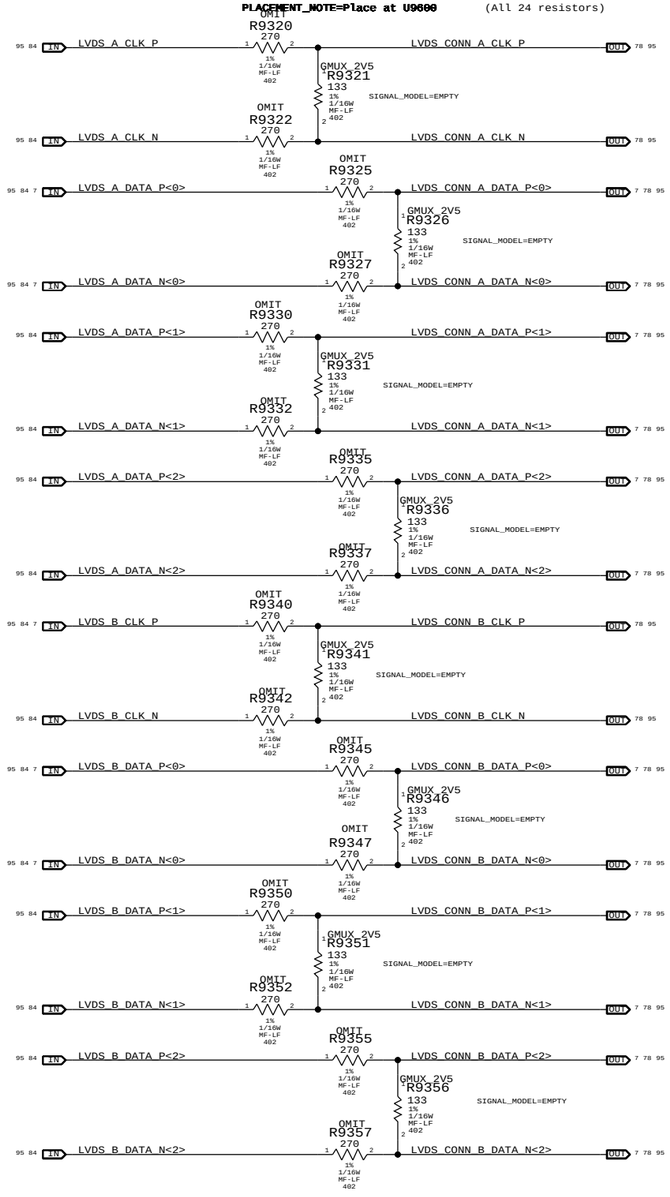
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	80	98

LVDS Transmitter Termination

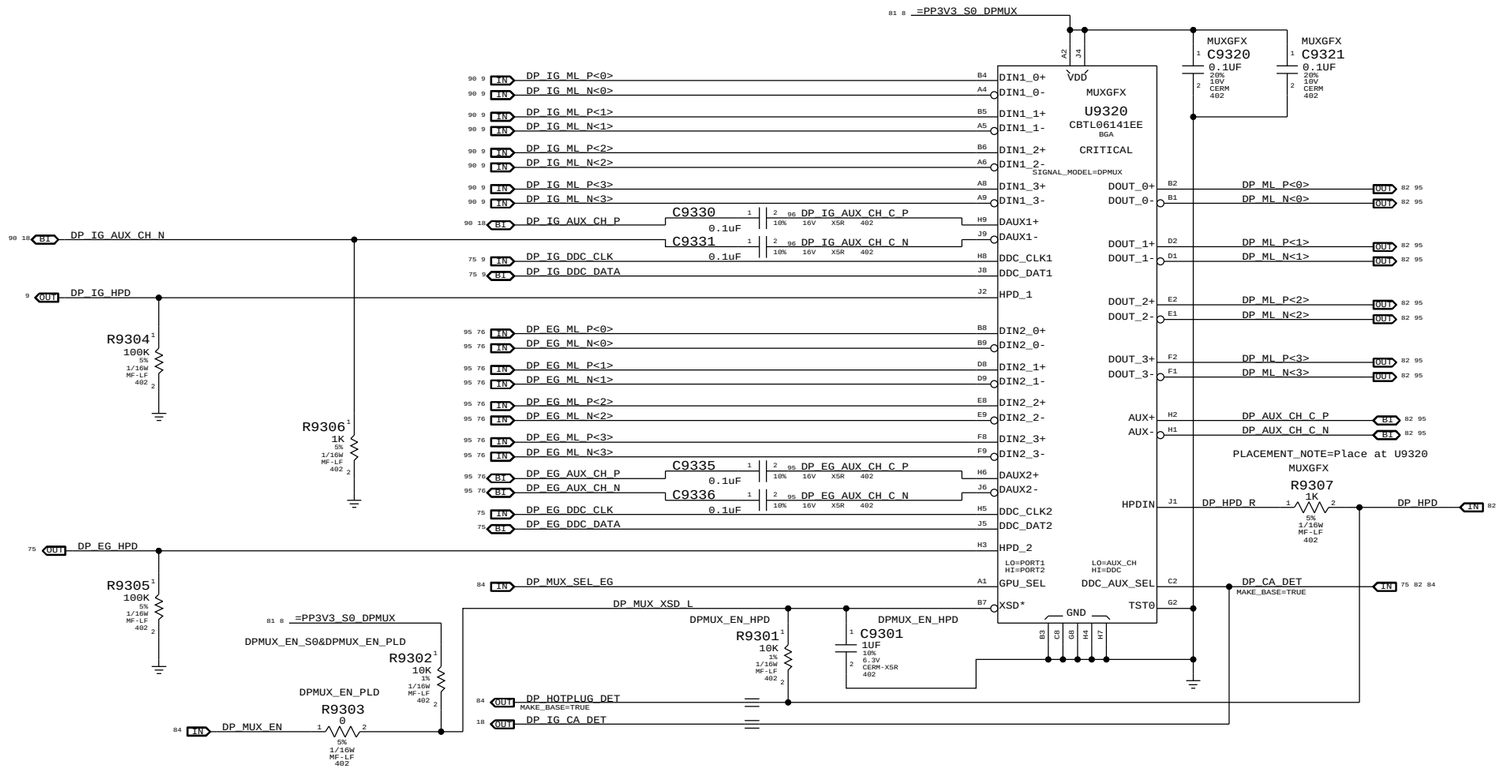
All emulated LVDS outputs require this termination

PLACEMENT_NOTE=Place at U9600 (All 24 resistors)

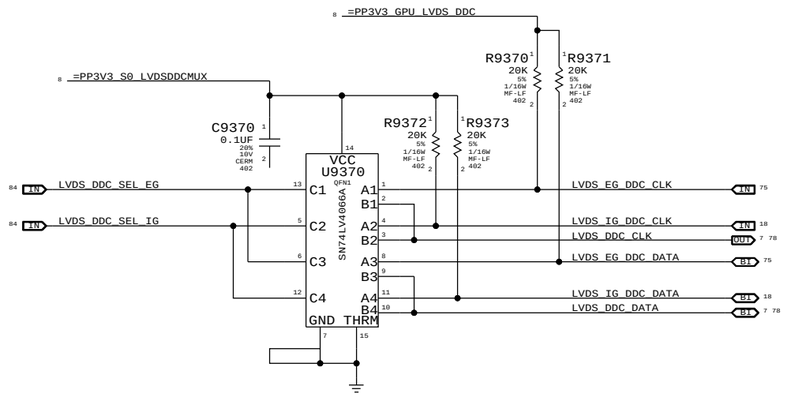


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0517	16	RES,MTL FILM,270 OHM,1%,1/16W,0402,SMD,L			GMUX_2V5
114S0174	16	RES,MTL FILM,1/16W,357 OHM,1,0402,SMD,LF			GMUX_1V8

DisplayPort Mux



LVDS DDC MUX



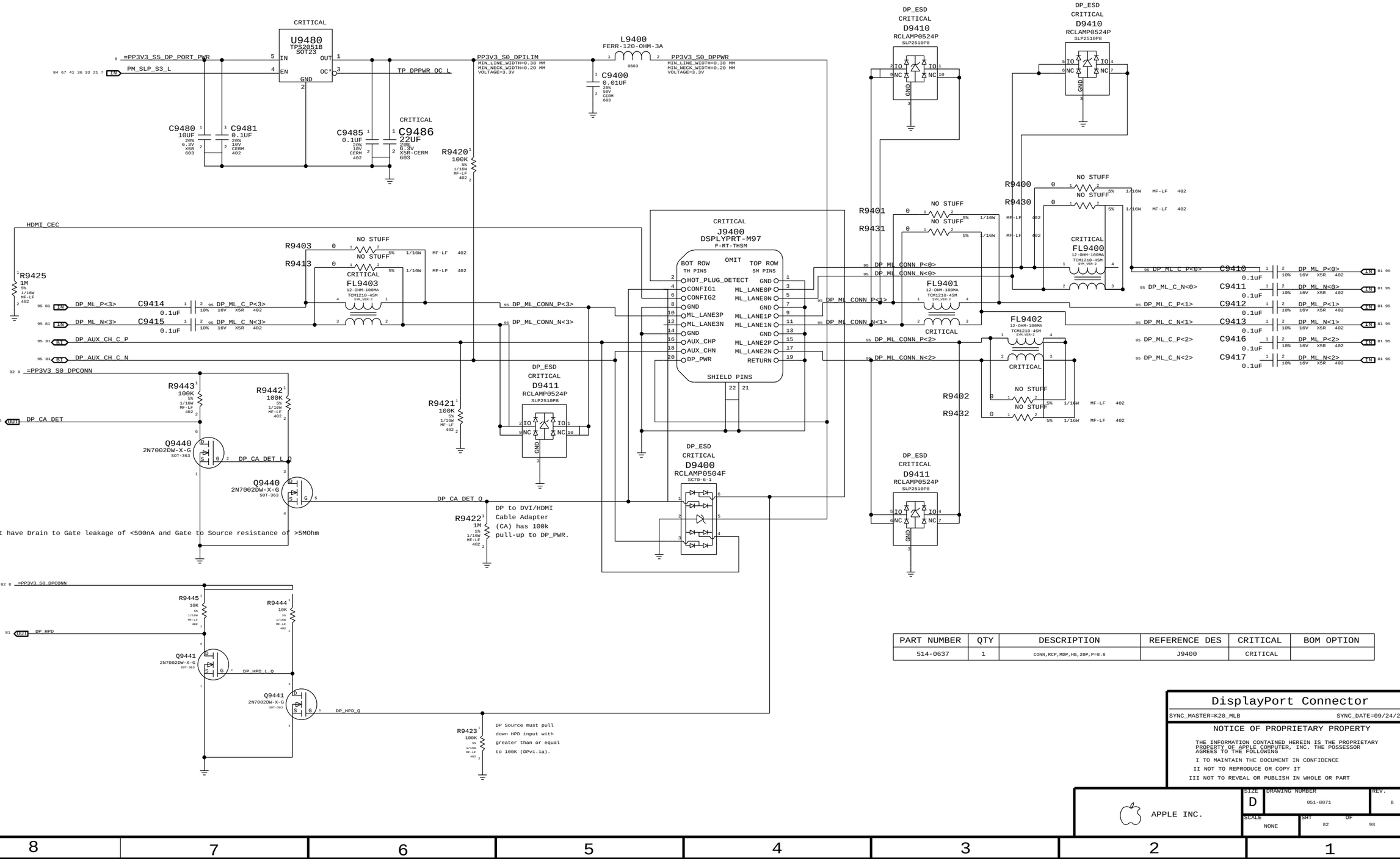
Muxed Graphics Support

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 81 OF 98	

Port Power Switch



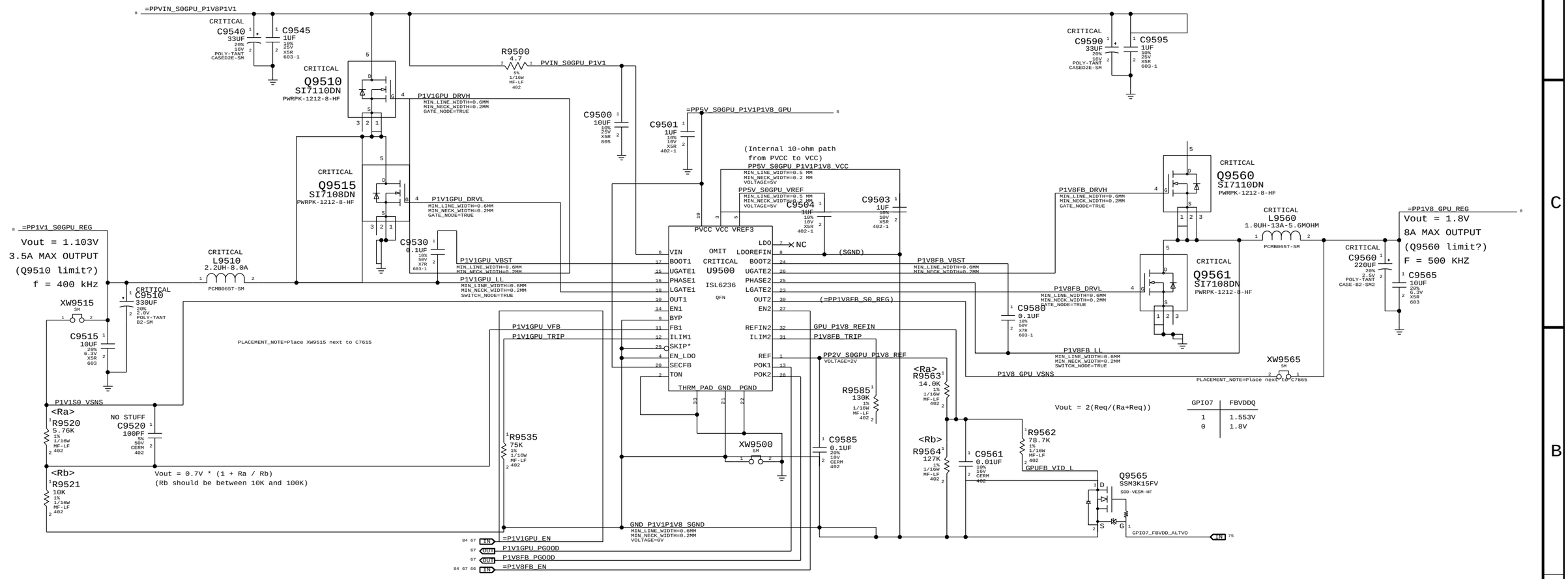
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0637	1	CONN,RCP,MDP,HB,20P,P=0.6	J9400	CRITICAL	

DisplayPort Connector

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 82 OF 98	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2312	1	IC,ISL6236,DUAL PWM CNTRL,QFN32	U9500	CRITICAL	

1.1V / 1V8 FB Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 83 OF 98	

GMUX CPLD

LVDS Receiver Termination

PLACEMENT_NOTE=Place at U9600 (All 14 resistors)

LVDS_IG_A_CLK_P	R9650	100	1% 1/16W MF-LF 402	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA_P<0>	R9651	100	1% 1/16W MF-LF 402	LVDS_IG_A_DATA_N<0>	
LVDS_IG_A_DATA_P<1>	R9652	100	1% 1/16W MF-LF 402	LVDS_IG_A_DATA_N<1>	
LVDS_IG_A_DATA_P<2>	R9653	100	1% 1/16W MF-LF 402	LVDS_IG_A_DATA_N<2>	
LVDS_IG_B_DATA_P<0>	R9654	100	1% 1/16W MF-LF 402	LVDS_IG_B_DATA_N<0>	
LVDS_IG_B_DATA_P<1>	R9655	100	1% 1/16W MF-LF 402	LVDS_IG_B_DATA_N<1>	
LVDS_IG_B_DATA_P<2>	R9656	100	1% 1/16W MF-LF 402	LVDS_IG_B_DATA_N<2>	
LVDS_EG_A_CLK_P	R9660	100	1% 1/16W MF-LF 402	LVDS_EG_A_CLK_N	
LVDS_EG_A_DATA_P<0>	R9661	100	1% 1/16W MF-LF 402	LVDS_EG_A_DATA_N<0>	
LVDS_EG_A_DATA_P<1>	R9662	100	1% 1/16W MF-LF 402	LVDS_EG_A_DATA_N<1>	
LVDS_EG_A_DATA_P<2>	R9663	100	1% 1/16W MF-LF 402	LVDS_EG_A_DATA_N<2>	
LVDS_EG_B_DATA_P<0>	R9664	100	1% 1/16W MF-LF 402	LVDS_EG_B_DATA_N<0>	
LVDS_EG_B_DATA_P<1>	R9665	100	1% 1/16W MF-LF 402	LVDS_EG_B_DATA_N<1>	
LVDS_EG_B_DATA_P<2>	R9666	100	1% 1/16W MF-LF 402	LVDS_EG_B_DATA_N<2>	

SIGNAL_MODEL=EMPTY

Required Pullups

=PP3V3_S0_GMUX

GMUX_DEBUG_RESET_L	R9680	1K	5% 1/16W MF-LF 402
JTAG_GMUX_TCK	R9690	4.7K	5% 1/16W MF-LF 402
EG_CLKREQ_OUT_L	R9695	10K	5% 1/16W MF-LF 402

NO STUFF R9679 10K 1% 1/16W MF-LF 402

PLACEMENT_NOTE=Place on top side at U9600

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K	5% 1/16W MF-LF 402
LVDS_DDC_SEL_IG	R9682	10K	5% 1/16W MF-LF 402
LVDS_DDC_SEL_EG	R9683	10K	5% 1/16W MF-LF 402

NO STUFF

EG_RESET_L	R9691	100K	5% 1/16W MF-LF 402
GMUX_INT	R9692	20K	5% 1/16W MF-LF 402
LCD_BKLT_PWM	R9693	100K	5% 1/16W MF-LF 402
EG_CLKREQ_IN_L	R9694	100K	5% 1/16W MF-LF 402

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

GMUX_JTAG_TCK Inversion

JTAG_GMUX_TCK → Q9670 SSM6N15FEAPE SOT563 → GMUX_JTAG_TCK_L

SILK_PART=GMUX_RST

PM_SLP_S3_L Isolation

PM_SLP_S3_L → Q9670 SSM6N15FEAPE SOT563 → GMUX_PM_SLP_S3_L (MAKE_BASE=TRUE)

EG_PWRSEQ_EN

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

Graphics MUX (GMUX)

SYNC_MASTER=T18_MXMGMUX SYNC_DATE=02/13/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B

SCALE: NONE SHT 84 OF 98

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
336S0027	1	IC,XP2-8,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_BK_BLANK
341S2501	1	IC,CPLD,LATTICE,132CSBGA,REV,K20	U9600	CRITICAL	GMUX_PROG

*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
*BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.

PPBUS_S0_LCDBKLT_PWR
R9730 0 5% 1/10W MF-LF 603
PPVIN_S0_LCDBKLT_BUF
CRITICAL L9701 22UH-2.5A IHLP2525CZ-SM
PPVOUT_S0_LCDBKLT_SW
PLACEMENT_NOTE=L9701 PLACE NEAR Q9701
CRITICAL C9701 10UF 10% 25V X5R 805
PLACEMENT_NOTE=C9701 PLACE NEAR L9701
XW9701 SM
GND_BKL_PWRGND
PLACEMENT_NOTE=XW9701 PLACE NEAR C9701
R9701 49.9 1% 1/16W MF-LF 402
C9702 0.1UF 10% 25V X5R 402
BKL_VIN
BOOST_FET_CNTL
CRITICAL Q9701 SI7308DN PWRPK-1212-8
PLACEMENT_NOTE=D9701 PLACE NEAR Q9701
D9701 SOD-123 RB160M-60G CRITICAL
PLACEMENT_NOTE=C9709 PLACE NEAR C9710
PLACEMENT_NOTE=C9710 PLACE NEAR J9000
CRITICAL NO STUFF C9709 2.2UF 10% 10V X7R 1210
CRITICAL C9710 1.0UF 10% 10V X7R 1210
BOOST_SINK
GND_BKL_PWRGND
PLACEMENT_NOTE=R9715 PLACE NEAR C9709 AND Q9701
R9704 100 1% 1/16W MF-LF 402
R9702 0.4 1% 1/6W MF 402
R9715 0.4 1% 1/6W MF 402
XW9702 SM
GND_BKL_PWRGND_X
PLACEMENT_NOTE=R9702 PLACE NEAR C9709 AND Q9701
*R9702 AND R9715 PIN 1 SHOULD BE PLACED NEAR C9709 PIN 2
C9712 47PF 5% 50V CERM 402 NO STUFF
PPVOUT_S0_LCDBKLT

BKL_VREF_4V9
R9731 187K 1% 1/16W MF-LF 402
PPBUS_S0_LCDBKLT_PWR
BKLT_EN
BKL_SYNC
BKLT_PLL
R9734 0 5% 1/16W MF-LF 402
BKL_VSYNC
R9707 2.67K 1% 1/16W MF-LF 402
C9703 1UF 10% 10V X5R 402
C9713 0.1UF 10% 25V X5R 402
R9705 100K 1% 1/16W MF-LF 402
R9706 10K 5% 1/10W MF-LF 402
PLACEMENT_NOTE=R9707 AWAY FROM Q9701
OMIT CRITICAL
U9700 APP001 QFN
VIN
VREF
ENA
VSYNC
ISET
RT
SSTCMP
DIM
LPF
LRT
DRV
ISWSEN
ISEN1
ISEN2
ISEN3
ISEN4
ISEN5
ISEN6
VSEN
GNDA
THRM_PAD
BKL_ISET
BKL_RT
BKL_SSTCMP
BKL_DIM
BKL_LPF
BKL_LRT
BOOST_SINK_R
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
PLACEMENT_NOTE=R9708 AWAY FROM Q9701
PLACEMENT_NOTE=R9709 AWAY FROM Q9701
R9708 100K 1% 1/16W MF-LF 402
R9709 10K 1% 1/16W MF-LF 402
R9703 5.1M 5% 1/16W MF-LF 402
BKL_SSTCMP_RC
C9705 0.0022UF 10% 50V CERM 402
BKLT_PWM_RC
R9733 4.7K 5% 1/16W MF-LF 402
C9706 0.0022UF 10% 50V CERM 402
C9714 1UF 10% 10V X5R 402
PLACEMENT_NOTE=R9714 AWAY FROM Q9701
BKL_VREF_4V9
R9713 0 5% 1/16W MF-LF 402
PLACEMENT_NOTE=R9713 AWAY FROM Q9701
BKLT_PLL_NOT
BKLT_PLL
R9714 10K 5% 1/16W MF-LF 402
C9707 2.2UF 20% 6.3V CERM 402-LF
BKLT_PLL
BKL_LRT_RC
C9708 0.1UF 10% 25V X5R 402
R9727 75K 1% 1/16W MF-LF 402
PLACEMENT_NOTE=R9727 AWAY FROM Q9701
GND_BKL_PWRGND
THRESHOLD=2.5V
BKL_VSEN
50.4*R9724/(R9723+R9724)=2.4V
R9723 1.2M 1% 1/10W MF-LF 603
R9724 60.4K 1% 1/16W MF-LF 402
PPVOUT_S0_LCDBKLT
R9717 10.2 0.1% 1/16W TF 402
LED_RETURN_6
R9718 10.2 0.1% 1/16W TF 402
LED_RETURN_5
R9719 10.2 0.1% 1/16W TF 402
LED_RETURN_4
R9720 10.2 0.1% 1/16W TF 402
LED_RETURN_3
R9721 10.2 0.1% 1/16W TF 402
LED_RETURN_2
R9722 10.2 0.1% 1/16W TF 402
LED_RETURN_1

CRITICAL Q9702 NTUD3127CXXG SOT-963 P-CHN
BKL_VREF_4V9
BKL_VREF_IN_4V9
R9700 10K 1% 1/16W MF-LF 402
BKL_PWR_EN
R9710 4.02K 1% 1/16W MF-LF 402
CRITICAL Q9702 NTUD3127CXXG SOT-963 N-CHN
LCD_BKLT_PWM
R9711 8.06K 1% 1/16W MF-LF 402

*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

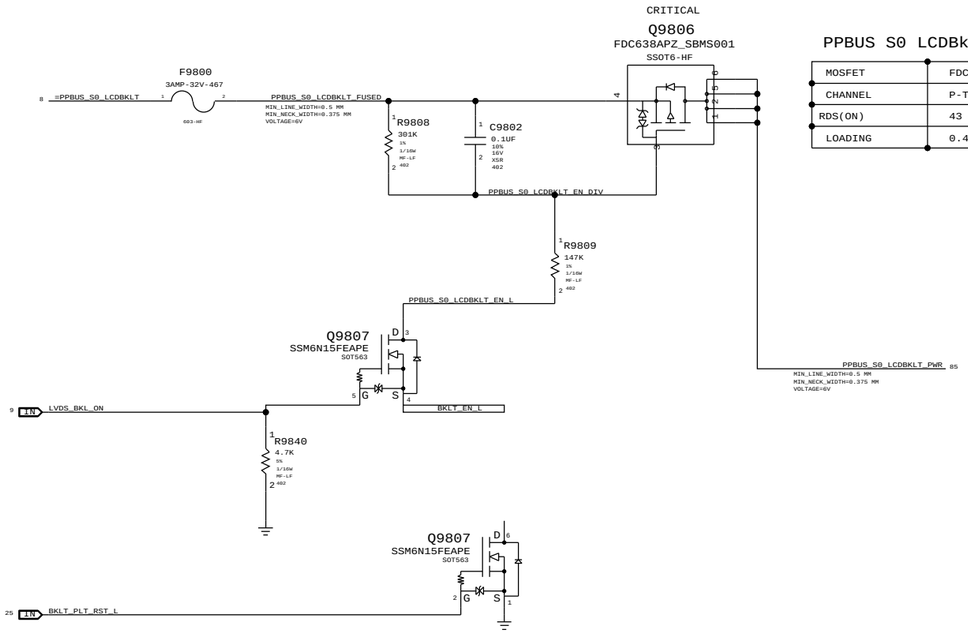
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2413	1	IC,APP001A,WHT LED BKLGHT CTR,SCRN,QFN20	U9700	CRITICAL	

LCD BACKLIGHT DRIVER

SYNC_MASTER=KIRAN_K20
SYNC_DATE=03/19/2009

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 85 OF 98	



PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

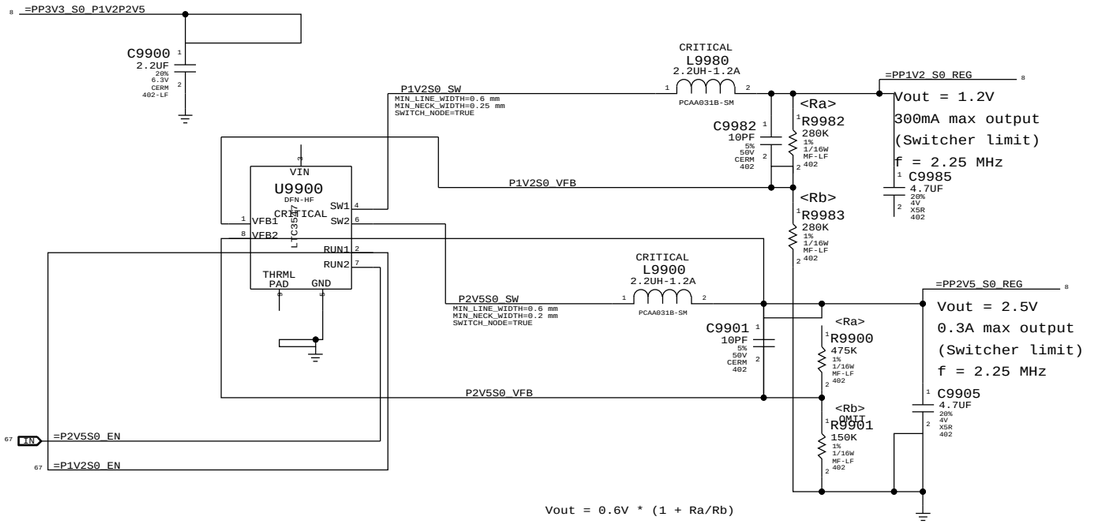
LCD Backlight Support

SYNC_MASTER=YLEE_K20 SYNC_DATE=07/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	86	98

GMUX 1.8V/1.2V S0 Switcher



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0428	1	RES,MTL FILM,1/16W,150K,1,0402,SMD,LF	R9901		GMUX_2V5
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R9901		GMUX_1V8

Misc Power Supplies

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	87	98

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9 10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9 10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 42 61
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 14 42
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 10 14 61
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 61
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	61
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 26
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	6 10
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	9 11
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	9 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	61

CPU/FSB Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE: NONE SHT 88 OF 98

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 27
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

Memory Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 89 OF 98	

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	PCIE_90D	PCIE	PEG_R2D_P<15..0> 69
	PCIE_90D	PCIE	PEG_R2D_N<15..0> 69
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0> 9 69
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0> 9 69
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0> 9 69
	PCIE_90D	PCIE	PEG_D2R_N<15..0> 9 69
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0> 69
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0> 69
	PCIE_90D	PCIE	PCIE_MINI_R2D_P 7 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_N 7 30
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P 17 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N 17 30
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P 7 17 30
	PCIE_90D	PCIE	PCIE_MINI_D2R_N 7 17 30
	PCIE_90D	PCIE	PCIE_FW_R2D_P 35
	PCIE_90D	PCIE	PCIE_FW_R2D_N 35
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P 17 35
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N 17 35
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P 17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_N 17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P 35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N 35
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P 7 31
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N 7 31
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P 17 31
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N 17 31
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P 7 17 31
	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N 7 17 31
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P 17 69
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N 17 69
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P 17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N 17 30
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P 17 35
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N 17 35
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P 17 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N 17 31
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP 17
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR 18 24
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y 18 24
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB 18 24
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC 18 24
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC 18 24
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET 18 24
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF 18 24
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0> 9 81
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0> 9 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P 18 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N 18 81
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET 18 24
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE 18 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P 18 84
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N 18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0> 18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0> 18 84
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3> 9 18
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3> 9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P 9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N 9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0> 18 84
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0> 18 84
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3> 9 18
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3> 9 18
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET 18 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE 18 24
SATA_HDD_R2D	SATA_100D	SATA	SATA_HDD_R2D_C_P 20 38
	SATA_100D	SATA	SATA_HDD_R2D_C_N 20 38
	SATA_100D	SATA	SATA_HDD_R2D_P 7 38
	SATA_100D	SATA	SATA_HDD_R2D_N 7 38
SATA_HDD_D2R	SATA_100D	SATA	SATA_HDD_D2R_P 20 38
	SATA_100D	SATA	SATA_HDD_D2R_N 20 38
	SATA_100D	SATA	SATA_HDD_D2R_C_P 7 38
	SATA_100D	SATA	SATA_HDD_D2R_C_N 7 38
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P 20 38
	SATA_100D	SATA	SATA_ODD_R2D_C_N 20 38
	SATA_100D	SATA	SATA_ODD_R2D_P 7 38
	SATA_100D	SATA	SATA_ODD_R2D_N 7 38
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P 20 38
	SATA_100D	SATA	SATA_ODD_D2R_N 20 38
	SATA_100D	SATA	SATA_ODD_D2R_C_P 7 38
	SATA_100D	SATA	SATA_ODD_D2R_C_N 7 38
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP 20

MCP Constraints 1

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 90 OF 98	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0> 13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>
PCI_AD24	PCI_55S	PCI	PCI_AD<24>
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>
PCI_AD	PCI_55S	PCI	PCI_PAR
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L 19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L 19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R 19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP 19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0> 7 19 41 43 84
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L 7 19 41 43 84
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L 19 25 84
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R 19 25
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC 25 41
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS 7 25 43
USB_EXTA	USB_90D	USB	USB_EXTA_P 20 39
	USB_90D	USB	USB_EXTA_N 20 39
	USB_90D	USB	USB_EXTA_MUXED_P
	USB_90D	USB	USB_EXTA_MUXED_N
USB_MINI	USB_90D	USB	USB_MINI_P 9 20
	USB_90D	USB	USB_MINI_N 9 20
USB_EXTD	USB_90D	USB	USB_EXTD_P 9 20
	USB_90D	USB	USB_EXTD_N 9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 20 30
	USB_90D	USB	USB_CAMERA_N 20 30
USB_BT	USB_90D	USB	USB_BT_P 20 30
	USB_90D	USB	USB_BT_N 20 30
USB_TPAD	USB_90D	USB	USB_TPAD_P 20 49
	USB_90D	USB	USB_TPAD_N 20 49
USB_IR	USB_90D	USB	USB_IR_P 20 40
	USB_90D	USB	USB_IR_N 20 40
USB_EXTB	USB_90D	USB	USB_EXTB_P 20 39
	USB_90D	USB	USB_EXTB_N 20 39
USB_EXCARD	USB_90D	USB	USB_EXCARD_P 20 31
	USB_90D	USB	USB_EXCARD_N 20 31
USB_EXTC	USB_90D	USB	USB_EXTC_P 20 96 98
	USB_90D	USB	USB_EXTC_N 20 96 98
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK 7 13 21 44
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA 7 13 21 44
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK 21 44
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA 21 44
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 9 21
	HDA_55S	HDA	HDA_BIT_CLK_R 21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 21 53
	HDA_55S	HDA	HDA_SYNC_R 21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L 21
	HDA_55S	HDA	HDA_RST_L 21 53
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 21 53
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 21 53
	HDA_55S	HDA	HDA_SDOUT_R 21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP 21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R 21 25
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK 25 41
SPI_CLK	SPI_55S	SPI	SPI_CLK_R 21 43
	SPI_55S	SPI	SPI_CLK 52
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R 21 43
	SPI_55S	SPI	SPI_MOSI 52
SPI_MISO	SPI_55S	SPI	SPI_MISO 21 43
	SPI_55S	SPI	SPI_MISO_R 52
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L 21 43
	SPI_55S	SPI	SPI_CS0_L

MCP Constraints 2

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 91 OF 98	

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 33
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	32 33
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 32
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 32
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	32
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 32
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 32
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 32
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 32
	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 32
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	32 34
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	32 34

Ethernet Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 92 OF 98	

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	35 37
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	35 37

Port 2 Not Used

FireWire Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B

SCALE	SHT	OF
NONE	93	98

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	7 44
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	7 44
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	44
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	44
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	44
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	44
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	7 44
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	7 44
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	44
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	60
	1TO1_DIFFPAIR		CHGR_CSI_N	60
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	60
	1TO1_DIFFPAIR		CHGR_CSO_N	60

SMC Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B

SCALE	SHT	OF
NONE	94	98

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

From T18 MXM:

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	NET_TYPE			
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	81 84
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	81 84
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	7 81 84
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	7 81 84
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	7 81 84
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	81 84
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	7 81 84
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	7 81 84
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_P	7 78
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_N	7 78
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_P	7 78
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N	7 78
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_P	78 81
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_N	78 81
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_P<2..0>	7 78 81
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_N<2..0>	7 78 81
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_P	78 81
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_N	78 81
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_P<2..0>	7 78 81
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_N<2..0>	7 78 81
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	82
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	82
DP_ML	DP_100D	DISPLAYPORT	**DP_ML_P<3..0>**	81 82
	DP_100D	DISPLAYPORT	**DP_ML_N<3..0>**	81 82
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	82
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	82
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	81 82
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	81 82

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	NET_TYPE			
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	71 72 79
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	71 72 79
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	71 72 79
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L	71 72 79
FB_AB_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_A_CKE	71 72 79
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS0_L	71 72
FB_AB_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST	71 72 79
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>	71 72 79
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>	71 72 79
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>	71 72 79
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>	71 72 79
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>	71 72 79
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>	71 72 79
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>	71 72 79
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>	71 72 79
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>	71 72 79
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>	71 72 79
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>	7 71 72 79
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>	7 71 72 79
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>	7 71 72 79
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>	7 71 72 79
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>	71 72 79
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>	71 72 79
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>	71 72 79
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>	71 72 79
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>	71 72 79
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>	71 72 79
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>	71 72 79
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>	71 72 79
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>	71 72 79
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>	71 72 79
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>	71 72 79
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>	71 72 79
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>	7 71 72 79
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>	7 71 72 79
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>	7 71 72 79
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>	7 71 72 79
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>	71 72 79
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>	71 72 79
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>	71 72 79
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>	71 72 79
FB_AB_CS1	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS1_L	71 79

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	NET_TYPE			
(CK505_DOT96)	CLK_SLOW_555	CLK_SLOW	GPU_CLK27M	75
CK505_CLK27MSS	CLK_SLOW_555	CLK_SLOW	GPU_CLK27M_SS	75
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_P	76 84
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_N	76 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<2..0>	76 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<2..0>	7 76 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<2..0>	76 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<2..0>	76 84
DP_ML	DP_100D	DISPLAYPORT	**DP_EG_ML_P<3..0>**	76 81
DP_ML	DP_100D	DISPLAYPORT	**DP_EG_ML_N<3..0>**	76 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_P	76 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_N	76 81
	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_P	81
	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N	81

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	NET_TYPE			
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	71 73 80
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	71 73 80
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	71 73 80
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>	71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>	7 71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>	7 71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L	71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L	7 71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L	71 73 80
FB_CD_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_B_CKE	71 73 80
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS0_L	7 71 73
FB_CD_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST	71 73 80
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>	71 73 80
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>	71 73 80
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>	71 73 80
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>	71 73 80
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>	71 73 80
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>	71 73 80
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>	71 73 80
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>	71 73 80
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>	71 73 80
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>	71 73 80
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>	7 71 73 80
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>	7 71 73 80
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>	7 71 73 80
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>	7 71 73 80
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>	71 73 80
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>	71 73 80
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>	71 73 80
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>	71 73 80
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>	71 73 80
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>	71 73 80
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>	71 73 80
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>	71 73 80
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>	71 73 80
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>	71 73 80
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>	71 73 80
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>	71 73 80
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>	7 71 73 80
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>	7 71 73 80
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>	7 71 73 80
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>	7 71 73 80
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>	71 73 80
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>	71 73 80
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>	71 73 80
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>	71 73 80
FB_CD_CS1	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS1_L	71 80

GPU (G96) Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 95 OF 98	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

FLASH MEMORY BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FLSH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0>	34
	ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0>	34
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	38
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	38
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	38
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	38
	SATA_100D	SATA	SATA_HDD_D2R_UF_P	38
	SATA_100D	SATA	SATA_HDD_D2R_UF_N	38
	SATA_100D	SATA	SATA_HDD_R2D_UF_P	38
	SATA_100D	SATA	SATA_HDD_R2D_UF_N	38
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCOREISNS_P	46 64
	SENSE_1TO1_55S	SENSE	MCPCOREISNS_N	46 64
CPUTHMSNS_D2_DP	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	47
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	47
CPU_THERMD_DP	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 47
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 47
GPUTHMSNS_D_DP	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	47
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	47
GPU_THERMD_DP	THERM_1TO1_55S	THERM	GPU_TDIODE_P	47 75
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	47 75
MCPTHMSNS_D_DP	THERM_1TO1_55S	THERM	MCPTHMSNS_D_P	7 47
	THERM_1TO1_55S	THERM	MCPTHMSNS_D_N	7 47
MCP_THERMD_DP	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	21 47
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	21 47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_P	46
	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_P	46
	SENSE_1TO1_55S	SENSE	DDRISNS_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_P	46
	SENSE_1TO1_55S	SENSE	GPUISENS_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPU_P	46 65
	SENSE_1TO1_55S	SENSE	1V05CPU_N	46 65
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_P	46
	SENSE_1TO1_55S	SENSE	DDRISNS_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPU_P	46
	SENSE_1TO1_55S	SENSE	P1V8GPU_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	45
	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	45
		GND	GND	
		SB_POWER	PP3V3_S5	7 8
		SB_POWER	PP3V3_S0	7 8 9
		SB_POWER	PP1V5_S0	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_P	
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P	46
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N	46
ASIC_CNTRLMEM1	FLSH_55S		NF_CLE_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_ALE_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_CE0_L_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_CE1_L_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_RE0_L_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_WE0_L_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CLE_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_ALE_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CE0_L_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CE1_L_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_RE0_L_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_WE0_L_R	96
ASIC_CNTRLMEM3	FLSH_55S		NF_CLE	96
ASIC_CNTRLMEM3	FLSH_55S		NF_ALE	96
ASIC_CNTRLMEM3	FLSH_55S		NF_CE0_L	96
ASIC_CNTRLMEM3	FLSH_55S		NF_CE1_L	96
ASIC_CNTRLMEM3	FLSH_55S		NF_RE0_L	96
ASIC_CNTRLMEM3	FLSH_55S		NF_WE0_L	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CLE	96
ASIC_CNTRLMEM2	FLSH_55S		NF_ALE	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CE0_L	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CE1_L	96
ASIC_CNTRLMEM2	FLSH_55S		NF_RE0_L	96
ASIC_CNTRLMEM2	FLSH_55S		NF_WE0_L	96

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7 30
	1TO1_DIFFPAIR		CHGR_CSI_R_P	60
	1TO1_DIFFPAIR		CHGR_CSI_R_N	60
	1TO1_DIFFPAIR		CHGR_CSO_R_P	45 60
	1TO1_DIFFPAIR		CHGR_CSO_R_N	45 60
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	39
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	39
(USB_EXTA)	USB_90D	USB	USB2_LT1_P	7 39
(USB_EXTA)	USB_90D	USB	USB2_LT1_N	7 39
(USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_P	
(USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_N	
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P	7 30
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N	7 30
	USB_90D	USB	CONN_USB2_BT_P	7 30
	USB_90D	USB	CONN_USB2_BT_N	7 30
	USB_90D	USB	USB_LT2_P	7 39
	USB_90D	USB	USB_LT2_N	7 39
	USB_90D	USB	USB2_EXCARD_CONN_P	7 31
	USB_90D	USB	USB2_EXCARD_CONN_N	7 31
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_P	81
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_N	81
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P	
	PCIE_90D	PCIE	PCIE_FC_R2D_C_N	
PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P	
	PCIE_90D	PCIE	PCIE_FC_D2R_N	
	PCIE_90D	PCIE	PCIE_FC_R2D_P	
	PCIE_90D	PCIE	PCIE_FC_R2D_N	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	7 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	7 31
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_N	7 56 57
	USB_90D	USB	USB_EXTC_P	20 91 98
	USB_90D	USB	USB_EXTC_N	20 91 98
	USB_90D	USB	USB_LT3_P	7 98
	USB_90D	USB	USB_LT3_N	7 98

Project Specific Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 96 OF 98	

M99 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE:From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

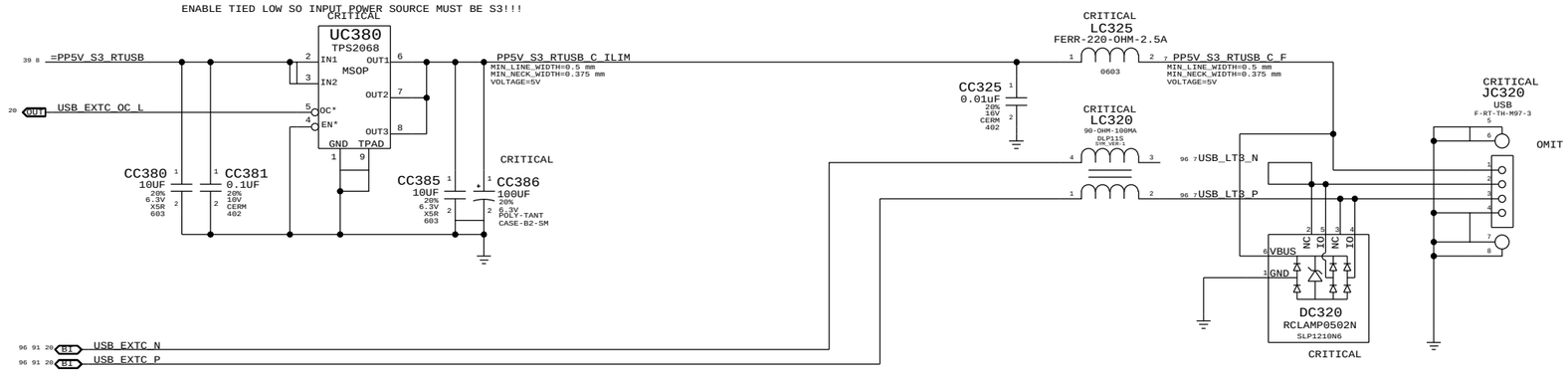
PCB Rule Definitions

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 97 OF 98	

Port Power Switch



LEFT USB PORT C

PLACE LC320 AND LC325 AT CONNECTOR PIN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	1	CONN,RCPT,USB,HB,4P	JC320	CRITICAL	

PROJECT SPECIFIC CONNS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 98 OF 98	