EL2 Block Diagram

VCC_CORE

VCC1.5

VCCP

1.8VSUS
VCC1.8

3VPCU
RVCC3
3VSUS
VCC3
5VPCU
RVCC5
5VSUS
VCC5
SMDDR_VTERM
SMDDR_VREF

Intel
PENRYN
uFCPGA
Page 3,4

CLOCK GENERATOR
CK505
ICS9LPR363
Page 2

FSB(667/800MHZ)

LCD PANEL
Page 19

LVDS

NB
CANTIGA
Page 5,7,8,9,10,11

PCI-E 16X Lan

VGA CONNECTOR
Page 20

LCD/LED

667/ 800 MHZ DDR II

DDRII-SODIMM1
DDRII-SODIMM2
Page 16, 17

SATA

SATA - HDD
Page 26

SATA

SATA - ODD
Page 26

DMI(x2/x4)

PCI-Express

PCIE-6

MINI CARD-1
WLAN
Page 24

PCIE-3

MINI CARD-2
UMA TV
Page 24

PCIE-5

LAN
RTL8111DL
Page 23

USB 2.0

SB
ICH9M
Page 12, 13, 14, 15

PCI-Express

Azalia

WLAN
Page 24

TV
Page 24

Bluetooth
Page 18

M/B USB2 X4
Page 27

Side USB X2
Page 27

Camera/ MIC
Page 29

Touch Screen
Page 23

Card Reader JMB385

6 IN 1

IO Board

LPC

32.768KHz

ITE8512
Page 28

AUDIO CODEC
ALC268
Page 21

Port-A

HP

Port-B

MIC JACK

FAN
Page 3

Key
Board
Page 29

FLASH
ROM
Page 28

CIR
Page 25

SPK AMP
Page 36

INT SPK

Daughter Board

Power
Board

IO Board

VGA
Board

PROJECT : EL2
Quanta Computer Inc.

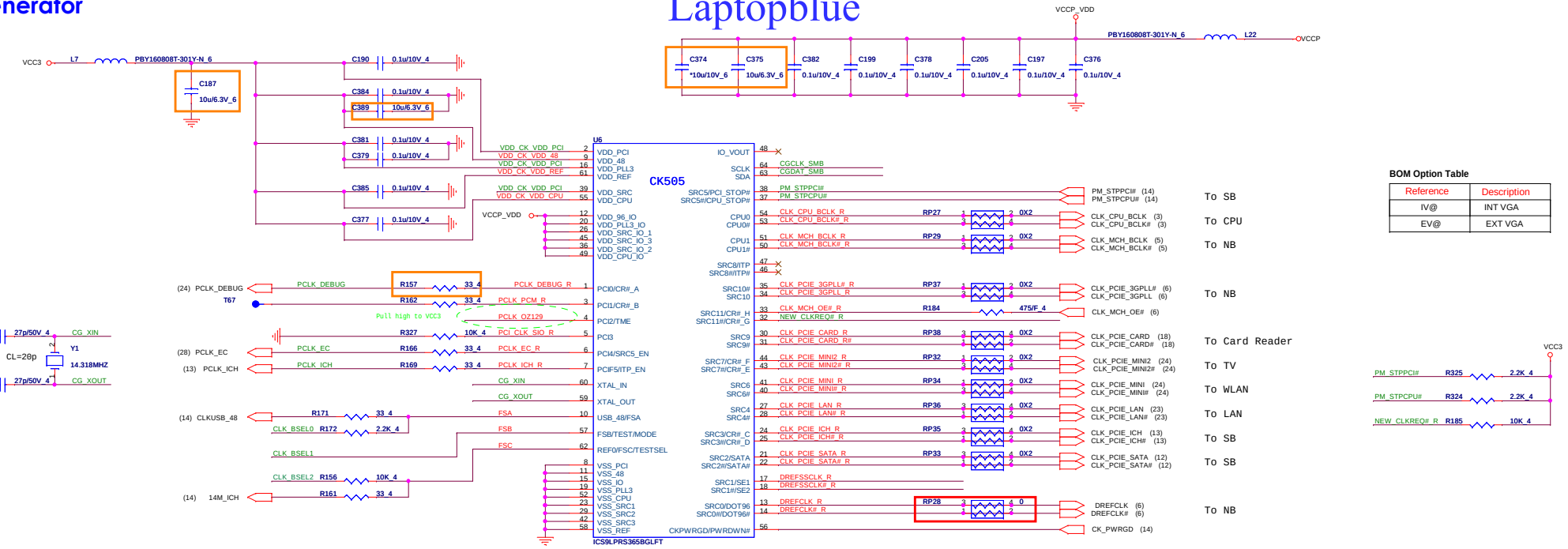
Size	Document Number	Rev
	Block Diagram	1A

Date: Thursday, August 13, 2009 Sheet 1 of 40

Clock Generator

Laptopblue

02

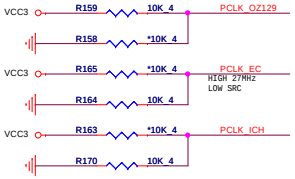


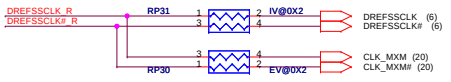
BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

	ICS9LPRS365 (ALPRS365K13)	RTM875T-608 (AL000875K06)	PULL HIGH	PULL DOWN
Pin 4	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37738 IS PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 7	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)

<MAIN>:ICS9LPRS365BGLFT QCI:ALPRS365K13
<SECOND>:SLG8SP512TTR: QCI:AL8SP512K05

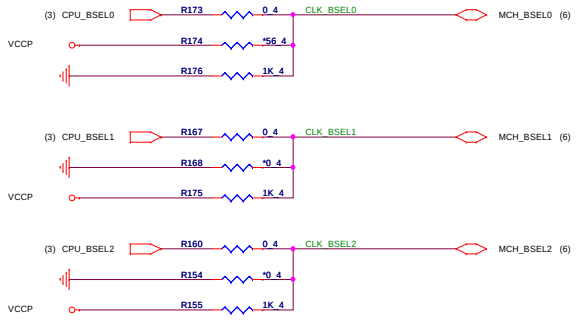




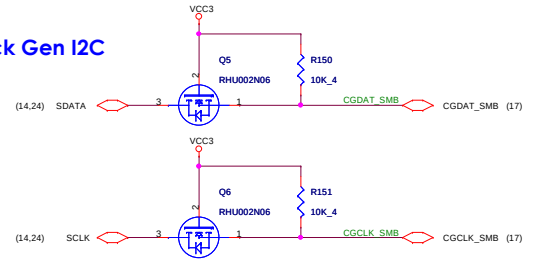
FREQ. SEL TABLE

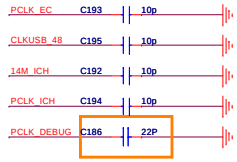
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Clock Gen I2C





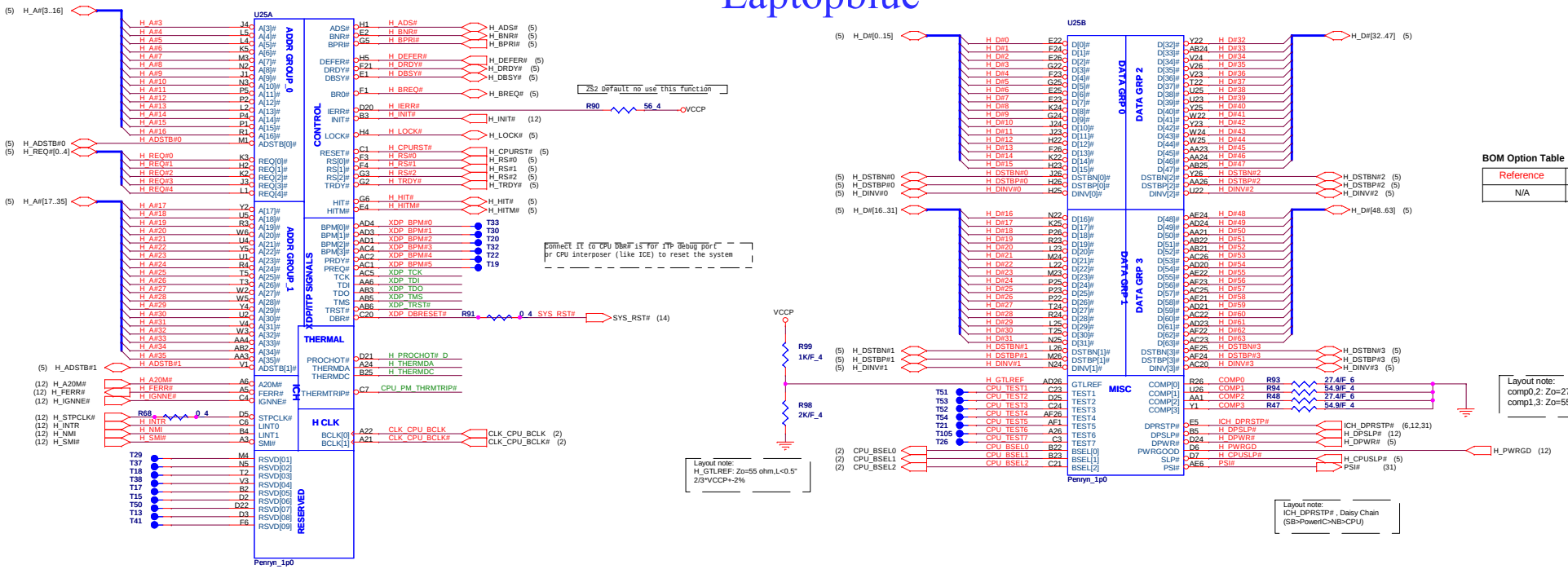
PROJECT : EL2
Quanta Computer Inc.

Size	Document Number	Rev
	CLK GEN	1A

Date: Thursday, August 13, 2009 Sheet 2 of 40

Laptopblue

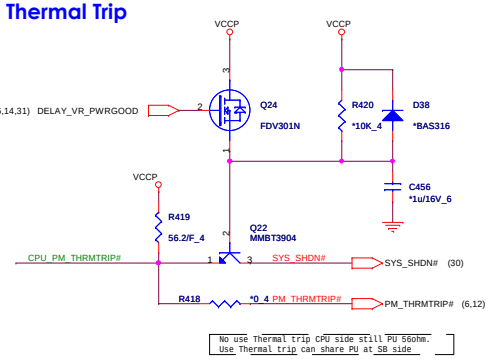
03



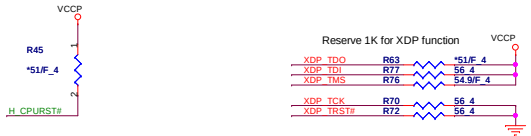
BOM Option Table

Reference	Description
N/A	N/A

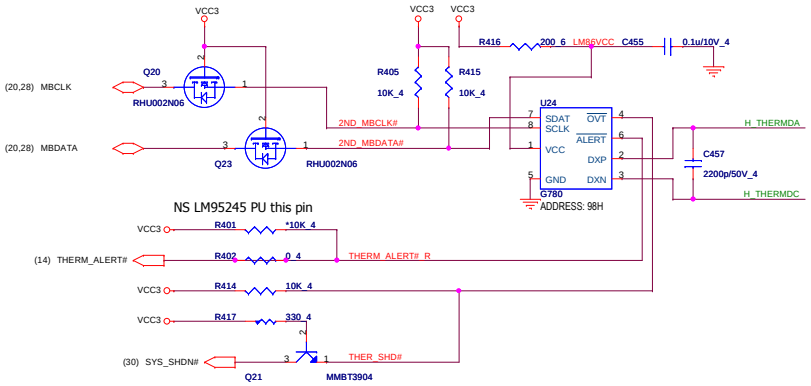
Thermal Trip



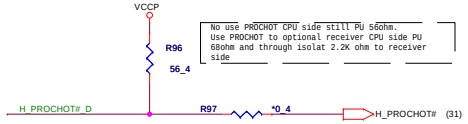
XDP



CPU Thermal monitor



Processor hot



PROJECT : EL2

Quanta Computer Inc.

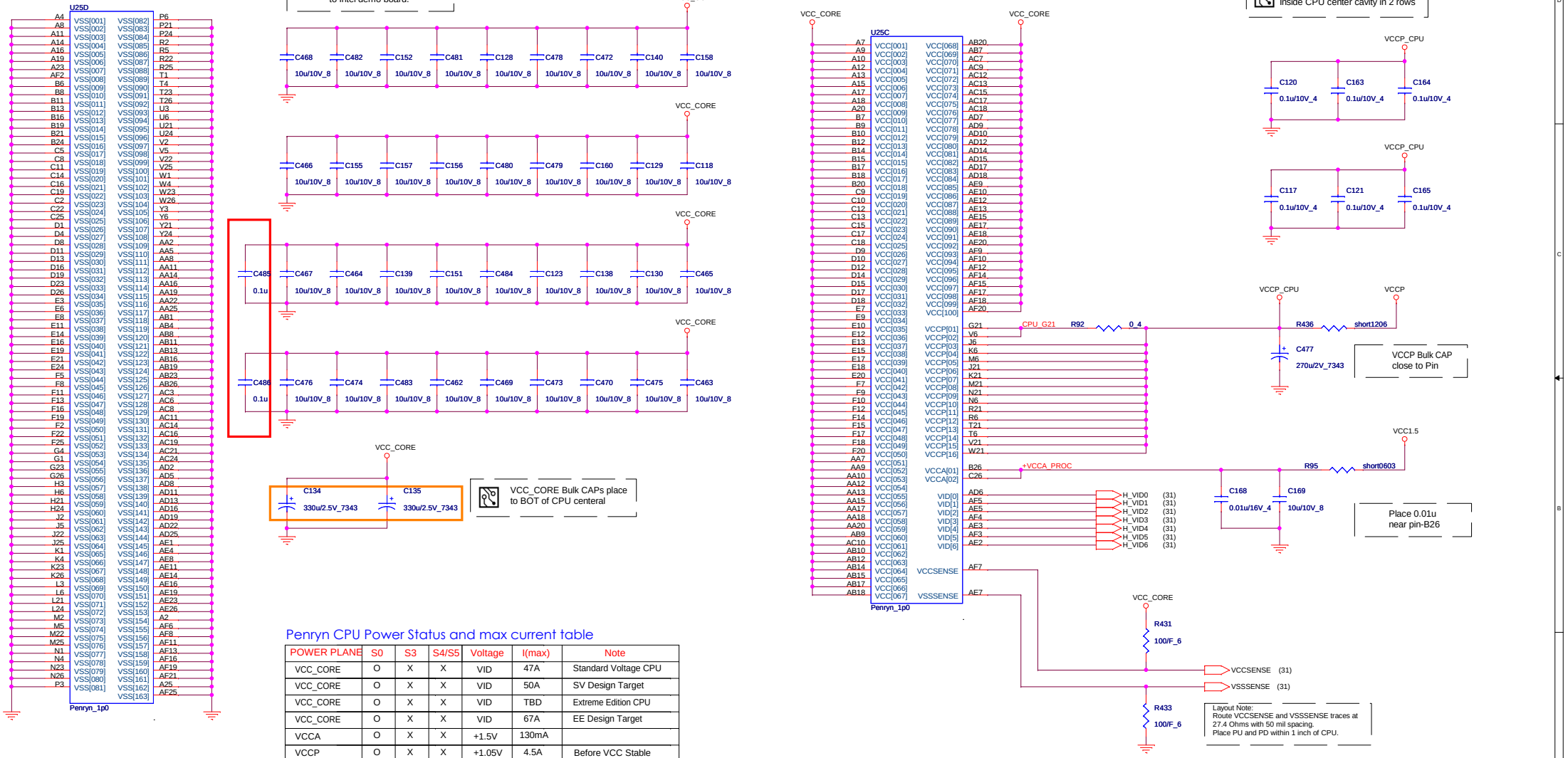
Size	Document Number	Rev
	CPU(1/2) HOST BUS	1A
Date: Thursday, August 13, 2009	Sheet 3 of 40	

Laptopblue

BOM Option Table

Reference	Description
N/A	N/A

Need NC 20PCS 10u before A1 BOM released(A0 all stuff)



Penryn CPU Power Status and max current table

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	47A	Standard Voltage CPU
VCC_CORE	O	X	X	VID	50A	SV Design Target
VCC_CORE	O	X	X	VID	TBD	Extreme Edition CPU
VCC_CORE	O	X	X	VID	67A	EE Design Target
VCCA	O	X	X	+1.5V	130mA	
VCCP	O	X	X	+1.05V	4.5A	Before VCC Stable
VCCP	O	X	X	+1.05V	2.5A	After VCC Stable

(See Penryn EMTS Rev:1.0 Table7,8 for voltage and current)

(See Penryn EMTS Rev:1.0 Table-3 for VID table)

PROJECT : EL2

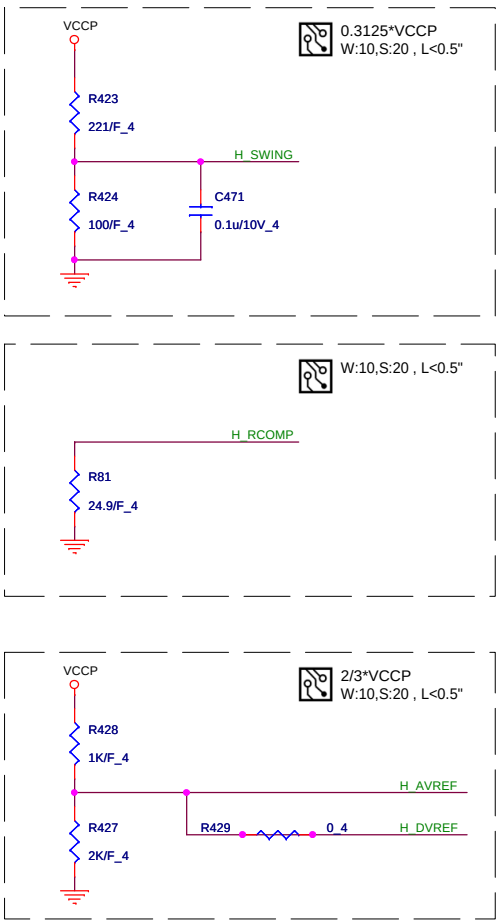
Quanta Computer Inc.

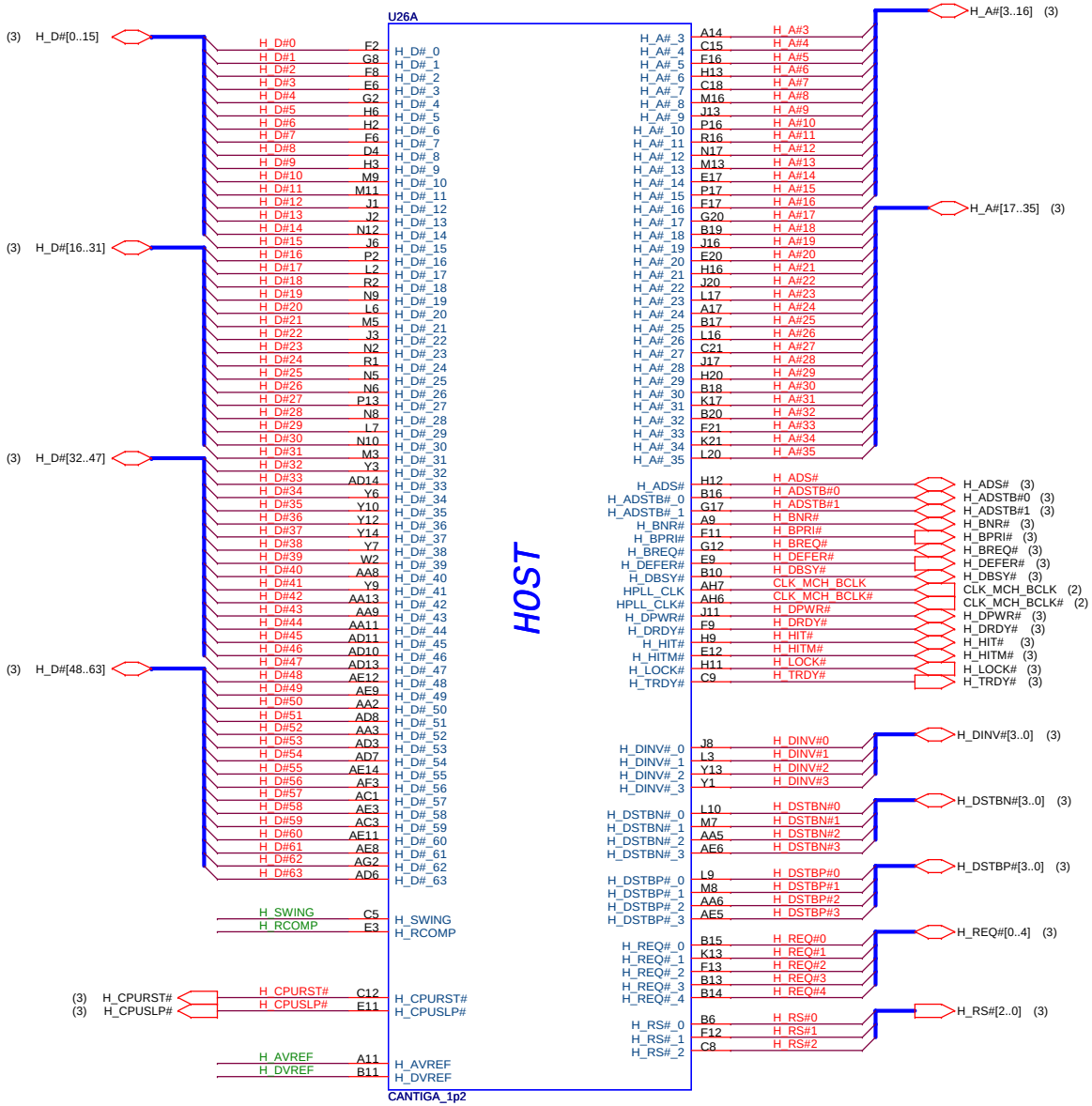
Size	Document Number	Rev
	CPU(2/2) POWER	1A

Date: Thursday, August 13, 2009 Sheet 4 of 40

Laptopblue

05





BOM Option Table

Reference	Description
N/A	N/A

PROJECT : EL2

Quanta Computer Inc.

Size	Document Number	Rev
	NB (1/7) HOST	1A
Date: Thursday, August 13, 2009	Sheet 5 of 40	

Laptopblue

06

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI
EV_IV@	EV&IV diff. value

U26B

RSVD / CONTROL/COMPENSATION

MCH_RSVD1 M36 RSVD1
MCH_RSVD2 N36 RSVD2
MCH_RSVD3 R33 RSVD3
MCH_RSVD4 T33 RSVD4
MCH_RSVD5 AH9 RSVD5
MCH_RSVD6 AH10 RSVD6
MCH_RSVD7 AH12 RSVD7
MCH_RSVD8 AH13 RSVD8
MCH_RSVD9 K12 RSVD9
MCH_RSVD14 T24 RSVD14
MCH_RSVD15 B31 RSVD15
MCH_RSVD17 M1 RSVD17
MCH_RSVD20 AY21 RSVD20
MCH_RSVD21 B2 RSVD21
MCH_RSVD22 BG23 RSVD22
MCH_RSVD23 BF23 RSVD23
MCH_RSVD24 BH18 RSVD24
MCH_RSVD25 BF18 RSVD25

DDR CLK/ CONTROL/COMPENSATION

SA_CK_0 AP24 M_CLK_DDR0 — M_CLK_DDR0 (17)
SA_CK_1 AT21 M_CLK_DDR1 — M_CLK_DDR1 (17)
SB_CK_0 AV24 M_CLK_DDR3 — M_CLK_DDR3 (17)
SB_CK_1 AU20 M_CLK_DDR4 — M_CLK_DDR4 (17)
SA_CK#_0 AP24 M_CLK_DDR#0 — M_CLK_DDR#0 (17)
SA_CK#_1 AR21 M_CLK_DDR#1 — M_CLK_DDR#1 (17)
SB_CK#_0 AU24 M_CLK_DDR#3 — M_CLK_DDR#3 (17)
SB_CK#_1 AV20 M_CLK_DDR#4 — M_CLK_DDR#4 (17)
SA_CKE_0 BC28 M_CKE0 — M_CKE0 (16,17)
SA_CKE_1 AY28 M_CKE1 — M_CKE1 (16,17)
SB_CKE_0 AY36 M_CKE3 — M_CKE3 (16,17)
SB_CKE_1 BB36 M_CKE4 — M_CKE4 (16,17)
SA_CS#_0 BA17 M_CS#0 — M_CS#0 (16,17)
SA_CS#_1 AY16 M_CS#1 — M_CS#1 (16,17)
SB_CS#_0 AV16 M_CS#2 — M_CS#2 (16,17)
SB_CS#_1 AR13 M_CS#3 — M_CS#3 (16,17)
SA_ODT_0 BD17 M_ODT0 — M_ODT0 (16,17)
SA_ODT_1 AY17 M_ODT1 — M_ODT1 (16,17)
SB_ODT_0 BF15 M_ODT2 — M_ODT2 (16,17)
SB_ODT_1 AY13 M_ODT3 — M_ODT3 (16,17)
SM_RCOMP BG22 M_RCOMP
SM_RCOMP# BH21 M_RCOMP#
SM_RCOMP_VOH BF28 SM_RCOMP_VOH
SM_RCOMP_VOL BH28 SM_RCOMP_VOL
SM_VREF AV42 SM_VREF
SM_PWROK AR36 SM_PWROK
SM_REXT BF17 SM_REXT
SM_DRAMRST# BC36 MCH_SM_DRAMRST# — T7
SM_DRAMRST# only for DDR3 (DDR2 NC)

CLK

DPLL_REF_CLK AB38 DREFCLK — DREFCLK (2)
DPLL_REF_CLK# A38 DREFCLK# — DREFCLK# (2)
DPLL_REF_SSCLK E41 DREFSSCLK — DREFSSCLK (2)
DPLL_REF_SSCLK# F41 DREFSSCLK# — DREFSSCLK# (2)
PEG_CLK F43 CLK_PCIE_3GPLL — CLK_PCIE_3GPLL (2)
PEG_CLK# E43 CLK_PCIE_3GPLL# — CLK_PCIE_3GPLL# (2)

JTAG

ME_JTAG_TCK AL34
JTAG_TDI T6 — ME_JTAG_TDI AK34
ME_JTAG_TDO AN35
JTAG_TMS T3 — ME_JTAG_TMS AM35

DMI

DMI_RXN_0 AE41 DMI_TXN0
DMI_RXN_1 AE37 DMI_TXN1
DMI_RXN_2 AE47 DMI_TXN2
DMI_RXN_3 AH39 DMI_TXN3 — DMI_TXN[3:0] (13)
DMI_RXP_0 AE40 DMI_TXP0
DMI_RXP_1 AE38 DMI_TXP1
DMI_RXP_2 AE48 DMI_TXP2
DMI_RXP_3 AH40 DMI_TXP3 — DMI_TXP[3:0] (13)
DMI_TXN_0 AE35 DMI_RXN0
DMI_TXN_1 AE43 DMI_RXN1
DMI_TXN_2 AE46 DMI_RXN2
DMI_TXN_3 AH42 DMI_RXN3 — DMI_RXN[3:0] (13)
DMI_TXP_0 AD35 DMI_RXP0
DMI_TXP_1 AE44 DMI_RXP1
DMI_TXP_2 AF46 DMI_RXP2
DMI_TXP_3 AH43 DMI_RXP3 — DMI_RXP[3:0] (13)

CFG

(2) MCH_BSEL0 T25 CFG_0
(2) MCH_BSEL1 R25 CFG_1
(2) MCH_BSEL2 P25 CFG_2
MCH_CFG_3 P20 CFG_3
T40 MCH_CFG_4 P24 CFG_4
T23 (11) MCH_CFG_5 C25 CFG_5
(11) MCH_CFG_6 N24 CFG_6
(11) MCH_CFG_7 M24 CFG_7
MCH_CFG_8 E21 CFG_8
T25 (11) MCH_CFG_9 C23 CFG_9
(11) MCH_CFG_10 C24 CFG_10
MCH_CFG_11 N21 CFG_11
T36 (11) MCH_CFG_12 P21 CFG_12
(11) MCH_CFG_13 T21 CFG_13
MCH_CFG_14 R20 CFG_14
T34 MCH_CFG_15 M20 CFG_15
T39 (11) MCH_CFG_16 L21 CFG_16
MCH_CFG_17 H21 CFG_17
T24 MCH_CFG_18 P29 CFG_18
T14 (11) MCH_CFG_19 R28 CFG_19
(11) MCH_CFG_20 T28 CFG_20

GRAPHICS VID

GFX_VID_0 B33 T128
GFX_VID_1 B32 T126
GFX_VID_2 G33 T11
GFX_VID_3 F33 T10
GFX_VID_4 E33 11
GFX_VR_EN C34 T8

PM

(14) PM_SYNC# R61 0_4 PM_SYNC# R R29
(3,12,31) ICH_DPRSTP# R425 0_4 ICH_DPRSTP# R B7
PM_EXTTS#0 R24 0_4 PM_EXTTS#0_1_EC_R N33
(17) PM_EXTTS#1 R39 0_4 TSRDIMM0_1_R F32
(3,14,31) DELAY_VR_PWRGOOD R18 0_4 AT40
(13,20) PLT_RST#_NB R67 100_4 RST_IN# MCH AT11
(3,12) PM_THRMTRIP# R73 *0_4 THRMTRIP# R T20
(14,31) PM_DPRSLPVR R41 0_4 DPRSLPVR_R R32

PM_SYNC#
PM_DPRSTP#
PM_EXT_TS#_0
PM_EXT_TS#_1
PWROK
RSTIN#
THERMTRIP#
DPRSLPVR

NB Thermal trip pin
No use Thermal trip NB side can NC.(NB has ODT)

PM_DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP , then to (G)MCH and CPU, in that order.

ME

CL_CLK AH37 CL_CLK0 — CL_CLK0 (14)
CL_DATA AH36 CL_DATA0 — CL_DATA0 (14)
CL_PWROK AN36 MPWROK — MPWROK (14,28)
CL_RST# AJ35 CL_RST#0 — CL_RST#0 (14)
CL_VREF AH34 MCH_CLVREF_R

MISC

DDPC_CTRLCLK N28 DDPC_CTRLCLK — T16
DDPC_CTRLDATA M28 DDPC_CTRLDATA — DDPC_CTRLDATA (11)
SDVO_CTRLCLK G36 SDVO_CTRLCLK — T5
SDVO_CTRLDATA E36 SDVO_CTRLDATA — SDVO_CTRLDATA (11)
CLKREQ# K36 CLK_MCH_OE# — CLK_MCH_OE# (2)
ICH_SYNC# H36 MCH_ICH_SYNC# — MCH_ICH_SYNC# (14)
TSATN# B12 TSATN#

DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

HDA

HDA_BCLK B28 T122
HDA_RST# B30 T125
HDA_SDI B29 T123
HDA_SDO C29 T124
HDA_SYNC A28 T121

NC

TP_MCH_NC1 T135 NC_1
TP_MCH_NC2 T136 NC_2
TP_MCH_NC3 T139 NC_3
TP_MCH_NC4 T140 NC_4
TP_MCH_NC5 T132 NC_5
TP_MCH_NC6 T137 NC_6
TP_MCH_NC7 T138 NC_7
TP_MCH_NC8 T134 NC_8
TP_MCH_NC9 T133 NC_9
TP_MCH_NC10 T130 NC_10
TP_MCH_NC11 T131 NC_11
TP_MCH_NC12 T129 NC_12
TP_MCH_NC13 T118 NC_13
TP_MCH_NC14 T117 NC_14
TP_MCH_NC15 T116 NC_15
TP_MCH_NC16 T115 NC_16
TP_MCH_NC17 T112 NC_17
TP_MCH_NC18 T114 NC_18
TP_MCH_NC19 T113 NC_19
TP_MCH_NC20 T111 NC_20
TP_MCH_NC21 T109 NC_21
TP_MCH_NC22 T108 NC_22
TP_MCH_NC23 T107 NC_23
TP_MCH_NC24 T110 NC_24
TP_MCH_NC25 T48 NC_25

CANTIGA_1p2

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

U26C

LVDS I/F

(19) INT_LVDS_PWM — INT_LVDS_PWM L32 — L_BKLT_CTRL
(19) INT_LVDS_BLON — INT_LVDS_BLON G32 — L_BKLT_EN
L_CTRL_CLK M32 — L_CTRL_CLK
L_CTRL_DATA M33 — L_CTRL_DATA
(19) INT_LVDS_EDIDCLK — INT_LVDS_EDIDCLK K33 — L_DDC_CLK
(11,19) INT_LVDS_EDIDDATA — INT_LVDS_EDIDDATA J33 — L_DDC_DATA
(19) INT_LVDS_DIGON — INT_LVDS_DIGON M29 — L_VDD_EN
LVDS_IBG C44 — LVDS_IBG
T1 — LVDS_VBG B43 — LVDS_VBG
LVDS_VREFH E37 — LVDS_VREFH
LVDS_VREFL E38 — LVDS_VREFL
(19) INT_TXLCLKOUT- — INT_TXLCLKOUT- C41 — LVDSA_CLK#
(19) INT_TXLCLKOUT+ — INT_TXLCLKOUT+ C40 — LVDSA_CLK
(19) INT_TXUCLKOUT- — INT_TXUCLKOUT- B37 — LVDSB_CLK#
(19) INT_TXUCLKOUT+ — INT_TXUCLKOUT+ A37 — LVDSB_CLK
(19) INT_TXLOUT0- — INT_TXLOUT0- H47 — LVDSA_DATA#_0
(19) INT_TXLOUT1- — INT_TXLOUT1- E46 — LVDSA_DATA#_1
(19) INT_TXLOUT2- — INT_TXLOUT2- G40 — LVDSA_DATA#_2
(19) INT_TXLOUT3- — INT_TXLOUT3- A40 — LVDSA_DATA#_3
(19) INT_TXLOUT0+ — INT_TXLOUT0+ H48 — LVDSA_DATA_0
(19) INT_TXLOUT1+ — INT_TXLOUT1+ D45 — LVDSA_DATA_1
(19) INT_TXLOUT2+ — INT_TXLOUT2+ F40 — LVDSA_DATA_2
(19) INT_TXLOUT3+ — INT_TXLOUT3+ B40 — LVDSA_DATA_3
(19) INT_TXUOUT0- — INT_TXUOUT0- A41 — LVDSB_DATA#_0
(19) INT_TXUOUT1- — INT_TXUOUT1- H38 — LVDSB_DATA#_1
(19) INT_TXUOUT2- — INT_TXUOUT2- G37 — LVDSB_DATA#_2
(19) INT_TXUOUT3- — INT_TXUOUT3- J37 — LVDSB_DATA#_3
(19) INT_TXUOUT0+ — INT_TXUOUT0+ B42 — LVDSB_DATA_0
(19) INT_TXUOUT1+ — INT_TXUOUT1+ G38 — LVDSB_DATA_1
(19) INT_TXUOUT2+ — INT_TXUOUT2+ F37 — LVDSB_DATA_2
(19) INT_TXUOUT3+ — INT_TXUOUT3+ K37 — LVDSB_DATA_3

LVDS

TV I/F (Disable)

INT_TV_COMP F25 — TVA_DAC
INT_TV_Y/G H25 — TVB_DAC
INT_TV_C/R K25 — TVC_DAC
INT_TV_RNT H24 — TV_RTN
TV_DCONSEL_1 E31
TV_DCONSEL_0 E32
TV_DCONSEL_0
TV_DCONSEL_1

0327 connected TV and CRT signal to GND

CRT I/F (Disable)

INTB E28 — CRT_BLUE
INTG G28 — CRT_GREEN
INTR J28 — CRT_RED
CRT_IRTN G29 — CRT_IRTN
INT_CRT_DDCCLK H32 — CRT_DDC_CLK
INT_CRT_DDCDAT J32 — CRT_DDC_DATA
J29 — CRT_HSYNC
E29 — CRT_TVO_IREF
L29 — CRT_VSYNC
CRTIREF

VGA

PCI-EXPRESS GRAPHICS

L<0.5" , if PCIE not support still connect to +VCC_PEG
+1.05V_VCC_PEG

PEG_COMPI T37 EXP_COMPX R22 49.9/F_4
PEG_COMPO T36

PEG_RX#_0 H44 PEG_RXN0
PEG_RX#_1 J46 PEG_RXN1
PEG_RX#_2 L44 PEG_RXN2
PEG_RX#_3 L40 PEG_RXN3
PEG_RX#_4 N41 PEG_RXN4
PEG_RX#_5 P48 PEG_RXN5
PEG_RX#_6 N44 PEG_RXN6
PEG_RX#_7 T43 PEG_RXN7
PEG_RX#_8 U43 PEG_RXN8
PEG_RX#_9 Y43 PEG_RXN9
PEG_RX#_10 Y48 PEG_RXN10
PEG_RX#_11 Y36 PEG_RXN11
PEG_RX#_12 AA43 PEG_RXN12
PEG_RX#_13 AD37 PEG_RXN13
PEG_RX#_14 AC47 PEG_RXN14
PEG_RX#_15 AD39 PEG_RXN15
PEG_RXN[15:0] (20)

PEG_RX_0 H43 PEG_RXP0
PEG_RX_1 J44 PEG_RXP1
PEG_RX_2 L43 PEG_RXP2
PEG_RX_3 L41 PEG_RXP3
PEG_RX_4 N40 PEG_RXP4
PEG_RX_5 P47 PEG_RXP5
PEG_RX_6 N43 PEG_RXP6
PEG_RX_7 T42 PEG_RXP7
PEG_RX_8 U42 PEG_RXP8
PEG_RX_9 Y42 PEG_RXP9
PEG_RX_10 W47 PEG_RXP10
PEG_RX_11 Y37 PEG_RXP11
PEG_RX_12 AA42 PEG_RXP12
PEG_RX_13 AD36 PEG_RXP13
PEG_RX_14 AC48 PEG_RXP14
PEG_RX_15 AD40 PEG_RXP15
PEG_RXP[15:0] (20)

PEG_TX#_0 J41 C_PEG_TXN0 C32 EV@0.1u/10V_4 PEG_TXN0
PEG_TX#_1 M46 C_PEG_TXN1 C535 EV@0.1u/10V_4 PEG_TXN1
PEG_TX#_2 M47 C_PEG_TXN2 C540 EV@0.1u/10V_4 PEG_TXN2
PEG_TX#_3 M40 C_PEG_TXN3 C27 EV@0.1u/10V_4 PEG_TXN3
PEG_TX#_4 M42 C_PEG_TXN4 C542 EV@0.1u/10V_4 PEG_TXN4
PEG_TX#_5 R48 C_PEG_TXN5 C538 EV@0.1u/10V_4 PEG_TXN5
PEG_TX#_6 N38 C_PEG_TXN6 C36 EV@0.1u/10V_4 PEG_TXN6
PEG_TX#_7 T40 C_PEG_TXN7 C34 EV@0.1u/10V_4 PEG_TXN7
PEG_TX#_8 U37 C_PEG_TXN8 C525 EV@0.1u/10V_4 PEG_TXN8
PEG_TX#_9 U40 C_PEG_TXN9 C41 EV@0.1u/10V_4 PEG_TXN9
PEG_TX#_10 Y40 C_PEG_TXN10 C28 EV@0.1u/10V_4 PEG_TXN10
PEG_TX#_11 AA46 C_PEG_TXN11 C530 EV@0.1u/10V_4 PEG_TXN11
PEG_TX#_12 AA37 C_PEG_TXN12 C39 EV@0.1u/10V_4 PEG_TXN12
PEG_TX#_13 AA40 C_PEG_TXN13 C532 EV@0.1u/10V_4 PEG_TXN13
PEG_TX#_14 AD43 C_PEG_TXN14 C528 EV@0.1u/10V_4 PEG_TXN14
PEG_TX#_15 AC46 C_PEG_TXN15 C527 EV@0.1u/10V_4 PEG_TXN15
PEG_TXN[15:0] (20)

PEG_TX_0 J42 C_PEG_TXP0 C31 EV@0.1u/10V_4 PEG_TXP0
PEG_TX_1 L46 C_PEG_TXP1 C534 EV@0.1u/10V_4 PEG_TXP1
PEG_TX_2 M48 C_PEG_TXP2 C539 EV@0.1u/10V_4 PEG_TXP2
PEG_TX_3 M39 C_PEG_TXP3 C26 EV@0.1u/10V_4 PEG_TXP3
PEG_TX_4 M43 C_PEG_TXP4 C541 EV@0.1u/10V_4 PEG_TXP4
PEG_TX_5 R47 C_PEG_TXP5 C537 EV@0.1u/10V_4 PEG_TXP5
PEG_TX_6 N37 C_PEG_TXP6 C35 EV@0.1u/10V_4 PEG_TXP6
PEG_TX_7 T39 C_PEG_TXP7 C33 EV@0.1u/10V_4 PEG_TXP7
PEG_TX_8 U38 C_PEG_TXP8 C524 EV@0.1u/10V_4 PEG_TXP8
PEG_TX_9 U39 C_PEG_TXP9 C40 EV@0.1u/10V_4 PEG_TXP9
PEG_TX_10 Y39 C_PEG_TXP10 C24 EV@0.1u/10V_4 PEG_TXP10
PEG_TX_11 Y46 C_PEG_TXP11 C529 EV@0.1u/10V_4 PEG_TXP11
PEG_TX_12 AA36 C_PEG_TXP12 C38 EV@0.1u/10V_4 PEG_TXP12
PEG_TX_13 AA39 C_PEG_TXP13 C531 EV@0.1u/10V_4 PEG_TXP13
PEG_TX_14 AD42 C_PEG_TXP14 C533 EV@0.1u/10V_4 PEG_TXP14
PEG_TX_15 AD46 C_PEG_TXP15 C523 EV@0.1u/10V_4 PEG_TXP15
PEG_TXP[15:0] (20)

CANTIGA_1p2

Check list note : CL_REF=0.35V

VCCP
R36 1K/F_4
MCH_CLVREF_R
C86 0.1u/10V_4
R37 511/F_6

SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

R23 0_6 +SMDDR_VREF
SM_VREF
R27 *10K/F_4 +1.8VSUS_GMCH
R29 *10K/F_4

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

VCCP
TSATN# 56_4 R430
VCC3
CLK_MCH_OE# 10K_4 R28
PM_EXTTS#0 10K_4 R35
PM_EXTTS#1 10K_4 R38
SM_REXT R74 499/F_4

IV&EV Dis/Enable LVDS setting(See DG 1.0 P190 Table 103)

R32 IV@0_4 LVDS_VREFH LVDS_VREFL — For IV @ 0ohm For EV@ NC
R21 IV@2.37K/F_4 LVDS_IBG — For IV @ 2.37K/F For EV@ NC
VCC3 R57 IV@10K_4 L_CTRL_CLK
R56 IV@10K_4 L_CTRL_DATA — For IV @ 2.37K 10K For EV@ NC

+1.8VSUS_GMCH
R442 80.6/F_4
M_RCOMP
R441 *20/F_4
+1.8VSUS_GMCH
R439 *20/F_4
M_RCOMP#
R438 80.6/F_4

+1.8VSUS_GMCH R449 1K/F_4
R445 3.01K/F_4
R447 1K/F_4
SM_RCOMP_VOH
C502 0.01u/16V_4
C505 2.2u/6.3V_6
SM_RCOMP_VOL
C498 0.01u/16V_4
C501 2.2u/6.3V_6

SM_PWROK only for DDR3.(DDR2 PD only)

HWPG_1.8V (28,33)
R26 *12K/F_4
SM_PWROK
R31 10K/F_6

IV&EV Dis/Enable PLL setting(See DG 1.0 P190 Table 103)

DREFCLK R455 EV@0_4
DREFCLK# R456 EV@0_4
DREFSSCLK R24 EV@0_4
DREFSSCLK# R25 EV@0_4
For IV @ NC
For EV@ 0ohm to GND

PROJECT : EL2
Quanta Computer Inc.

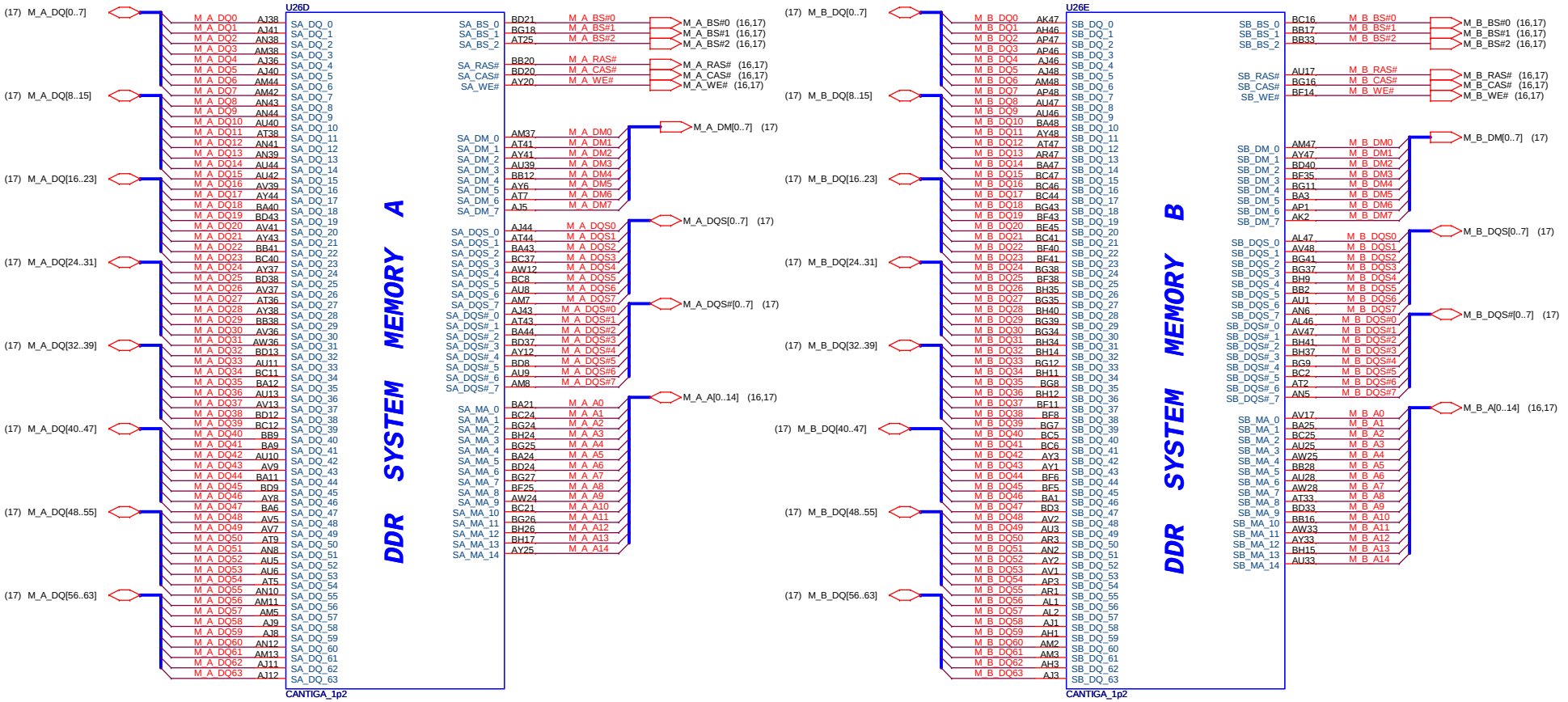
Size	Document Number	Rev
	NB(2/7)	1A
Date: Thursday, August 13, 2009	Sheet 6 of 40	

Laptopblue

BOM Option Table

Reference	Description
N/A	N/A

07



PROJECT : EL2

Quanta Computer Inc.

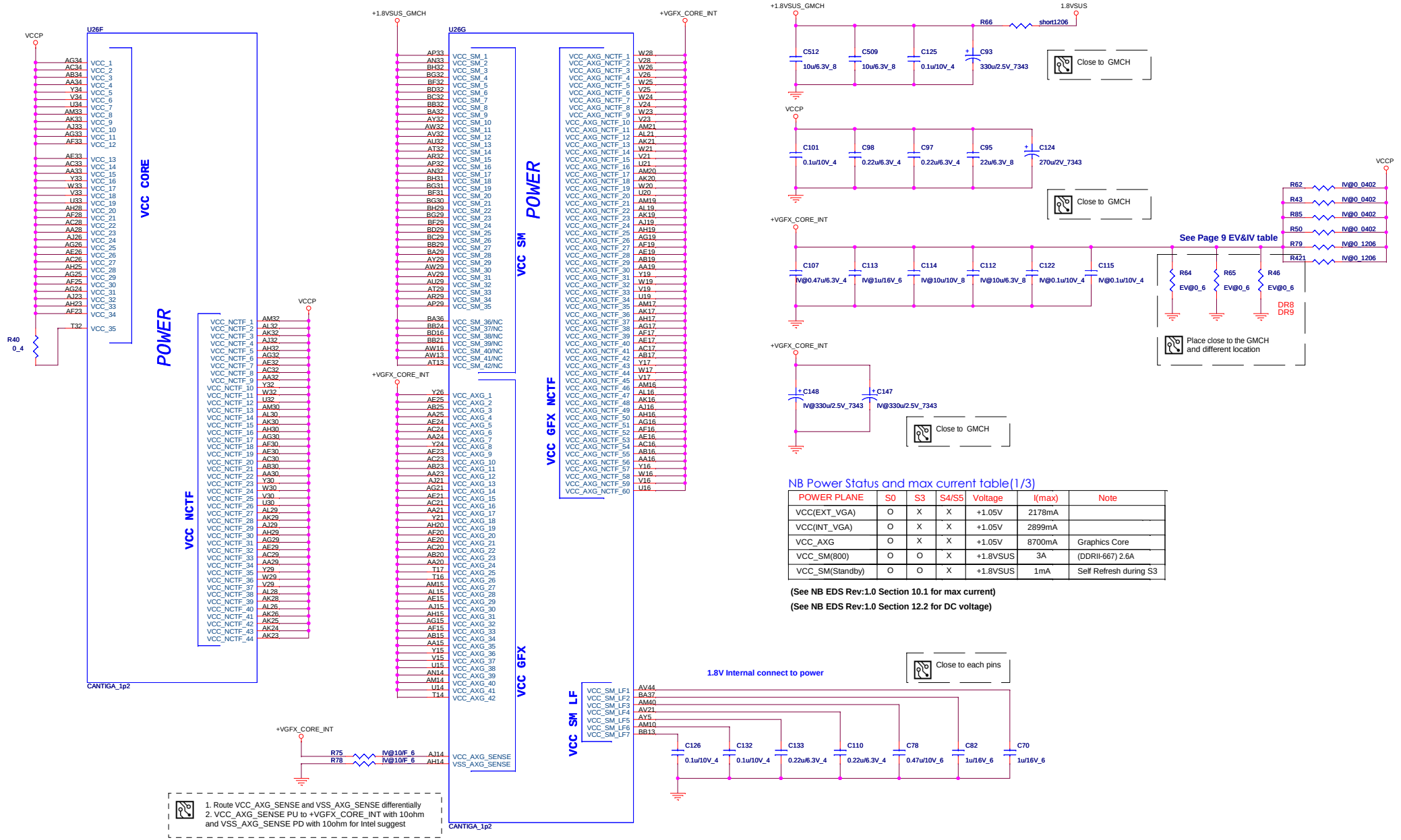
Size	Document Number	Rev
	DDRII	1A
Date: Thursday, August 13, 2009	Sheet 7 of 40	

Laptopblue

08

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA



NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)

(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

PROJECT : EL2

Quanta Computer Inc.

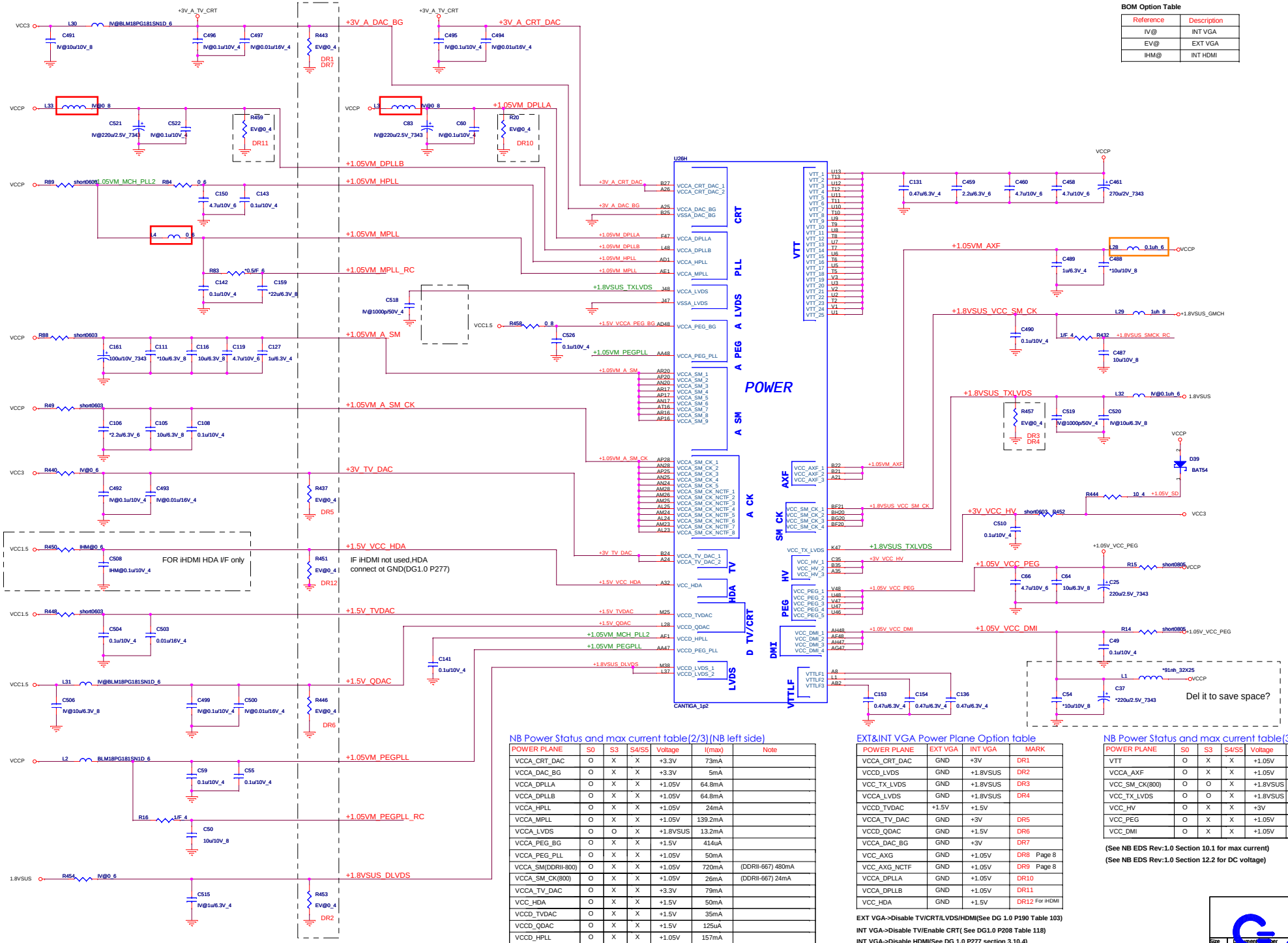
Size	Document Number	Rev
	NB(4/7) VCC ,NCTF	1A

Date: Thursday, August 13, 2009 Sheet 8 of 40

Laptopblue

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI



NB Power Status and max current table(2/3)(NB left side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCA_CRT_DAC	O	X	X	+3.3V	73mA	
VCCA_DAC_BG	O	X	X	+3.3V	5mA	
VCCA_DPLLA	O	X	X	+1.05V	64.8mA	
VCCA_DPLLB	O	X	X	+1.05V	64.8mA	
VCCA_HPLL	O	X	X	+1.05V	24mA	
VCCA_MPLL	O	X	X	+1.05V	139.2mA	
VCCA_LVDS	O	O	X	+1.8VSUS	13.2mA	
VCCA_PEG_BG	O	X	X	+1.5V	414uA	
VCCA_PEG_PLL	O	X	X	+1.05V	50mA	
VCCA_SM(DDRII-800)	O	X	X	+1.05V	720mA	(DDRII-667) 480mA
VCCA_SM_CK(800)	O	X	X	+1.05V	26mA	(DDRII-667) 24mA
VCCA_TV_DAC	O	X	X	+3.3V	79mA	
VCC_HDA	O	X	X	+1.5V	50mA	
VCCD_TVDAC	O	X	X	+1.5V	35mA	
VCCD_QDAC	O	X	X	+1.5V	125uA	
VCCD_HPLL	O	X	X	+1.05V	157mA	
VCCD_PEG_PLL	O	X	X	+1.05V	50mA	
VCCD_LVDS	O	O	X	+1.8VSUS	80mA	

EXT&INT VGA Power Plane Option table

POWER PLANE	EXT VGA	INT VGA	MARK
VCCA_CRT_DAC	GND	+3V	DR1
VCCD_LVDS	GND	+1.8VSUS	DR2
VCC_TX_LVDS	GND	+1.8VSUS	DR3
VCCA_LVDS	GND	+1.8VSUS	DR4
VCCD_TVDAC	+1.5V	+1.5V	
VCCA_TV_DAC	GND	+3V	DR5
VCCD_QDAC	GND	+1.5V	DR6
VCCA_DAC_BG	GND	+3V	DR7
VCC_AXG	GND	+1.05V	DR8 Page 8
VCC_AXG_NCTF	GND	+1.05V	DR9 Page 8
VCCA_DPLLA	GND	+1.05V	DR10
VCCA_DPLLB	GND	+1.05V	DR11
VCC_HDA	GND	+1.5V	DR12 For iHDMI

EXT VGA->Disable TV/CRT/LVDS/HDMI(See DG 1.0 P190 Table 103)

INT VGA->Disable TV/Enable CRT(See DG1.0 P208 Table 118)

INT VGA->Disable HDMI(See DG 1.0 P277 section 3.10.4)

NB Power Status and max current table(3/3)(NB Right side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VTT	O	X	X	+1.05V	852mA	FSB at 1067MHz
VCCA_AXF	O	X	X	+1.05V	322mA	
VCC_SM_CK(800)	O	O	X	+1.8VSUS	124mA	(DDRII-667) 120mA
VCC_TX_LVDS	O	O	X	+1.8VSUS	119mA	
VCC_HV	O	X	X	+3V	106mA	
VCC_PEG	O	X	X	+1.05V	1782mA	
VCC_DMI	O	X	X	+1.05V	456mA	

(See NB EDS Rev:1.0 Section 10.1 for max current)

(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

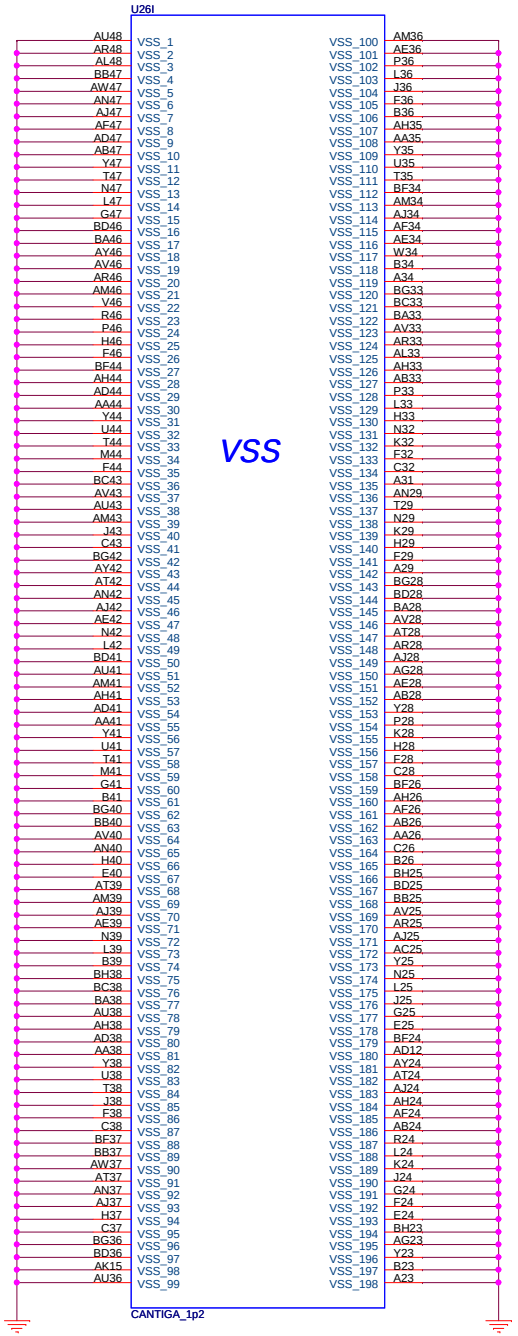
PROJECT : EL2

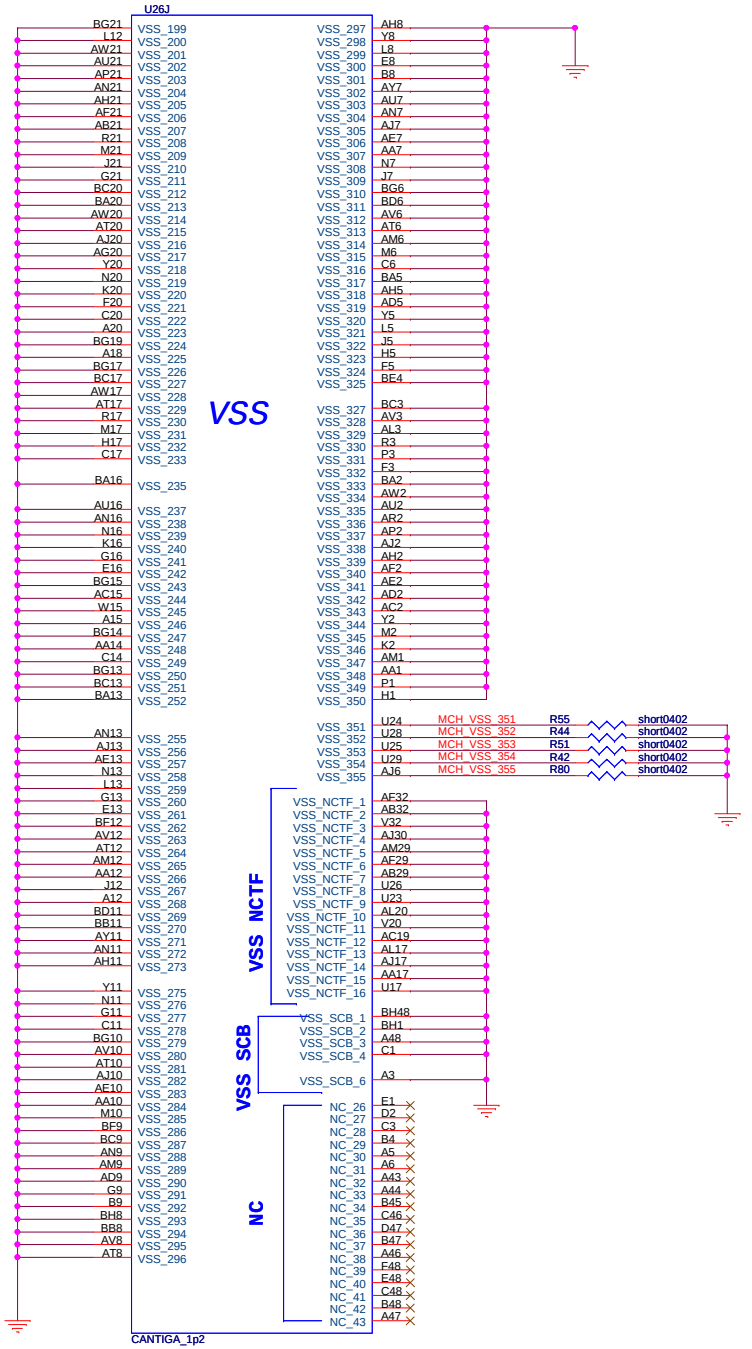
Quanta Computer Inc.

Size: NB(N) POWER | Rev: 1A

Date: Thursday, August 13, 2009 | Sheet 9 of 40

Laptopblue





BOM Option Table

Reference	Description
N/A	N/A

PROJECT :	EL2
Quanta Computer Inc.	
Size	Document Number: NB(6/7) VSS
Rev	1A
Date:	Thursday, August 13, 2009
Sheet	10 of 40

North Bridge Strap Pin Configuration Table

(See DG 1.0 P295 Table 184)
(See NB EDS 1.0 P187 Table 74)

Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
CFG[2:0]	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
CFG[4:3]	Reserved			
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	(6) MCH_CFG_5 R53 *4.02K/F_4	
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	(6) MCH_CFG_6 R54 *10K/F_4	**Enable iTPM**
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	(6) MCH_CFG_7 R52 *4.02K/F_4	
CFG8	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	(6) MCH_CFG_9 R434 *4.02K/F_4	
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)	(6) MCH_CFG_10 R435 *4.02K/F_4	
CFG11	Reserved			
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	(6) MCH_CFG_12 R71 *4.02K/F_4	
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)	(6) MCH_CFG_13 R69 *4.02K/F_4	
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	(6) MCH_CFG_16 R67 *4.02K/F_4	
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	(6) MCH_CFG_19 R59 *4.02K/F_4 VCC3	
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	(6) MCH_CFG_20 R58 *4.02K/F_4 VCC3	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	(6) SDVO_CTRLDATA R30 *2.2K/F_4 VCC3	
L_DDC_DATA	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present;PCIE disable	(6,19) INT_LVDS_EDIDDATA R33 *2.2K/F_4 VCC3	
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	(6) DDPC_CTRLDATA R60 *2.2K/F_4 VCC3	

BOM Option Table

Reference	Description
N/A	N/A

Enable iTPM Table

PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPI_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGPIO5	PU 10K to +3V_S5	SB Strap pin

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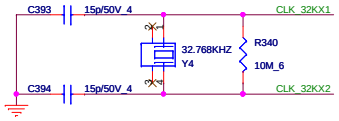
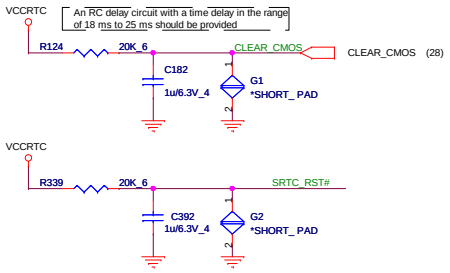
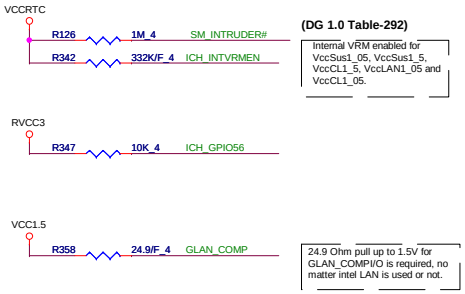
RTC CRYSTAL



RESET JUMP





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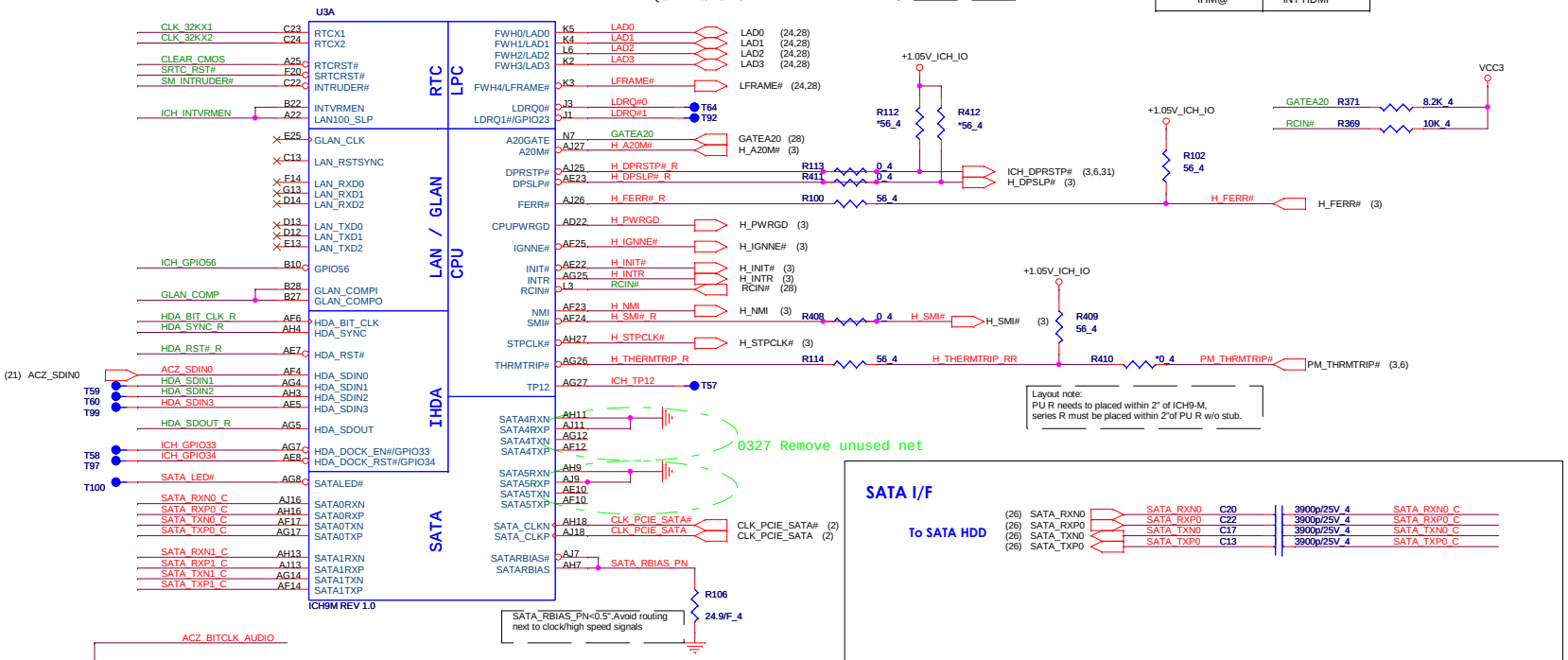
LDRQ0/1# : Internal PU

Layout note:
DPRSTP# , Daisy Chain
(SB>Power>NB>CPU)

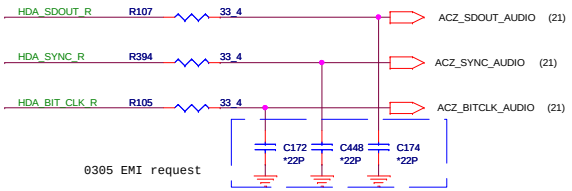
BOM Option Table

Reference	Description
IHM@	INT HDMI

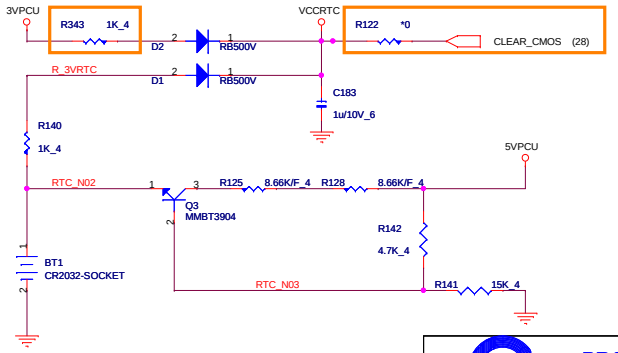


SATA I/F

HD Audio I/F(CODEC& iHDMI)

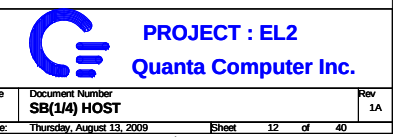


RTC BATTERY



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT: 0/0 RSVD; 0/1 Enter XOR Chain; 1/0 Normal opration(Default); 1/1 Set PCIE port config bit 1	(14) ICH_TP3 — ICH_TP3 R368 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R R108 *1K_4 +3V_HDA_IO_ICH PU VCC1.5



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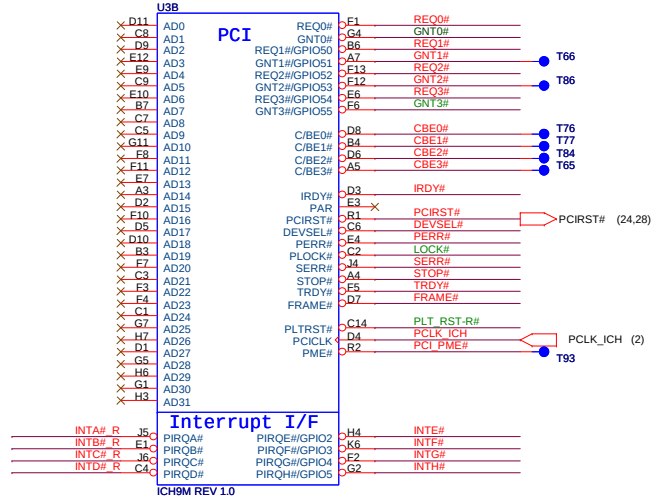
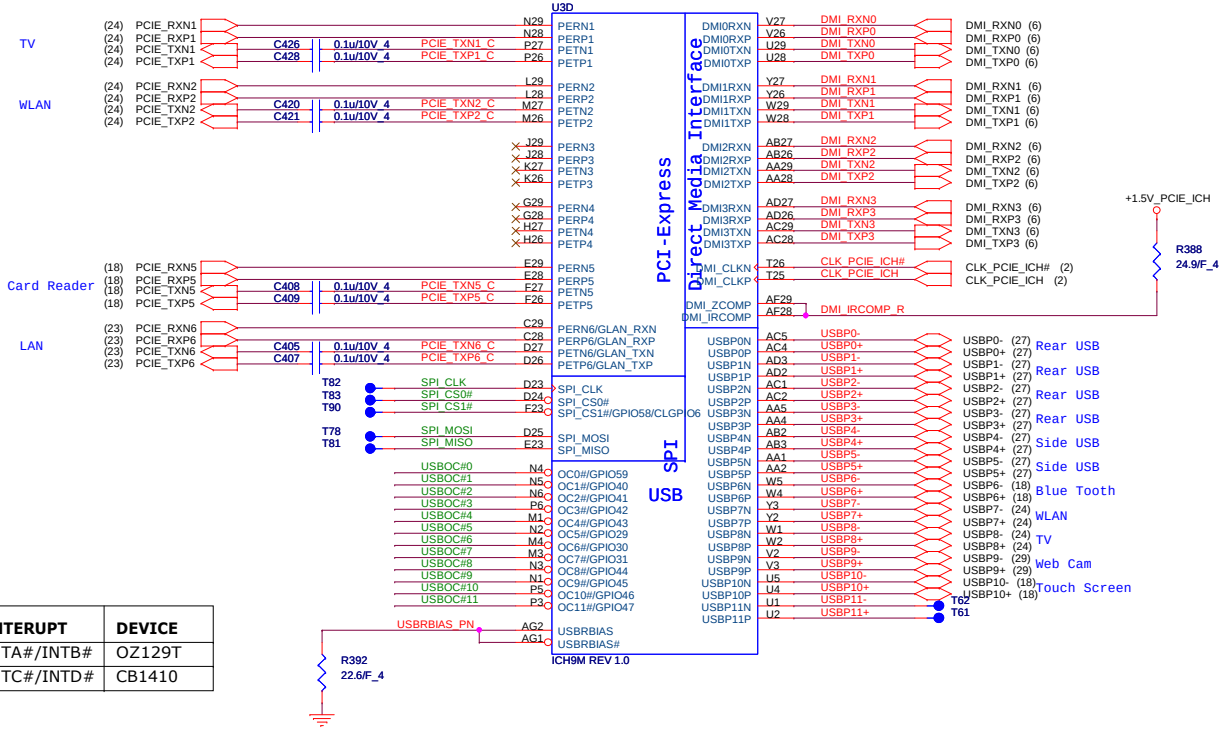
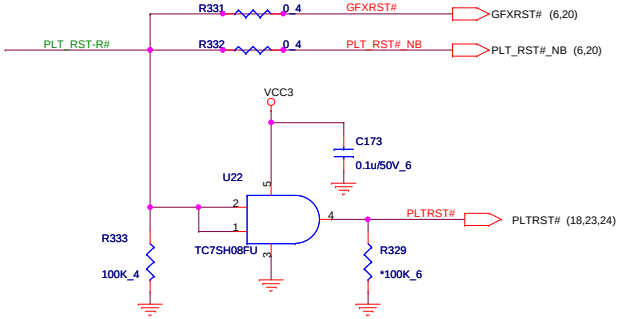
BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA





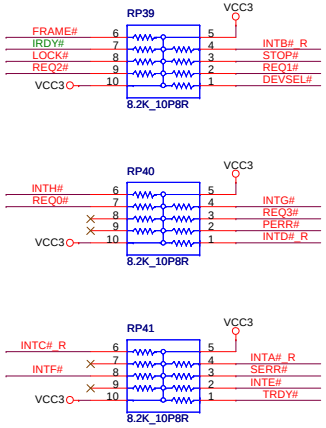


PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#/INTB#	OZ129T
REQ1# / GNT1#	AD20	INTC#/INTD#	CB1410

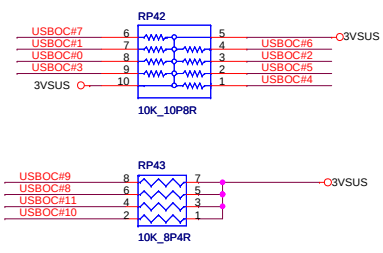
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R330 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	Disable iTPM SPI_MOSI R138 *20K_4 3VSUS
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default) 1 / 0 / PCI 1 / 1 / LPC	GNT0# R364 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# R363 *1K_4

PCI PULL-UP



USBOC# PULL-UP



PROJECT : EL2

Quanta Computer Inc.

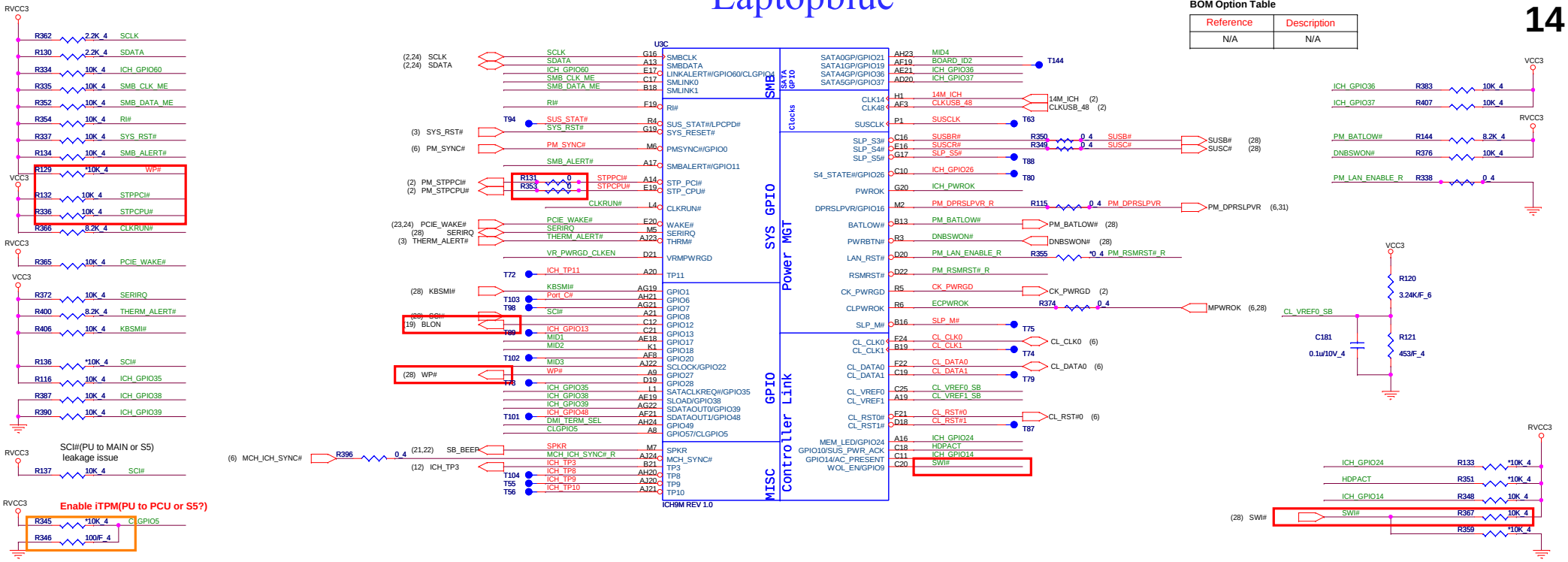
Size	Document Number	Rev
	SB (2/4) PCIE/PCI/USB	1A

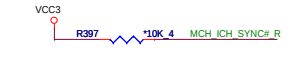
Date: Thursday, August 13, 2009 Sheet 13 of 40

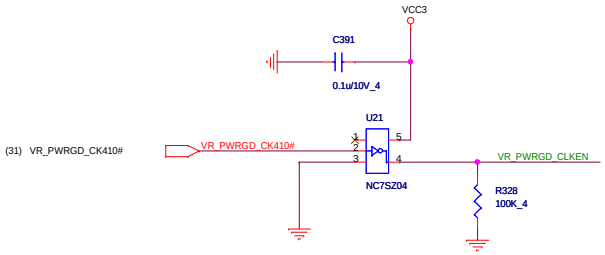
Laptopblue

BOM Option Table

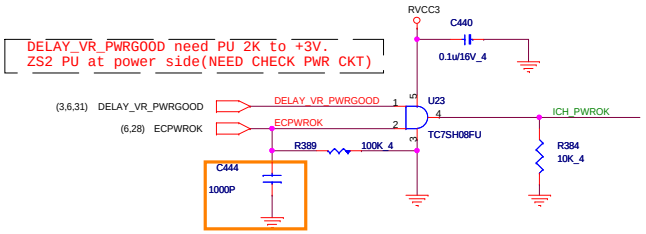
Reference	Description
N/A	N/A

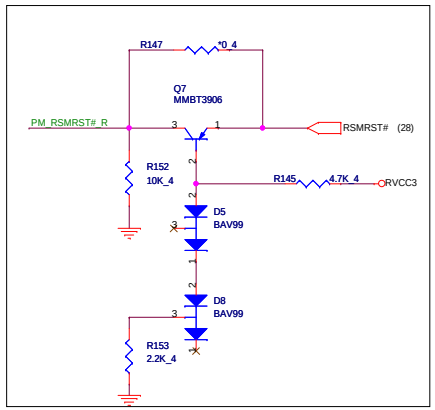


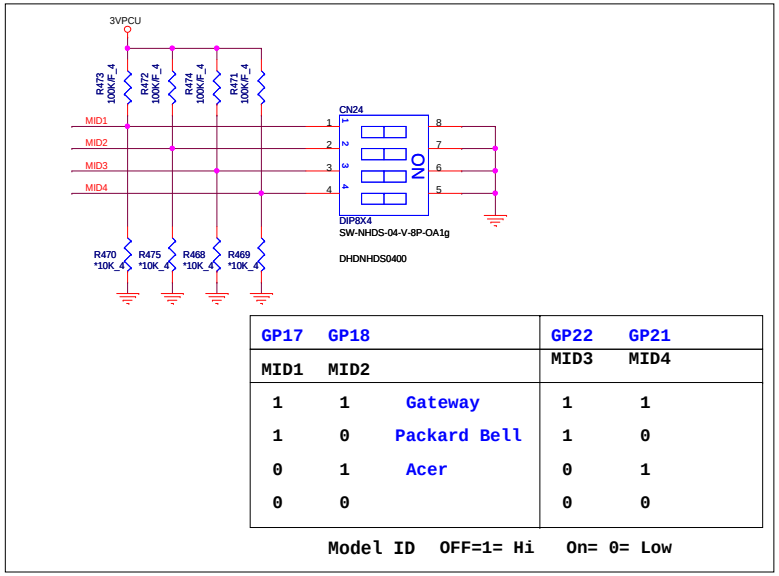




DELAY_VR_PWRGOOD need PU 2K to +3V.
ZS2 PU at power side(NEED CHECK PWR CKT)







GP17	GP18		GP22	GP21
MID1	MID2		MID3	MID4
1	1	Gateway	1	1
1	0	Packard Bell	1	0
0	1	Acer	0	1
0	0		0	0

Model ID OFF=1= Hi On= 0= Low

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	SPKR R370 *1K_4 VCC3
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R393 *1K_4

PROJECT : EL2
Quanta Computer Inc.

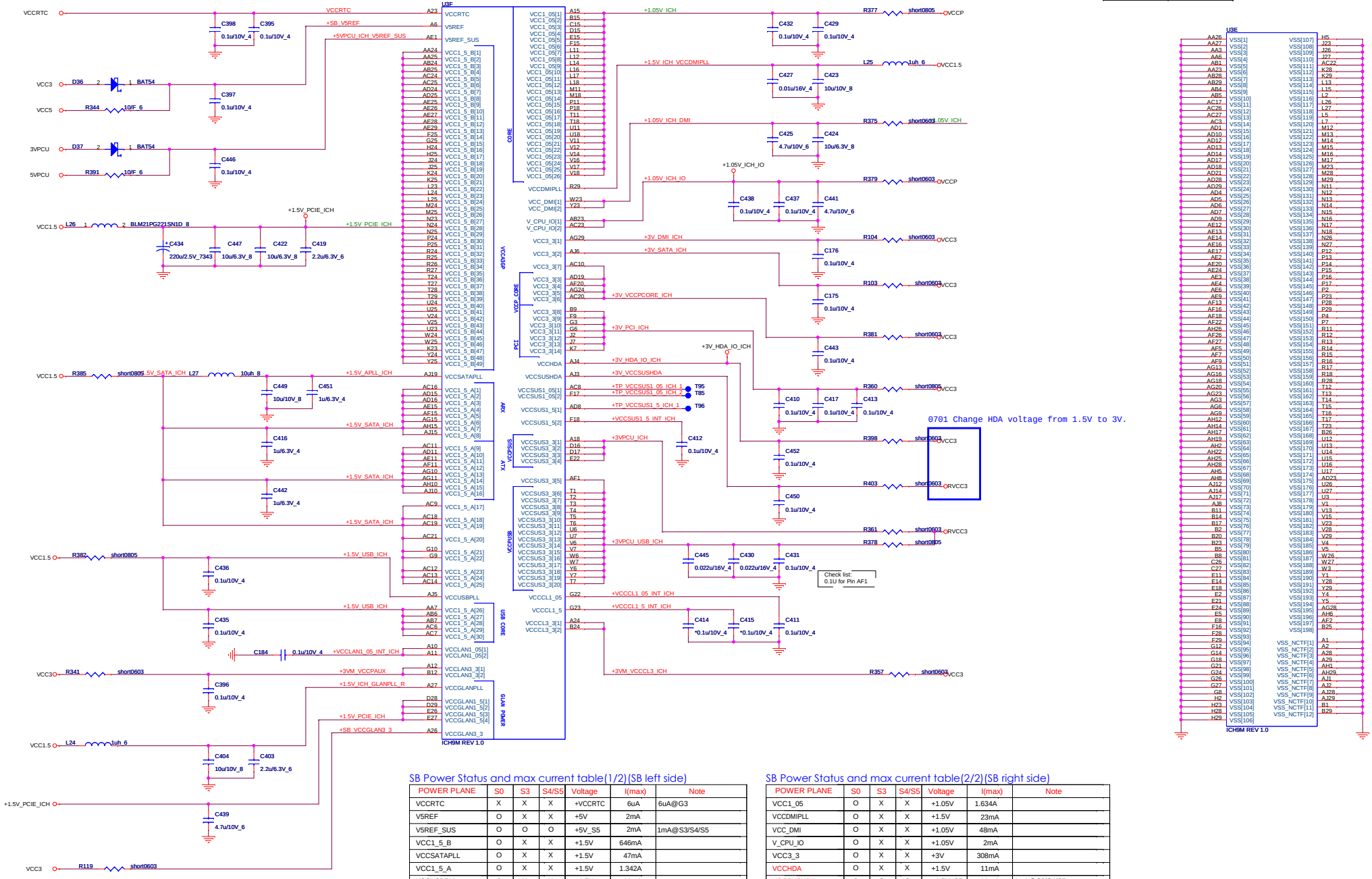
Size	Document Number	Rev
	SB(3/4) GPIO	1A

Date: Thursday, August 13, 2009 Sheet 14 of 40

Laptopblue

BOM Option Table

Reference	Description
N/A	N/A



SB Power Status and max current table(1/2)(SB left side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCRTC	X	X	X	+VCCRTC	6uA	6uA@G3
V5REF	O	X	X	+5V	2mA	
V5REF_SUS	O	O	O	+5V_S5	2mA	1mA@S3/S4/S5
VCC1_5_B	O	X	X	+1.5V	646mA	
VCCSATAPLL	O	X	X	+1.5V	47mA	
VCC1_5_A	O	X	X	+1.5V	1.342A	
VCCUSBPLL	O	X	X	+1.5V	11mA	
VCCLAN1_05	O	X	X	+1.05V	X	Powered by Vcc1_05 in S0
VCCLAN3_3	O	X	X	+3V	19mA	Tied to +3V,not +3VSUS
VCCGLANPLL	O	X	X	+1.5V	23mA	
VCCGLAN1_5	O	X	X	+1.5V	80mA	
VCCGLAN3_3	O	X	X	+3V	1mA	

SB Power Status and max current table(2/2)(SB right side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC1_05	O	X	X	+1.05V	1.634A	
VCCDMIPLL	O	X	X	+1.5V	23mA	
VCC_DMI	O	X	X	+1.05V	48mA	
V_CPU_IO	O	X	X	+1.05V	2mA	
VCC3_3	O	X	X	+3V	308mA	
VCCHDA	O	X	X	+1.5V	11mA	
VCCSUSHDA	O	O	O	+1.5V_S5	11mA	1mA@S3/S4/S5
VCCSUS1_05	O	O	O	+1.05V	X	Powered by Vcc1_05 in S0
VCCSUS1_5	O	O	O	+1.5V	X	Powered by Vcc1_5_A in S0
VCCSUS3_3	O	O	O	+3VSUS	212mA	52mA@S3/S4/S5
VCCCL1_05	O	X	X	+1.05V	X	Powered by Vcc1_05 in S0
VCCCL1_5	O	X	X	+1.5V	X	Powered by Vcc1_5_A in S0
VCCCL3_3	O	X	X	+3V	19mA	Tied to +3V,not +3VSUS

Note:VCCSUS1_05 , VCCSUS1_5 are powered by VccSus3_3 in S3/S4/S5

PROJECT : EL2
Quanta Computer Inc.

Size	Document Number	Rev
	SB(4/4) POWER	1A
Date: Thursday, August 13, 2009	Sheet 15 of 40	

DDR2 Dual channel A/B PULL UP

Laptopblue

BOM Option Table

Reference	Description
N/A	N/A

M_A_A[14..0] → M_A_A[14..0] (7,17)

M_B_A[14..0] → M_B_A[14..0] (7,17)

DDRII A CHANNEL

SMDDR_VTERM

C85 C71 C104 C102 C56 C67 C65 C91 C89 C44 C53 C52 C100 — 0.1u/10V_4

DDRII B CHANNEL

SMDDR_VTERM

C45 C73 C103 C96 C94 C47 C48 C69 C77 C92 C51 C46 C80 — 0.1u/10V_4

Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM

M_A_A3 / M_A_A1	RP15	1 3	2 4	56X2 → SMDDR_VTERM
M_A_A5 / M_A_A8	RP12	1 3	2 4	56X2 → SMDDR_VTERM
M_A_A4 / M_A_A2	RP9	1 3	2 4	56X2 → SMDDR_VTERM
M_A_A11	RP4	1 3	2 4	56X2 → SMDDR_VTERM
(6,17) M_CKE1				
(6,17) M_CKE0	RP5	1 3	2 4	56X2 → SMDDR_VTERM
M_A_A9				
M_A_A12	RP2	1 3	2 4	56X2 → SMDDR_VTERM
(7,17) M_A_BS#2				
(7,17) M_A_BS#1	RP16	1 3	2 4	56X2 → SMDDR_VTERM
M_A_A0				

M_A_A7 / M_A_A6	RP7	1 3	2 4	56X2 → SMDDR_VTERM
(6,17) M_CKE3 / (7,17) M_B_BS#2	RP3	1 3	2 4	56X2 → SMDDR_VTERM
(6,17) M_ODT1 / (6,17) M_CS#1	RP25	1 3	2 4	56X2 → SMDDR_VTERM
(6,17) M_CS#3 / (6,17) M_ODT3	RP24	1 3	2 4	56X2 → SMDDR_VTERM
M_A_A10	RP18	1 3	2 4	56X2 → SMDDR_VTERM
(7,17) M_A_BS#0				
(7,17) M_A_CAS# / (7,17) M_A_WE#	RP22	1 3	2 4	56X2 → SMDDR_VTERM
(6,17) M_CS#0 / (7,17) M_A_RAS#	RP20	1 3	2 4	56X2 → SMDDR_VTERM
(7,17) M_B_CAS# / (7,17) M_B_WE#	RP21	1 3	2 4	56X2 → SMDDR_VTERM
M_B_A11	RP1	1 3	2 4	56X2 → SMDDR_VTERM
(6,17) M_CKE4				
(6,17) M_ODT2 / (7,17) M_B_RAS#	RP19	1 3	2 4	56X2 → SMDDR_VTERM
M_A_A13	RP26	1 3	2 4	56X2 → SMDDR_VTERM
(6,17) M_ODT0				
M_B_A13	RP23	1 3	2 4	56X2 → SMDDR_VTERM
(6,17) M_CS#2				

M_B_A10	RP17	1 3	2 4 56X2 → SMDDR_VTERM
(7,17) M_B_BS#0			
M_B_A3 / M_B_A1	RP13	1 3	2 4 56X2 → SMDDR_VTERM
(7,17) M_B_BS#1	RP14	1 3	2 4 56X2 → SMDDR_VTERM
M_B_A0			
M_B_A7 / M_B_A6	RP8	1 3	2 4 56X2 → SMDDR_VTERM
M_B_A8 / M_B_A5	RP10	1 3	2 4 56X2 → SMDDR_VTERM
M_B_A2 / M_B_A4	RP11	1 3	2 4 56X2 → SMDDR_VTERM
M_B_A12 / M_B_A9	RP6	1 3	2 4 56X2 → SMDDR_VTERM

M_A_A14 — R17 — 56_4 → SMDDR_VTERM

M_B_A14 — R19 — 56_4 → SMDDR_VTERM

PROJECT : EL2

Quanta Computer Inc.

Size	Document Number	Rev
	DDR RES. ARRAV	1A

Date: Thursday, August 13, 2009 Sheet 16 of 40

DDR II DIMM Socket

BOM Option Table

Reference	Description
N/A	N/A

M_A_DM[0..7] (7)
M_A_DQS[0..7] (7)
M_A_DQS#[0..7] (7)
M_A_A[0..14] (7,16)

(7) M_A_DQ[0..7]
(7) M_A_DQ[8..15]
(7) M_A_DQ[16..23]
(7) M_A_DQ[24..31]
(7) M_A_DQ[32..39]
(7) M_A_DQ[40..47]
(7) M_A_DQ[48..55]
(7) M_A_DQ[56..63]

SMDDR_VREF_DIMM
1.8VSUS

CN17

PC4800 DDR2 SDRAM
SO-DIMM (200P)

DDR2_5.6H

M_CLK_DDR0 (6)
M_CLK_DDR#0 (6)
PM_EXTTS#0 (6)
M_CKE0 (6,16)
M_CKE1 (6,16)
M_A_BS#2 (7,16)
M_A_BS#0 (7,16)
M_A_BS#1 (7,16)
M_A_RAS# (7,16)
M_A_WE# (7,16)
M_CS#0 (6,16)
M_A_CAS# (7,16)
M_CS#1 (6,16)
M_ODT0 (6,16)
M_ODT1 (6,16)
M_CLK_DDR1 (6)
M_CLK_DDR#1 (6)
R82 10K_4
R86 10K_4
VCC3

CH-A SPD ADDRESS:??????

M_B_DM[0..7] (7)
M_B_DQS[0..7] (7)
M_B_DQS#[0..7] (7)
M_B_A[0..14] (7,16)

(7) M_B_DQ[0..7]
(7) M_B_DQ[8..15]
(7) M_B_DQ[16..23]
(7) M_B_DQ[24..31]
(7) M_B_DQ[32..39]
(7) M_B_DQ[40..47]
(7) M_B_DQ[48..55]
(7) M_B_DQ[56..63]

SMDDR_VREF_DIMM
1.8VSUS

CN18

PC4800 DDR2 SDRAM
SO-DIMM (200P)

DDR2_10.1H

M_CLK_DDR3 (6)
M_CLK_DDR#3 (6)
PM_EXTTS#1 (6)
M_CKE3 (6,16)
M_CKE4 (6,16)
M_B_BS#2 (7,16)
M_B_BS#0 (7,16)
M_B_BS#1 (7,16)
M_B_RAS# (7,16)
M_B_WE# (7,16)
M_CS#2 (6,16)
M_B_CAS# (7,16)
M_CS#3 (6,16)
M_ODT2 (6,16)
M_ODT3 (6,16)
M_CLK_DDR4 (6)
M_CLK_DDR#4 (6)
R426 10K_4
R422 10K_4
CGDAT_SMB (2)
CGCLK_SMB (2)
VCC3

CH-A SPD ADDRESS:??????

1.8VSUS
+C90 330u/2.5V_3528
C513 2.2u/6.3V_6
C517 2.2u/6.3V_6
C61 2.2u/6.3V_6
C74 2.2u/6.3V_6
C511 2.2u/6.3V_6
VCC3
C84 0.1u/10V_4
C62 0.1u/10V_4
C88 0.1u/10V_4
C68 0.1u/10V_4
C145 2.2u/6.3V_6
C144 0.1u/10V_4
SMDDR_VREF_DIMM
C19 0.1u/10V_4
C16 2.2u/6.3V_6

1.8VSUS
+C79 330u/2.5V_3528
C507 2.2u/6.3V_6
C99 2.2u/6.3V_6
C514 2.2u/6.3V_6
C87 2.2u/6.3V_6
C516 2.2u/6.3V_6
1.8VSUS
VCC3
C58 0.1u/10V_4
C76 0.1u/10V_4
C72 0.1u/10V_4
C81 0.1u/10V_4
C149 2.2u/6.3V_6
C146 0.1u/10V_4
SMDDR_VREF_DIMM
C21 0.1u/10V_4
C18 2.2u/6.3V_6

SMDDR_VREF_DIMM
R11 short0603
SMDDR_VREF
R5 *10K_4
R8 *10K_4
1.8VSUS

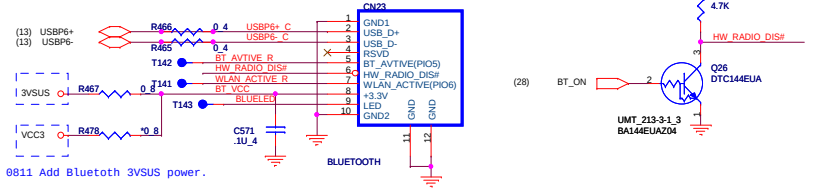
PROJECT : EL2
Quanta Computer Inc.

Size	Document Number	Rev
	DDR SO-DIMM	1A

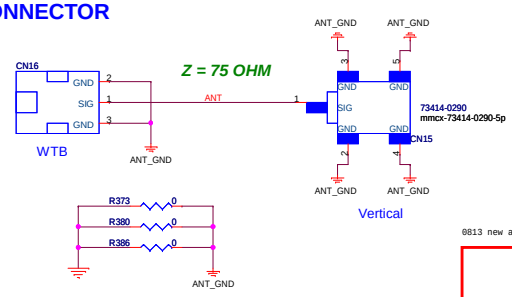
Date: Thursday, August 13, 2009 Sheet 17 of 40

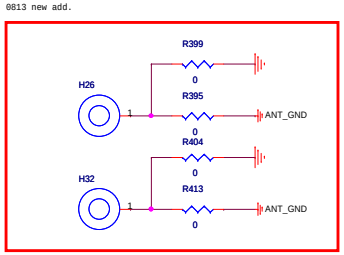
Laptopblue

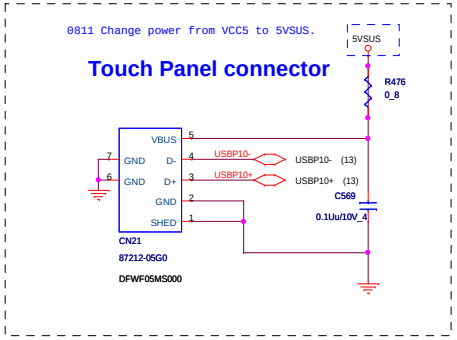
BLUETOOTH

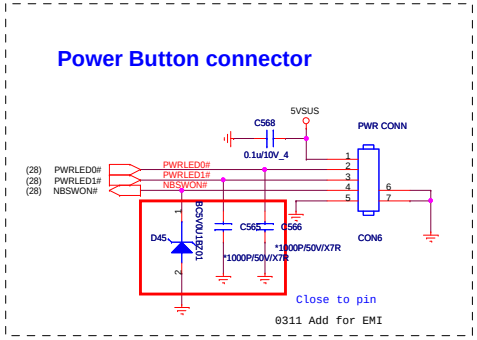


TV ANT. CONNECTOR

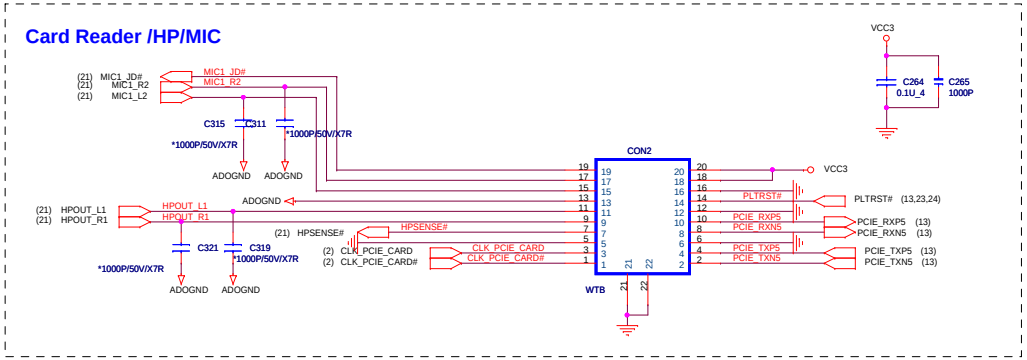








Card Reader /HP/MIC

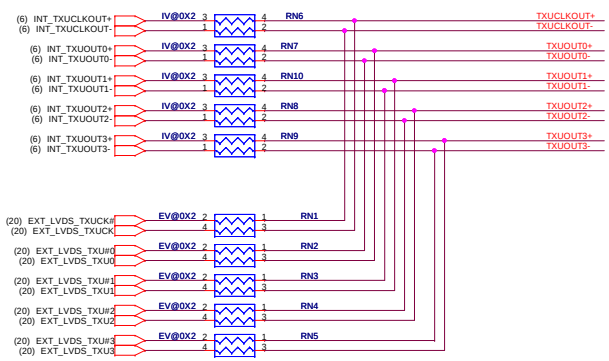


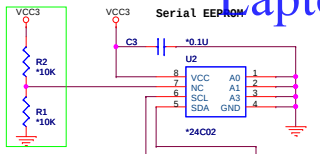
PROJECT : EL2

Quanta Computer Inc.

Size	Document Number	Rev
	Connector	1A

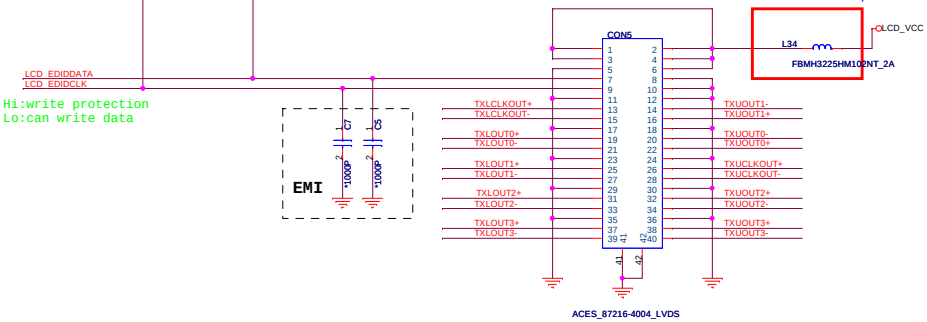
Date: Thursday, August 13, 2009 Sheet 18 of 40

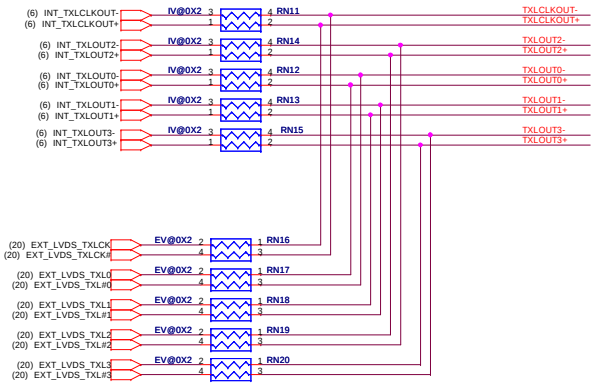


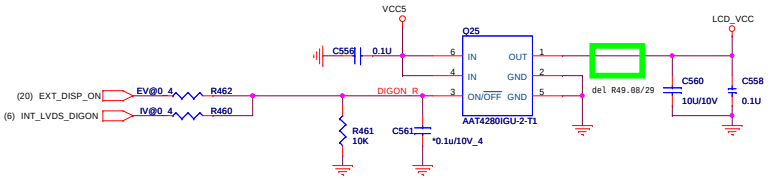


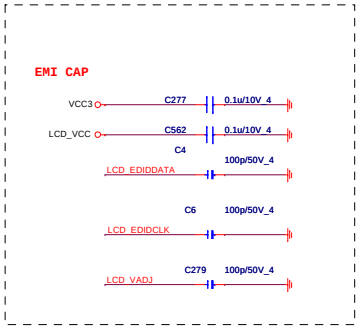
LCD CONNECTOR

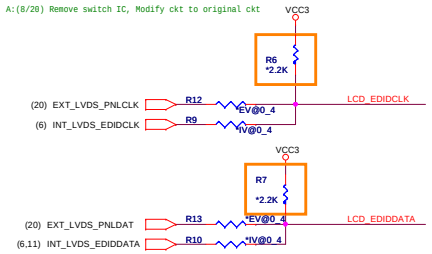
0526 EMI request.

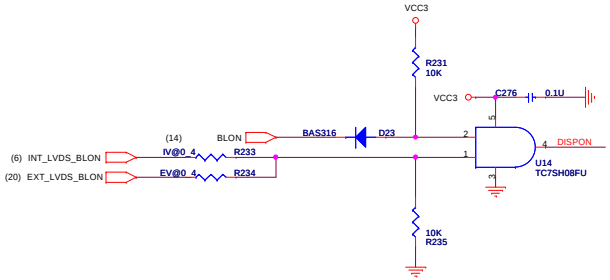




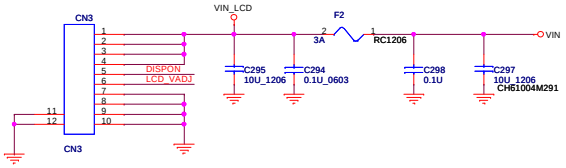


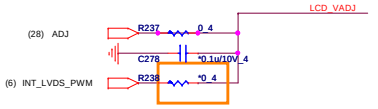




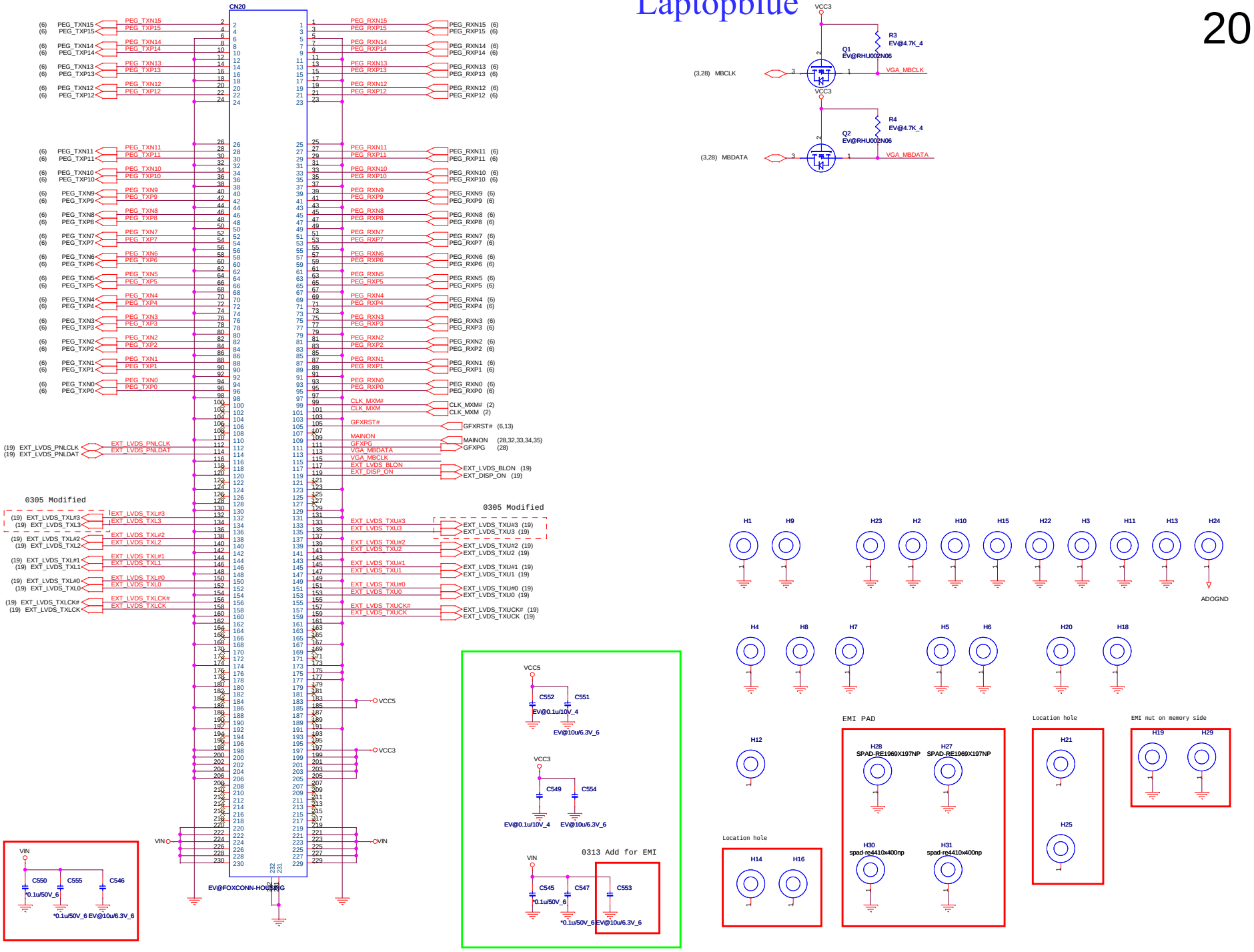


TO INVERTER POWER





PROJECT : EL2		
Quanta Computer Inc.		
Size	Document Number: LCD CONNECTOR	Rev: 1A
Date: Thursday, August 13, 2009	Sheet 19 of 40	



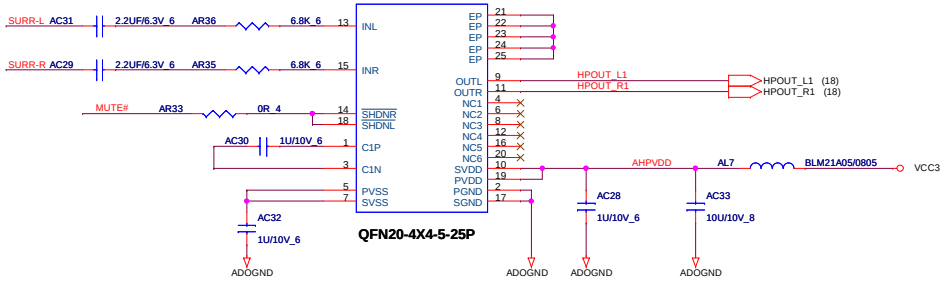
PROJECT : EL2		
Quanta Computer Inc.		
Size	Document Number: MXM CONNECTOR/ Screw	Rev: 1A
Date: Thursday, August 13, 2009	Sheet 20 of 40	

Codec(ALC268)

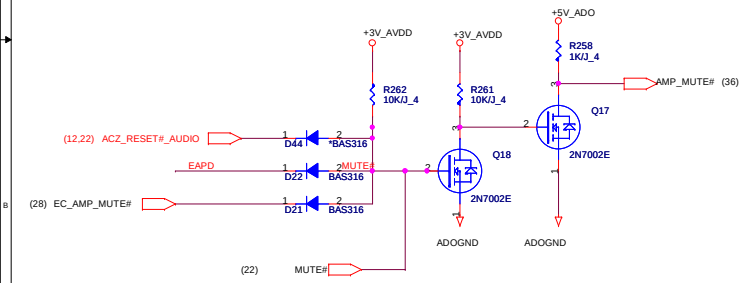
Head Phone Amplifier

AU7

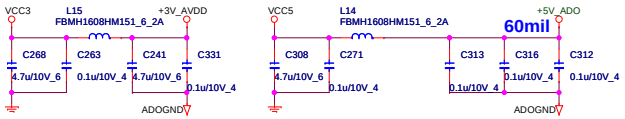
MAX4411/TPA4411MRTJ

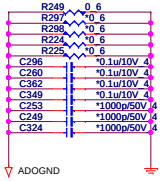


MUTE



Amplifier POWER



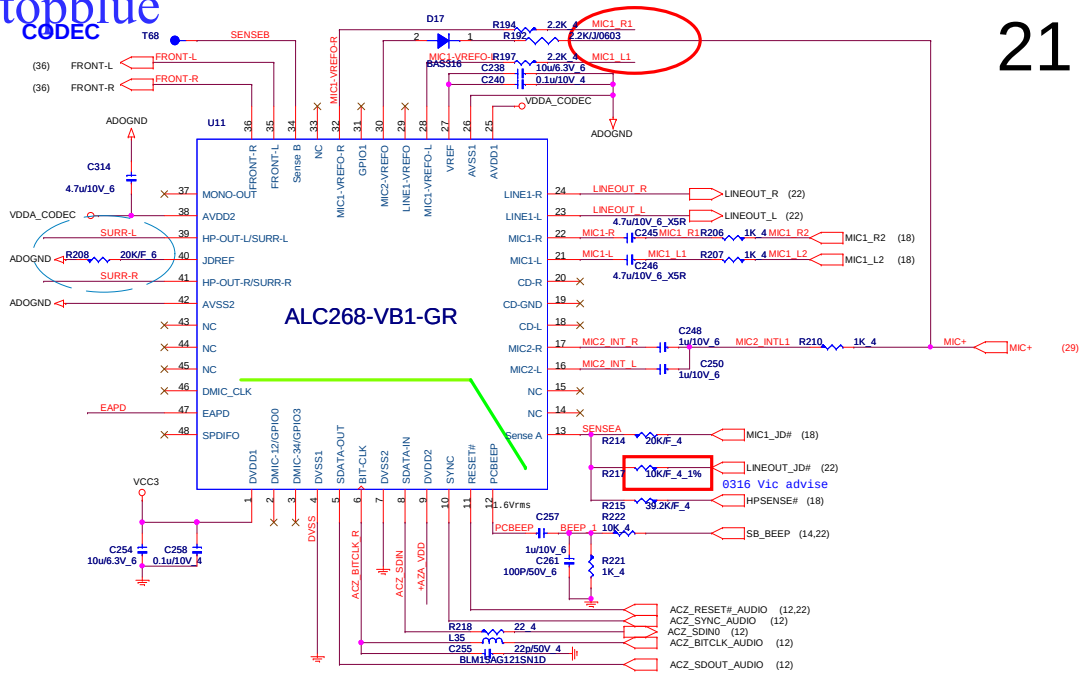


Tied at one point only
under the codec or
near the codec

Laptopblue

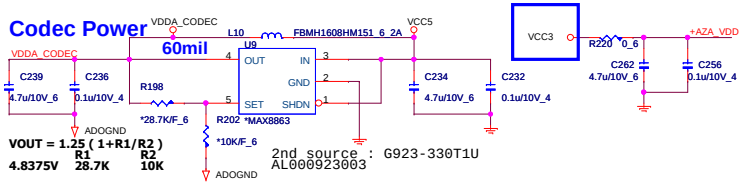
21

CODEC



Codec Power

0701 Modify from VCC1.5 to VCC3.



VOUT = 1.25 (1+R1/R2)

R1	R2
4.8375V	28.7K	10K

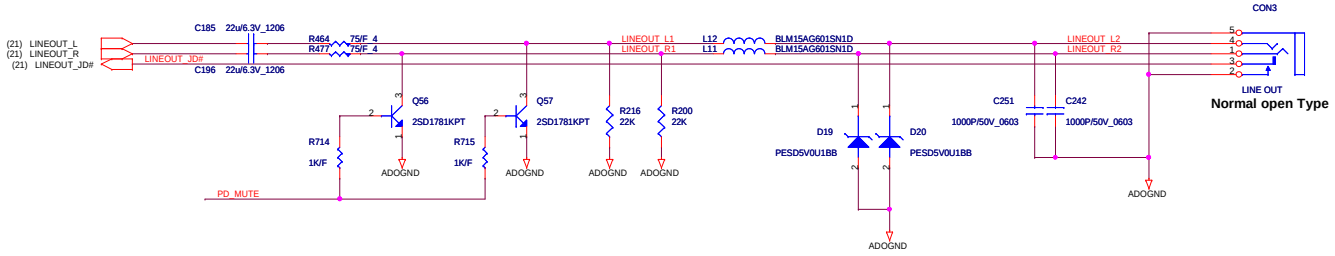
2nd source : G923-330T1U
AL000923003

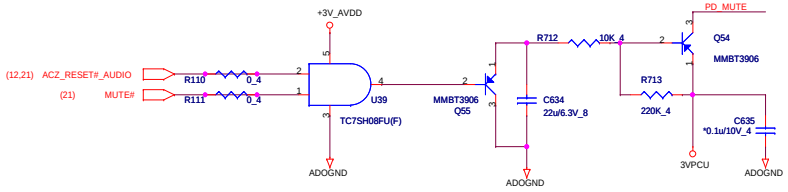
PROJECT : EL2
Quanta Computer Inc.

Size	Document Number	Rev
	Codec ALC268-VB1-GR	1A
Date: Thursday, August 13, 2009	Sheet 21 of 40	

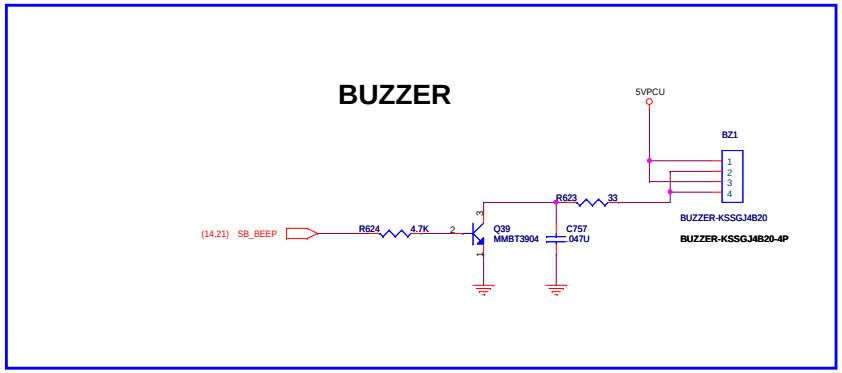
PROJECT : EL2
Quanta Computer Inc.

LINE OUT





0708 Add Buzzer circuit.



PROJECT : EL2
Quanta Computer Inc.

Size	Document Number	Rev
	LINEOUT JACK	1A
Date: Thursday, August 13, 2009	Sheet 22 of 40	

Remove R395 if external power 1.2v is used.
Remove R446 if switching regulator is enable

建議4.7uH power choke, tolerance <20%, 耐電流 >600mA, efficiency >75%

Reserve EEPROM for first stage. No stuff.

Rich Power comment:No matter U28 mounted or not ,R397 always shall be mounted!

X'tal 25MHz

Change X'tal the same EL1V

XTL-5_3X3_2-3_8-1_2H

EC-A-01

RTL8111DL

modified 2009/01/13 by Rich Power comment

CLK G have't CLKREQB function

0413 Follow EL7 LAN function.

Tramsformer

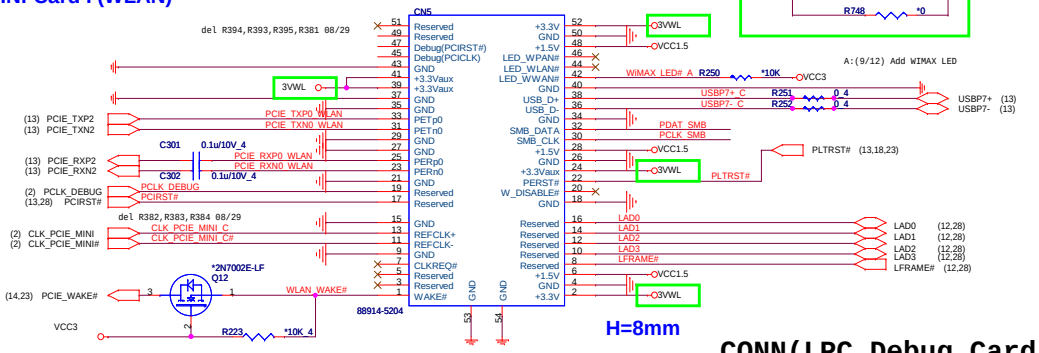
DBBL5MLAN01

LFE9276A-R

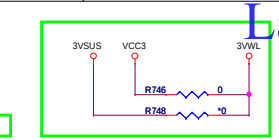
1000:Yellow

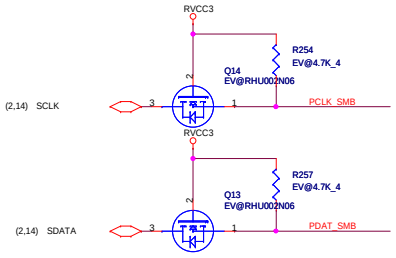
100:Green

MINI-Card I (WLAN)



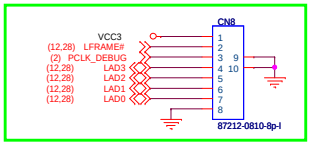
ACES P/N:DFHD52MS065





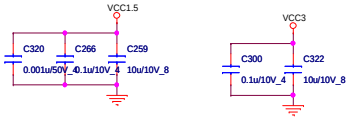
CONN(LPC Debug Card)

ES2

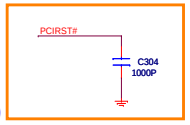


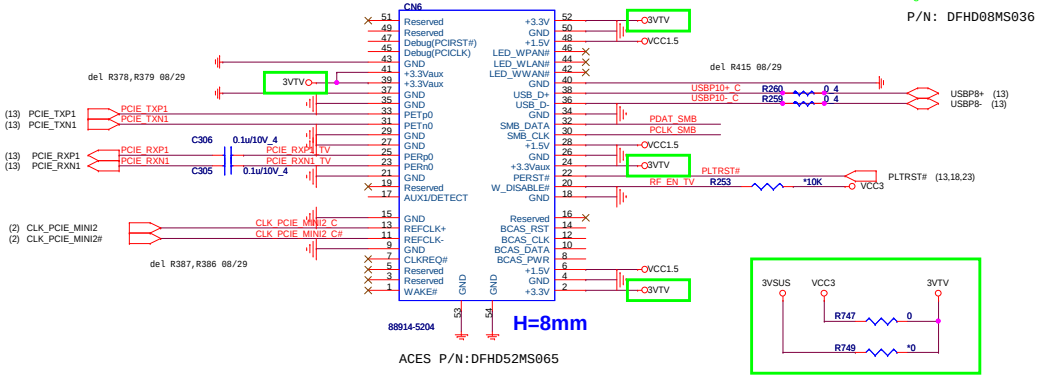
0408 Add for debug

P/N: DFHD08MS036

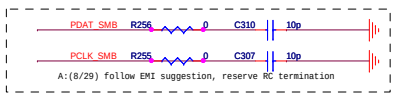


MINI-Card II (TV)





ACES P/N:DFHD52MS065



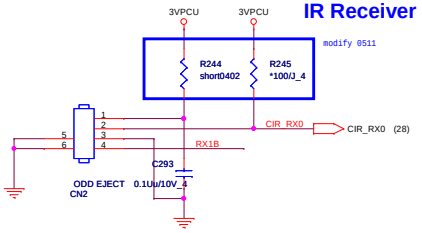
PROJECT : EL2

Quanta Computer Inc.

Size	Document Number	Rev
	MINI CARD/NEW CARD	1A
Date: Thursday, August 13, 2009	Sheet 24 of 40	

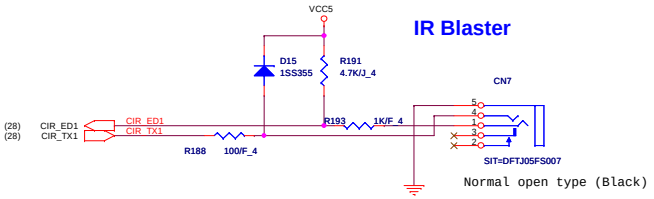
From EL8

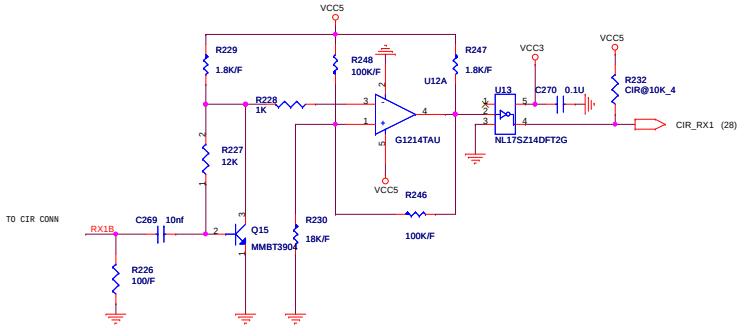
IR Receiver



modify 0605

IR Blaster





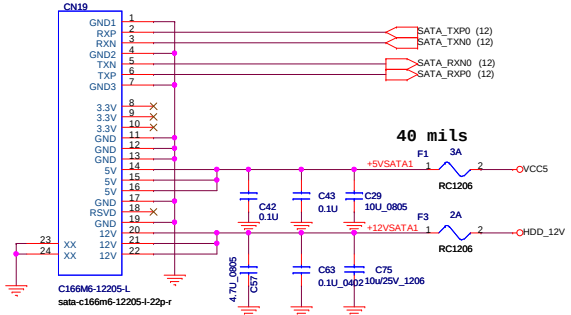
Size	Document Number: IR Blaster /Receiver	Rev: 1A
Date: Thursday, August 13, 2009	Sheet 25 of 40	

PROJECT : EL2

Quanta Computer Inc.

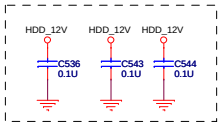
SATA HDD

From EL1



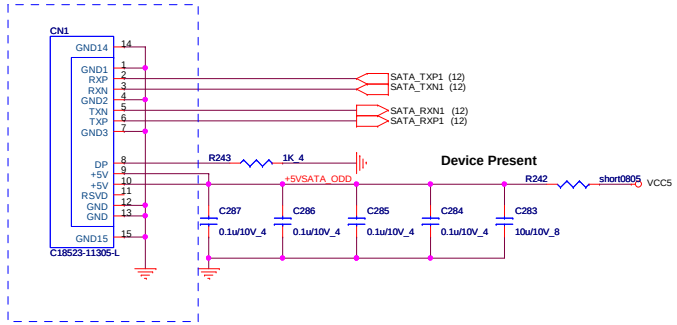
P/N: DFHS22FR151

for EMI 0805



SATA ODD

From PB6



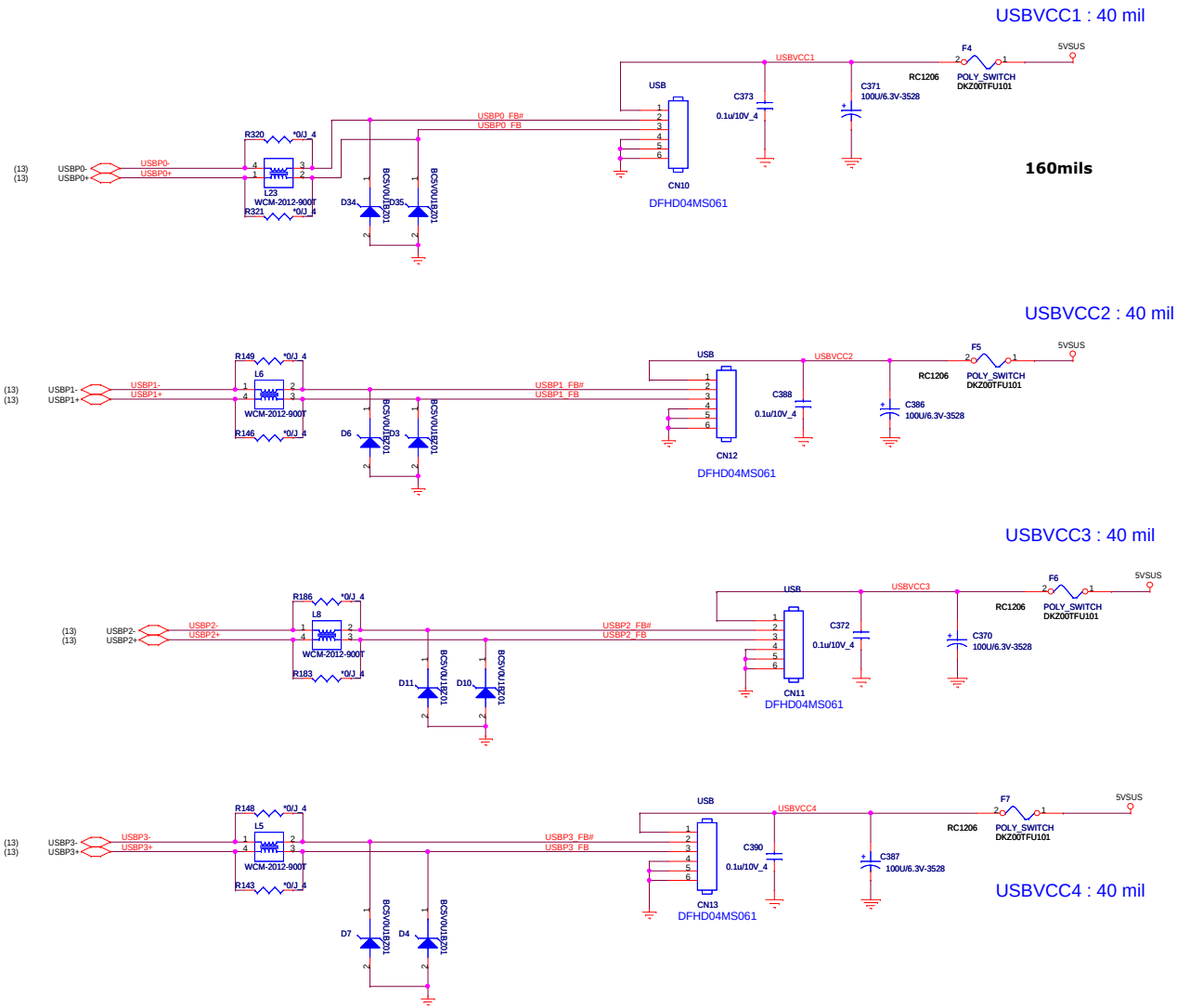
P/N: DFHS13FR016

PROJECT : EL2

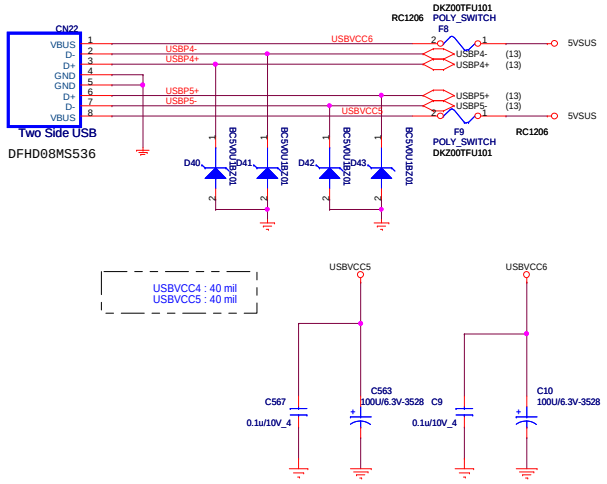
Quanta Computer Inc.

Size	Document Number	Rev
	SATA HDD /ODD	1A
Date: Thursday, August 13, 2009	Sheet 26 of 40	

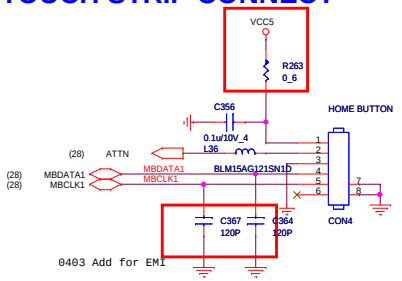
REAR USB PORT X4



SIDE USB PORT X2

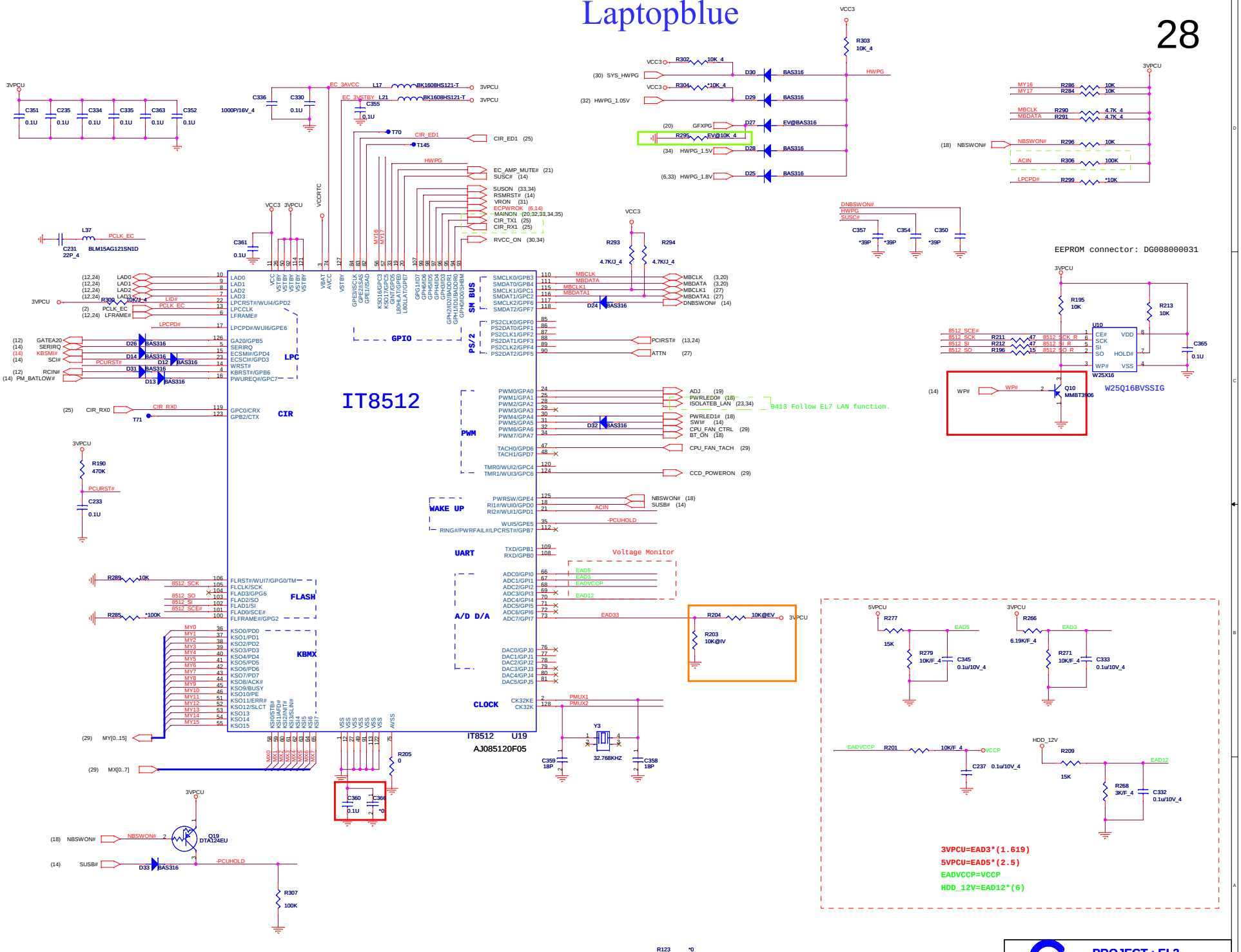


TO TOUCH STRIP CONNECT

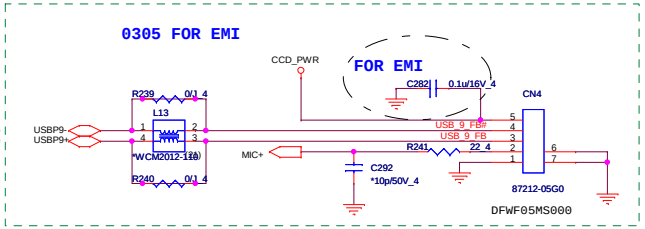


HOME BUTTON

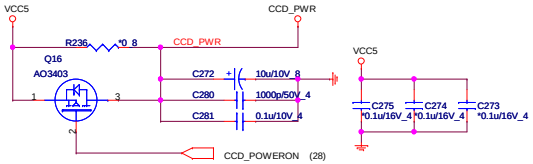
PROJECT : EL2		
Quanta Computer Inc.		
Size	Document Number: USB Connector/ Touch Strip	Rev: 1A
Date: Thursday, August 13, 2009	Sheet 27 of 40	


IT8512
IT8512 U19
AJ085120F05
LPC
CIR
GPIO
PS/2
SM BUS
PWM
WAKE UP
UART
A/D D/A
CLOCK
FLASH
KBMX
Voltage Monitor
EEPROM connector: DG008000031
W25Q16BVSSIG
0413 Follow EL7 LAN function.
3VPCU=EAD3*(1.619)
5VPCU=EAD5*(2.5)
EADVCCP=VCCP
HDD_12V=EAD12*(6)

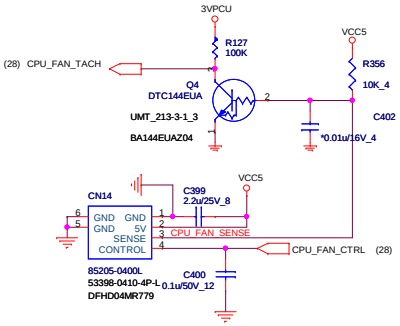
WEB CAM MODULE



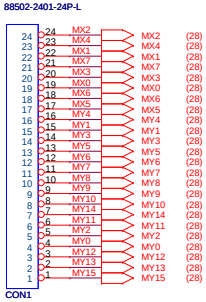
CAMERA POWER



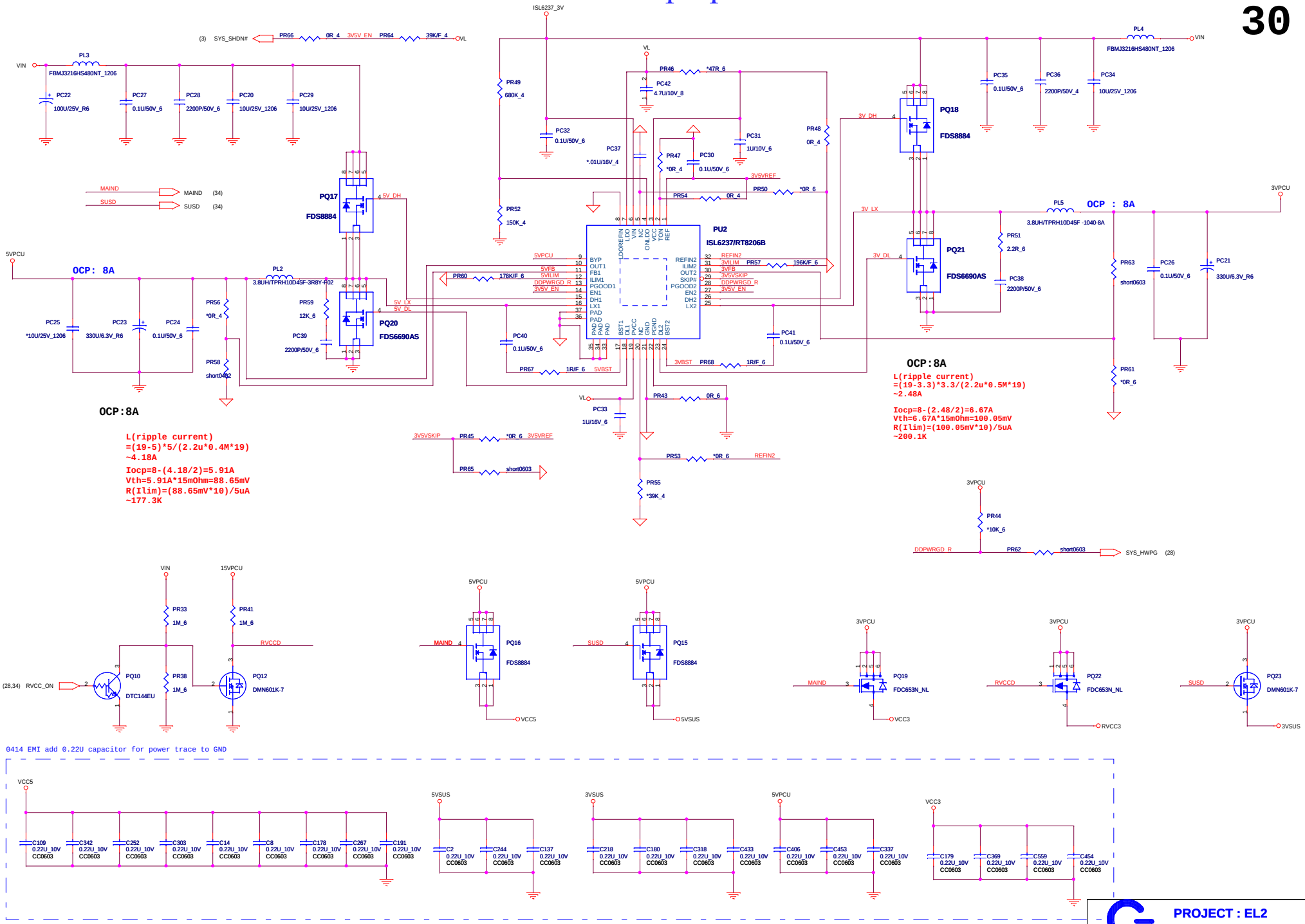
CPU FAN

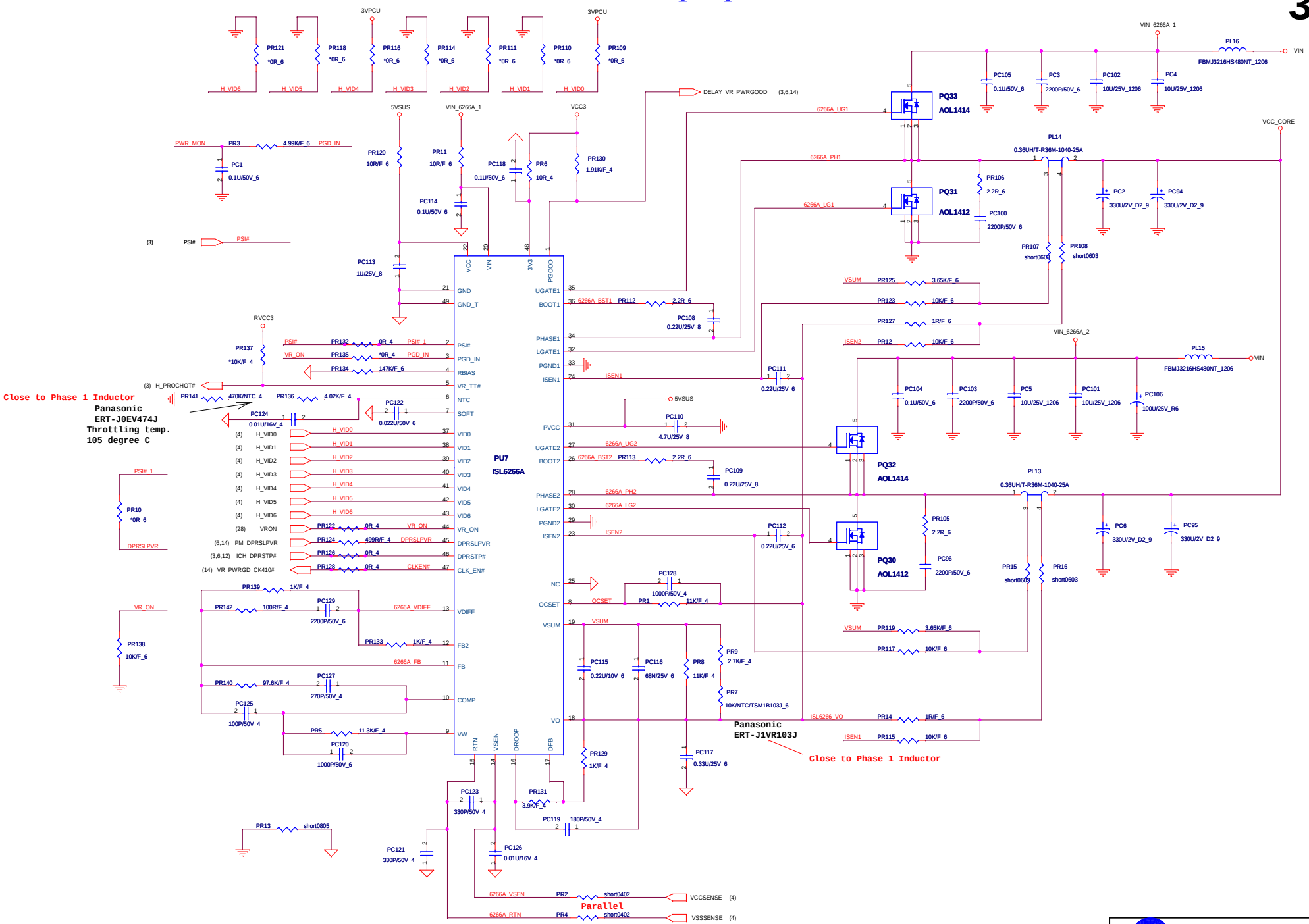


KEYBOARD

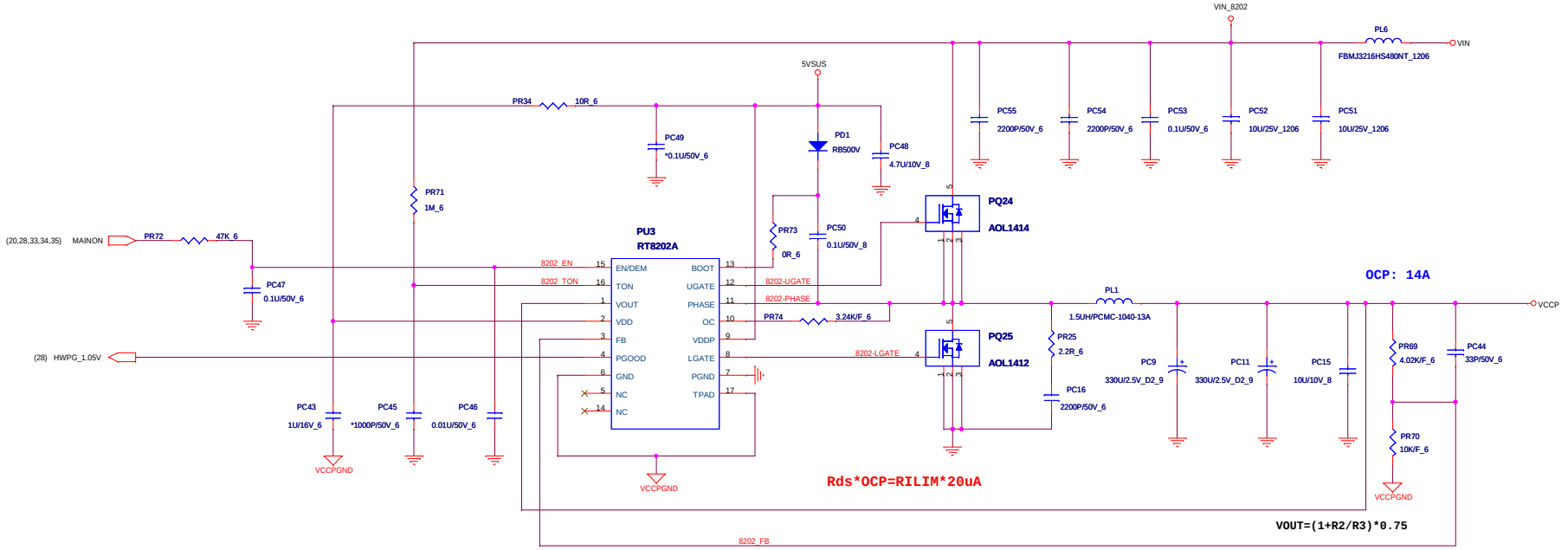


PROJECT : EL2		
Quanta Computer Inc.		
Size	Document Number: CPU FAN/ Web Cam/ KB	Rev: 1A
Date: Thursday, August 13, 2009	Sheet 29 of 40	


ISL6237_3V
VIN
VL
PU2
ISL6237/RT8206B
PQ17
FDS8884
PQ18
FDS8884
PQ20
FDS6690AS
PQ21
FDS6690AS
5VPCU
3VPCU
OCP: 8A
OCP:8A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=8-(4.18/2)=5.91A
Vth=6.67A*15mOhm=88.65mV
R(Ilim)=(88.65mV*10)/5uA
~177.3K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=100.05mV
R(Ilim)=(100.05mV*10)/5uA
~200.1K
0414 EMI add 0.22U capacitor for power trace to GND
PROJECT : EL2
Quanta Computer Inc.
SYSTEM 5V/3V (ISL6237)
Thursday, August 13, 2009
Sheet 30 of 40



PROJECT : EL2			
Quanta Computer Inc.			
Size	Document Number		Rev
	CPU CORE(ISL6266A)		1A
Date: Thursday, August 13, 2009		Sheet 31 of 40	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

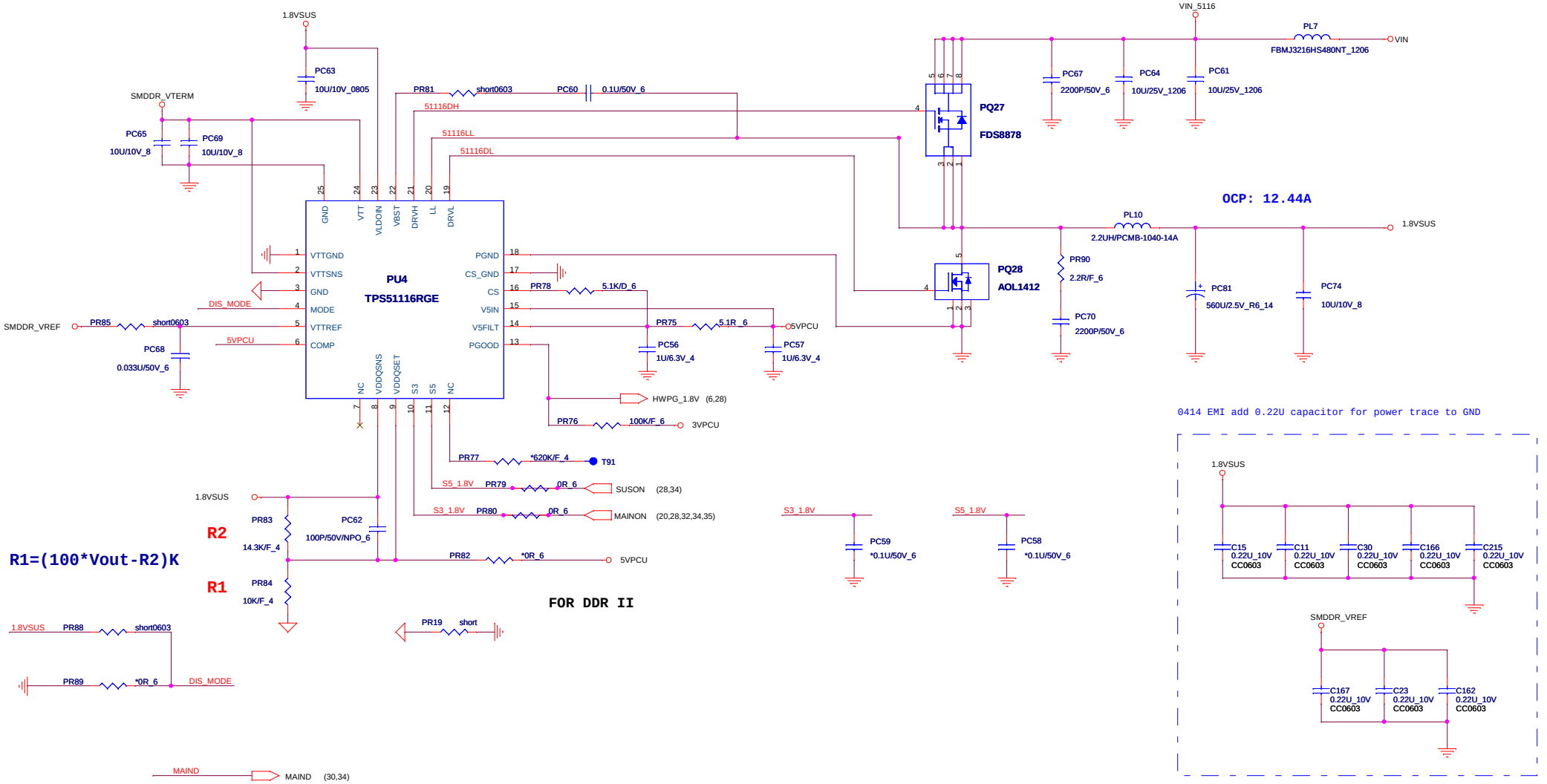
AOL1412 Rds=4.6mOhm

14A OCP --- OC=3.22K

PROJECT : EL2

Quanta Computer Inc.

Size	Document Number	Rev
	VTT 1.05V (RT8202)	1A
Date: Thursday, August 13, 2009	Sheet 32 of 40	

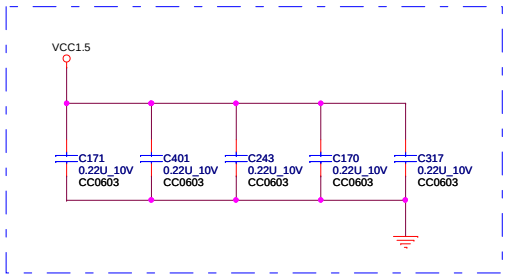


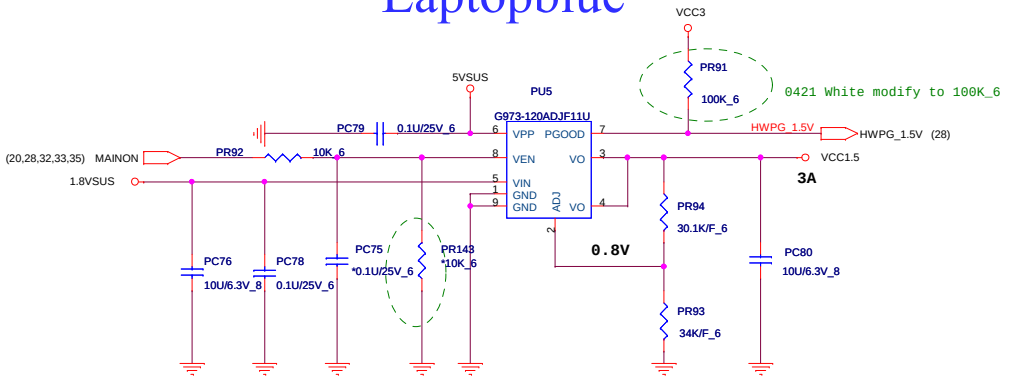
PROJECT : EL2

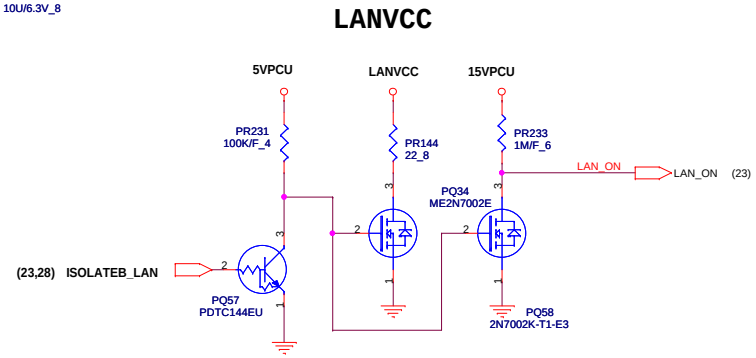
Quanta Computer Inc.

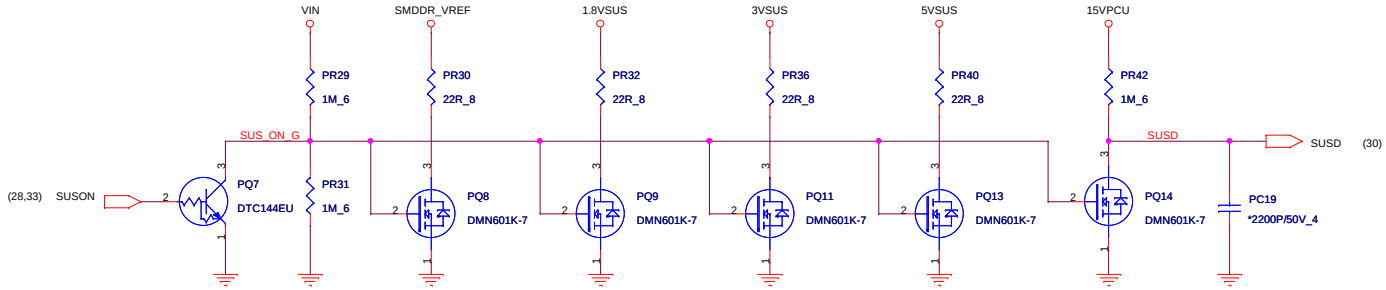
Size	Document Number	Rev
	DDR 1.8V(TPS51116)	1A
Date: Thursday, August 13, 2009	Sheet 33 of 40	

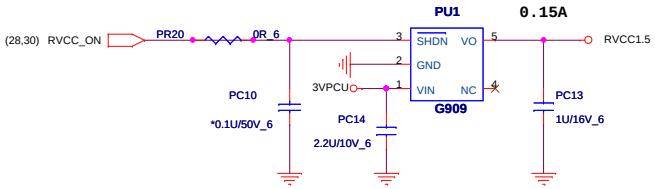
0414 EMI add 0.22U capacitor for power trace to GND



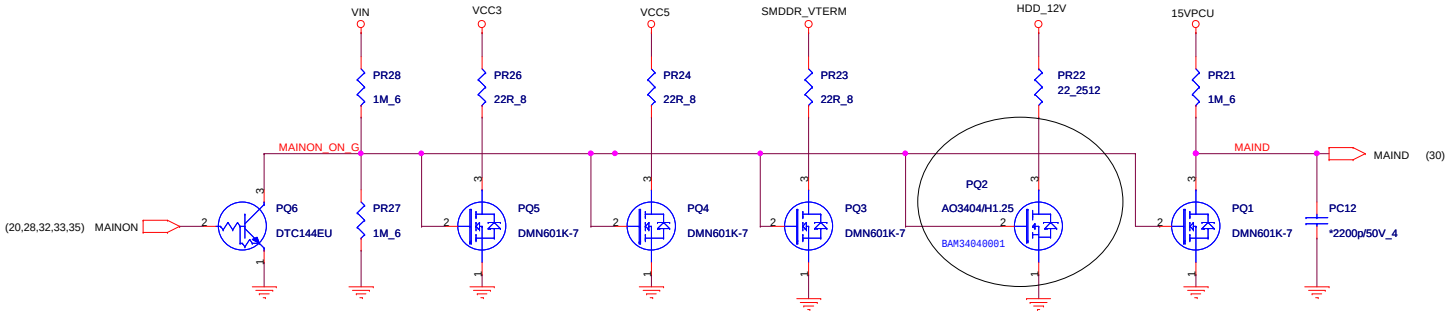








0526 Remove VCC1.8 and add HDD_12V discharge circuit

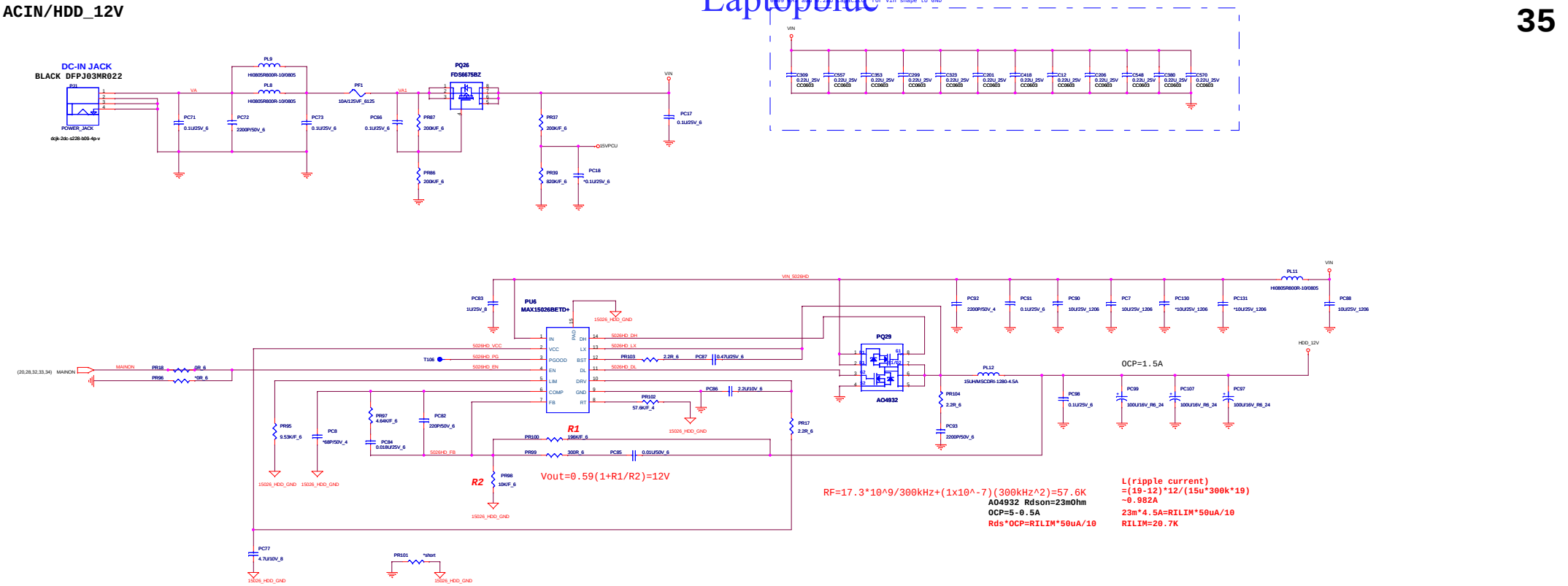


PROJECT : EL2

Quanta Computer Inc.

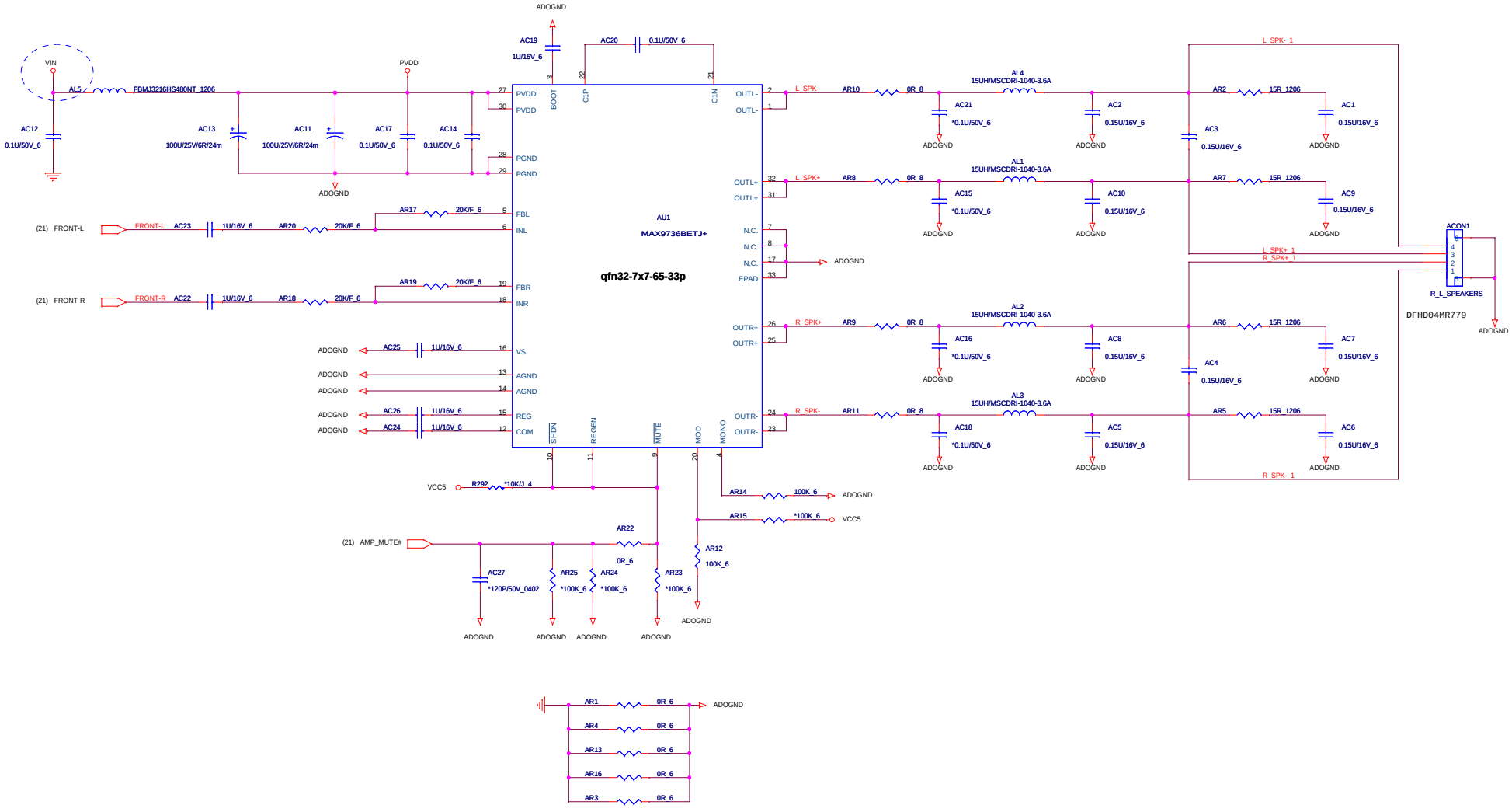
Size	Document Number	Rev
	Discharge (1.25V/1.5V)	1A

Date: Thursday, August 13, 2009 Sheet 34 of 40



PROJECT : EL2			
Quanta Computer Inc.			
Size	Document Number		Rev
	ACIN/ HDD_12V		1A
Date: Thursday, August 13, 2009		Sheet 35 of 40	

PROJECT :
Quanta Com



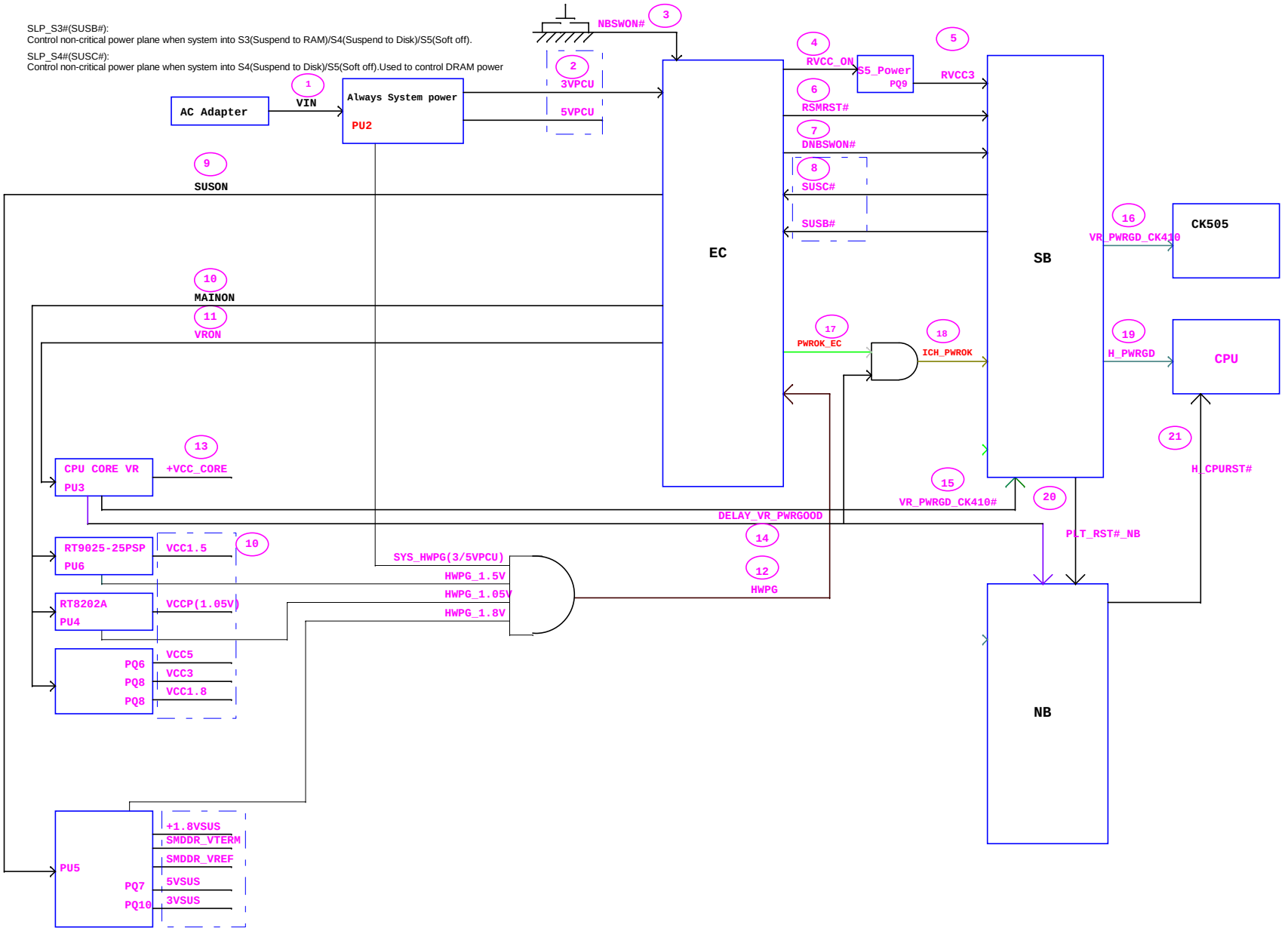
PROJECT : EL2

Quanta Computer Inc.

Size	Document Number	Rev
	Speaker AMP.	1A
Date: Thursday, August 13, 2009	Sheet 36 of 40	

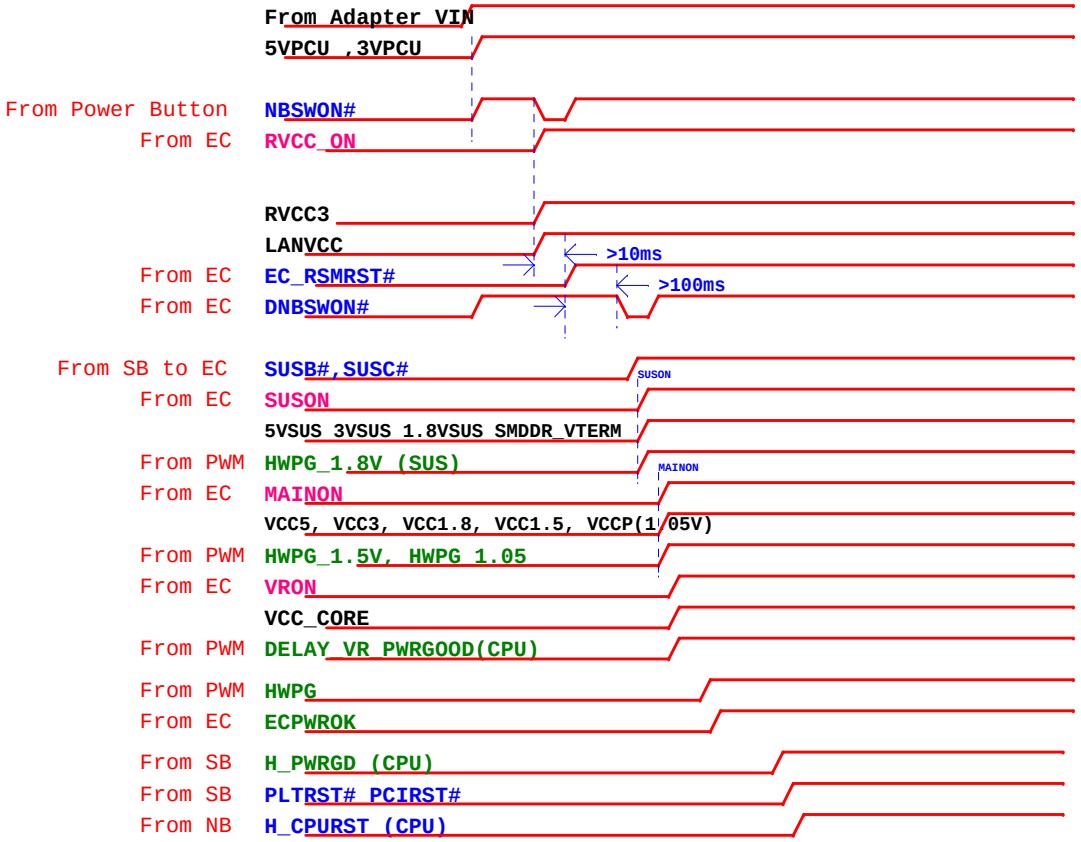
SLP_S3#(SUSB#):
Control non-critical power plane when system into S3(Suspend to RAM)/S4(Suspend to Disk)/S5(Soft off).

SLP_S4#(SUSC#):
Control non-critical power plane when system into S4(Suspend to Disk)/S5(Soft off).Used to control DRAM power



PROJECT : EL2
Quanta Computer Inc.
Power Sequence Diagram
Rev 1A
Thursday, August 13, 2009
Sheet 37 of 49

Power On Sequence



PROJECT : EL2

Quanta Computer Inc.

Size	Document Number	Rev
	Power Sequence Timing	1A

Date: Thursday, August 13, 2009 Sheet 38 of 40

When into B stage:
1. Change L34 to 0 ohm resistor (0805).
2. Change C293,C569 to 0.1U (CH41002X893).
3. C4,C6,C279 change to CH11006JB18.
4. Short R244, remove R245.
5. U12A need to reply right footprint for parts.

6. R305 SWI# pull high circuit remove.

1. Modify USB circuit:
   Change switch circuit to fuse circuit.
2. Change L34 to R467.
3. Modify IR circuit:
   Short R244, remove R245,
   Exchange CIR_TX1 and CIR_ED1signal.
4. Cahnge footprint for right size.
5. R305 SWI# pull high circuit remove.
6. Change +AZA_VDD from VCC3 to VCC1.5
7. Modify CN21 pin define.
8. Add HDD_12V discharge circuit and remove VCC1.8 discharge circuits.
9. Short R464.
10. Page 14, Add Model ID switch circuits
11. Remove page28 MID circuits.
12. Page 22 , Modify Line out circuit
13. Page 14, Delete R139, R135, C185. (SB)
14. Page 21, Delete D18. (Codec)
    Modify Head Phone and line out circuit.
15. Modify IR blaster circuit.

C stage:
1. Change SB HDA voltage from 1.5v to 3V, and Codec +AZA_VDD from 1.5v to 3v.
2. Remove R292, short AR21. (solve Speaker pop noise)
3. Add Buzzer circuit. (P.22)
4. Add LAN power control circuit. (P.34, P.23)
5. Modify FAN pin define.
6. Change Home button power from VCC3 to VCC5

RAMP stage:
1.Change CS64 to D45 (ESD solution).
2.Bluetooth power add 3VSUS power.
3.Add Mini PCIE device power select circuits.
4.Change Touch module power from VCC5 to 5VSUS.
5.Exchange SB USB port (Bluetooth and Side USB).
6.Add R380,R386 between ANT_GND to DGND.
7.Change Darlington circuit DGND to AGND, VCC3 change to +3V_AVDD.
8.Add short pad and short 0 ohm.
9.Add TV_ANT_GND to DGND circuit. (p18)
10.Add RVCC3 to LANVCC. (P23)

PROJECT : EL2
Quanta Computer Inc.
Document Number: Change List
Rev: 1A
Date: Monday, March 16, 2009 Sheet 39 of 45

PROJECT : EL2
Quanta Computer Inc.
Change List