

Redwood 11.6" Schematic Document

Bay Trail - M

2014-04-01

REV : A00

DY : None Installed

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Cover Page

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Document Number

Redwood 11.6"

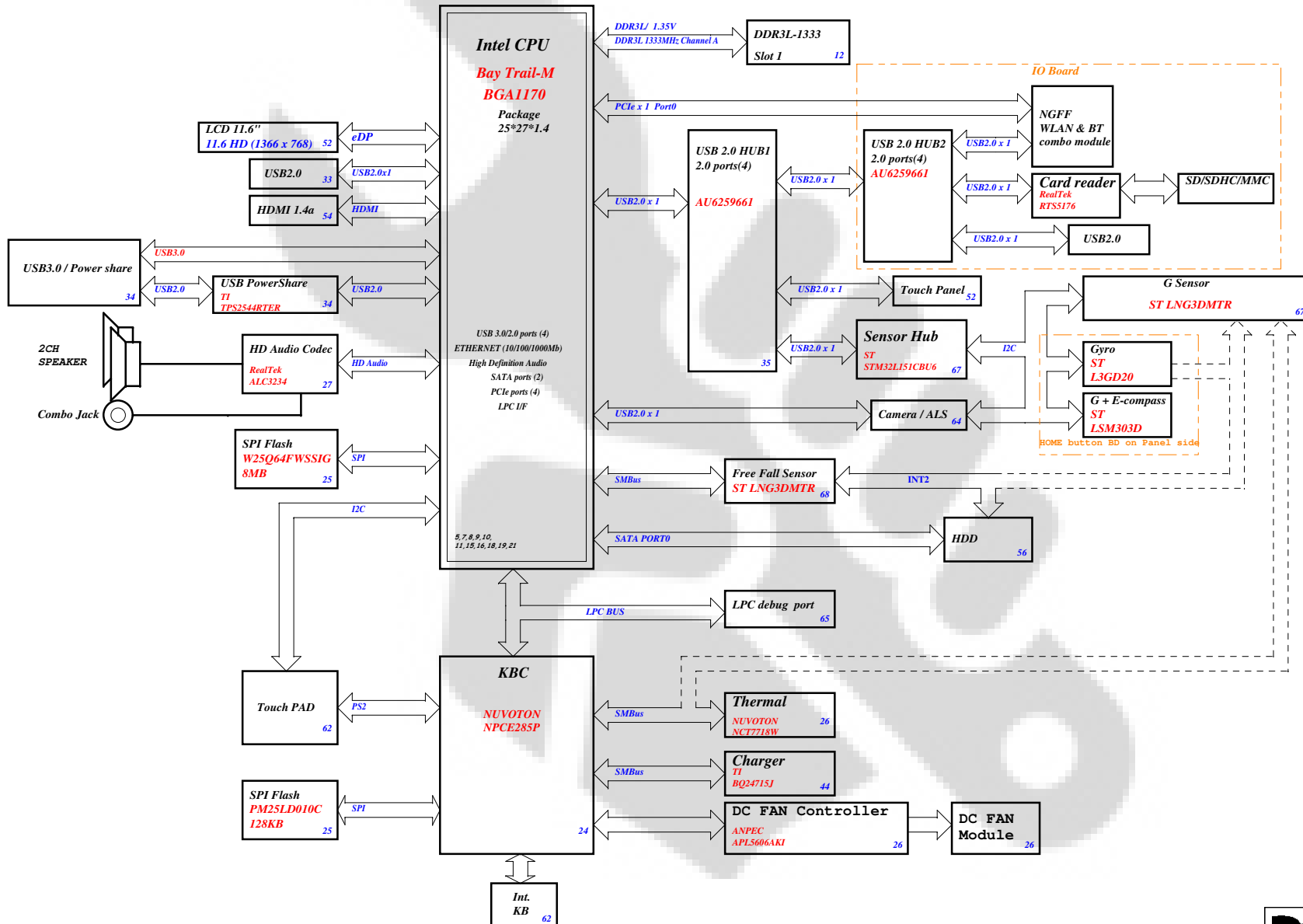
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Sheet 1 of 102

Redwood 11.6" Board Block Diagram

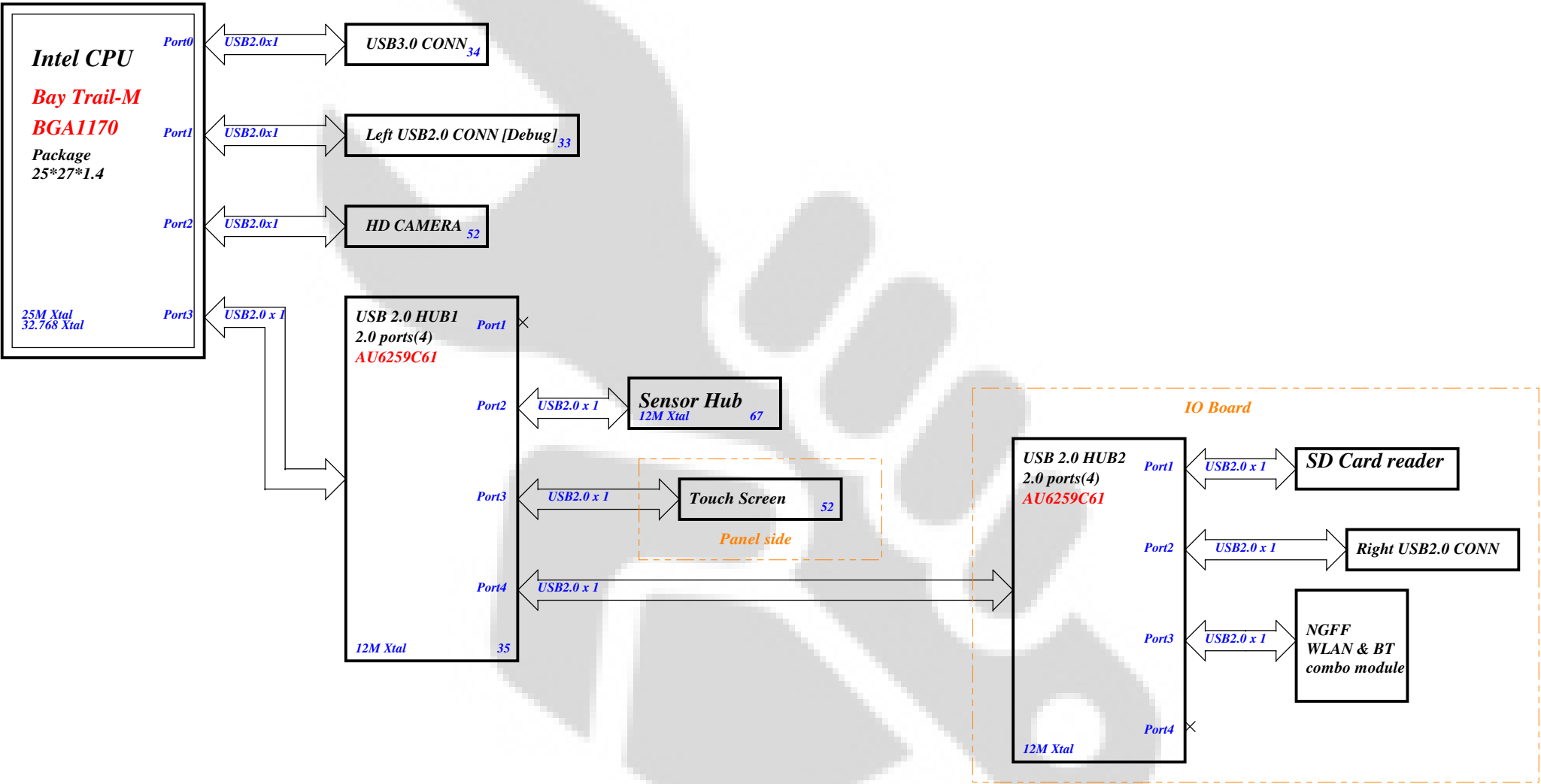
Project code : 4PD00K010001
PCB P/N : 13270
Revision : -1



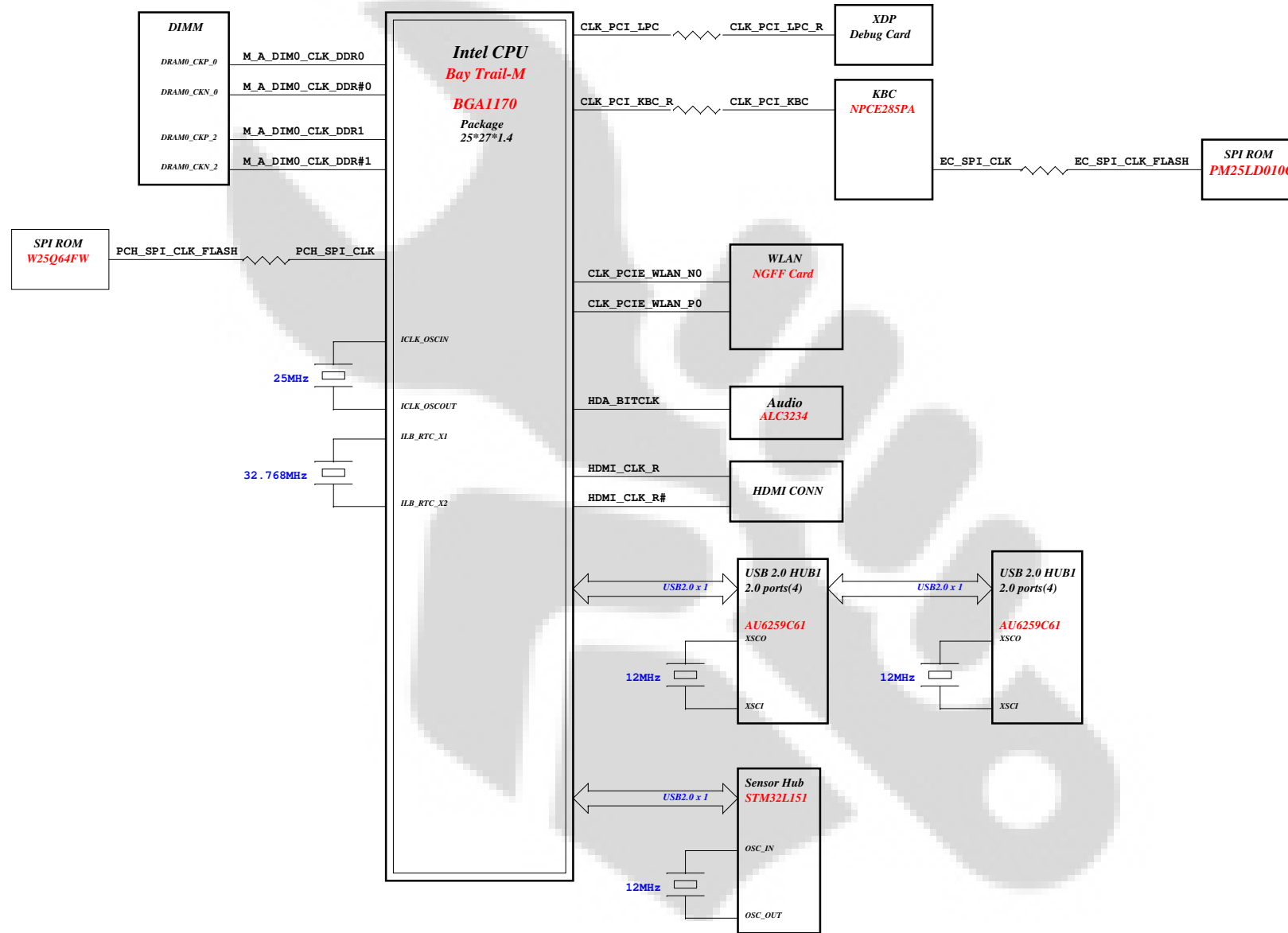
CHARGER	BQ24715J	44
INPUTS	OUTPUTS	
DCBATOUT	BT+	
SYSTEM DC/DC	TPS51225	45
INPUTS	OUTPUTS	
DCBATOUT	5V_S5	
DCBATOUT	3D3V_S5	
CPU DC/DC	ISL95833	46-47
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
SYSTEM DC/DC	SY8206	50
INPUTS	OUTPUTS	
DCBATOUT	1D0V_S5	
SYSTEM DC/DC	TPS51363	49
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3	
SYSTEM LDO	TLV70218	51
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	
SYSTEM LDO	TLV70218	51
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	
Step Down Regulator	SYW232	51
INPUTS	OUTPUTS	
1D0V_S0_P6	1D05V_S0	
LOAD SWITCH	TPS22966	37
INPUTS	OUTPUTS	
1D8V_S5	1D8V_S0	
LOAD SWITCH	TPS22965	37
INPUTS	OUTPUTS	
1D0V_S5	1D0V_S0	

PCB LAYER
L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

USB Port Block Diagram



Clock Block Diagram



SSID = CPU

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CPU (CFG)

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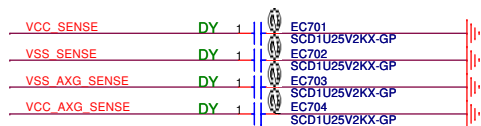
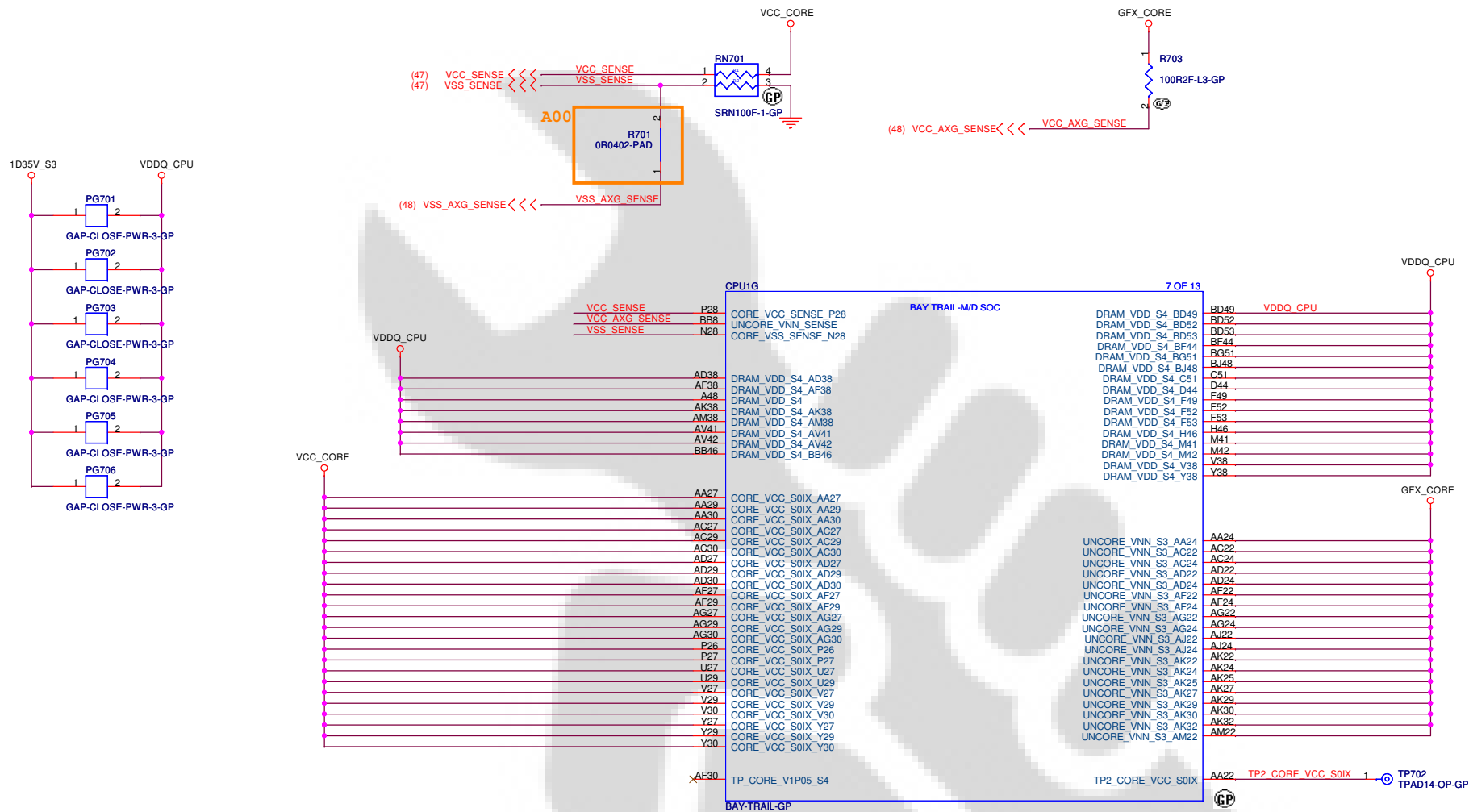
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Sheet 6 of 102

SSID = CPU



reserve the 0402 0.1u caps on reset for EMI.

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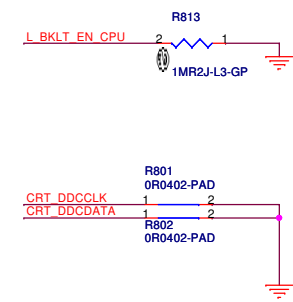
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Sheet 7 of 102

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SSID = CPU



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**CPU (DDI/EDP/GPIO)**

Rev

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Sheet 8 of 102

Sheet 8 of 102

SSID = CPU

CPU1I 9 OF 13		
BAY TRAIL-MD SOC		
A11	VSS1	AC36
A15	VSS2	AC38
A19	VSS3	AD19
A23	VSS4	AD21
A27	VSS5	AD25
A31	VSS6	AD32
A35	VSS7	AD33
A39	VSS8	AD7
A43	VSS9	AD7
A47	VSS10	AE1
AA1	VSS11	AE11
AA16	VSS12	AE12
AA19	VSS13	AE14
AA21	VSS14	AE3
AA3	VSS15	AE4
AA32	VSS16	AE40
AA35	VSS17	AE42
AA38	VSS18	AE43
AA53	VSS19	AE45
AB4	VSS20	AE48
AB41	VSS21	AE50
AB45	VSS22	AE51
AB47	VSS23	AE53
AB48	VSS24	AE6
AB50	VSS25	AE8
AB51	VSS26	AE9
AB6	VSS27	AE10
AC16	VSS28	AE12
AC18	VSS29	AF25
AC19	VSS30	AF32
AC21	VSS31	AF47
VSS32	VSS32	AG16
VSS33	VSS33	AG25
VSS34	VSS34	AG36
VSS35	VSS35	VSS70

CPU1J 10 OF 13		
BAY TRAIL-MD SOC		
AG38	VSS71	AH47
AH4	VSS72	AH48
AH41	VSS73	AH50
AH45	VSS74	AH51
AH7	VSS75	AH6
AH9	VSS76	AM44
AJ1	VSS77	AM51
AJ16	VSS78	AM7
AJ21	VSS79	AN1
AJ25	VSS80	AN11
AJ27	VSS81	AN12
AJ29	VSS82	AN14
AJ3	VSS83	AN22
AJ30	VSS84	AN3
AJ32	VSS85	AN33
AJ33	VSS86	AN35
AJ35	VSS87	AN36
AJ38	VSS88	AN38
AJ53	VSS89	AN40
AK10	VSS90	AN42
AK14	VSS91	AN43
AK16	VSS92	AN45
AK33	VSS93	AN46
AK41	VSS94	AN48
AK44	VSS95	AN49
AM12	VSS96	AN5
AM19	VSS97	AN51
AM24	VSS98	AN53
AM25	VSS99	AN6
AM29	VSS100	AN8
AM33	VSS101	AN9
AM35	VSS102	AP40
AM36	VSS103	AT12
AM40	VSS104	AT16
M28	VSS105	AT19

CPU1K 11 OF 13		
BAY TRAIL-MD SOC		
AT24	VSS141	AY36
AT27	VSS142	AY4
AT30	VSS143	AY50
AT35	VSS144	AY9
AT38	VSS145	BA14
AT4	VSS146	BA19
AT47	VSS147	BA22
AT52	VSS148	BA27
AU1	VSS149	BA32
AU24	VSS150	BA35
AU3	VSS151	BA40
AU30	VSS152	BA53
AU38	VSS153	BB19
AU51	VSS154	BB27
AV12	VSS155	BB35
AV13	VSS156	BC20
AV14	VSS157	BC22
AV18	VSS158	BC26
AV19	VSS159	BC28
AV24	VSS160	BC32
AV27	VSS161	BC34
AV30	VSS162	BC42
AV35	VSS163	BD19
AV38	VSS164	BD24
AV47	VSS165	BD27
AV51	VSS166	BD30
AV7	VSS167	BD35
AW13	VSS168	BE19
AW19	VSS169	BE2
AW8	VSS170	BE35
AW27	VSS171	BE8
AW35	VSS172	BF12
AW10	VSS173	BF16
AY22	VSS174	BF24
AY32	VSS175	BF38

CPU1L 12 OF 13		
BAY TRAIL-MD SOC		
BF30	VSS211	E8
BF36	VSS212	F19
BF4	VSS213	F2
BG31	VSS214	F27
BG34	VSS215	F30
BG39	VSS216	F35
BG42	VSS217	F5
BG45	VSS218	F7
BG49	VSS219	G10
BJ11	VSS220	G20
BJ15	VSS221	G22
BJ19	VSS222	G26
BJ23	VSS223	G28
BJ27	VSS224	G32
BJ31	VSS225	G34
BJ35	VSS226	G42
BJ39	VSS227	H19
BJ43	VSS228	H27
BJ7	VSS229	H35
C14	VSS230	J1
C31	VSS231	J16
C34	VSS232	J19
C39	VSS233	J22
C42	VSS234	J27
C45	VSS235	J32
C49	VSS236	J35
D12	VSS237	J40
D16	VSS238	J53
D24	VSS239	K14
D30	VSS240	K22
D36	VSS241	K32
D38	VSS242	K36
E19	VSS243	K4
E35	VSS244	K50
VSS245	VSS245	VSS280

CPU1M 13 OF 13		
BAY TRAIL-MD SOC		
K9	VSS261	U3
L13	VSS262	U30
L19	VSS263	U32
L27	VSS264	U38
L35	VSS265	U40
M19	VSS266	U42
M26	VSS267	U43
M27	VSS268	U45
M34	VSS269	U46
M35	VSS270	U48
M38	VSS271	U49
M47	VSS272	U5
M51	VSS273	U51
N1	VSS274	U53
N16	VSS275	U6
N38	VSS276	U8
N51	VSS277	U9
P13	VSS278	V12
P16	VSS279	V16
P19	VSS280	V19
P20	VSS281	V21
P24	VSS282	V35
P32	VSS283	V40
P35	VSS284	V44
P38	VSS285	V51
P4	VSS286	V7
P47	VSS287	V10
P52	VSS288	V14
P9	VSS289	V16
T40	VSS290	V25
U1	VSS291	V33
U11	VSS292	V34
U12	VSS293	V44
U14	VSS294	V7
U21	VSS295	V9
VSS316	VSS316	VSS350

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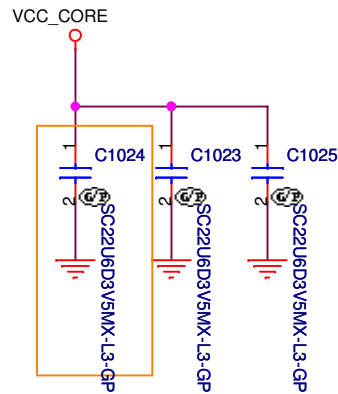
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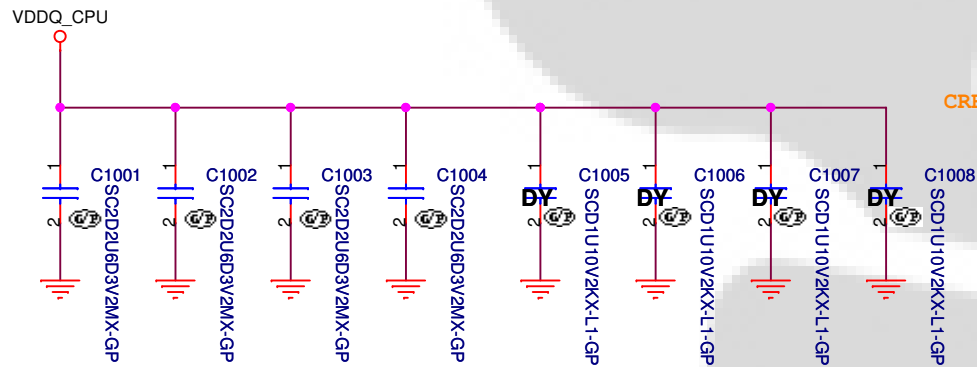
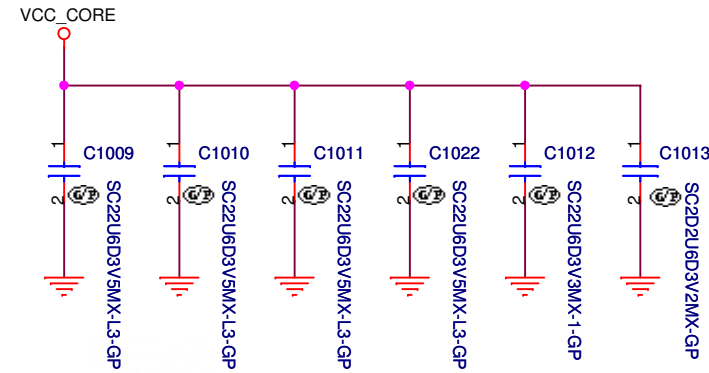
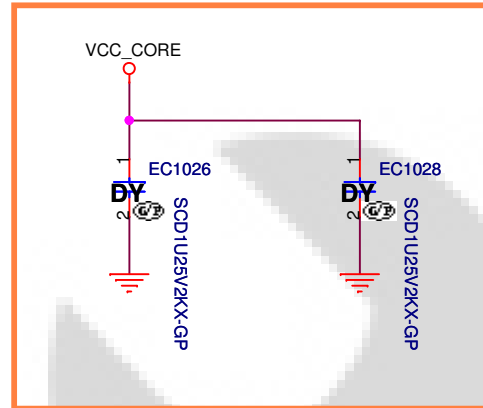
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Redwood 11.6"		
Date: Tuesday, April 01, 2014	Sheet 9 of 102	

reserve the 0402 0.1u caps on reset for EMI.

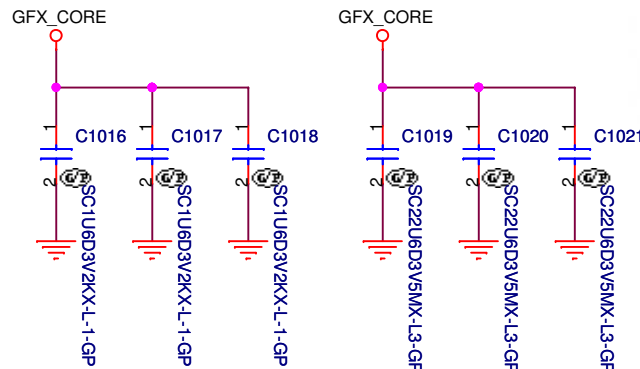
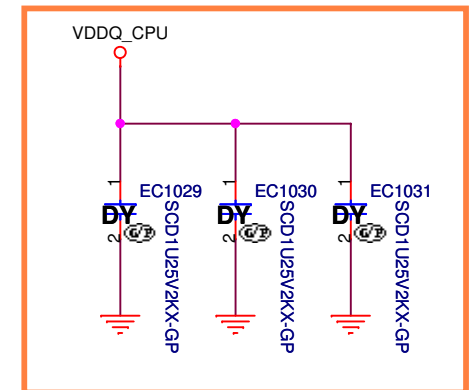
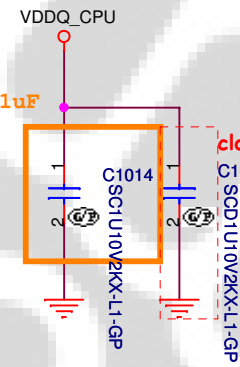


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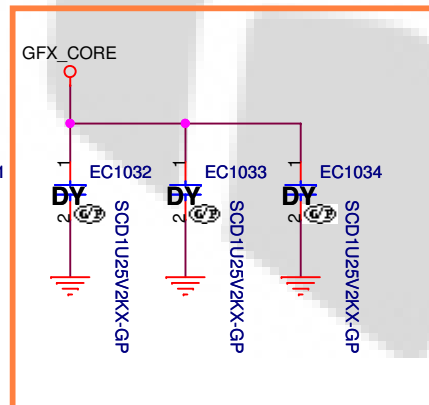


CRB放1uF

close to pin AD38 & AF38



reserve the 0402 0.1u caps on reset for EMI.



reserve the 0402 0.1u caps on reset for EMI.

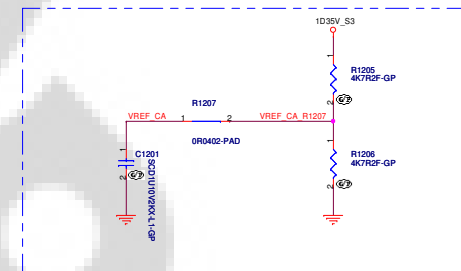
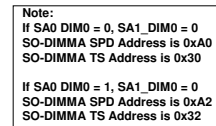
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Rev

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Date:

Tuesday, April 01, 2014

Sheet

13

of

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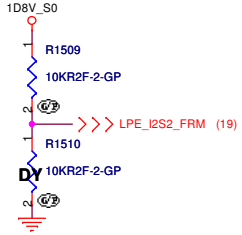
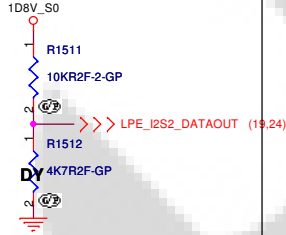
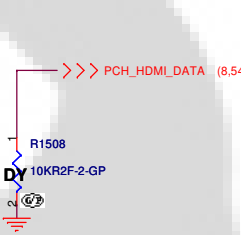
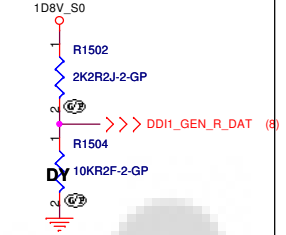
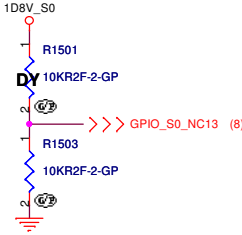
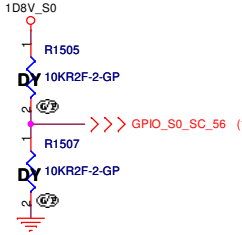
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Sheet 14 of 102

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

EDS_Revlp5 define the strap removed for MDSI P.21

Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI	Normal Operation	DDI0 detected	DDI1 detected	DDI1 detected	
Low	LPC	Override	DDI0 not detected	DDI1 not detected	DDI1 not detected	

2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

30.2 LPE_I2S2_DATAOUT/ GPIO_S0_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO_S0_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

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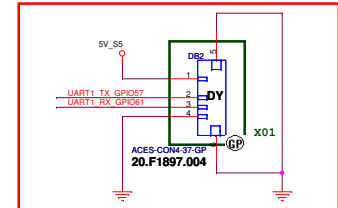
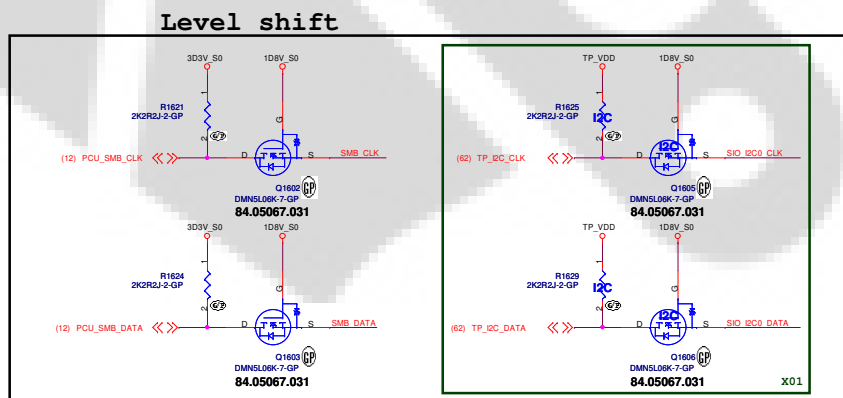
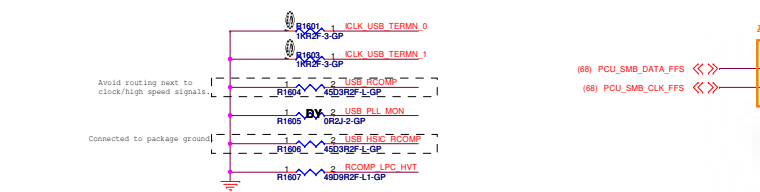
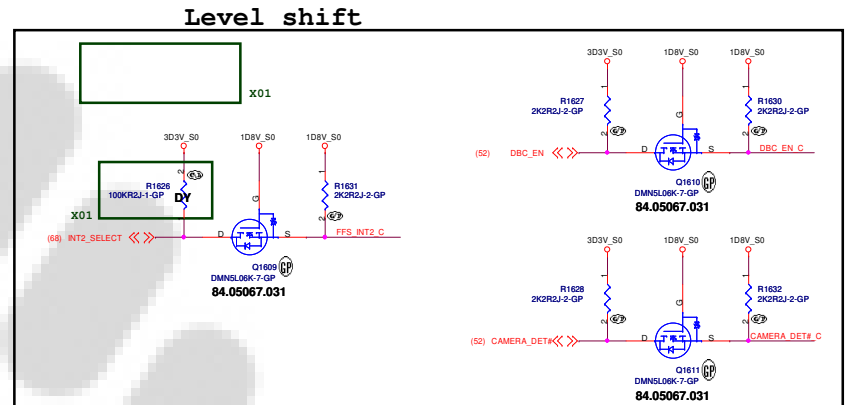
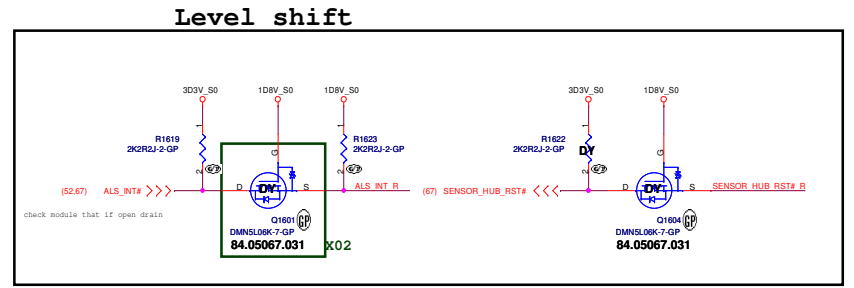
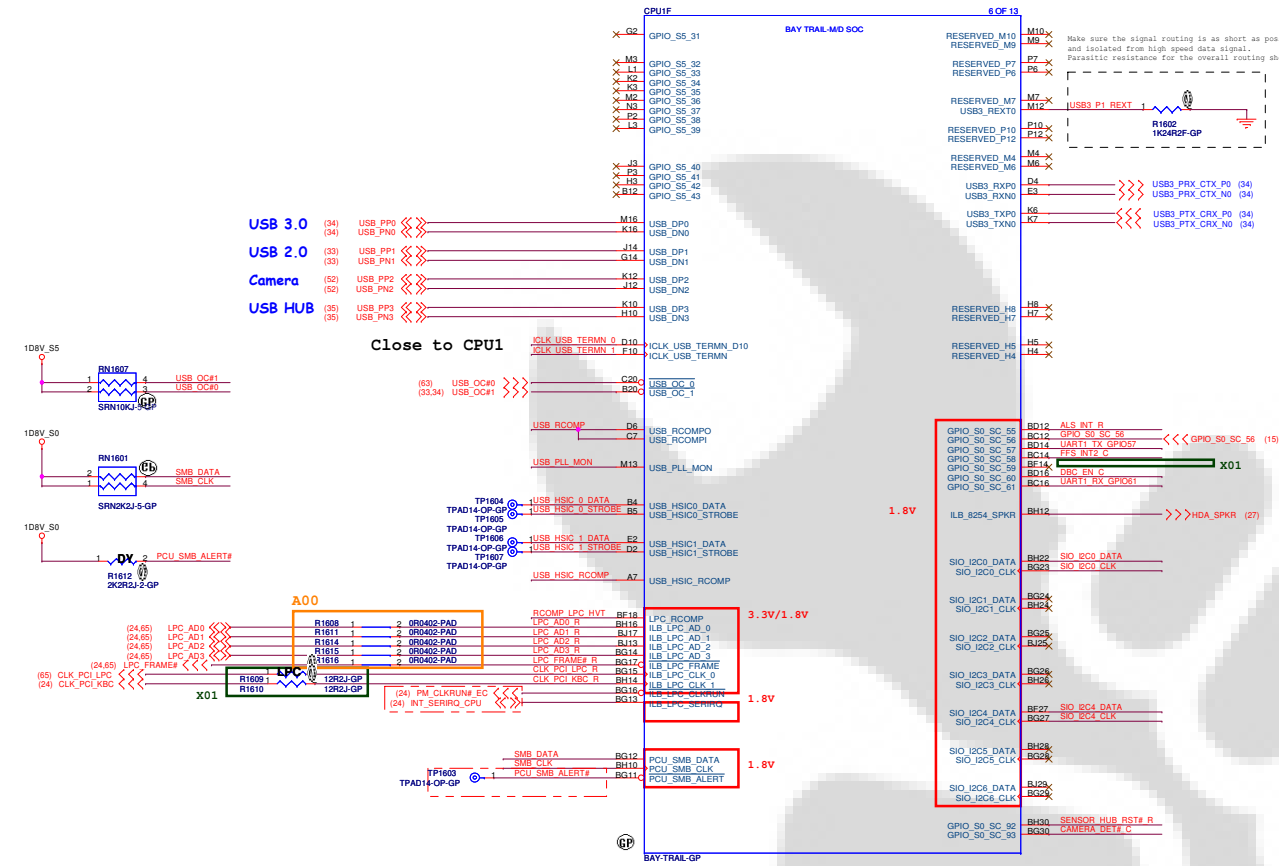
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Size A3 Document Number: **Redwood 11.6"** Rev: **A00**

Date: Tuesday, April 01, 2014 Sheet 15 of 102

SSID = PCH



Port		Type	Device	Address (Write/Read)
PCH	SMB_CLK/SMB_DATA	Master	Touch pad	0x58 / 0x59
			SODIMM	0xA0
			Free Fall Sensor	0x32 / 0x33

$$\text{VGS (th)} = 1\text{V}$$

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Size	Document Number
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Date	Rev
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SSID = PCH

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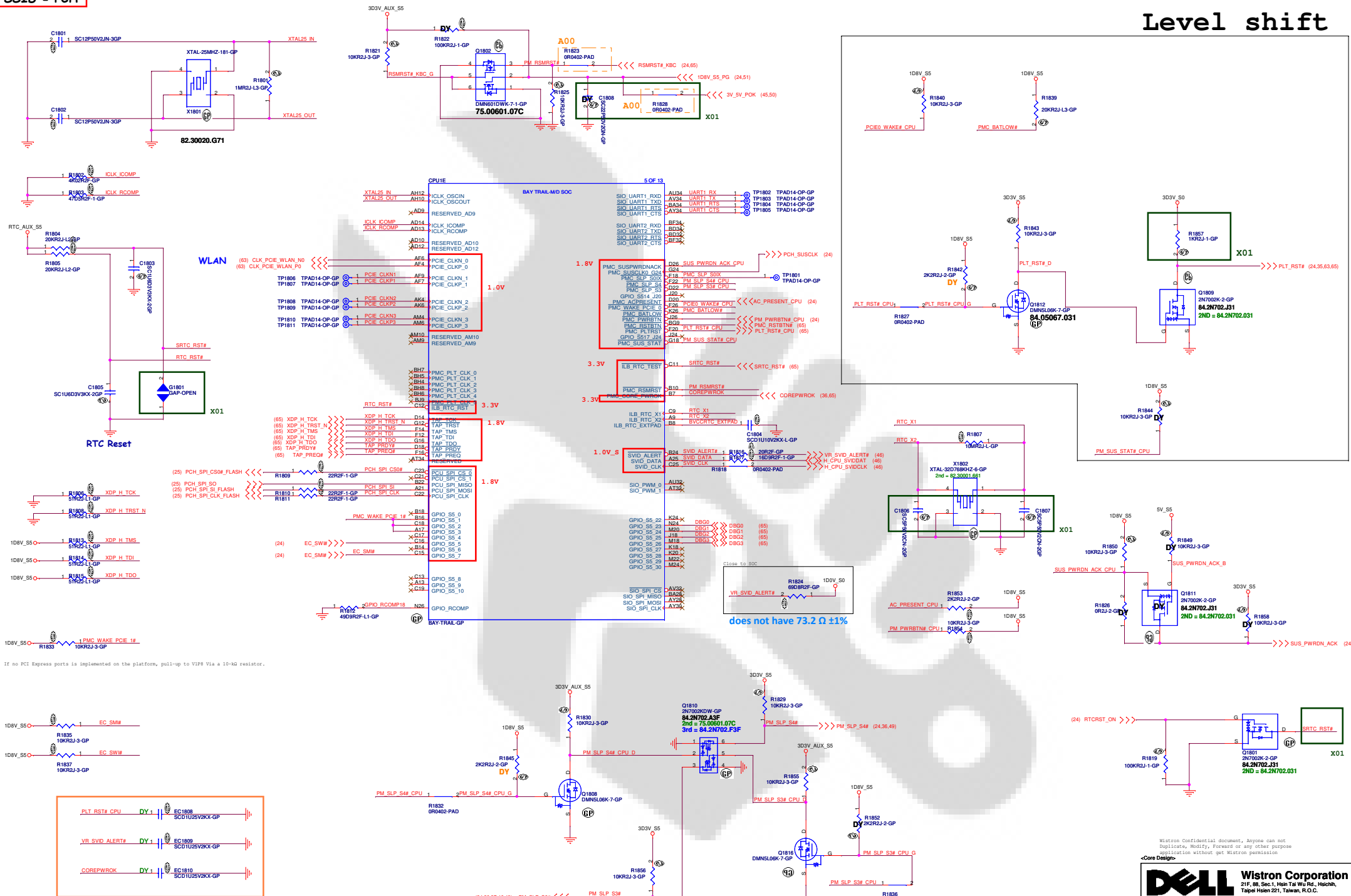
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CPU (DMI/FDI/PM)			
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Date: Tuesday, April 01, 2014		Sheet 17 of	102

SSID = PCH

Level shift



reserve the 0402 0.1u caps on reset for EMI

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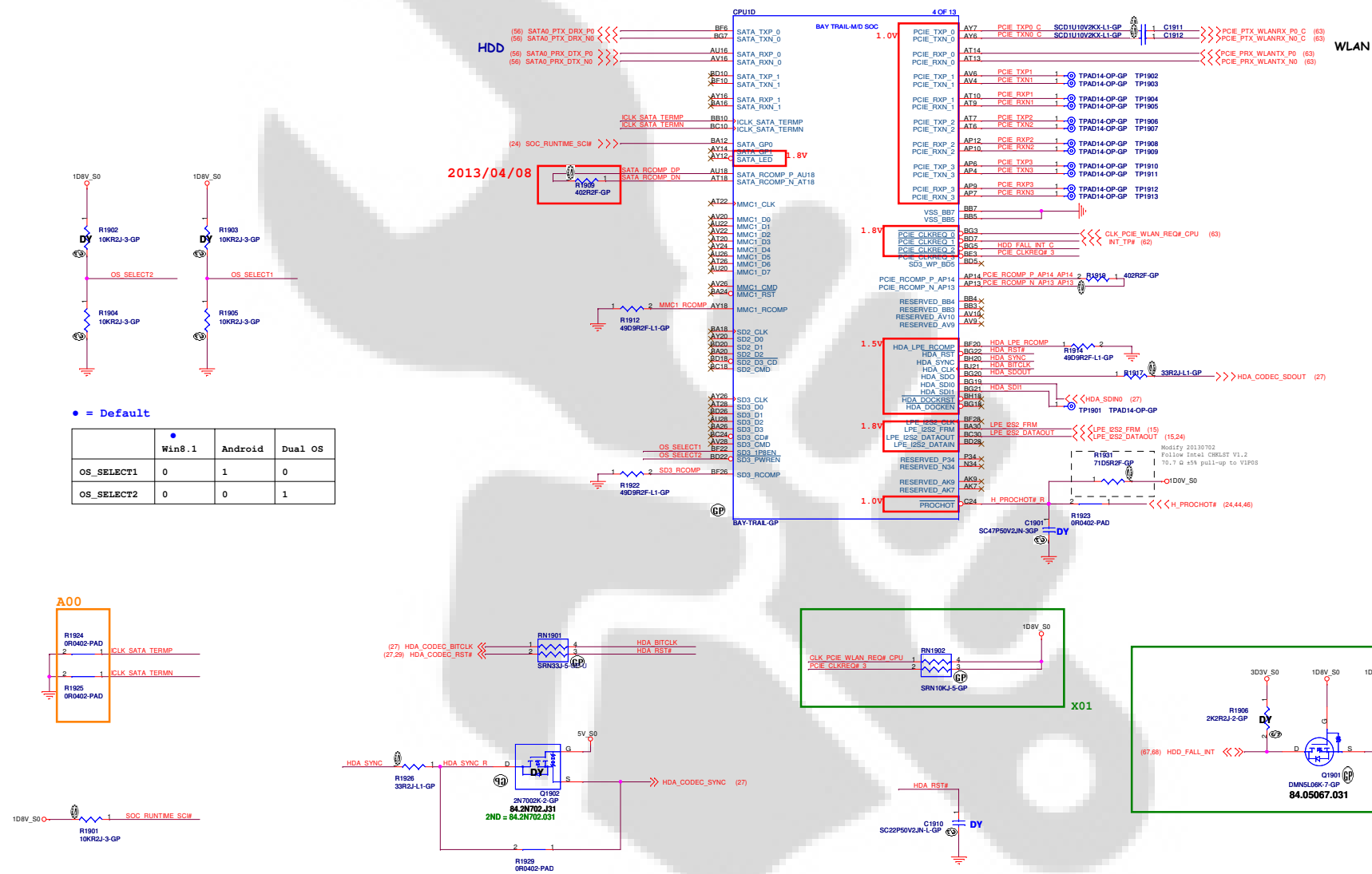
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CPU (CLK/SPI/SIDEBAND/JTAG)			
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Redwood 11.6"		A00	
Date:	ISSUED: April 01, 2014	Sheet	18 of 102

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SSID = PCH




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Size A2	Document Number	Rev	AA0
<p>Redwood 11.6"</p>		Sheet	19 of 192
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SSID = PCH

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Sheet 20 of 102

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Sheet 22 of 102

SSID = PCH

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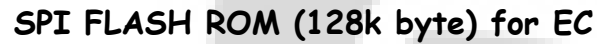
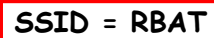
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Title		
CPU (VSS)		
Size A4	Document Number	Rev A00
Date: Tuesday, April 01, 2014		Sheet 23 of 102

SPI FLASH ROM (8M byte) for PCH

[illegible]

Title			
Flash(KBC+PCH)/RTC			
Size A3	Document Number		Rev
	Redwood 11.6"		A00
Date:	Tuesday, April 01, 2014	Sheet 25 of	102

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Sheet 28 of 102

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Rev
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Date: Tuesday, April 01, 2014

Sheet 30 of 102

SSID = LAN

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Title Reserved			
Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014	Sheet	31	of 102

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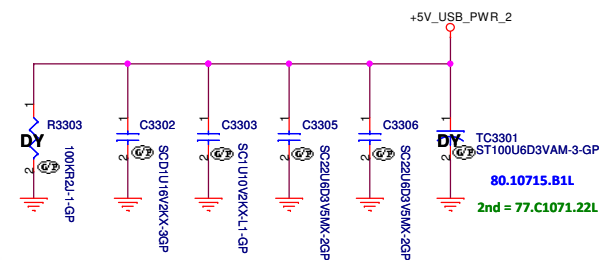
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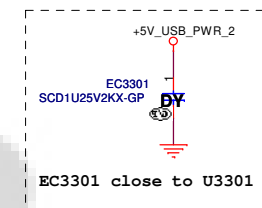


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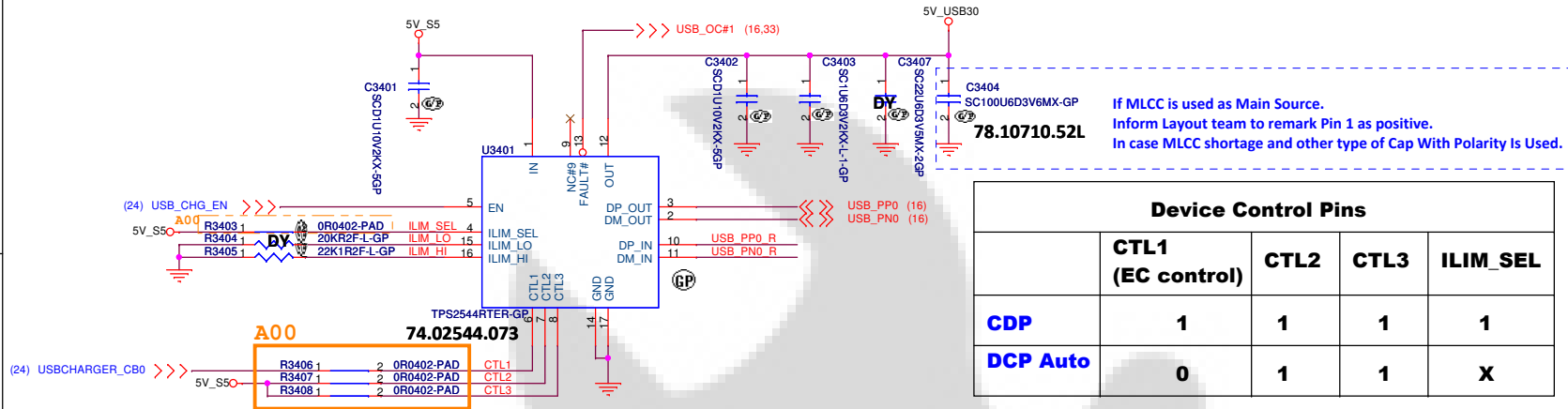
Title			Reserved		
Size	Document Number				Rev
A4	Redwood 11.6"				A00
Date:	Tuesday, April 01, 2014			Sheet 32 of 102	



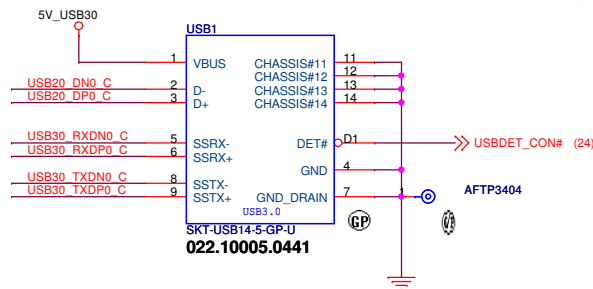
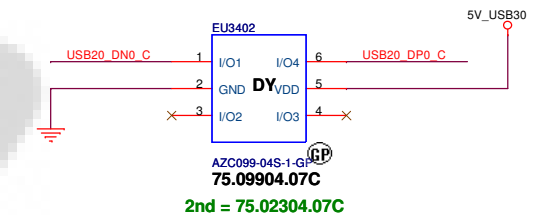
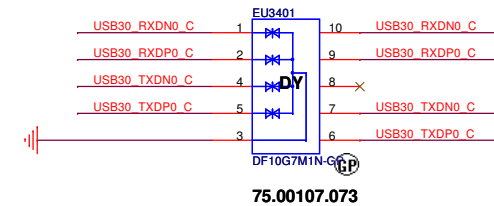
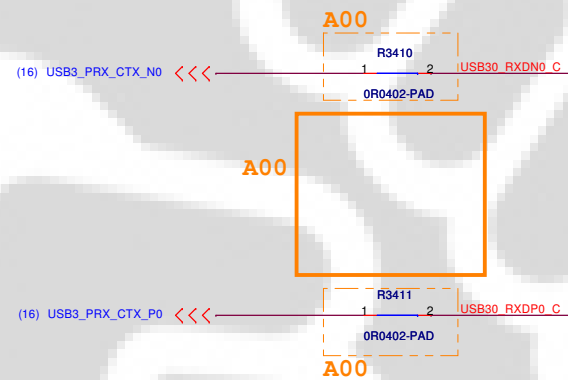
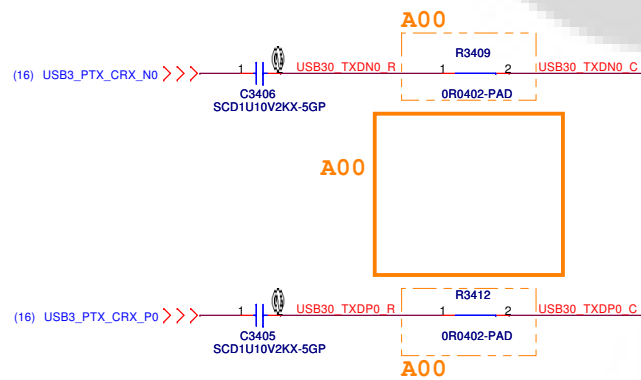
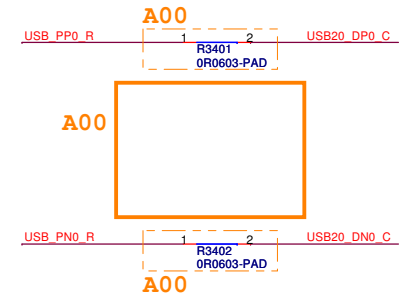
Vendor	Vendor P/N	Wistron P/N	Priority	Rate current
SILERGY	SY6288DAAC	074.06288.009B	1ST	2A Low Active
GMT	G524B2T11U	074.00524.0C9F	2ND	2.5A Low Active



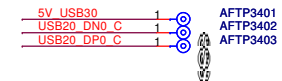
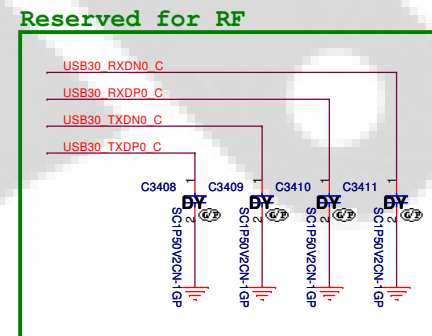
USB Charger



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X



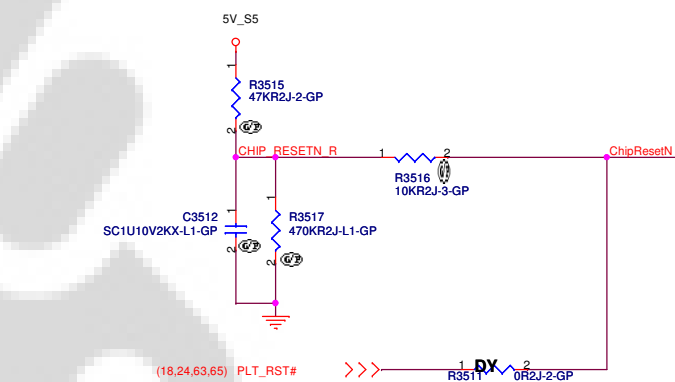
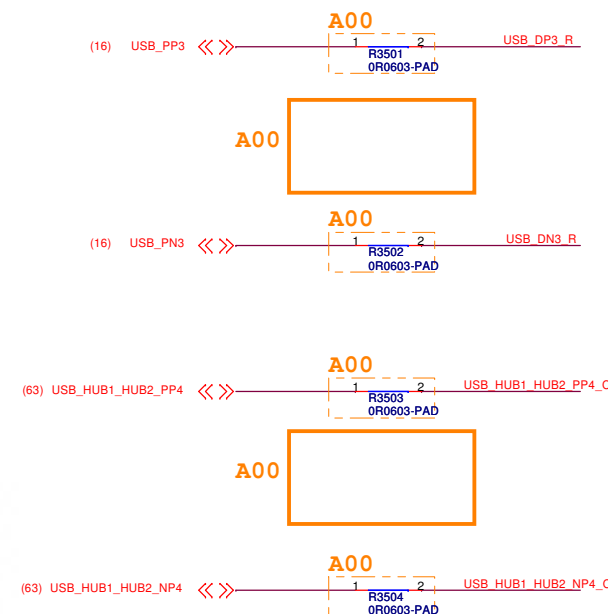
USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	



<Core Design>



Title			
USB power share / 3.0 Port			
Size A3	Document Number		Rev
	Redwood 11.6"		A00
Date:	Tuesday, April 01, 2014	Sheet 34 of	102

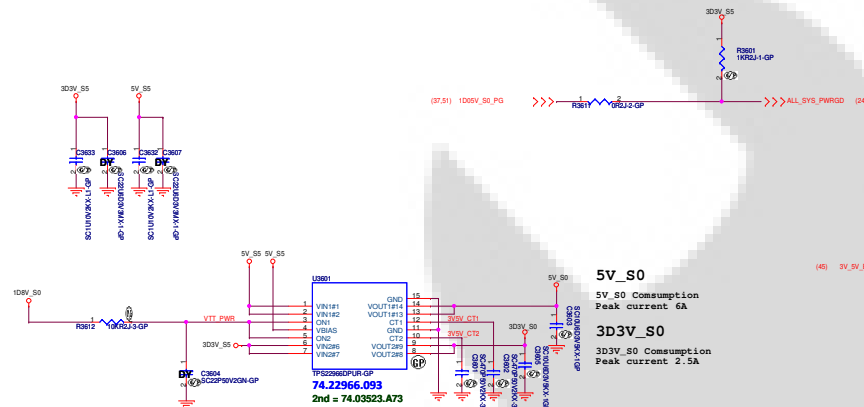


Pair	Device
1	N/A
2	Sensor Hub
3	TOUCH PANEL
4	USB Hub2

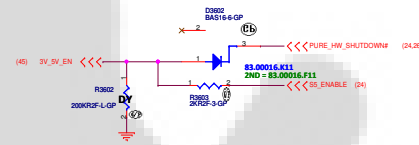
A00

```
SSID = Reset.Suspend
```

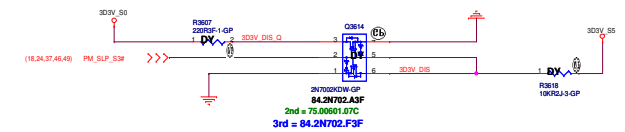
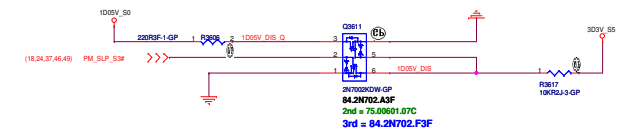
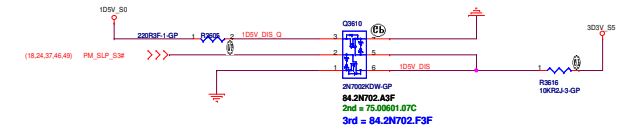
ROSA Run Power



Power Good

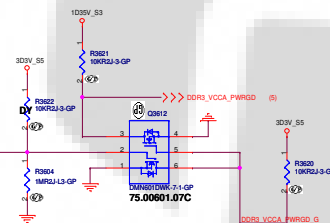
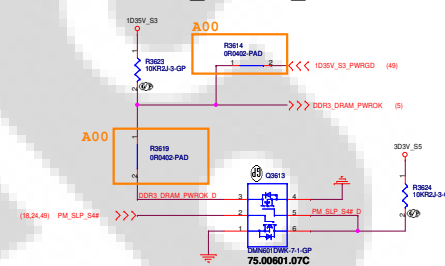


Discharge circuit



Power Sequence

DDR3_VCCA_PWRGD

**DDR3_DRAM_PWROK**

Does not link to SOC!!

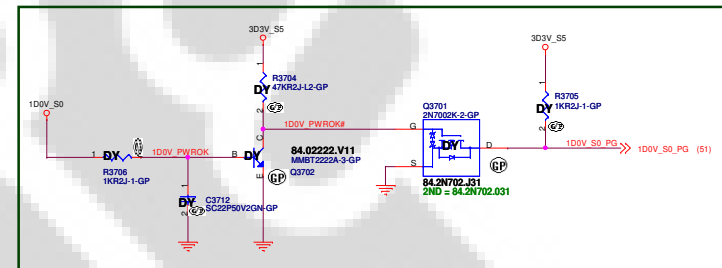
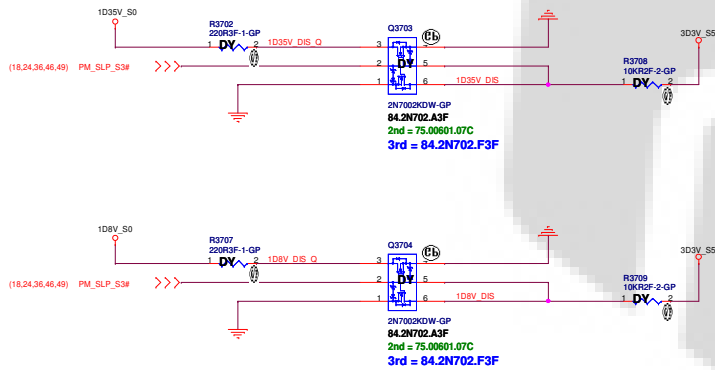
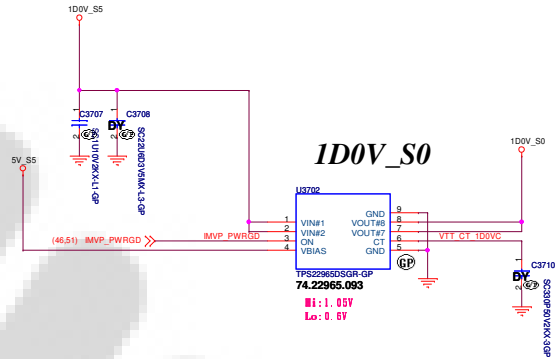
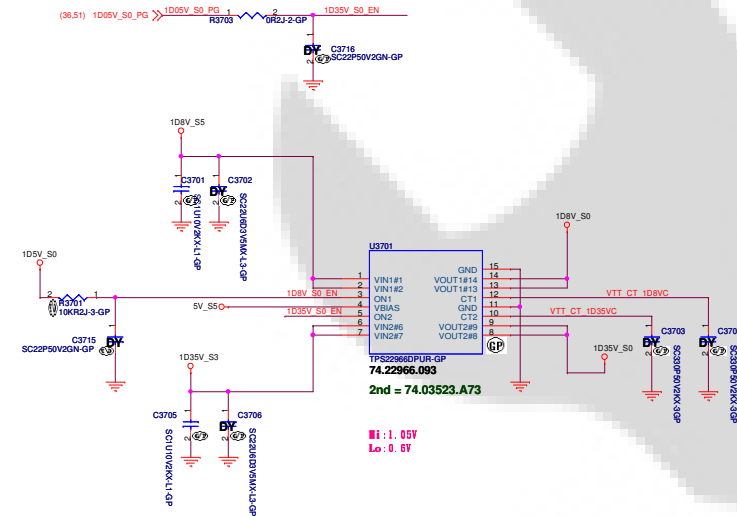
Delay 110ms with ALL_SYS_PWRGO

From EC

20130507
KBC GPIO77
delay ??? total
need KBC to modify!!!

COREPWROK

1D35V_S0 1D8V_S0



X01

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Title ADAPTER OCP / S3 reduction			
Size A2	Document Number Redwood 11.6"	Rev A00	
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Redwood 11.6"

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Title Reserved			
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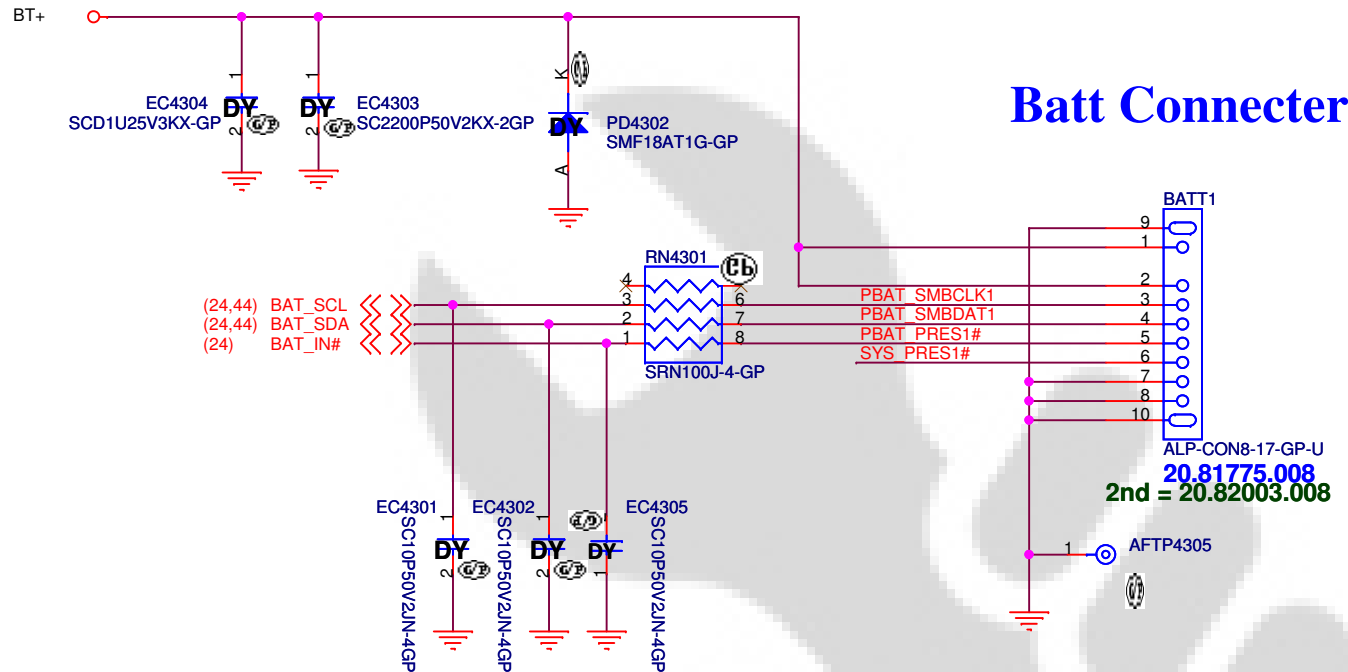
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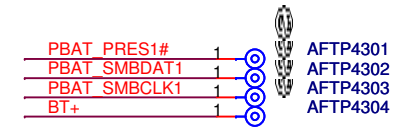
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Title Reserved			
Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014	Sheet	41	of 102

SSID = PWR.Support

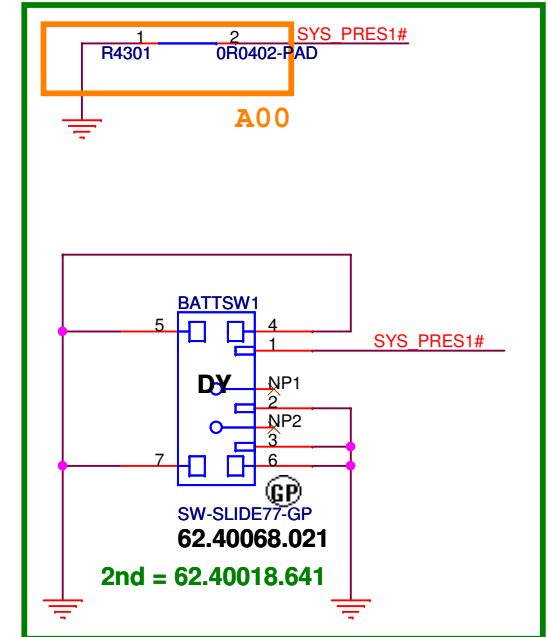


Batt Connector



Placement: Close to Batt Connector

X02



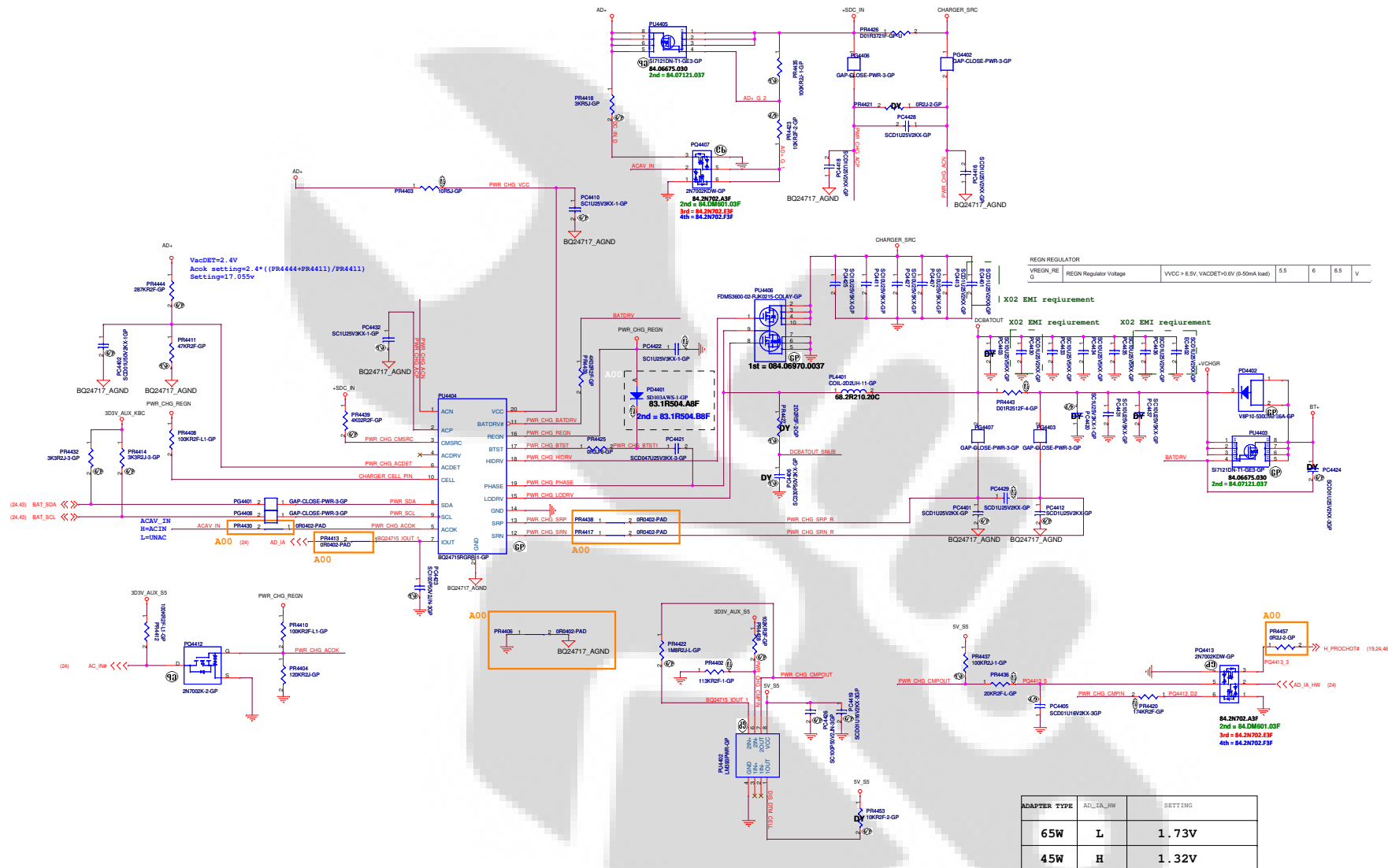
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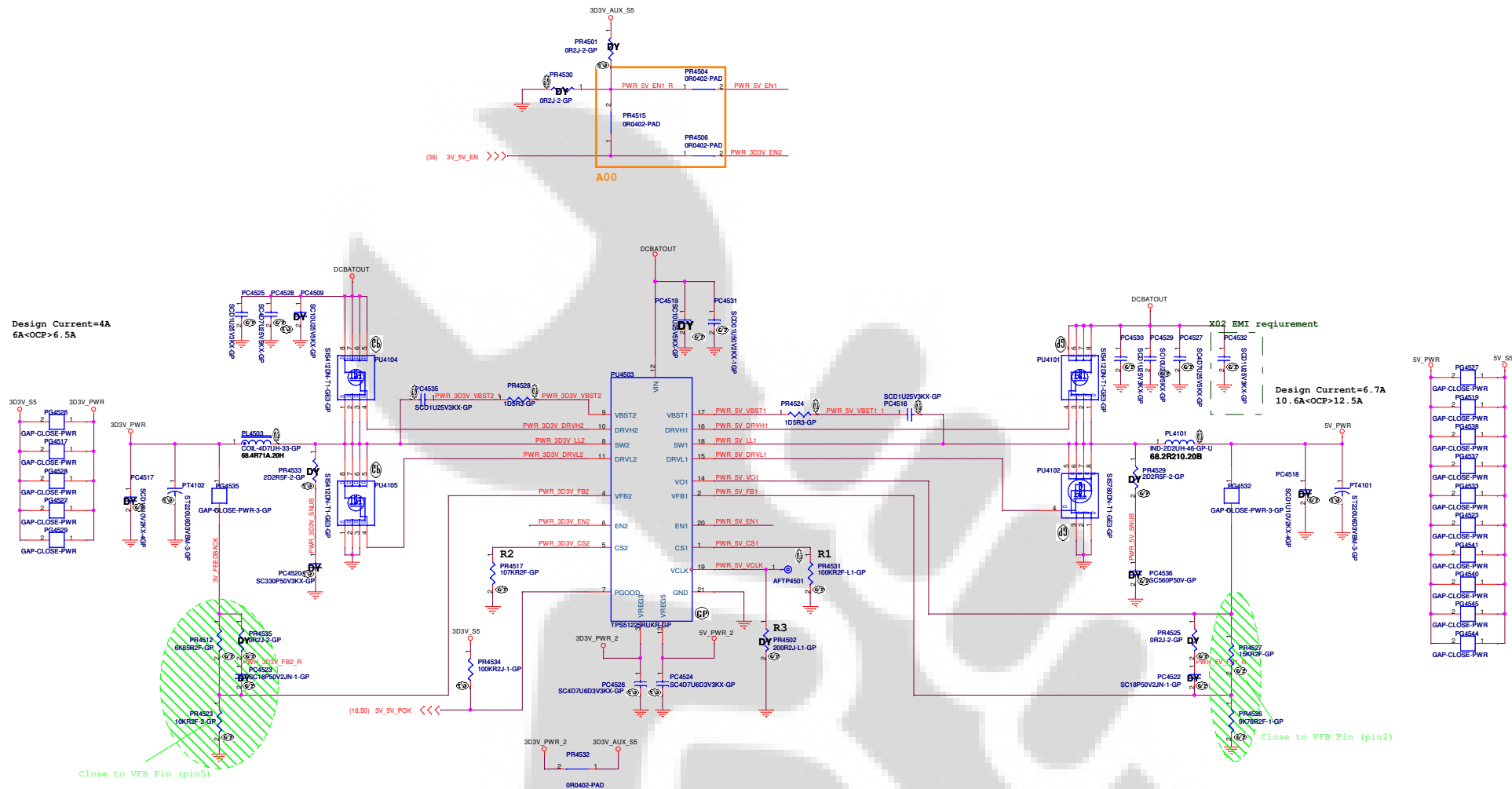


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Title			BATT CONN		
Size	Document Number				Rev
A4	Redwood 11.6"				A00
Date:	Tuesday, April 01, 2014		Sheet	43	of 102



```
SSID = PWR.Plane.Regulator_5v3p3v
```



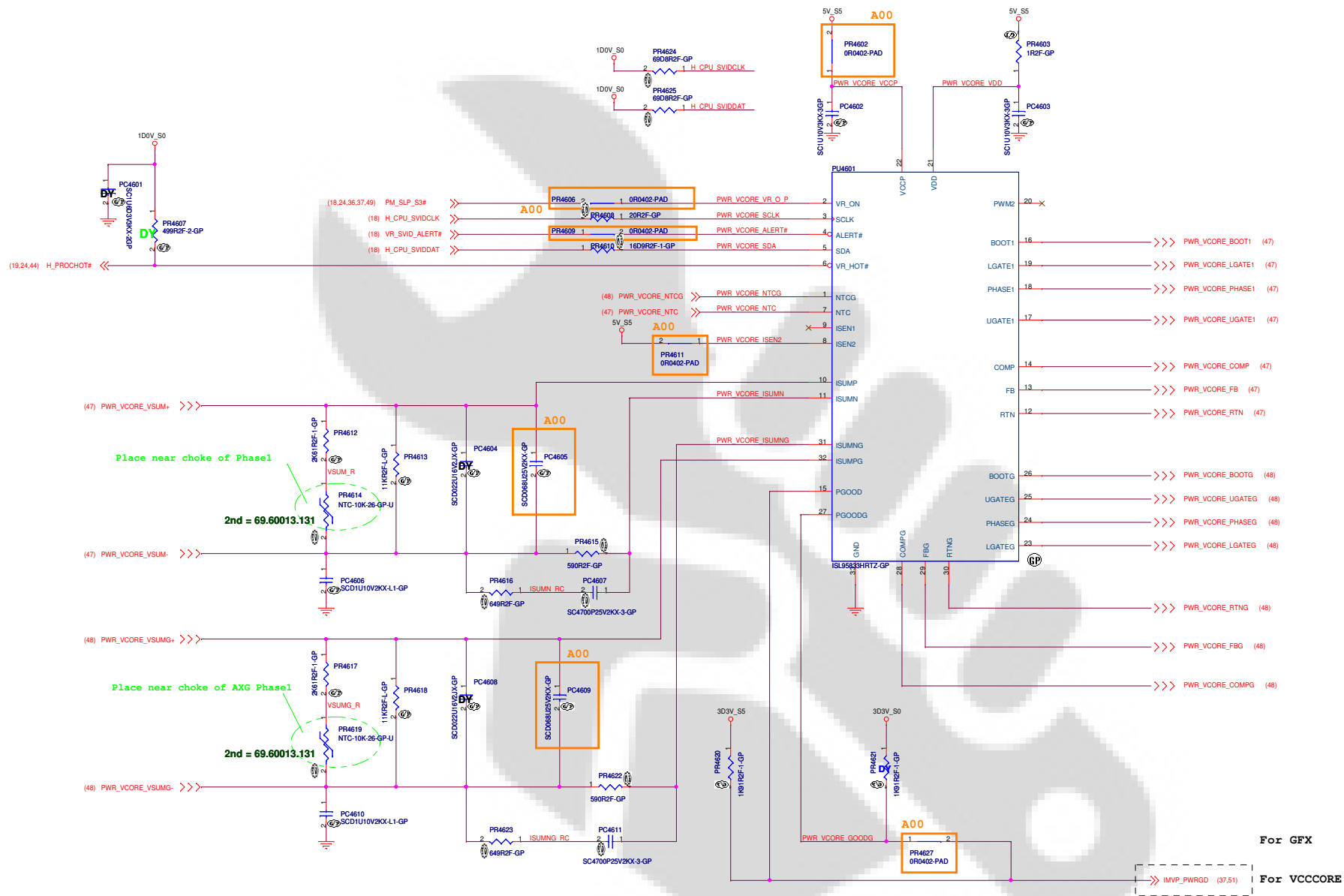
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 4.7UH PCB0603T-4R7MS Cyntec 28mhm/33mhm Isat =6.5Arms 68.4R71A.20H
O/P cap:CHIP CAP T 220U 6.3V M3528 PSL /NEC/ 28mhm / 77.C2271.45L
R/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.0412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.0412.037

TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
R1	100K	20K
R2	107K	21.5K
R3	DY	200

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U FCMC063T-2R2M 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP T 220 6.3V M3528 PSL /NEC/ 25mOhm / 77.C271.45L
L/S:SI5412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
H/S:SI5780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00708.037

SSID = CPU.Regulator



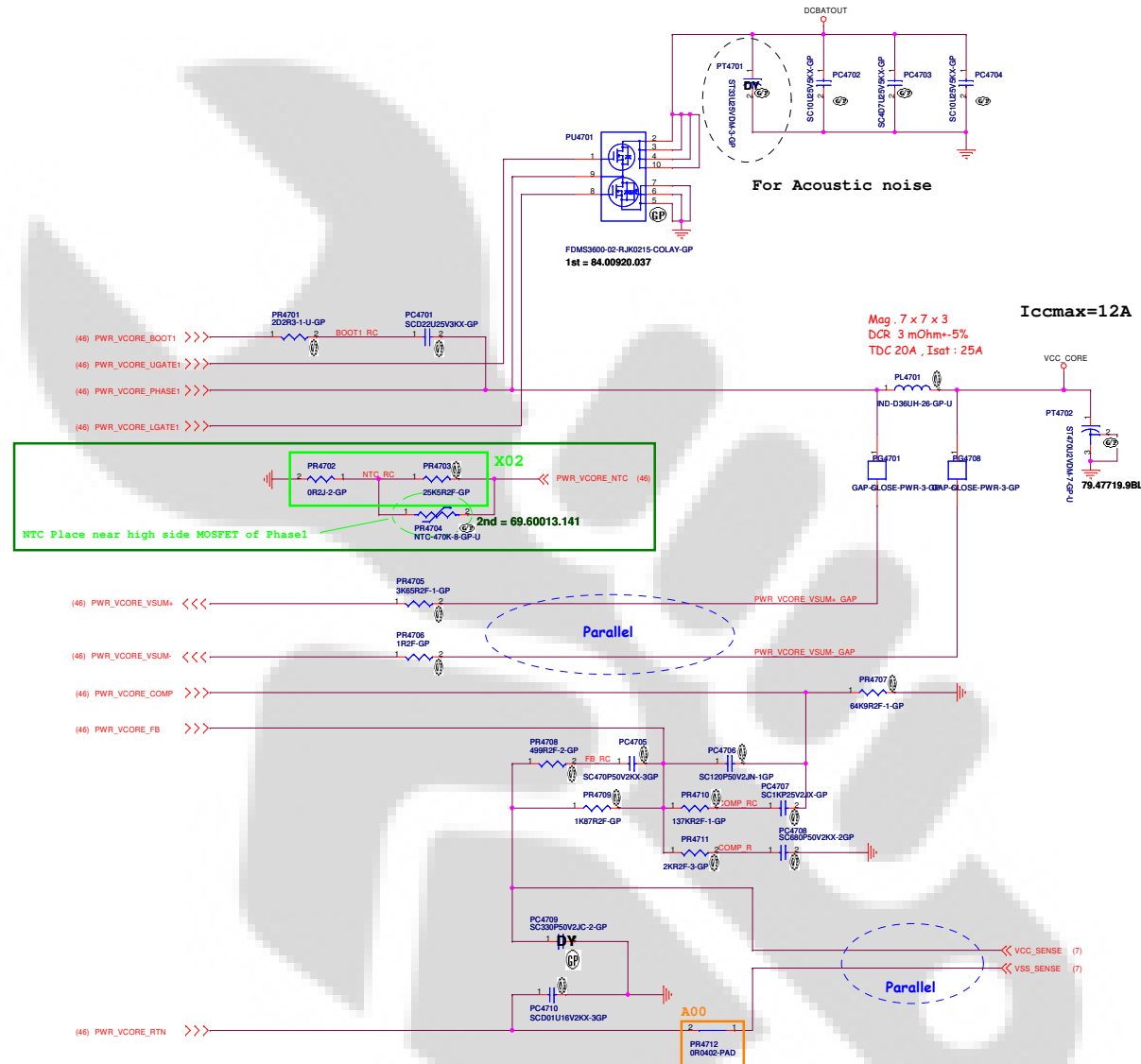
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File **ISL95833 CPUCORE(1/3)**

Size C	Document Number Redwood 11.6"	Rev A
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Date: Tuesday, April 01, 2014 Sheet 46 of 102

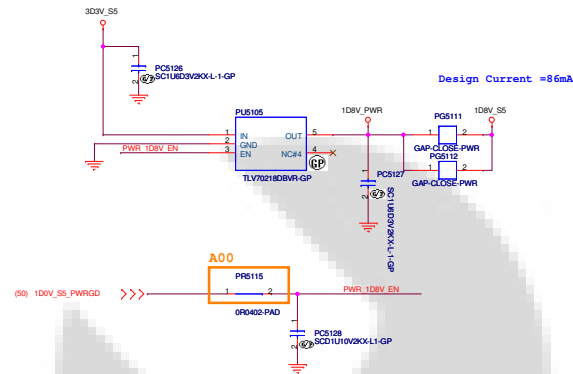


www.vinafix.vn

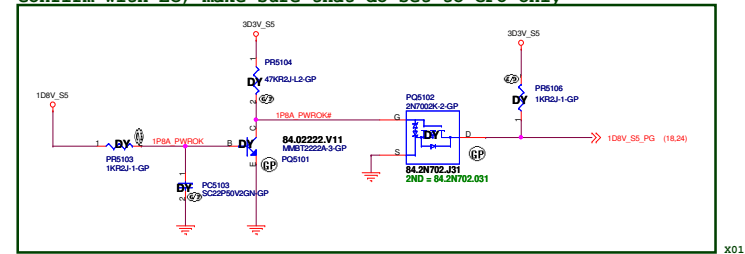


SSID = PWR.Plane.Regulator_1p8v

TLV70218 for 1D8V_S5



confirm with EC, make sure that do set to GPO only



TLV70215 for 1D5V_S0

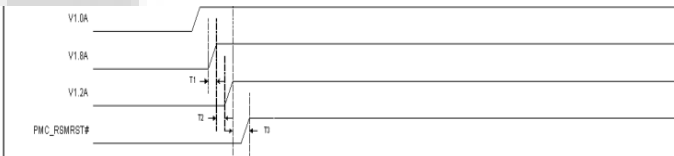
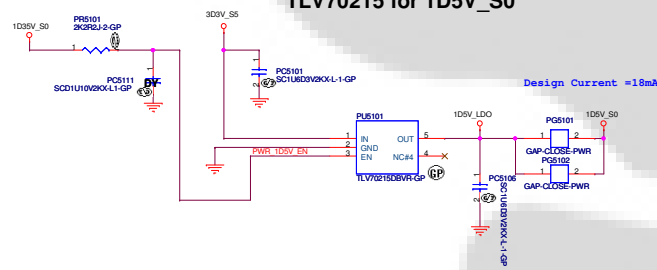
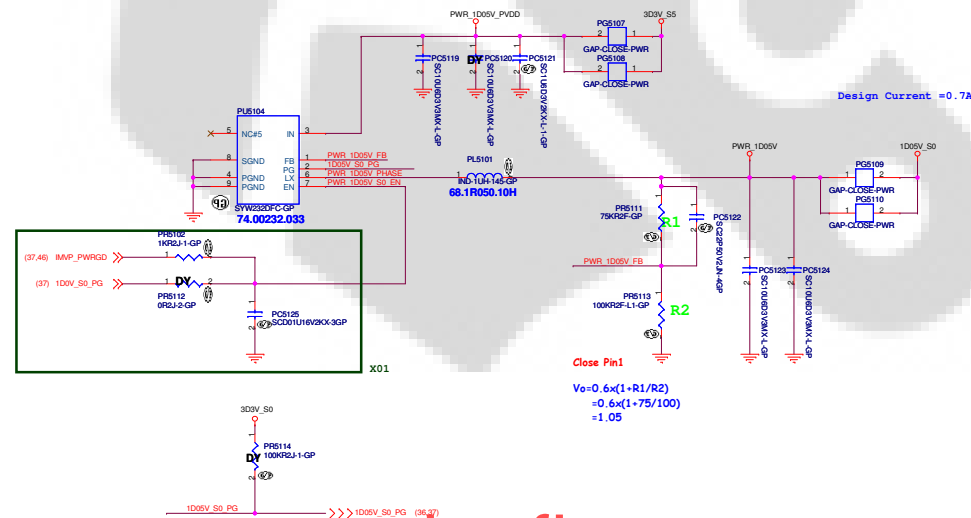


Table 4-12. Cold Boot Timing Spec

Parameter	Description	Min	Typ	Max	Units
T0	RTC_VCC stable to ILB_RTC_TEST# high	9			ms
T1	VR ramp up time from 10% to 90% voltage level			2	ms
T2	Rail to subsequent rail turn on delay	10		2000	us

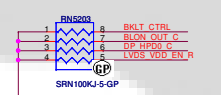
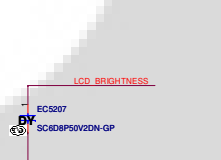
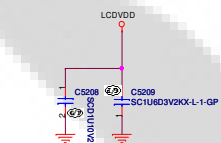
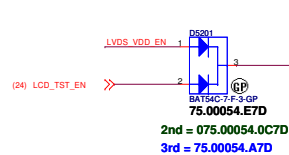
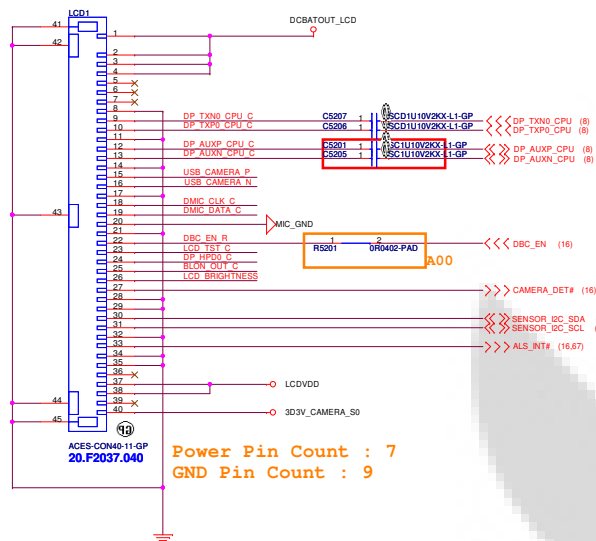
SYW232 for 1D05V_S0



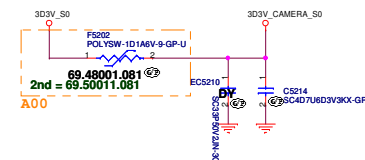
$$V_o = 0.6 \times (1 + R1/R2) \\ = 0.6 \times (1 + 75/100) \\ = 1.05$$

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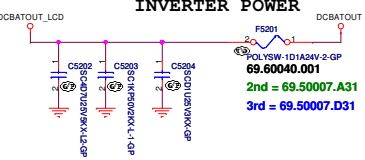
Panel Conn.



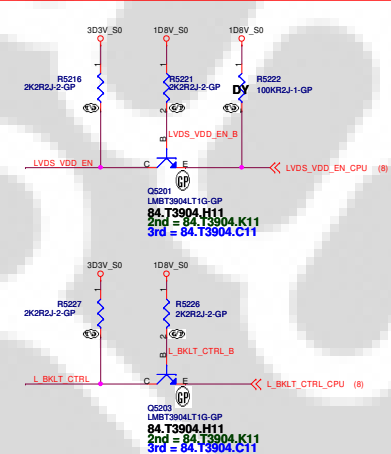
CAMERA POWER



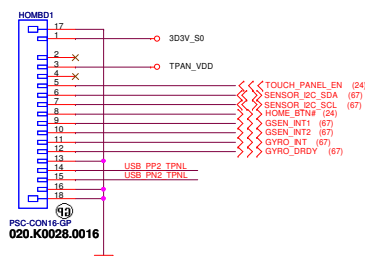
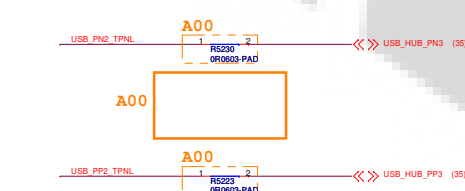
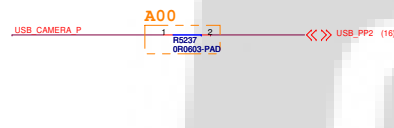
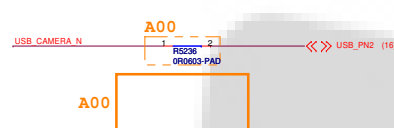
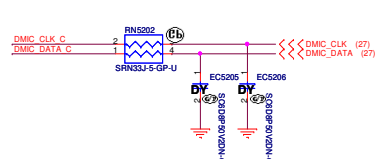
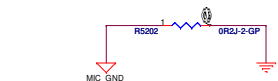
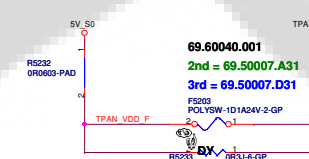
INVERTER POWER



Level shift



TOUCH PANEL POWER



<Core Design>

Blanking

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Title

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A4

Document Number

Redwood 11.6"

Rev
A00

Date: Tuesday, April 01, 2014

Sheet 53 of 102

SSID = VIDEO

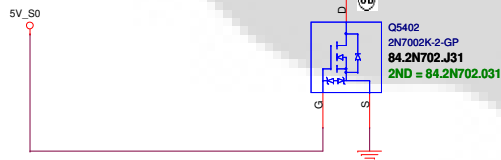
HDMI Level Shifter & CONNECTOR

HDMI CONN



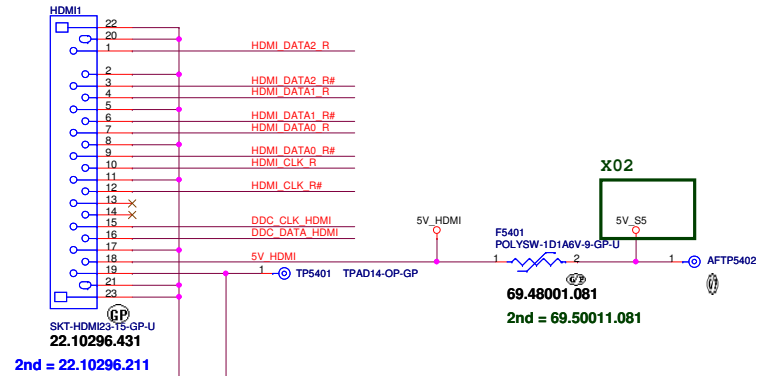
Close to HDMI Connector

Close to Level Shift



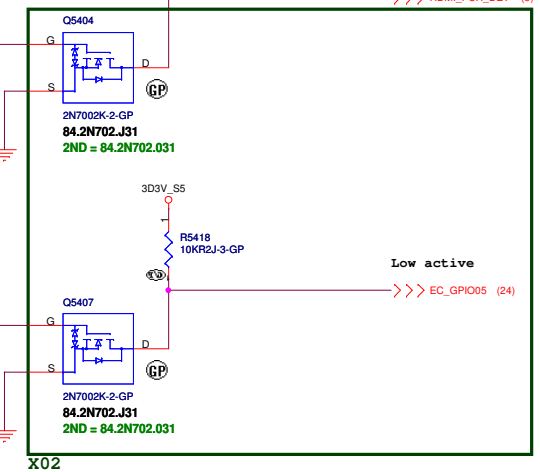
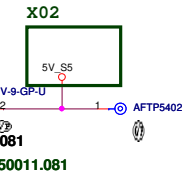
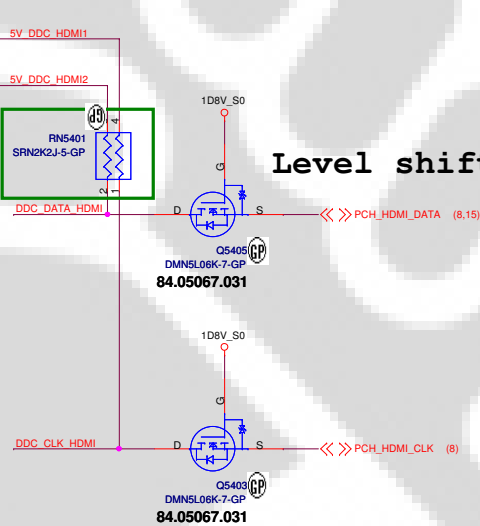
HDMI_CLK_R#	DY	R5417	150R2F-4-L-GP	HDMI_CLK_R
HDMI_DATA0_R#	DY	R5418	150R2F-4-L-GP	HDMI_DATA0_R
HDMI_DATA1_R#	DY	R5419	150R2F-4-L-GP	HDMI_DATA1_R
HDMI_DATA2_R#	DY	R5416	150R2F-4-L-GP	HDMI_DATA2_R

Reserve 150 ohm bridge resistance
on the HDMI trace as circle for EMI



close to connector

Level shift



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Core Designs


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Title: HDMI Level Shifter/Connector			
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Date: Tuesday, April 01, 2014	Sheet: 54	of: 102	

SSID = Display Port

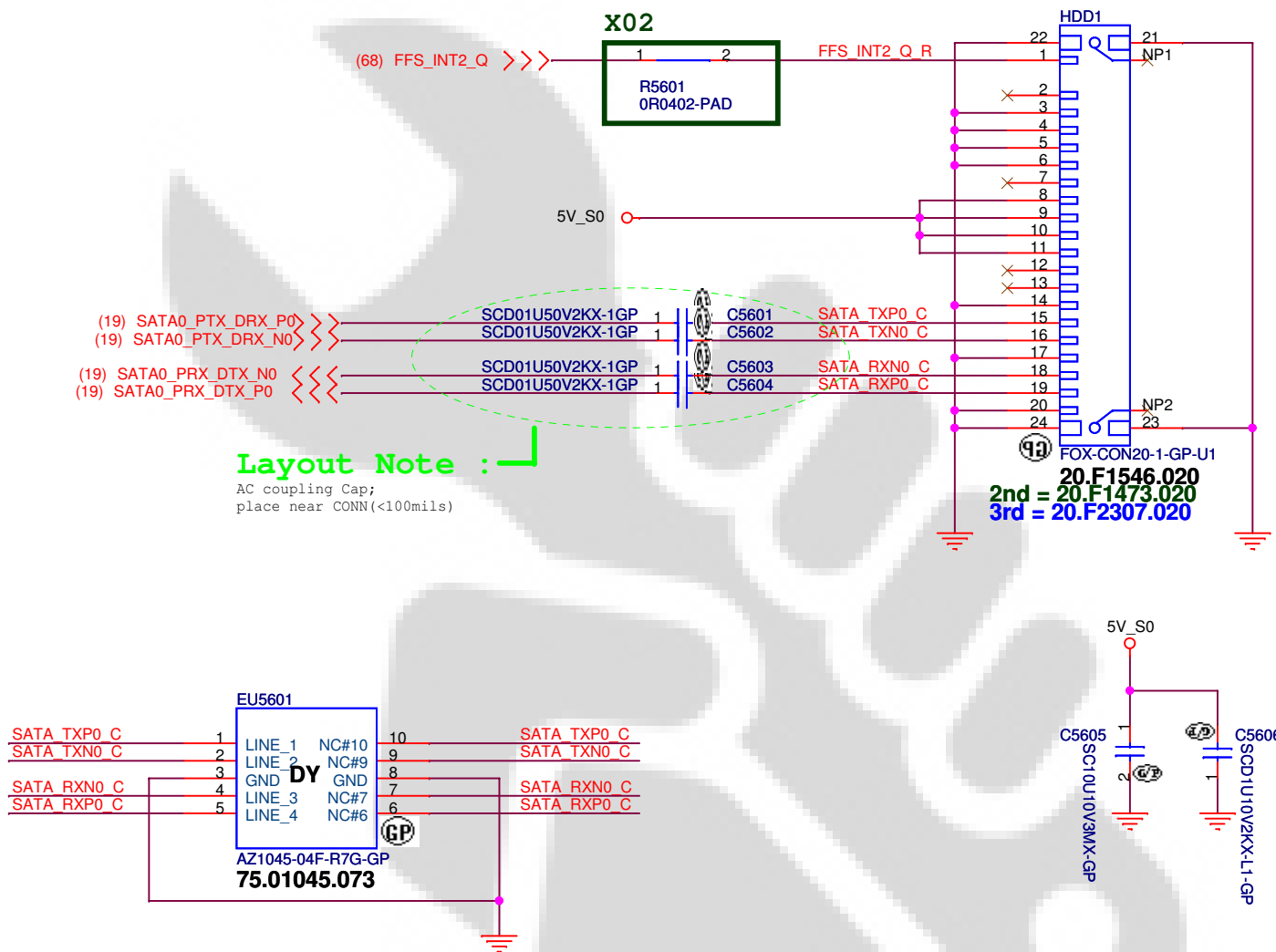
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Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014	Sheet	55	of 102

SATA HDD Connector



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HDD Connector

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A4

Document Number

Redwood 11.6"

Rev
A00

Date: Tuesday, April 01, 2014

Sheet 56 of 102

102

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Title			Reserved		
Size	Document Number				Rev
A4	Redwood 11.6"				A00
Date:	Tuesday, April 01, 2014			Sheet 57 of	102

SSID = Wireless

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Reserved

Size
A4

Document Number

Redwood 11.6"

Rev
A00

Date: Tuesday, April 01, 2014

Sheet 58 of 102

SSID = 3G

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Title WWAN CONN			
Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014		Sheet 59 of 102	

SSID = mSATA

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Size
A4

Document Number

Redwood 11.6"

Rev
A00


Date: Tuesday, April 01, 2014

Sheet 60 of 102

SSID = User.Interface

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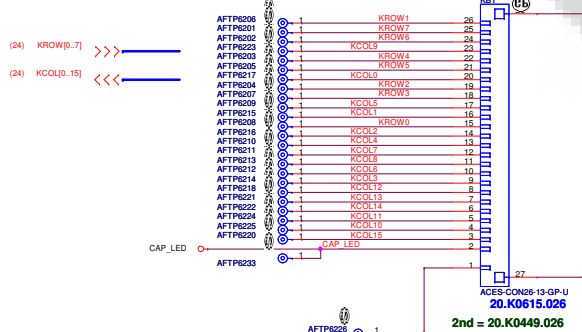
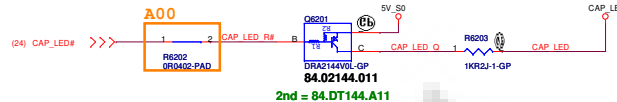
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Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014		Sheet 61	of 102

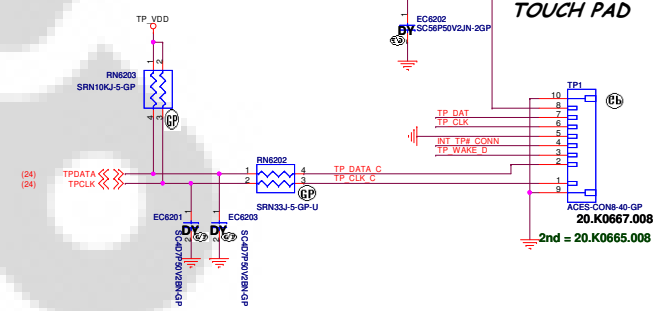
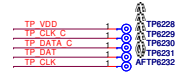
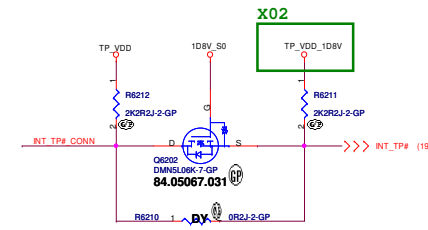
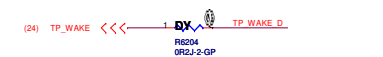
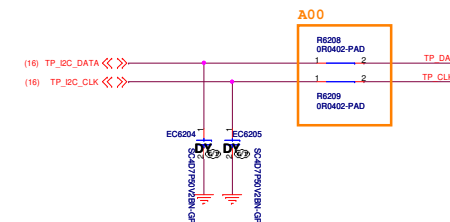
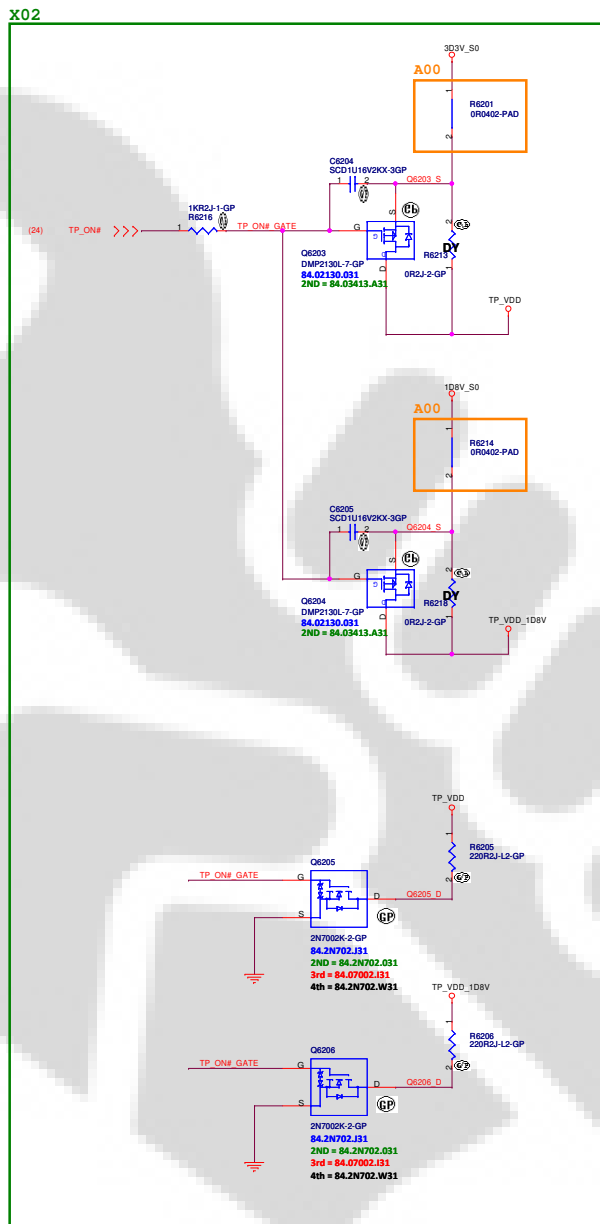
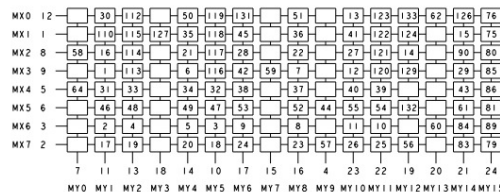
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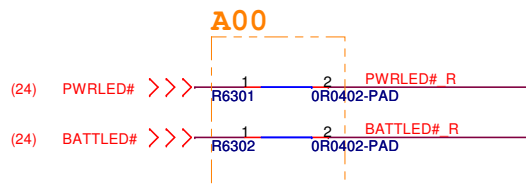
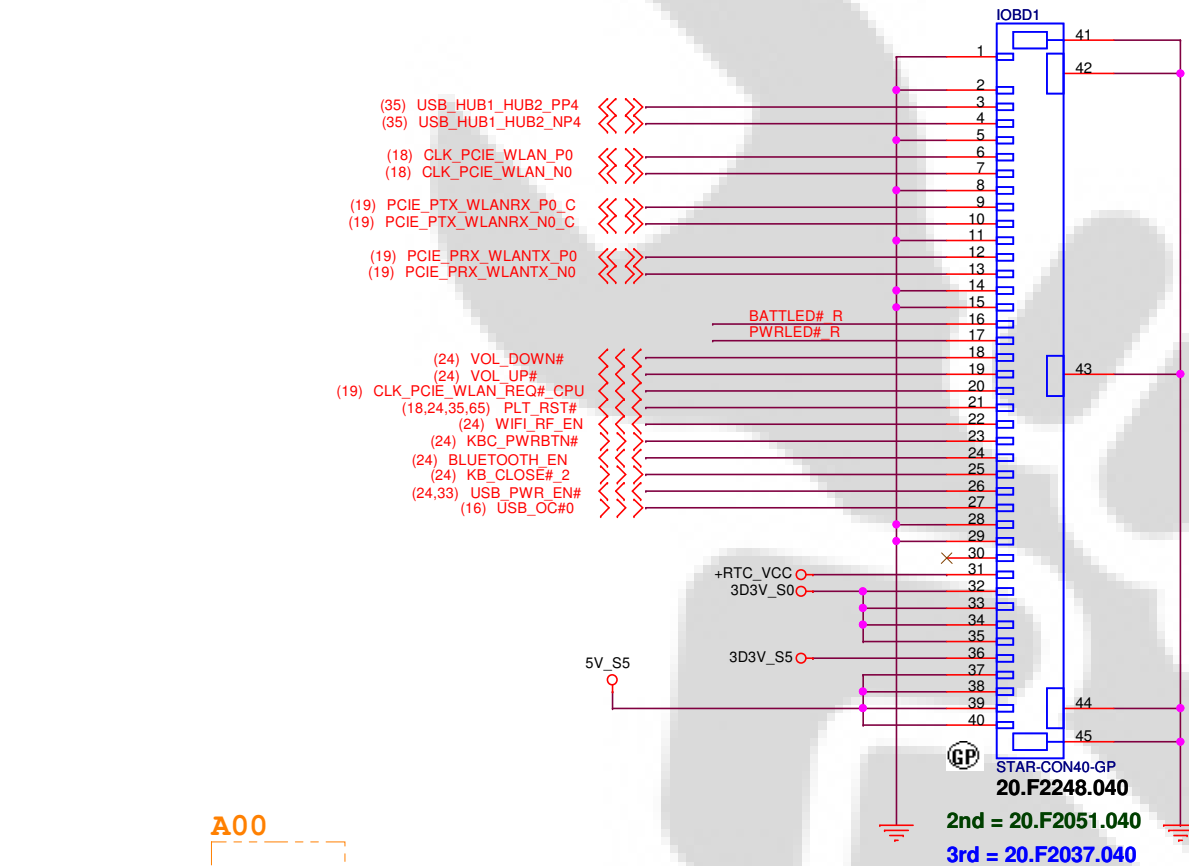
CAP LED Control

LOW actived from KBC GPIO



Pin	Signal
1	KS11
2	KS17
3	KS16
4	KS09
5	KS14
6	KS15
7	KS00
8	KS12
9	KS13
10	KS05
11	KS01
12	KS10
13	KS02
14	KS04
15	KS07
16	KS08
17	KS06
18	KS03
19	KS012
20	KS013
21	KS014
22	KS011
23	KS010
24	KS015
25	LED+
26	LED-





Power Pin Count : 10
GND Pin Count : 9

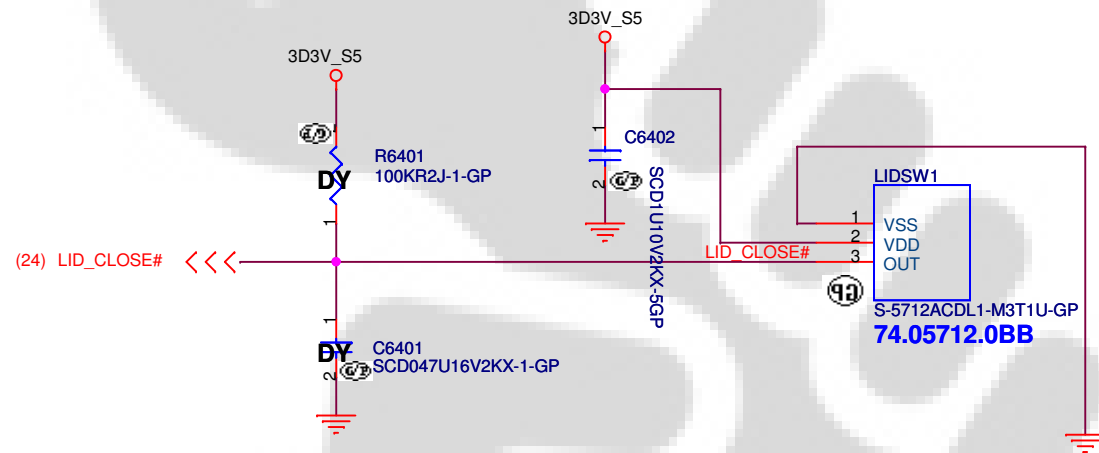
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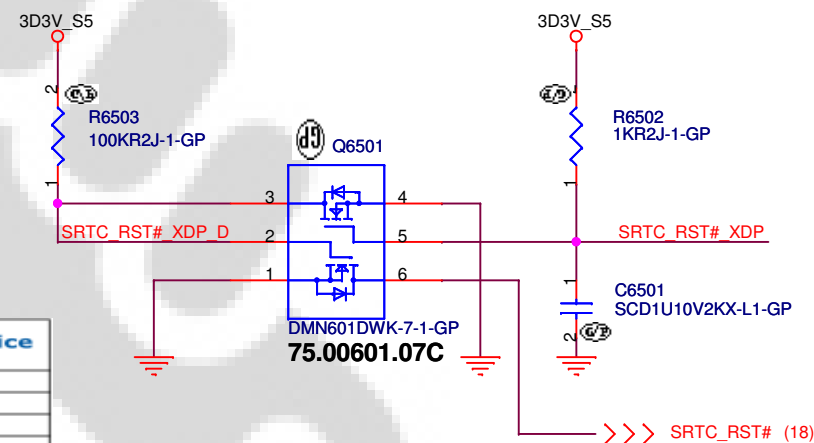
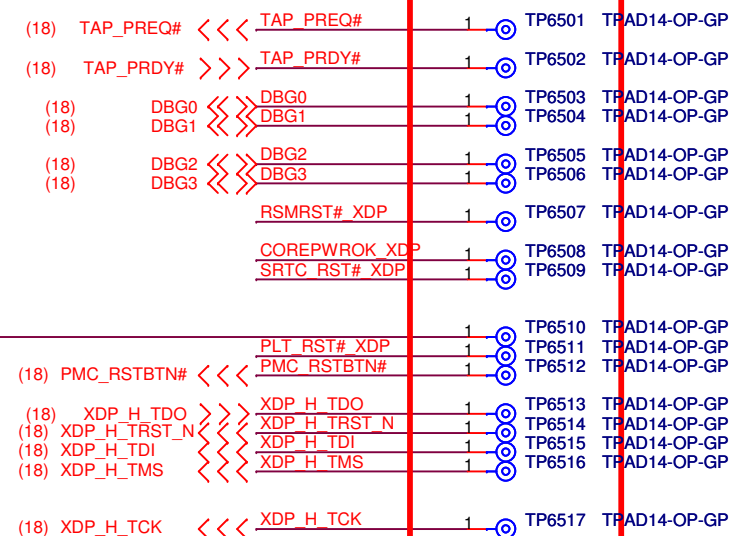
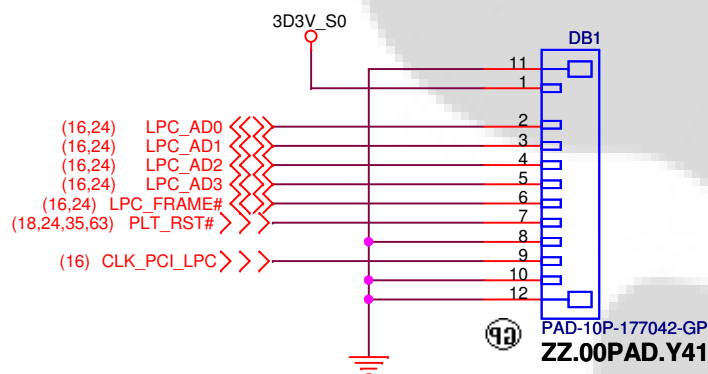
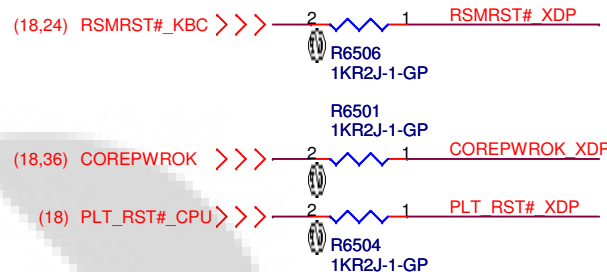
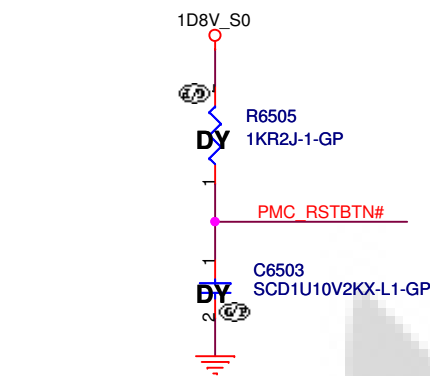
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Title		
IO Board Connector		
Size	Document Number	Rev
Custom	Redwood 11.6"	A00
Date:	Tuesday, April 01, 2014	Sheet 63 of 102



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Title Hall Sensor			
Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014	Sheet 64	of 102	



Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title: **Debug connector**

Size: A4 Document Number: **Redwood 11.6"** Rev: **A00**

Date: Tuesday, April 01, 2014 Sheet: 65 of 102

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Document Number

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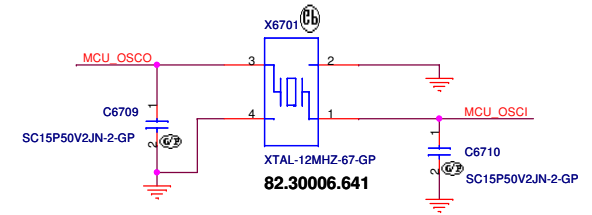
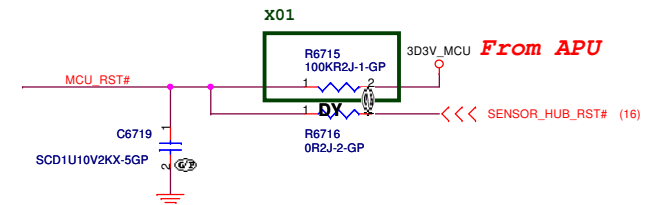
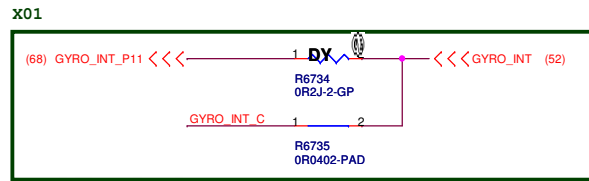
Rev
A00

Date: Tuesday, April 01, 2014

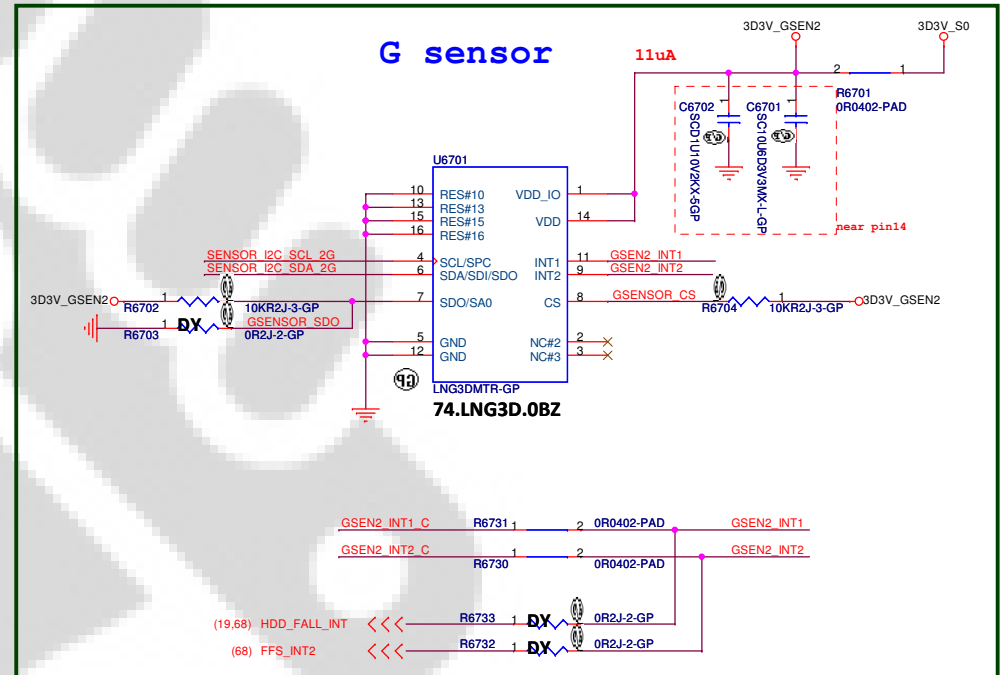
Sheet 66 of 102

```
SSID = User.Interface
```

Sensor Hub



G sensor



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DELL

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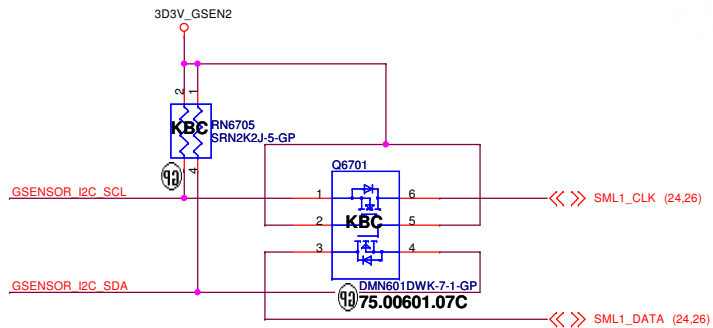
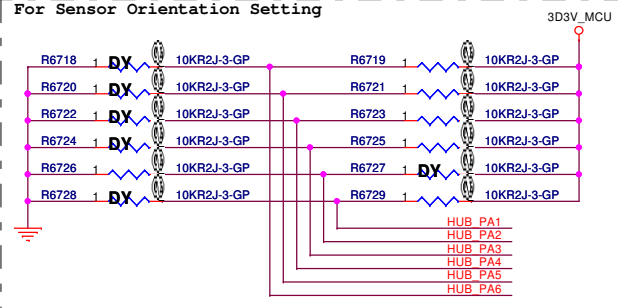
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Size A3	Document Number Redwood 11.6"	Rev A00
Date: Tuesday, April 01, 2014	Sheet 67	of 102

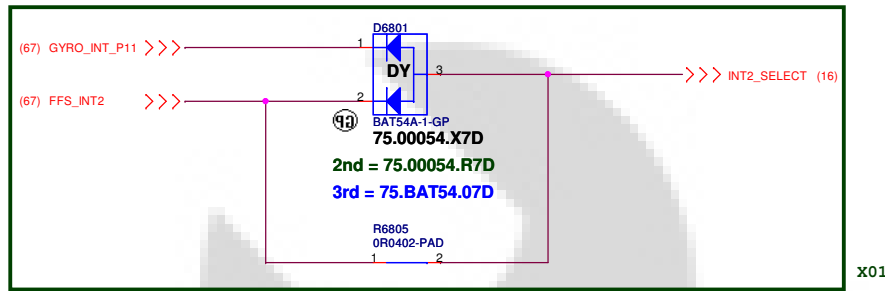
Close to each other

Close to each other

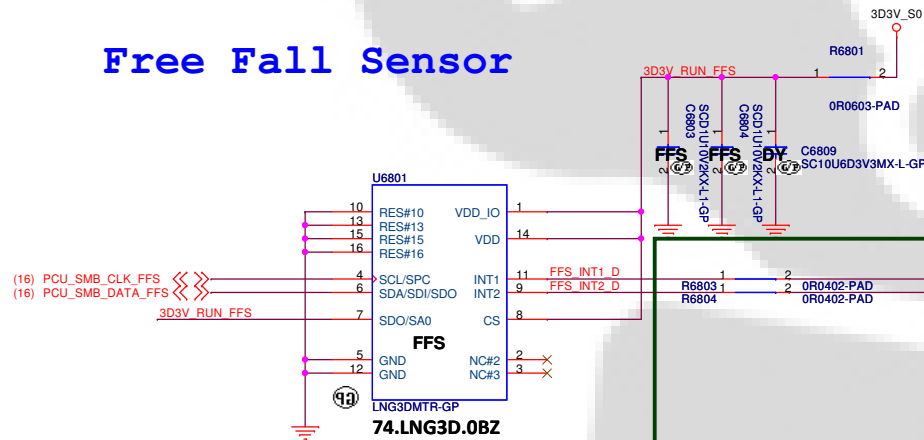
For Sensor Orientation Setting



SSID = User.Interface



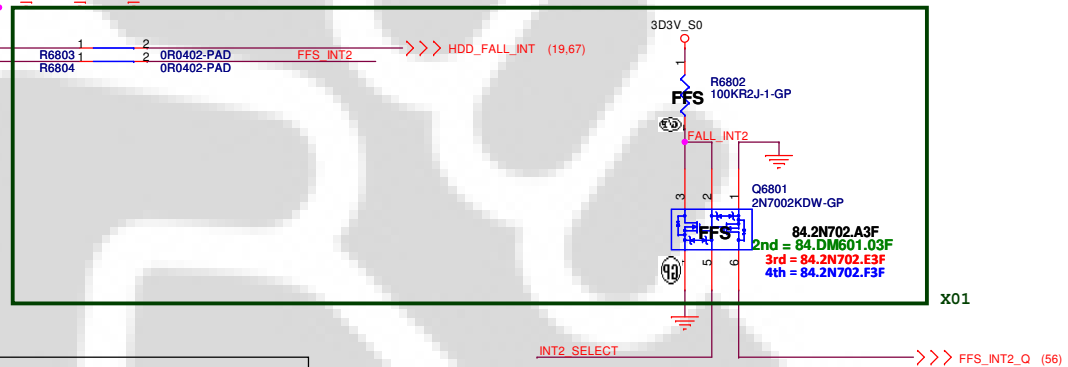
Free Fall Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6701



Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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Title			Free Fall Sensor		
Size			Redwood 11.6"		
Date:			Tuesday, April 01, 2014		
Sheet			68 of 102		
Rev			A00		

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Thunderbolt (2/5)

Size
A4

Document Number

Redwood 11.6"

Rev

A00

Date: Tuesday, April 01, 2014

Sheet 69 of 102

Blanking

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Title			Thunderbolt (3/5)		
Size	Document Number				Rev
A4	Redwood 11.6"				A00
Date:	Tuesday, April 01, 2014			Sheet 70 of 102	

Blanking

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Thunderbolt (4/5)

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A4

Document Number

Redwood 11.6"

Rev

A00

Date: Tuesday, April 01, 2014

Sheet 71 of 102

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Title			Thunderbolt (5/5)		
Size	Document Number				Rev
A4	Redwood 11.6"				A00
Date:	Tuesday, April 01, 2014			Sheet 72 of 102	

Blanking

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Title

Reserved

Size
A4

Document Number

Redwood 11.6"

Rev

A00

Date: Tuesday, April 01, 2014

Sheet 73 of 102

Blanking

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Title

Reserved

Size
A4

Document Number

Redwood 11.6"


Rev
A00

Date: Tuesday, April 01, 2014

Sheet 74 of 102

Blanking

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Title Reserved			
Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014		Sheet 75 of 102	

Blanking

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Title Reserved			
Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014		Sheet 76	of 102

Blanking

<Core Design>



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Title

Reserved

Size
A4

Document Number

Redwood 11.6"

Rev
A00

Date: Tuesday, April 01, 2014

Sheet 77 of 102

Blanking

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Reserved

Size
A4

Document Number

Redwood 11.6"

Rev
A00

Date: Tuesday, April 01, 2014

Sheet 78 of 102

Blanking

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Reserved

Size
A4

Document Number

Redwood 11.6"

Rev

A00

Date: Tuesday, April 01, 2014

Sheet 79 of 102

Blanking

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Title

Reserved

Size
A4

Document Number

Redwood 11.6"


Rev
A00

Date: Tuesday, April 01, 2014

Sheet 80 of 102

Blanking

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Title Reserved			
Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014	Sheet 81	of	102

Blanking

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Title

Reserved

Size
A4

Document Number

Redwood 11.6"

Rev
A00

Date: Tuesday, April 01, 2014

Sheet 82 of 102

Blanking

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Title

Reserved

Size
A4

Document Number

Redwood 11.6"

Rev

A00

Date: Tuesday, April 01, 2014

Sheet 83 of 102

Blanking

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Title

Switchable GFX LCD(1/2)

Size
A4

Document Number

Redwood 11.6"

Rev

A00

Date: Tuesday, April 01, 2014

Sheet 84 of 102

Blanking

<Core Design>



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Switchable GFX LCD(2/2)

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A4

Document Number

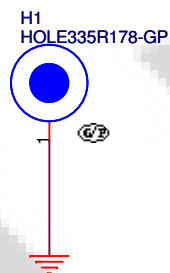
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Rev
A00

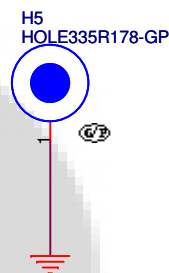
Date: Tuesday, April 01, 2014

Sheet 85 of 102

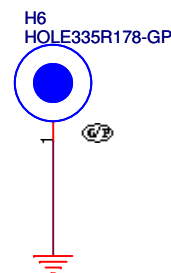
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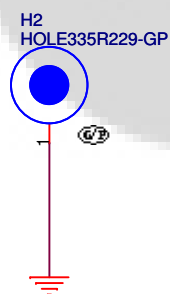
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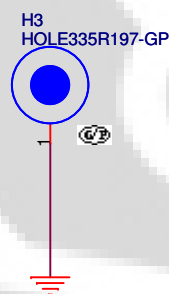
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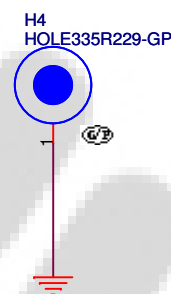
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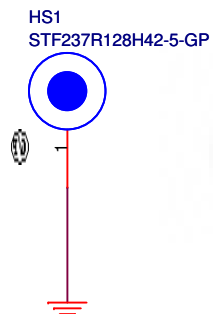
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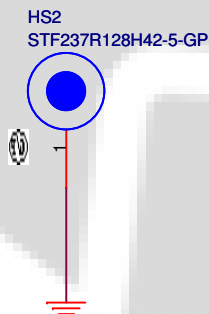


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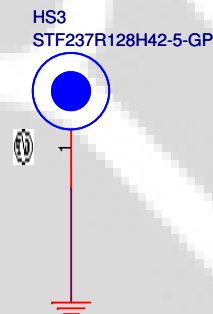
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34.4UV01.101



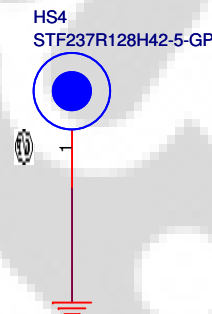
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34.4UV01.101



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34.4UV01.101



34.4UV28.101

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UNUSED PARTS/EMI Capacitors

Size
A4

Document Number

Redwood 11.6"

Rev

A00

Date: Tuesday, April 01, 2014

Sheet 86 of 102

Blanking

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

Size
A4

Document Number

Redwood 11.6"


Rev
A00

Date: Tuesday, April 01, 2014

Sheet 87 of 102

Blanking

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Reserved			
Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014		Sheet 88 of	102

SSID = Finger Print

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Title

Reserved

Size
A4

Document Number

Redwood 11.6"

Rev

A00

Date: Tuesday, April 01, 2014


Sheet 89 of 102

SSID = Express Card

Blanking



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Title Reserved			
Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014		Sheet 90 of 102	

SSID = Smart Card

Blanking



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Title

Reserved

Size
A4

Document Number

Redwood 11.6"

Rev

A00

Date: Tuesday, April 01, 2014

Sheet 91 of 102

Blanking

<Core Design>



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

Size
A4

Document Number

Redwood 11.6"

Rev
A00

Date: Tuesday, April 01, 2014


Sheet 92 of 102

SSID = Docking

Blanking



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Title			
<i>Reserved</i>			
Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014	Sheet	93	of 102

SSID = Intel LAN

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Title			
<i>Reserved</i>			
Size A4	Document Number Redwood 11.6"		Rev A00
Date: Tuesday, April 01, 2014		Sheet 94 of	102

Blanking

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PCH XDP

Size
A4

Document Number

Redwood 11.6"

Rev

A00

Date: Tuesday, April 01, 2014

Sheet 96 of 102

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table of content

Size
A4

Document Number

Redwood 11.6"

Rev

A00

Date: Tuesday, April 01, 2014

Sheet 97 of 102



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Size
A4

Document Number

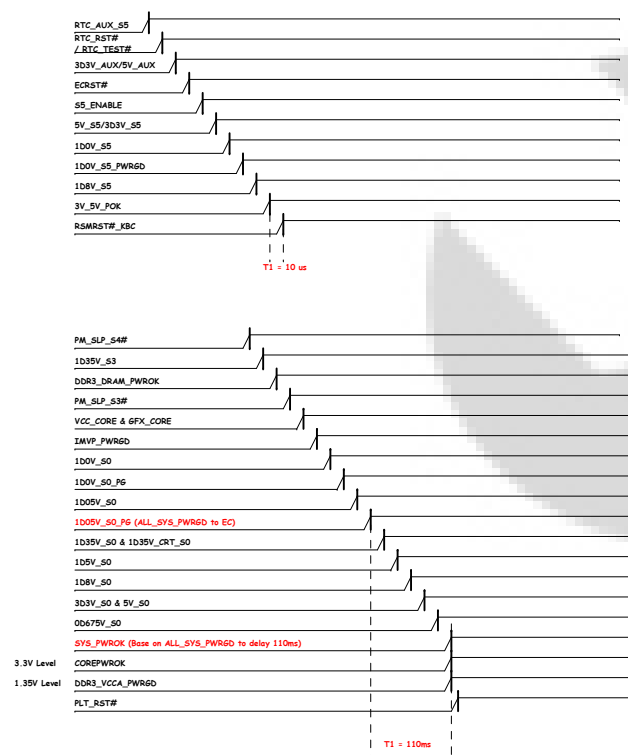
Redwood 11.6"

Rev
A00

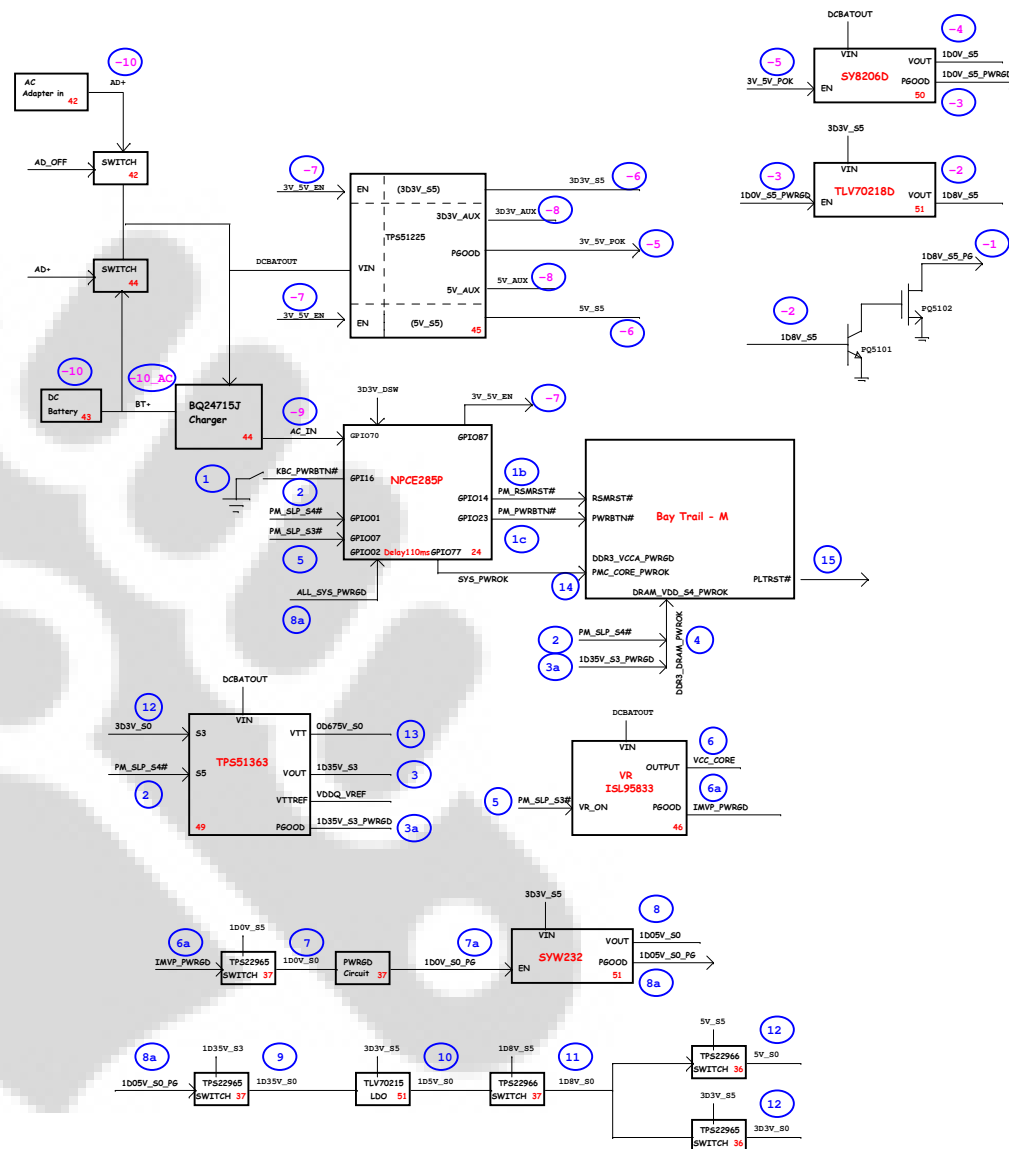
Date: Tuesday, April 01, 2014

Sheet 98 of 102

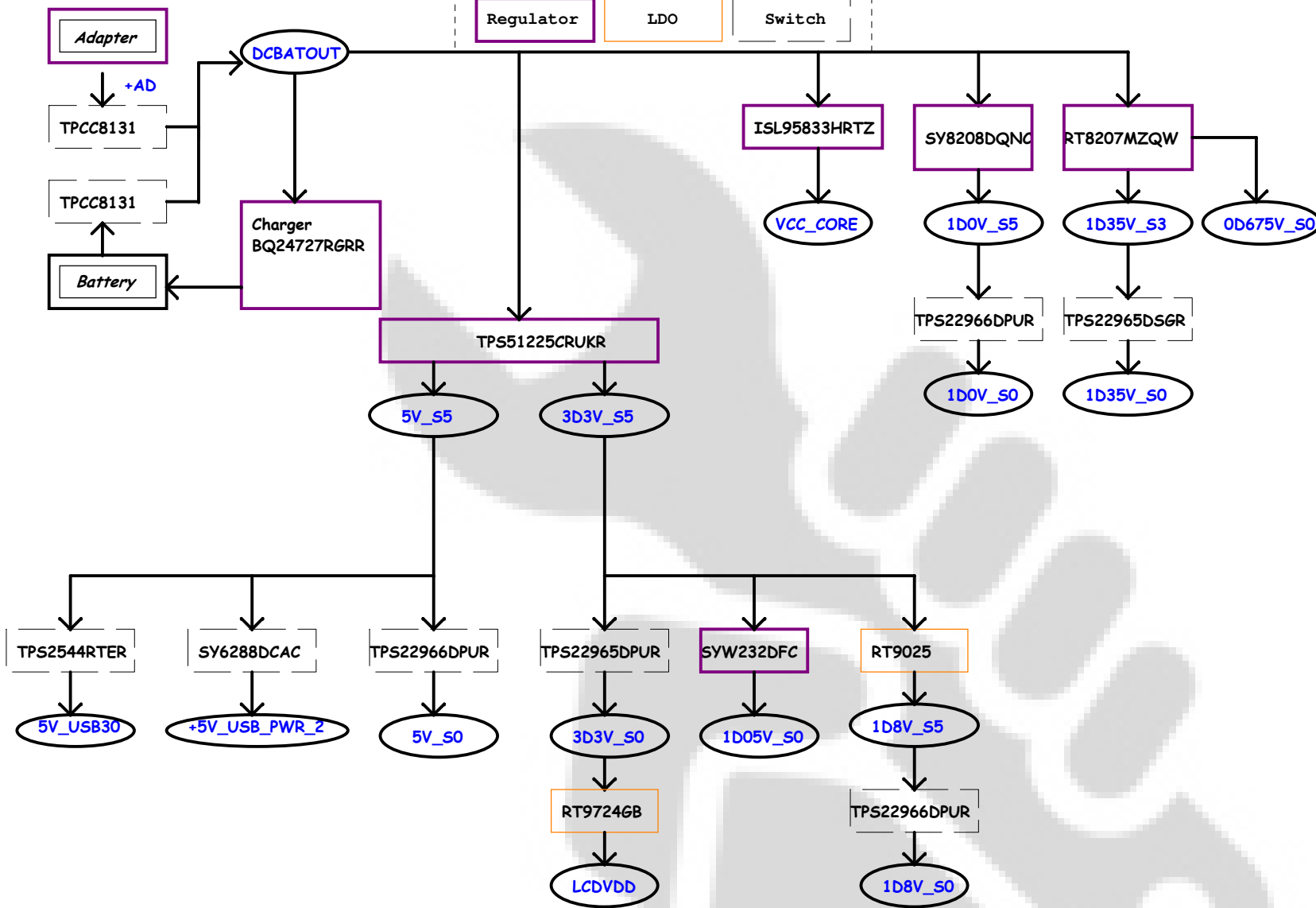
Intel-Power Up Sequence with non-S0ix



Bay Trail - M POWER UP SEQUENCE DIAGRAM



Power Shape

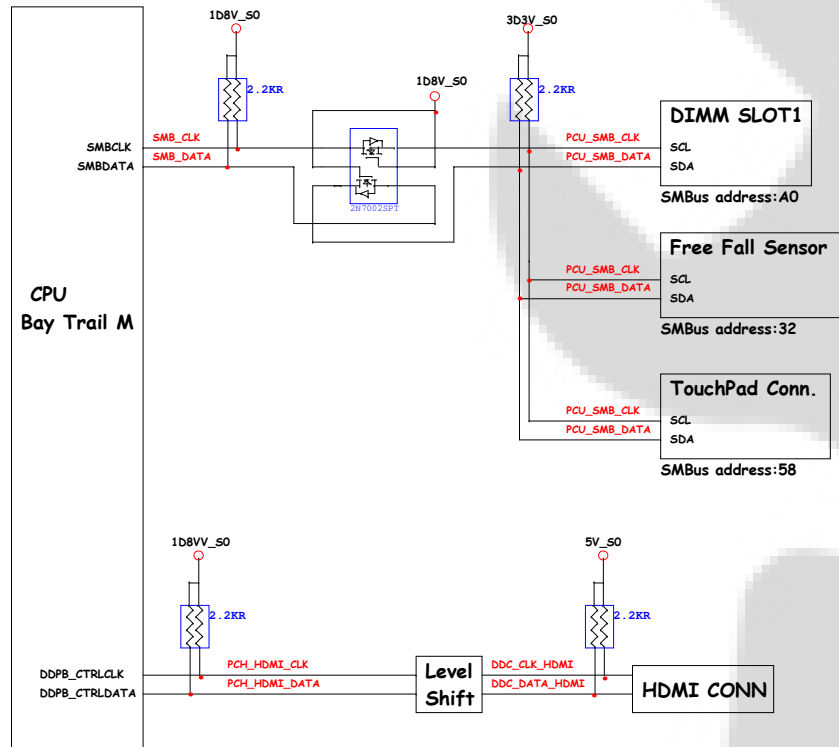


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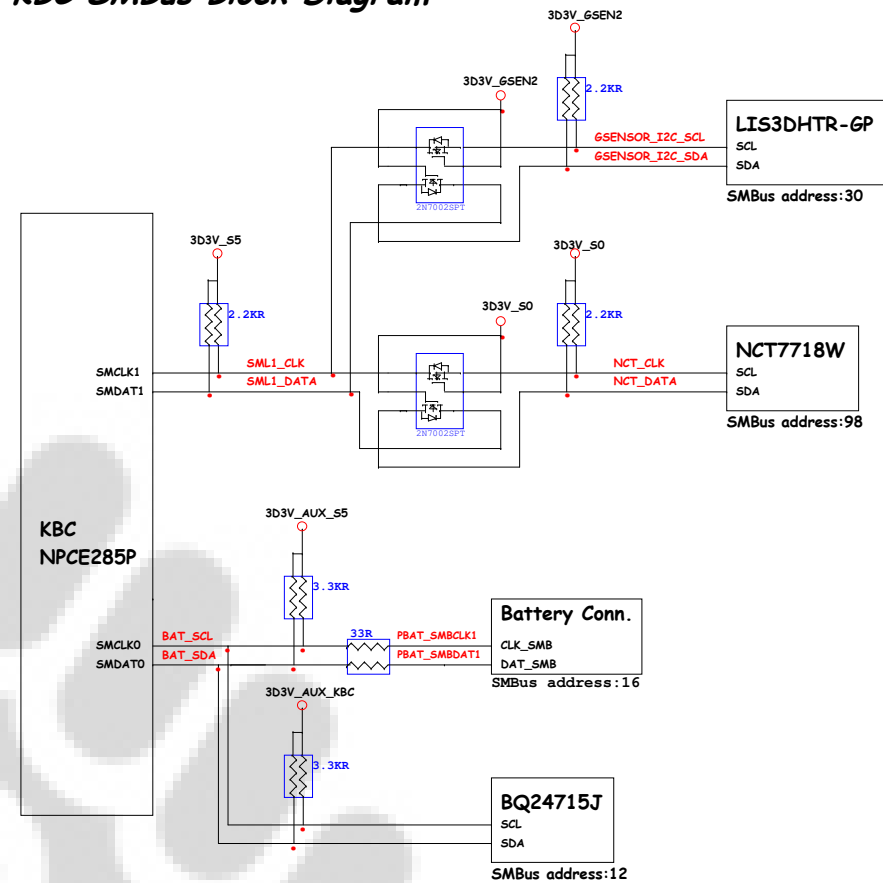
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Title Power Block Diagram			
Size A3	Document Number Redwood 11.6"	Rev A00	
Date: Tuesday, April 01, 2014	Sheet 100 of 102		

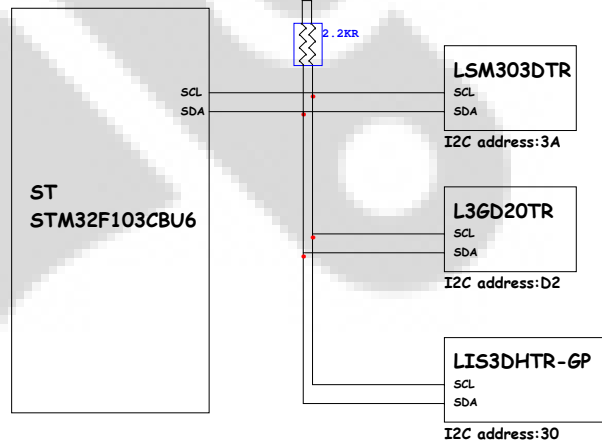
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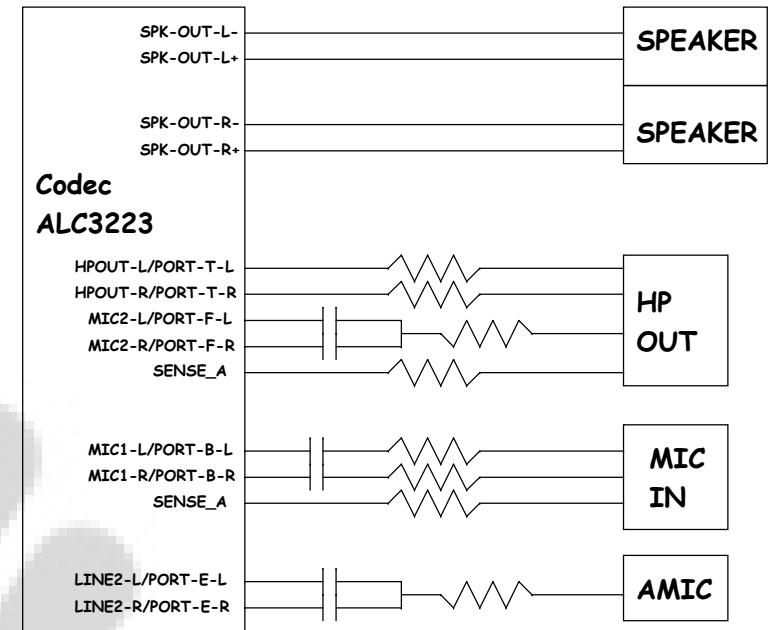
KBC SMBus Block Diagram



Sensor Hub I2C Block Diagram



Audio Block Diagram



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Title **THERMAL/AUDIO BLOCK DIAGRAM**

Size Custom	Document Number Redwood 11.6"	Rev A00
Date: Tuesday, April 01, 2014	Sheet 102 of 102	