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Compal Confidential

Schematics Document

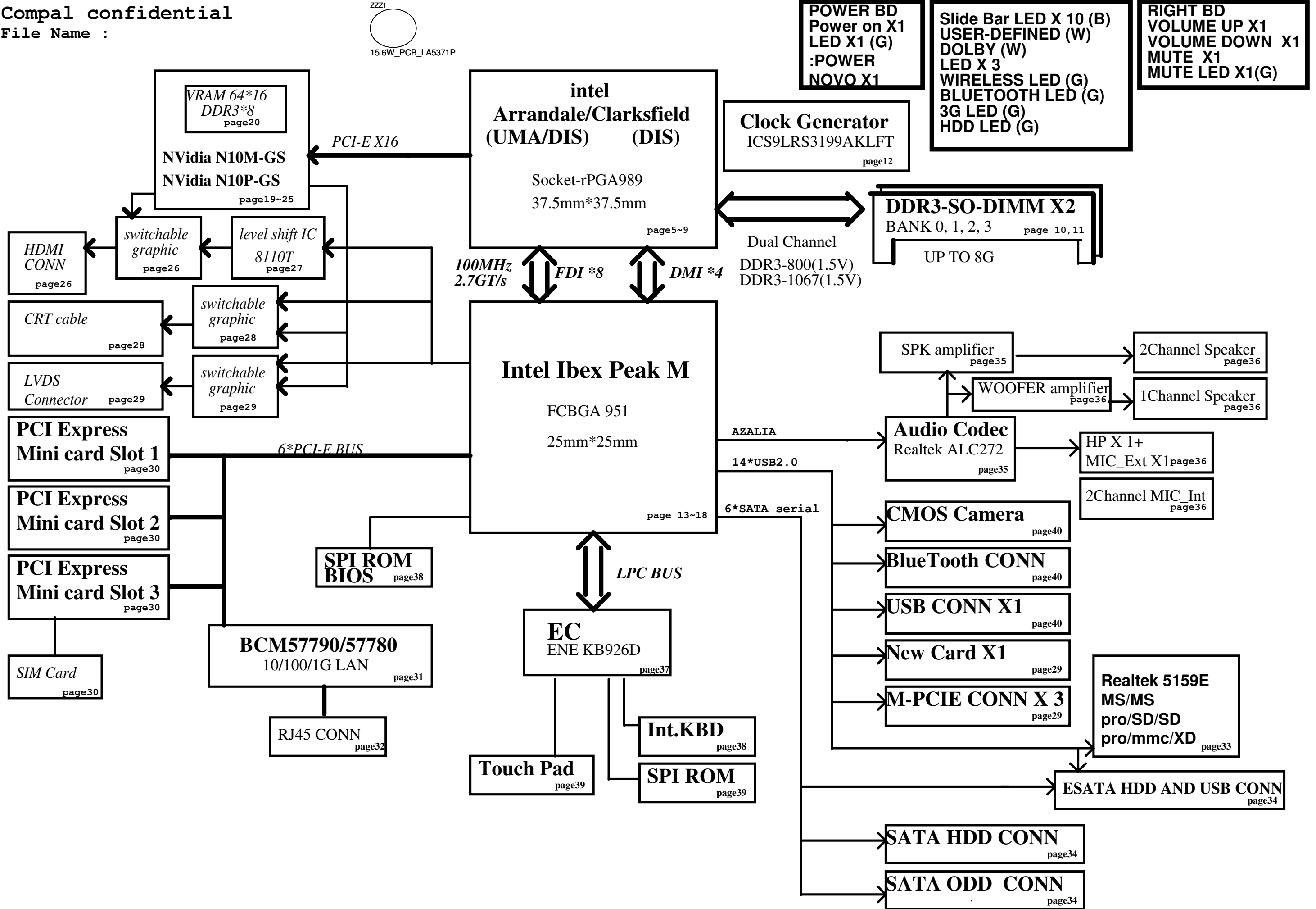
Arrandale/Clarksville

with Intel IBEX PEAK-M core logic

NIWBA

REV: 0.1

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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title Cover Sheet		
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				Date: Tuesday, March 24, 2009 Sheet 1 of 52		



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DDR3 Voltage Rails

<div>power plane</div> <div>State</div>				+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
	+B	+5VALW +3VALW	+1.5V	
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW									
SMB_EC_CK2	KB926	X	X	X	X	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW											+3VALW
SMBCLK	PCH	V	X	X	V	V	X	X	X	X	V	X
SMBDATA	+3VALW	+3VALW			+3VS	+3VS					+3VS	
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW											
SML1CLK	PCH	X	X	V	X	X	X	V	X	V	X	X
SML1DATA	+3VALW			+3VALW				+3VS		+3VS		

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

@ FUNCTION

EVT		NON-USE	
45@	(45 BOM)		
GIGA@	(GIGA LAN)	100@	(100 LAN)
NO TVSW@	(NON TV POWER SW)	TVSW@	(TV POWER SW)
ARRAY@	(ARRAY MIC)	MONO@	(MONO MIC)
S512@	FOR X76 BOM		
H512@	FOR X76 BOM		
S1024@	FOR X76 BOM		
H1024@	FOR X76 BOM		
X76@	(X76 BOM)		
M1@	(DDR M1 MODE)		
3G@	(3G MODE)		
10M@	FOR 10M CHIP		
10P@	FOR 10P CHIP		
UMA@	FOR Auberndale		
DIS@	FOR Auberndale/Clarksfield		
VGA@	FOR NVIDIA PART		

PCIE PORT LIST

PORT	DEVICE
1	NEW CARD
2	WLAN
3	LAN
4	3G
5	
6	TV TUNNER
7	
8	

USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
1	RIGHT SIDE
2	CMOS
3	
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	TV TUNNER
10	NEW CARD
11	BT
12	
13	3G

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VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID orPower supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6	GPIO5	N10M-GS	N10P-GS
GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	1	0.9V	0, 10

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

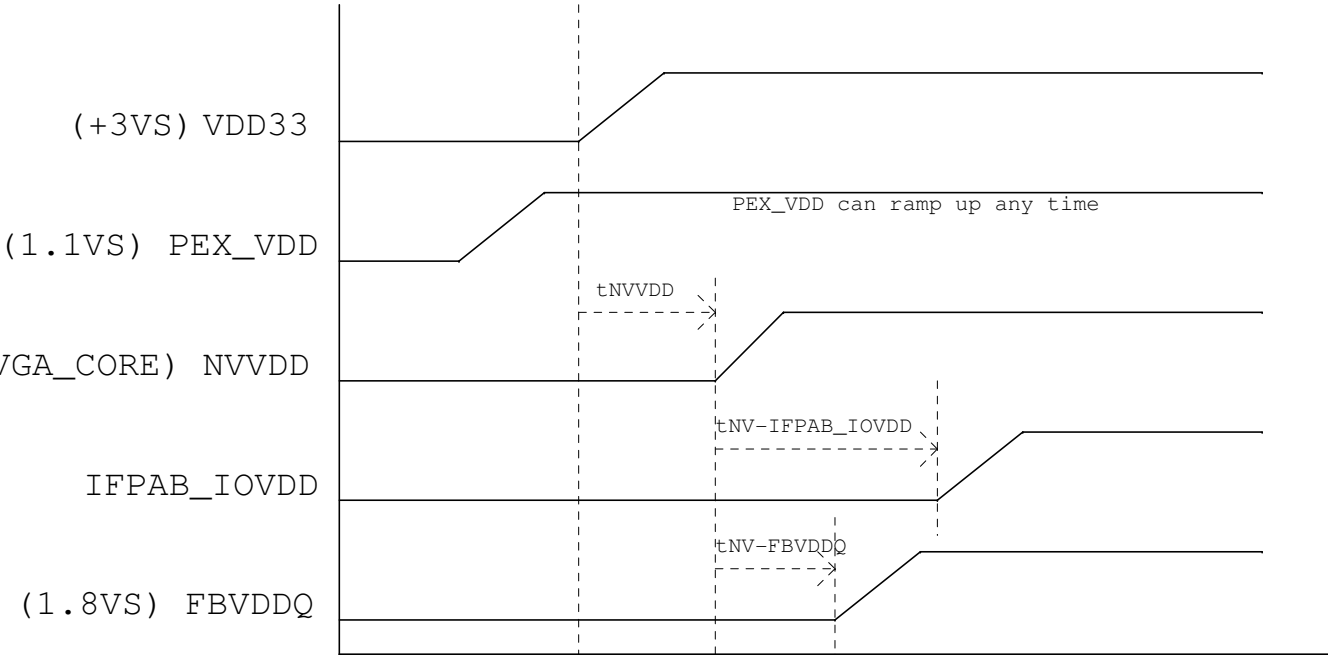
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK (MHz)	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)		(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

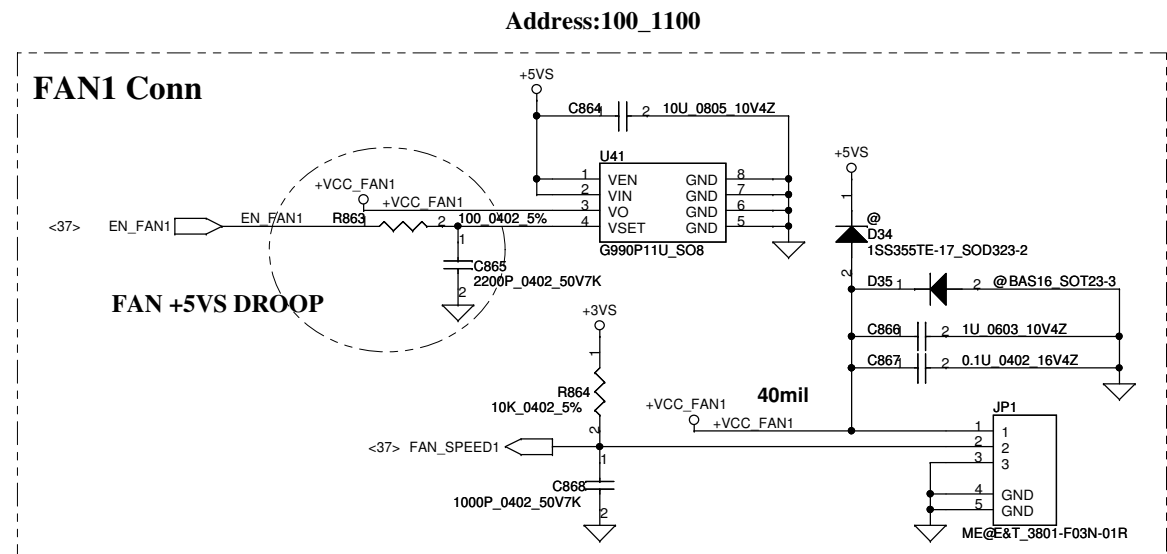
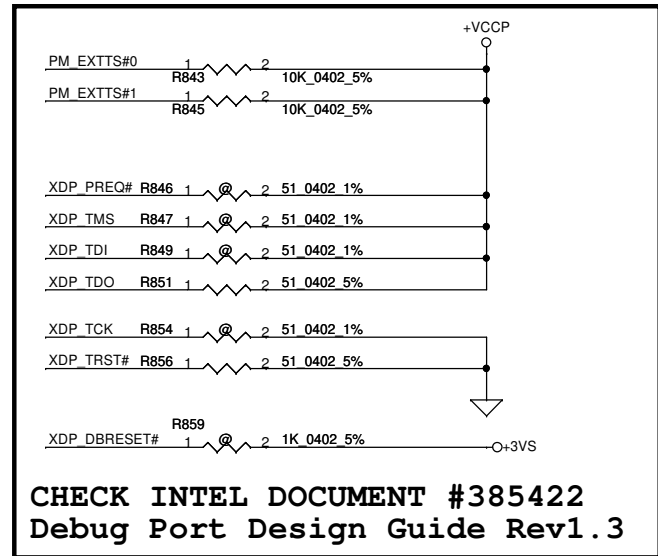
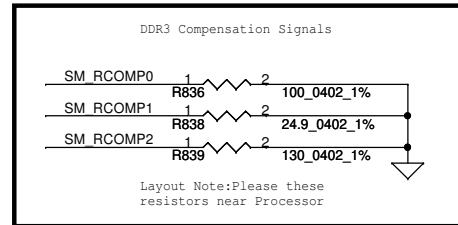
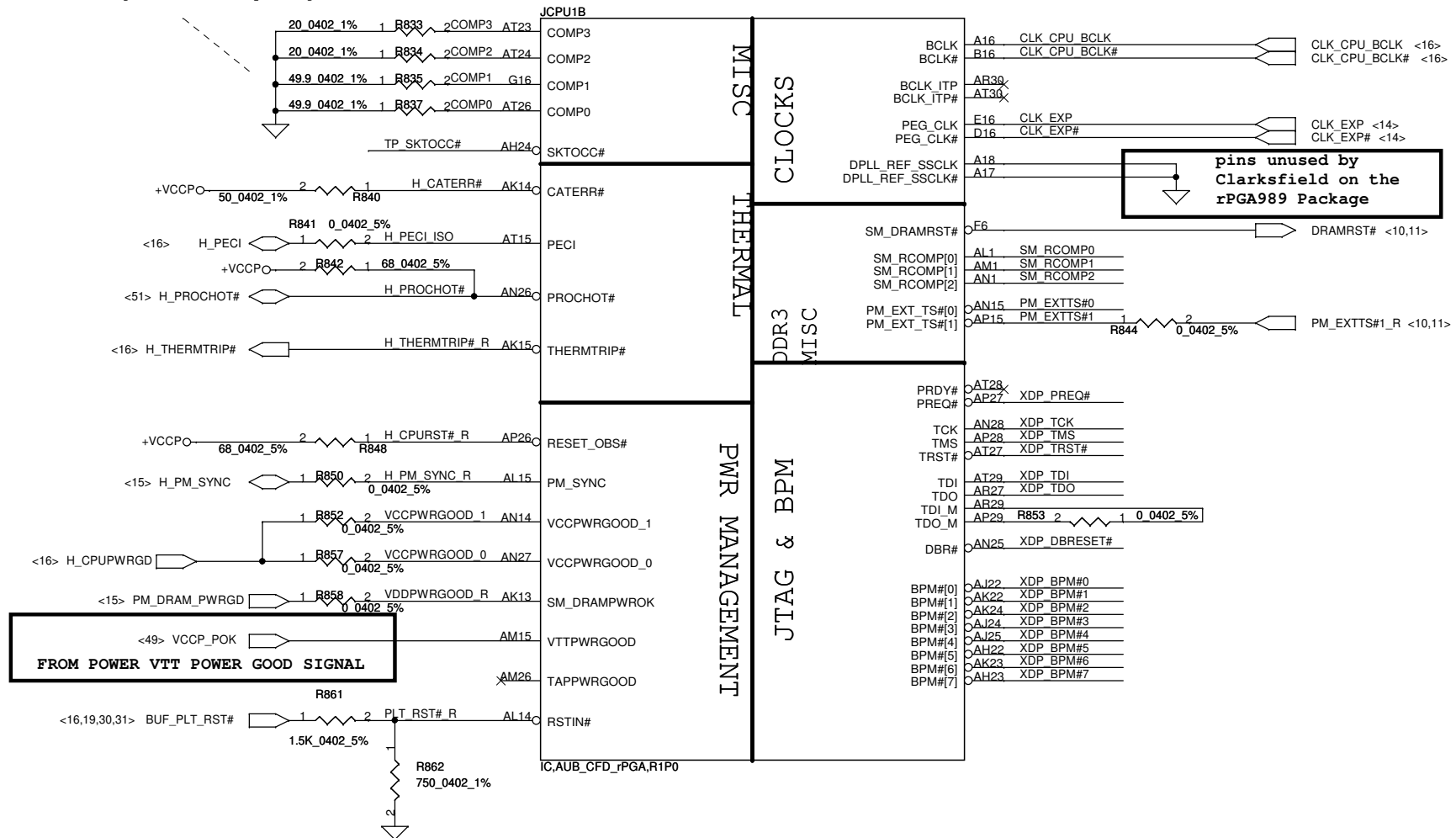
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK (MHz)	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)		(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

Power Sequence

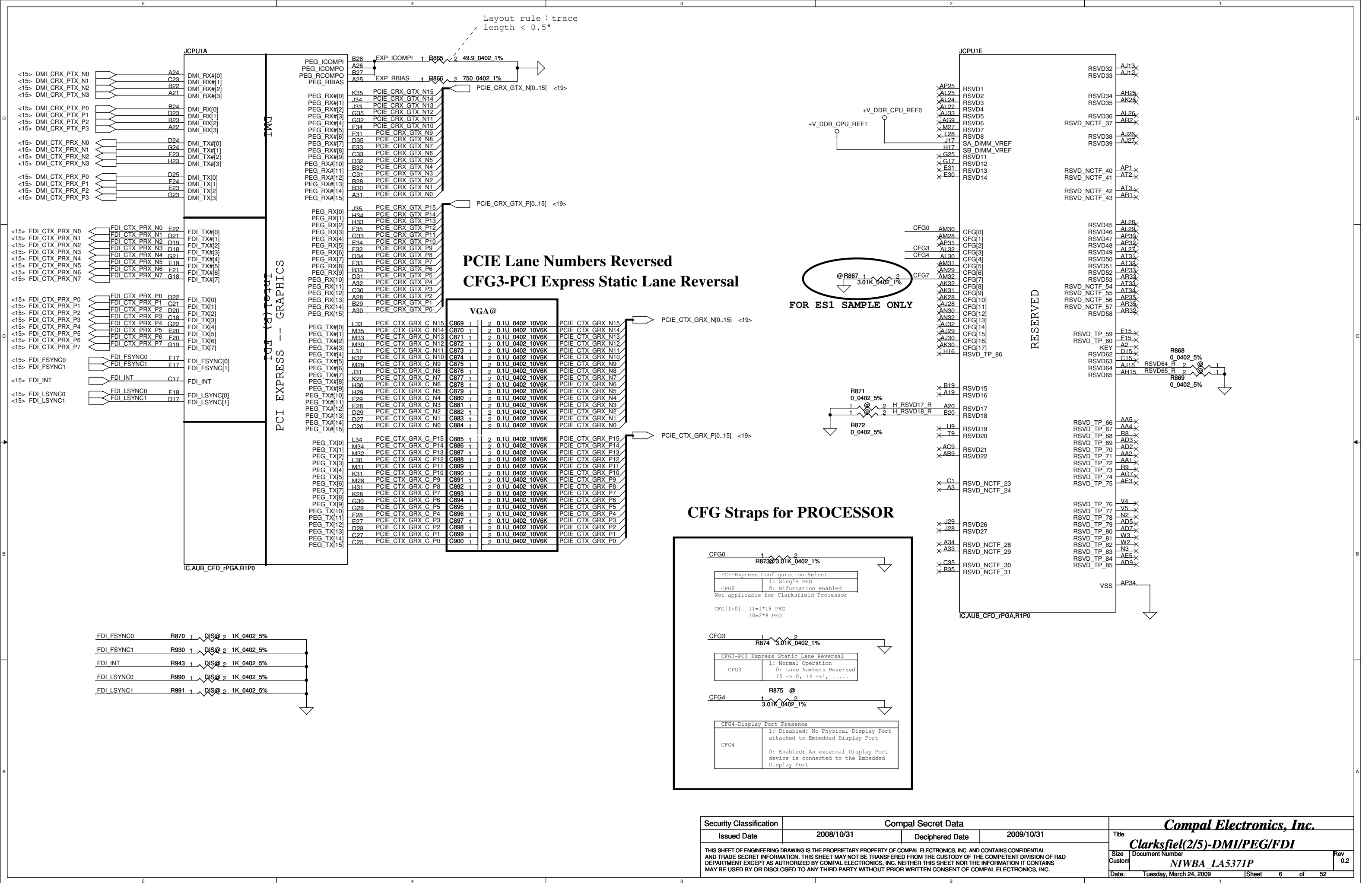
The ramp time for any rail must be more than 40us

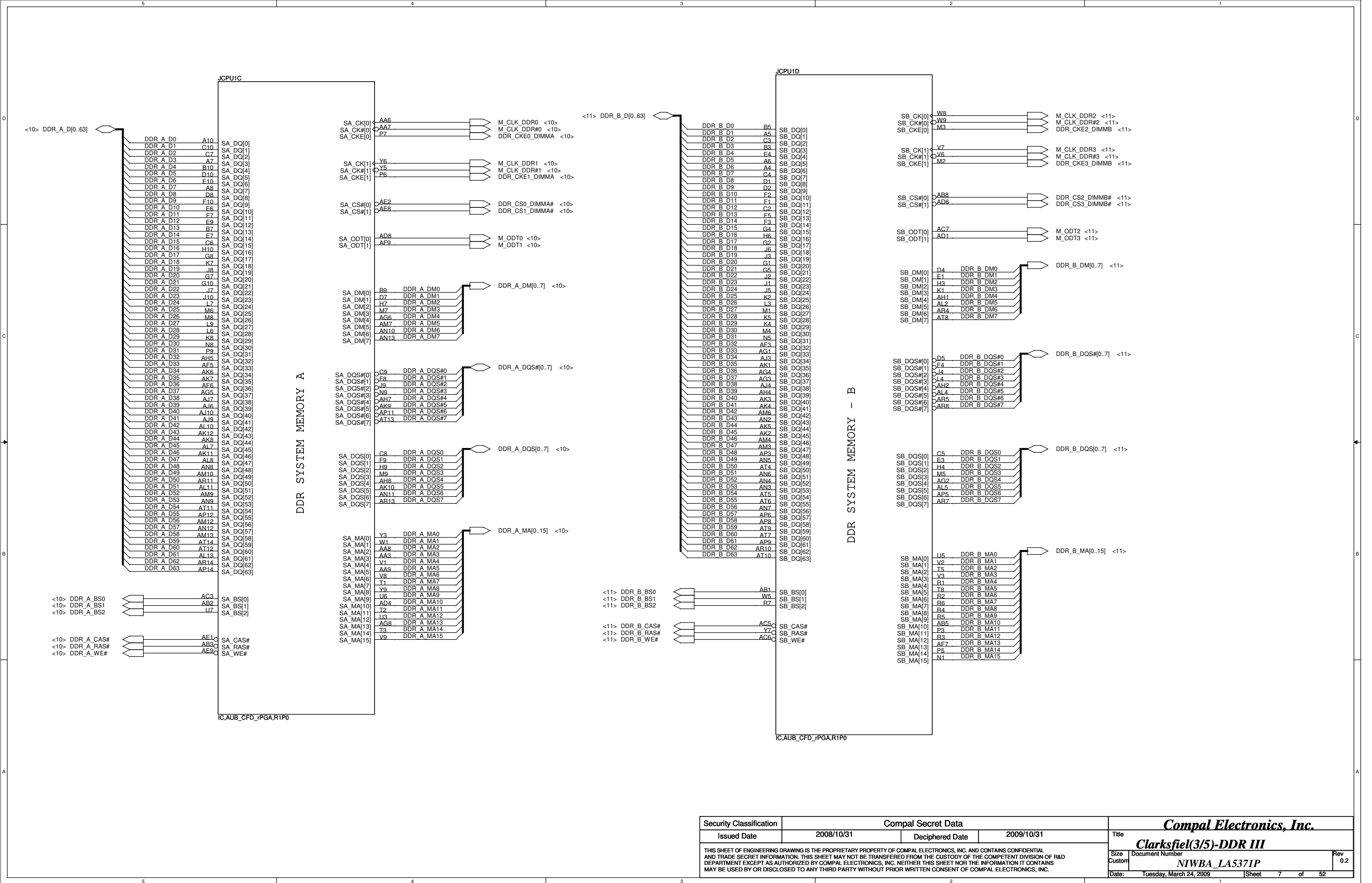


Layout rule : 10mil width trace
length < 0.5", spacing 20mil

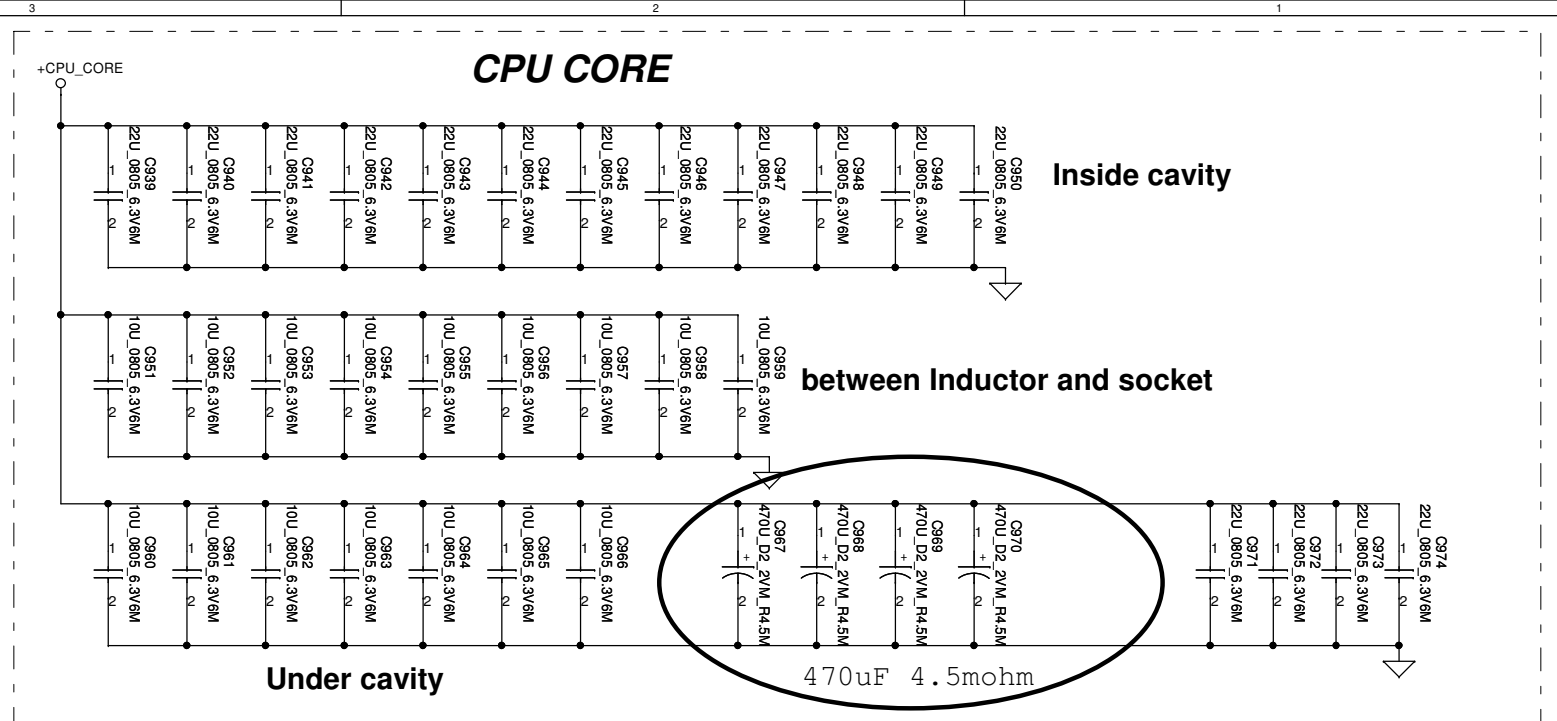
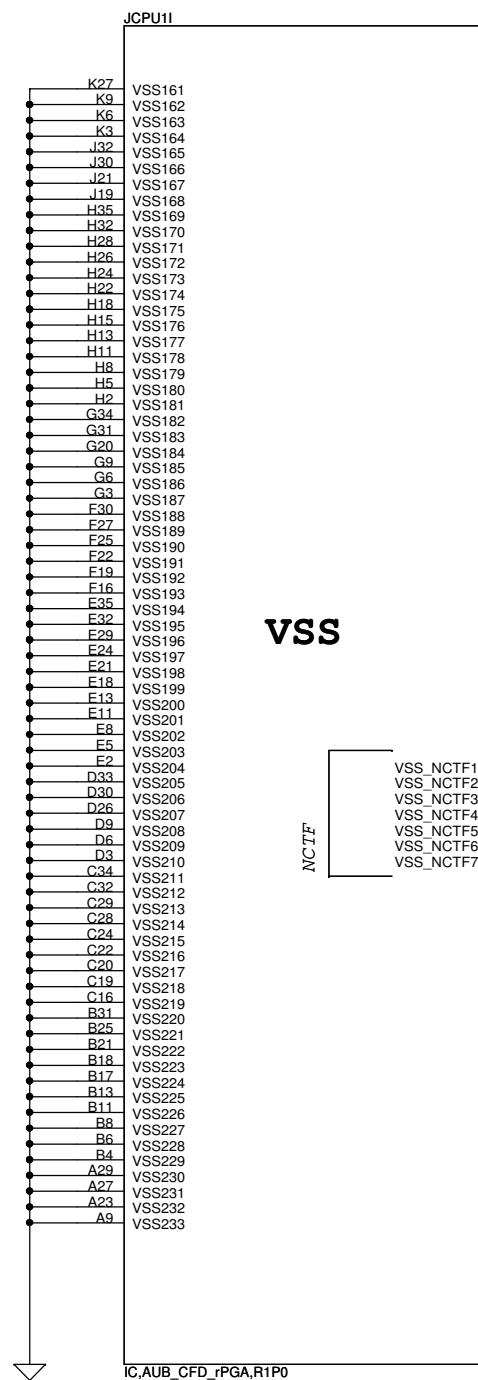
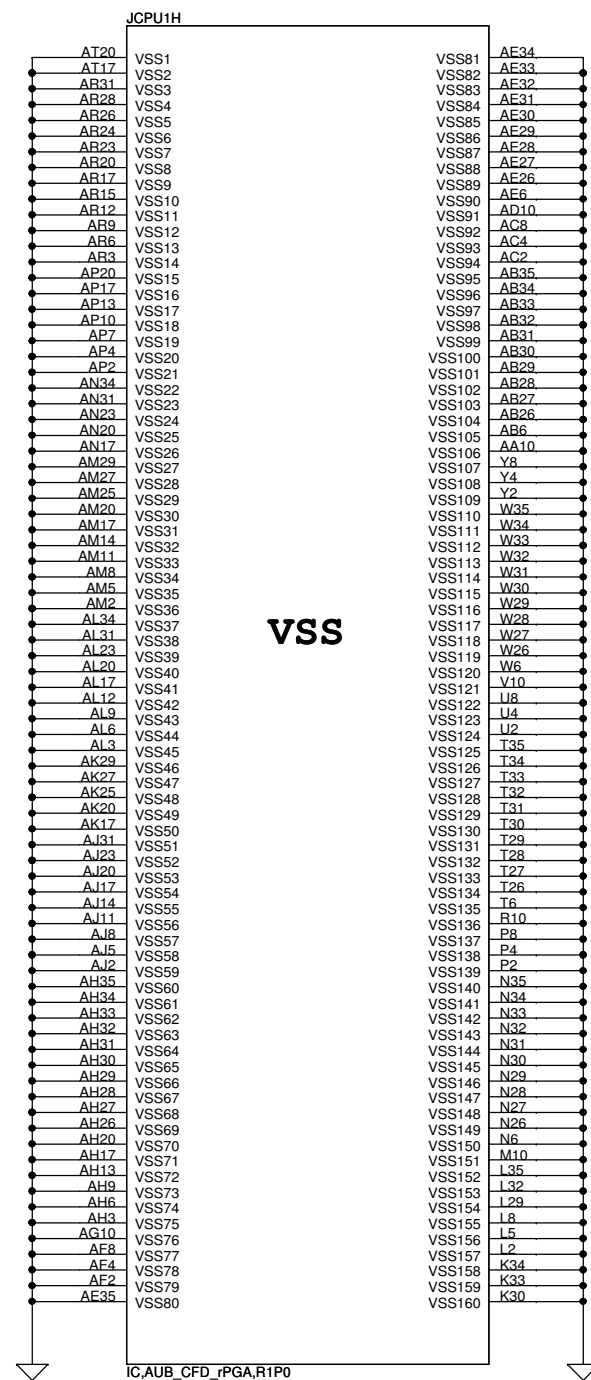


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Size	Custom	Document Number	NIWBA_LA5371P		Rev 0.2
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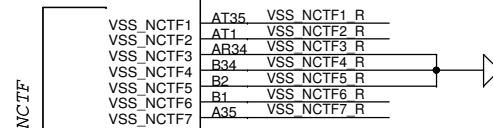




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+CPU_CORE = 12*0805 22uf  INSIDE CAVITY
              7*0805 10uf  UNDER CAVITY AND 9*0805 10uf  BETWEEN INDUCTOR AND SOCKET ON TOP LAYER
              4*470uf/4m ohm 2*470uf
```



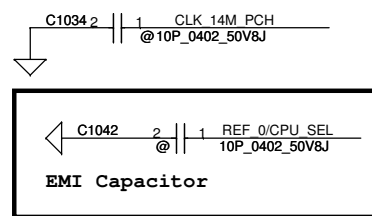
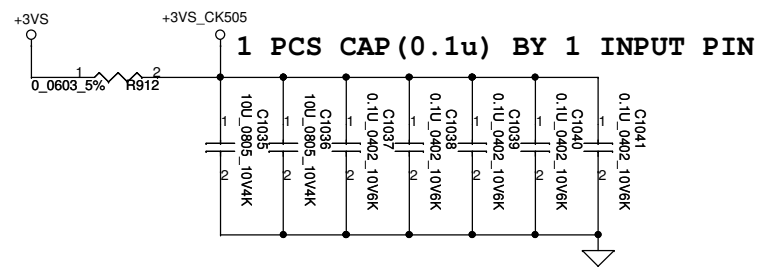
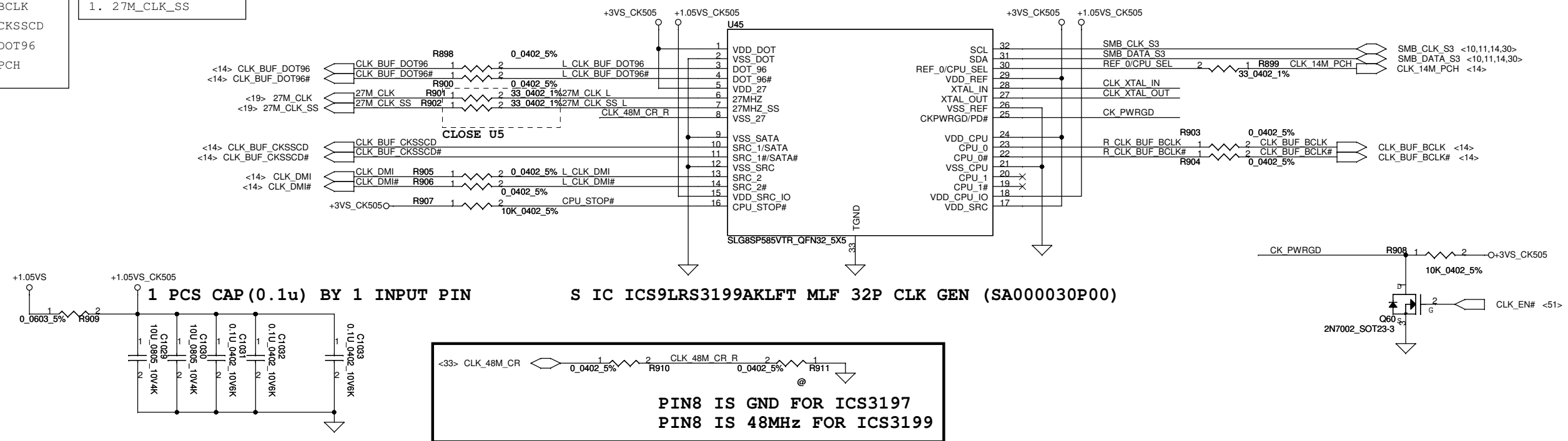
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								Size	Document Number					Rev
								Custom	NIWBA_LA5371P					0.2
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CLK GEN TO PCH

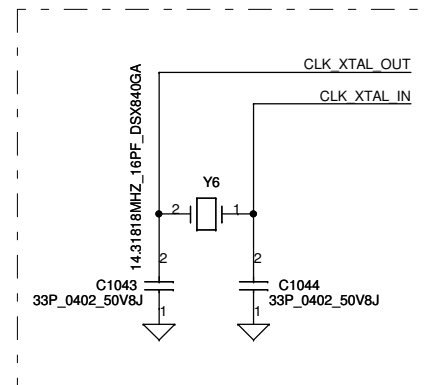
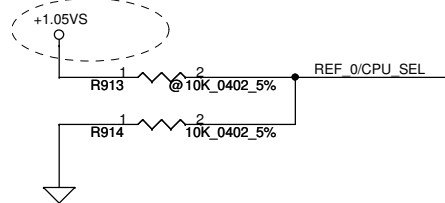
1. CLK_DMI
2. CLK_BUF_BCLK
3. CLK_BUF_CKSSCD
4. CLK_BUF_DOT96
5. CLK_14M_PCH

CLK GEN TO VGA

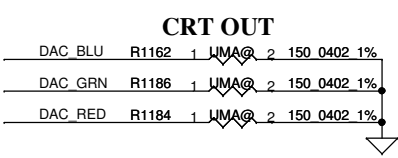
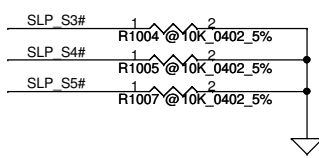
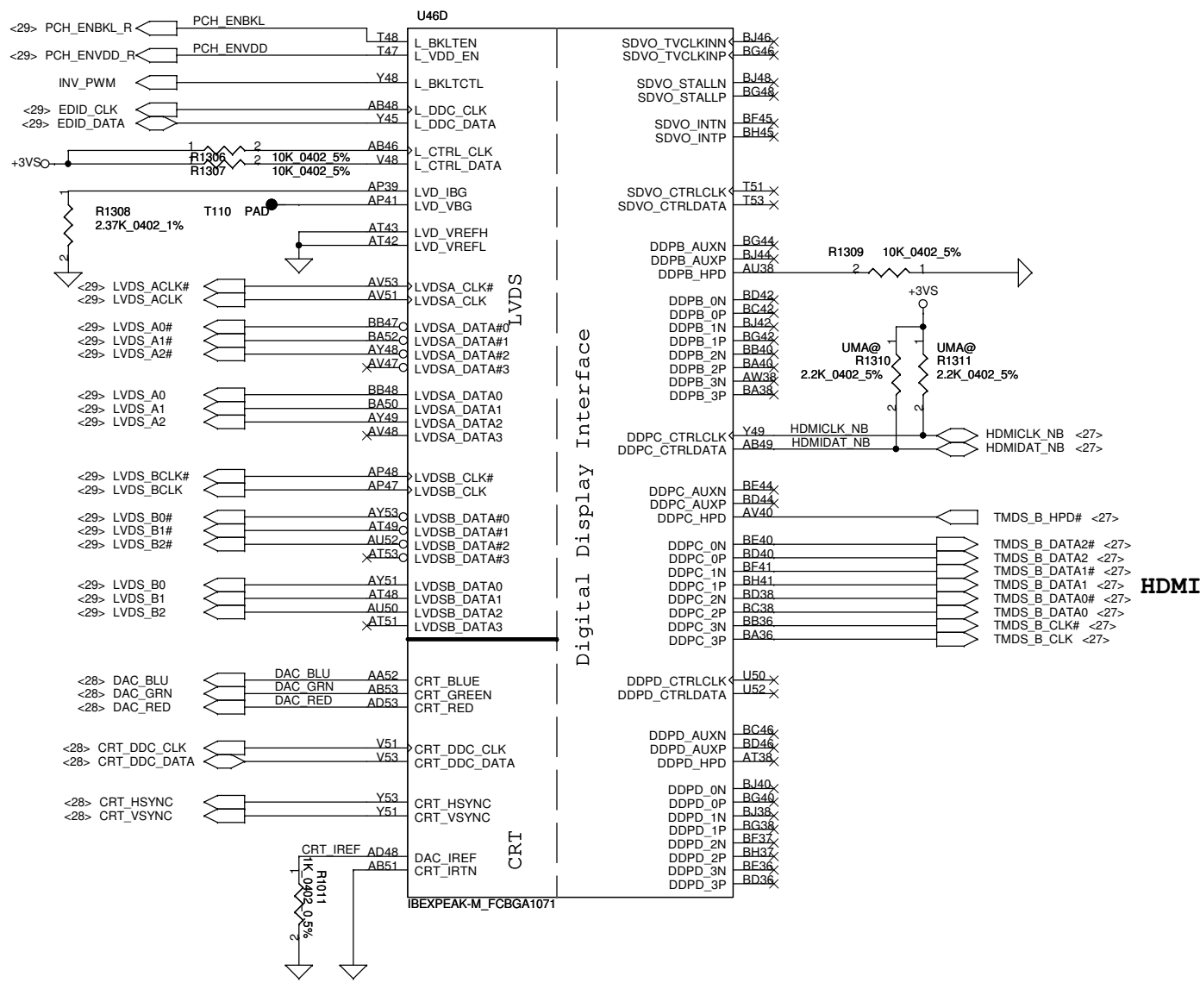
1. 27M_CLK
1. 27M_CLK_SS



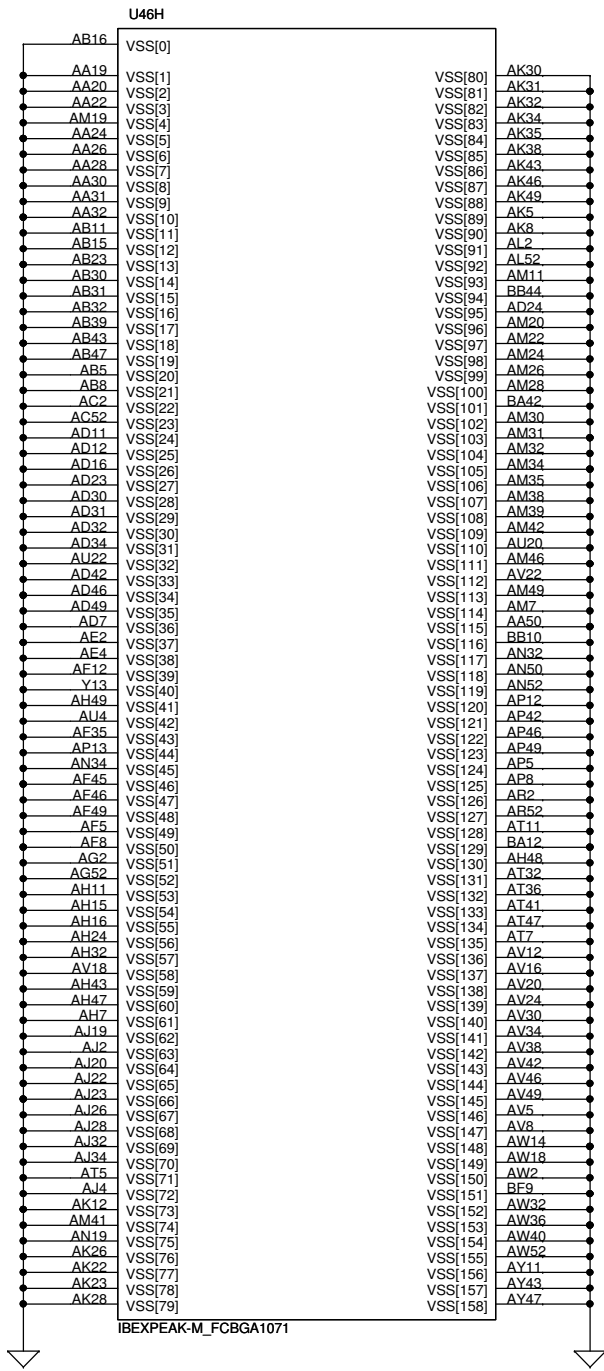
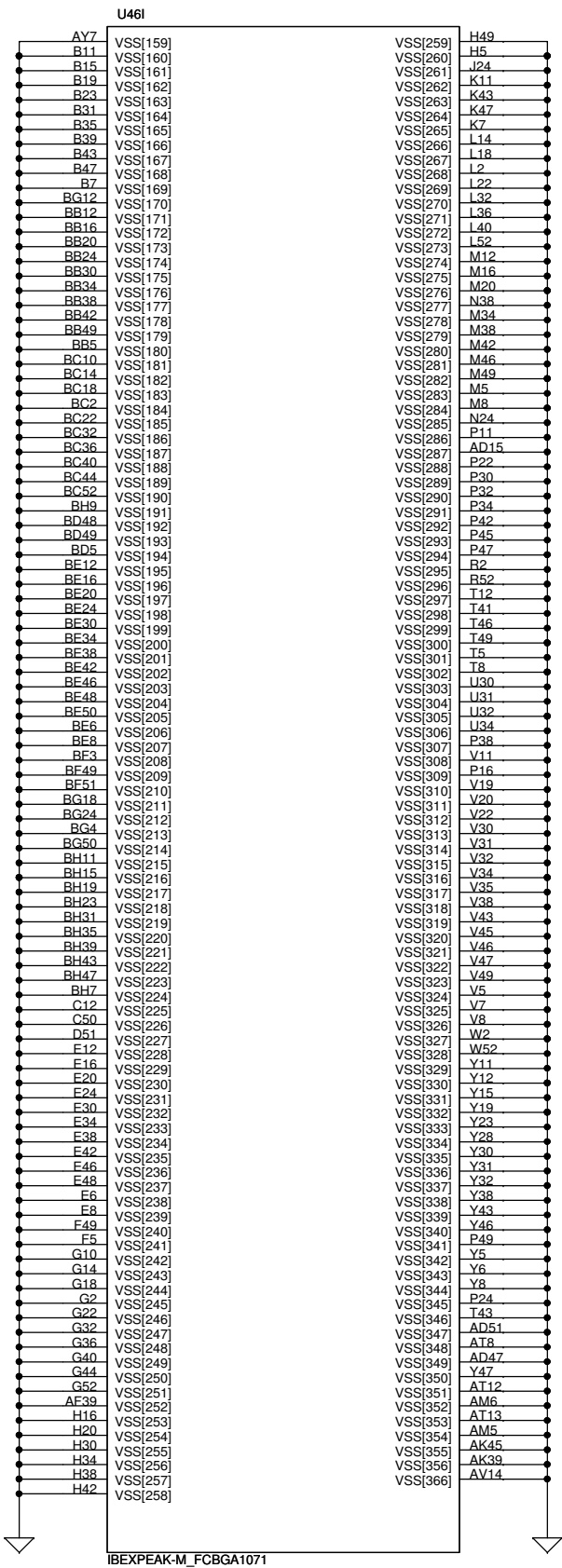
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



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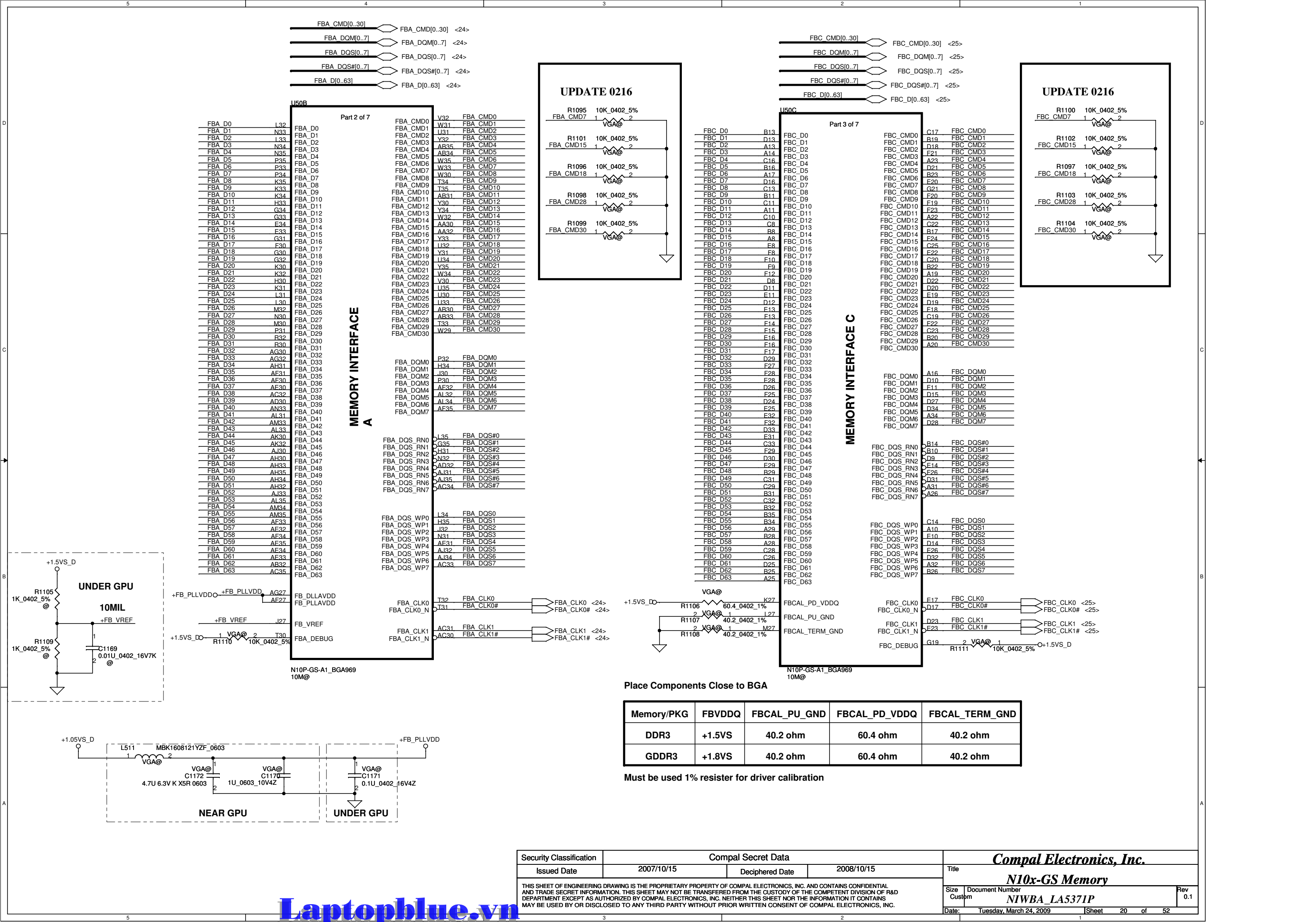


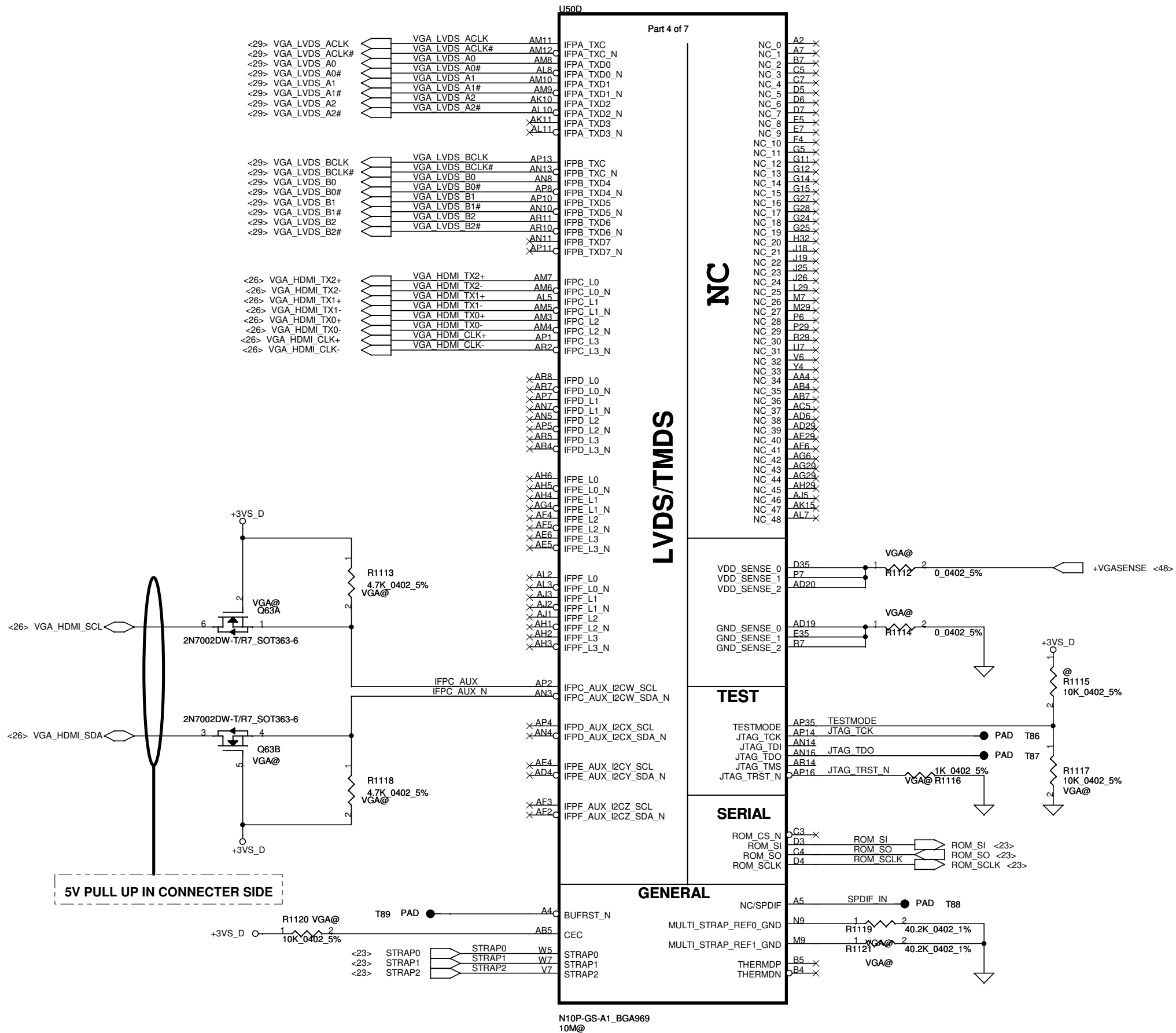
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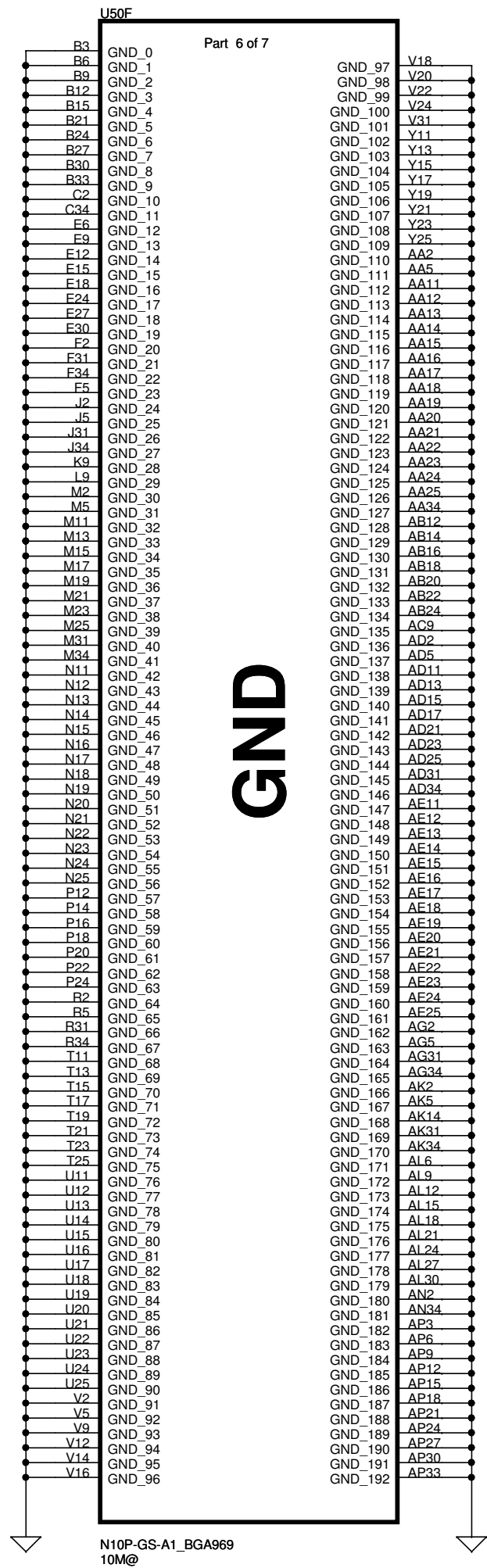


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				Size Custom	Rev 0.2
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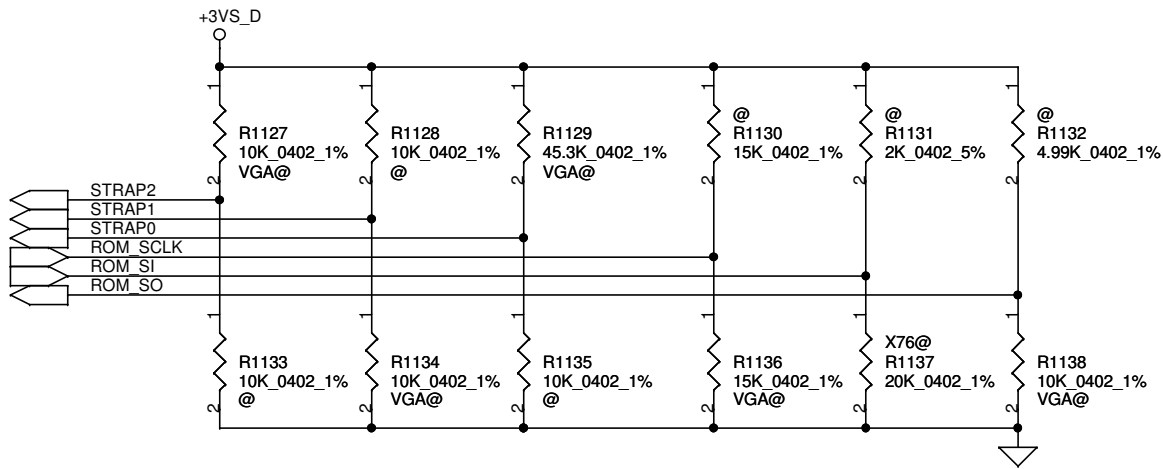
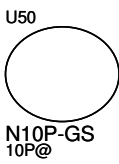
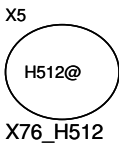
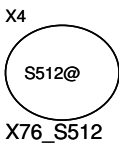
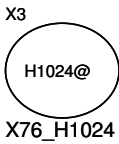
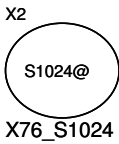








<21> STRAP2
<21> STRAP1
<21> STRAP0
<21> ROM_SCLK
<21> ROM_SI
<21> ROM_SO



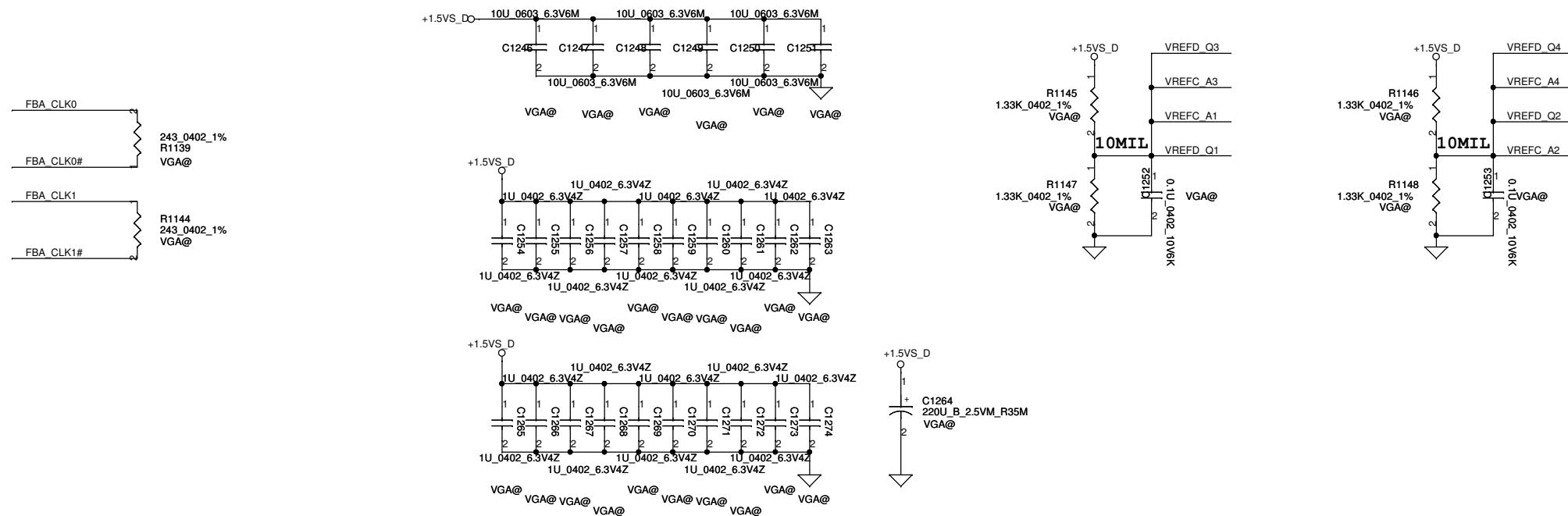
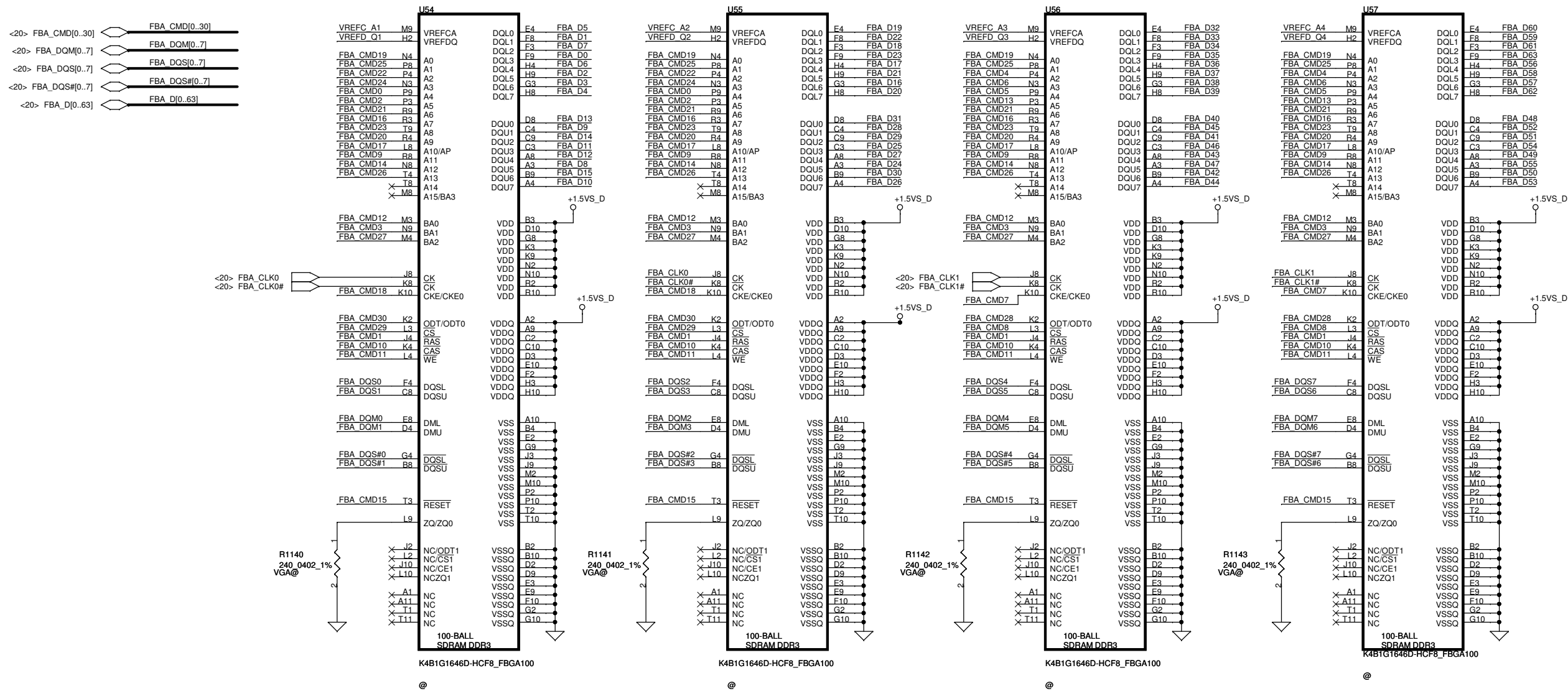
GB1 Family GPU Strap Options

		GPU DEVID	RAM_CFG	GPU DEVID				
GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
N10P-GS (0xA34)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
N10M-GS (0xA74)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

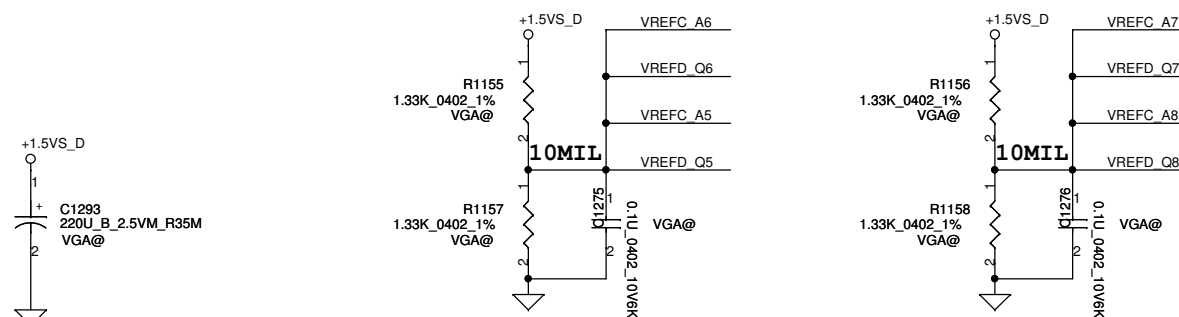
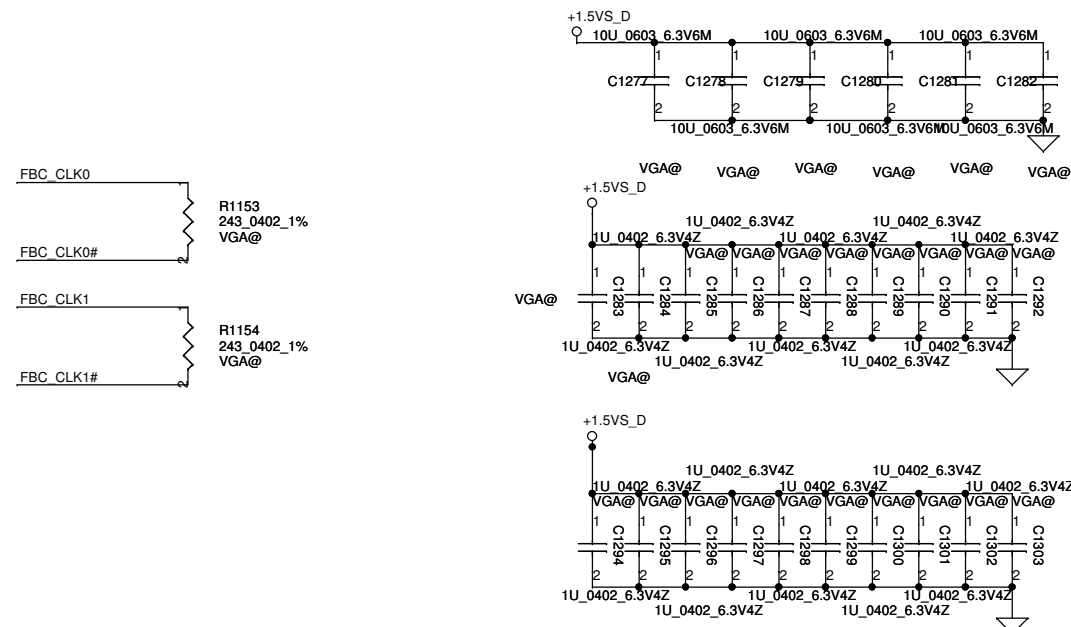
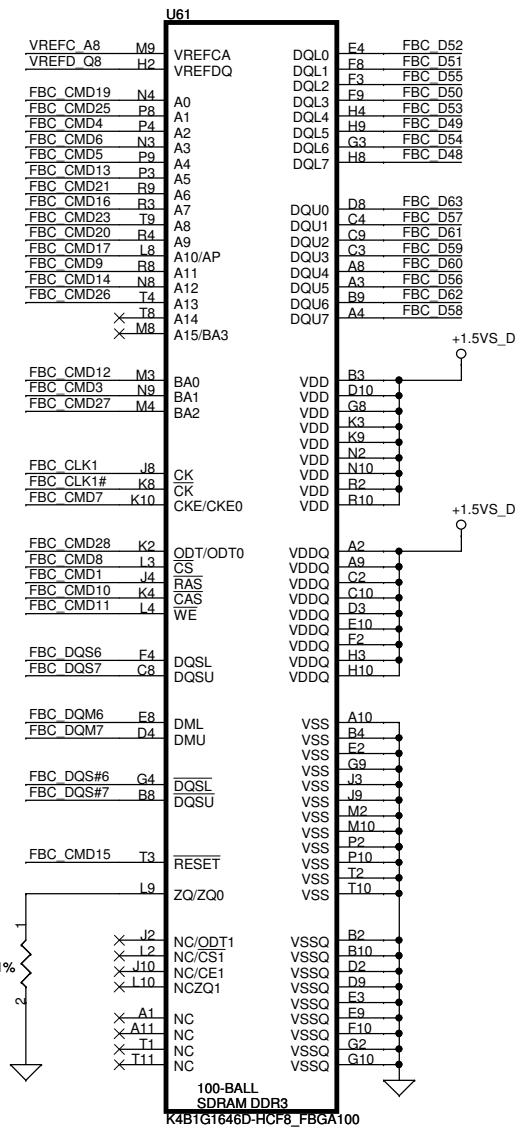
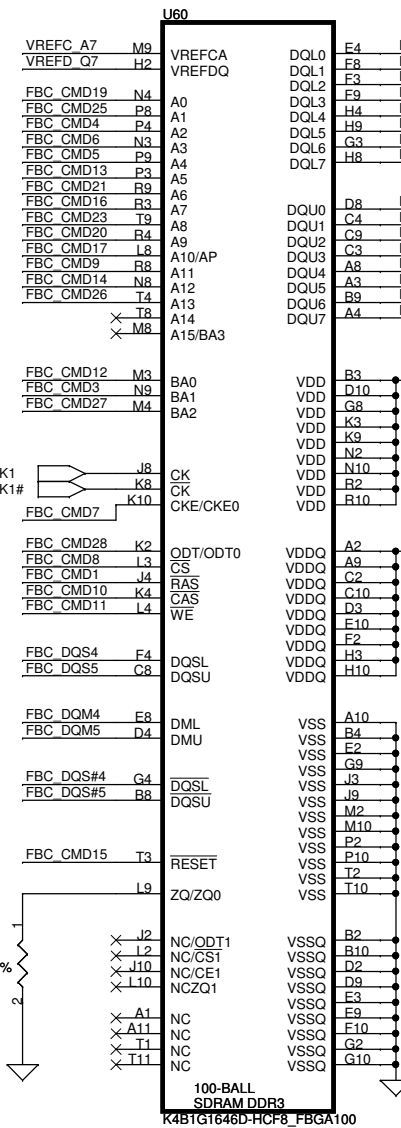
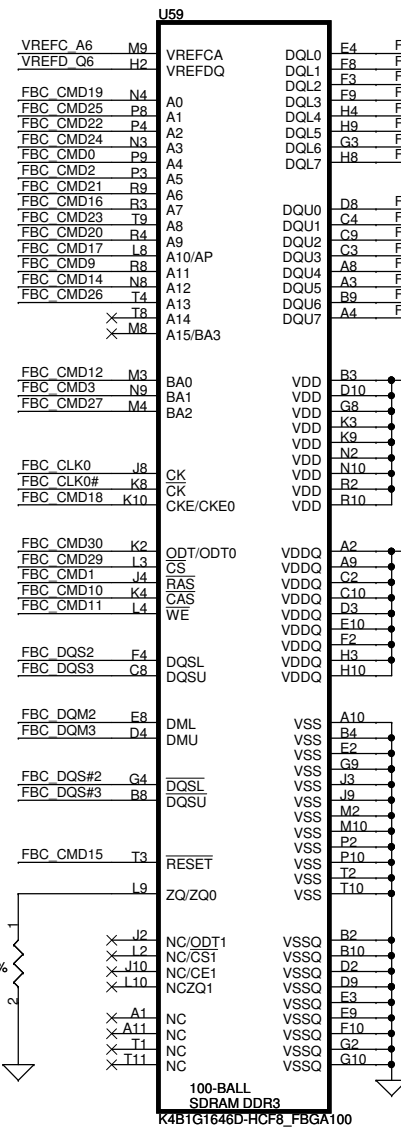
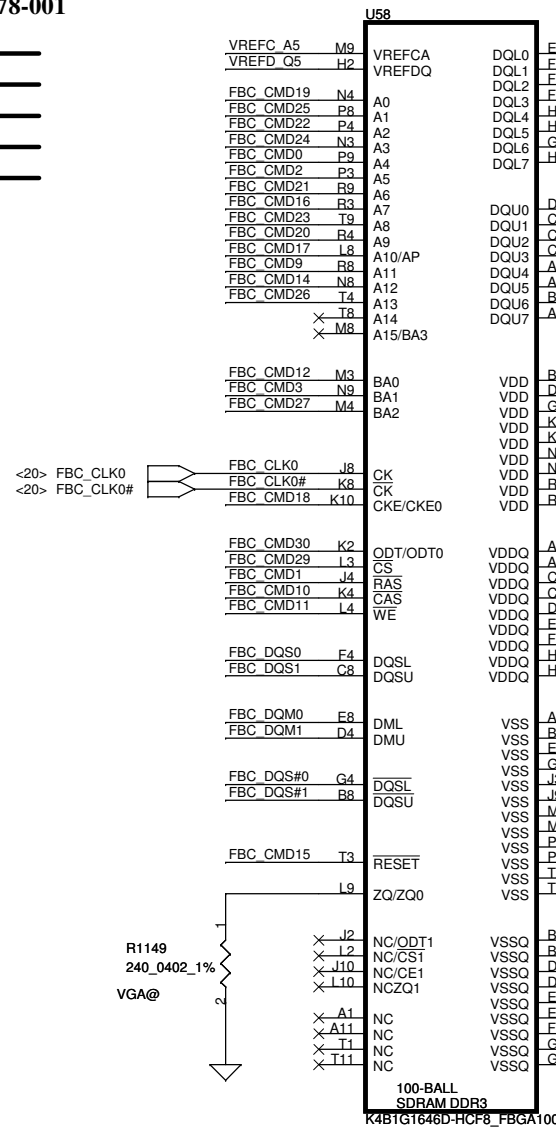
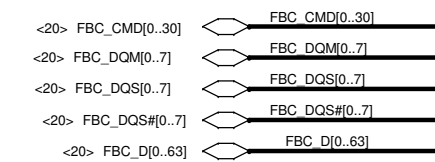
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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	
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				Size Custom	Rev 0.1
				Date: Tuesday, March 24, 2009	Sheet 23 of 52

N10x 40nm DDR3 MAPPING
NVIDIA COCUMENT FOR DA-3978-001



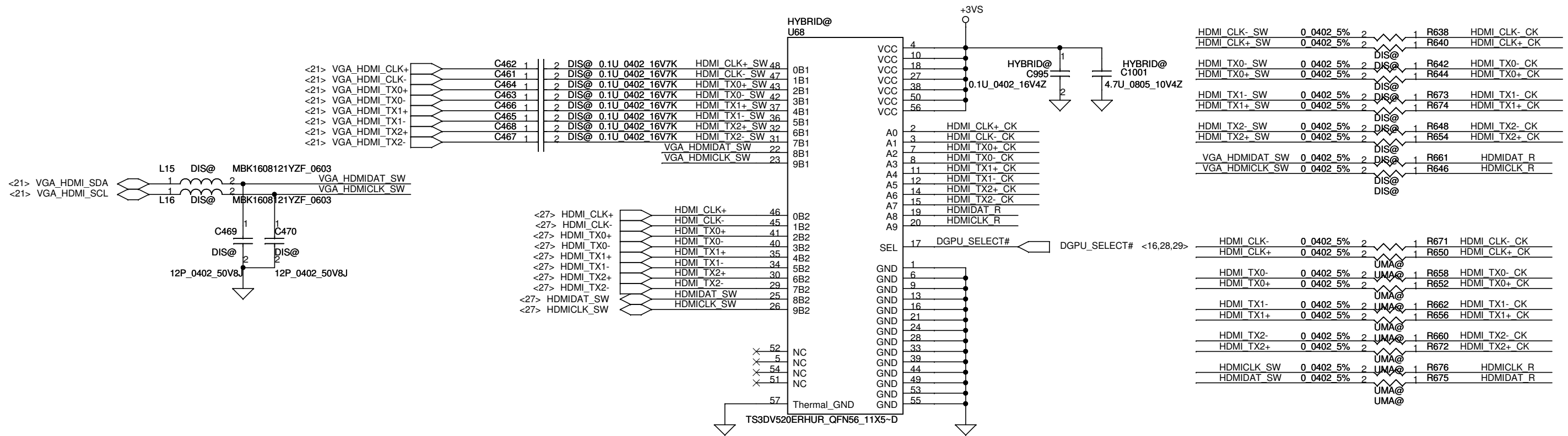
Security Classification		Compal Secret Data		Compal Electronics, Inc. VRAM DDRA	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				Document Number	
				NIWBA_LA5371P	
Date: Tuesday, March 24, 2009		Sheet 24 of 52			

N10x 40nm DDR3 MAPPING
NVIDIA COCUMENT FOR DA-3978-001

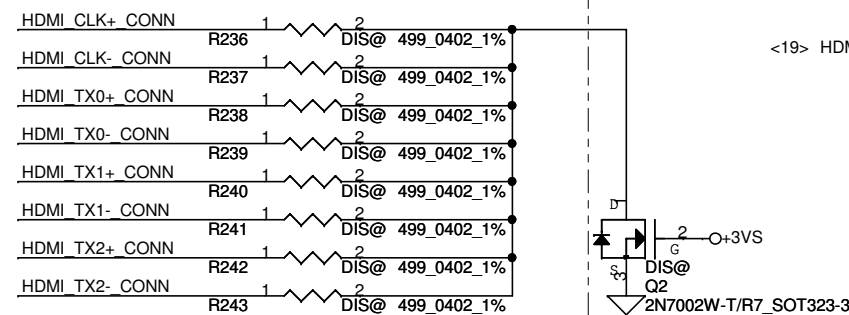


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title VRAM DDRA		
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				Custom	NIWBA_LA5371P	0.1
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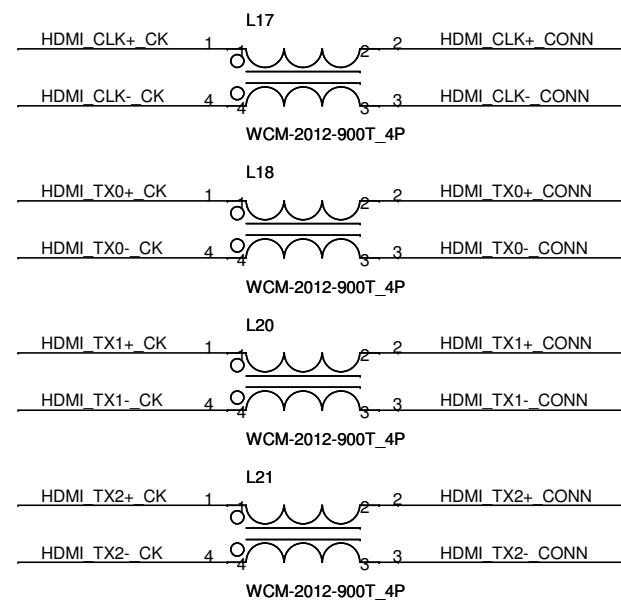
HDMI switch1



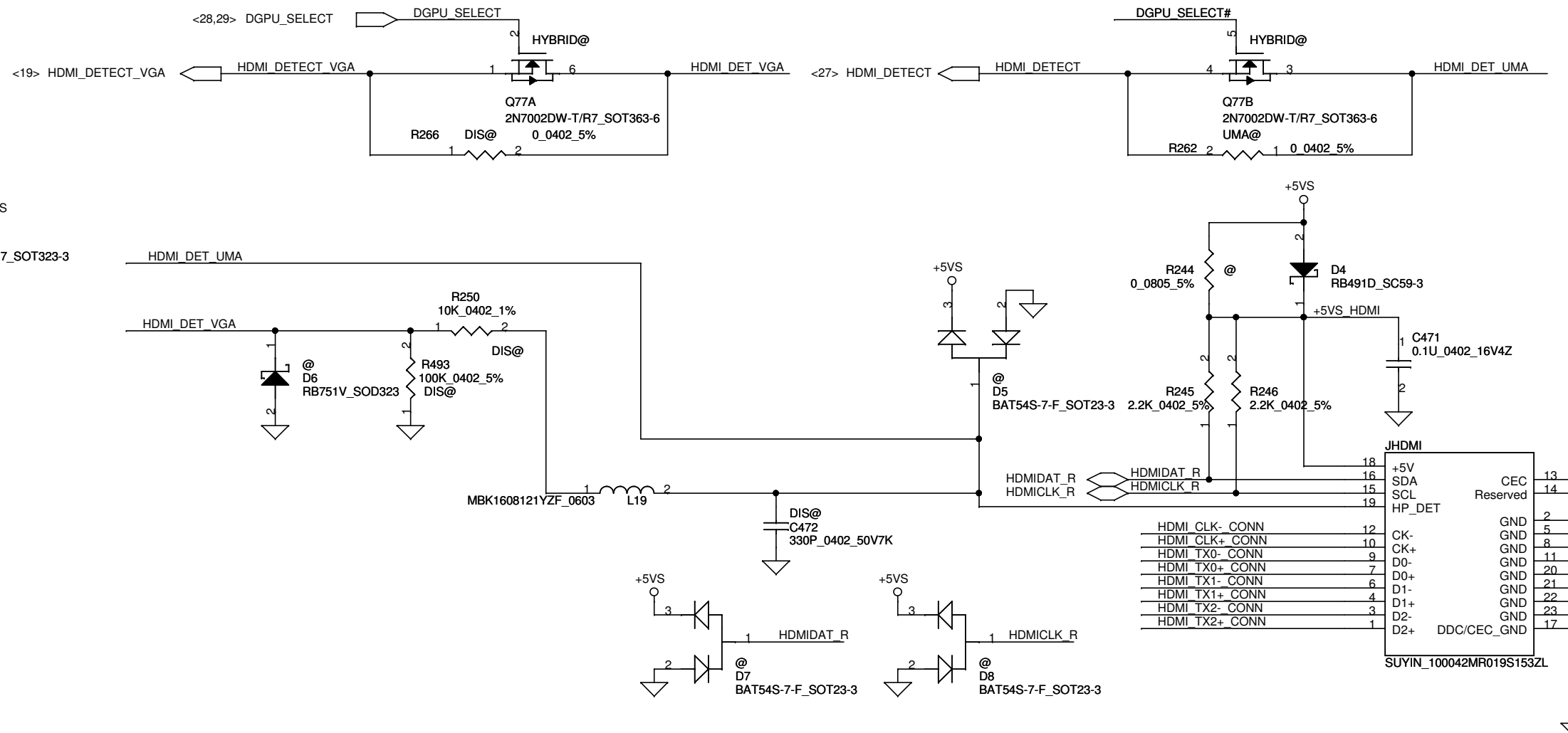
TMDS pull down (500ohm) resistors G9x only



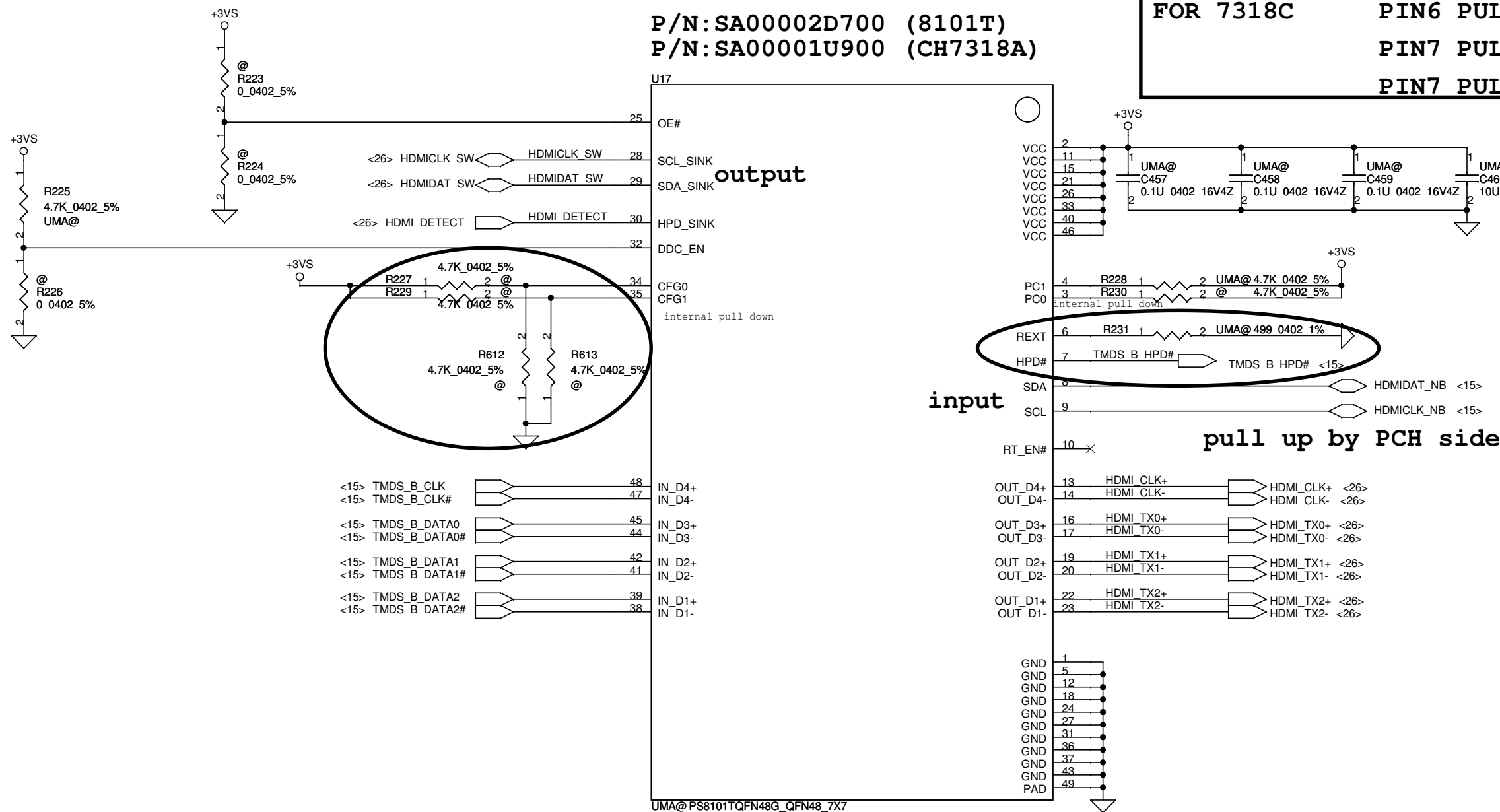
NEAR CONNECT



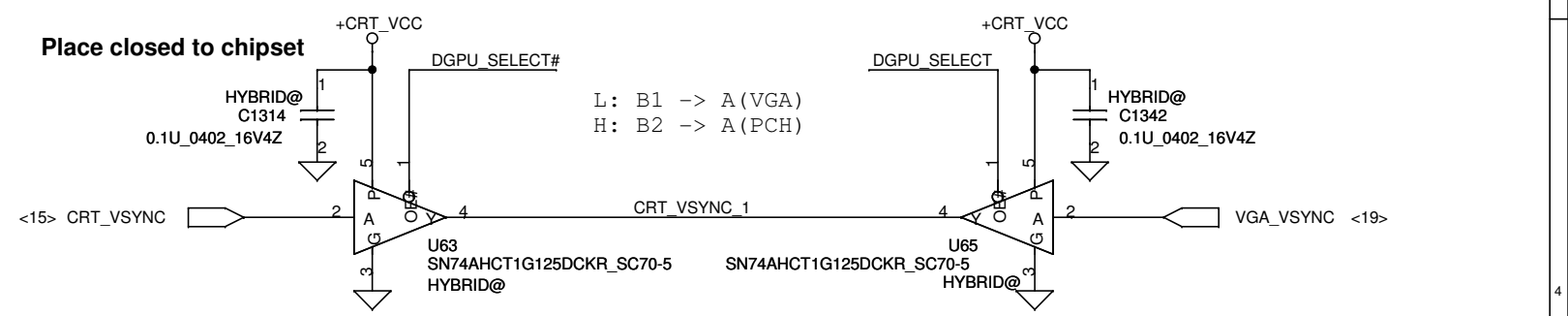
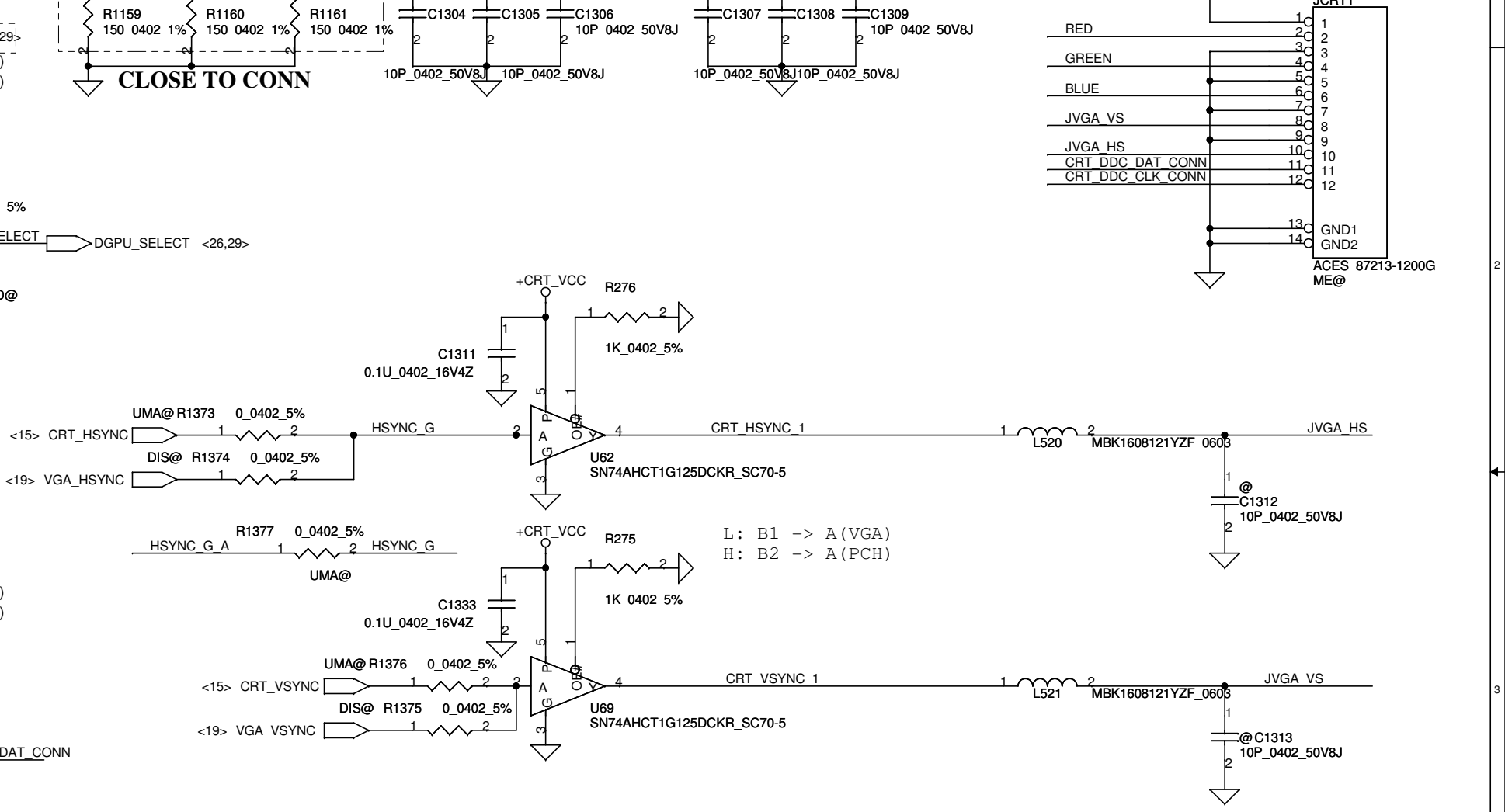
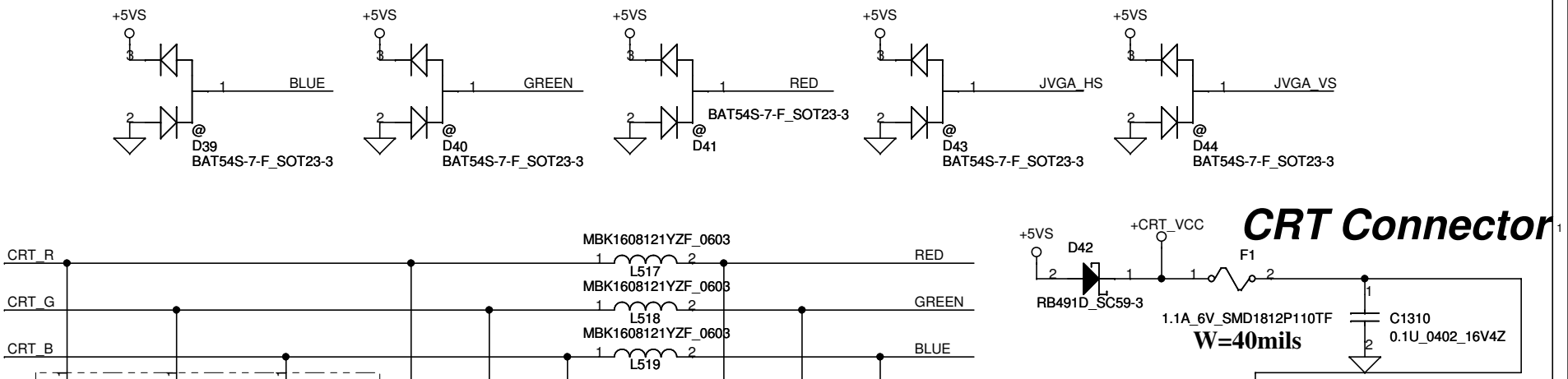
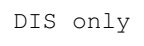
HDMI CLK+ CK	R251	1	@	2	0	0402	5%	HDMI CLK+ CONN
HDMI CLK- CK	R252	1	@	2	0	0402	5%	HDMI CLK- CONN
HDMI TX0+ CK	R253	1	@	2	0	0402	5%	HDMI TX0+ CONN
HDMI TX0- CK	R254	1	@	2	0	0402	5%	HDMI TX0- CONN
HDMI TX1+ CK	R255	1	@	2	0	0402	5%	HDMI TX1+ CONN
HDMI TX1- CK	R256	1	@	2	0	0402	5%	HDMI TX1- CONN
HDMI TX2+ CK	R257	1	@	2	0	0402	5%	HDMI TX2+ CONN
HDMI TX2- CK	R258	1	@	2	0	0402	5%	HDMI TX2- CONN



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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Level Shiftter_PS8101T
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				Custom	<i>KIWB1/B2_LA4601P</i>
				Date: Tuesday, March 24, 2009	Sheet 26 of 52

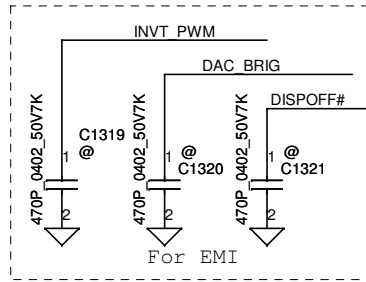
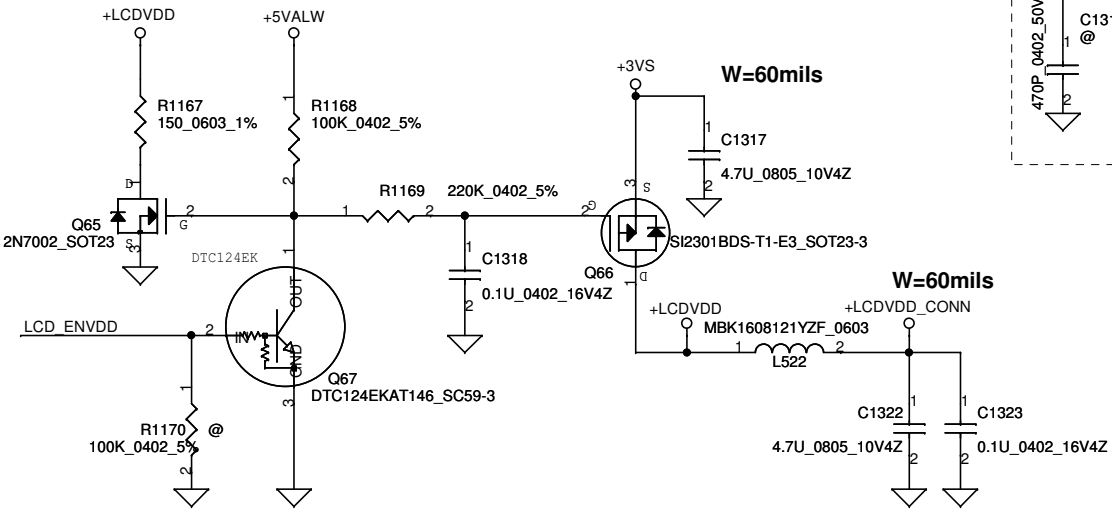


Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
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Size	Custom	Document Number	KIWB1/B2_LA4601P		Rev
Date: Tuesday, March 24, 2009		Sheet 27 of 52		0.1	

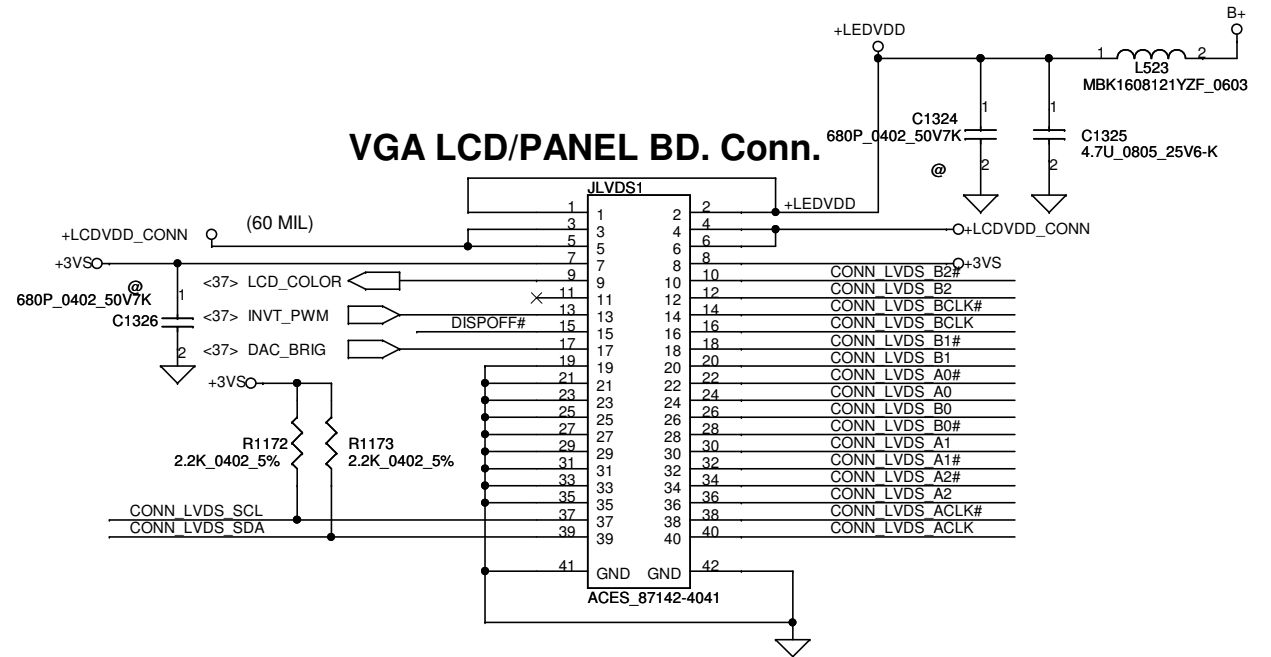


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Issued Date		2007/10/15	Deciphered Date	2008/10/15	Title		
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					Size	Document Number	Rev
					Custom	NIWBA_LA5371P	0.1
Date:		Tuesday, March 24, 2009		Sheet 28 of 52			
C		D		E			

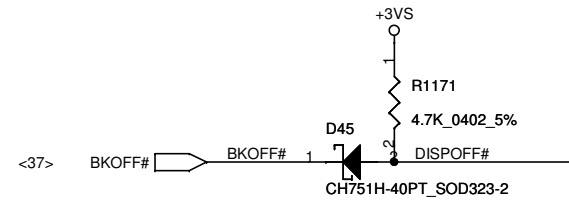
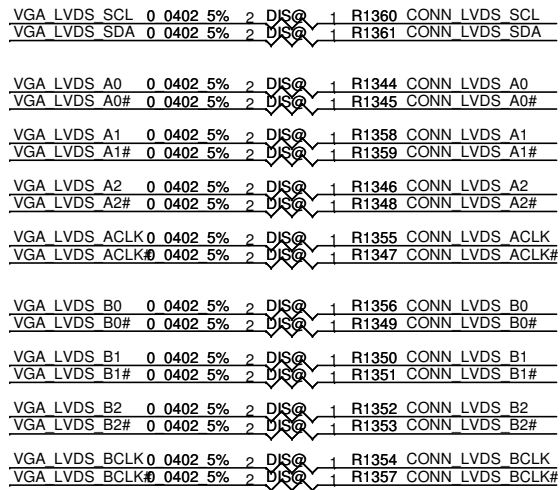
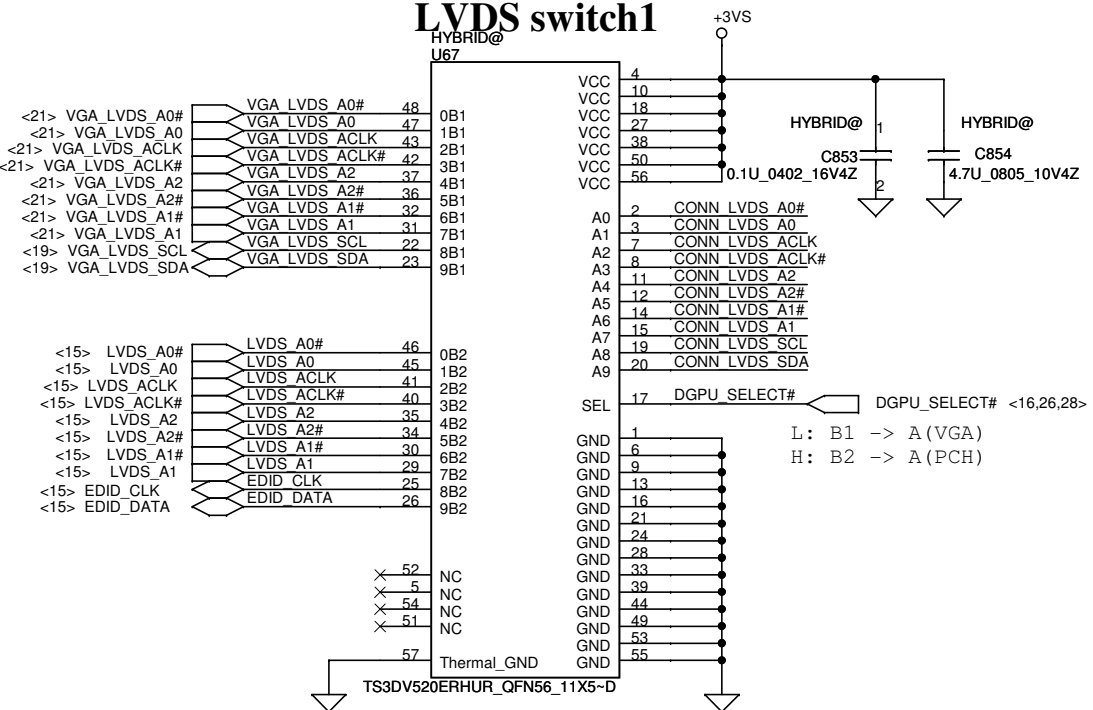
LCD POWER CIRCUIT



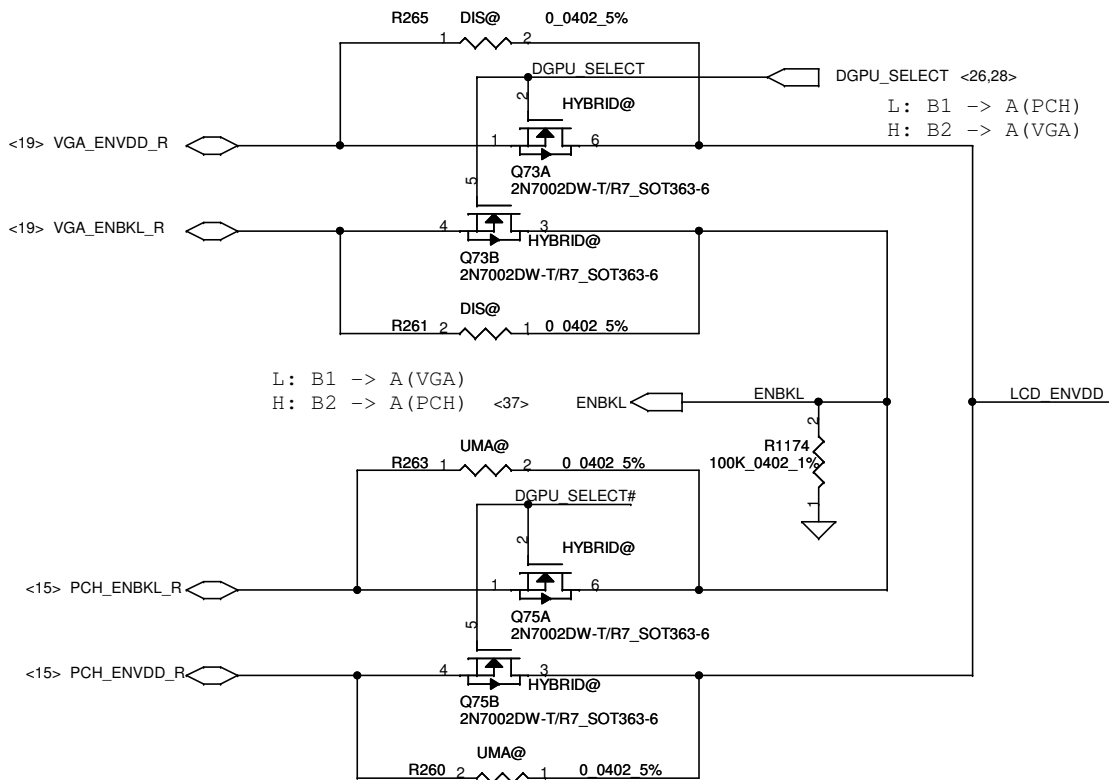
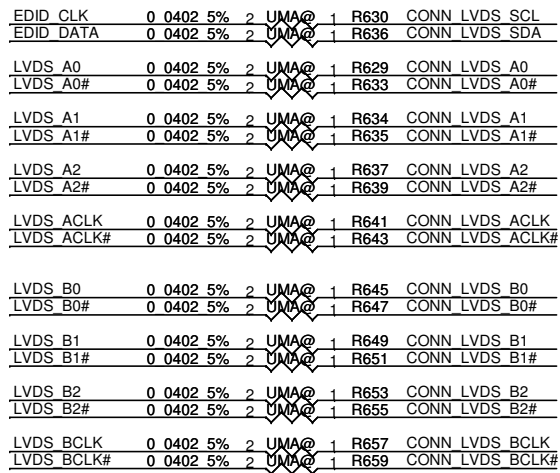
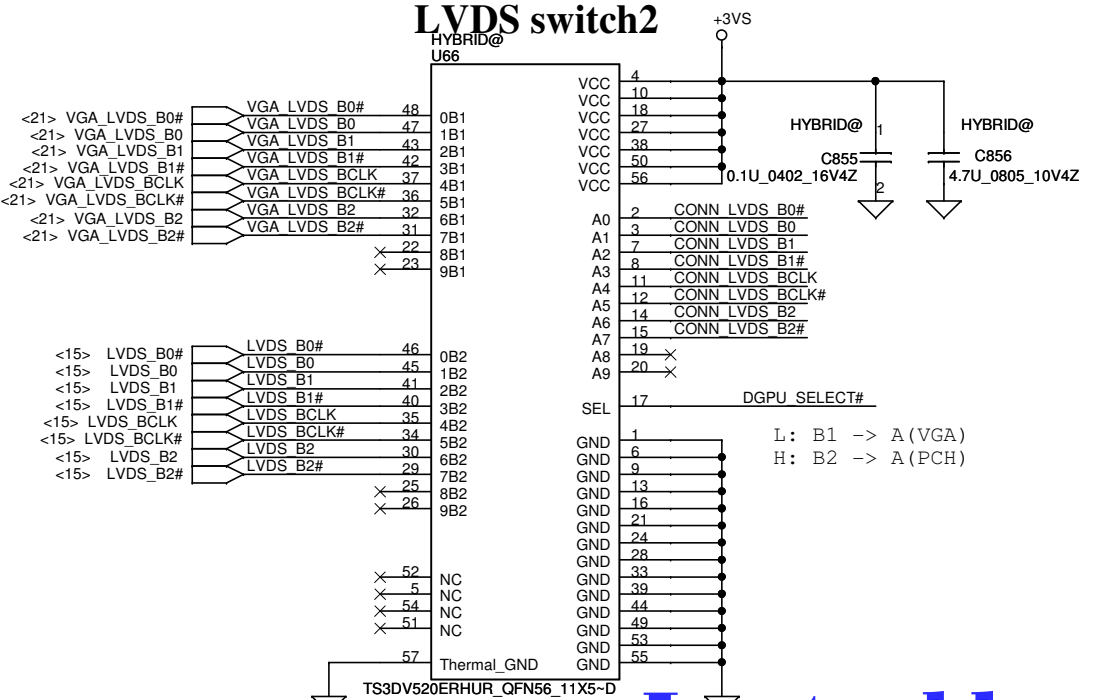
VGA LCD/PANEL BD. Conn.



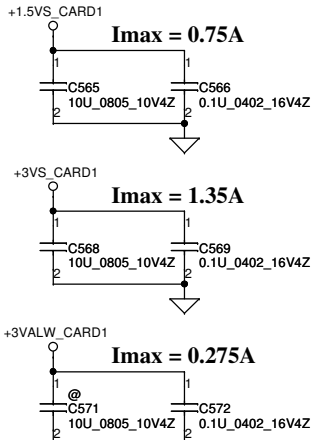
LVDS switch1



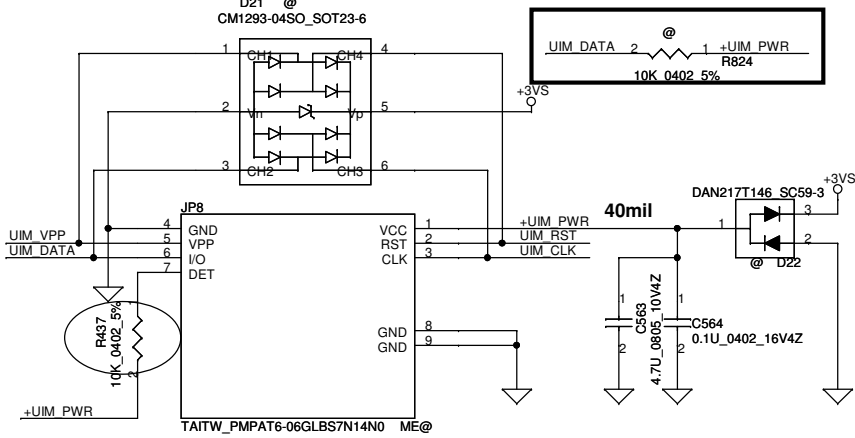
LVDS switch2



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Mini-Express Card(Slot 1-TV TUNNER) 4.0mm high

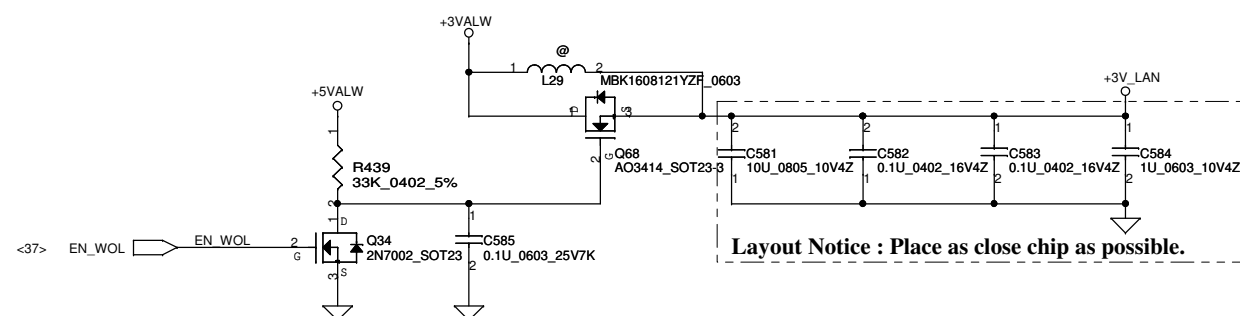
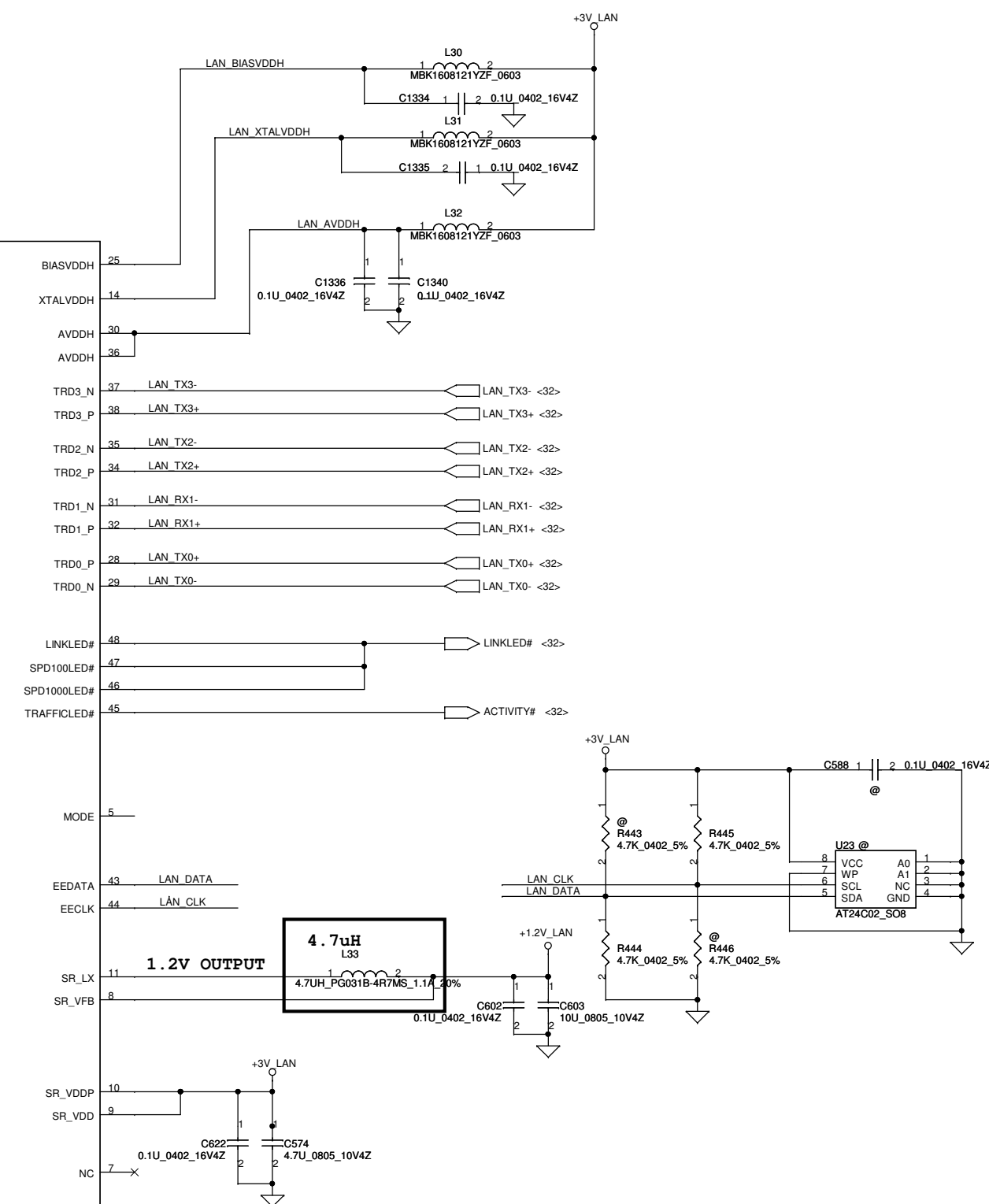
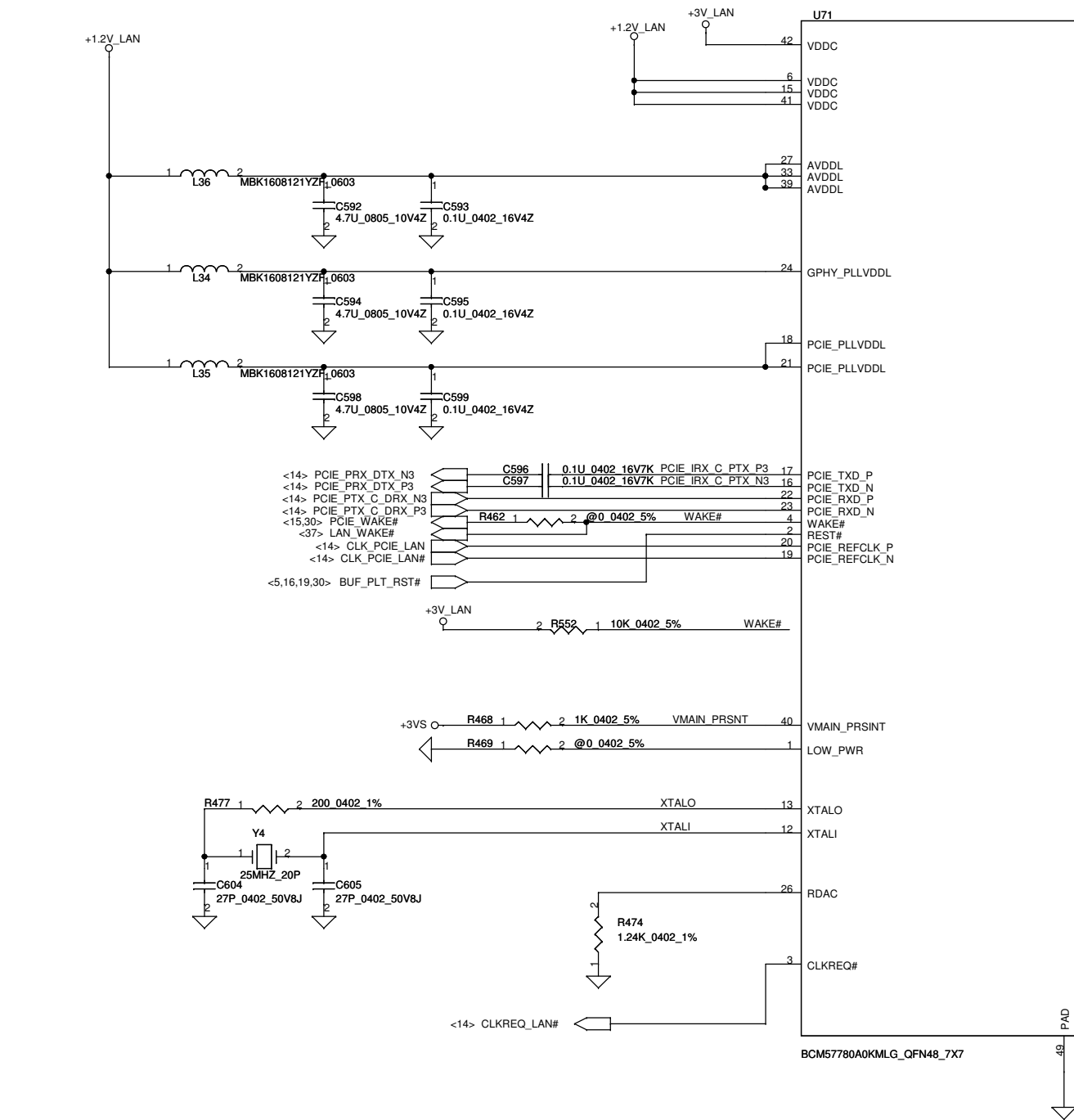
5.6mm high

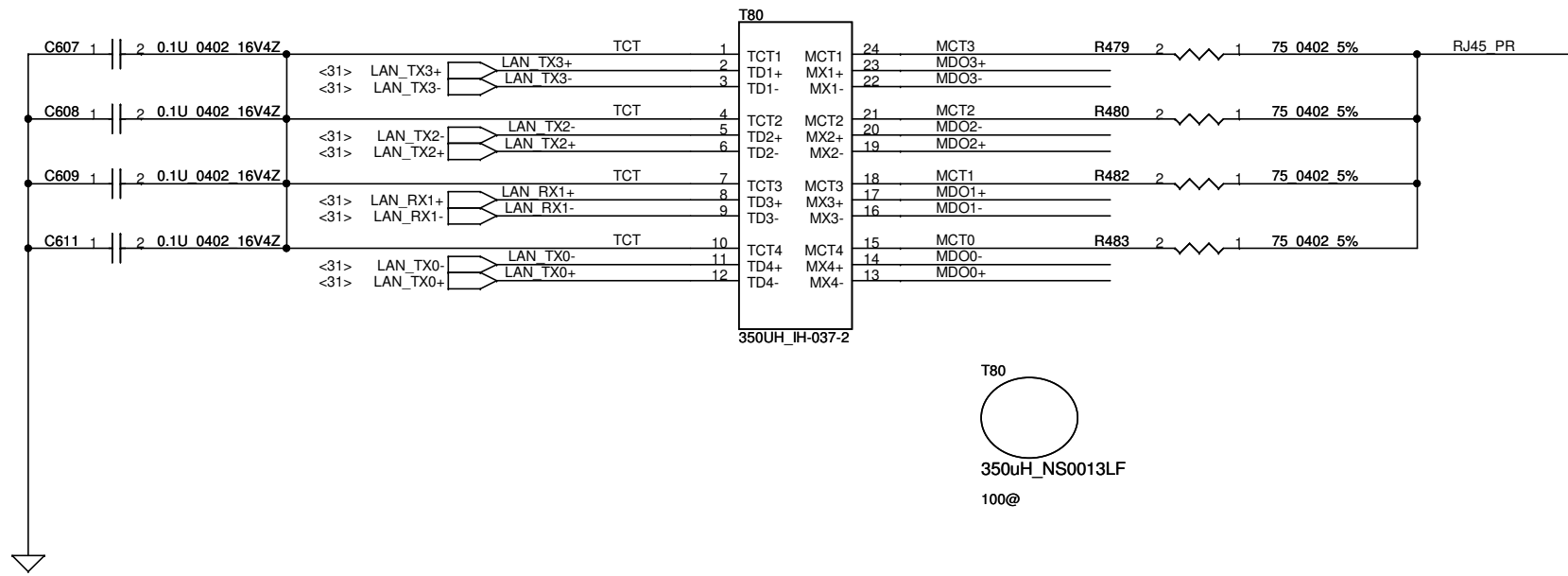


Pin	Signal
1	GND
2	USB20 N10
3	USB20 P10
4	CPUSB#
5	RSV
6	RSV
7	SMB_CLK
8	SMB_DATA
9	+1.5V_CARD1
10	+1.5V
11	WAKE#
12	+3.3VAUX
13	PERST#
14	+3VS_CARD1
15	CPUSB#
16	CPUSB#
17	CPUSB#
18	REFCLK+
19	REFCLK-
20	GND
21	GND
22	PERn0
23	PERp0
24	GND
25	PETn0
26	PETp0
27	GND
28	GND

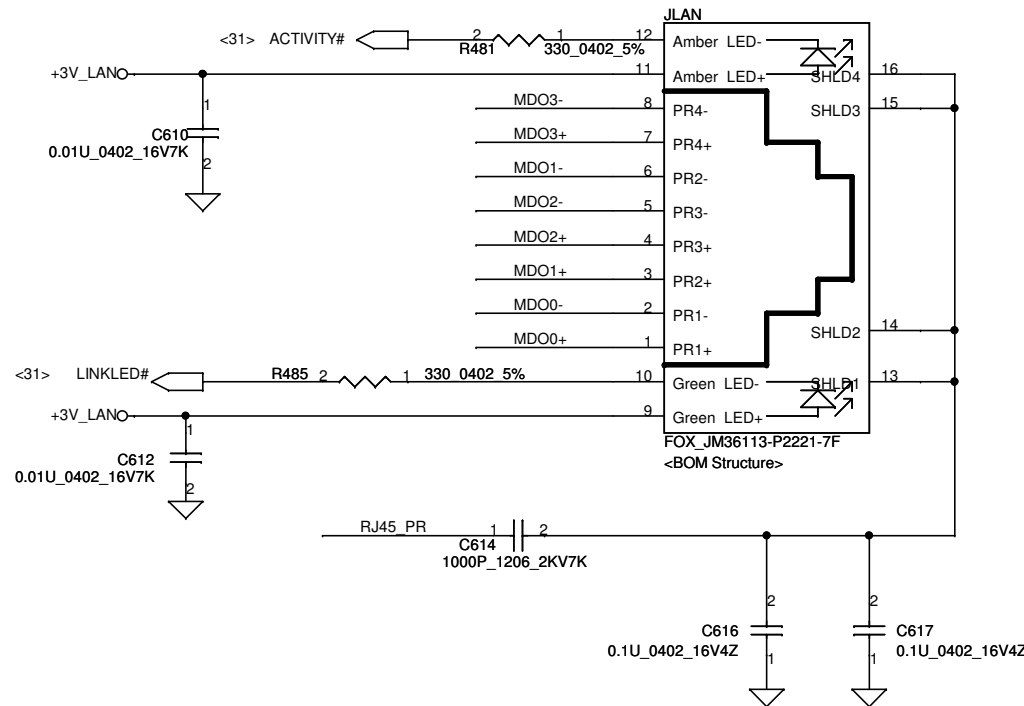
SANTA_130832-I

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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	Mini-Card/3G/FeliCa/BT		
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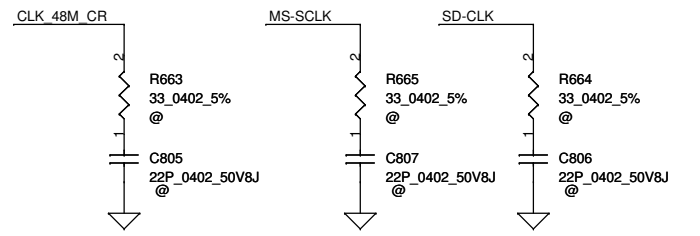
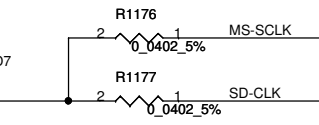
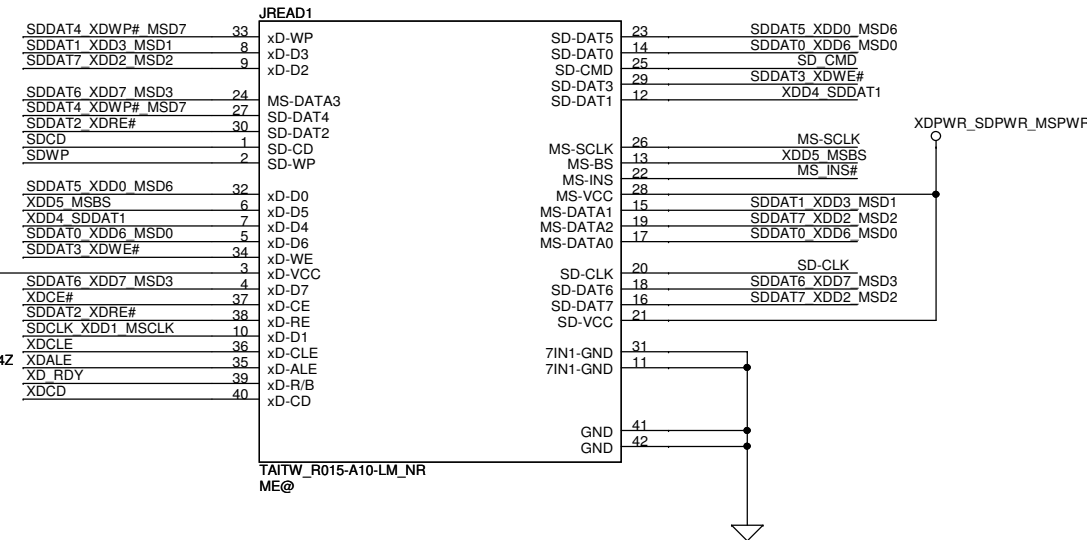
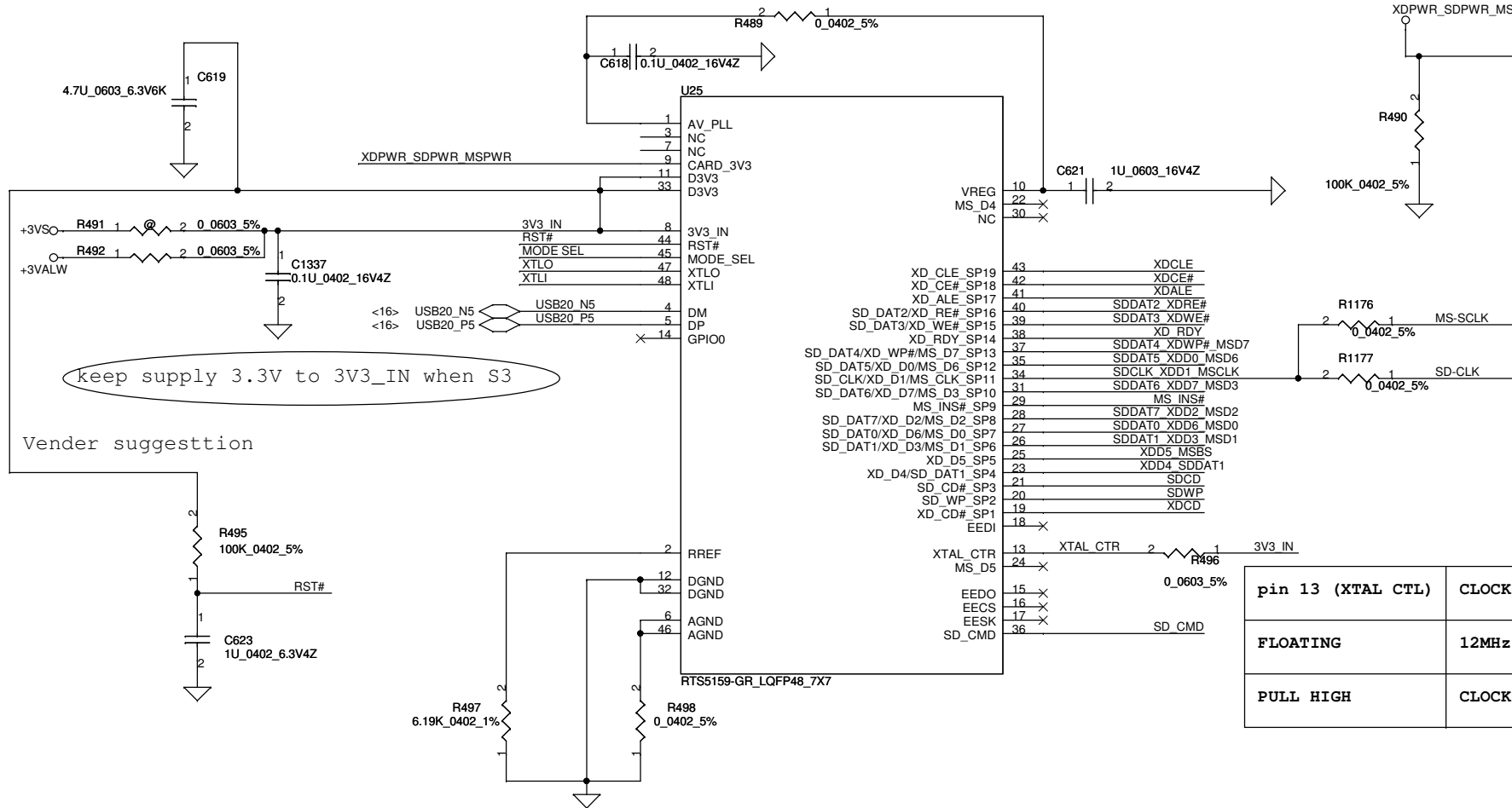


RJ11+RJ45 CONN



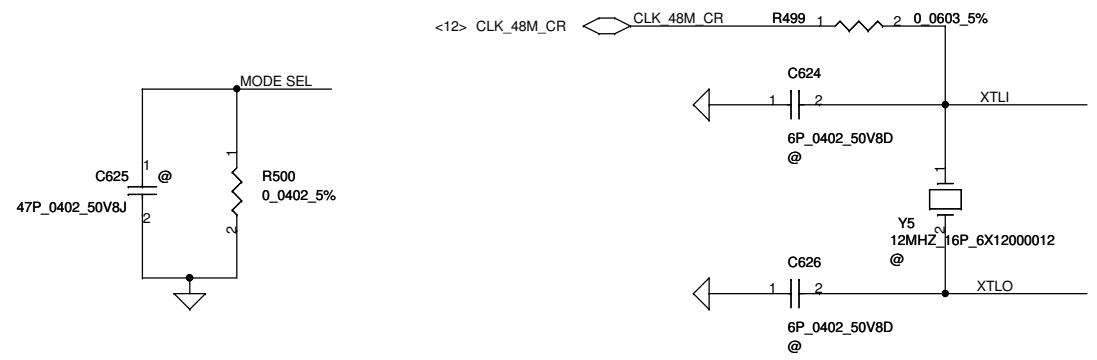
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				Size Custom	Document Number
				KIWB1/B2_LA4601P	
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0513 : CARD_3V3 旁路電阻 100K change to 4.7u CAP==>預留
0521 : change C79 form 4.7u to 0.1u, add R47 100K ohm,
change C526 form 1u to 4.7u

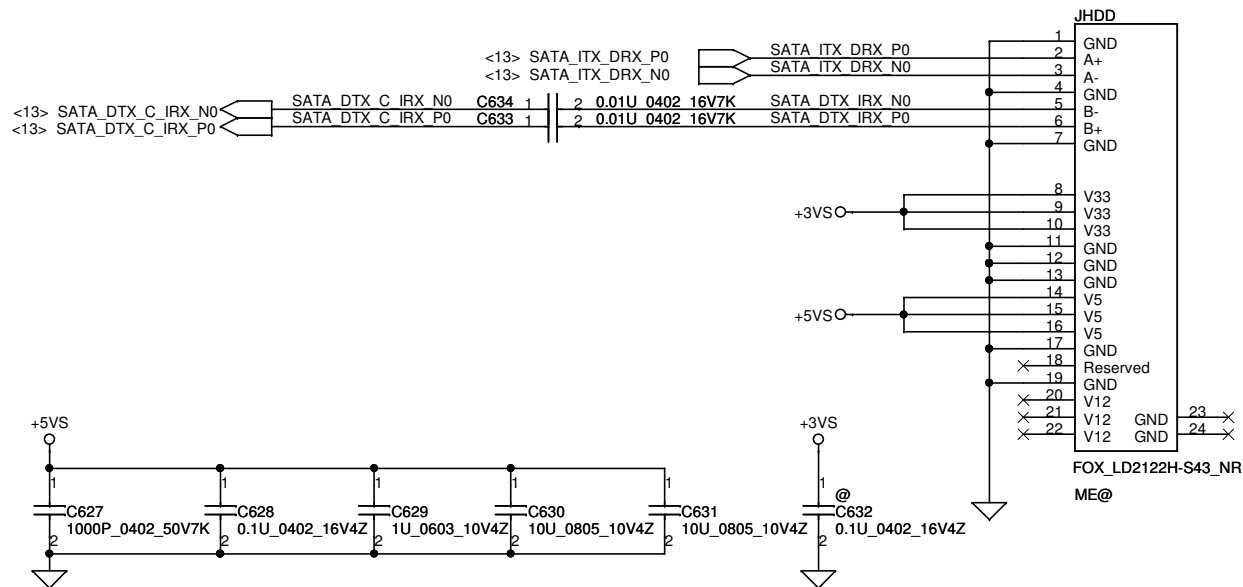


pin 13 (XTAL CTL)	CLOCK SOURCE	REMARK
FLOATING	12MHz CRYSTAL INPUT	
PULL HIGH	CLOCK GENERATOR'S 48MHZ INPUT	INPUT TO PIN48

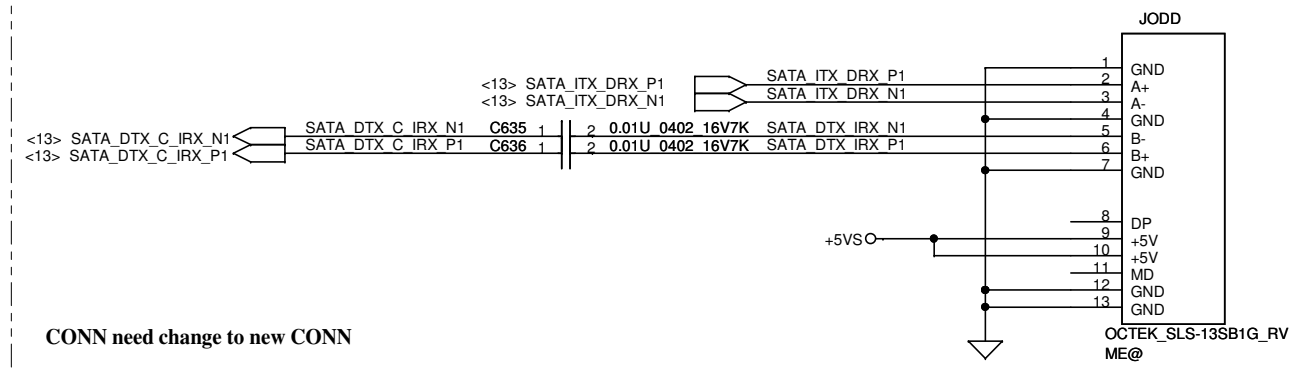
MCLK and SDCLK 該二電阻是預留給EMI solution使用, (但請靠近RTS5158E側).
將SD_DAT1 連接到RTS5158E的pin23



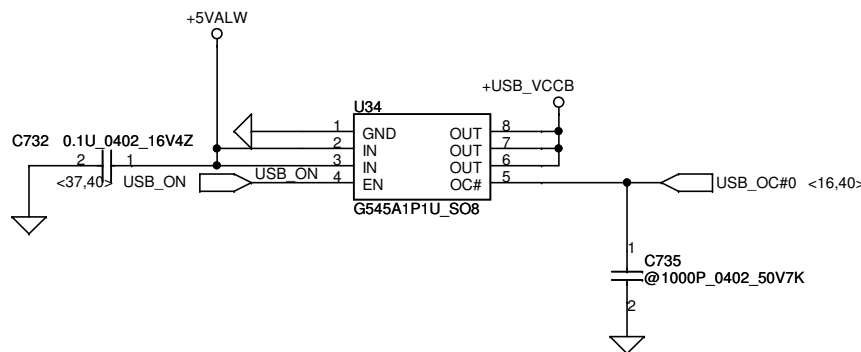
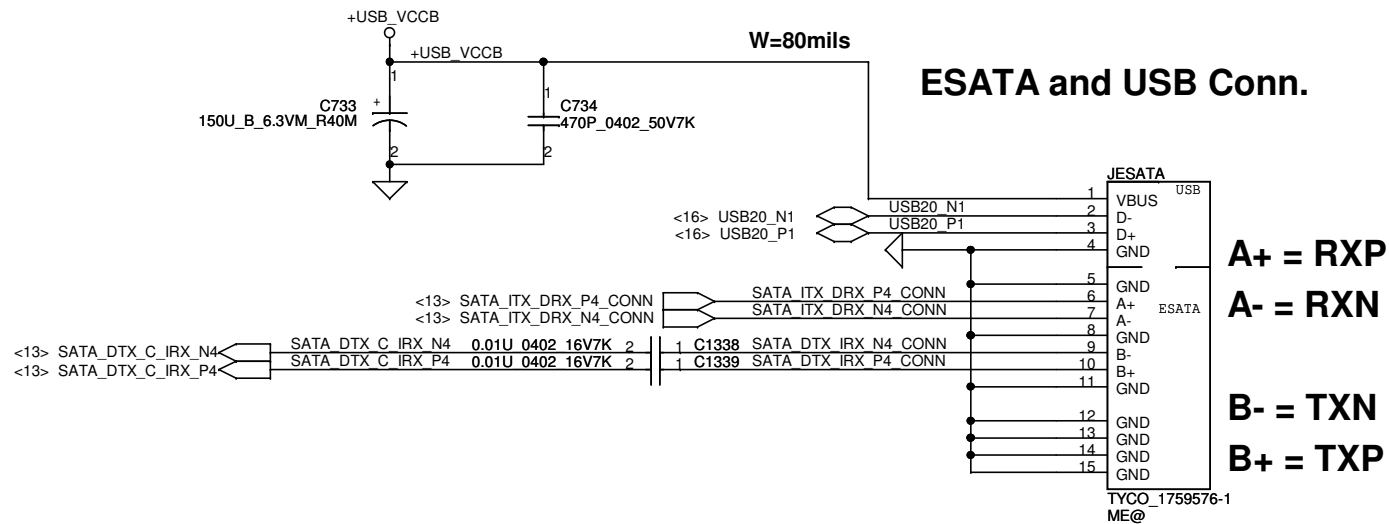
SATA HDD Conn.



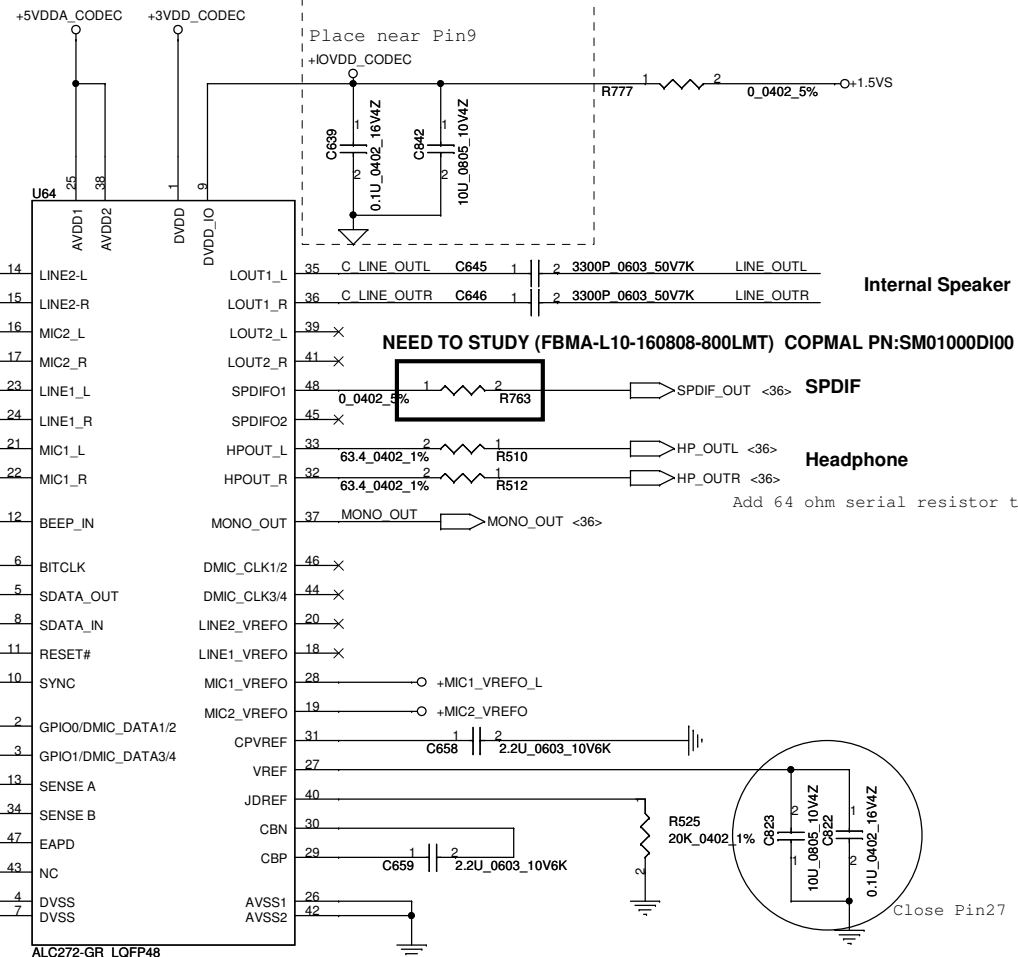
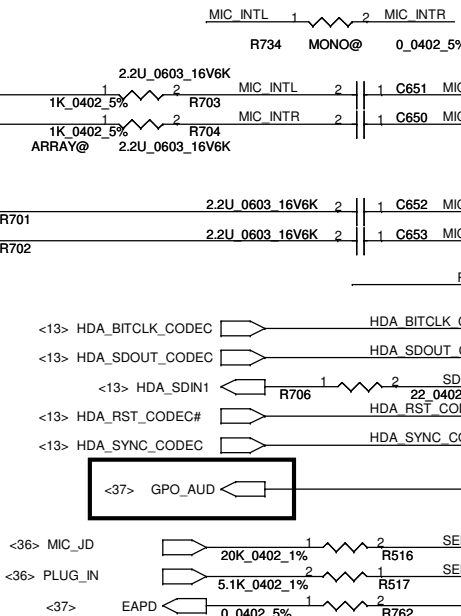
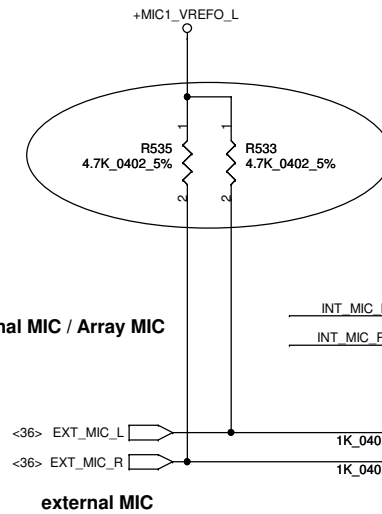
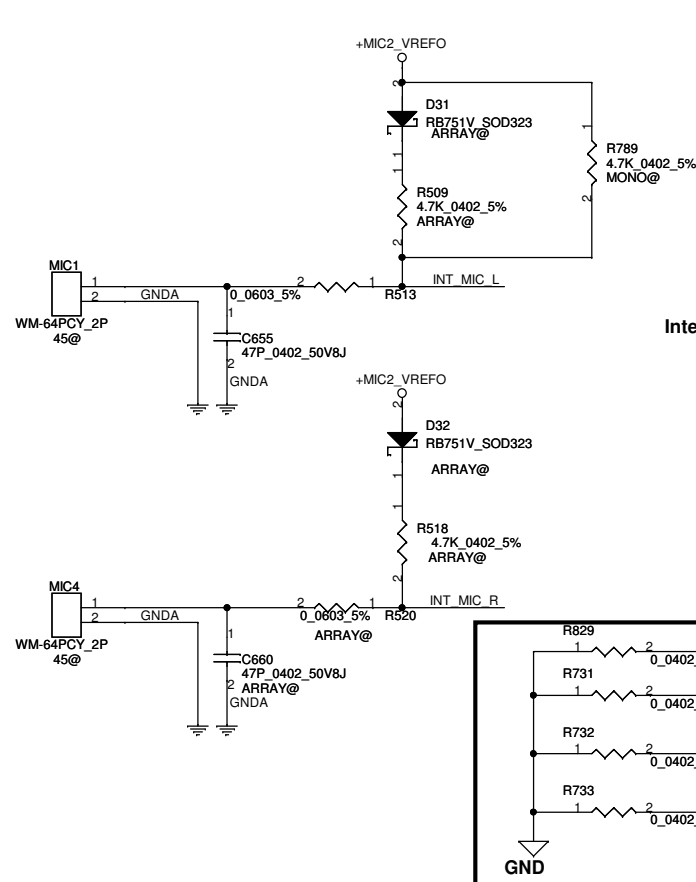
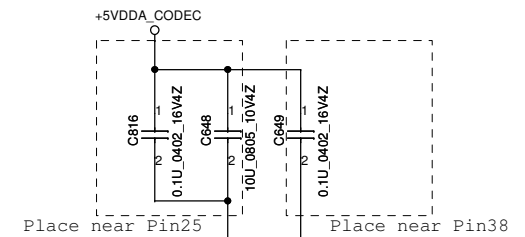
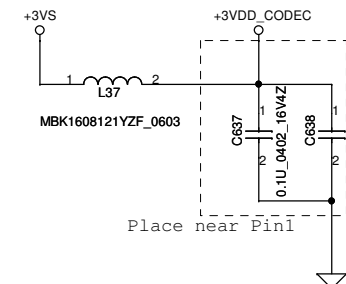
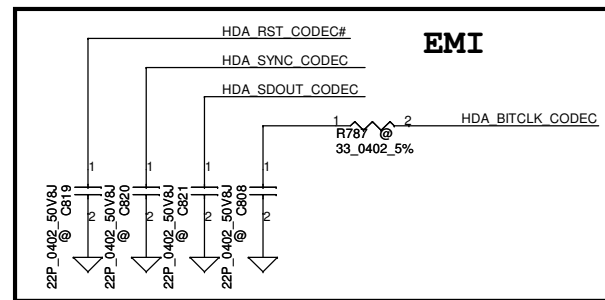
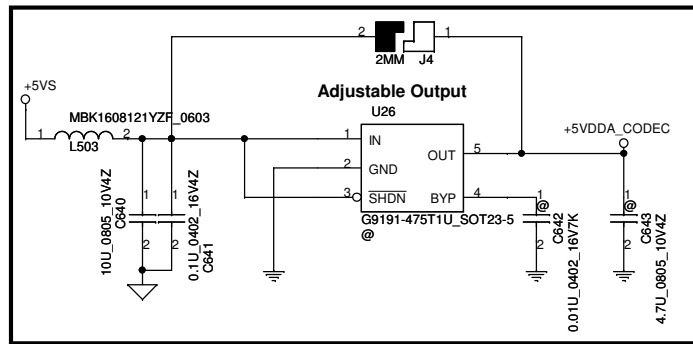
SATA ODD Conn.



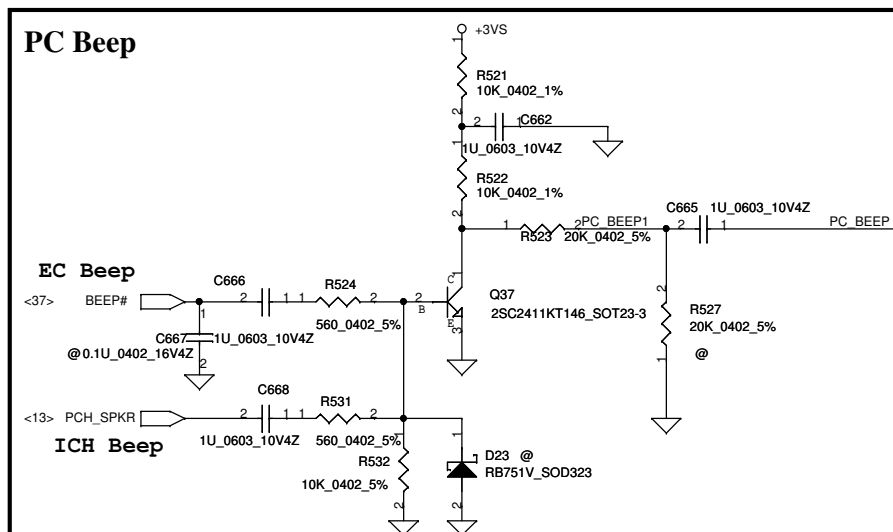
ESATA and USB Conn.



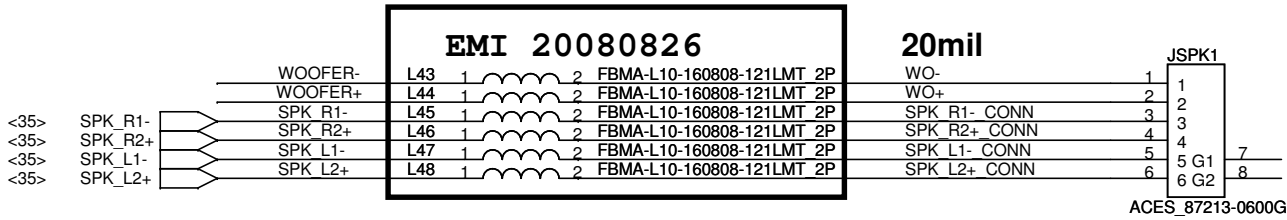
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc. HDD & ODD Connector	
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Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1 (Pin21/22)	External	Mic in
MONO-OUT (Pin37)	Internal	Internal Subwoofer
MIC2 (Pin16/17)	Internal	Internal Mic

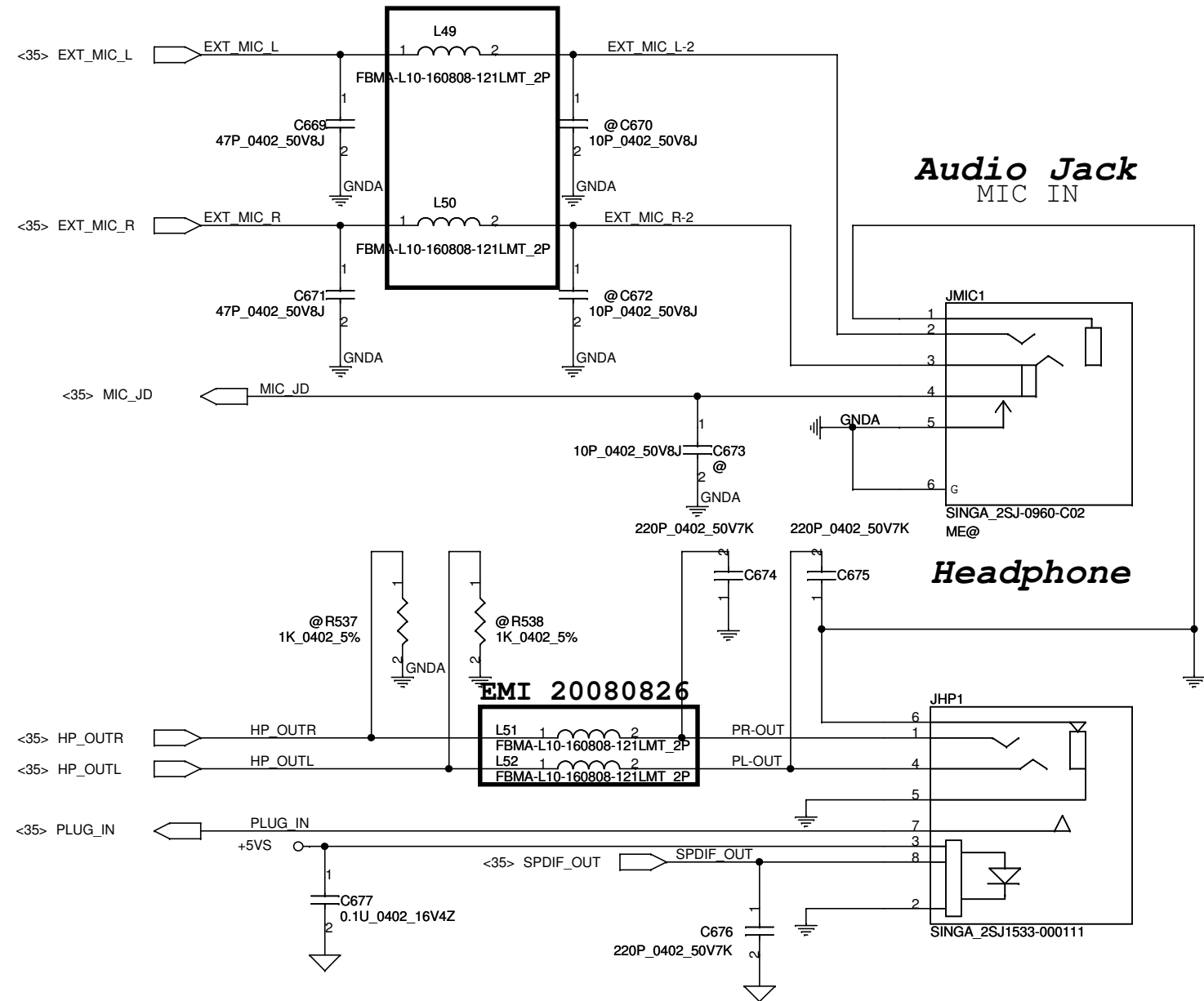


SubWoofer Conn. Speaker Connector



Audio Jack

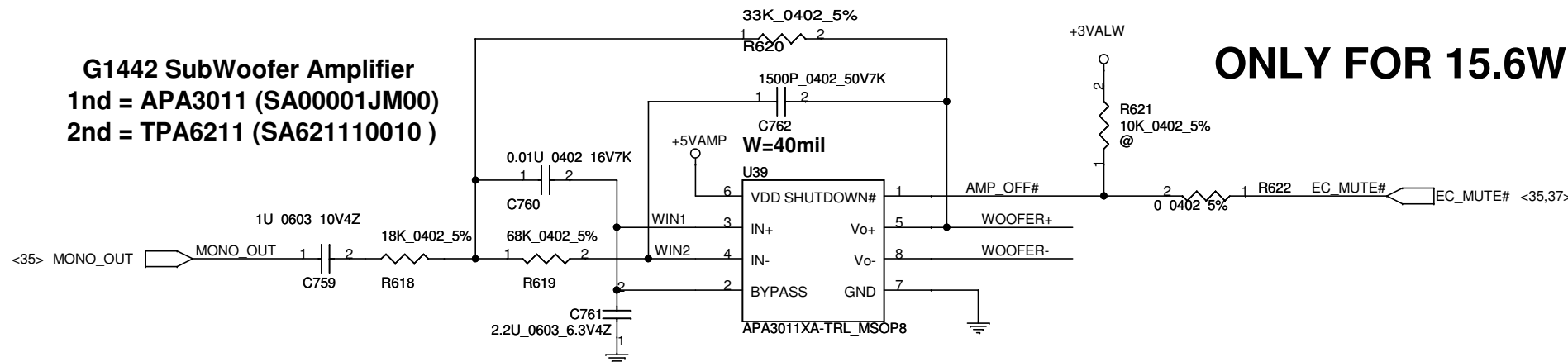
EMI 20080826



Audio Jack MIC IN

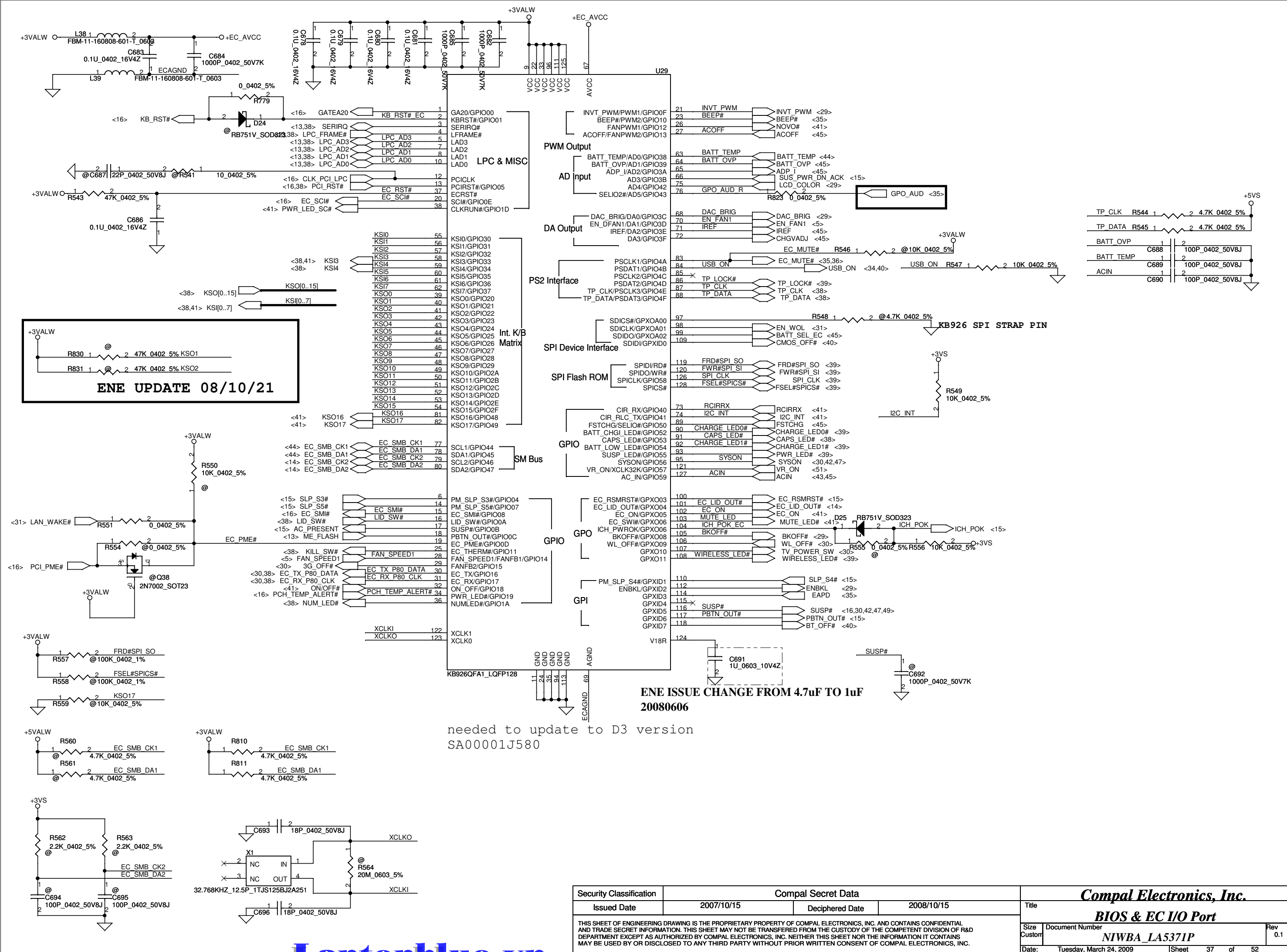
Headphone

G1442 SubWoofer Amplifier 1nd = APA3011 (SA00001JM00) 2nd = TPA6211 (SA621110010)

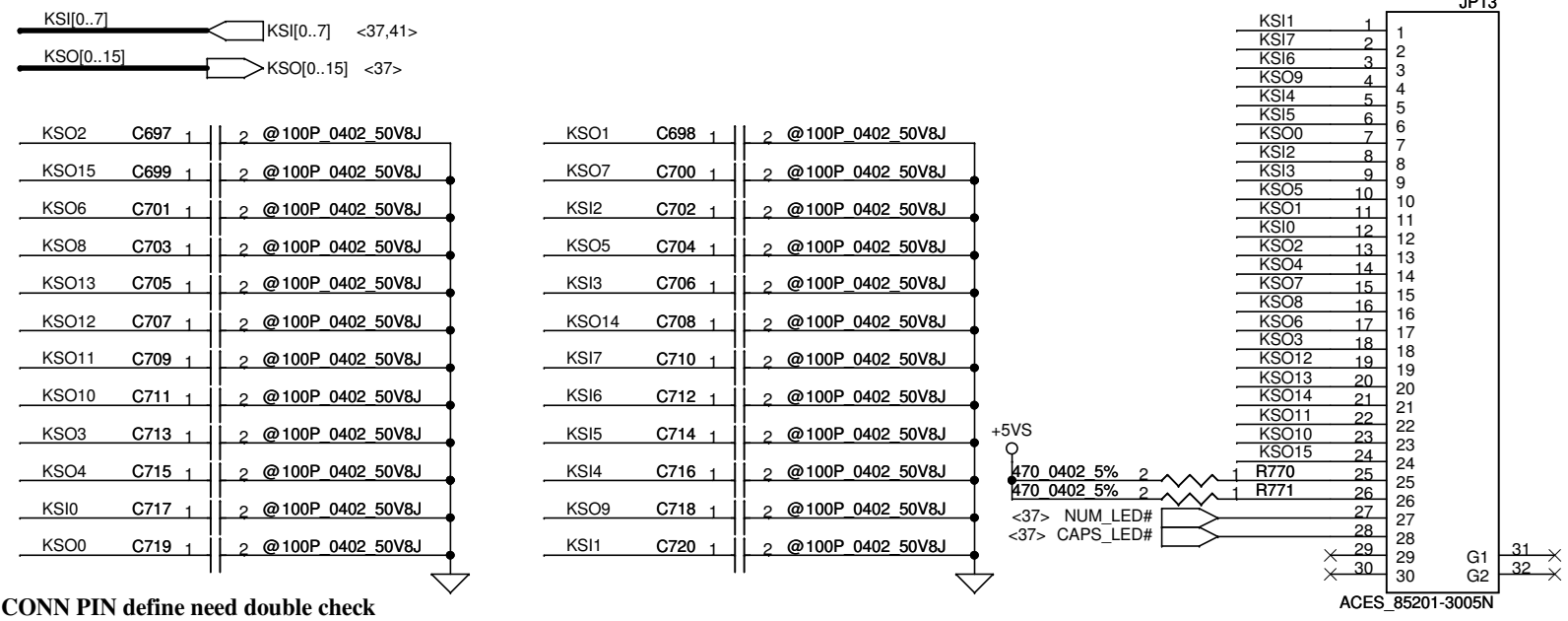


ONLY FOR 15.6W

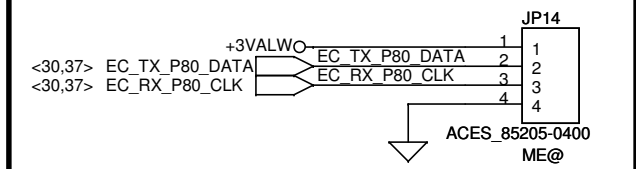
Security Classification	Compal Secret Data			Compal Electronics, Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title AMP, Audio speaker CONN	
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				Date: Tuesday, March 24, 2009	Sheet 36 of 52



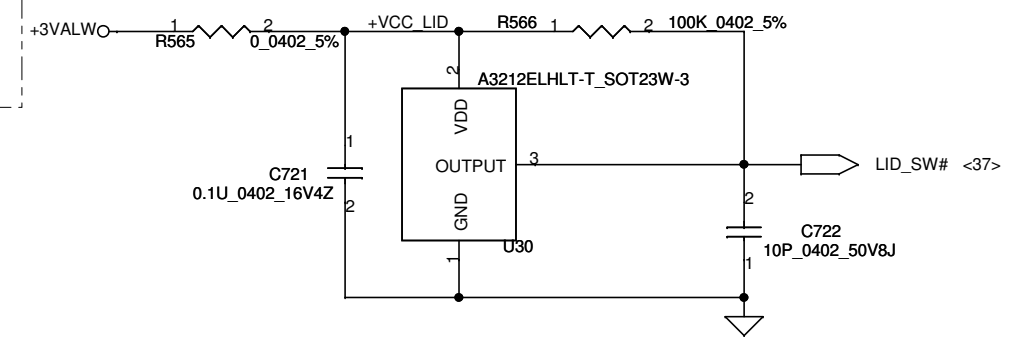
INT_KBD Conn.



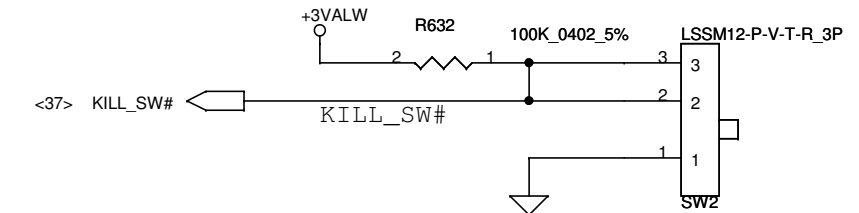
EC DEBUG PORT



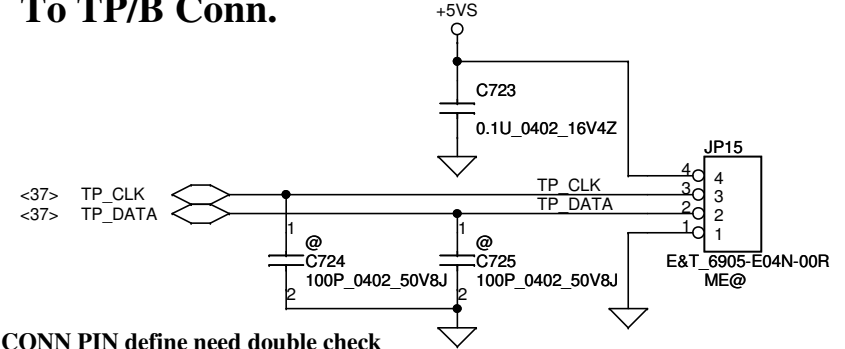
Lid Switch



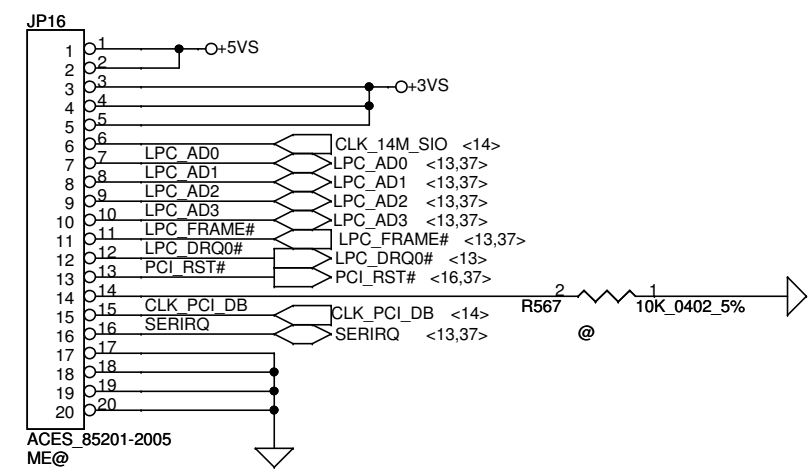
Kill Switch



To TP/B Conn.

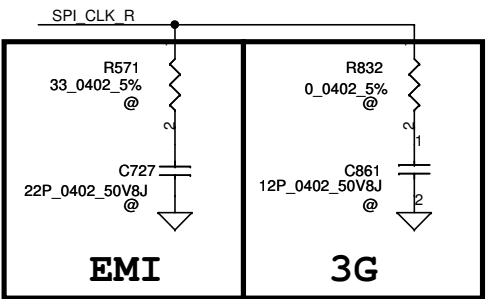
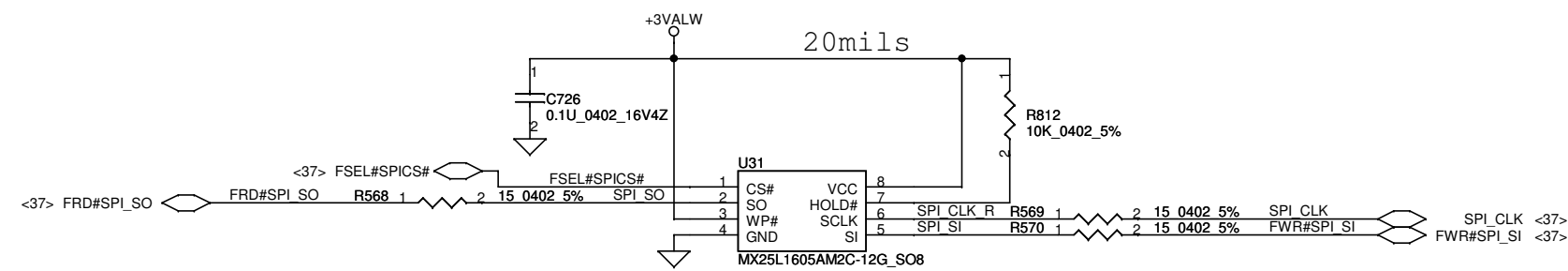


FOR LPC SIO DEBUG PORT



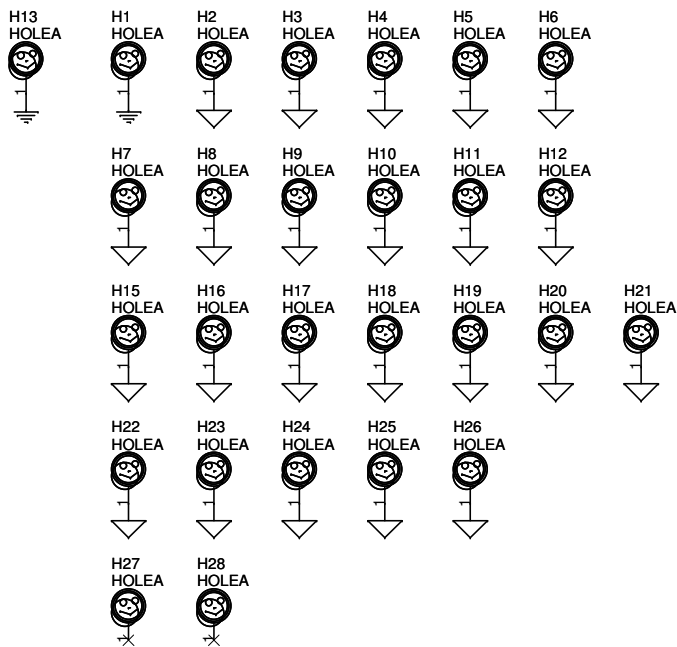
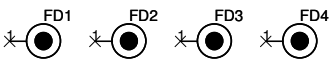
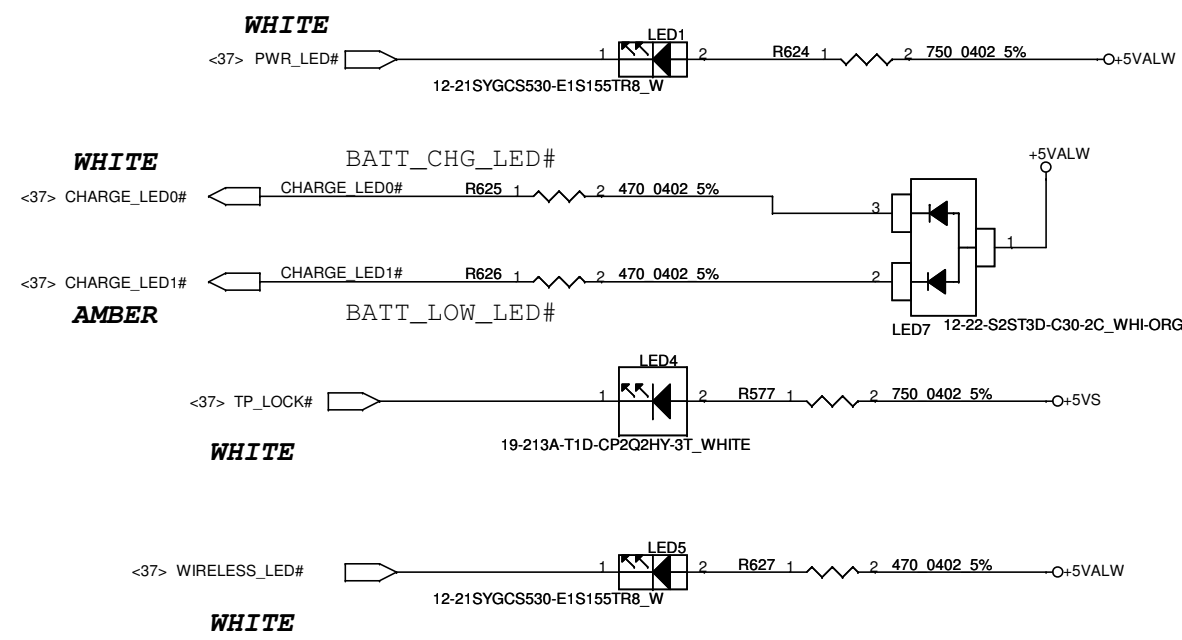
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Issued Date		Deciphered Date		KB /SW /LPC Debug Conn.	
2007/10/15		2008/10/15		KIWB1/B2_LA4601P	
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FOR EC 16M SPI ROM

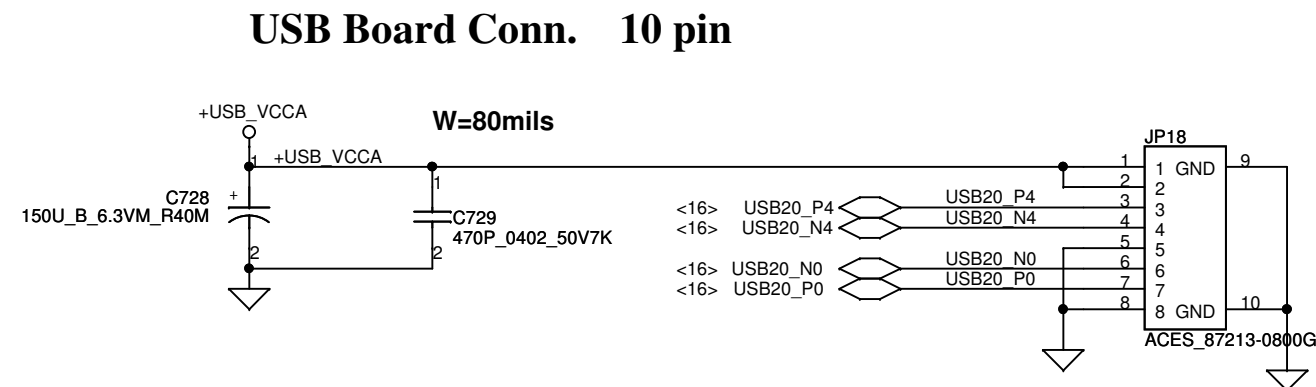
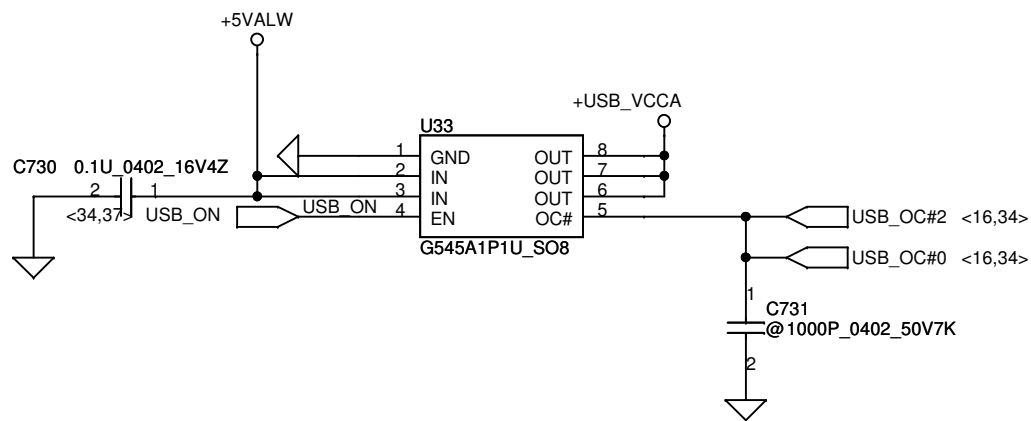


LED

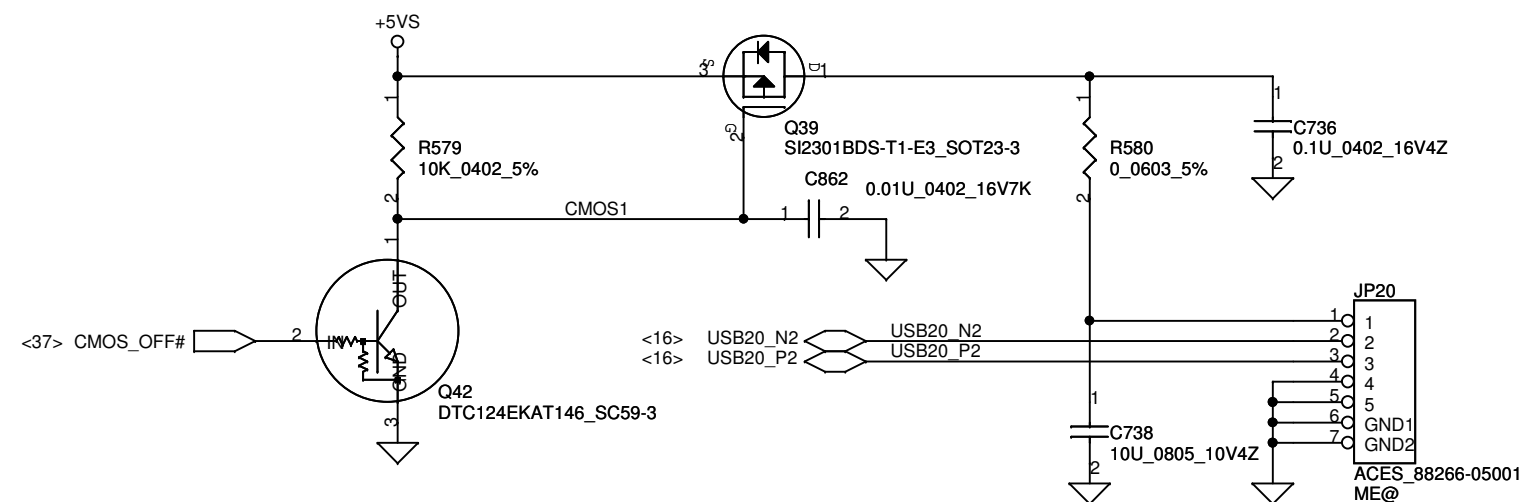
SC500005B00, If=5mA, Vf=2.7V~3.15V, R=460~390ohm



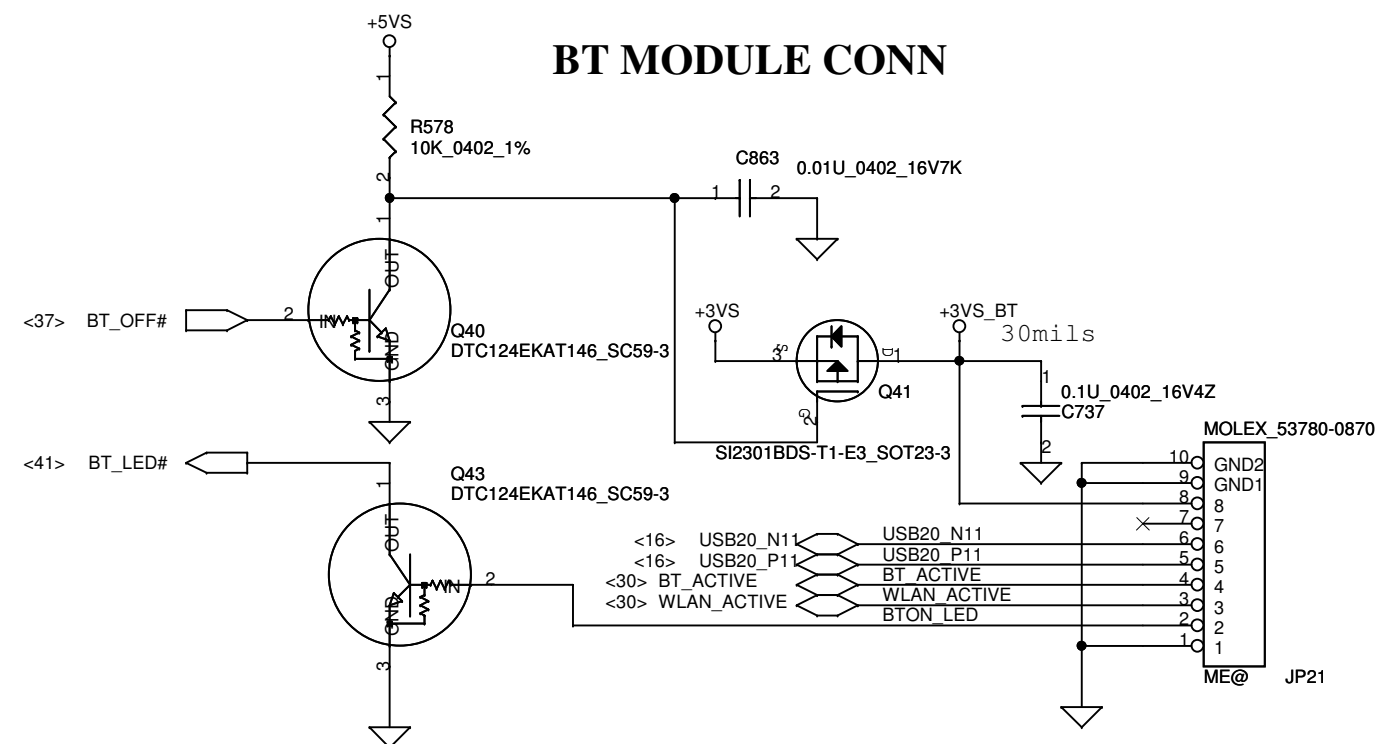
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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CMOS Camera Conn

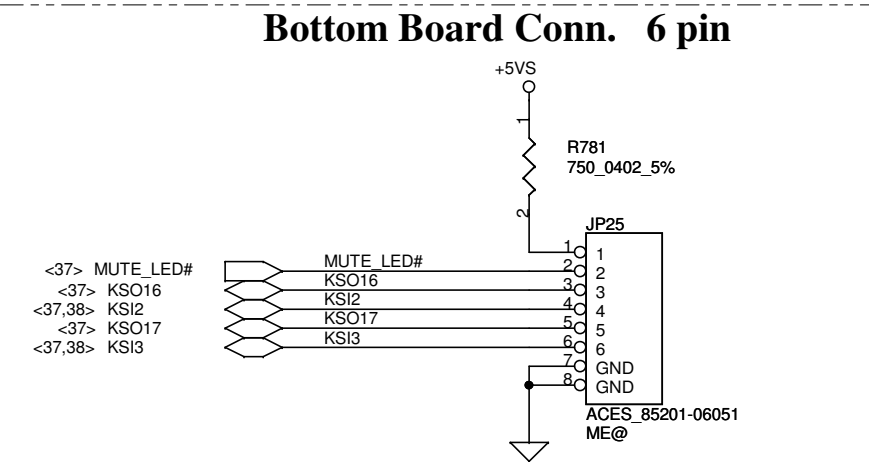
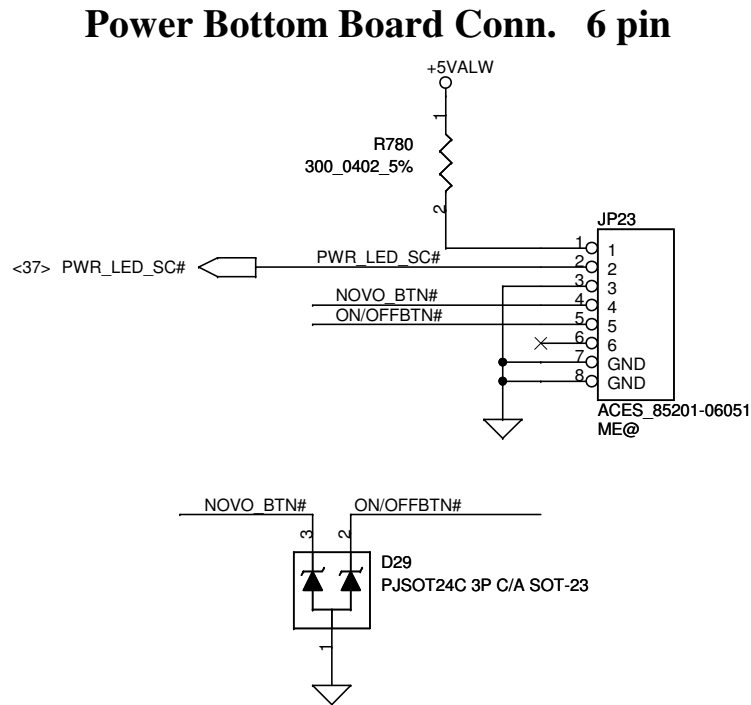
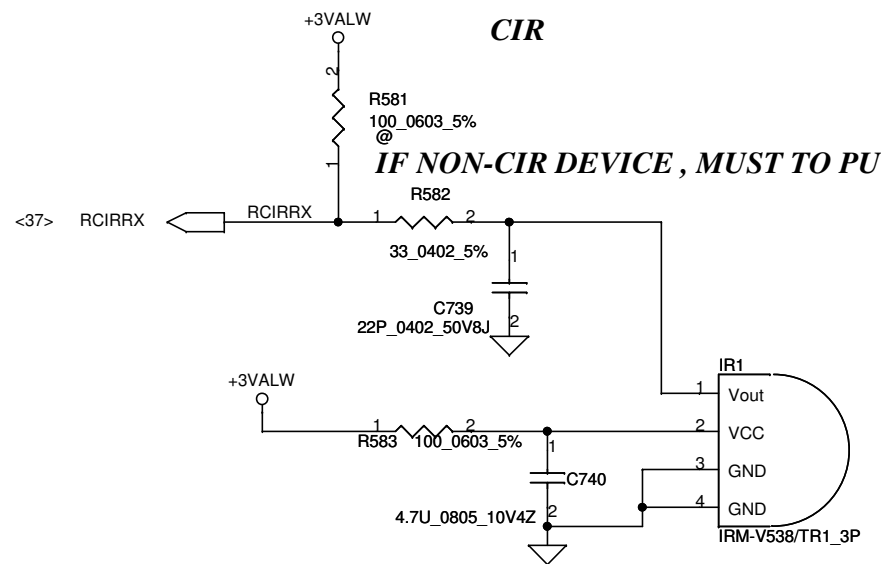


BT MODULE CONN

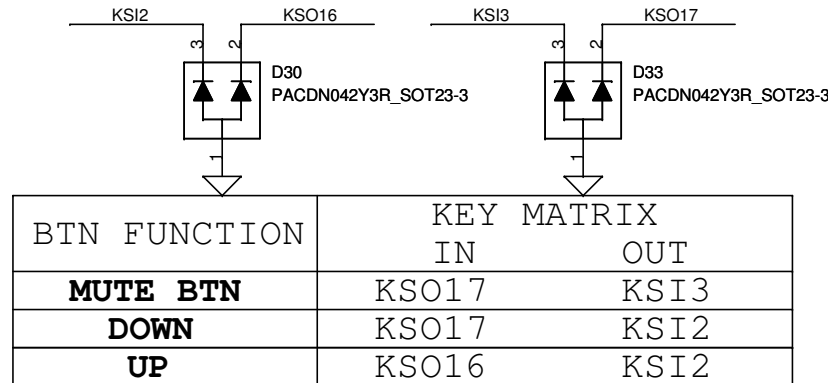


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Laptopblue.vn



EMI REQUEST 1ST = SCA00000G00
2ST = SCA00000T00

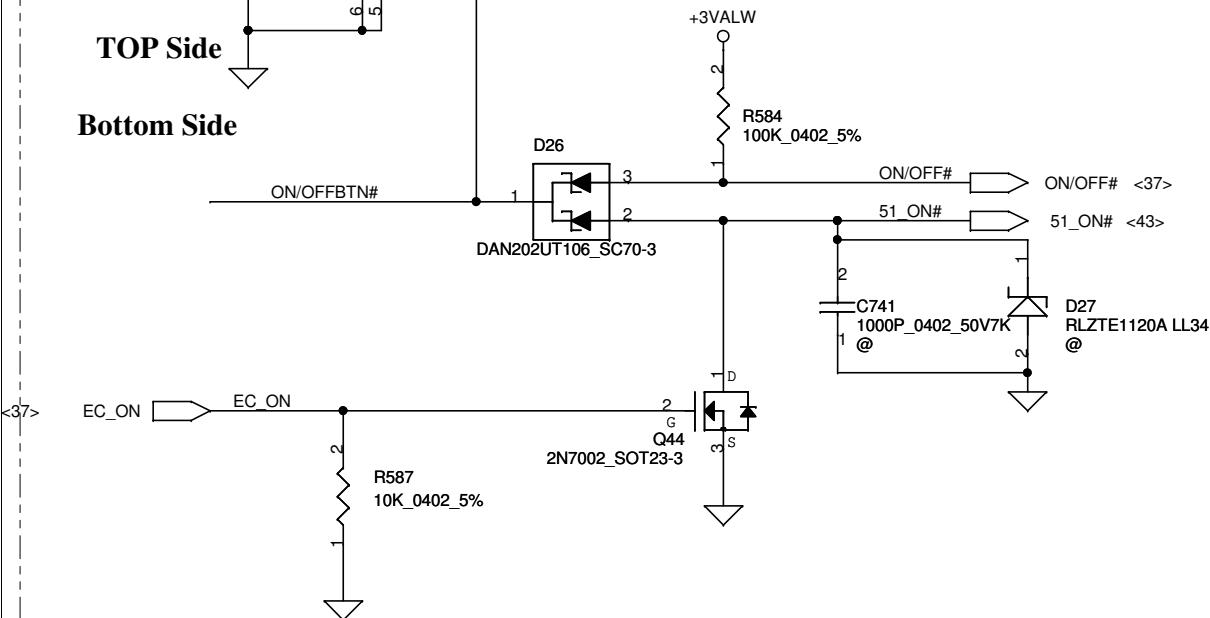


ON/OFF switch

Power Button

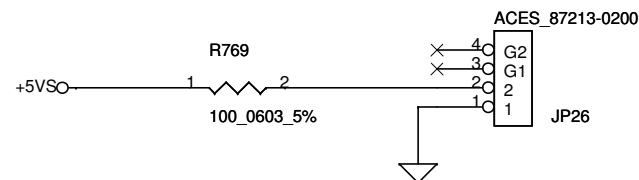
TOP Side

Bottom Side

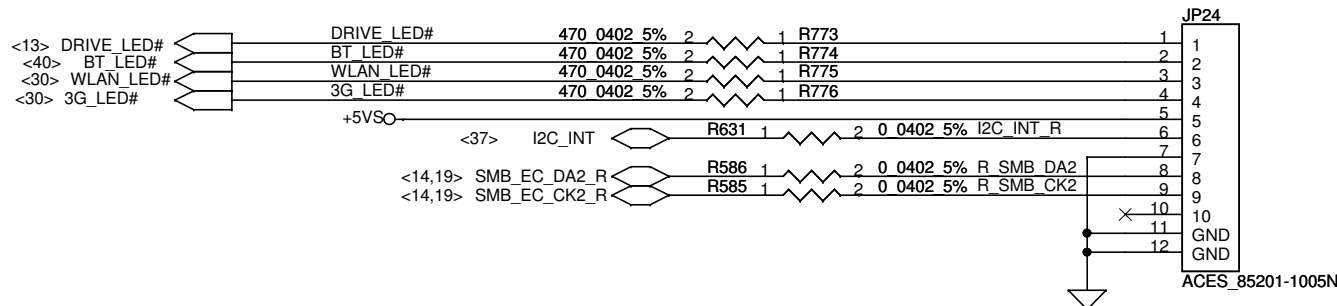
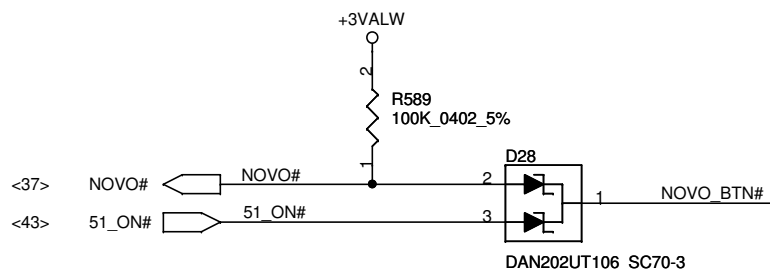


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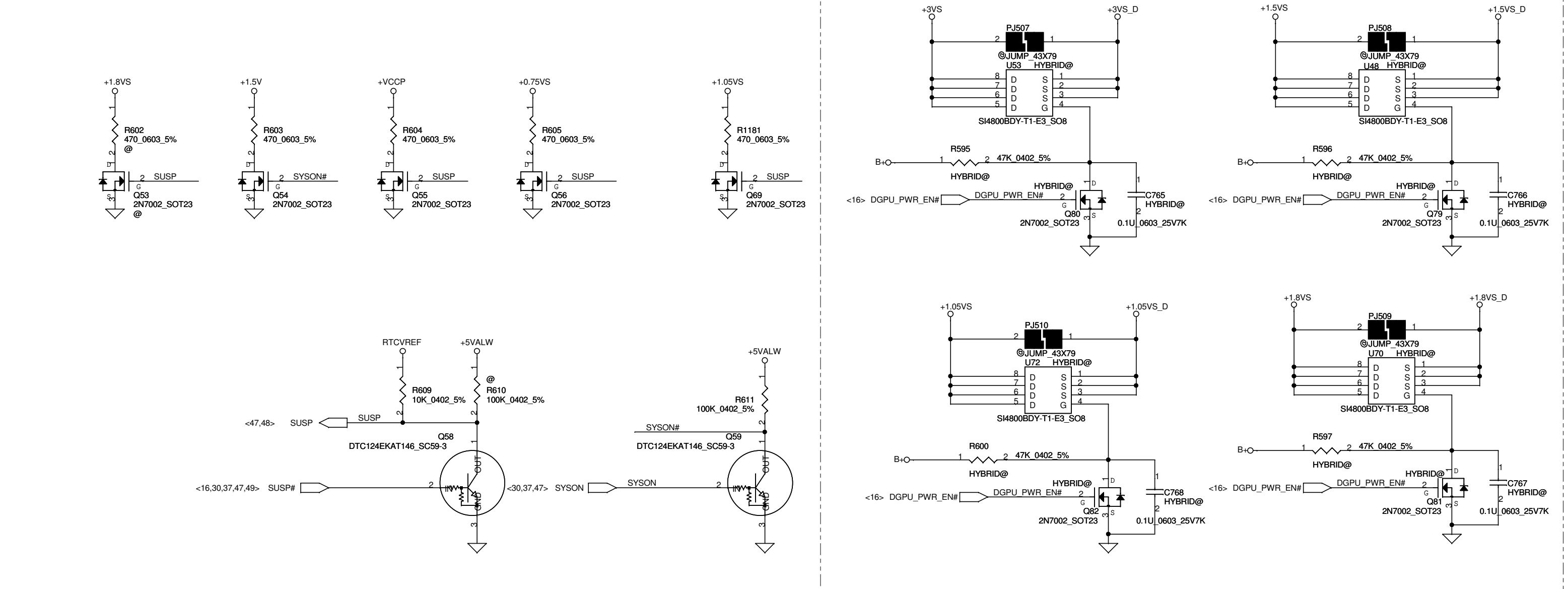
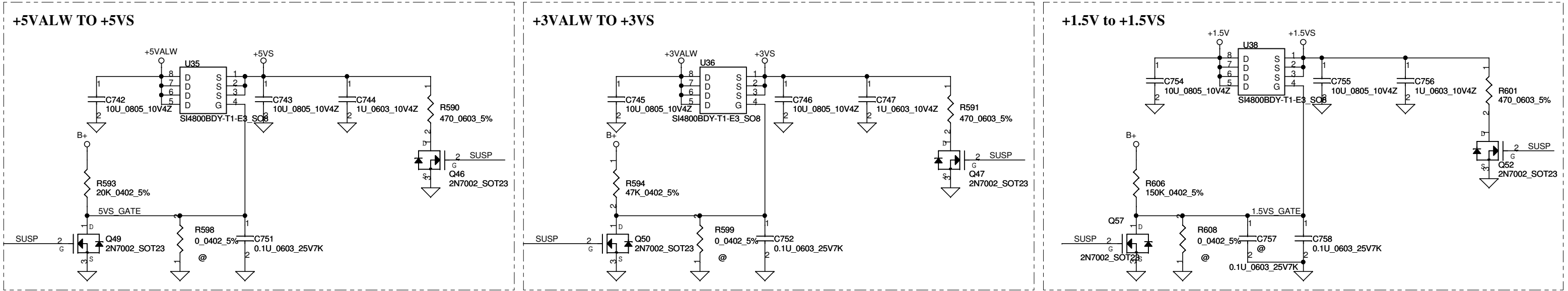
IDEAPAD BOARD 2PIN



Slide Board Conn. 10 pin

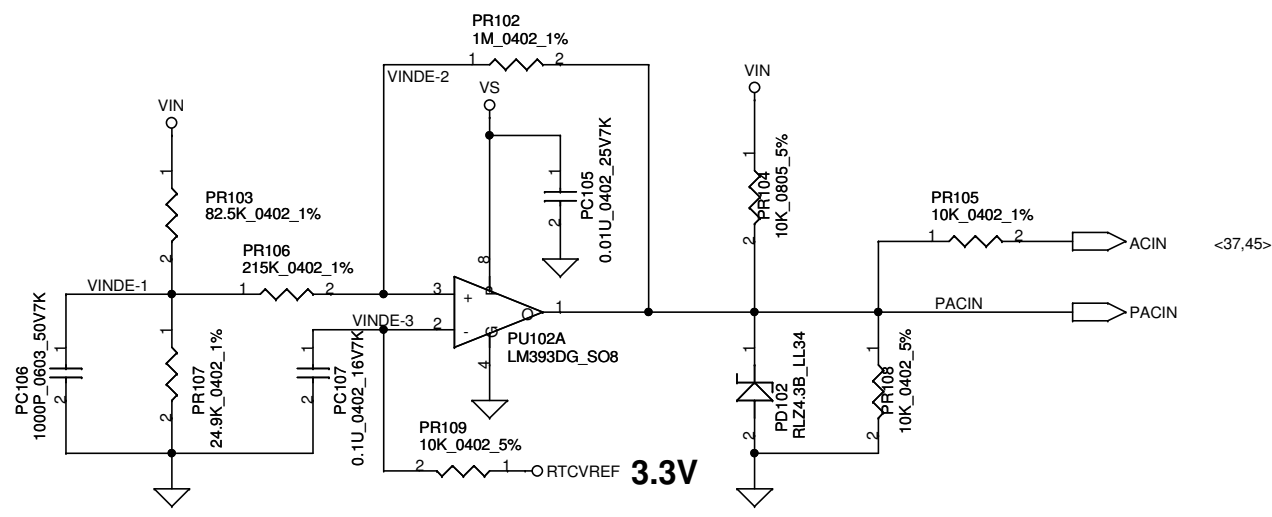
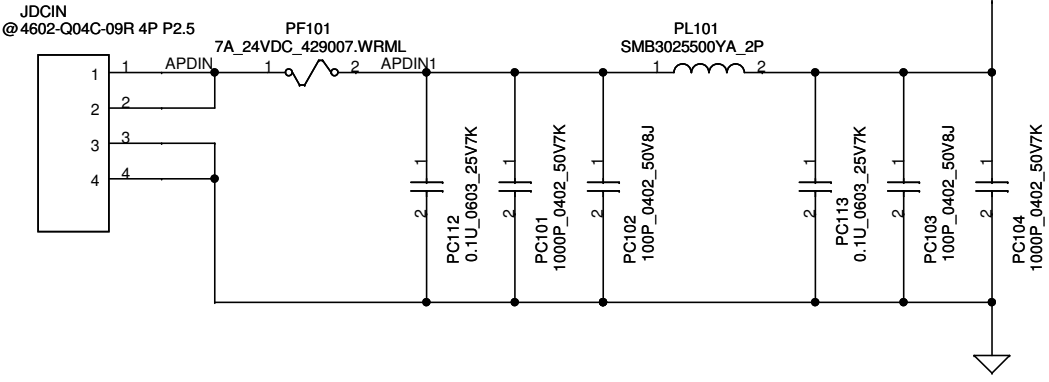


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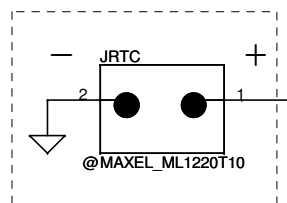
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DC030006J00

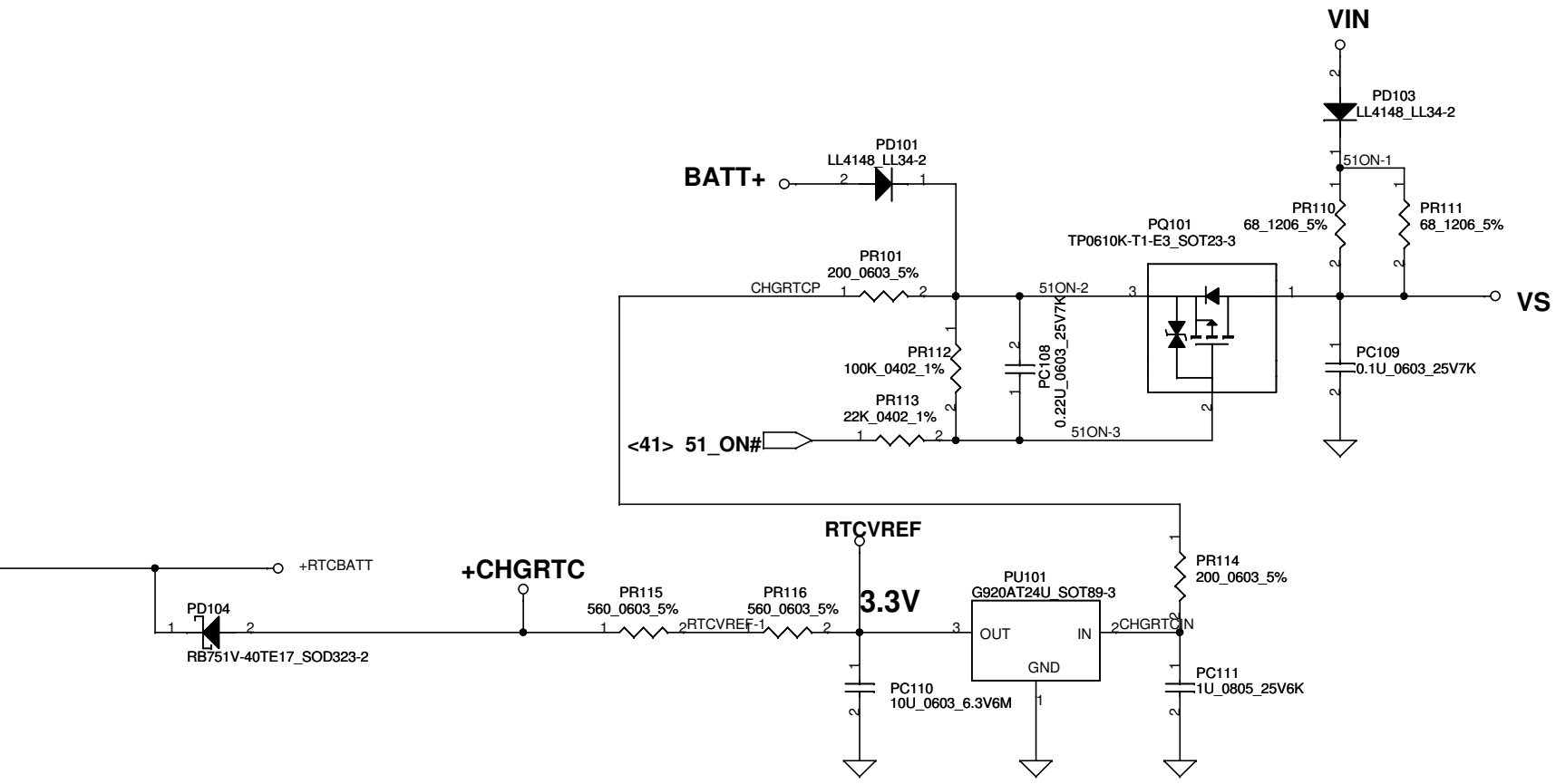


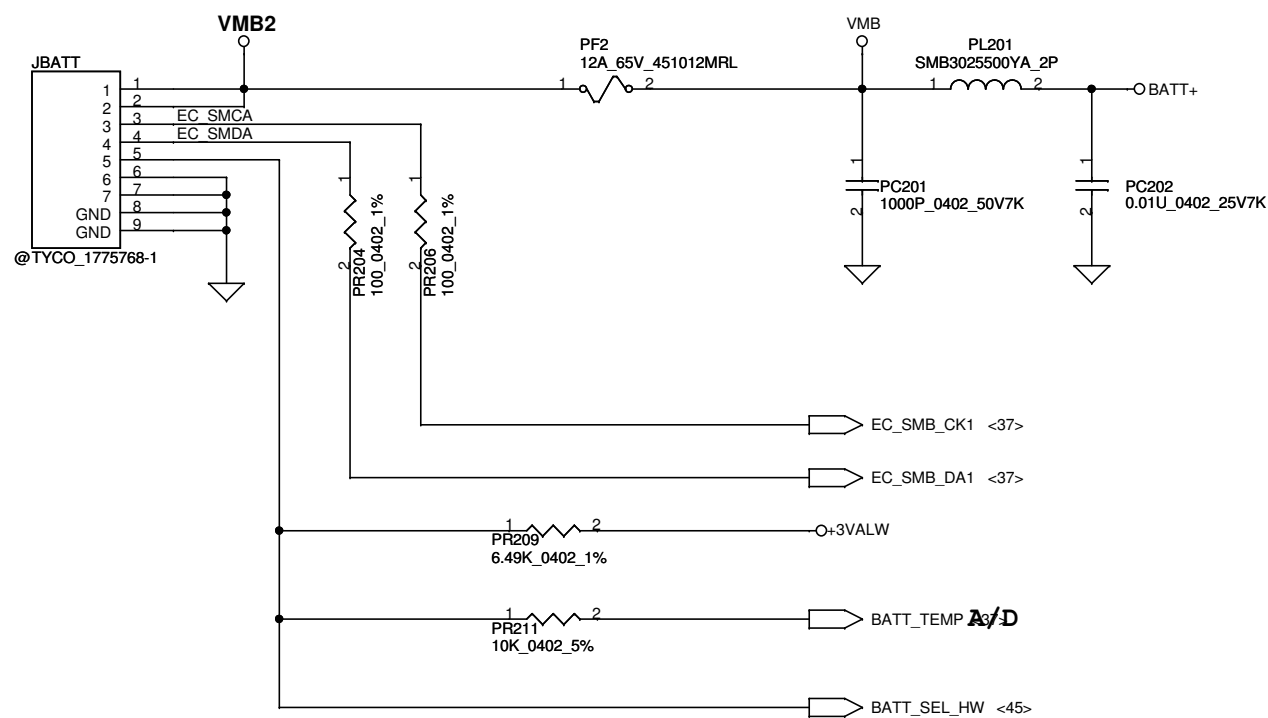
Vin Detector		
High	18.135	17.566
Low	14.866	14.355

RTC Battery



SP093MX0000

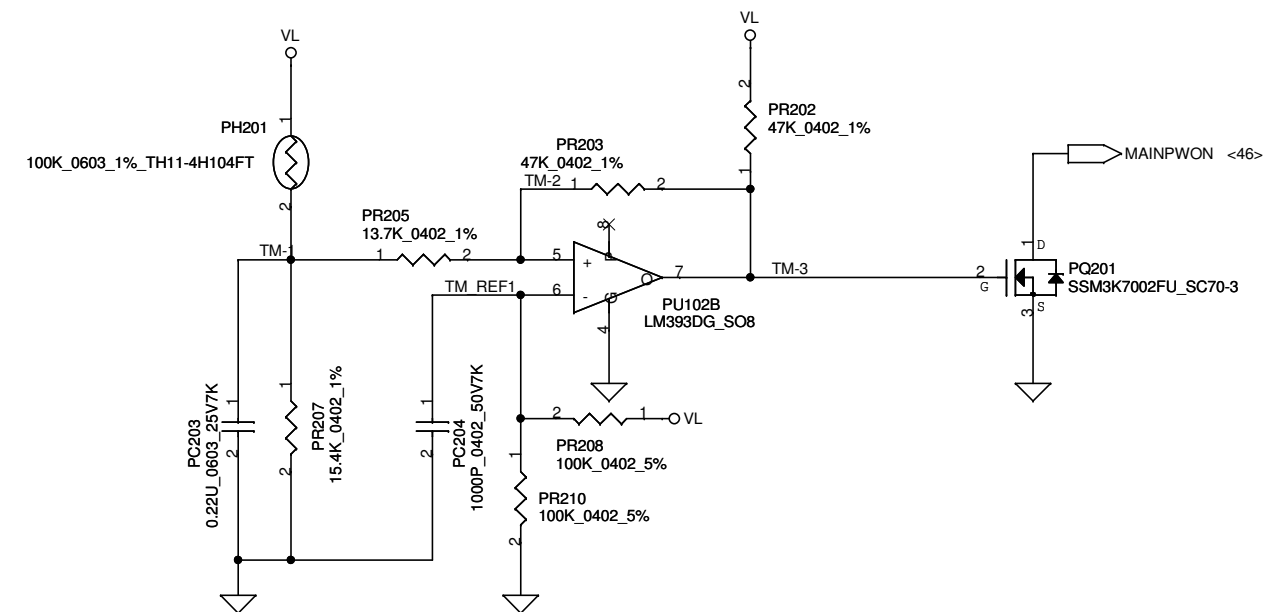




PH1 under CPU botten side :

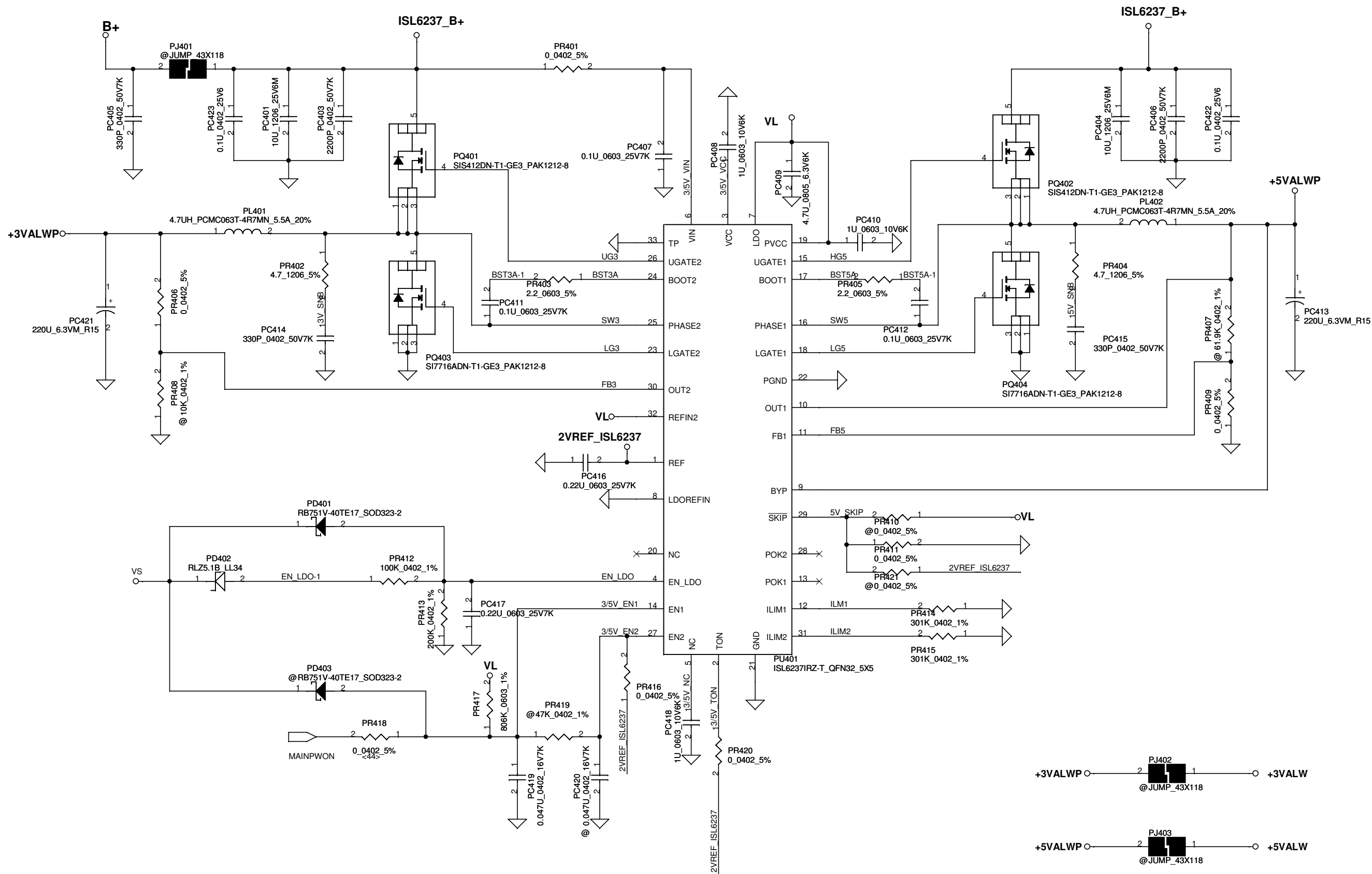
CPU thermal protection at 92 degree C

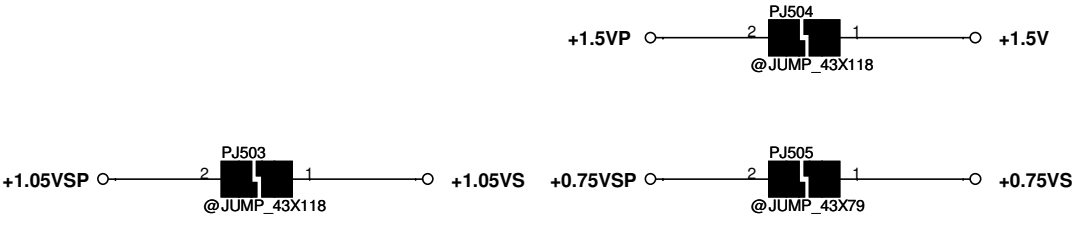
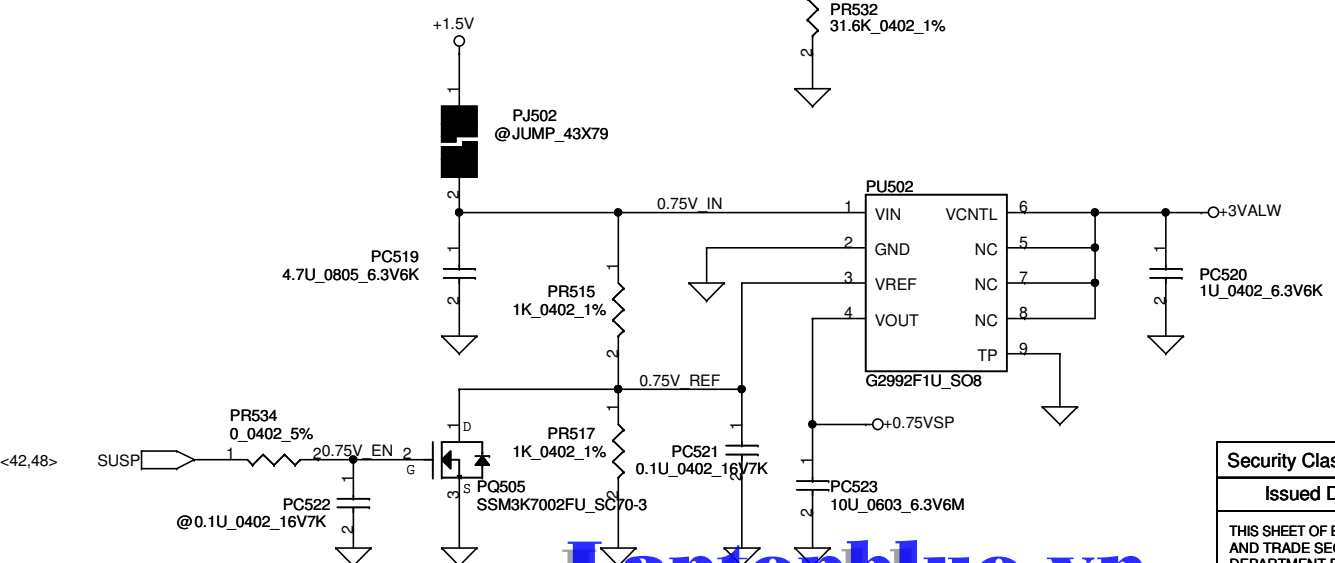
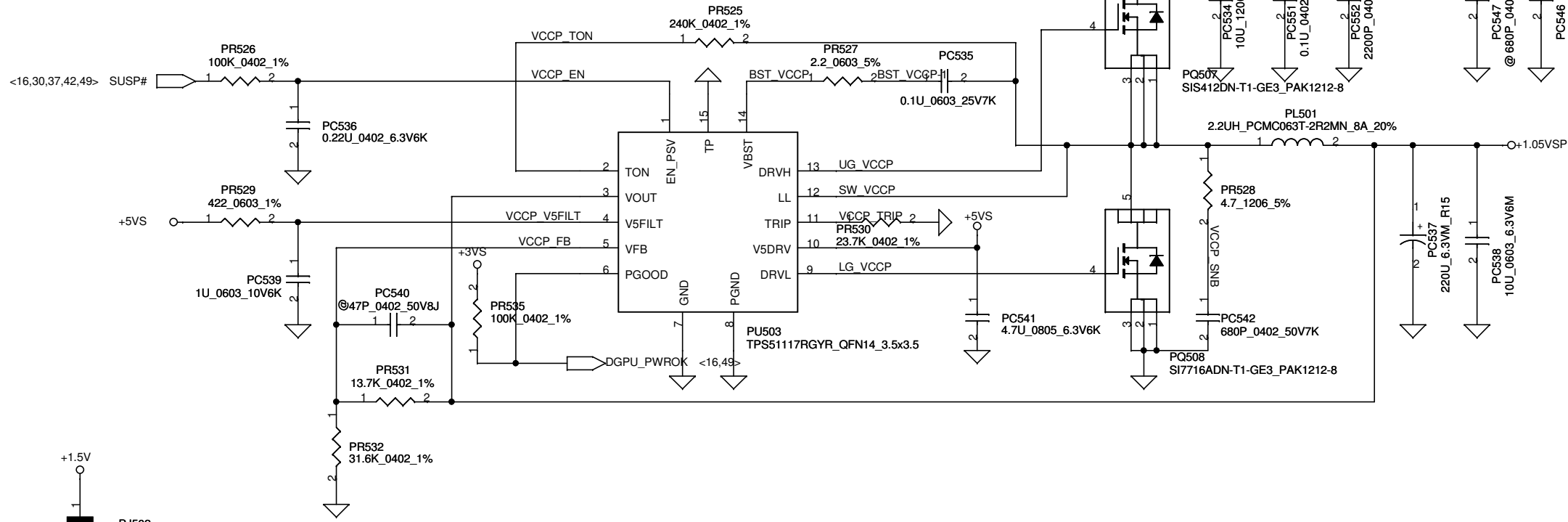
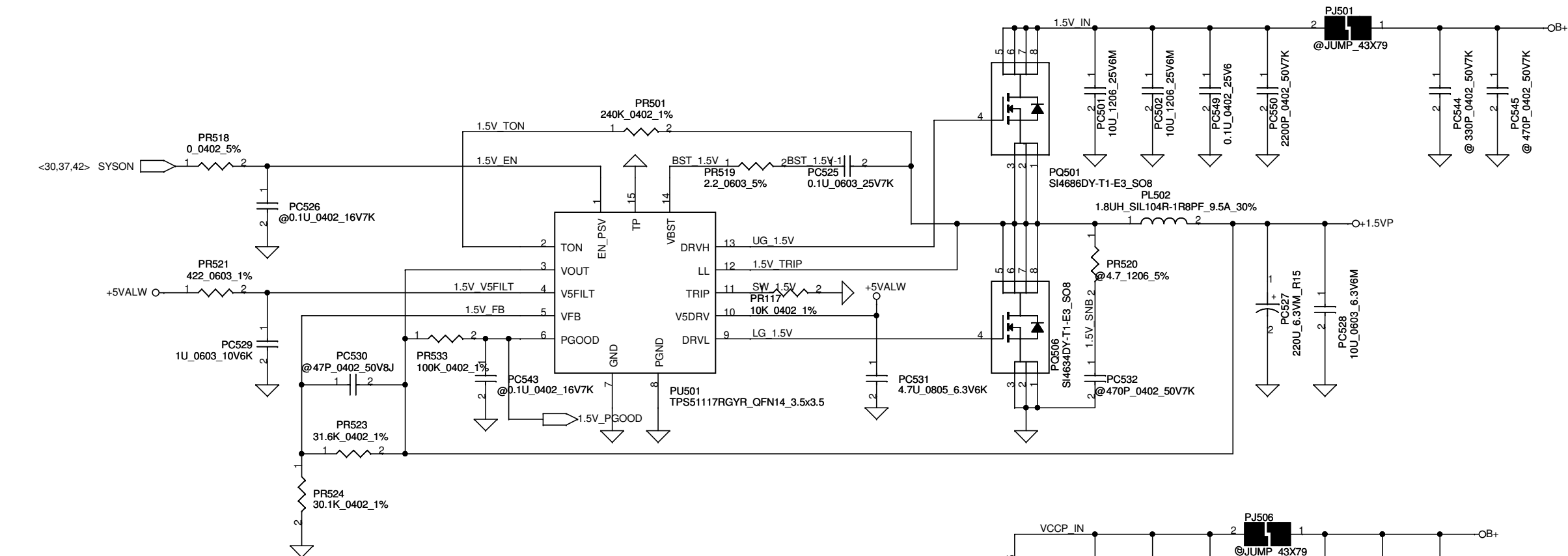
Recovery at 56 degree C





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Item	Reason for change	PG#	Modify List	Date	Phase
1					
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