Compal Confidential

ZIWB2/ZIWB3/ZIWE1
DIS M/B Schematics Document

Intel Boardwell U Processor with DDR3L
AMD Topaz XT / Jet LE

2014-02-10

LA-B091P

REV：1.0

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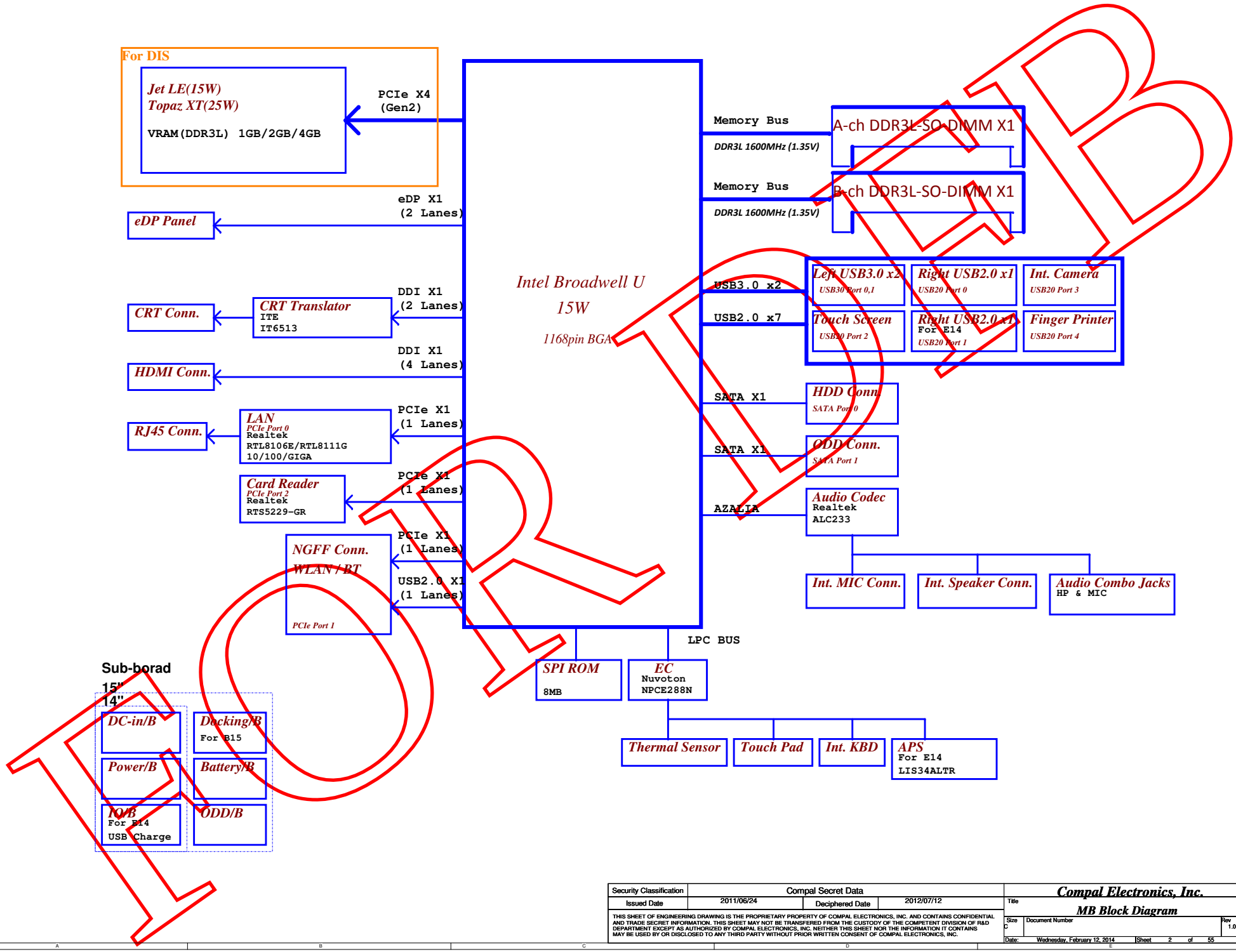
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	Cover Page		
Size: C	Document Number: LA-B091P		Rev: 1.0
Date: Wednesday, February 12, 2014	Sheet 1 of 55		



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Title: MB Block Diagram

Size	Document Number	Rev
C		1.0

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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Touch Screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB Port (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

Item	BOM Structure	
ZIWB2 (14")	B14@	
ZIWB3 (15")	B15@	
ZIWE1 (14")	E14@	
CPU_SA00006SM20	i3_4200U@	
CPU_SA00007AM00	QFSV@	
CPU_SA00006SU30	i3_4100U@	
CPU_SA00007QL10	i3_4005U@	
CPU_SA00006SX20	i3_4010U@	
LAN 10/100 Transformer	100@	
LAN GIGA Transformer	GIGA@	
LAN Switch mode	SWITCH@	
LAN RTL8106E-CG	8106ELDO@	
LAN RTL8111GS-CG	8111GLDO@	
LAN RTL8106EUS-CG	8106ESW@	
LAN RTL8111GUS-CG	8111GSW@	
Audio_233	233@	
Audio_233VB	233VB@	
For B15	Docking@	
For B14, E14	NoDocking@	
For Deep Sleep	DS3@	
For No Deep Sleep	NoDS3@	
WLAN Support ISCT	ISCT@	
WLAN No Support ISCT	NoISCT@	
For Intel ZERO ODD	ZODD@	
For No Intel ZERO ODD	NoZODD@	
For Green CLK	GCLK@	
For No Green CLK	NoGCLK@	
For No Green CLK	NoGCLKDIS@	Only in DIS Schematic
Green CLK IC For DIS	GCLKDIS@	
Green CLK IC For UMA	GCLKUMA@	
GPU support Dual Rank	DR@	Only in DIS Schematic
GPU Jet LE	JET@	
GPU Topaz XT	TOPAZ@	
For DIS	PX@	
For UMA	UMA@	
Camera	COMS@	
APS (G-sensor)	GS@	
Touch Screen	TS@	
HDMI	HDMI@	
USB 2.0	USB2@	
USB 3.0	USB3@	
Full HD Panel (2 Lane)	FHD@	
ENE EC 9012	9012@	
HDMI Royalty	45@	
Connector	ME@	
VRAM indentify	X76@	No USE
Un-pop component for EMI	@EMI@	
Un-pop component for ESD	@ESD@	
DA600140000	PCB_14_DIS@	
DA600141000	PCB_14_UMA@	
DA600140100	PCB_15_DIS@	
DA600141100	PCB_15_UMA@	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

EC SM Bus2 address

Device	Address
Thermal Sensor	0100 1100

PCH SM Bus address

Device	Address	
DDR_JDIMM1	1010 000x	A0h
DDR_JDIMM2	1010 010x	A4h

AMD-GPU SM Bus address

Device	Address	
Internal thermal sensor	0100 0001	41h

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	V +3VGS	X	X	X	X	V +3VS	V +3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
PCH_SML0CLK PCH_SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VGS	X	V +3VS	X	X	V +3VS	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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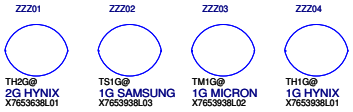
Topaz XT_VRAM_STRAP

		X76@ Vendor UV5, UV6, UV7, UV8	ID	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV21	X76@ R_pd RV24
2GBytes	ZZZ01 TH2G@	Hynix 4096Mbits SA00006E800 256Mx16 H5TC4G63AFR-11C	0	0	0	0	NC	4.75K
1GBytes	ZZZ02 TS1G@	Samsung 2048Mbits SA000068U40 128Mx16 K4W2G1646Q-BC1A	1	0	0	1	8.45K	2K
1GBytes	ZZZ03 TM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	2	0	1	0	4.53K	2K
1GBytes	ZZZ04 TH1G@	Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	3	0	1	1	6.98K	4.99K
2GBytes	ZZZ05 TM2G@	Micron 4096Mbits SA000077K00 256Mx16 MT41J256M16HA-093G:E	4	1	0	0	4.53K	4.99K
2GBytes	ZZZ06 TS2G@	Samsung 4096Mbits SA000076P00 256Mx16 K4W4G1646D-BC1A	5	1	0	1	3.24K	5.62K
1GBytes	ZZZ07 TM1G2@	Micron 2048Mbits SA00005XB00 128Mx16 MT41K128M16JT-107G:K	6	1	1	0	3.4K	10K
2GBytes	ZZZ08 TM2G2@	Micron 4096Mbits SA000065D00 256Mx16 MT41K256M16HA-107G:E	7	1	1	1	4.75K	NC



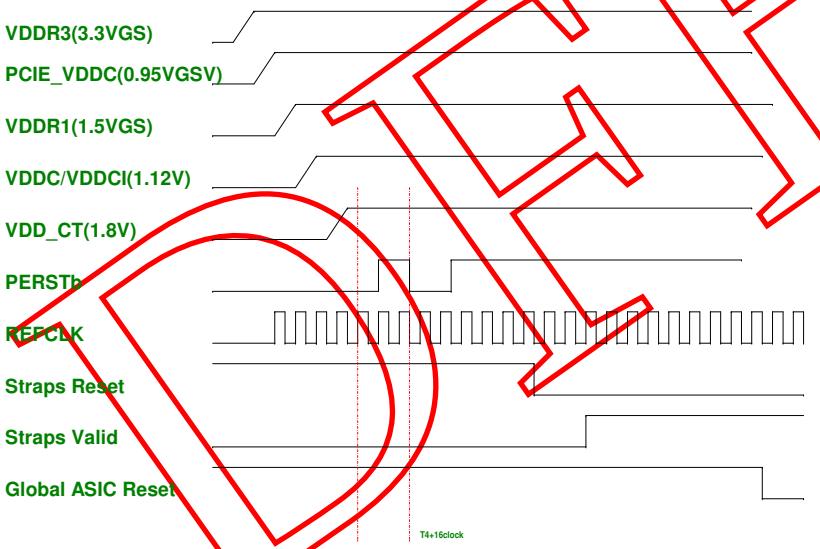
Jet LE_VRAM_STRAP

		X76@ Vendor UV5, UV6, UV7, UV8	ID	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV21	X76@ R_pd RV24
1GBytes	ZZZ09 JH1G@	Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	0	0	0	0	NC	4.75K
1GBytes	ZZZ10 JM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	0	0	1	8.45K	2K
1GBytes	ZZZ11 JS1G@	Samsung 2048Mbits SA000068U40 128Mx16 K4W2G1646Q-BC1A	2	0	1	0	4.53K	2K
2GBytes	ZZZ12 JH2G@	Hynix 4096Mbits SA00006E800 256Mx16 H5TC4G63AFR-11C	3	0	1	1	6.98K	4.99K
2GBytes	ZZZ13 JS2G@	Samsung 4096Mbits SA000076P00 256Mx16 K4W4G1646D-BC1A	4	1	0	0	4.53K	4.99K
2GBytes	ZZZ14 JM2G@	Micron 4096Mbits SA000077K00 256Mx16 MT41J256M16HA-093G:E	5	1	0	1	3.24K	5.62K
2GBytes	ZZZ08 JM2G2@	Micron 4096Mbits SA000065D00 256Mx16 MT41K256M16HA-107G:E	6	1	1	0	3.4K	10K
1GBytes	ZZZ16 JM1G2@	Micron 2048Mbits SA00005XB00 128Mx16 MT41K128M16JT-107G:K	7	1	1	1	4.75K	NC

Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

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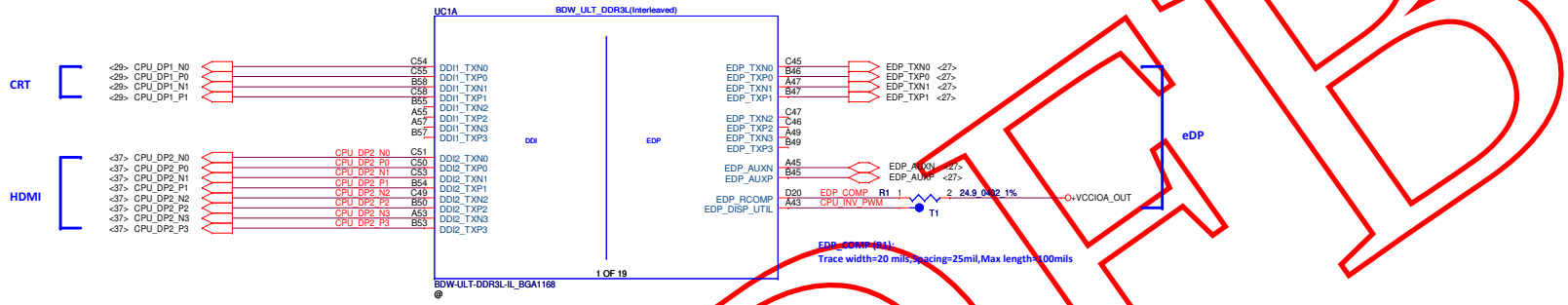
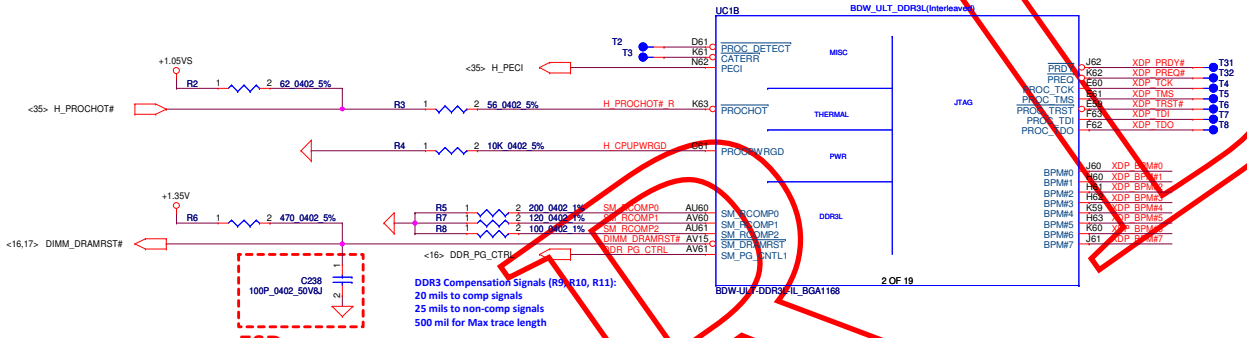
DAZ
DA600140000
PCB 14I LA-B091P REV0 M/B DIS 3
PCB_14_DIS@

DAZ
DA600140100
PCB 14K LA-B091P REV0 M/B DIS 6
PCB_15_DIS@

DAZ
DA600141000
PCB 14I LA-B092P REV0 M/B UMA 3
PCB_14_UMA@

DAZ
DA600141100
PCB 14K LA-B092P REV0 M/B UMA 6
PCB_15_UMA@





UC1
SA00007G020
Intel 2957U 1.4G 2M D0 2cBGA CPU
2957U@

UC1
SA00007G220
S IC CL8064701569500 QFAN D0 1.7G BGA
3558U@

UC1
SA00006SL70
S IC CL8064701477202 QEVD C0 1.8G BGA
i7_4500U@

UC1
SA00006SM80
S IC CL8064701477702 SR170 C0 1.6G C38!
i5_4200U@

UC1
SA00007AM00
S IC CL8064701614813 QFSY C0 1.6G BGA
QFSY@

UC1
SA00006SU50
S IC CL8064701476302 SR16P C0 1.8G C38!
i3_4100U@

UC1
SA00007Q70
S IC CL8064701478404 QEAR D0 1.7G C38
i3_4005U@

UC1
SA00006SX80
S IC CL8064701478202 SR16Q C0 1.7G C38!
i3_4010U@

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Compal Electronics, Inc.			
Title	HSW MCP(1/11) DDI,MSIC,XDP		
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Interleaved Memory

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Compal Electronics, Inc.			
Title	HSW MCP(2/11) DDRIII		
Size: C	Document Number: LA-B091P		Rev: 1.0
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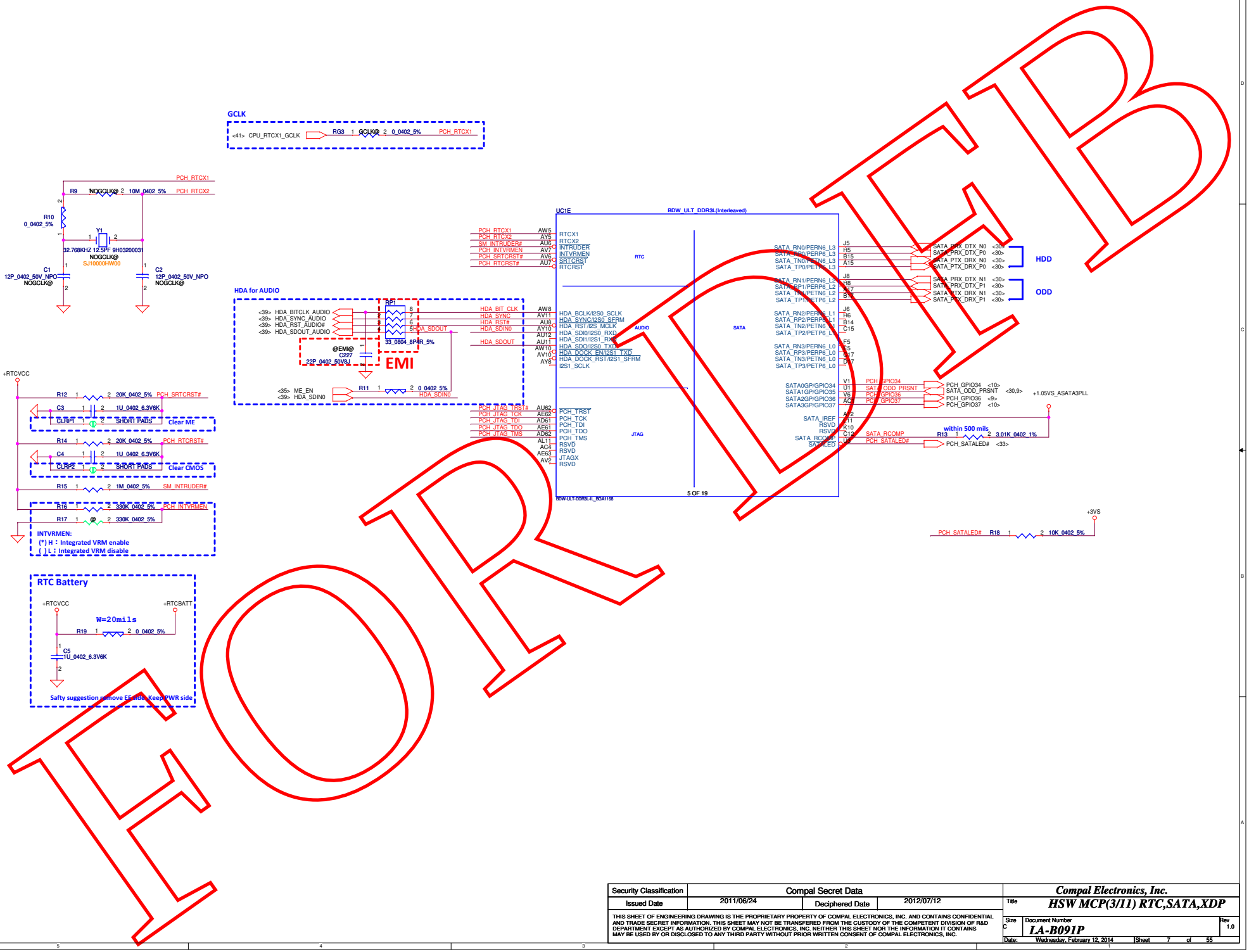

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Compal Electronics, Inc.			
Title	HSW MCP(3/11) RTC,SATA,XDP		
Size C	Document Number LA-B091P		Rev 1.0
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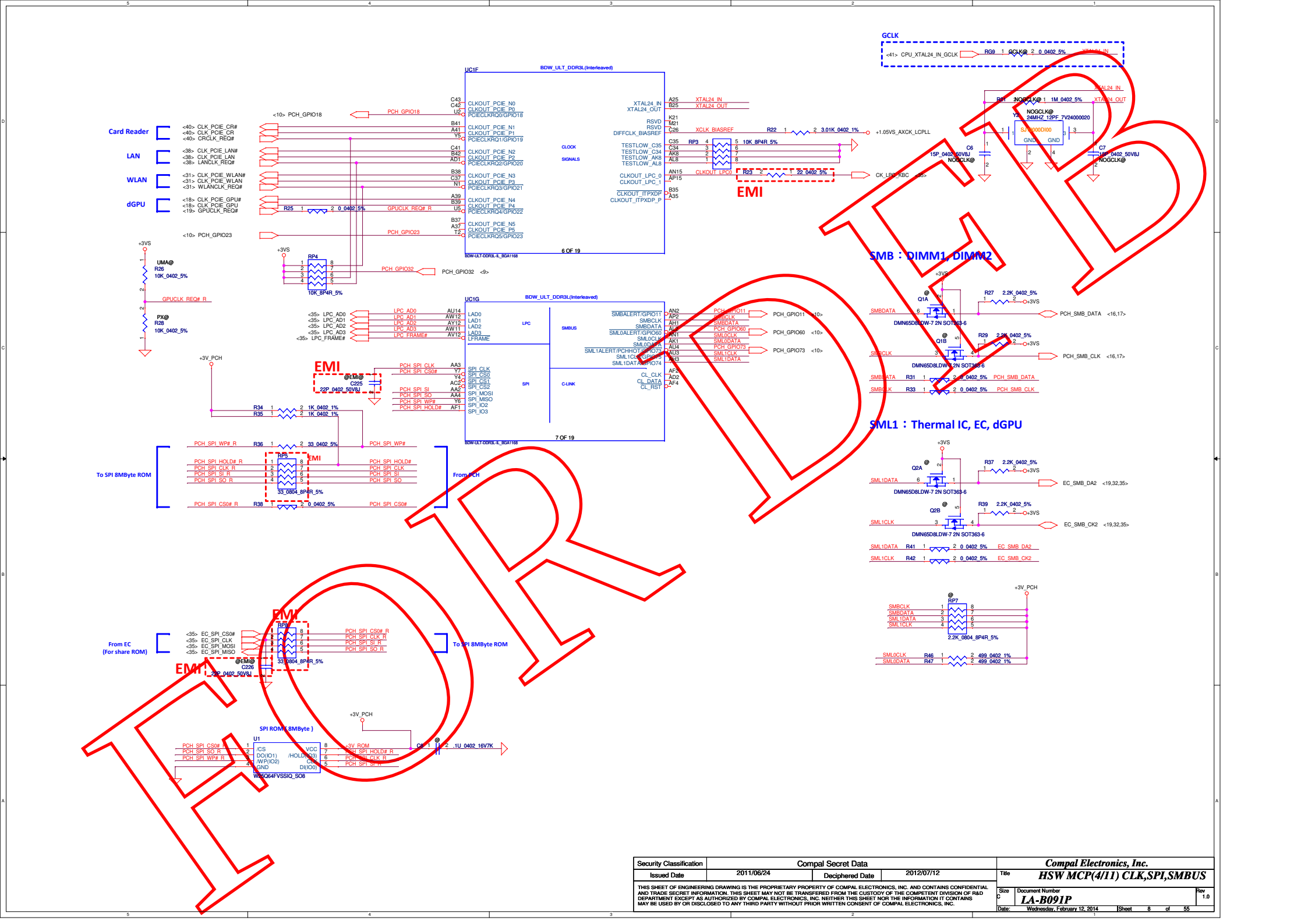
GCLK
<41> CPU_XTAL24_IN_GCLK
RG9 1 GCLK@ 2 0_0402_5%
XTAL24_IN
UC1F
BDW_ULT_DDR3L(Interleaved)
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
PCIECLKRQ0/GPIO18
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
PCIECLKRQ1/GPIO19
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
PCIECLKRQ2/GPIO20
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
PCIECLKRQ3/GPIO21
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
PCIECLKRQ4/GPIO22
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
PCIECLKRQ5/GPIO23
CLOCK SIGNALS
XTAL24_IN
XTAL24_OUT
RSVD
DIFFCLK_BIASREF
XCLK_BIASREF
R22 2 3.01K_0402_1%
+1.05VS_AXCK_LCPLL
TESTLOW_C35
TESTLOW_C34
TESTLOW_AK8
TESTLOW_AL8
RP3 10K_8P4R_5%
CLKOUT_LPC_0
CLKOUT_LPC_1
CLKOUT_LPC0
R23 22_0402_5%
CK_LPC_KBC <35>
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
6 OF 19
BDW-ULT-DDR3L-IL_BGA1168
EMI
Card Reader
LAN
WLAN
dGPU
<40> CLK_PCIE_CR#
<40> CLK_PCIE_CR
<40> CRCLK_REQ#
<38> CLK_PCIE_LAN#
<38> CLK_PCIE_LAN
<38> LANCLK_REQ#
<31> CLK_PCIE_WLAN#
<31> CLK_PCIE_WLAN
<31> WLANCLK_REQ#
<18> CLK_PCIE_GPU#
<18> CLK_PCIE_GPU
<19> GPUCLK_REQ#
<10> PCH_GPIO18
PCH_GPIO18
R25 1 2 0_0402_5%
GPUCLK_REQ# R
<10> PCH_GPIO23
PCH_GPIO23
+3VS
UMA@
R26
10K_0402_5%
GPUCLK_REQ# R
PX@
R28
10K_0402_5%
RP4
10K_8P4R_5%
PCH_GPIO32
PCH_GPIO32 <9>
XTAL24_IN
XTAL24_OUT
R81 2 NOGCLK@ 1 1M_0402_5%
NOGCLK@
Y2 24MHZ_12PF_7V24000020
SJ100000I00
GND GND
C6 15P_0402_50V8J NOGCLK@
C7 15P_0402_50V8J NOGCLK@
SMB：DIMM1, DIMM2
UC1G
BDW_ULT_DDR3L(Interleaved)
LPC
SMBUS
SPI
C-LINK
LAD0
LAD1
LAD2
LAD3
LFRAME#
<35> LPC_AD0
<35> LPC_AD1
<35> LPC_AD2
<35> LPC_AD3
<35> LPC_FRAME#
SMBALERT/GPIO11
SMBCLK
SMBDATA
SML0ALERT/GPIO60
SML0CLK
SML0DATA
SML1ALERT/PCHHOT#/GPIO73
SML1CLK/GPIO58
SML1DAT A/GPIO74
PCH_GPIO11 <10>
PCH_GPIO60 <10>
PCH_GPIO73 <10>
SML0CLK
SML0DATA
SML1CLK
SML1DATA
CL_CLK
CL_DATA
CL_RST
7 OF 19
BDW-ULT-DDR3L-IL_BGA1168
+3V_PCH
@EMI@ C225 22P_0402_50V8J
PCH_SPI_CLK
PCH_SPI_CS0#
PCH_SPI_SI
PCH_SPI_SO
PCH_SPI_WP#
PCH_SPI_HOLD#
SPI_CLK
SPI_CS0
SPI_CS1
SPI_CS2
SPI_MOSI
SPI_MISO
SPI_IO2
SPI_IO3
R34 1 2 1K_0402_1%
R35 1 2 1K_0402_1%
To SPI 8MByte ROM
From PCH
PCH_SPI_WP#_R
PCH_SPI_HOLD#_R
PCH_SPI_CLK_R
PCH_SPI_SI_R
PCH_SPI_SO_R
PCH_SPI_CS0#_R
R36 1 2 33_0402_5%
RP5 33_0804_8P4R_5%
R38 1 2 0_0402_5%
SML1：Thermal IC, EC, dGPU
Q1A
Q1B
Q2A
Q2B
DMN65D8LDW-7 2N SOT363-6
SMBDATA
SMBCLK
SML1DATA
SML1CLK
R27 2.2K_0402_5%
R29 2.2K_0402_5%
R37 2.2K_0402_5%
R39 2.2K_0402_5%
+3VS
PCH_SMB_DATA <16,17>
PCH_SMB_CLK <16,17>
EC_SMB_DA2 <19,32,35>
EC_SMB_CK2 <19,32,35>
R31 1 2 0_0402_5% PCH_SMB_DATA
R33 1 2 0_0402_5% PCH_SMB_CLK
R41 1 2 0_0402_5% EC_SMB_DA2
R42 1 2 0_0402_5% EC_SMB_CK2
RP7 2.2K_0804_8P4R_5%
SML0CLK
SML0DATA
R46 1 2 499_0402_1%
R47 1 2 499_0402_1%
From EC
(For share ROM)
<35> EC_SPI_CS0#
<35> EC_SPI_CLK
<35> EC_SPI_MOSI
<35> EC_SPI_MISO
@EMI@ C226 22P_0402_50V8J
PCH_SPI_CS0#_R
PCH_SPI_CLK_R
PCH_SPI_SI_R
PCH_SPI_SO_R
To SPI 8MByte ROM
SPI ROM (8MByte)
U1
W25Q64FVSSIQ_SO8
CS
DO(IO1)
/WP(IO2)
GND
VCC
/HOLD(IO3)
CLK
DI(IO0)
+3V_ROM
C8 @ 1 2 .1U_0402_16V7K
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HSW MCP(4/11) CLK,SPI,SMBUS
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Document Number
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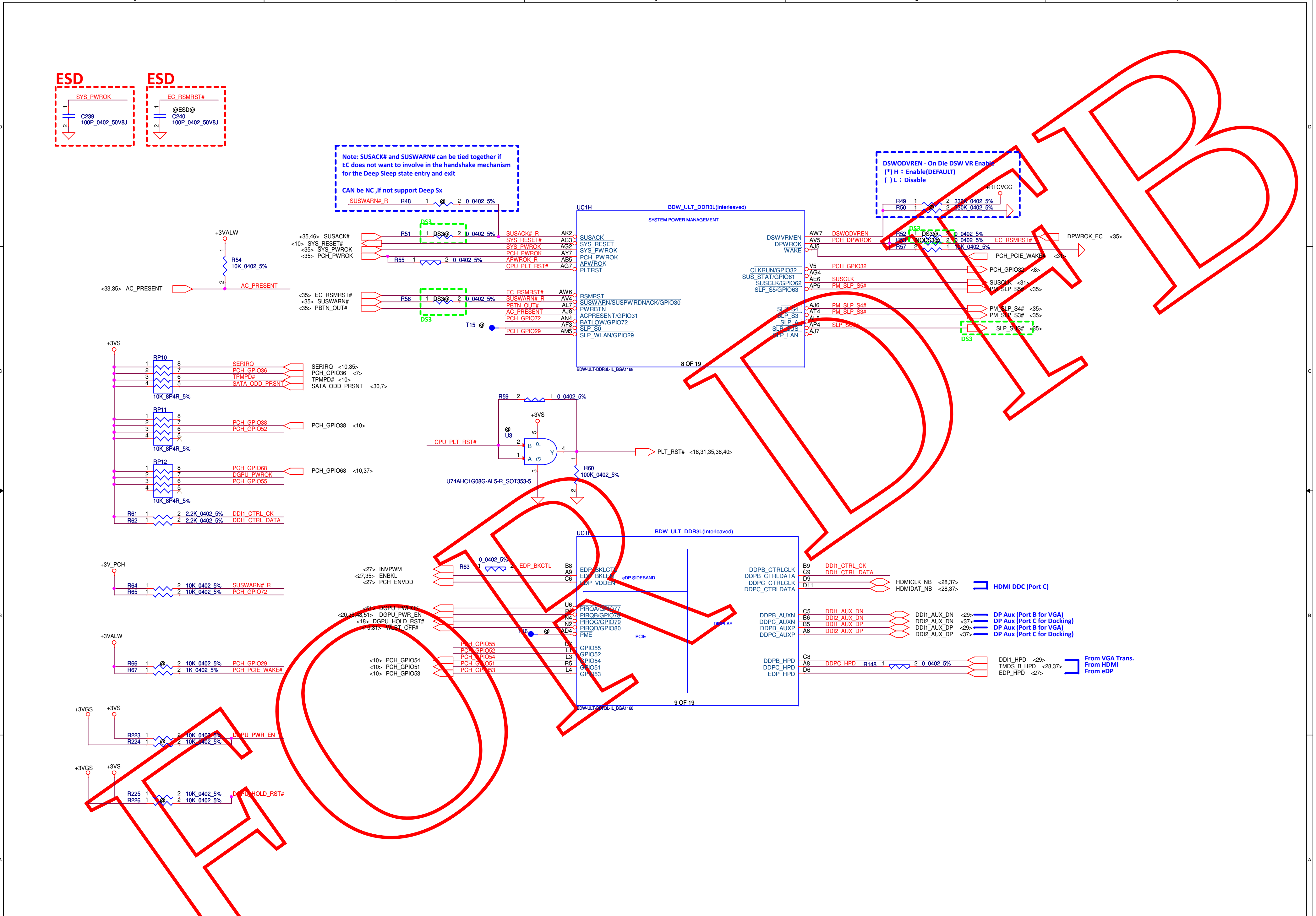


ESD
SYS_PWROK
C239
100P_0402_50V8J
ESD
EC_RSMRST#
@ESD@
C240
100P_0402_50V8J
Note: SUSACK# and SUSWARN# can be tied together if
EC does not want to involve in the handshake mechanism
for the Deep Sleep state entry and exit
CAN be NC ,if not support Deep Sx
DSWODVREN - On Die DSW VR Enable
(*) H : Enable(DEFAULT)
( ) L : Disable
+RTCVCC
UC1H
BDW_ULT_DDR3L(Interleaved)
SYSTEM POWER MANAGEMENT
SUSACK
SYS_RESET
SYS_PWROK
PCH_PWROK
APWROK
PLTRST
RSMRST
SUSWARN/SUSPWRDNACK/GPIO30
PWRBTN
ACPRESENT/GPIO31
BATLOW/GPIO72
SLP_S0
SLP_WLAN/GPIO29
DSWVRMEN
DPWROK
WAKE
CLKRUN/GPIO32
SUS_STAT/GPIO61
SUSCLK/GPIO62
SLP_S5/GPIO63
SLP_S4
SLP_S3
SLP_A
SLP_SUS
SLP_LAN
8 OF 19
BDW-ULT-DDR3L-IL_BGA1168
DPWROK_EC <35>
PCH_PCIE_WAKE# <34>
PCH_GPIO32 <8>
SUSCLK <31>
PM_SLP_S5# <35>
PM_SLP_S4# <35>
PM_SLP_S3# <35>
SLP_SUS# <35>
+3VALW
R54
10K_0402_5%
<33,35> AC_PRESENT
+3VS
RP10
10K_8P4R_5%
SERIRQ <10,35>
PCH_GPIO36 <7>
TPMPD# <10>
SATA_ODD_PRSNT <30,7>
RP11
10K_8P4R_5%
PCH_GPIO38 <10>
RP12
10K_8P4R_5%
PCH_GPIO68 <10,37>
R61 2.2K_0402_5% DDI1_CTRL_CK
R62 2.2K_0402_5% DDI1_CTRL_DATA
U3
U74AHC1G08G-AL5-R_SOT353-5
PLT_RST# <18,31,35,38,40>
R60
100K_0402_5%
UC1I
BDW_ULT_DDR3L(Interleaved)
eDP SIDEBAND
EDP_BKLCTL
EDP_BKLEN
EDP_VDDEN
PIRQA/GPIO77
PIRQB/GPIO78
PIRQC/GPIO79
PIRQD/GPIO80
PME
GPIO55
GPIO52
GPIO54
GPIO51
GPIO53
DDPB_CTRLCLK
DDPB_CTRLDATA
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPB_AUXN
DDPC_AUXN
DDPB_AUXP
DDPC_AUXP
DDPB_HPD
DDPC_HPD
EDP_HPD
9 OF 19
BDW-ULT-DDR3L-IL_BGA1168
HDMICLK_NB <28,37>
HDMIDAT_NB <28,37>
HDMI DDC (Port C)
DDI1_AUX_DN <29>
DDI2_AUX_DN <37>
DDI1_AUX_DP <29>
DDI2_AUX_DP <37>
DP Aux (Port B for VGA)
DP Aux (Port C for Docking)
DP Aux (Port B for VGA)
DP Aux (Port C for Docking)
DDI1_HPD <29>
TMDS_B_HPD <28,37>
EDP_HPD <27>
From VGA Trans.
From HDMI
From eDP
<27> INVPWM
<27,35> ENBKL
<27> PCH_ENVDD
<51> DGPU_PWROK
<20,35,48,51> DGPU_PWR_EN
<18> DGPU_HOLD_RST#
<10,31> WLBT_OFF#
<10> PCH_GPIO54
<10> PCH_GPIO51
<10> PCH_GPIO53
+3V_PCH
R64 10K_0402_5% SUSWARN#_R
R65 10K_0402_5% PCH_GPIO72
+3VALW
R66 10K_0402_5% PCH_GPIO29
R67 1K_0402_5% PCH_PCIE_WAKE#
+3VGS
+3VS
R223 10K_0402_5% DGPU_PWR_EN
R224 10K_0402_5%
R225 10K_0402_5% DGPU_HOLD_RST#
R226 10K_0402_5%
FOR DFB

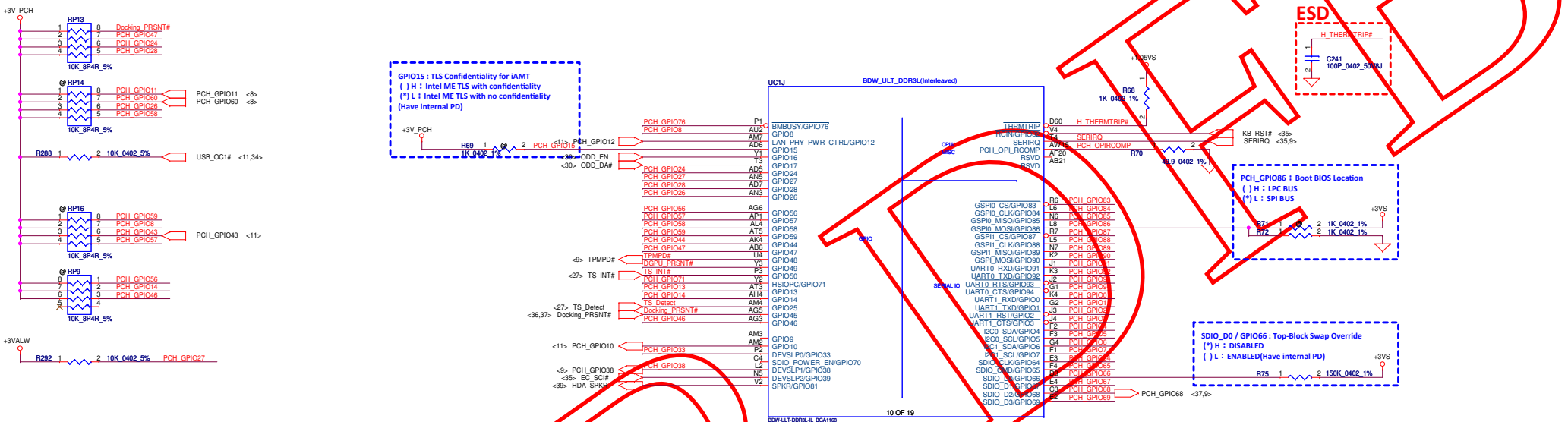
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

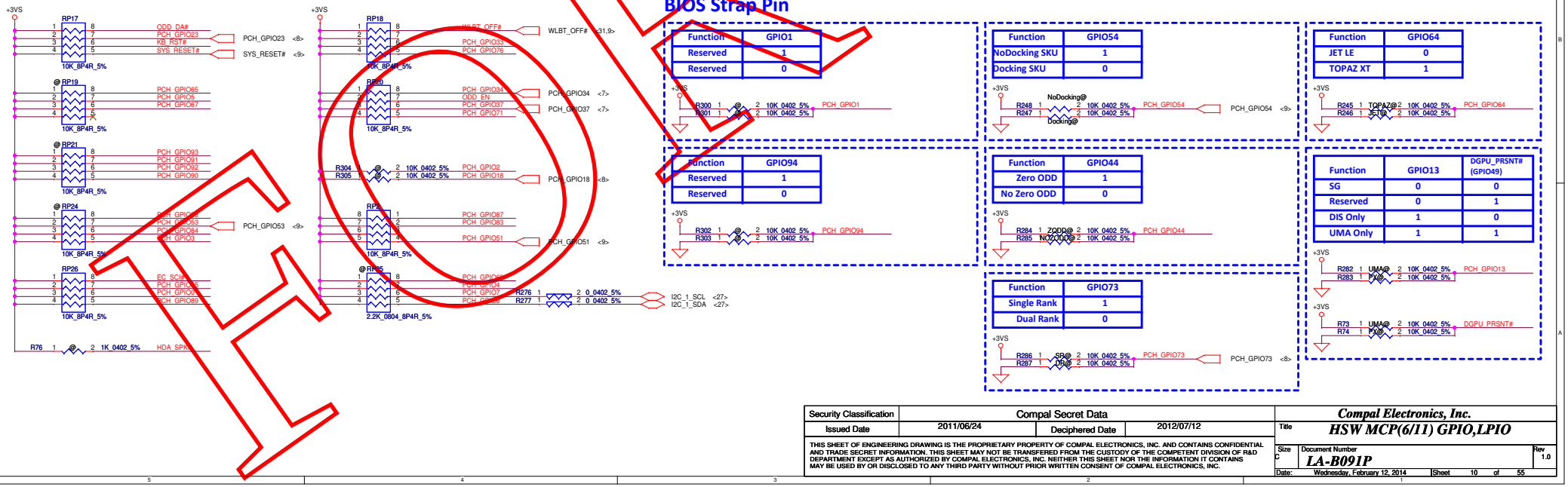
Compal Electronics, Inc.

Title: **HSW MCP(5/11) PM,GPIO,DDI**

Size: C | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 |





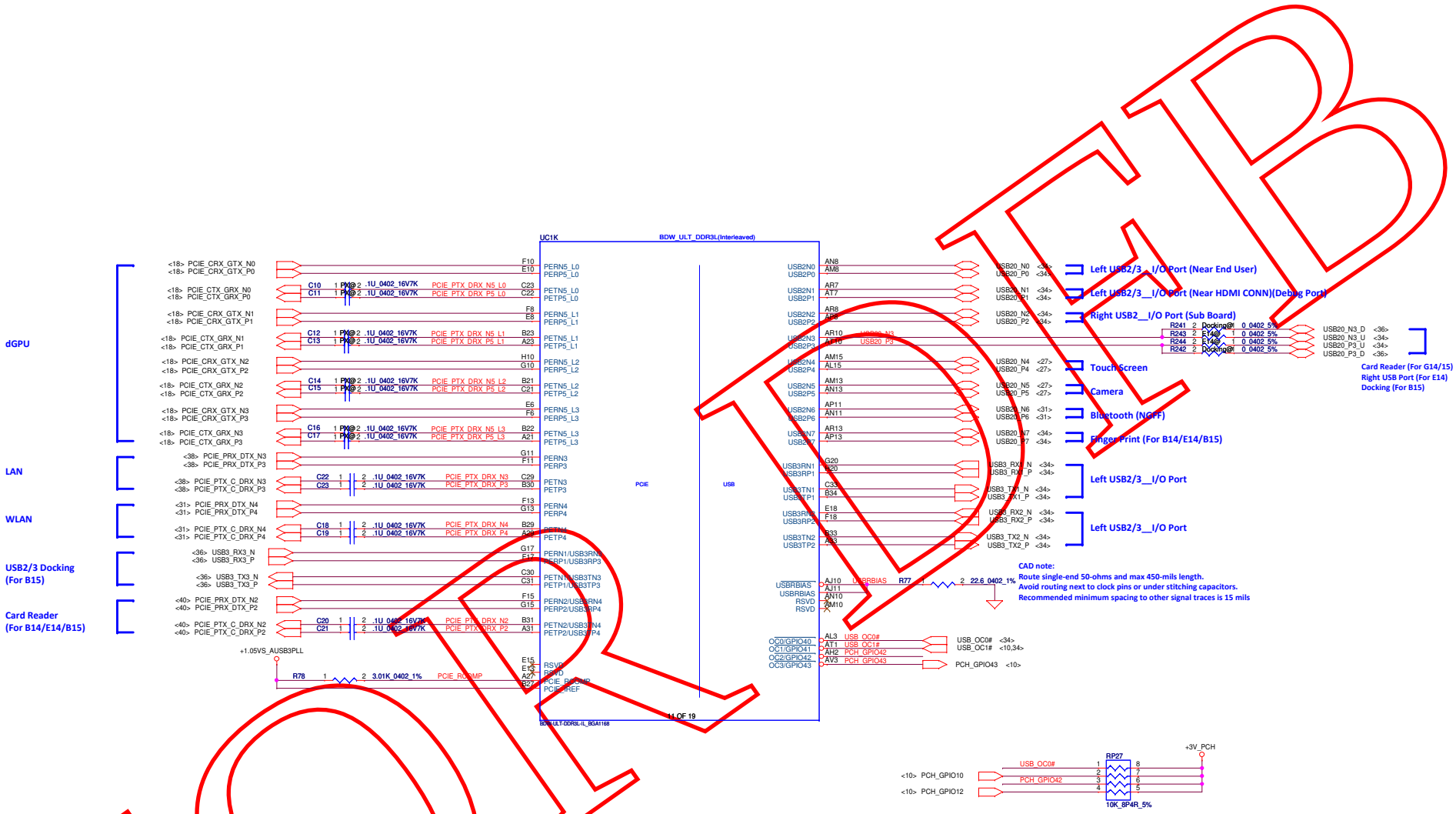
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

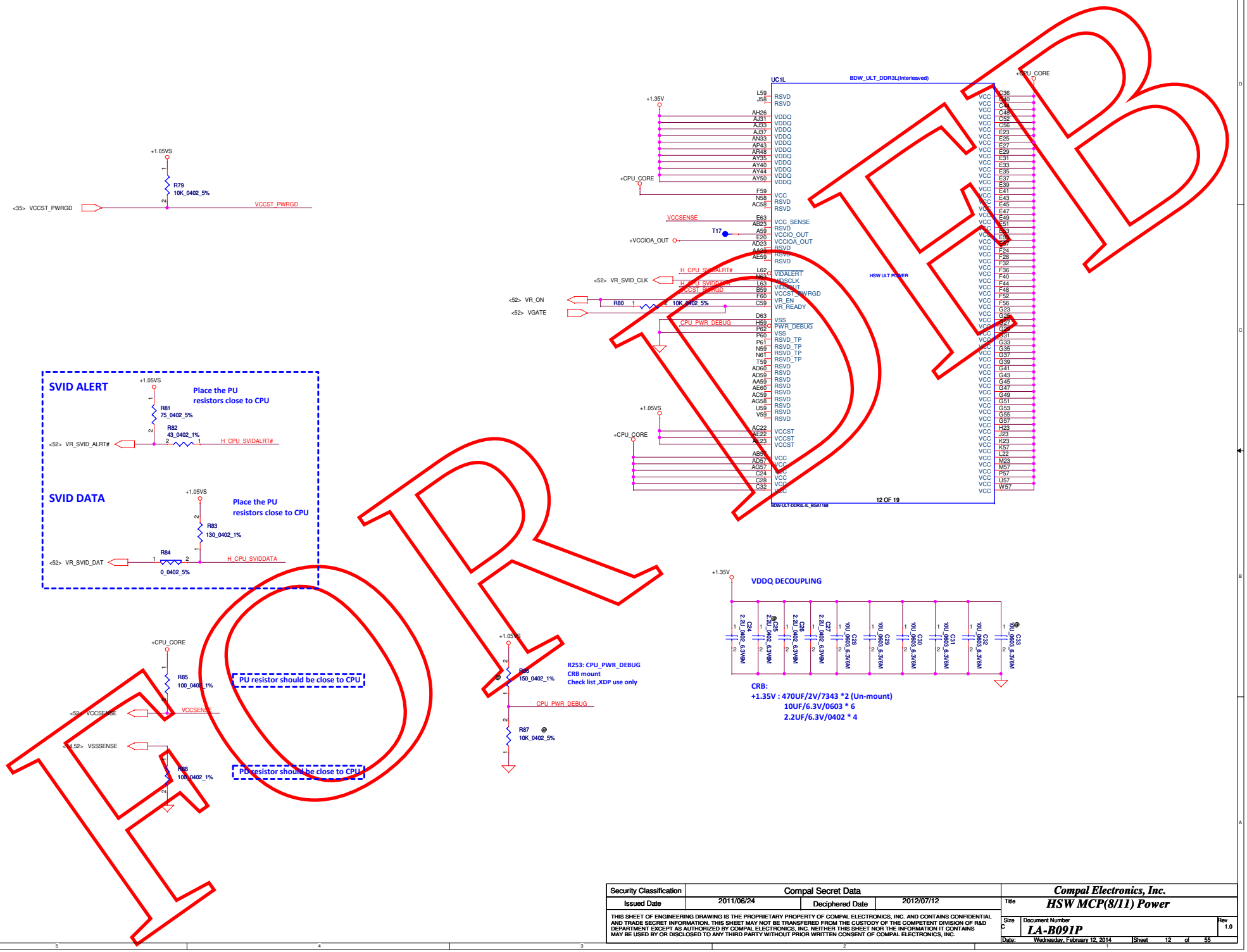
Title: HSW MCP(6/11) GPIO,LPIO

Size: C | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 10 of 55

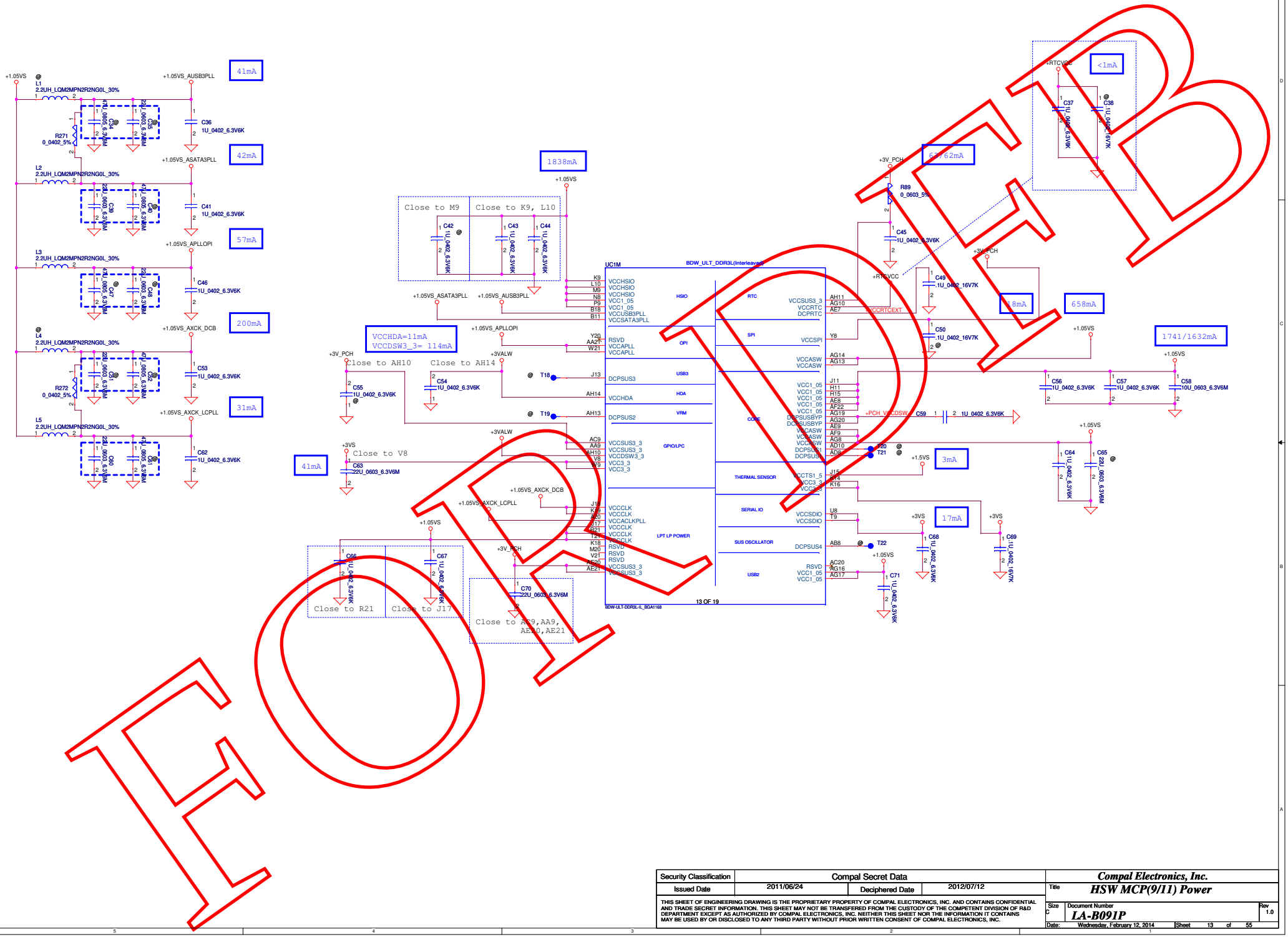


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	HSW MCP(7/11) PCIE,USB		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 11 of 55		



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title	HSW MCP(8/11) Power		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 12 of 55		



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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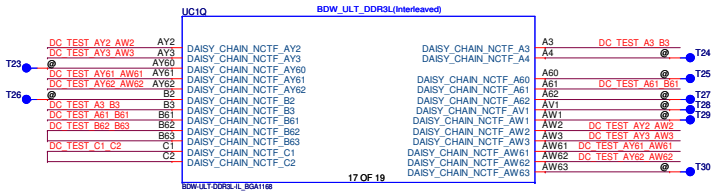
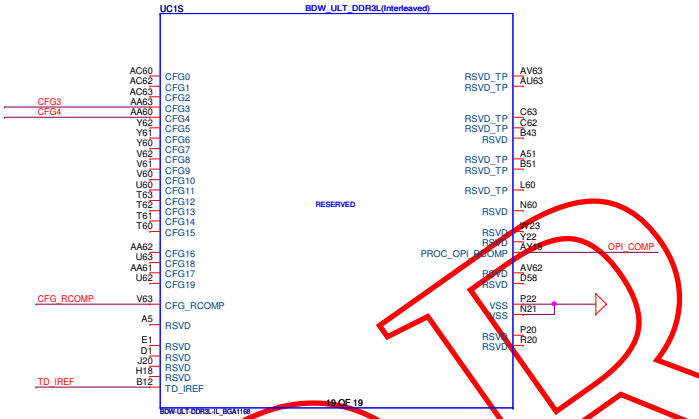
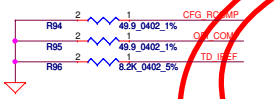
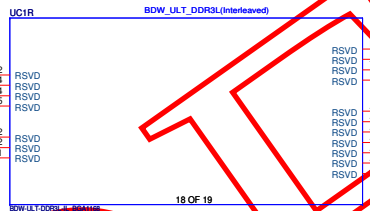
Compal Electronics, Inc.			
Title	HSW MCP(9/11) Power		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014		Sheet 13 of 55	

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	HSW MCP(10/11) GND		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 14 of 55		

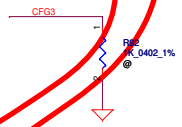




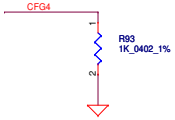




CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title	HSW MCP(11/11) RSVD		
Size	Document Number		Rev
C	LA-B091P		1.0
Date:	Wednesday, February 12, 2014	Sheet	15 of 55

DIMM1
Reverse Type
Near CPU

D/DQ Signals link to CPU
CMD Signals from CPU
Clock Signals from CPU
CTL Signals from CPU
SMBUS Signals link to CPU

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

Layout Note:
Place near JDIMM1.199

Address : 00

ESD

DDR3L SODIMM ODT GENERATION

For ODT & VTT
power control

Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

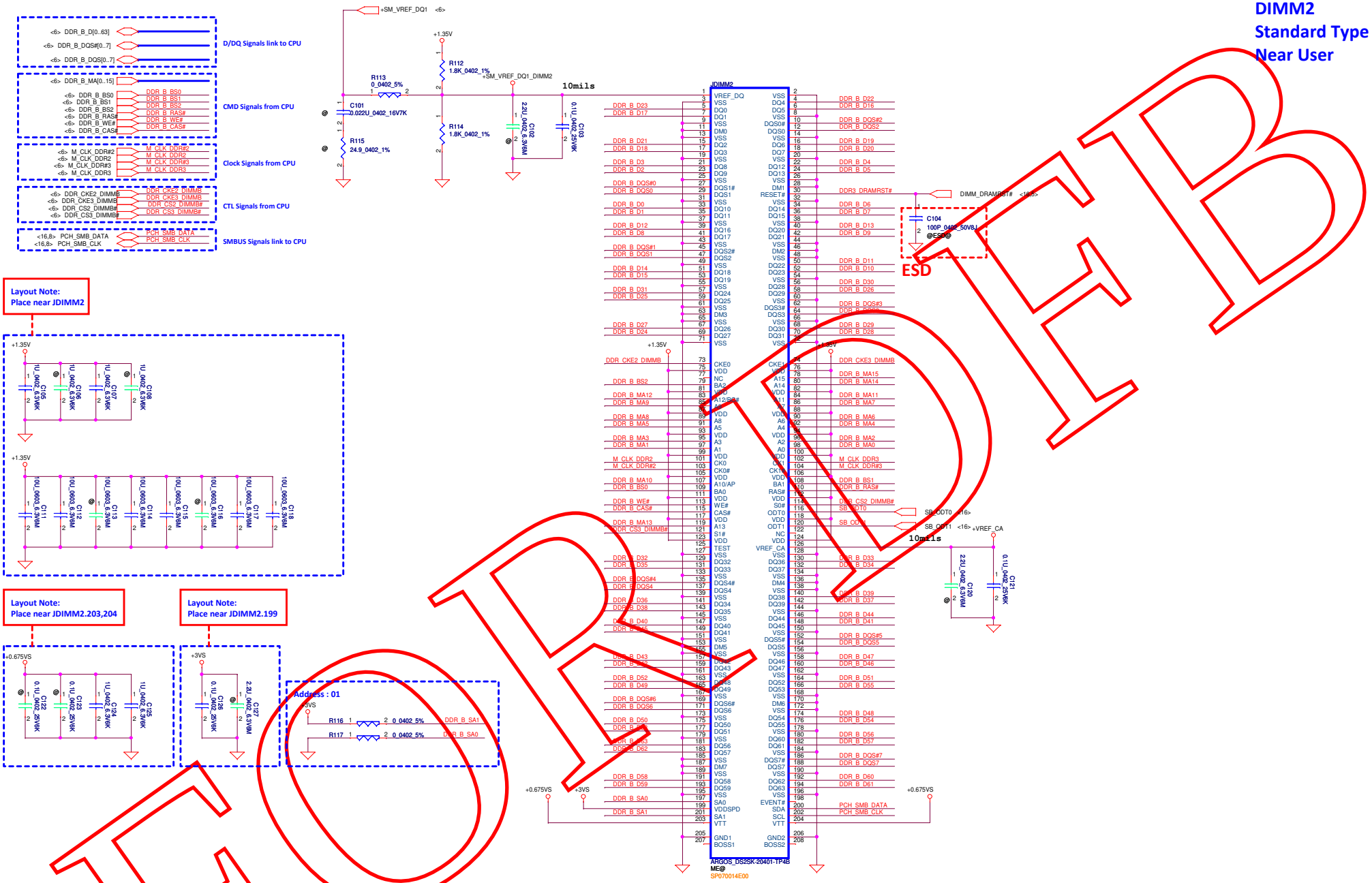
Compal Electronics, Inc.

Title: DDR3L_DIMMA

Size	Document Number	Rev
C	LA-B091P	1.0

Date: Wednesday, February 12, 2014 Sheet 16 of 55

DIMM2
Standard Type
Near User



FOR REVIEW ONLY

Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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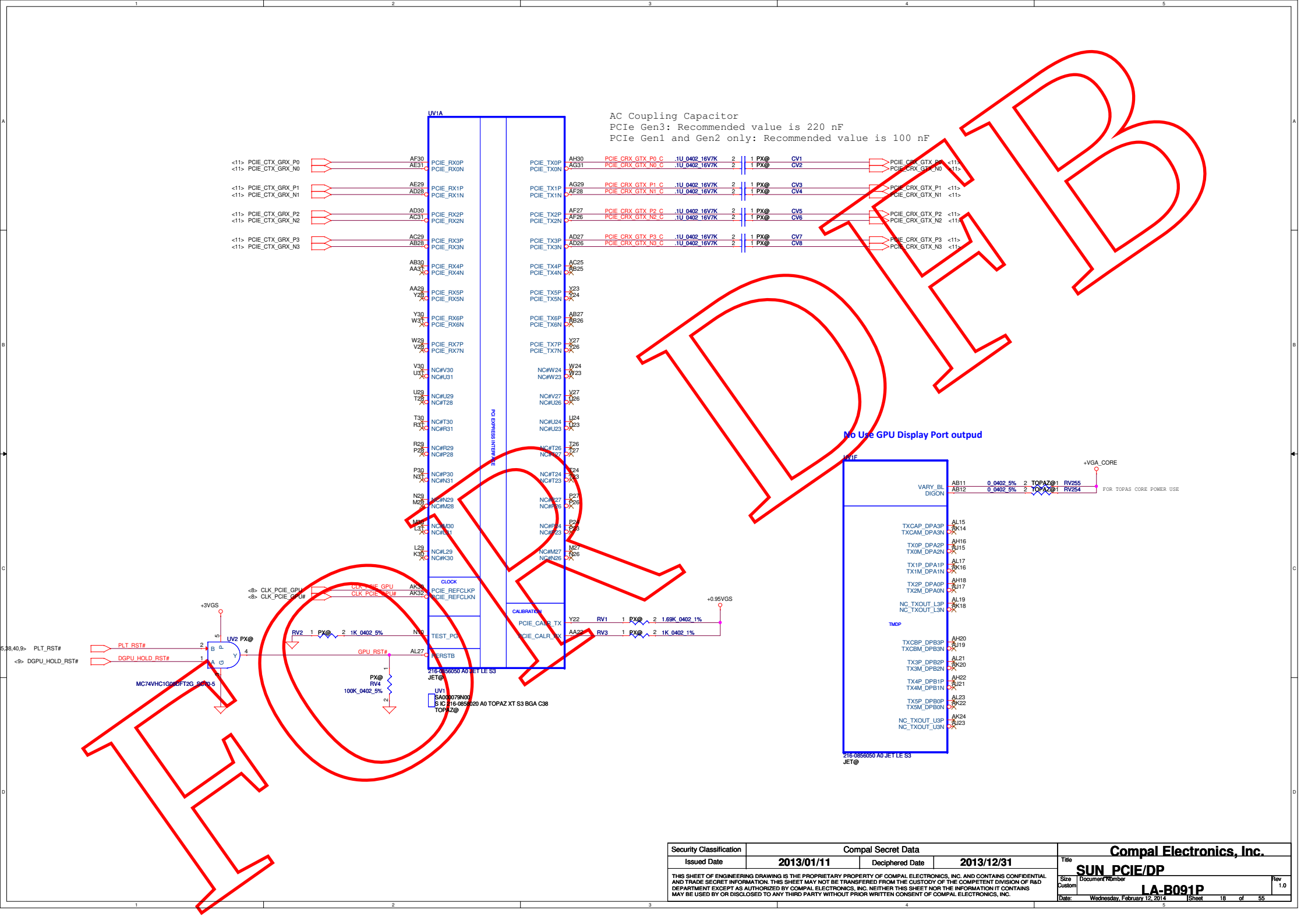
Compal Electronics, Inc.

Title: DDR3L DIMMB

Size	Document Number	Rev
C	LA-B091P	1.0

Date: Wednesday, February 12, 2014 Sheet 17 of 55



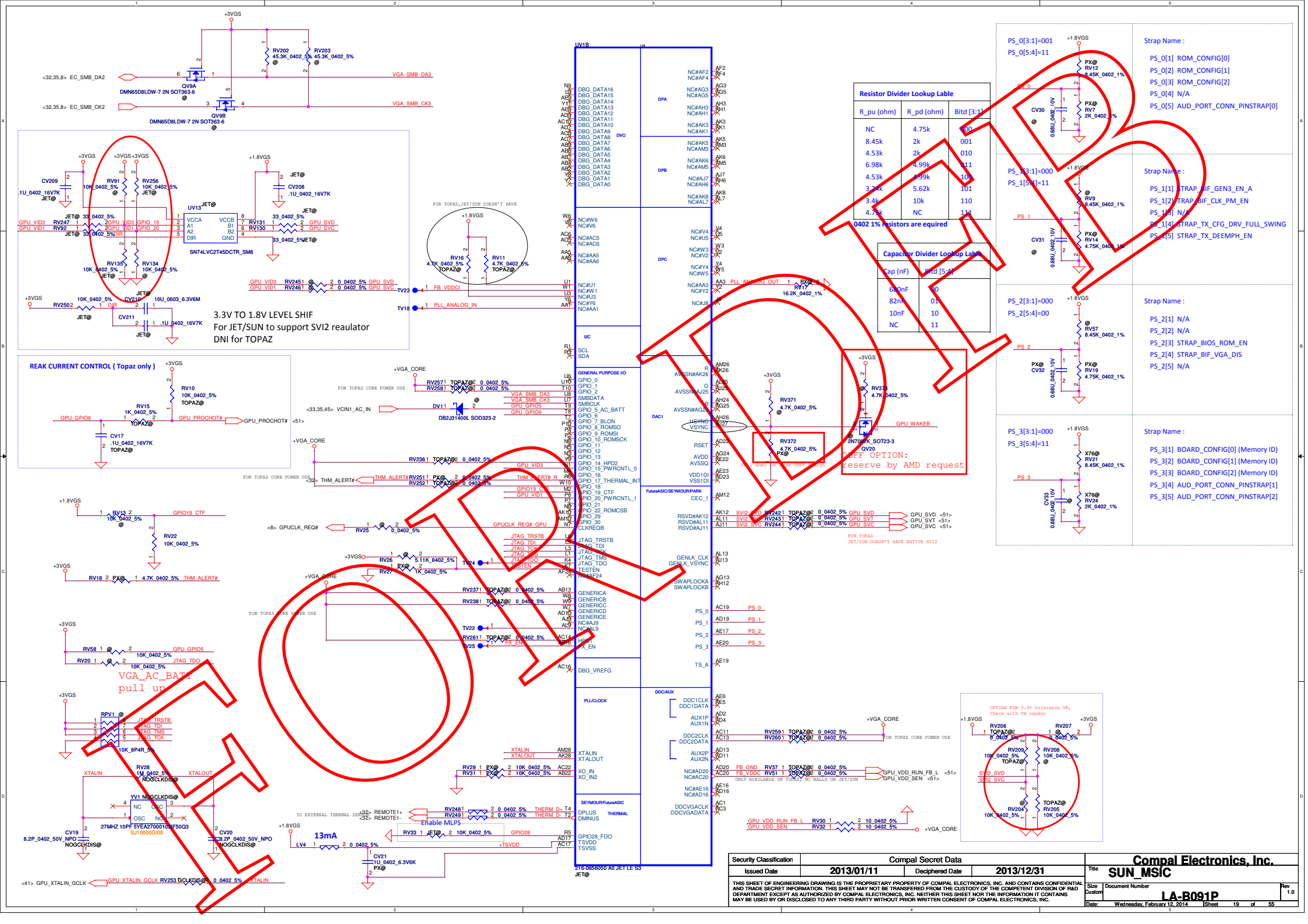
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_PCIE/DP

Size: Custom | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 18 of 55



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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Compal Electronics, Inc.

Title: SUN_MSIC

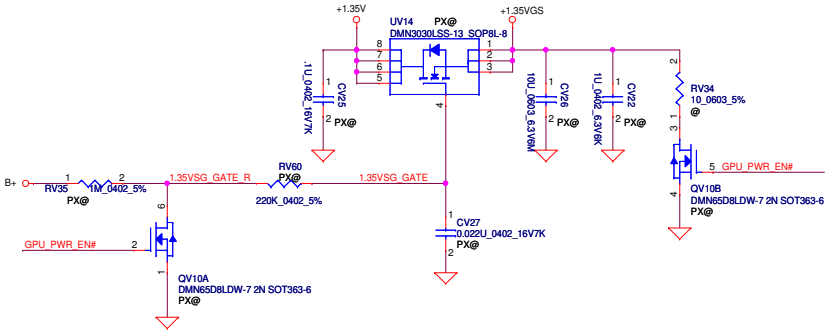
Size: Custom | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 19 of 55

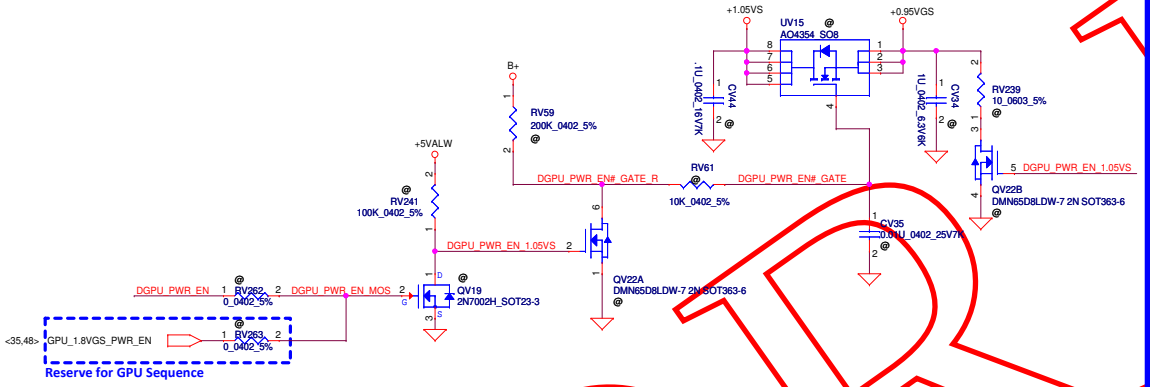
216-0856050 A0 JET LE S3

JET@

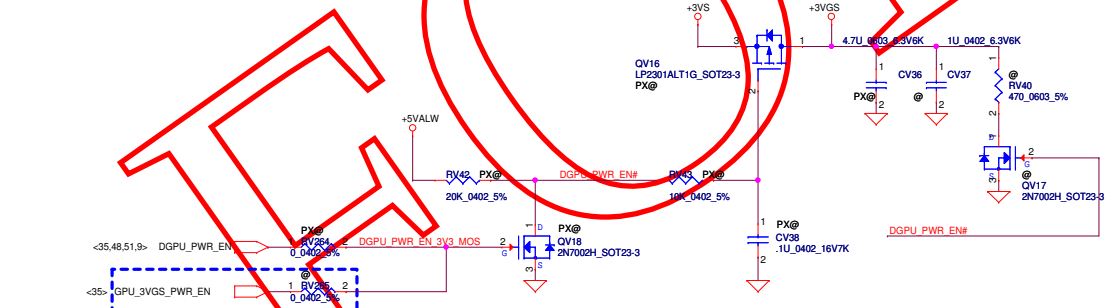
+1.35VS to +1.35VGS (6.234A)



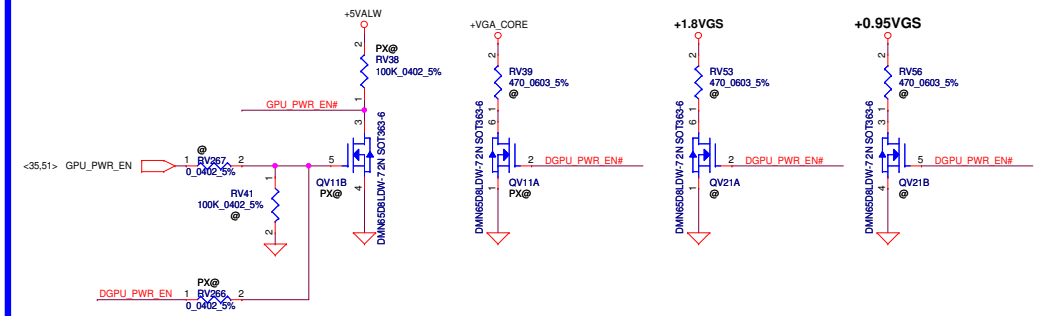
+1.05VS to +0.95VGS



+3VS to +3VS_VGA (25mA)



No Use GPU Display Port outpud



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_Power/GND

Size: Custom | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 20 of 55

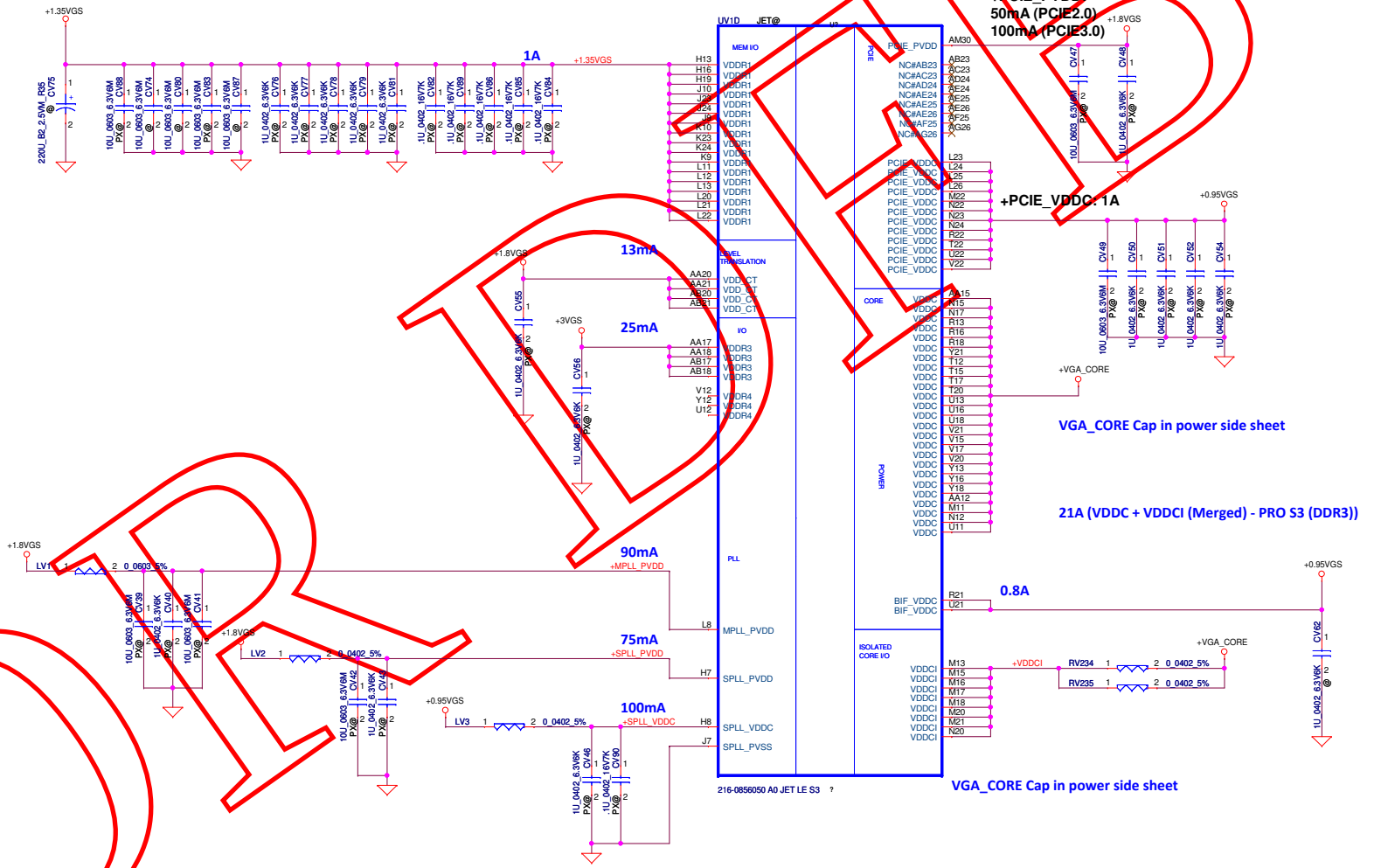
+VGA_CORE		10uF	2.2uF	1uF	0.1uF
VDDC	TBD	7	16	4	3
VDDCI	3.5A				

+0.95VGS		10uF	1uF	0.1uF
PCIE_VDDC	1A	1	5(1@)	0
BIF_VDDC	0.8A	0	1(1@)	0
SPLL_VDDC	100mA	0	1	1

+1.35VGS		10uF	1uF	0.1uF	0.01uF
VDDR1	1.5A	5(3@)	5	5	0

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	0
MPLL_PVDD	130mA	2	1	0
SPLL_PVDD	75mA	0	1	0
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	0	1	0
+TSVDD	13mA	0	1	0
+DP_VDDR		1	1	0
+DP_VDDC		0	1	1

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	1	0



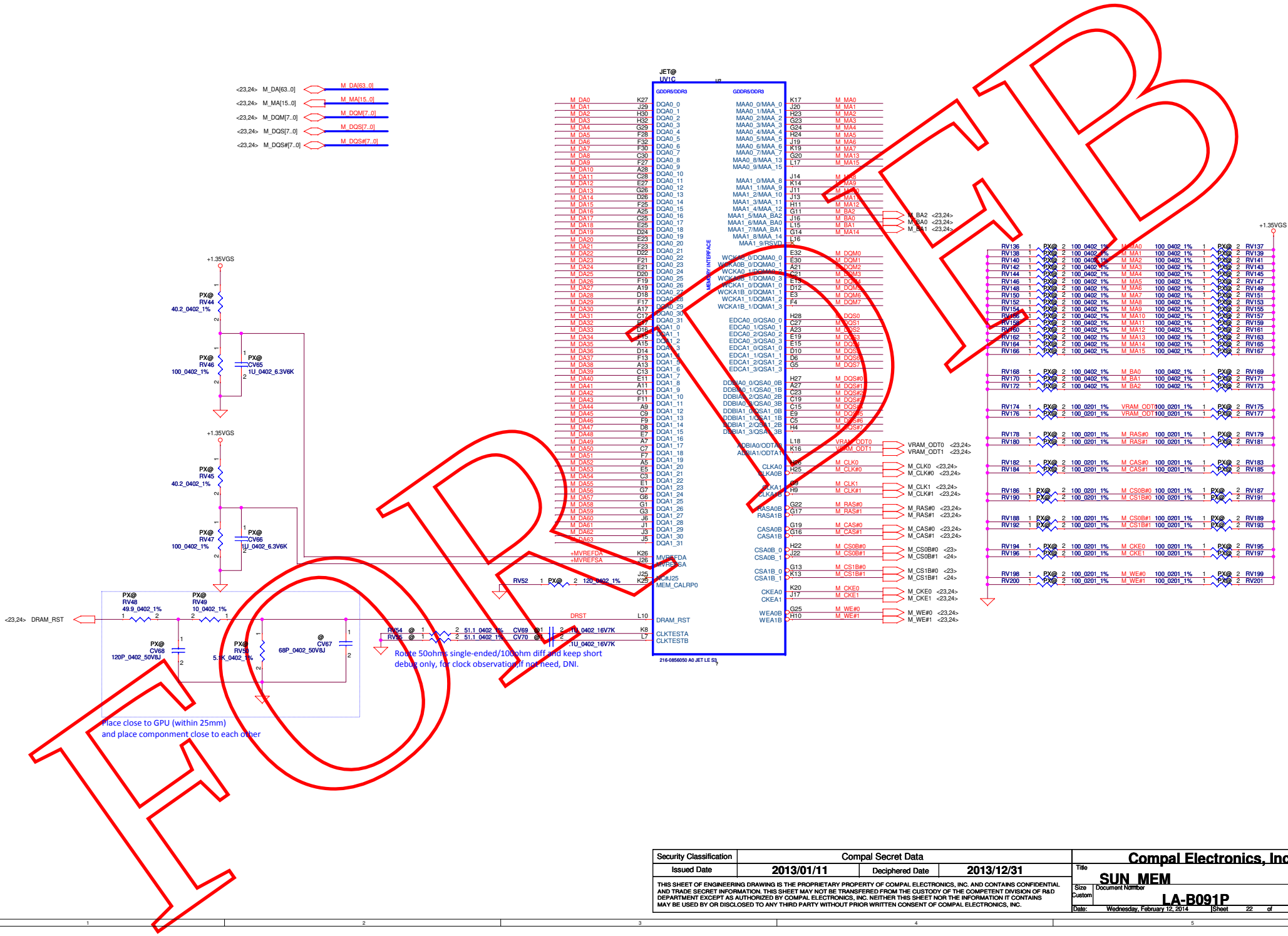
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_Power

Size: Custom | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 21 of 55



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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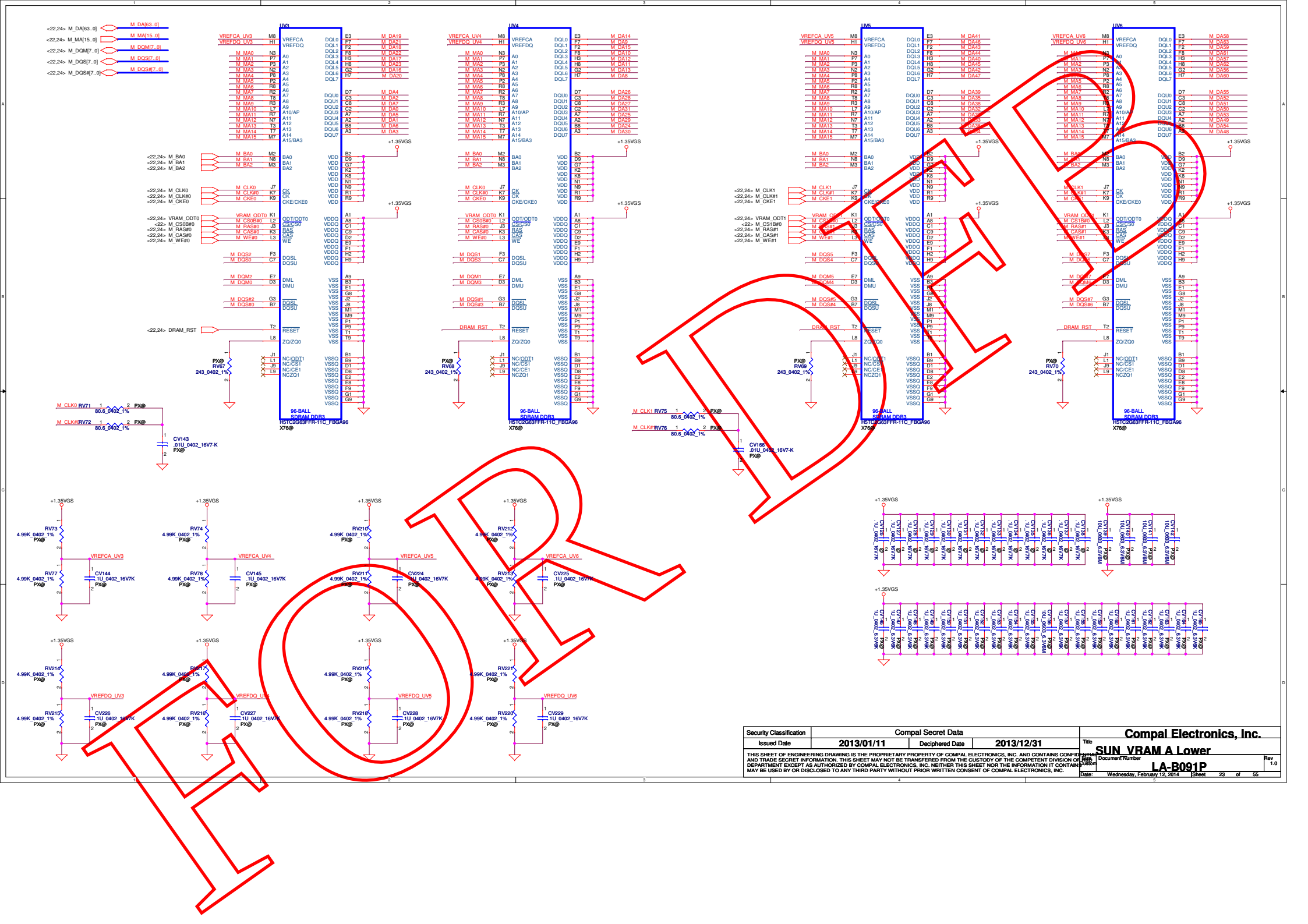
Compal Electronics, Inc.

Title: **SUN_MEM**

Size: Custom | Document Number: **LA-B091P** | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 22 of 55



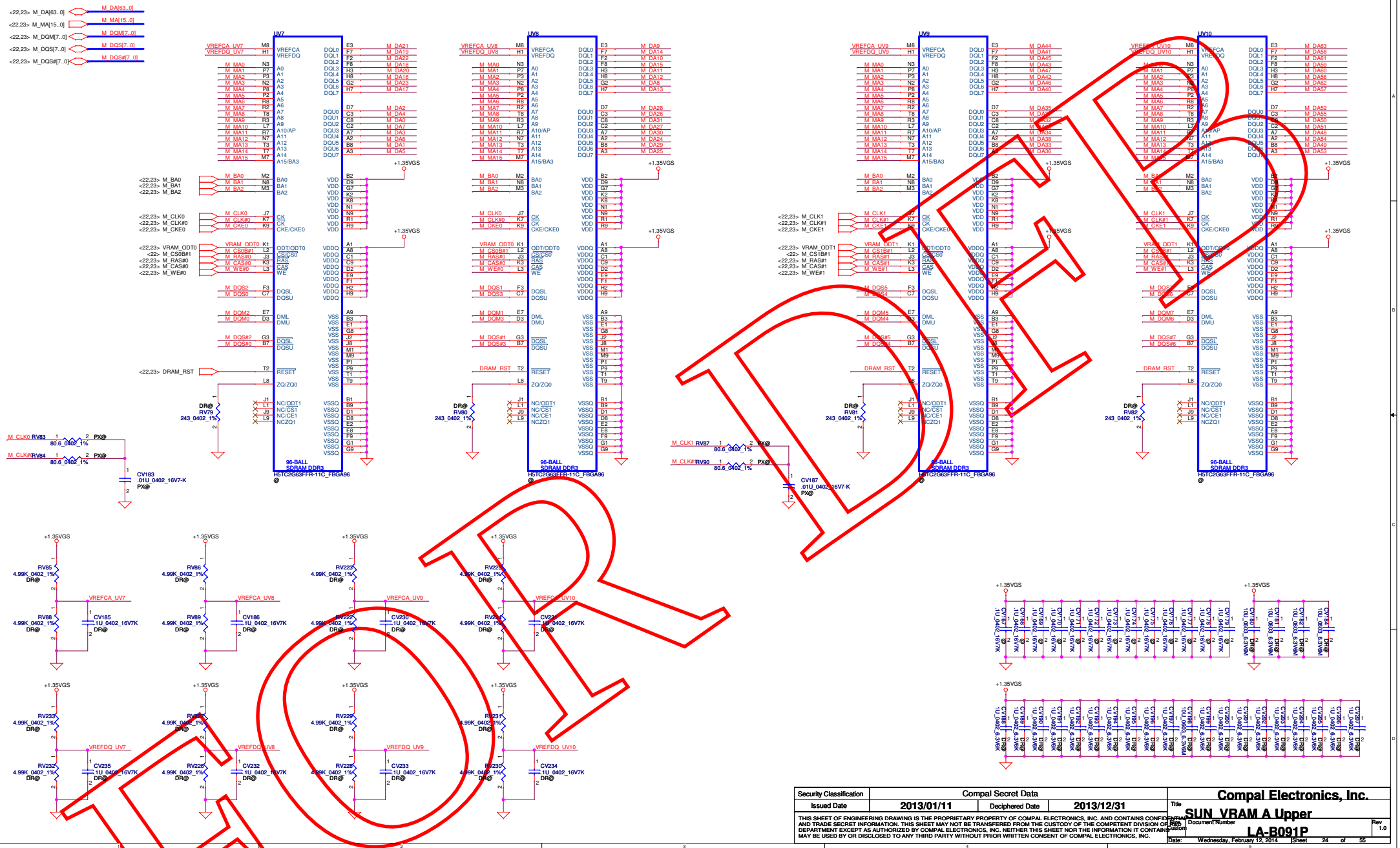
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_VRAM A Lower

Size: B | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 23 of 55



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_VRAM A Upper

Size: B | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 24 of 55

Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: **SUN_VRAM A Lower**

Size: Custom | Document Number: **LA-B091P** | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 25 of 55

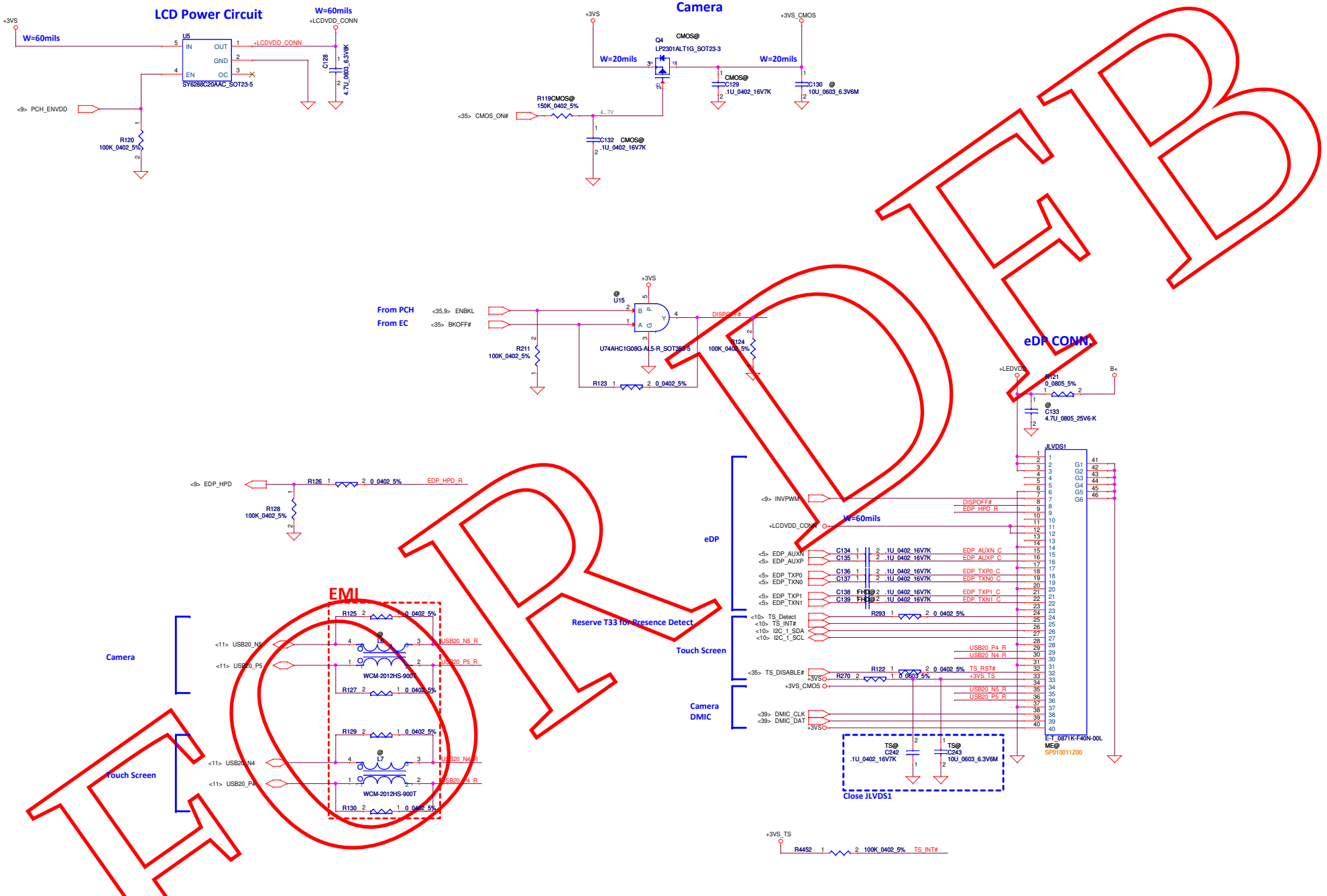
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: **SUN_VRAM A Upper**

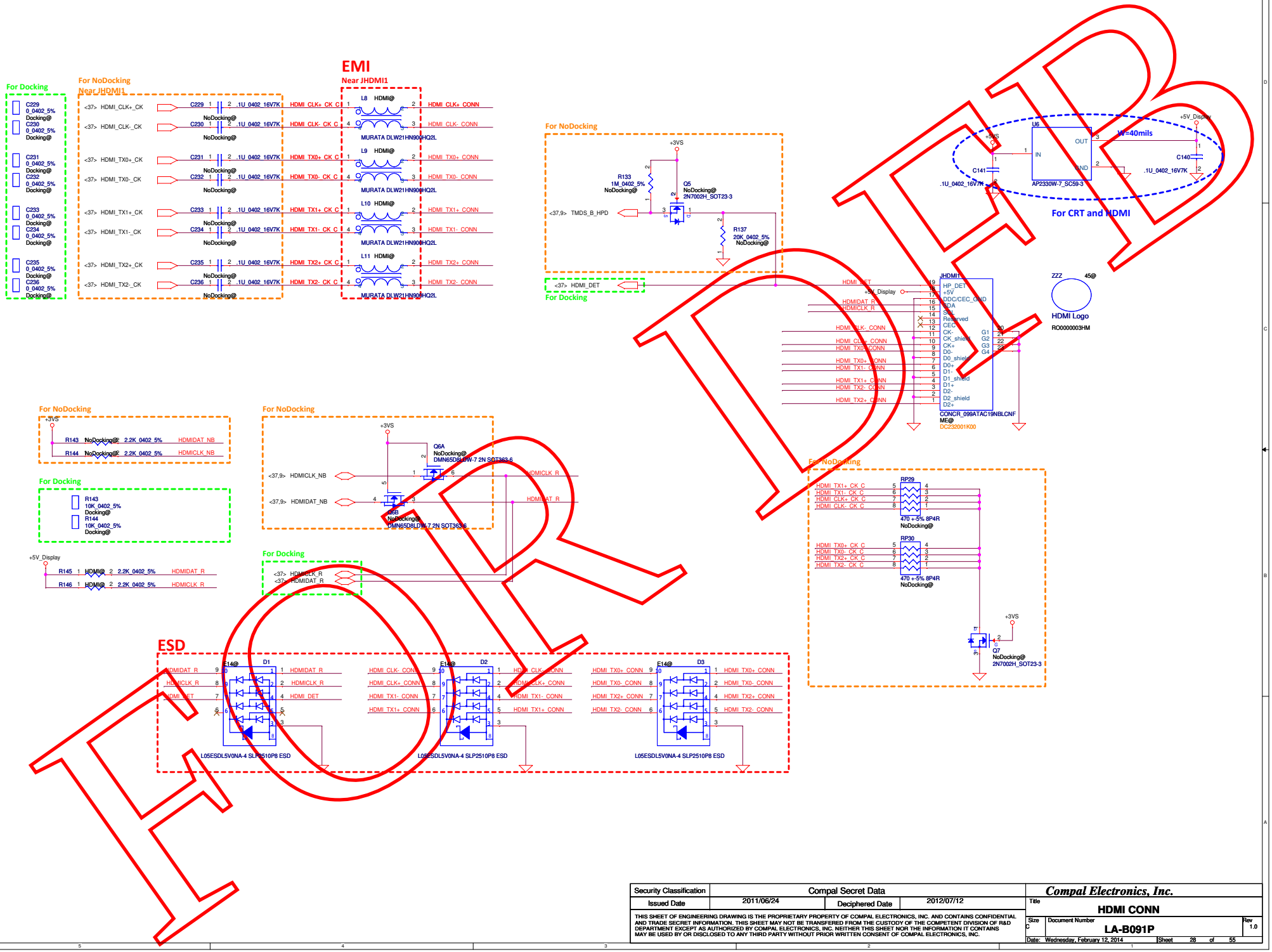
Size: Custom | Document Number: **LA-B091P** | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 26 of 55



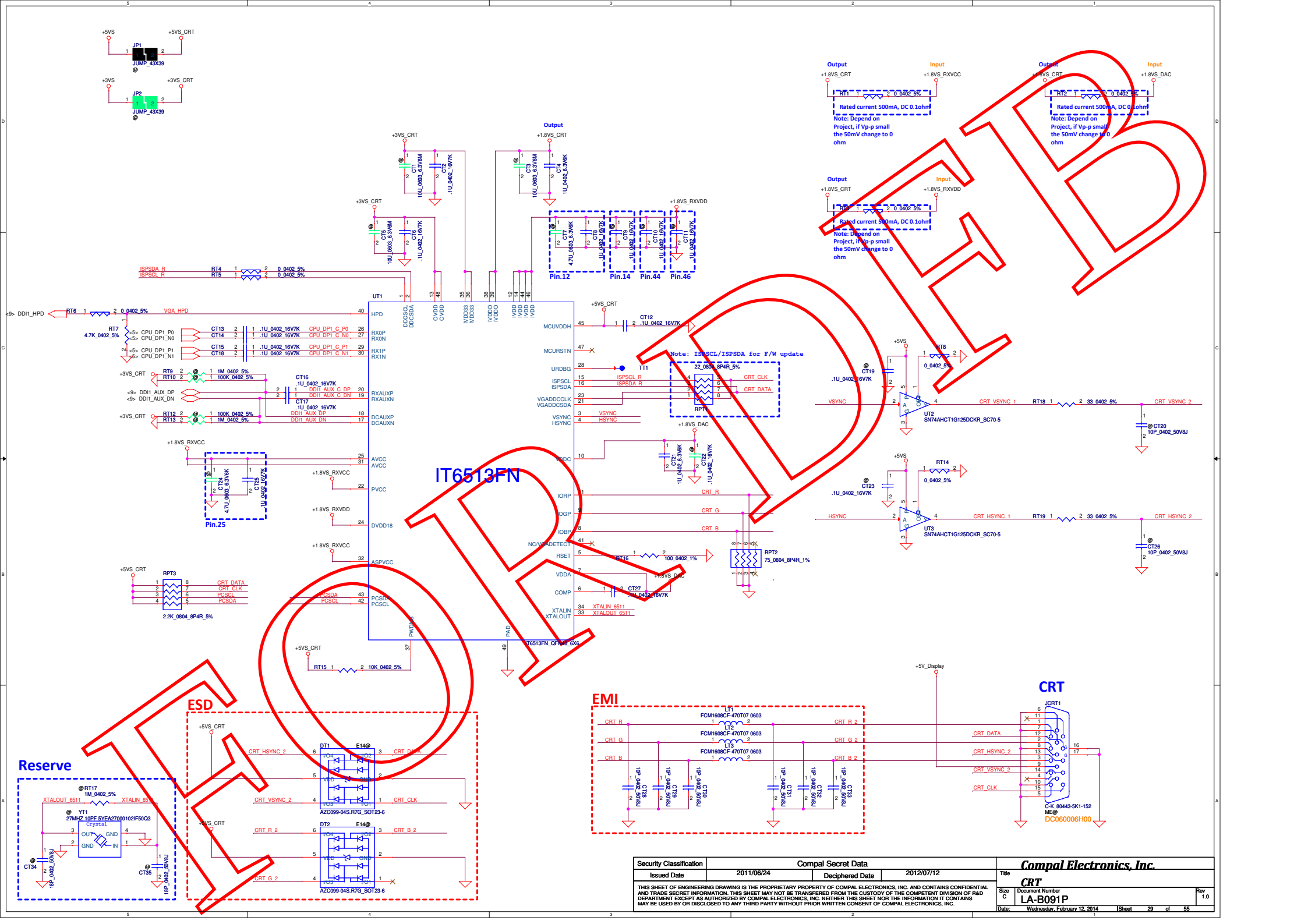
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title	LVDS/CAMERA		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 27 of 55		

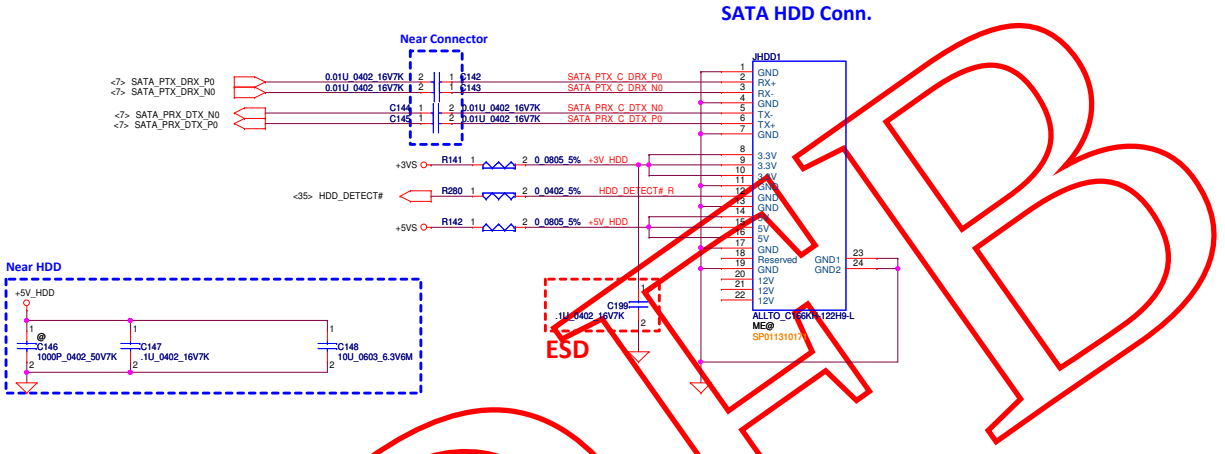


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12

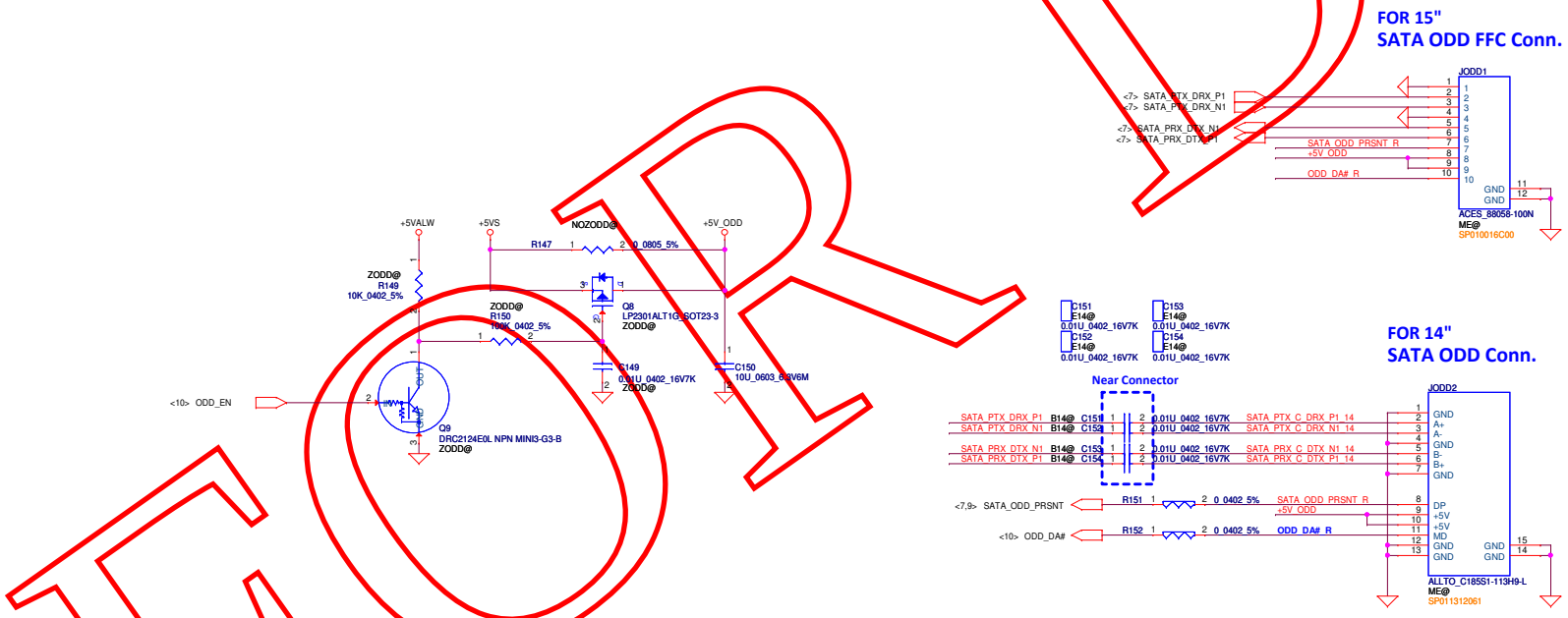
Title	HDMI CONN		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 28 of 55		


IT6513FN
ESD
EMI
CRT
Reserve
Pin.12
Pin.14
Pin.44
Pin.46
Pin.25
Note: ISPSCL/ISPSDA for F/W update
Rated current 500mA, DC 0.1ohm
Note: Depend on Project, if Vp-p small the 50mV change to 0 ohm
UT1
IT6513FN_QFN48_6X6
UT2
SN74AHCT1G125DCKR_SC70-5
UT3
SN74AHCT1G125DCKR_SC70-5
AZC099-04S.R7G_SOT23-6
CK_80443-5K1-152
DC060006H00
Compal Secret Data
2011/06/24
2012/07/12
Compal Electronics, Inc.
CRT
LA-B091P
Wednesday, February 12, 2014

HDD



ODD

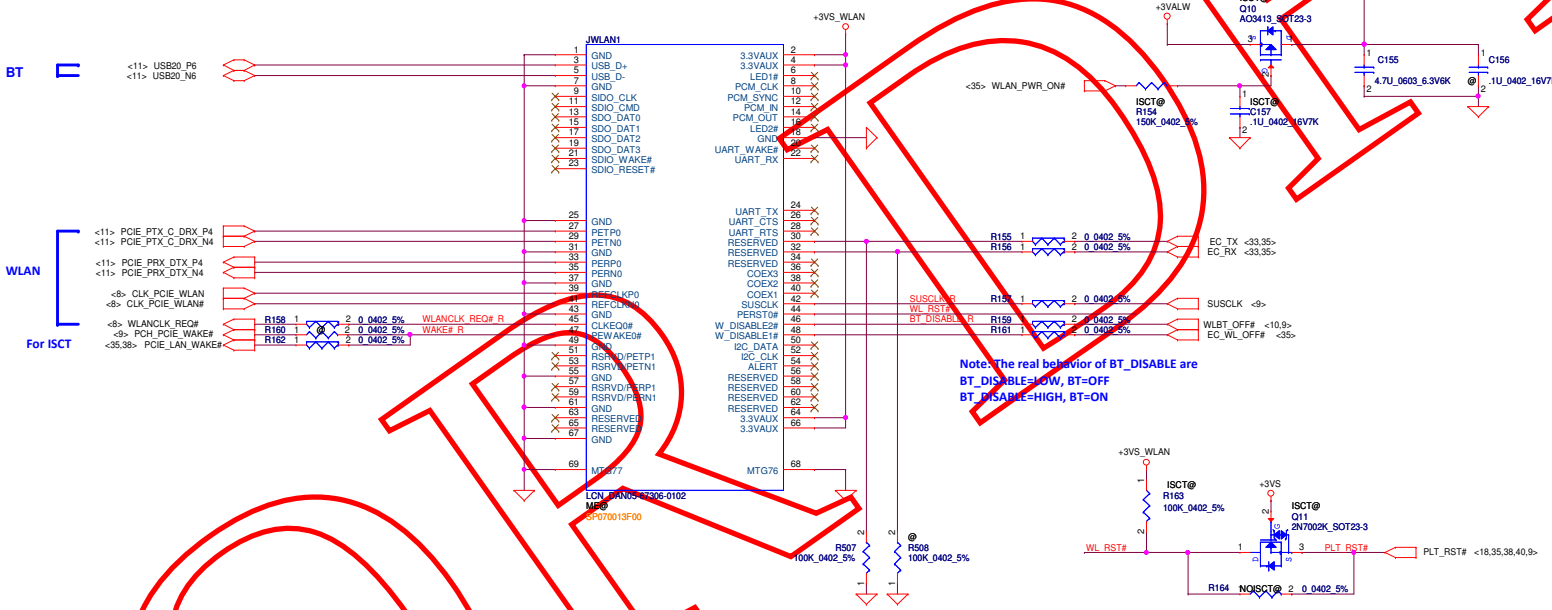


Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title: HDD/ODD/BT Connector			
Size: C	Document Number: LA-B091P		Rev: 1.0
Date: Wednesday, February 12, 2014	Sheet 30 of 55		

NGFF for WLAN / BT(Key E)

Support ISCT(Intel Smart Connect Technology)

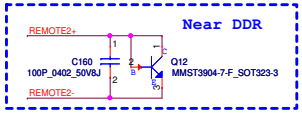


FOR REVIEW

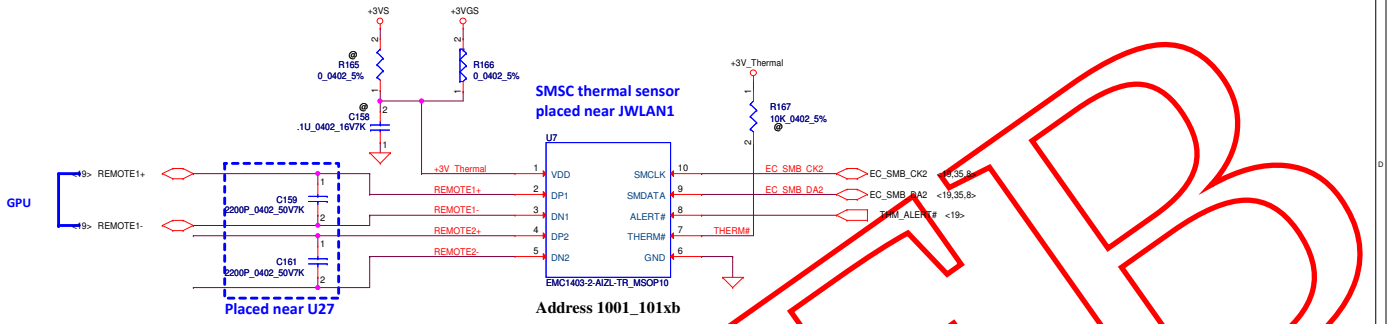
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title	Mini-Card/NEW Card/SIM		
Size	Document Number	LA-B091P	Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 31 of 55		

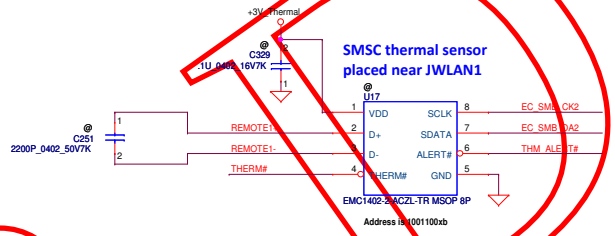
3 Channel

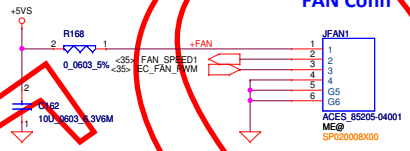


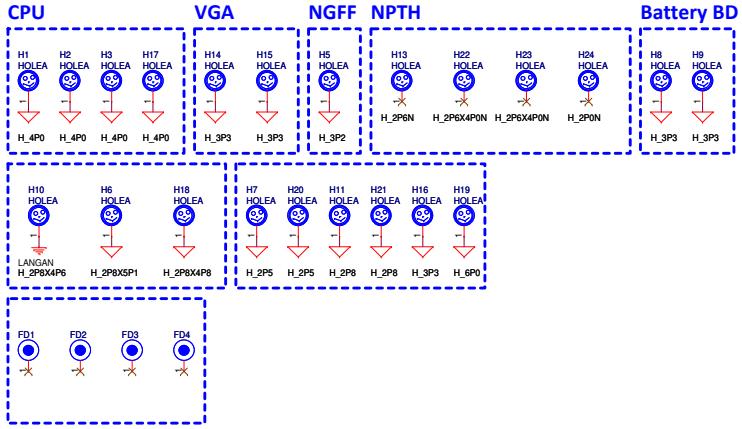
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



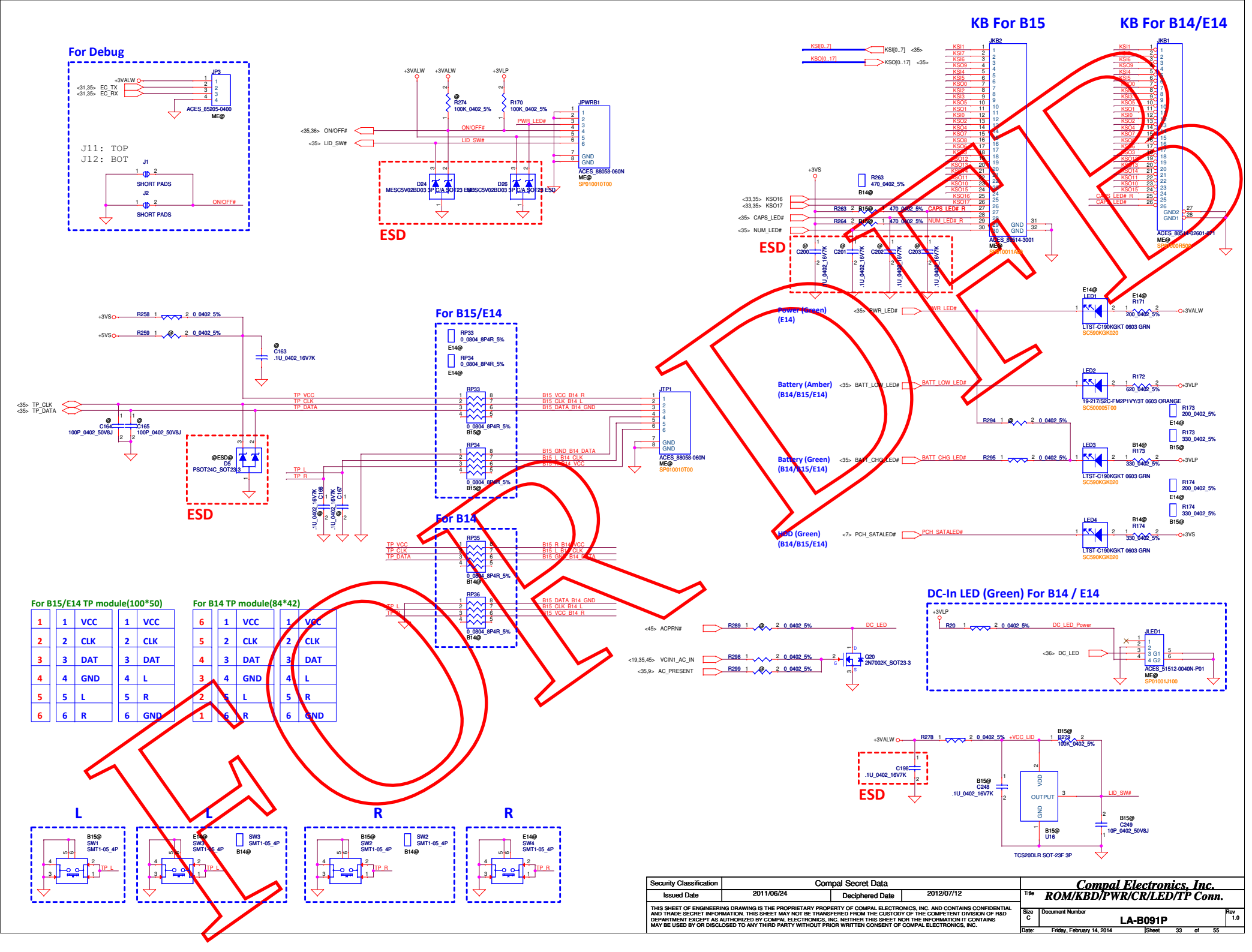
2 Channel







Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	Fintek-Thermal IC/FAN/screw		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 32 of 55		

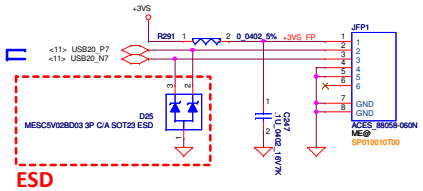


Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Title	Compal Electronics, Inc. ROM/KBD/PWR/CR/LED/TP Conn.
Size	C
Document Number	LA-B091P
Rev	1.0
Date:	Friday, February 14, 2014
Sheet	33 of 55

Finger Print

Finger Print
(For B14/E14/B15)

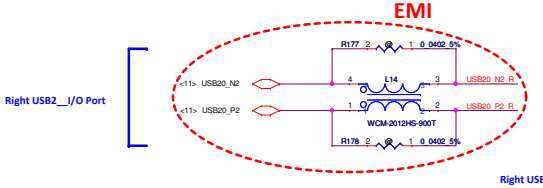


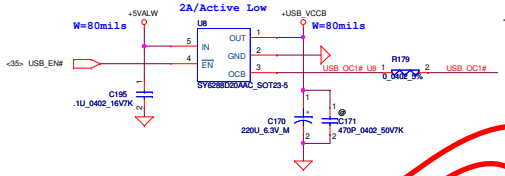
ESD

USB2.0_Port

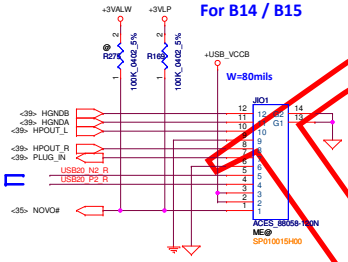
EMI

Right USB2__I/O Port



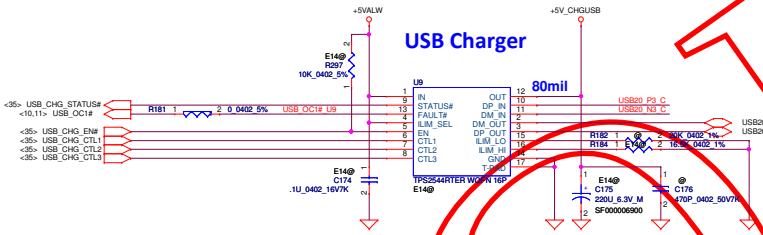


For B14 / B15



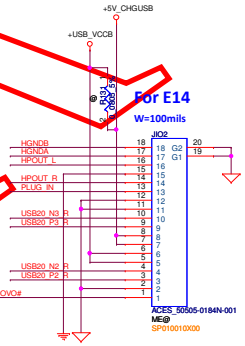
Right USB2__I/O Port

USB Charger



Right USB2__I/O Port
(For E14)

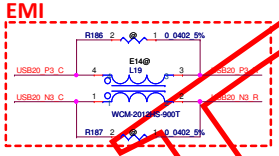
For E14



Right USB2__I/O Port
(For E14)

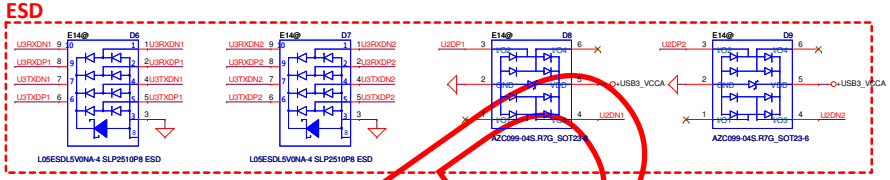
Right USB2__I/O Port

EMI



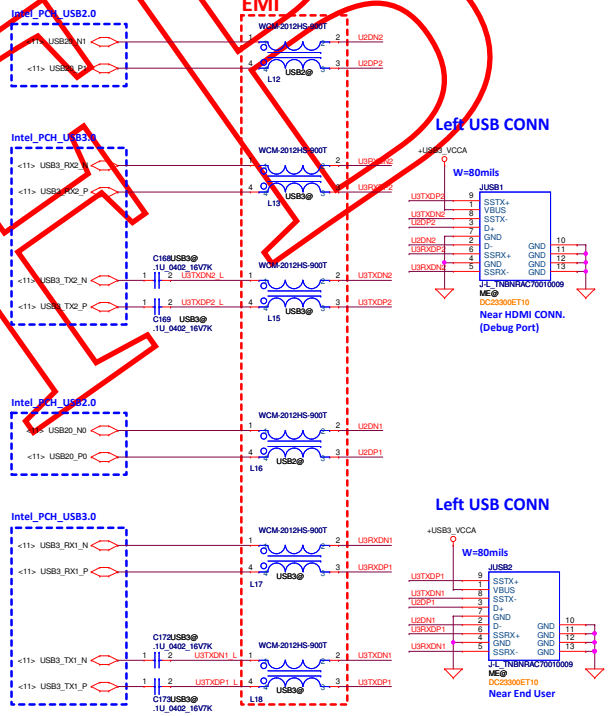
ESD

ESD

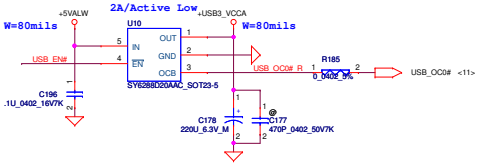


USB3.0_Port

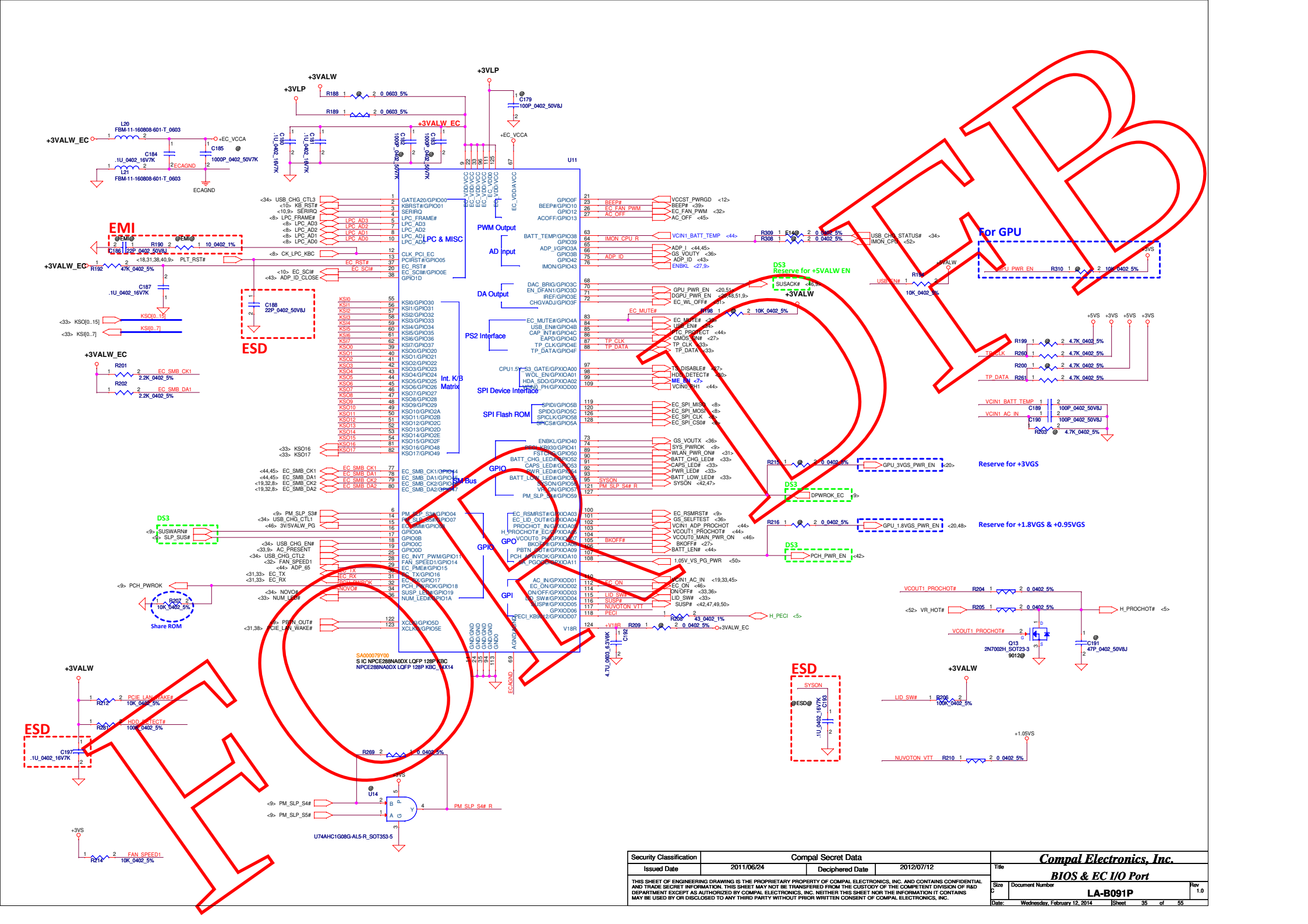
EMI



Place TX AC coupling Cap (C843~C850). Close to connector



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	USB3.0/Left USB Ports		
Document Number			Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 34 of 55		


+3VALW_EC
+3VLP
+3VALW
+EC_VCCA
ECAGND
EMI
ESD
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SMBus
GPO
GPI
U11
For GPU
Reserve for +5VALW EN
Reserve for +3VGS
Reserve for +1.8VGS & +0.95VGS
Share ROM
NPCE288NA0DX LQFP 128P KBC
U74AHC1G08G-AL5-R_SOT353-5
Security Classification
Compal Secret Data
Issued Date
2011/06/24
Deciphered Date
2012/07/12
Compal Electronics, Inc.
BIOS & EC I/O Port
LA-B091P
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Wednesday, February 12, 2014
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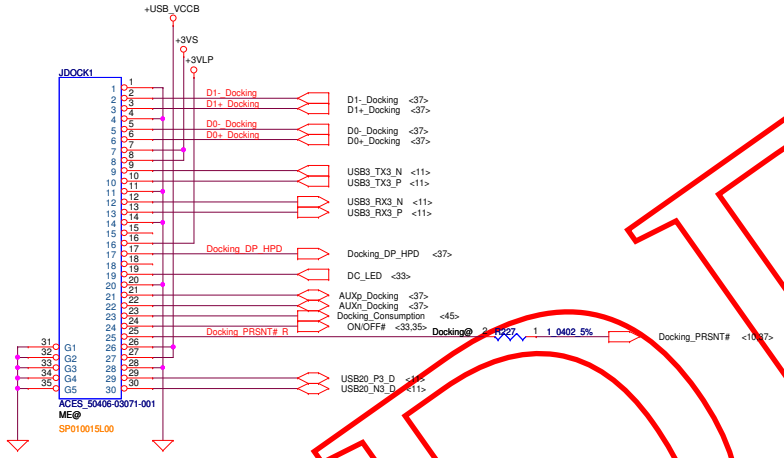
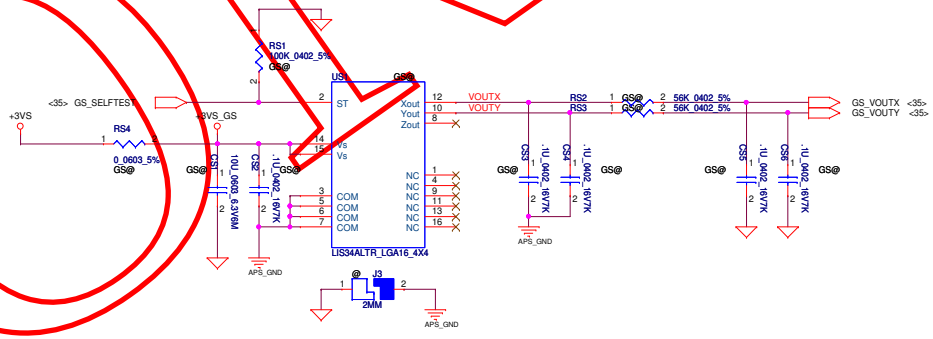
To Docking BD



APS (G-Sensor)



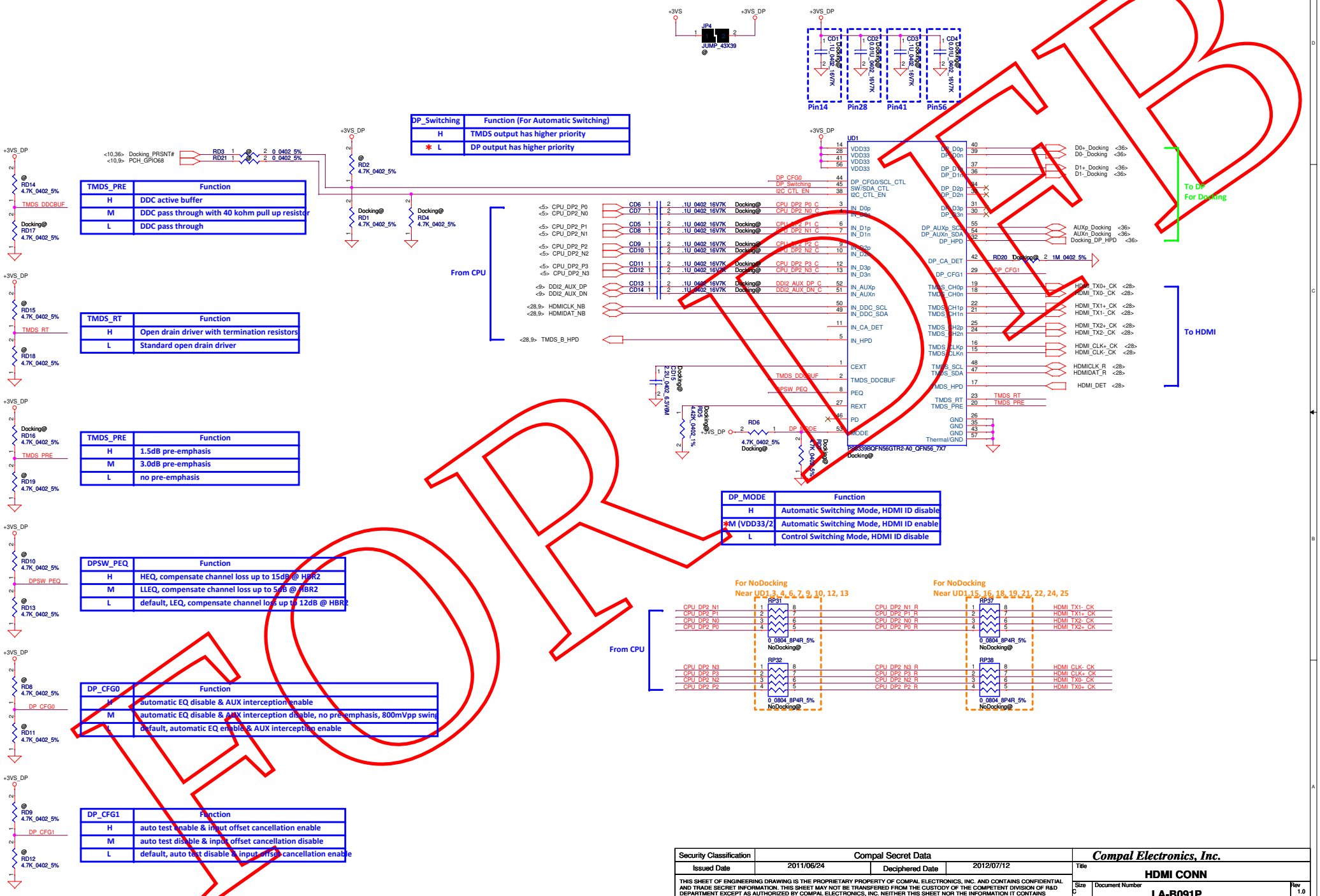
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Docking

Size: C | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 36 of 55


DP_Switching | Function (For Automatic Switching)
H | TMDS output has higher priority
* L | DP output has higher priority
TMDS_PRE | Function
H | DDC active buffer
M | DDC pass through with 40 kohm pull up resistor
L | DDC pass through
TMDS_RT | Function
H | Open drain driver with termination resistors
L | Standard open drain driver
TMDS_PRE | Function
H | 1.5dB pre-emphasis
M | 3.0dB pre-emphasis
L | no pre-emphasis
DPSW_PEQ | Function
H | HEQ, compensate channel loss up to 15dB @ HBR2
M | LLEQ, compensate channel loss up to 5dB @ HBR2
L | default, LEQ, compensate channel loss up to 12dB @ HBR2
DP_CFG0 | Function
H | automatic EQ disable & AUX interception enable
M | automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing
L | default, automatic EQ enable & AUX interception enable
DP_CFG1 | Function
H | auto test enable & input offset cancellation enable
M | auto test disable & input offset cancellation disable
L | default, auto test disable & input offset cancellation enable
DP_MODE | Function
H | Automatic Switching Mode, HDMI ID disable
*M (VDD33/2) | Automatic Switching Mode, HDMI ID enable
L | Control Switching Mode, HDMI ID disable
From CPU
To DP For Docking
To HDMI
UD1
PS8339BQFN56GTR2-A0_QFN56_7X7
JP4
JUMP_43X39
For NoDocking Near UD1 3, 4, 6, 7, 9, 10, 12, 13
For NoDocking Near UD1 15, 16, 18, 19, 21, 22, 24, 25
Pin14
Pin28
Pin41
Pin56
Security Classification | Compal Secret Data
Issued Date | 2011/06/24
Deciphered Date | 2012/07/12
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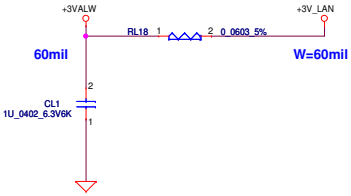
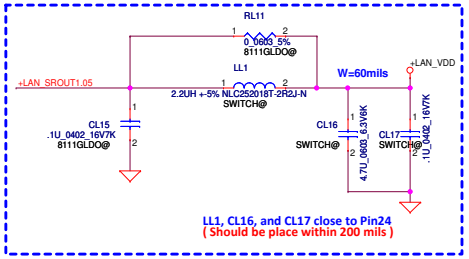
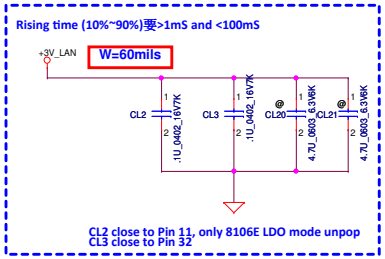
Compal Electronics, Inc.
Title: HDMI CONN
Size: C | Document Number: LA-B091P | Rev: 1.0
Date: Wednesday, February 12, 2014 | Sheet 37 of 55

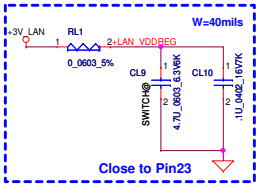


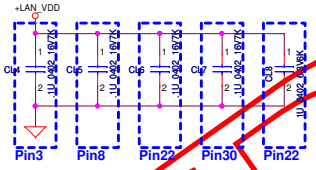


		1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
SA00005V700	RTL8111G	LDO	X	X	X	O	O
	~~RTL8111G~~	~~External~~	~~X~~	~~X~~	~~X~~	~~X~~	~~O~~
	RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
SA00005Y00	RTL8106E	LDO	X	X	X	X	X

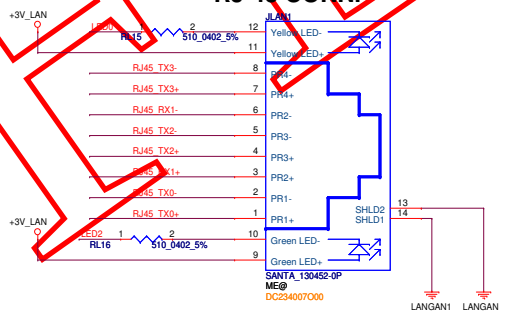
Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.

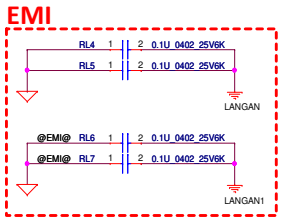


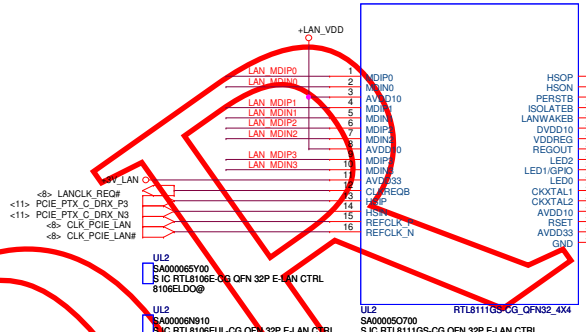


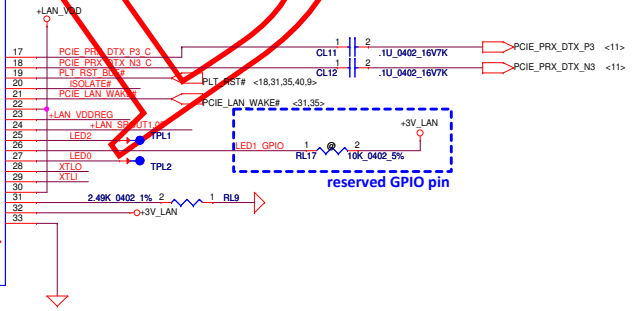


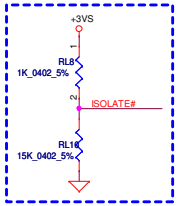
RJ-45 CONN.

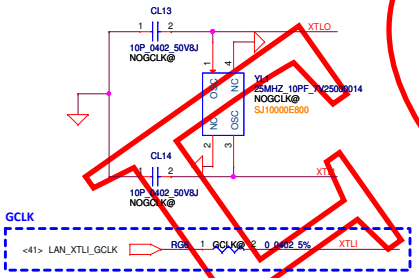


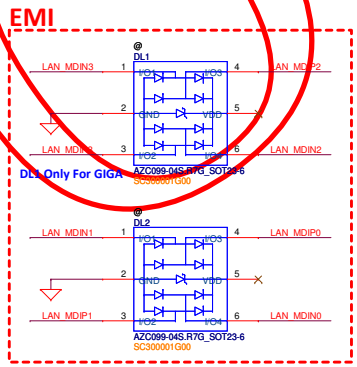


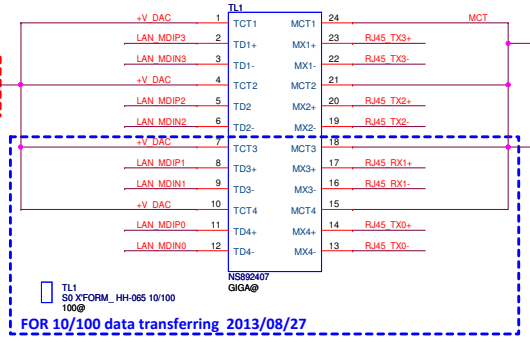


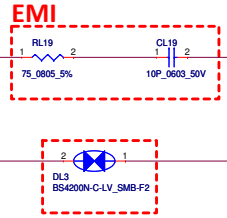




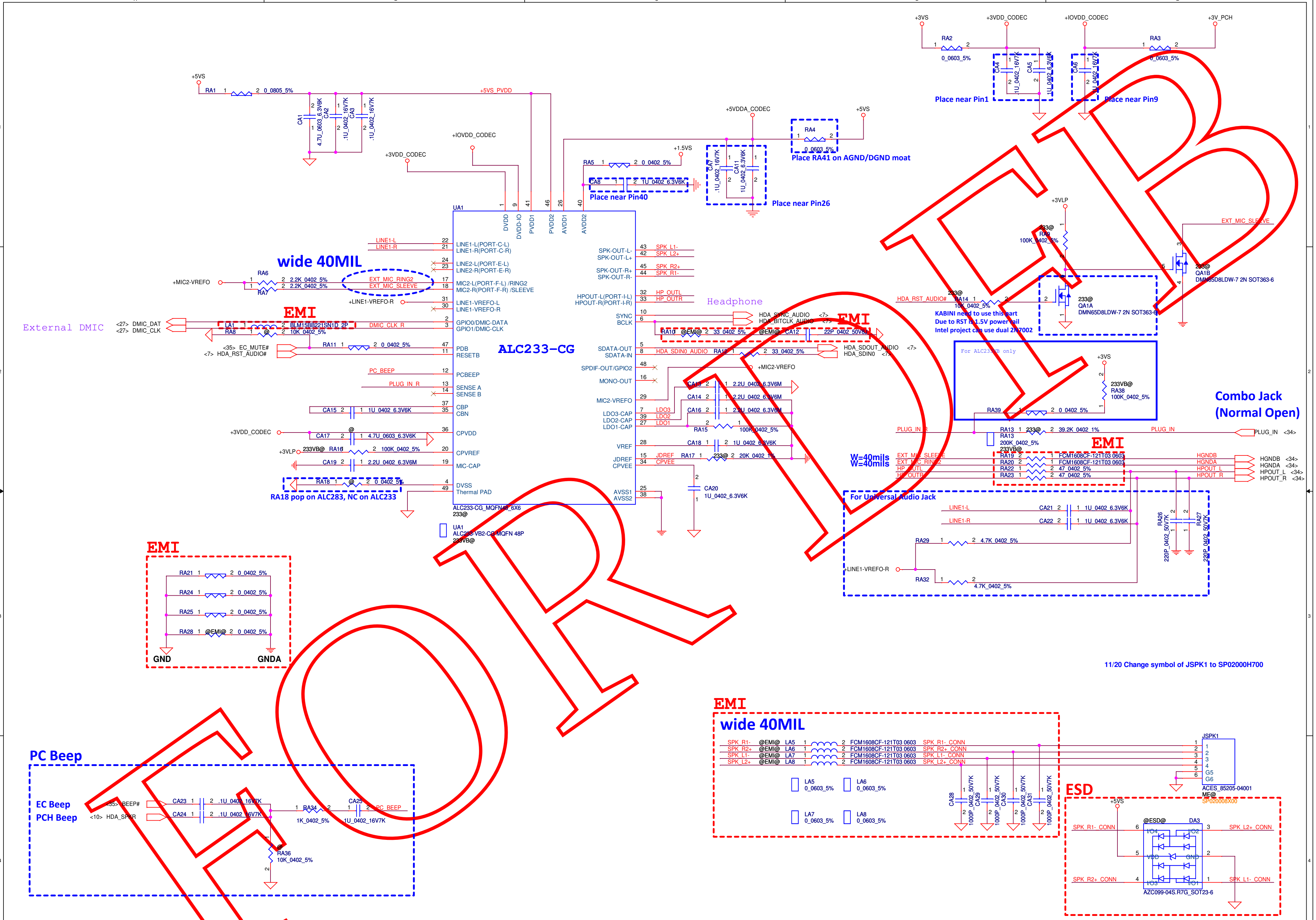




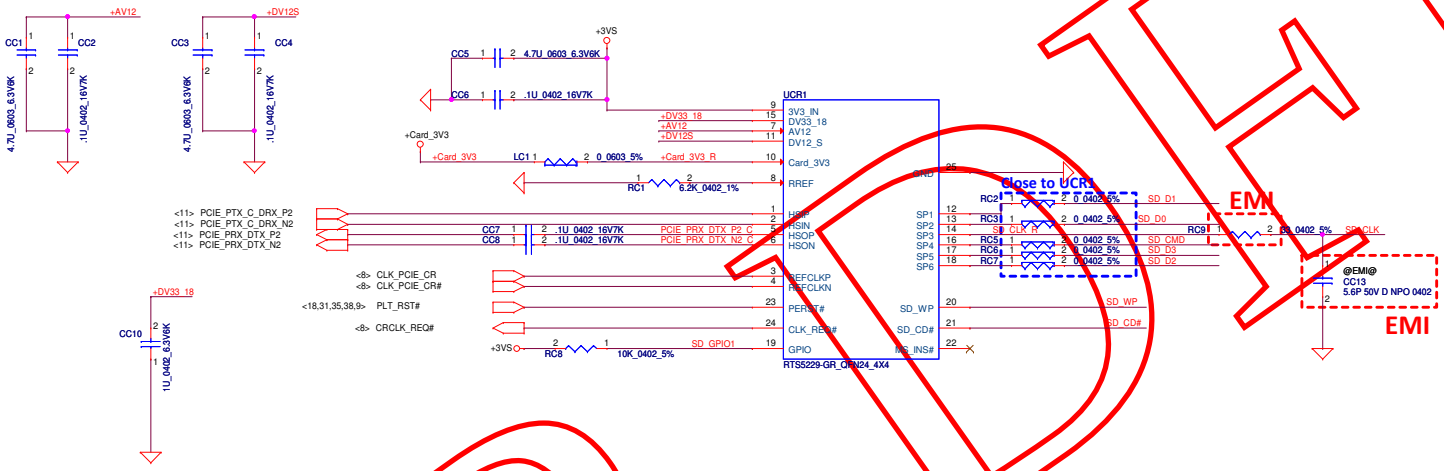




Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	LAN RTL8411-CG		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 38 of 55		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/07/12	Title: HD Audio Codec_ALC3225
			Size: C Document Number: LA-B091P Rev: 1.0
			Date: Wednesday, February 12, 2014 Sheet 39 of 55



FOR PDB

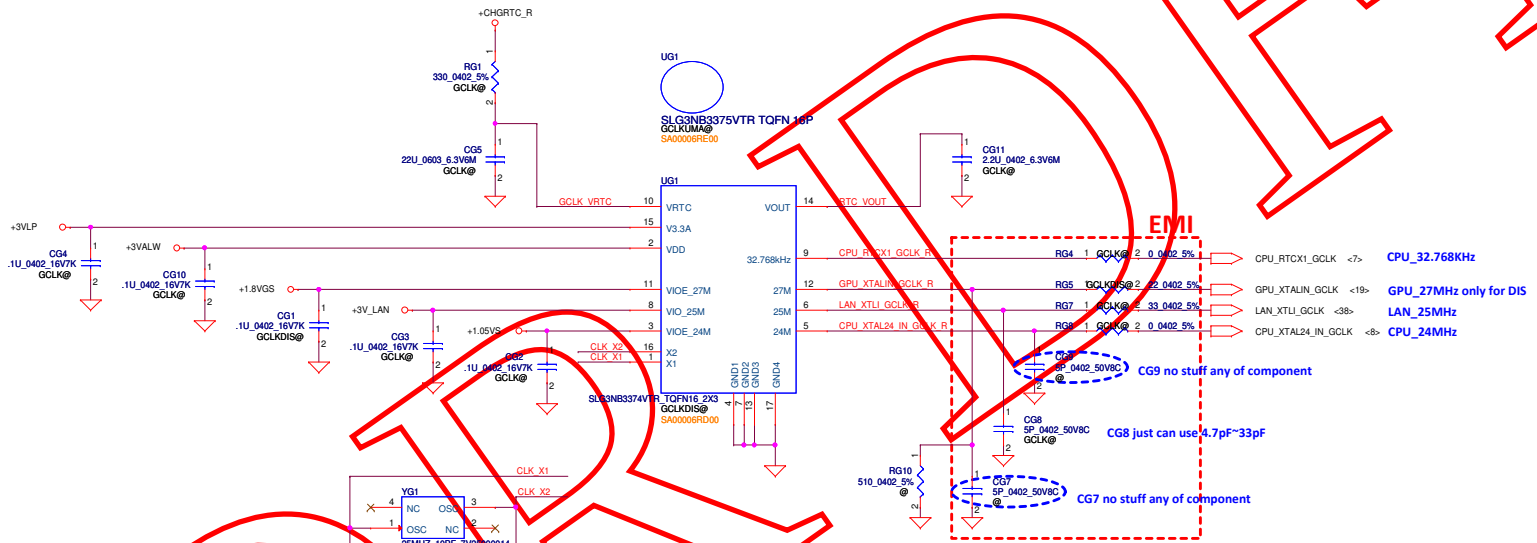
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: P24-CardRead/RTS5229

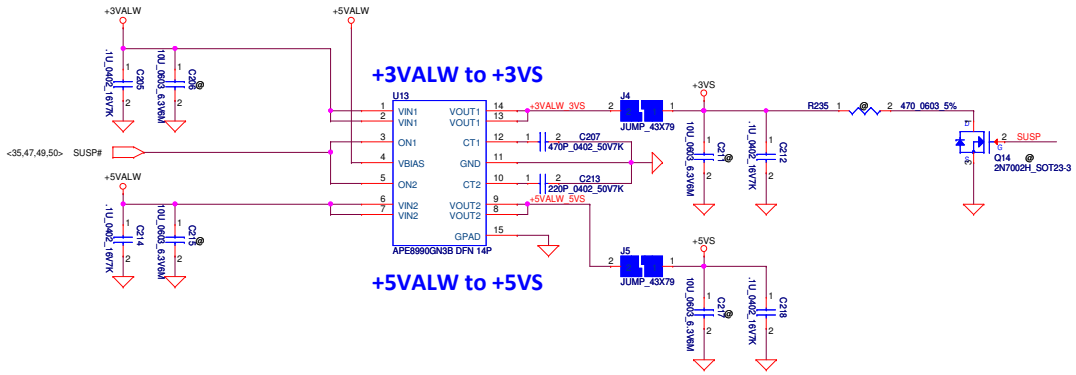
Size	Document Number	Rev
C	LA-B091P	1.0

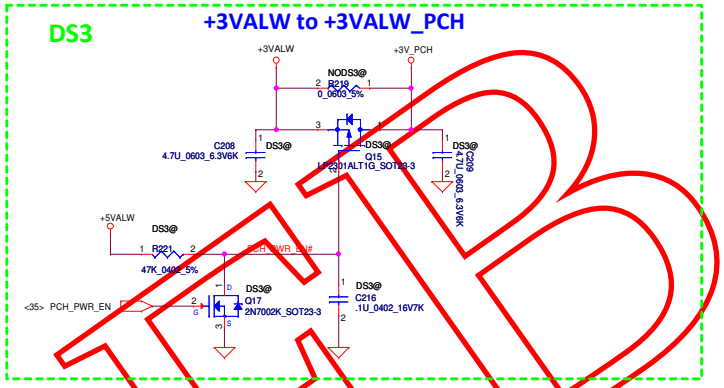
Date: Wednesday, February 12, 2014 Sheet 40 of 55

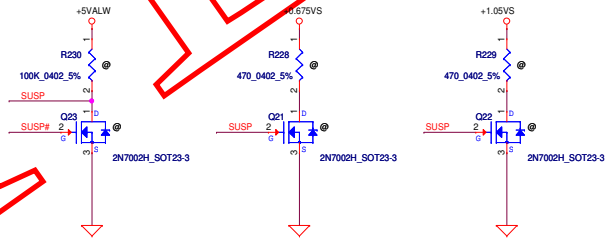


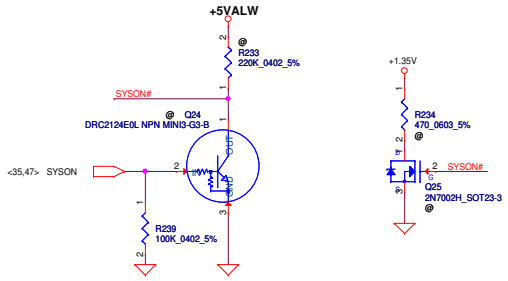
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title: GCLK			
Size	Document Number: LA-B091P		Rev: 1.0
Date: Wednesday, February 12, 2014	Sheet 41 of 55		

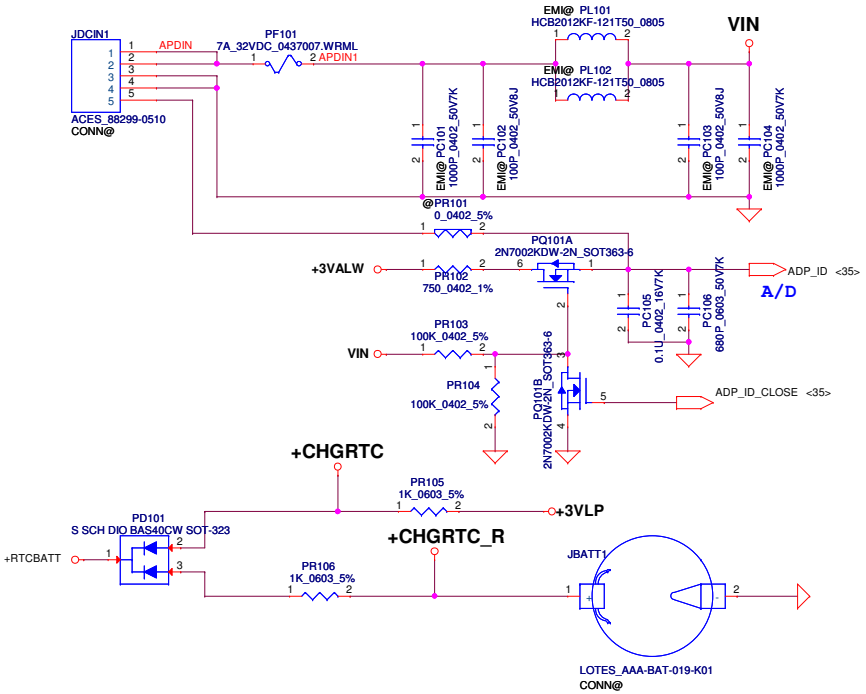








Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	DC Interface		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 42 of 55		



RTC Battery

ADP_ID

AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

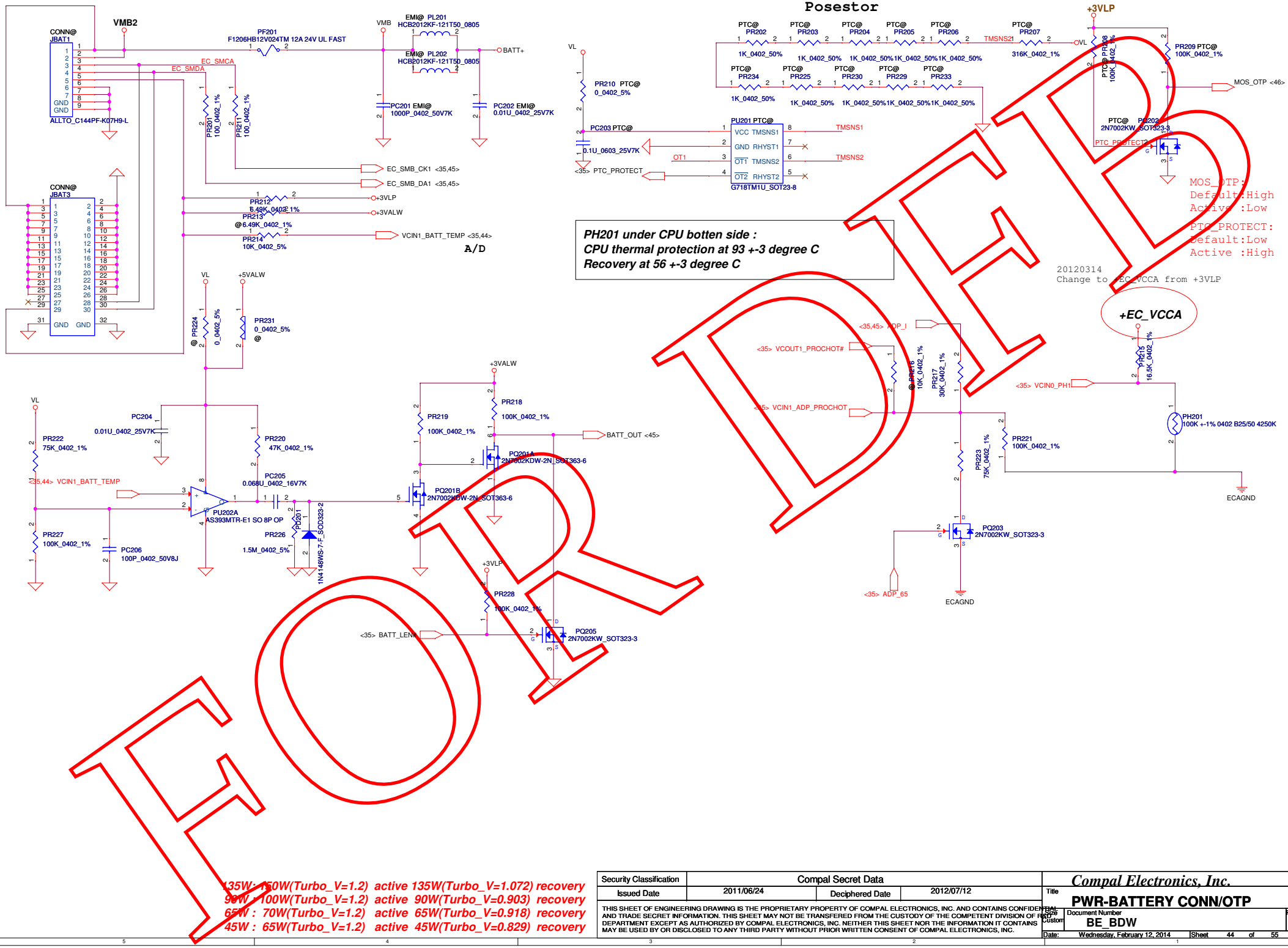
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PWR DCIN / RTC Battery

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 43 of 55



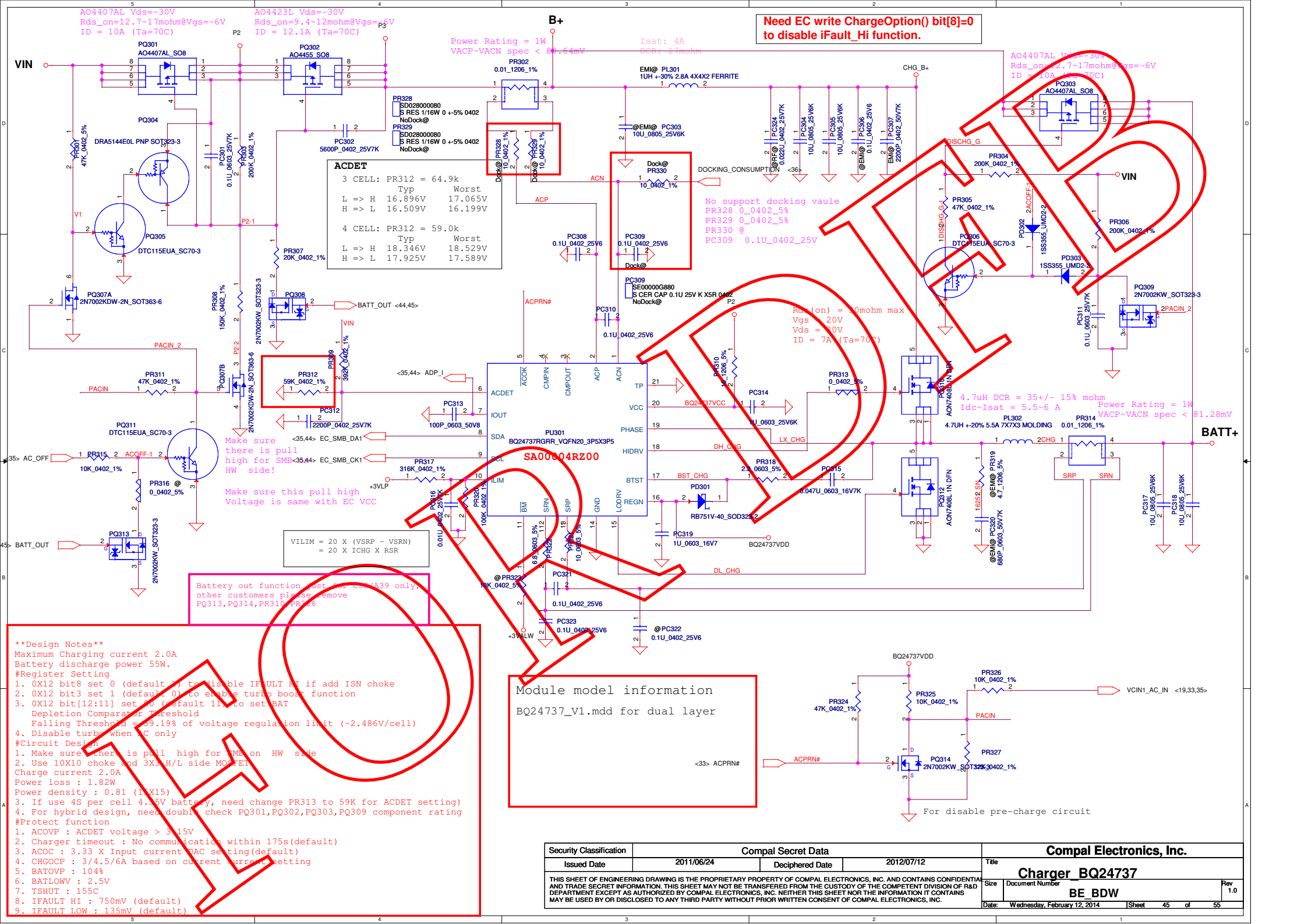
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 44 of 55


AO4407AL Vds=-30V
Rds_on=12.7~17mohm@Vgs=-6V
ID = 10A (Ta=70C)
AO4423L Vds=-30V
Rds_on=9.4~12mohm@Vgs=-6V
ID = 12.1A (Ta=70C)
Need EC write ChargeOption() bit[8]=0 to disable iFault_Hi function.
B+
VIN
BATT+
CHG_B+
Power Rating = 1W
VACP~VACN spec < 80.64mV
Isat: 4A
DCR: 27mohm
EMI@ PL301
1UH +-30% 2.8A 4X4X2 FERRITE
PR302 0.01_1206_1%
PQ301 AO4407AL_SO8
PQ302 AO4455_SO8
PQ303 AO4407AL_SO8
PQ304 DRA5144E0L PNP SOT323-3
PQ305 DTC115EUA_SC70-3
PQ306 DTC115EUA_SC70-3
PQ307A 2N7002KDW-2N_SOT363-6
PQ307B 2N7002KDW-2N_SOT363-6
PQ308 2N7002KW_SOT323-3
PQ309 2N7002KW_SOT323-3
PQ310 AON7408L_1N DFN
PQ311 DTC115EUA_SC70-3
PQ312 AON7408L_1N DFN
PQ313 2N7002KW_SOT323-3
PQ314 2N7002KW_SOT323-3
ACDET
3 CELL: PR312 = 64.9k
Typ Worst
L => H 16.896V 17.065V
H => L 16.509V 16.199V
4 CELL: PR312 = 59.0k
Typ Worst
L => H 18.346V 18.529V
H => L 17.925V 17.589V
No support docking vaule
PR328 0_0402_5%
PR329 0_0402_5%
PR330 @
PC309 0.1U_0402_25V
Rds(on) = 10mohm max
Vgs = 20V
Vds = 30V
ID = 7A (Ta=70C)
4.7uH DCR = 35+/- 15% mohm
Idc~Isat = 5.5~6 A
PL302 4.7UH +-20% 5.5A 7X7X3 MOLDING
PR314 0.01_1206_1%
Power Rating = 1W
VACP~VACN spec < 81.28mV
PU301 BQ24737RGRR_VQFN20_3P5X3P5
SA00004RZ00
ACDET
IOUT
SDA
SCL
ILIM
ACOK
CMPIN
CMPOUT
ACP
ACN
TP
VCC
PHASE
HIDRV
BTST
REGN
BM
SRN
SRP
GND
LODRV
VILIM = 20 X (VSRP - VSRN)
= 20 X ICHG X RSR
Make sure there is pull high for SMB HW side!
Make sure this pull high Voltage is same with EC VCC
Battery out function just for CQ8/A39 only, other customers please remove PQ313,PQ314,PR310,PR316
Module model information
BQ24737_V1.mdd for dual layer
For disable pre-charge circuit
Design Notes
Maximum Charging current 2.0A
Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
2. 0X12 bit3 set 1 (default 0) to enable turbo boost function
3. 0X12 bit[12:11] set 10 (default 11) to set BAT
Depletion Comparator Threshold
Falling Threshold = 99.19% of voltage regulation limit (~2.486V/cell)
4. Disable turbo when OTG only
#Circuit Design
1. Make sure there is pull high for SMB on HW side
2. Use 10X10 choke and 3X3 H/L side MOSFET
Charge current 2.0A
Power loss : 1.82W
Power density : 0.81 (10X15)
3. If use 4S per cell 4.35V battery, need change PR313 to 59K for ACDET setting)
4. For hybrid design, need double check PQ301,PQ302,PQ303,PQ309 component rating
#Protect function
1. ACOVP : ACDET voltage > 3.15V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 104%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 135mV (default)
Security Classification
Compal Secret Data
Issued Date
2011/06/24
Deciphered Date
2012/07/12
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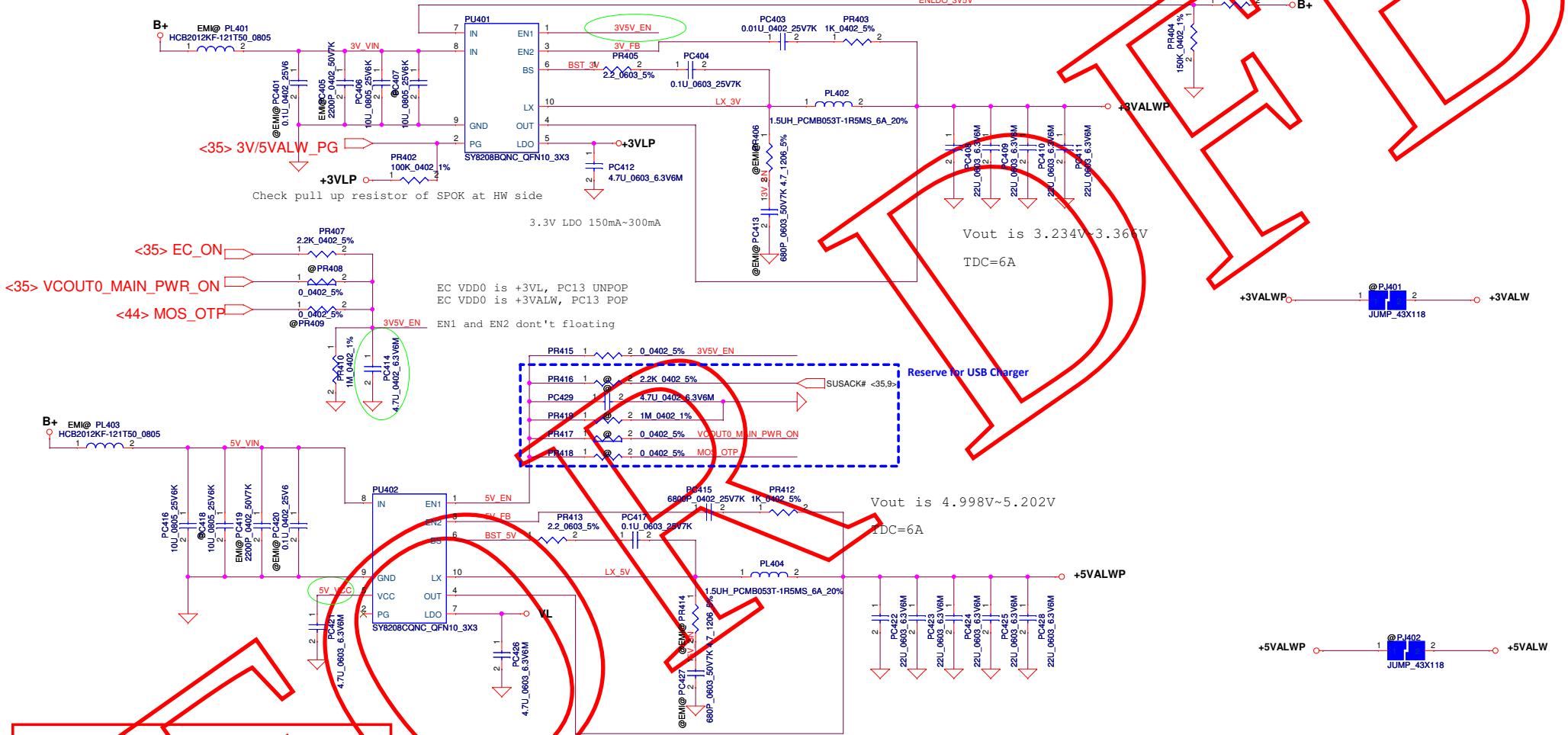
Compal Electronics, Inc.
Title
Charger_BQ24737
Size
Document Number
BE_BDW
Rev
1.0
Date: Wednesday, February 12, 2014
Sheet 45 of 55

Module model information

SY8208B_V2.mdd

EN1 and EN2 dont't floating

Change 3V5V_EN to 3VALW_EN



Module model information

SY8208C_V2.mdd

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number: BE_BDW | Rev: 1.0

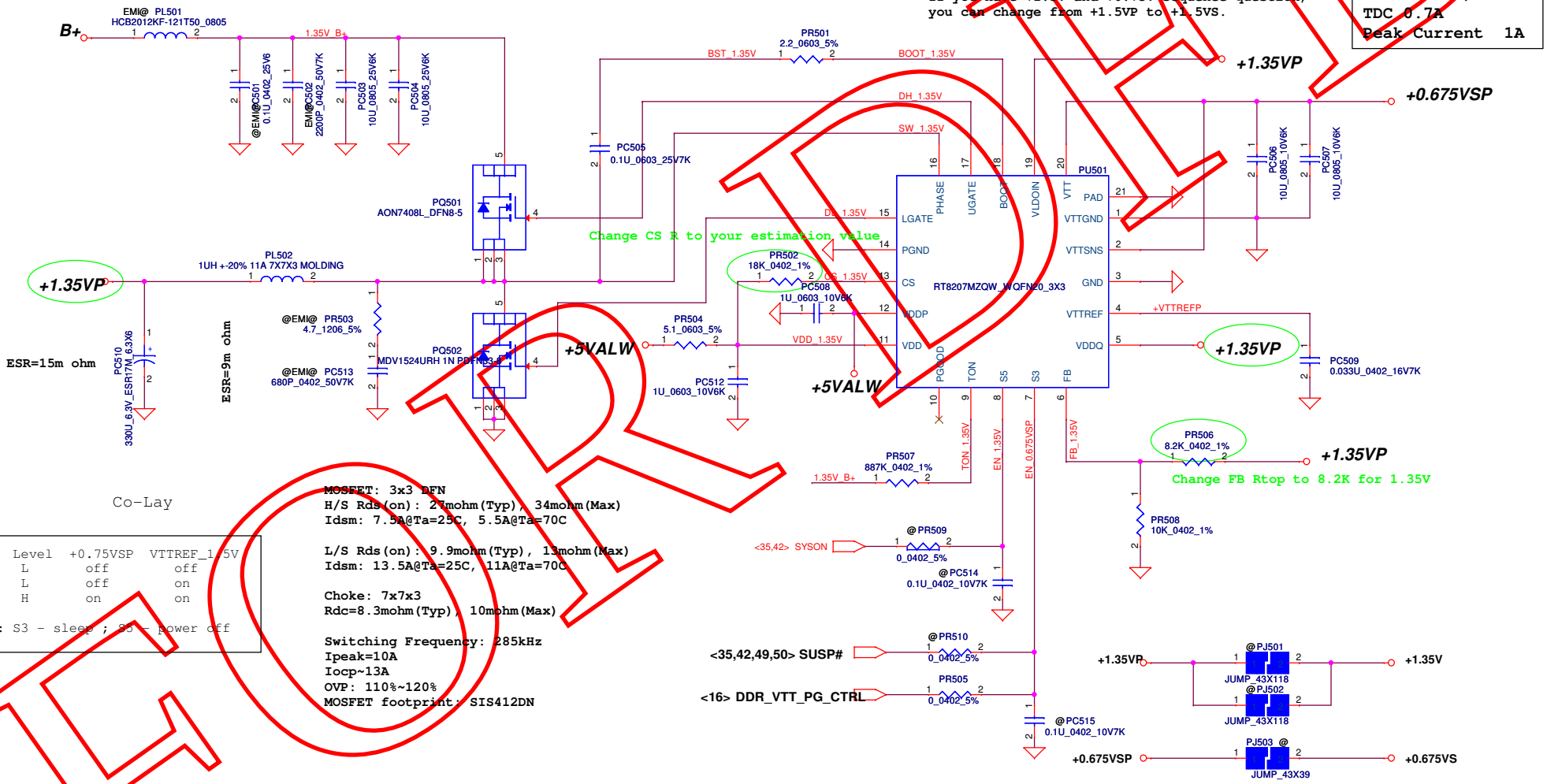
Date: Wednesday, February 12, 2014 | Sheet 46 of 55

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



Co-Lay

Mode	Level	+0.75VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
MOSFET footprint: SIS412DN

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

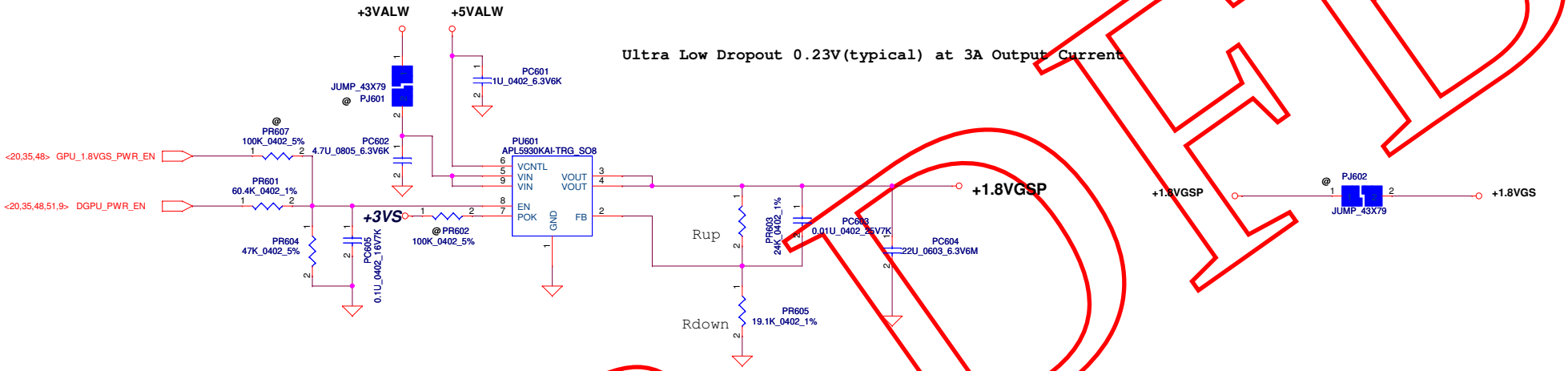
Title: RT8207M

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 47 of 55

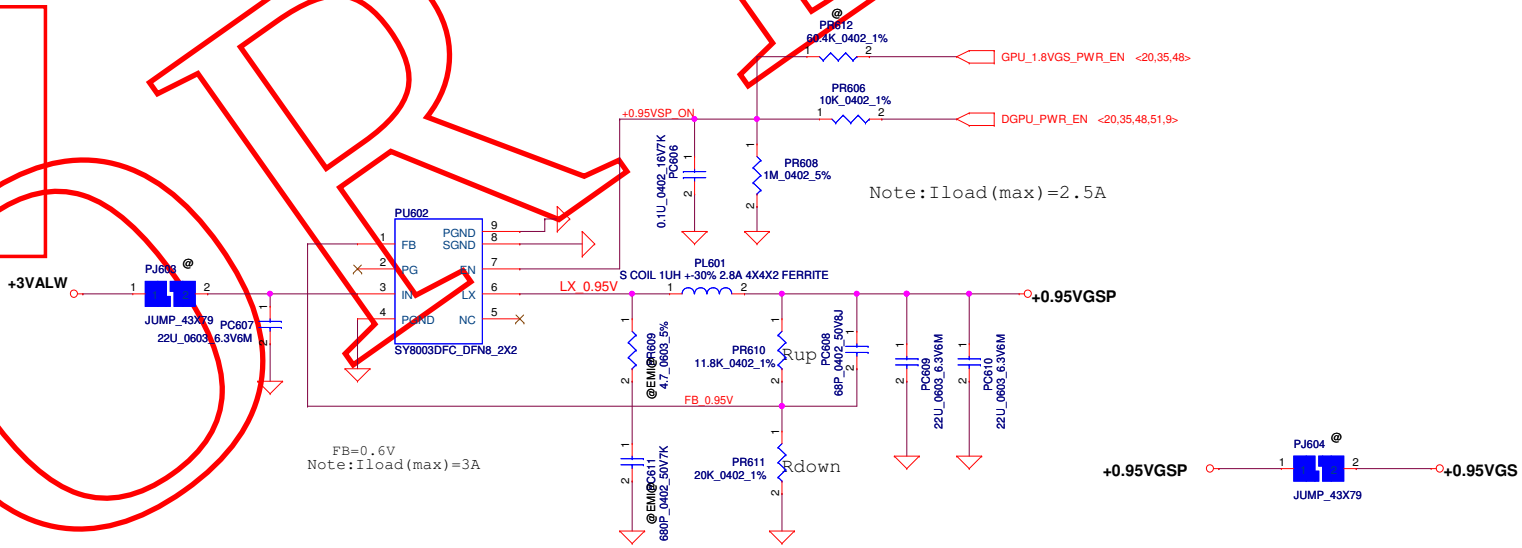
Module model information

APL5930_V1.mdd



Module model information

SY8003_V1.mdd



Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

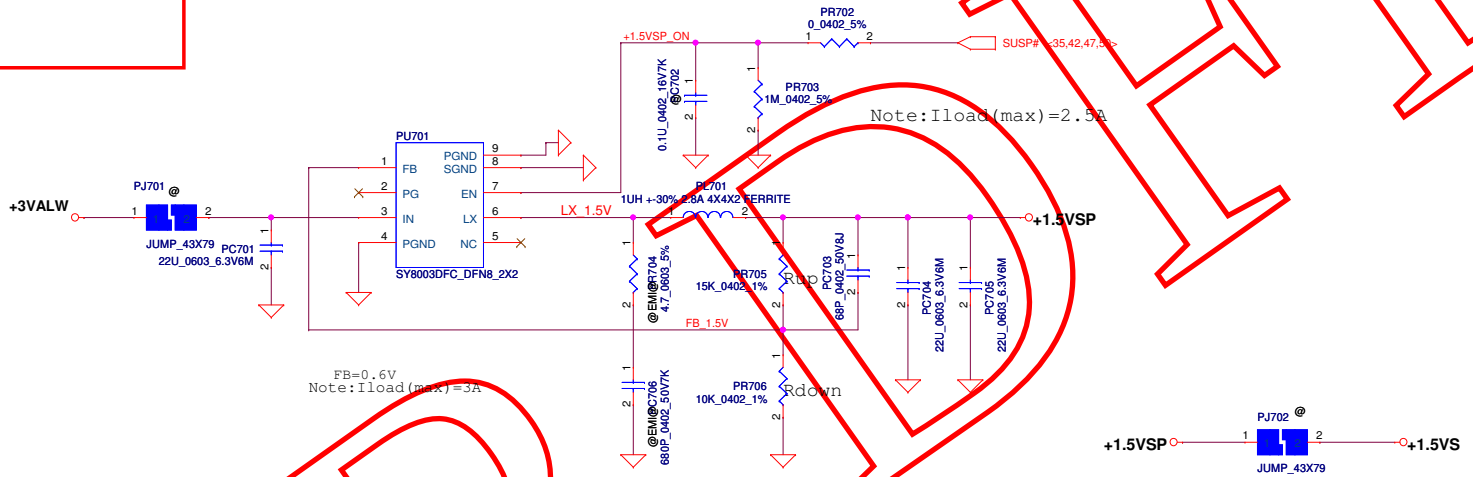
Title: +1.8VGS-+0.95VVGS

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 48 of 55

Module model information

SY8003_V1.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: +1.5VS

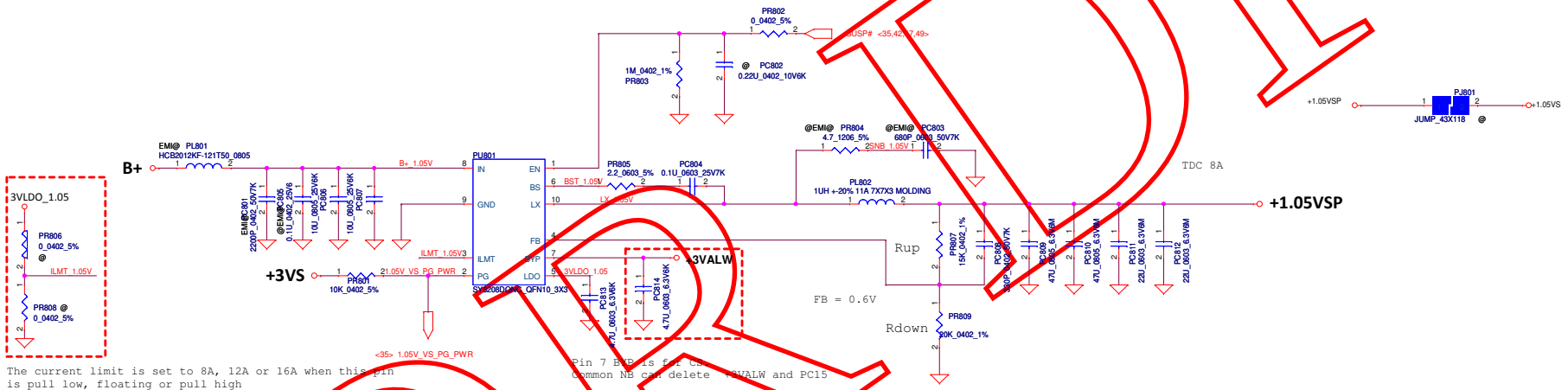
Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 49 of 55

Module model information

SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS
Common NB can delete +3VALW and PC15

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

Vout=1.05V

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: +1.05VS

Size	Document Number	Rev
C	BE_BDW	1.0

Date: Wednesday, February 12, 2014 Sheet 50 of 55

Module model information

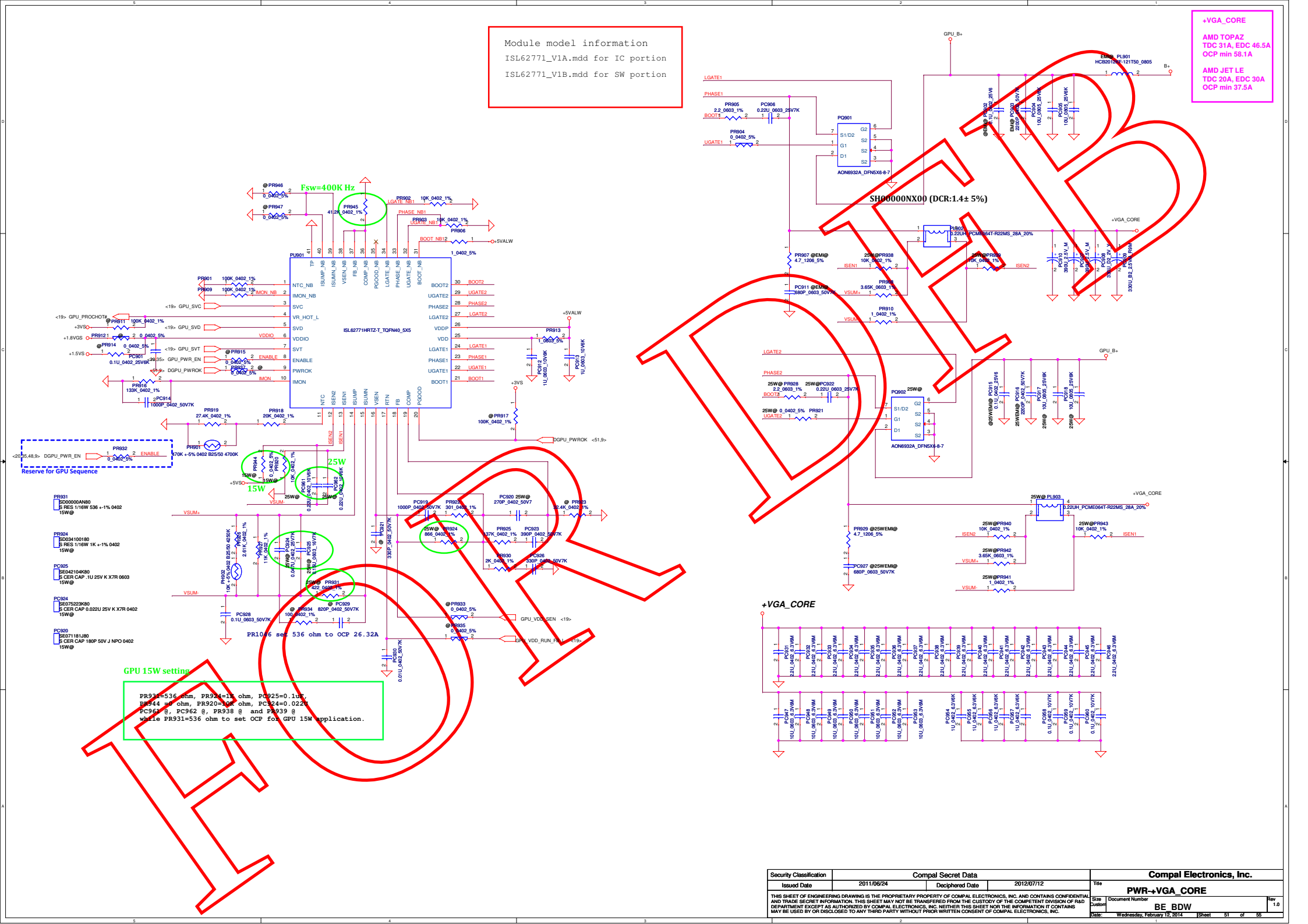
ISL62771_V1A.mdd for IC portion

ISL62771_V1B.mdd for SW portion

+VGA_CORE

AMD TOPAZ
TDC 31A, EDC 46.5A
OCP min 58.1A

AMD JET LE
TDC 20A, EDC 30A
OCP min 37.5A



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/07/12	Title: PWR-+VGA_CORE
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Module model information:
ISL95813 (for 15W & 28W CPU)

Base on BDW PDDG Rev_0_73		
Location	15W TDC 14A MAX 32A OCP 39A Loadline=-2.0mv/A	Note
PR1120	499 Ohm	OCP
PR537	1.27kOhm	Droop
PC528	0.022uF	RC Match
PR507	90.9kOhm	PROG1
PR703	93.1kOhm	IMON
PC518	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<3.4mohm@Vgs=10V
<3.9mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.12UH (Size:7*7*3)
Rdc=0.62mohm +-5%
Heat Rating Current=41.5A
Saturation Current=41A

+1.05VS
Follow intel guideline
PR1102 130_0402_1%
PR1103 54.9_0402_1%
PC1102 1U_0402_6.3V6K

Note:
VR_SVID_ALRT# Pull high on HW side

<12> VR_SVID_DAT
<12> VR_SVID_ALRT#
<12> VR_SVID_CLK
<12> VR_ON
<12> VGATE
<35> IMON_CPU
<35> VR_HOT#

PR1104 169K_0402_1%
Note:
PR1104=169K
=>Icc(max)=33A
fsw=700KHz

PU1101
ISL95813HRZ-T_QFN20_3X4
PAD, SCLK, ALERT#, SDA, PRGM1, VR_ON, PGOOD, IMON, VR_HOT#, NTC, COMP, FB, RTN, ISUMN, ISUMP, LGATE, PHASE, UGATE, BOOT, VCC, PRGM2

@PR1101 1.91K_0402_1%
PR1122 1.5K_0402_1%
PC1101 1000P_0402_50V7K
PR1106 97.6K_0402_1%

Note:
VR_HOT# Pull high on HW side

PH1101 470K +-5% 0402 B25/50 4700K
PR1110 3.83K_0402_1%
PR1111 27.4K_0402_1%
PC1109 47P_0402_50V8J

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

PR1105 0_0603_5%
PR1108 2.2_0603_5%
PC1108 0.22U_0603_16V7K
PC1111 0.1U_0402_25V6
+5VS

PR1112 124K_0402_1%
Note:
PR1112=124K
=>Slew rate=53mV/us
Vboot = 1.7V

PR1113 909_0402_1%
PC1113 680P_0402_25V7K
@PC1112 33P_0402_50V8J

PR1114 2K_0402_1%
PC1114 330P_0402_50V7K
PR1115 10_0402_1%
PC1115 390P_0402_50V7K
PR1116 1.27K_0402_1%
Droop

PR1117 4.99M_0402_1%

RC Match
PC1116 0.033U_0402_25V7K
PC1117 0.1U_0402_16V4Z
PR1119 11K_0402_1%
PR1118 4.42K_0402_1%
PH1102 10K +-5% 0402 B25/50 4250K

<12> VCCSENSE
<12,14> VSSSENSE

@PC1118 330P_0402_50V7K
@PC1119 0.082U_0402_16V7K
PC1120 0.01U_0402_50V7K

OCP Setting
PR1120 287_0402_1%

@PC1121 4700P_0402_25V7K
@PR1121 1.5K_0402_1%

Local sense put on HW site

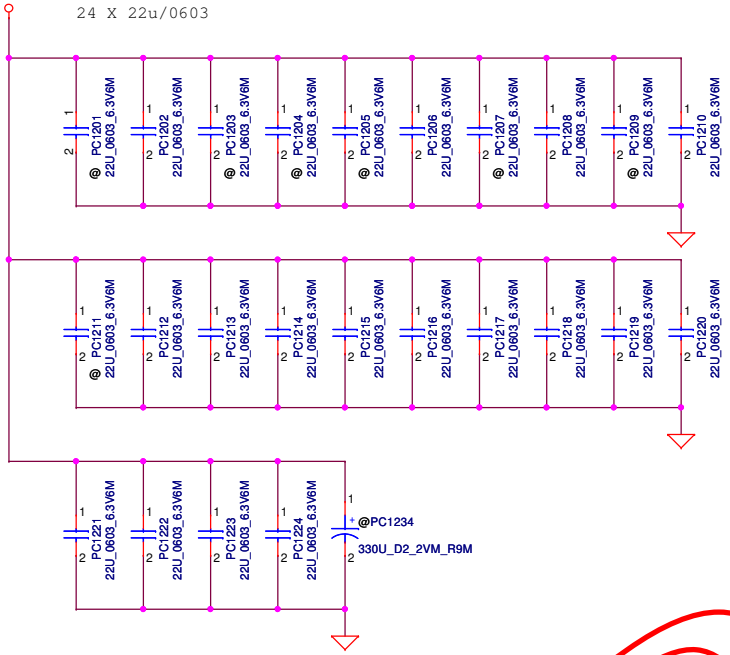
CPU_B+
PC1103 10U_0805_25V6K
PC1104 10U_0805_25V6K
EMI@PC1105 10U_0402_6.3V7K
EMI@PC1106 220P_0402_50V7K
@RC@ PC1107 0.022U_0402_25V7K
PC1123 330_25V_M
PC1122 680_25V_M
EMI@ PL1103 HCB2012KF-121T50_0805
@EMI@ PL1104 HCB2012KF-121T50_0805
B+

PQ1101 MDV1525URH_PDRN33-8-5
PQ1103 MDU1511RH_POWERDFN56-8-5
PQ1102 MDU1511RH_POWERDFN56-8-5

PL1102 .15UH 20% PCME064T-R15MS0R667 36A
+CPU_CORE
@EMI@PR1107 4.7_1206_5%
@EMI@PC1110 680P_0603_50V7K
PR1109 3.65K_0603_1%

FAE

+CPU_CORE



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: **PWR-PROCESSOR DECOUPLING**

Size	Document Number	Rev
Custom	BE_BDW	1.0

Date: Wednesday, February 12, 2014 Sheet 53 of 55

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 54 of 55

ZIWB2/ZIWB3/ZIWE1 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			EVT TO DVT
1	P.36	Modify DP_SEL schematic	Because the first design is wrong.
2	P.34	Delete D28	It already reserve in sub BD
3	P.36	Modify HPD schematic	Because the first design is wrong.
4	P.36	Modify DP AUX schematic	Cap already reserve in sub BD
5	P.20	Reserve +1.05VS to +0.95VGS	AMD's suggestion
6	P.33	Add D26 for ESD	
7	P.42	Add RV198, RV199	AMD's suggestion
8	P.22~24	Add GPU Termination Resistance	AMD's suggestion
			DVT TO PVT
1	P.35	change U11.111 power rail to +3VLP	It only use +3VLP
2	P.33	un-pop R294, pop R295.	B series's LED need to follow E series
3	P.10	Add R247, R248	For BIOS Stap Pin
4	P.20	Add RV60, delete RV36	for GPU Sequence
5	P.20	Add RV61, delete RV240	for GPU Sequence
6	P.37	Change DP Switch IC solution	For HDMI audio issue
7	P.35	Add C197 for ESD	
8	P.33	Add C198 for ESD	
9	P.30	Add C199 for ESD	
			PVT TO PRE-MP
1	P.33	Reserve R298, R299 for DC-in LED control	To avoid LED shimmer
2	P.38	Change DL1 and DL2 footprint for ESD	

Compal Electronics, Inc.		
Title: HW-PIR1		
Size: Custom	Document Number: LA-B091P	Rev: 1.0
Date: Wednesday, February 12, 2014	Sheet 55 of 55	