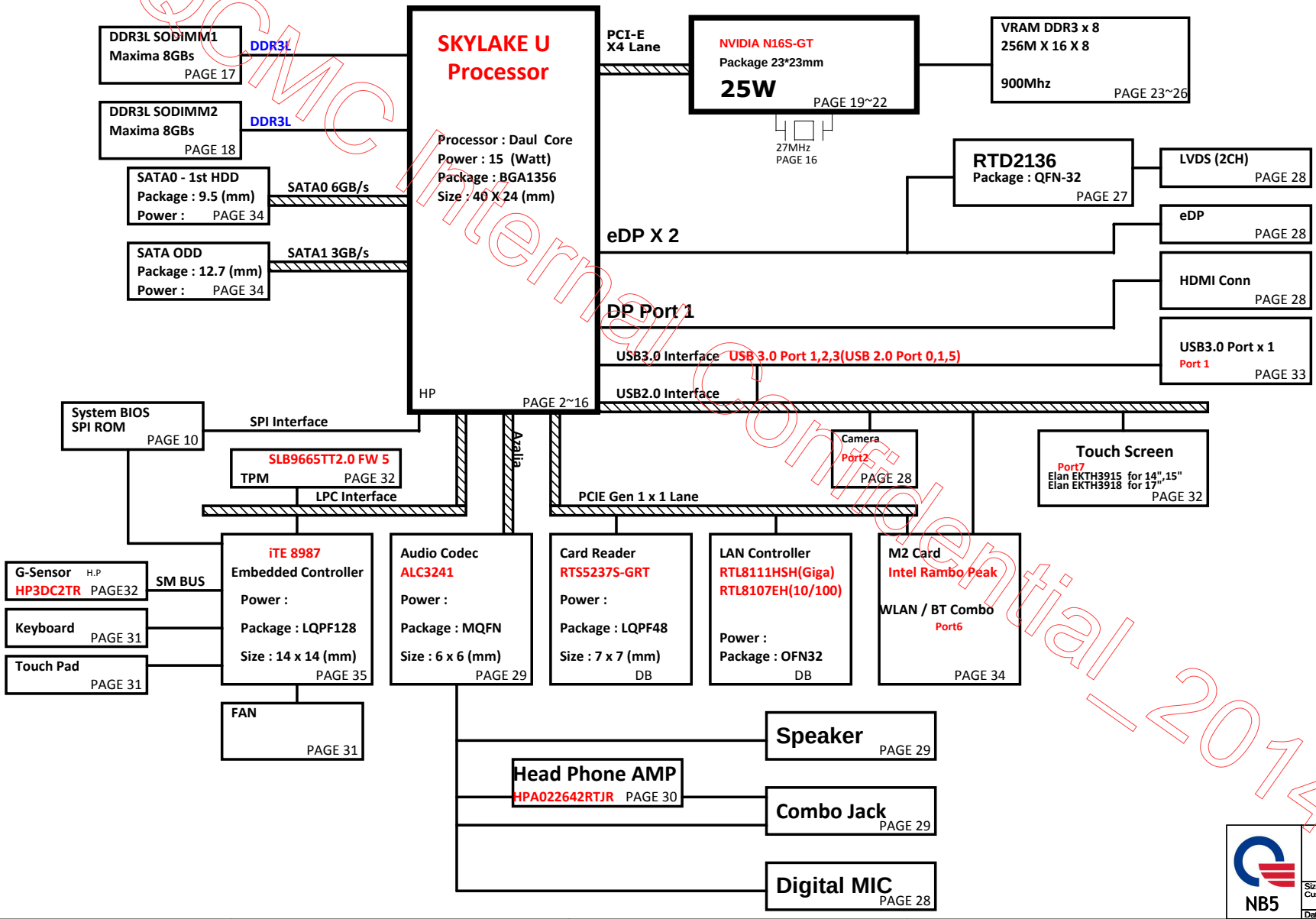
DIS (14" / 15" / 17") Chocolate
Intel SKYLAKE ULT Platform Block Diagram

PCB 10L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : SGND1
LAYER 7 : IN3
LAYER 8 : IN4
LAYER 9 : SGND2
LAYER 10 : BOT



NB5

PROJECT : X1B-10L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram for ICT Review	1A
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HDMI

U20A — SKL_ULT

28	IN_D2#	IN_D2#	E55	DDI1_TXN[0]	
28	IN_D2	IN_D2	F55	DDI1_TXP[0]	
28	IN_D1#	IN_D1#	E58	DDI1_TXN[1]	
28	IN_D1	IN_D1	F58	DDI1_TXP[1]	
28	IN_D0#	IN_D0#	F53	DDI1_TXN[2]	
28	IN_D0	IN_D0	G53	DDI1_TXP[2]	
28	IN_CLK#	IN_CLK#	F56	DDI1_TXN[3]	
28	IN_CLK	IN_CLK	G56	DDI1_TXP[3]	

DDI

C50	DDI2_TXN[0]	
D50	DDI2_TXP[0]	
C52	DDI2_TXN[1]	
D52	DDI2_TXP[1]	
A50	DDI2_TXN[2]	
B50	DDI2_TXP[2]	
D51	DDI2_TXN[3]	
C51	DDI2_TXP[3]	

EDP

EDP_TXN[0]	C47	INT_EDP_TXN0	INT_EDP_TXN0	27	
EDP_TXP[0]	C46	INT_EDP_TXP0	INT_EDP_TXP0	27	
EDP_TXN[1]	D46	INT_EDP_TXN1	INT_EDP_TXN1	27	
EDP_TXP[1]	C45	INT_EDP_TXP1	INT_EDP_TXP1	27	
EDP_TXN[2]	A45				
EDP_TXP[2]	B45				
EDP_TXN[3]	A47				
EDP_TXP[3]	B47				
EDP_AUXN	E45	INT_EDP_AUXN	INT_EDP_AUXN	27	
EDP_AUXP	F45	INT_EDP_AUXP	INT_EDP_AUXP	27	
EDP_DISP_UTIL	B52	EDP_DISP_UTIL	TP52		

DISPLAY SIDEBANDS

28	SDVO_CLK	L13	GPP_E18/DDPB_CTRLCLK	
28	SDVO_DATA	L12	GPP_E19/DDPB_CTRLDATA	
TP113	DDPC_CTRLDATA	N7	GPP_E20/DDPC_CTRLCLK	
		N8	GPP_E21/DDPC_CTRLDATA	
TP114	DDPD_CTRLDATA	N11	GPP_E22/DDPD_CTRLCLK	
		N12	GPP_E23/DDPD_CTRLDATA	
+VCCIO	R100 24.9/F_4 EDP_RCOMP	E52	EDP_RCOMP	

		DDI1_AUXN	G50		
		DDI1_AUXP	F50		
		DDI2_AUXN	F48		
		DDI2_AUXP	G48		
		DDI3_AUXN	G46		
		DDI3_AUXP	F46		
GPP_E13/DDPB_HPD0	L9	HDMI_HPD_CON	HDMI_HPD_CON	28	
GPP_E14/DDPC_HPD1	L7				
GPP_E15/DDPD_HPD2	L5				
GPP_E16/DDPE_HPD3	N9				
GPP_E17/EDP_HPD	L10	ULT_EDP_HPD	ULT_EDP_HPD	27,28	
EDP_BKLTEN	R12	PCH_LVDS_BLON	PCH_LVDS_BLON	28	
EDP_BKLTCTL	R11	PCH_DPST_PWM	PCH_DPST_PWM	27	
EDP_VDDEN	U13	PCH_DISP_ON	PCH_DISP_ON	28	

*SKL_ULT
REV = 1

1 OF 20

DDPB_CTRLDATA/ GPP_E19
Display Port B Detected
This signal has a weak internal pull-down.
0 = Port B is not detected.
1 = Port B is detected.

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.

DB Del R98, R110

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V — R93 *10K/F_4 — ULT_EDP_HPD — R96 100K_4

+3V 4,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44
+1.0V 4,6,16,32,35,40
+VCCIO 6,16,40
+VCCSTPLL 4,5,6,9,40,41

Close to EC

+VCCSTPLL — PM_THRMTRIP# R420 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

U20D — SKL_ULT

+VCCSTPLL

	R421 *49.9/F_4	CATERR#	D63	CATERR#	
35	EC_PECI	EC_PECI	A54	PECI	
35,36,41	H_PROCHOT#	R395 499/F_4 PROCHOT#	C65	PROCHOT#	
35	PM_THRMTRIP#	PM_THRMTRIP#	C63	THERMTRIP#	
			A65	SKTOCC#	

CPU MISC

16	XDP_BPM0	C55	BPM#[0]	
16	XDP_BPM1	D55	BPM#[1]	
		B54	BPM#[2]	
		C56	BPM#[3]	
33	3D_FW_GPIO R608 *0_4	FW_GPIO_R	A6	GPP_E3/CPU_GP0
TP40		CPU_GP1	A7	GPP_E7/CPU_GP1
TP105		CPU_GP2	BA5	GPP_B3/CPU_GP2
TP103		CPU_GP3	AY5	GPP_B4/CPU_GP3

SI Add

R206	49.9/F_4	PROC_POPIRCOMP	AT16
R201	49.9/F_4	PCH_OPI_RCOMP	AU16
R114	49.9/F_4	EDRAM_OPIO_RCOMP	H66
R106	49.9/F_4	EOPIO_RCOMP	H65

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

JTAG

PROC_TCK	B61	XDP_TCK0	XDP_TCK0	16	
PROC_TDI	D60	XDP_TDI_CPU	XDP_TDI_CPU	16	
PROC_TDO	A61	XDP_TDO_CPU	XDP_TDO_CPU	16	
PROC_TMS	C60	XDP_TMS_CPU	XDP_TMS_CPU	16	
PROC_TRST#	B59	XDP_TRST#_CPU	XDP_TRST#_CPU	16	
PCH_JTAG_TCK	B56	JTAG_TCK_PCH	JTAG_TCK_PCH	16	
PCH_JTAG_TDI	D59	JTAG_TDI_PCH	JTAG_TDI_PCH	16	
PCH_JTAG_TDO	A56	JTAG_TDO_PCH	JTAG_TDO_PCH	16	
PCH_JTAG_TMS	C59	JTAG_TMS_PCH	JTAG_TMS_PCH	16	
PCH_TRST#	C61	XDP_TRST#_CPU			
JTAGX	A59	JTAGX_PCH	JTAGX_PCH	16	

*SKL_ULT
REV = 1

4 OF 20

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R408 *51_4
XDP_TDI_CPU R407 *51_4
XDP_TDO_CPU R393 *51_4

+1.0V — R78 *0_4/S

R403	*51_4	JTAGX_PCH
R404	51_4	JTAG_TMS_PCH
R418	51_4	JTAG_TDI_PCH
R419	51_4	JTAG_TDO_PCH
R405	51_4	JTAG_TCK_PCH

Close to Chipset

+1.0V — H_PROCHOT# R49 1K_4

XDP_TCK0 R417 51_4
XDP_TRST#_CPU R399 51_4

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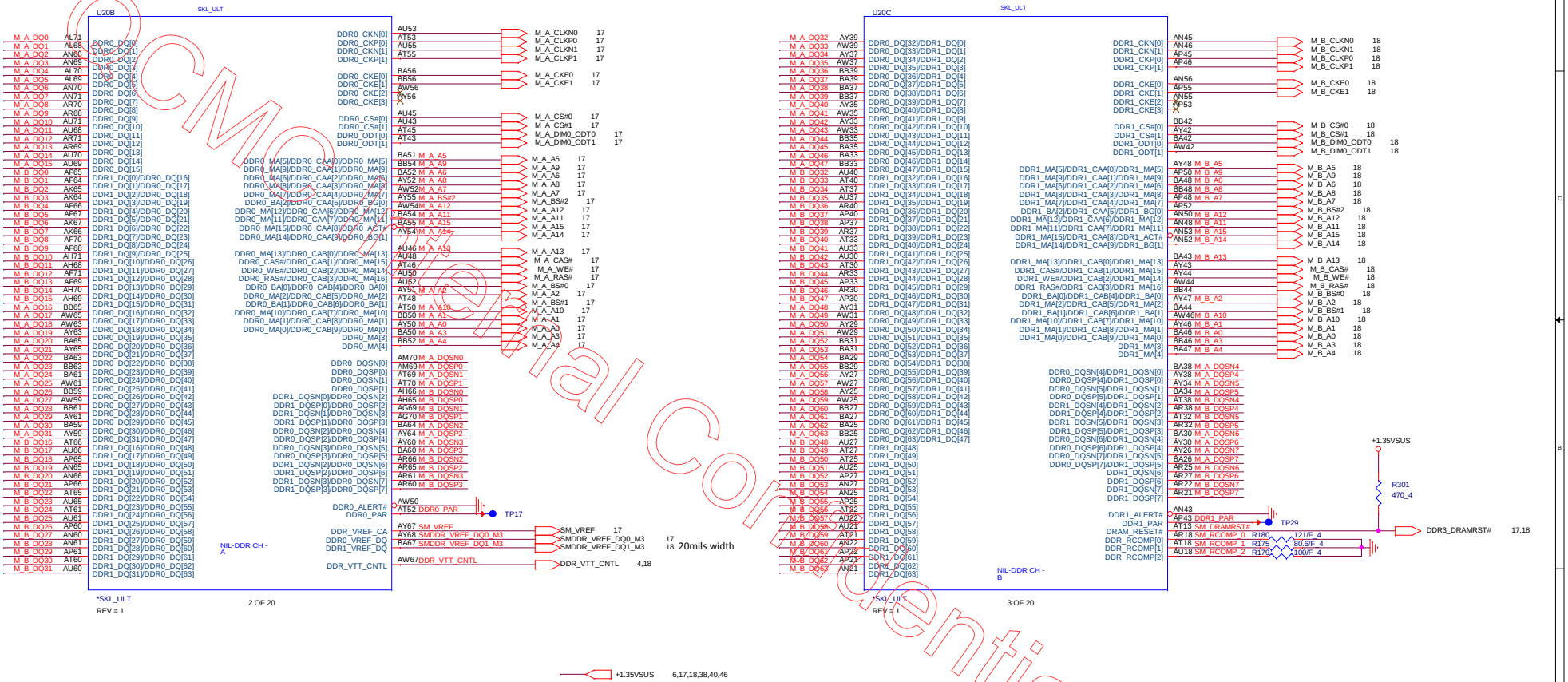
17 M_A_DQSN[7:0]
17 M_A_DQSP[7:0]
18 M_B_DQSN[7:0]
18 M_B_DQSP[7:0]
17 M_A_DQ[63:0]
18 M_B_DQ[63:0]

SkyLake ULT Processor (DDR3L)



NB5	PROJECT : X1B-10L Quanta Computer Inc.	
Size: Custom	Document Number: SKYPAKE 3/20(DDR3-A I/F)	Rev: 1A
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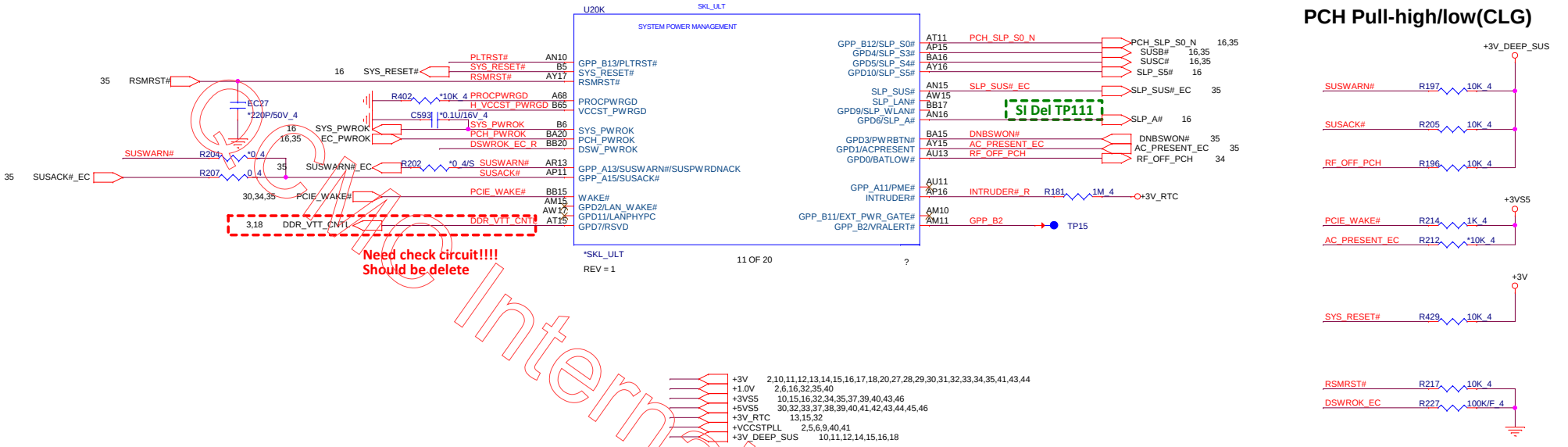
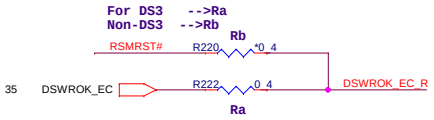


PCH Pull-high/low(CLG)

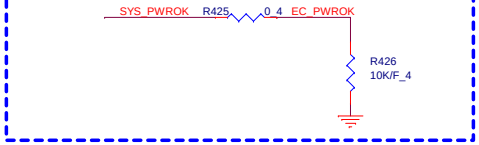
For DS3 Sequence



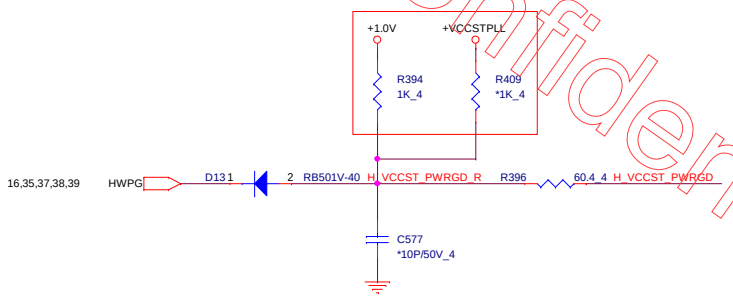
PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns

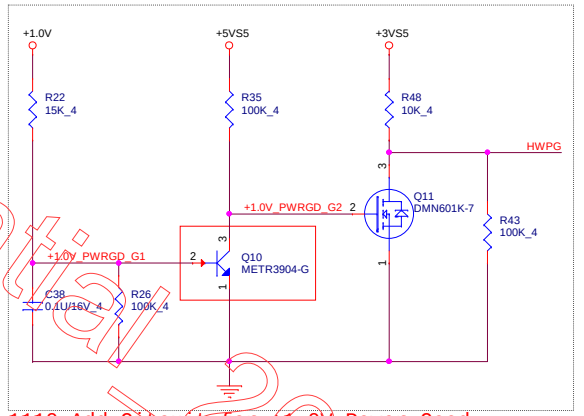
System PWR_OK(CLG)



1216 Change R409 and R394 from +VCCSTPLL or +1.0V co-layout.



R10479 close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



1110 Add Circuit for +1.0V Power Good

NB5	PROJECT : X1B-10L Quanta Computer Inc.	
Size: Custom	Document Number: SKYPAKE 5/20(Power Manger)	Rev: 1A
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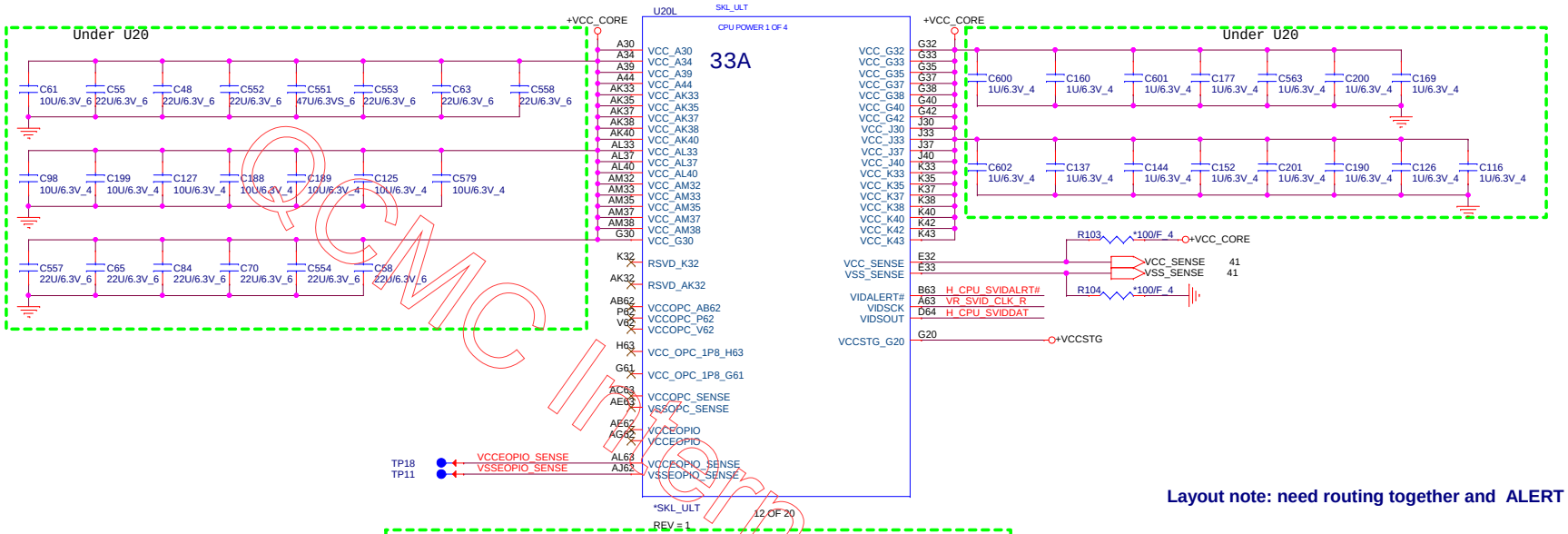
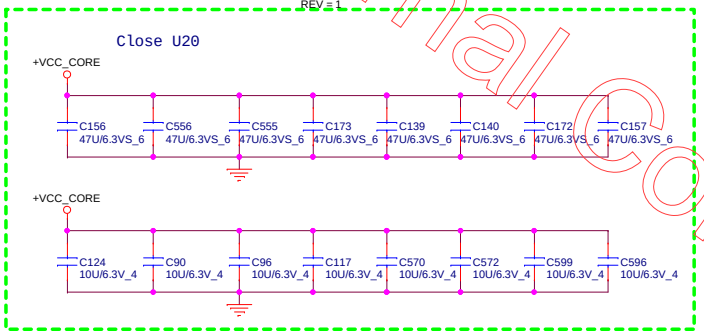
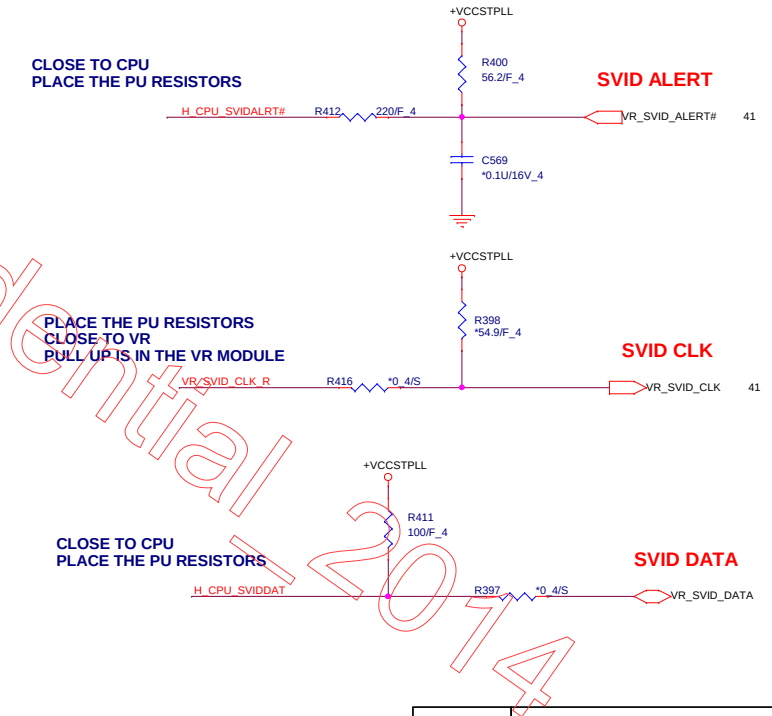


100- ±1% pull-up to VCC near processor.



Layout note: need routing together and ALERT need between CLK and DATA.



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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Quanta Computer Inc.

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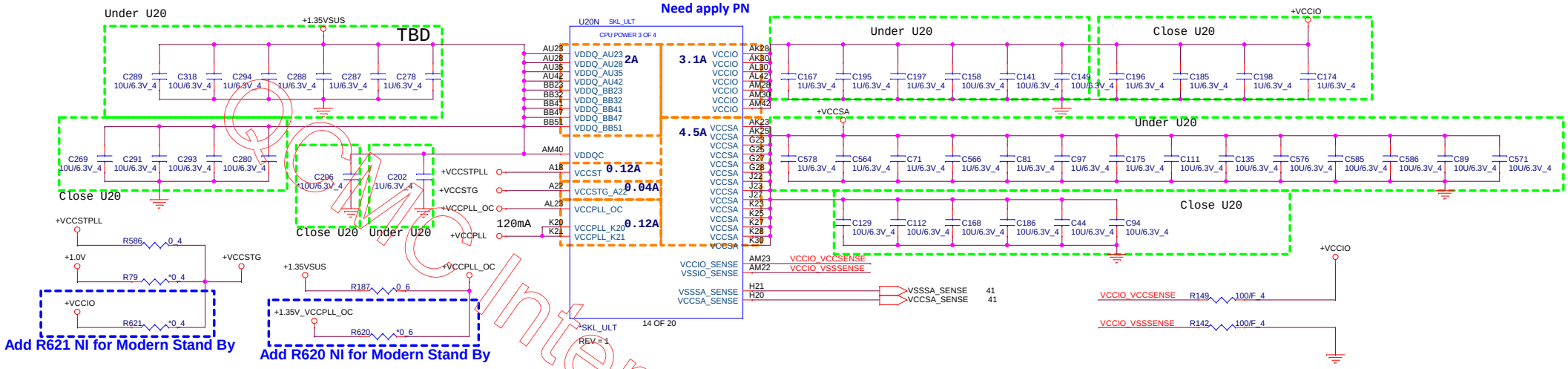
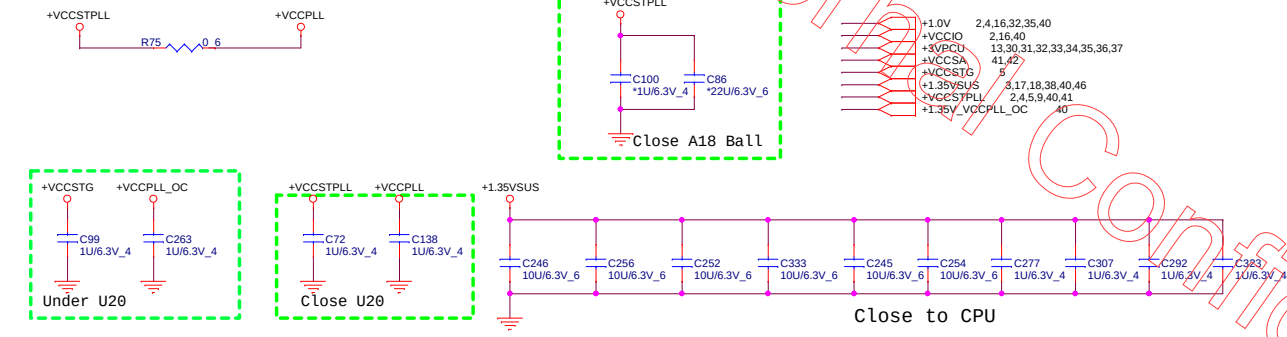
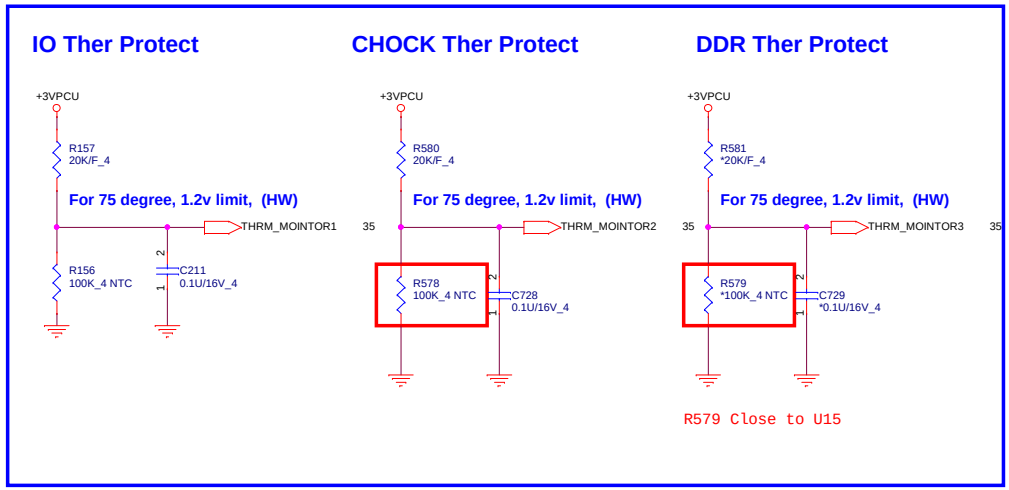




Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	SKYPAKE 7/20 (POWER-2)	1A
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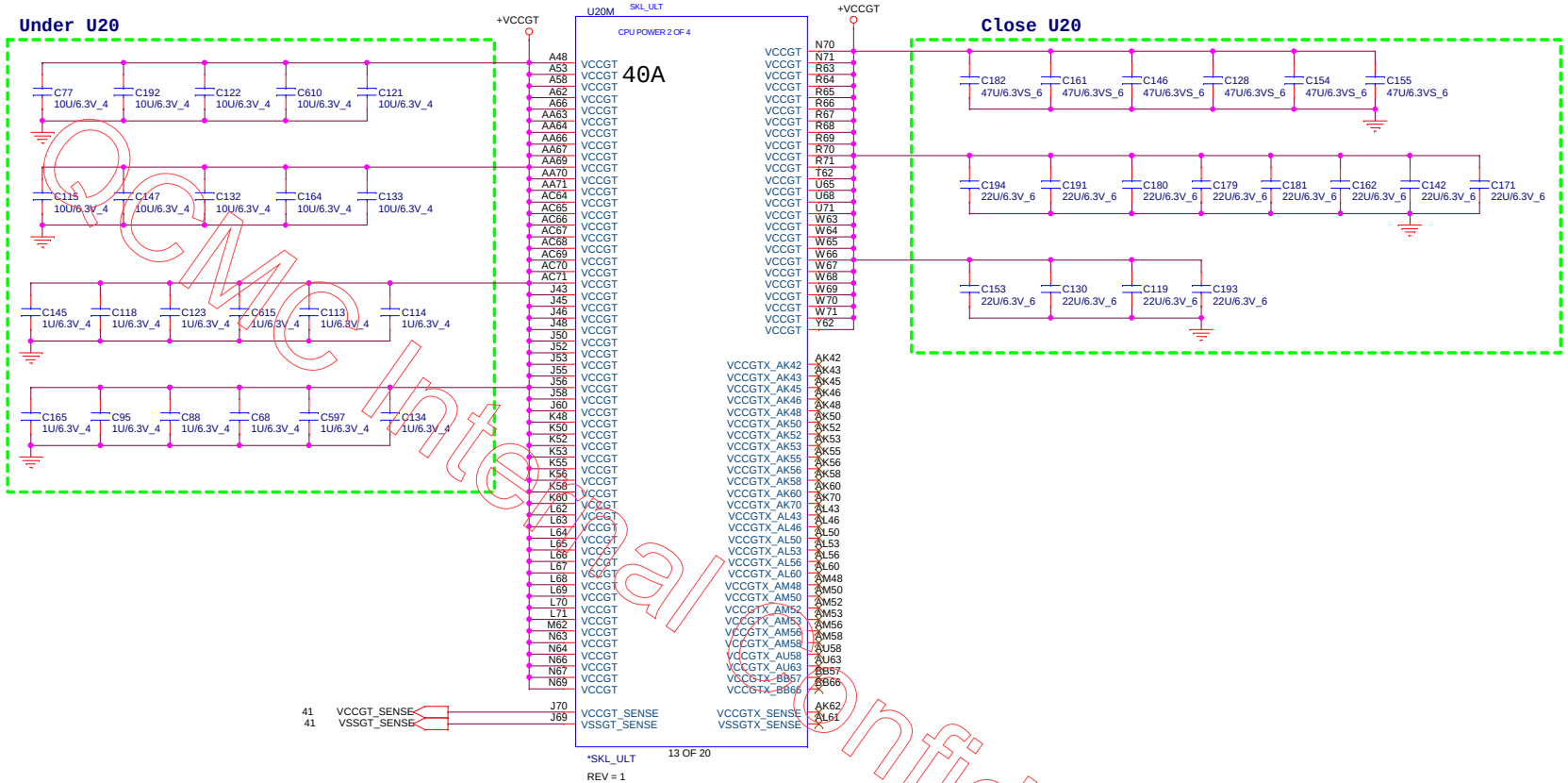

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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Quanta Computer Inc.

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Custom	SKYPAKE 8/20 (POWER-3)	1A

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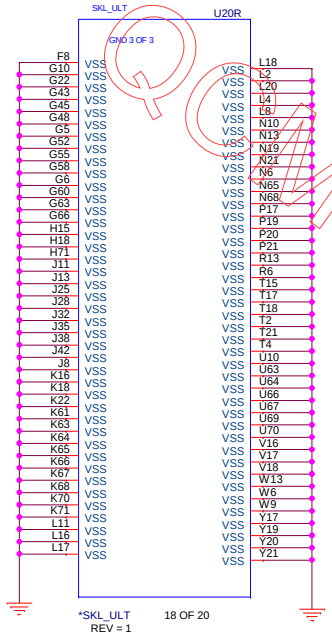

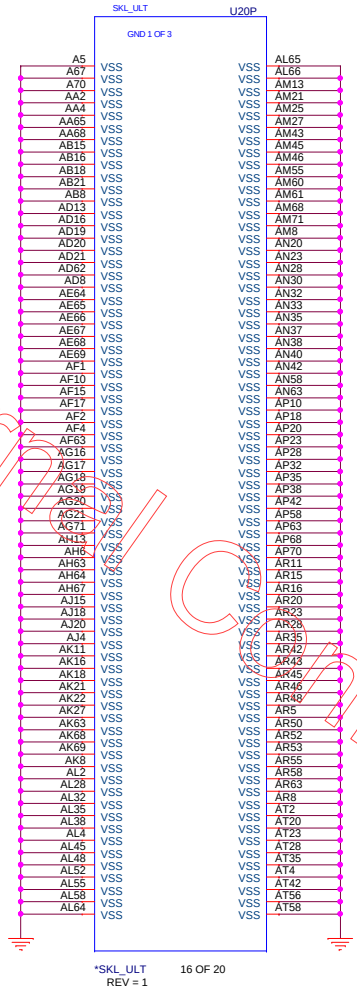

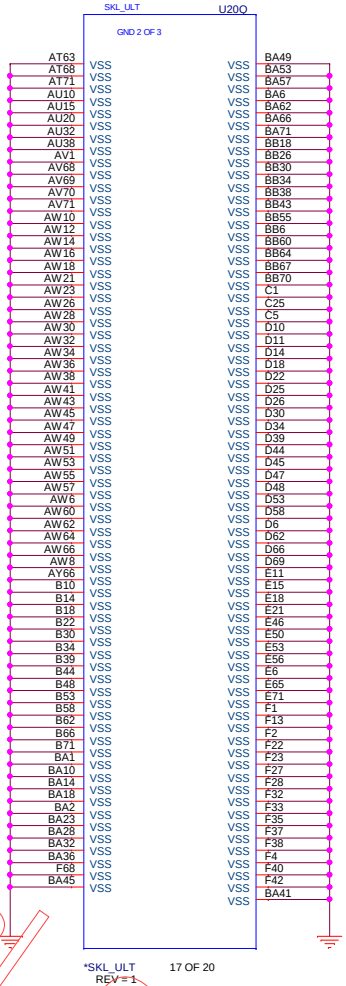

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	SKYPAKE 9/20 (GND-1)	1A
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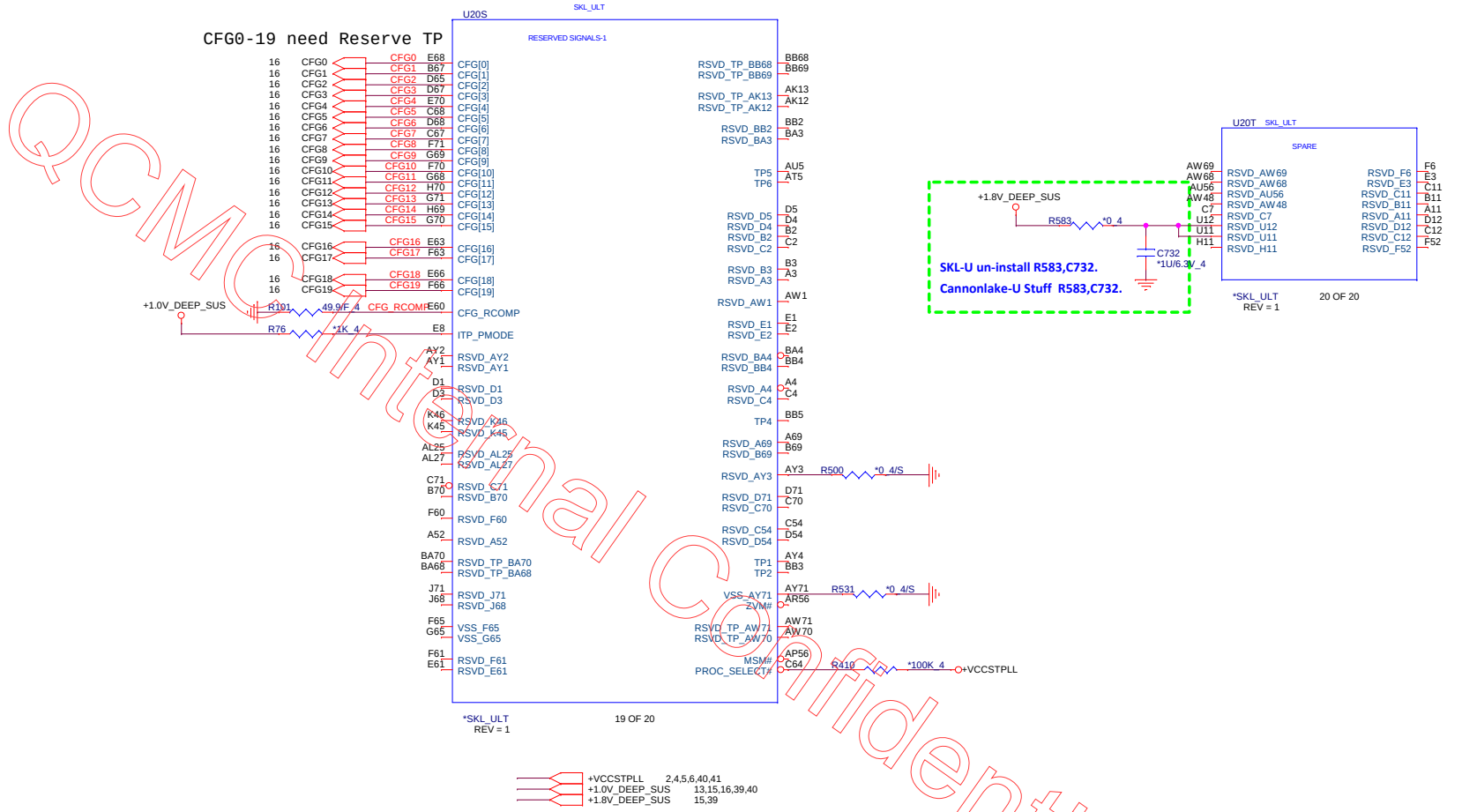

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R430 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R443 1K_4 SI Change

NB5	PROJECT : X1B-10L Quanta Computer Inc.	
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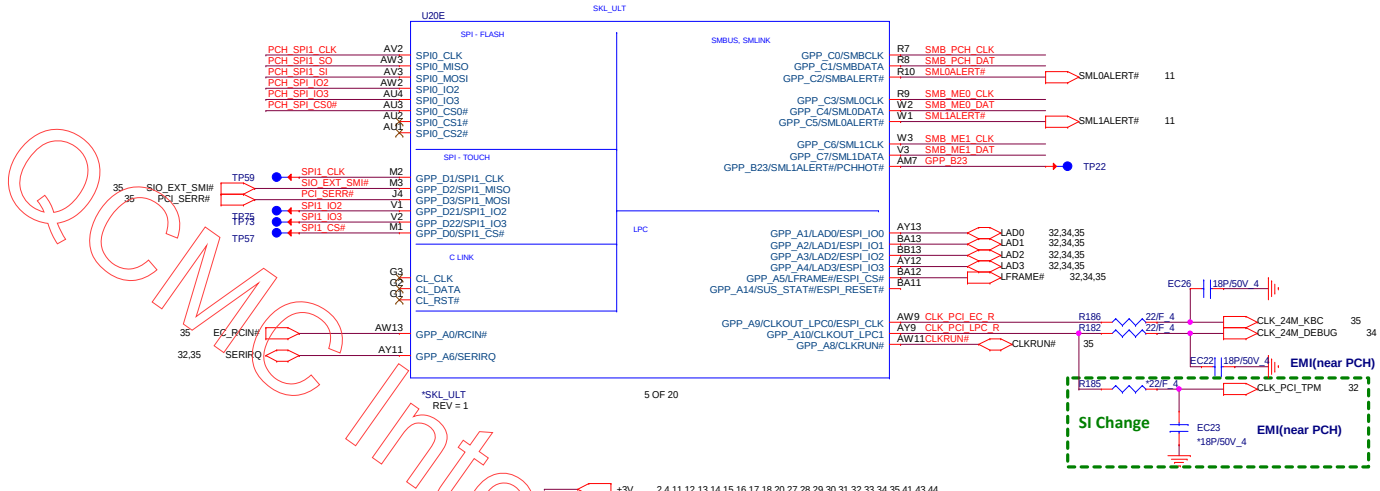
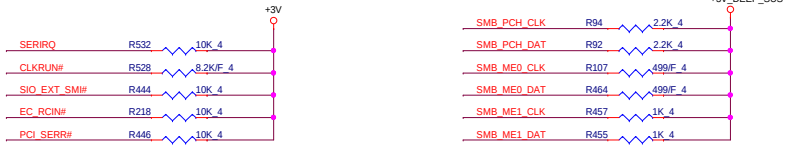
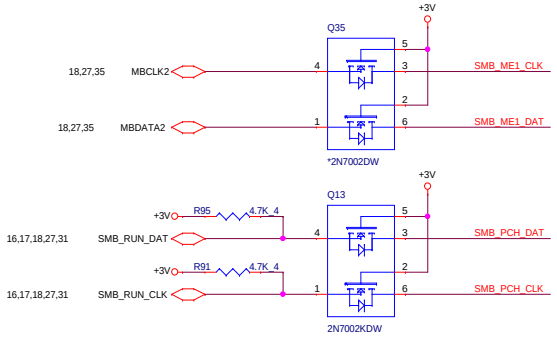


GPIO Pull UP



SMBus/Pull-up(CLG)



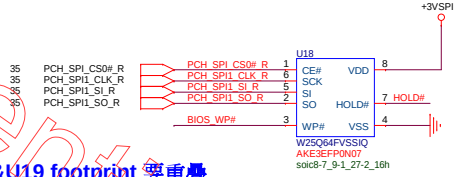
CPU heat pipe local thermal sensor
DDR thermal sensor
RTD2136
EC

Touch Pad
XDP
DDR3-L

PCH SPI ROM(CLG)

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE2EZN0Q00 (GD25B64CSIGR)
Socket		DFHS08FS023 (HOUSING 8P 2R FS)

4M SPI ROM Socket

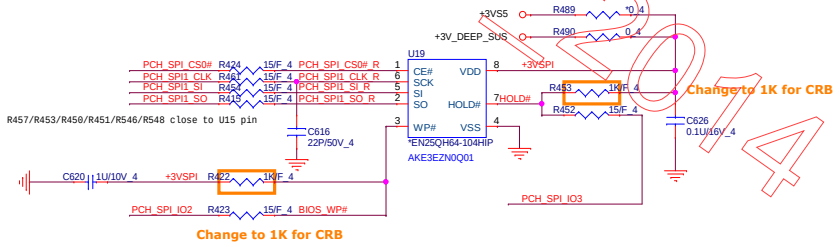


U18&U19 footprint 要重疊

TP66-71 need place to TOP

TP53 PCH_SPI_CS0#_R
TP79 PCH_SPI1_CLK_R
TP72 PCH_SPI1_SI_R
TP50 PCH_SPI1_SO_R
TP45 BIOS_WP#
TP69 HOLD#

PCH SPI ROM(CLG)



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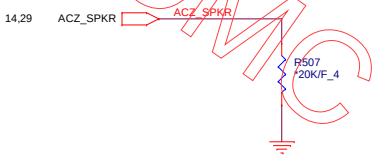
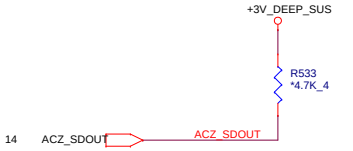
Functional Strap Definitions

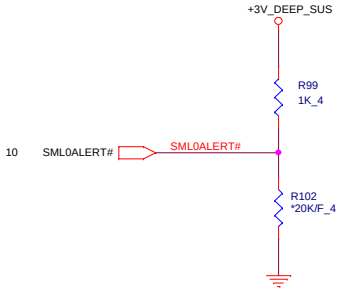
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



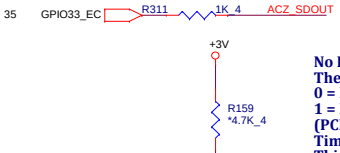
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

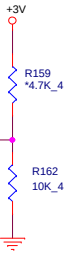


No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

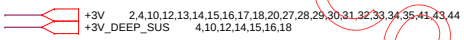


No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.





No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC

No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

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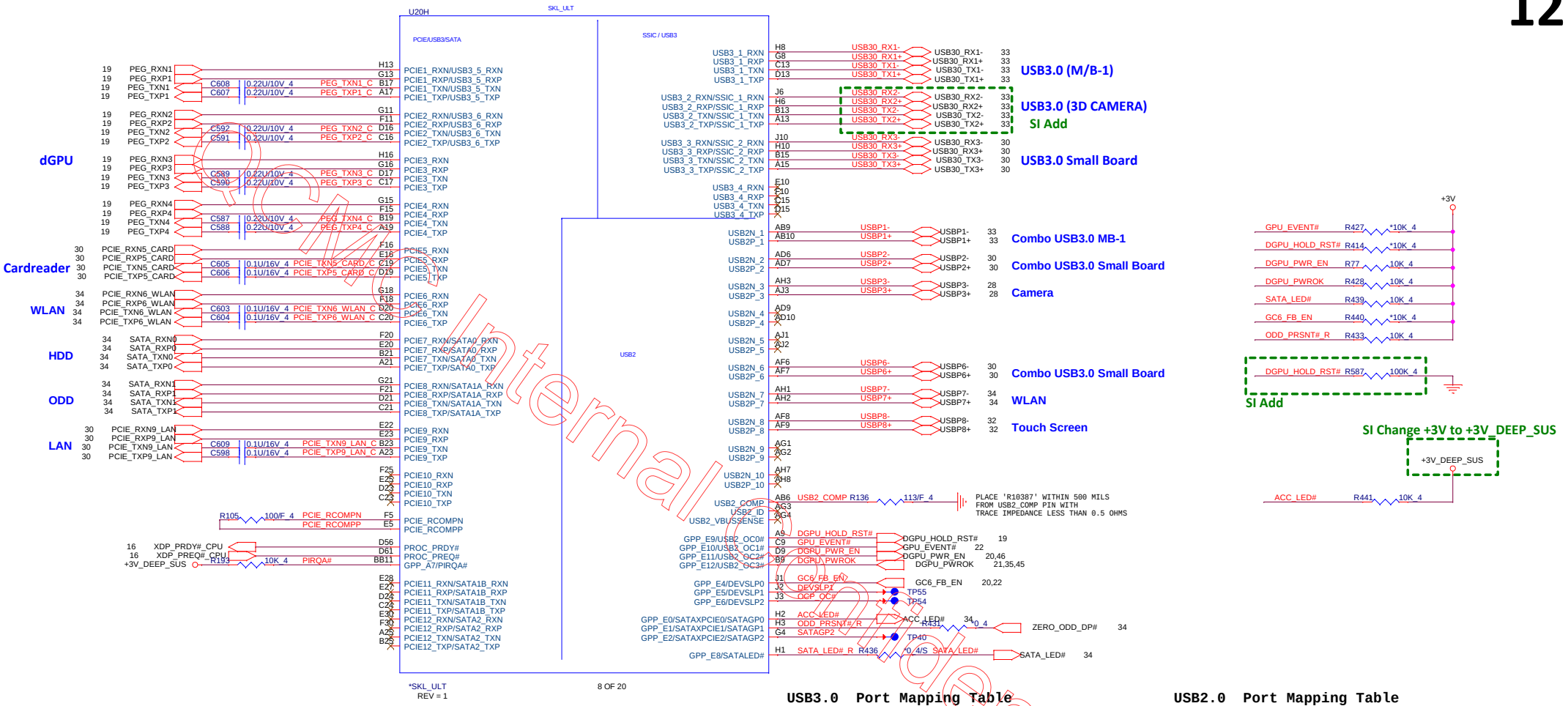

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	Un-used
Port2	dGPU	Port1	CardReader
Port3	dGPU	Port2	WLAN
Port4	dGPU	Port3	LAN
Port5	CardReader	Port4	VGA
Port6	WLAN	Port5	Un-used
Port7	HDD		
Port8	ODD		
Port9	LAN		
Port10	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 3D CAMERA
PORT-3	Cobime USB3.0 Smaii Board
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 Smaii Board
PORT-3	Camera
PORT-4	NC
PORT-5	NC
PORT-6	Cobime USB3.0 Smaii Board
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

+3V 2,4,10,11,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44
+3V_DEEP_SUS 4,10,11,14,15,16,18

PROJECT : X1B-10L
Quanta Computer Inc.
NB5
Size: Custom | Document Number: SKYPAKE 16/20 (PCIE/USB) | Rev: 1A
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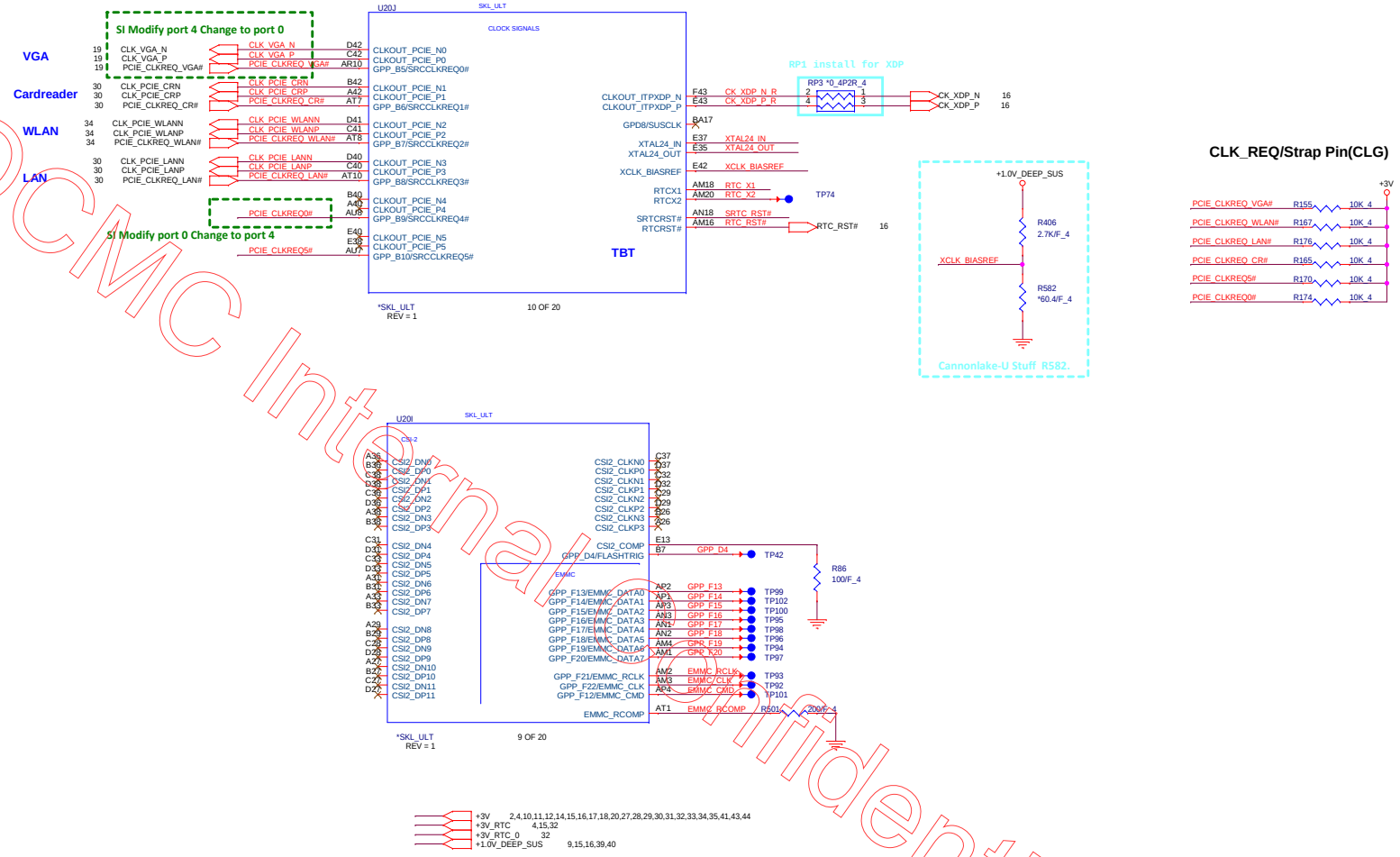
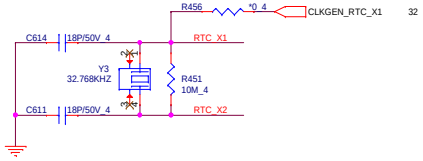
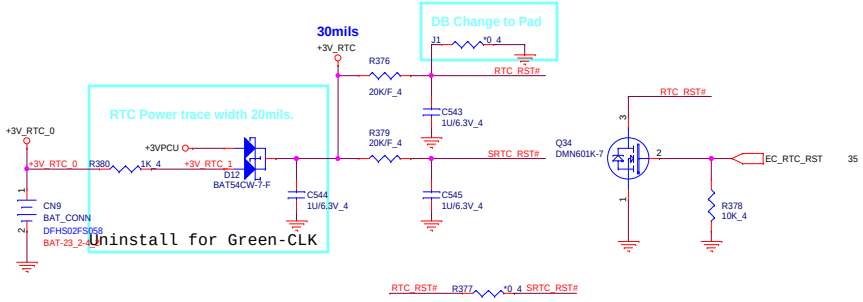


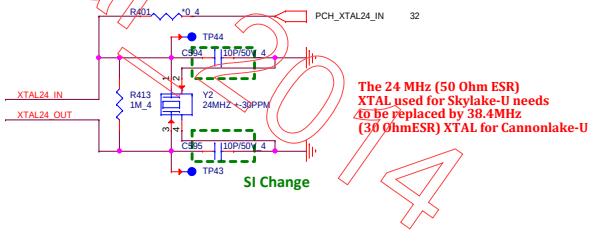
RTC Clock 32.768KHz



RTC Circuitry(RTC)



External Crystal and Green Clock



NB5	PROJECT : X1B-10L Quanta Computer Inc.	
Size: Custom	Document Number: SKYPAKE 17/20 (CLK)	Rev: 1A
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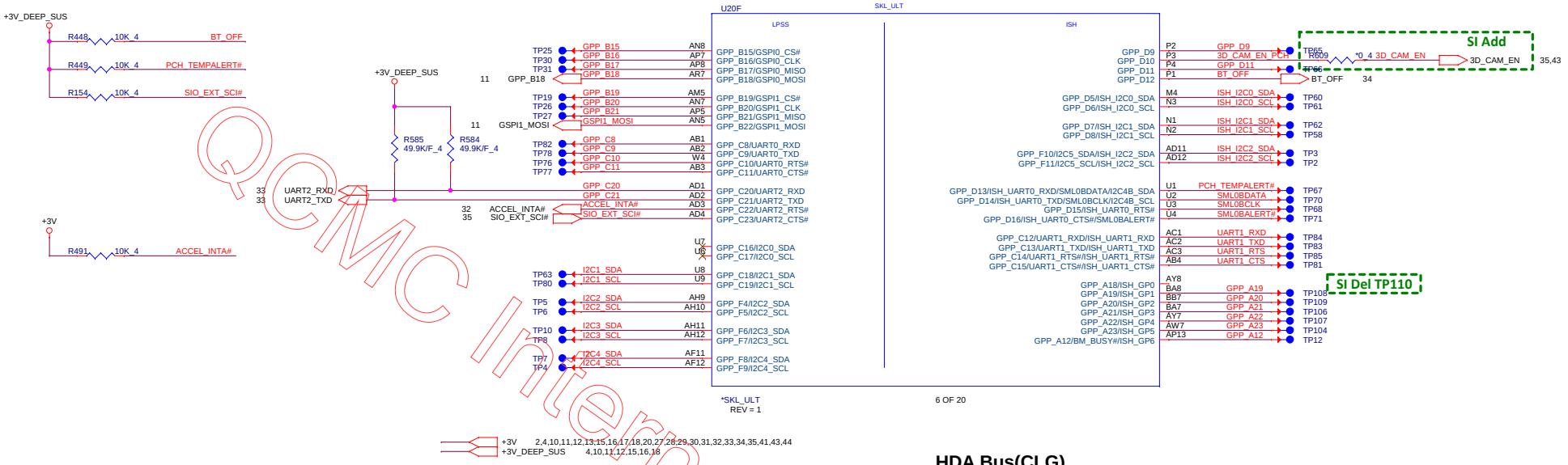
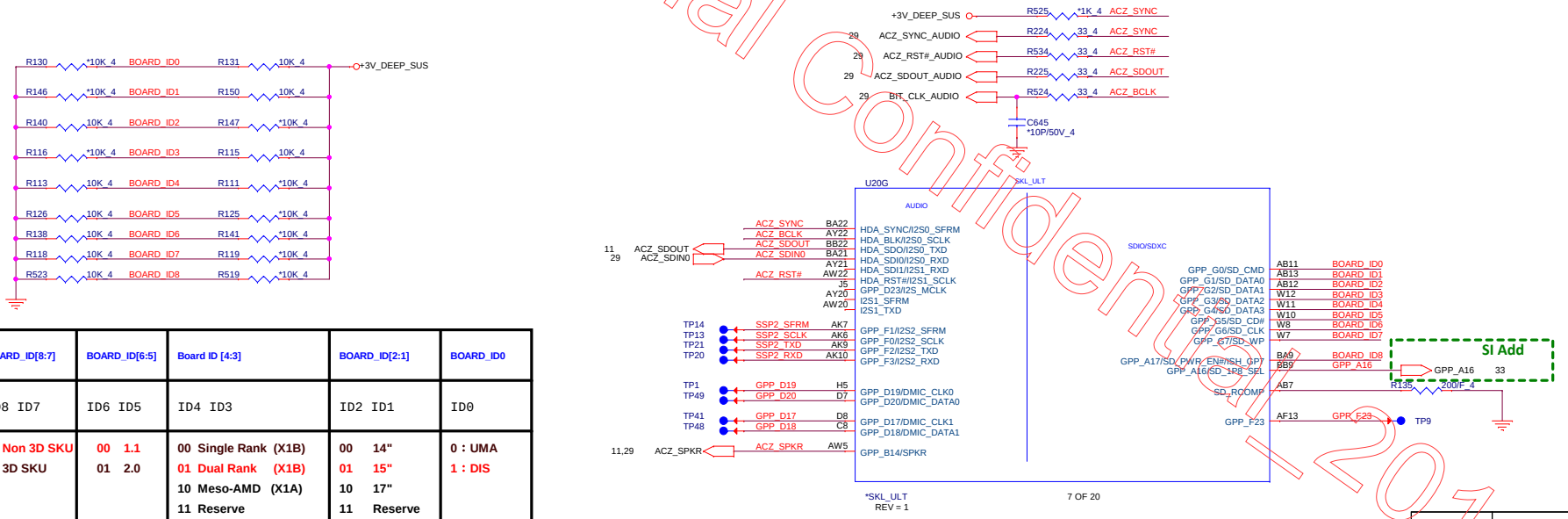
Skylake (GPIO)



+3V 2,4,10,11,12,13,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44
+3V_DEEP_SUS 4,10,11,12,15,16,18

HDA Bus(CLG)



Skylake U	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	00 Non 3D SKU 01 3D SKU	00 1.1 01 2.0	00 Single Rank (X1B) 01 Dual Rank (X1B) 10 Meso-AMD (X1A) 11 Reserve	00 14" 01 15" 10 17" 11 Reserve	0 : UMA 1 : DIS

PROJECT : X1B-10L
Quanta Computer Inc.
NB5
Size: Custom | Document Number: SKYPAKE 19/20 (GPIO) | Rev: 1A
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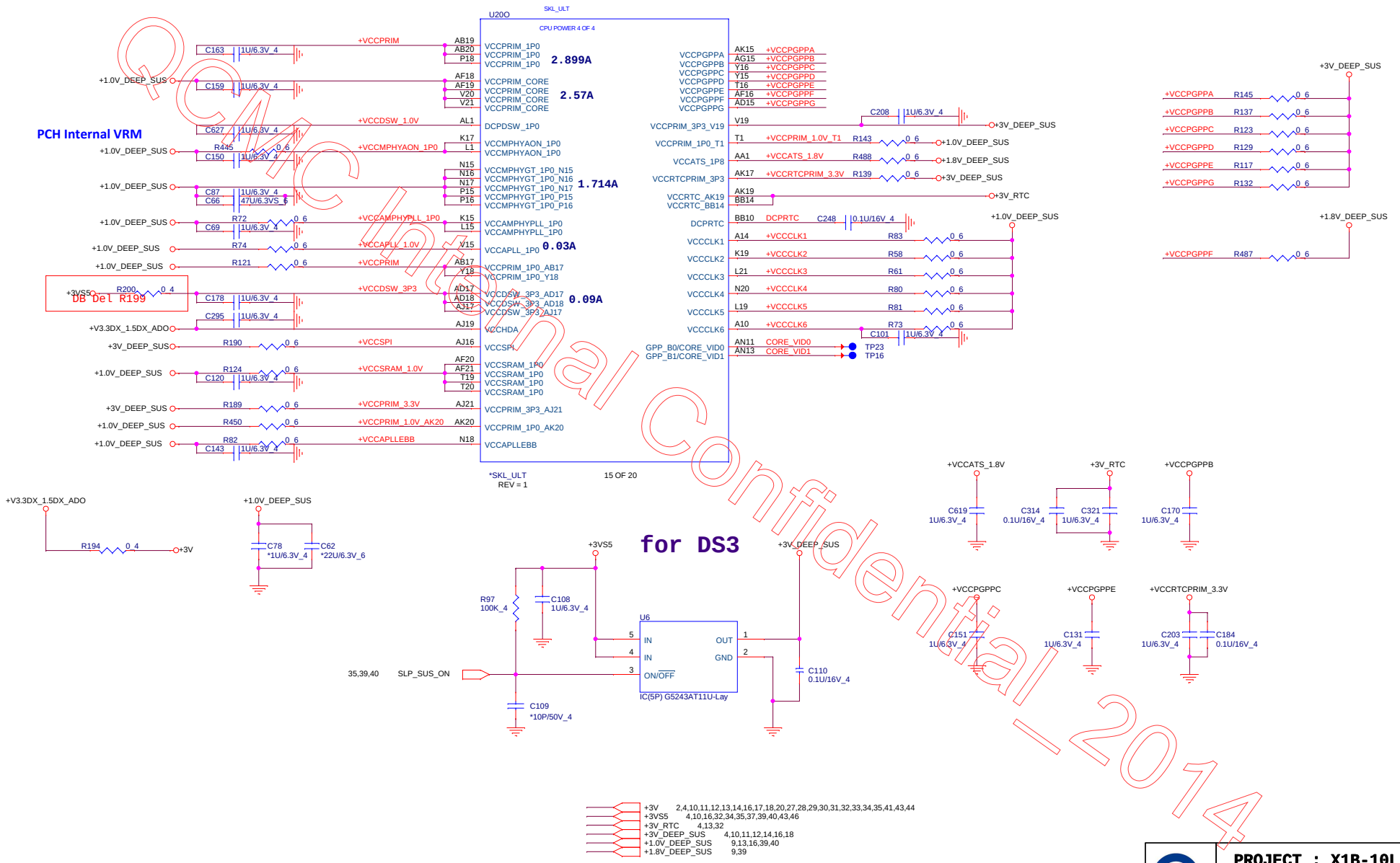
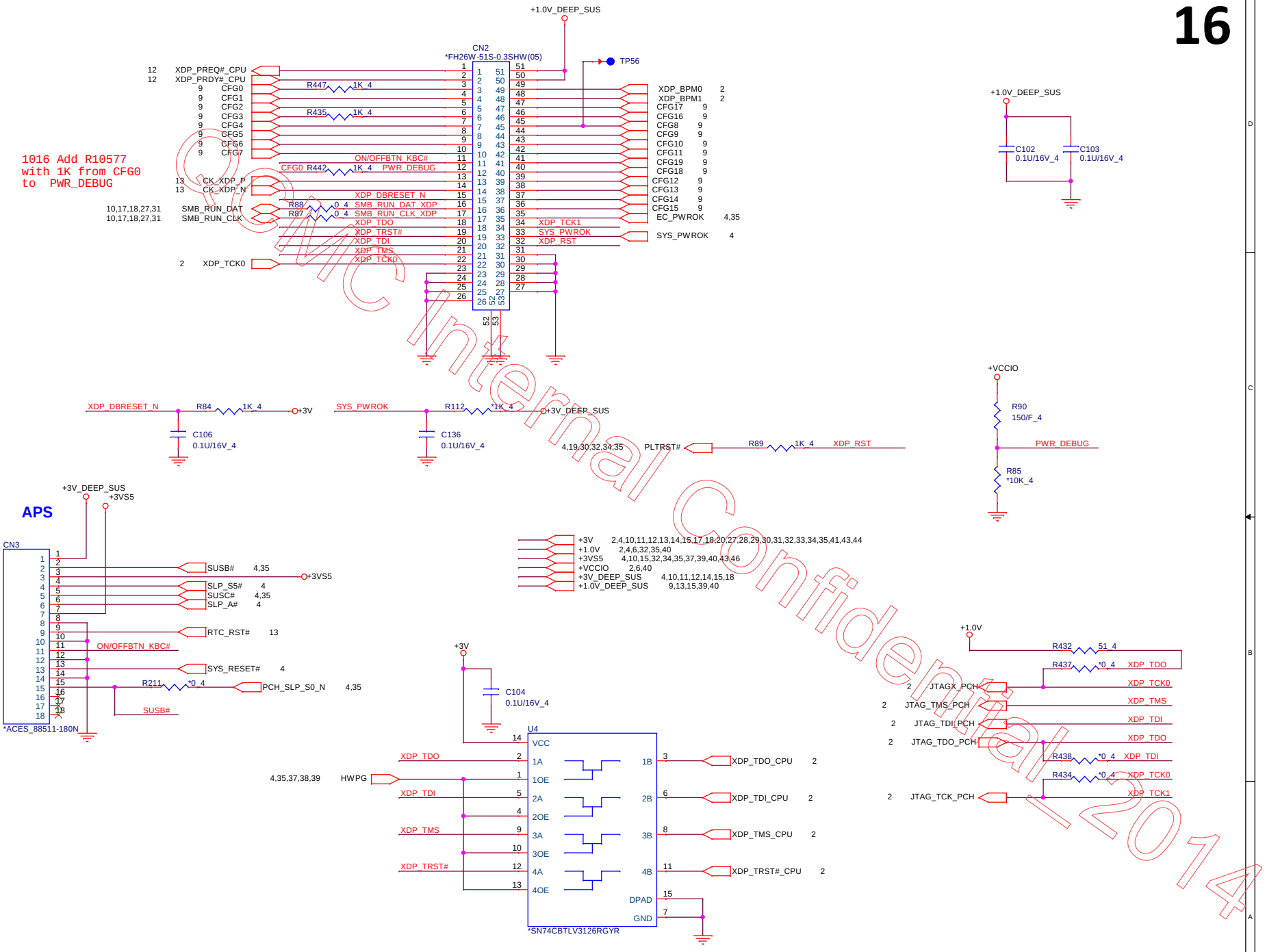
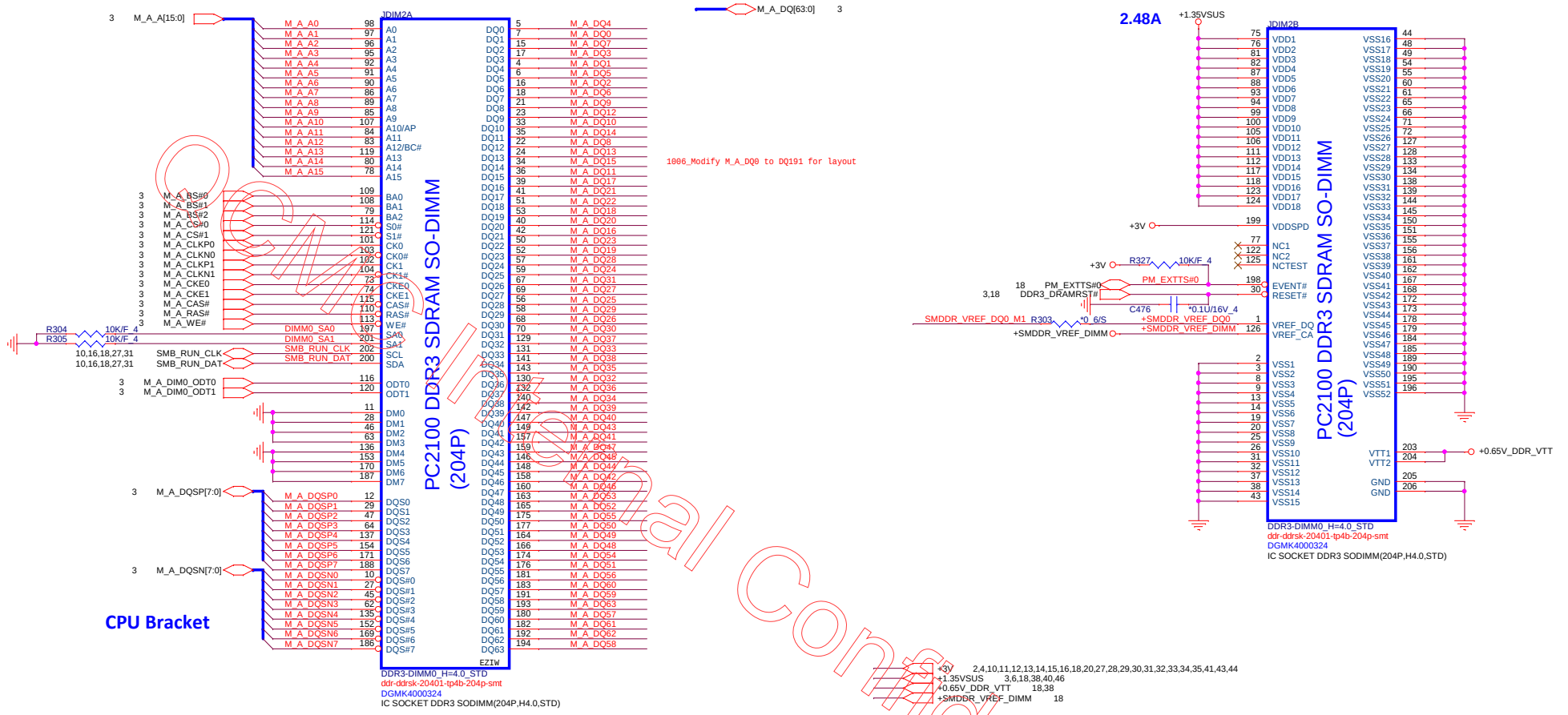


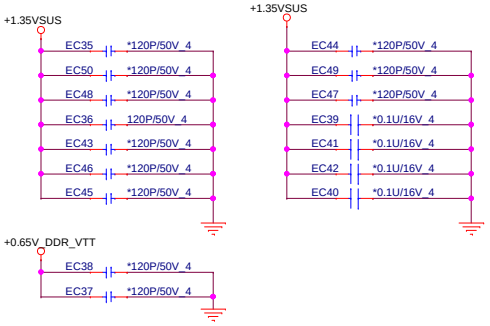
PROJECT : X1B-10L			
Quanta Computer Inc.			
NB5	Size: Custom	Document Number: SKYPAKE 20/20(PCH POWER)	Rev: 1A
	Date: Tuesday, May 05, 2015	Sheet 15 of 49	



NB5	PROJECT : X1B-10L Quanta Computer Inc.	
	Size / Document Number: HSW XDP & APS	Rev 1A
	Date: Tuesday, May 05, 2015	Sheet 16 of 49

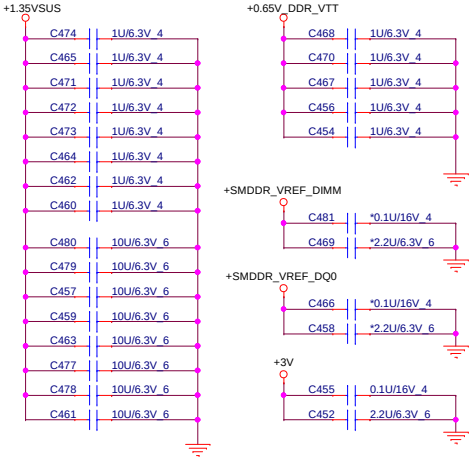


For EMI RESERVE

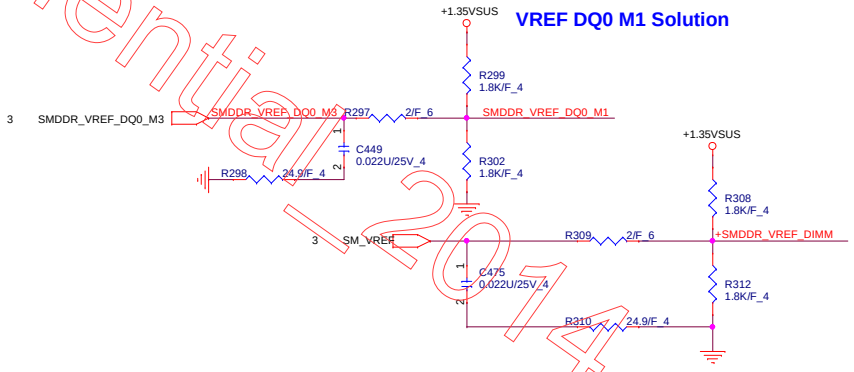


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



VREF DQ0 M1 Solution



NB5	PROJECT : X1B-10L Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM0-STD(4.0H)	Rev: 1A
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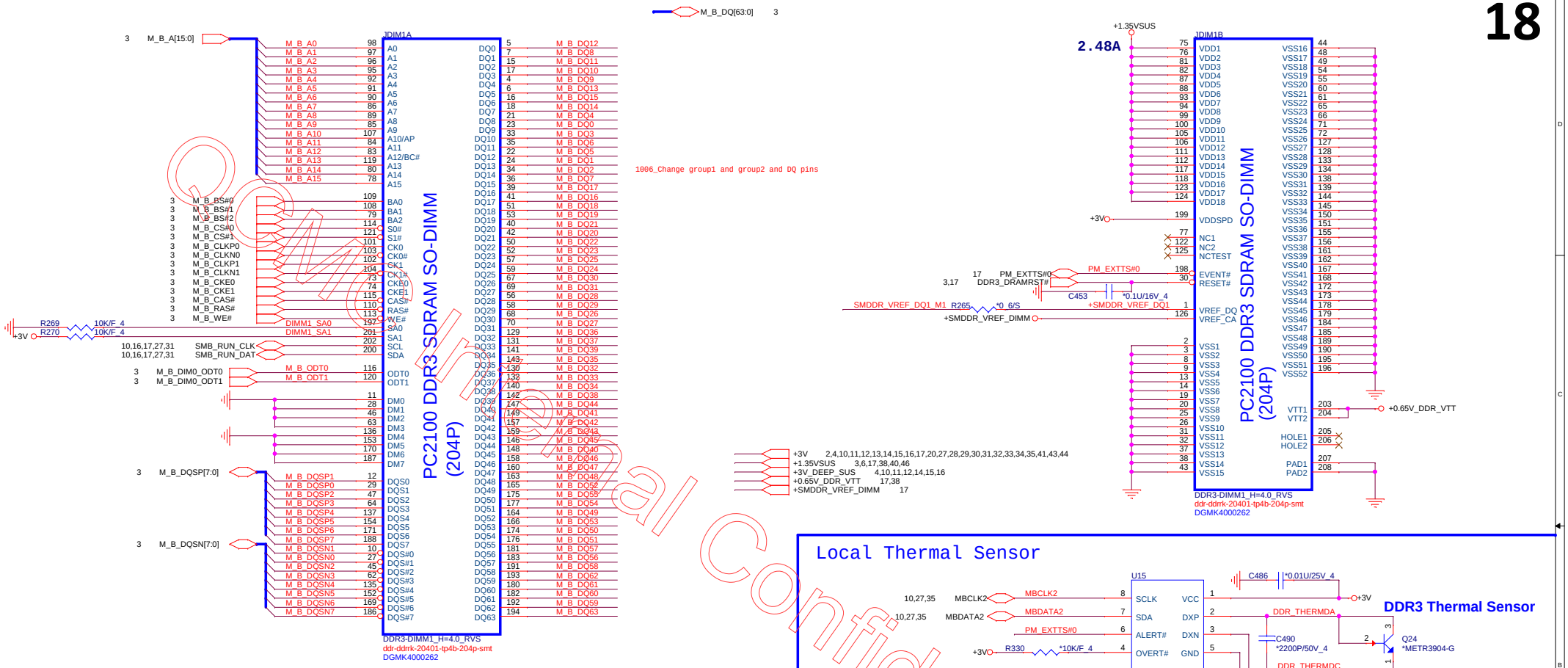
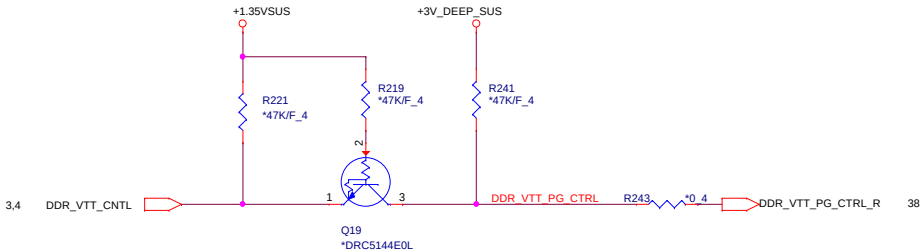
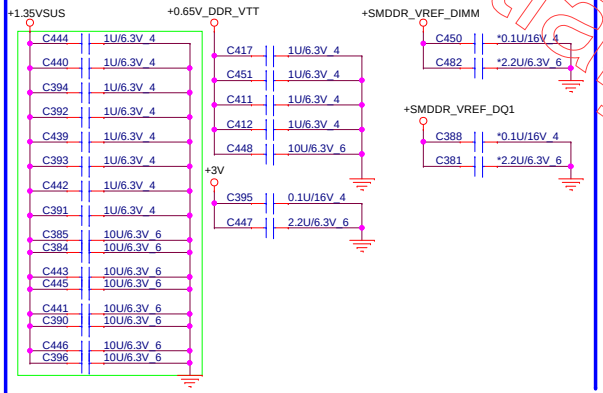


Local Thermal Sensor

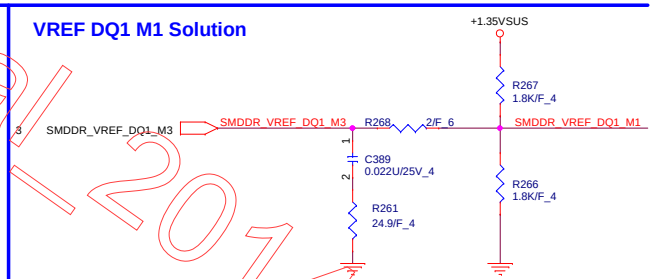
Co-lay for ODT
From Intel MOW, ODT directly connection to CPU



Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector



VREF DQ1 M1 Solution



NB5	PROJECT : X1B-10L Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM1-RVS(4.0H)	Rev: 1A
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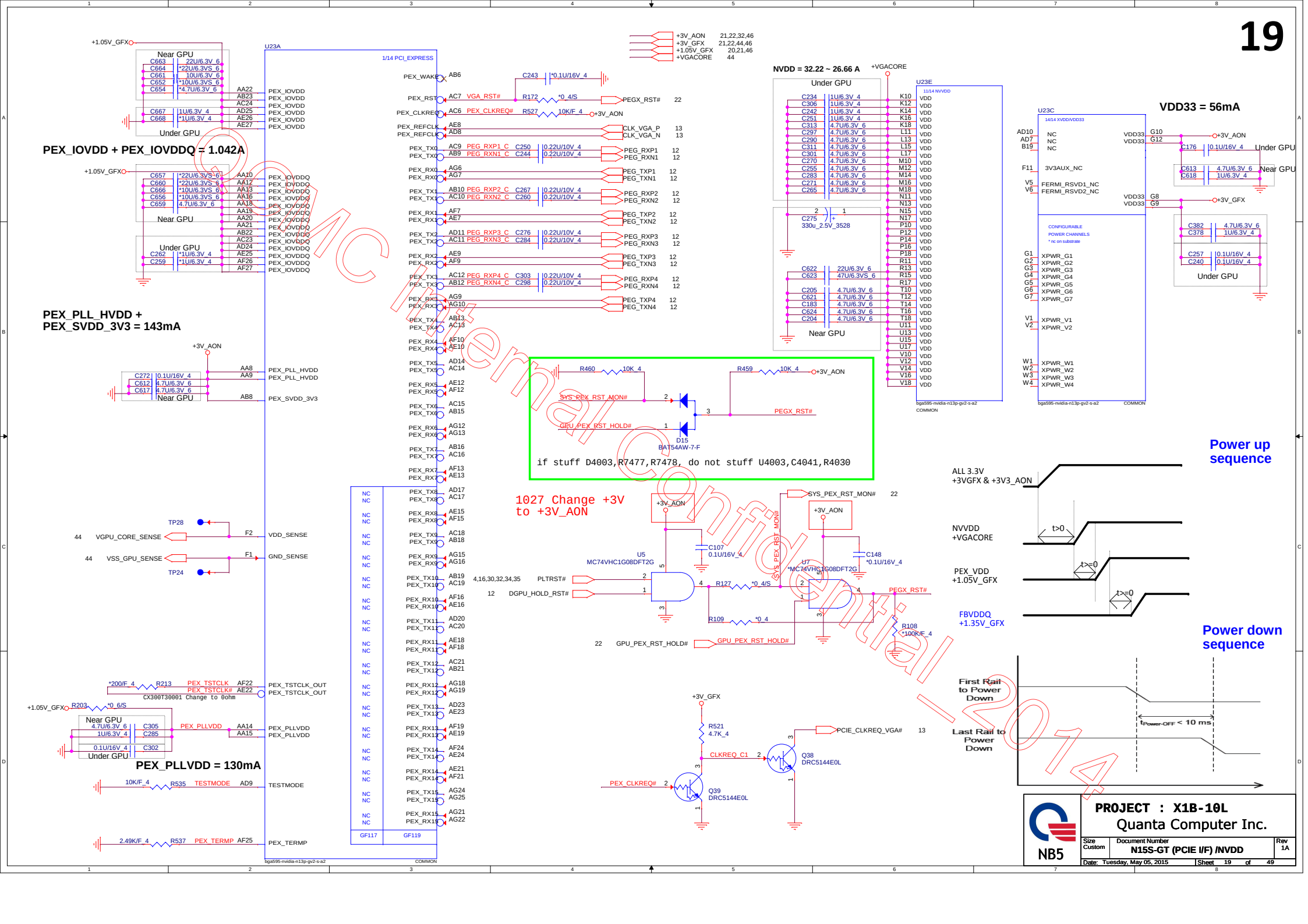
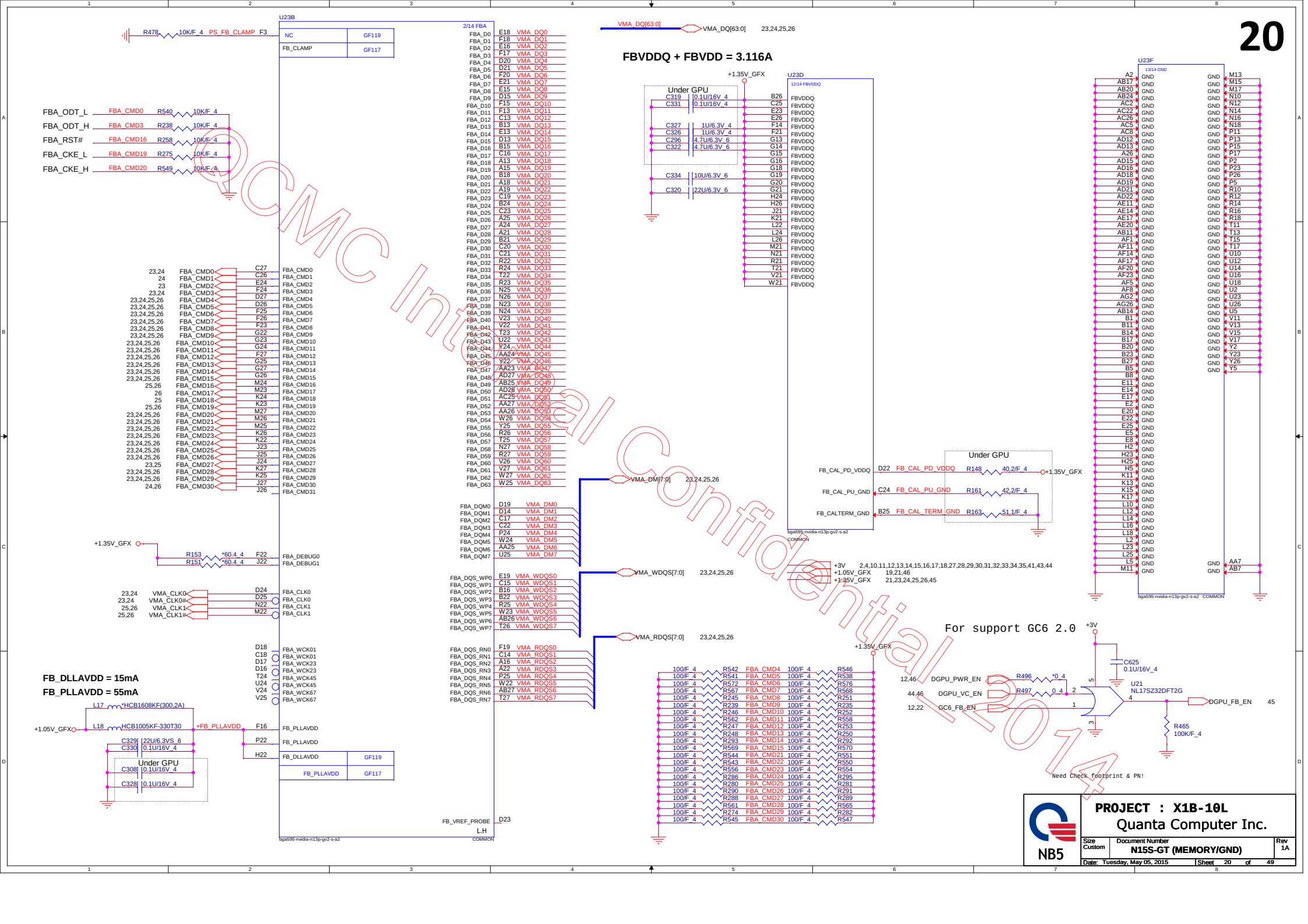
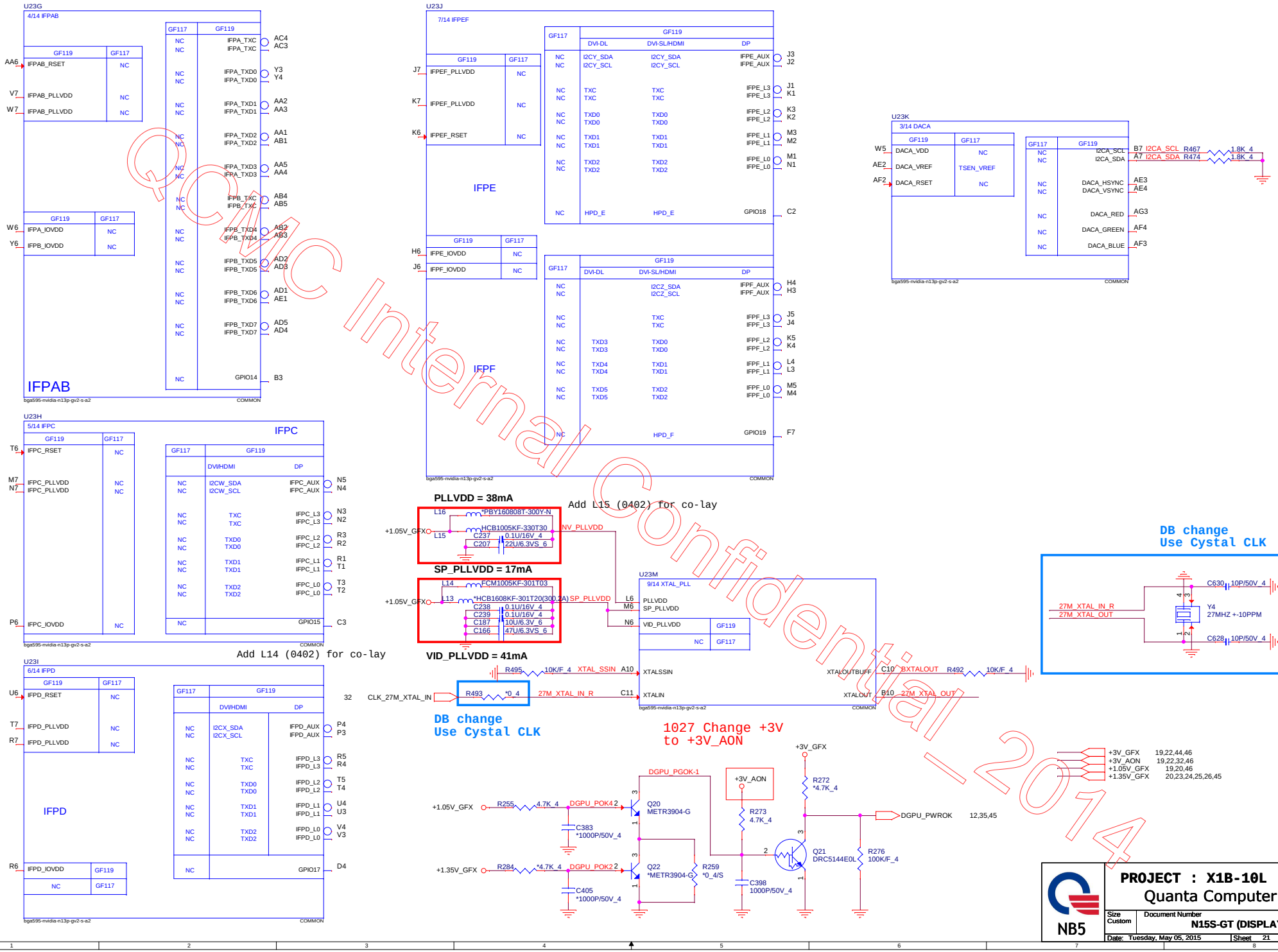
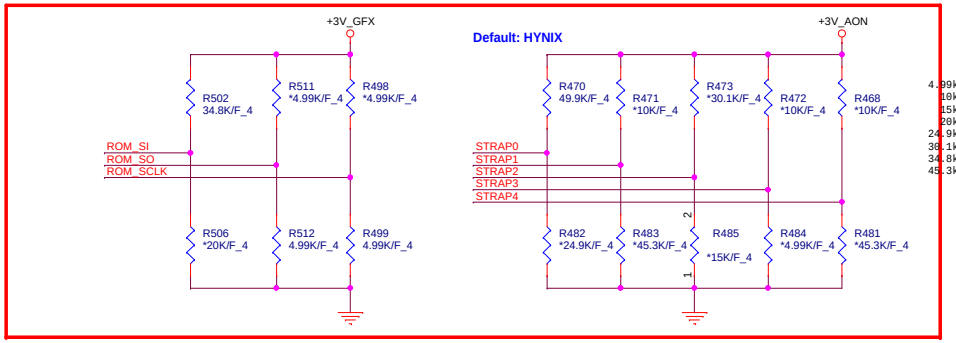
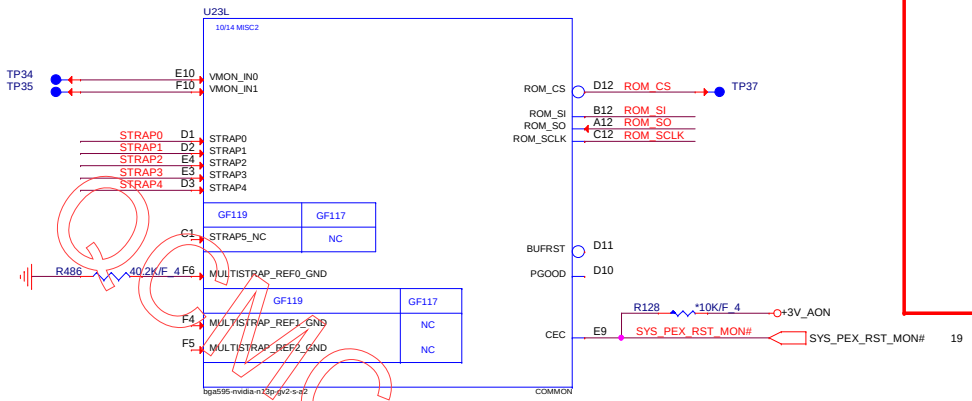
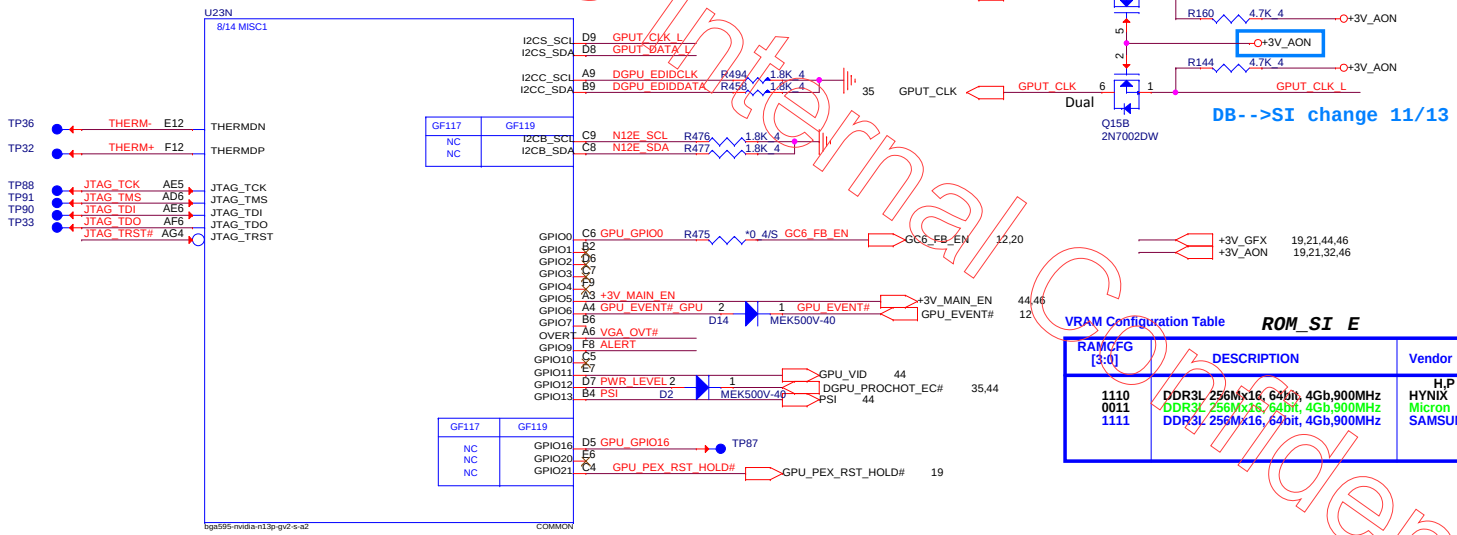












DB-->SI change 11/13

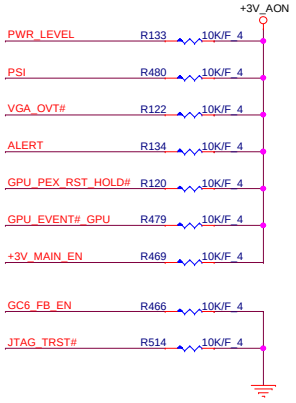


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

VRAM Configuration Table **ROM_SI E**

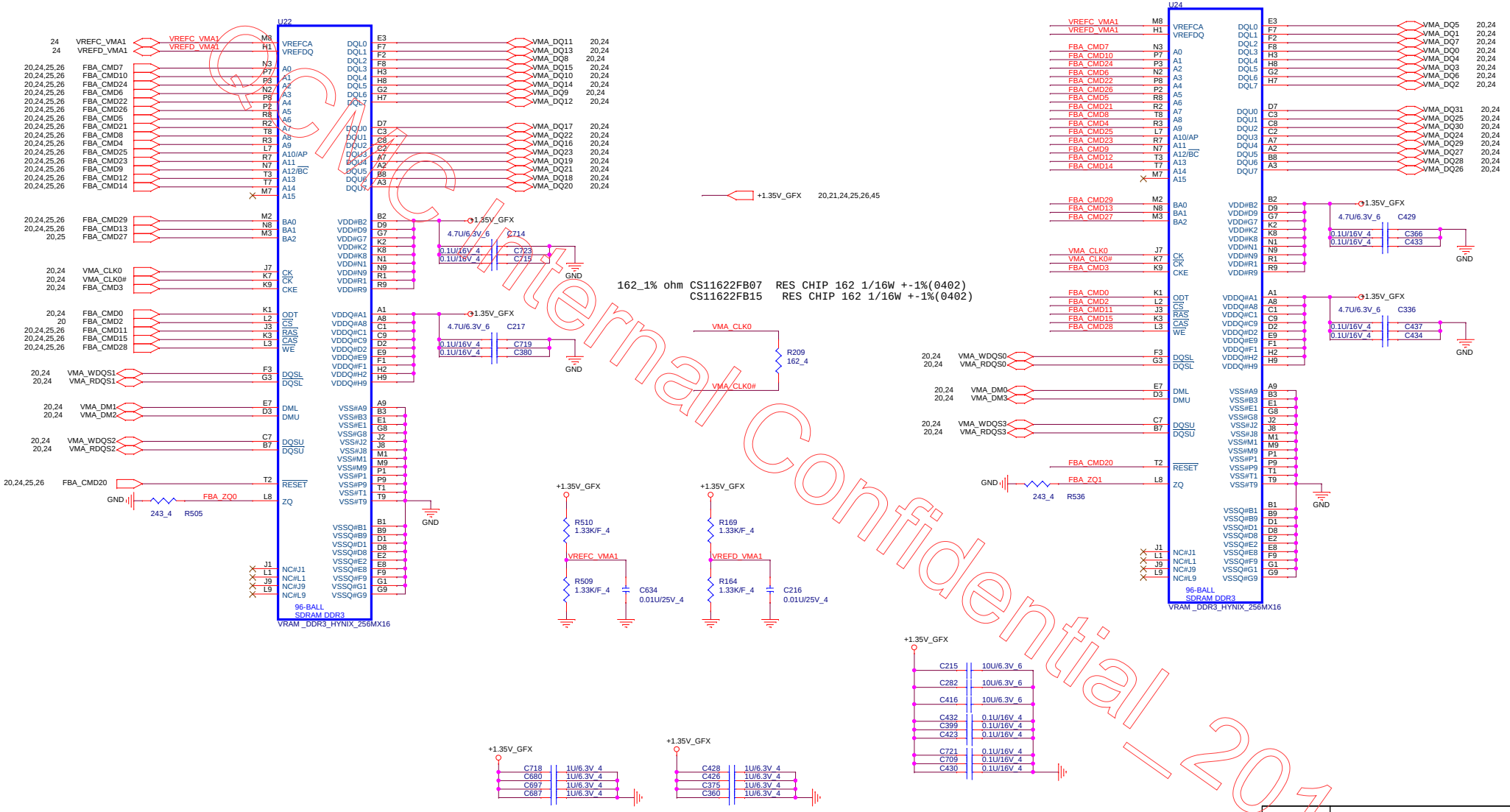
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	256Mx16 Strap	128Mx16 Strap	QBC	TOP B/S
1110	DDR3L 256Mx16, 64bit, 4Gb,900MHz	H,P HYNIX	H5TC4G63CFR-N0C	0XE	TBD	AKD5PZDTW02	AKD5PZDTW01
0011	DDR3L 256Mx16, 64bit, 4Gb,900MHz	Micron	MT41J256M16HA-093G:E	0x4	TBD	AKD5PZSTL01	AKD5PZSTL00
1111	DDR3L 256Mx16, 64bit, 4Gb,900MHz	SAMSUNG	K4W4G1646E-BC1A	0XF	TBD	AKD5PGDT501	AKD5PGDT500

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

Rank0

HYU 256Mx16, H5TC4G63CFR-N0C QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500



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NB5
Size: Custom | Document Number: DDR3L - RANK0 | Rev: 1A
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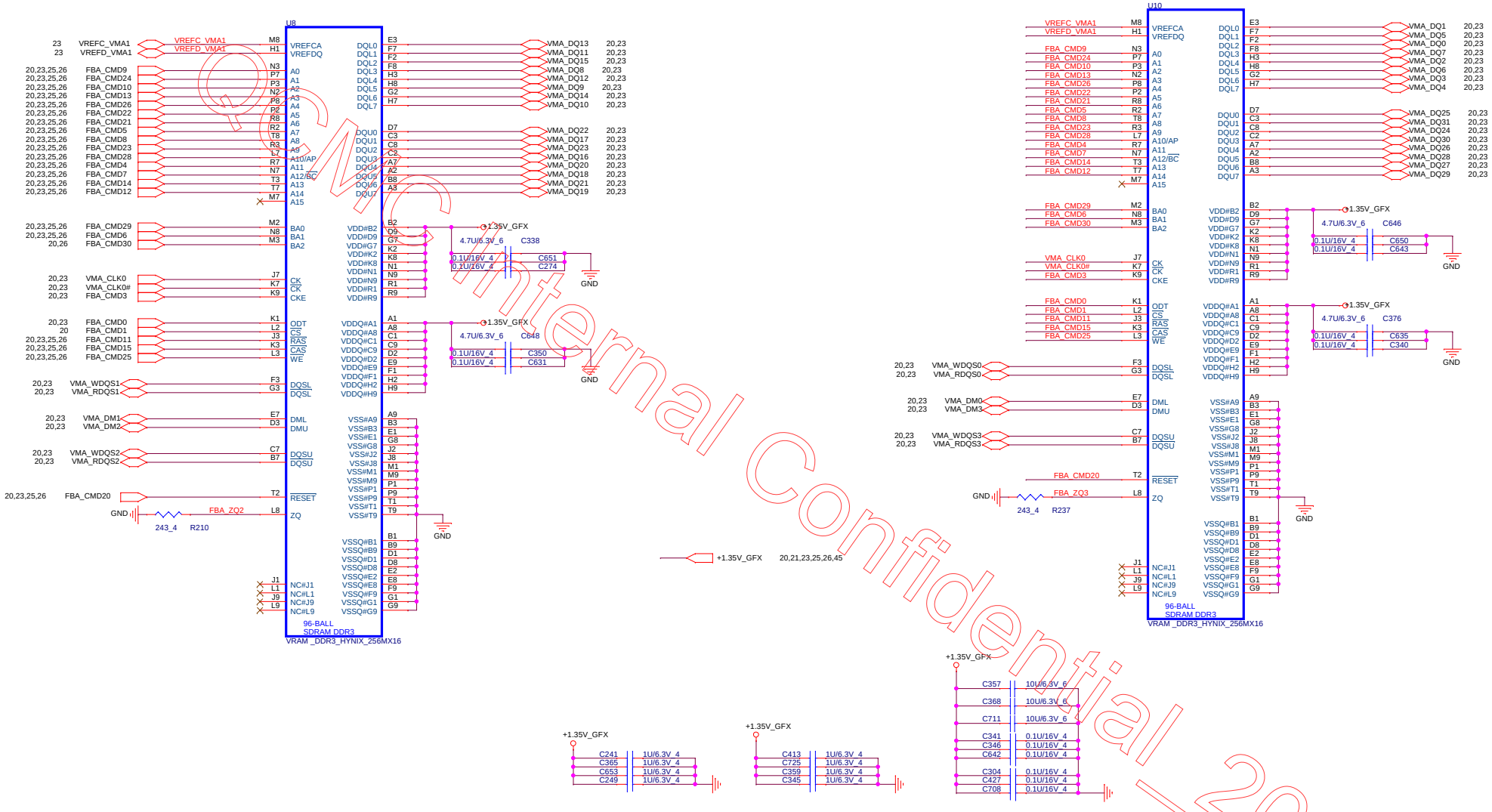
Rank1

HYU 256Mx16, H5TC4G63CFR-N0C QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500



PROJECT : X1B-10L
Quanta Computer Inc.
NB5
Size: Custom | Document Number: DDR3L - RANK1 | Rev: 1A
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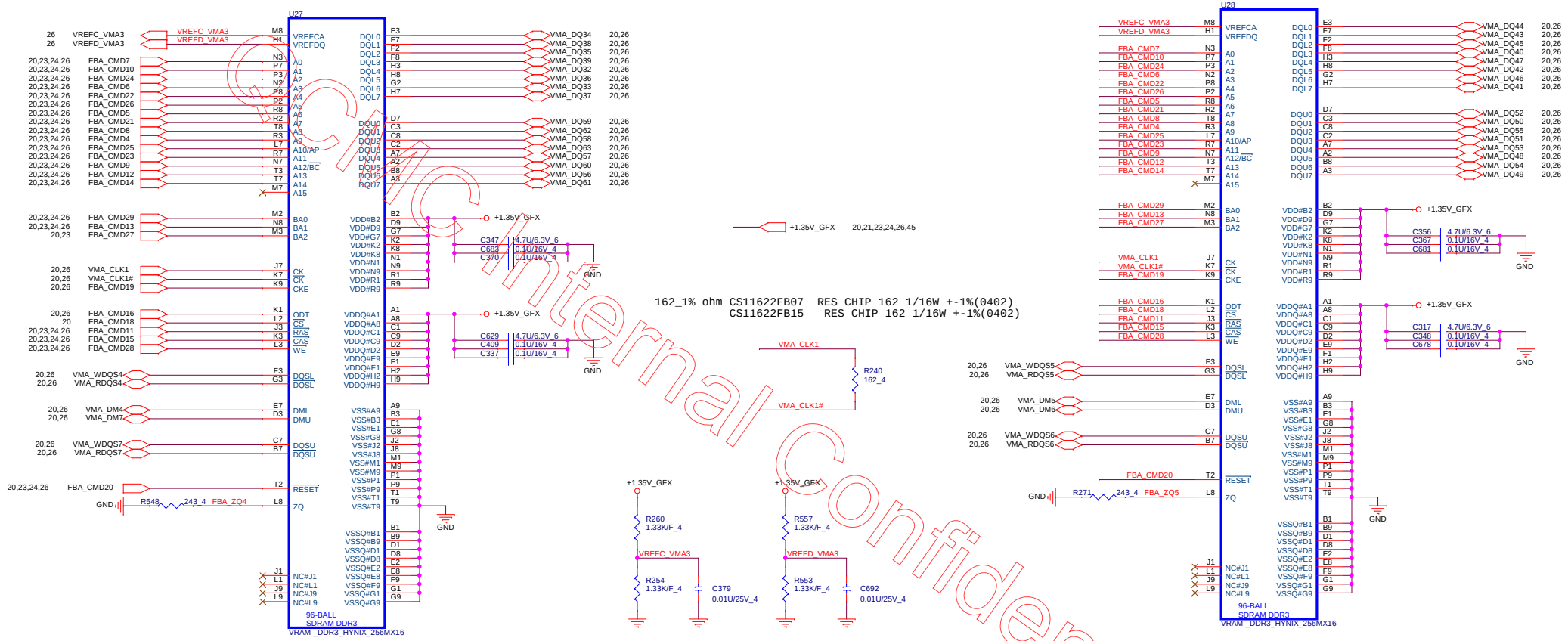
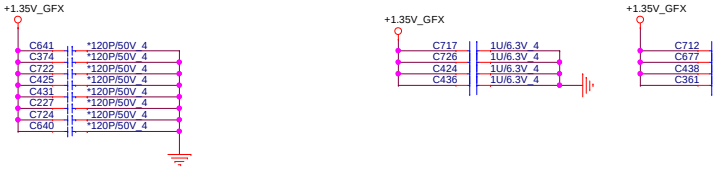
Rank0

HYU 256Mx16, H5TC4G63CFR-N0C QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500



FOR EMI Request



PROJECT : X1B-10L
Quanta Computer Inc.
NB5
Size: Custom | Document Number: DDR3L - RANK0 | Rev: 1A
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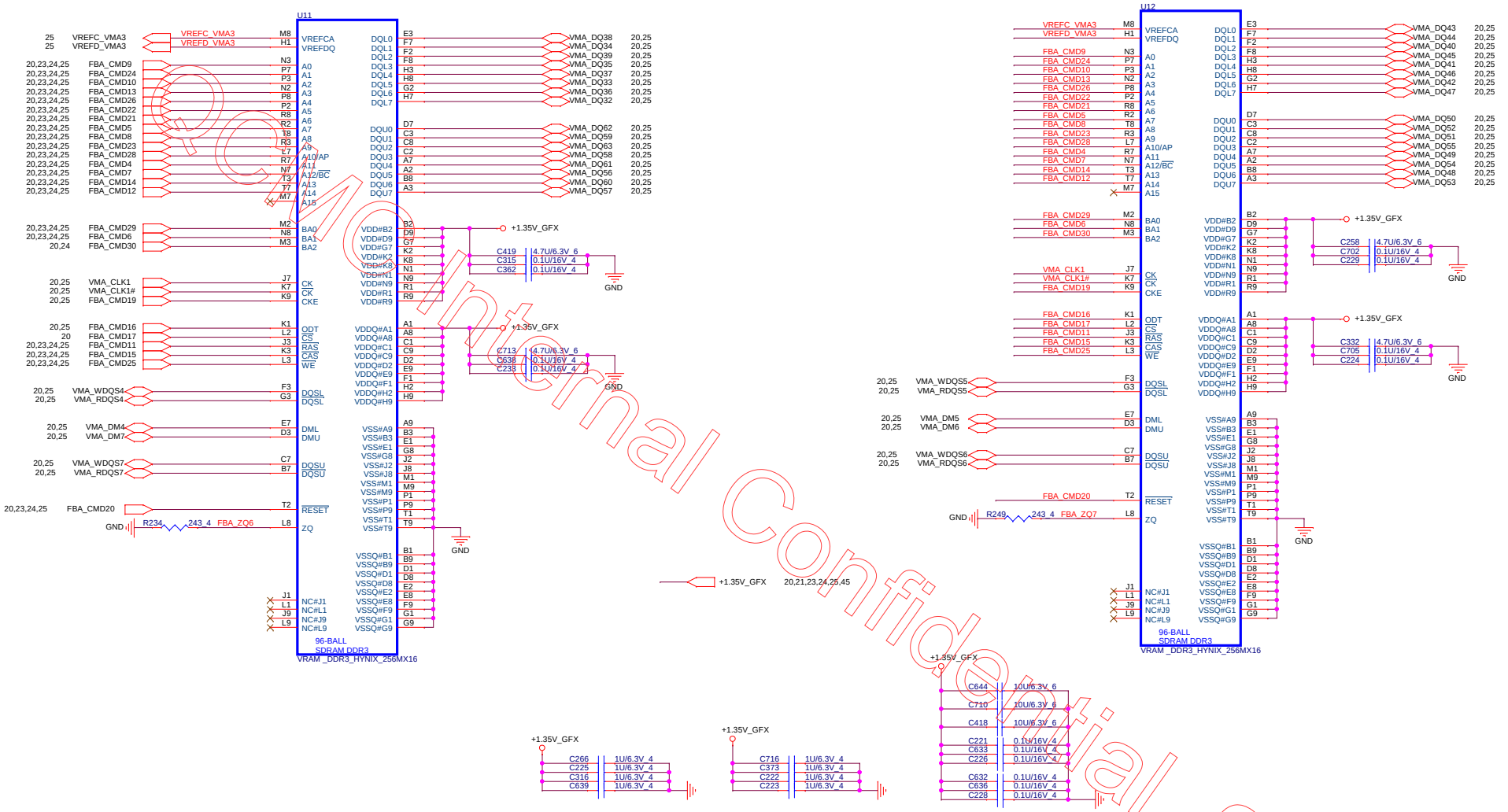
Rank1

HYU 256Mx16, H5TC4G63CFR-N0C QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500



PROJECT : X1B-10L	
Quanta Computer Inc.	
NB5	Size: Custom
Document Number: DDR3L - RANK1	Rev: 1A
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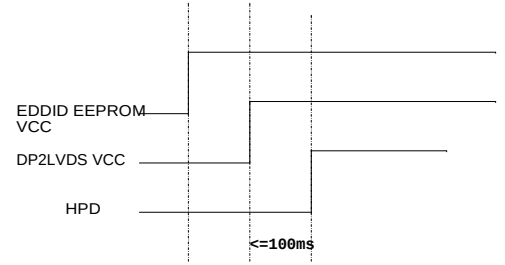
RTD2136S Power Up Sequence



Reserve for co layout EDP CON, EDP only please stuff

R65 0_4 INT_eDP_AUXN_R → INT_eDP_AUXN_R 28
R66 0_4 INT_eDP_AUXP_R → INT_eDP_AUXP_R 28
R69 0_4 INT_eDP_TXP0_R → INT_eDP_TXP0_R 28
R70 0_4 INT_eDP_TXN0_R → INT_eDP_TXN0_R 28
R67 0_4 INT_eDP_TXP1_R → INT_eDP_TXP1_R 28
R68 0_4 INT_eDP_TXN1_R → INT_eDP_TXN1_R 28

+3.3V_2136_A
+1.2V_2136
+3.3V_2136_D
Pin 18: keep 80mil Trace
+SWR_LX

U3 RTD2136R

EDP_HPD_2136 R64 *100k/F_4
DP_HPD
TESTMODE
AUX-CH_N
AUX-CH_P
LANE0P
LANE0N
LANE1P
LANE1N
CIICSCL1
CIICSDA1
MIICSDA1
MIICSCL1
MIICSDA0
MIICSCL0
NC
SWR_LX
DP_V12
SWR_VCCK
VCCK
DP_V33
SWR_VDD
PVCC
DP_GND
GND
DP_REXT
PWMOUT
PWM_VCC
PWMIN
BL_EN

2 INT_EDP_AUXN → INT_EDP_AUXN C79 *0.1U/16V_4 INT_eDP_AUXN_2136
2 INT_EDP_AUXP → INT_EDP_AUXP C80 *0.1U/16V_4 INT_eDP_AUXP_2136
2 INT_EDP_TXP0 → INT_EDP_TXP0 C82 *0.1U/16V_4 INT_eDP_TXP0_2136
2 INT_EDP_TXN0 → INT_EDP_TXN0 C83 *0.1U/16V_4 INT_eDP_TXN0_2136
2 INT_EDP_TXP1 → INT_EDP_TXP1 C75 *0.1U/16V_4 INT_eDP_TXP1_2136
2 INT_EDP_TXN1 → INT_EDP_TXN1 C76 *0.1U/16V_4 INT_eDP_TXN1_2136

TXO0- TXO0+ TXO1- TXO1+ TXO2- TXO2+ TXOC- TXOC+ TXO3- TXO3+
TXE0- TXE0+ TXE1- TXE1+ TXE2- TXE2+ TXEC- TXEC+ TXE3- TXE3+

TXLOUT0-_2136 28
TXLOUT0+_2136 28
TXLOUT1-_2136 28
TXLOUT1+_2136 28
TXLOUT2- 28
TXLOUT2+ 28
TXLCLKOUT- 28
TXLCLKOUT+ 28
TXUOUT0- 28
TXUOUT0+ 28
TXUOUT1- 28
TXUOUT1+ 28
TXUOUT2- 28
TXUOUT2+ 28
TXUCLKOUT- 28
TXUCLKOUT+ 28

BL_EN → 2136_LVDS_BLON → 2136_LVDS_BLON 28

SCL1_2136
SDA1_2136
28 EDIDDATA_2136
28 EDIDCLK_2136
SDAT_2136
SCLK_2136

10,16,17,18,31 SMB_RUN_CLK R62 *0_4
10,16,17,18,31 SMB_RUN_DAT R63 *0_4
Reserve

IC底部需接GND

PCH_DPST_PWM R32 *100K/F_4
Use 1% Res on R32
R47 *12K/F_4

2136_DISP_ON → 2136_DISP_ON 28
2136_DPST_PWM → 2136_DPST_PWM 28

For eDP, close to U3
2 PCH_DPST_PWM R31 0_4 EDP_DPST_PWM 28

10,18,35 MBCLK2 R53 *0_4 SCL1_2136
10,18,35 MBDATA2 R54 *0_4 SDA1_2136
Default(LVDS Only)

LVDS Only
2,28 ULT_EDP_HPD R46 *1K/F_4 EDP_HPD_2136
+3V R42 *4.7K_4 SCLK_2136
SDAT_2136
R40 *4.7K_4

+3V 2,4,10,11,12,13,14,15,16,17,18,20,28,29,30,31,32,33,34,35,41,43,44
+3V C105 0.1U/16V_4

L10: need use CV-4709MN00 for Vendor suggestion

keep 80 mil
+3V L8 *PBY160808T-600Y-N USING 60R 2A
+3.3V_2136_D
C47 *10U/6.3VS_6
C45 *0.1U/16V_4
C46 *0.1U/16V_4
CLOSE TO Pin22

+3.3V_2136_D
C56 *0.1U/16V_4
C52 *22U/6.3VS_6
Close to Pin18

+3V
+3.3V_2136_A
L12 *PBY160808T-600Y-N USING 60R 1A
C93 *10U/6.3V_6
C74 *0.1U/16V_4
C85 *0.1U/16V_4
Close to Pin5

+SWR_LX
+1.2V_2136
L9 *4.7UH_1A
R39 *0_8
C64 *22U/6.3VS_6
C60 *0.1U/16V_4
C57 *0.1U/16V_4
C59 *0.1U/16V_4
Close to Pin17
Close to Pin43
Close to Pin11

SWR MODE	LDO MODE
Stuff L9	Stuff R39

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Quanta Computer Inc.
NB5
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LID Switch

do not modify to short pad

35 EMU_LID — R55 0_4 — PN_BLON — D1 MEK500V-40 — BLON_CON — C67 22P/50V_4 — R44 100K/F_4

OUT_LVDS_BLON — R45 1K/F_4

OUT_LVDS_BLON — R56 100K/F_4

OUT_DPST_PWM — R51 1K/F_4 — VADJ1

C73 33P/50V_4

100mA

+VIN — +VIN_BLIGHT — C582 0.1U/25V_4 — C584 0.01U/25V_4

For LVDS

Close to LVDS connector

Power Switch Reserve

80 mil trace

27 2136_DISP_ON — R15 *0_8 — +3VLCD_CON

R19 *100K/F_4 — C30 *4.7U/6.3V_4

For eDP

Close to LVDS connector

+3V — C21 1U/6.3V_4

2 PCH_DISP_ON — R16 100K/F_4

R16 close to U1 for eDP,stuff

U1 AP2821KTR-G1-H: 5 IN, 4 IN, 3 ON/OFF, 1 OUT, 2 GND

L6 HCB1608KF-181T15_S0_6

C24 0.01U/50V_4 — C26 0.1U/16V_4 — C19 10U/6.3V_6

+3VLCD_CON

for eDP,stuff U1 & L6

for LVDS,stuff C30 & R15,R19

+VIN — C580 *4.7U/25V_8 — C575 0.1U/25V_4

+VIN — C581 *4.7U/25V_8 — C574 0.1U/25V_4 — C583 0.1U/25V_4 — C568 0.1U/25V_4 — C573 0.1U/25V_4

+3V — +3V_CAM — C561 *0.01U/50V_4 — C560 *4.7U/6.3V_6

+3VLCD_CON — C547 0.047U/25V_4 — C546 0.047U/25V_4

GS12401-1011-9H
lvds-50671-04041-001-40p-l
DFFC40FR068

CN8

+3V — C548 1000P/50V_4

EDIDCLK_R
EDIDDATA_R
TXLOUT0-
TXLOUT0+
TXLOUT1-
TXLOUT1+
TXLOUT2-
TXLOUT2+
TXLCLKOUT-
TXLCLKOUT+
TXUOUT0-
TXUOUT0+
TXUOUT1-
TXUOUT1+
TXUOUT2-
TXUOUT2+
TXUCLKOUT-
TXUCLKOUT+

For LVDS Only: Stuff Rc

For EDP Only: Stuff Rd

2,27 ULT_EDP_HPD — R36 *0_4 Rc — R38 0_4 Rd — ULT_EDP_HPD_R

PV Del R390,R391

PV Change

MCM2012B600GBE

12 USBP3- — 12 USBP3+ — +3V_CAM — L28 — USBP3-_C — USBP3+_C

29 DIGITAL_CLK — L10 BLM15AG121SN1D — DIGITAL_CLK_L

29 DIGITAL_D1 — L11 BLM15AG121SN1D — DIGITAL_D1_L

VADJ1

BLON_CON

SI Change

C92 *10P/50V_4 — C91 *10P/50V_4

+VIN_BLIGHT

RF

For LVDS Only:

+3V — R34 *4.7K_4 EDIDCLK_2136 — R33 *4.7K_4 EDIDDATA_2136

C49 *10P/50V_4 — C50 *10P/50V_4

1106 change HDMI signal connection for layout

+3V 2,4,10,11,12,13,14,15,16,17,18,20,27,29,30,31,32,33,34,35,41,43,44

+5V 29,30,31,32,33,34,43

+VIN 31,33,34,36,37,38,39,41,42,43,44,45,46

2 IN_D0 — IN_D0 C253 — 0.1U/16V_4 C_TX0_HDMI+

2 IN_D0# — IN_D0# C261 — 0.1U/16V_4 C_TX0_HDMI-

2 IN_D1 — IN_D1 C236 — 0.1U/16V_4 C_TX1_HDMI+

2 IN_D1# — IN_D1# C247 — 0.1U/16V_4 C_TX1_HDMI-

2 IN_D2 — IN_D2 C220 — 0.1U/16V_4 C_TX2_HDMI+

2 IN_D2# — IN_D2# C230 — 0.1U/16V_4 C_TX2_HDMI-

2 IN_CLK — IN_CLK C268 — 0.1U/16V_4 C_IN_CLK

2 IN_CLK# — IN_CLK# C279 — 0.1U/16V_4 C_IN_CLK#

Close to HDMI connector

+3V — Q40 2N7002K(DMN601K-7)

DGPU_CL_HDMIP — R508 470/F_4 C_TX2_HDMI+ — R513 470/F_4 C_TX2_HDMI-

R516 470/F_4 C_TX1_HDMI+ — R517 470/F_4 C_TX1_HDMI-

R518 470/F_4 C_TX0_HDMI+ — R522 470/F_4 C_TX0_HDMI-

R526 470/F_4 C_IN_CLK — R530 470/F_4 C_IN_CLK#

R529 1 — 2 100K/F_4 — C647 0.1U/16V_4

Close to Q40

+3V — R520 1M_4 — Q37 2N7002K(DMN601K-7)

2 HDMI_HPD_CON — 3 HDMI_HPD — R515 20K/F_4

HDMI SMBus Isolation

+3V — R504 2.2K_4 — Q36 2N7002DW — R503 2.2K_4 — +3V

2 SDVO_CLK — HDMI_SCLK

2 SDVO_DATA — HDMI_SDATA

+5V_HDMIC — D4 MEK500V-40 — D3 MEK500V-40

5V_HSMBCK R192 2.2K_4 — 5V_HSMBDT R191 2.2K_4

C286 *10P/50V_4 — C299 *10P/50V_4

+5V_HDMIC — C309 *0.01U/50V_4

for EMI request

HDMI_SCLK — HDMI_SDATA — +5V_HDMIC — HDMI_HPD — HDMI_DET_C

VC7 *TVM0G5R5M220R — C649 220P/50V_4

CN10 HDMI CONN

C_TX2_HDMI+ — C_TX2_HDMI- — C_TX1_HDMI+ — C_TX1_HDMI- — C_TX0_HDMI+ — C_TX0_HDMI- — C_TXC_HDMI+ — C_TXC_HDMI-

SHELL1 — D2+ — D2 Shield — D2- — D1+ — D1 Shield — D1- — D0+SHELL2 — D0 Shield — D0- — CK+ — CK Shield — CK- SHELL2 — CE Remote — NC — DDC CLK — DDC DATA — GND — +5V — HP DET — SHELL2

For EDP Only: stuff Cap

For LVDS only stuff Resistor

27 TXLCLKOUT+ — TXLCLKOUT+

27 TXLCLKOUT- — TXLCLKOUT-

27 TXLOUT2+ — TXLOUT2+

27 TXLOUT2- — TXLOUT2-

27 INT_eDP_TXP1_R — C37 0.1U/16V_4

27 TXLOUT0+_2136 — R27 *0_4 — TXLOUT0+

27 TXLOUT0-_2136 — R29 *0_4 — TXLOUT0-

27 INT_eDP_TXN1_R — C40 0.1U/16V_4

27 INT_eDP_TXP0_R — C32 0.1U/16V_4

27 TXLOUT1+_2136 — R20 *0_4 — TXLOUT1+

27 TXLOUT1-_2136 — R24 *0_4 — TXLOUT1-

27 INT_eDP_TXN0_R — C34 0.1U/16V_4

27 INT_eDP_AUXN_R — C53 0.1U/16V_4

27 EDIDDATA_2136 — R386 *0_4 — EDIDDATA_R

27 EDIDCLK_2136 — R388 *0_4 — EDIDCLK_R

27 INT_eDP_AUXP_R — C54 0.1U/16V_4

For LVDS Only close CN8

R60 *100K/F_4

27 2136_DPST_PWM — Ra — R57 *0_4 OUT_DPST_PWM

27 2136_LVDS_BLON — Rb — R41 *0_4 OUT_LVDS_BLON

For eDP, close to CN8

2 PCH_LVDS_BLON — R59 0_4 OUT_LVDS_BLON

27 EDP_DPST_PWM — R50 10/F_4 OUT_DPST_PWM

For EDP Only: Reserved

+3V — R385 *100K_4 EDIDDATA_R — R387 *100K_4 EDIDCLK_R

+3V — R52 *1K_4 OUT_DPST_PWM — R71 *1K_4 OUT_LVDS_BLON

EMI Solution

C_TX2_HDMI+ — R166 220/F_4 — C_TX2_HDMI-

C_TX1_HDMI+ — R173 220/F_4 — C_TX1_HDMI-

C_TX0_HDMI+ — R177 220/F_4 — C_TX0_HDMI-

C_TXC_HDMI+ — R184 220/F_4 — C_TXC_HDMI-

C_IN_CLK — R183 0_4 — C_TXC_HDMI+

C_IN_CLK# — R188 0_4 — C_TXC_HDMI-

+5V — 40 mils — F1 H=1.4mm(Max) FUSE1A6V_POLY — +5V_HDMIC

C310 0.1U/16V_4

VC1 *TVM0G5R5M220R — SSM14 spec is 40V 1A

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM/D-MIC	1A

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Audio Codec

Close to PIN9

>40mils trace

Close to PIN27

Close to PIN38

Close to PIN21

Close to PIN25

TO Digital MIC

SI Add

General MODE	3D Camera MODE
Stuff R611,R612	Stuff R613,R614

U13 Analog / Digital

TO Headphone jack

TO Audio Jack MIC

Close to Pin 35

Close to Pin 22

Close to codec

Close to Pin 39

Close to Pin 45

Vset=1.242V

check value

Check layout mount location

Speaker 4 ohm: 40mils

Close to CN4

INT SPEAKER CONN

Close to CODEC

place to near U1000 or under U1000

SI Modify

CN12 COMBOJACK_6P

PROJECT : X1B-10L

Quanta Computer Inc.

NB5

Size: Custom | Document Number: Audio Codec | Rev: 1A

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Head Phone out

Add 1uF caps for the AC coupling. (IDT recommend)

PV Change

Placement close the CODEC (U13)

TPA6133A2

HPA022642RTJR

If Don't Use AMP need install

HPOUT_L R277 *0_4 LINEOUT_L_C → LINEOUT_L_C 29

HPOUT_R R294 *0_4 LINEOUT_R_C → LINEOUT_R_C 29

+3V 2,4,10,11,12,13,14,15,16,17,18,20,27,28,29,31,32,33,34,35,41,43,44

+5V 28,29,31,32,33,34,43

+5VSS 4,32,33,37,38,39,40,41,42,43,44,45,46

+3VPCU 6,13,31,32,33,34,35,36,37

+3VLANVCC 32,43

HOLE

1020
Change H2 Footprint from
H-TC236BC315D110P2 to H-C236D110P2

CPU

H6 *INTEL-BKT-SHARK-ULT

H12 *H-C236D110P2

H1 *O-Y16X-4

H2 *H-TC236BC315D110P2

GPU

H7 *H-TC276BC197D146P2

H9 *H-TC276BC197D146P2

H4 *H-C315D157P2

H8 *H-TC315BC276D157P2

H5 *H-TC236BC276D118P2

H10 *H-TC236BC315D118P2

H11 *H-TC236BC315D118P2

H13 H-TC197BC102D102P2

H3 *H-C98D98N

PAD4 *spad-re197x394np

PAD2 *O-Y16X-3

PAD1 *SPAD-RE315X157NP

EC21 *Clamp-Diode

R168 *64.9K/F_6

PAD3 *spad-y11x-1np

10112 Add Pad4 Footprint *spad-y11x-1np

PAD5 *spad-c157np

PAD6 *spad-c157np

PAD7 *spad-x1b-1np

DB Add

1119 H15 disconnect to GND

SI Del USB Co_Layout Resistance

DEEP_PWRLED#

HD_EC#

NBSWON1#

C7 *220P/50V_4

C16 *220P/50V_4

C15 *220P/50V_4

+5VSS C51 *0.1U/16V_4

+3VPCU C35 *0.1U/16V_4

+3VLANVCC C39 *0.1U/16V_4

+3V C43 *0.1U/16V_4

+3VPCU R3 10K_4

DEEP_PWRLED# → Q2 DRC5144E0L

PWR_LED# → PWR_LED# 35

C1 0.1U/16V_4

SI Change

MCM2012B900GBE L5

MCM2012B900GBE L7

USBP2+ USBP2- USB30_TX3+ USB30_TX3- USB30_RX3+ USB30_RX3- USBP6+ USBP6-

PCIE_CLKREQ_CR# PCIE_CLKREQ_LAN# PLTRST# PCIE_WAKE# USBPW_ON# NBSWON1# LID_EC# DEEP_PWRLED#

+3VPCU +3VLANVCC +3V +5VSS

LAN_XTAL25_IN

PCIE_TXP9_LAN PCIE_TXN9_LAN CLK_PCIE_LANP CLK_PCIE_LANN PCIE_RXP9_LAN PCIE_RXN9_LAN PCIE_TXP5_CARD PCIE_TXN5_CARD CLK_PCIE_CRP CLK_PCIE_CRN PCIE_RXP5_CARD PCIE_RXN5_CARD

CN1 Card LAN 55P

PROJECT :	X1B-10L
Quanta Computer Inc.	
Size: C	Document Number: Card Reader
Rev: 1A	
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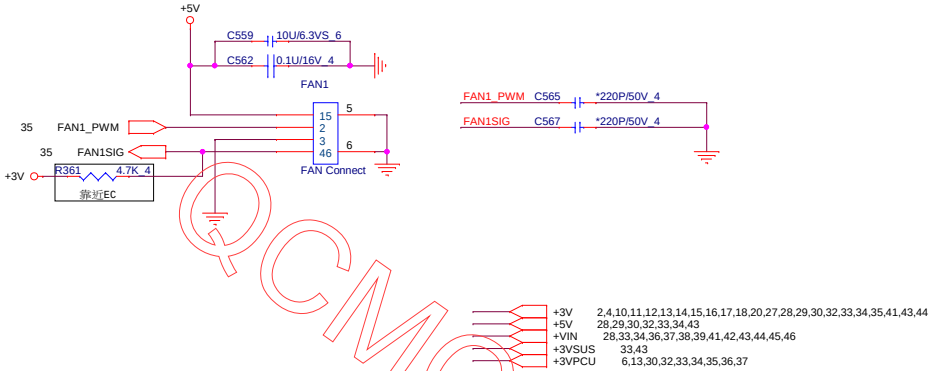
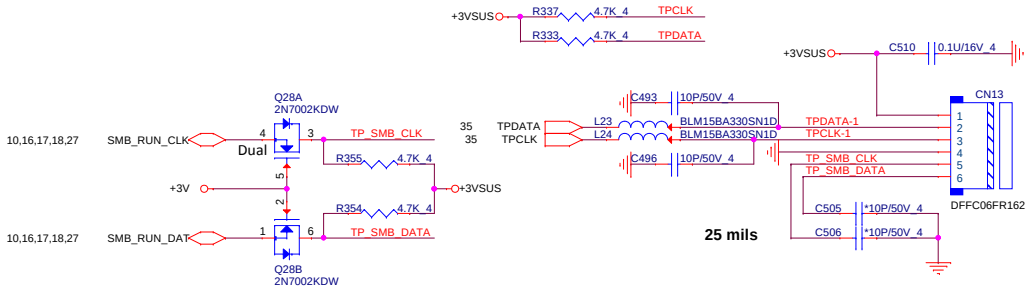
NB5

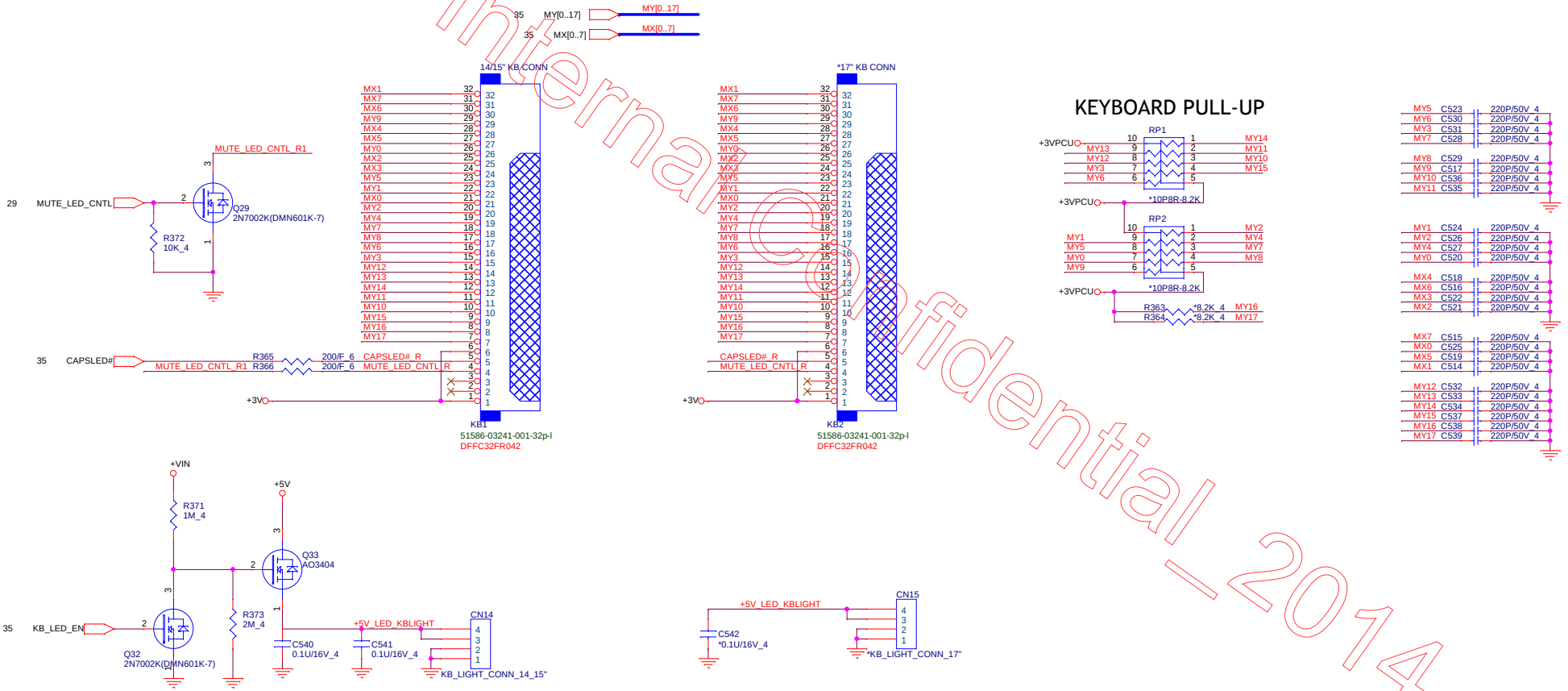
FAN



Touch Pad Connector



KEYBOARD Con.



NB5	PROJECT : X1B-10L Quanta Computer Inc.	
Size Custom	Document Number PB/TP/KB/FAN/EMI Cap	Rev 1A
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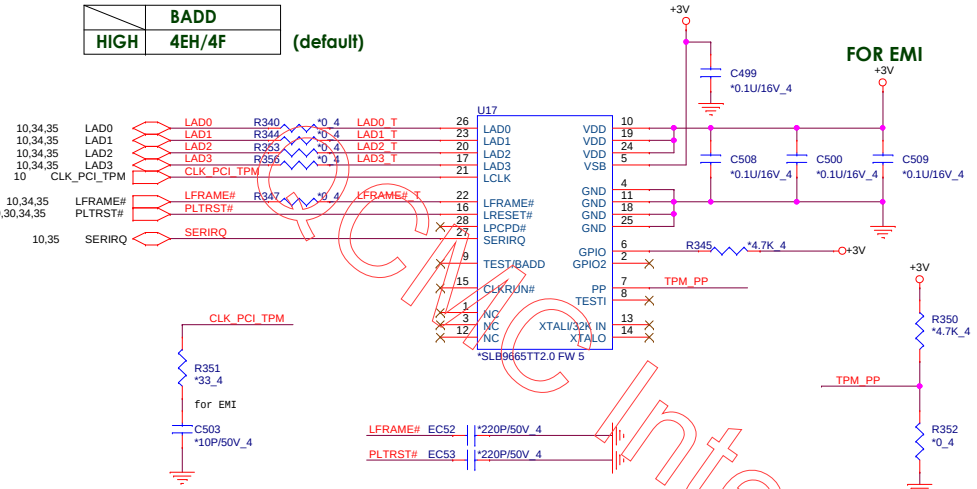
TPM (2.0)

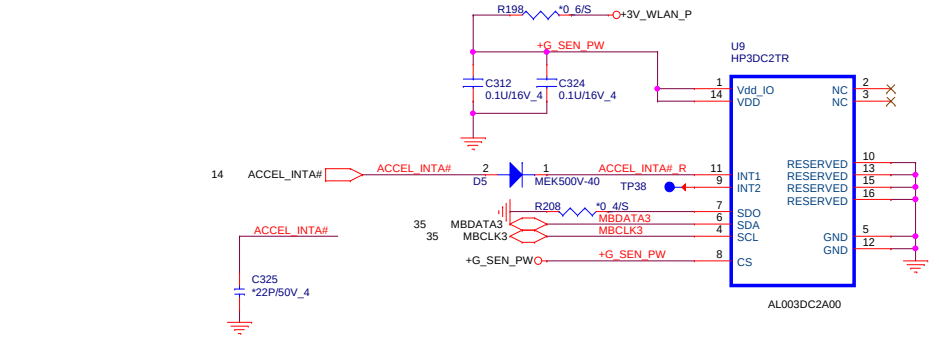
Address

	BADD
HIGH	4EH/4F (default)

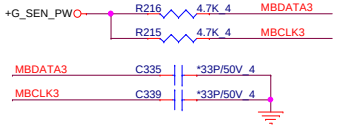


Accelerometer Sensor

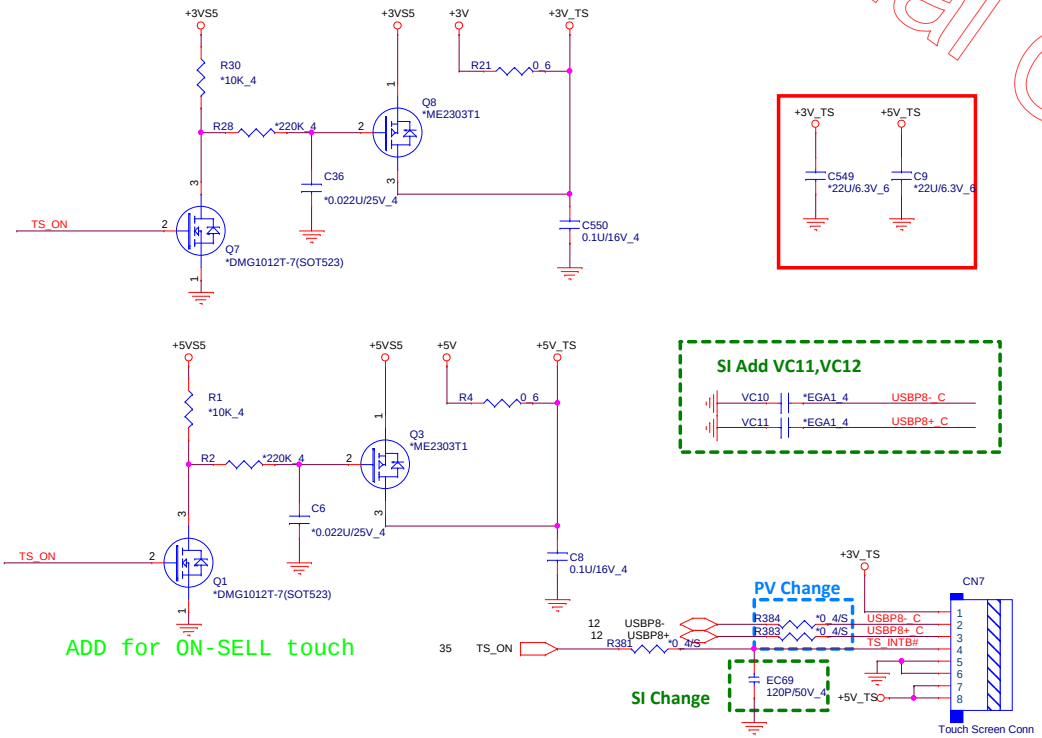
G-Sensor Power need check



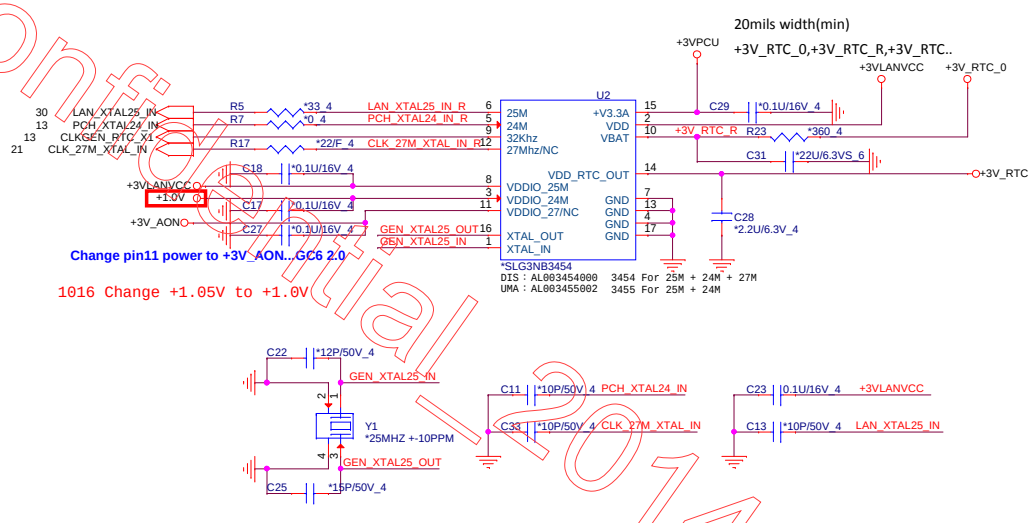
+3V 2,4,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,33,34,35,41,43,44
+1.0V 2,4,6,16,35,40
+3VS5 4,10,15,16,34,35,37,39,40,43,46
+5VS5 4,30,33,37,38,39,40,41,42,43,44,45,46
+3VPCU 6,13,30,31,33,34,35,36,37
+3V_RTC 4,13,15
+3V_AON 19,21,22,46
+3V_RTC_0 13
+3VLANVCC 30,43
+3V_WLAN_P 34



Touch screen



Green CLK Circuitry



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Size: Custom	Document Number: TPM/G-Sensor/G-CLK/TS/FP	Rev: 1A
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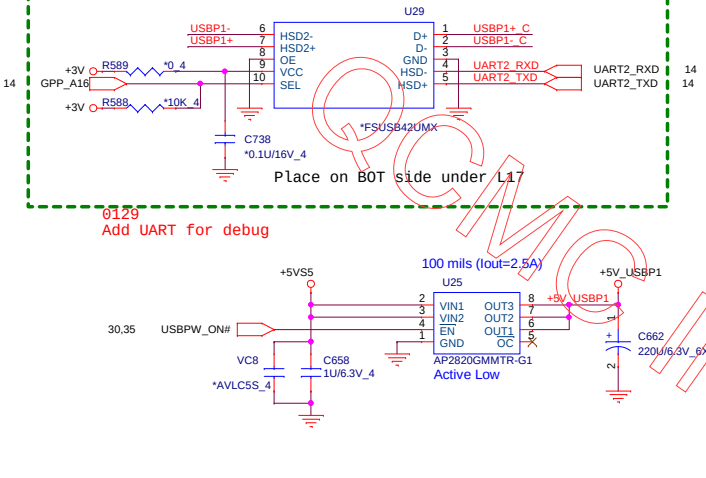
USB 2.0/3.0 Combo

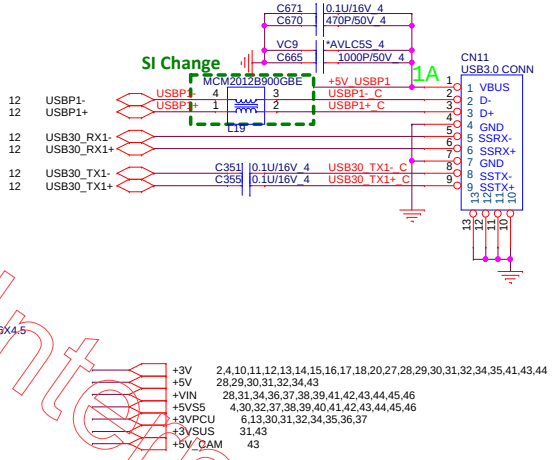
UART for DEBUG

SI Add



SI Del USB Co_Layout Resistance

SI Change

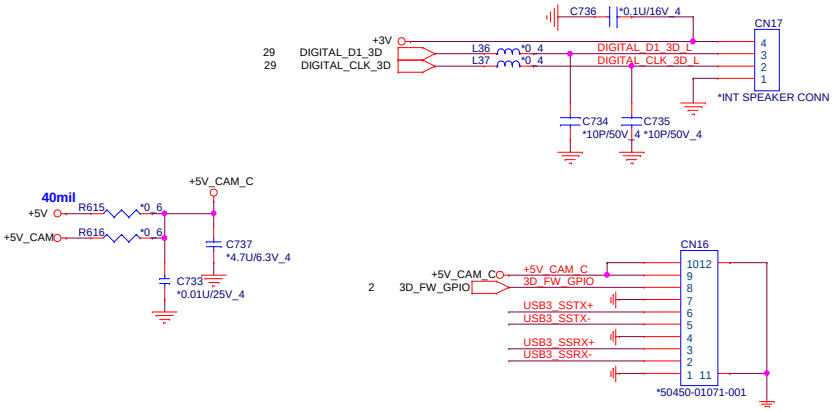


+3V	2,4,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,34,35,41,43,44
+5V	28,29,30,31,32,34,43
+VIN	28,31,34,36,37,38,39,41,42,43,44,45,46
+5VS5	4,30,32,37,38,39,40,41,42,43,44,45,46
+3VPCU	6,13,30,31,32,34,35,36,37
+3VSUS	31,43
+5V_CAM	43

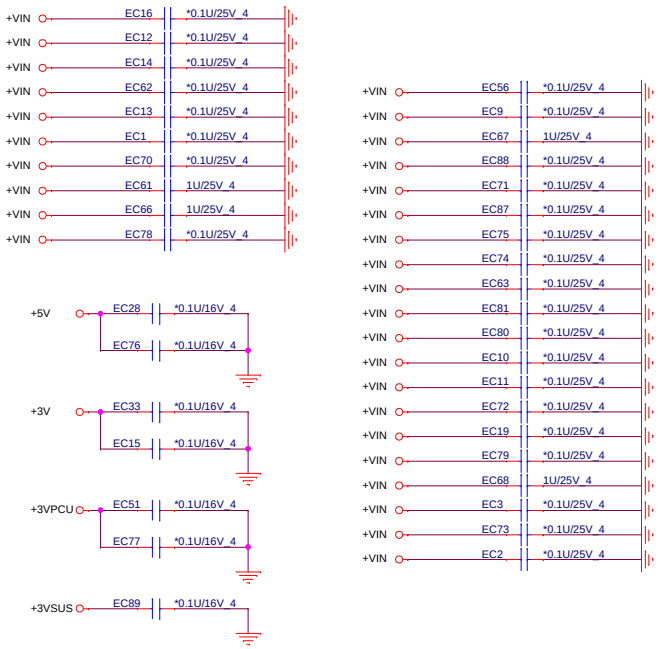
3D CAMERA

3D Camera Conn.

SI Add 3D Camera Function

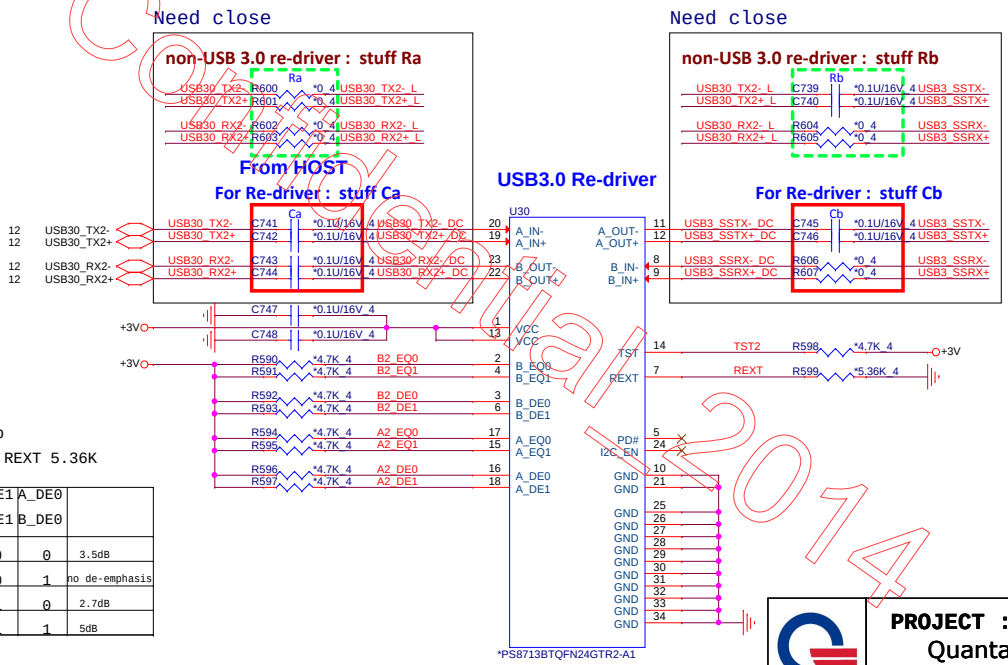


EMI CAP



USB3.0 re-driver for 3D CAMERA

SI Add



AEQ 9.5db / ADE 3.5db

BEQ 13db / BDE 5db / REXT 5.36K

A_EQ1	A_EQ0		A_DE1	A_DE0	
B_EQ1	B_EQ0		B_DE1	B_DE0	
0	0	9.5dB	0	0	3.5dB
0	1	13dB	0	1	no de-emphasis
1	0	4.5dB	1	0	2.7dB
1	1	7.5dB	1	1	5dB

TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing

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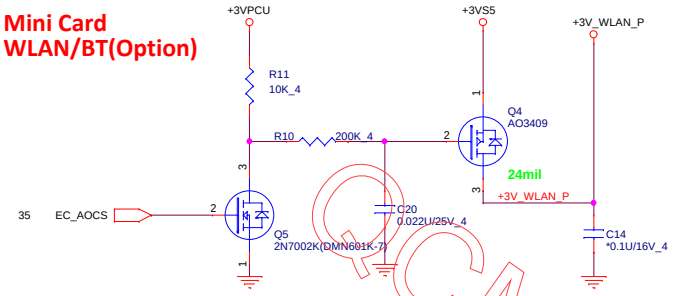
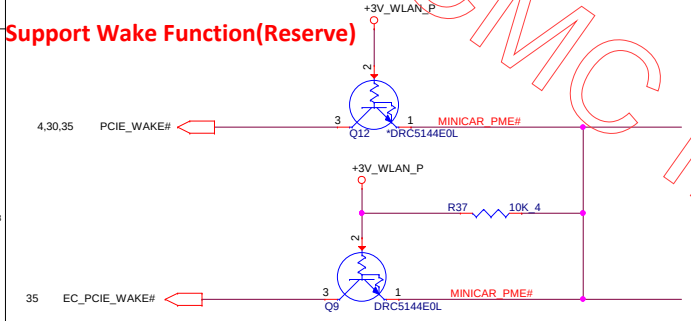
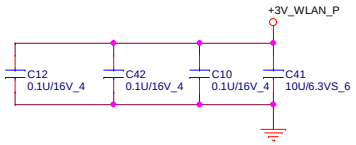
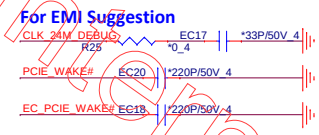
Mini Card WLAN/BT(Option)

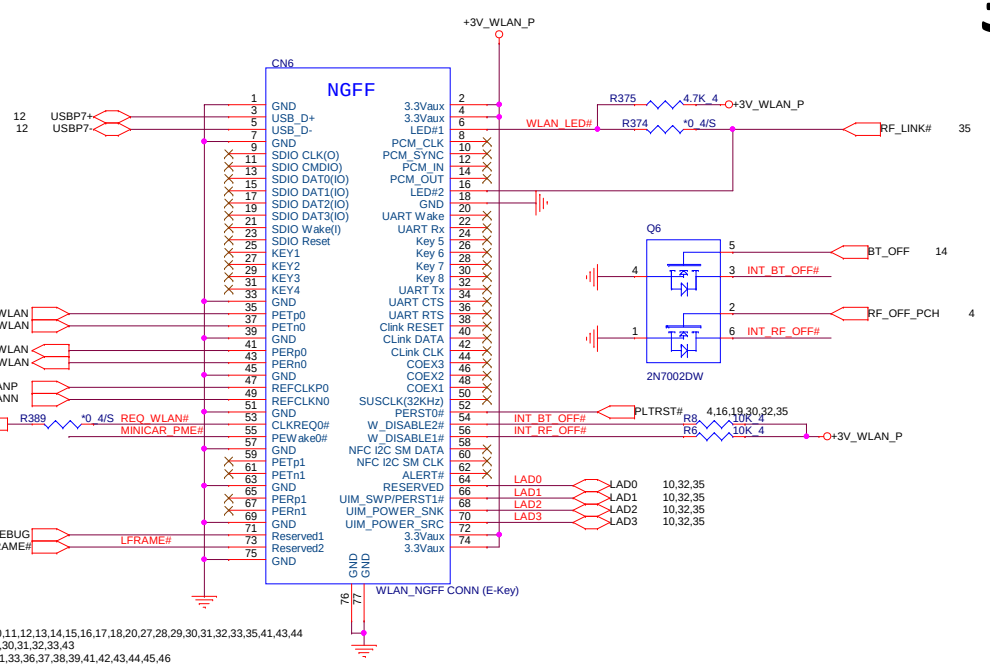


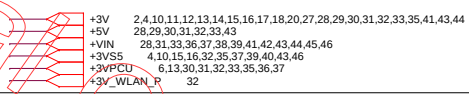
Support Wake Function(Reserve)





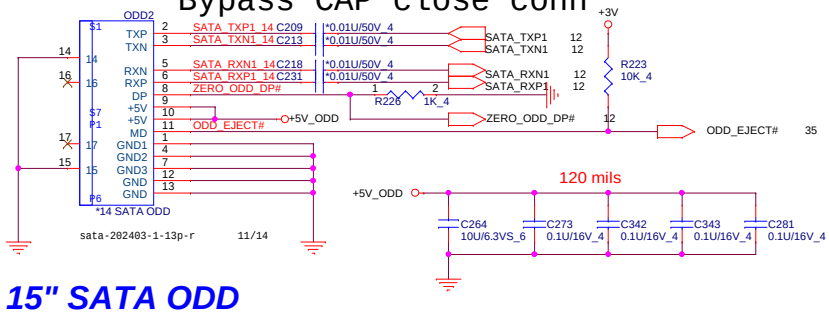




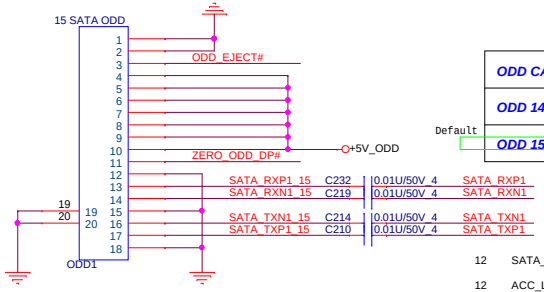


14" SATA ODD

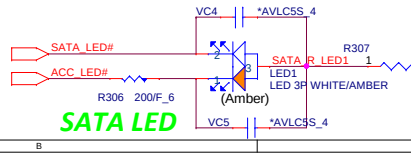
Bypass CAP close conn



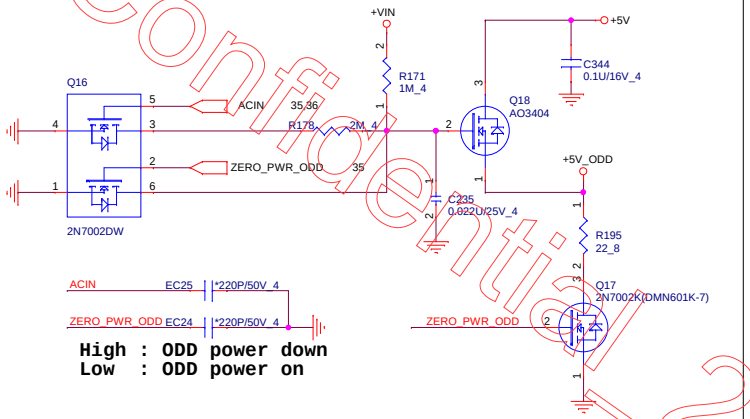
15" SATA ODD



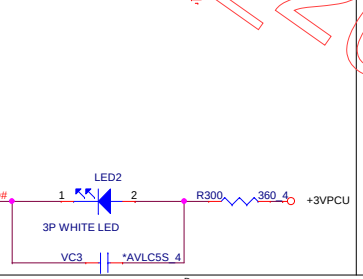
ODD CAP Setting	C209/C213/C218/C231	C210/C214/C219/C232
ODD 14"	O	X
Default ODD 15"/17"	X	O



SATA LED

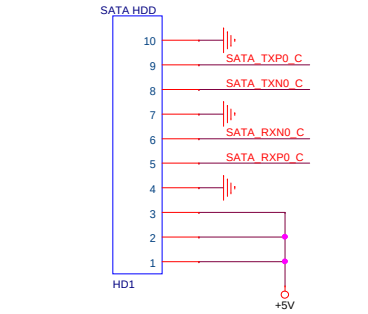


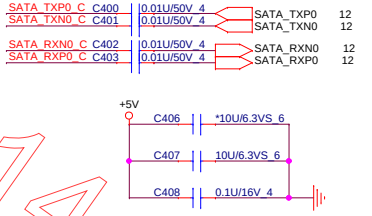
High : ODD power down
Low : ODD power on



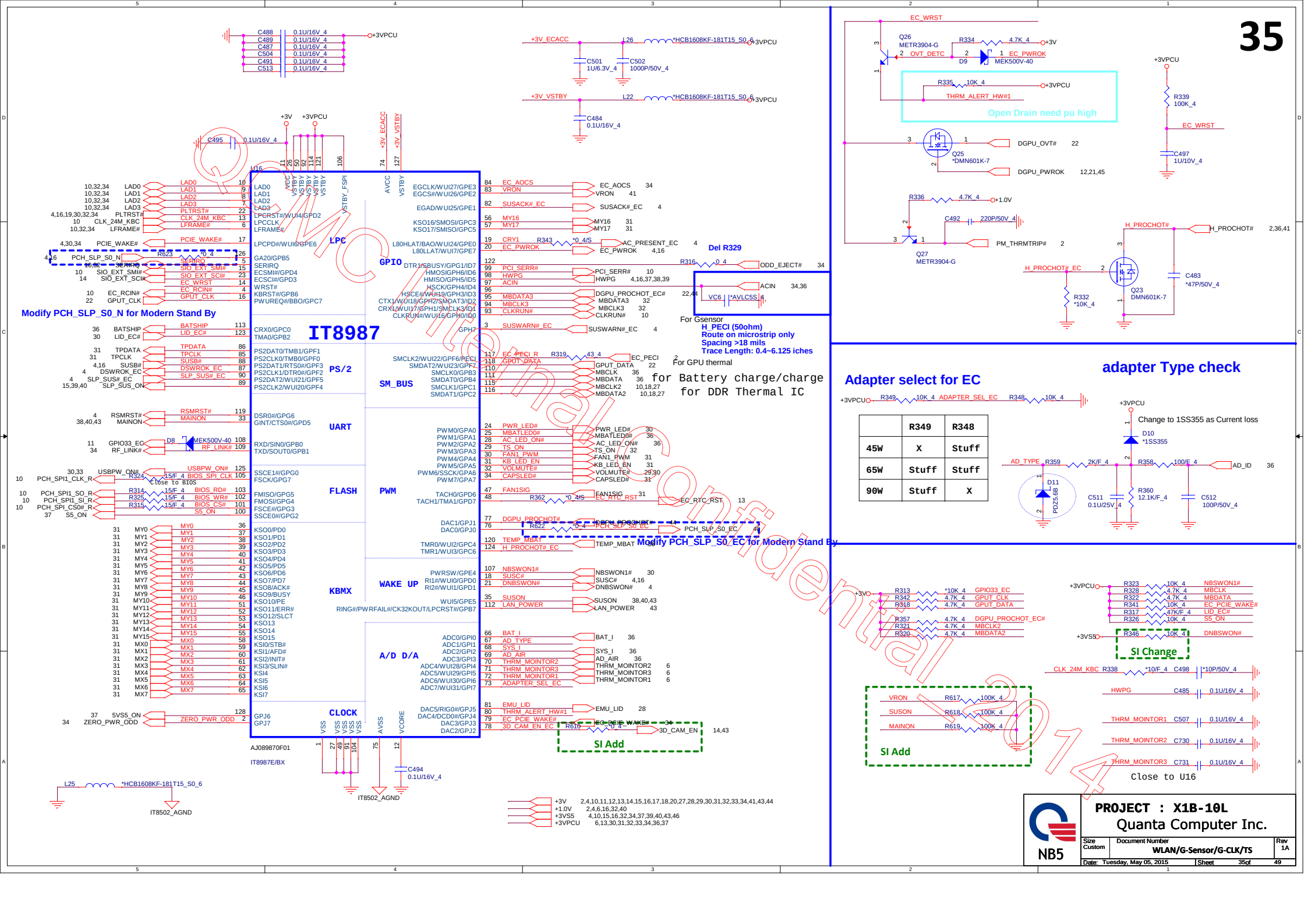
PWR LED

HDD





NB5	PROJECT : X1B-10L Quanta Computer Inc.	
Size Custom	Document Number WLAN/NGFF/MSATA	Rev 1A
Date: Tuesday, May 05, 2015	Sheet 34 of 49	



	R349	R348
45W	X	Stuff
65W	Stuff	Stuff
90W	Stuff	X

DC_JACK
90W

Do Not add test pad on BATDIS_G signal

14"

2015/4/29 updated

Place this ZVS close to Diode away +VIN

Place this ZVS close to Far-Far away +VIN

For EMI

For ISN

Place this cap close to EC

ACDET=14.985V

VIDCHG = 8 or 16 × (VSRN – VSRP)

BQ24780SRUYR

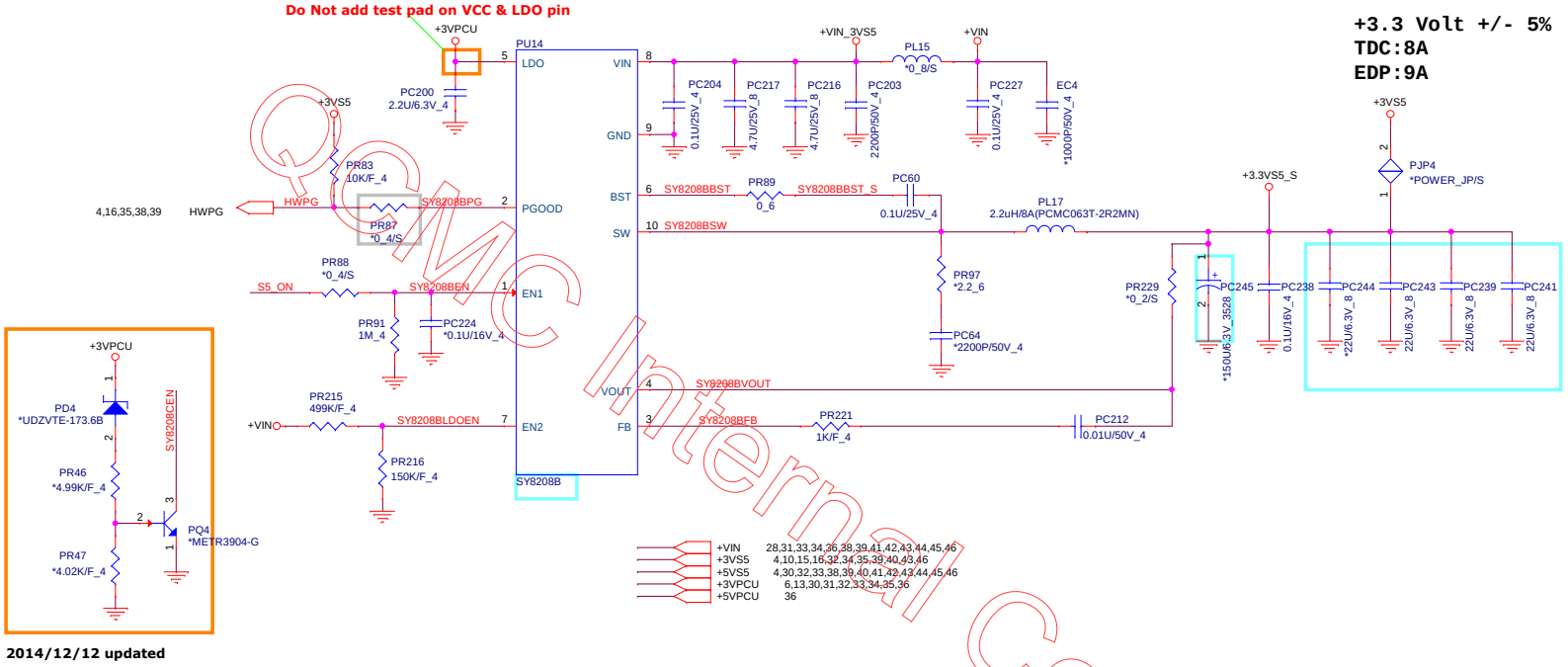
15"

17"

2015/4/29 updated

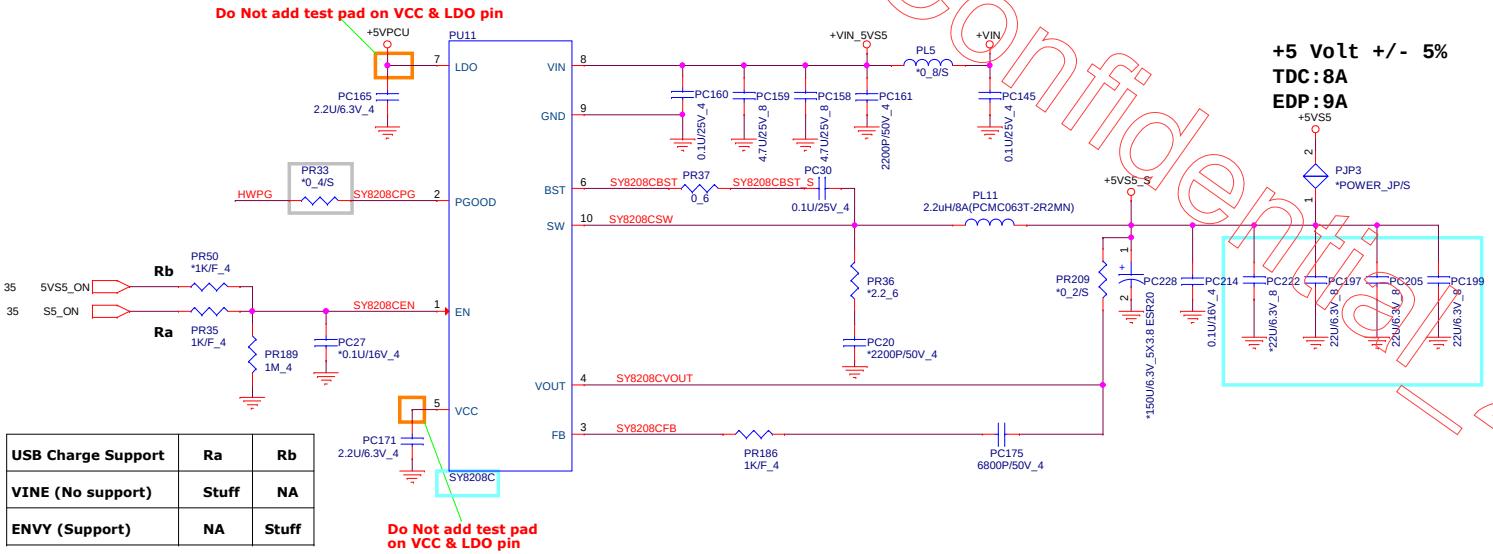
+VIN 28,31,33,34,37,38,39,41,42,43,44,45,46
+3VPCU 6,13,30,31,32,33,34,35,37
+5VPCU 37

NB5	PROJECT : X1B-10L Quanta Computer Inc.	
Size Custom	Document Number Charger (BQ24780)	Rev 1A
Date: Tuesday, May 05, 2015	Sheet 36 of 49	



+3.3 Volt +/- 5%
TDC:8A
EDP:9A

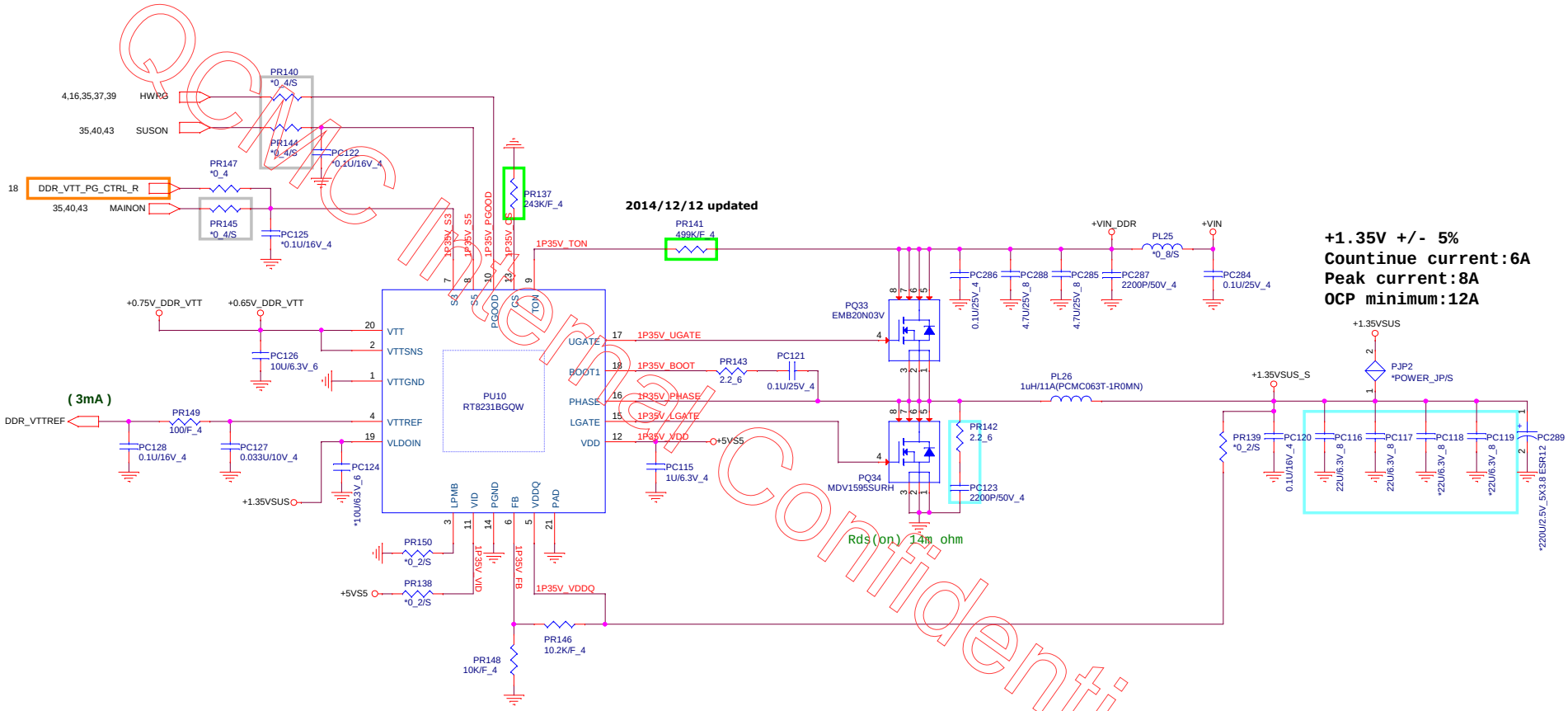
2014/12/12 updated



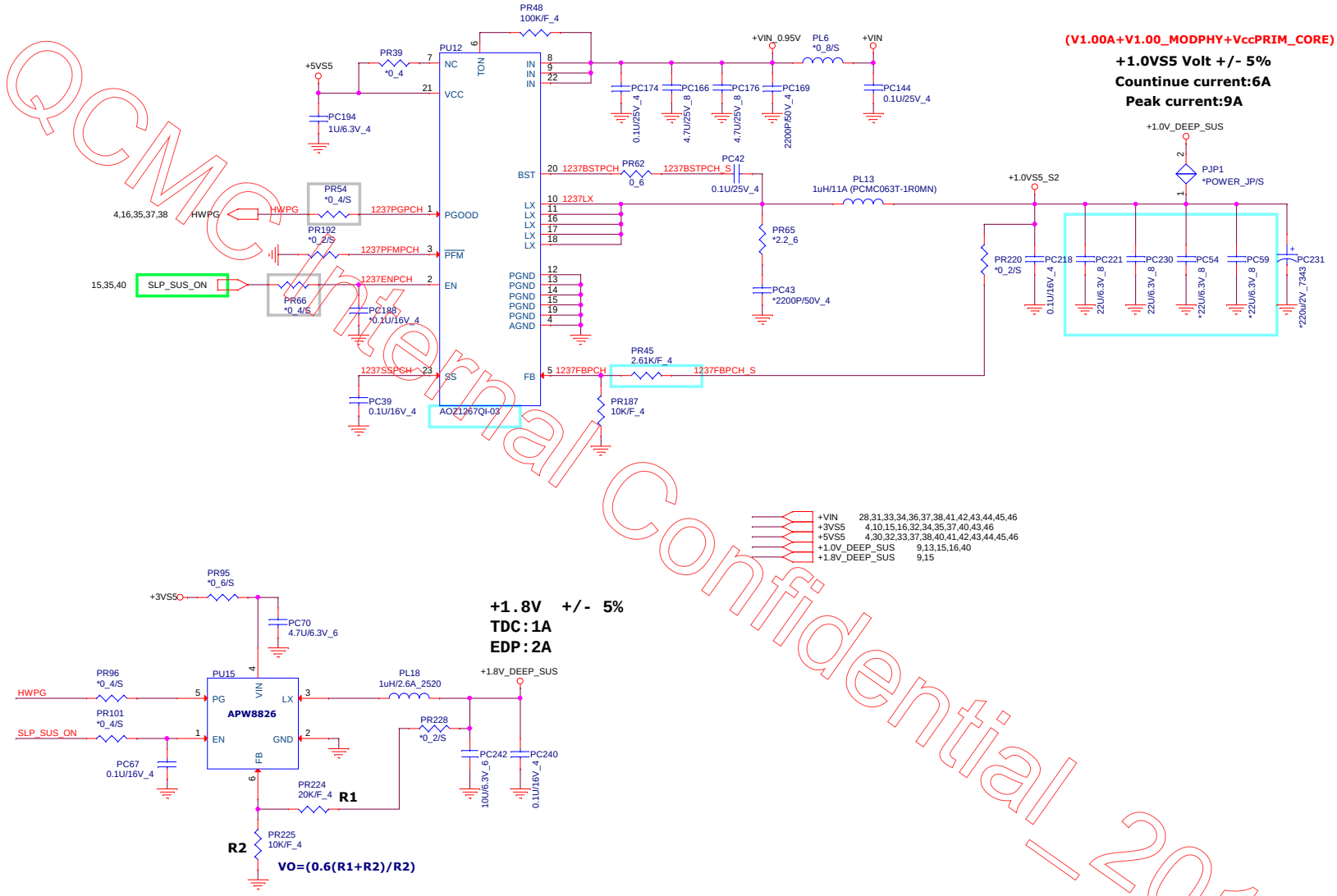
+5 Volt +/- 5%
TDC:8A
EDP:9A

USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

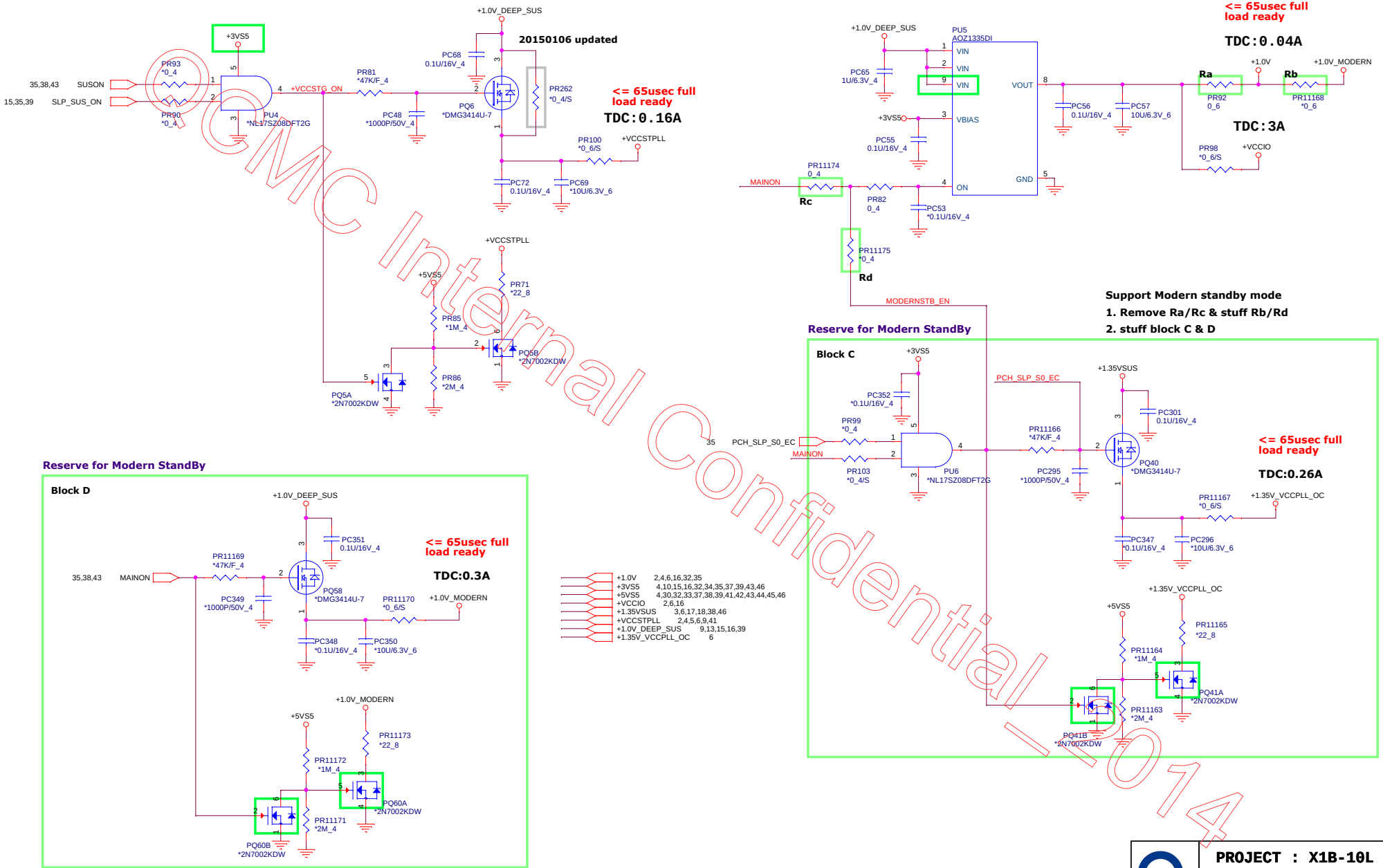
+VIN 28,31,33,34,36,37,39,41,42,43,44,45,46
+5VS5 4,30,32,33,37,39,40,41,42,43,44,45,46
+1.35VSUS 3,6,17,18,40,46
+0.65V_DDR_VTT 17,18



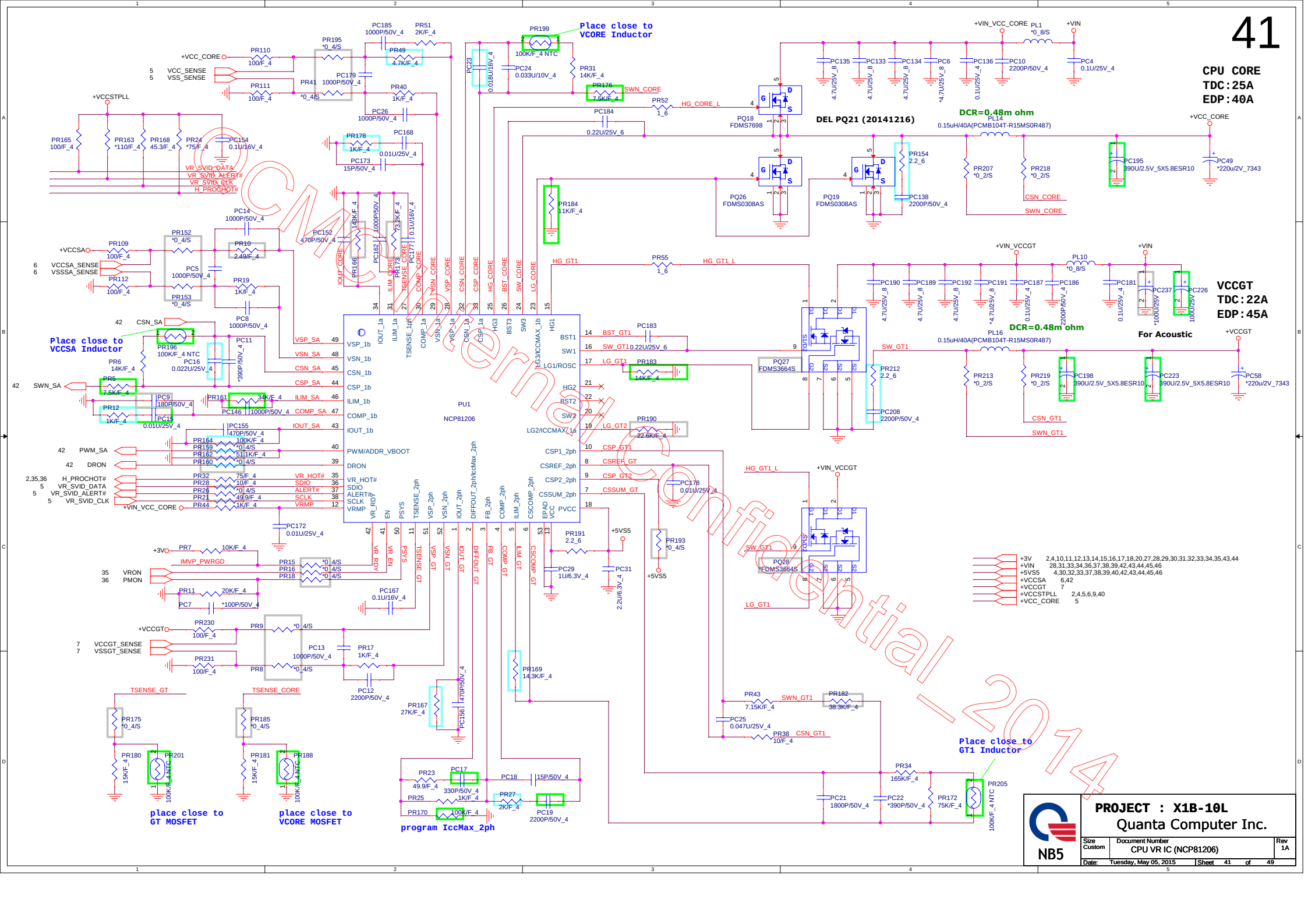
PROJECT :	X1B-10L
	Quanta Computer Inc.
Size	Document Number: DDR3 (RT8231B)/1.8VS5
Rev	1A
NB5	Tuesday, August 05, 2015
Sheet	38 of 49

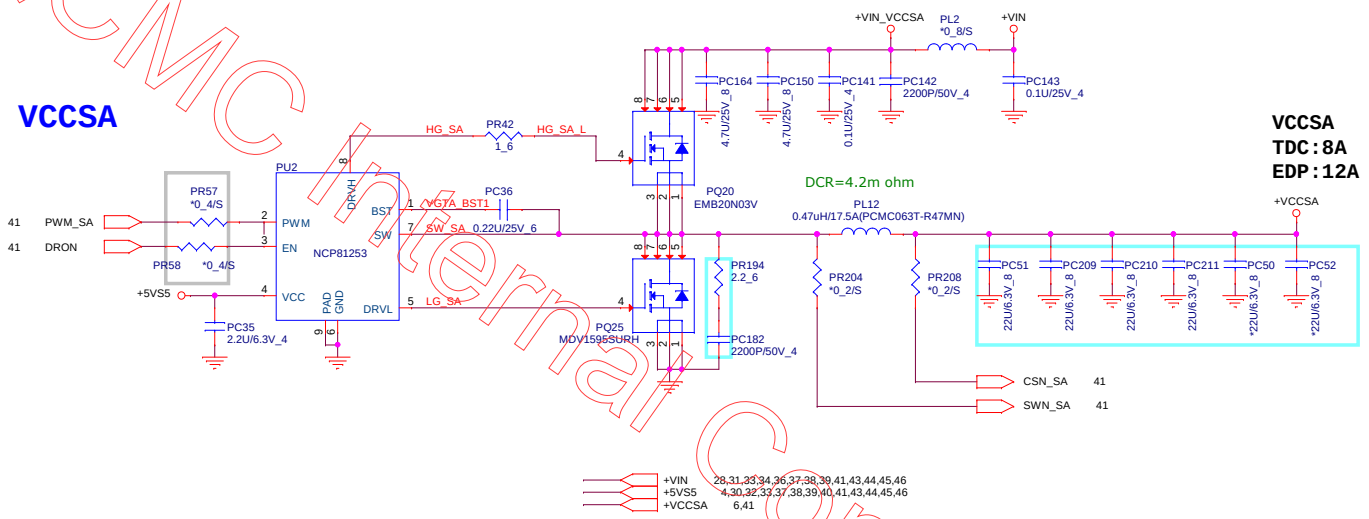


PROJECT : X1B-10L	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: +1.1VS5 (RT8228)/2.5V; Rev: 1A
Date: Tuesday, May 05, 2015	Sheet 39 of 49



NB5	PROJECT : X1B-10L Quanta Computer Inc.	
Size Custom	Document Number +1.0V/+VCCSTPLL	Rev 1A
Date: Wednesday, May 06, 2015	Sheet 40 of 49	


41
CPU CORE
TDC:25A
EDP:40A
DCR=0.48m ohm
DEL PQ21 (20141216)
VCCGT
TDC:22A
EDP:45A
For Acoustic
Place close to VCORE Inductor
Place close to VCCSA Inductor
Place close to GT1 Inductor
place close to GT MOSFET
place close to VCORE MOSFET
program IccMax_2ph
NCP81206
PU1
Compal Confidential
PROJECT : X1B-10L
Quanta Computer Inc.
NB5
CPU VR IC (NCP81206)
Tuesday, May 05, 2015



NB5

PROJECT : X1B-10L

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	1A

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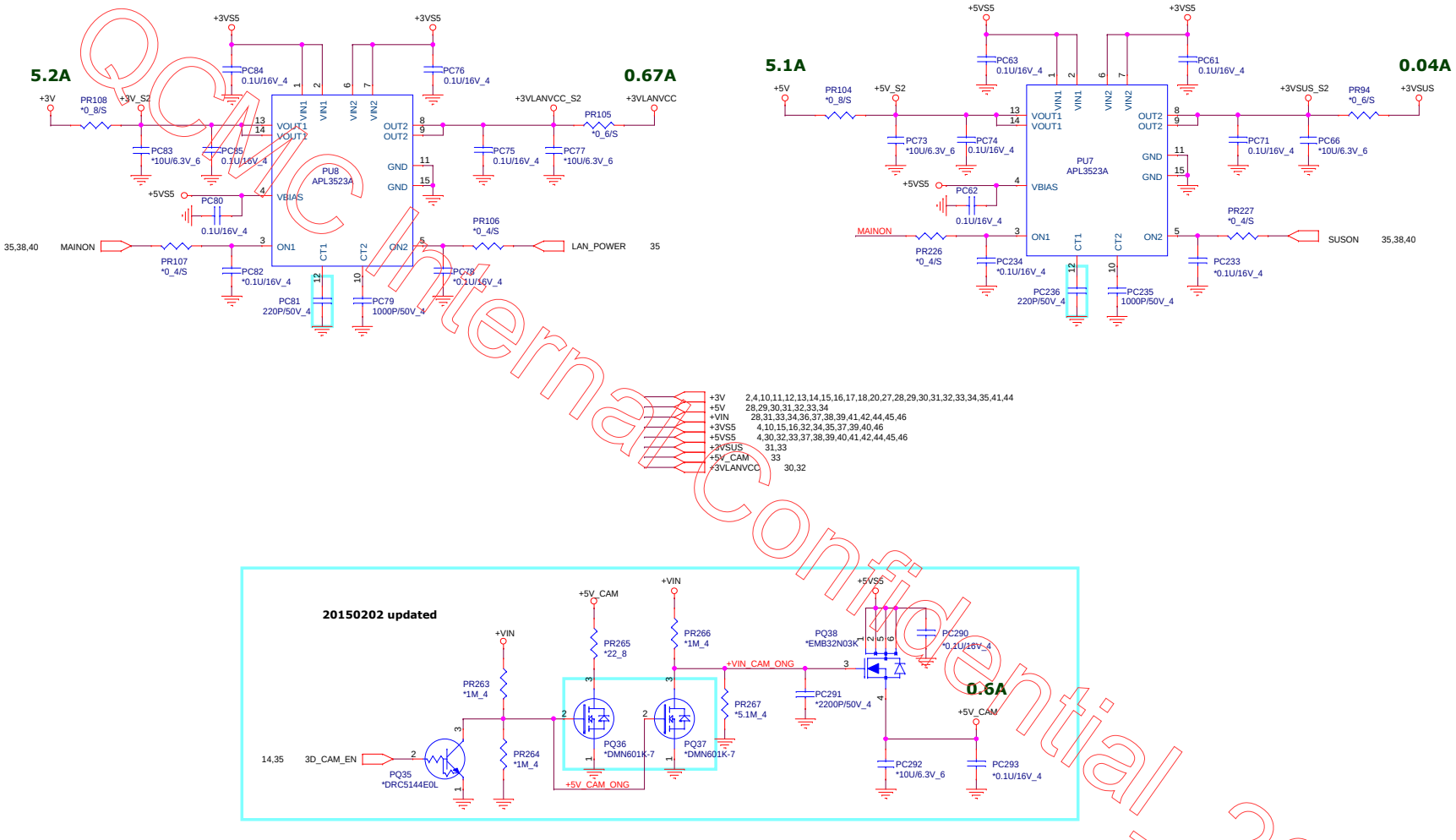

+3V 2,4,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,44
+5V 28,29,30,31,32,33,34
+VIN 28,31,33,34,36,37,38,39,41,42,44,45,46
+3VS5 4,10,15,16,32,34,35,37,39,40,46
+5VS5 4,30,32,33,37,38,39,40,41,42,44,45,46
+3VSUS 31,33
+5V_CAM 33
+3VLANVCC 30,32

NB5

PROJECT : X1B-10L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448)	1A

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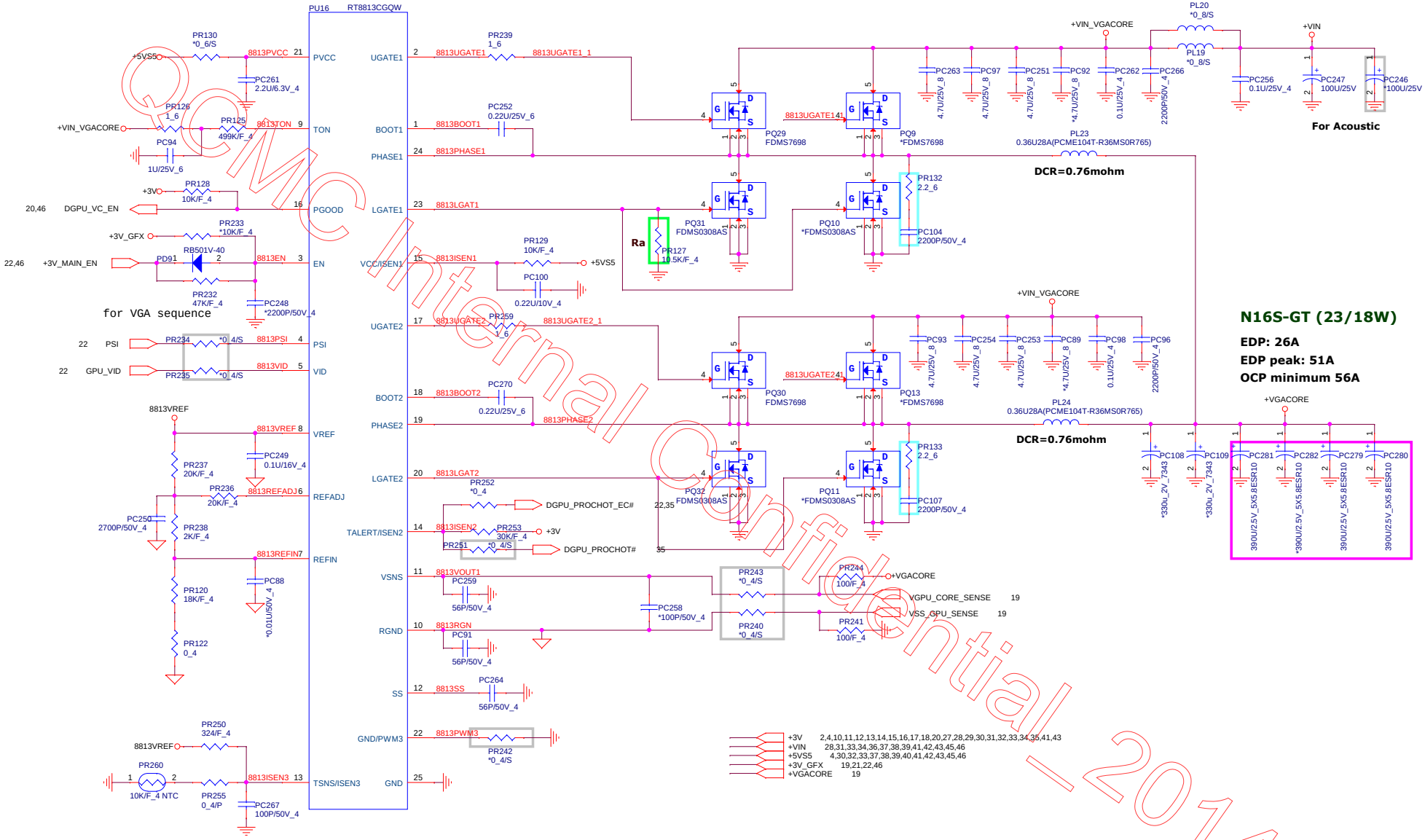
VGA Core



NB5	PROJECT : X1B-10L Quanta Computer Inc.	
Size: Custom	Document Number: +VGACORE (RT8813A)	Rev: 1A
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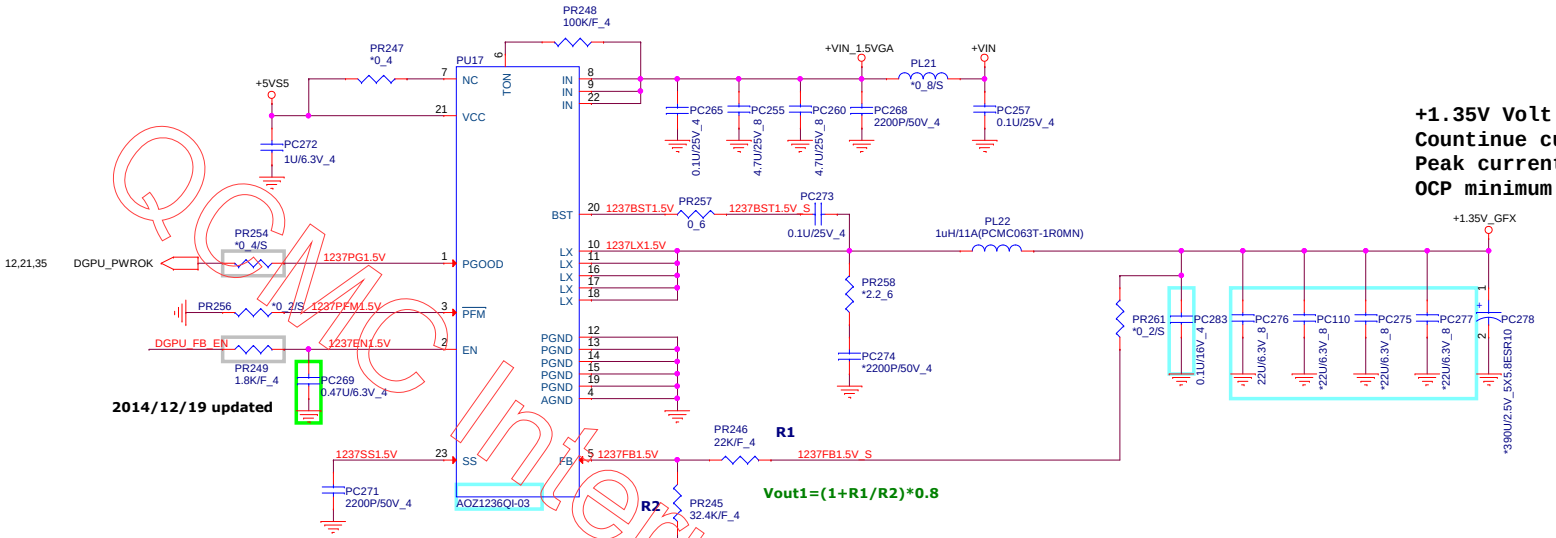
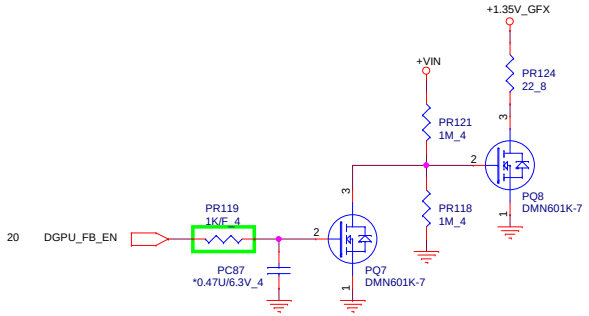


+1.35V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A

+VIN	28,31,33,34,36,37,38,39,41,42,43,44,46
+5VS5	4,30,32,33,37,38,39,40,41,42,43,44,46
+1.35V_GFX	20,21,23,24,25,26



PROJECT : X1B-10L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.35V_VGA(AOZ1237)	1A

NB5

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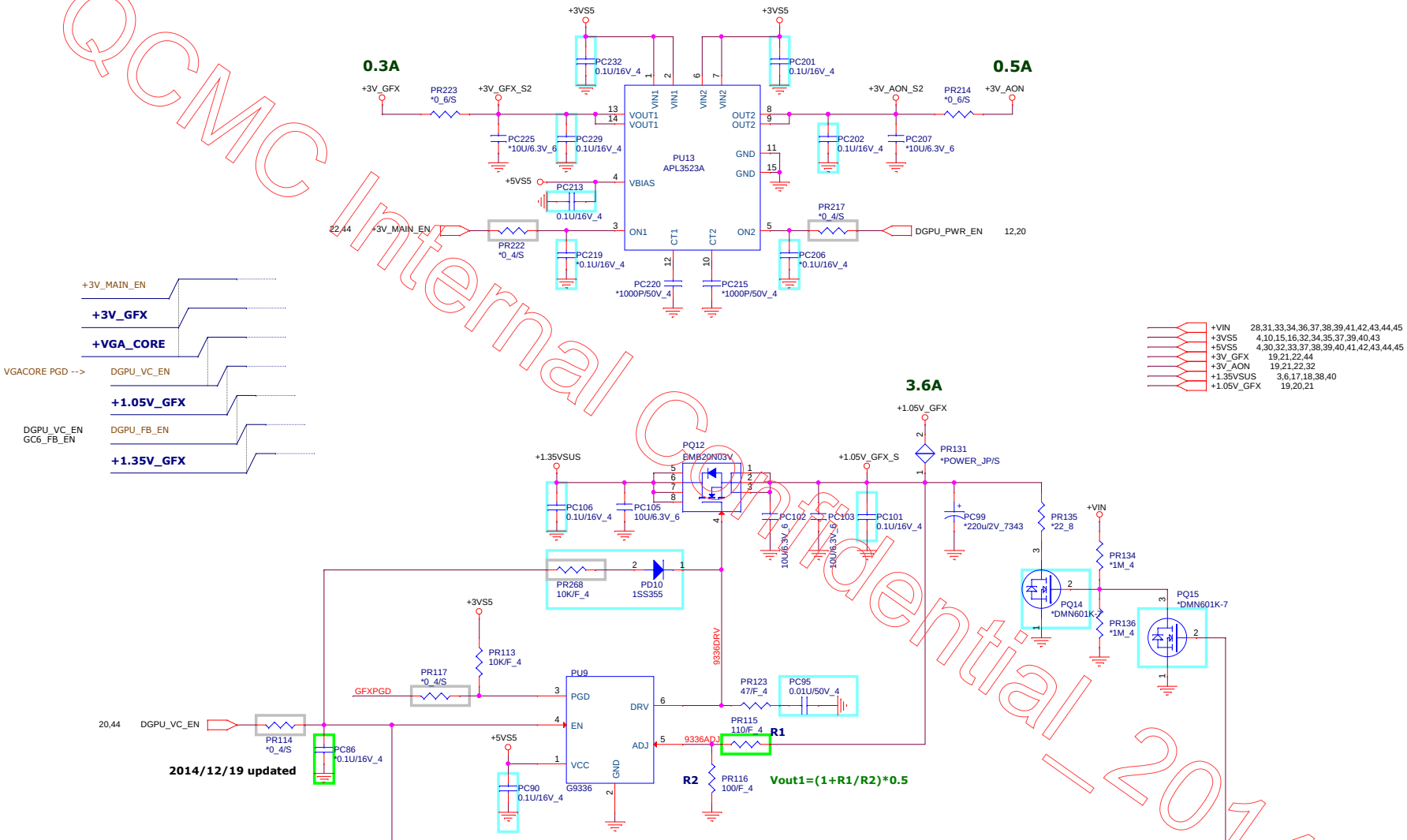
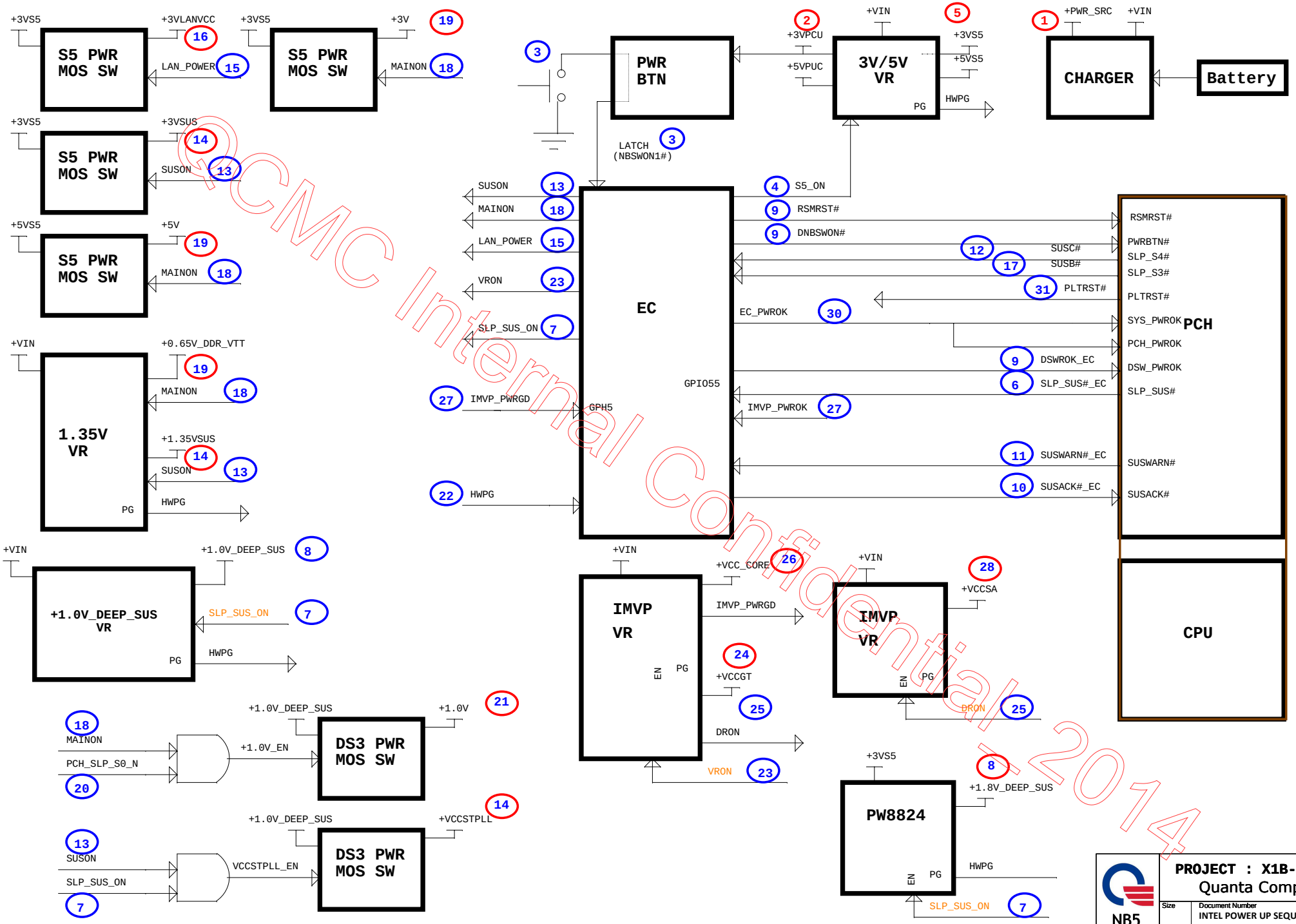
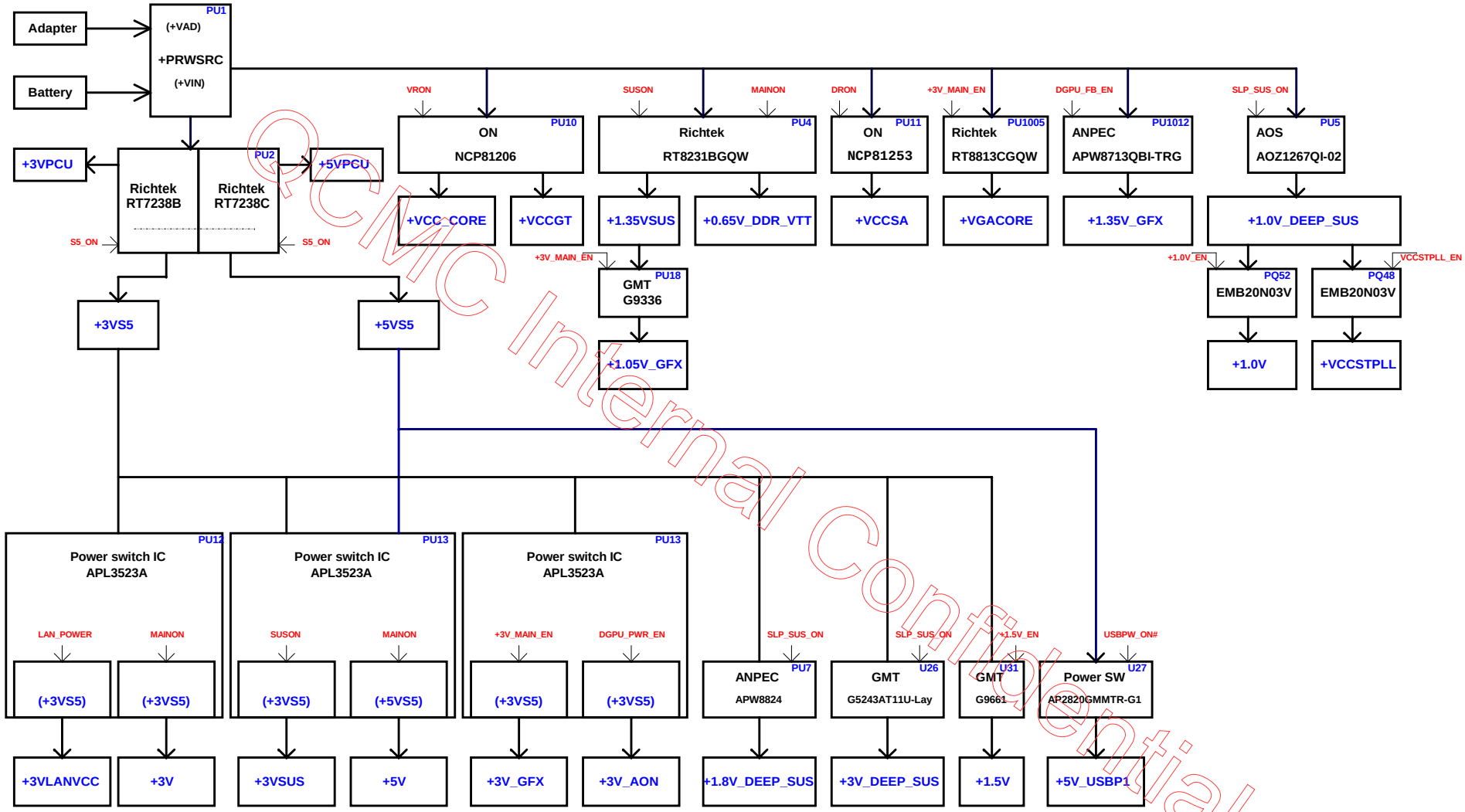


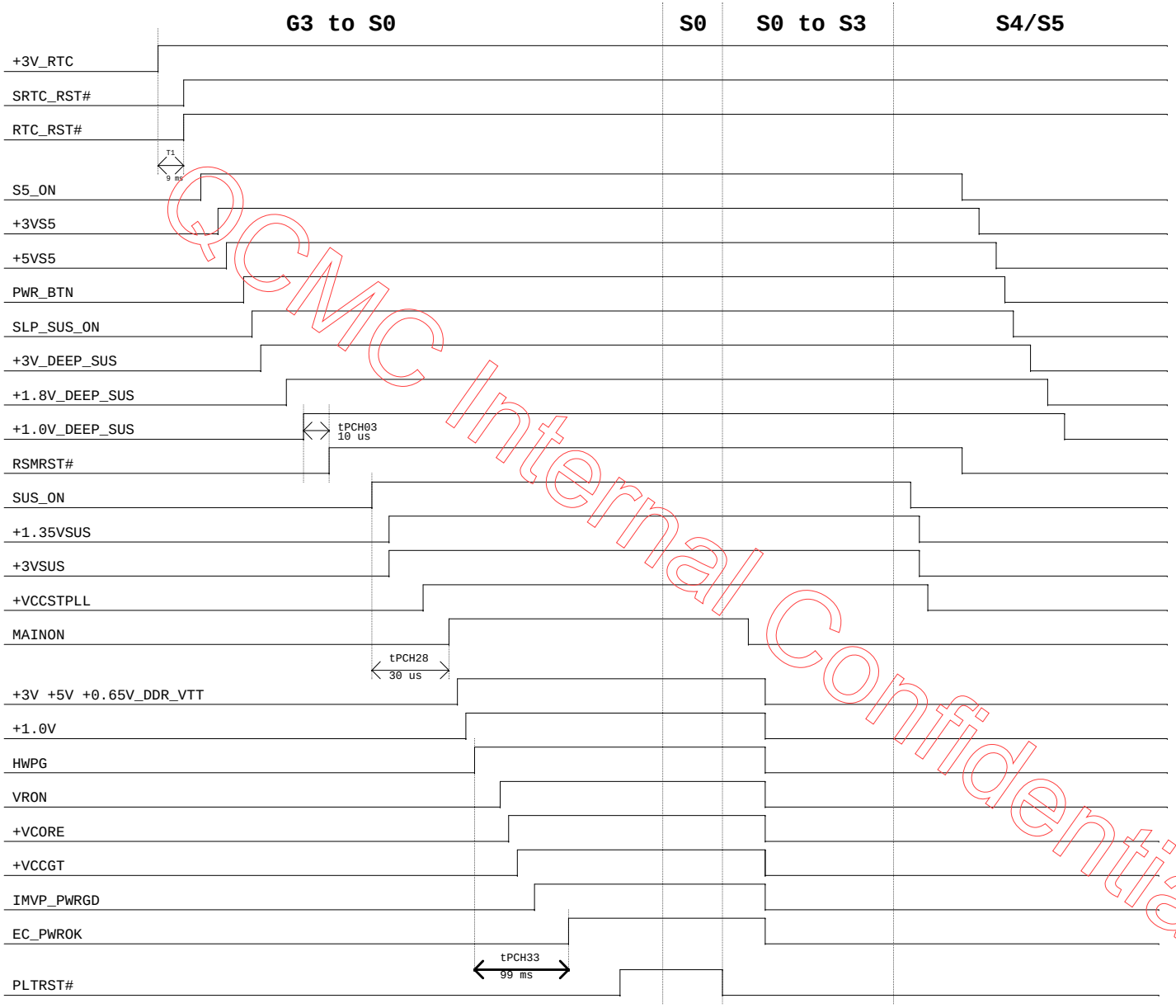
Quanta Computer Inc.	PROJECT : X1B-10L	
NB5	Size: Custom	Document Number: 1.05V_VGA/3V_VGA — Rev: 1A
	Date: Tuesday, May 05, 2015	Sheet 46 of 49



NB5	PROJECT : X1B-10L Quanta Computer Inc.	
Size	Document Number INTEL POWER UP SEQUENCE	Rev 1A
Date: Tuesday, May 05, 2015	Sheet 47 of 49	



PROJECT : X1B-10L
Quanta Computer Inc.
NB5
Size | Document Number: Power Block Diagram | Rev 1A
Date: Tuesday, May 05, 2015 | Sheet 48 of 49



NB5	PROJECT : X1B-10L Quanta Computer Inc.	
	Size:	Document Number: Intel POWER UP SEQUENCE — Rev: 1A
	Date: Tuesday, May 05, 2015	Sheet 49 of 49