
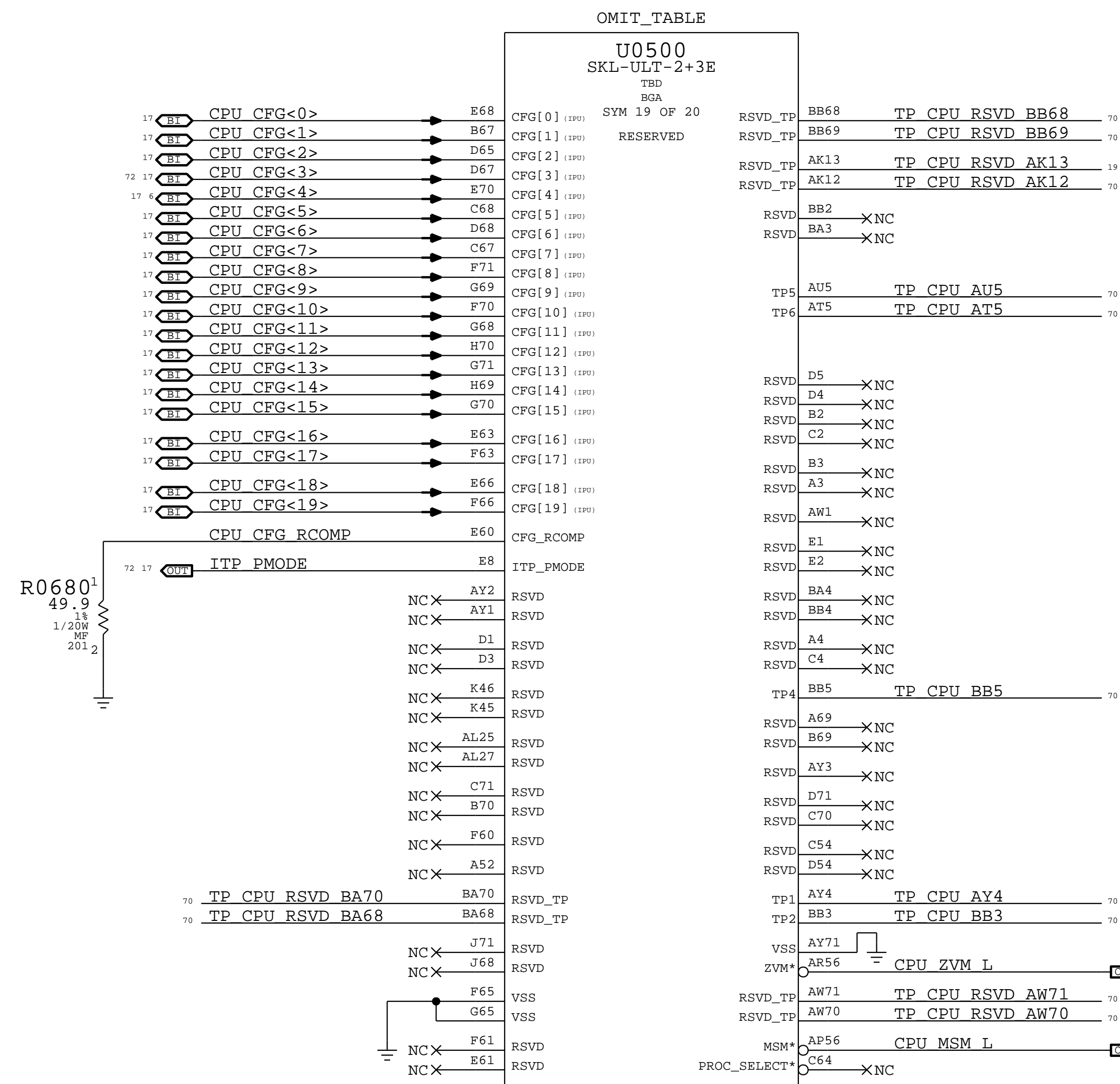
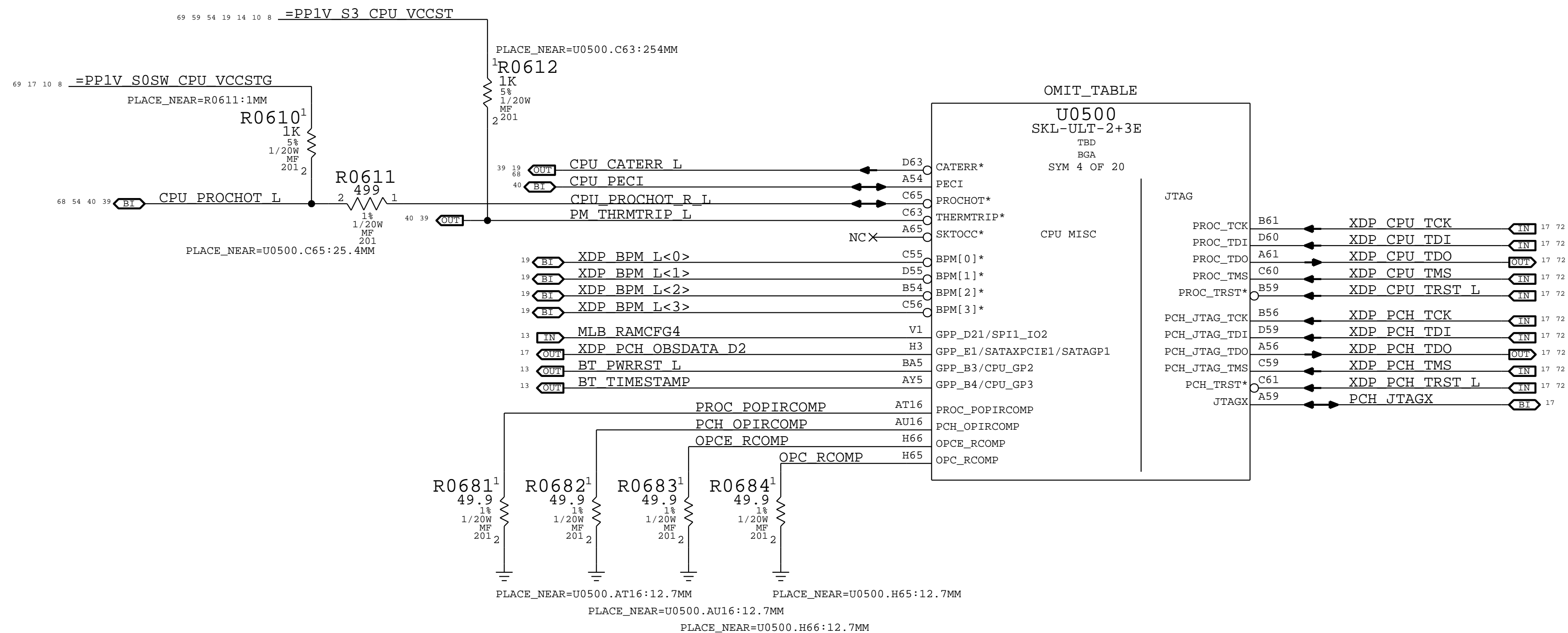

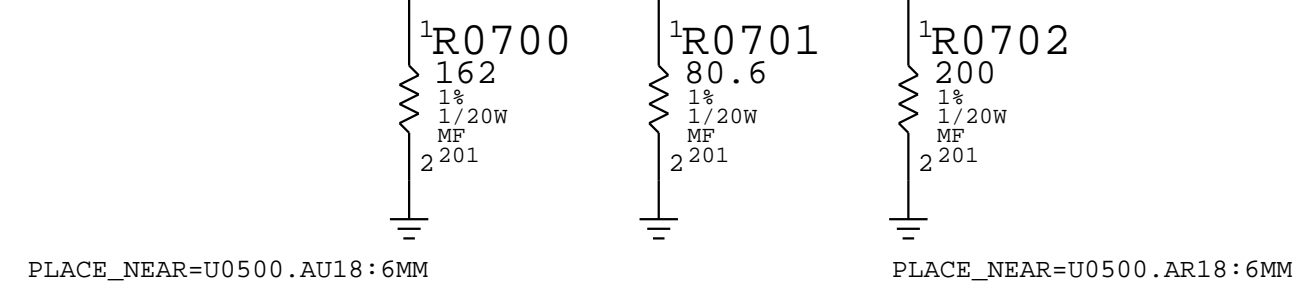
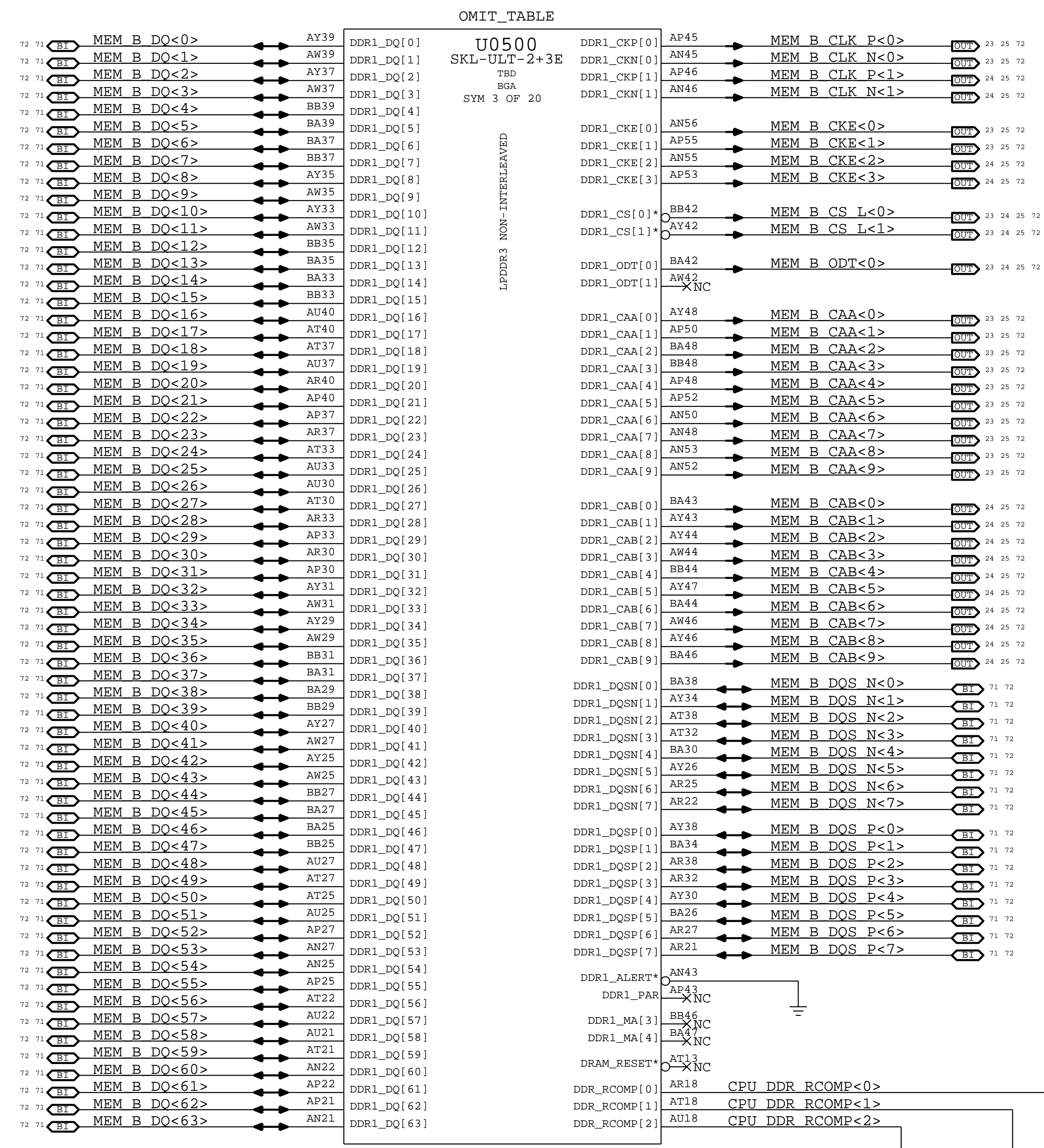
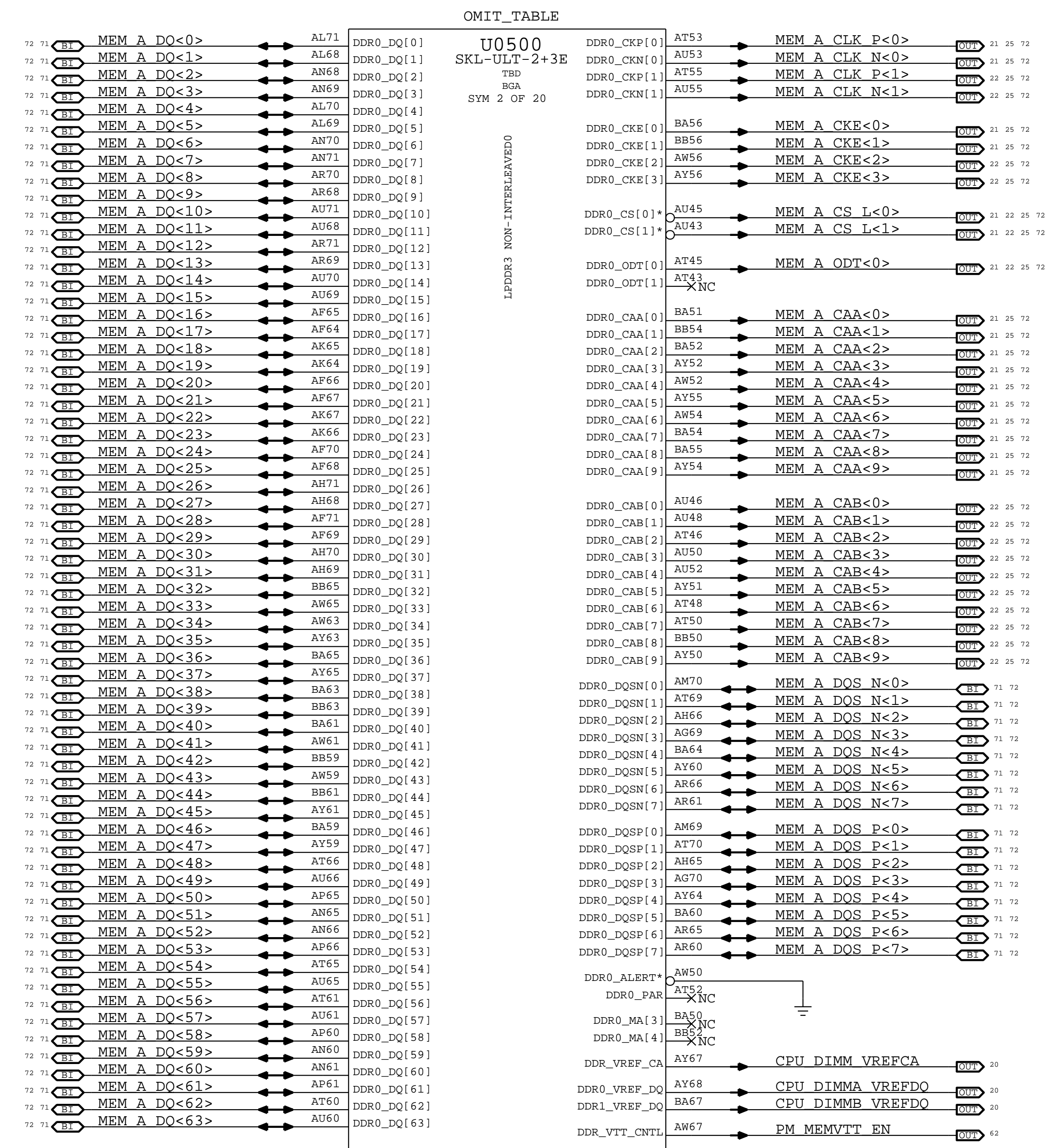


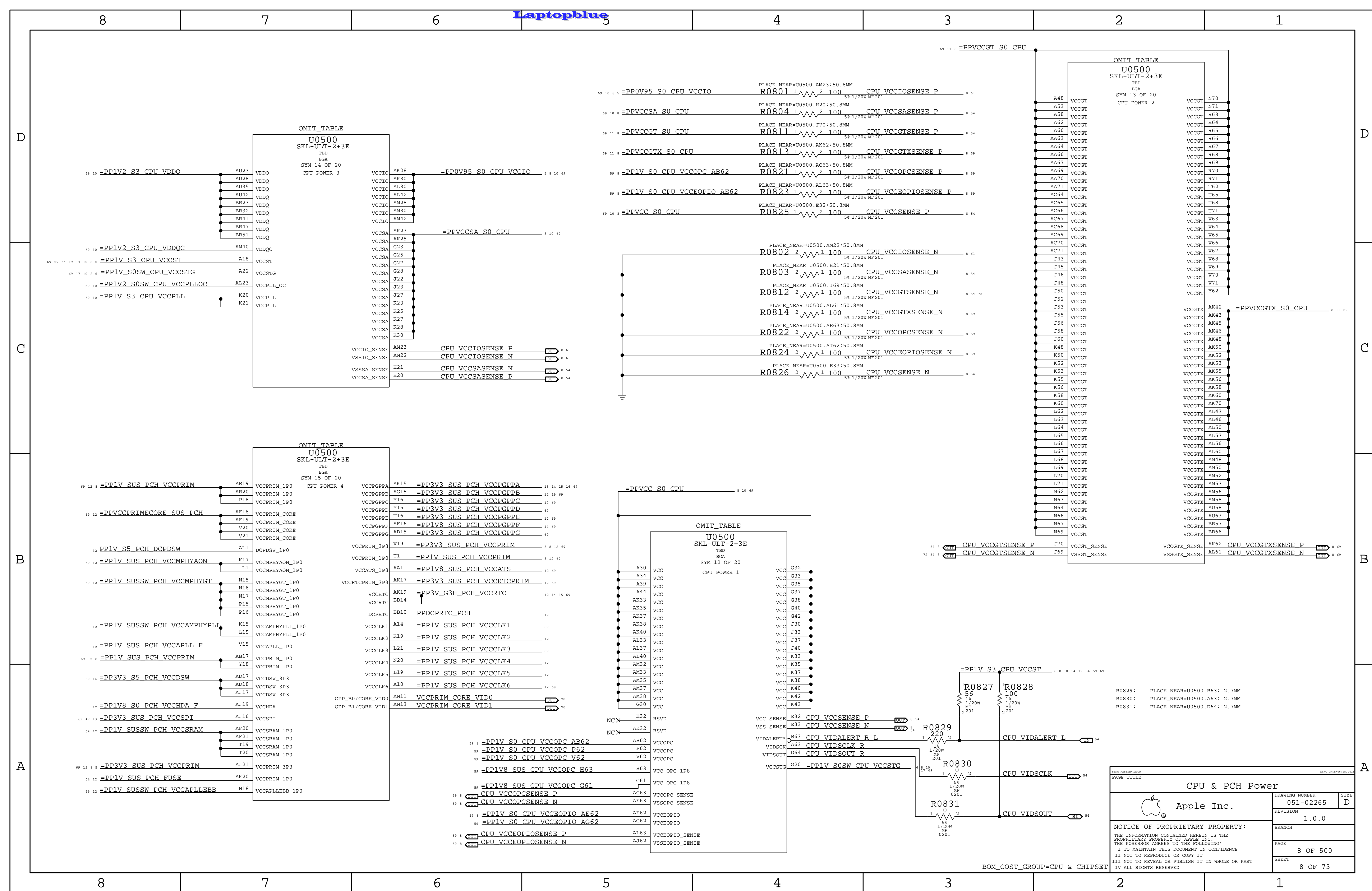
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LAST CHANGE: Thu Aug 4 21:00:42 2016			
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		051-02265	D
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		BRANCH	
		PAGE	5 OF 500
		SHEET	
			5 OF 73



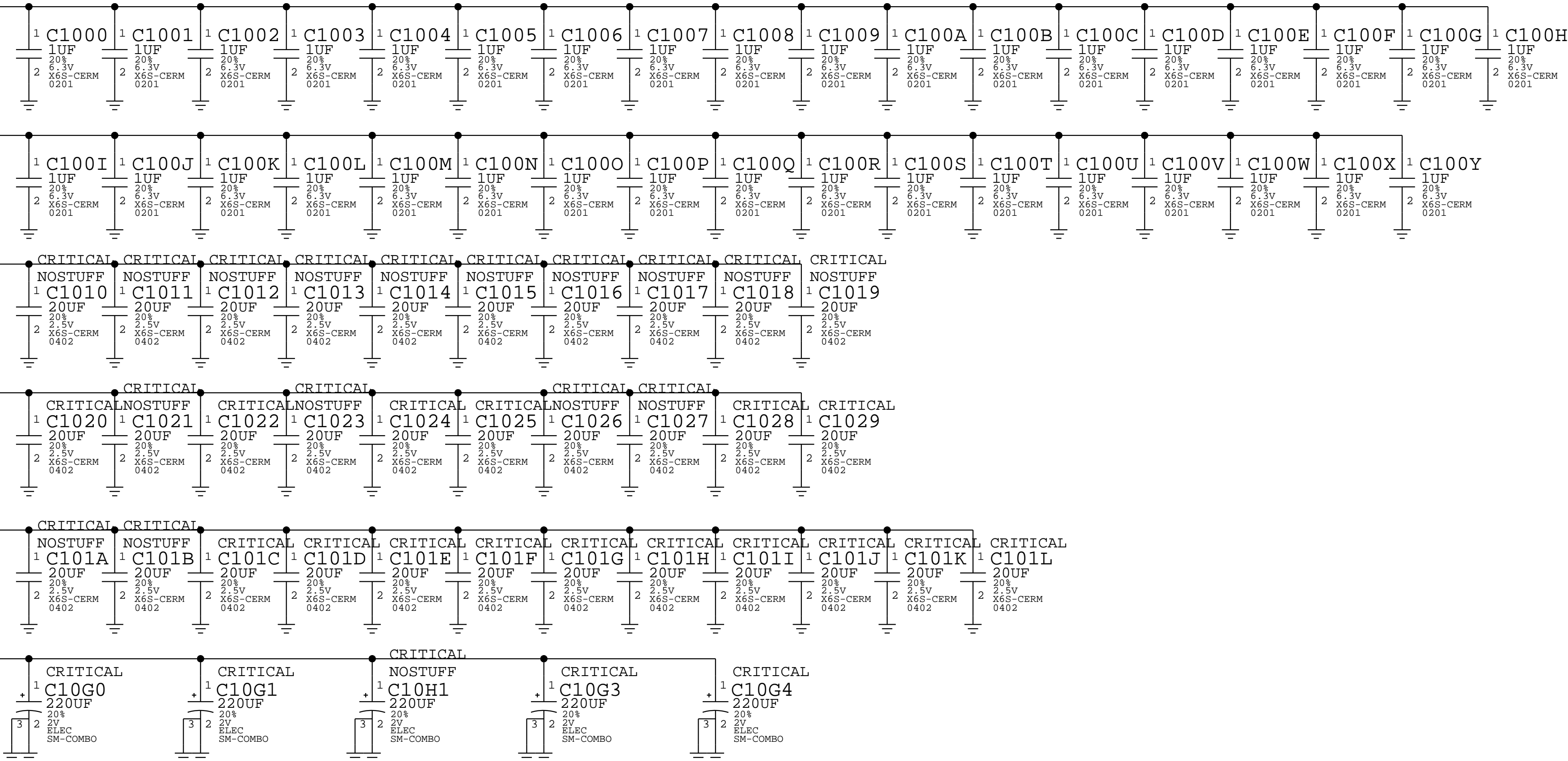
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LAST CHANGE: Thu Aug 4 21:00:42 2016			
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CPU MISC/JTAG/CFG/RSVD		DRAWING NUMBER	SIZE
 Apple Inc.		051-02265	D
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		SHEET	6 OF 73

BOM_COST_GROUP=CPU & CHIPSET

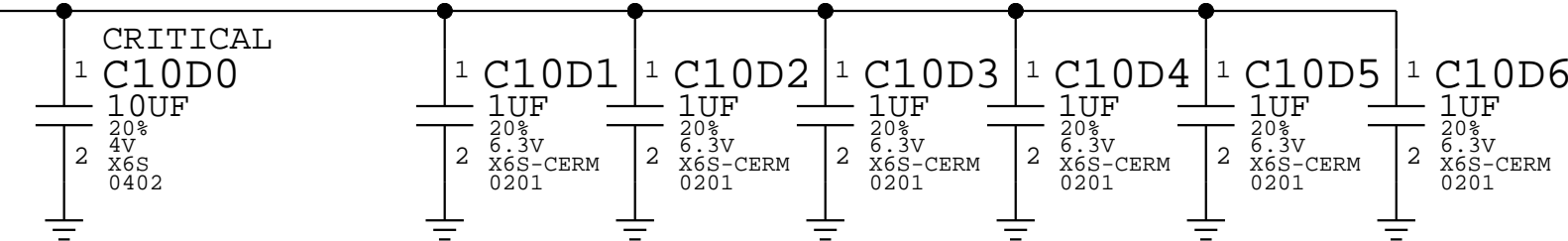




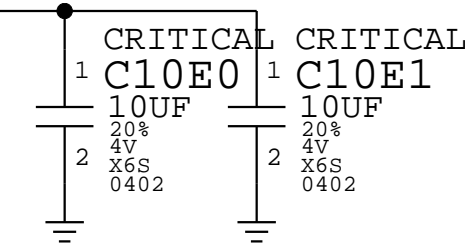
69 8 =PPVCC_S0_CPU



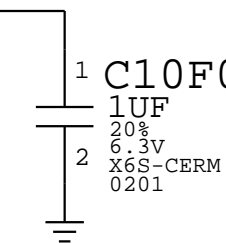
99 =PP1V_S0_CPU_VCCOPC



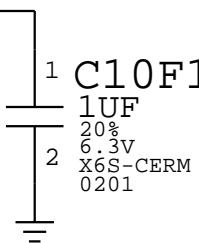
99 =PP1V_S0_CPU_VCCEOPIO



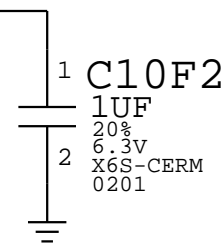
69 8 =PP1V_S3_CPU_VCCPLL



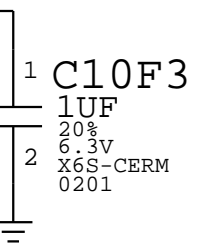
69 8 =PP1V2_S0SW_CPU_VCCPLLOC



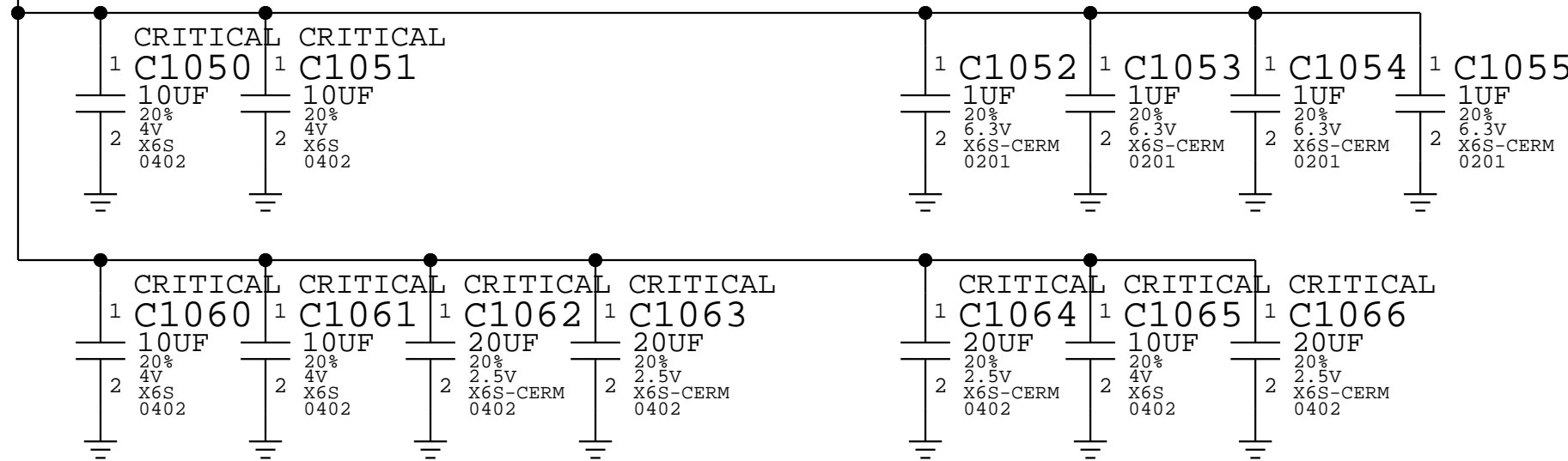
99 54 19 14 8 69 =PP1V_S3_CPU_VCCST



69 17 8 6 =PP1V_S0SW_CPU_VCCSTG



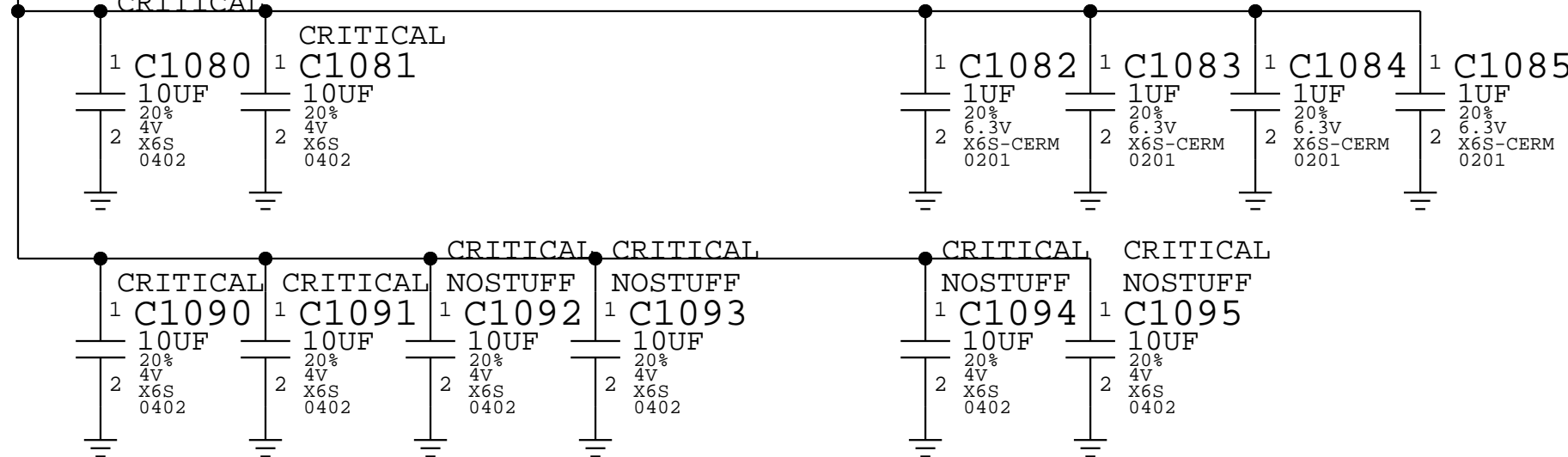
69 8 =PP1V2_S3_CPU_VDDQ



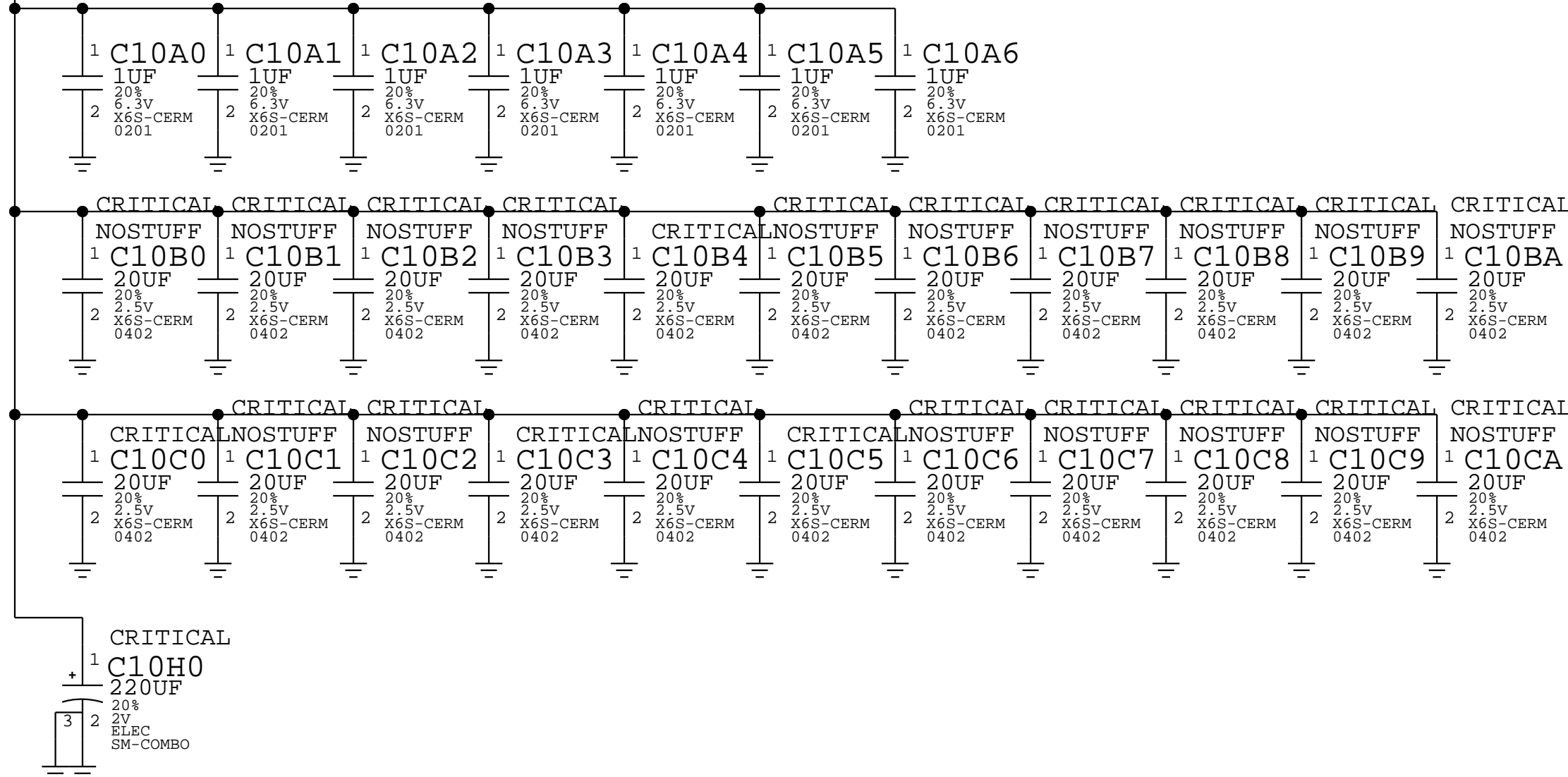
69 8 =PP1V2_S3_CPU_VDDQC



69 5 =PP0V95_S0_CPU_VCCIO



69 8 =PPVCCSA_S0_CPU



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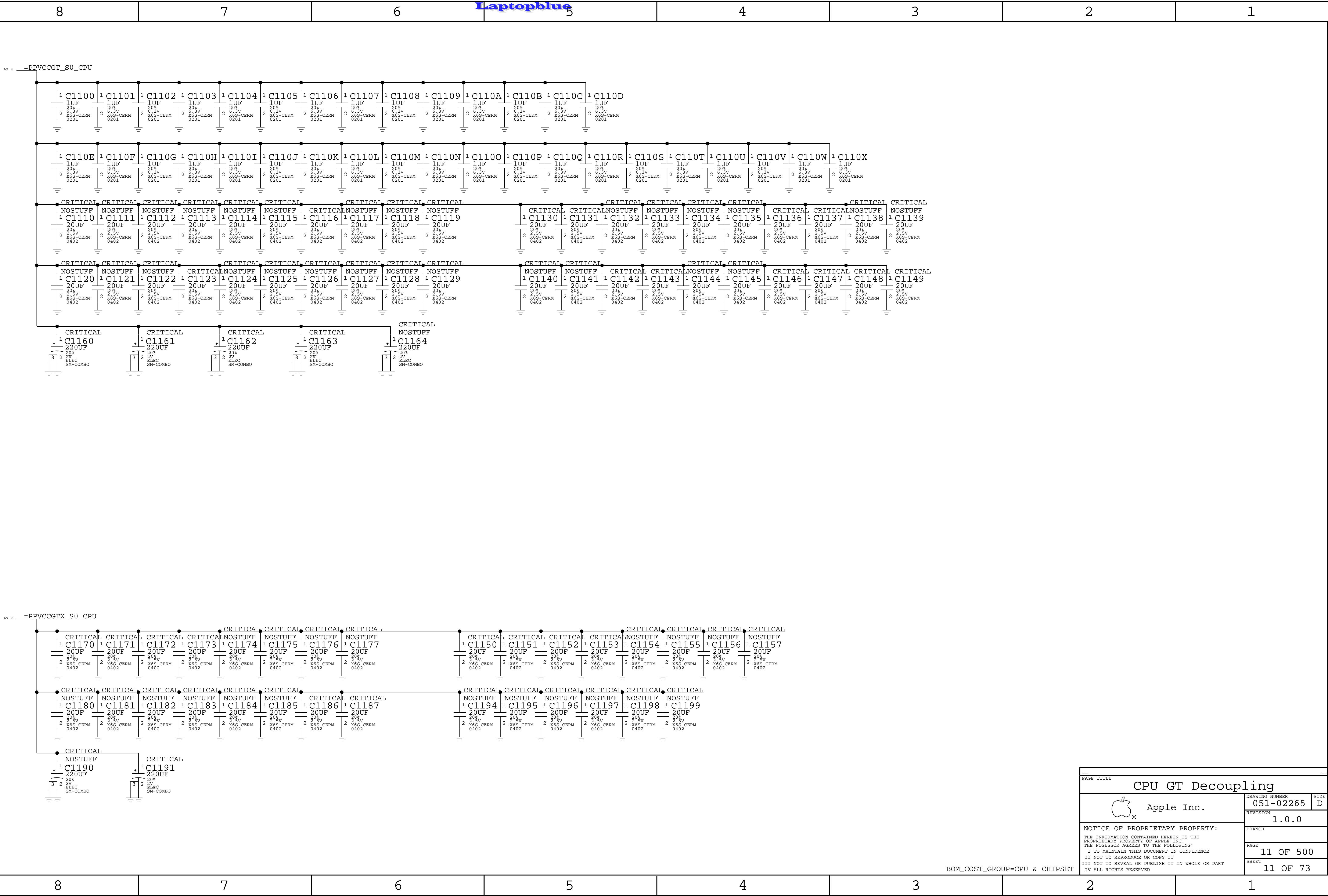
Apple Inc.

Apple logo

SYNC_MASTER=PAULM

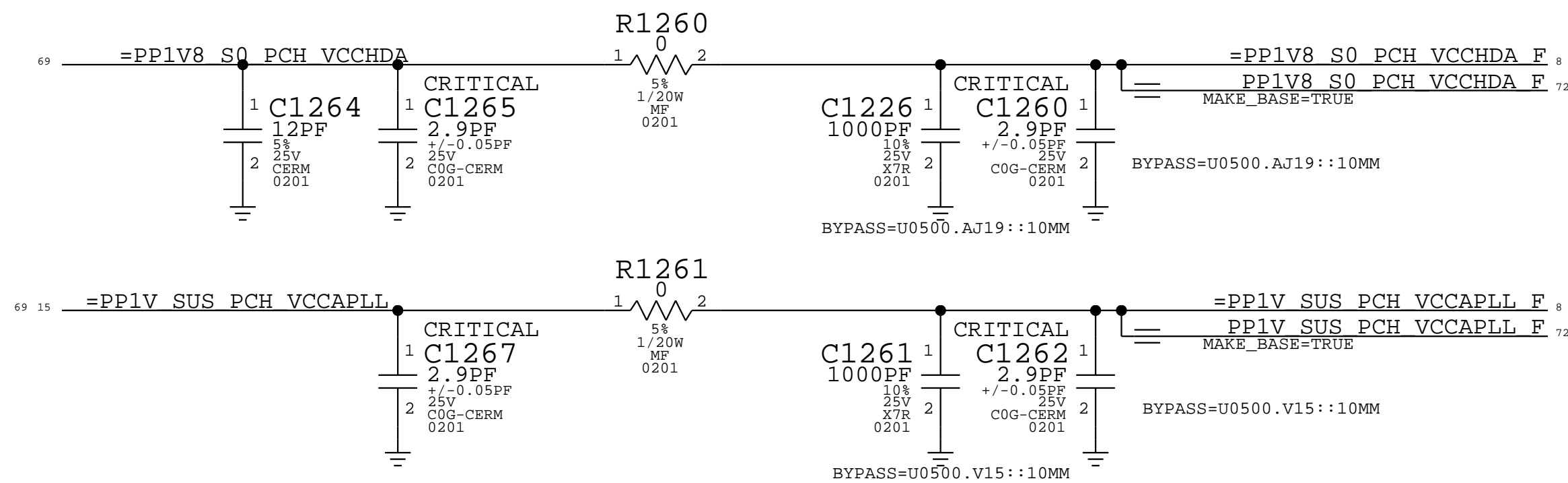
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BOM_COST_GROUP=CPU & CHIPSET





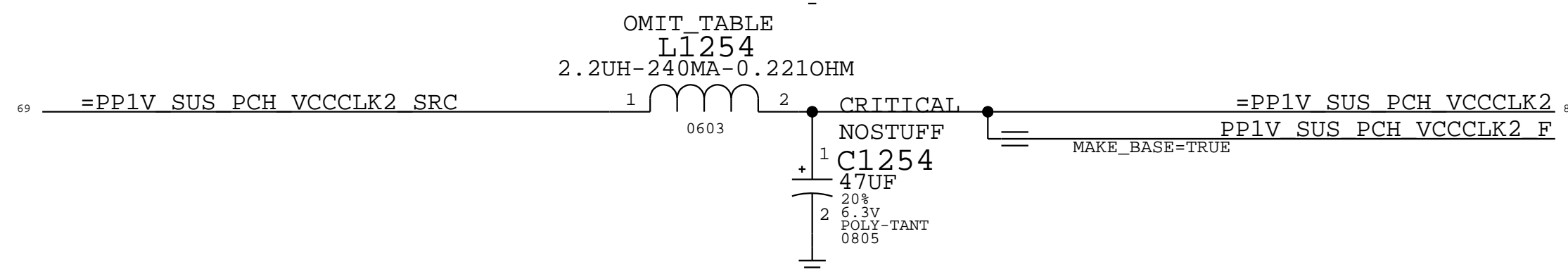
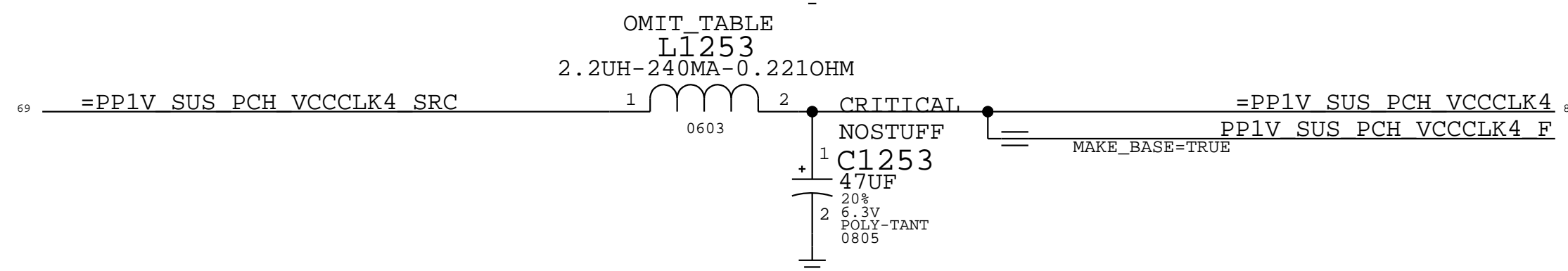
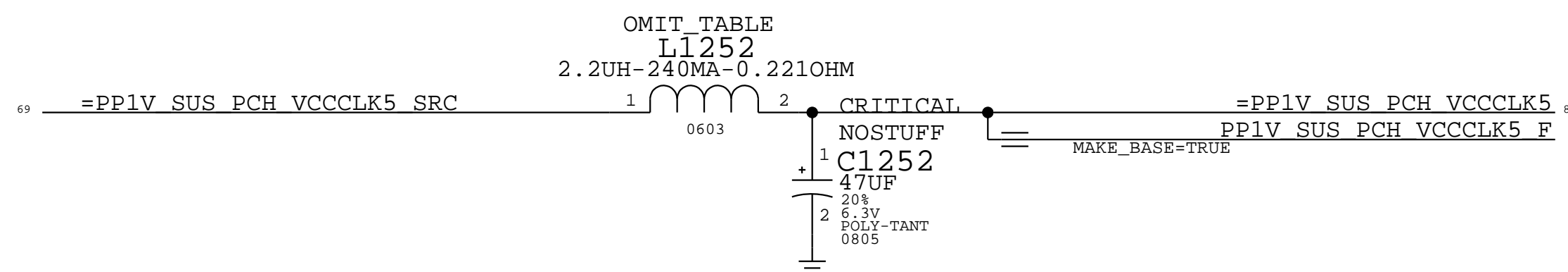
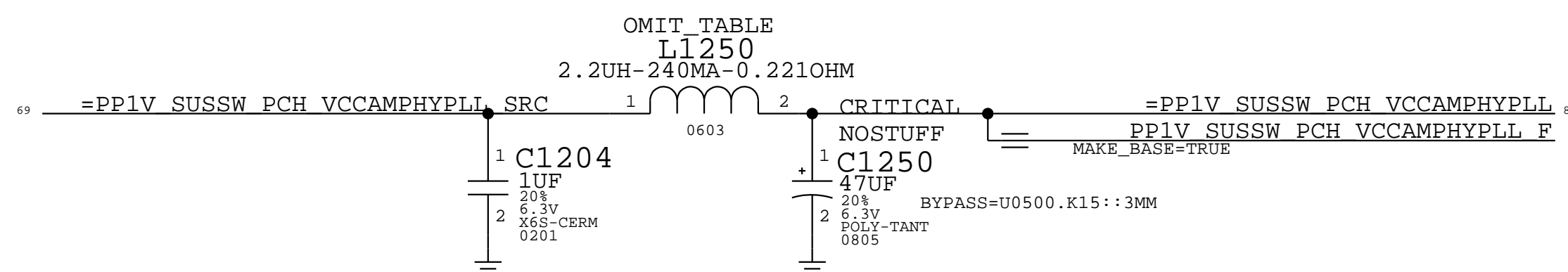
CPU CIRCUITS GENERATE NOISE AT WIFI BAND FREQUENCIES.
USE SPECIFIC 3PF CAPS FOR BEST FILTERING OF THOSE FREQUENCIES.



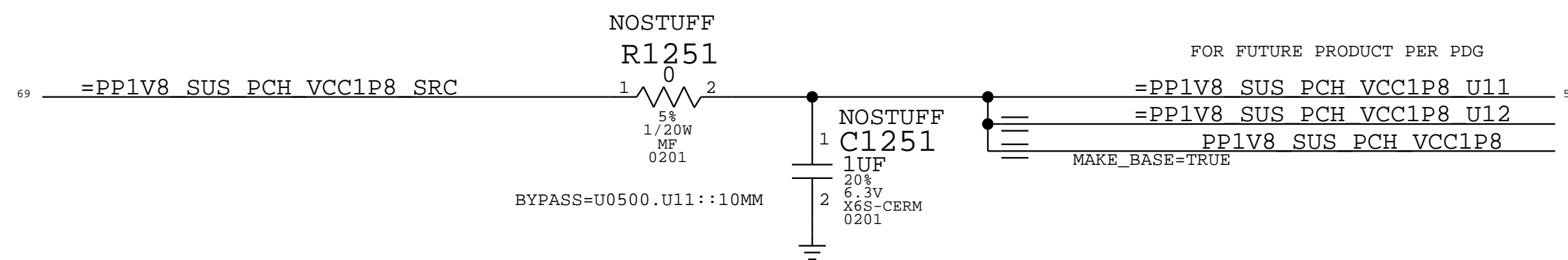
FILTER PLACEHOLDERS ONLY


RAIL SIDE

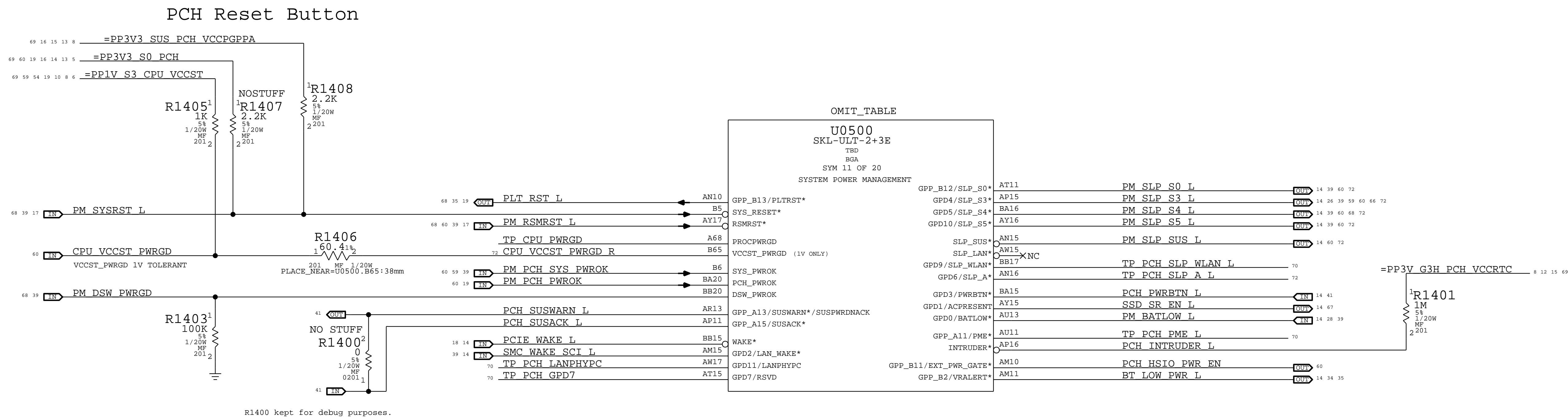
PCH SIDE



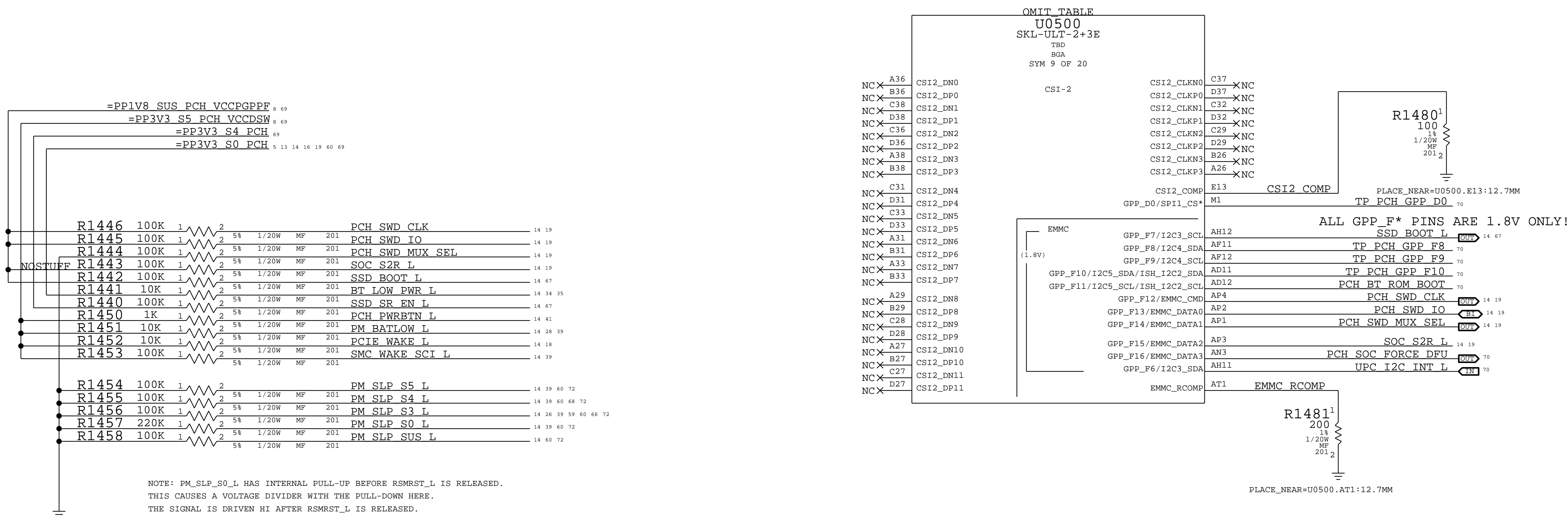
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	4	RES,MF,1A MAX,00HM,5%,0603	L1250,L1252,L1253,L1254		




PAGE TITLE				
PCH Decoupling				
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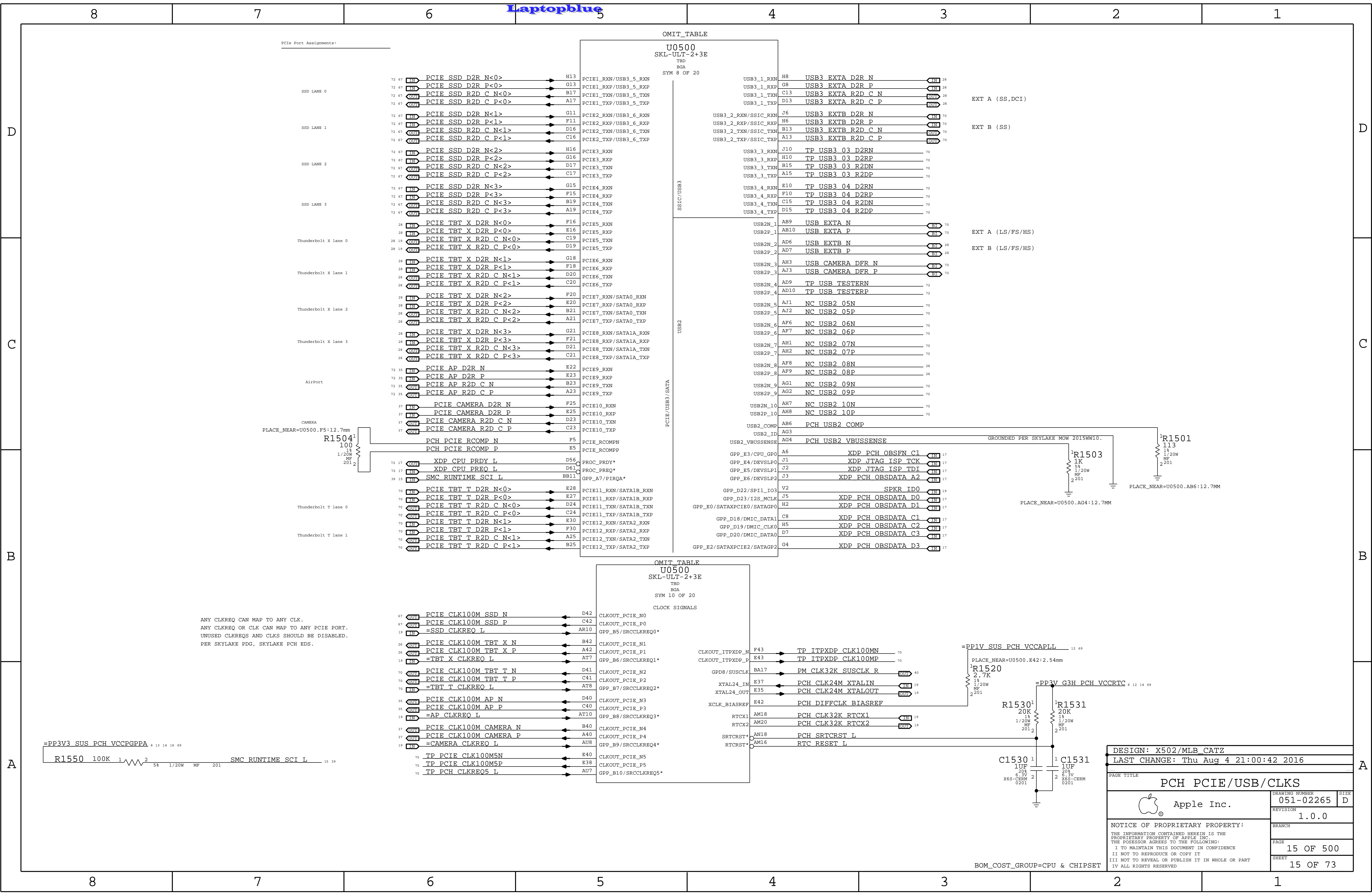


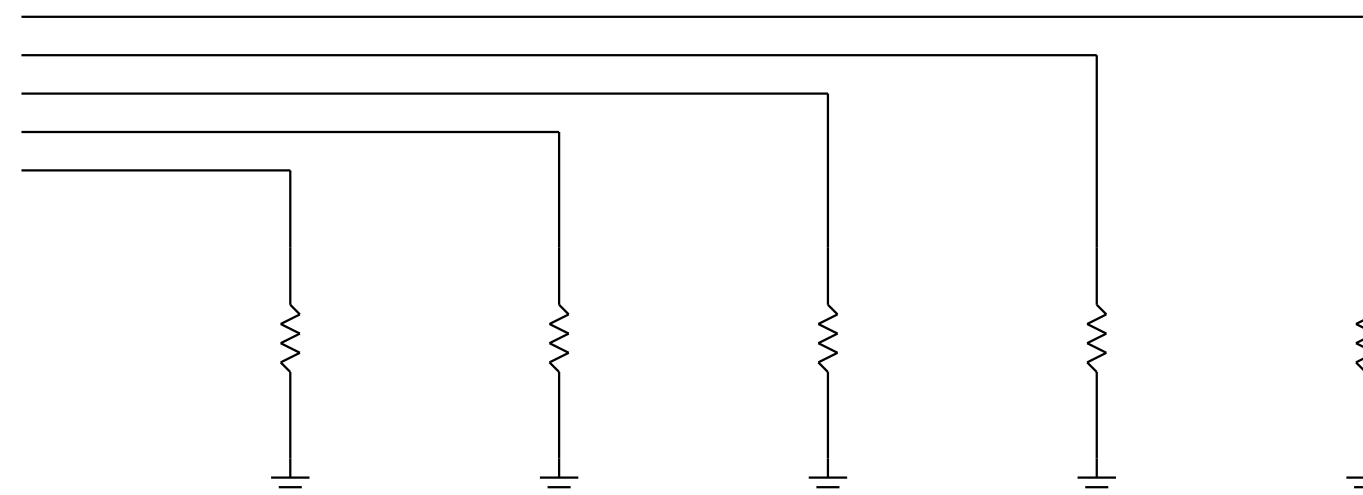
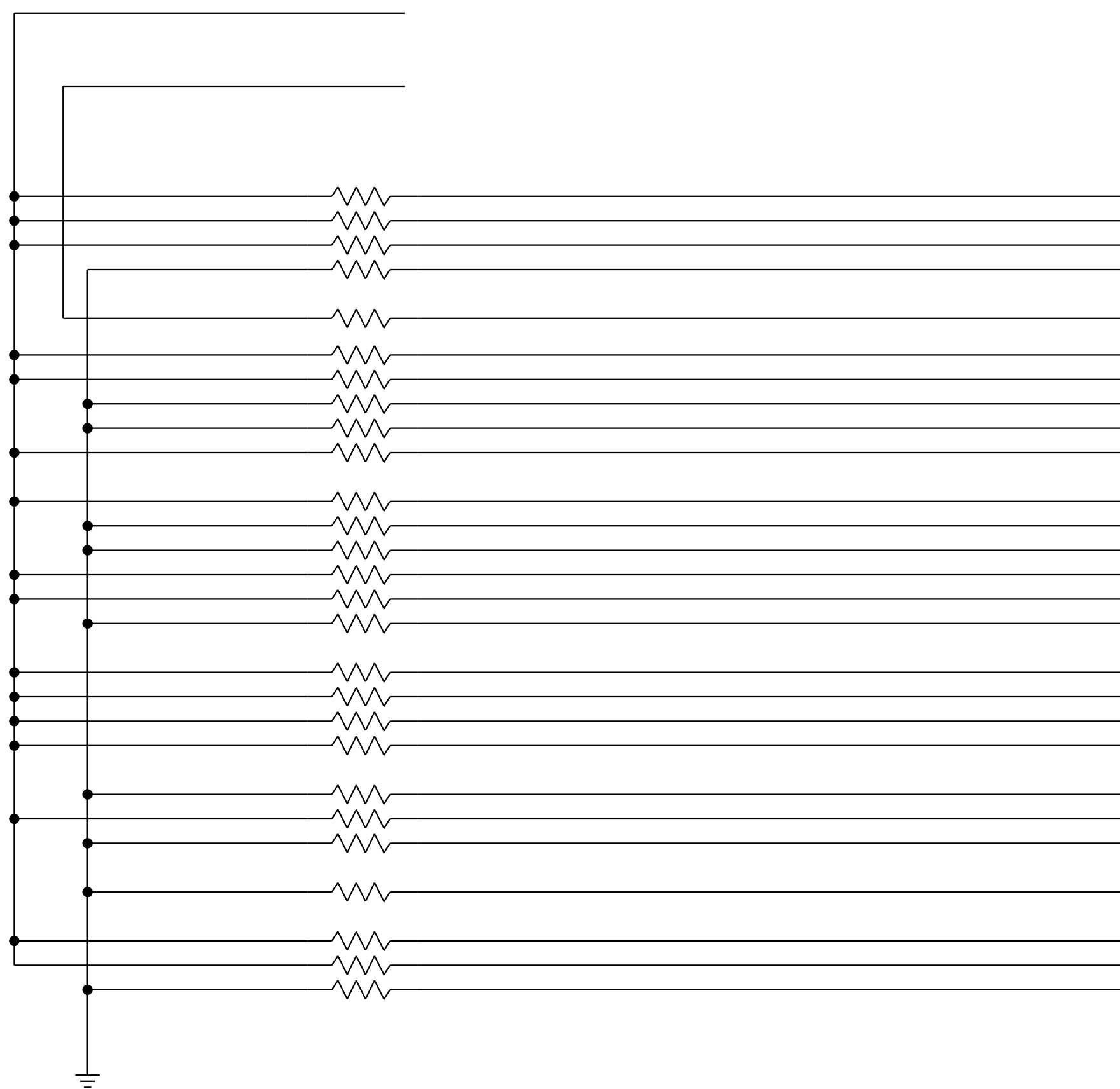
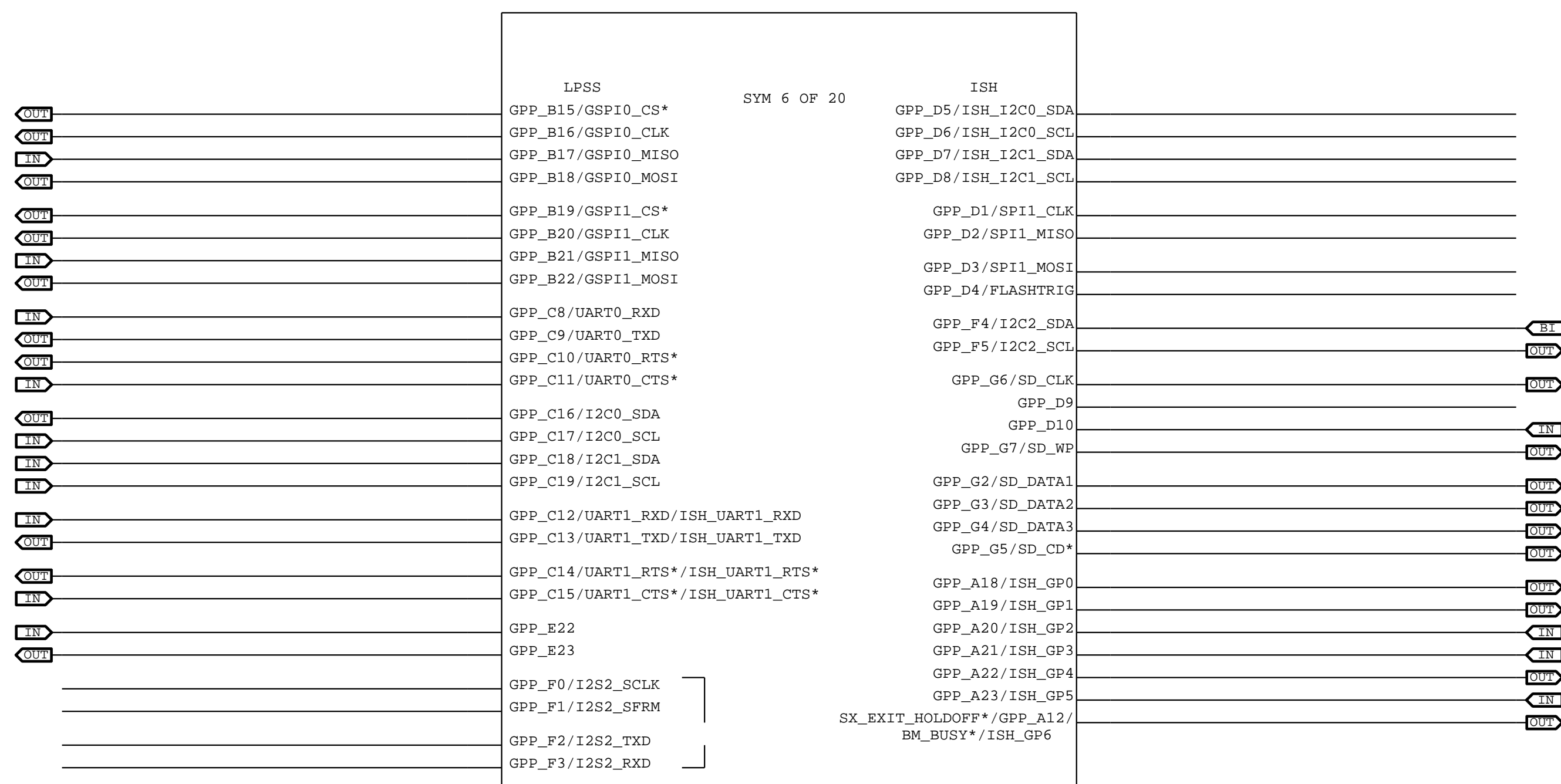
R1400 kept for debug purposes.




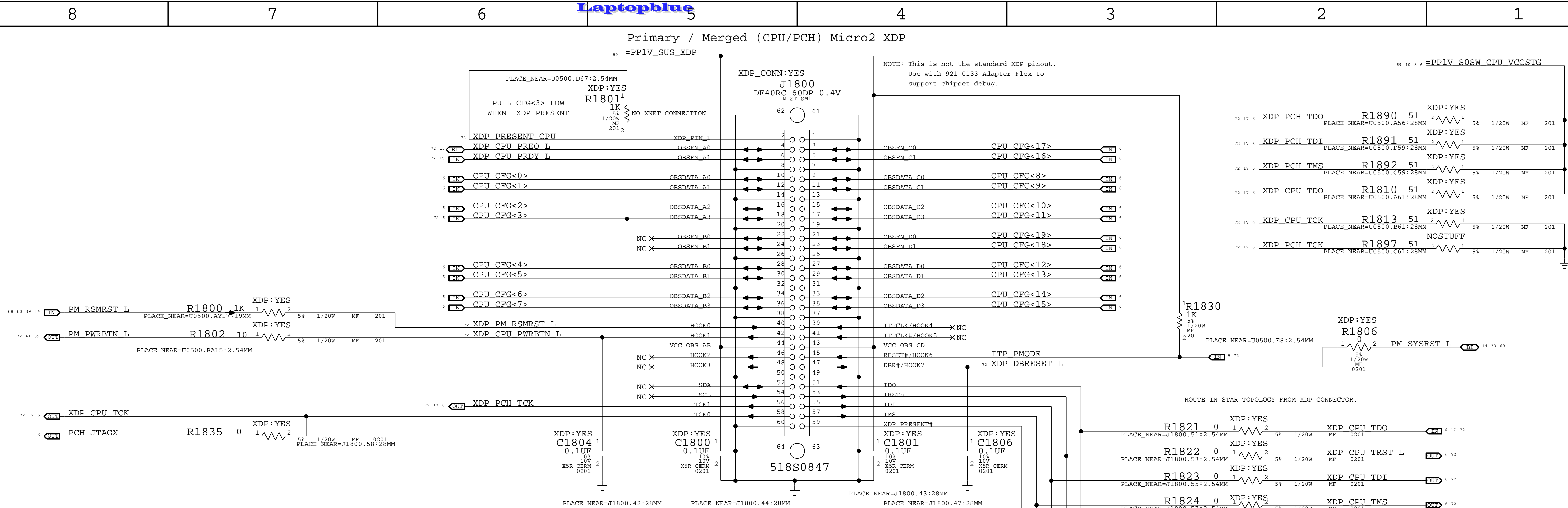
NOTE: PM_SLP_S0_L HAS INTERNAL PULL-UP BEFORE RSMRST_L IS RELEASED.
THIS CAUSES A VOLTAGE DIVIDER WITH THE PULL-DOWN HERE.
THE SIGNAL IS DRIVEN HI AFTER RSMRST_L IS RELEASED.

DESIGN: X502/MLB_CATZ		
LAST CHANGE: Thu Aug 4 21:00:42 2016		
PAGE TITLE		
PCH Power Management		
 Apple Inc.®	DRAWING NUMBER	051-02265
	REVISION	1.0.0
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PCH XDP Signals

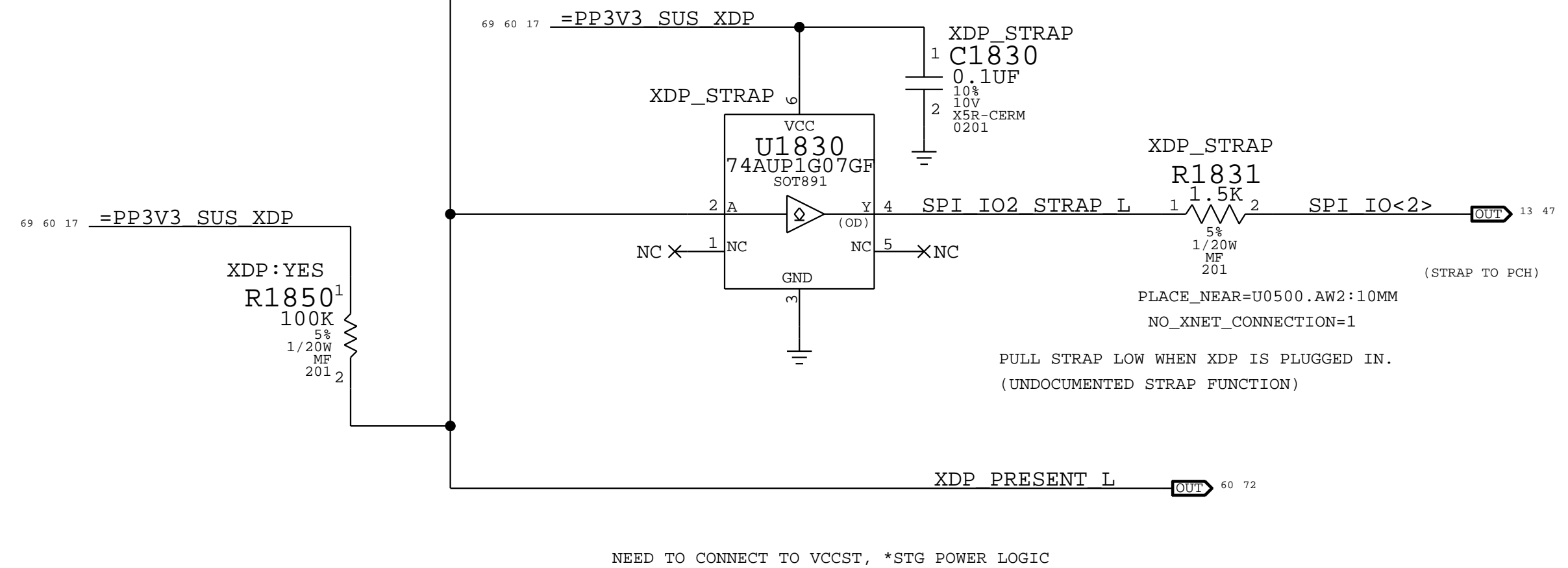
These signals do not connect to the Primary (Merged) XDP connector in this architecture. The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation. They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.


PCH/XDP Signals				Non-XDP Signals			
15	TP	XDP JTAG ISP TCK	MAKE_BASE=TRUE	==	JTAG ISP TCK	28	TP
15	TP	XDP JTAG ISP TDI	MAKE_BASE=TRUE	==	JTAG ISP TDI	28	TP
15	B1	XDP PCH OBSDATA A2			TP1870		
15	B1	XDP PCH OBSDATA A3			TP1871		
5	B1	XDP PCH OBSDATA B0			TP1872		
13	B1	XDP PCH OBSDATA C0			TP1873		
15	B1	XDP PCH OBSDATA C1			TP1874		
15	B1	XDP PCH OBSDATA C2			TP1875		
15	B1	XDP PCH OBSDATA C3			TP1876		
15	B1	XDP PCH OBSDATA D0			TP1877		
15	B1	XDP PCH OBSDATA D1			TP1878		
6	B1	XDP PCH OBSDATA D2			TP1879		
15	B1	XDP PCH OBSDATA D3			TP1880		
15	B1	XDP PCH OBSFN C1			TP1881		
5	Q004	XDP USB EXTA OC L	MAKE_BASE=TRUE	==	USB EXTA OC L	28	Q004
5	Q004	XDP USB EXTB OC L	MAKE_BASE=TRUE	==	USB EXTB OC L	28	Q004
5	Q004	XDP USB EXTC OC L	MAKE_BASE=TRUE	==	USB EXTC OC L	28	Q004
5	Q004	XDP USB EXTD OC L	MAKE_BASE=TRUE	==	USB EXTD OC L	28	Q004

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

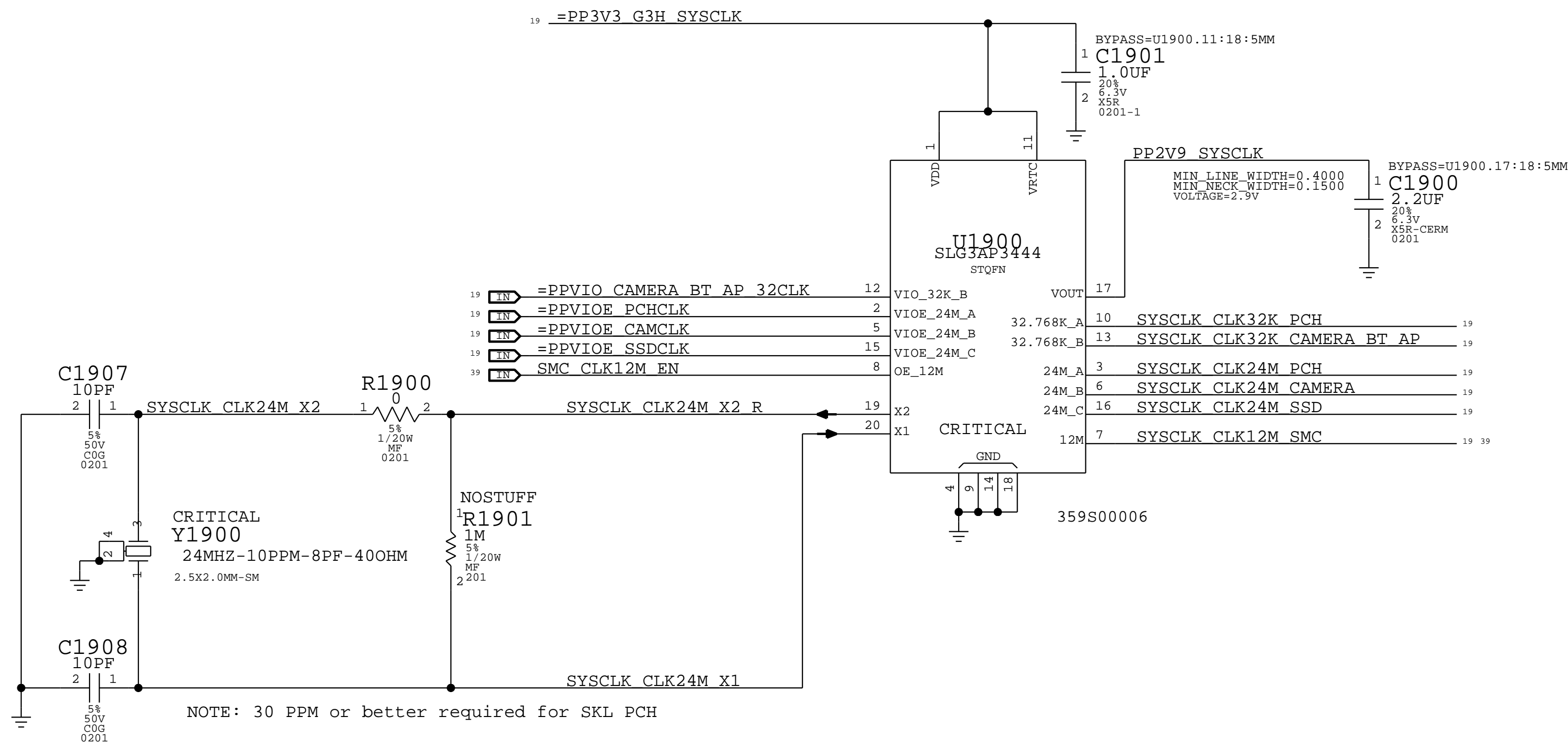
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.



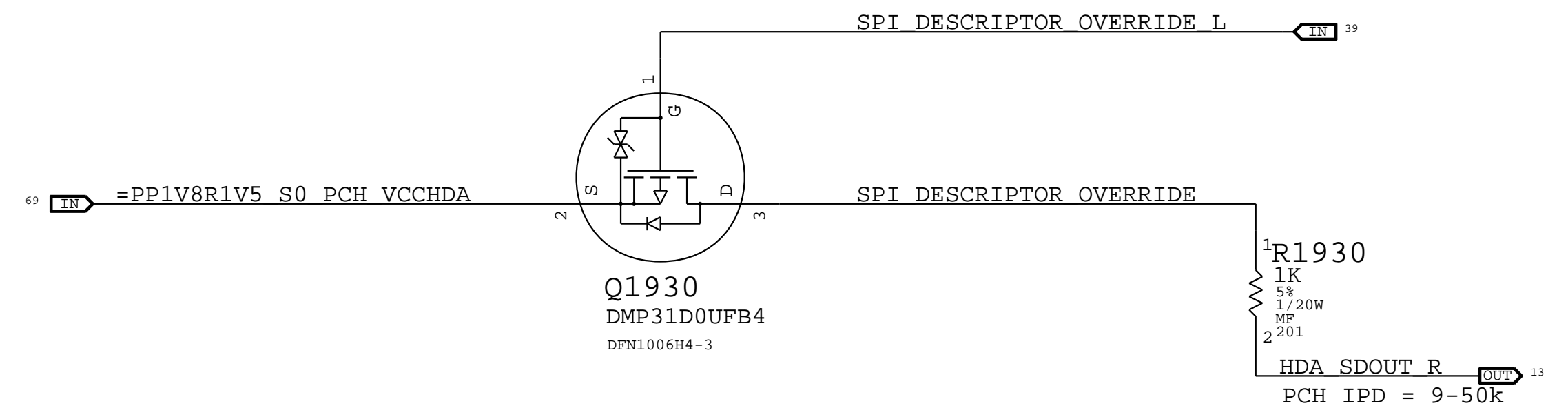
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LAST CHANGE: Thu Aug 4 21:00:42 2016		
PAGE TITLE		
CPU/PCH Merged XDP		
 Apple Inc.	DRAWING NUMBER	051-02265
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	SHEET	17 OF 73

BOM_COST_GROUP=DEBUG

System 32kHz / 12MHz / 24MHz Clock Generator



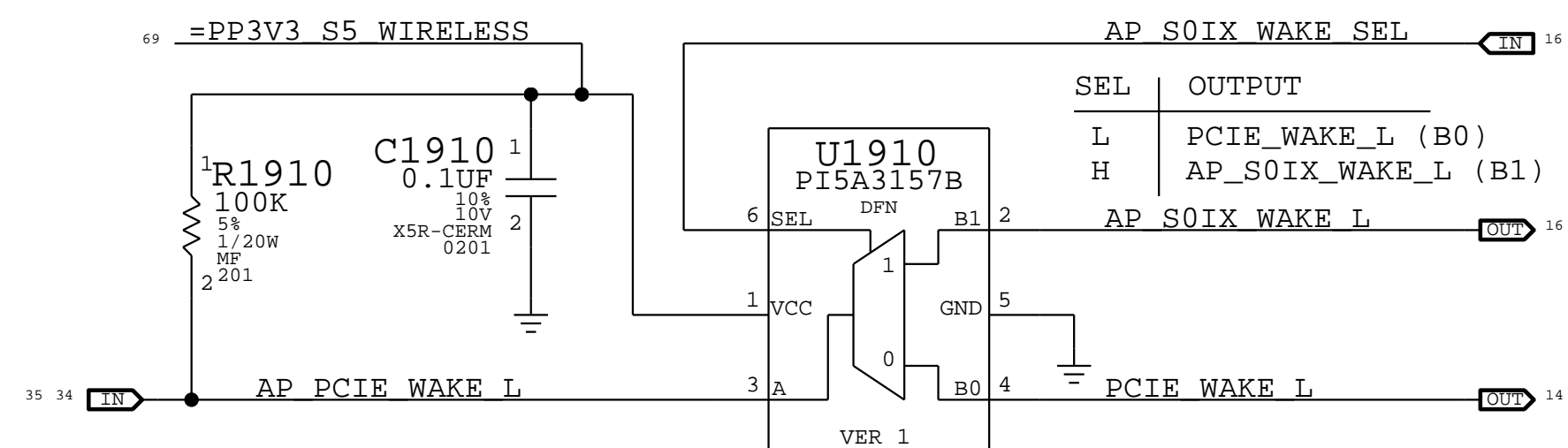
PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting.

**** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing



D

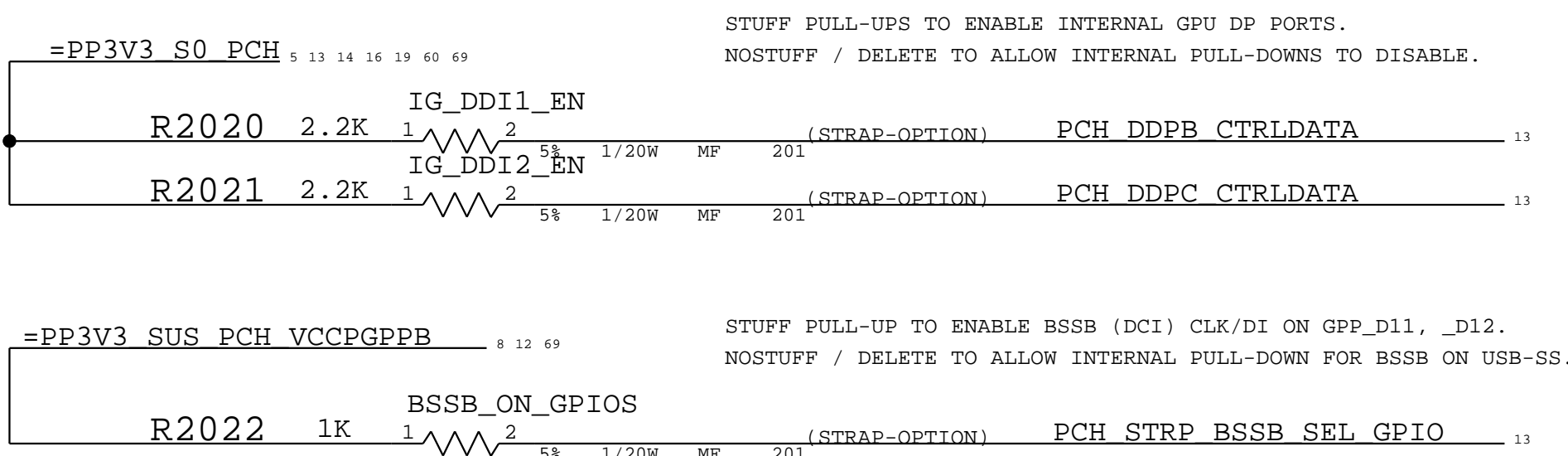
C

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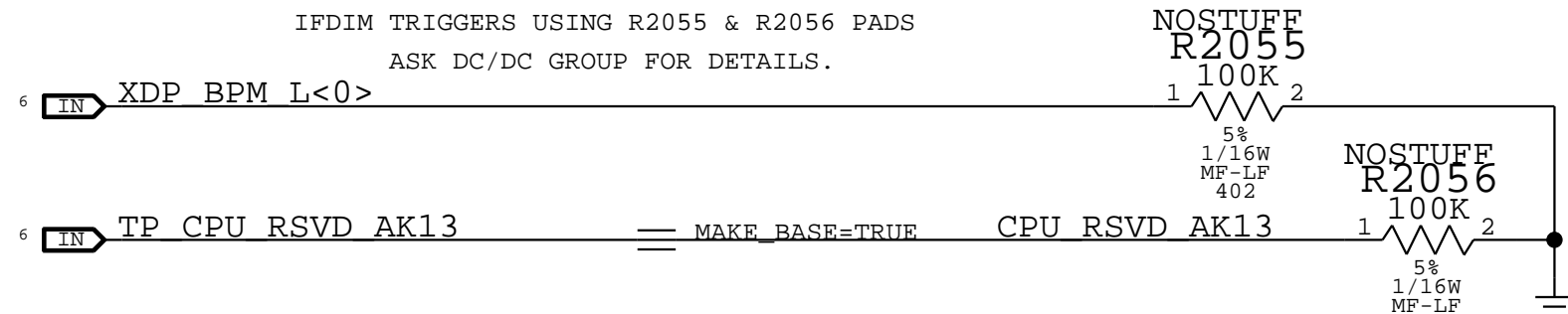
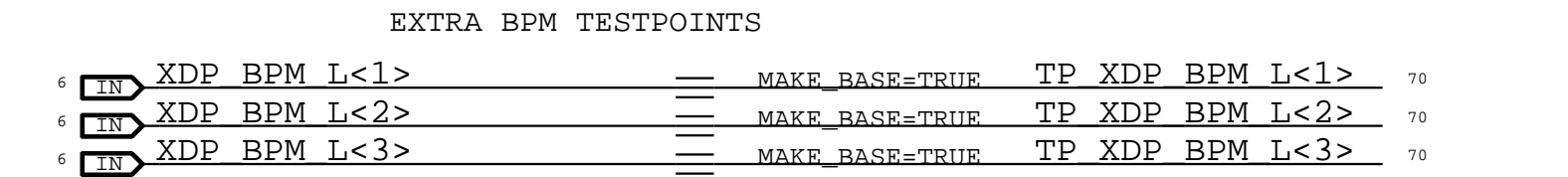
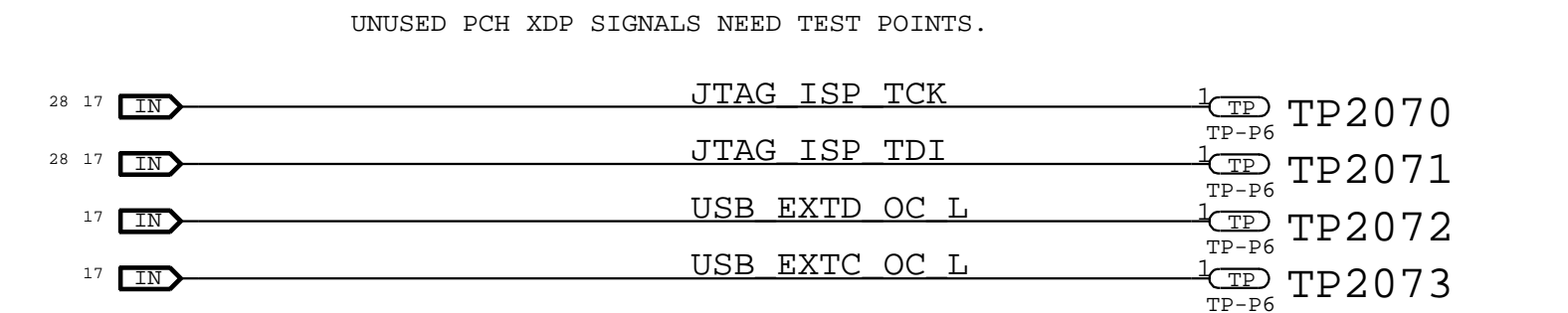
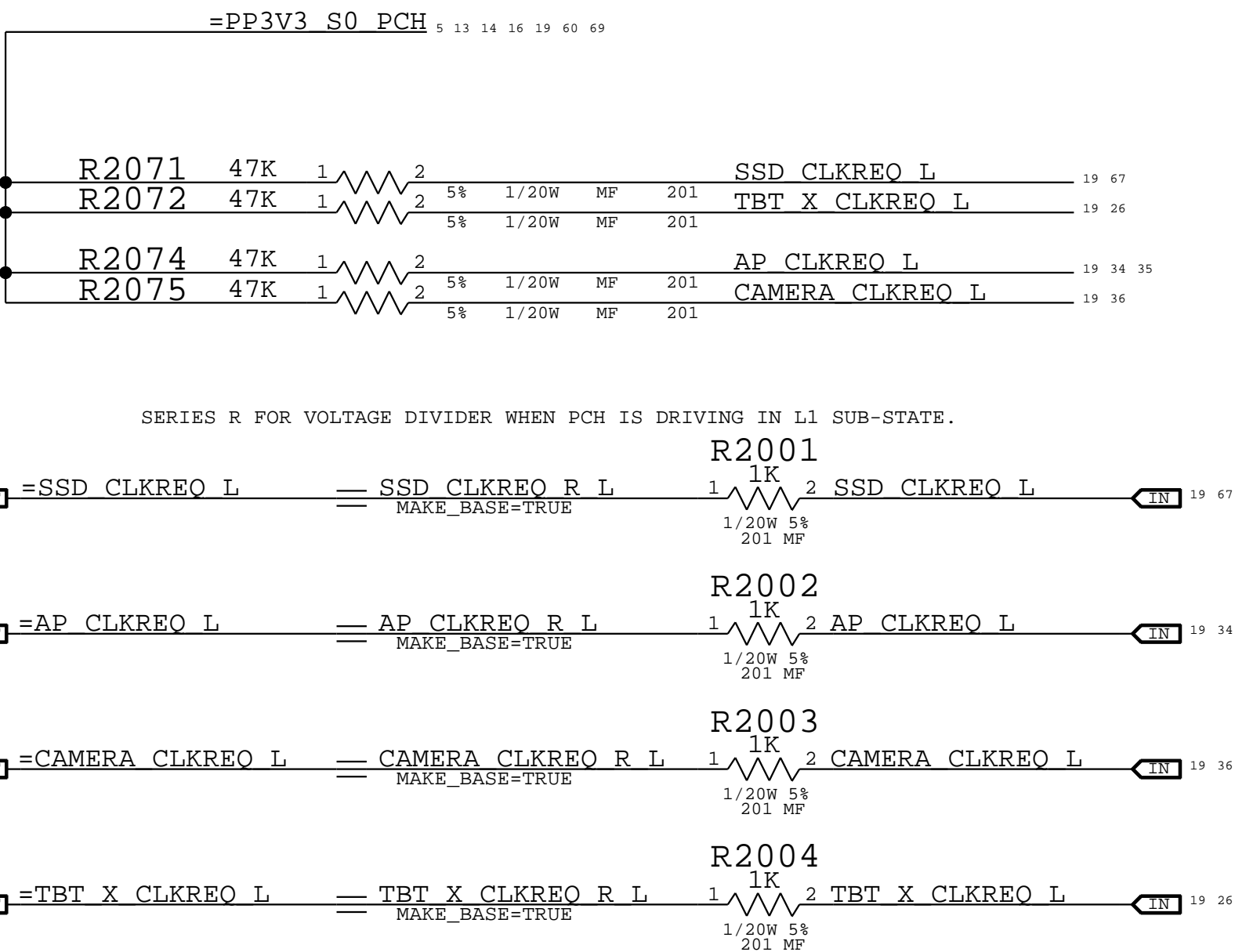
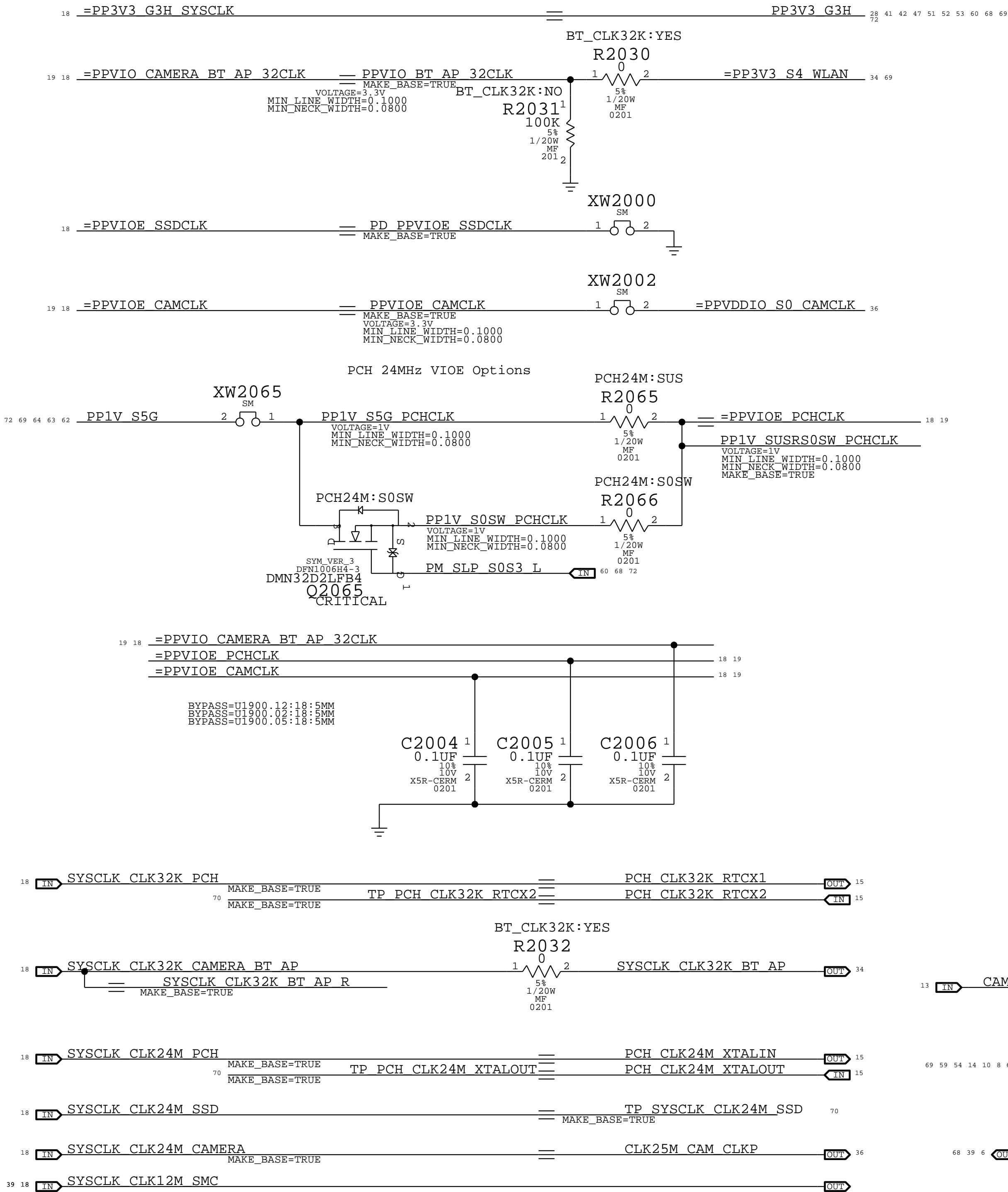
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OPTION STRAPS

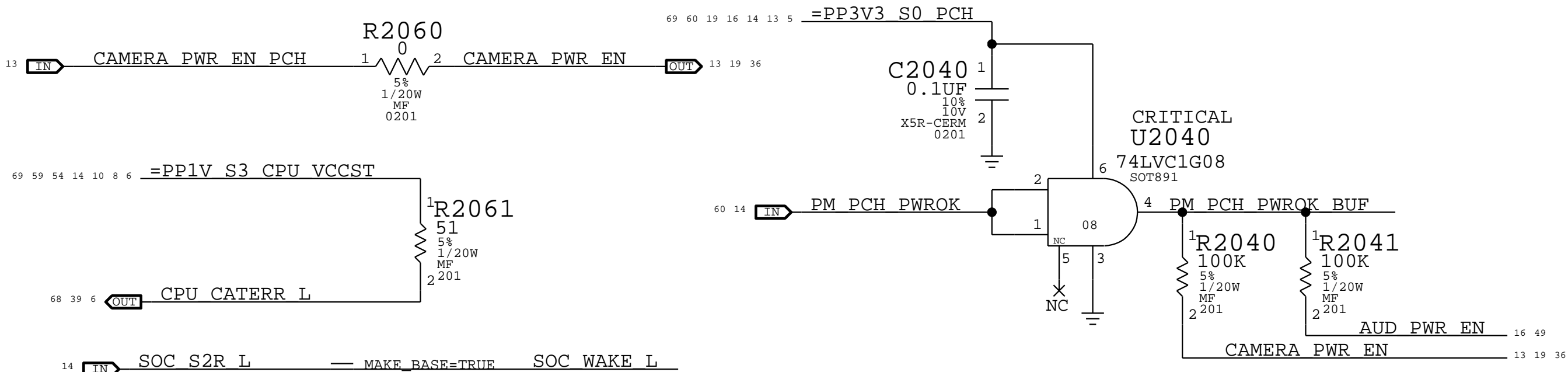
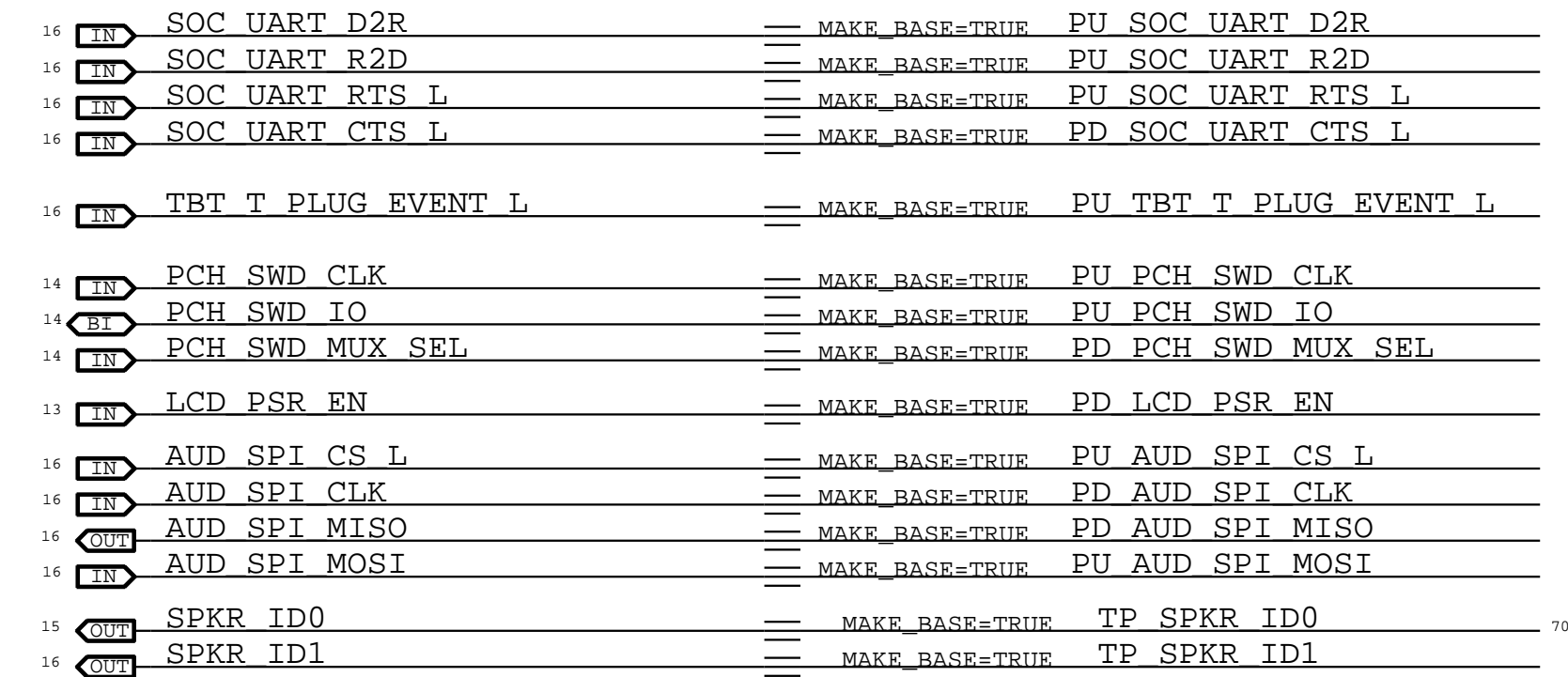
PROJECT DEPENDANT



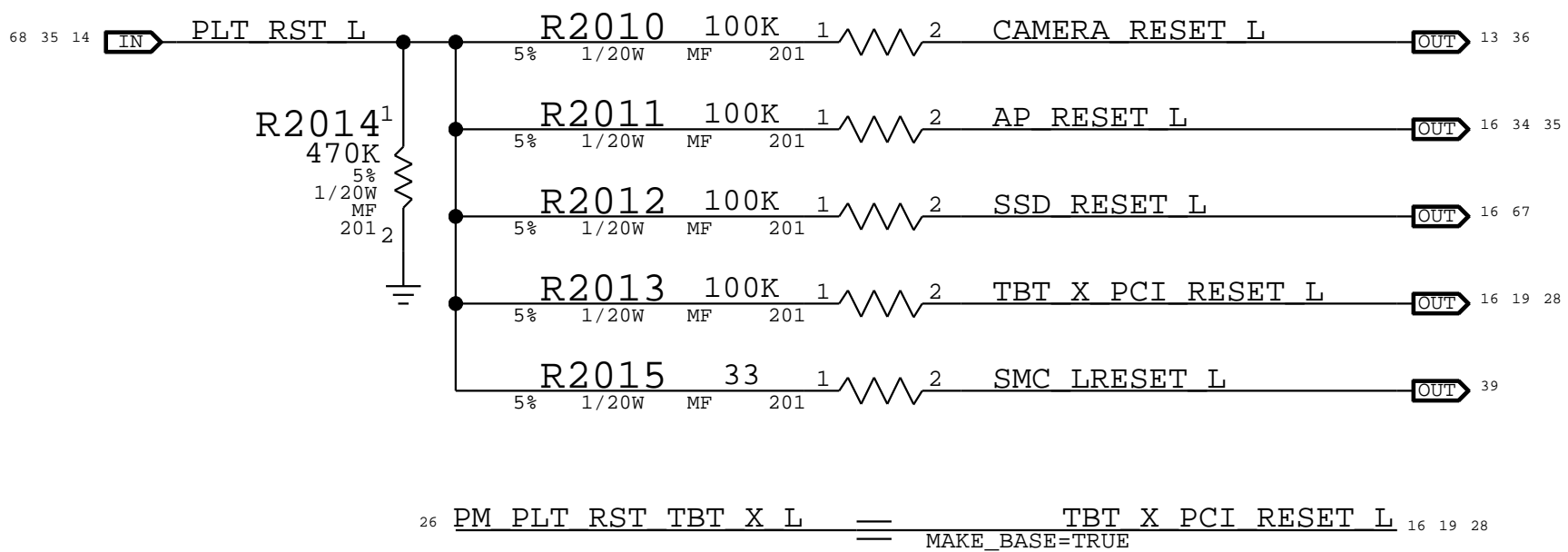
GREENCLK CLOCK CONNECTIONS.



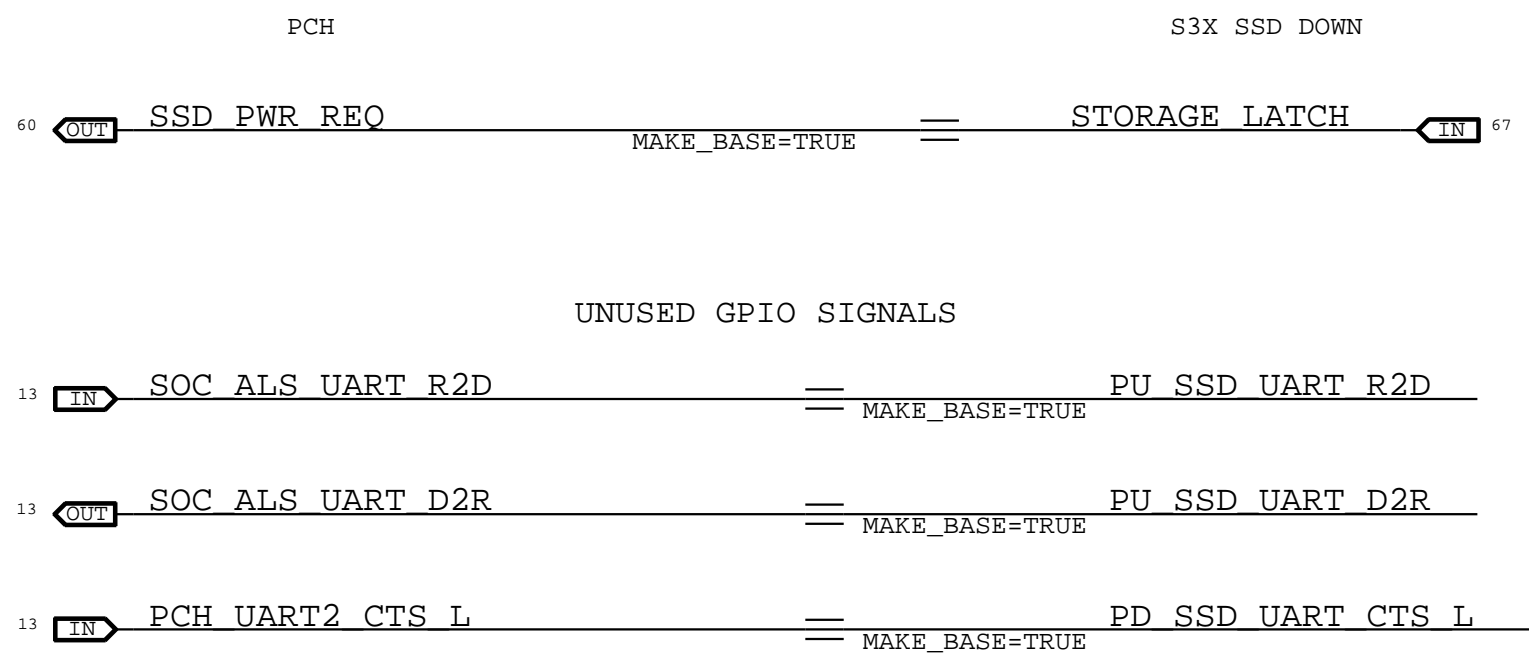
UNUSED GPIO SIGNALS



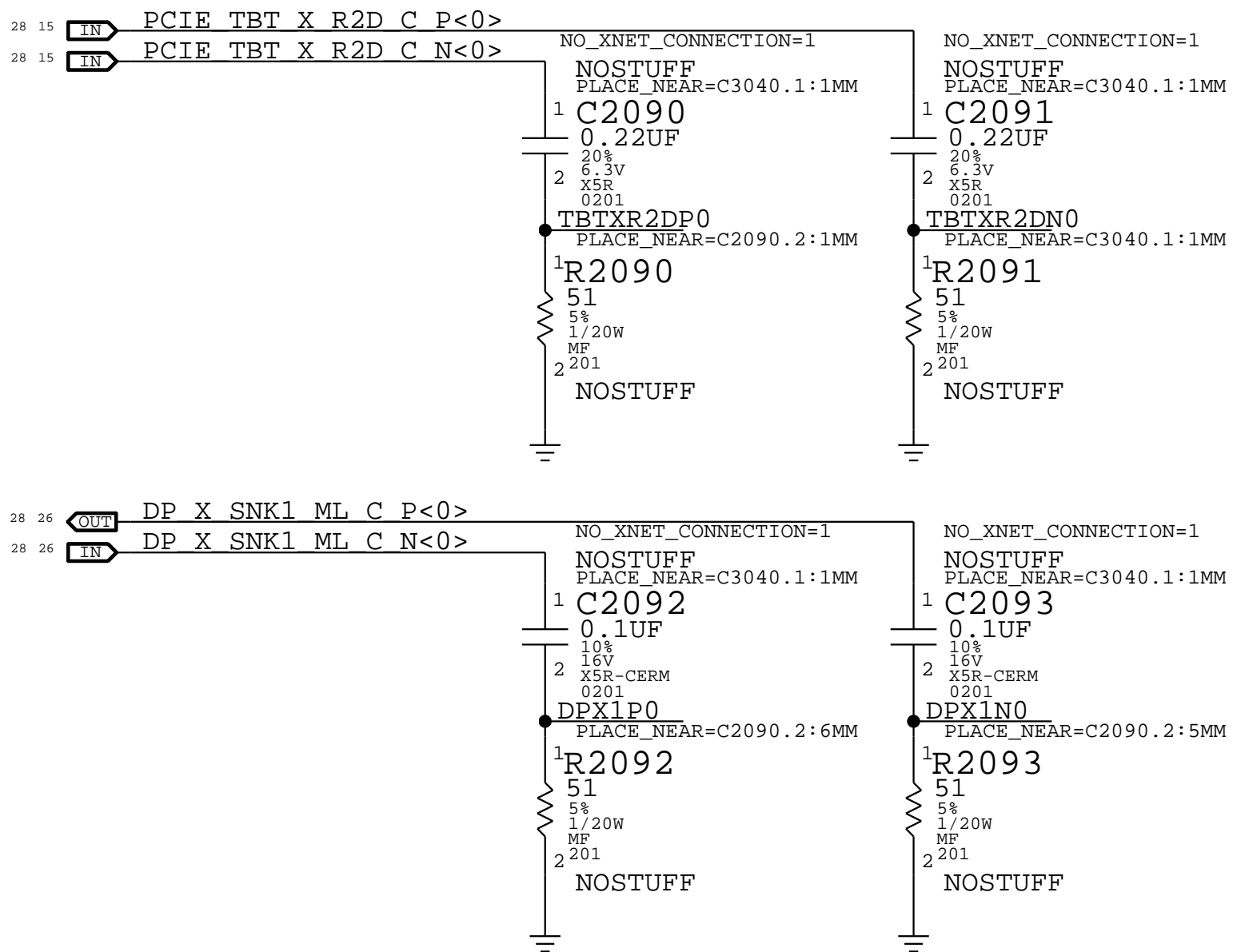
RESETS




S3X SSD CONTROL



PROBE POINTS



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Chipset Support 2		
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	SHEET	19 OF 73

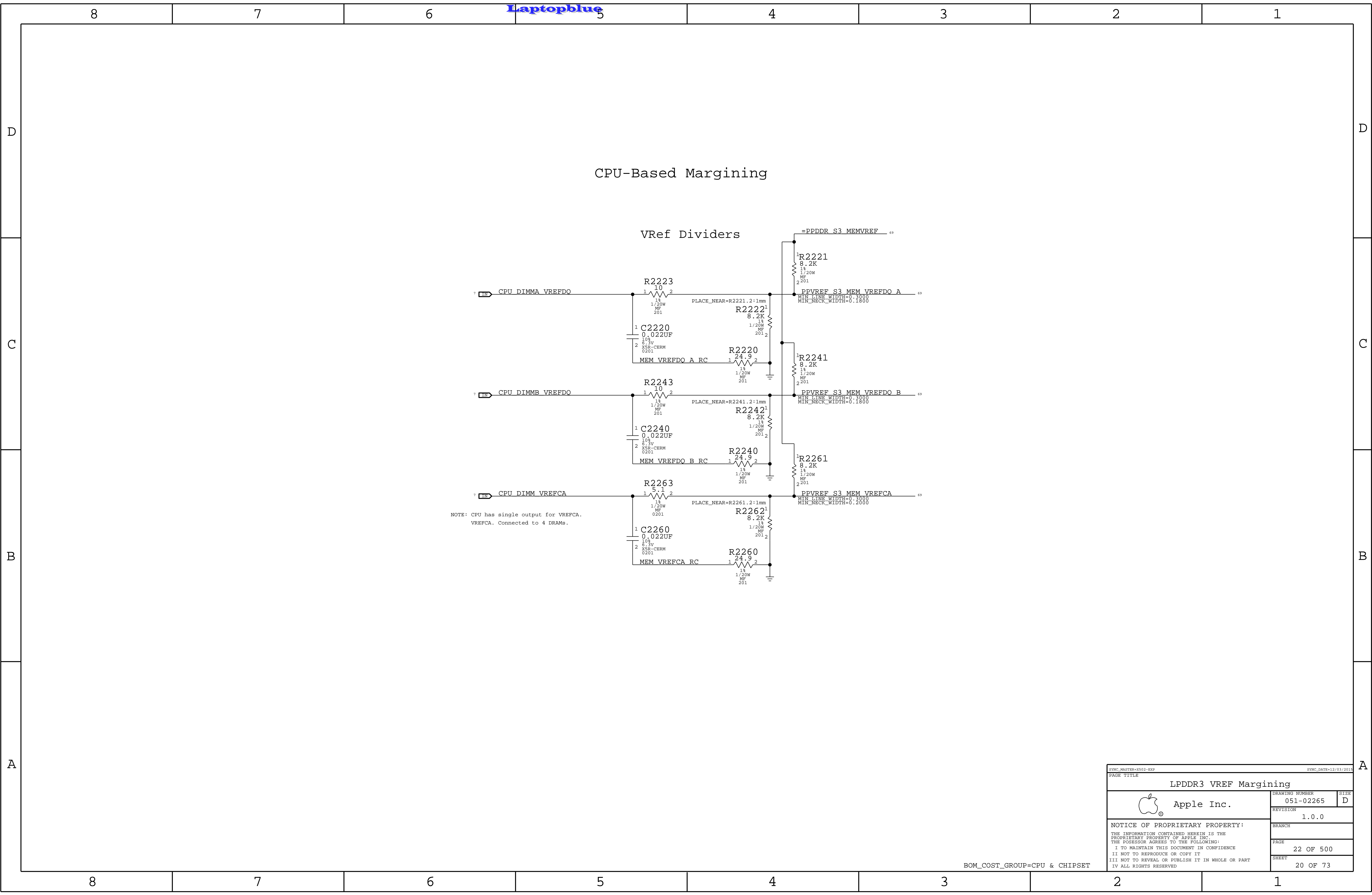
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BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=X502-EXP

SYNC_DATE=12/03/2015

PAGE TITLE

LPDDR3 VREF Margining

Apple Inc.

DRAWING NUMBER

051-02265

SIZE

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1.0.0

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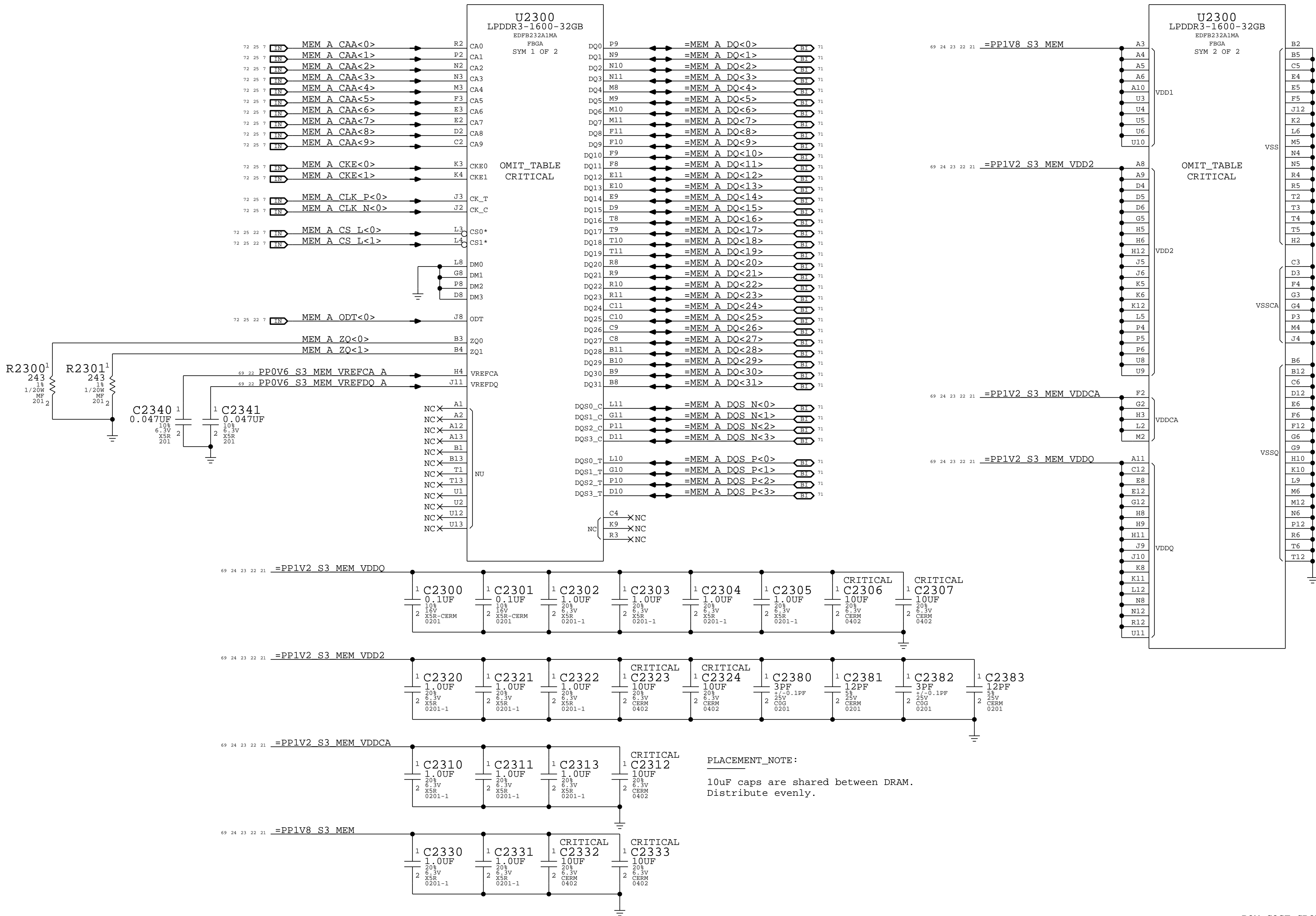
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20 OF 73

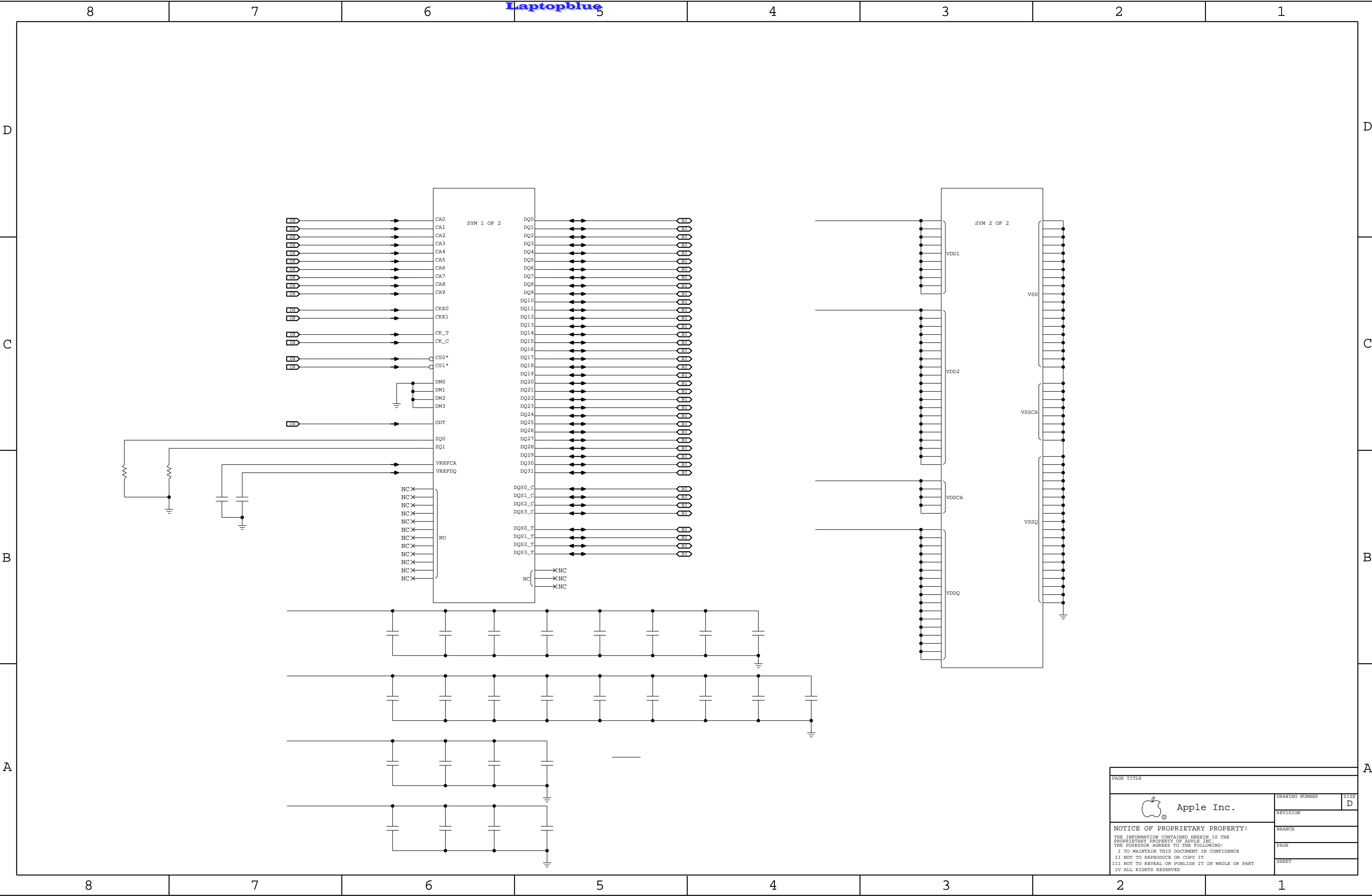
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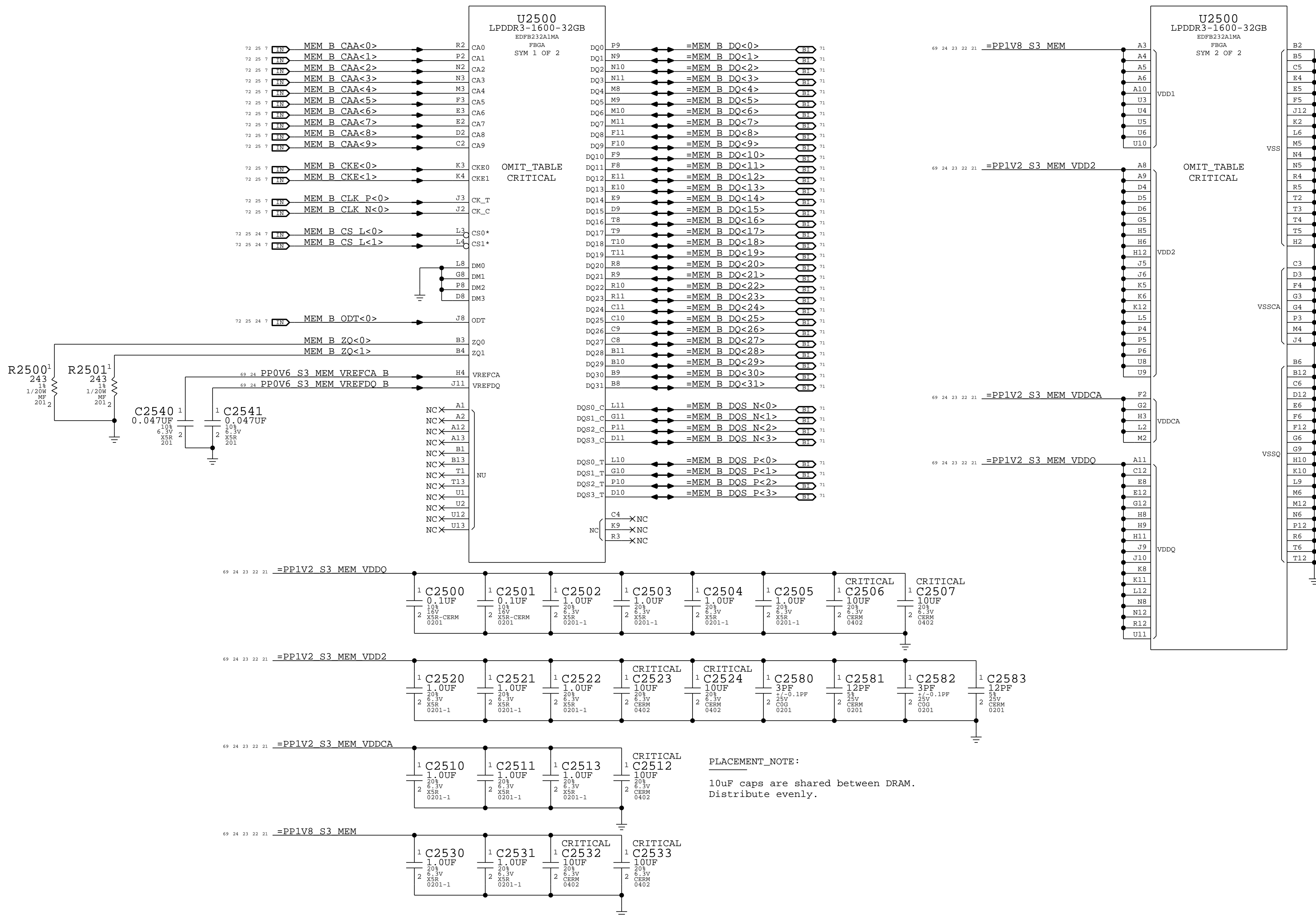
LPDDR3 CHANNEL A (0-31)




SYNC_MASTER=X502-EXE		SYNC_DATE=12/03/2015	
PAGE TITLE			
LPDDR3 DRAM Channel A		(00-31)	
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		PAGE	23 OF 500
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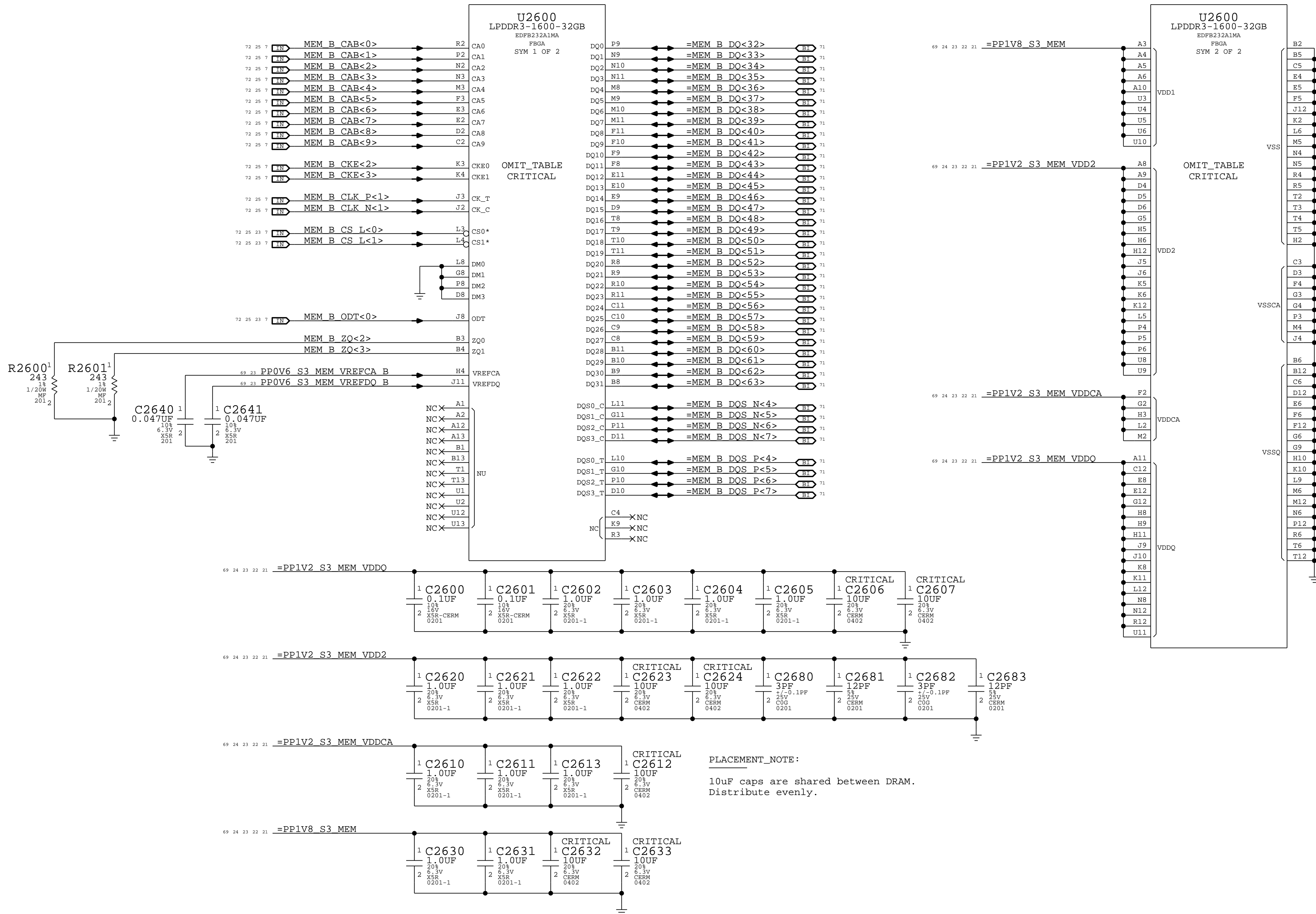


LPDDR3 CHANNEL B (0-31)




SYNC_MASTER=X502-EXP			SYNC_DATE=12/03/2015			
PAGE TITLE						
LPDDR3 DRAM Channel B (00-31)						
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			SHEET		23 OF 73	

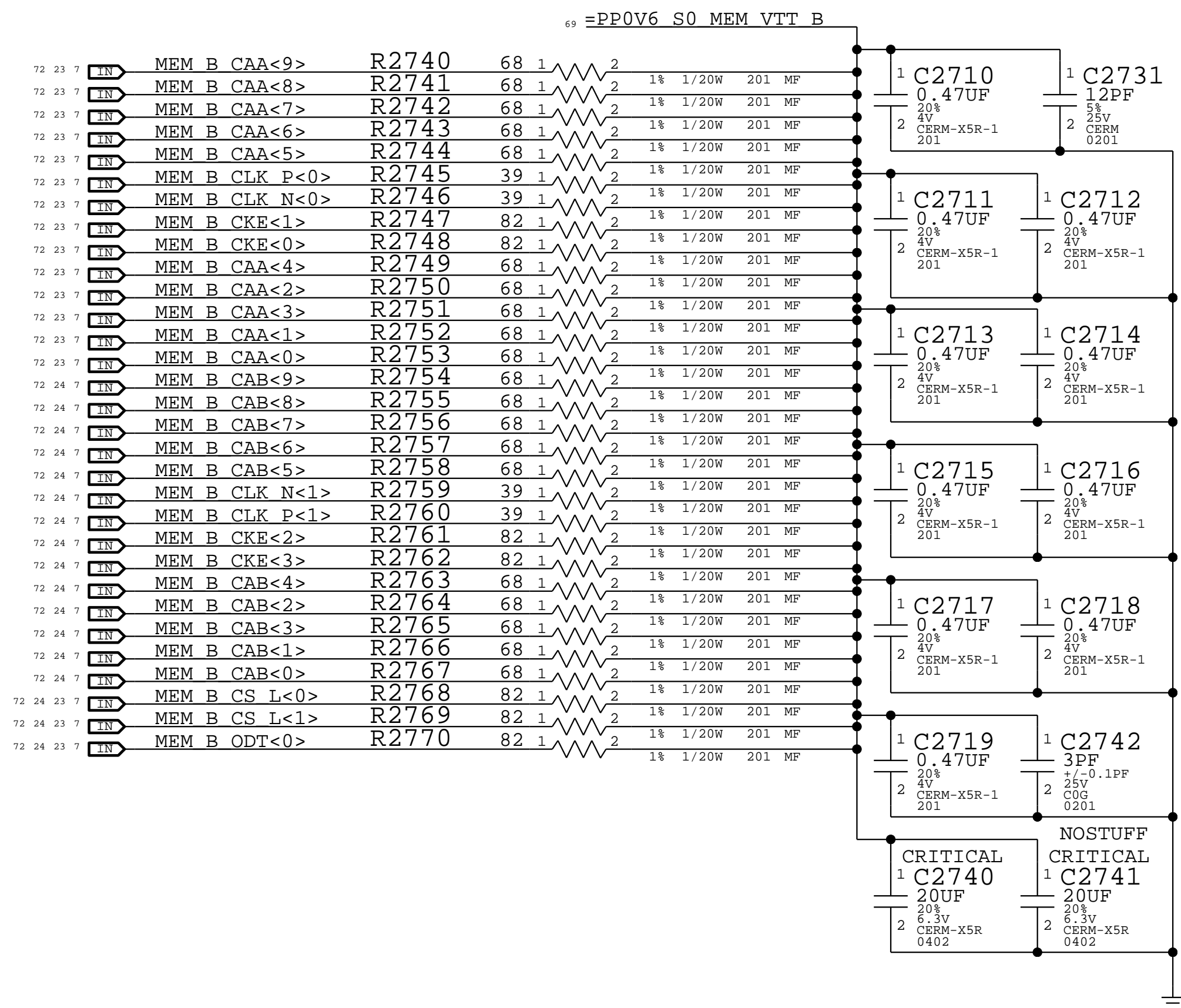
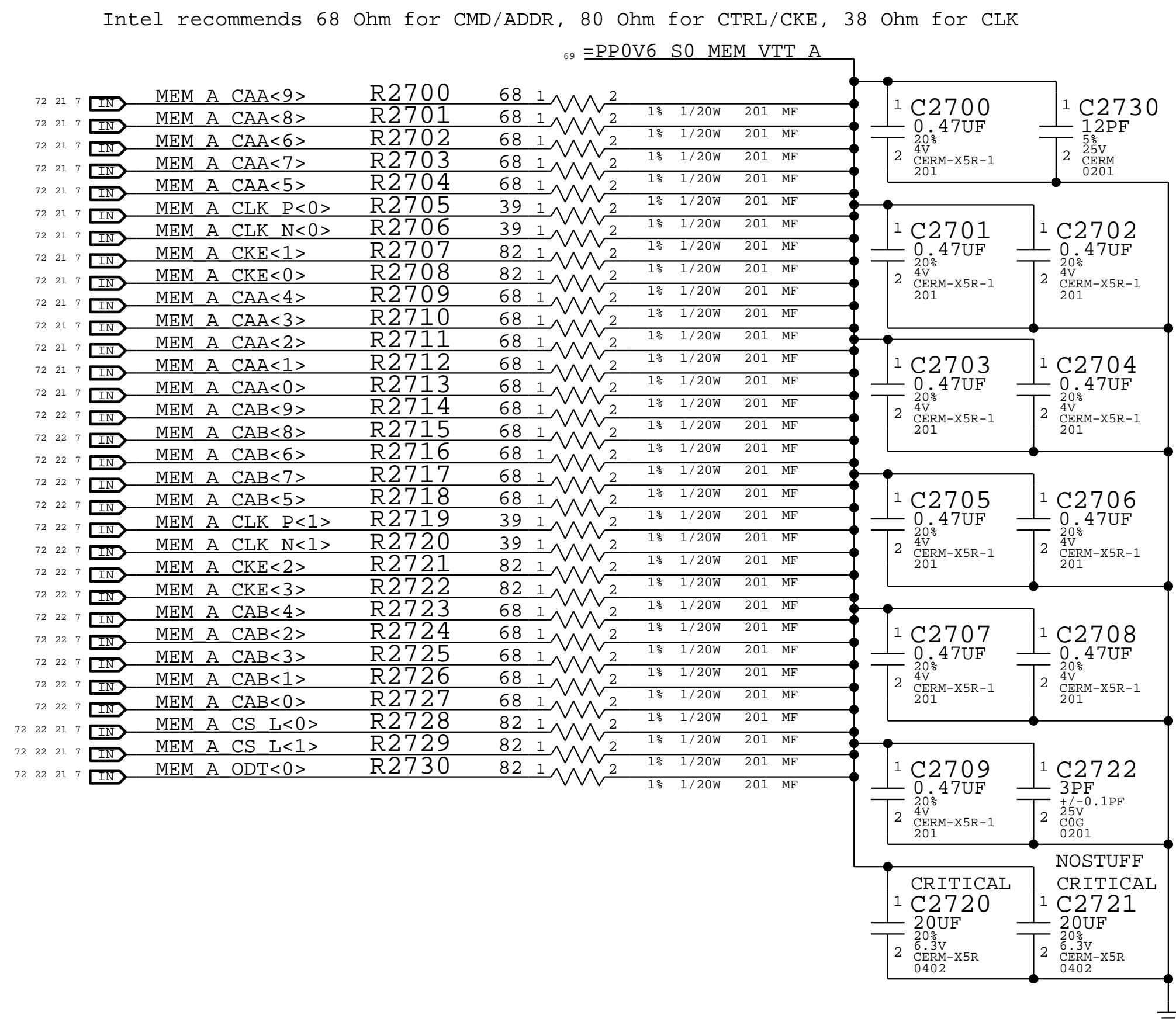
LPDDR3 CHANNEL B (32-63)

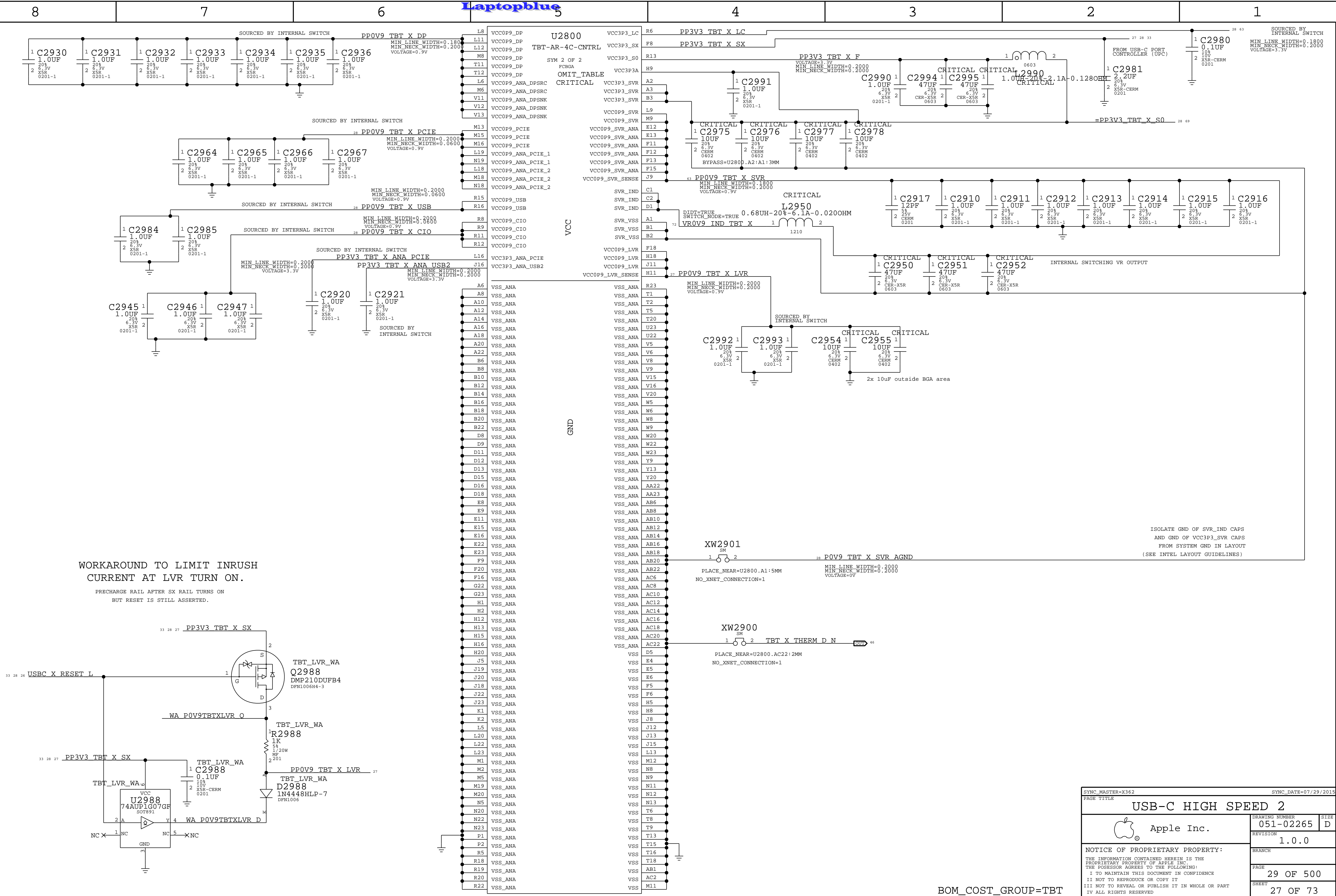


PLACEMENT_NOTE:
10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=X502-EXP		SYNC_DATE=12/03/2015	
PAGE TITLE			
LPDDR3 DRAM Channel B (32-63)			
	DRAWING NUMBER	051-02265	SIZE
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BOM_COST_GROUP=DRAM





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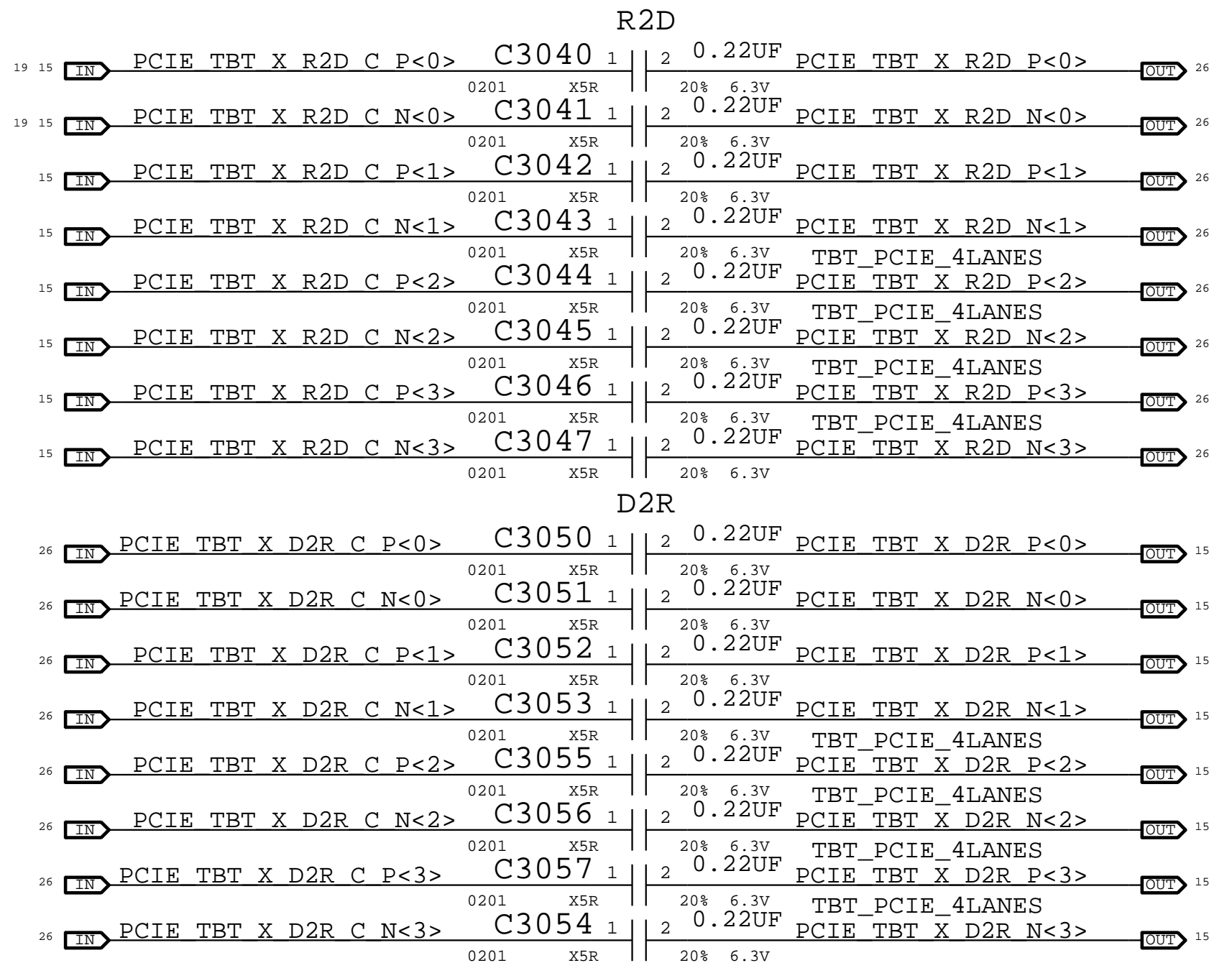
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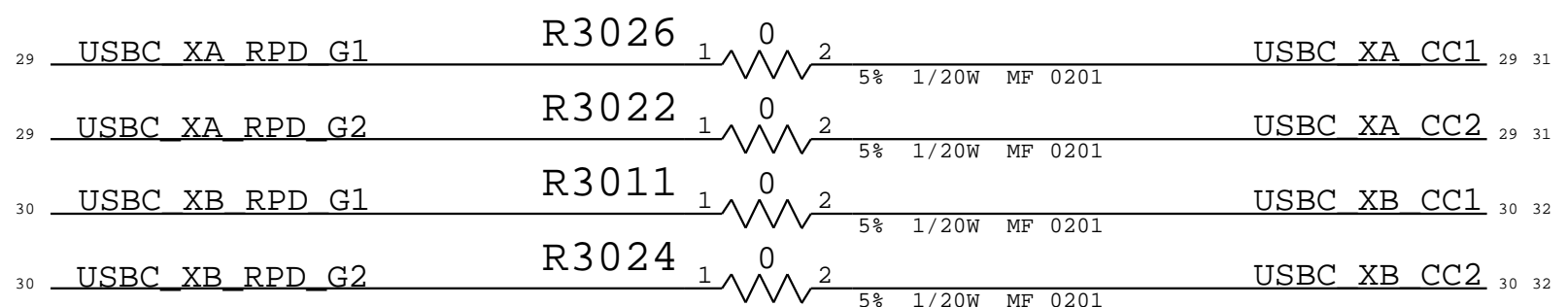
A

RIDGE AC COUPLING

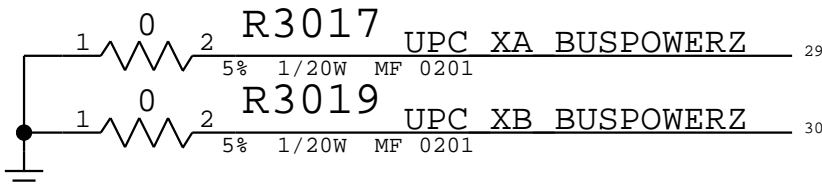


ACE RPD STRAPPING

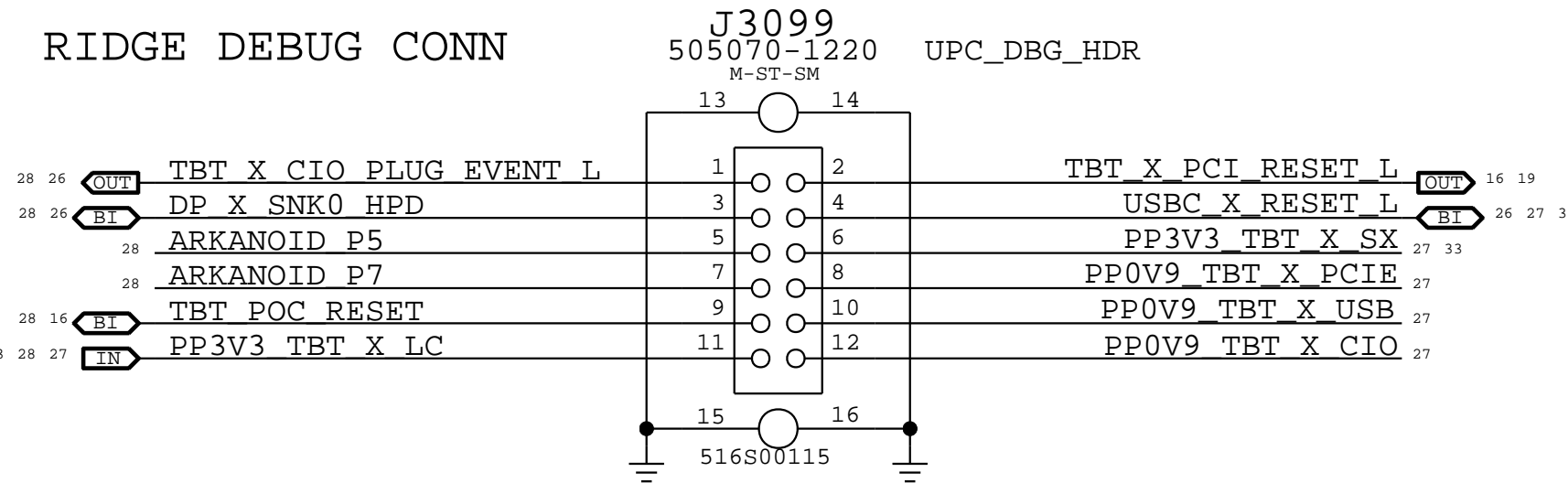
CONNECT G1/G2 TO CC1/CC2 TO RECEIVE POWER UNDER DB CASE
CONNECT G1/G2 TO GND TO NOT RECEIVE POWER UNDER DB CASE



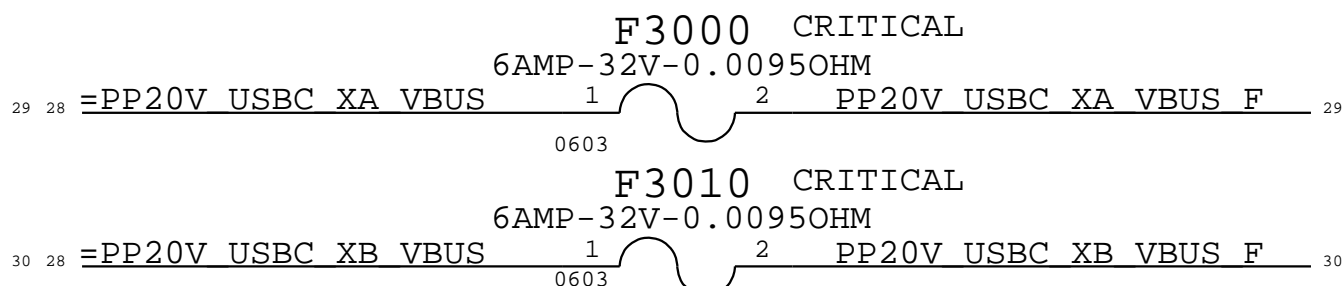
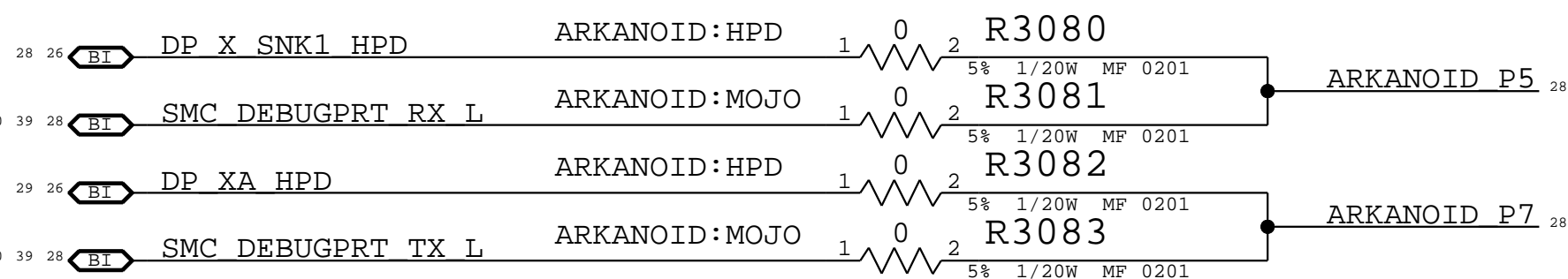
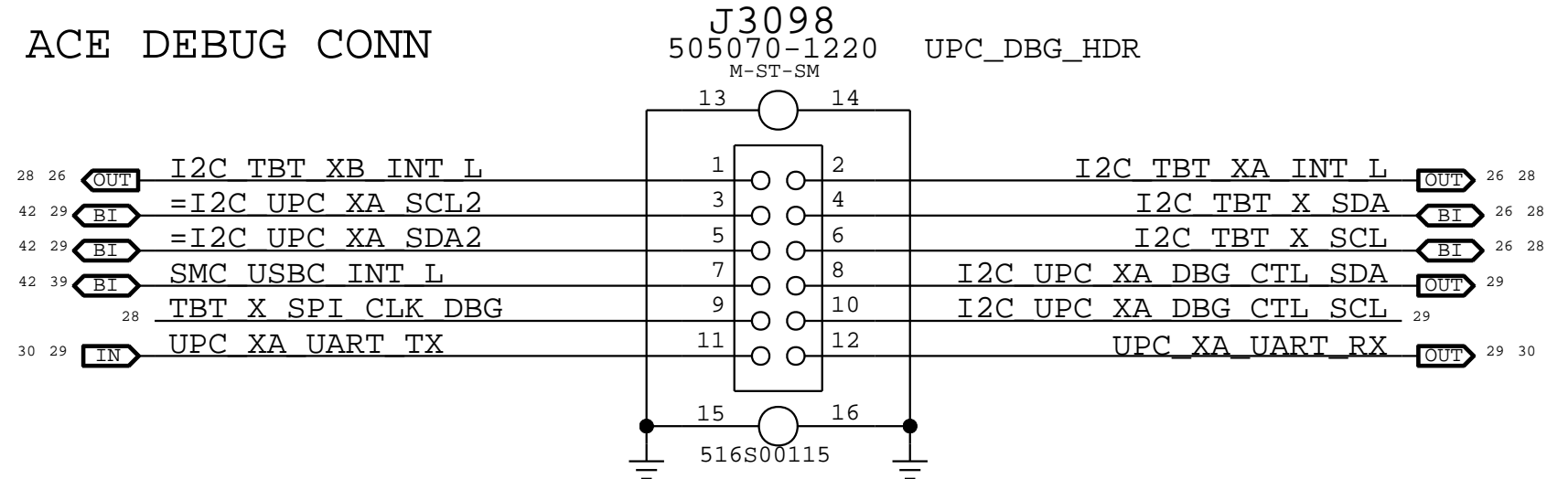
ACE BUSPOWERZ STRAPPING



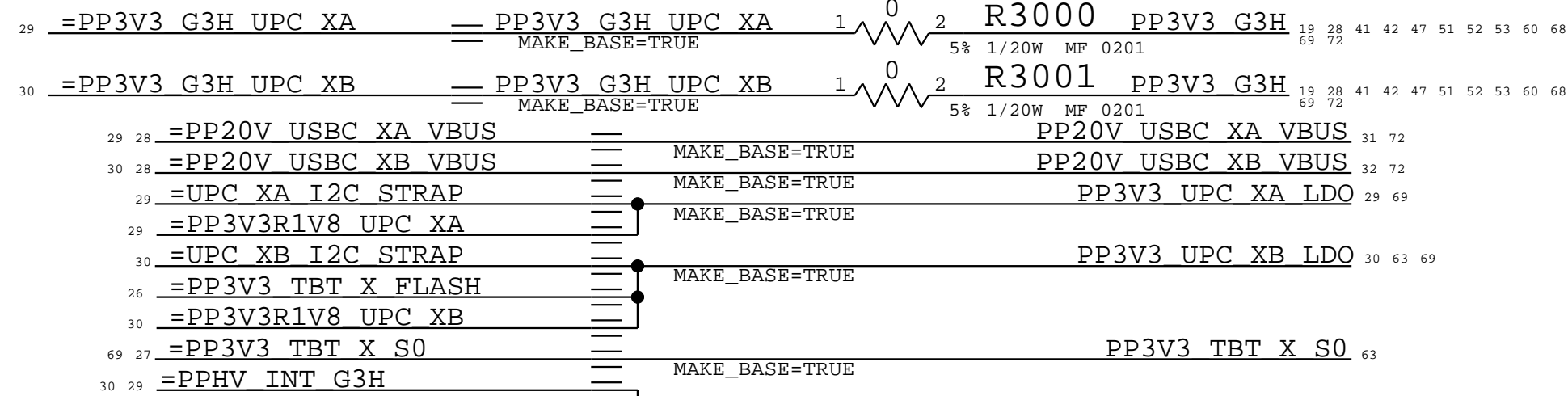
RIDGE DEBUG CONN



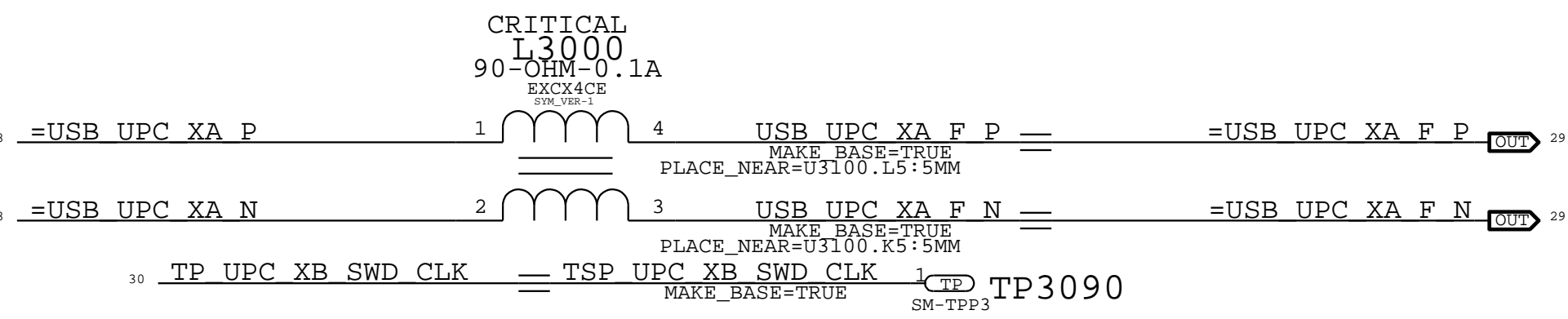
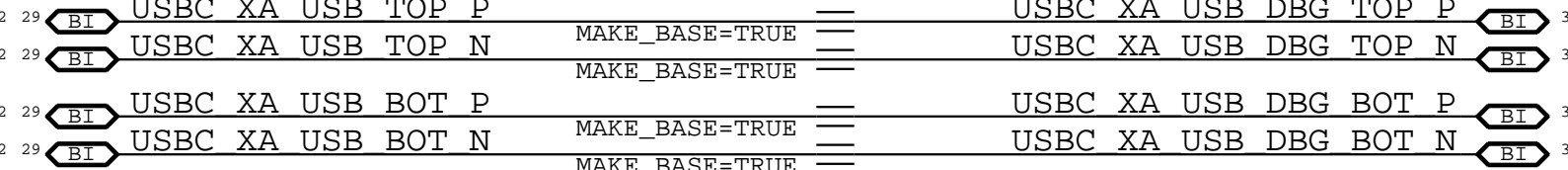
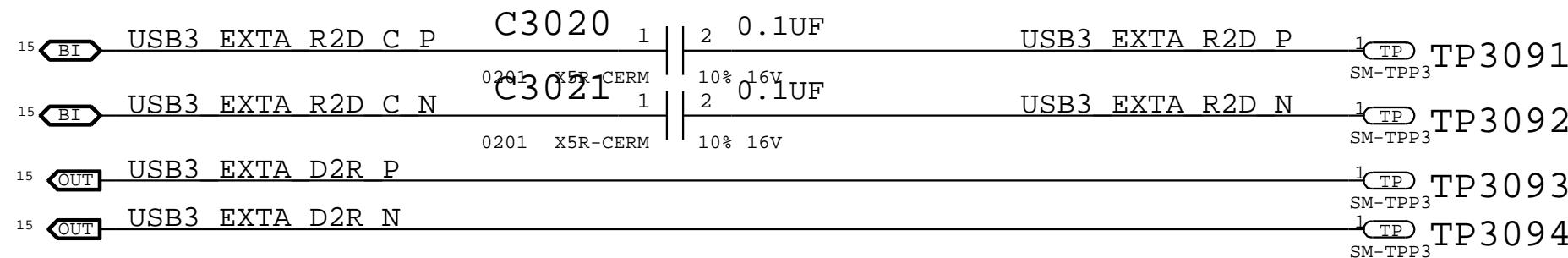
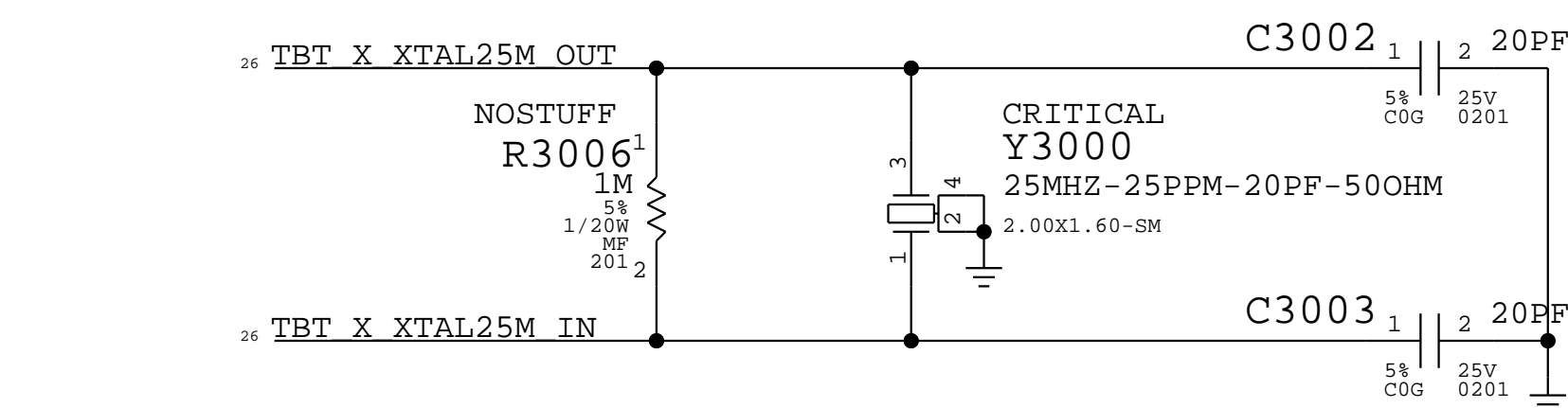
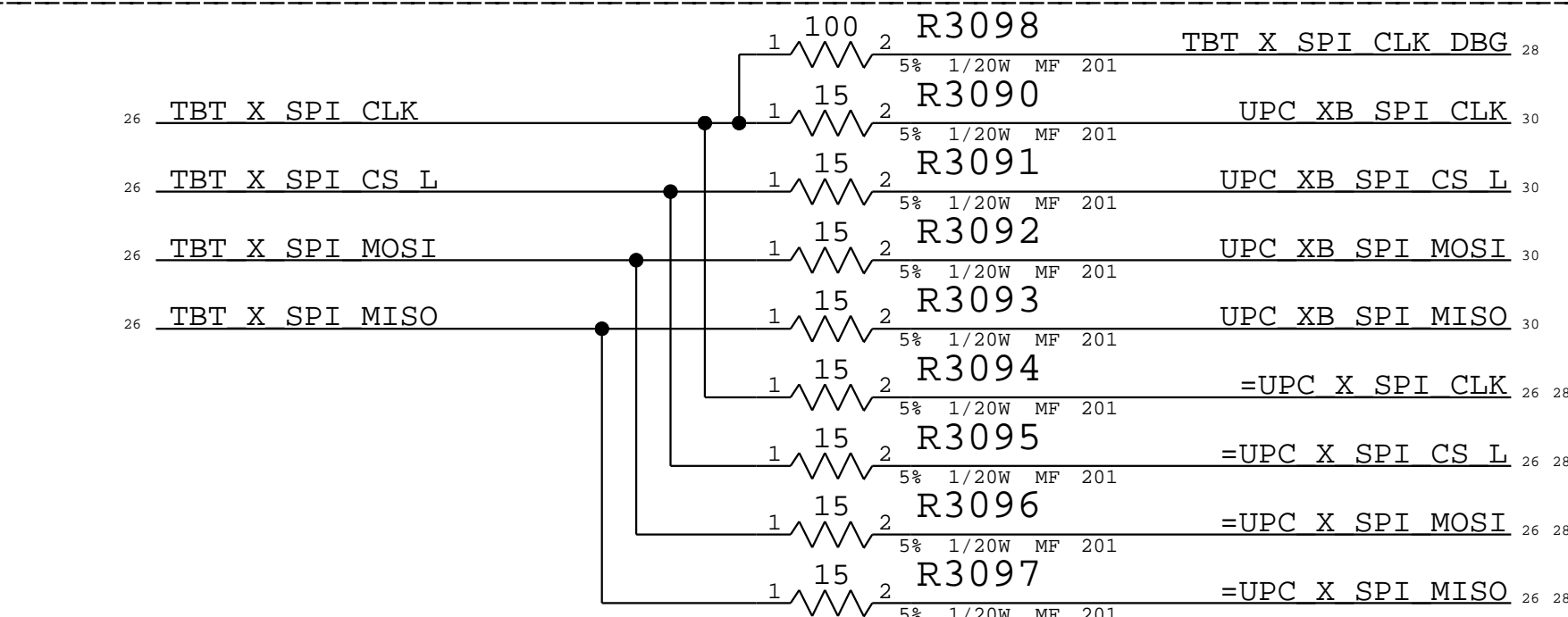
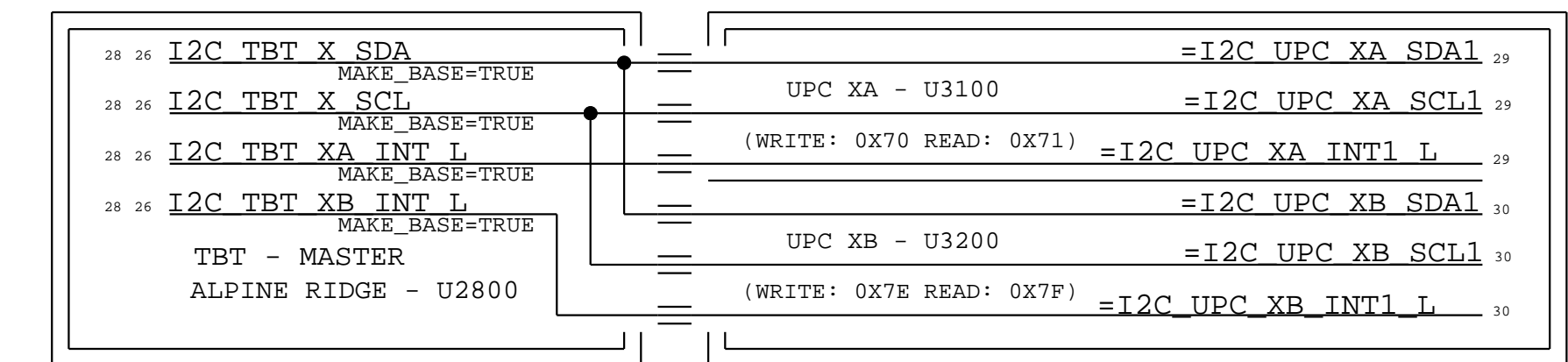
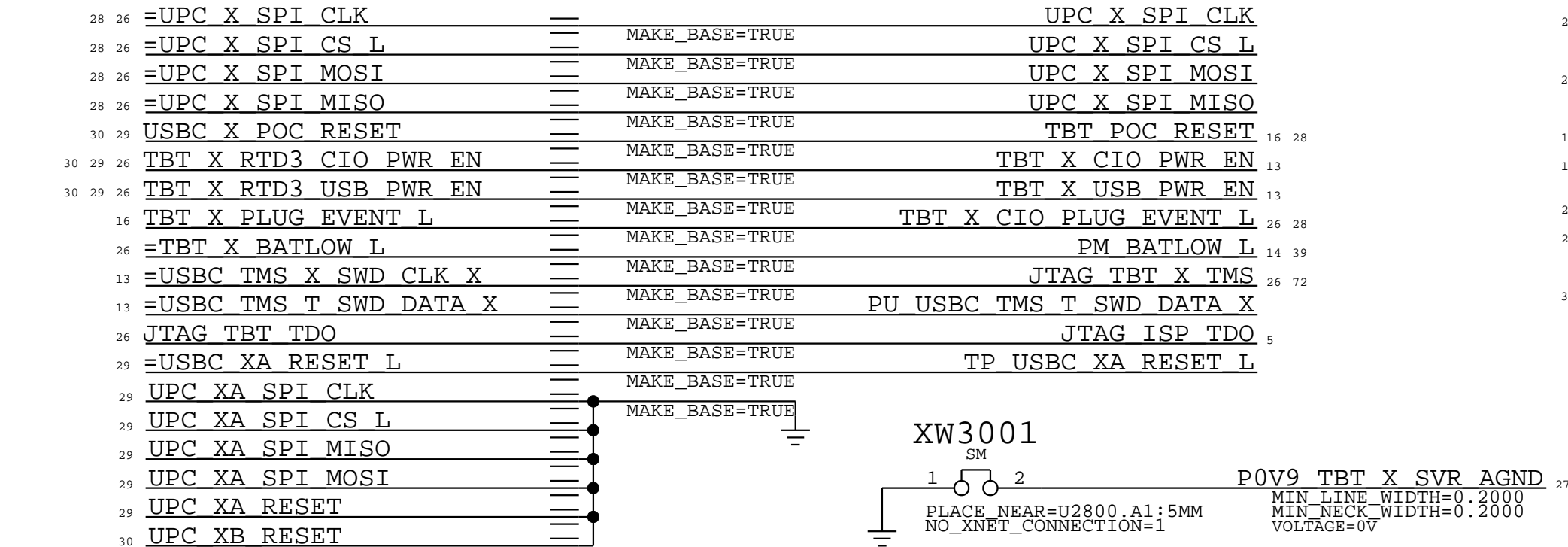
ACE DEBUG CONN



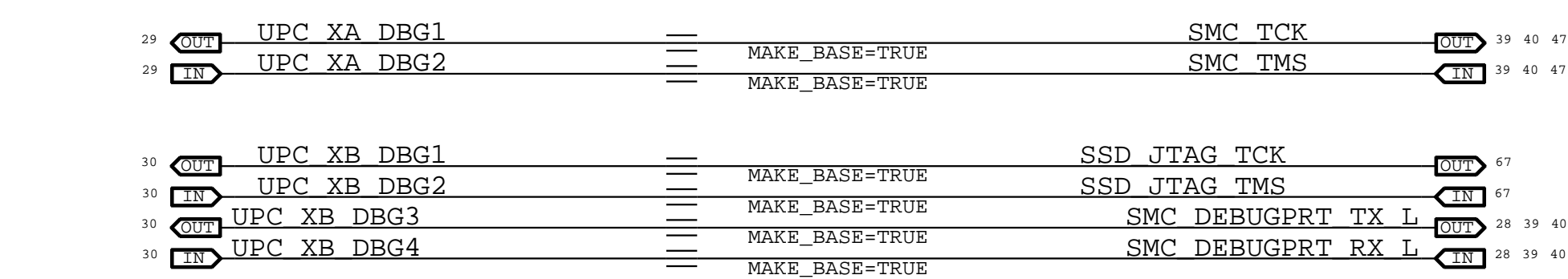
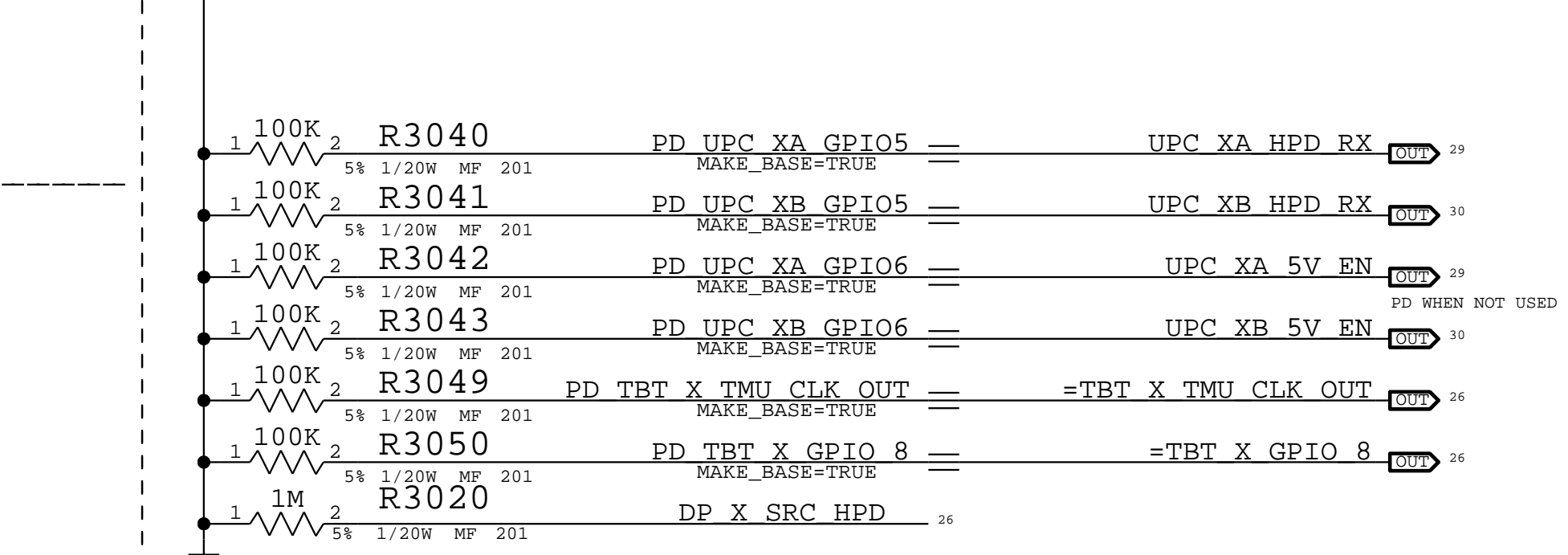
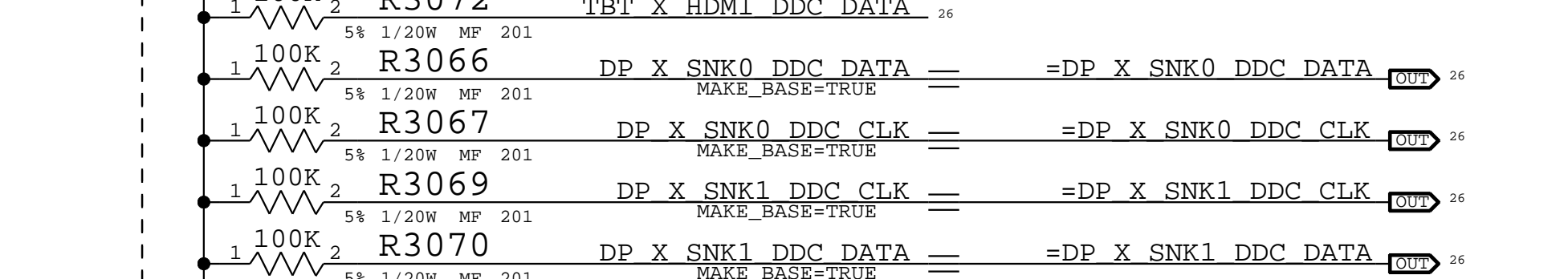
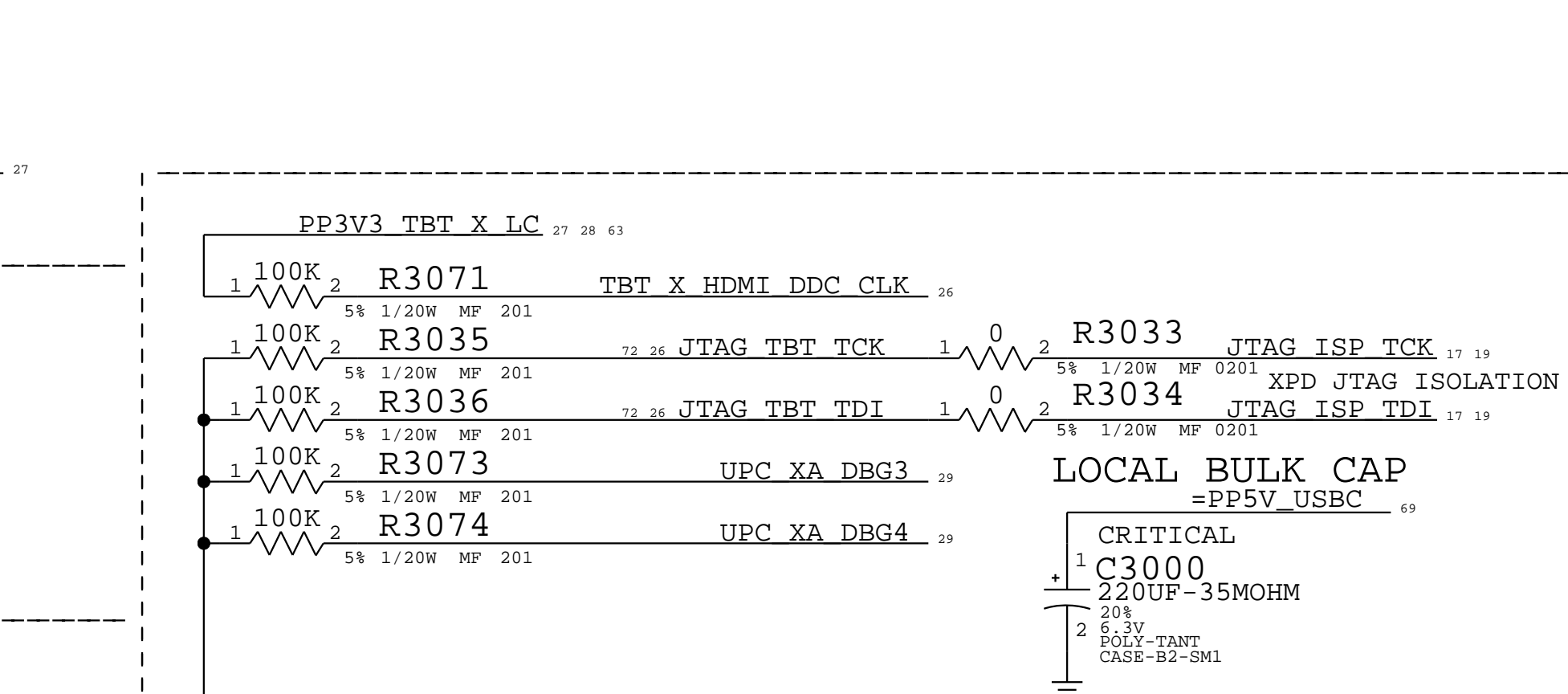
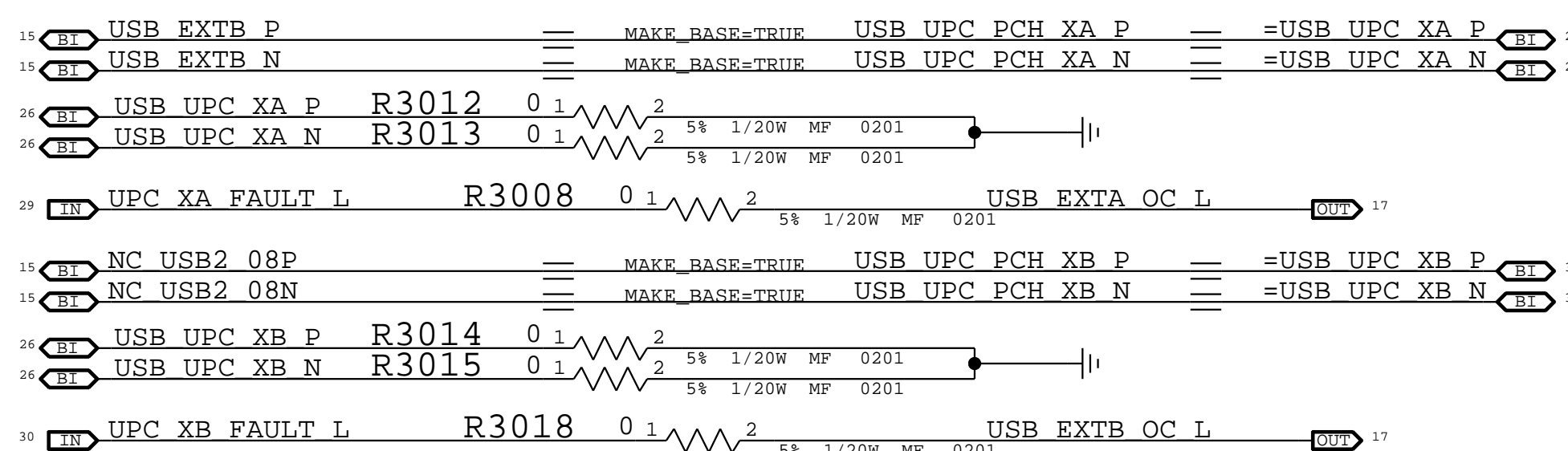
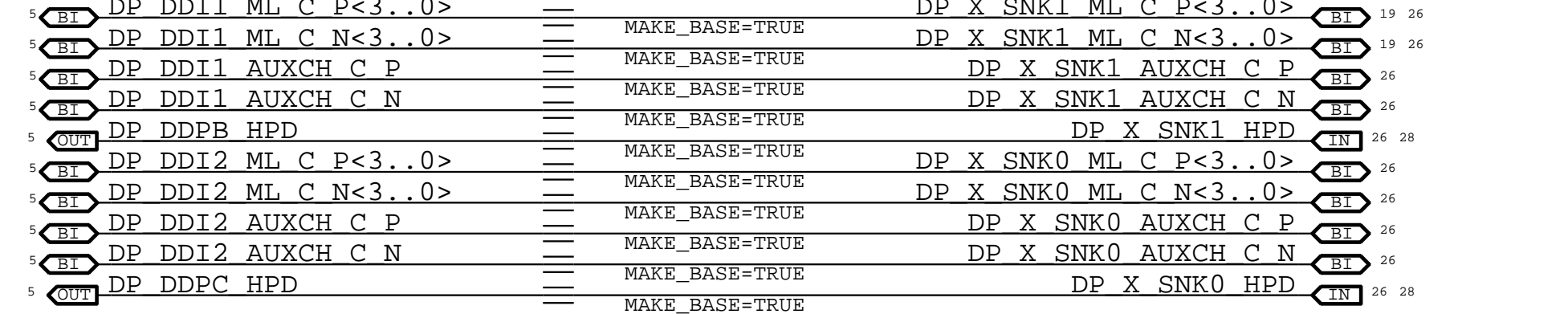
POWER ALIASES




MISC ALIASES



DP / USB SOURCE ALIASES

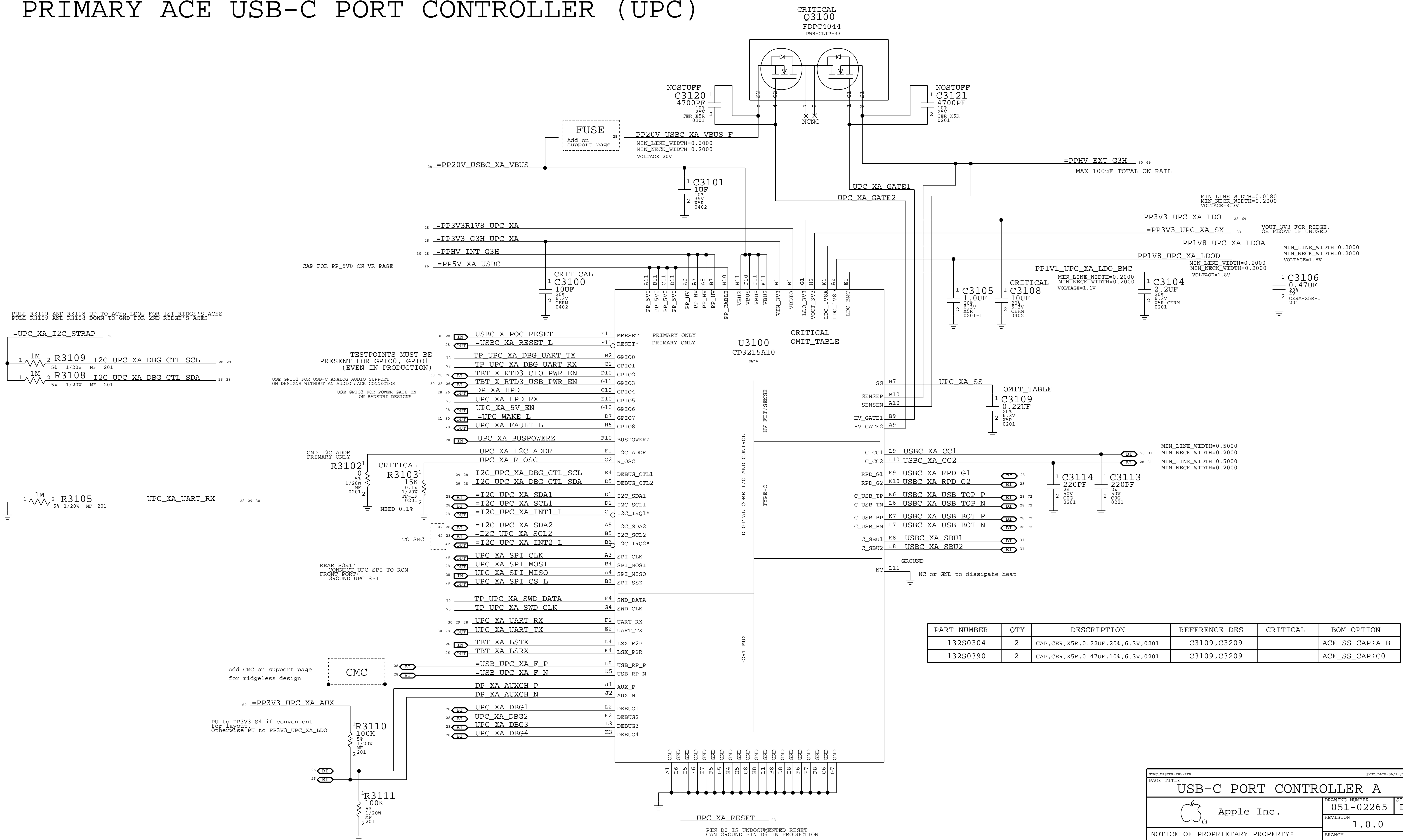


DESIGN: X502/MLB CATZ
LAST CHANGE: Fri Aug 5 13:34:33 2016

PAGE TITLE		
USB-C SUPPORT		
 Apple Inc.	DRAWING NUMBER	051-02265
	REVISION	1.0.0
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	SHEET	28 OF 73

BOM_COST_GROUP=USB-C

PRIMARY ACE USB-C PORT CONTROLLER (UPC)

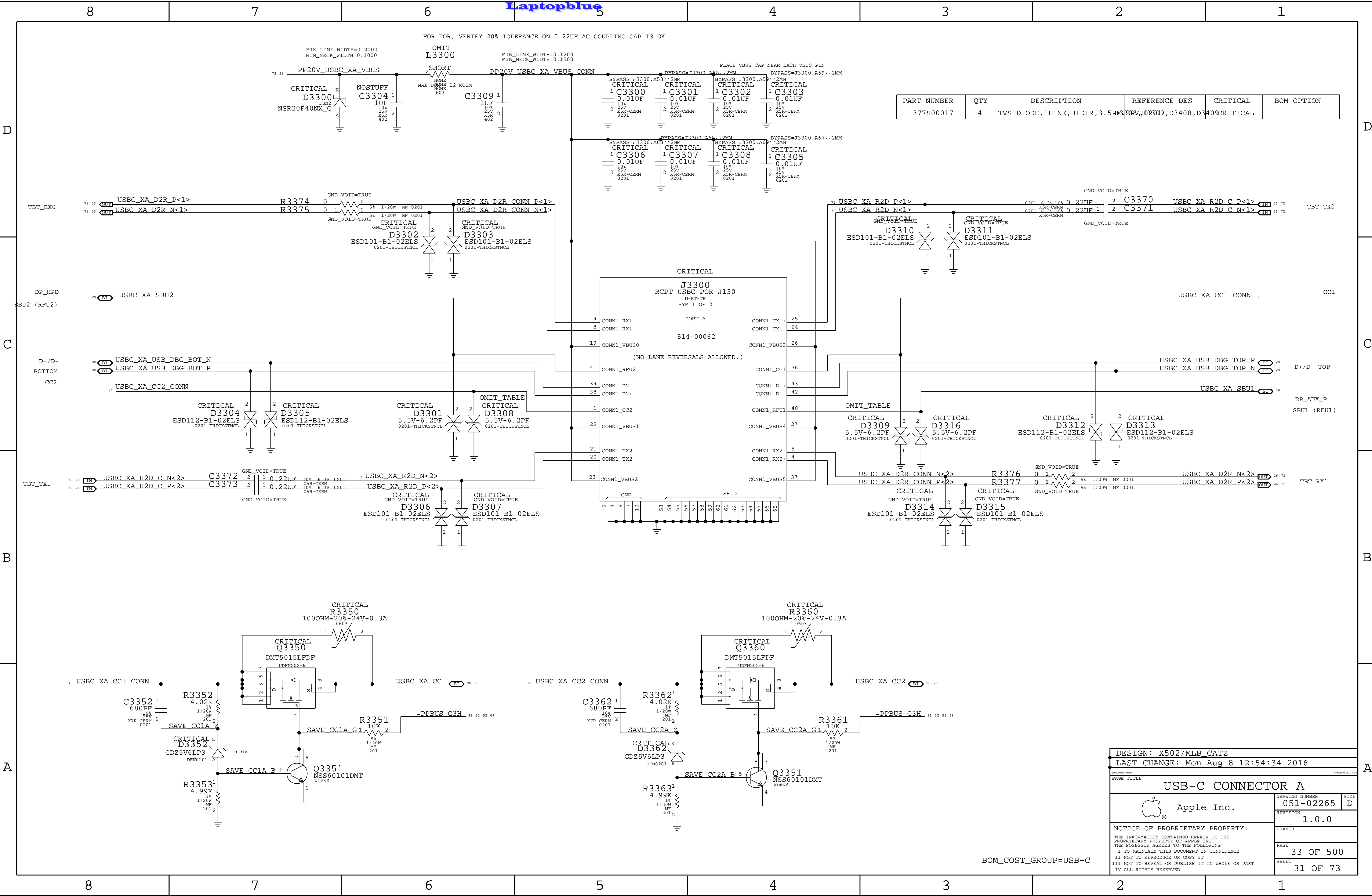


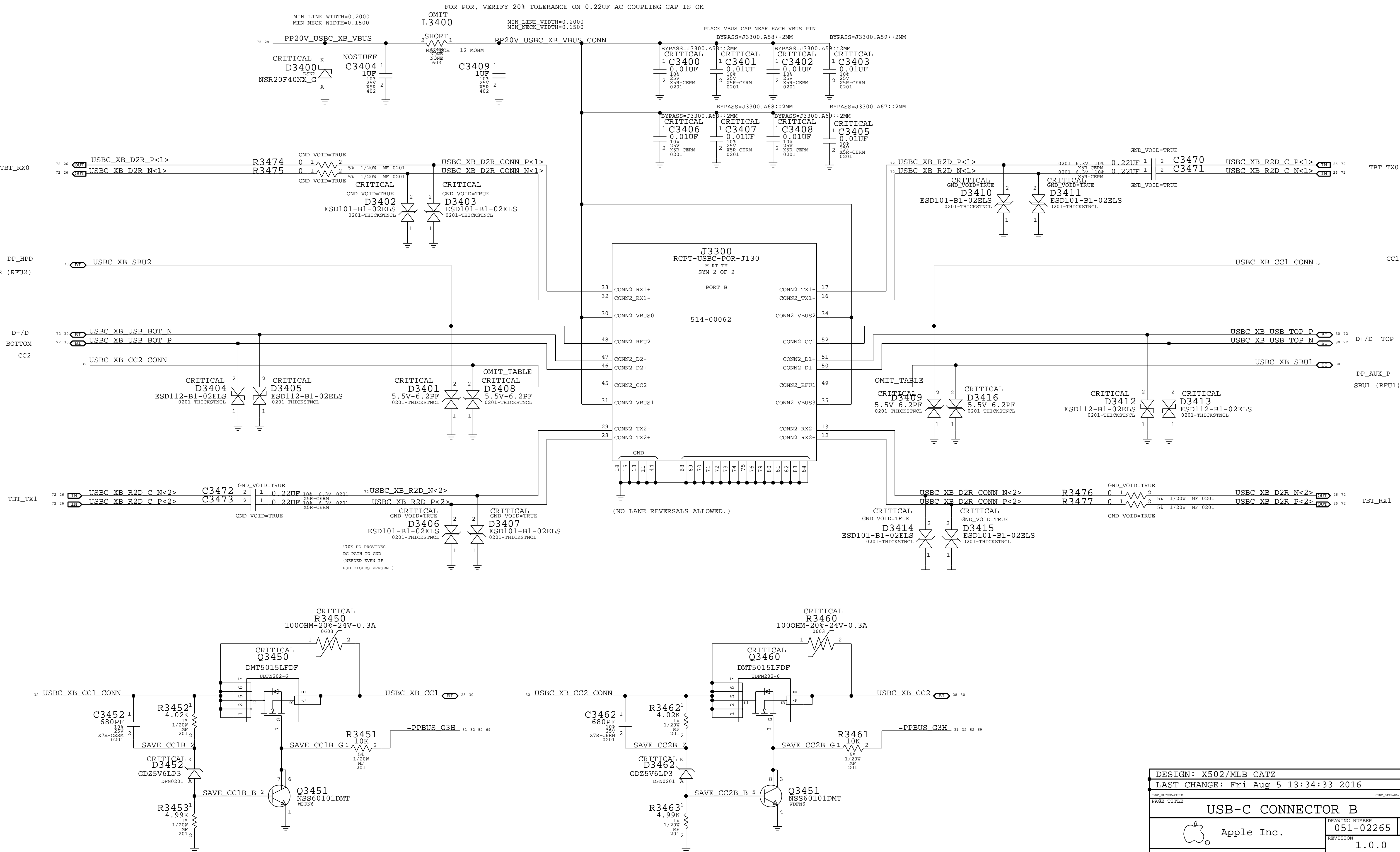
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
132S0304	2	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C3109,C3209		ACE_SS_CAP:A_B
132S0390	2	CAP,CER,X5R,0.47UF,10%,6.3V,0201	C3109,C3209		ACE_SS_CAP:C0

PAGE TITLE		DRAWING NUMBER		SIZE
USB-C PORT CONTROLLER A		051-02265		D
Apple Inc.		REVISION		1.0.0
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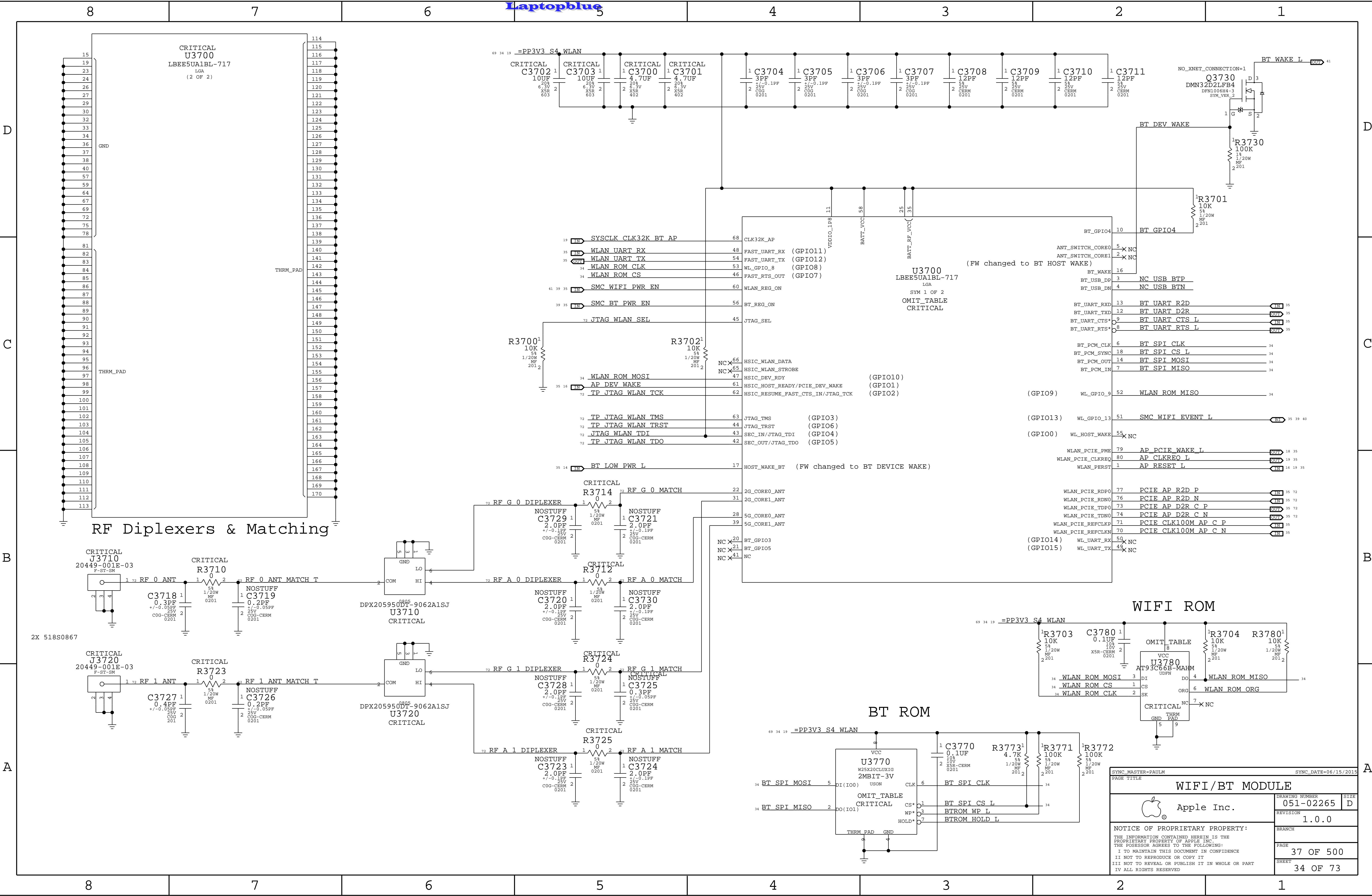
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BOM_COST_GROUP=USB-C










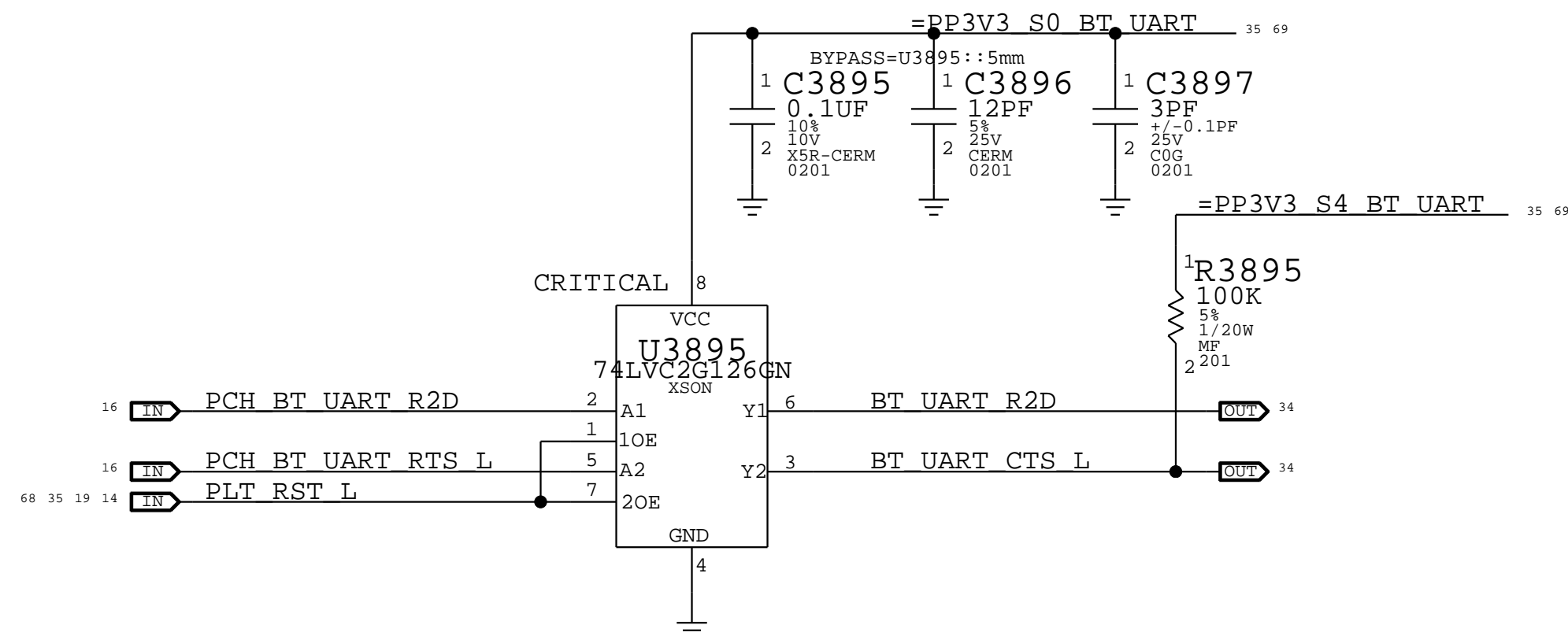
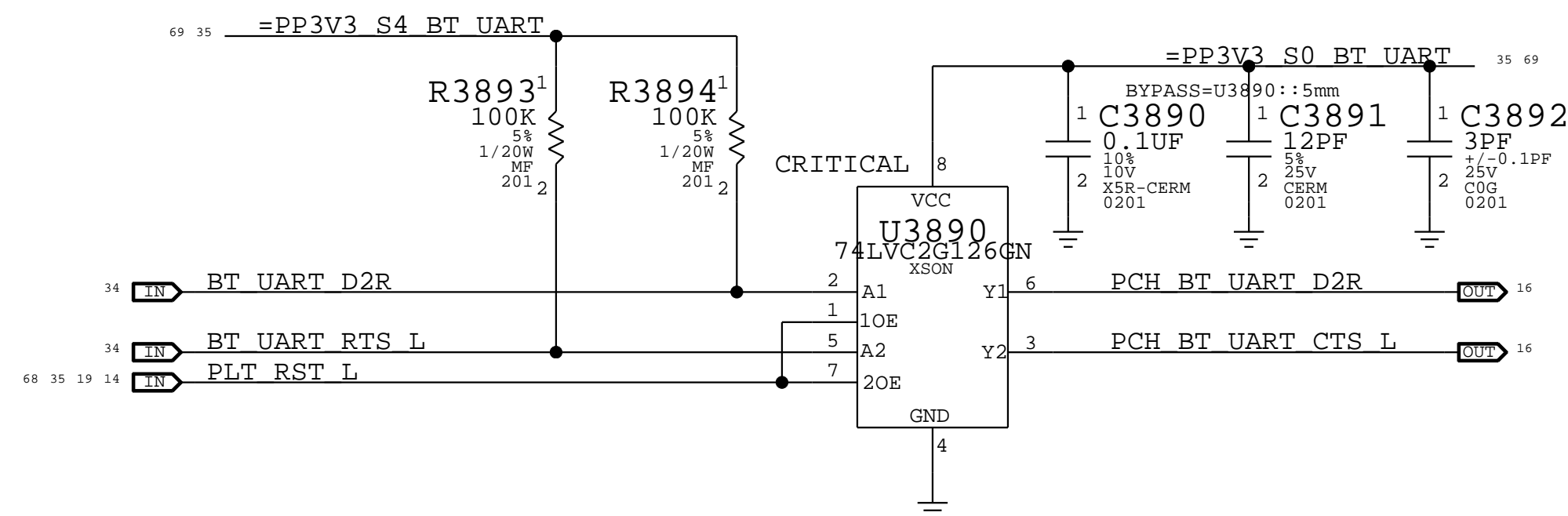
RF Diplexers & Matching

WIFI ROM

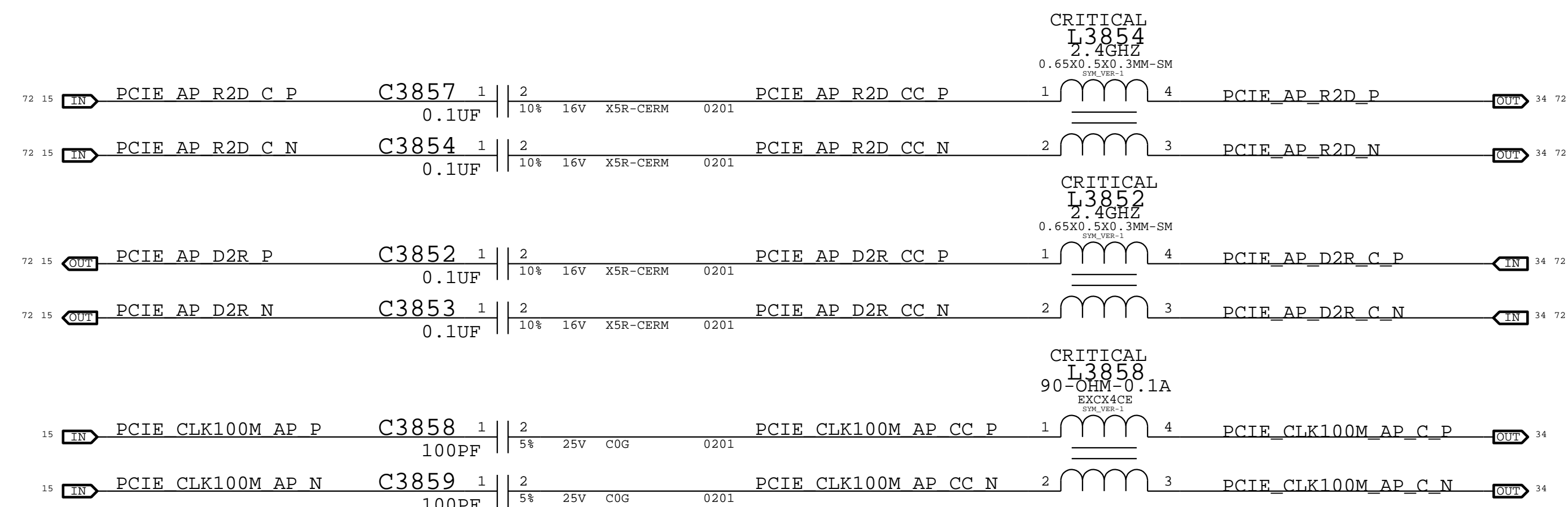
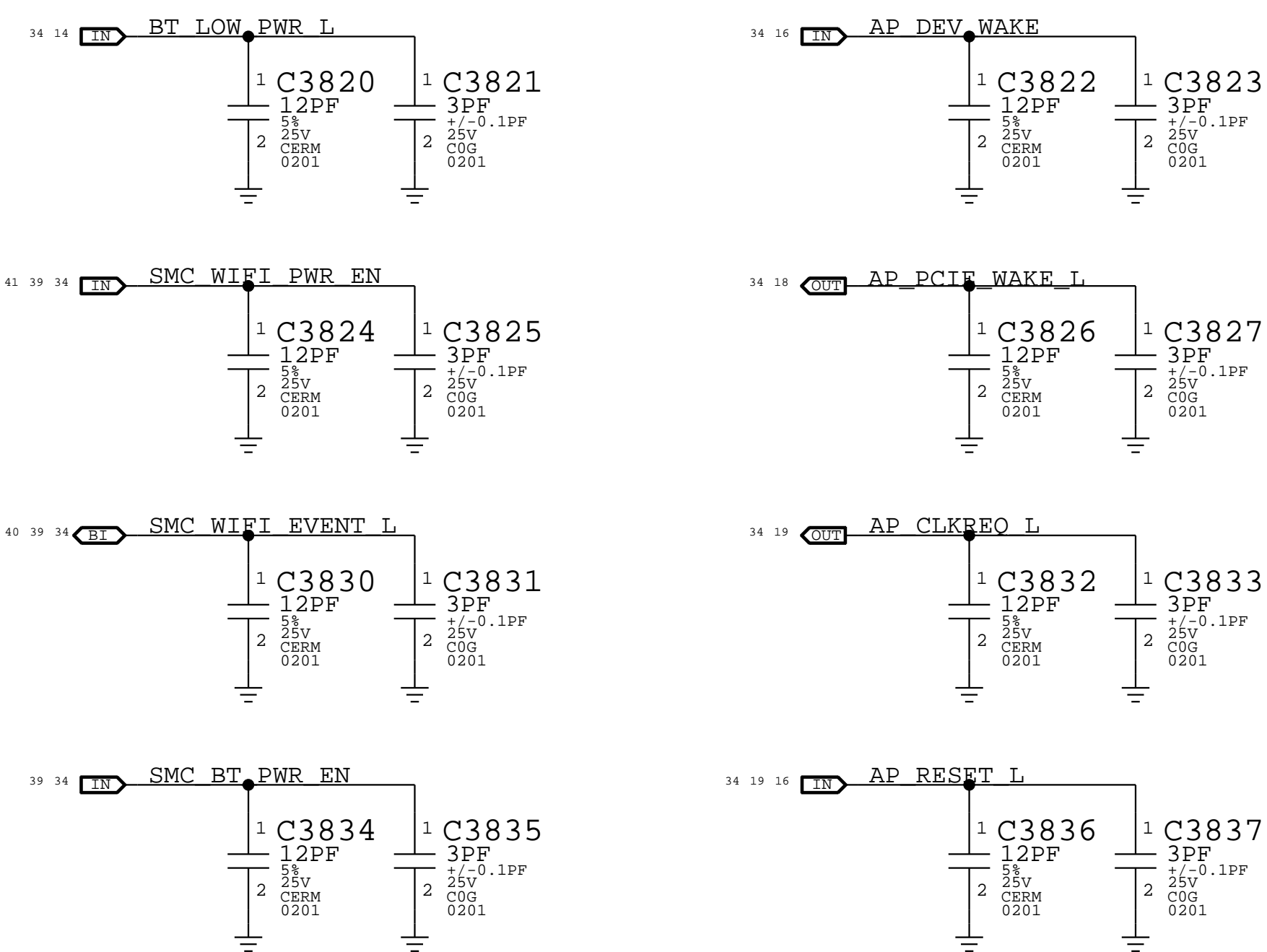
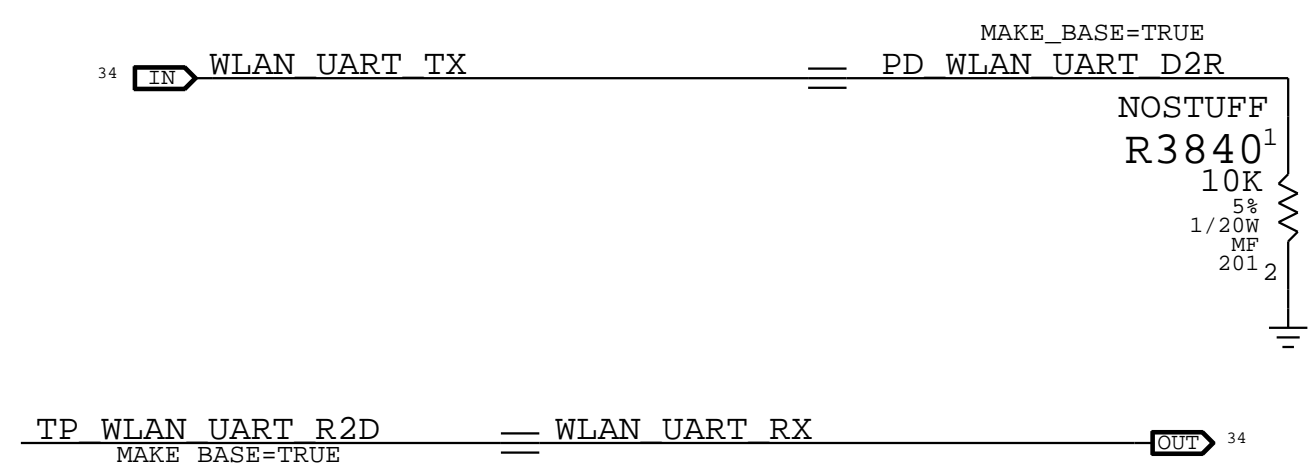
BT ROM


SYNC_MASTER=PAULM		SYNC_DATE=06/15/2015	
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WIFI/BT MODULE			
	Apple Inc.	DRAWING NUMBER	051-02265
		REVISION	1.0.0
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		PAGE	37 OF 500
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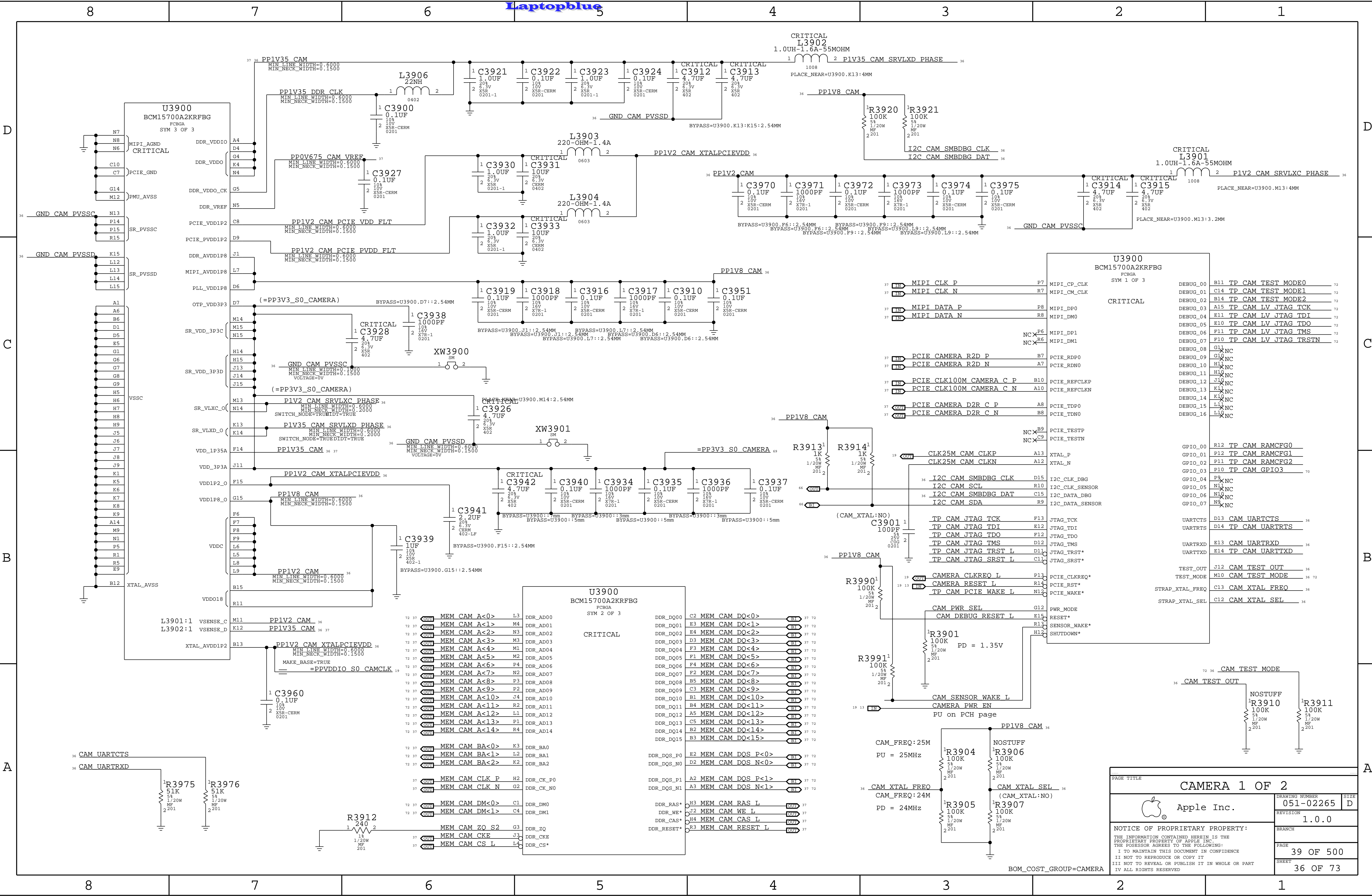
BT UART Isolation

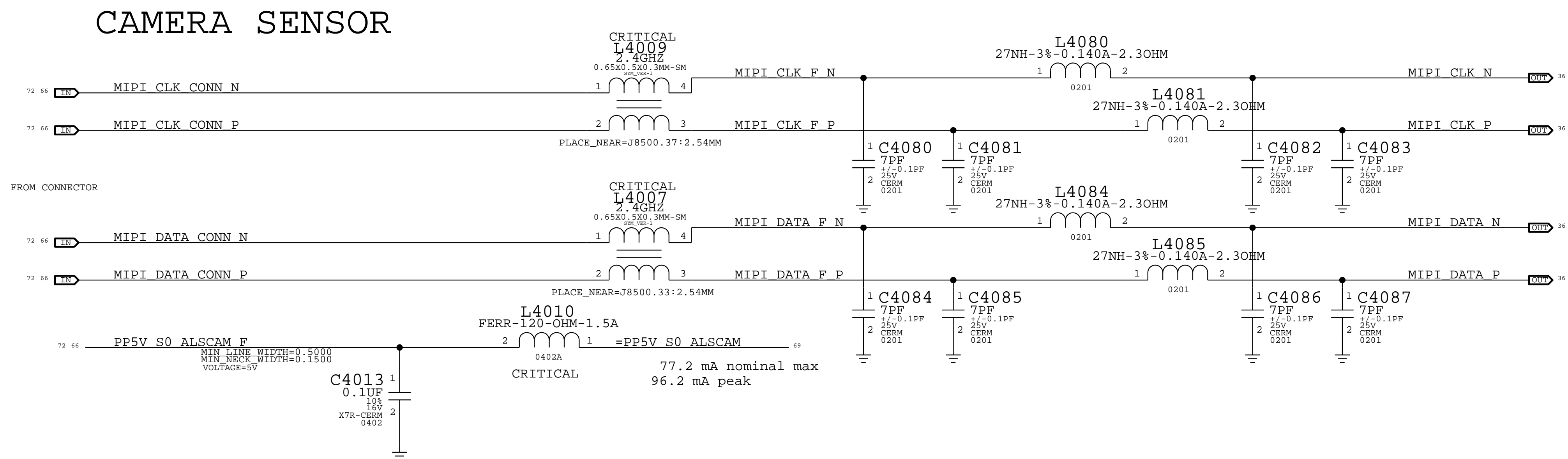
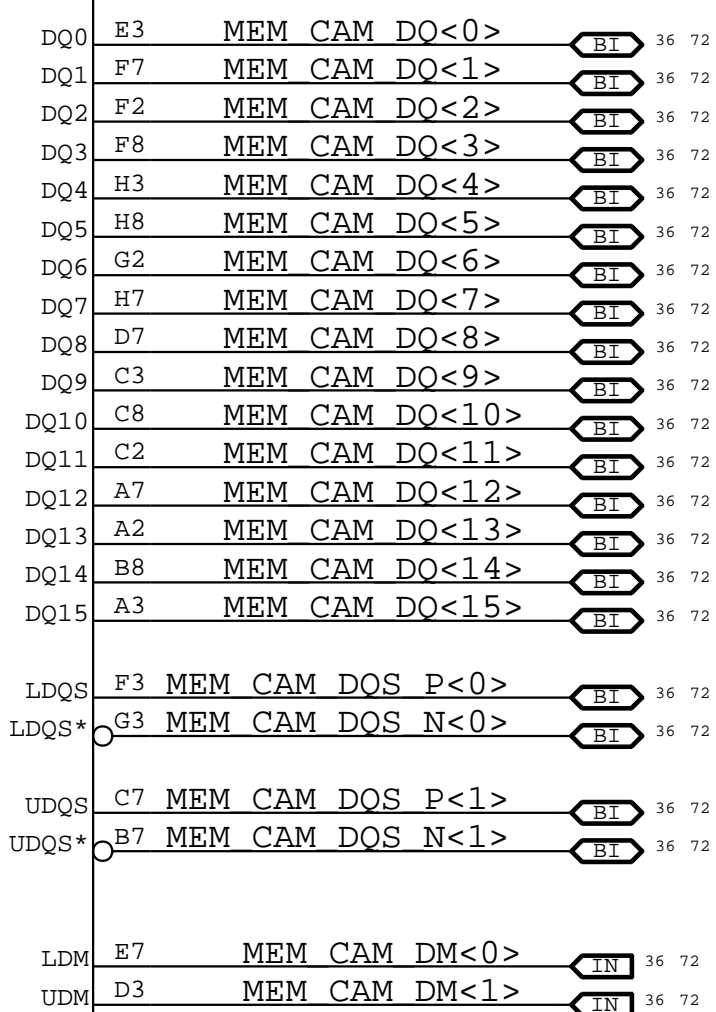
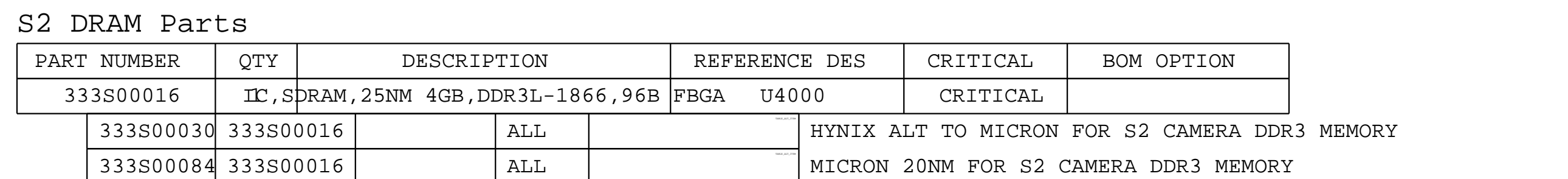
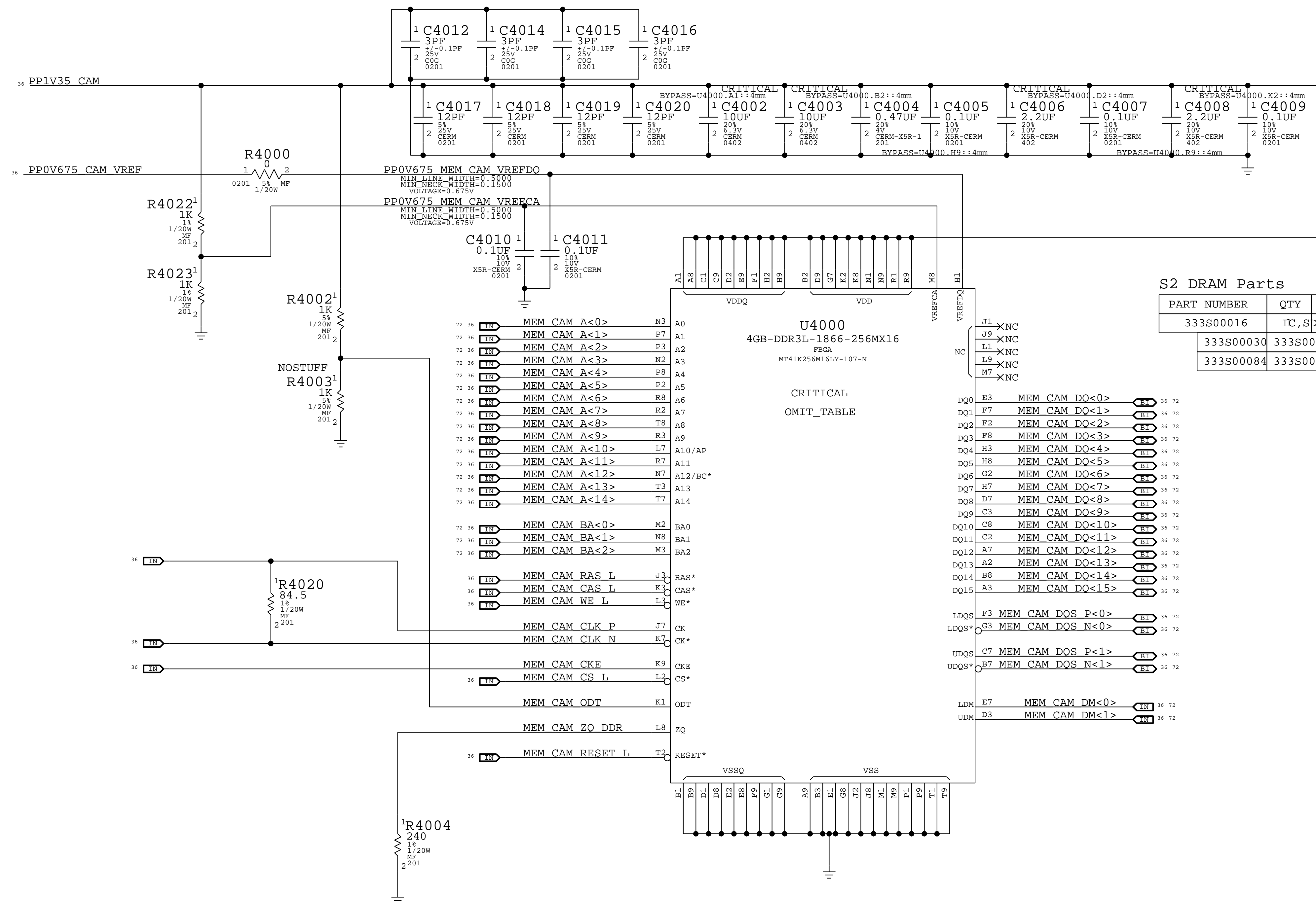



WIFI UART ISOLATION



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WIFI/BT Module Support			
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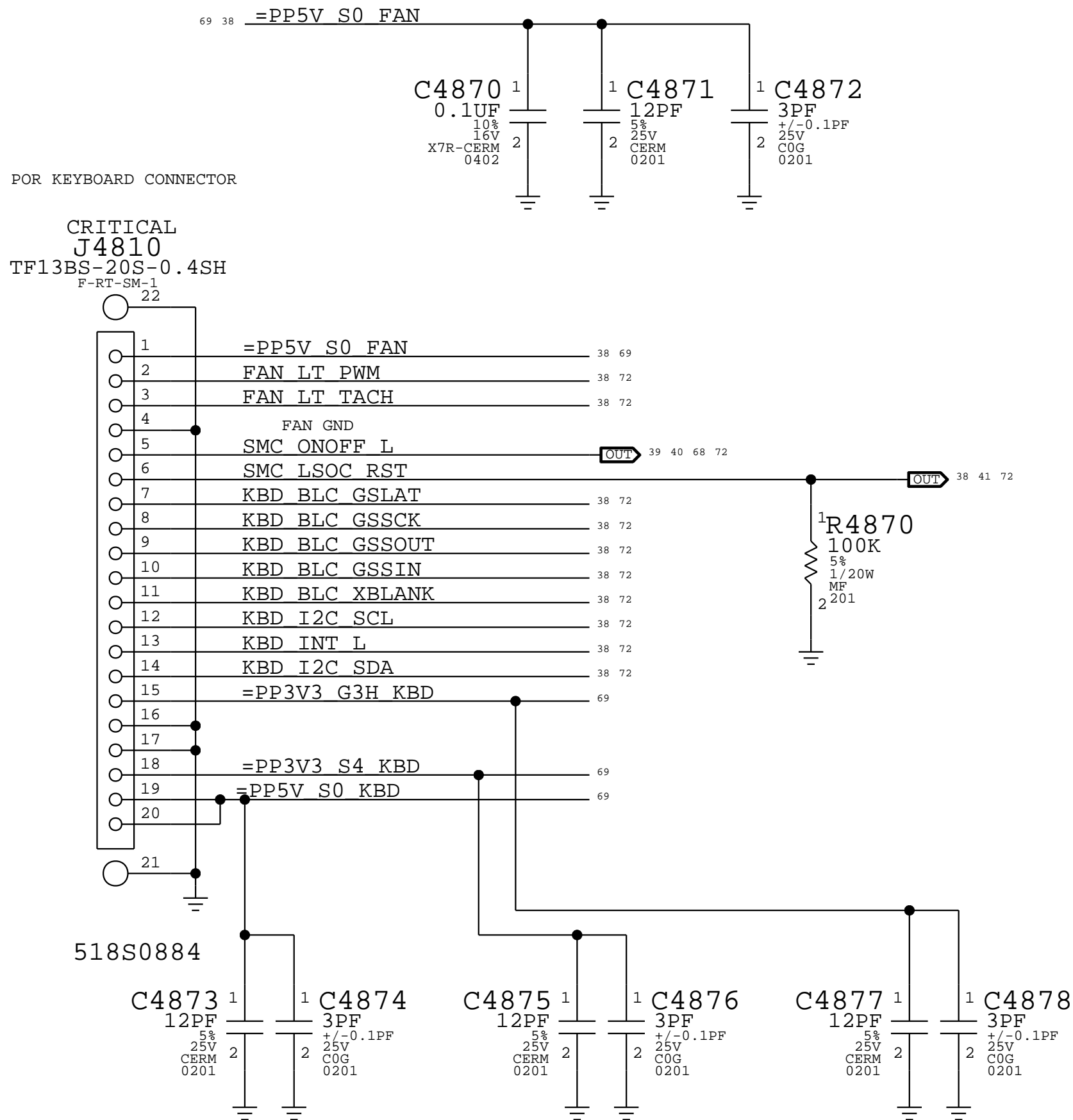




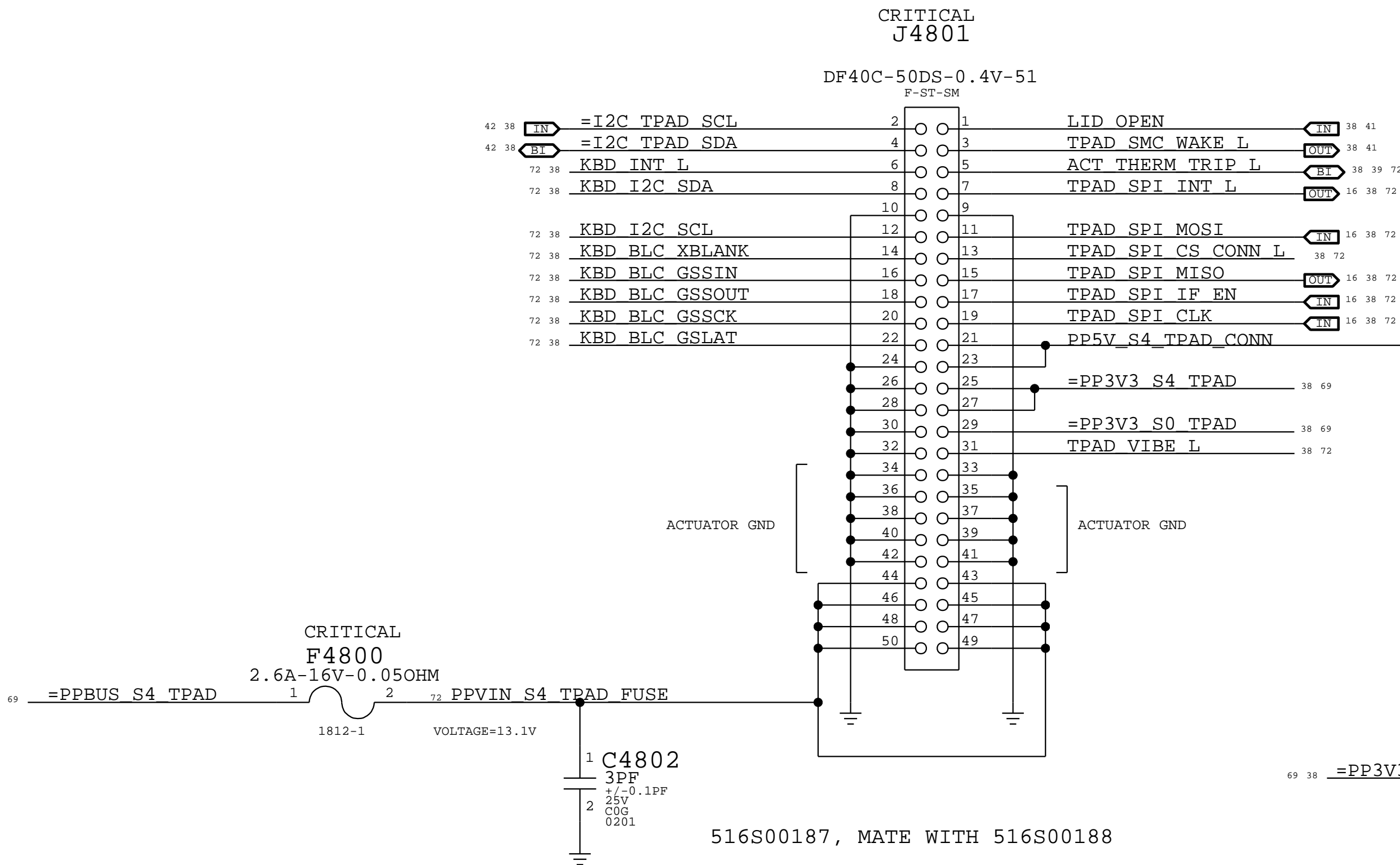
PAGE TITLE		CAMERA 2 OF 2	
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		REVISION	1.0.0
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		SHEET	37 OF 73

BOM_COST_GROUP=CAMERA

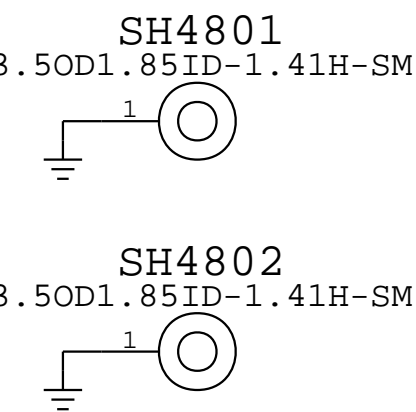
KEYBOARD CONNECTOR



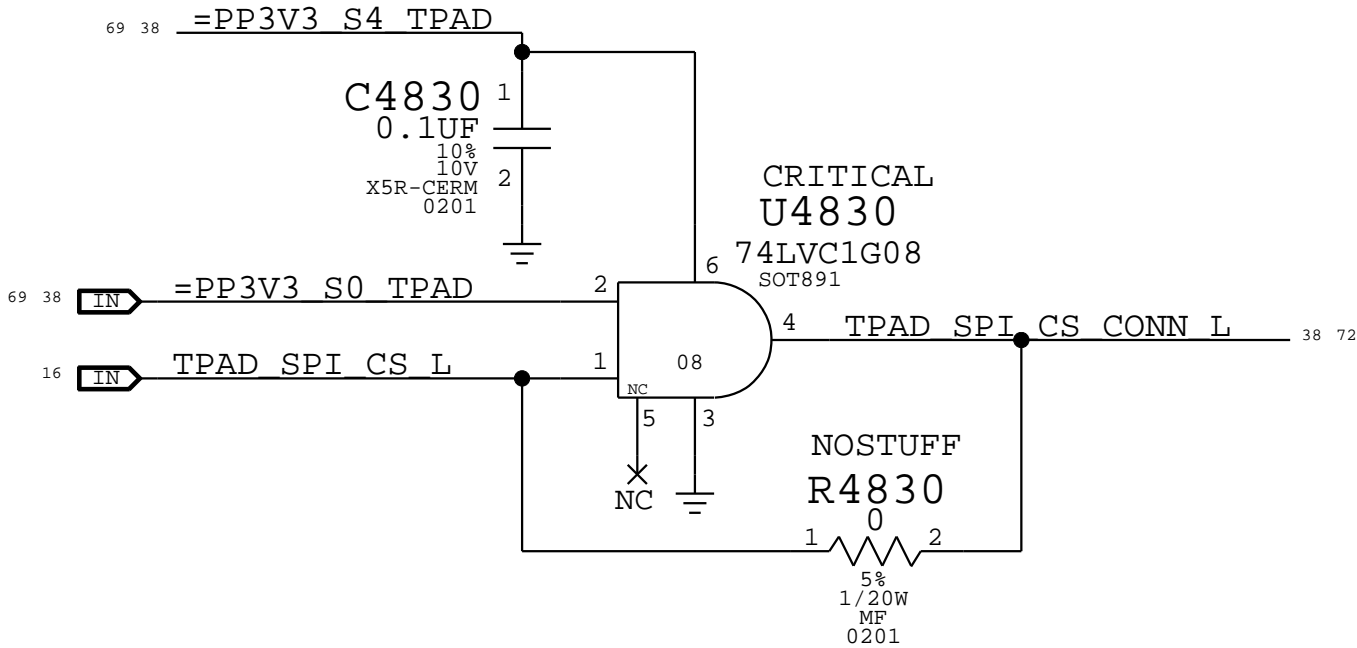
TPAD CONNECTOR



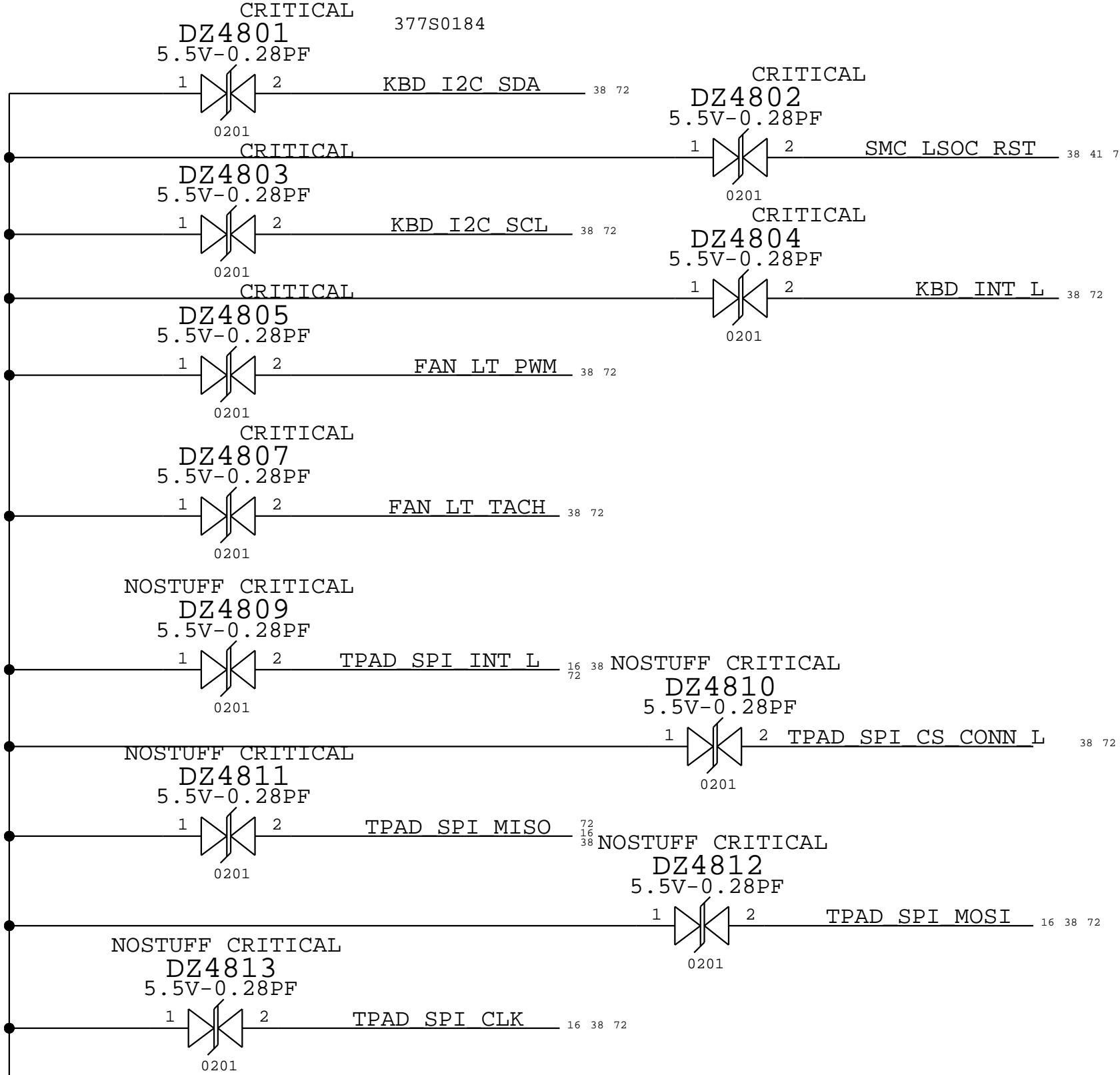
COWLING BOSES



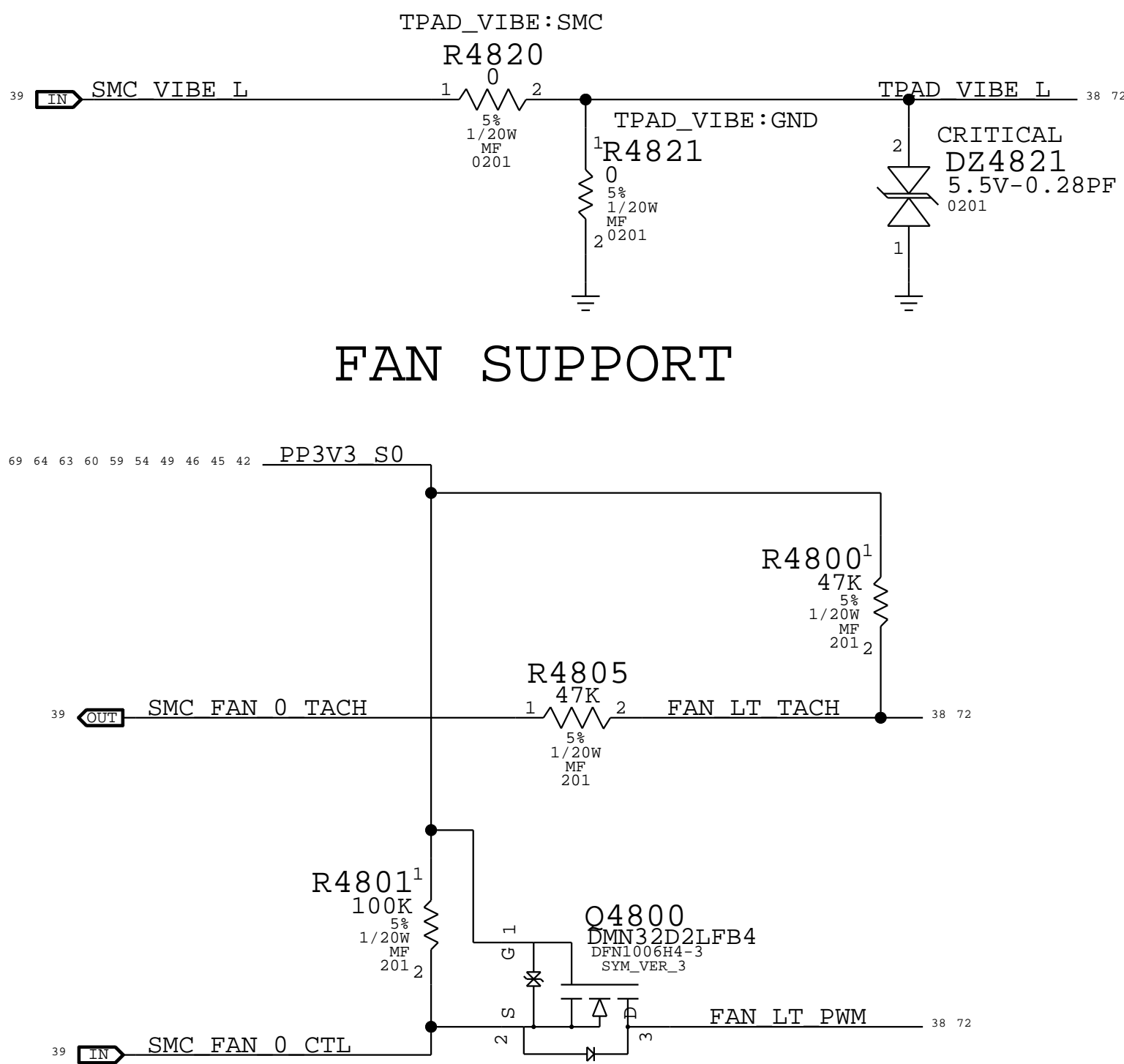
CS ISOLATION




ESD DIODES



FAN SUPPORT



PAGE TITLE		
P1:KEYBOARD & TRACKPAD CONN		
 Apple Inc.	DRAWING NUMBER	051-02265
	REVISION	1.0.0
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BOM_COST_GROUP=KEYBOARD

D

C

B

A

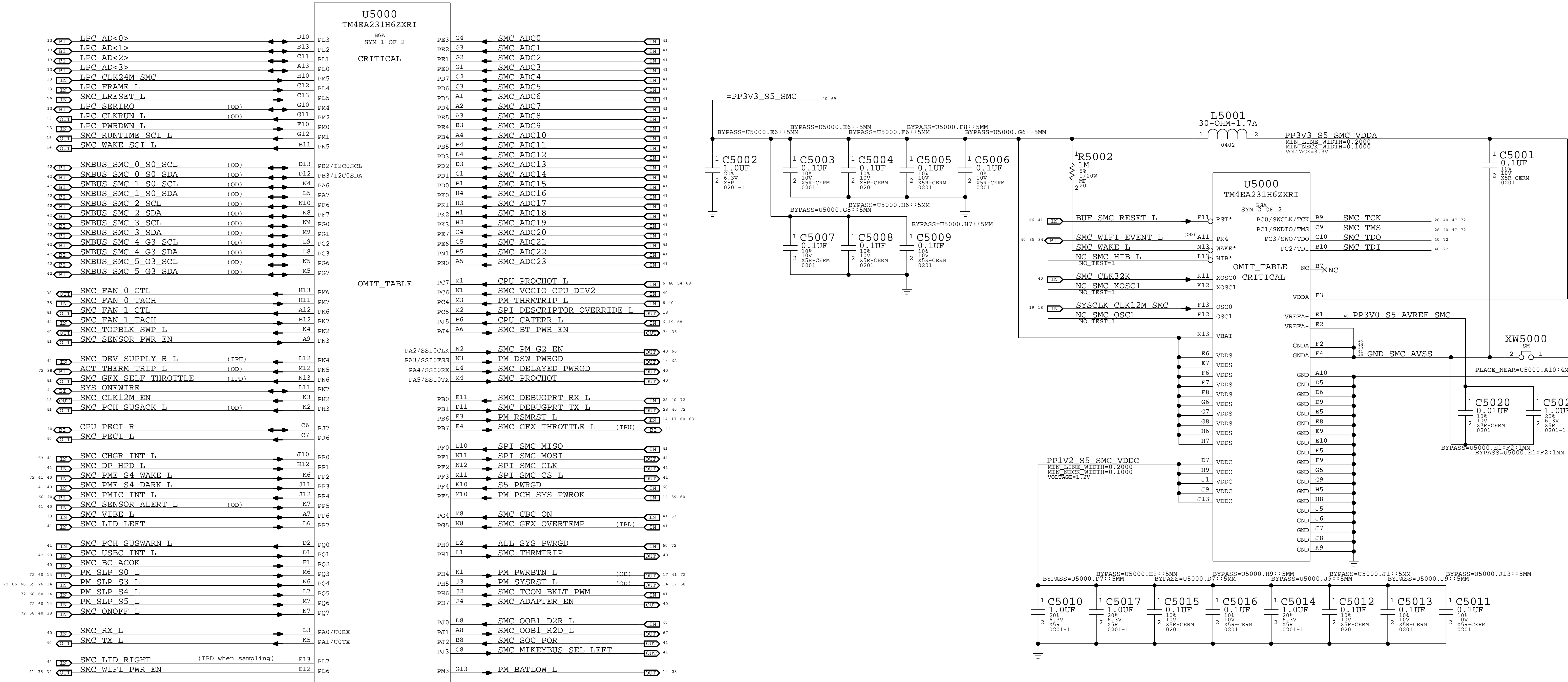
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C

B

A

Laptopblue

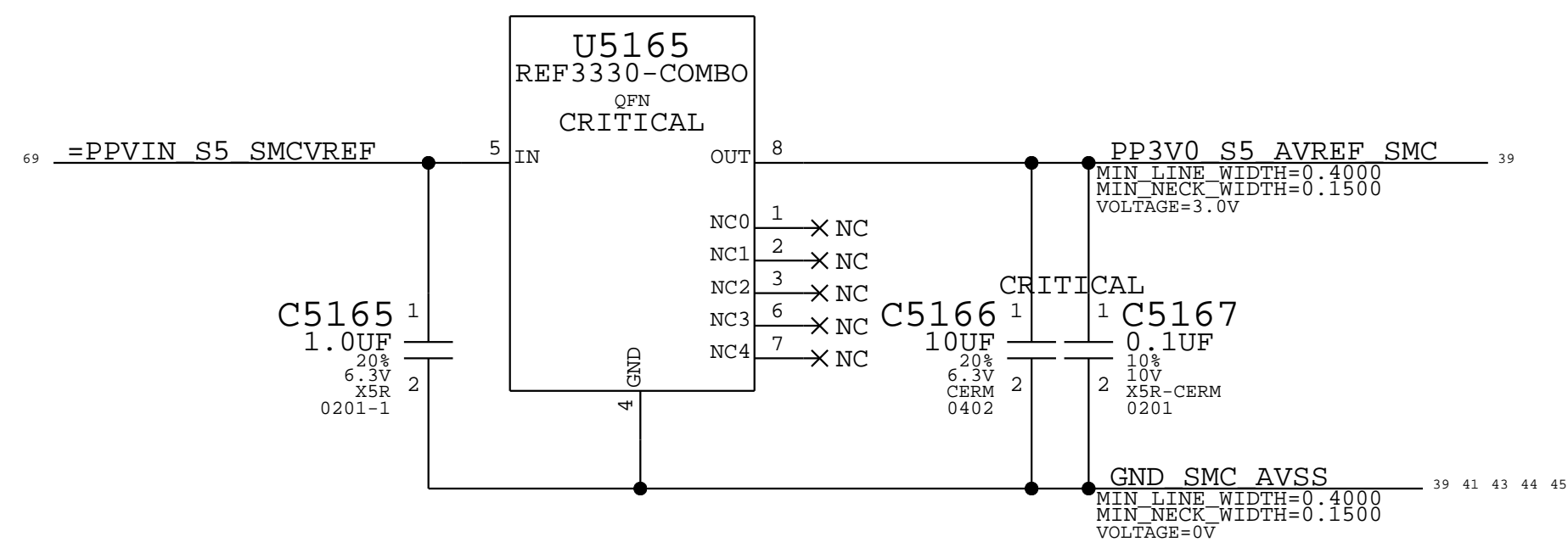


NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

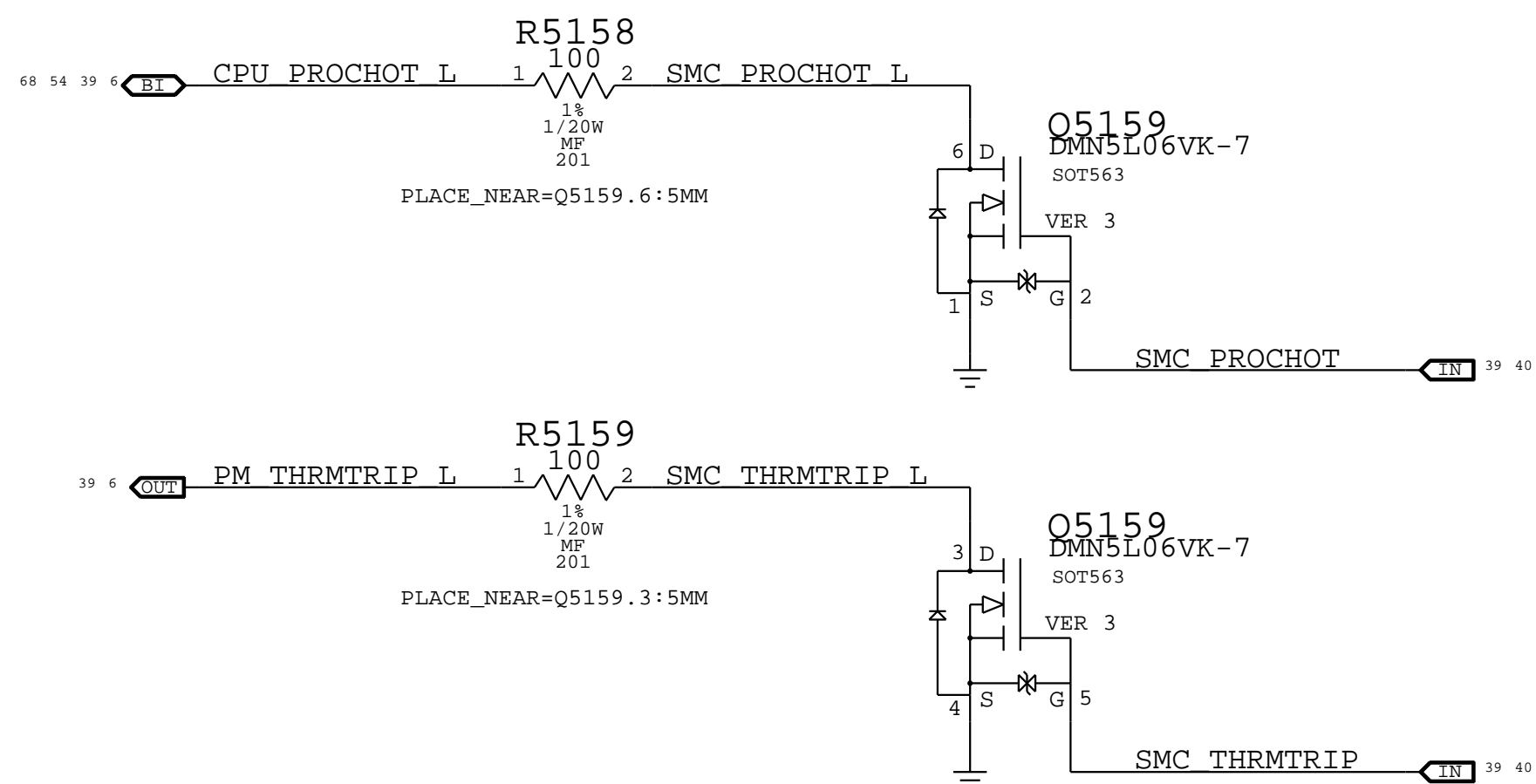
NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SYNC_MASTER=PAULM		SYNC_DATE=06/15/2015	
PAGE TITLE			
SMC			
		DRAWING NUMBER	051-02265
		REVISION	1.0.0
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		PAGE	50 OF 500
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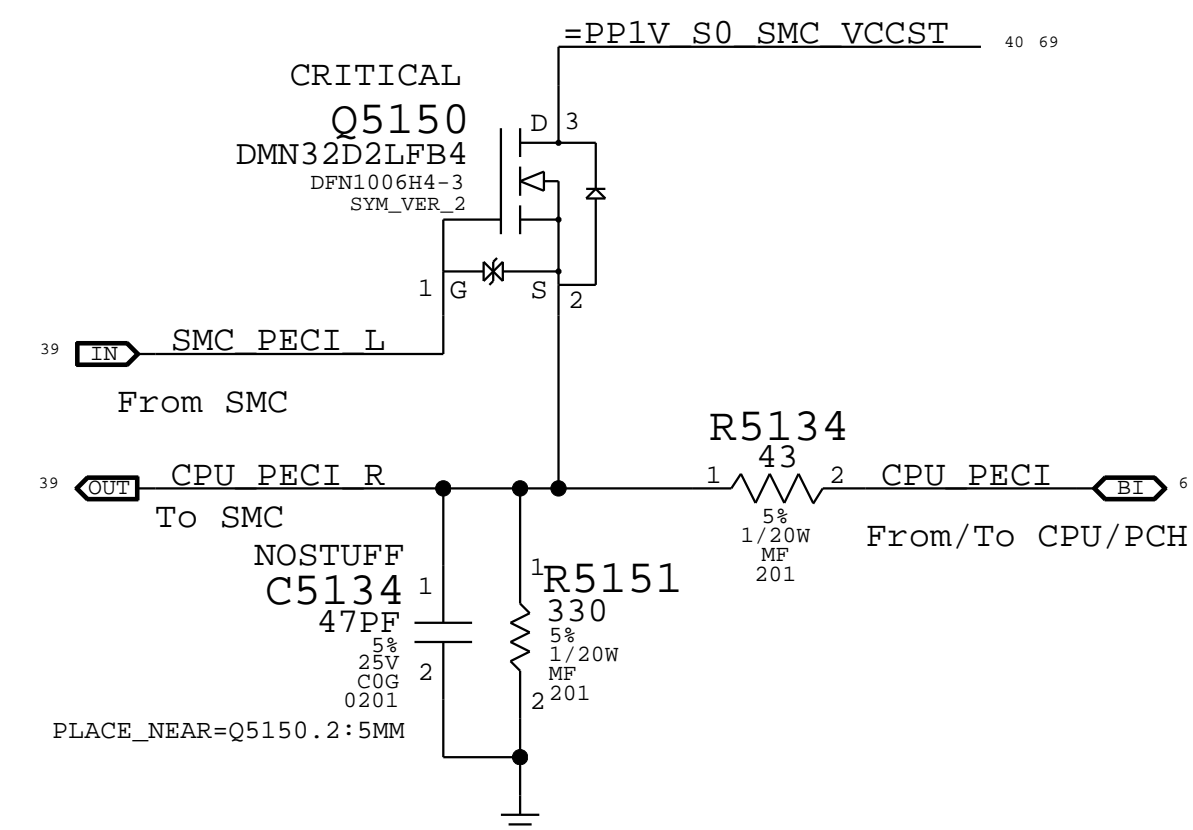
SMC AVREF Supply



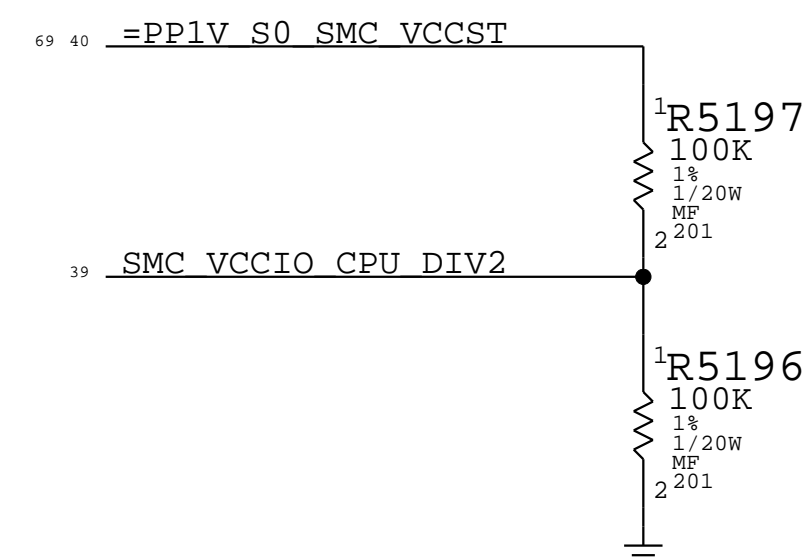
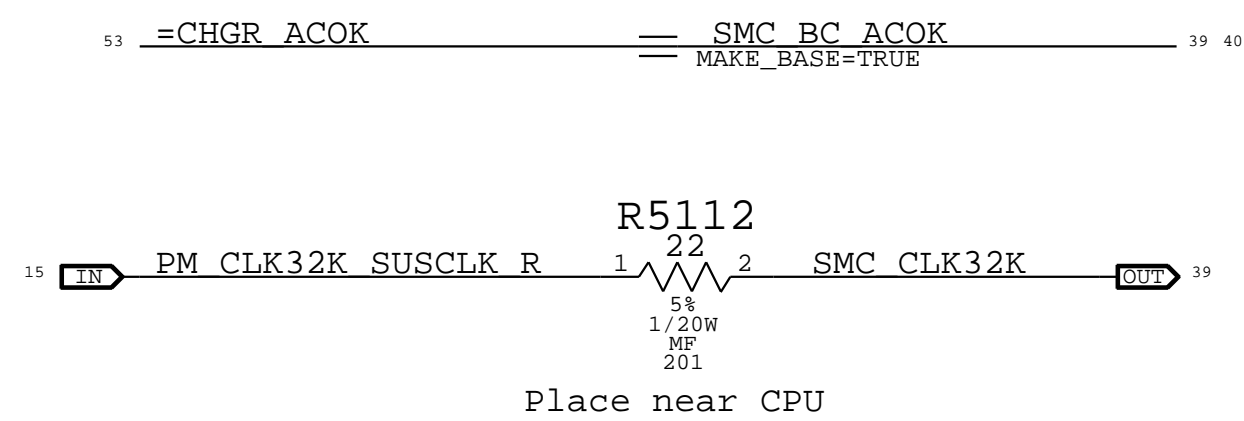
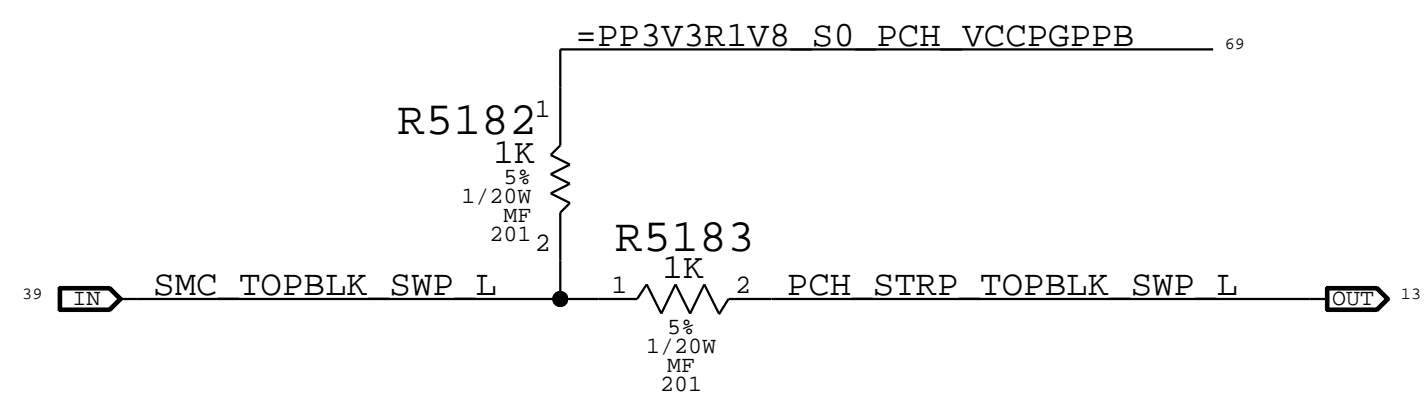
PROCHOT/THRMTRIP Support




PECI Support



Top-Block Swap

[illegible]

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SMC Shared Support		051-02265		D
 Apple Inc.		REVISION		
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D

C

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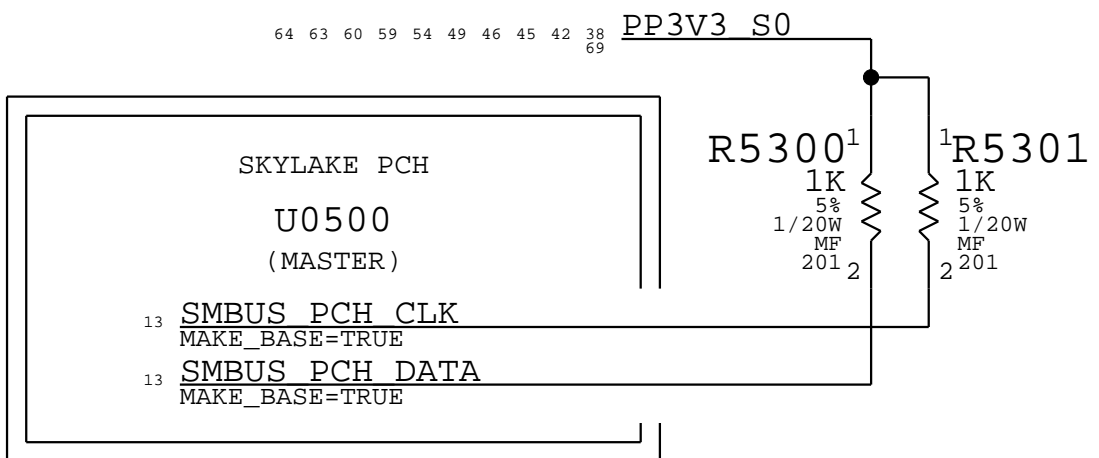
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C

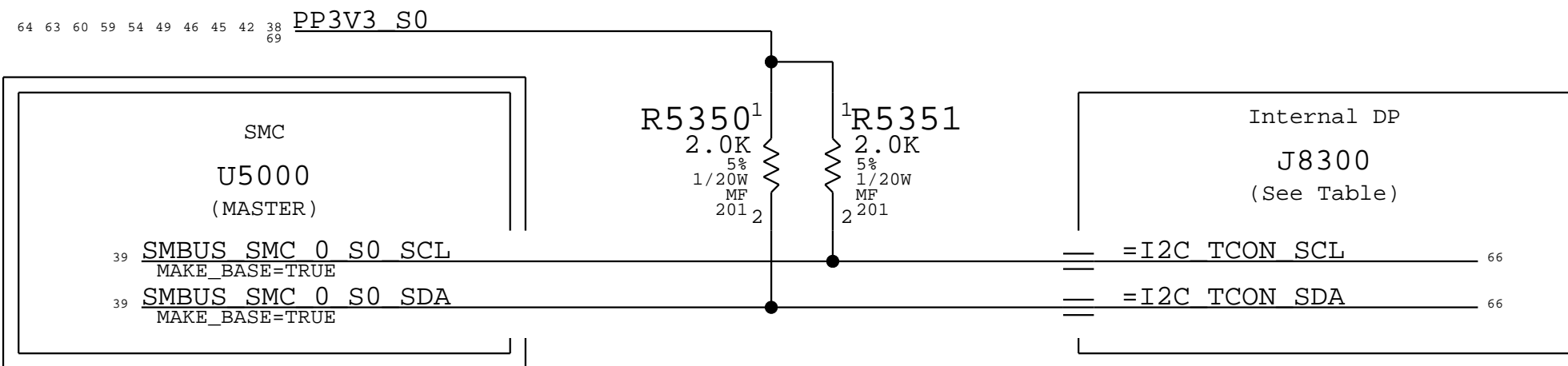
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A

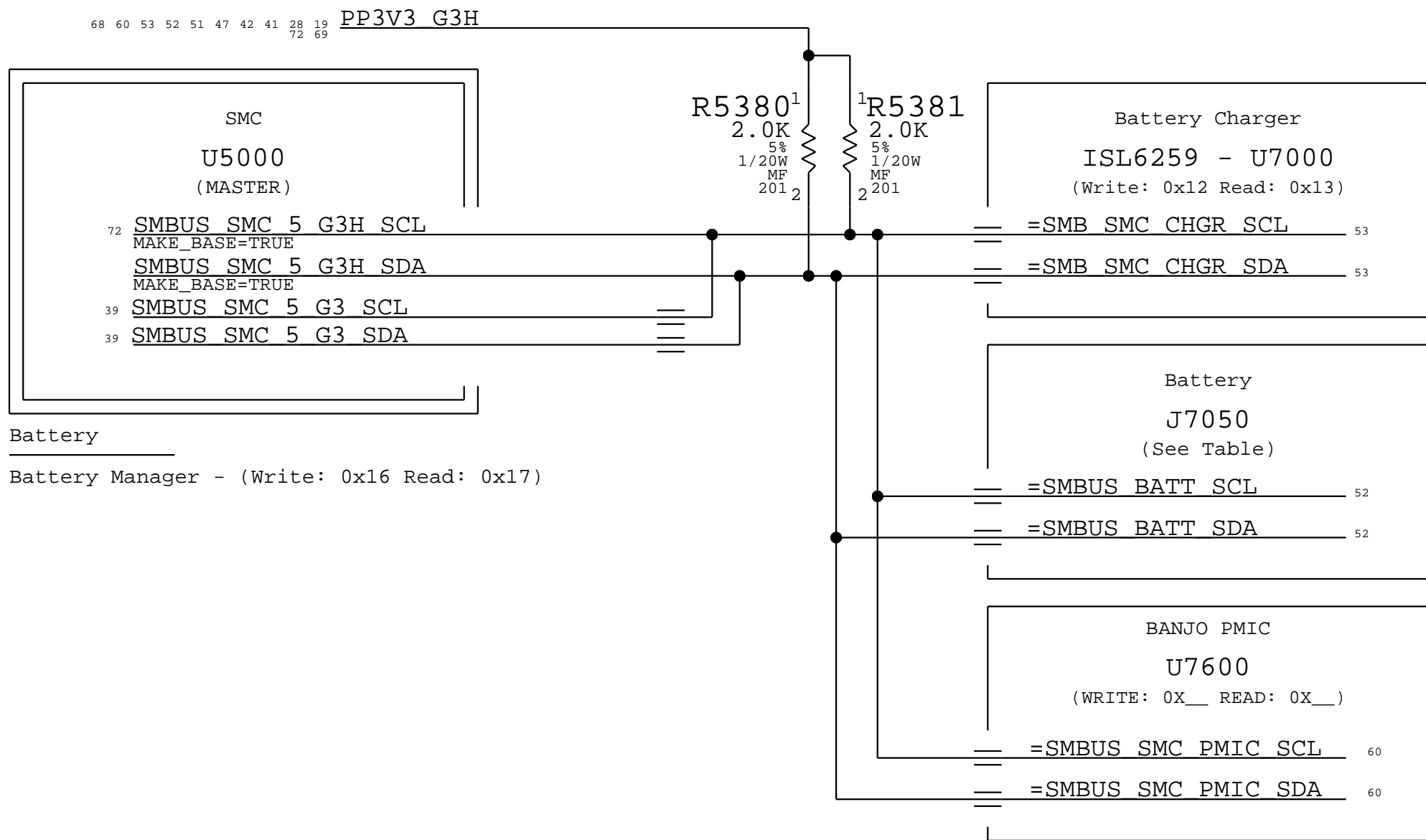
SKYLAKE PCH S0 "SMBus 0" CONNECTIONS



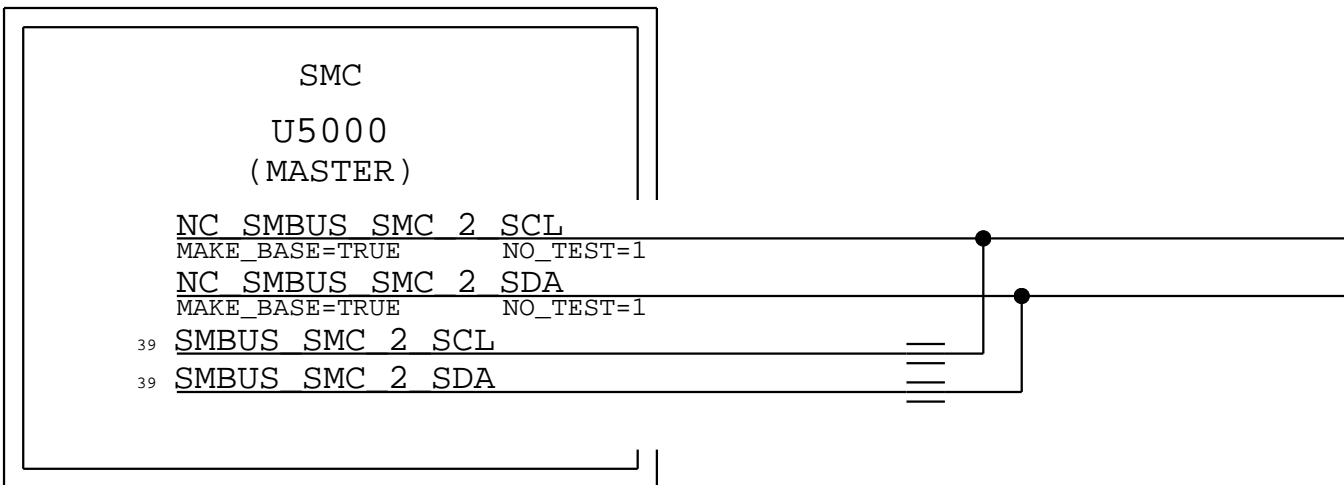
SMC SMBus "0" S0 Connections



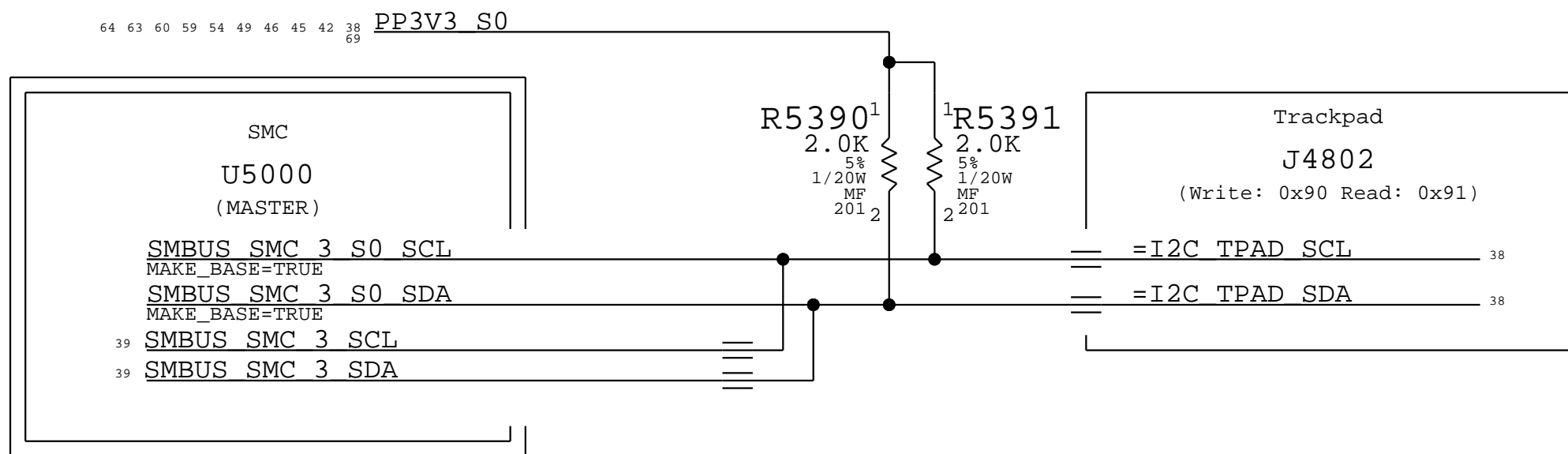
SMC SMBus "5" G3H Connections



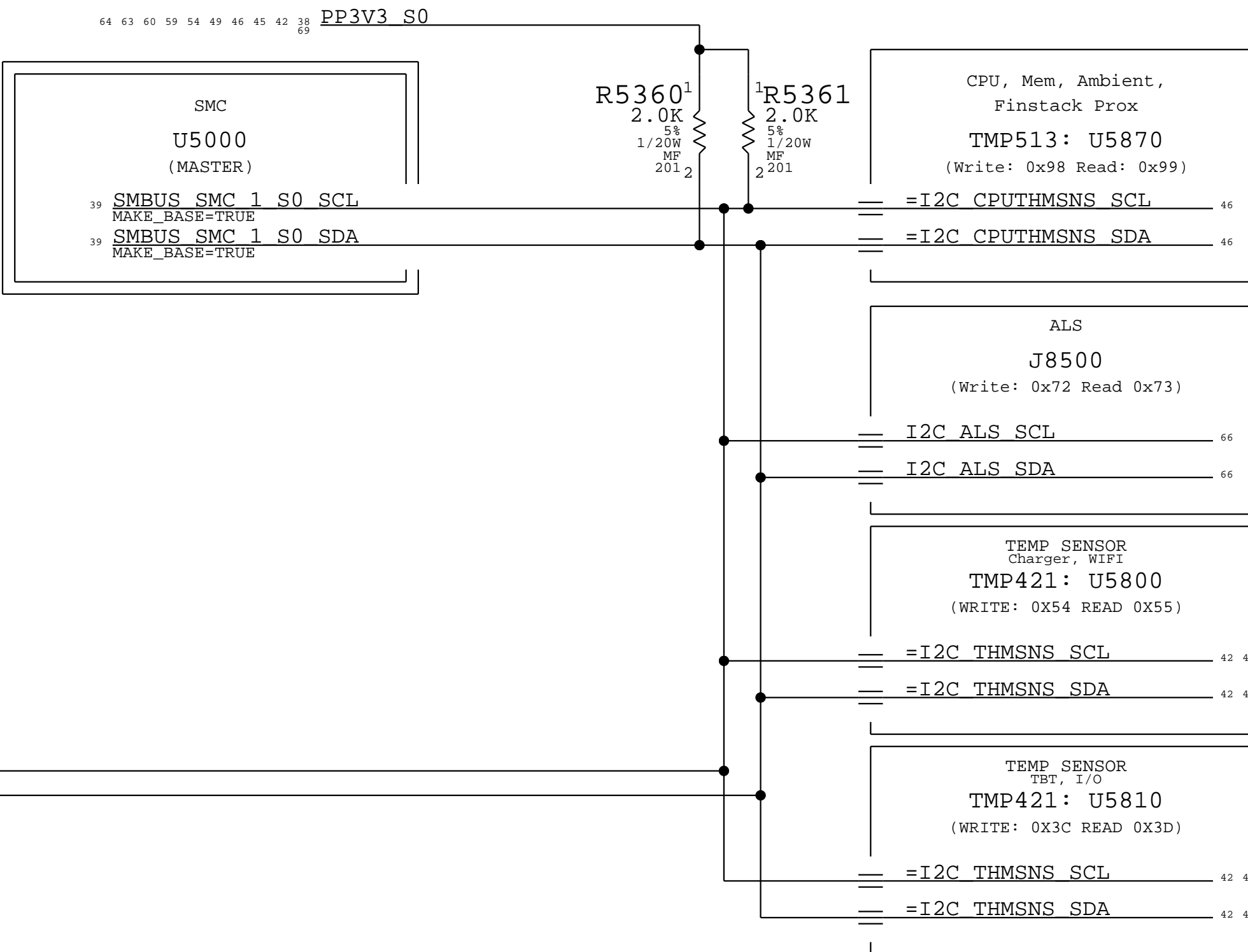
SMC SMBus "2" S3 Connections



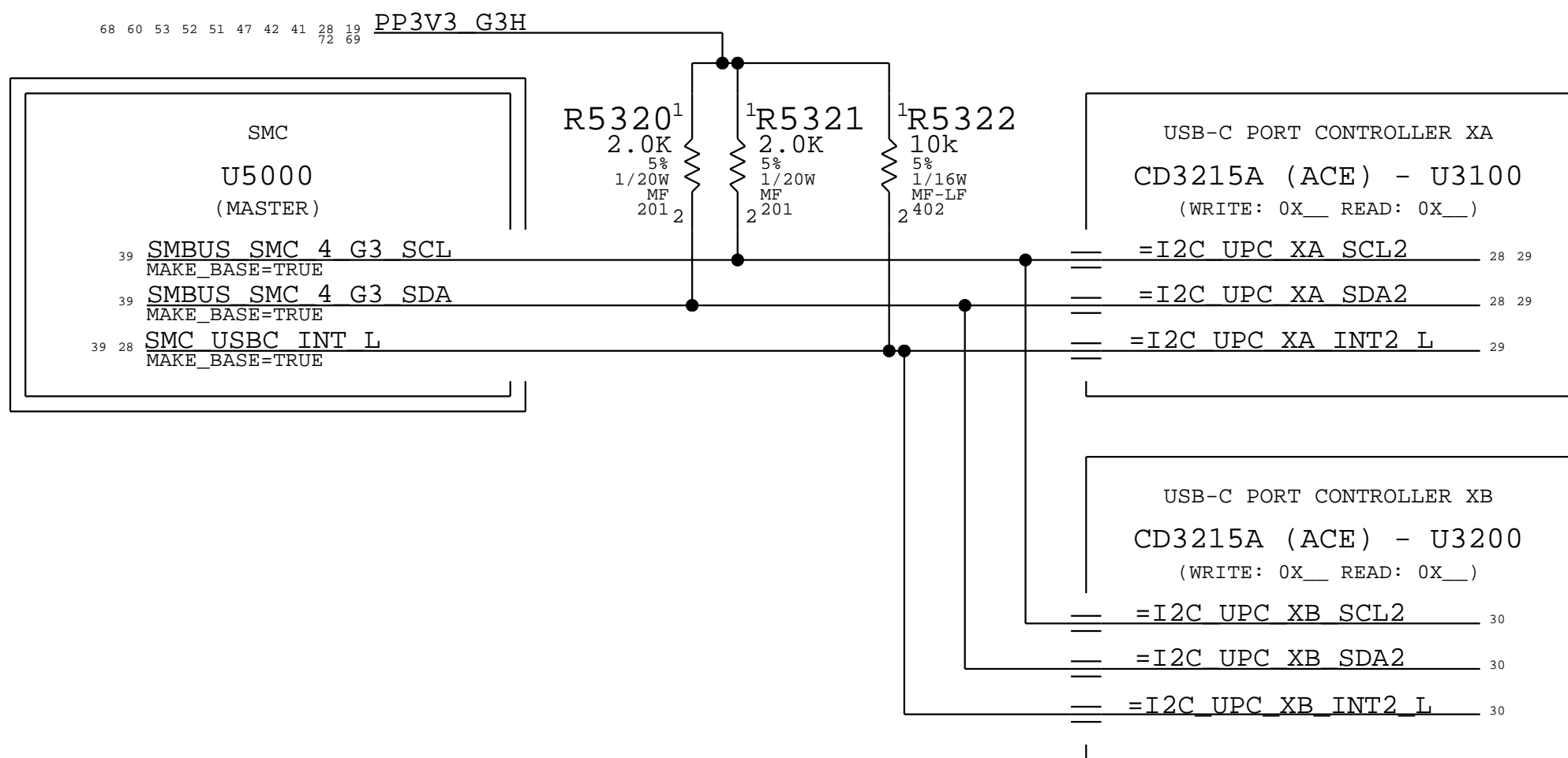
SMC SMBus "3" S0 Connections



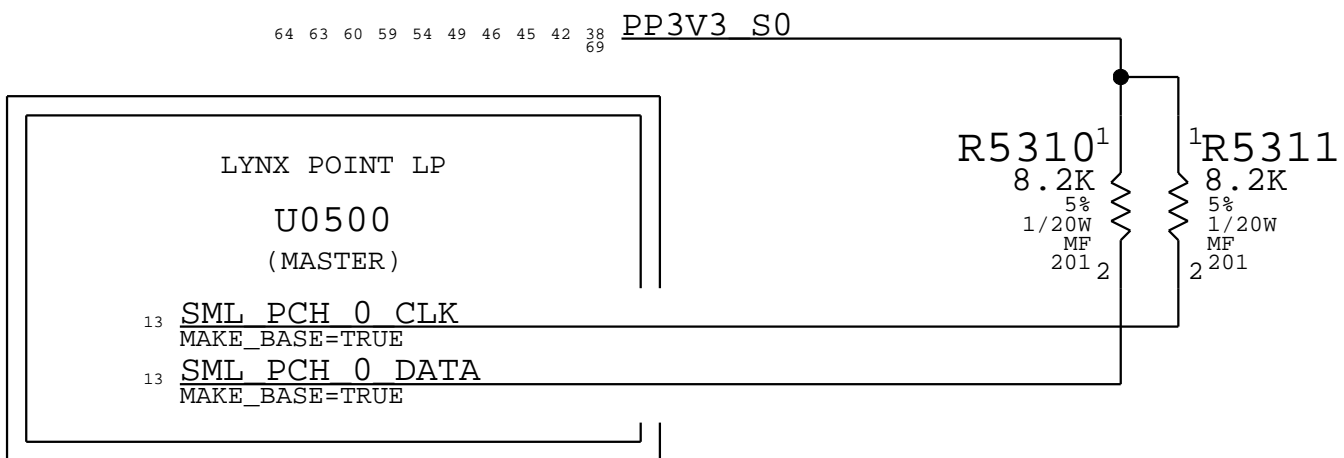
SMC SMBus "1" S0 Connections



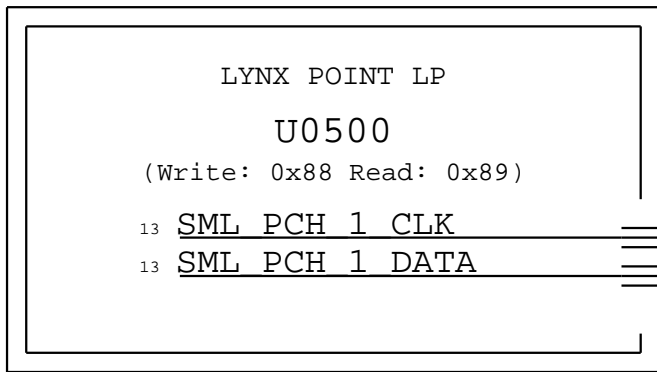
SMC SMBUS "4" G3H CONNECTIONS



LYNX POINT LP S0 "SMLink 0" Connections




LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to access PCH.

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

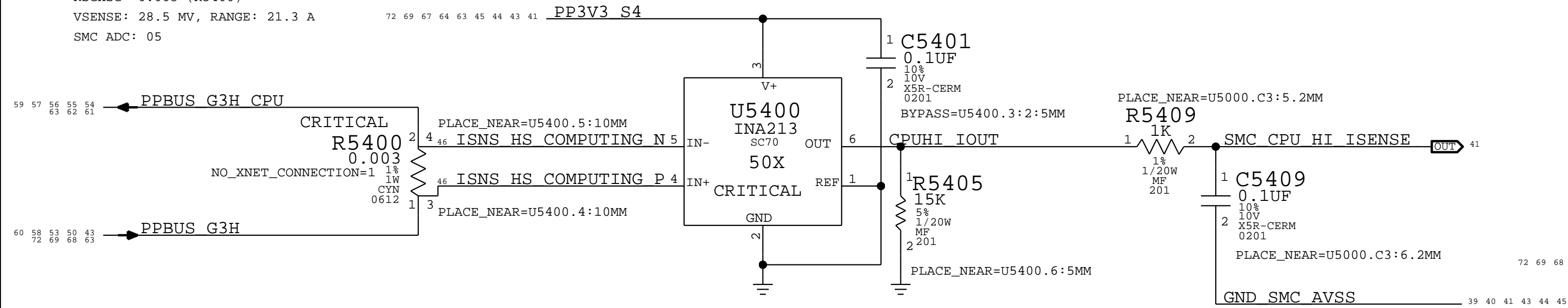
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SMBus Connections

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	REVISION	1.0.0		
	BRANCH			
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	SHEET	42 OF 73		

BOM_COST_GROUP=SMC

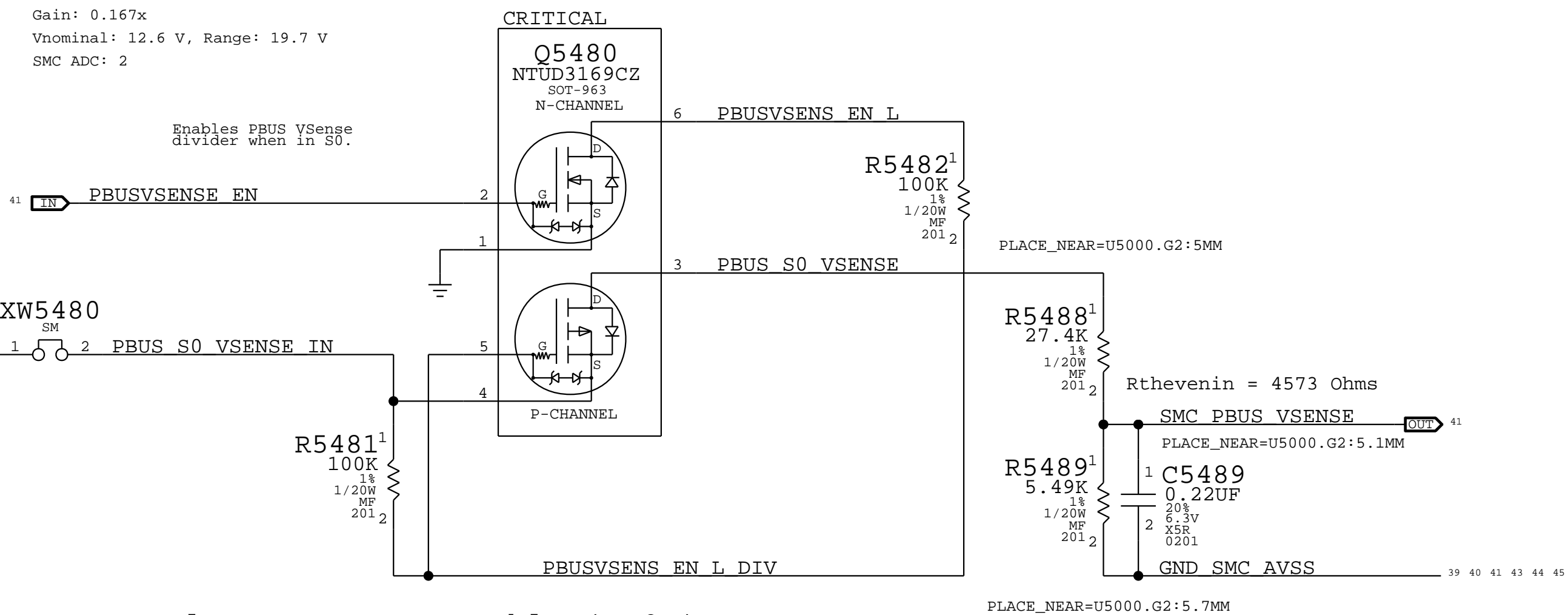
CPU High Side Current Sense (IC0R)

GAIN: 50X, EDP: 9.5 A
Rsense: 0.003 (R5400)
VSENSE: 28.5 MV, RANGE: 21.3 A
SMC ADC: 05



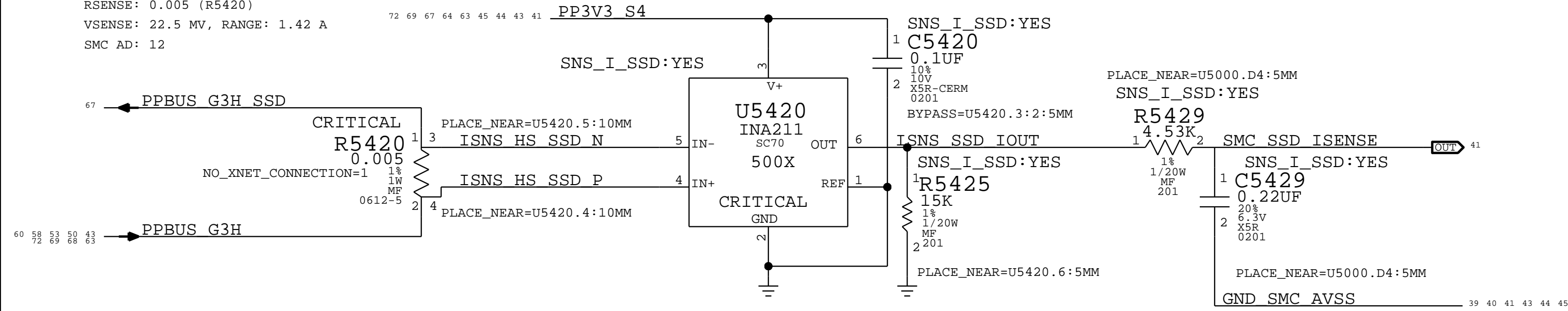
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 19.7 V
SMC ADC: 2



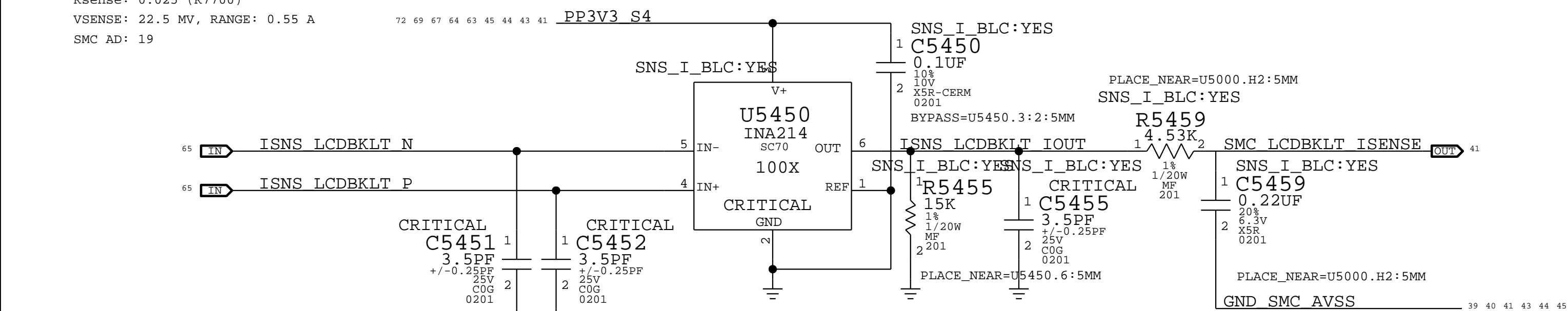
SSD NAND CURRENT SENSE (IHNC)

GAIN: 500X, EDP: 0.9 A
RSense: 0.005 (R5420)
VSENSE: 22.5 MV, RANGE: 1.42 A
SMC AD: 12



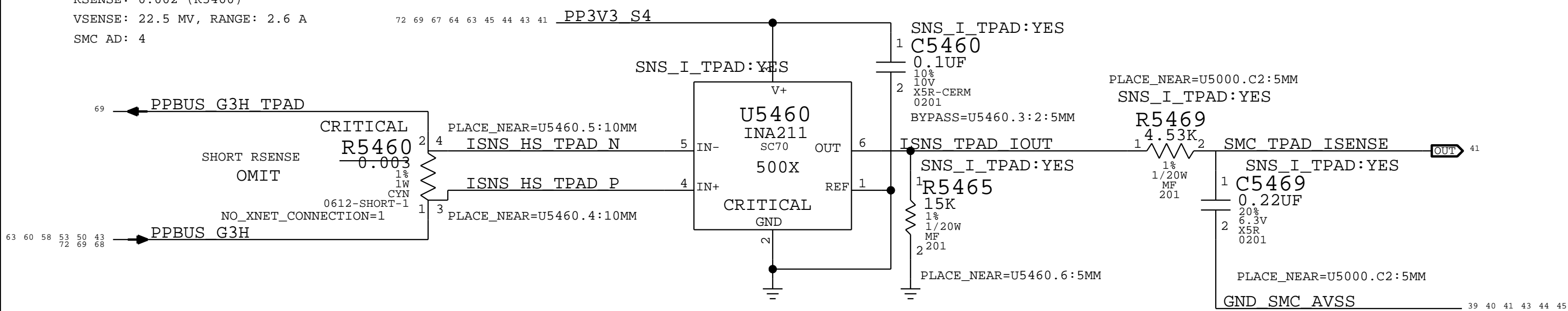
LCD BACKLIGHT CURRENT SENSE (IBLR)

GAIN: 100X, EDP: 0.9 A
Rsense: 0.025 (R7700)
VSENSE: 22.5 MV, RANGE: 0.55 A
SMC AD: 19



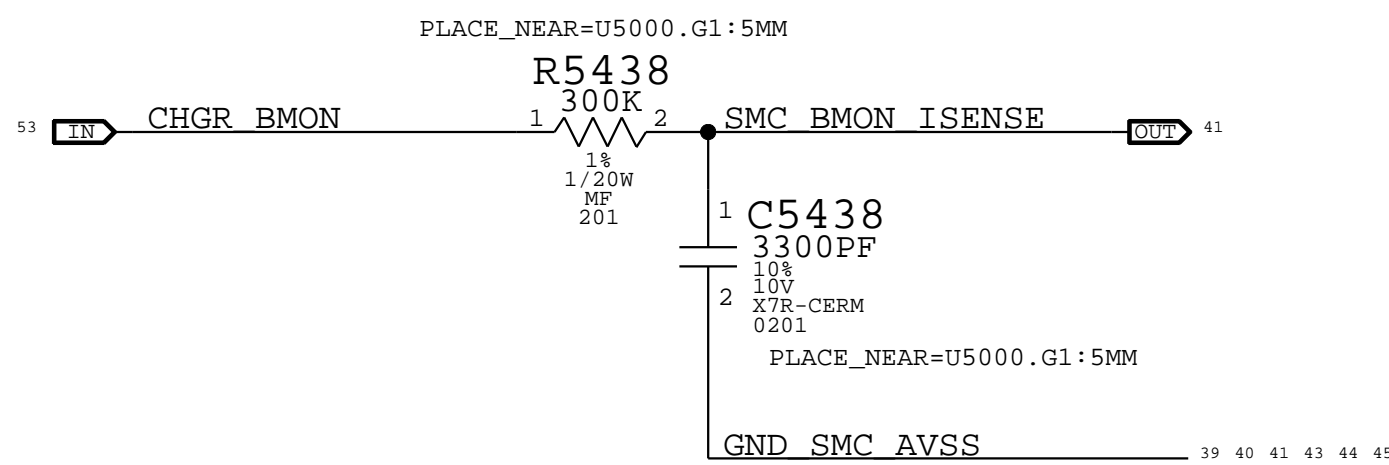
TRACKPAD ACTUATOR X239 CURRENT SENSE (ITAR)

GAIN: 200X, EDP: 0.9 A
RSense: 0.002 (R5460)
VSENSE: 22.5 MV, RANGE: 2.6 A
SMC AD: 4



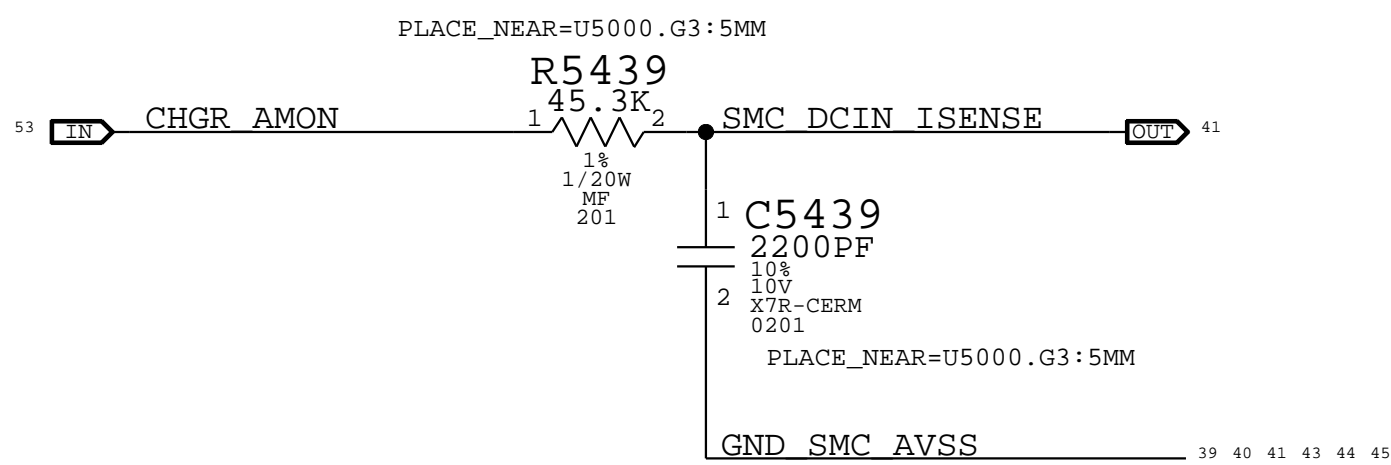
Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A
RSense: 0.005 (R7160)
SMC ADC: 03



DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
RSense: 0.010 (R7120)
SMC ADC: 01



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5429		SNS_I_SSD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		SNS_I_BLC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		SNS_I_TPAD:NO

DESIGN: X502/MLB CATZ		
LAST CHANGE: Thu Aug 4 21:00:42 2016		
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Power Sensors High Side		
	DRAWING NUMBER	051-02265
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BOM_COST_GROUP=SENSORS

A

8

7

6

Laptopblue

5

4

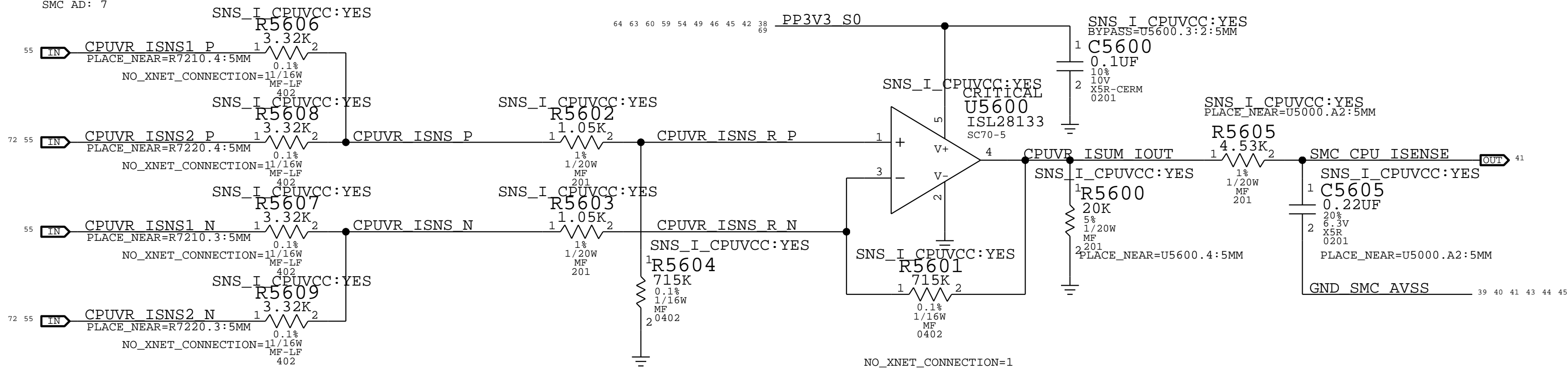
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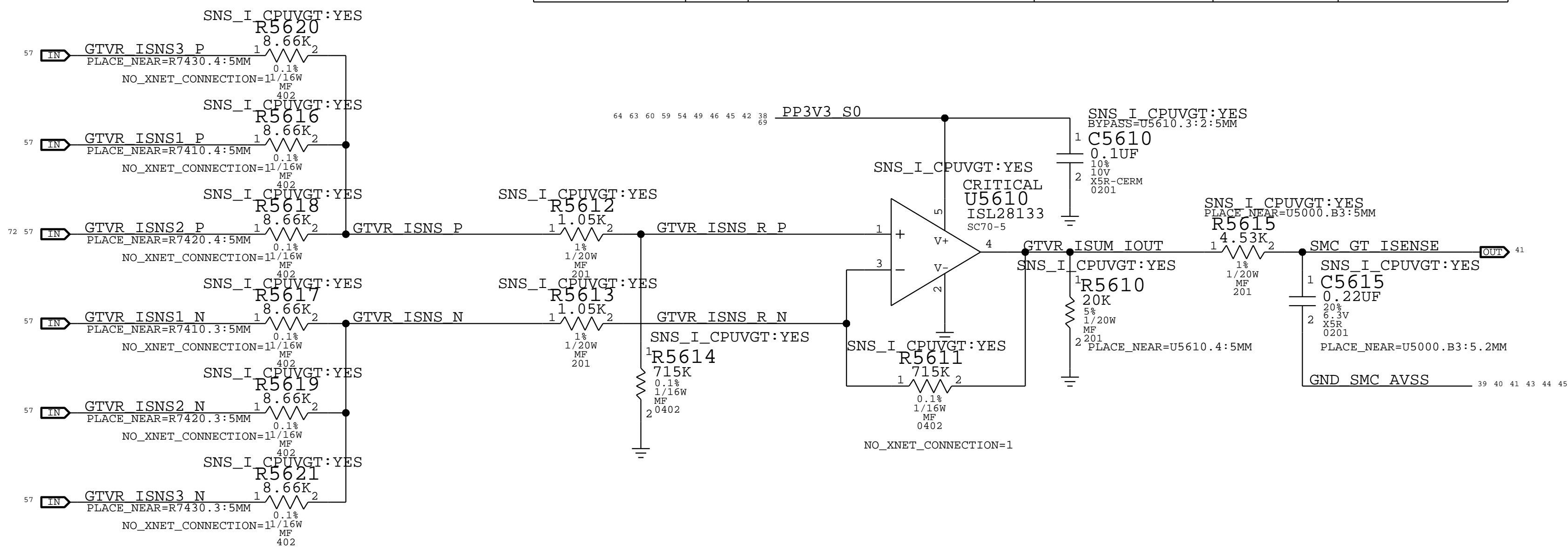
CPU VCC CURRENT SENSE (ICAC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R7700)
VSENSE: 22.5 mV, RANGE: 2.27 A
SMC AD: 7



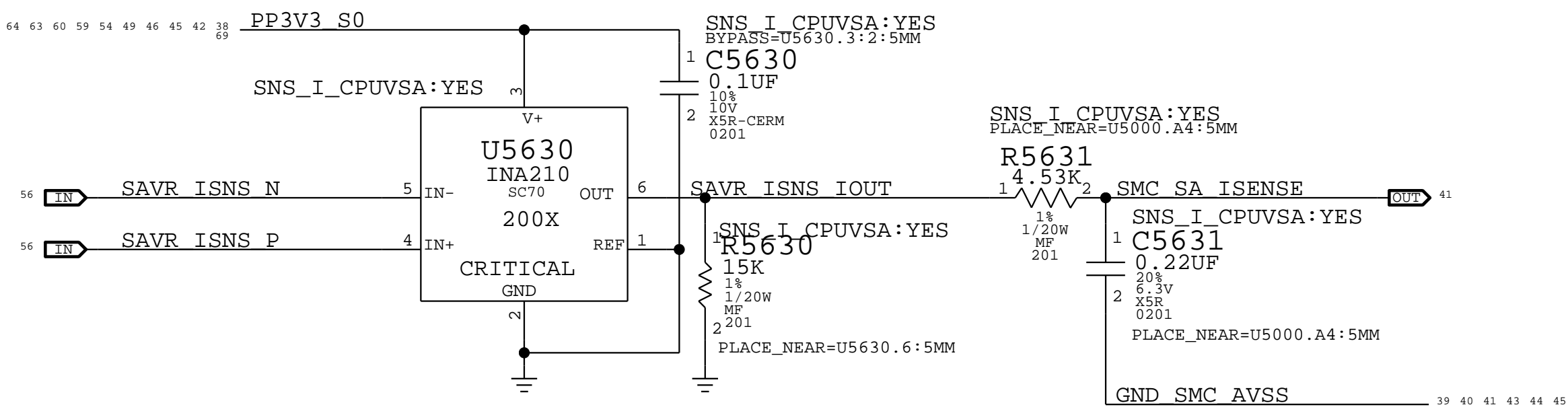
CPU GT CURRENT SENSE (ICGC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R7700)
VSENSE: 22.5 mV, RANGE: 2.27 A
SMC AD: 9



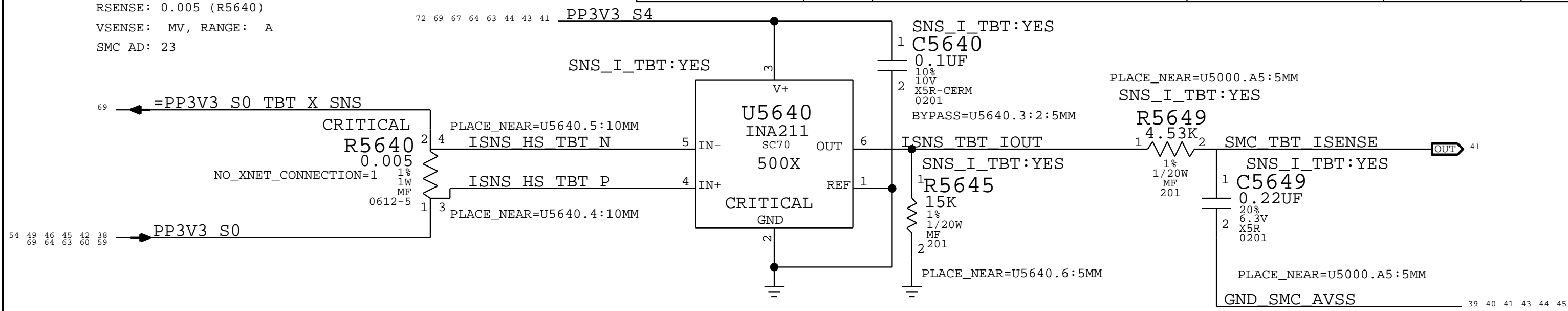
CPU SA CURRENT SENSE (ICSC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R7700)
VSENSE: 22.5 mV, RANGE: 7.67 A
SMC AD: 10



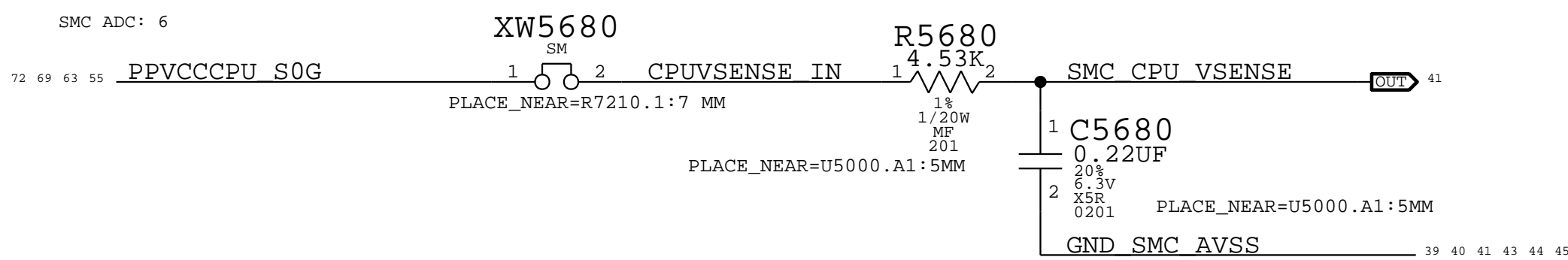
TBT CURRENT SENSE (IULC)

GAIN: 500X. EDP: A
RSENSE: 0.005 (R5640)
VSENSE: mV, RANGE: A
SMC AD: 23



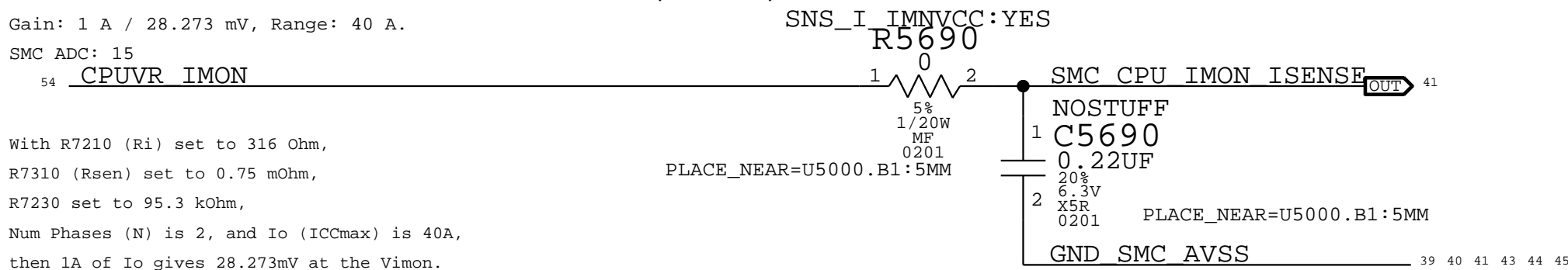
CPU CORE VOLTAGE SENSE (VCAC)

SMC ADC: 6



CPU CORE IMON CURRENT SENSE (ICAM)

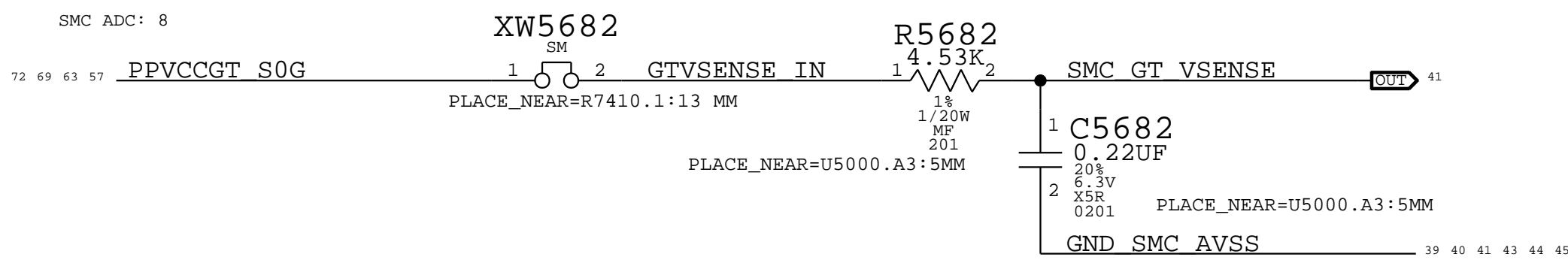
Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 15



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5605		SNS_I_CPUVCC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5615		SNS_I_CPUVGT:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5631		SNS_I_CPUVSA:NO

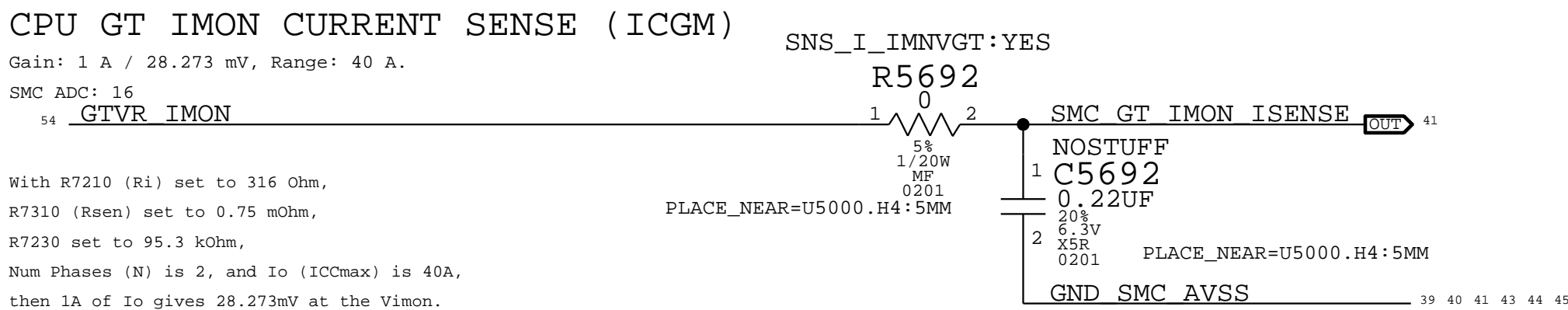
CPU GT VOLTAGE SENSE (VCGC)

SMC ADC: 8



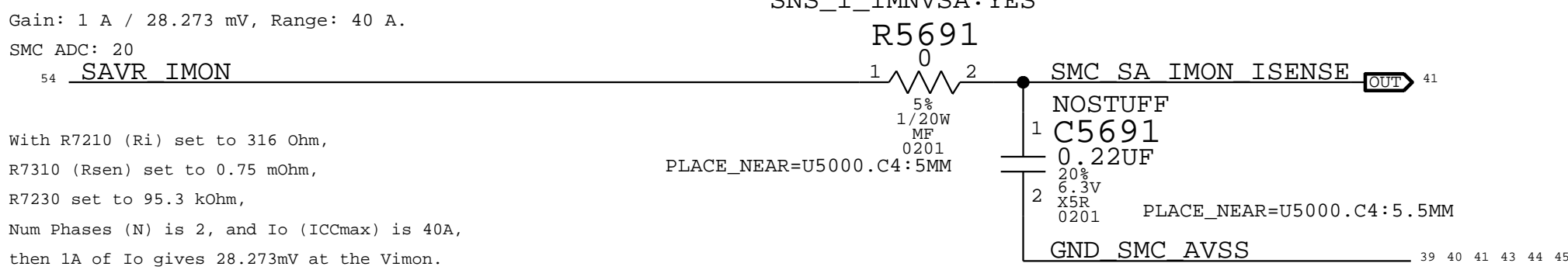
CPU GT IMON CURRENT SENSE (ICGM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 16



CPU SA IMON CURRENT SENSE (ICSM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 20



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5649		SNS_I_TBT:NO

DESIGN: X502/MLB_CATZ		
LAST CHANGE: Thu Aug 4 21:00:42 2016		
PAGE TITLE		
Power Sensors Extended		
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BRANCH		
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BOM_COST_GROUP=SENSORS

8

7

6

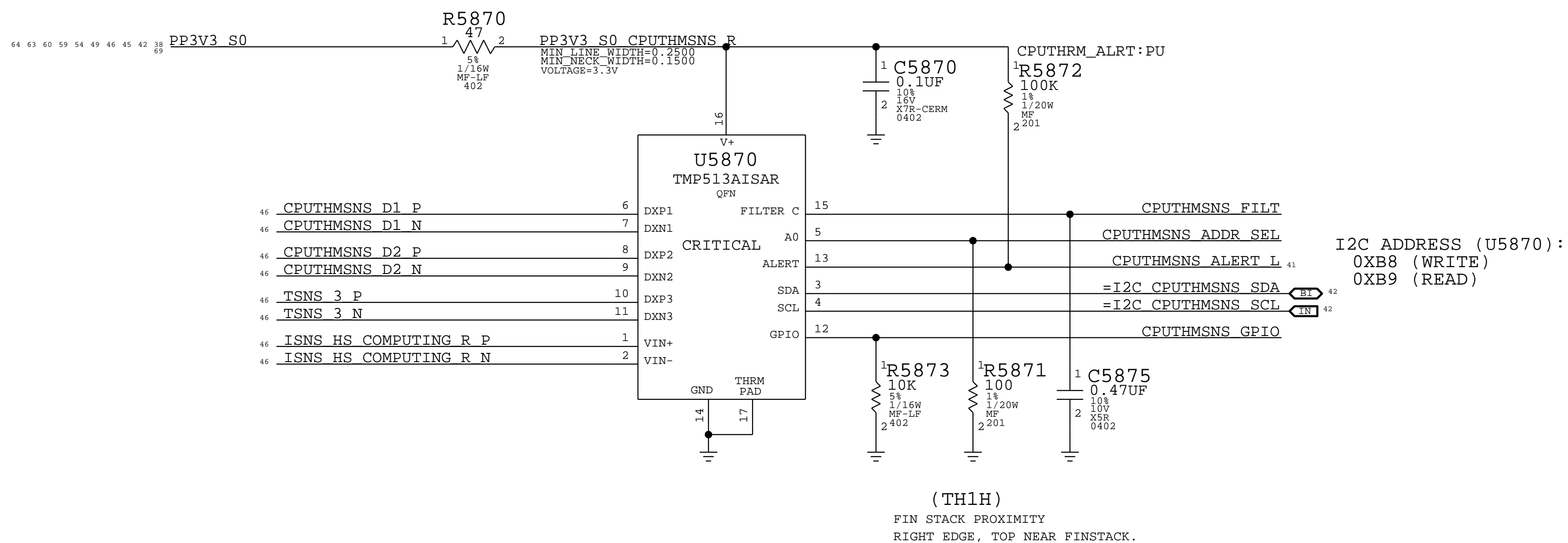
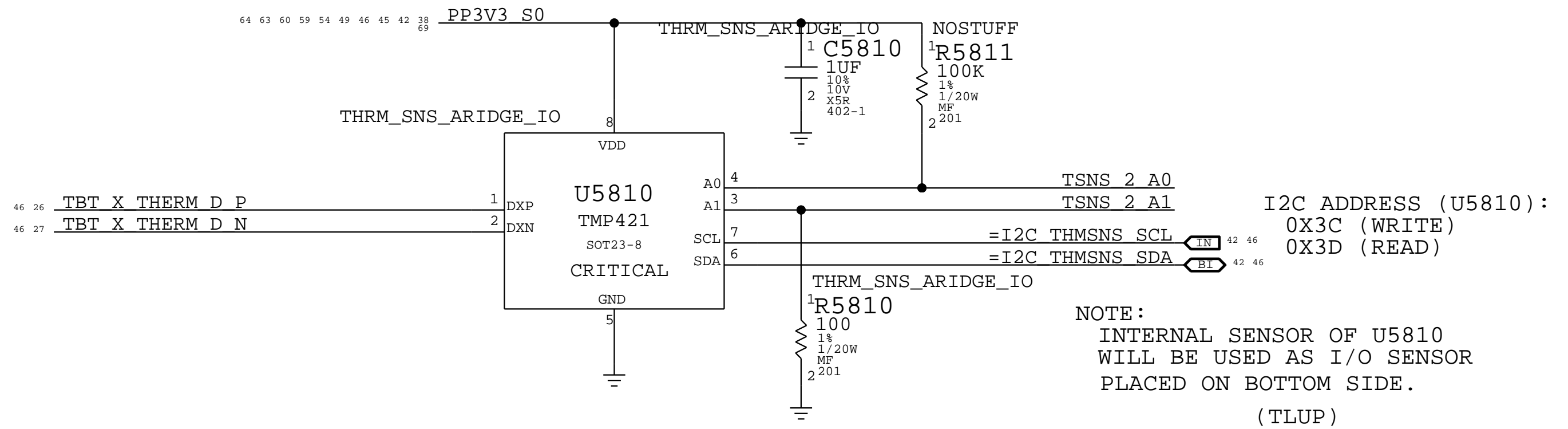
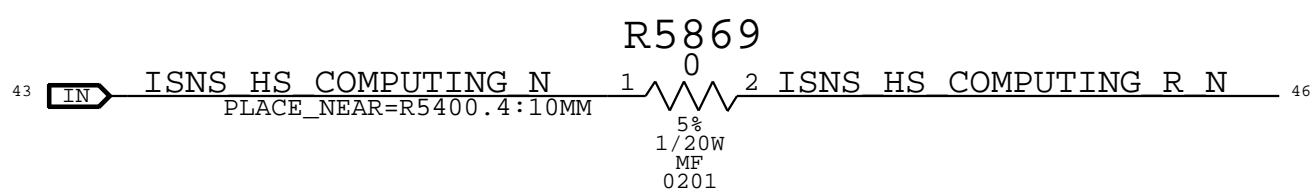
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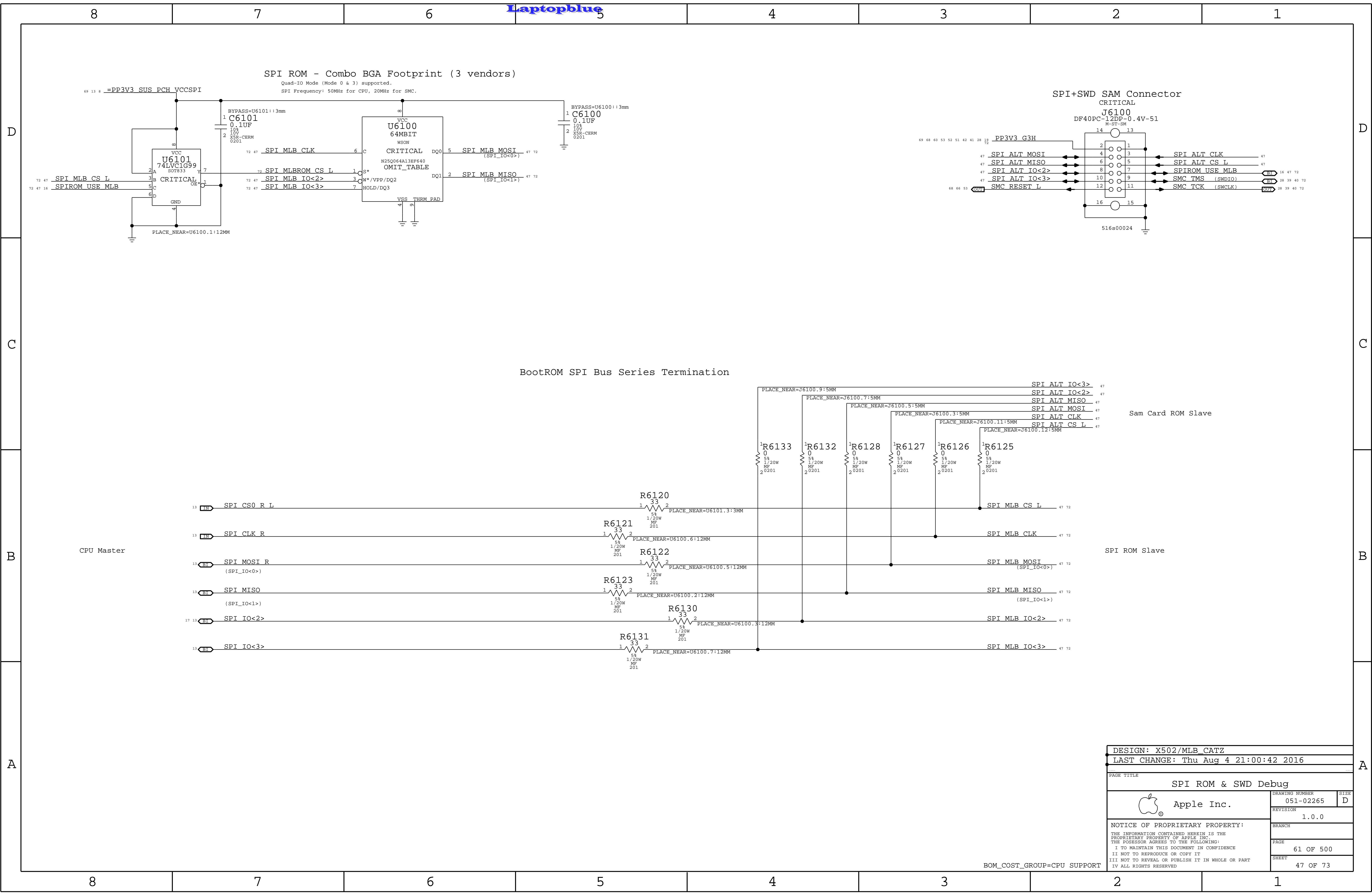
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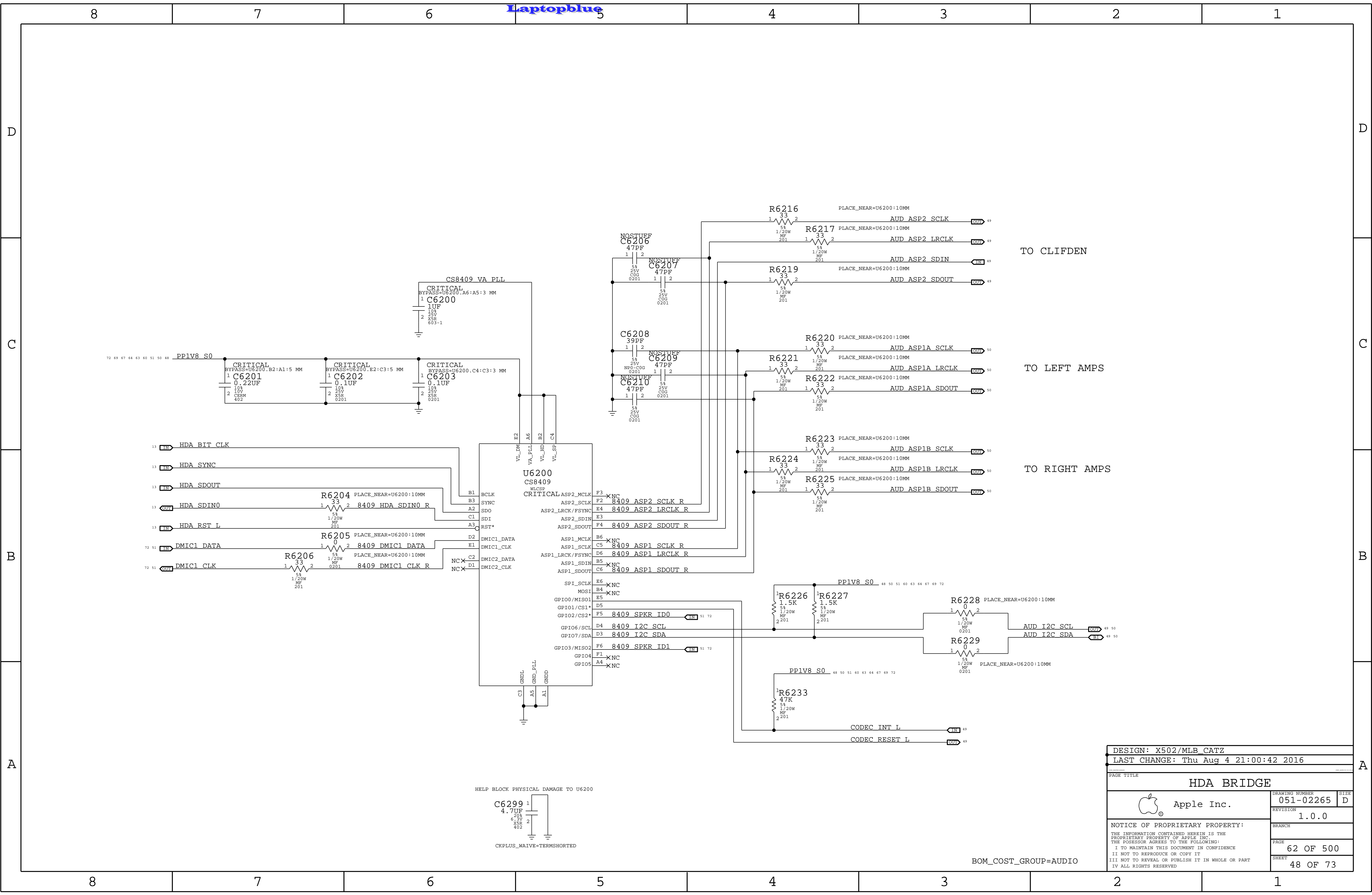
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1



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Thermal Sensors			
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		1.0.0	
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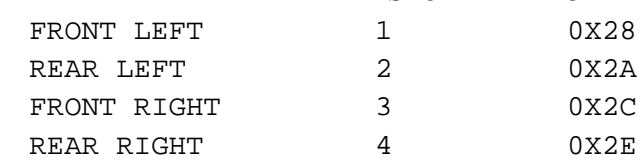
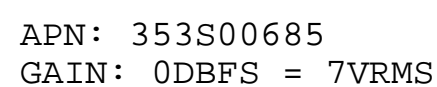
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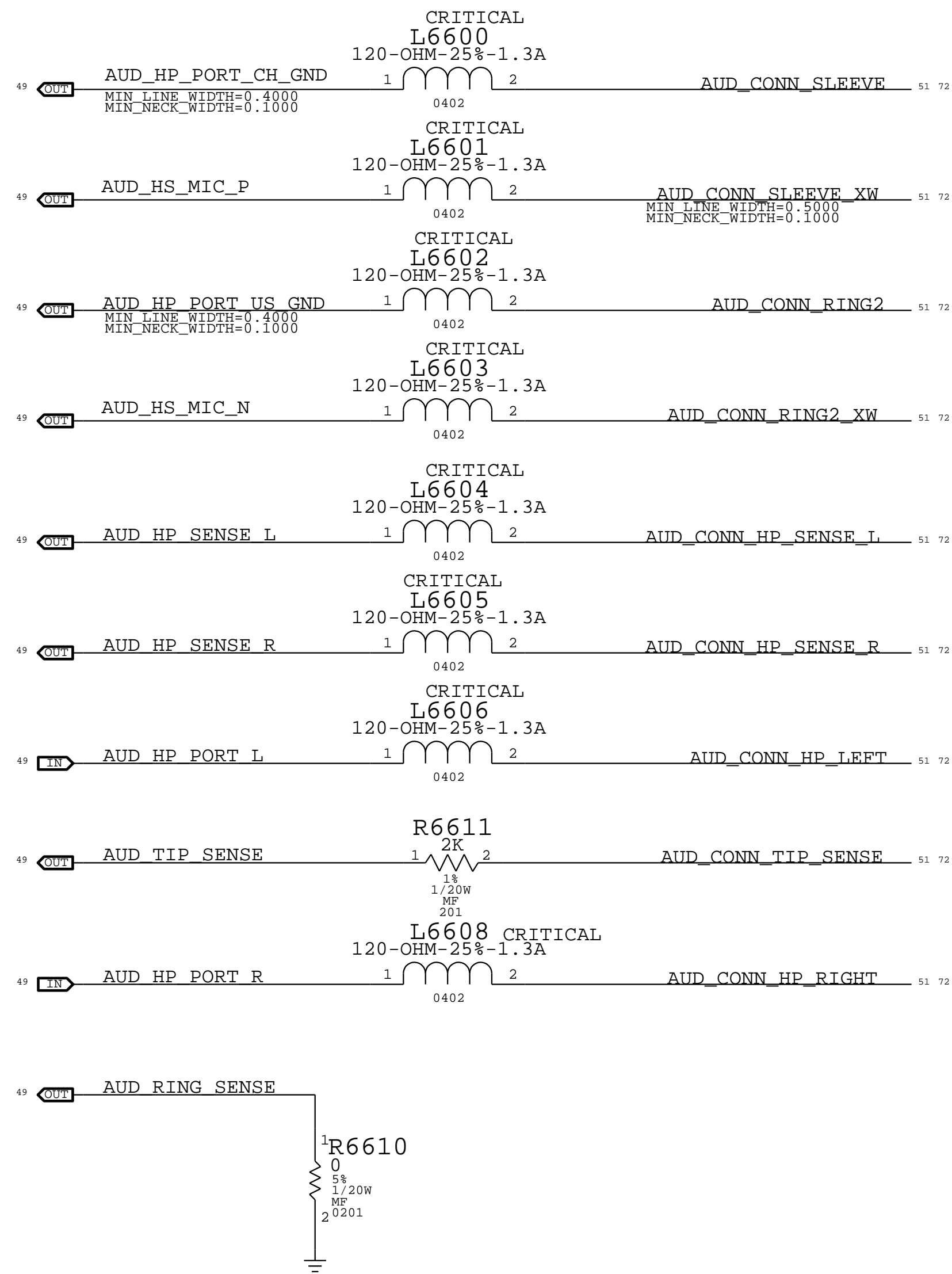
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BOM_COST_GROUP=AUDIO

C

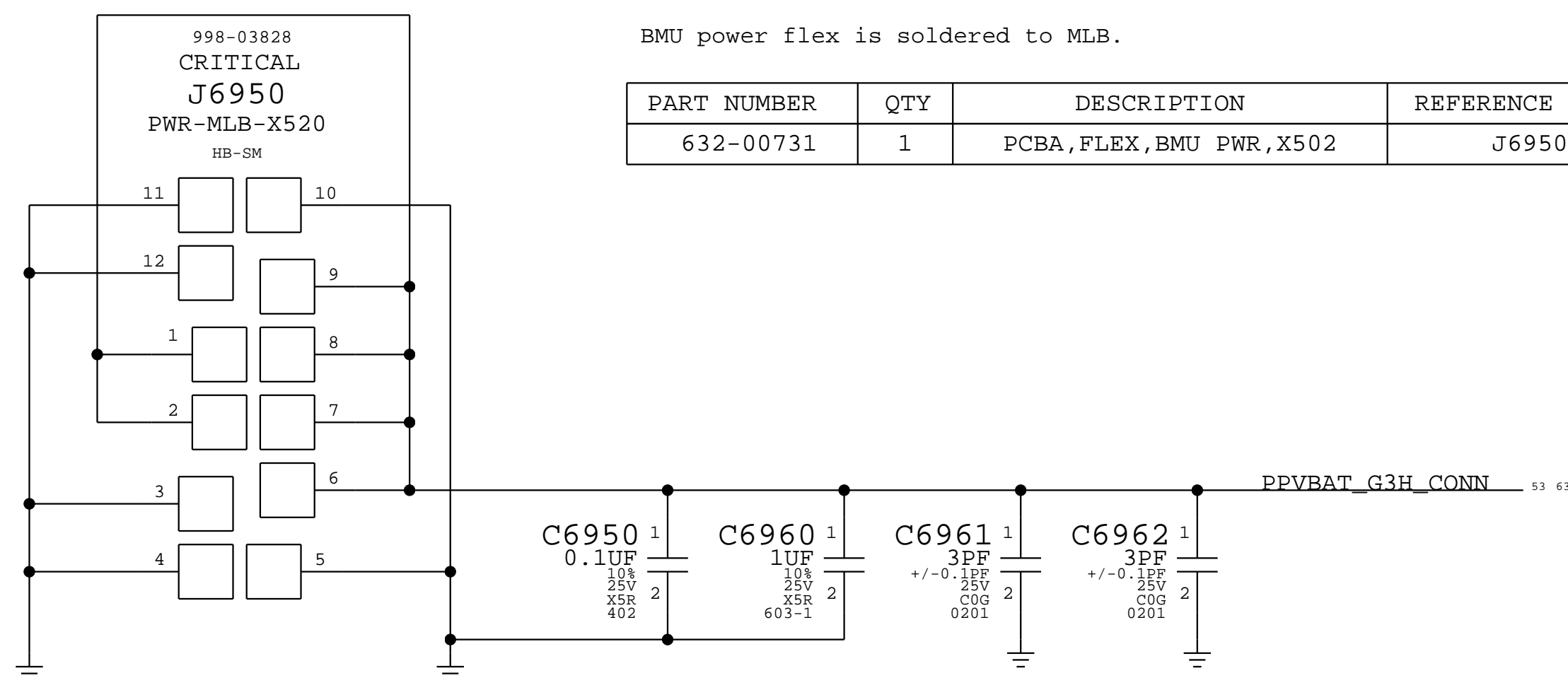
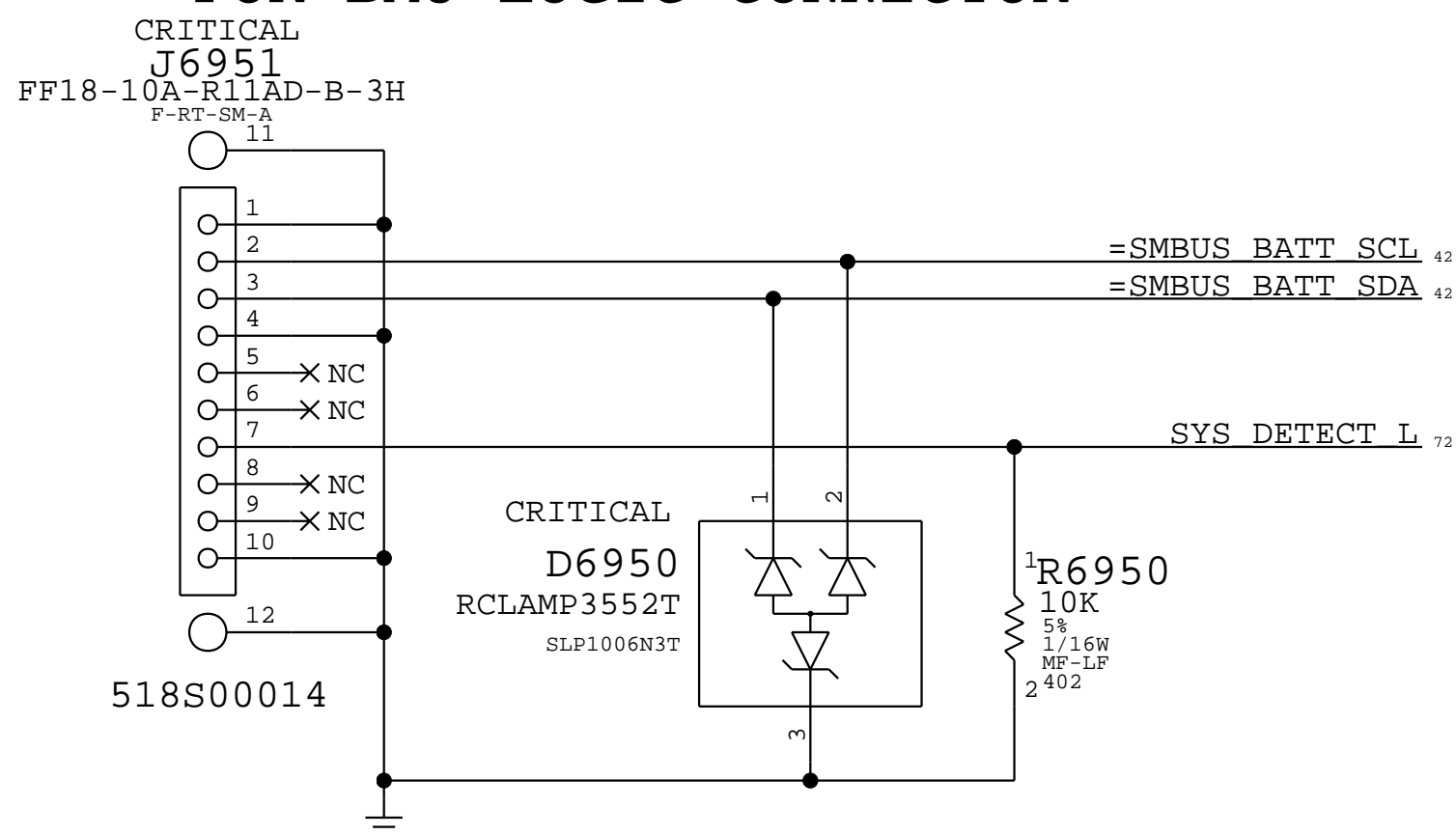
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JACK TRANSLATORS			
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		PAGE	
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		SHEET	
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POR BATTERY (BMU) FLEX SOLDER PADS.

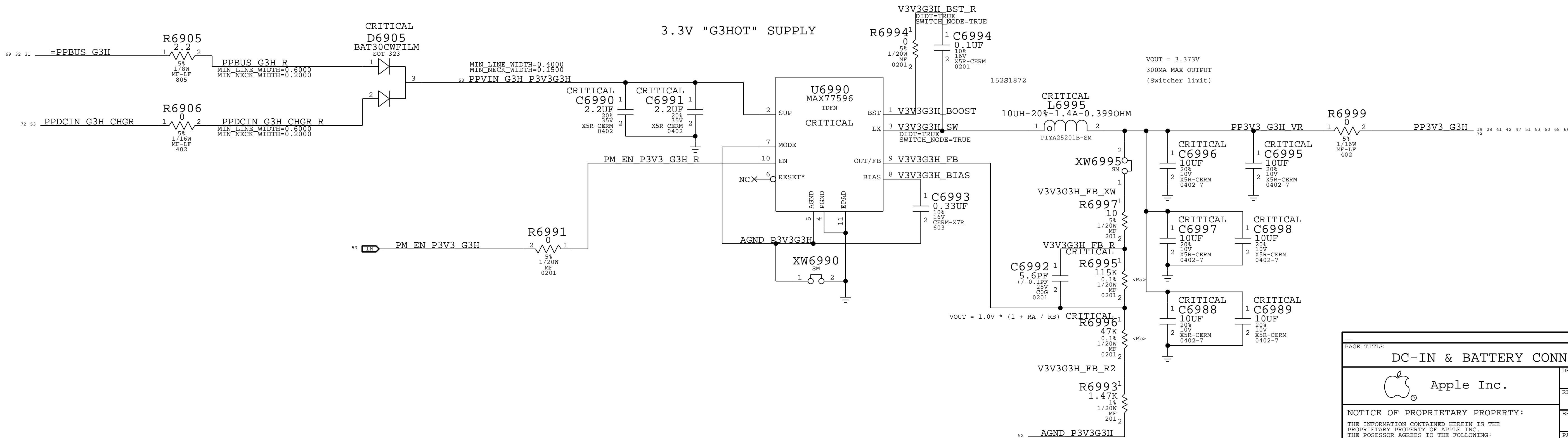
POR BMU LOGIC CONNECTOR




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00731	1	PCBA,FLEX,BMU PWR,X502	J6950	CRITICAL	

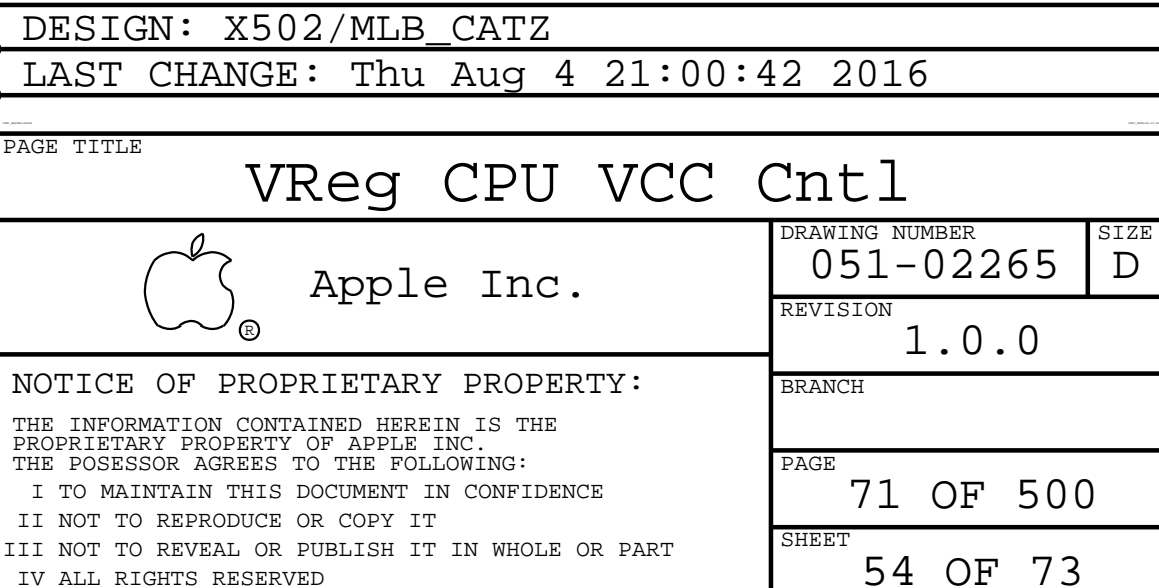
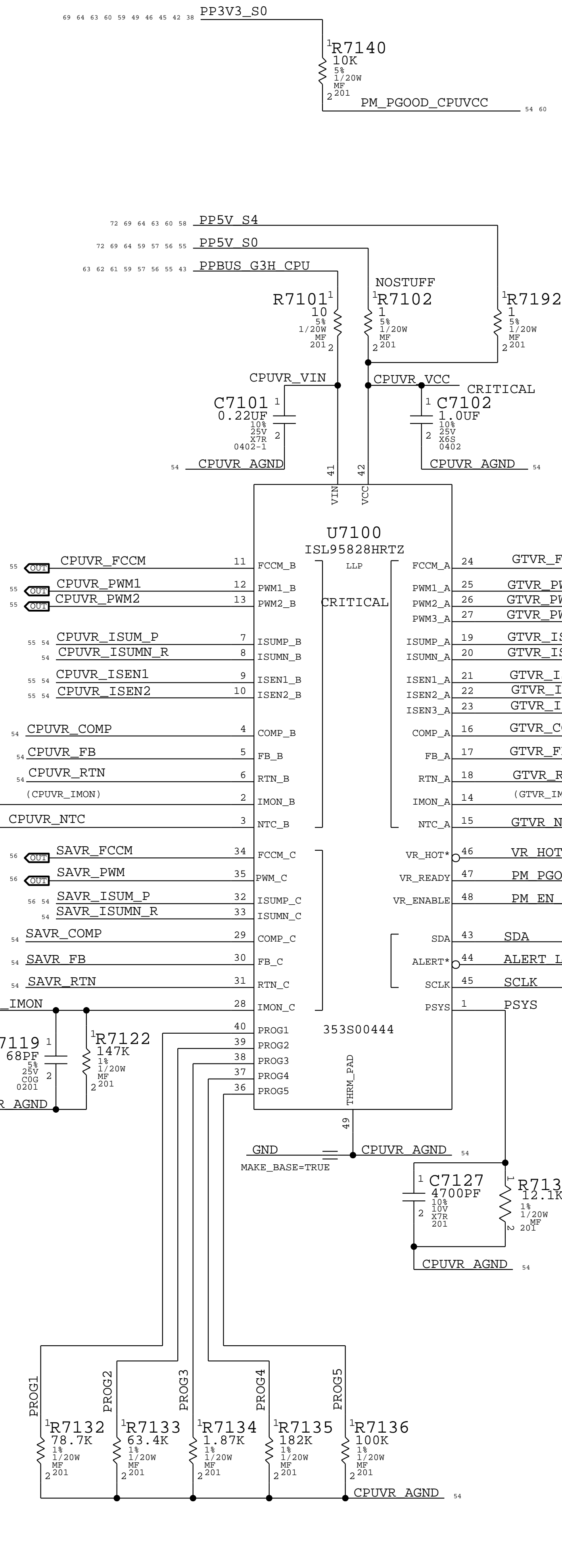
BMU power flex is soldered to MLB.

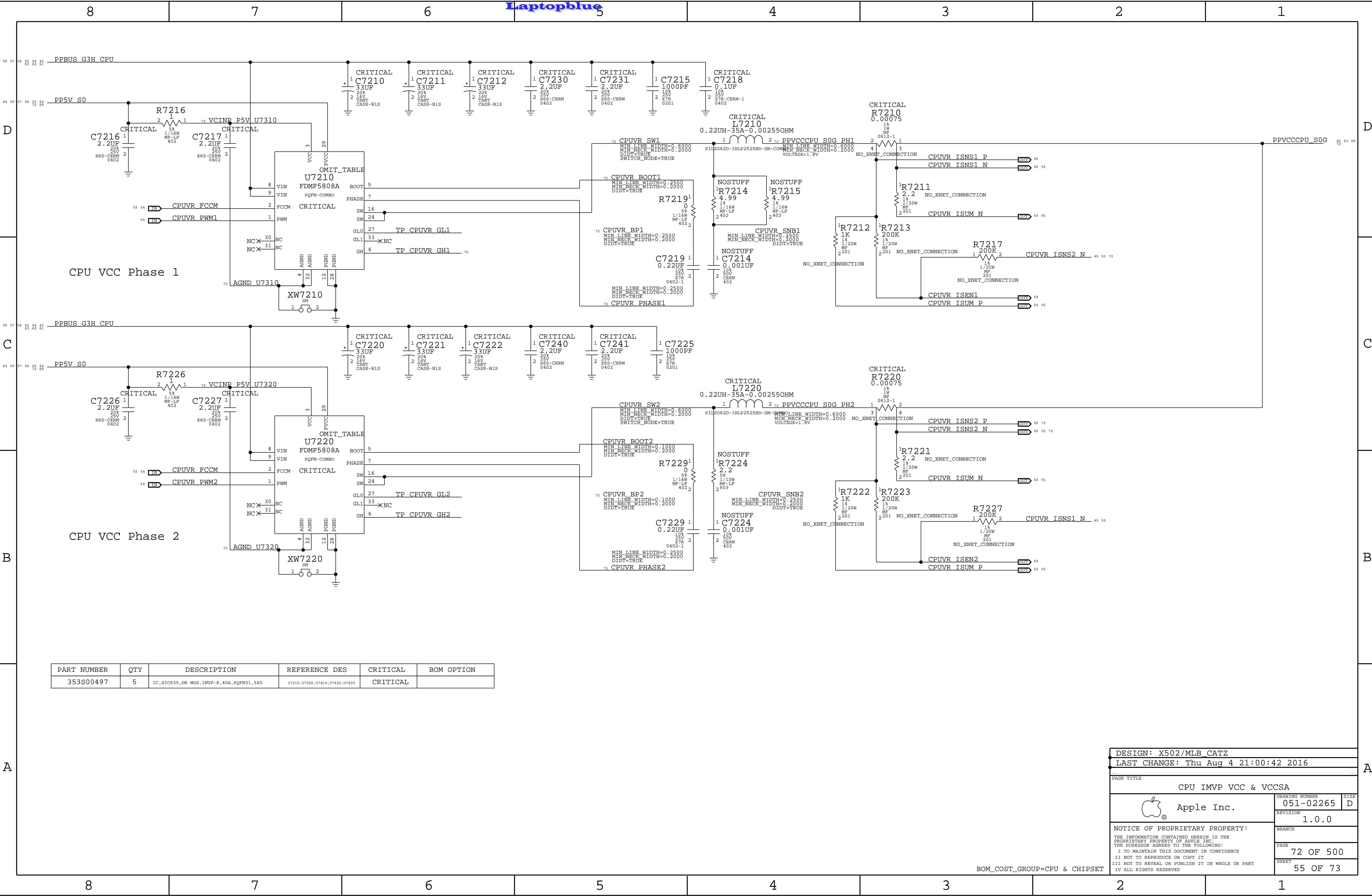
3.3V "G3HOT" SUPPLY




BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE		DRAWING NUMBER		SIZE
DC-IN & BATTERY CONNECTORS		051-02265	D	
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		SHEET 52 OF 73		



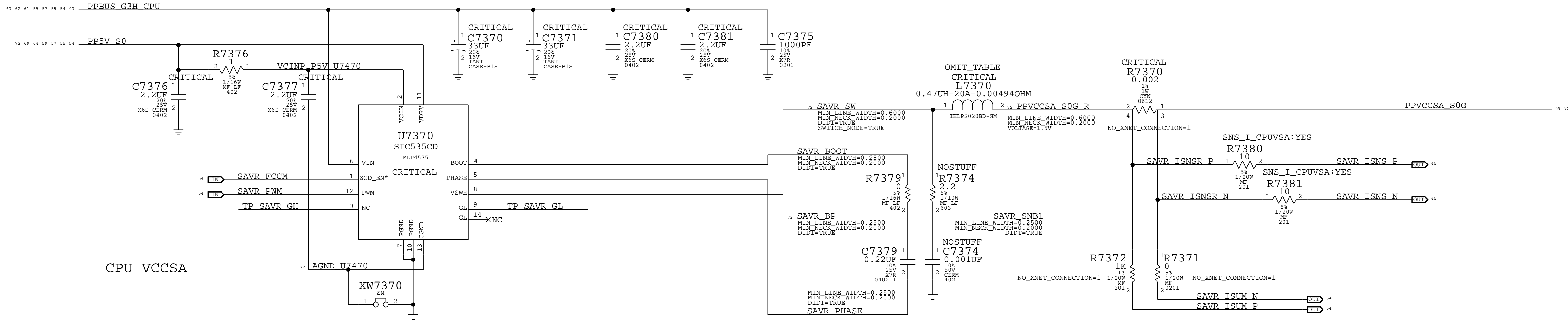


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	5	IC, SIC635, DR MOS, IMVP-8, 40A, PQFN31, 5X5	U7210, U7220, U7410, U7420, U7430	CRITICAL	

DESIGN: X502/MLB_CATZ		
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PAGE TITLE		
CPU IMVP VCC & VCCSA		
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	REVISION	1.0.0
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	PAGE	72 OF 500
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BOM_COST_GROUP=CPU & CHIPSET

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00241	1	IND,MLD,0.47UH,4.9MO,17.5A,5.4X5.2X2.4MM	L7370	CRITICAL	



CPU VCCGT Phase 1

CPU VCCGT Phase 2

CPU VCCGT PHASE 3

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PAGE TITLE

GT IMVP VCCGT



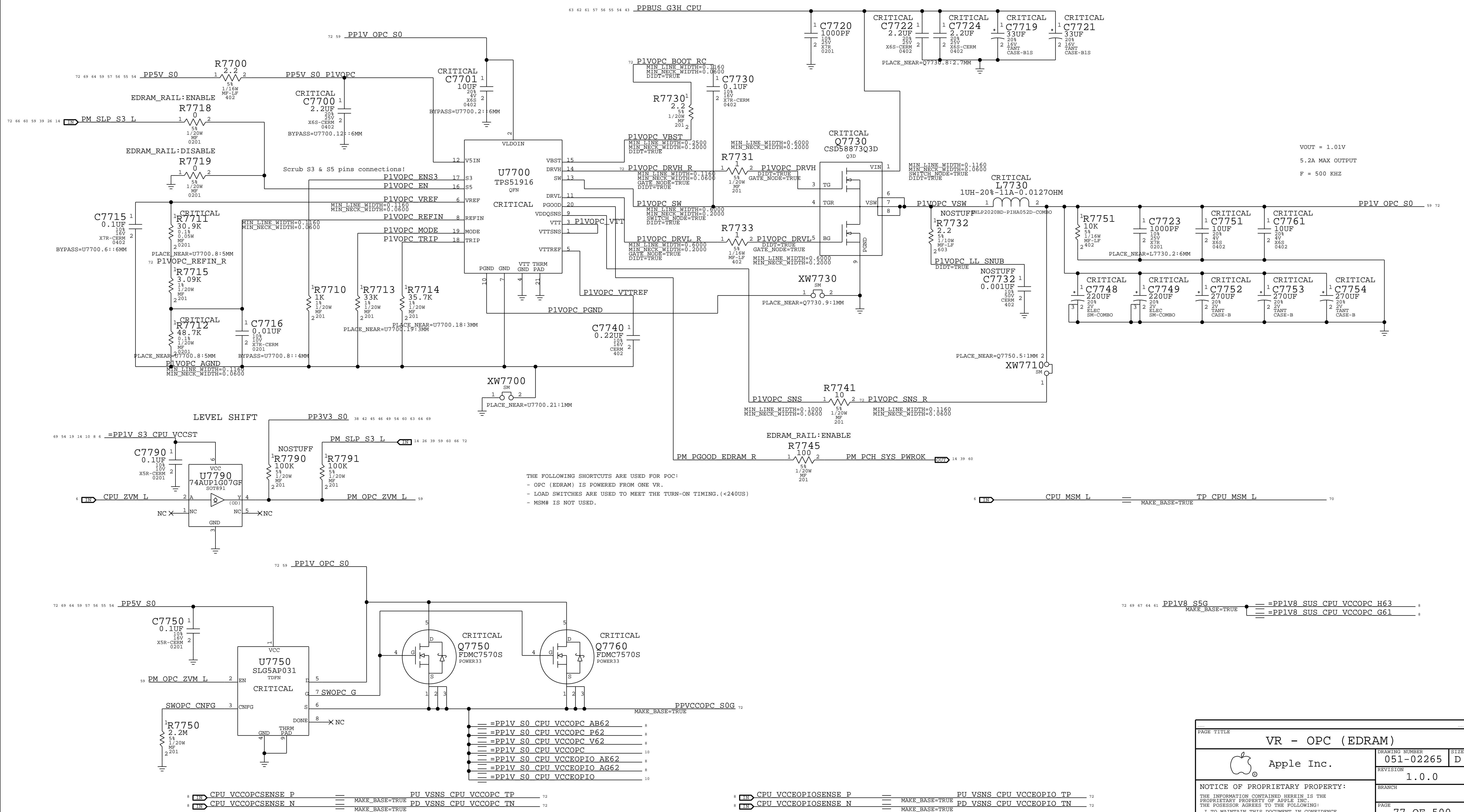
Apple Inc.

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BOM_COST_GROUP=CPU & CHIPSET

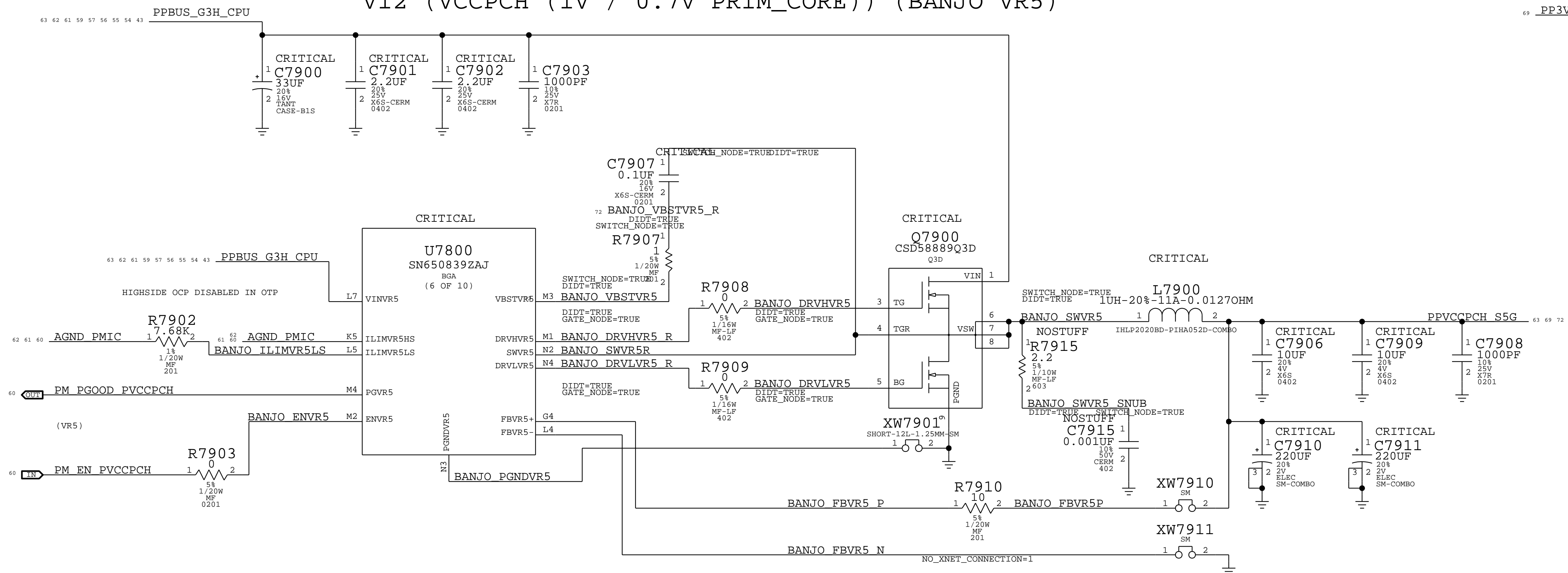
1V S0 REGULATOR FOR EDRAM (ON-PACKAGE CACHE)



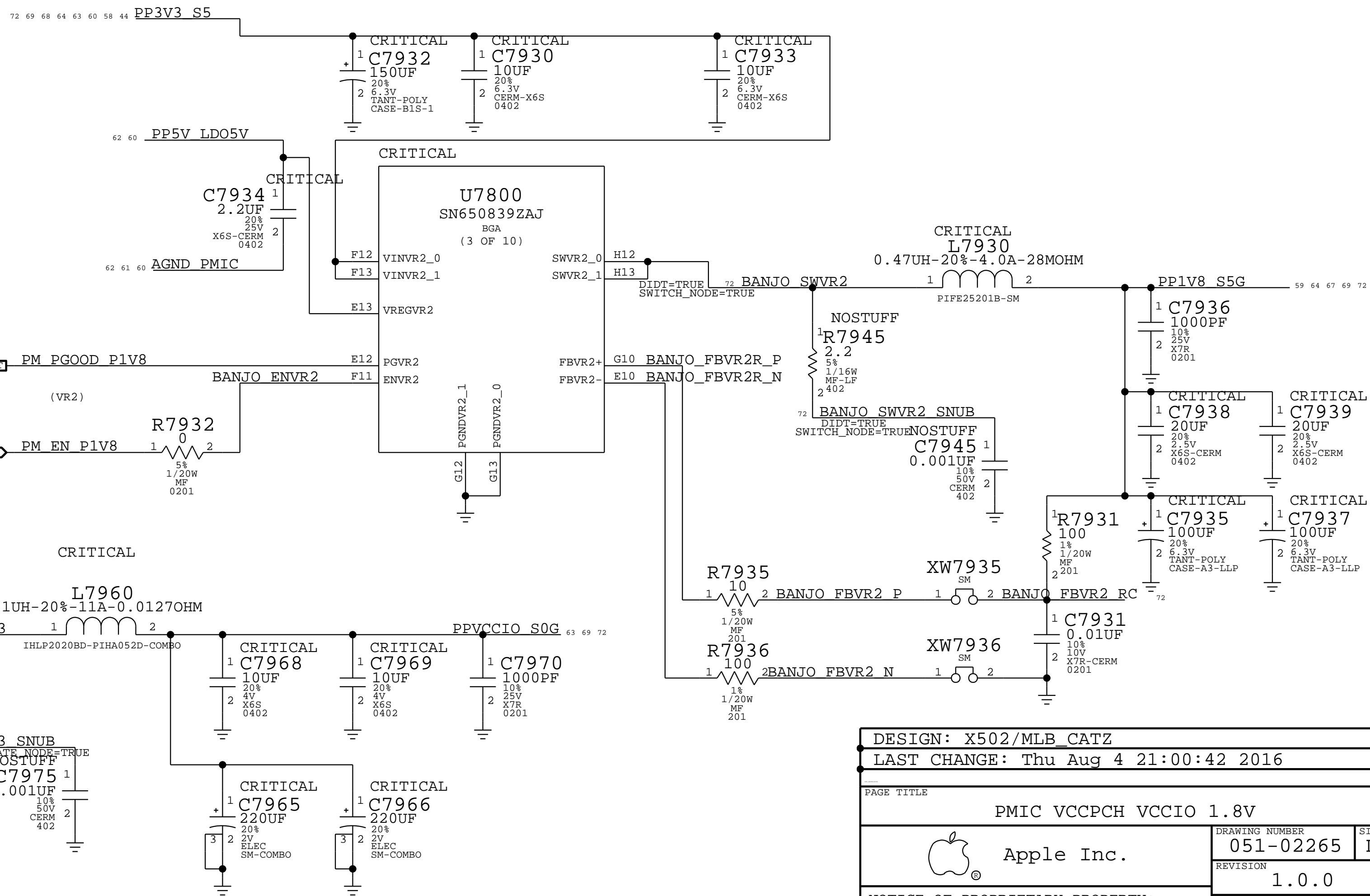
BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE		VR - OPC (EDRAM)	
	Apple Inc.	DRAWING NUMBER	051-02265
		REVISION	1.0.0
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		SHEET	59 OF 73

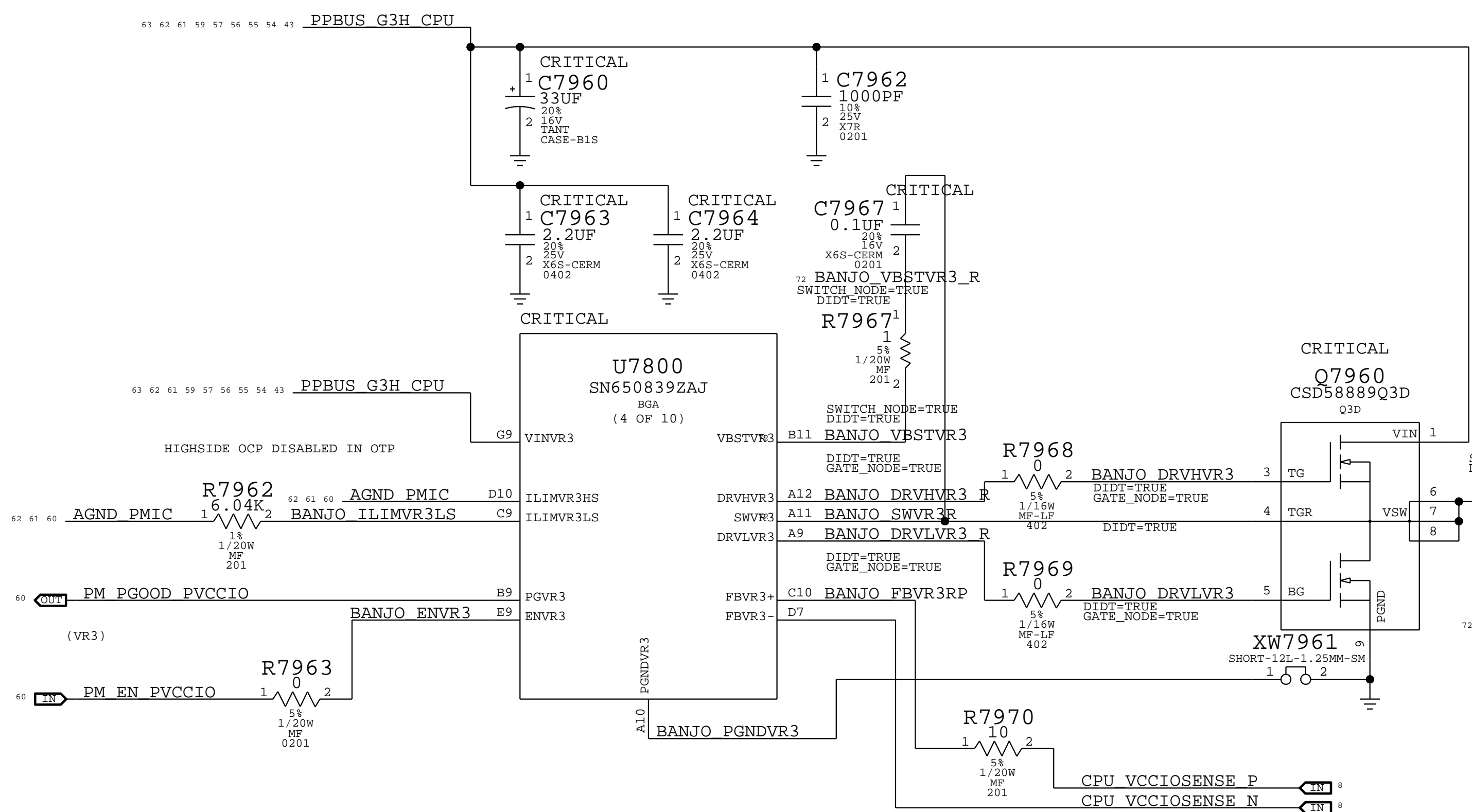
V12 (VCCPCH (1V / 0.7V PRIM_CORE)) (BANJO VR5)



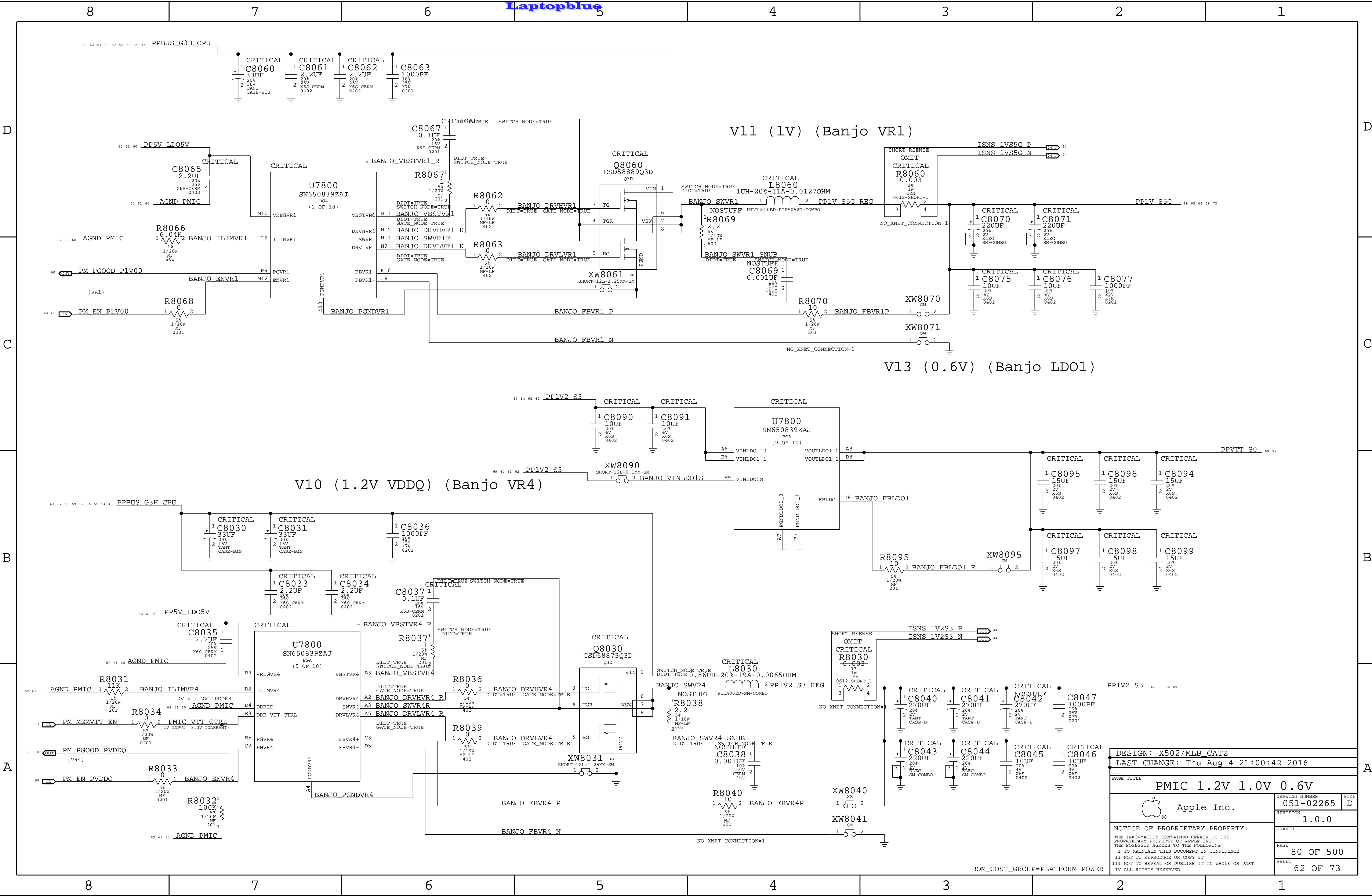
V8 (1.8V) (Banjo VR2)




V4 (0.95V VCCIO) (BANJO VR3)



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PAGE TITLE		
PMIC VCCPCH VCCIO 1.8V		
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PAGE TITLE		
PMIC 1.2V 1.0V 0.6V		
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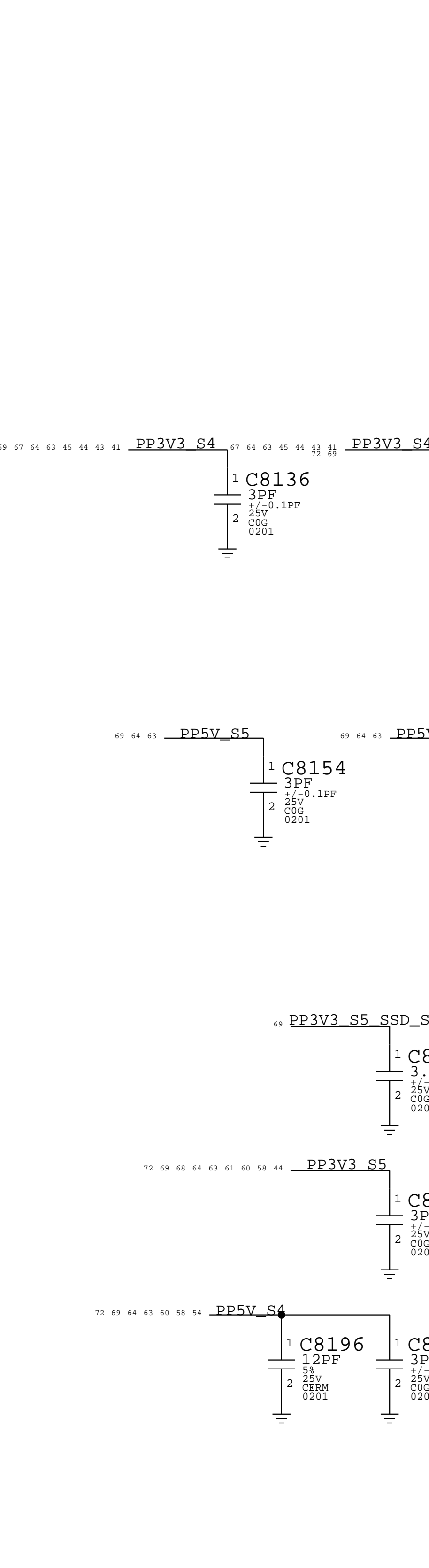
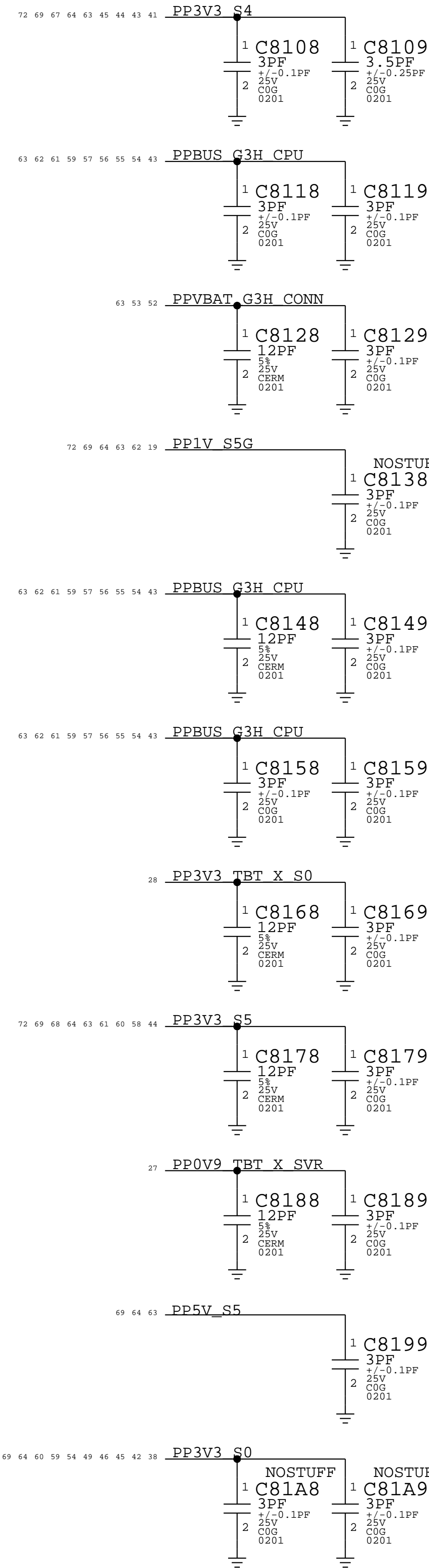
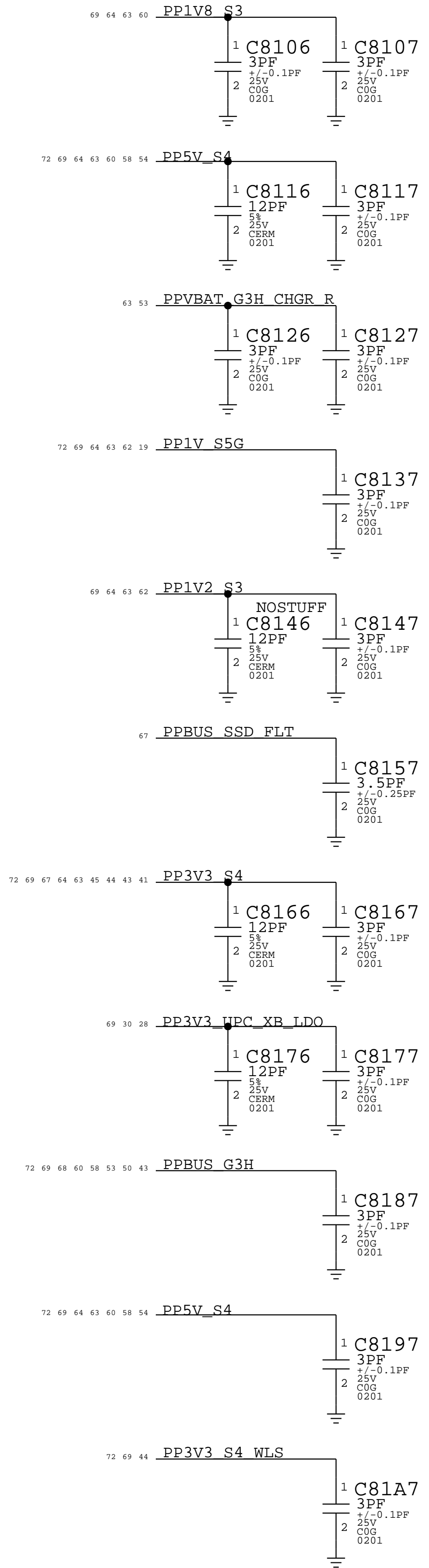
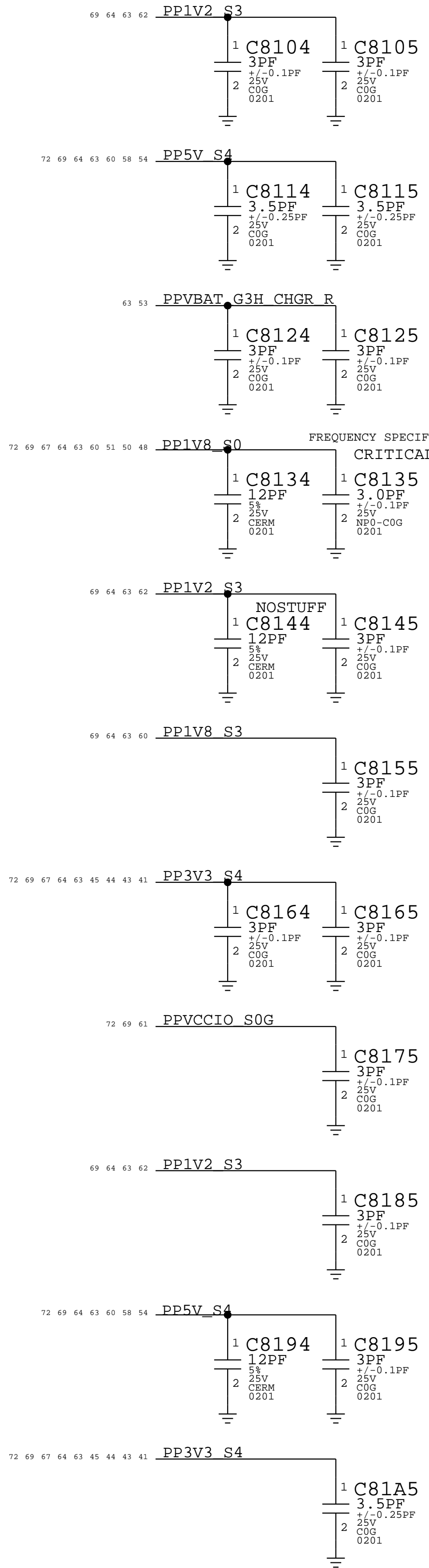
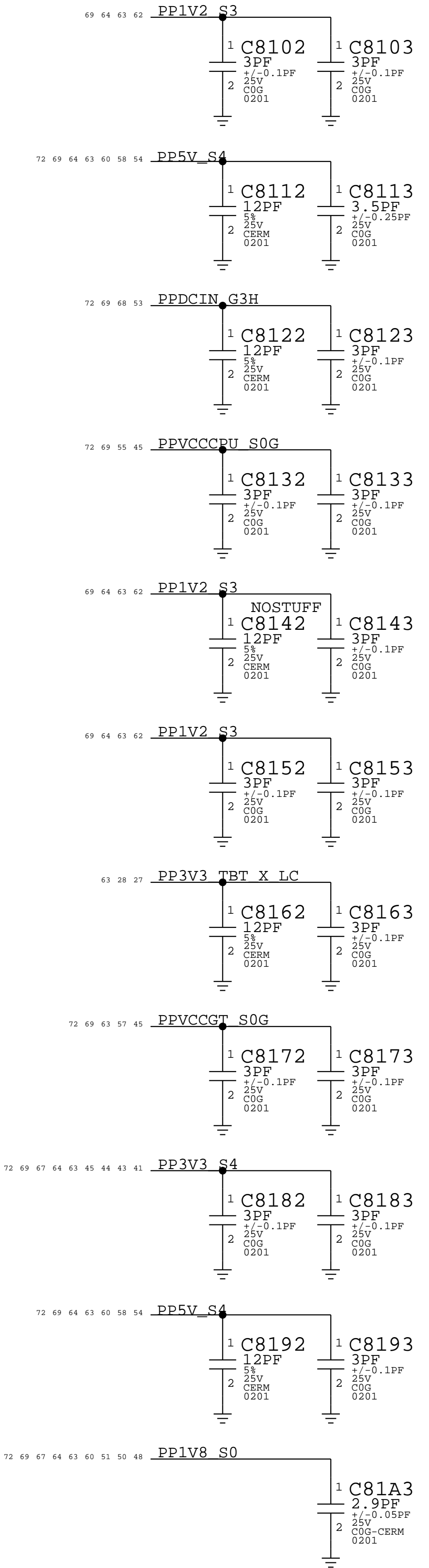
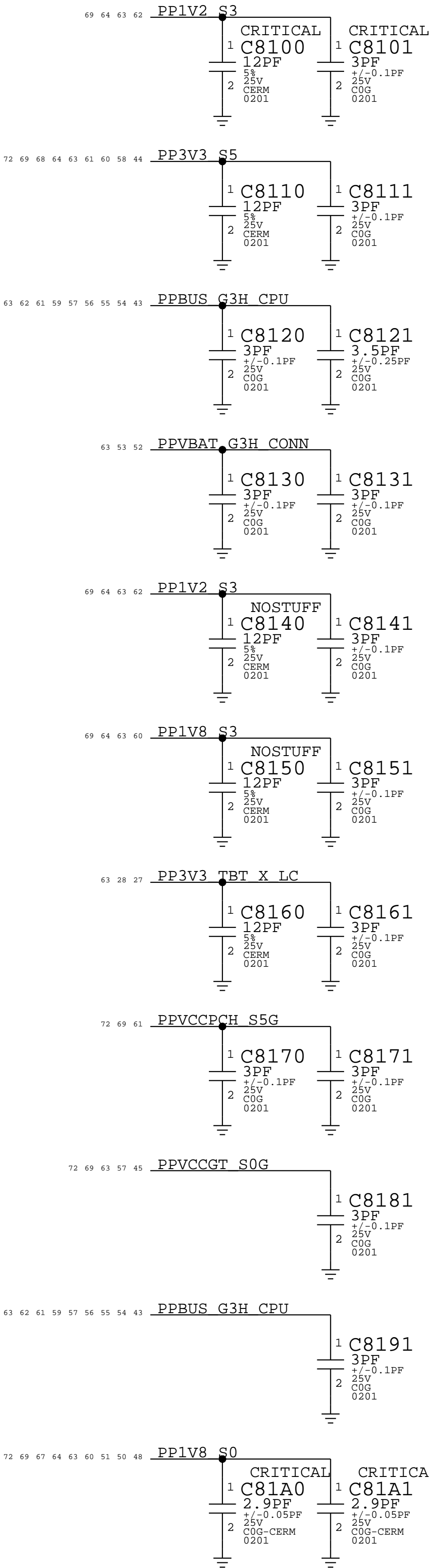
A


D

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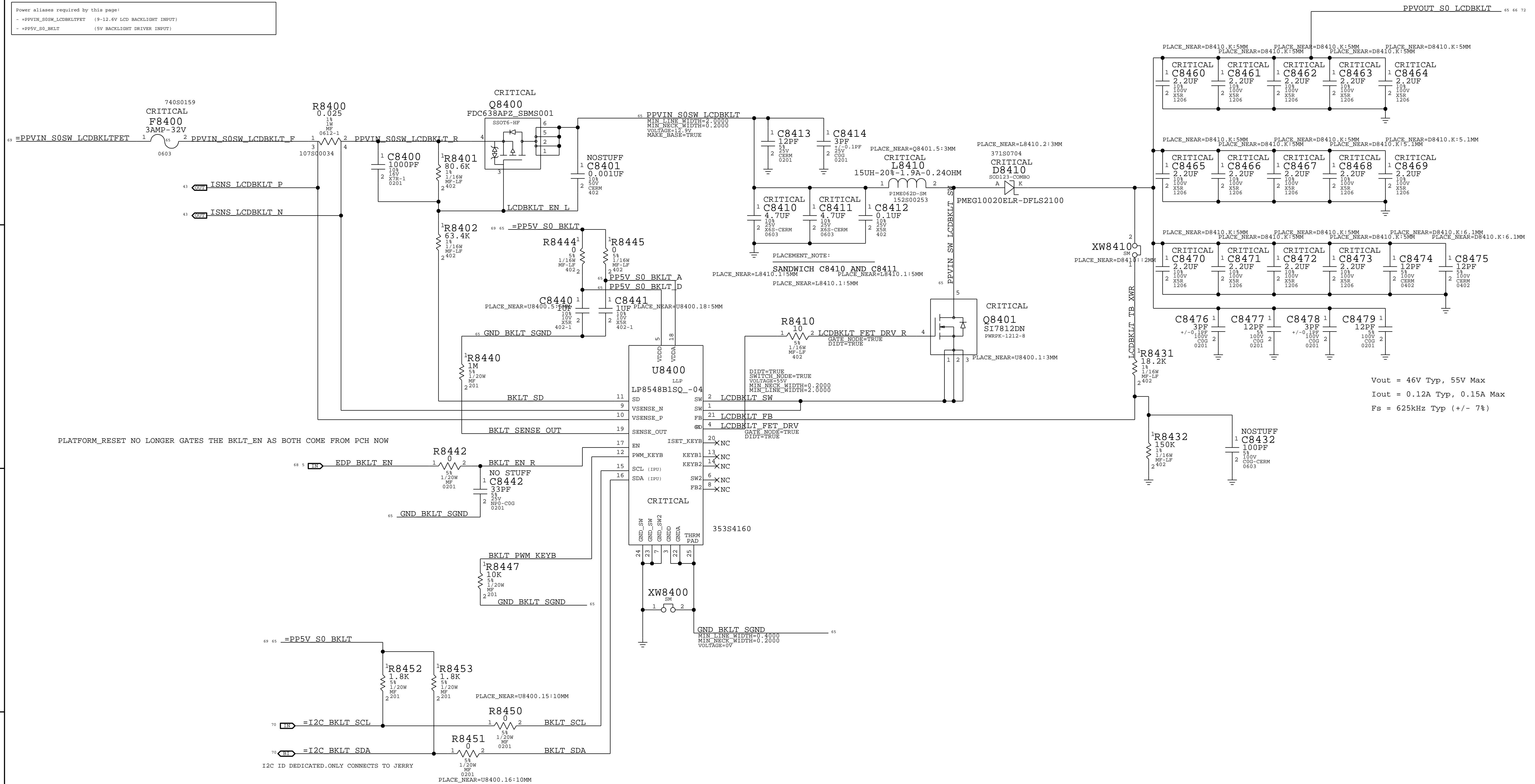
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LAST CHANGE: Thu Aug 4 21:00:42 2016		
PAGE TITLE		
RAIL DESENSE CAPS		
 Apple Inc.	DRAWING NUMBER	051-02265
	REVISION	1.0.0
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	PAGE	81 OF 500
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Page Notes

Power aliases required by this page:

```
- =PFVIN_S0SW_LCDBKLTFT (9-12.6V LCD BACKLIGHT INPUT)
```

```
- =PP5V_S0_BKLT      (5V BACKLIGHT DRIVER INPUT)
```




Vout = 46V Typ, 55V Max
Iout = 0.12A Typ, 0.15A Max
Fs = 625kHz Typ (+/- 7%)

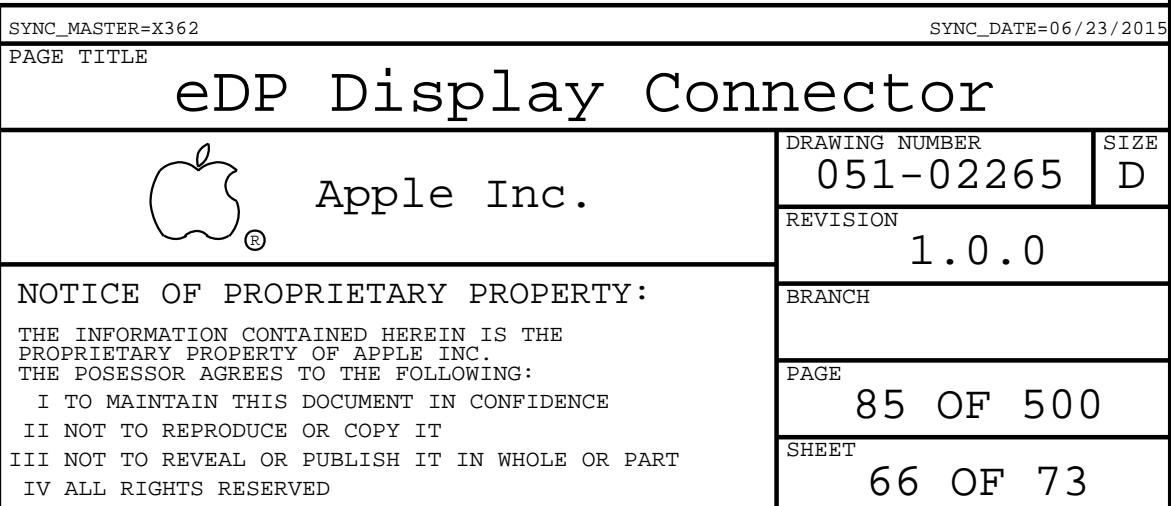
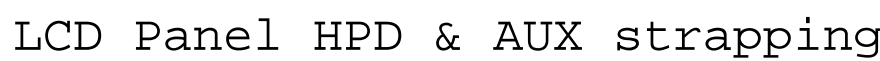
LINE WIDTHS

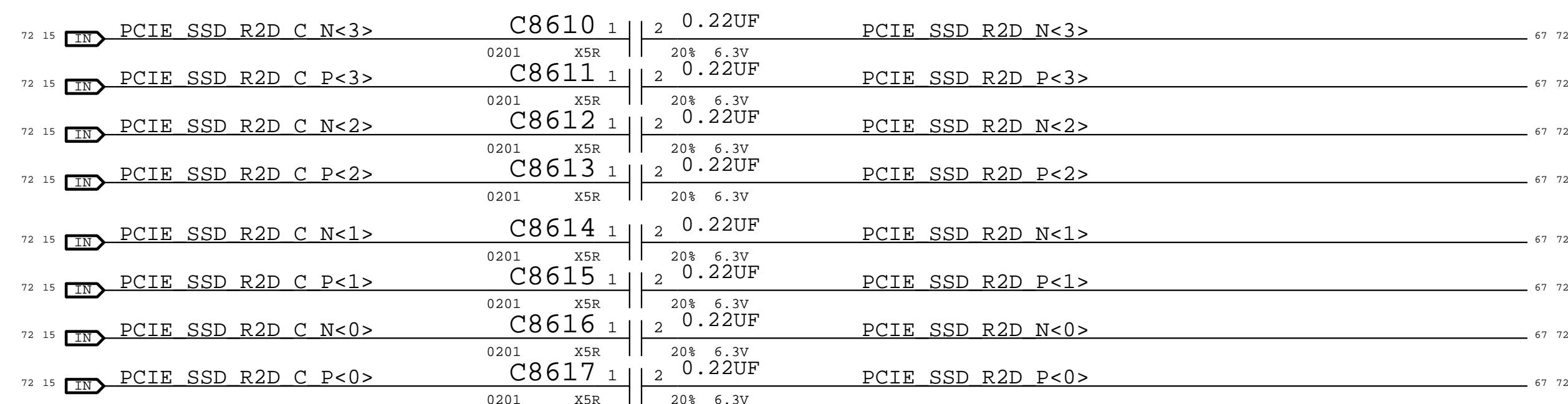
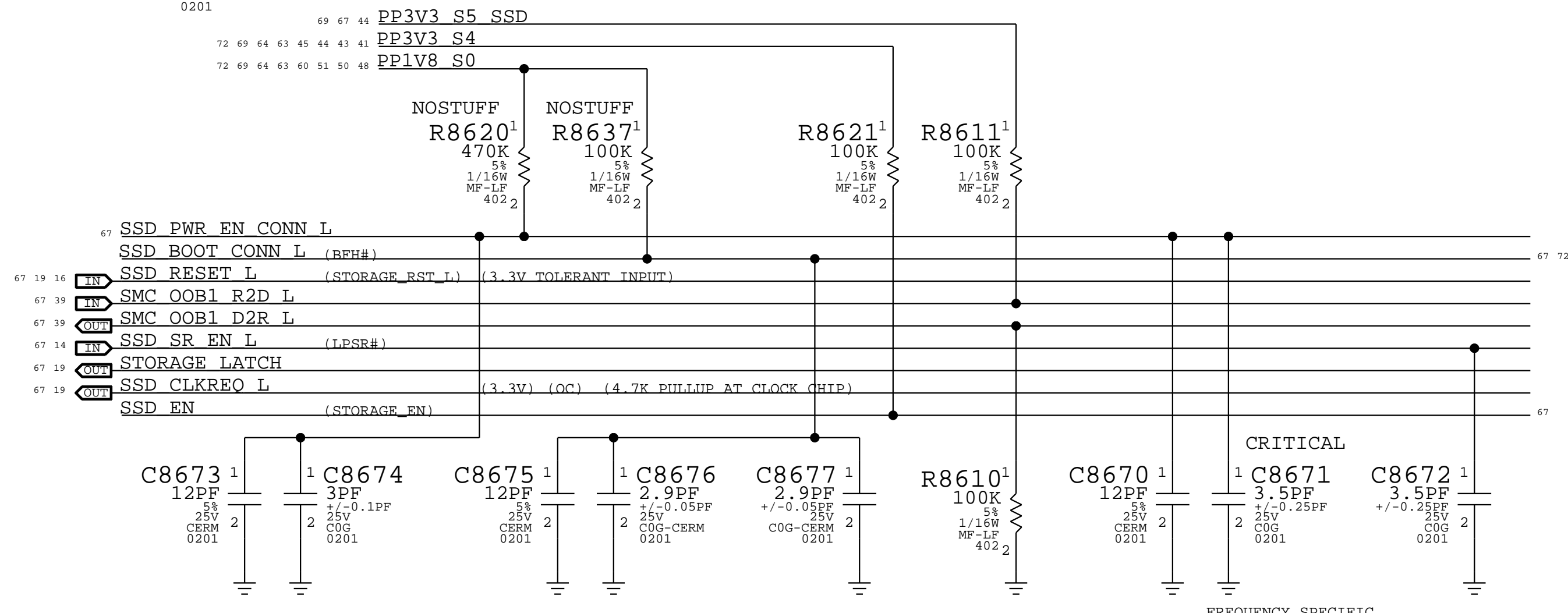
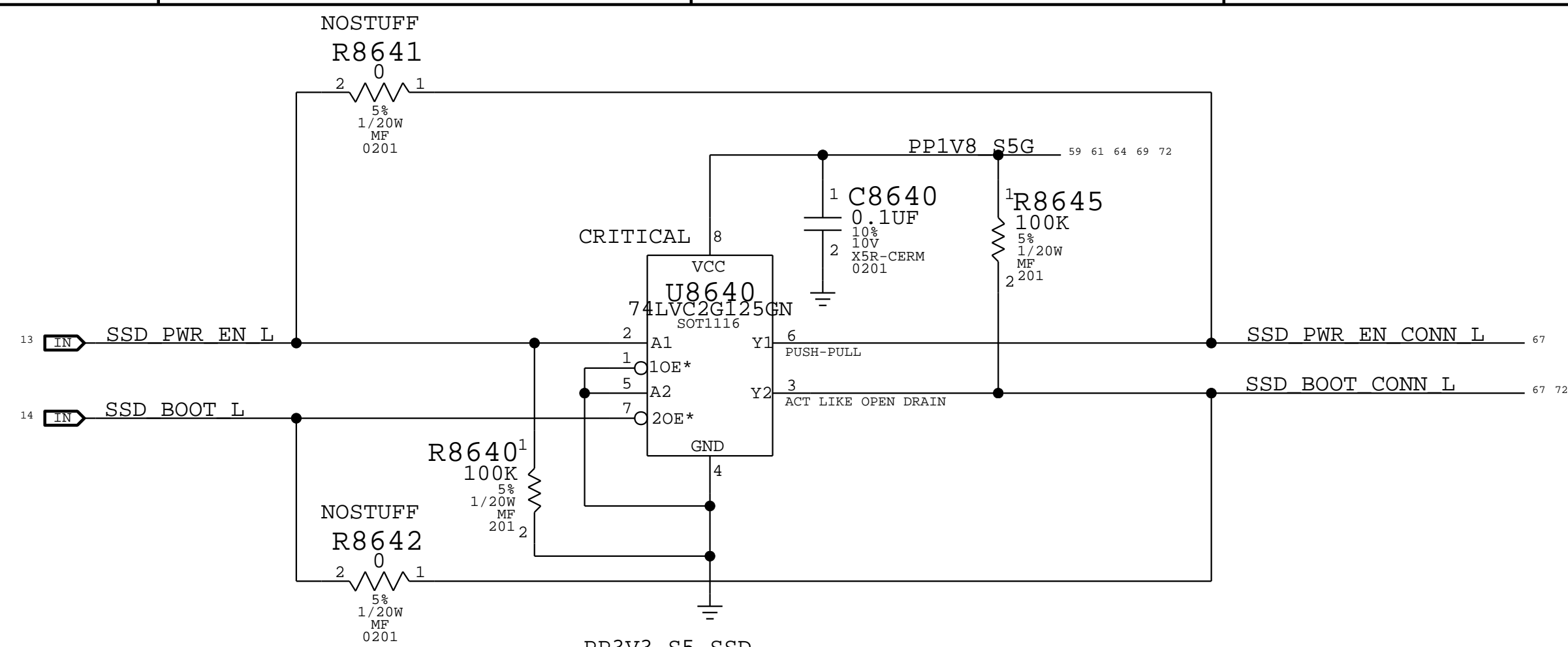
PBUS LINE WIDTHS

LCD BKLT LINE WIDTHS

PP5V_S0_BKLT_A	65	PPVIN_S0SW_LCDBKLT_F	65	LCDBKLT_FET_DRV	65	PPVIN_SW_LCDBKLT_SW	65
MIN_LINE_WIDTH=2.0000		MIN_LINE_WIDTH=6.0000		MIN_LINE_WIDTH=6.0000		MIN_LINE_WIDTH=2.0000	
MIN_NECK_WIDTH=0.2000		MIN_NECK_WIDTH=0.2000		MIN_NECK_WIDTH=0.2000		MIN_NECK_WIDTH=0.2000	
VOLTAGE=5V		VOLTAGE=12.9V		VOLTAGE=5V		VOLTAGE=5V	
		PPVIN_S0SW_LCDBKLT_R	65	GATE_NODE=TRUE		D1D1=TRUE	
		MIN_LINE_WIDTH=2.0000				SWITCH_NODE=TRUE	
		MIN_NECK_WIDTH=0.2000				D1D1=TRUE	
		VOLTAGE=12.9V				PPVOUT_S0_LCDBKLT	65 66 72
		PPVIN_S0SW_LCDBKLT	65			MIN_LINE_WIDTH=0.5000	
		MIN_LINE_WIDTH=2.0000				MIN_NECK_WIDTH=0.2000	
		MIN_NECK_WIDTH=0.2000				VOLTAGE=55V	
		VOLTAGE=12.9V					

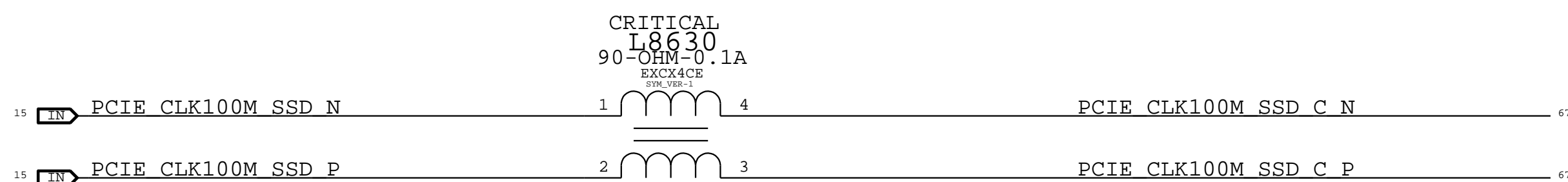
FORM NO. 100 (REVISED 10/01)		FORM NO. 100 (REVISED 10/01)	
PAGE TITLE			
LCD Backlight Driver			
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			SIZE D
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AC CAPS FOR PCIE GEN 3

Per PCIe spec, only TX side should have AC cap

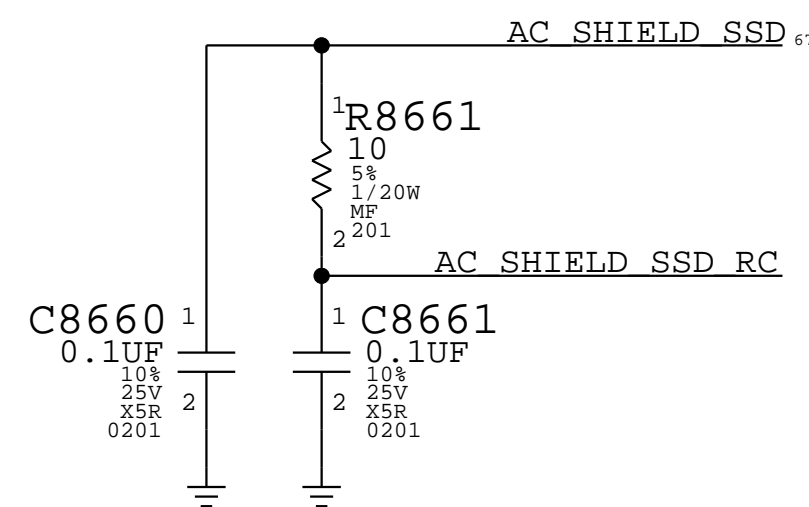
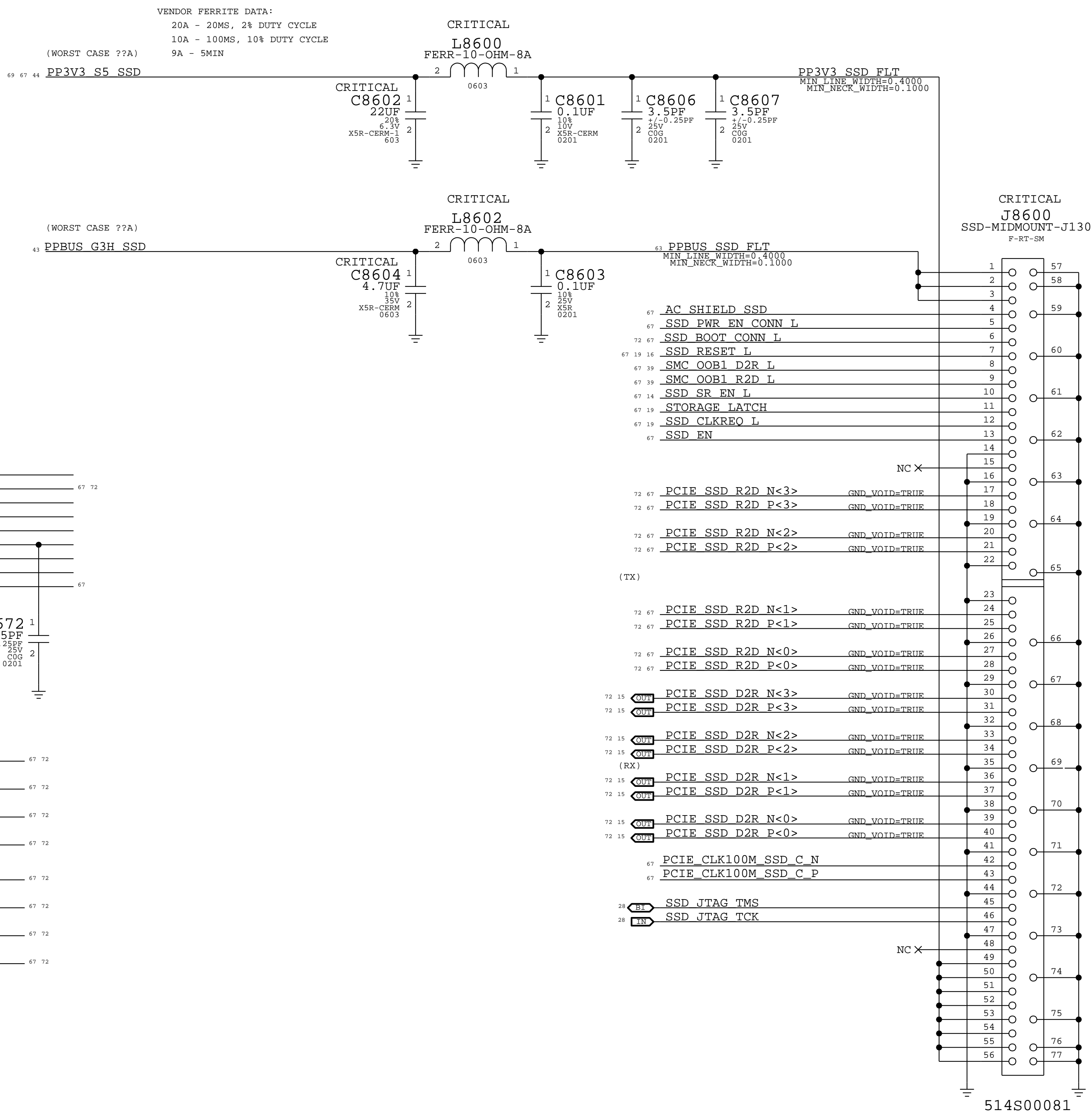
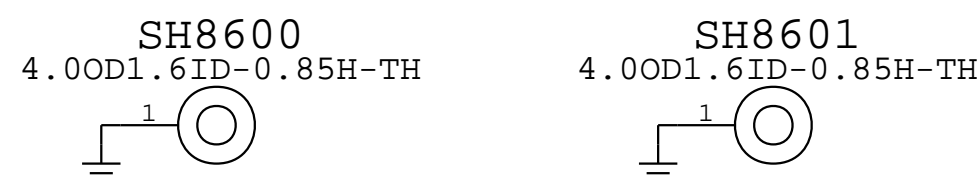



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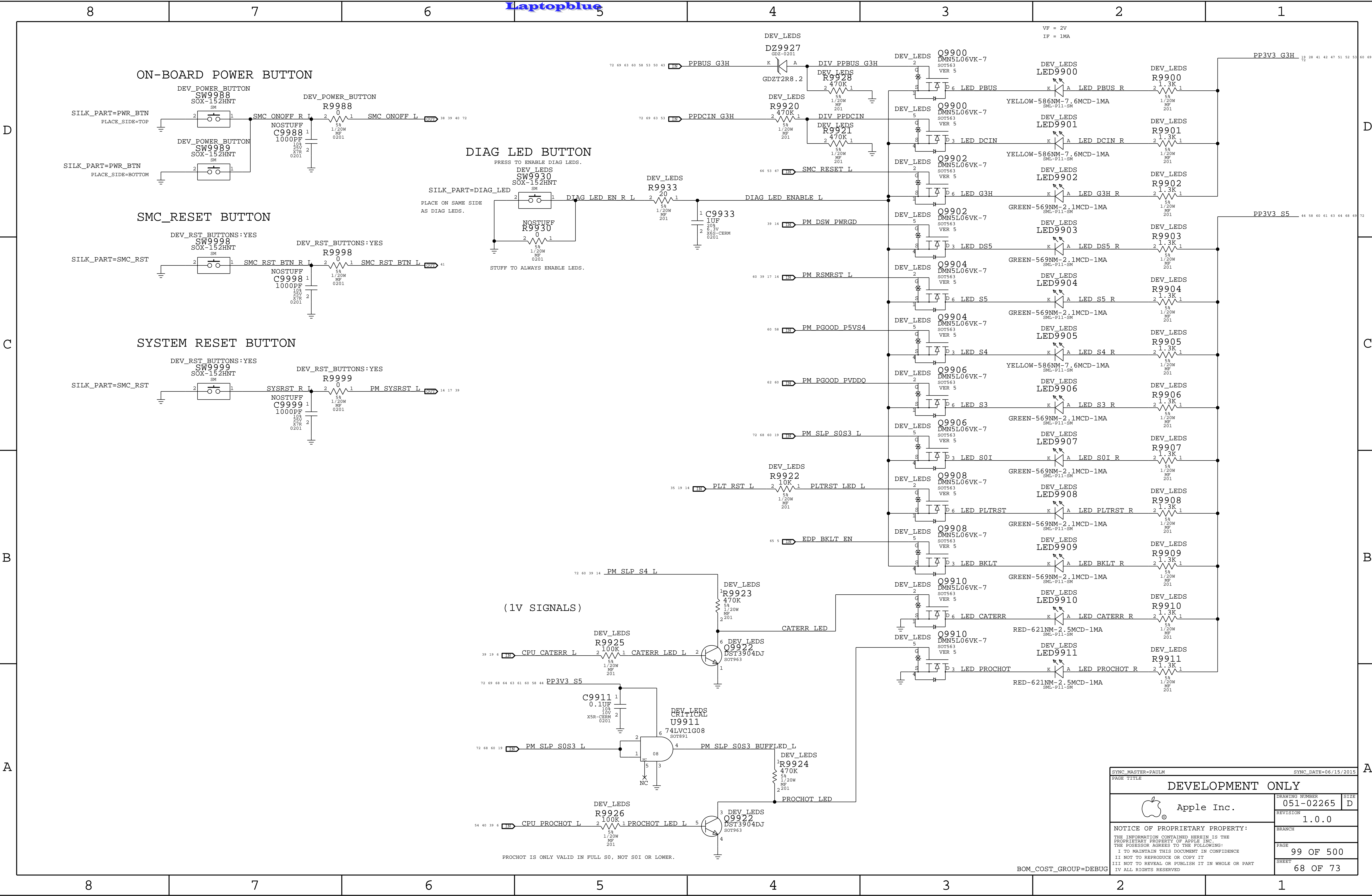
1. POWER-ON TO PERST_L DE-ASSERTION = 10MS MINIMUM
2. PP3V3_EN: PROVIDE 10MS EARLY WARNING TO SSD THAT POWER WILL BE OFF.
(PIN 47, PP3V3_EN, IS NOT USED BY SAMSUNG UAX AND SANDISK SSD.)
3. PCIE CLK100M ARE 2.5V SIGNALS.
4. OOB SIGNALS: UART 3.3V, 115.2 KBAUD, 8B, NO PARITY, 1 STOP BIT.


SSD STANDOFFS

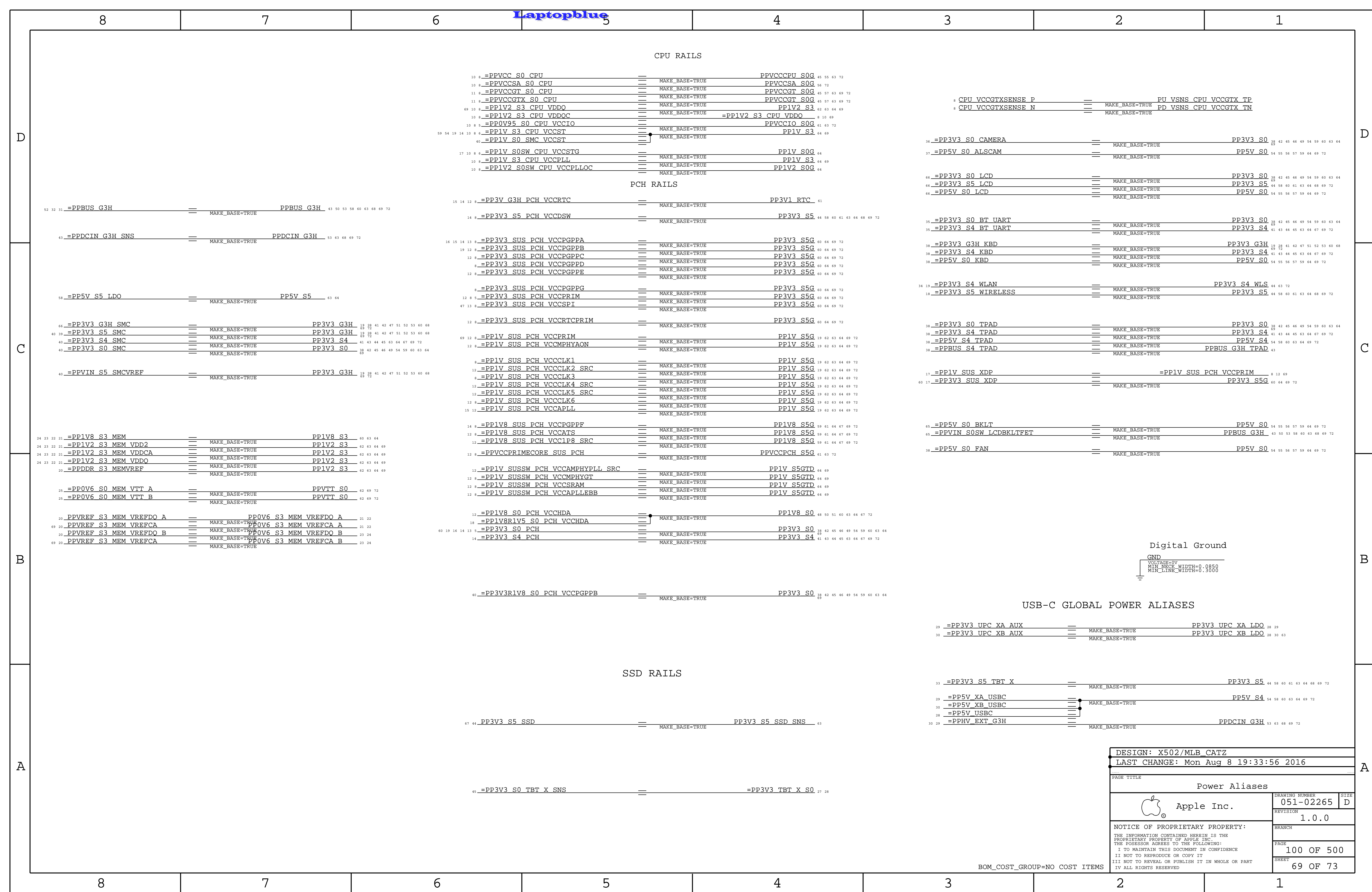
860-00380





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SSD MODULE		
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UNUSED GPIOS, HSIO

8		VCCPRIM_CORE_VID0	==	MAKE_BASE=TRUE	NO_TEST=1	NC VCCPRIM_CORE_VID0
9		VCCPRIM_CORE_VID1	==	MAKE_BASE=TRUE	NO_TEST=1	NC VCCPRIM_CORE_VID1
16		MLB_DEV_L	==	MAKE_BASE=TRUE	NO_TEST=1	NC MLB_DEV_L

16	IN	I2C UPC SDA	==	MAKE_BASE=TRUE	NO_TEST=1	NC	I2C UPC SDA
16	IN	I2C UPC SCL	==	MAKE_BASE=TRUE	NO_TEST=1	NC	I2C UPC SCL



13	IN	PCH BSSB CLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC	PCH BSSB CLK
13	IN	PCH BSSB DATA	==	MAKE_BASE=TRUE	NO_TEST=1	NC	PCH BSSB DATA

16	IN	TBT X DPMUX SEL	—	MAKE_BASE=TRUE	NO_TEST=1	NC TBT X DPMUX SEL
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14	TBT T CIO PWR EN	==	MAKE_BASE=TRUE	No_TEST=1	NC TBT T CIO PWR EN
14	TBT T USB PWR EN	==	MAKE_BASE=TRUE	No_TEST=1	NC TBT T USB PWR EN
14	TBT T PCI RESET L	==	MAKE_BASE=TRUE	No_TEST=1	NC TBT T PCI RESET L
14	TBT T DPMUX SEL	==	MAKE_BASE=TRUE	No_TEST=1	NC TBT T DPMUX SEL
14	=TBT T CLKREQ L	==	MAKE_BASE=TRUE	No_TEST=1	NC TBT T CLKREQ L
14	PCIE CLK100M TBT T N	==	MAKE_BASE=TRUE	No_TEST=1	NC PCIE CLK100M TBT TN
14	PCIE CLK100M TBT T P	==	MAKE_BASE=TRUE	No_TEST=1	NC PCIE CLK100M TBT TP
14	PCIE TBT T D2R N<0>	==	MAKE_BASE=TRUE	No_TEST=1	NC PCIE TBT T D2RN0
14	PCIE TBT T D2R P<0>	==	MAKE_BASE=TRUE	No_TEST=1	NC PCIE TBT T D2RP0
14	PCIE TBT T R2D C N<0>	==	MAKE_BASE=TRUE	No_TEST=1	NC PCIE TBT T R2D CN0
14	PCIE TBT T R2D C P<0>	==	MAKE_BASE=TRUE	No_TEST=1	NC PCIE TBT T R2D CP0
14	PCIE TBT T D2R N<1>	==	MAKE_BASE=TRUE	No_TEST=1	NC PCIE TBT T D2RN1
14	PCIE TBT T D2R P<1>	==	MAKE_BASE=TRUE	No_TEST=1	NC PCIE TBT T D2RP1
14	PCIE TBT T R2D C N<1>	==	MAKE_BASE=TRUE	No_TEST=1	NC PCIE TBT T R2D CN1
14	PCIE TBT T R2D C P<1>	==	MAKE_BASE=TRUE	No_TEST=1	NC PCIE TBT T R2D CP1



15		USB CAMERA DFR N	---	MAKE_BASE=TRUE	NO_TEST=1	NC USB2 03N
16		USB CAMERA DFR P	---	MAKE_BASE=TRUE	NO_TEST=1	NC USB2 03P







```
13 IN DEBUGUART SEL SOC — MAKE_BASE=TRUE NO_TEST=1 NC DEBUGUART SEL SOC
```

1		USB3_EXTB_D2R_N	==	MAKЕ_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_D2RN
15		USB3_EXTB_D2R_P	==	MAKЕ_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_D2RP
16		USB3_EXTB_R2D_C_N	==	MAKЕ_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_R2DCN
17		USB3_EXTB_R2D_C_P	==	MAKЕ_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_R2DCP

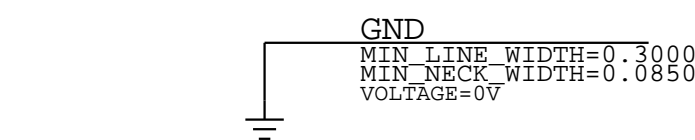
26	B₁	=DP X SRC ML P<3..0>	==	MAKE_BASE=TRUE	NO_TEST=1	NC DP X SRC ML CP<3..0>
26	B₂	=DP X SRC ML N<3..0>	==	MAKE_BASE=TRUE	NO_TEST=1	NC DP X SRC ML CN<3..0>

26	B₁	=DP X SRC AUX P	==	MAKE_BASE=TRUE	NO_TEST=1	NC DP X SRC AUXCHP
26	B₂	=DP X SRC AUX N	==	MAKE_BASE=TRUE	NO_TEST=1	NC DP X SRC AUXCHN

15		USB EXTA N	==	MAKE_BASE=TRUE	NO_TEST=1	NC USB2 01N
15		USB EXTA P	==	MAKE_BASE=TRUE	NO_TEST=1	NC USB2 01P

15		NC USB2 05N	NO TEST=1
15		NC USB2 05P	NO TEST=1
15		NC USB2 06N	NO TEST=1
15		NC USB2 06P	NO TEST=1
15		NC USB2 07N	NO TEST=1
15		NC USB2 07P	NO TEST=1

15	BI	NC USB2 09N	NO_TEST=1
15	BI	NC USB2 09P	NO_TEST=1
15	BI	NC USB2 10N	NO_TEST=1
15	BI	NC USB2 10P	NO_TEST=1



Digital Ground

14	IN	TP BT I2S_CLK	MAK_F_BASE=TRUE	NO_TEST=1	NC BT I2S_CLK
14	IN	TP BT I2S_D2R	MAK_F_BASE=TRUE	NO_TEST=1	NC BT I2S_D2R
14	IN	TP BT I2S_R2D	MAK_F_BASE=TRUE	NO_TEST=1	NC BT I2S_R2D
14	IN	TP BT I2S_SYNC	MAK_F_BASE=TRUE	NO_TEST=1	NC BT I2S_SYNC
36	IN	TP CAM_GPIO3	MAK_F_BASE=TRUE	NO_TEST=1	NC CAM_GPIO3
6	IN	TP CPU_A5	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_A5
6	IN	TP CPU_AU5	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_AU5
6	IN	TP CPU_AY4	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_AY4
6	IN	TP CPU_BB3	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_BB3
6	IN	TP CPU_BB5	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_BB5
50	IN	TP CPU_MSM_L	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_MSM_L
9	IN	TP CPU_NCTFVSS_A5	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_NCTFVSS_A5
9	IN	TP CPU_NCTFVSS_A70	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_NCTFVSS_A70
9	IN	TP CPU_NCTFVSS_AV1	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_NCTFVSS_AV1
9	IN	TP CPU_NCTFVSS_B71	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_NCTFVSS_B71
9	IN	TP CPU_NCTFVSS_BA1	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_NCTFVSS_BA1
9	IN	TP CPU_NCTFVSS_BA71	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_NCTFVSS_BA71
9	IN	TP CPU_NCTFVSS_BB70	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_NCTFVSS_BB70
9	IN	TP CPU_NCTFVSS_C1	MAK_F_BASE=TRUE	NO_TEST=1	NC CPU_NCTFVSS_C1

13	TP PCH CLKOUT LPC1	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH CLKOUT LPC1
14	TP PCH GPD7	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPD7

14	TP PCH GPP D0	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP D0
14	TP PCH GPP D1	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP D1
14	TP PCH GPP D3	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP D3
14	TP PCH GPP D4	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP D4
14	TP PCH GPP E15	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP E15
14	TP PCH GPP F8	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP F8
14	TP PCH GPP F9	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP F9
14	TP PCH GPP F10	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP F10
14	PCH BT ROM BOOT	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP F11
13	PCH SOC DFU STATUS	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP F18
13	SOC PANIC L	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP F19
13	SOC S2R ACK L	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP F20
13	SOC SLEEP L	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH GPP F21
14	TP PCH LANPHYPC	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH LANPHYPC
14	TP PCH PME L	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH PME L

17	TP PCH SLP WLAN L	MAK_F_BASE=TRUE	NO_TEST=1	NC PCH SLP WLAN L
17	TP PCH STRP ESPI	MAK_F_BASE=TRUE	NO_TEST=1	NC PCH STRP ESPI
17	TP PCH STRP TLSCONF	MAK_F_BASE=TRUE	NO_TEST=1	NC PCH STRP TLSCONF
60	TP PMIC PGC	MAK_F_BASE=TRUE	NO_TEST=1	NC PMIC PGC
17	TP SPI CS1 L	MAK_F_BASE=TRUE	NO_TEST=1	NC SPI CS1 L
17	TP SPI CS2 L	MAK_F_BASE=TRUE	NO_TEST=1	NC SPI CS2 L
17	TP SYSCLK CLK24M SSD	MAK_F_BASE=TRUE	NO_TEST=1	NC SYSCLK CLK24M SSD





17	TP USB3_03 D2RN	MAKFE_RASEaTRUE	NO_TESTa1	NC USB3_03 D2RN
18	TP USB3_03 D2RP	MAKFE_RASEaTRUE	NO_TESTa1	NC USB3_03 D2RP
19	TP USB3_03 R2DN	MAKFE_RASEaTRUE	NO_TESTa1	NC USB3_03 R2DN
20	TP USB3_03 R2DP	MAKFE_RASEaTRUE	NO_TESTa1	NC USB3_03 R2DP
21	TP USB3_04 D2RN	MAKFE_RASEaTRUE	NO_TESTa1	NC USB3_04 D2RN
22	TP USB3_04 D2RP	MAKFE_RASEaTRUE	NO_TESTa1	NC USB3_04 D2RP
23	TP USB3_04 R2DN	MAKFE_RASEaTRUE	NO_TESTa1	NC USB3_04 R2DN
24	TP USB3_04 R2DP	MAKFE_RASEaTRUE	NO_TESTa1	NC USB3_04 R2DP

16	IN	PCH SOC FORCE DFU	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH SOC FORCE DFU
17	OUT	PCH SOC WDOG	==	MAKE_BASE=TRUE	NO_TEST=1	NC PCH SOC WDOG
18	OUT	UPC I2C INT L	==	MAKE_BASE=TRUE	NO_TEST=1	NC UPC I2C INT L


```
30  IN TP UPC XB SWD DATA == MAKE_BASE=TRUE NO_TEST=1 NC UPC XB SWD DATA
```

29	TP UPC XA SWD DATA	==	MAKE_BASE=TRUE	NO_TEST=1	NC UPC XA SWD DATA
29	TP UPC XA SWD CLK	==	MAKE_BASE=TRUE	NO_TEST=1	NC UPC XA SWD CLK

15	TP PCIE CLK100M5P	MAKE_BASE=TRUE	NO_TEST=1	NC PCIE CLK100M5P
15	TP PCIE CLK100M5N	MAKE_BASE=TRUE	NO_TEST=1	NC PCIE CLK100M5N
15	TP PCH_CLKREQ5_L	MAKE_BASE=TRUE	NO_TEST=1	NC PCH_CLKREQ5_L
15	TP ITPXDP CLK100MP	MAKE_BASE=TRUE	NO_TEST=1	NC ITPXDP CLK100MP
15	TP ITPXDP CLK100MN	MAKE_BASE=TRUE	NO_TEST=1	NC ITPXDP CLK100MN
55	TP CPUVVR GH1	MAKE_BASE=TRUE	NO_TEST=1	NC CPUVVR GH1
6	TP CPU RSVD BB69	MAKE_BASE=TRUE	NO_TEST=1	NC CPU RSVD BB69
6	TP CPU RSVD BB68	MAKE_BASE=TRUE	NO_TEST=1	NC CPU RSVD BB68
6	TP CPU RSVD BA70	MAKE_BASE=TRUE	NO_TEST=1	NC CPU RSVD BA70
6	TP CPU RSVD BA68	MAKE_BASE=TRUE	NO_TEST=1	NC CPU RSVD BA68
6	TP CPU RSVD AW71	MAKE_BASE=TRUE	NO_TEST=1	NC CPU RSVD AW71
6	TP CPU RSVD AW70	MAKE_BASE=TRUE	NO_TEST=1	NC CPU RSVD AW70
6	TP CPU RSVD AK12	MAKE_BASE=TRUE	NO_TEST=1	NC CPU RSVD AK12
10	TP SPKR ID0	MAKE_BASE=TRUE	NO_TEST=1	NC SPKR ID0
60	TP PGOOD PVCCIO	MAKE_BASE=TRUE	NO_TEST=1	NC PGOOD PVCCIO
60	TP PGOOD P1V00	MAKE_BASE=TRUE	NO_TEST=1	NC PGOOD P1V00
19	TP PCH_CLK32K_RTCX2	MAKE_BASE=TRUE	NO_TEST=1	NC PCH_CLK32K_RTCX2
19	TP PCH_CLK24M_XTALOUT	MAKE_BASE=TRUE	NO_TEST=1	NC PCH_CLK24M_XTALOUT
19	TP XDP BPM L<3>	MAKE_BASE=TRUE	NO_TEST=1	NC XDP BPM L<3>
19	TP XDP BPM L<2>	MAKE_BASE=TRUE	NO_TEST=1	NC XDP BPM L<2>
19	TP XDP BPM L<1>	MAKE_BASE=TRUE	NO_TEST=1	NC XDP BPM L<1>

				MAKE_BASE					
65		=I2C BKLTL SCL	==	TRUE	I2C BKLTL SCL		66	72	
65		=I2C BKLTL SDA	==	TRUE	I2C BKLTL SDA		66	72	


8		7		6		5		4		3		2		1											
D	Memory Bit/Byte Swizzle														D										
	CPU							CPU																	
C	DRAM							DRAM							C										
	MAKE_BASE							MAKE_BASE																	
B	72	71	70	69	68	67	66	72	71	70	69	68	67	66	B										
	MEM A DQ<0>	MEM A DQ<1>	MEM A DQ<2>	MEM A DQ<3>	MEM A DQ<4>	MEM A DQ<5>	MEM A DQ<6>	MEM B DQ<0>	MEM B DQ<1>	MEM B DQ<2>	MEM B DQ<3>	MEM B DQ<4>	MEM B DQ<5>	MEM B DQ<6>											
A	MEM A DQ<7>	MEM A DQ<8>	MEM A DQ<9>	MEM A DQ<10>	MEM A DQ<11>	MEM A DQ<12>	MEM A DQ<13>	MEM B DQ<7>	MEM B DQ<8>	MEM B DQ<9>	MEM B DQ<10>	MEM B DQ<11>	MEM B DQ<12>	MEM B DQ<13>	A										
	MEM A DQ<14>	MEM A DQ<15>	MEM A DQ<16>	MEM A DQ<17>	MEM A DQ<18>	MEM A DQ<19>	MEM A DQ<20>	MEM B DQ<14>	MEM B DQ<15>	MEM B DQ<16>	MEM B DQ<17>	MEM B DQ<18>	MEM B DQ<19>	MEM B DQ<20>											
BOM_COST_GROUP=NO COST ITEMS																									

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