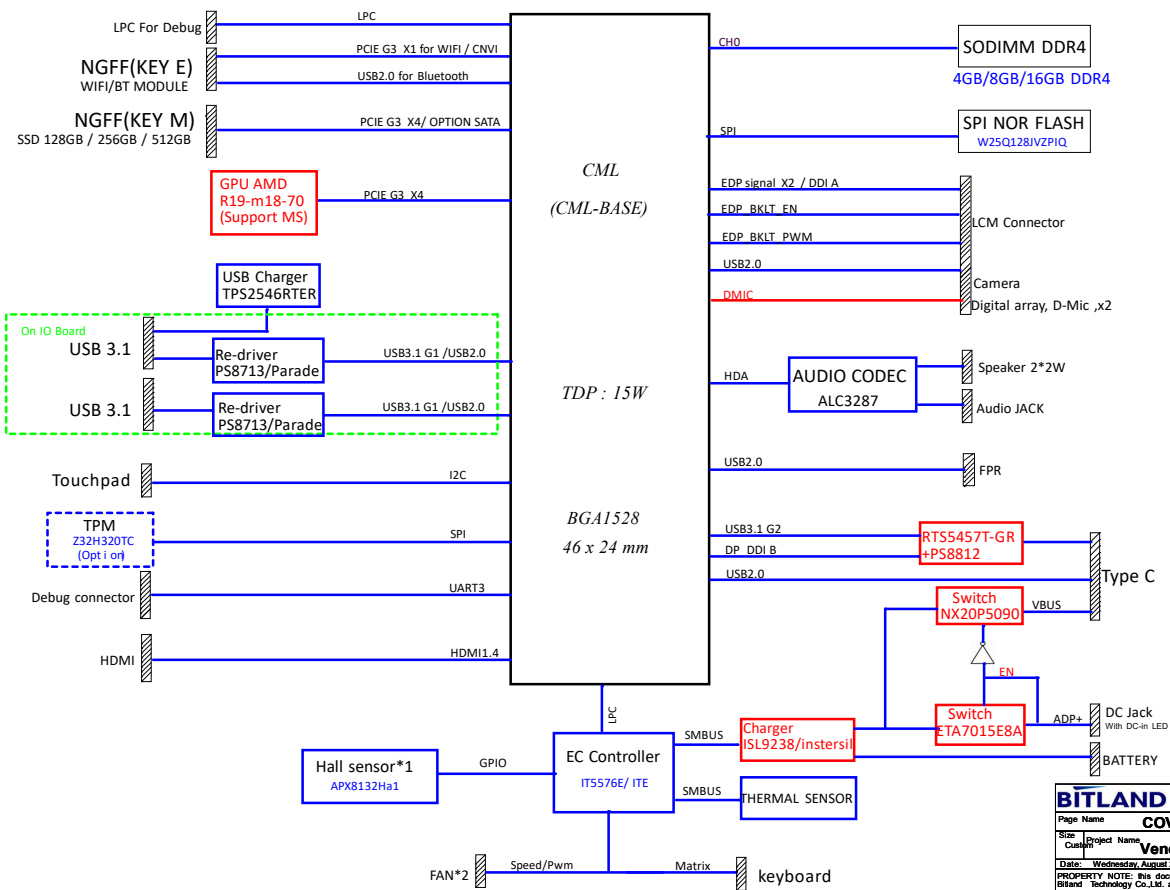


Veneno for Lenovo



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24--SYSTEM FLASH	54 -- NA	84--IO Board_USB3.0 Redriver
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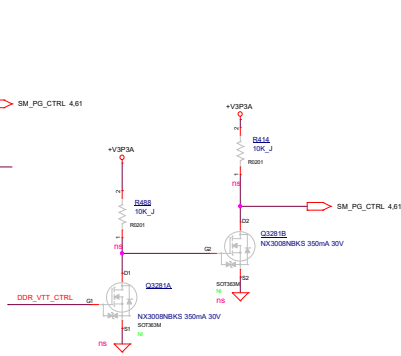
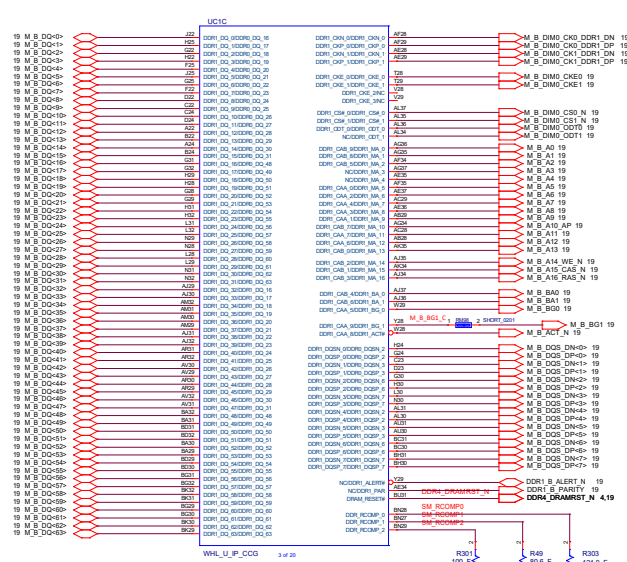
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Rev: 2.000
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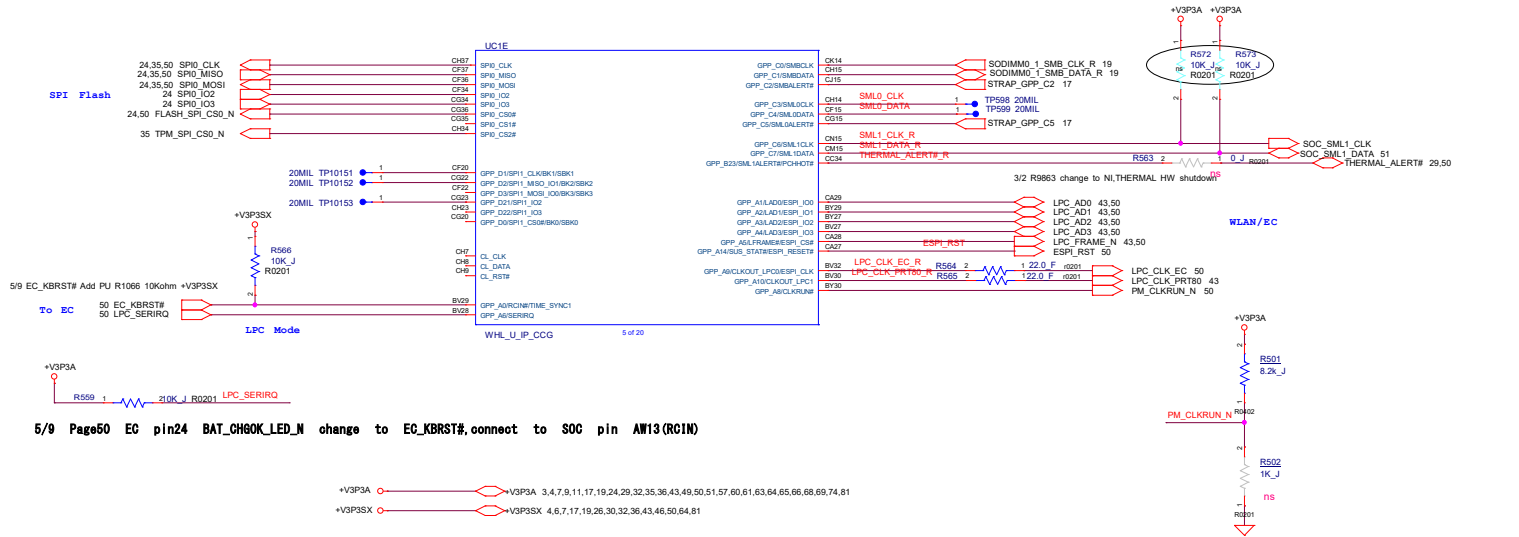
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SPI0_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SMLALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC is selected for EC. (Default) 1 = eSPI is selected for EC. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SMLALERT# / PCHHOT# / GPP_B23	Reserved	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

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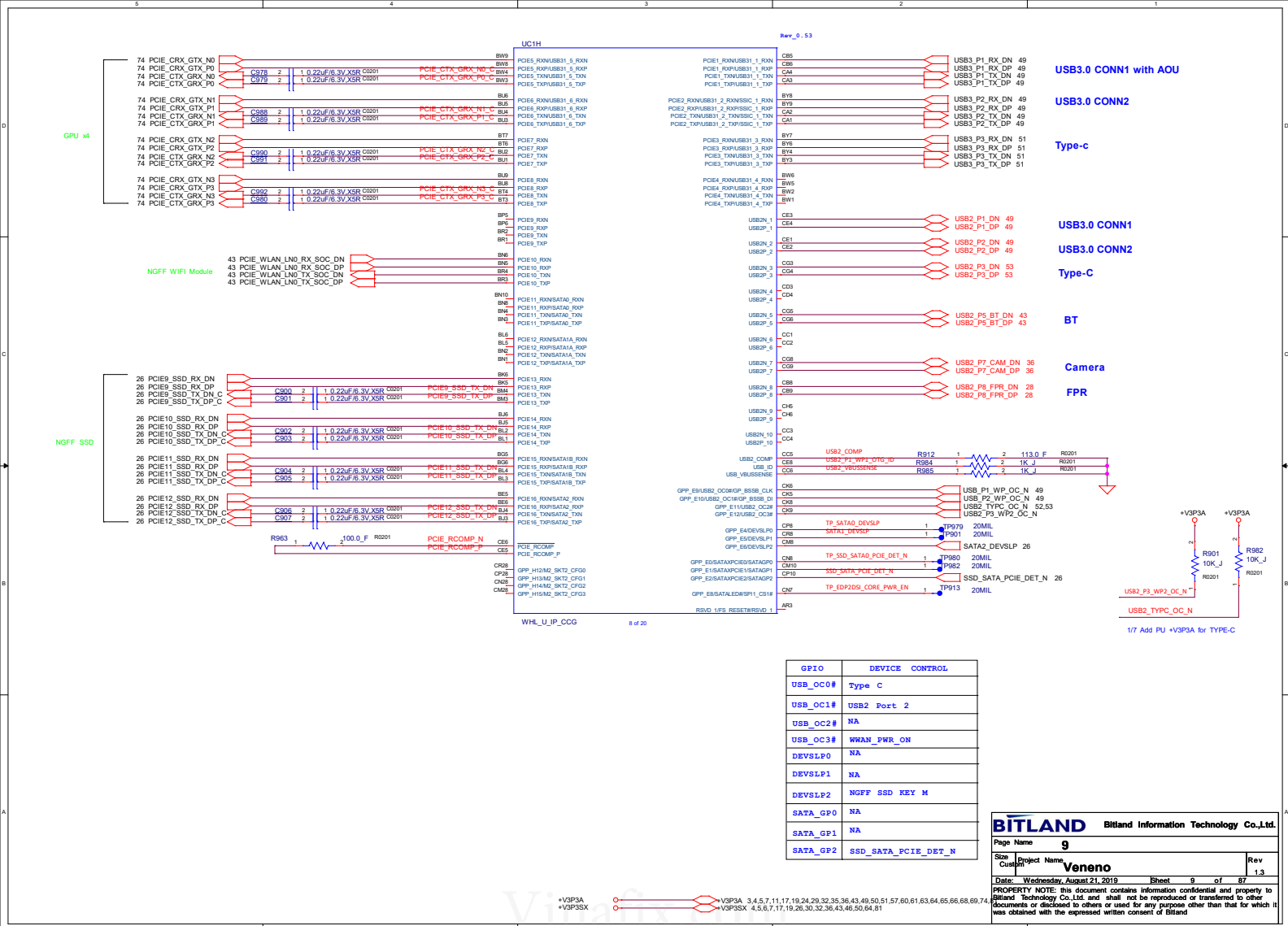
Rev
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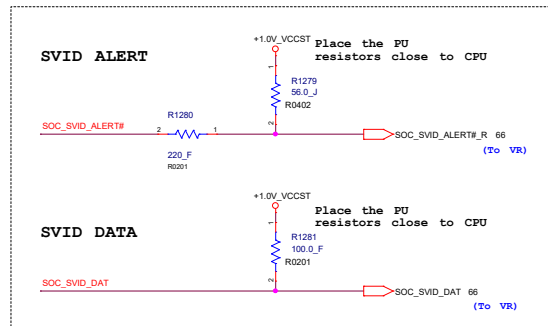
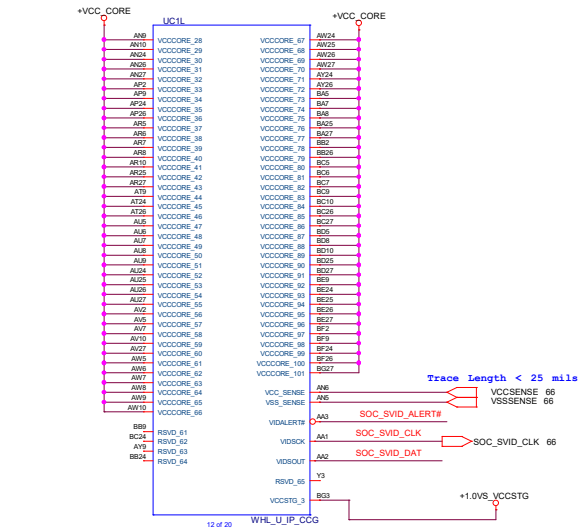
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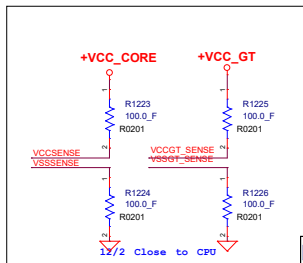
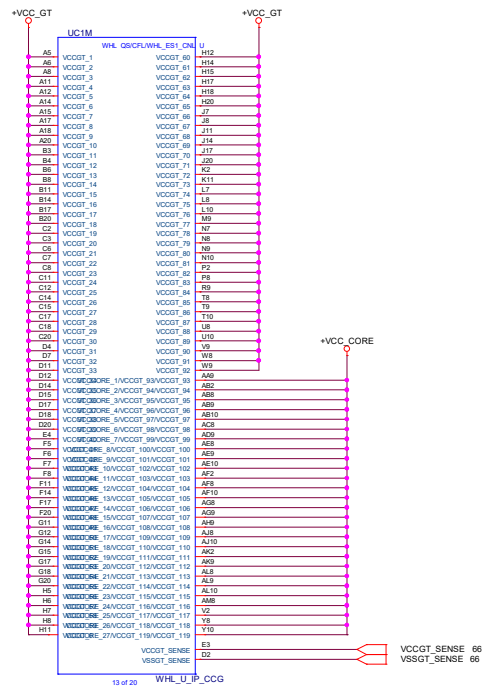
SIZE	2GB	4GB	8GB	16GB
MEM_DEC0	0	1	0	1
MEM_DEC1	0	0	1	1

Vender	Samsung	Hynix	Micron	
MEM_DEC2	0	1	0	
MEM_DEC3	0	0	1	





+VCC_CORE 15.66,67
+1.0V_VCCSTG 3.7,10,17,64,66
+VCC_GT 15.66,67
+1.0V_VCCST 3.7,10,17,64,66



Package Sensing Recommendations

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
VccGT_SENSE / VssGT_SENSE			
VccGA_SENSE / VssGA_SENSE			
VccGD_SENSE / VssGD_SENSE ^[1]			
		NA	

Note: [1] Does not apply when rails are merged.

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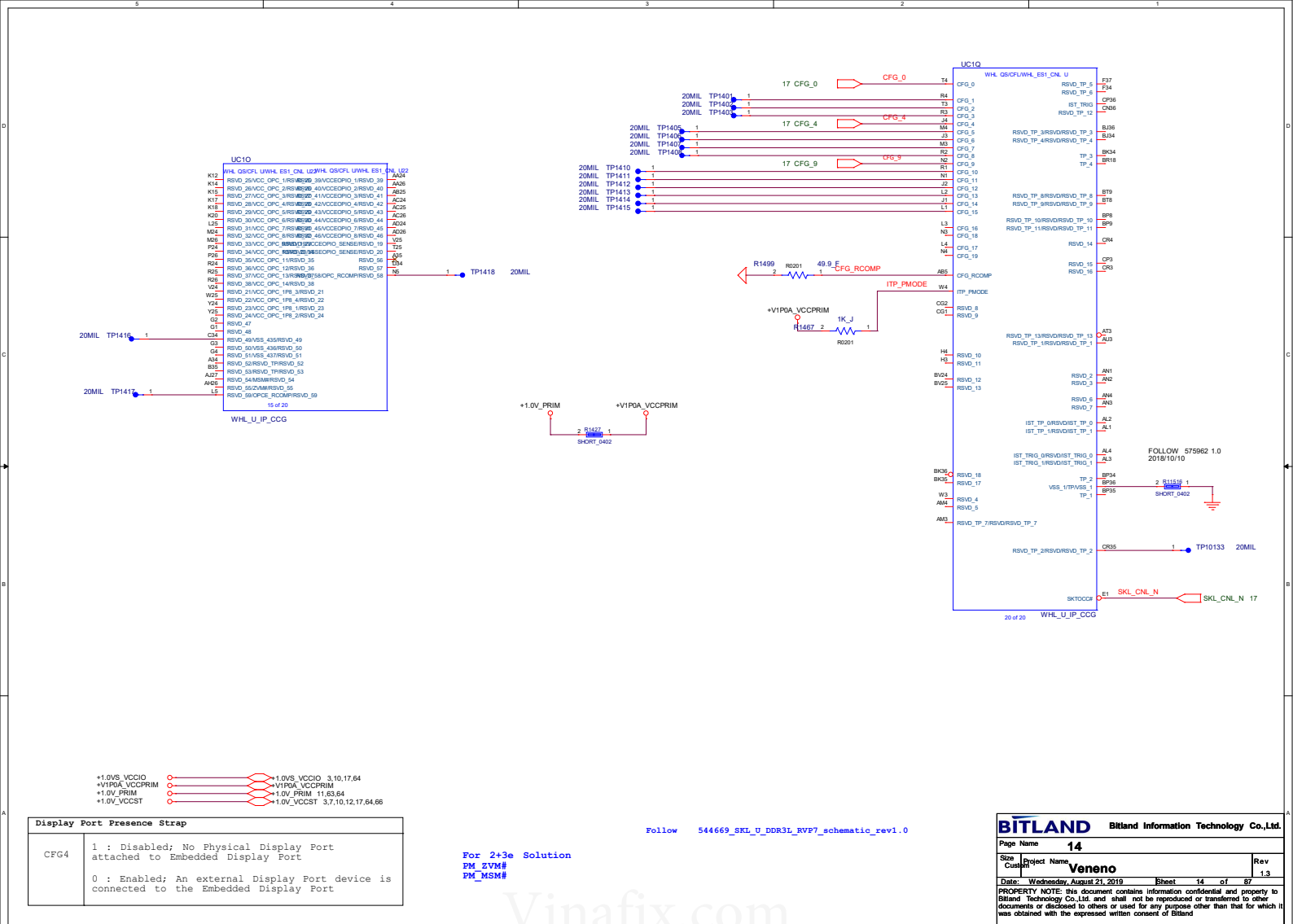
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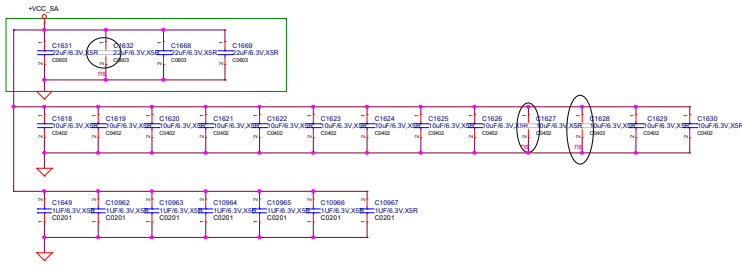
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UC1R		
CR34	VSS_342	VSS_330
B7E	VSS_351	VSS_337
B7E	VSS_351	VSS_346
CP35	VSS_371	VSS_354
CM37	VSS_381	VSS_364
CM37	VSS_381	VSS_374
AW1	VSS_401	VSS_385
CM1	VSS_411	VSS_394
BD5	VSS_421	VSS_395
BD5	VSS_380	VSS_315
BD5	VSS_370	VSS_305
AA	VSS_380	VSS_309
AA	VSS_380	VSS_301
AE24	VSS_400	VSS_344
AE24	VSS_410	VSS_353
AE24	VSS_420	VSS_363
AE24	VSS_428	VSS_373
AE24	VSS_434	VSS_383
AE24	VSS_438	VSS_387
AE24	VSS_440	VSS_391
AE24	VSS_444	VSS_395
AE24	VSS_448	VSS_399
AE24	VSS_452	VSS_403
AE24	VSS_456	VSS_407
AE24	VSS_460	VSS_411
AE24	VSS_464	VSS_415
AE24	VSS_468	VSS_419
AE24	VSS_472	VSS_423
AE24	VSS_476	VSS_427
AE24	VSS_480	VSS_431
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AE24	VSS_508	VSS_459
AE24	VSS_512	VSS_463
AE24	VSS_516	VSS_467
AE24	VSS_520	VSS_471
AE24	VSS_524	VSS_475
AE24	VSS_528	VSS_479
AE24	VSS_532	VSS_483
AE24	VSS_536	VSS_487
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AE24	VSS_796	VSS_747
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AE24	VSS_984	VSS_935
AE24	VSS_988	VSS_939
AE24	VSS_992	VSS_943
AE24	VSS_996	VSS_947
AE24	VSS_1000	VSS_951

UC1S			BY2S		
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BT35	VSS_283	VSS_186	BT35	VSS_189	BY2S
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BT35	VSS_589	VSS_492	BT35	VSS_495	BY2S
BT35	VSS_592	VSS_495	BT35	VSS_498	BY2S
BT35	VSS_595	VSS_498	BT35	VSS_501	BY2S
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BT35	VSS_604	VSS_507	BT35	VSS_510	BY2S
BT35	VSS_607	VSS_510	BT35	VSS_513	BY2S
BT35	VSS_610	VSS_513	BT35	VSS_516	BY2S
BT35	VSS_613	VSS_516	BT35	VSS_519	BY2S
BT35	VSS_616	VSS_519	BT35	VSS_522	BY2S
BT35	VSS_619	VSS_522	BT35	VSS_525	BY2S
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BT35	VSS_625	VSS_528	BT35	VSS_531	BY2S
BT35	VSS_628	VSS_531	BT35	VSS_534	BY2S
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BT35	VSS_643	VSS_546	BT35	VSS_549	BY2S
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BT35	VSS_889	VSS_792	BT35	VSS_795	BY2S
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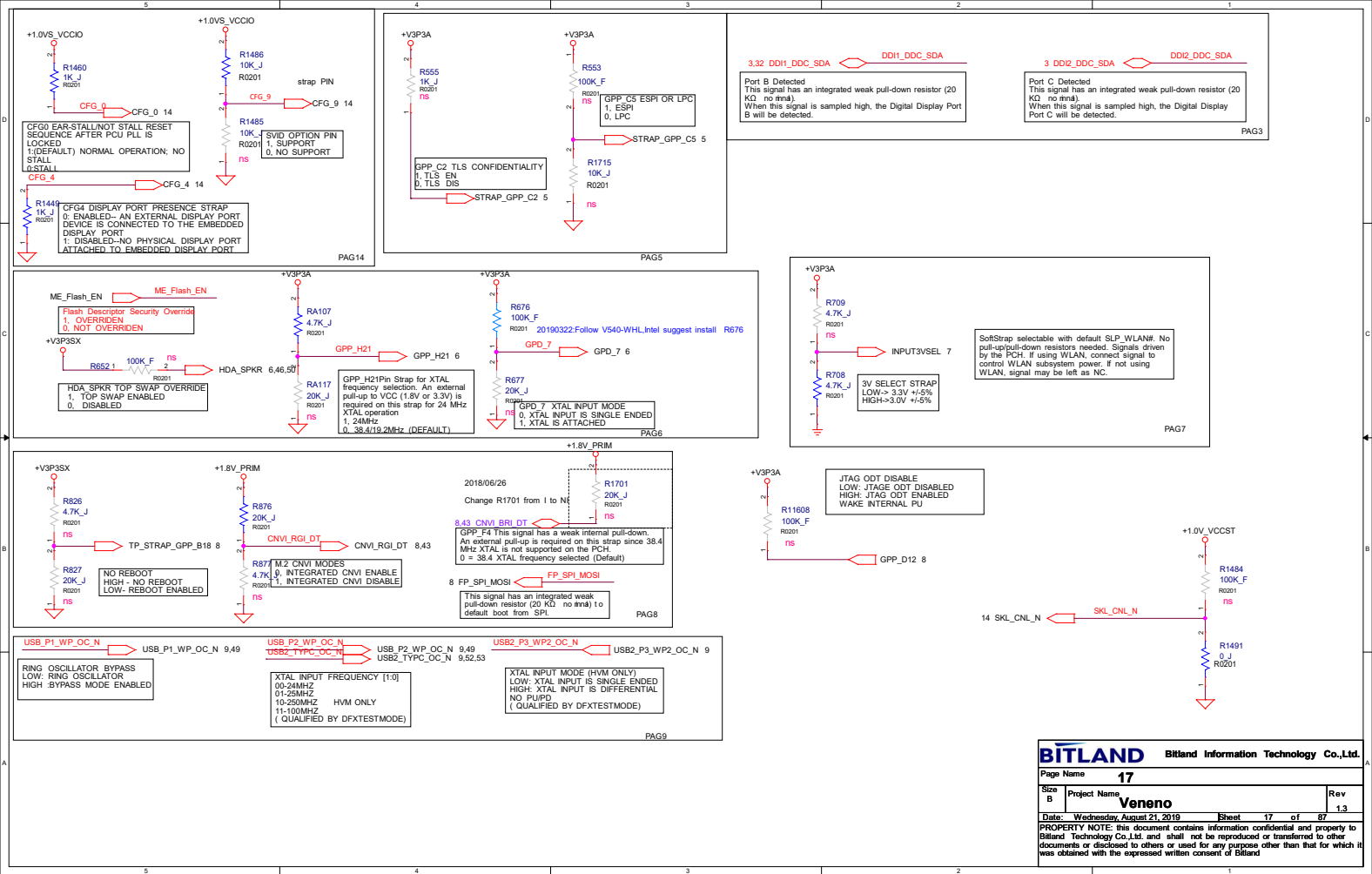
+VCC_SA
47uF x2
10uF x13
1uF x7

12/30 check PD8

+VCC_CORE
+VCC_GT
+VCC_SA

BITLAND		Bitland Information Technology Co., Ltd.	
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Date	Wednesday, August 24, 2016	Page	16 of 87
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Rev 1.3	
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BITLAND Bitland Information Technology Co.,Ltd.	
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BPAGE DRAWING

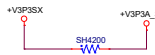
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Wed Jun 03 11:22:52 2015

BITLAND		Bitland Information Technology Co., Ltd.	
Page Name		25	
Size	Project Name	Rev	
Custom	Veneno	1.3	
Date:	Wednesday, August 21, 2019	Sheet	25 of 87

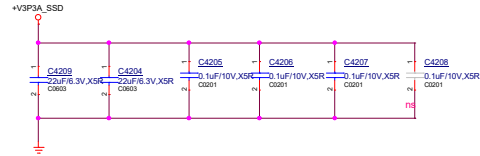
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M.2 SSD Module

1. 4A @ADATA 128GB SSD
2. 6A @ADATA 256GB SSD



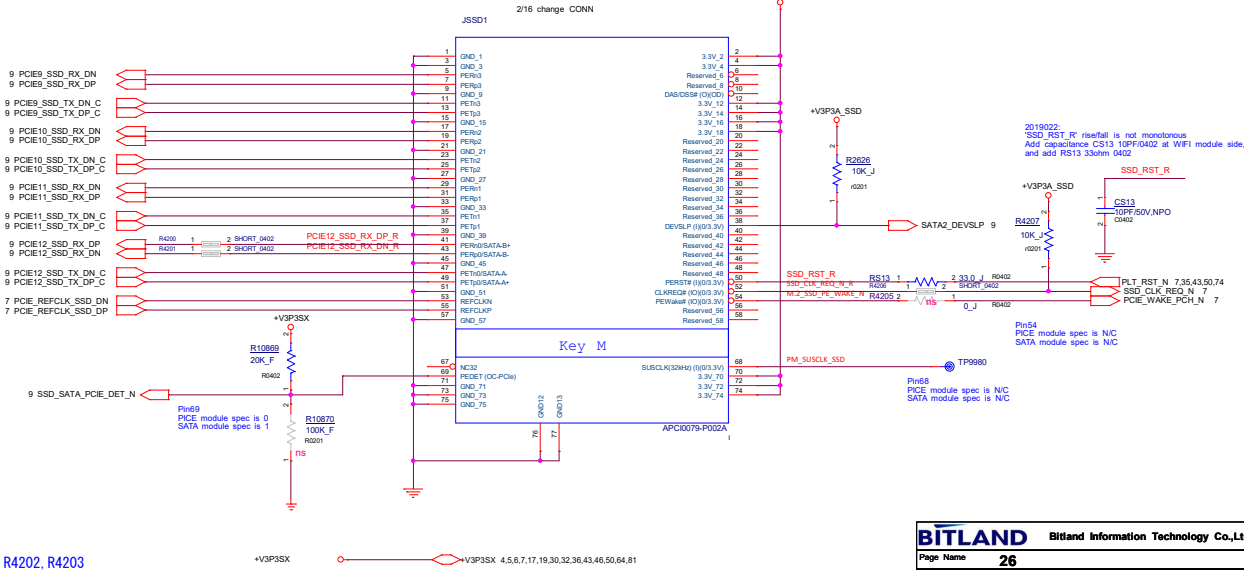
Change SH4200 0805 shunt to resistor



CIS ok

PCIE12 RX
follow intel
CRB

Difference with annou
SSD interface SATA change to PCIE
if install SATA CARD R4200,R4201 need install 0.01uF
C0606,C0607 need install 0.01uF



Co-lay PCIE12 RX reserved R4202,R4203
please close to R4200,R4201

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BPAGE DRAWING

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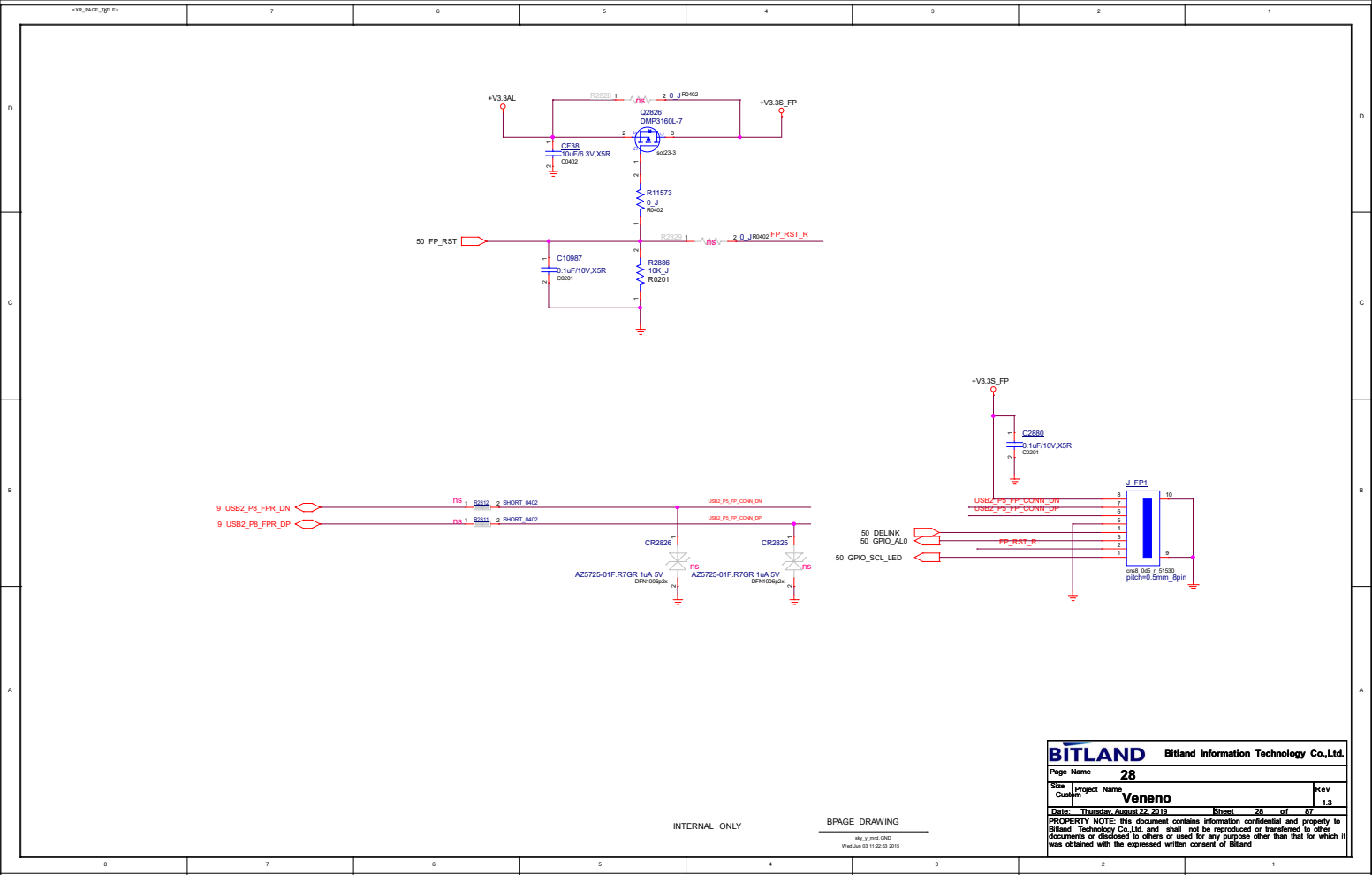
8

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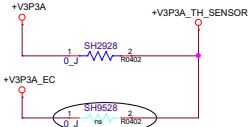
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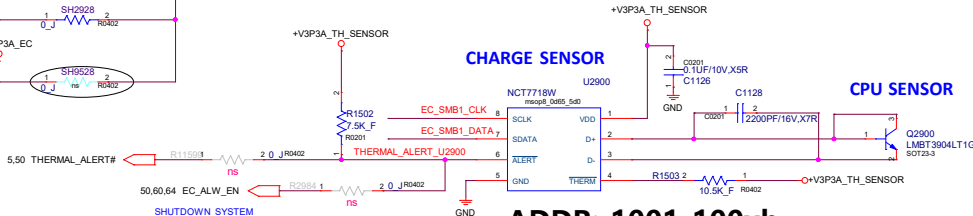
Thermal Sensor



EC

50.52.76 EC_SMB1_CLK
50.52.76 EC_SMB1_DATA

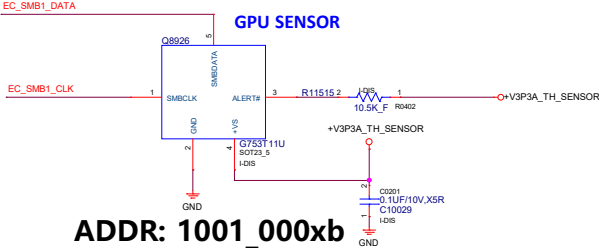
CHARGE SENSOR



CPU SENSOR

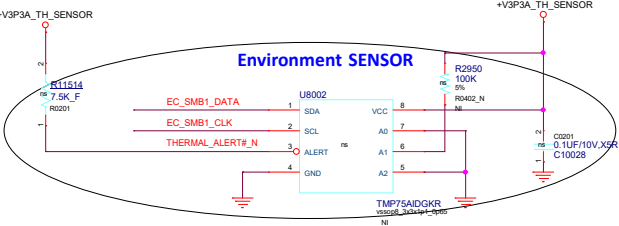
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GPU SENSOR



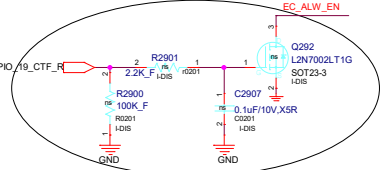
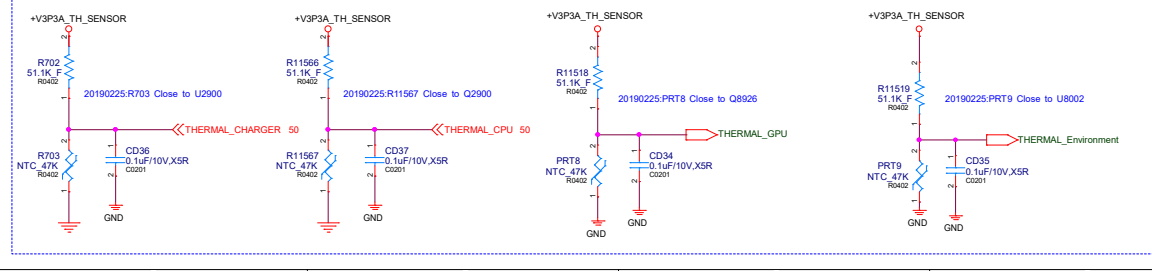
ADDR: 1001_000xb

Environment SENSOR



ADDR: 1001_010xb

20190507: install all NTC for FVT debug

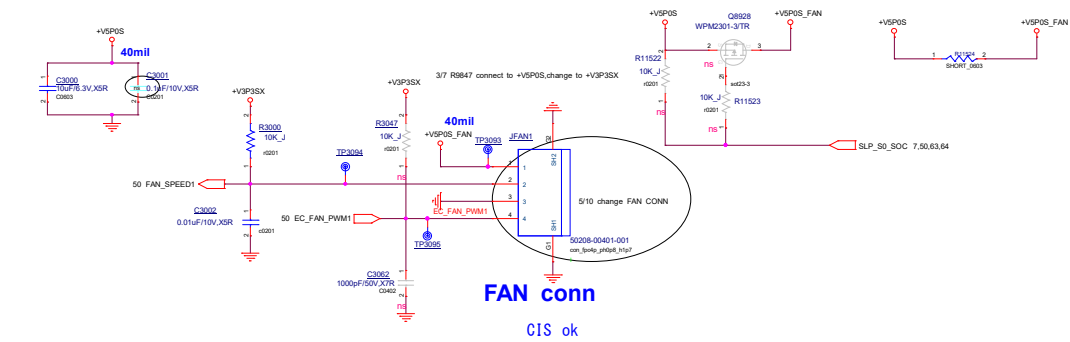


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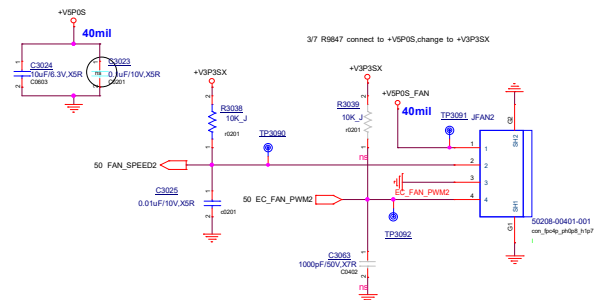
Page Name	29	
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+VSP0S 32.46.64
+VSP3SX 4.5,6.7,17,19,26,32,36,43,46,50,64,81



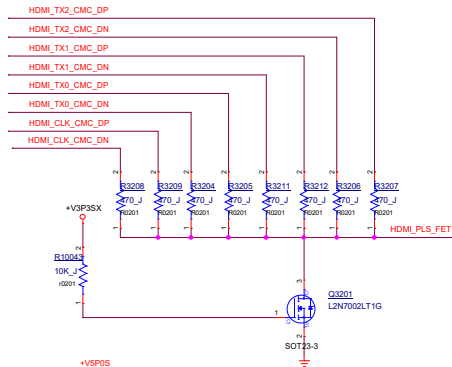
BITLAND Bitland Information Technology Co., Ltd.			
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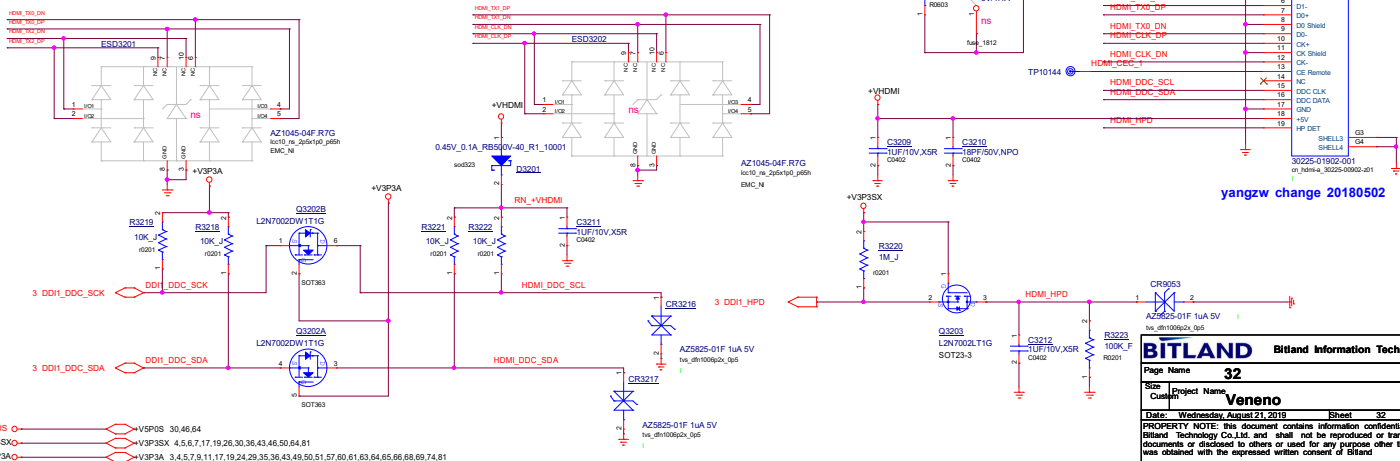
BITLAND Bitland Information Technology Co.,Ltd.		
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for EMI Co-lay



FUSE need to be 1.1A



yangzw change 20180502

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BPAGE DRAWING

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Wed Jun 03 11:22:55 2015

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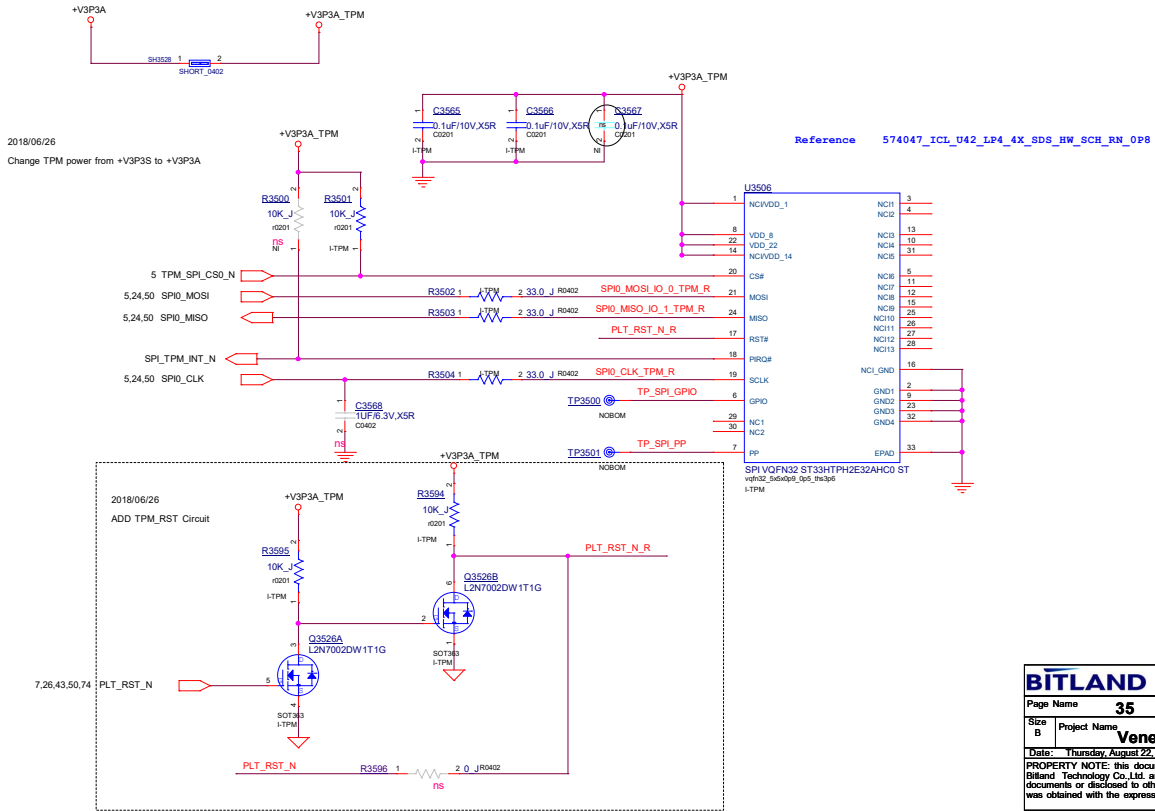
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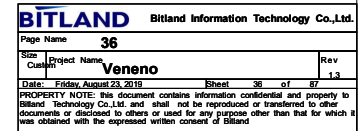
TPM 2.0



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Date: Thursday, August 22, 2019		Sheet	35 of 37

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13" GNI
14" NC

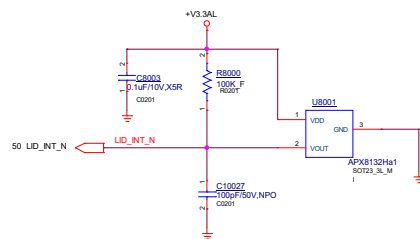


USB2.0

BITLAND		Bitland Information Technology Co.,Ltd.	
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LID Sensor

Working voltage 2.4/ 2.7/ 5.5
max current 2.5mA typ:3uA



+V3.3AL 11,28,49,50,58,60

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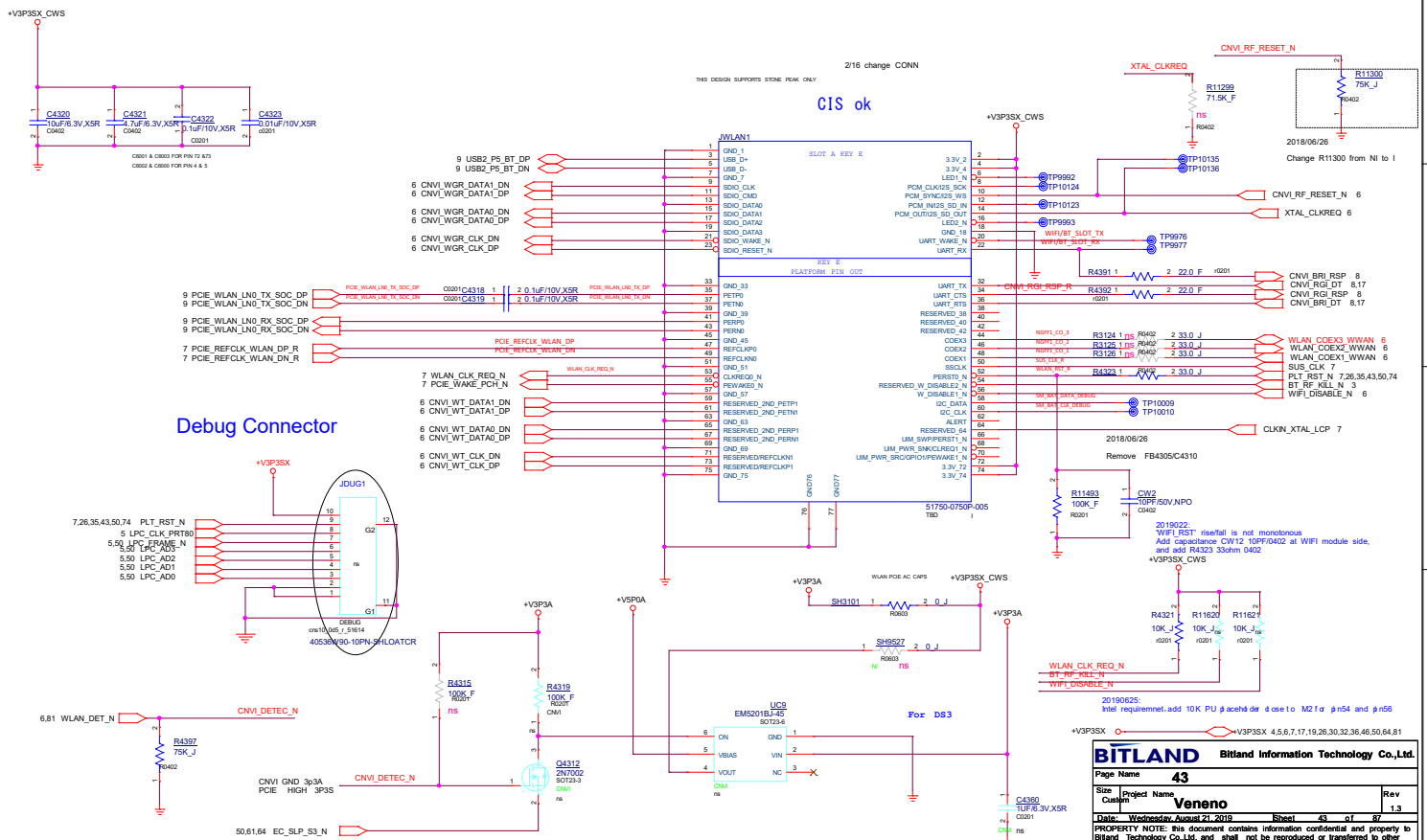
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WIFI & BT Module



		7		6		5		4		3		2		1			
D														D			
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BITLAND

Bitland Information Technology Co.,Ltd.

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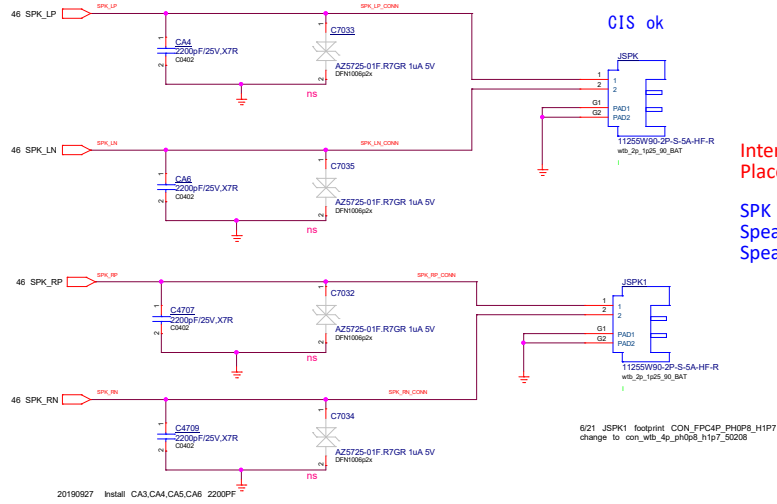
INTERNAL ONLY

BPAGE DRAWING

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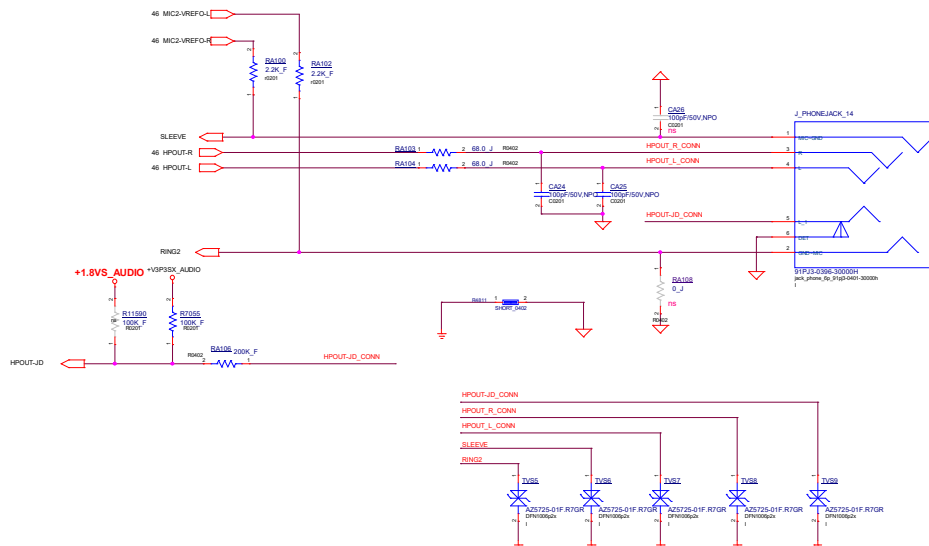
Vinafix.com

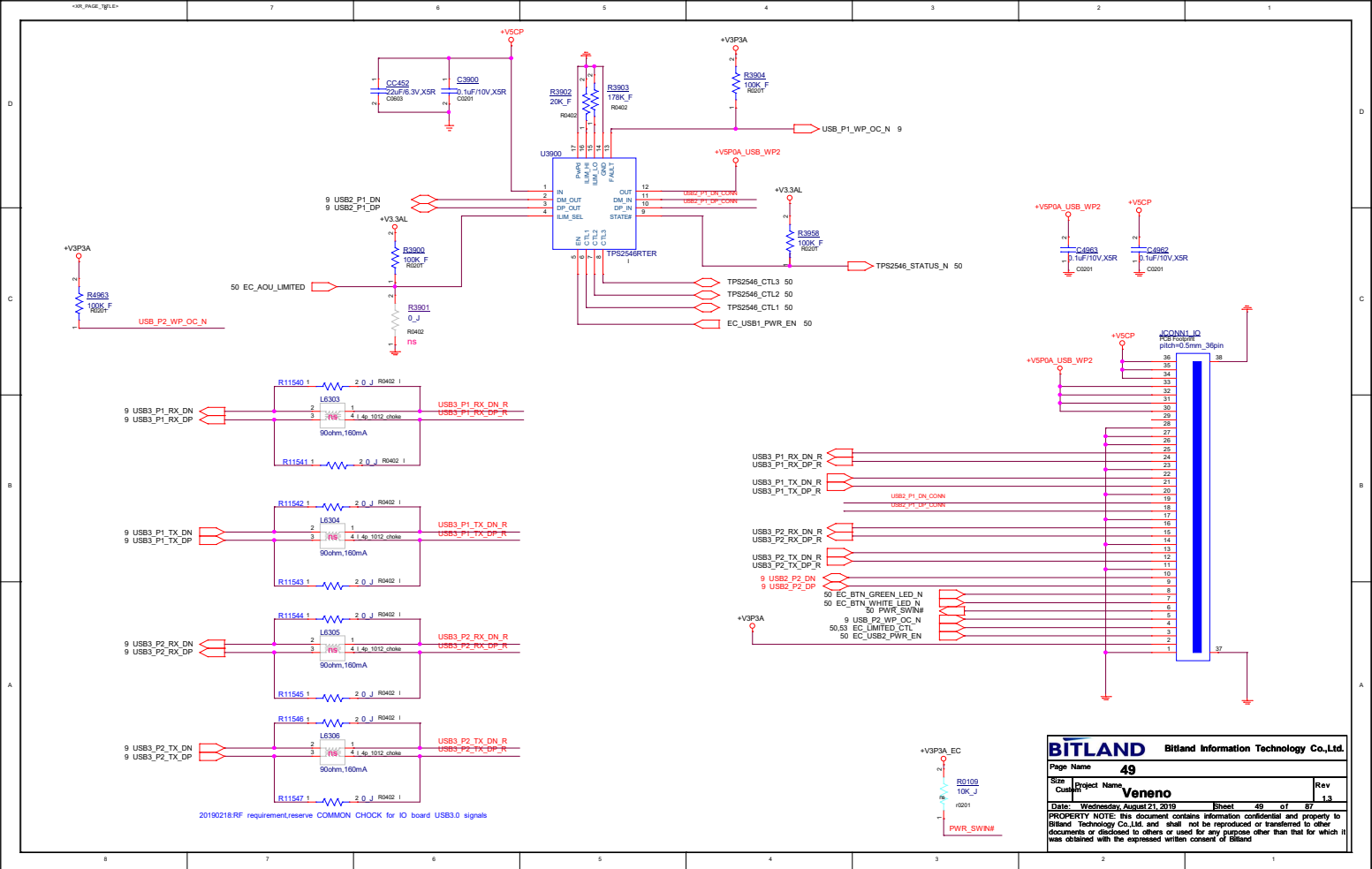
Speaker



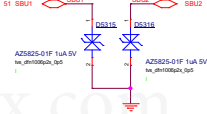
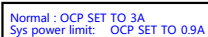
BITLAND Bitland Information Technology Co.,Ltd			
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Important:
To ensure reliable headset detection for all fast/slow plug-in scenarios use a jack with the detect switch all the way at the end so that the switch is tripped only when the jack is plugged all the way in.





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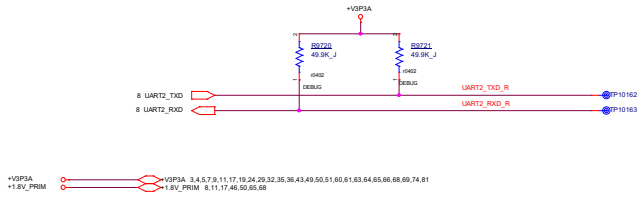
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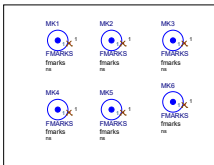
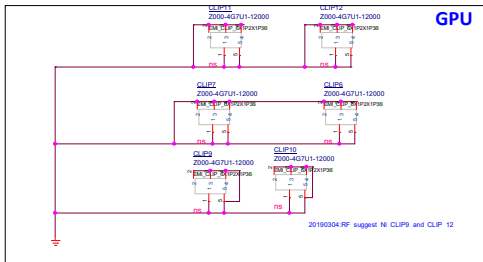
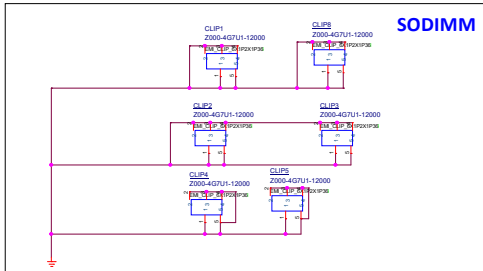
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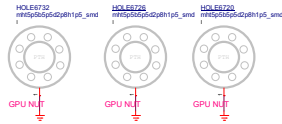


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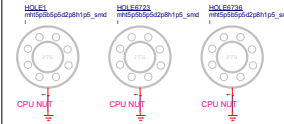


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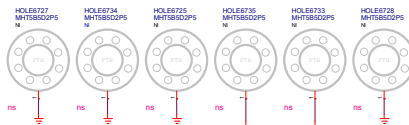
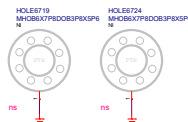
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CPU NUT

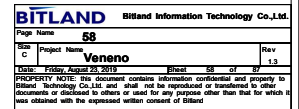


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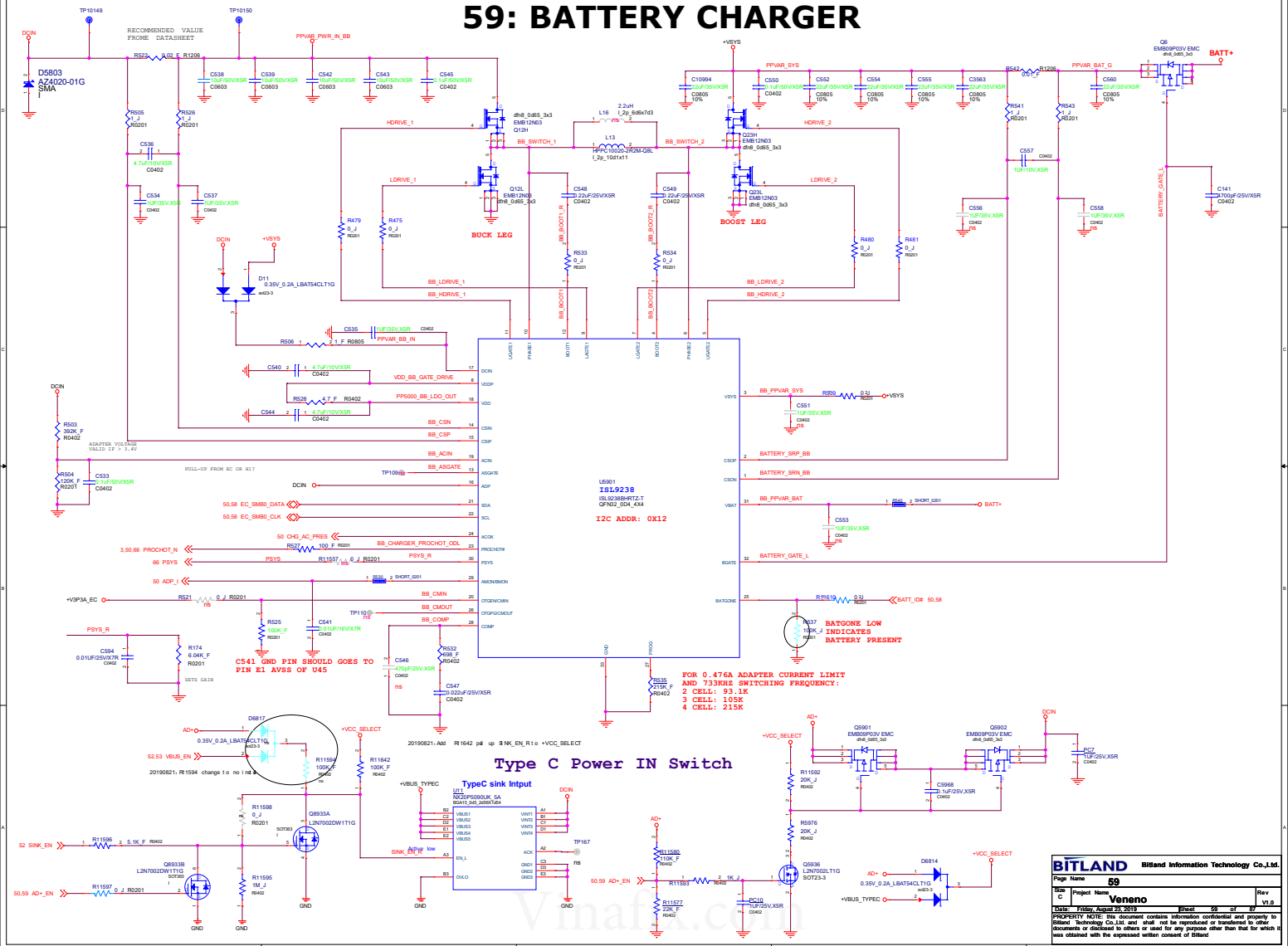


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BATT+ ○ ———— ◇ BATT+ 59
+V3.3AL ○ ———— ◇ +V3.3AL 11,28,38,49,50,60
DCIN ○ ———— ◇ DCIN 59



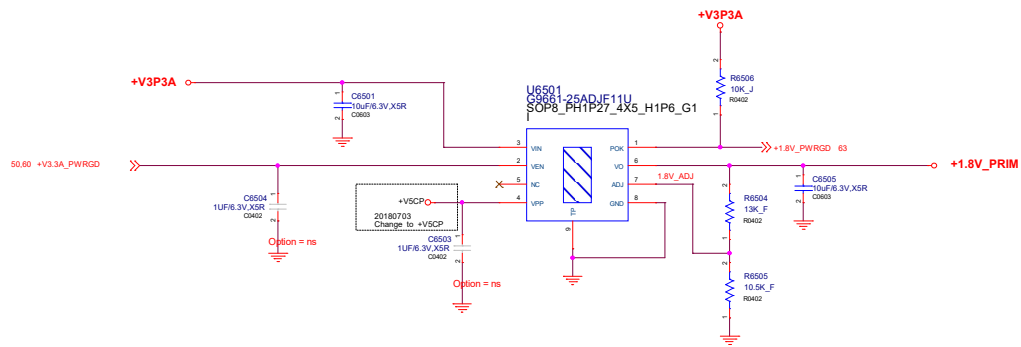
59: BATTERY CHARGER





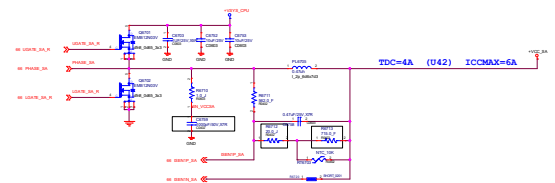
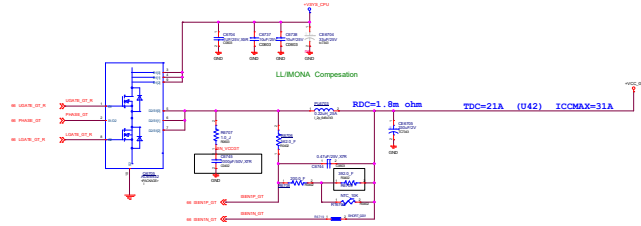
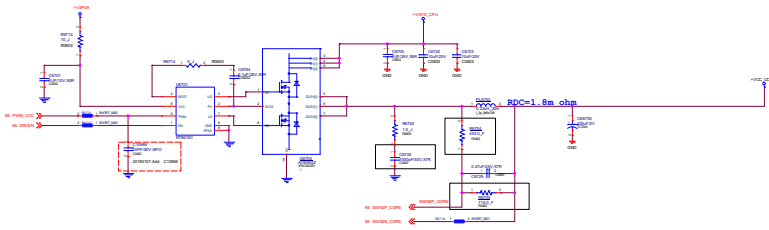
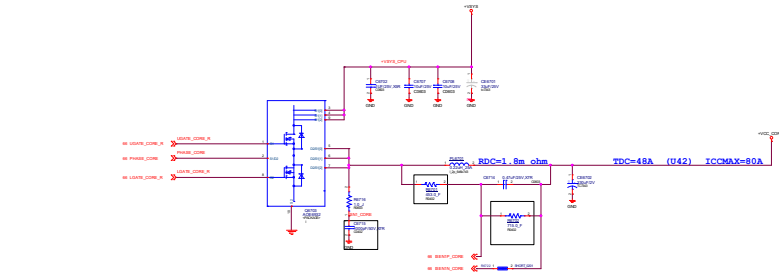


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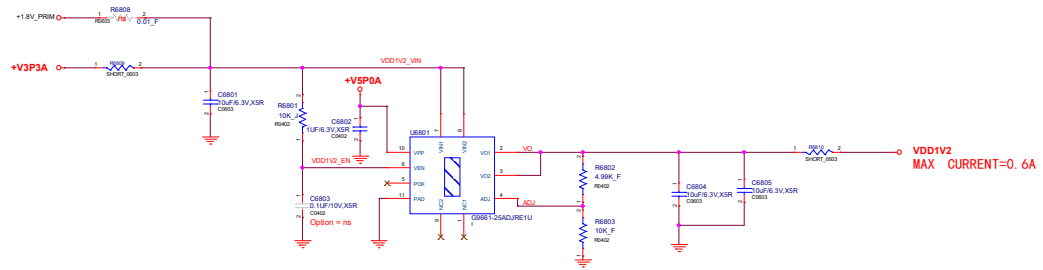
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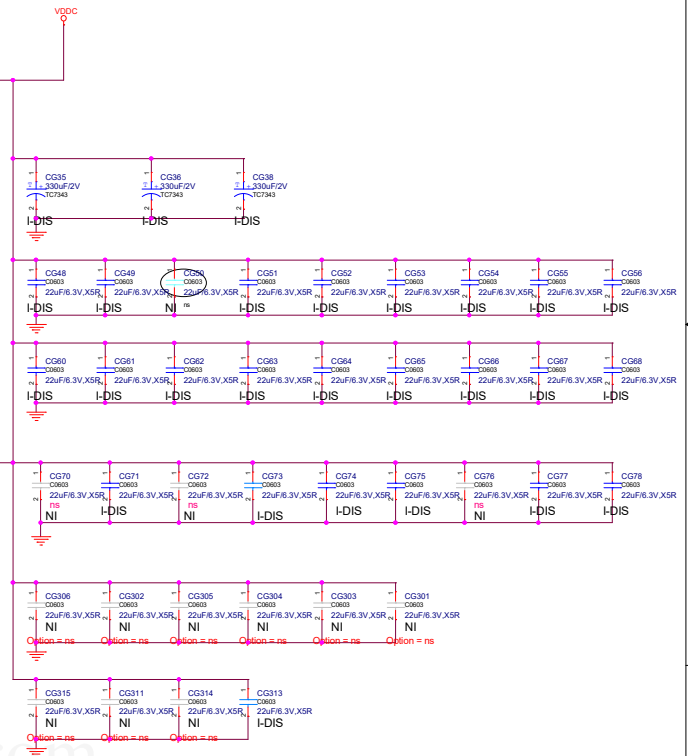
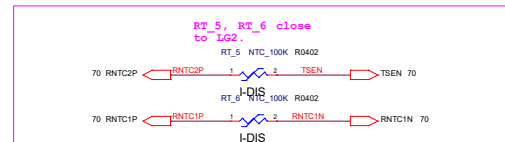
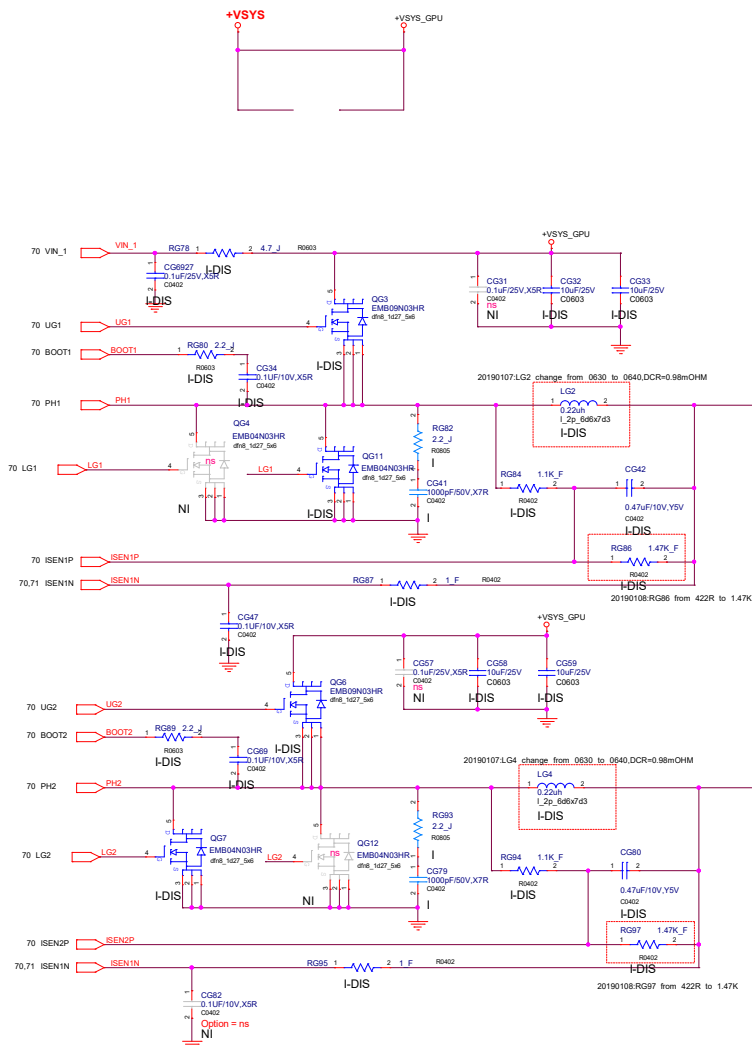
70: GPU POWER

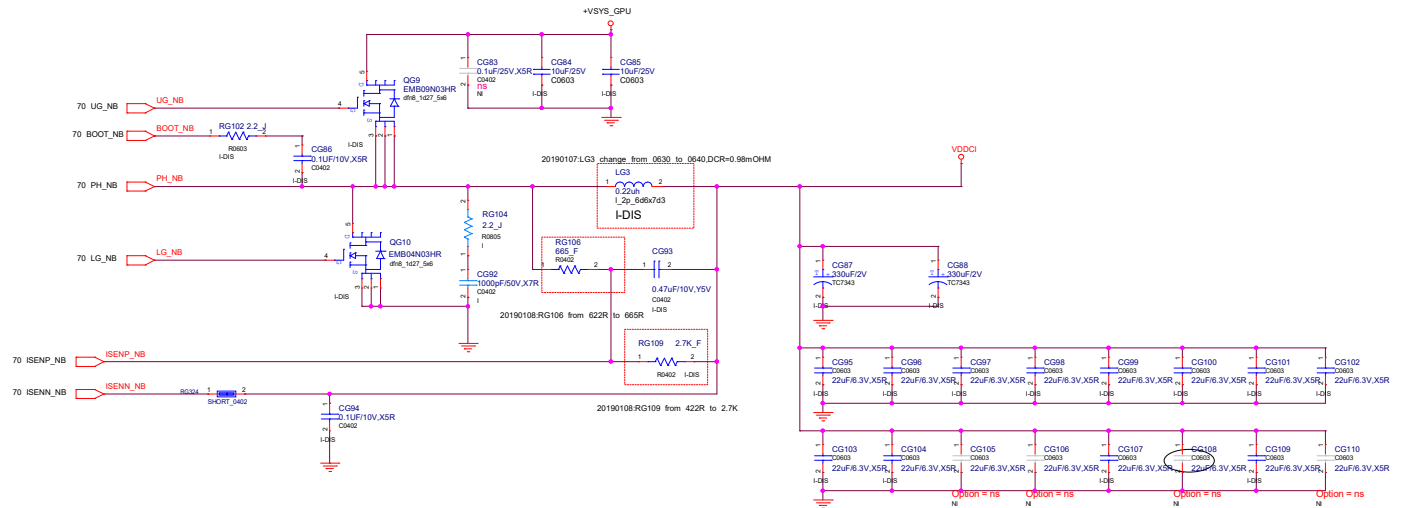
The schematic diagram illustrates the GPU power section for the RT3662AC. It features several power rails and decoupling components:

- +VSP0A:** A power rail connected to the VCC pin (pin 27) of the RT3662AC. It includes a 4.7k resistor (RG14) and a 4.7k capacitor (CG11).
- +VDD33:** A power rail connected to the VDD pin (pin 28) of the RT3662AC. It includes a 10k resistor (RG29) and a 10k capacitor (CG13).
- 1V8_AON:** A power rail connected to the VDDIO pin (pin 22) of the RT3662AC. It includes a 4.7k resistor (RG35) and a 10k capacitor (CG15).
- 74 GPU_PWROK:** A signal pin (pin 18) connected to the PWROK pin of the RT3662AC.
- 76 SVC, 76 SVD, 76 SVT:** Signal pins (pins 19, 20, 21) connected to the SVC, SVD, and SVT pins of the RT3662AC.
- 74 NVDD_PG00D:** A signal pin (pin 3) connected to the PG00D pin of the RT3662AC.
- 76 GPUVR_HOT:** A signal pin (pin 11) connected to the VROT_L pin of the RT3662AC.
- 72 RNTC1N_NB, 72 RNTC1P_NB:** Signal pins (pins 71, 72) connected to the RNTC1N and RNTC1P pins of the RT3662AC.
- 79 FB_VDDCI:** A power rail connected to the FB_VDDCI pin (pin 29) of the RT3662AC. It includes a 10k resistor (RG73) and a 10k capacitor (CG26).
- 79 FB_VSSC:** A power rail connected to the FB_VSSC pin (pin 30) of the RT3662AC. It includes a 10k resistor (RG74) and a 10k capacitor (CG27).

The RT3662AC is a 28-pin device with the following pins:

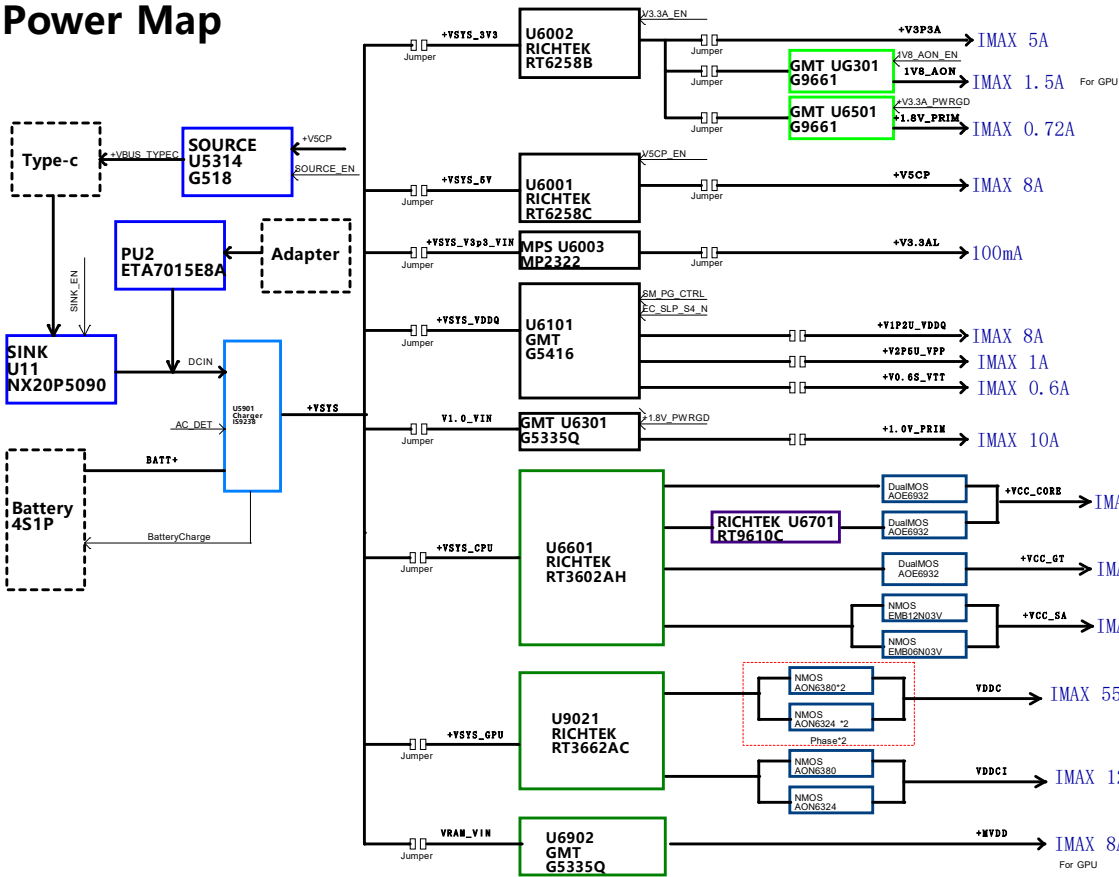
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- 28: VDD
- 29: FB_VDDCI
- 30: FB_VSSC
- 31: UG_NB
- 32: PH_NB
- 33: LG_NB
- 34: P_VCC
- 35: LG1
- 36: PH1
- 37: UG1
- 38: BOOT1
- 39: LG2
- 40: PH2
- 41: GND
- 42: VDDIO
- 43: IMON_NB
- 44: IMON
- 45: VREF_PINSET
- 46: VREF
- 47: VSEN
- 48: ISEN2P
- 49: ISEN2N
- 50: BOOT2
- 51: UG2
- 52: PH2
- 53: LG2
- 54: VSEN
- 55: ISEN2P
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- 57: BOOT2
- 58: UG2
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- 60: LG2
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- 62: ISEN2P
- 63: ISEN2N
- 64: BOOT2
- 65: UG2
- 66: PH2
- 67: LG2
- 68: VSEN
- 69: ISEN2P
- 70: ISEN2N
- 71: BOOT2
- 72: UG2
- 73: PH2
- 74: LG2
- 75: VSEN
- 76: ISEN2P
- 77: ISEN2N
- 78: BOOT2
- 79: UG2
- 80: PH2
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- 82: VSEN
- 83: ISEN2P
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- 324: UG2
- 32





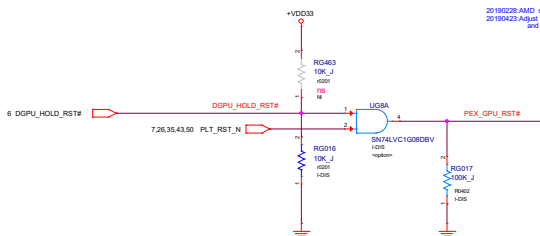
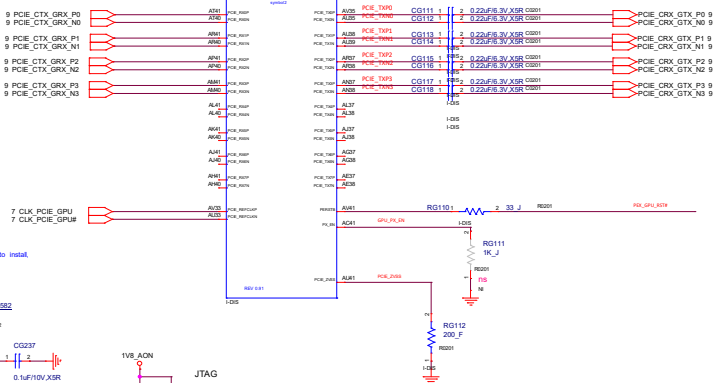
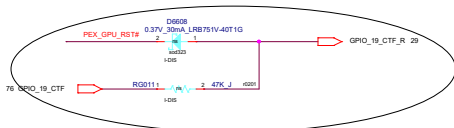
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Power Map

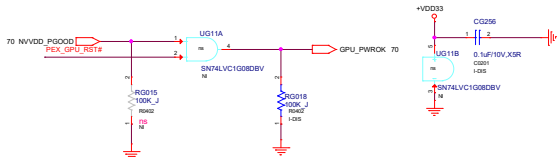
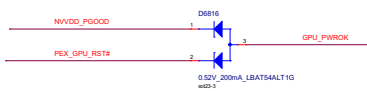
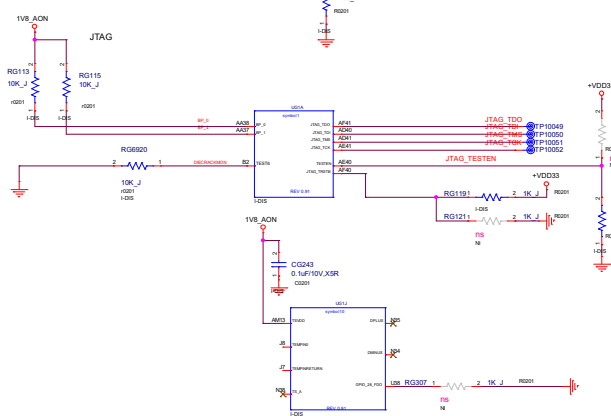
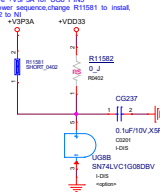


- Converter
- Controller
- MOS
- Driver
- LDO
- SWITCH

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20190228 AMD suggest Reserve +V/PSA for USB PINS
20190423 Adjust DGPU MS power sequence, change R11551 to install, and change R11552 to N1

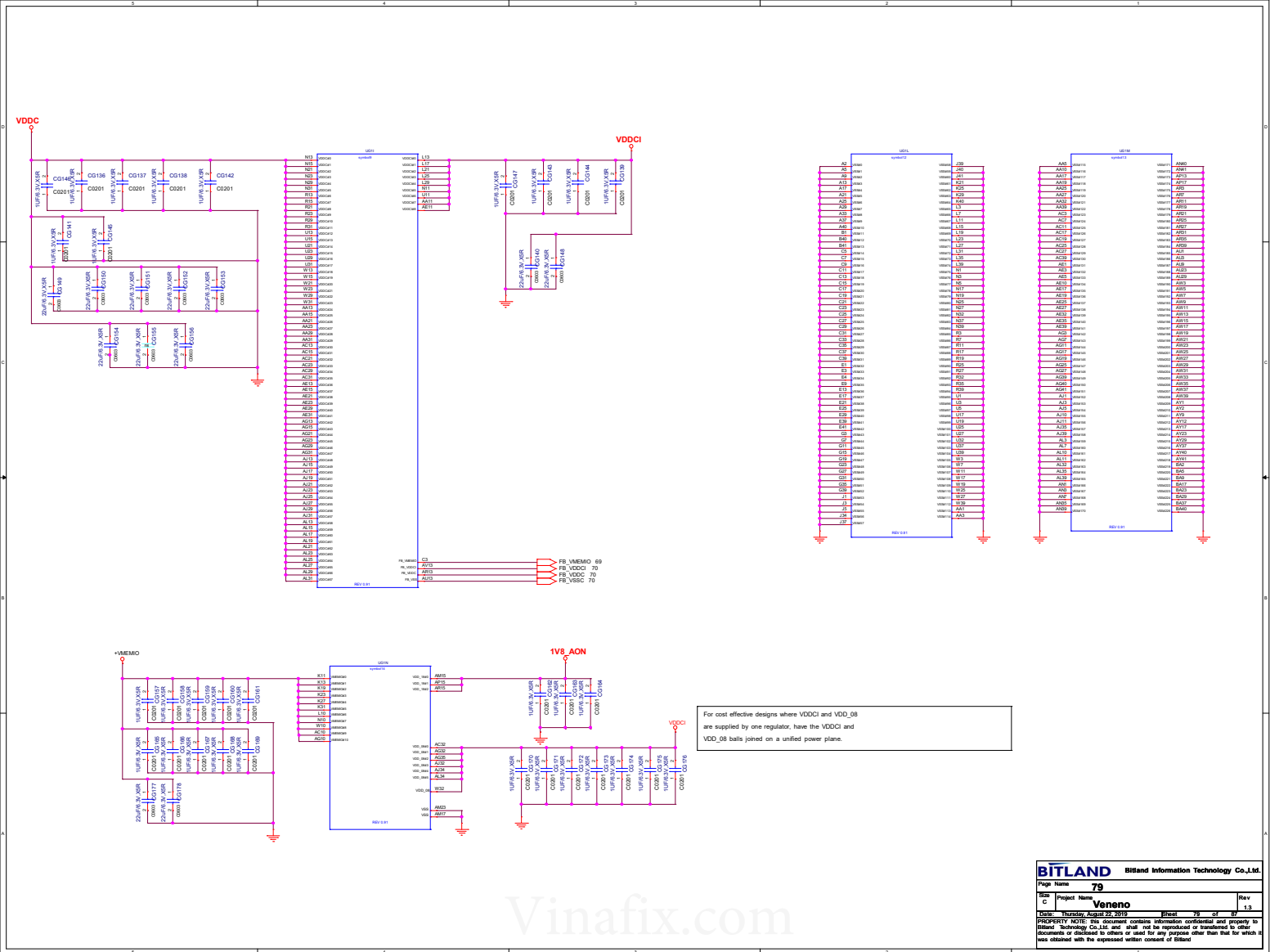


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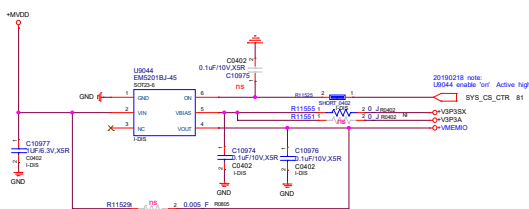
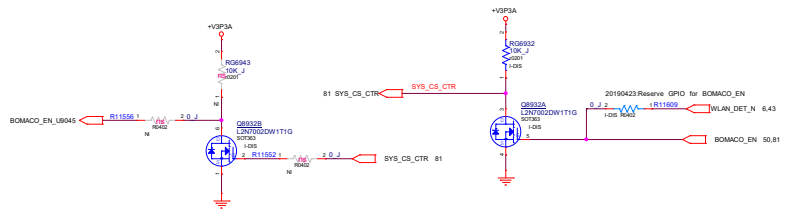
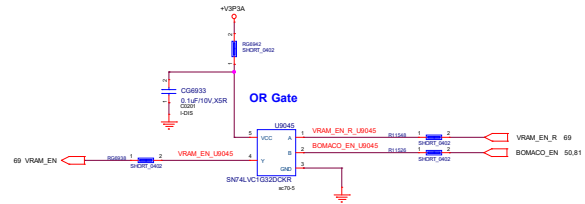
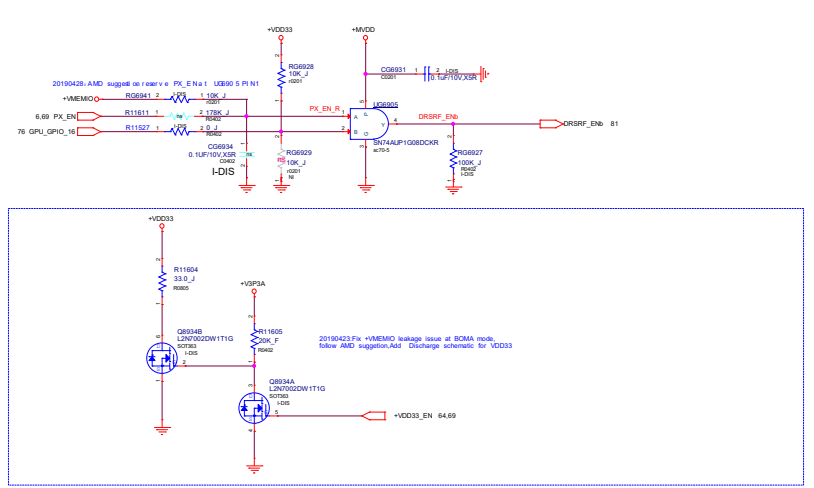
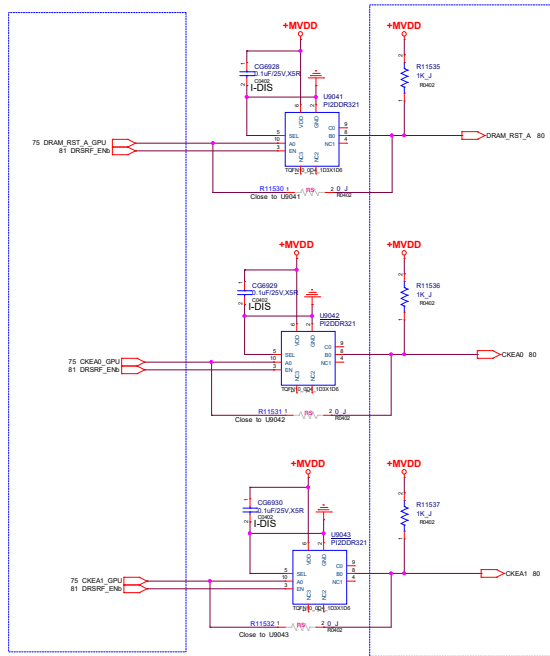
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