PROJECT NAME : BAL23
PCB NO : LA-D804P(Stoney)

Dell / Compal Confidential

Schematic Document

AMD Stoney FT4
AMD R16M-M30 (23 X 23mm)+GDDR5 x2

2016-6-17 Rev: 1.0(A00)

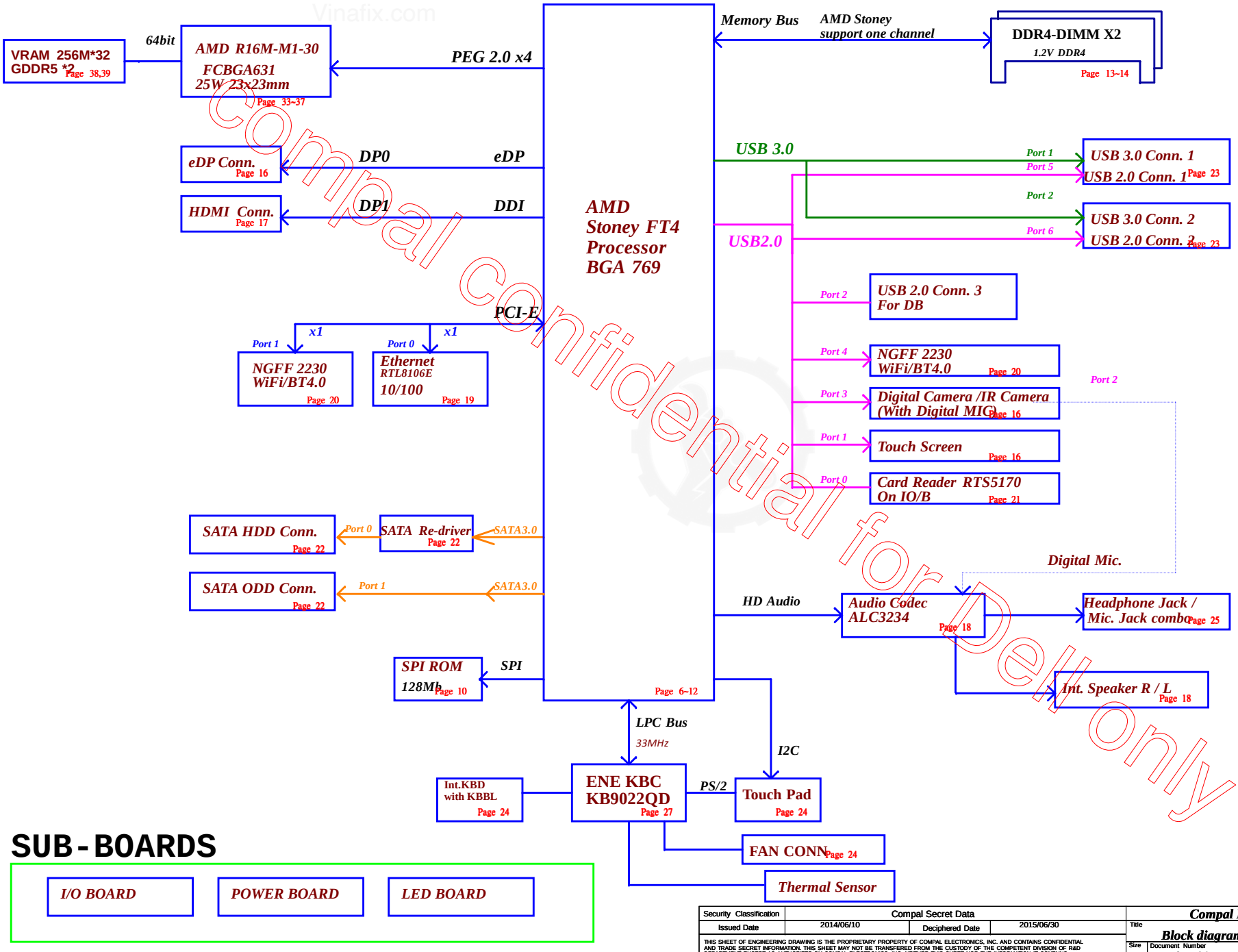
Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: **Cover Page**

Size	Document Number	Rev
	LA-D804P	0.1

Date: Monday, June 20, 2016 Sheet 1 of 54



SUB - BOARDS

I/O BOARD | POWER BOARD | LED BOARD

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

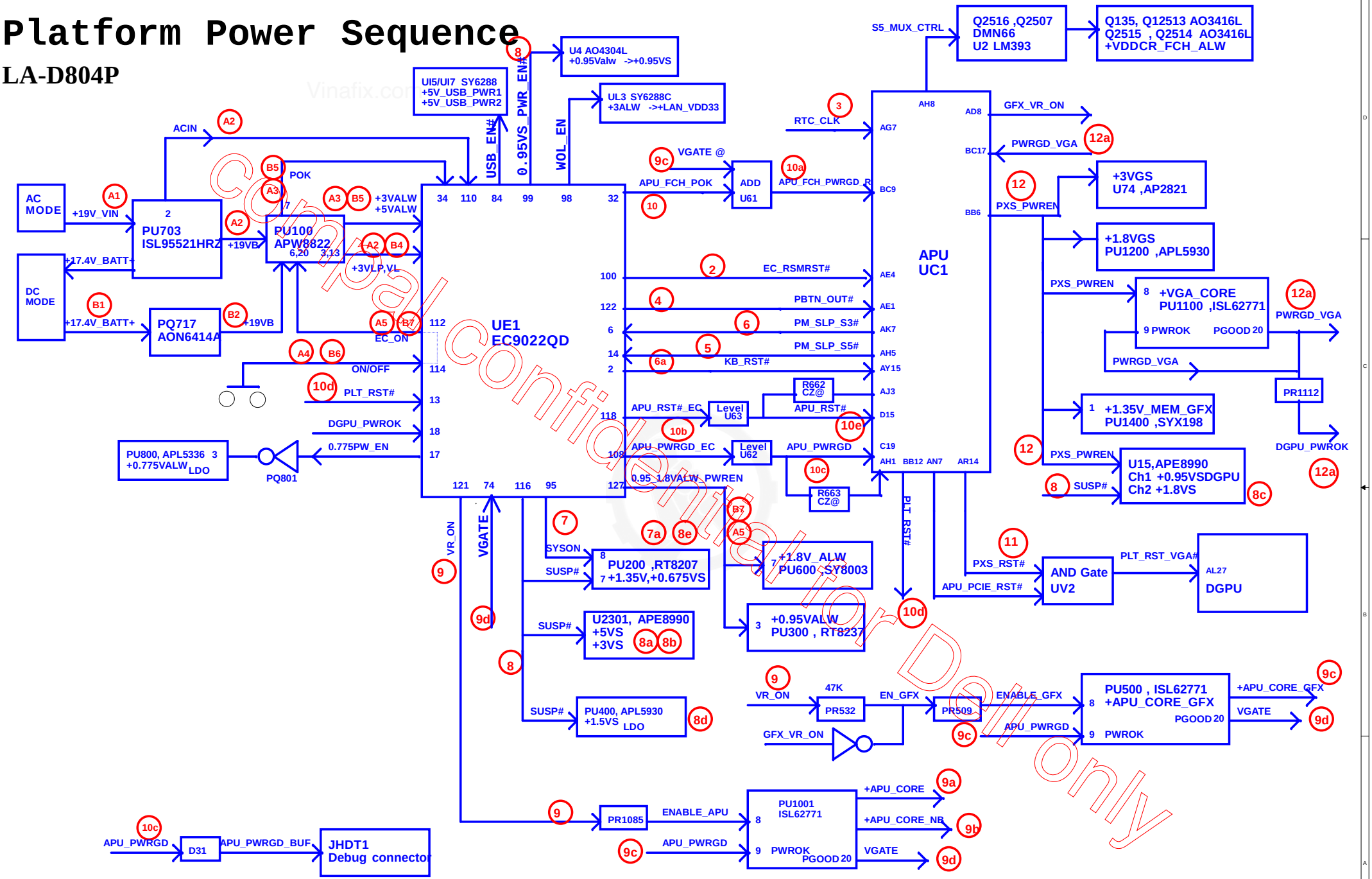
Title: **Block diagram**

Size	Document Number	Rev
	LA-D804P	0.1

Date: Monday, June 20, 2016 | Sheet 2 of 54

Platform Power Sequence

LA-D804P



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: **Power Sequence diagram**

Size	Document Number	Rev
	LA-D804P	0.1

Date: Monday, June 20, 2016 Sheet 3 of 54

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

BOARD ID Table

Board ID	
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	BAL23 AMD Stoney DIS EVT
11	BAL23 AMD Stoney UMA EVT
12	BAL23 AMD Stoney DVT1
13	BAL23 AMD Stoney DVT2
14	BAL23 AMD Stoney X build
15	
16	
17	
18	
19	

SMBUS Control Table

	SOURCE	BATT	Charger	DIMM	APU	GPU	Thermal Sensor		
EC_SMB_CK1 EC_SMB_DA1	KB9022Q	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9022Q				V	V	V		
EC_I2C_TPCLK EC_I2C_TPDAT	KB9022Q								
APU_SCLK0 APU_SDATA0	APU			V					
APU_SCLK1 APU_SDATA1	APU								
APU_SIC APU_SID	APU						V		

Link

ULT	
USB3.0	
Port1	
Port2	USB3 connector 1
Port3	USB3 connector 2
Port4	
USB2.0	
Port0	Card Reader
Port1	Touch Screen Panel
Port2	USB connector 3 (D/B)
Port3	Camera
Port4	NGFF Card (WLAN)
Port5	USB3 connector 1
Port6	USB3 connector 2
Port7	
PCI GPP	
Lane 1	10/100 LAN
Lane 2	NGFF Card (WLAN)
Lane 3	
PCI GFX	
Lane 1	PEG (AMD)EXO UL
Lane 2	PEG (AMD)EXO UL
Lane 3	PEG (AMD)EXO UL
Lane 4	PEG (AMD)EXO UL
SATA	
SATA0	HDD
SATA1	ODD

CLOCK SIGNAL	
CLKOUT_PCIE0	10/100 LAN
CLKOUT_PCIE1	NGFF Card (WLAN)
CLKOUT_PCIE2	
CLKOUT_PCIE3	
GFX CLK	dGPU

Symbol Note :

: means Digital Ground

: means Analog Ground

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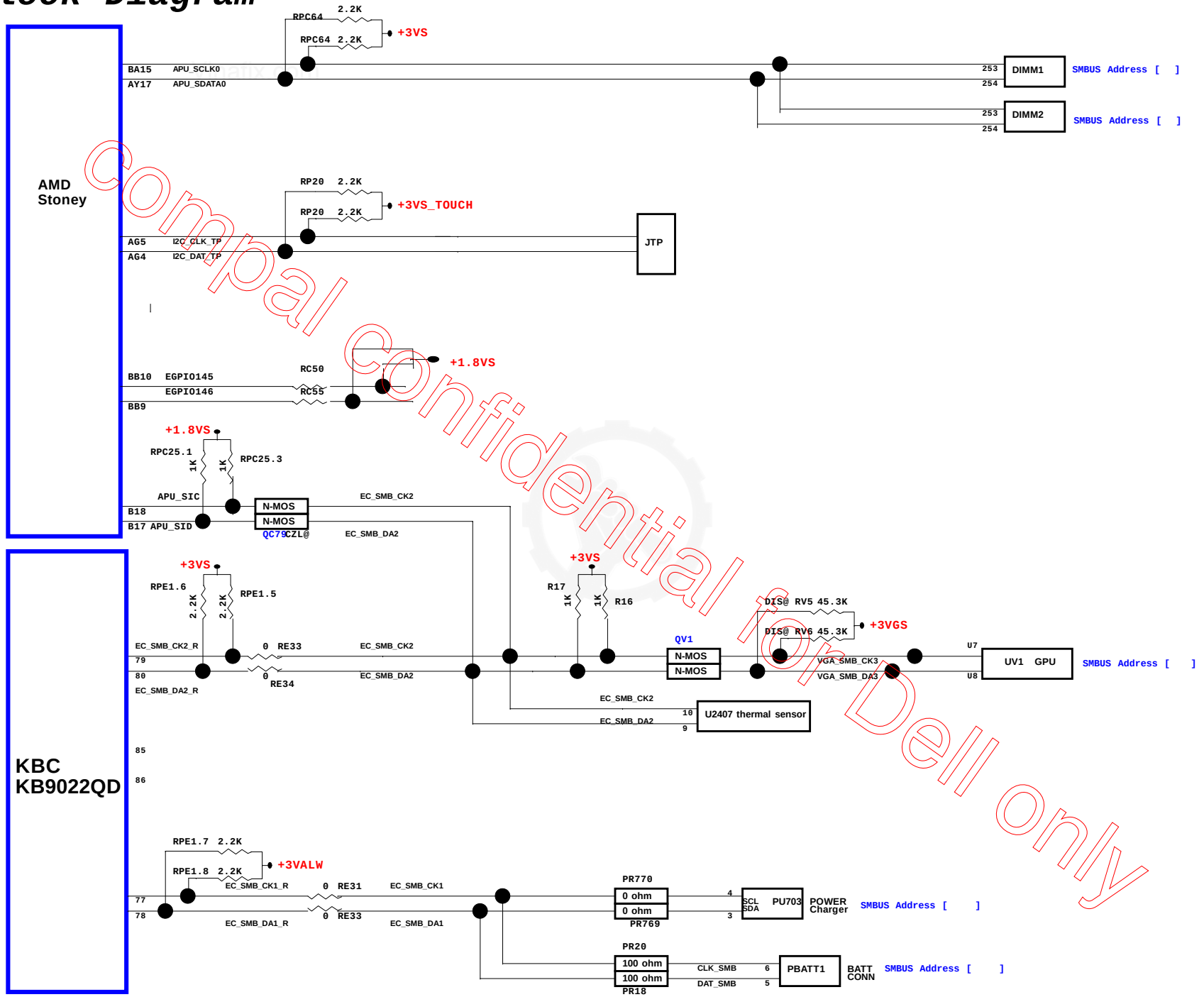
Title: Notes List

Size | Document Number: LA-D804P | Rev: 0.1

Date: Monday, June 20, 2016 | Sheet 4 of 54

SMBus Block Diagram



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

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Title: SMBus block diagram

Size	Document Number	Rev
	LA-D804P	0.1

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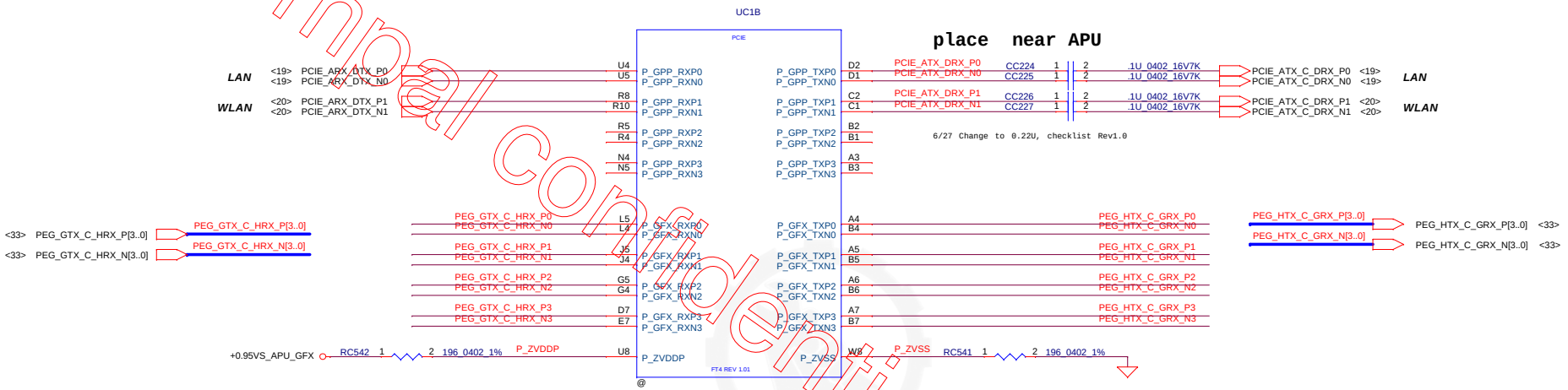
Main Func = CPU



CPU R1 PN	CPU R3 PN
UC1 SA0000A2A0L A6_R1@ S IC A6-9200 AM9200AKN23AC 2G BGA 769P	UC1 SA0000A2A1L A6_R3@ S IC A6-9200 AM9200AKN23AC 2G BGA A31!
UC1 SA00009W80L E2_R1@ S IC E2-9000 EM9000AKN23AC 1.8G BGA 769P	UC1 SA00009W81L E2_R3@ S IC E2-9000 EM9000AKN23AC 1.8G BGA A31!
UC1 SA0000A280L A9_R1@ S IC A9-9400 AM9400AKN23AC 2.4G BGA 769P	UC1 SA0000A281L A9_R3@ S IC A9-9400 AM9400AKN23AC 2.4G BGA A31!
UC1 SA00009PC1L A99430_R1@ S IC A9-9430 2D3201AJN23AC 3.2G BGA 769P	

update CPU R3 PN 5/26

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: FP4 PCIE/UMI

Size: Custom | Document Number: LA-D804P | Rev: 0.1

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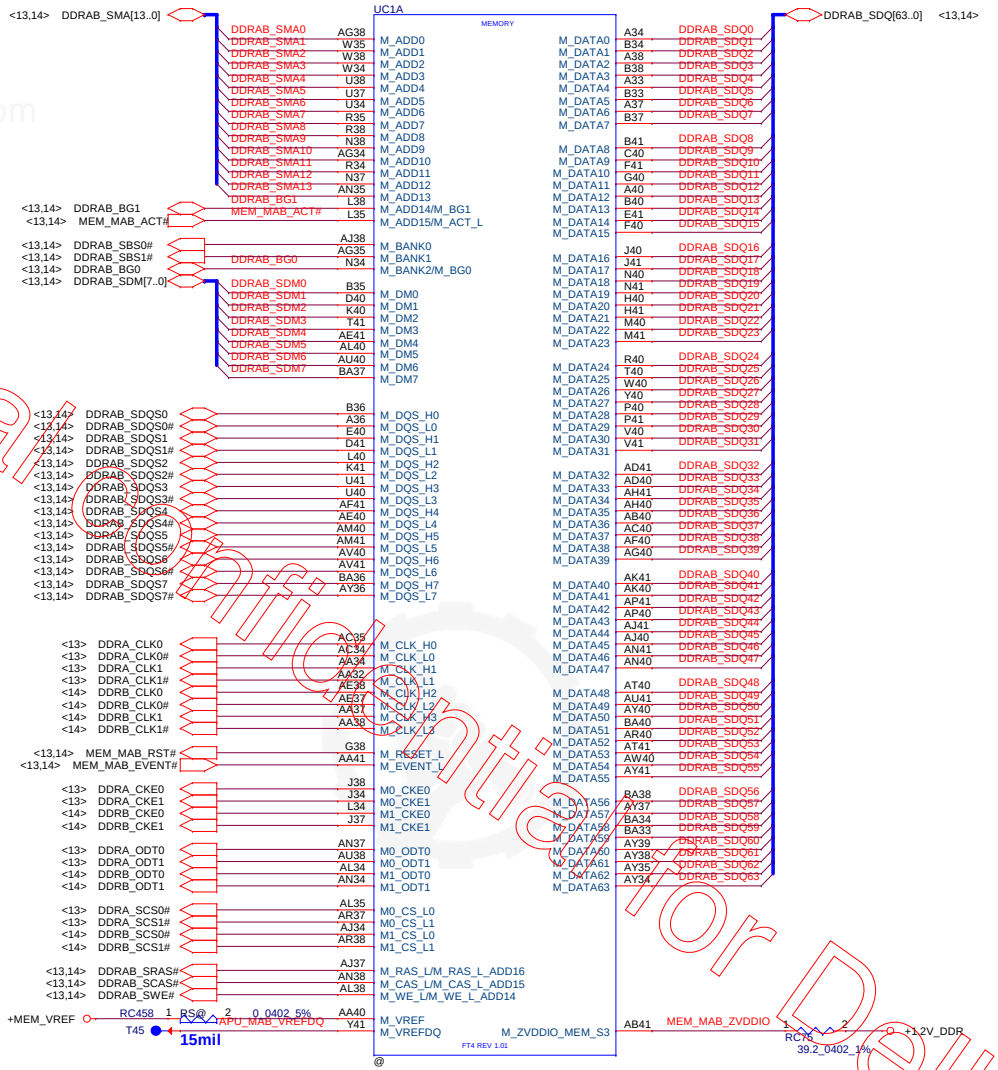
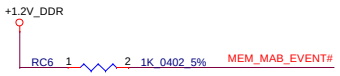
Main Func = CPU

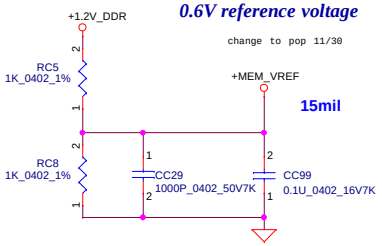


Place them close to APU within 1"

EVENT# pull high



0.6V reference voltage



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: FP4 DDRIII MEMORY

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Date: Monday, June 20, 2016 | Sheet 7 of 54

Main Func = CPU

follow DG change to 0-Ω CRB 12/07

Place resistor(0ohm) for SVT(RC673) on VRM side

SVC ,SVD place on APU side

reserve 0 ohm 11/24

reserve 0 ohm 11/24

reserve 0 ohm 11/24

Place near APU

remove cap for emi 12/07

DP1: HDMI
DP0: eDP

2014/08/12 Modify

del cz@ 10/15

PU at EC side

follow esd require 11/27

HDT+

HDT debug + HDT@

change to 0.01u 10/19

change to pu up11/19

modify to R-Short 4/29

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.			
Title	FT4 DISP/MISC/HDT		
Size	Document Number		Rev
Custom	LA-D804P		0.1
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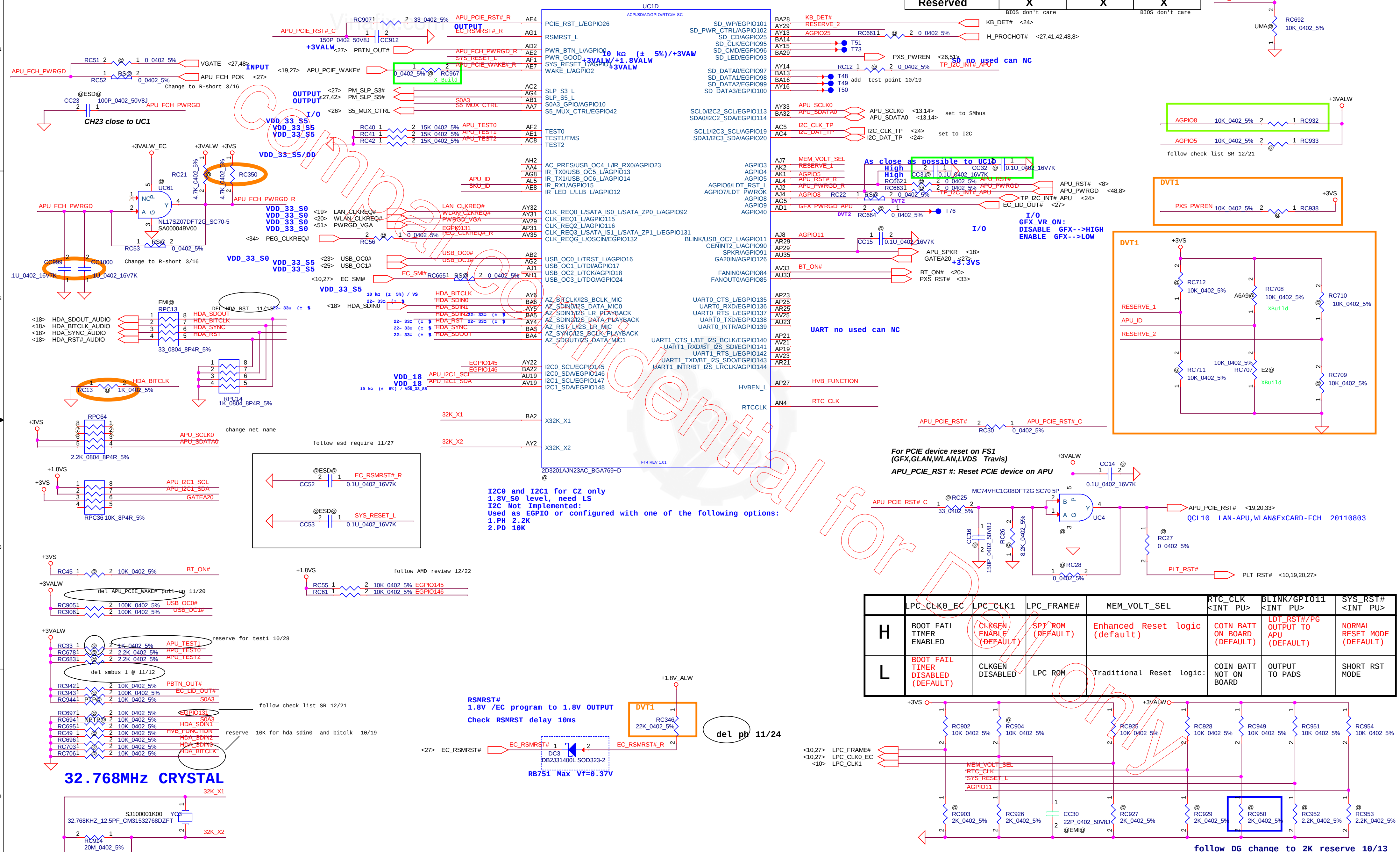
Main Func = CPU

	RESERVE_1 (AGPIO4)	APU_ID (AGPIO15)	RESERVE_2 (AGPIO102)
A6A9@	X	1	X
E2@	X	0	X
Reserved	X	X	X
Reserved	X	X	X
	BIOS don't care		BIOS don't care



	LPC_CLK0_EC	LPC_CLK1	LPC_FRAME#	MEM_VOLT_SEL	RTC_CLK <INT PU>	BLINK/GPIO11 <INT PU>	SYS_RST# <INT PU>
H	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	SPI ROM (DEFAULT)	Enhanced Reset logic (default)	COIN BATT ON BOARD (DEFAULT)	LDT_RST#/PG OUTPUT TO APU (DEFAULT)	NORMAL RESET MODE (DEFAULT)
L	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	LPC ROM	Traditional Reset logic:	COIN BATT NOT ON BOARD	OUTPUT TO PADS	SHORT RST MODE

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/06/10	Deciphered Date 2015/06/30	Title: FT4 GPIO/AZ/MISC/STRAPS

Size: Custom | Document Number: LA-D804P | Rev: 0.1
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Main Func = CPU

UC1E

CLK/SATA/USB/SPI/LPC

HDD
ODD
VGA
LAN
WLAN

SATA_TX0P / SATA_TX0N
SATA_RX0N / SATA_RX0P
SATA_TX1P / SATA_TX1N
SATA_RX1N / SATA_RX1P
SATA_ZVSS / SATA_ZVDDP
SATA_ACT_L/GPIO130
DEVSLP0/EGPIO67
DEVSLP1/EGPIO70
GFX_CLKP / GFX_CLKN
GPP_CLK0P / GPP_CLK0N
GPP_CLK1P / GPP_CLK1N
GPP_CLK2P / GPP_CLK2N
GPP_CLK3P / GPP_CLK3N
X48M_X1 / X48M_X2
X25M_48M_OSC

USBCLK/25M_48M_OSC
USB_ZVSS
USB_HSD0P / USB_HSD0N
USB_HSD1P / USB_HSD1N
USB_HSD2P / USB_HSD2N
USB_HSD3P / USB_HSD3N
USB_HSD4P / USB_HSD4N
USB_HSD5P / USB_HSD5N
USB_HSD6P / USB_HSD6N
USB_HSD7P / USB_HSD7N
USB_SS_ZVSS / USB_SS_ZVDDP
USB_SS_0TXP / USB_SS_0TXN
USB_SS_0RXP / USB_SS_0RXN
USB_SS_1TXP / USB_SS_1TXN
USB_SS_1RXP / USB_SS_1RXN
USB_SS_2TXP / USB_SS_2TXN
USB_SS_2RXP / USB_SS_2RXN

- Card Reader
- Touch screen panel
- USB Conn IO PORT3 (DVT1) — change to port2 3/16
- Camera
- Mini Card (WLAN)
- USB Conn MB PORT1
- USB Conn MB PORT2

usb 3.0

- USB Conn PORT1
- USB Conn PORT2

emc request 11/26

SPI_CLK/ESPI_CLK/EGPIO117
SPI_DO/ESPI_DAT0/EGPIO121
SPI_DI/ESPI_DAT1/EGPIO120
SPI_HOLD_L/ESPI_DAT3/EGPIO133
SPI_WP_L/ESPI_DAT2/EGPIO122
SPI_CS1_L/EGPIO118
SPI_TPM_CS_L/AGPIO76
ESPI_ALERT_L/LDRQ0_L
ESPI_RESET_L/KBRST_L/AGPIO129
SPI_CS2_L/ESPI_CS_L/EGPIO119

LPC_CLK0_EC / LPC_CLK1 / LPC_FRAME# / LPC_AD0 / LPC_AD1 / LPC_AD2 / LPC_AD3
LPCCLK0/EGPIO74
LPCCLK1/EGPIO75
LFRAME_L
LAD0 / LAD1 / LAD2 / LAD3
LPC_RST_L
LPC_CLKRUN_L/AGPIO88
LPC_PD_L/AGPIO21
LPC_PME_L/AGPIO22
LPC_SMI_L/AGPIO86
SERIRQ/AGPIO87

OUTPUT

VDD_33_S5
CZ-->S0, CZL->S5

FT4 REV 201
@ 2D3201AJN23AC_BGA769-D

7/25 Add, EMI request

+3.3VS

48MHz CRYSTAL

YC2
48MHZ_8PF_X3S048000D81H-W
Part Number = SJ10000AF00

C796 5.6P_0402_50V8D
C797 5.6P_0402_50V8D

8MB SPI ROM

UC5
/CS / DO(IO1) / /WP(IO2) / GND / VCC / /HOLD(IO3) / CLK / DI(IO0)

JH1 CONN@
CS# / WP# / HOLD# / GND / VCC / SCLK / SI/SIO0 / SO/SIO1
ACES_91960-0084N_MX25L3206EM2I

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

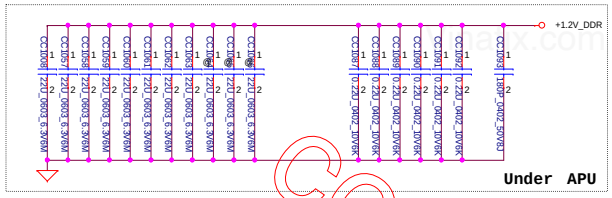
Compal Electronics, Inc.

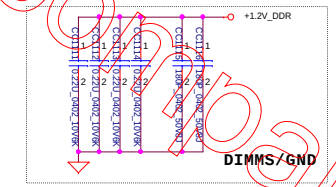
Title: FT4 SATA/CLK/USB/SPI

Size: Custom | Document Number: LA-D804P | Rev: 0.1

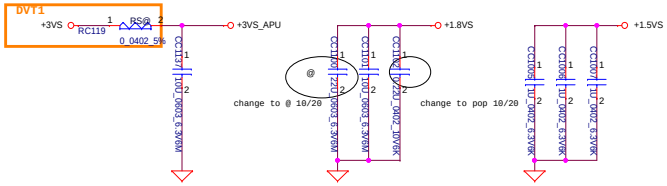
Date: Monday, June 20, 2016 | Sheet 10 of 54

Main Func = CPU



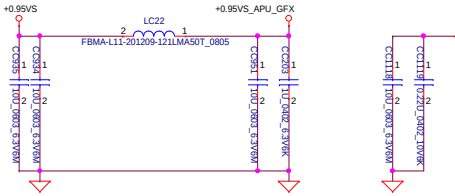


FOR DEBUG ONLY

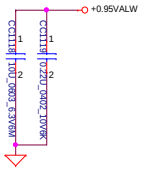


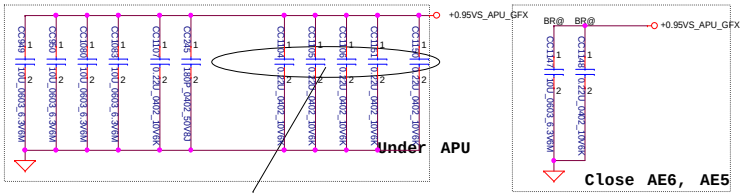
+0.95VALW/+0.95VS OF APU +VDDP_VS

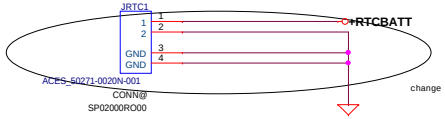
VDD_095 VDD_095_GFX

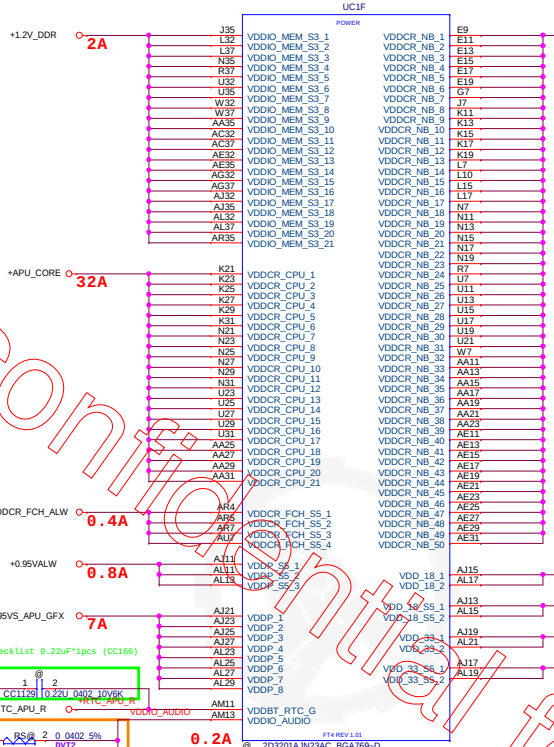


+VDDP_ALW

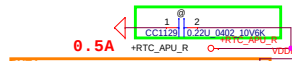


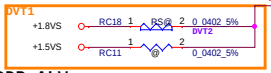


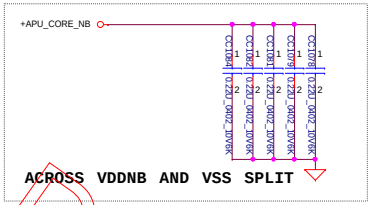


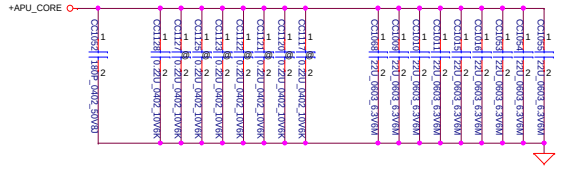


extra 0.22uF, Follow AMD checklist 0.22uF*1pcs (CC166)

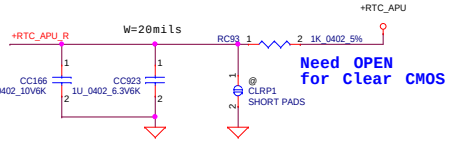




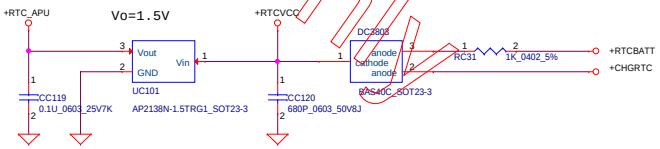




RTC OF APU



Need OPEN for Clear CMOS



OPEN

SHORT

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: FT4 PWR

Size	Document Number	Rev
C	LA-D804P	0.1

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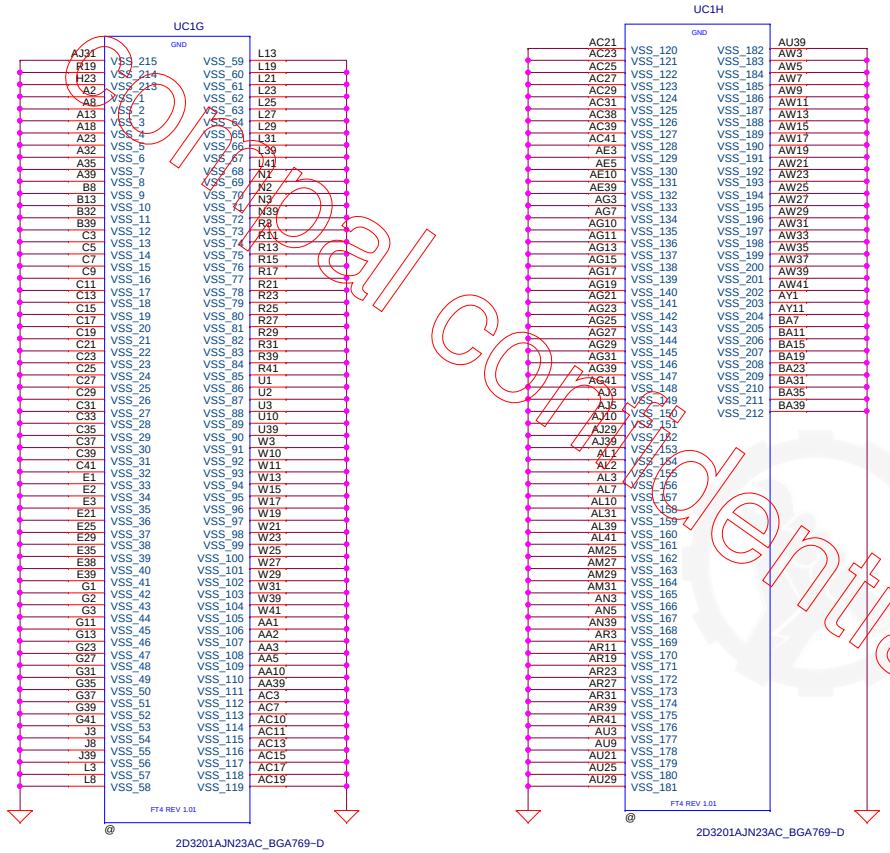
Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: FT4 GND

Size	Document Number	Rev
Custom	LA-D804P	0.1

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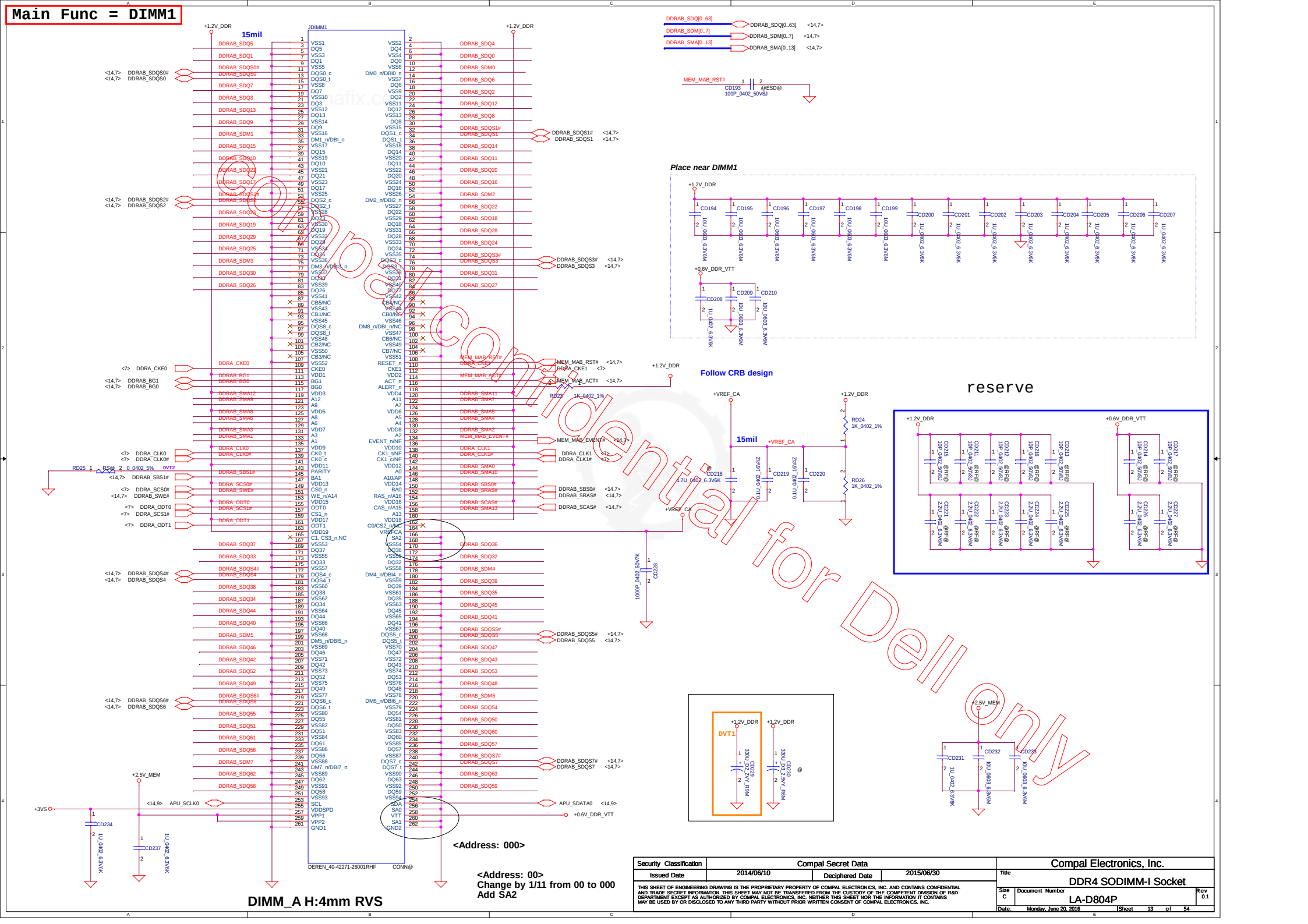
Main Func = DIMM1



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

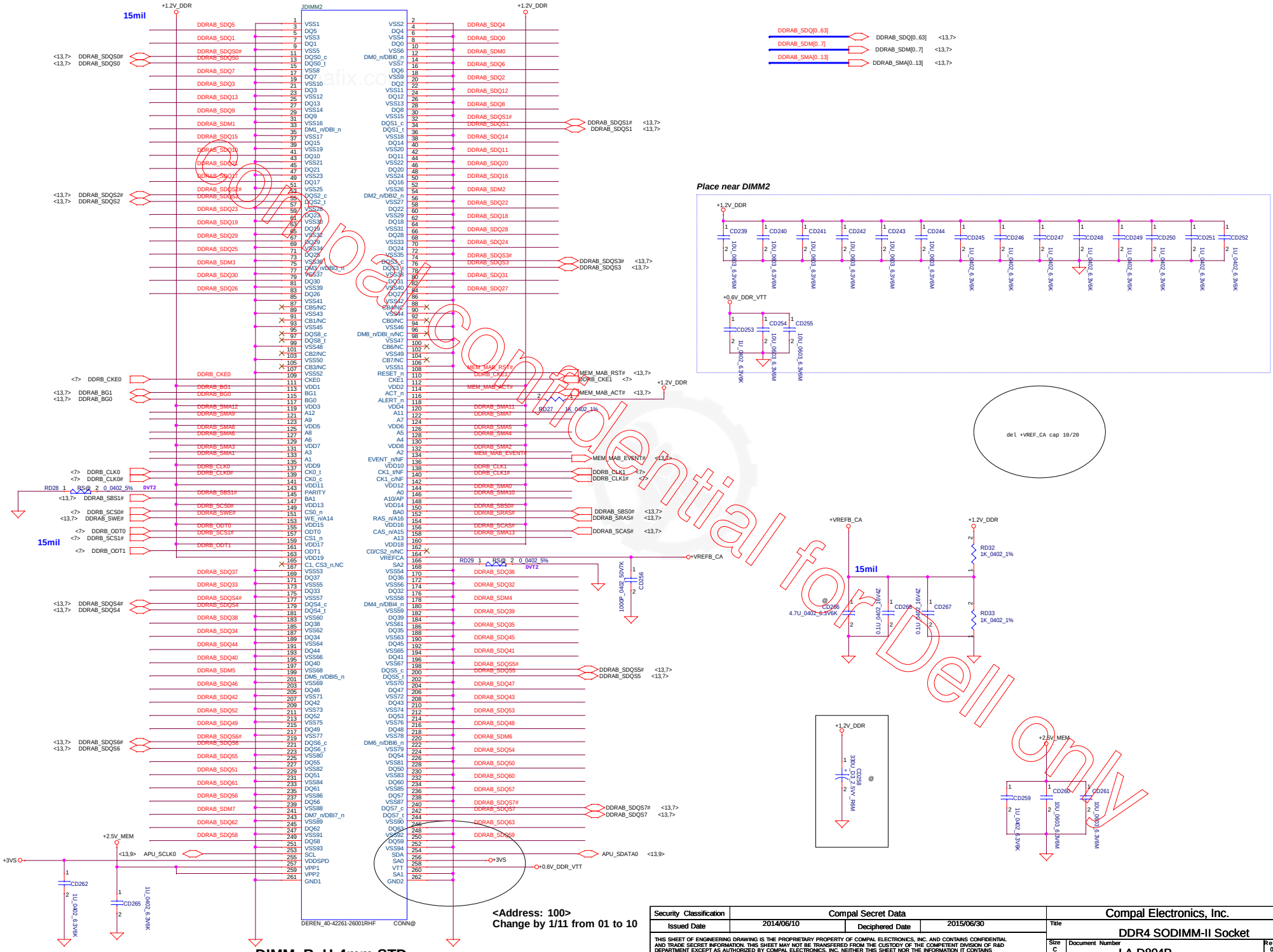
Compal Electronics, Inc.

Title: DDR4 SODIMM-I Socket

Size	Document Number	Rev
C	LA-D804P	0.1

Date: Monday, June 20, 2016 Sheet 13 of 54

Main Func = DIMM2



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: DDR4 SODIMM-II Socket

Size	Document Number	Rev
C	LA-D804P	0.1

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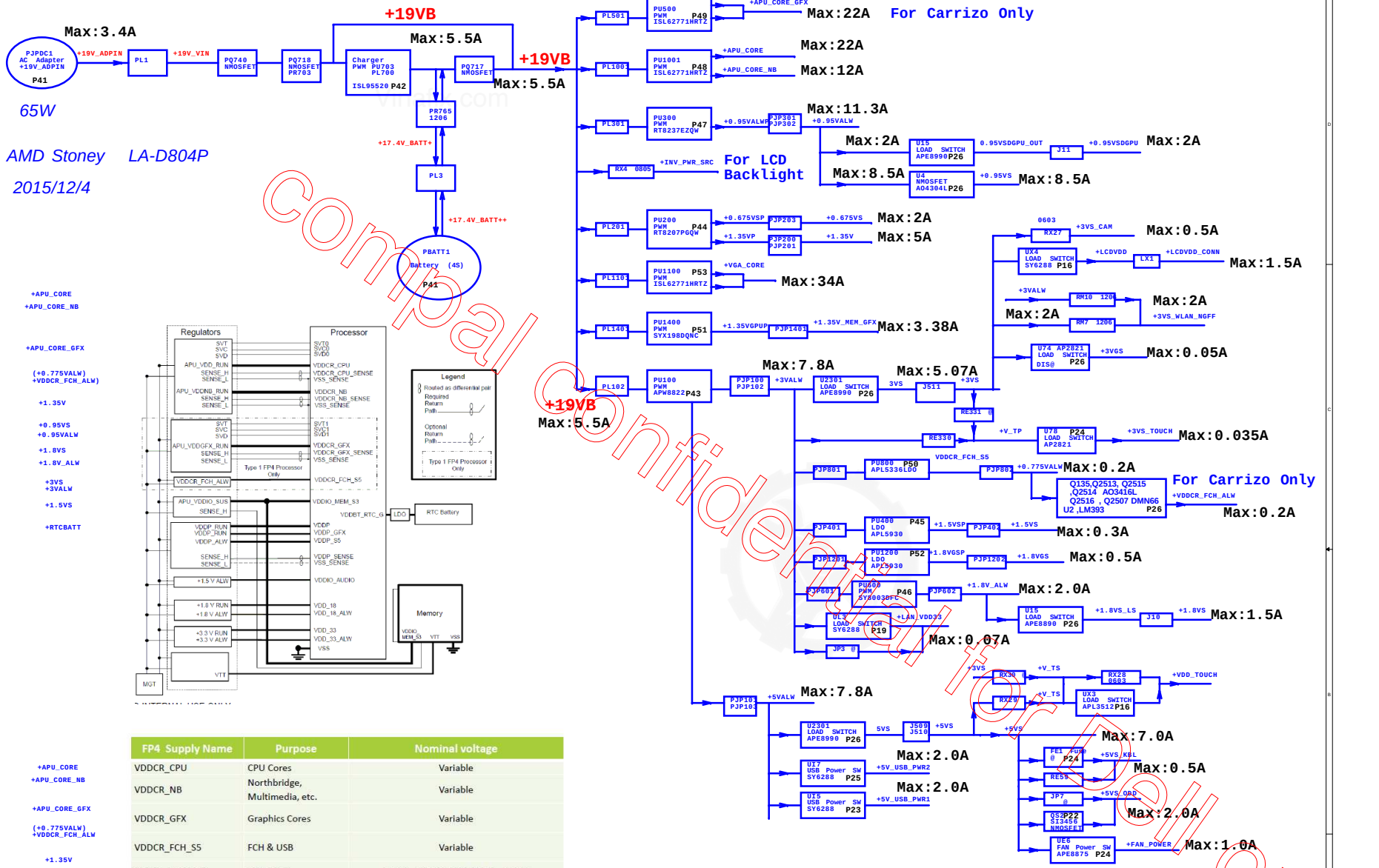
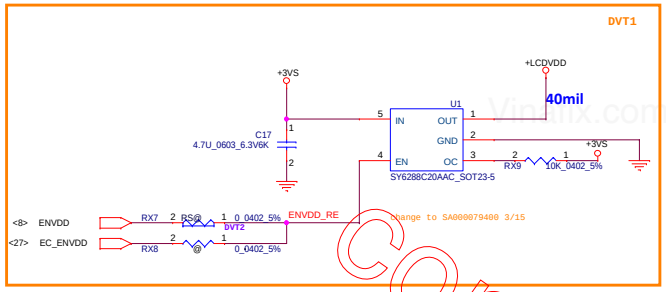
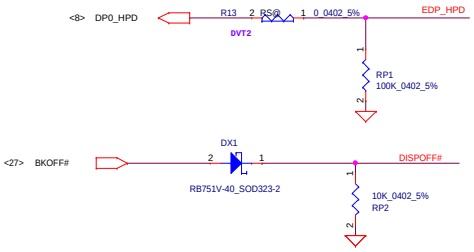


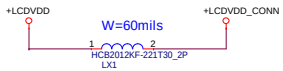
FP4 Supply Name	Purpose	Nominal voltage
VDDCR_CPU	CPU Cores	Variable
VDDCR_NB	Northbridge, Multimedia, etc.	Variable
VDDCR_GFX	Graphics Cores	Variable
VDDCR_FCH_S5	FCH & USB	Variable
VDDIO_MEM_S3	MEM PHY	DDR3 = 1.5V, 1.35V, DDR4 = 1.20V
VDDP	PCIE & DISPLAY PHYs	1.05V
VDDP_GFX	x8 dGPU PCIE PHY	
VDDP_S5	USB PHYs	
VDD_18	PLLs	1.8V
VDD18_S5	RTC, USB2, USB3	1.8V
VDD_33	GPIO (S0), SDIO, I2C, LPC, etc.	3.3V
VDD_33_S5	GPIO (S5), USB2	3.3V
VDDIO_AUDIO	AZ, I2S	1.5V (AZ)/1.8V (I2S)
VDDBT_RTC_G	RTC	1.5V

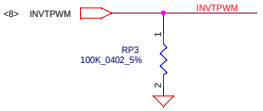
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/06/10	Deciphered Date 2015/06/30	Title: Green CLK
			Size: Document Number: LA-D804P Rev: 0.1
			Date: Monday, June 20, 2016 Sheet 15 of 54

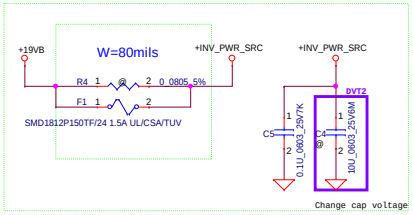
Main Func = LCD

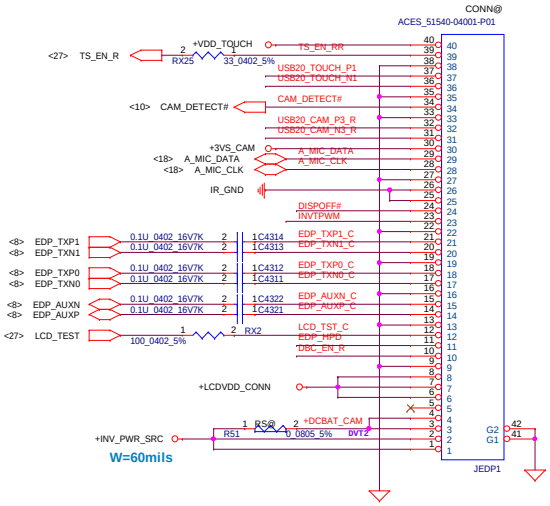




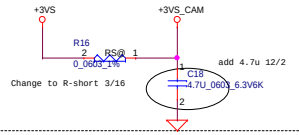


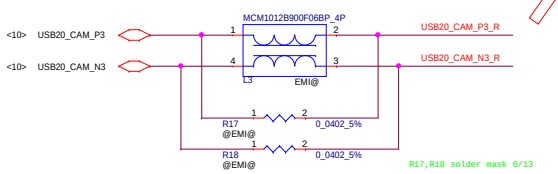


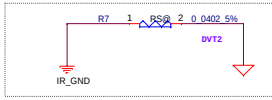




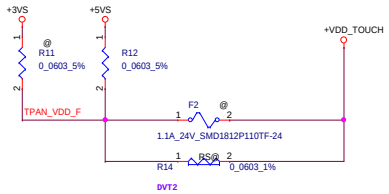
Webcam PWR CTRL

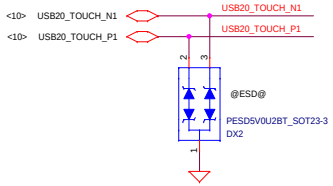


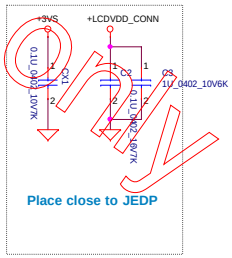




* Touch Screen Panel







Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

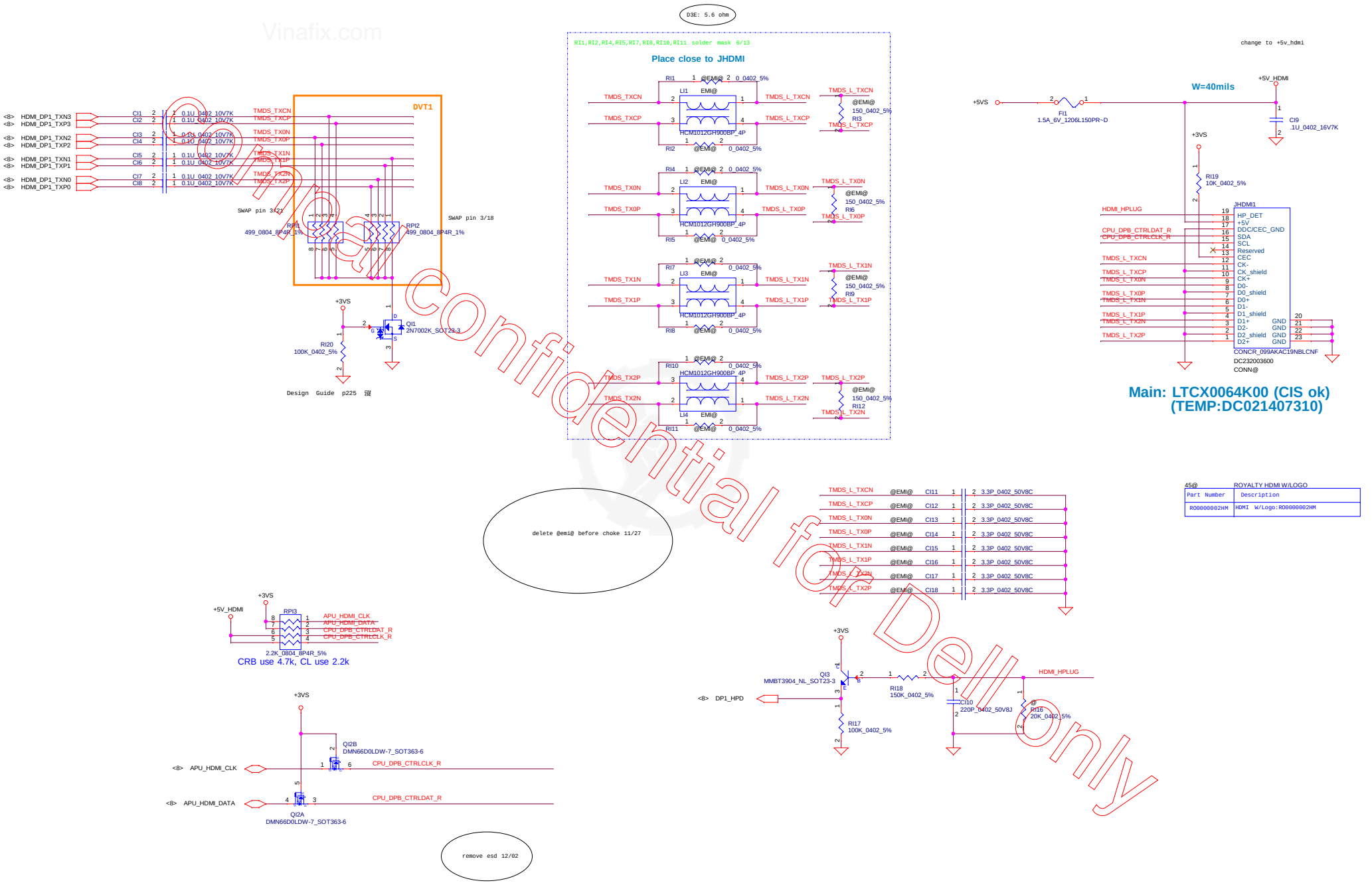
Compal Electronics, Inc.

Title: eDP / webcam / TouchScreen

Size	Document Number	Rev
	LA-D804P	0.1

Date: Monday, June 20, 2016 Sheet 16 of 54

Main Func = HDMI



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

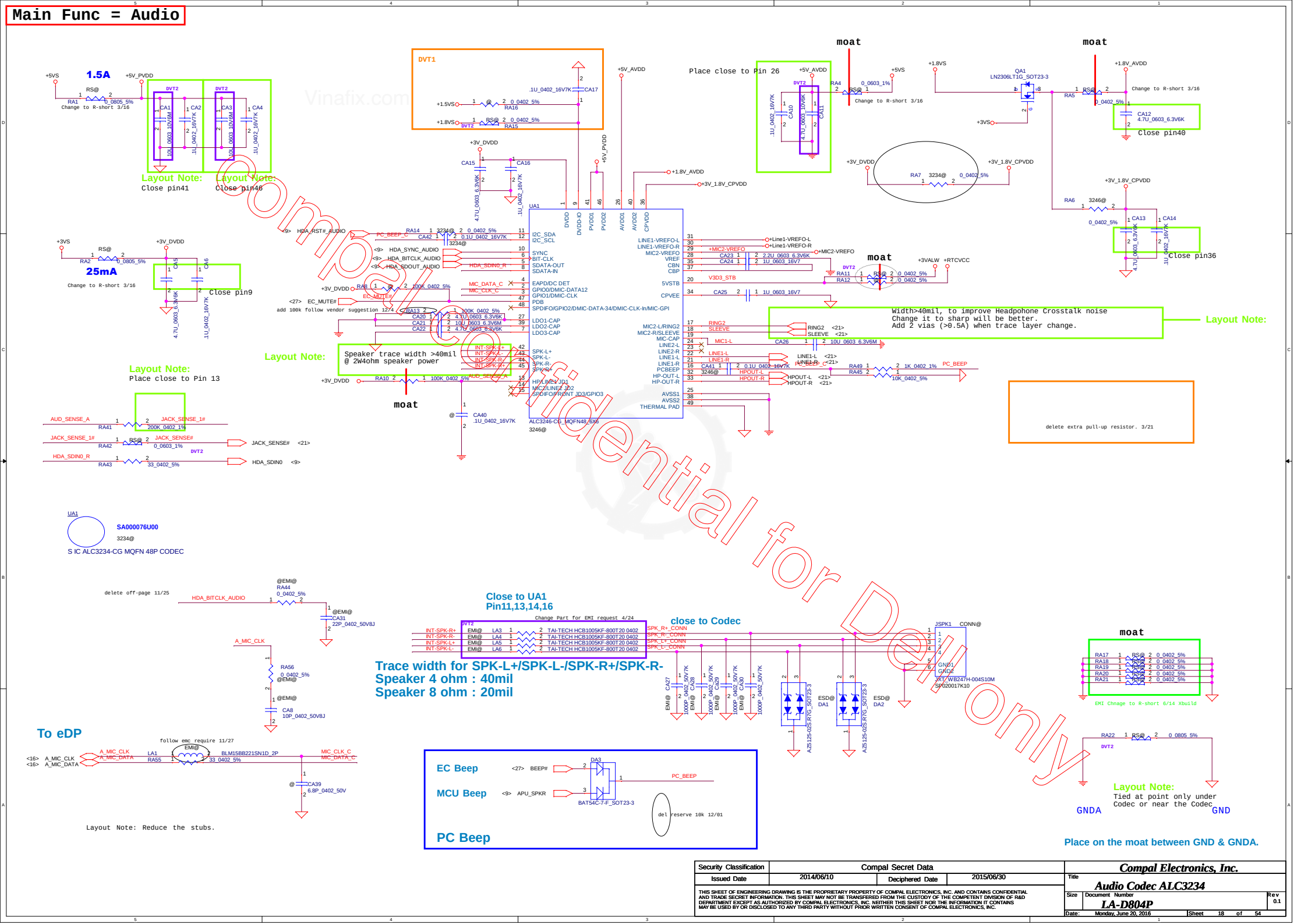
Compal Electronics, Inc.

Title: **HDMI**

Size	Document Number	Rev
	LA-D804P	0.1

Date: Monday, June 20, 2016 Sheet 17 of 54

Main Func = Audio



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: Audio Codec ALC3234

Size	Document Number	Rev
	LA-D804P	0.1

Date: Monday, June 20, 2016 Sheet 18 of 54

Main Func = LAN

followe nuvision Patrick suggestion

+LAN_VDD33 rising time : >0.5ms and <100ms

OPEN

+3VALW — JP3 2MM — +LAN_VDD33

W=40mils W=40mils

<27> WOL_EN

CL9 1U_0402_6.3V6K

UL3 AP22802AW5-7 SOT25 5P (IN, OUT, GND, EN, OC)

RL7 10K_0402_5%

RL6 100K_0402_5%

followe nuvision Patrick suggestion

10/100 ethernet design : 20mil

+LAN_VDD10

CL3 0.1U_0402_25V6 CL5 0.1U_0402_25V6

W=40mils

+LAN_VDD33 1.5A

CL8 0.1U_0402_10V7K CL7 4.7U_0603_6.3V6K

RL5 0_0603_1% RSG@ +LAN_VDDREG

Change to R-short 3/16

CL14 0.1U_0402_25V6

Place close to UL1: Pin 32

followe nuvision Patrick suggestion

UL1 RTL8106E-CG_QFN32_4X4

CL1, CL2 close to UL1 Pin 17, 18

MDI0+ MDI0- MDI1+ MDI1- MDIP0 MDIN0 MDIP1 MDIN1

+LAN_VDD10 +LAN_VDD33 +LAN_VDDREG

AVDD10 AVDD10 AVDD33 DVDD33

<10> CLK_PCIE_LAN <10> CLK_PCIE_LAN# REFCLK_P REFCLK_N

<9> LAN_CLKREQ# CLKREQB

XTLI XTLO CKXTAL1 CKXTAL2

T94 T95 LED0 LED1

2.49K_0402_1%~D RL2 RSET GND

HSOP HSON HSIP HSIN PERSTB ISOLATEB LANWAKEB GPO NC

PCIE_ARX_DTX_P0_C PCIE_ARX_DTX_N0_C 0.1U_0402_10V7K CL1 CL2 PCIE_ARX_DTX_P0 PCIE_ARX_DTX_N0 <6>

PCIE_ATX_C_DRX_P0 PCIE_ATX_C_DRX_N0 PCIE_ATX_C_DRX_P0 PCIE_ATX_C_DRX_N0 <6>

PLT_RST#_R 0_0402_5% RSG@ RL8 RL9 PLT_RST# APU_PCIE_RST# PLT_RST# <10,20,27,9> APU_PCIE_RST# <20,33,9>

DVT2

ISOLATEB

APU_PCIE_WAKE# APU_PCIE_WAKE# <27,9>

10K_0402_5% @ RL1 +LAN_VDD33

followe nuvision Patrick suggestion

LAN TL1 350UH_NS14-1-LF

MDI1- MDI1+ +V_DAC +V_DAC MDI0- MDI0+ RD+ RD- RCT TCT TD+ TD- RX+ RX- RCT TCT TX+ TX- MDO1- MDO1+ MCT0 MCT1 MDO0- MDO0+

+V_DAC CL12 0.01U_0402_16V7K

Place close to TCT pin

MCT0 MCT1 RL14 RL15 75_0603_5%

T-GND_L EMI@ CL13 100P_1206_2KV8J

DVT1 modify to Digital GND 3/21

follow esd require reserve 12/2

EU3501 @ESD@

MDI1- MDI1+ MDI0- MDI0+

JLAN1 SANTA_130460-N CONN@

PR4- PR4+ PR2- PR3- PR3+ PR2+ PR1- PR1+ GND GND GND GND

change conn 12/3

DVT1 modify to Digital GND 3/21

+LAN_VDD33 RL10 10K_0402_5% APU_PCIE_WAKE#

+3VS +LAN_VDD33

LAN_CLKREQ# RL11 @ 10K_0402_5%

WOL_EN RL12 @ 10K_0402_5%

+3VS RL3 1K_0402_5% ISOLATEB RL4 15K_0402_1%

Reserve 10K pull LAN_IO

CL10 10P_0402_50V8J CL11 10P_0402_50V8J YL1 XTLI XTLO XTAL0 GND0 XTAL1 GND1 25MHZ_10PF_7V25000014

XTAL

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

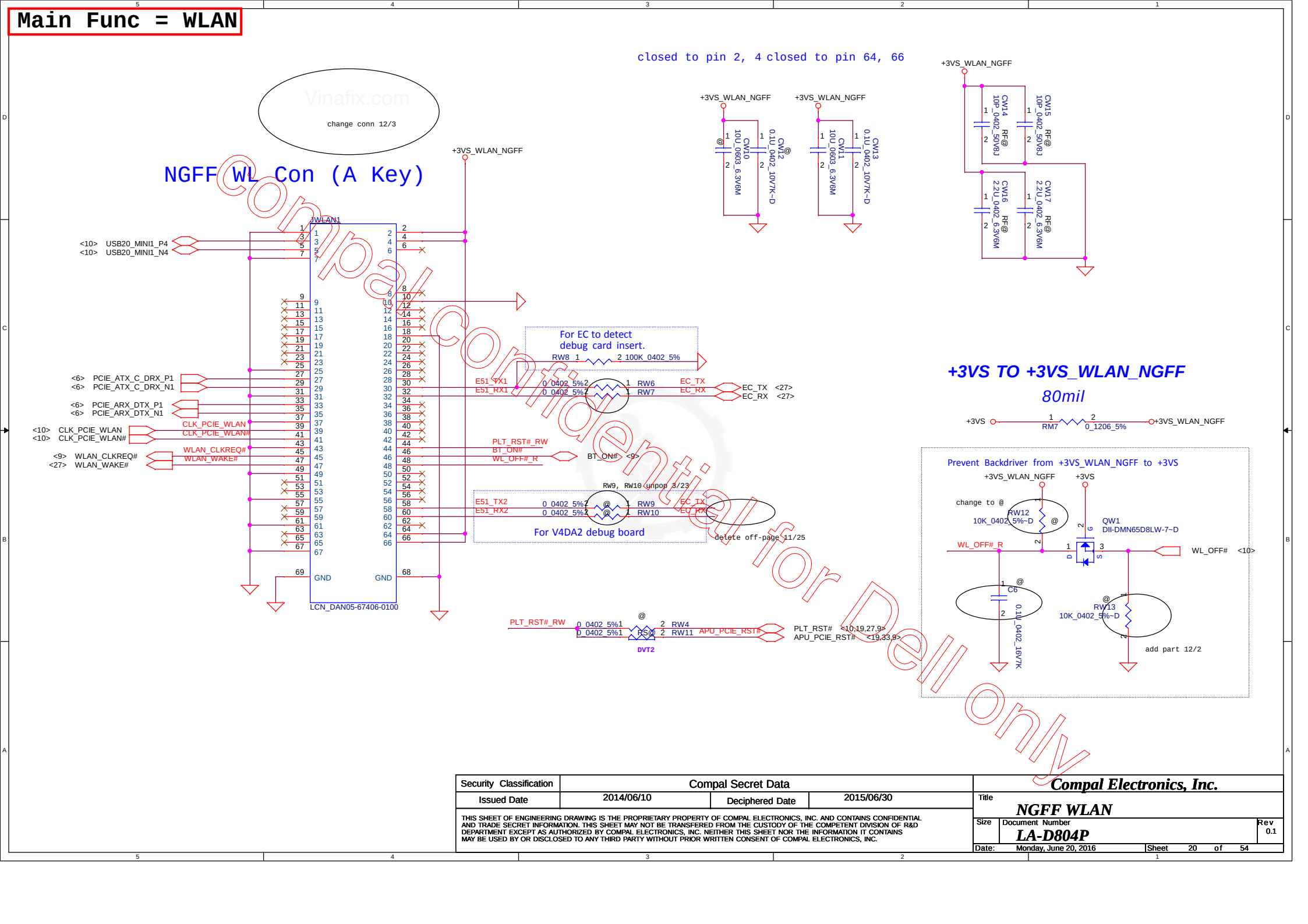
Compal Electronics, Inc.

Title: LAN RTL8106EUS

Size: Custom | Document Number: LA-D804P | Rev: 0.1

Date: Monday, June 20, 2016 | Sheet 19 of 54

Main Func = WLAN



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

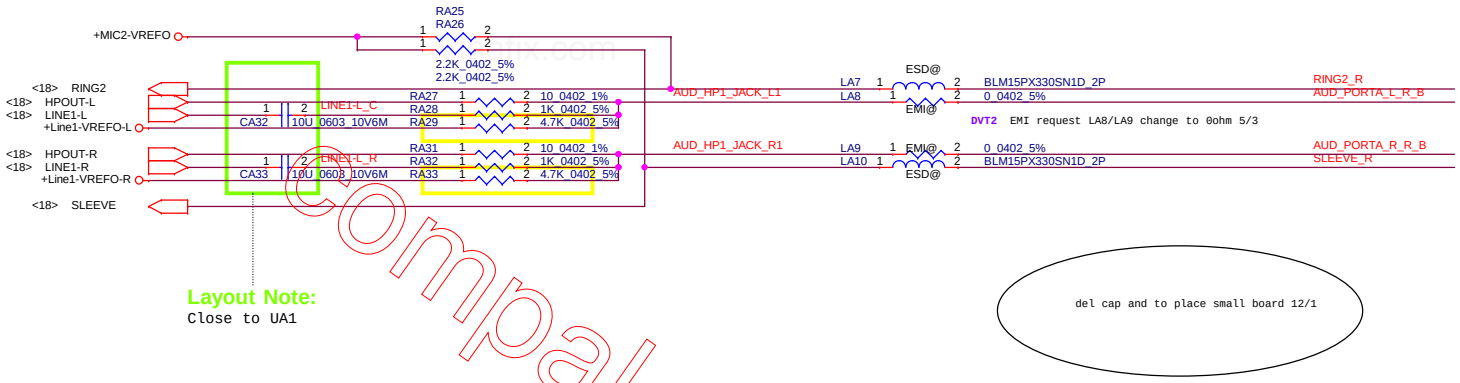
Compal Electronics, Inc.

Title: **NGFF WLAN**

Size	Document Number	Rev
	LA-D804P	0.1

Date: Monday, June 20, 2016 Sheet 20 of 54

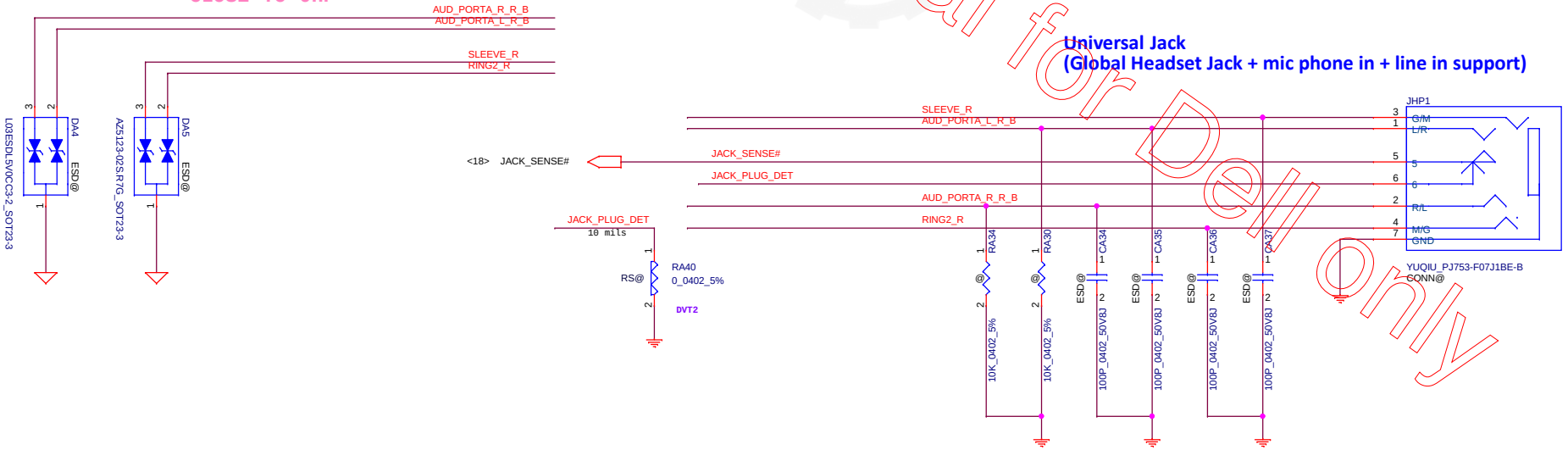
Main Func = Audio Jack



Layout Note:
Close to UA1

del cap and to place small board 12/1

CLOSE TO JHP



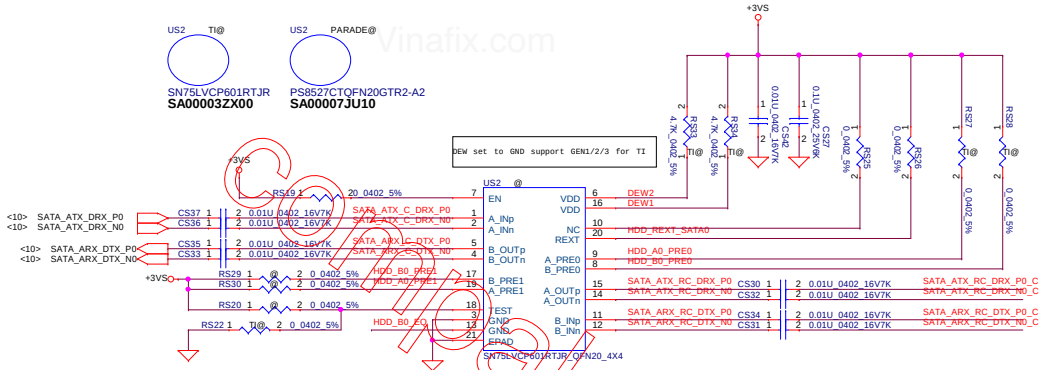
Universal Jack
(Global Headset Jack + mic phone in + line in support)

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

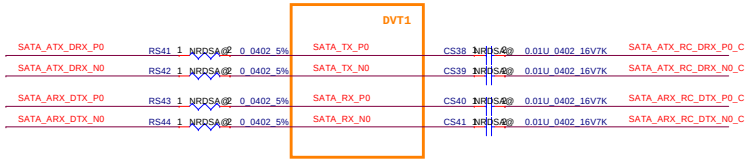
Title	JACK	
Size	Document Number: LA-D804P	Rev: 0.1
Date: Monday, June 20, 2016	Sheet 21 of 54	

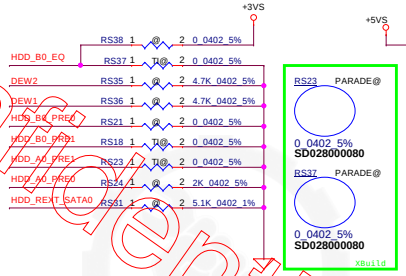
Main Func = HDD



Re-driver EQ setting

Vendor	Part number	RS18	RS22	RS23	RS27	RS28	RS33	RS34	RS37
Parade(M)	SA00007JU10	NC	NC	V	NC	NC	NC	NC	V
TI (2nd)	SA00003ZX00	V	V	V	V	V	4.7K	4.7K	V





DVT1

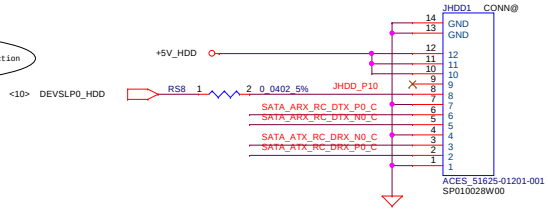
delete ESD component 03/18

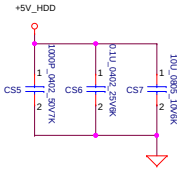
DEVSLP[0] PU 10K, means not support DEVSLP function

+5V_HDD Source

80 mils

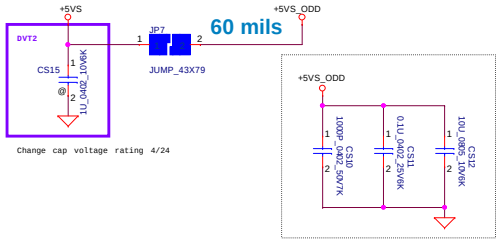
SHORT





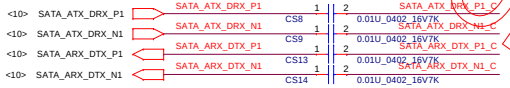
ODD Power Control

need short 11/30



SOC TX

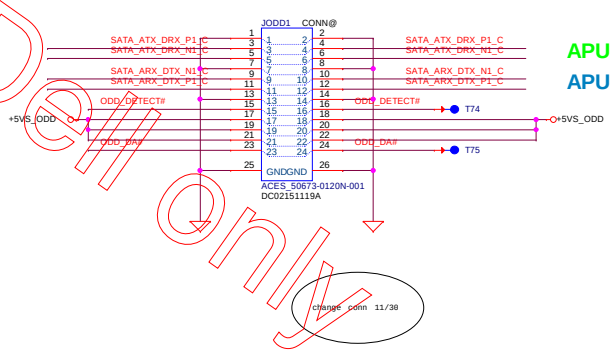
SOC RX



SATA ODD Connector (FFC Type)

APU TX

APU RX



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

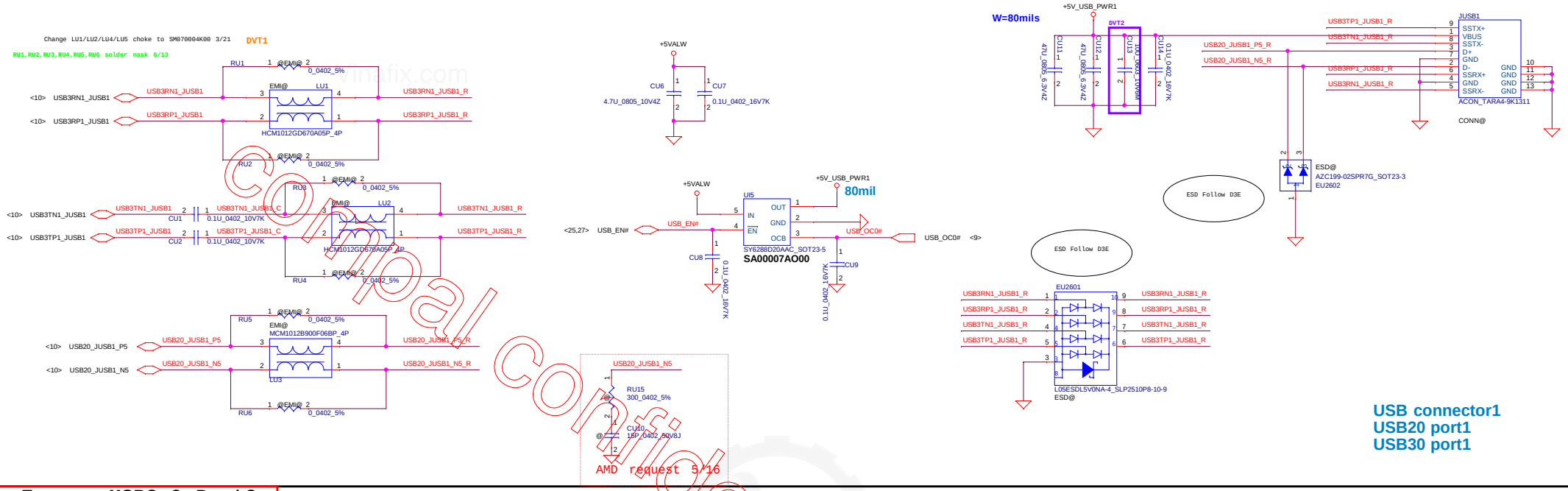
Compal Electronics, Inc.

Title: HDD

Size | Document Number: LA-D804P | Rev: 0.1

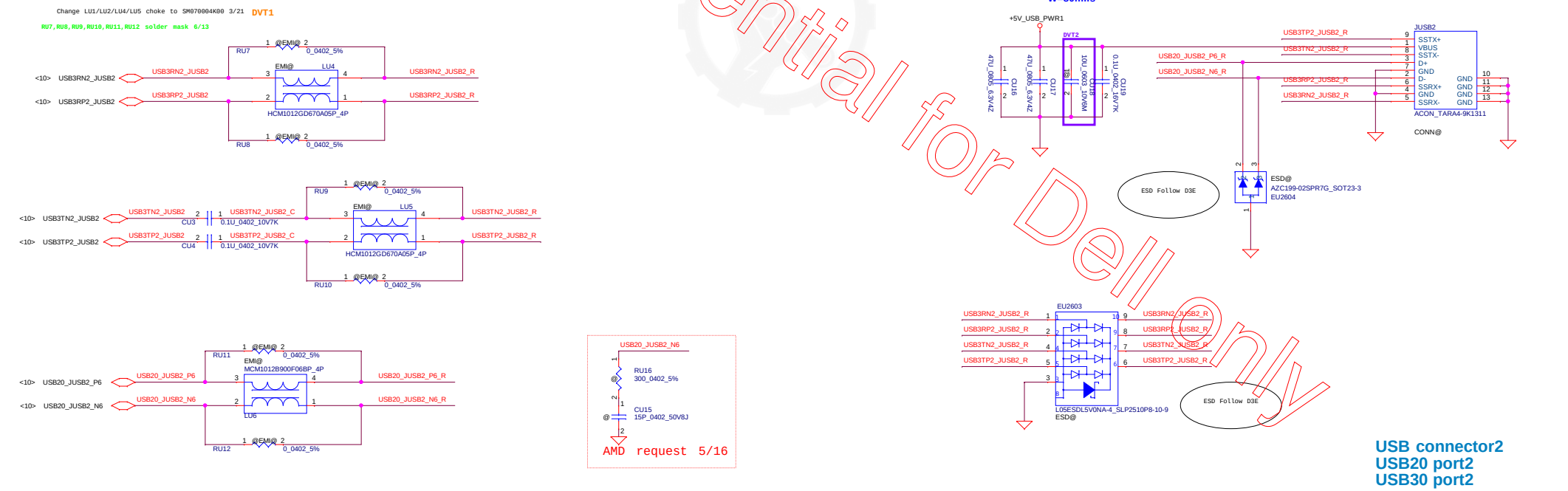
Date: Monday, June 20, 2016 | Sheet 22 of 54

Main Func = USB3.0 Port1



USB connector1
USB20 port1
USB30 port1

Main Func = USB3.0 Port2



USB connector2
USB20 port2
USB30 port2

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

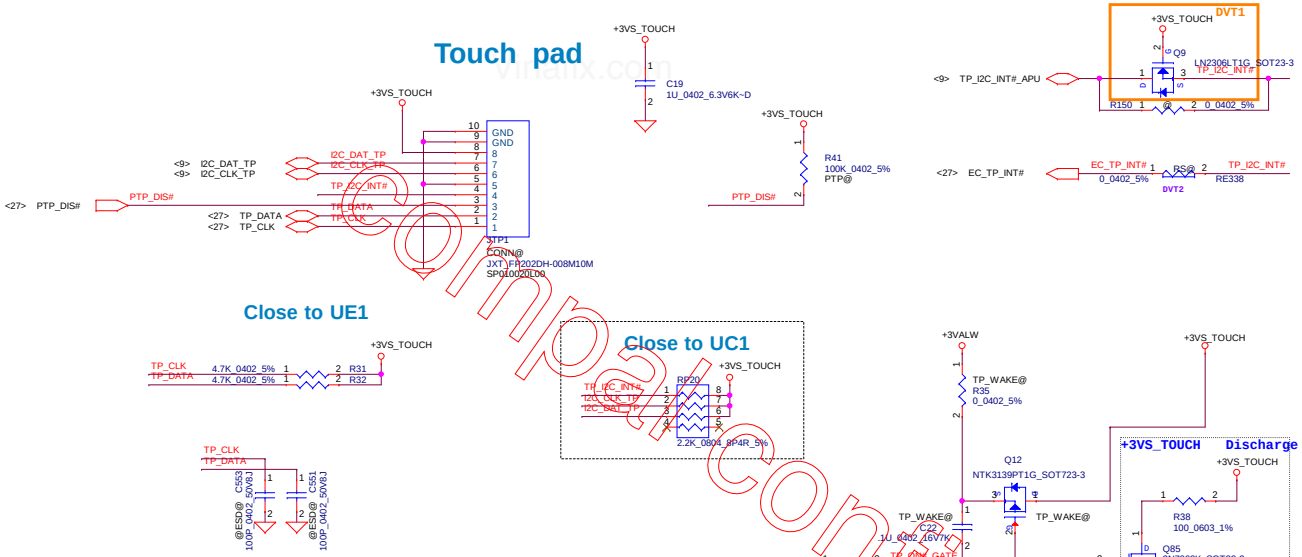
Title: USB3.0

Size: | Document Number: LA-D804P | Rev: 0.1

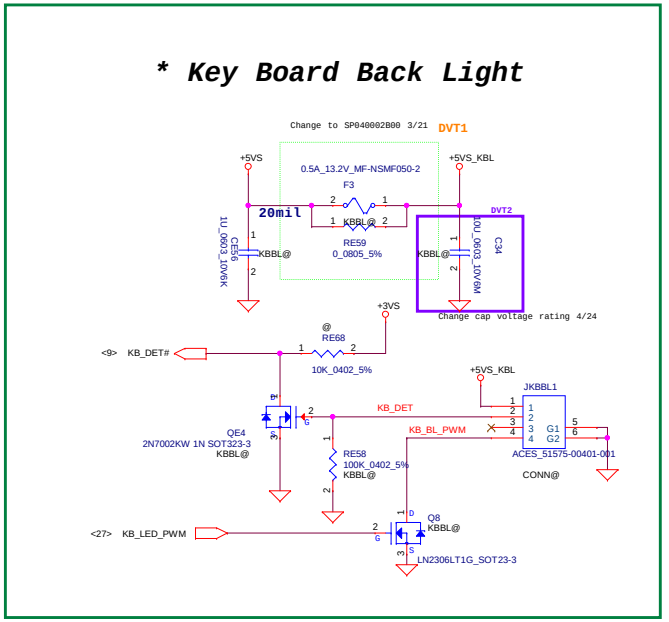
Date: Monday, June 20, 2016 | Sheet 23 of 54

Main Func = Touch Pad

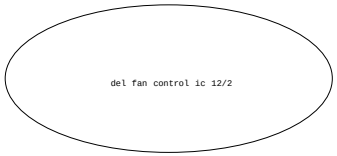
Touch pad

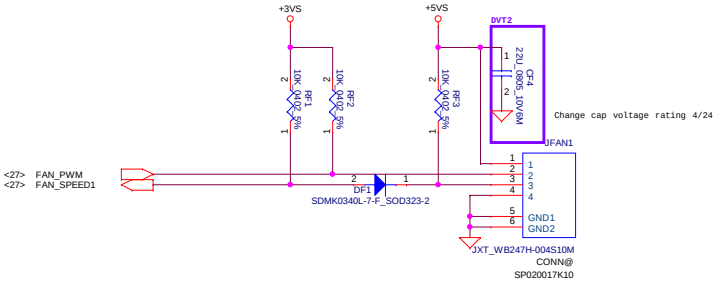


* Key Board Back Light



Main Func = FAN Control

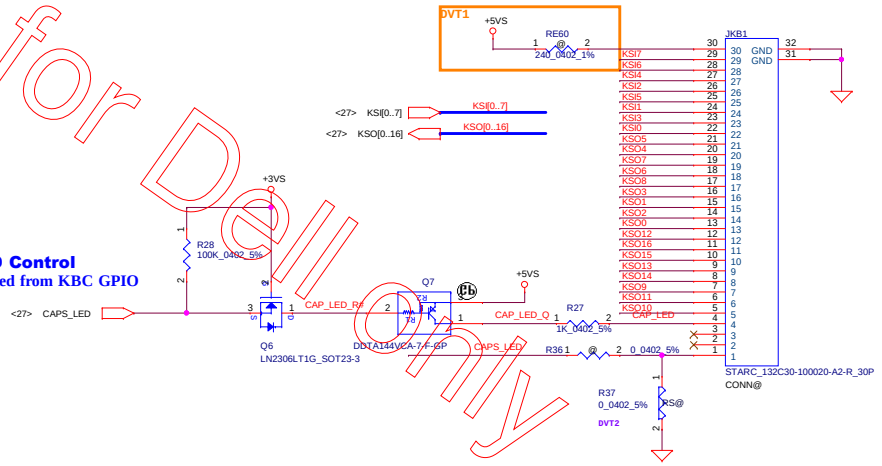




INT_KBD Connector

Main: SP01001H600 (CIS ok)

JKB1 Change footprint to STARC-132C30-100020-A2-R_30P Xbuild 6/14



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

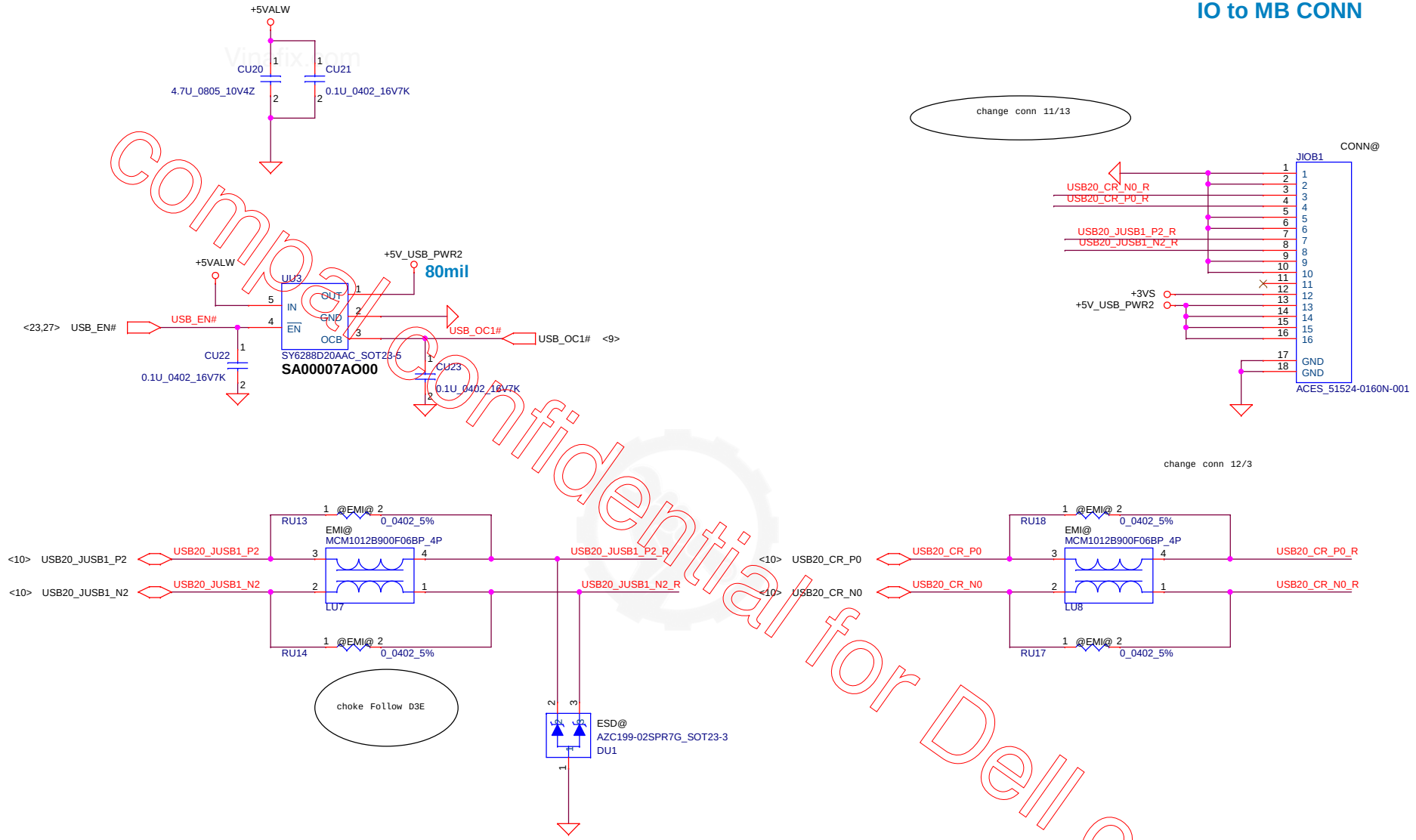
Title: **FAN / TP / PWR SW / KBBL**

Size	Document Number	Rev
	LA-D804P	0.1

Date: Monday, June 20, 2016 Sheet 24 of 54

Main Func = IO Connector

IO to MB CONN



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title	IO-DB	
Size: B	Document Number: LA-D804P	Rev: 0.1
Date: Monday, June 20, 2016	Sheet 25 of 54	

Main Func = DC Interface

+5VS and +3VS switch

SHORT

Max:7.0A

10mil

EM5209VF DFN 14P DUAL LOAD SW

SA00007PM00

Change cap voltage rating 4/24

+3VS to +3VGS
+1.8V_ALW to +1.8VS

2000mA

20mil(0.5A)

EM5209VF DFN 14P DUAL LOAD SW

SA00007PM00

modify on 3/16

For Test,
APE8937(SA000070L00)
AOZ1336(SA00006U600)
TPS22967(SA000070S00)

100mil(1.5A)

SY6288C20AAC_SOT23-5

Max:5.07A

SHORT

10mil

EM5209VF DFN 14P DUAL LOAD SW

SA00007PM00

Change cap voltage rating 4/24

1500mA

Change Cap. voltage rating 4/24

del reserve circuit 12/2

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

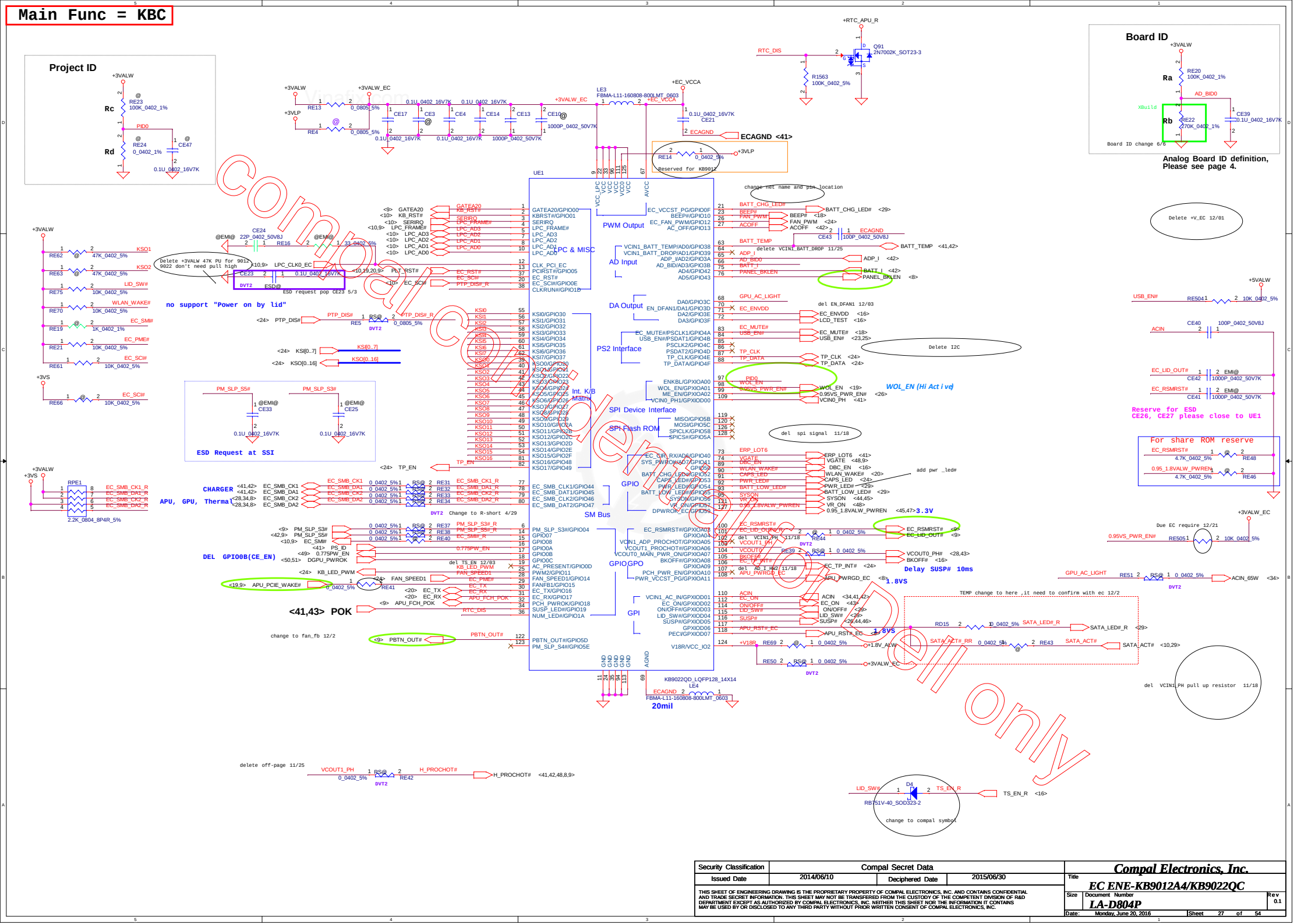
Compal Electronics, Inc.

Title: DC/DC Interface

Size: | Document Number: LA-D804P | Rev: 0.1

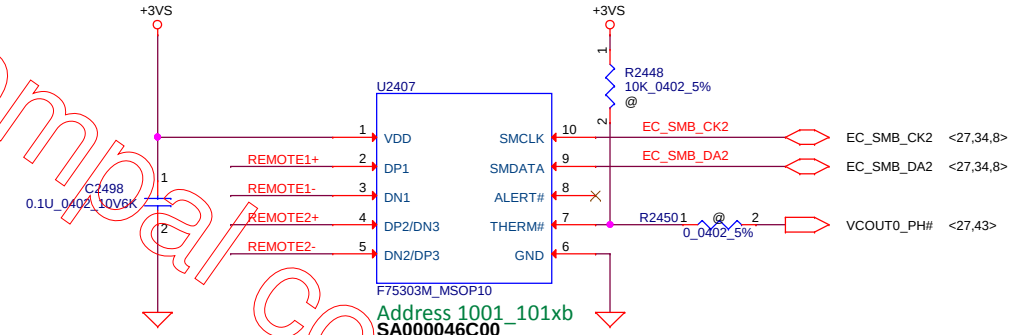
Date: Monday, June 20, 2016 | Sheet 26 of 54

Main Func = KBC



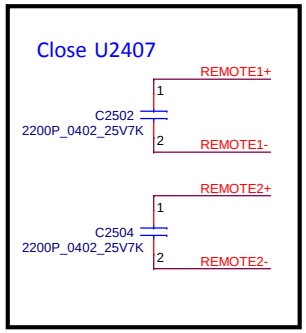
Main Func = Thermal Sensor

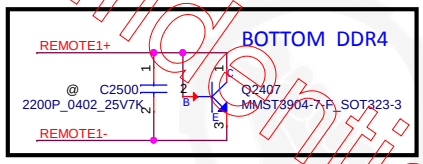
Fintek thermal sensor
placed near by TOP DDR4

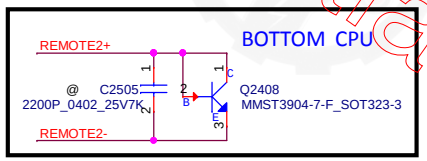


Address 1001_101xb
SA000046C00

2nd source
SA000029210 ->EMC1403-2-AIZL-TR







REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

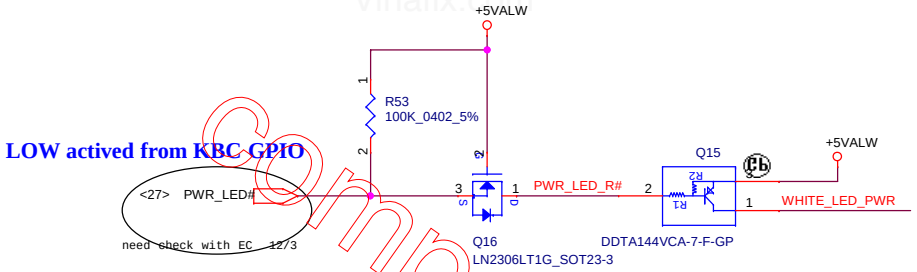
Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

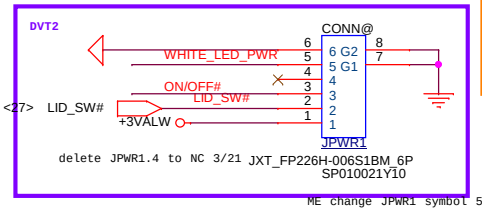
Compal Electronics, Inc.

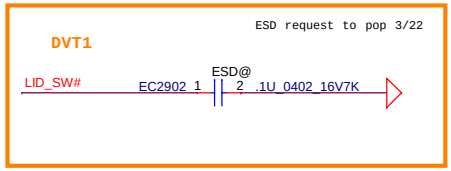
Title	Thermal Sensor	
Size	Document Number LA-D804P	Rev 0.1
Date: Monday, June 20, 2016	Sheet 28 of 54	

Main Func = POWER BTN

Power button

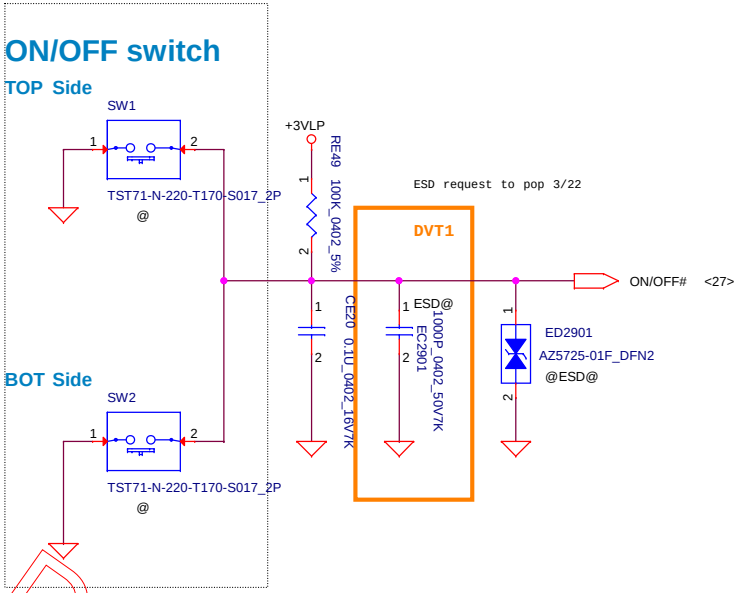






Pop only before MP

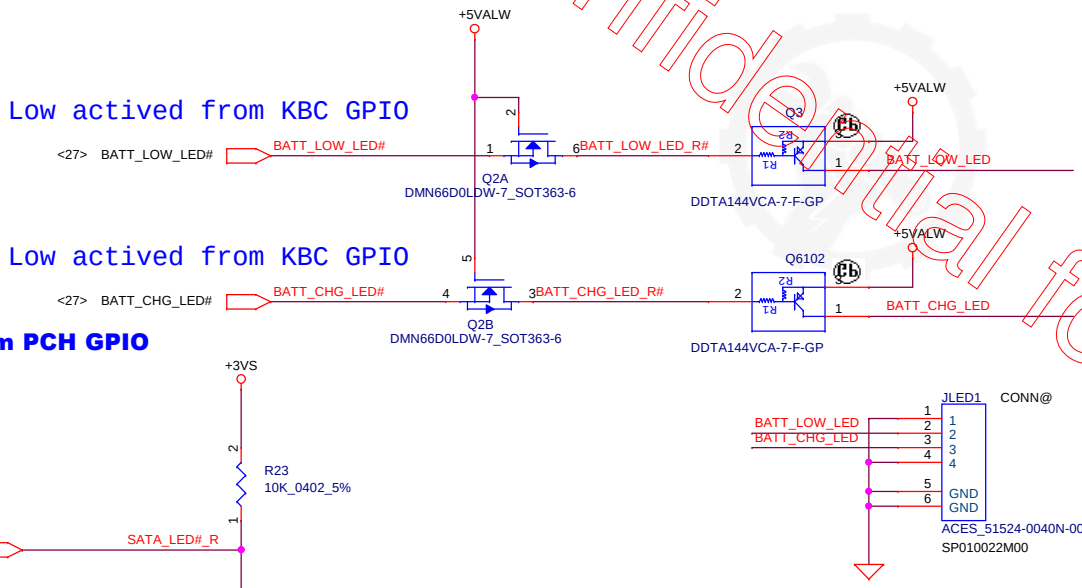
ON/OFF switch



SW1/SW2 Change to SN10000B310

EC2901 must be used 1000pF.

Main Func = Battery BTN



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: **Reserved Page**

Size | Document Number: **LA-D804P** | Rev: 0.1

Date: Monday, June 20, 2016 | Sheet 29 of 54

Main Func = Screw Hole

DVT1

ZZZ

Part Number	Description
DA6001LB000	PCB 1PG LA-D804P REV0 MB 5

PCB_R1@

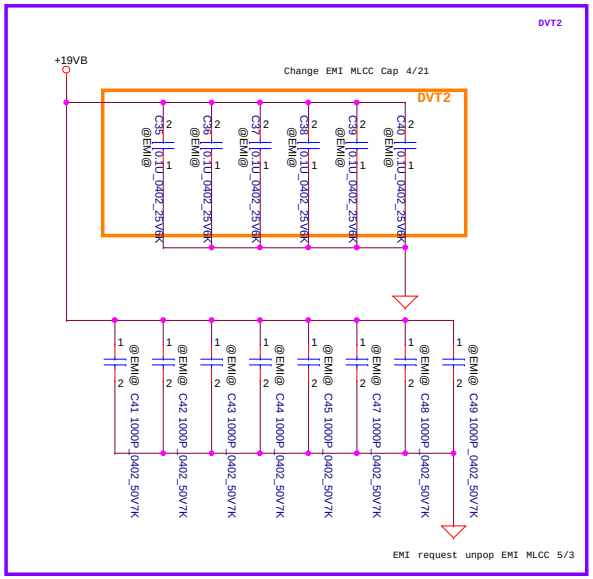
ZZZ

Part Number	Description
DA6001LB011	PCB 1PG LA-D804P REV1 MB GOLD 5 A31 !

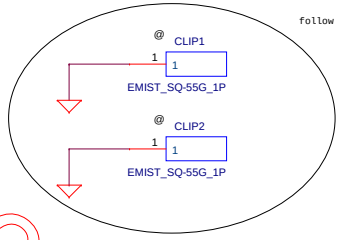
PCB_R3@

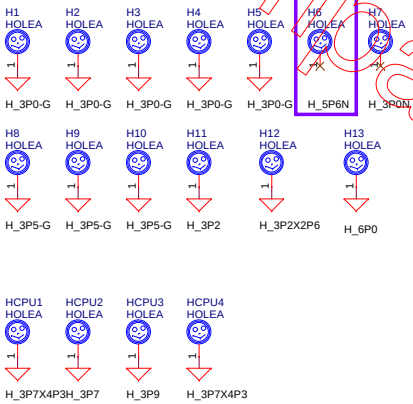
Follow EMC require add cap around +19VB 11/25

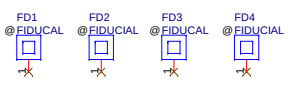
need to place separately



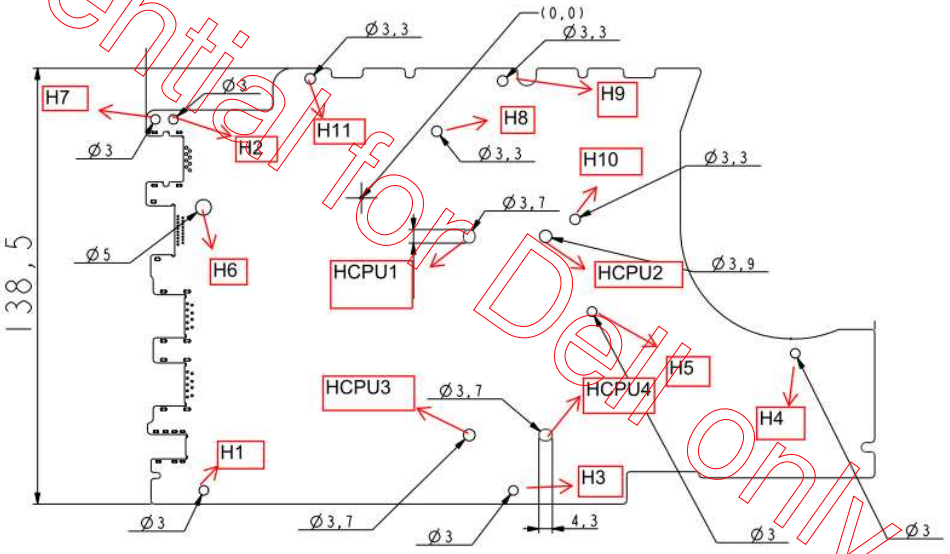
follow EMI require 12/15







del FD5 FD6 12/1



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: **Screw Hole**

Size | Document Number: **LA-D804P** | Rev: 0.1

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SSID1 = TPM2.0

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	2015/07/21

Compal Electronics, Inc.

Title	TPM	
Size: Custom	Document Number: LA-D804P	Rev: 0.1
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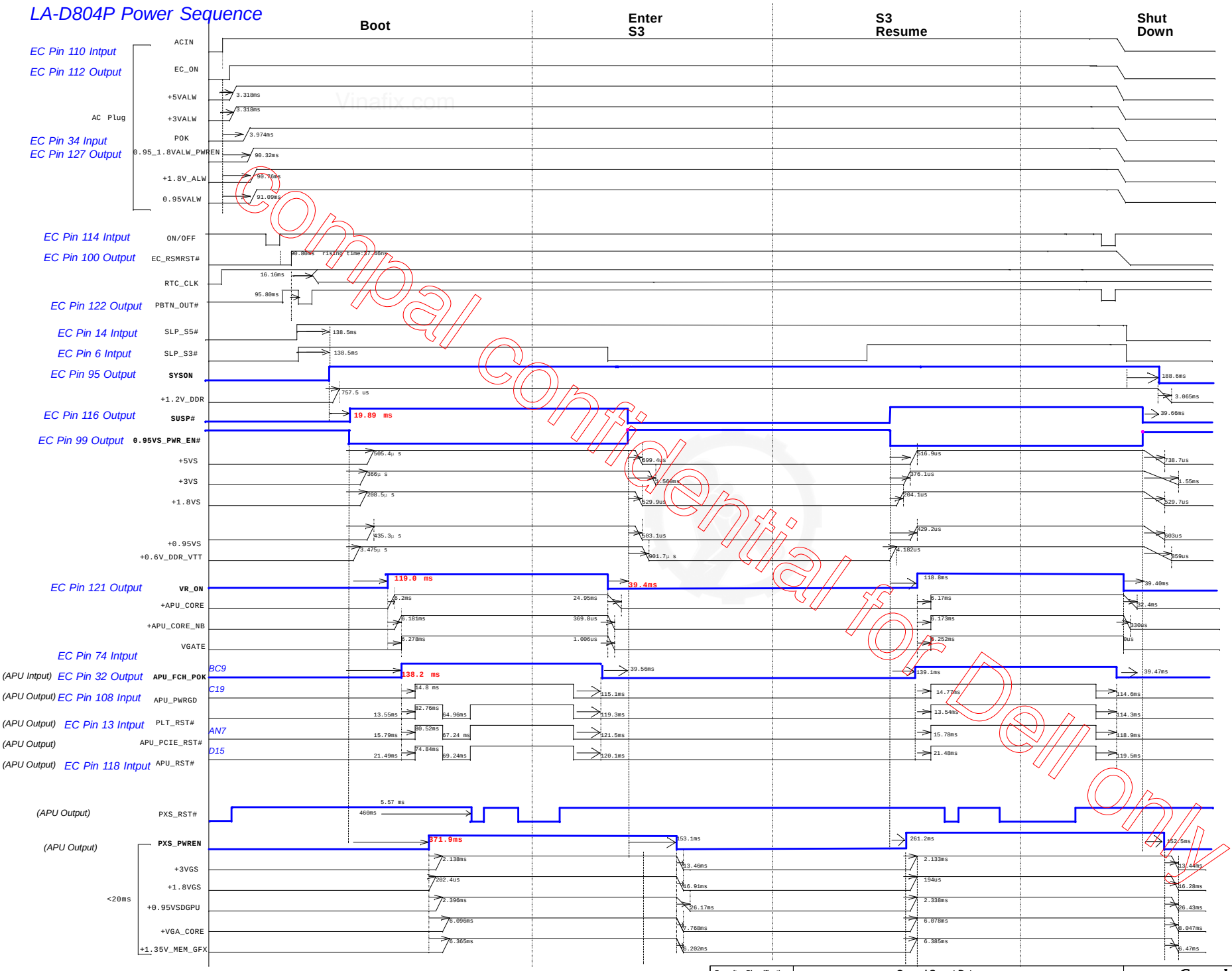
LA-D804P Power Sequence



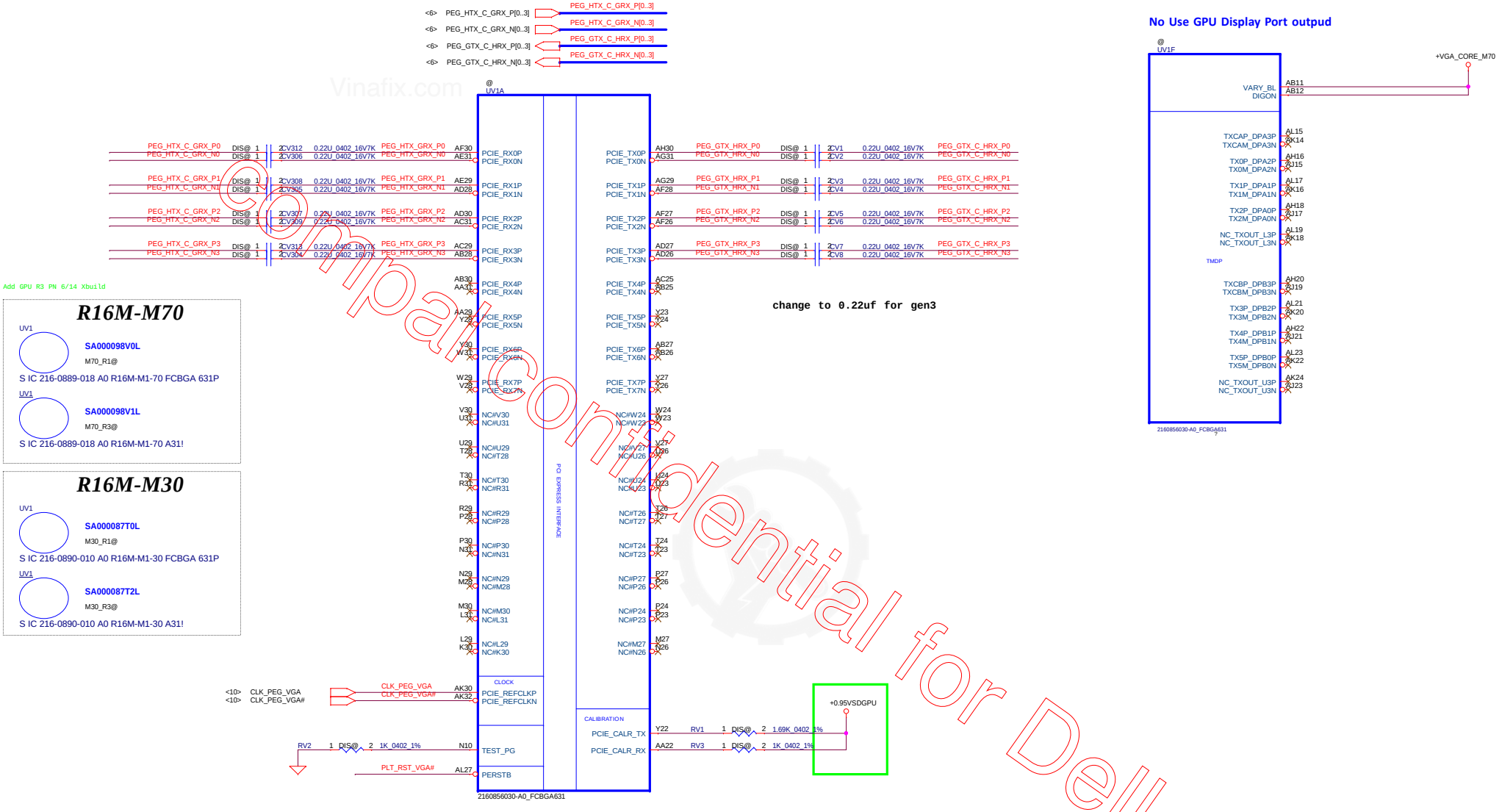
Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: **Power Sequence Timing**

Size	Document Number	Rev
	LA-D804P	0.1

Date: Monday, June 20, 2016 | Sheet 32 of 54



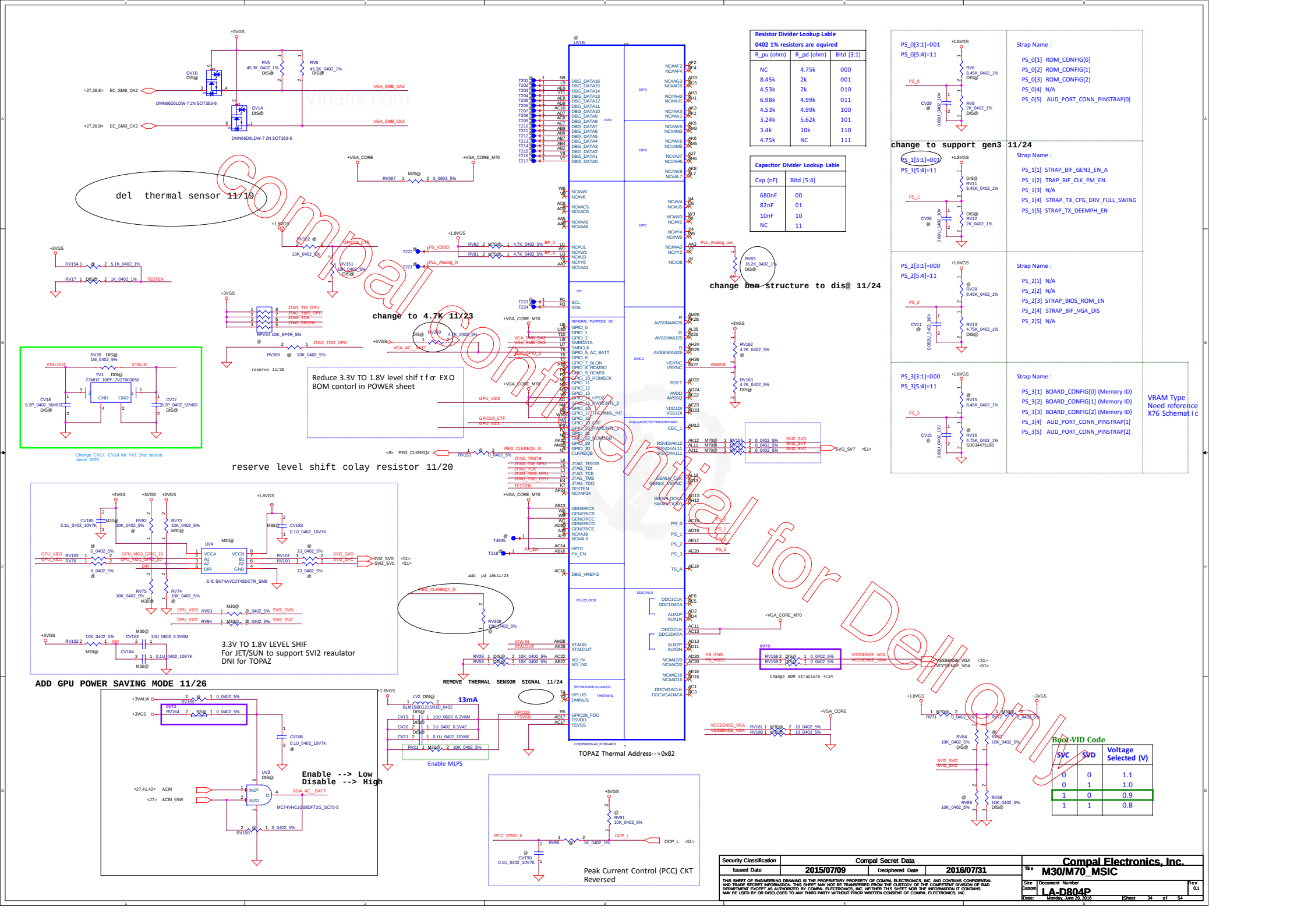
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: M30/M70_PCIE/DP

Size: Custom | Document Number: LA-D804P | Rev: 0.1

Date: Monday, June 20, 2016 | Sheet 33 of 54



Resistor Divider Lookup Lable

0402 1% resistors are equired

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

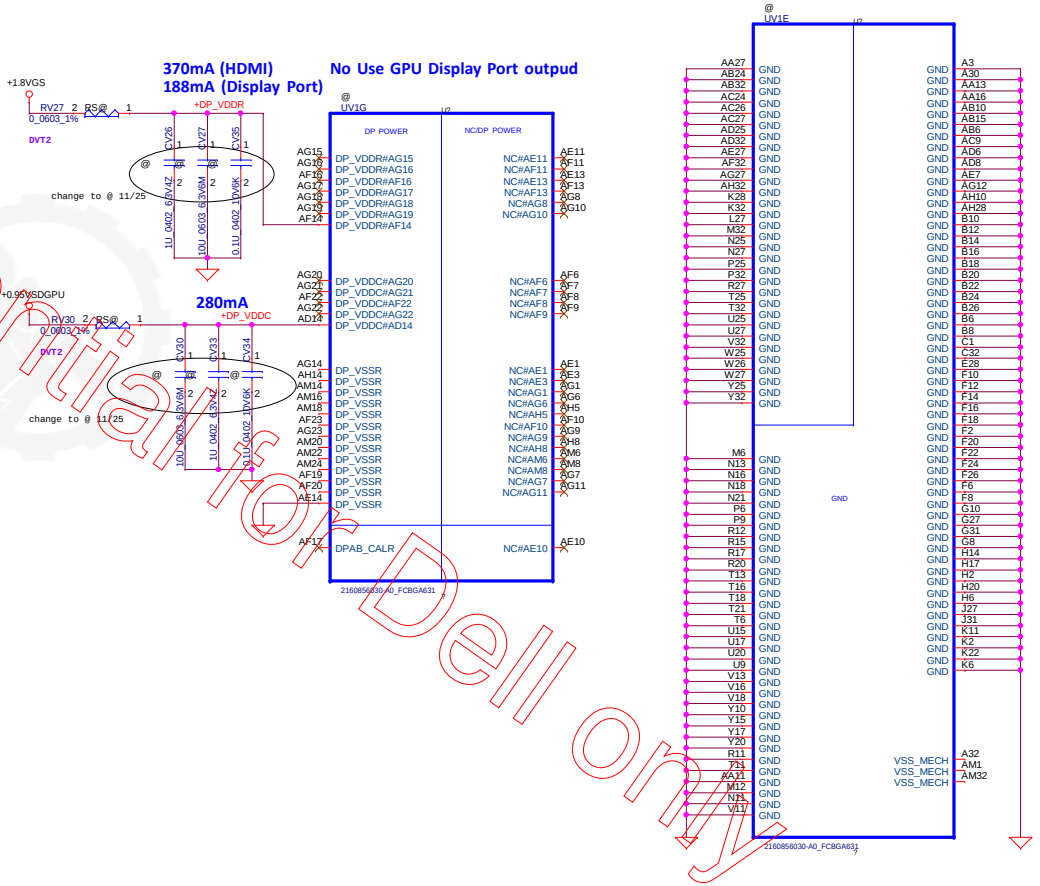
PS_0[3:1]=001 PS_0[5:4]=11	Strap Name : PS_0[1] ROM_CONFIG[0] PS_0[2] ROM_CONFIG[1] PS_0[3] ROM_CONFIG[2] PS_0[4] N/A PS_0[5] AUD_PORT_CONN_PINSTRAP[0]
PS_1[3:1]=001 PS_1[5:4]=11	Strap Name : PS_1[1] STRAP_BIF_GEN3_EN_A PS_1[2] TRAP_BIF_CLK_PM_EN PS_1[3] N/A PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING PS_1[5] STRAP_TX_DEEMPH_EN
PS_2[3:1]=000 PS_2[5:4]=11	Strap Name : PS_2[1] N/A PS_2[2] N/A PS_2[3] STRAP_BIOS_ROM_EN PS_2[4] STRAP_BIF_VGA_DIS PS_2[5] N/A
PS_3[3:1]=000 PS_3[5:4]=11	Strap Name : PS_3[1] BOARD_CONFIG[0] (Memory ID) PS_3[2] BOARD_CONFIG[1] (Memory ID) PS_3[3] BOARD_CONFIG[2] (Memory ID) PS_3[4] AUD_PORT_CONN_PINSTRAP[1] PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title	M30/M70_MSIC		
Size	Document Number		Rev
Custom	LA-D804P		0.1
Date:	Monday, June 20, 2016	Sheet	34 of 54



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: M30/M70_Power/GND

Size: Custom | Document Number: LA-D804P | Rev: 0.1

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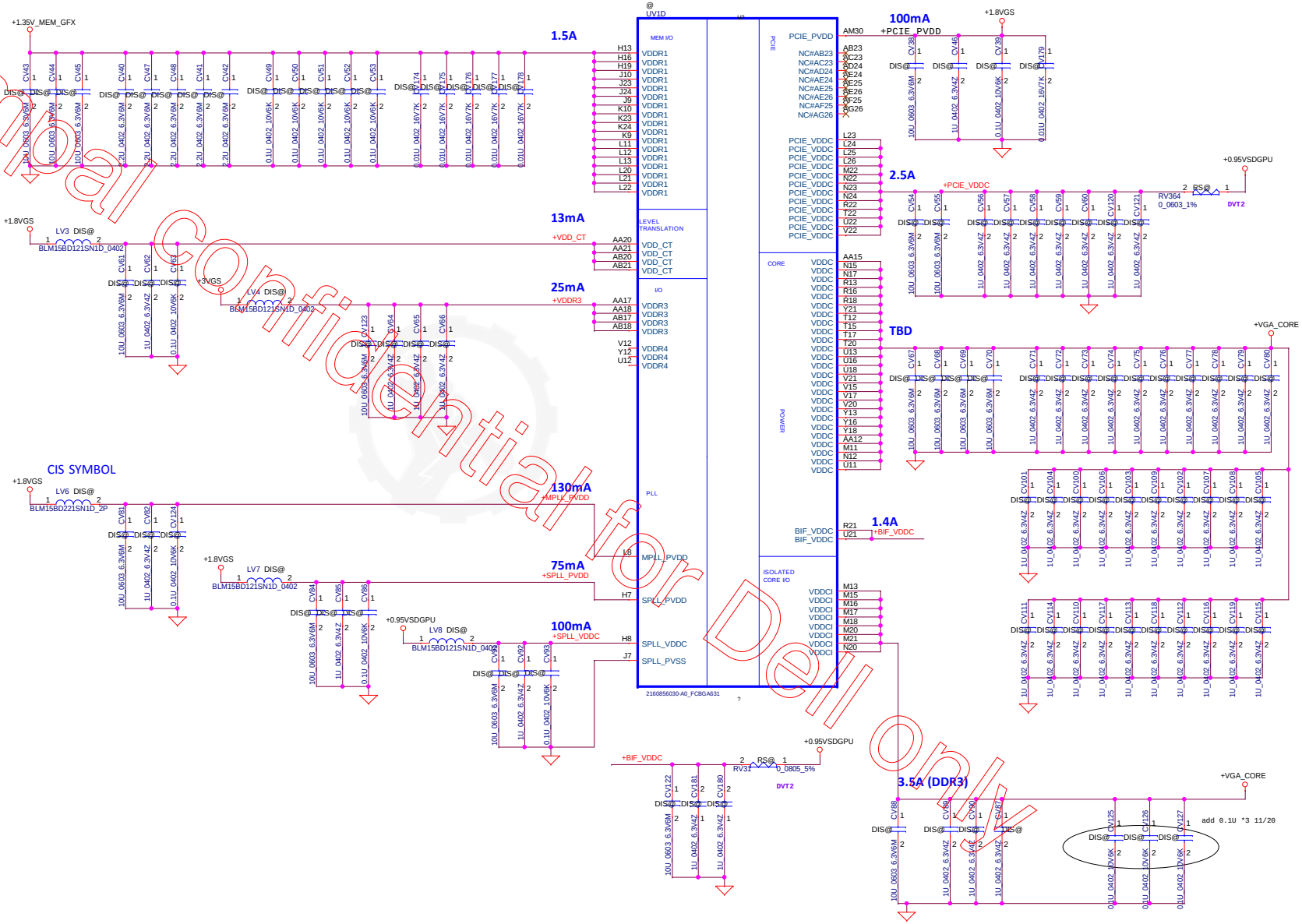
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VSDGPU		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	1	0
SPLL_VDDC	100mA	1	1	1

+1.5V_MEM_GFX		10uF	2.2uF	0.1uF	0.01uF
VDDR1	1.5A	3	5	5	5

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



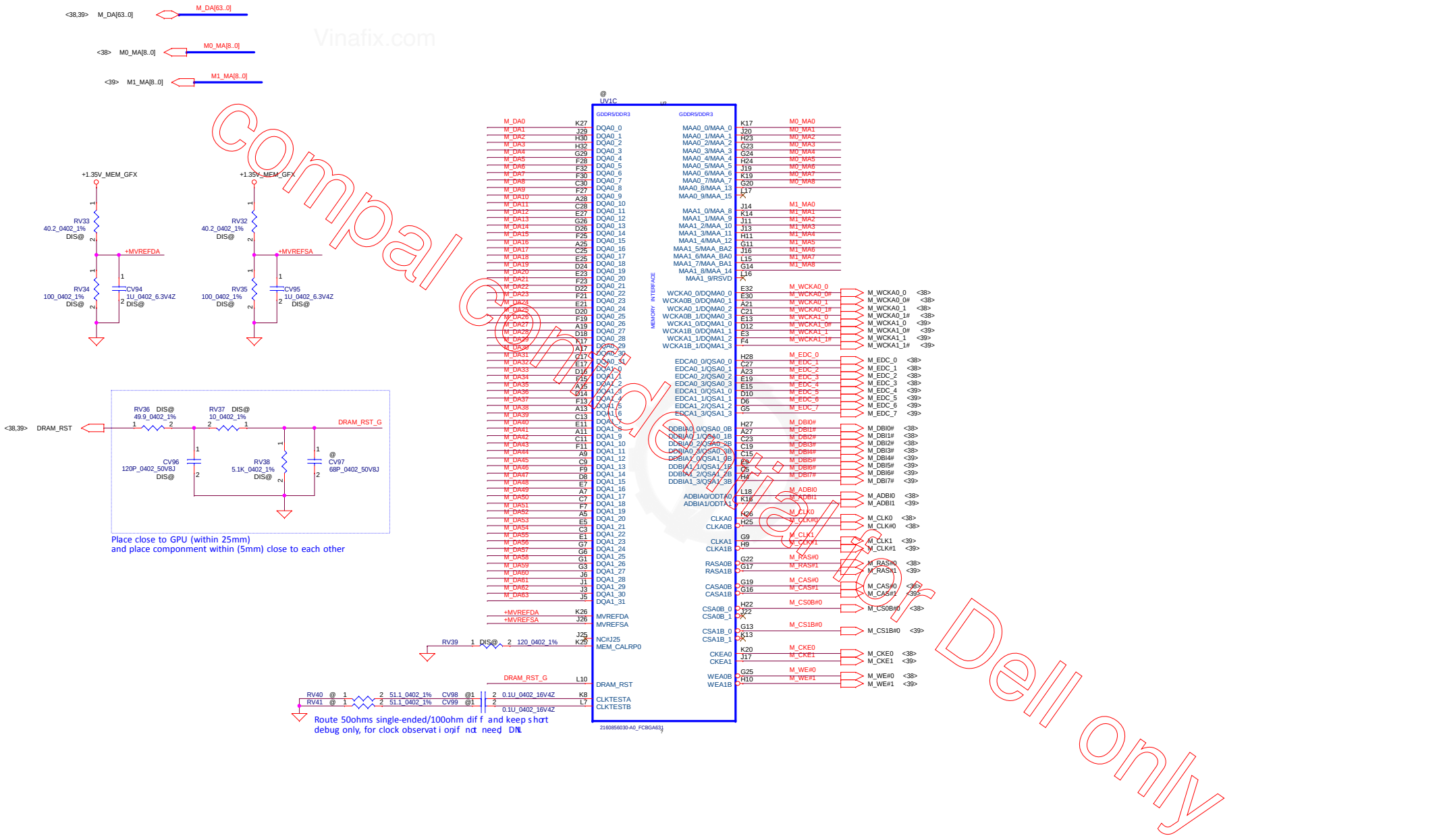
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: M30/M70_Power

Size: Custom | Document Number: LA-D804P | Rev: 0.1

Date: Monday, June 20, 2016 | Sheet 36 of 54



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: **M30/M70_MEM**

Size	Document Number	Rev
Custom	LA-D804P	0.1

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clamshell configuration 11/26

VRAM R1 PN	VRAM R3 PN
UV13 SA000092D0L S2G_R1@	UV13 SA000094R1L S2G_R3@
S IC D5 256M32 K4G80325FB-HC28 FBGA 170P	S IC D5 256M32 K4G80325FB-HC03 FBGA A31!
UV13 SA00009U10L H2G_R1@	UV13 SA00009U11L H2G_R3@
S IC D5 256M32 H5GC8H24MJR-R0C BGA 170P	S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!
UV13 SA00009TV0L M2G_R1@	UV13 SA00009TV1L M2G_R3@
S IC D5 256M32 MT51J256M32HF-70:A FBGA	S IC D5 256M32 MT51J256M32HF-70:A A31!

del cap 11/24

Stitching Caps OPTION for MEM signals that have a change of reference plane voltage
Add stitching caps when required, one cap per three signals

SAM 4G 11/17

MF=0

170-BALL SGRAM GDDR5 H5GC4H24AJR-R0C_BGA170

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

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Compal Electronics, Inc.

Title: GDDR5_A0

Size: | Document Number: LA-D804P | Rev: 0.1

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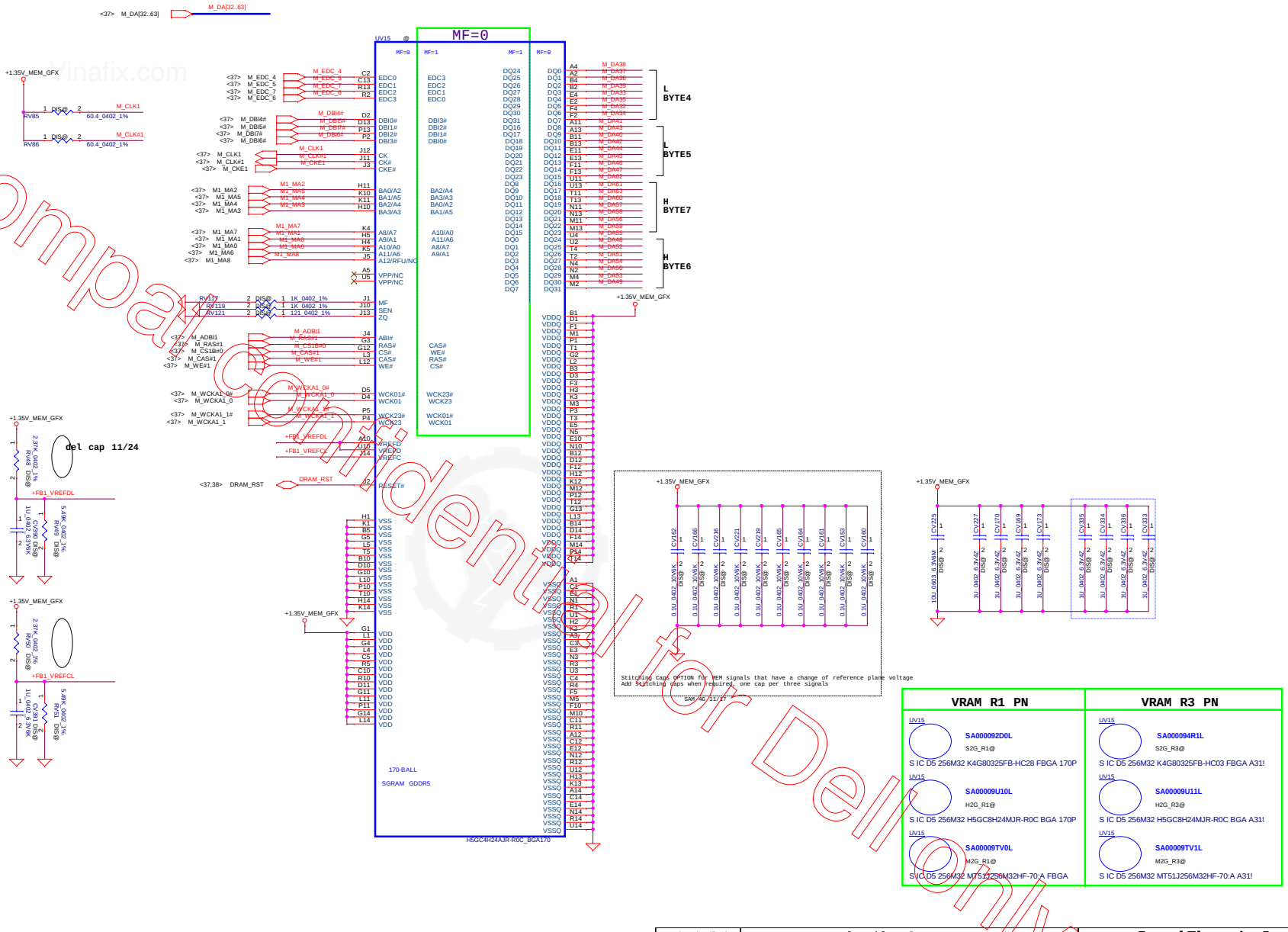
clamshell configuration 11/26



Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title	GDDR5_B0		
Size	Document Number	LA-D804P	Rev 0.1
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Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µ s

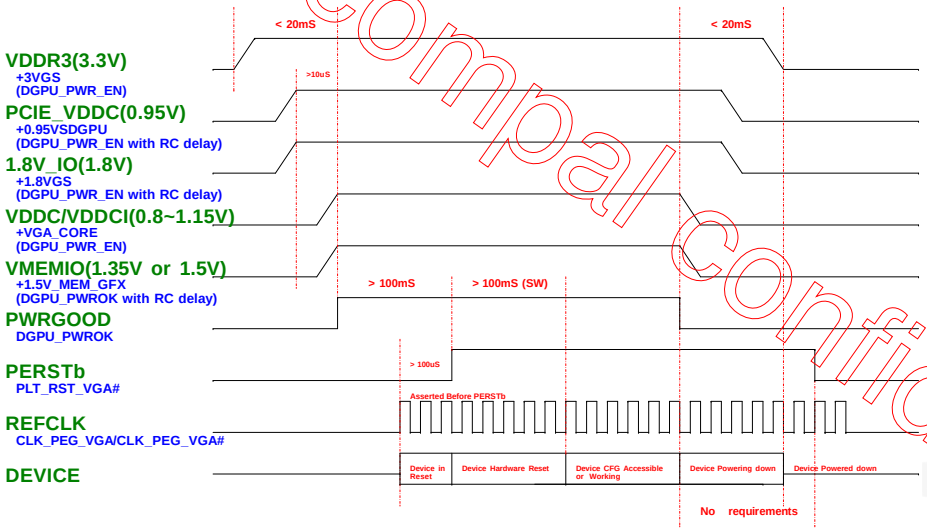
2. It is recommended that the 3.3-V rail ramp up first.

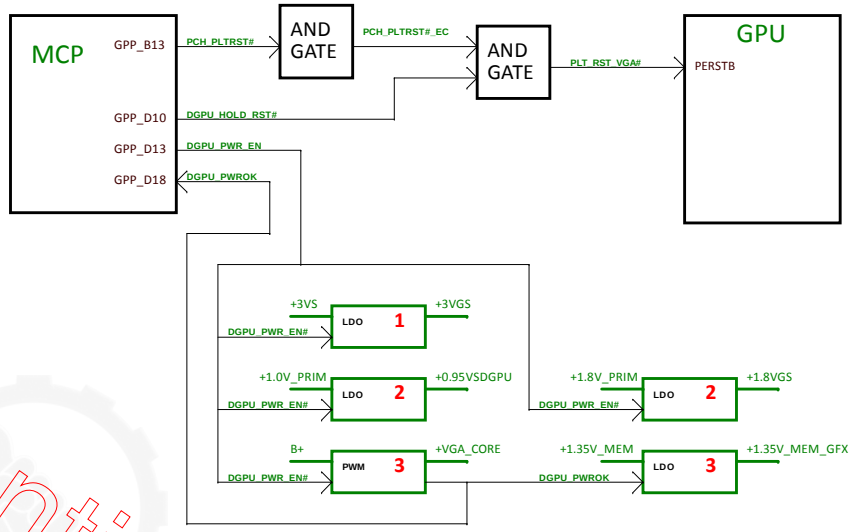
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.

4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/µ s).

5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

6. For power down, reversing the ramp-up sequence is recommended.





SAMSUNG 2G (000)	HYNIX 2G (110)	MICRON 2G (111)
RV16 2G_S@ 4.75K_0402_1% SD034475180	RV15 2G_H@ 3.4K_0402_1% SD034340180 / RV16 2G_H@ 10K_0402_1% SD034100280	RV15 2G_M@ 4.75K_0402_1% SD034475180

Update on 3/24

Table 3–21 Resistor Divider Lookup T

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

For AMD R16M-M30/M70 VRAM Only

Memory ID	P/N	Vendor	Description	Size
000	SA000092D1L	SAMSUNG	S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	2GB
110	SA00009U10L	Hynix	S IC D5 256M32 H5GC8H24MJR-R0C BGA 170P	2GB
111	SA00009TV0L	Micron	S IC D5 256M32 MT51J256M32HF-70:A FBGA	2GB

Update on 3/24

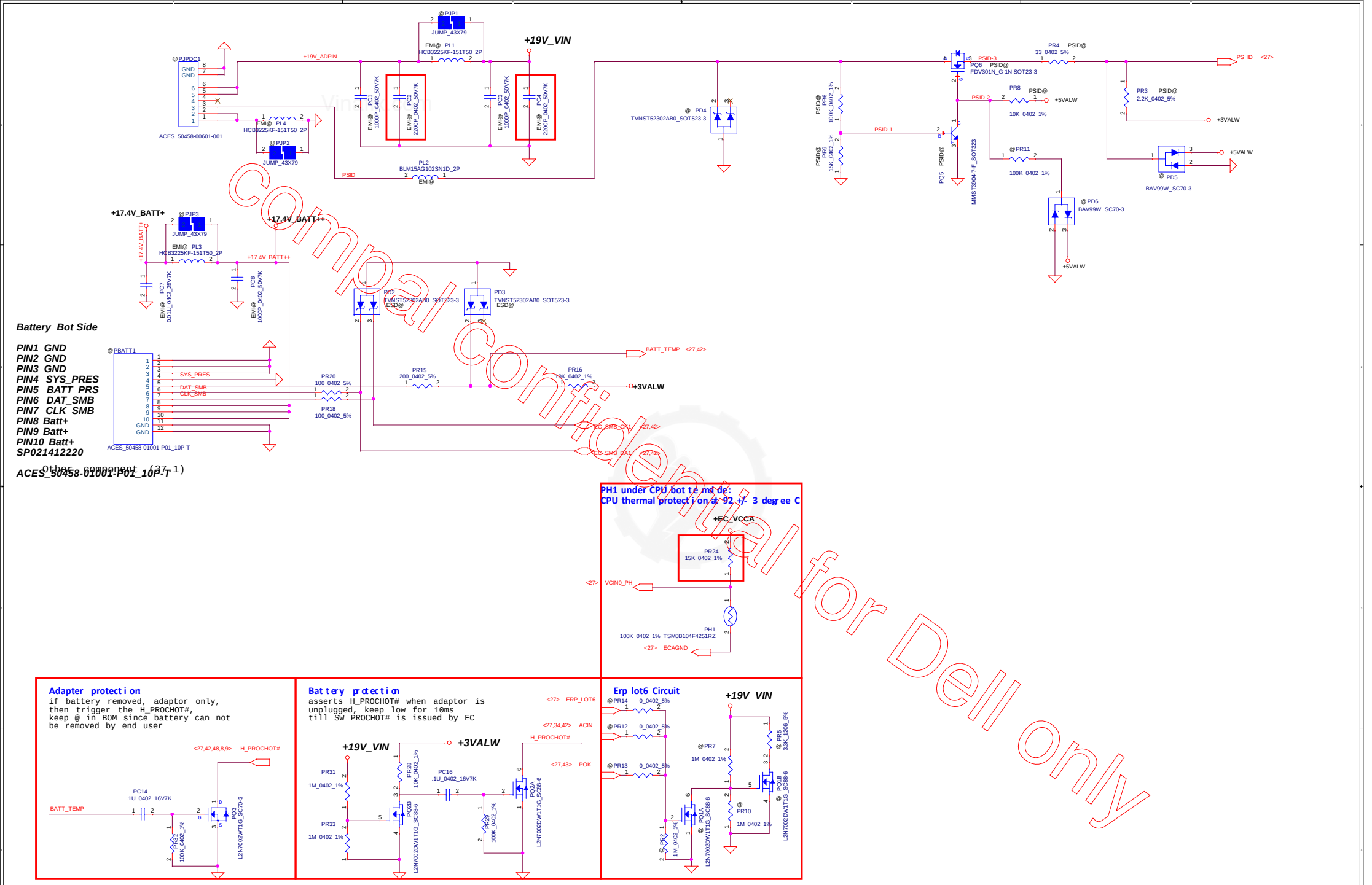
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: M30/M70_NOTE

Size | Document Number: LA-D804P | Rev: 0.1

Date: Monday, June 20, 2016 | Sheet 40 of 54



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Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.			
Title	PWR_DCIN/BATT CONN/OTP		
Size	Document Number		Rev X01(0.2)
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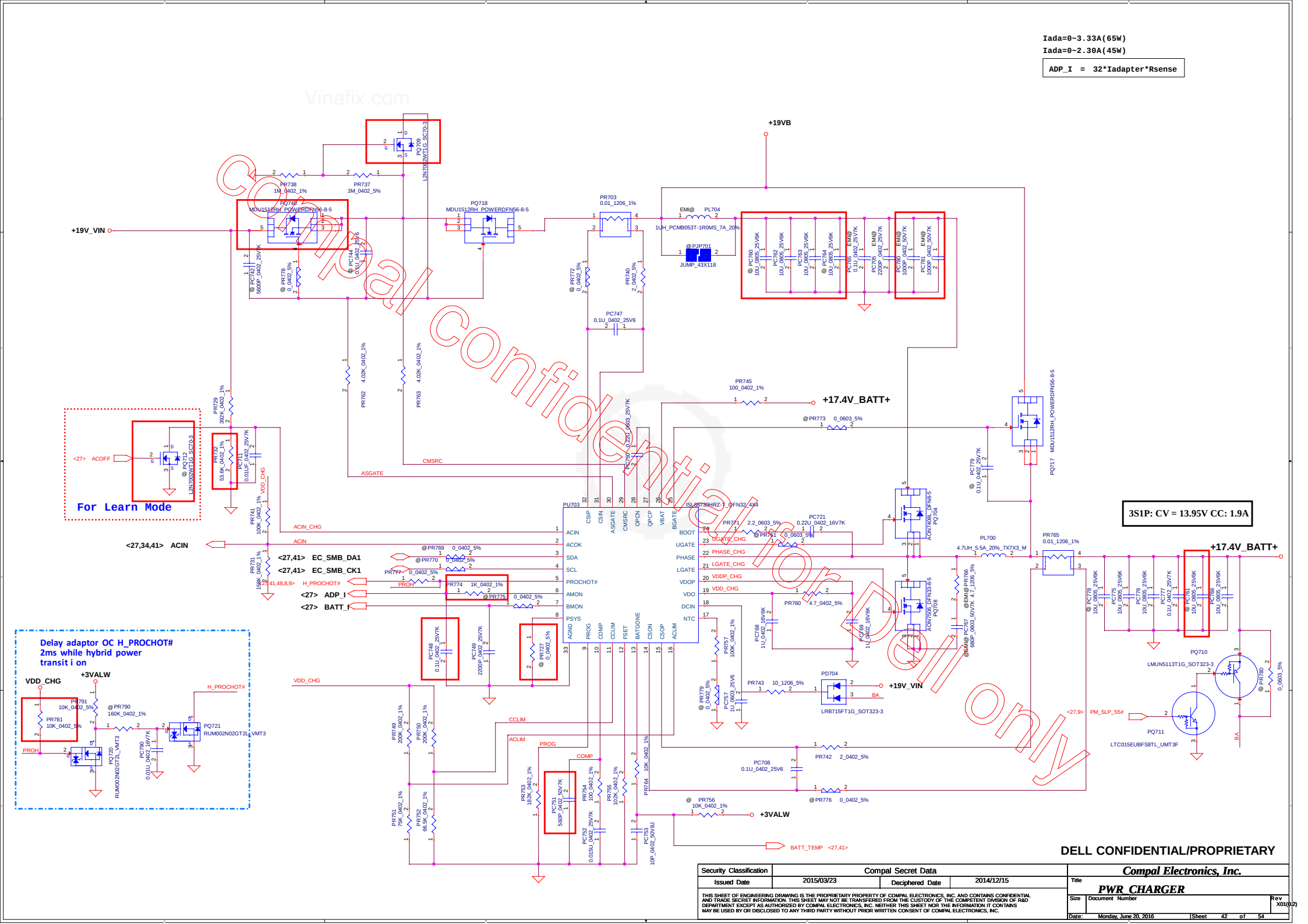
Iada=0~3.33A(65W)
Iada=0~2.30A(45W)

ADP_I = 32*Iadapter*Rsense



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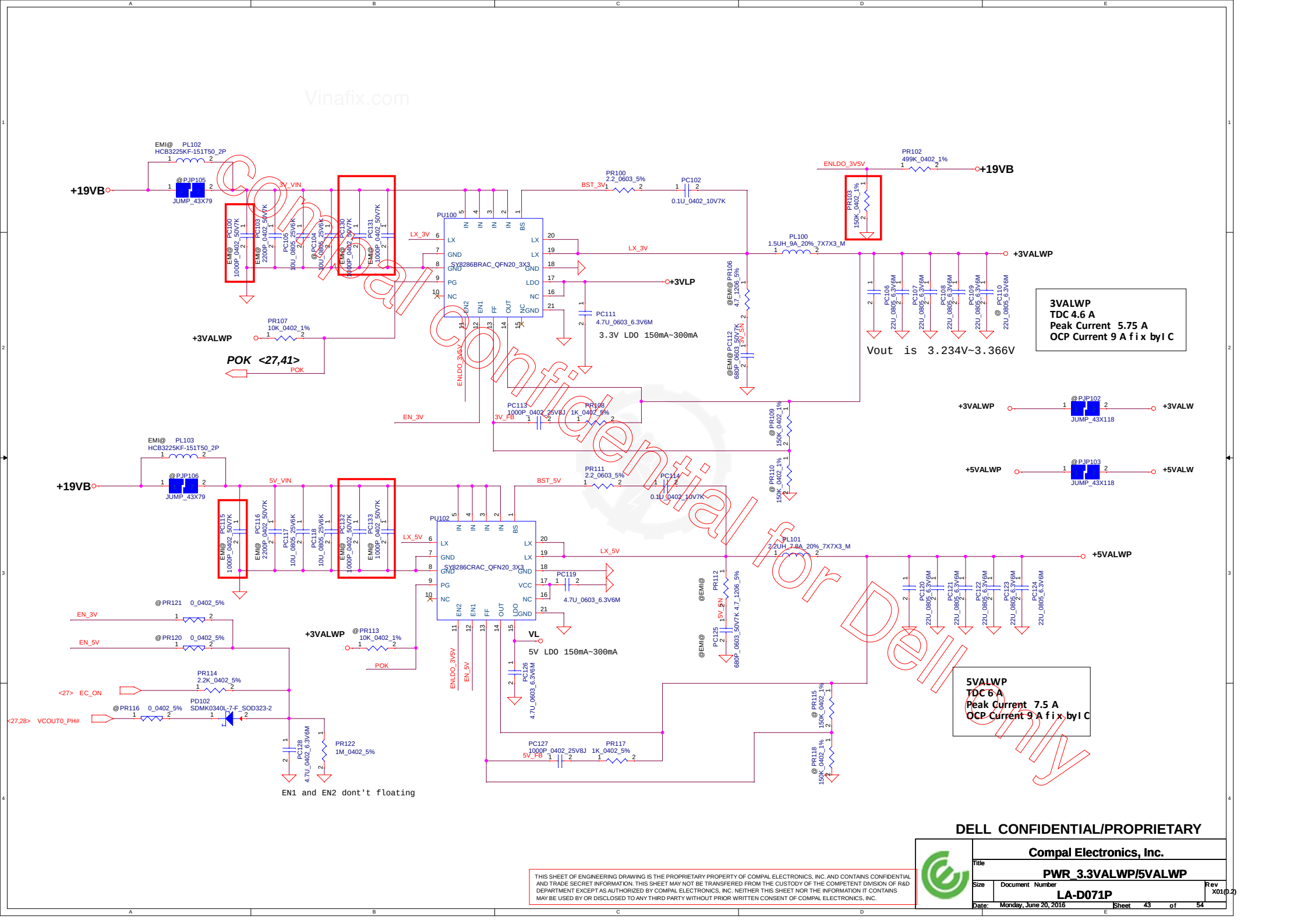
Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.			
Title	PWR_CHARGER		
Size	Document Number		Rev X01(0.2)
Date: Monday, June 20, 2016		Sheet 42 of 54	

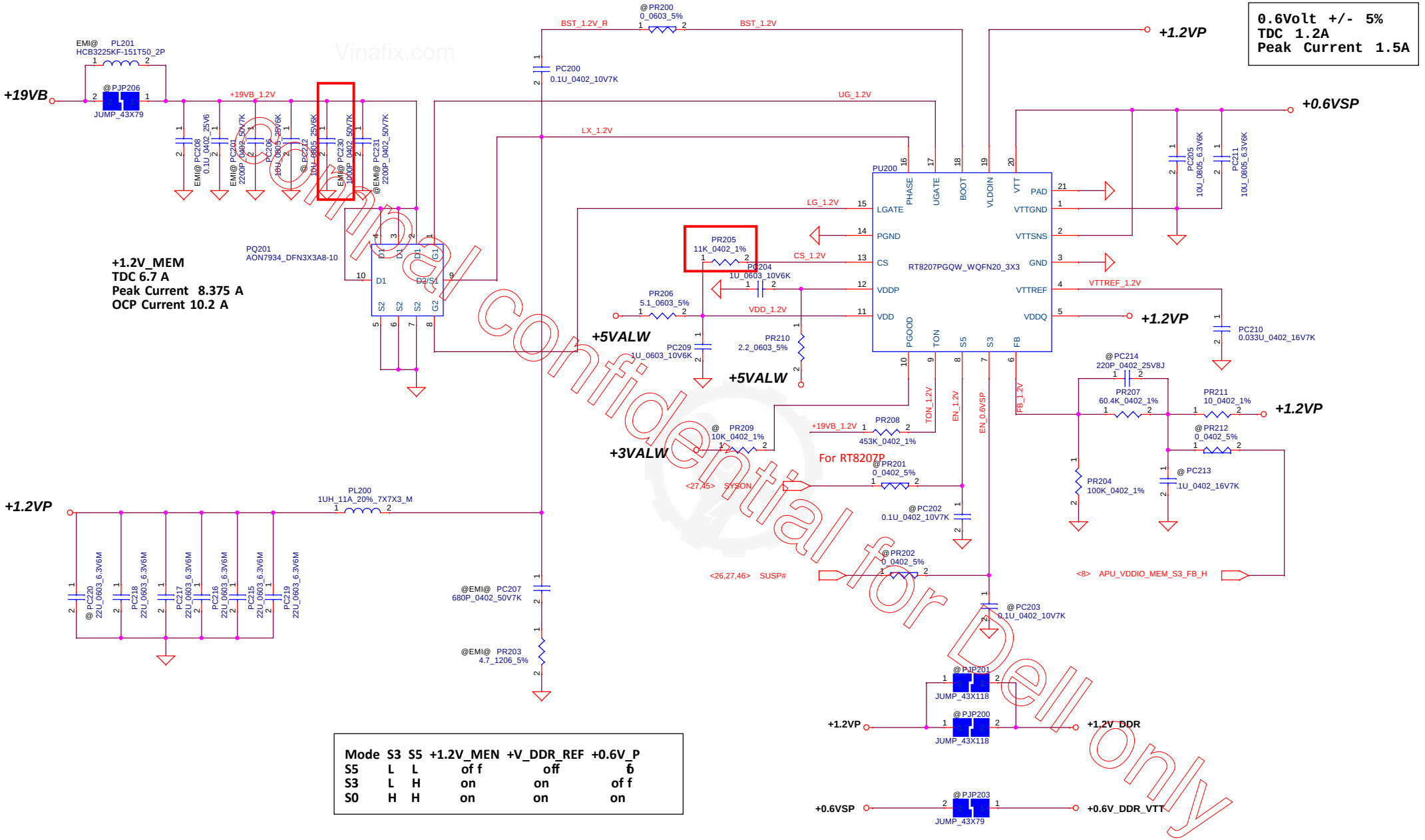


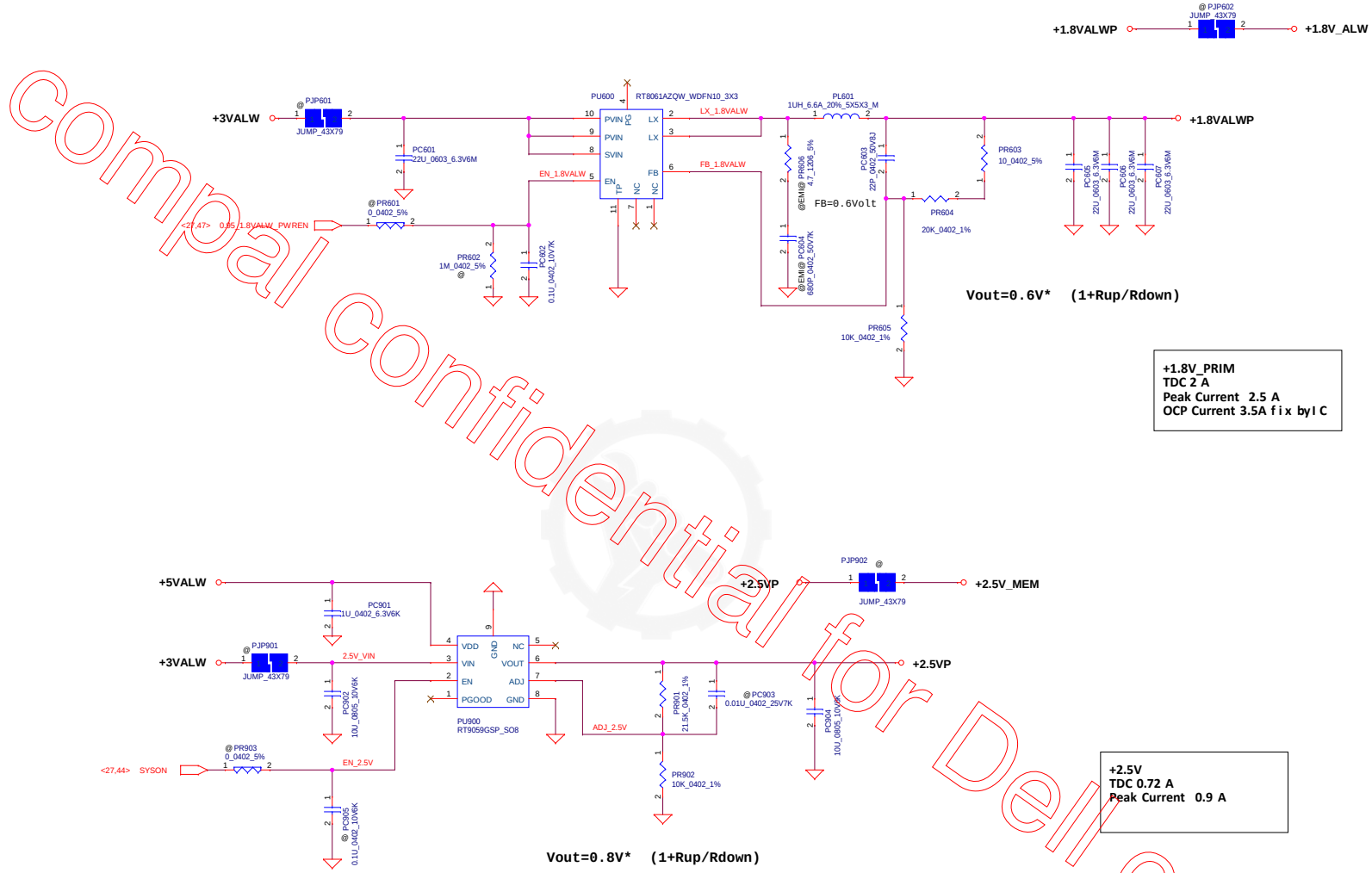
Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size | Document Number: LA-D071P | Rev: X01(0.2)

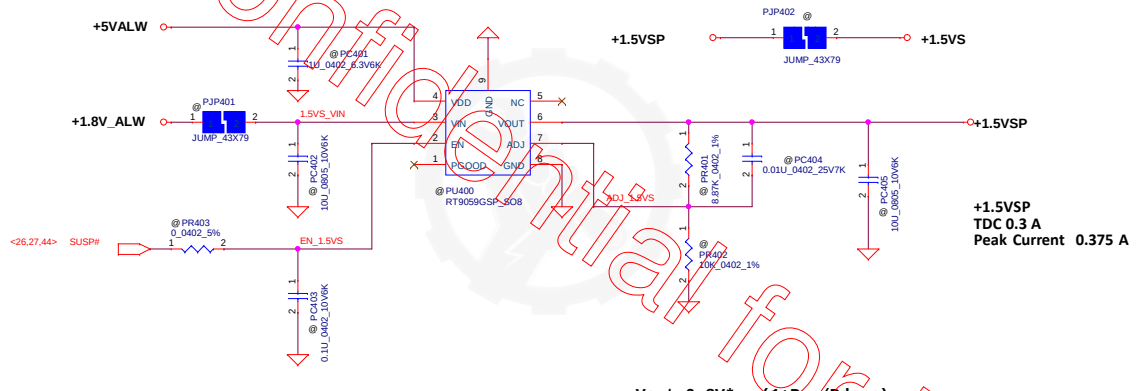
Date: Monday, June 20, 2016 | Sheet 43 of 54





Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.			
Title	PWR_+1.8V_PRIM and +2.5V		
Size C	Document Number		Rev X01(0.2)
Date: Monday, June 20, 2016		Sheet 45 of 54	



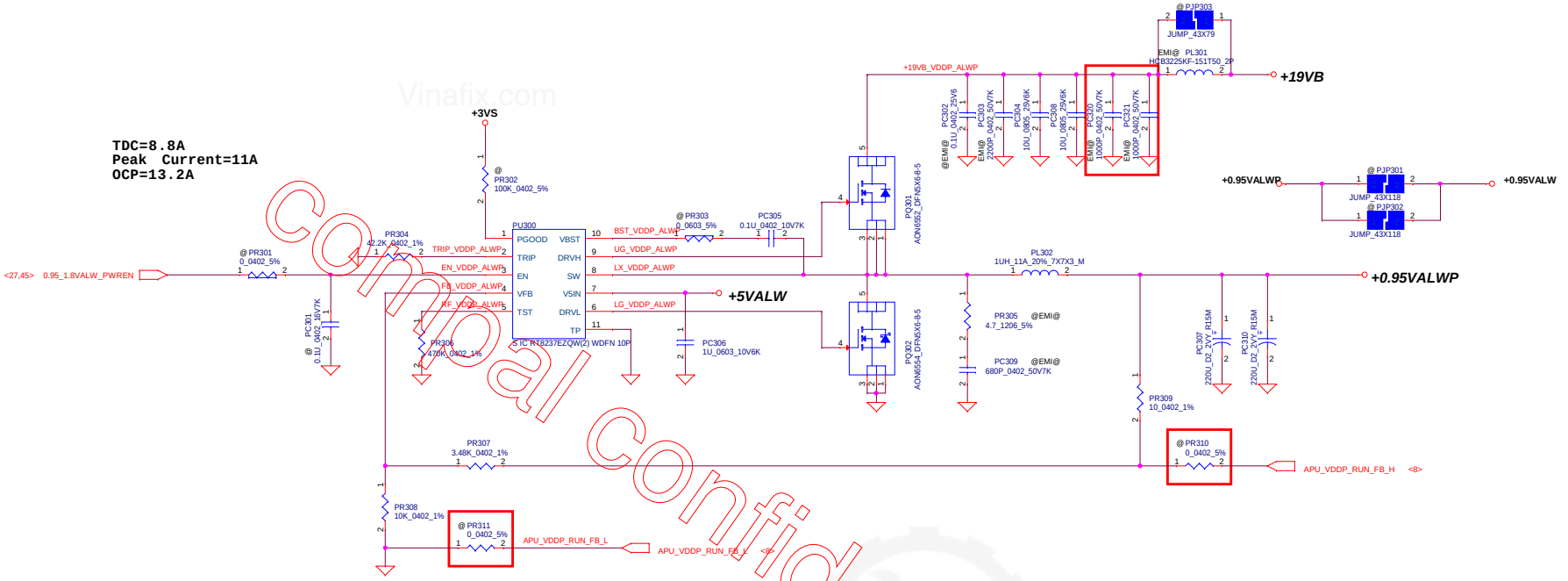
Security Classification	Compal Secret Data		
Issued Date	2014/03/31	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **PWR_1.5VSP**

Size	Document Number	Rev
		0.1

Date: Monday, June 20, 2016 | Sheet 46 of 54



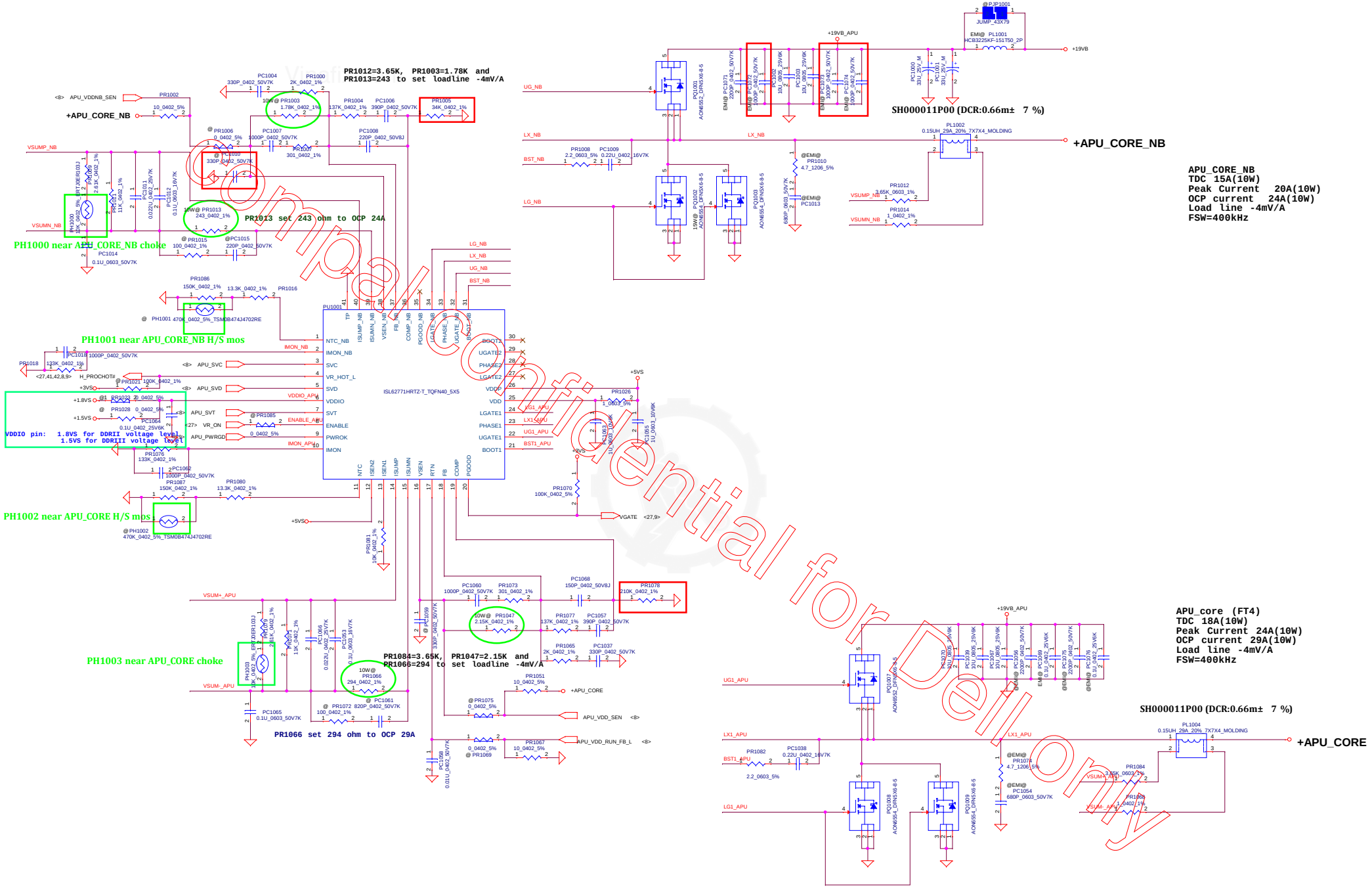
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: P45-PWR_VDDP_ALWP(+0.95V)

Size	Document Number	Rev
C		1.0

Date: Monday, June 20, 2016 Sheet 47 of 54



Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

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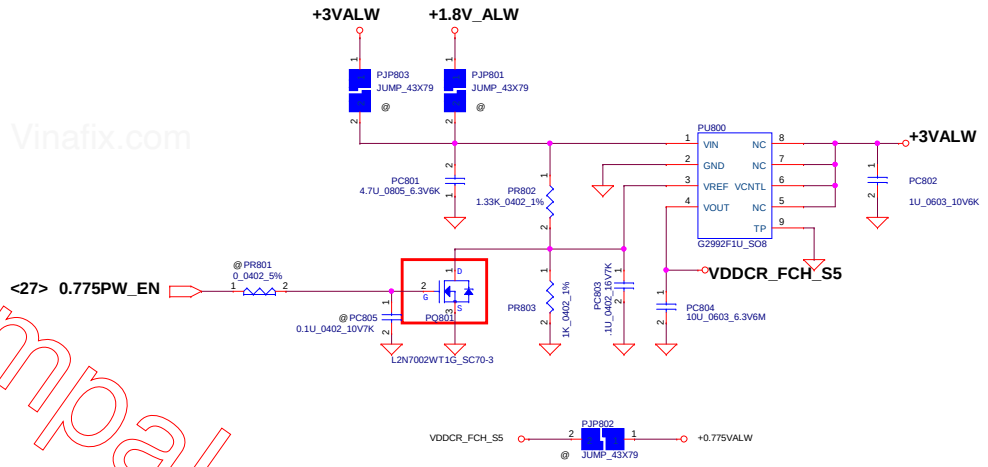
Compal Electronics, Inc.	
Title	PWR_APU_CORE/APU_CORE_NB
Size: Custom	Document Number: Rev 0.1
Date: Monday, June 20, 2016	Sheet 48 of 54



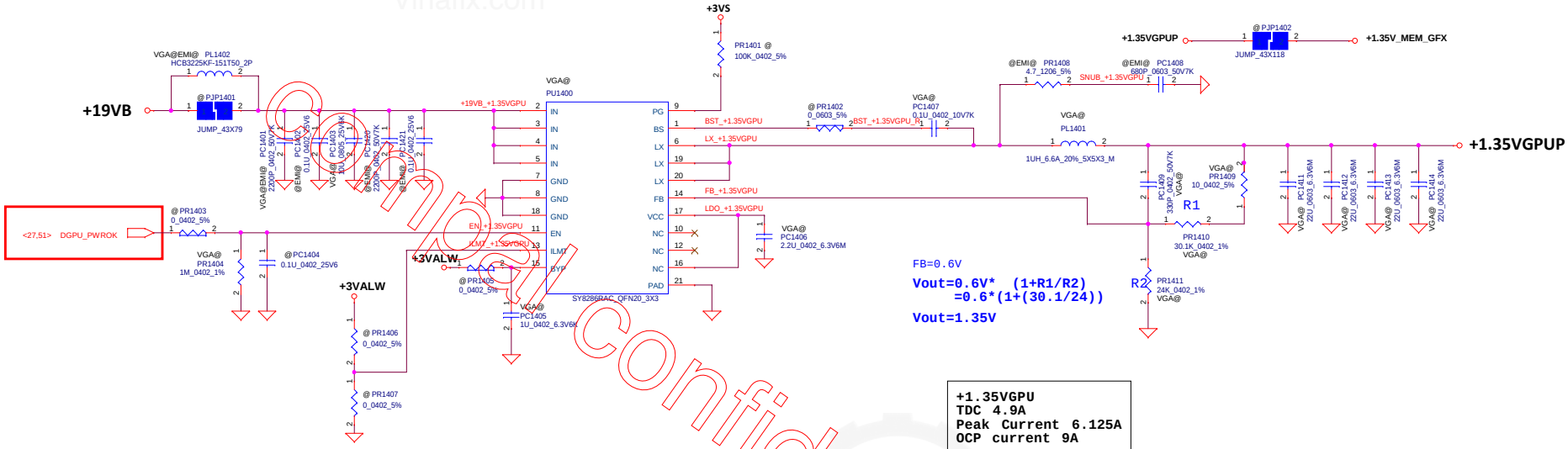
Security Classification	Compal Secret Data		
Issued Date	2014/03/31	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **PWR_VDDCR_FCH_S5(+0.775V)**

Size	Document Number	Rev
		0.1

Date: Monday, June 20, 2016 | Sheet 49 of 54

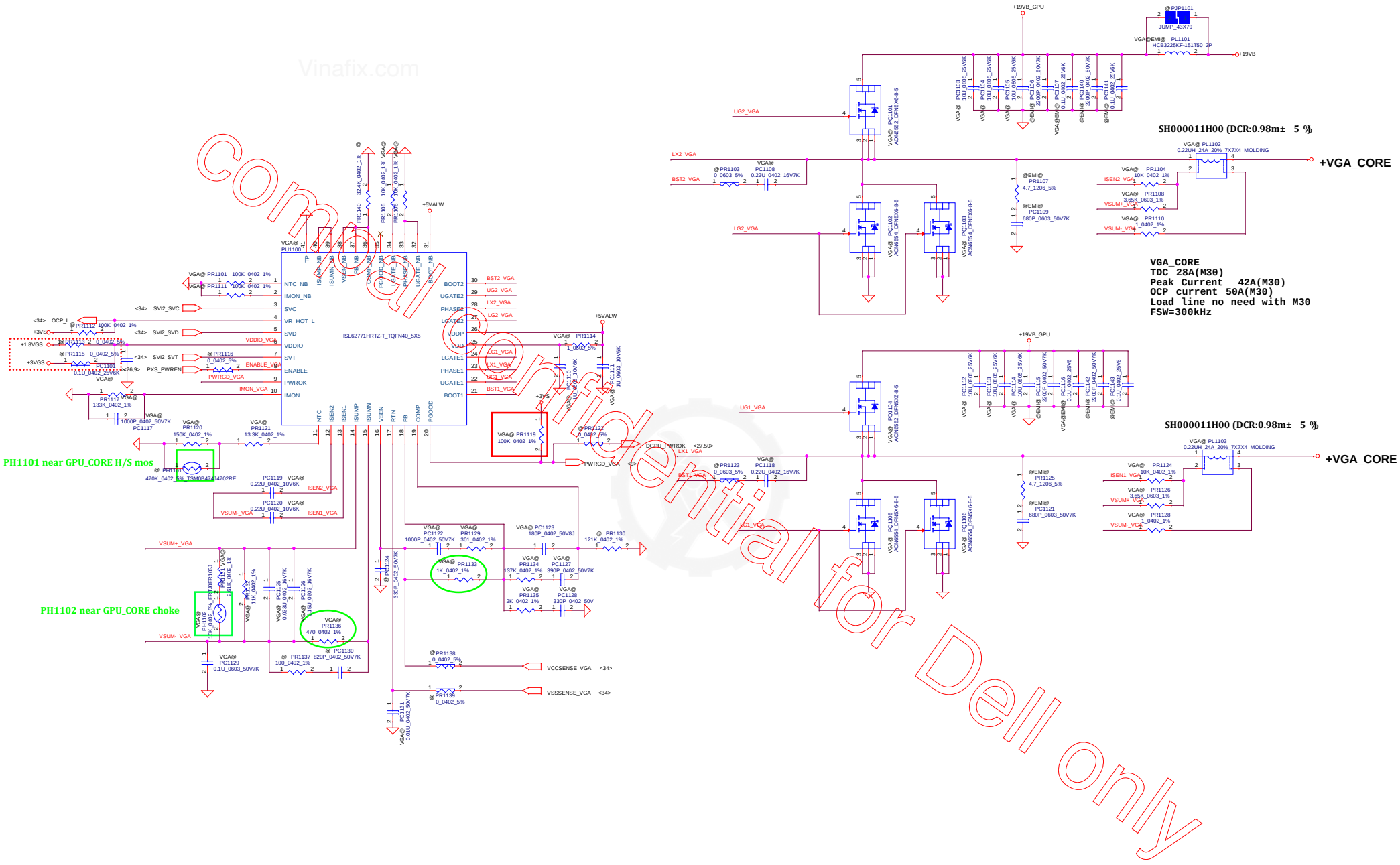


The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

OCP setting	ILMT(pin13)
6A	Pull low
9A	Floating
12A	Pull high

Security Classification	Compal Secret Data		
Issued Date	2014/03/31	Deciphered Date	2015/04/30

Compal Electronics, Inc.	
Title	PWR_+1.35VGPU
Size	Document Number / Rev 0.1
Date: Monday, June 20, 2016	Sheet 50 of 54



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

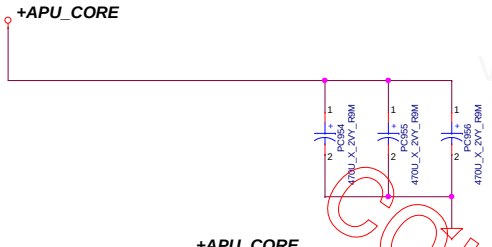
Title: **PWR_VGA_CORE**

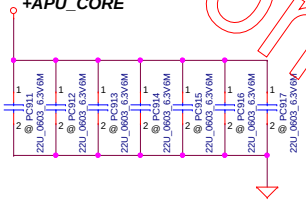
Size	Document Number	Rev
Custom		0.1

Date: Monday, June 20, 2016 Sheet 51 of 54

+APU_CORE

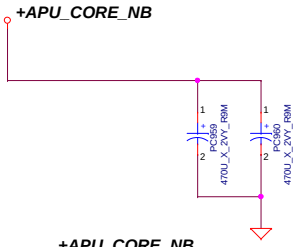
APU_CORE
470uF*3

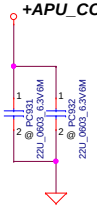


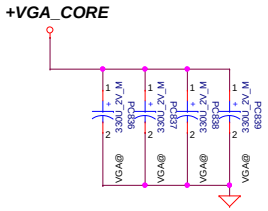


+APU_CORE_NB

APU_CORE_NB
470uF*2







DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

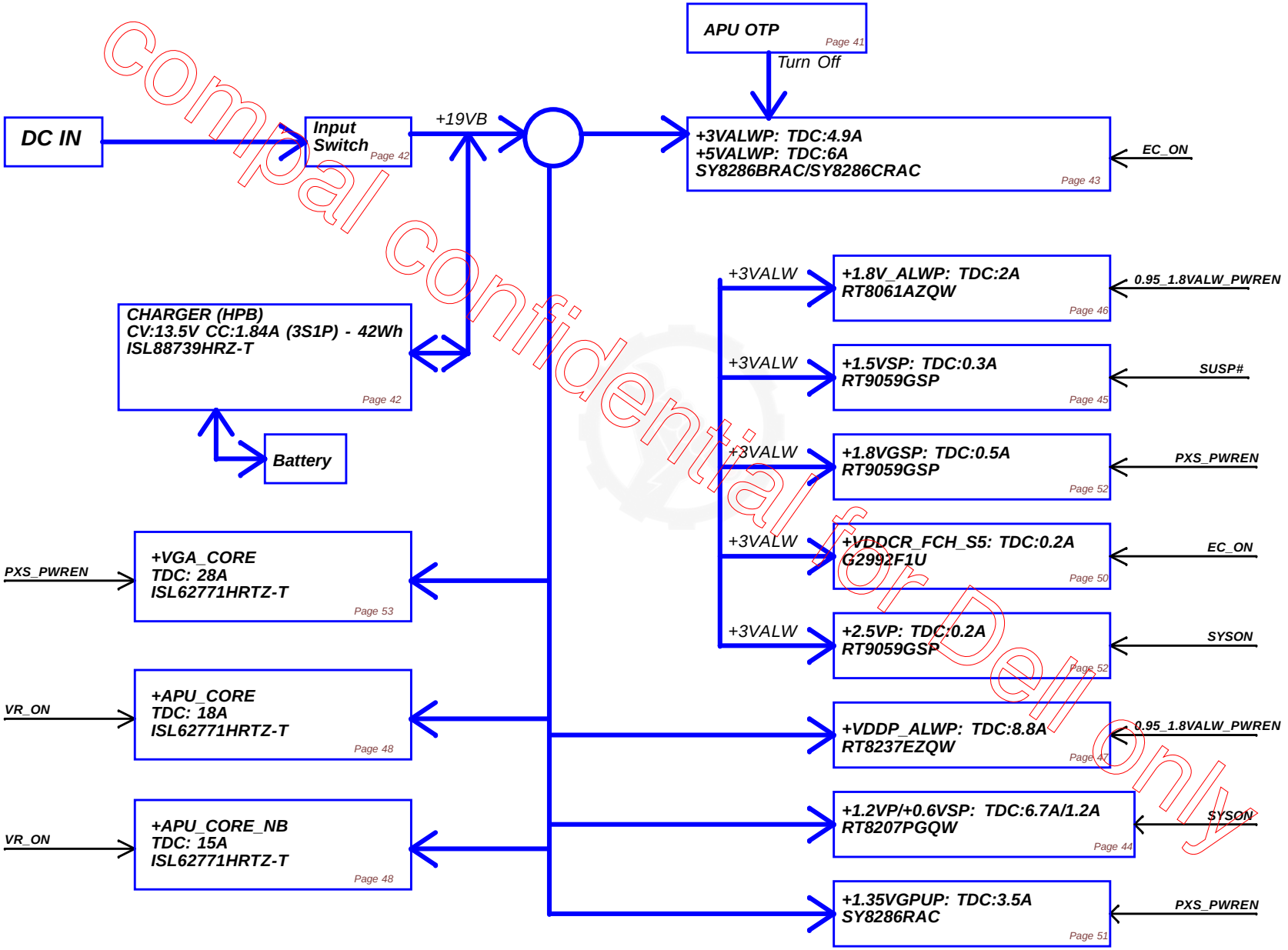
Compal Electronics, Inc.

Title: PWR_PROCESSOR DECOUPLING

Size	Document Number	Rev
	LA-C142P	0.1

Date: Monday, June 20, 2016 Sheet 52 of 54

Power block



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.			
Title	PWR_POWER BLOCK DIAGRAM		
Size	Document Number		Rev 1.0
Date: Monday, June 20, 2016	Sheet 53 of 54		

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	42	CHARGER	2016/3/24	COMPAL	customer recommend	change PU703 from SA00009RO00 to SA00009Q50L	0.2
2	42	CHARGER	2016/3/24	COMPAL	adjust T/V setting	change PR732 from 49.9K to 53.6K	0.2
3	42	CHARGER	2016/3/24	COMPAL	design change	add PC751 560P change PR774 from 0 to 1K change PC748 from 2200P to 0.1U delete PC760 PC761 PC764	0.2
4	46	+1.5VSP	2016/3/24	COMPAL	change power rail from 1.5V to 1.8V by EE side	delete all 1.5VS component	0.2
5	48	APU_CORE	2016/3/24	COMPAL	design change to adjust APU_CORE setting	delete PC1010 change PR1005 from 11.5K to 34K change PR1078 from 95.3K to 210K	0.2
6	47	VDDP_ALWP	2016/3/24	COMPAL	design change	delete PR310,PR311	0.2
7	51	VGA_CORE	2016/3/24	COMPAL	design change from EE recommend	add PR1119 100K	0.2
8	41	DCIN/BATT CONN/OTP	2016/5/06	COMPAL	adjust OTP setting from thermal recommend	change PR24 from 14K to 16.9K	0.3
9	41	DCIN/BATT CONN/OTP	2016/5/06	COMPAL	design change to remove Err_lot6 circuit	delete PR2,PR5,PR7,PR10,PQ1	0.3
10	44	+1.2V_MEN/+0.6V_DDR	2016/5/06	COMPAL	adjust OCP setting	change PR205 from 8.25K to 11K	0.3
11	42	CHARGER	2016/5/06	COMPAL	design change	change PQ740 from SB000014900 to SB00000SY00	0.3
12	41	DCIN/BATT CONN/OTP	2016/6/16	COMPAL	design change from EMI recommend	change PC2,PC4 from 0.1U to 2200P	1.0
13	43	3.3VALWP/5VALWP	2016/6/16	COMPAL	design change	change PR103 from 499K to 150K	1.0
14	41	DCIN/BATT CONN/OTP	2016/6/16	COMPAL	adjust OCP setting	change PR24 from 16.9K to 15K	1.0

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.			
Title	PWR-PIR		
Size	Document Number		Rev 0.1
Date: Monday, June 20, 2016	Sheet 54 of 54		

HW Schematic chang list (P.I.R)

Item	Page	Date	Rev.	Reason for change	Modify Item
1	26	1/28	0.2	Modify the capacitor value	C621 change 1uF capacitor to 4.7uF , C620 change 4.7uF capacitor to 1uF
2	26	1/28	0.2	Part count reduce	C344 Bom structure change to " DIS@ "
3	9	1/28	0.2	Modify Resistor value	RC346 47k ohm change to 22k ohm (SD028220280)
4	30	1/28	0.2	Modify PCB Part number	Modify PCB part number to DA6001LB000
5	13	1/29	0.2	Change Capacitor to H1.9	CD229 Change to SGA20331E10
6	26	3/13	0.2	Modify RC Delay for +1.8VGS	1.8VGS_0.95VSDGPU_ON connect to U15.3 & U15.5
7	9	3/13	0.2	Reserve RC938	RC938 change to unpop
8	24	3/15	0.2	Pop Q9 for touch-pad (PTP)	Q9 Change to pop
9	16	3/15	0.2	BOM change to cost reduce	+LCDVDD power switch U1 change to SA000079400
10	11.18	3/15	0.2	Audio codec change to +1.8VS to cost down +1.5VS LDO	Add RC18/RA15/RA16 ,reserve +1.5VS
11	24	3/15	0.2	JKB1.30 remove KB_DET# (follow Tulip)	Add RE60 reserve to +5VS
12		3/16	0.2	Part count reduce	Change to R-short RC119,RA1,RA2,RA4,RA5,RL5,R16,RC53,RC52
13	10.25	3/16	0.2	Change I/O USB conn. Port (AMD request)	USB20 Port7 change to Port2
14	22	3/16	0.2	SATA net name modify	Modify to SATA_TX_P0/N0 SATA_RX_P0/N0
15	22	3/16	0.2	Remove SATA ESD	Delete EU3101
16	17	3/18	0.2	For layout request swap RP12 pin	Swap RPI2 pin
17	9	3/18	0.2	Modify BIOS strap pin	Net name vram size/APU_ID/Panel size_ID change to VBIOS_ID1/ID2/ID3
18	23	3/21	0.2	Change USB3.0 EMI choke to pass EA test	LU1/LU2/LU4/LU5 SM070003Z00 change to SM070004K00
19	29	3/21	0.2	Change power on switch part number	SW1/SW2 change to SN10000B310
20	26	3/21	0.2	Modify to meet the GPU power sequence	Modify R438 1K to 33K ohm (SD028330280)
21	30	3/21	0.2	ME drawing add a screw hole	Add H13 H_6P0 screw hole
22	24	3/21	0.2	BOM change to cost reduce	F3 BOM SP040002400 change to SP040002B00
23	30	3/21	0.2	DFx review stand of f padcan't placevi a	H11 H_3P2-G modify to H_3P2
24	17	3/21	0.2	For layout swap RPI1 pin	Swap RPI1 pin
25	18	3/21	0.2	Vendor feedback have extra pull-up Resistor same funct i on as RA25/ RA26	Remove RA46, RA47
27	29	3/21	0.2	Remove PWR/Board unused pin	Remove JPWR1.4 +5VALW net name
28	19	3/22	0.2	Design change for Hi-pot test fail at EVT	LANGND Change to GND
29	26	3/22	0.2	Reserve 0.1uF for +0.95VSDGPU output	Add C625 0.1uF
30	9	3/22	0.2	Reserve BIOS strap pin	VBIOS ID1/ID2/ID3 change to RESERVE_1/APU_ID/RESERVE_2
31	27	3/22	0.2	Board ID update to DVT1 Set t i ng	RE22 change to 200k_0402_1% (SD034200380)
32	29	3/22	0.2	ESD request to pop	Pop EC2902 ,EC2901
33	29	3/22	0.2	Update JPWR1 Footprint	Update JPWR1 footprint "ACES_51678-00601-W01_6P-T"
34	18	3/22	0.2	Add Audio codec ALC3234 Part number	add ALC3234 PN "SA000076U00"
35	27	3/23	0.2	EC/BIOS comment no use	Unpop RE40,RE44,RW9,RW10
36	16	3/24	0.2	Sourcer request change main source	LX1 change main source to SM01000EJ00
37	40	3/24	0.2	VRAM Strap pin set t i ng update	Modify BOM structure 2G_S@ ,2G_H@ ,2G_M@
38	11	3/24	0.2	For PWR to add MLCC*9	Unpop CC1117,CC1120,CC1121,CC1122,CC1123,CC1125,CC1127
39	22	3/25	0.2	SATA Parade Re-driver EQ set t i ng to def ault 12. 2dB	unpop RS22,RS27,RS28,RS37
40	26	3/25	0.2	Pop 0.1uF for +1.8VS & +0.95VSDGPU output	Pop C26,C625

HW Schematic chang list (P.I.R)

Item	Page	Date	Rev.	Reason for change	Modify Item
41	30	4/21	0.3	Increase EMI MLCC Cap voltage rat i ng	Change C35,C36,C37,C38,C39,C40 to SE00000G880
42	16	4/24	0.3	Increase Cap. voltage rat i ng	Change C4 10u_6.3V to 10u_25V voltage rat i ng
43		4/24	0.3	Increase Cap. voltage rat i ng	Change C34,C2305,C2306,C2308,C2323,CA1,CA3,CU13,CU18,Cs15 10u_6.3v to 10u_10v voltage rat i ng
44	18	4/24	0.3	Increase Cap. voltage rat i ng	Change CA11 4.7u_6.3V to 4.7u_10V voltage rat i ng
45	24	4/24	0.3	Increase Cap. voltage rat i ng	Change CF4 22u_6.3V to 22u_10v voltage rat i ng
46	30	4/25	0.3	ME drawing modify screw hole	Modify H6 5P0N to 5P6N
47	18	4/25	0.3	Change Part from EMI request	LA3,LA4,LA5,LA6 "SM01000BV00" change to "SM01000NX00"
48	34	4/25	0.3	Part count calculate	Change RV158,RV159,RV164 BOM structure to DIS@
49		4/29	0.3	Part count reduce	Change to R-short RC458,RC32,RC22,RC665,RC1675,RC18,RD25,RD28,RD29,RX7,R13,R6, R14,R51.R7,RA15,RA42,RA11,RA22,RL9,RW11,RA40,RE338,R37,RE5,RE31,RE32, RE33,RE34,RE37,RE38,RE50,RE51,RE42,RE39,RV164,RV27,RV30,RV31,RV364
50	8	4/29	0.3	Part count calculate	Change RC29,RC23,RC664 BOM structure to @
51	27	5/3	0.3	Board ID change to DVT2	RE22 change to 240k_0402_1% (SD000001B80)
52	6	5/3	0.3	Add AMD Stoney A9-9400 BOM	Add A9-9400 Part number SA0000A280L
53	27	5/3	0.3	ESD request to pop	Pop CE23
54	30	5/3	0.3	EMI request to unpop MLCC Cap.	Unpop C35,C36,C37,C38,C39,C40,C41,C42,C43,C44,C45,C46,C47,C48,C49
55	21	5/3	0.3	EMI request to change part	LA8,LA9 Change to 0_0402_5%
56	29	5/3	0.3	ME Update JPWR1 Footprint	Update JPWR1 footprint to "JXT_FP226H-006S1BM_6P"
57	9	5/3	0.3	APU_ID Modify BOM structure	E2A6@ Change to E2A6A9@
58	6	5/3	0.3	Add E2-9000/A6-9200 PR sample PN	Modify E2-9000 "SA00009W80L" , A6-9200 " SA0000A2A0L"
59	22	5/3	0.3	Add TI re-driver EQ set t i ng (7dB	Pop RS33, RS34 to 4.7k_0402_5% , pop RS18,RS22,RS23,RS27,RS28
60	9	5/26	1.0	Reserve 0ohm for APU_PCIE_WAKE#	Add RC967 for APU_PCIE_WAKE# (unpop)
61	26	5/26	1.0	Modify +0.95VSDGPU & +1.8VGS slew rate to meet GPU sequence	C343,C344 change to 2200pF (SE075222K80)
62	27	6/6	1.0	Board ID change to X build set t i ng	RE22 change to 270k 1% ohm (SD00000G280)
63	9	6/6	1.0	Change BIOS APU_ID strap pin	RC708->A6A9@ , RC707->E2@
64	29	6/6	1.0	Reserve MB power bot t on(S W1, S W2)	SW1 ,SW2 change BOM structure to @
65	6	6/6	1.0	Add AMD Stoney CPU R3 PN	Add Stoney E2-9000 ,A6-9200, A9,9400 R3 PN
66		6/13	1.0	DFB issue : co-lay un-used pin need to solder mask	RI1,RI2,RI4,RI5,RI7,RI8,RI10,RI11,RU1,RU2,RU3,RU4,RU5,RU6,RU7, RU8,RU9,RU10,RU11,RU12,RU13,RU14,RU17,RU18,R17,R18 solder mask
67	24	6/14	1.0	Change JKB1 Footprint(DFB issue)	Change JKB1 Footprint to use SP01001LN00 footprint (2nd source)
68	18	6/14	1.0	EMI part count reduce	RA17,RA18,RA19,RA20,RA21 0ohm Change to R-short
69	24	6/14	1.0	Add GPU R3 PN	Add AMD M1-30 R3 PN
70	24	6/14	1.0	Add VRAM R3 PN	Add VRAM Samsung , Hynix, Micron R3 PN
71	30	6/15	1.0	Add PCB R3 PN	Add PCB R3 PN "DA6001LB011"
72	11	6/16	1.0	Extra 0.22uF Cap. , Follow AMD checklist	CC1129 Change Bom Structure to @