

MODEL NAME : DDR51(15")/DDR71(17")
PROJECT CODE : ANRDDR5100/ANRDDR7100
PCB NO :
DAC0000E000 : LA-F551P M/B NV G1G2
DAC0000F000 : LA-F552P M/B NV G3
DAB0002I000 : LA-F553P M/B AMD
DA4002AV000 : LS-D751P LOGO_15/B
DA80017I000 : LS-D752P LOGO_17/B
DA4002B000S : LS-D753P PWR_15/B
DA4002AW000 : LS-D754P PWR_17/B
DA80017J000 : LS-D755P IO_12L/B
DA4002ND000 : LS-F551P TRON_LCD_15/B
DA4002NE000 : LS-F552P TRON_REAR_15/B
DA80017K000 : LS-D759P IO_14L/B
DA4002NG000 : LS-F554P TRON_LCD_17/B
DA4002NH000 : LS-F555P TRON_REAR_17/B
DA4002NF000 : LS-F553P TRON_FRONT_15/B
DA4002NI000 : LS-F556P TRON_FRONT_17/B
DA30000W300 : LF-D751P Head_15/B
DA30000W400 : LF-D752P Head_17/B
DA30000W401 : LF-D752P Head_17/B(For LOGO_15/B)
DA300013900 : LF-F551 TRON_15/B
DA300013E00 : LF-F552 TRON_17/B

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DDR51
Coffee Lake-H 45W
CNL PCH-H with nVIDIA N17E

REV : 1.0 (A00)
2018.02.06

@ : Nopop Component
EMI@,ESD@,RF@ : EMI/ESD/RF part
CONN@ : Connector Component
@EMI@,@ESD@,@RF@ : Total debug Component

ZZZ PCB@
PCB 26S LA-F552P REV0 M/B NV G3 16
DAC0000F000

ZZZ PCBR1@
PCB 26S LA-F552P REV1 M/B NV G3 16
DAC0000F010


ZZZ PCBR3@
PCB 26S LA-F552P REV1 MB NV TRIP 16 A31!
DAC0000F011

ZZZ DAZR1@
PCB DDR51 LA-F552P LS-D751P-52P/D754P 02
DAZ26S00200

ZZZ DAZR3@
PCB DDR51 LA-F552P LS-D751 02 TRIP A31 !
DAZ26S00201

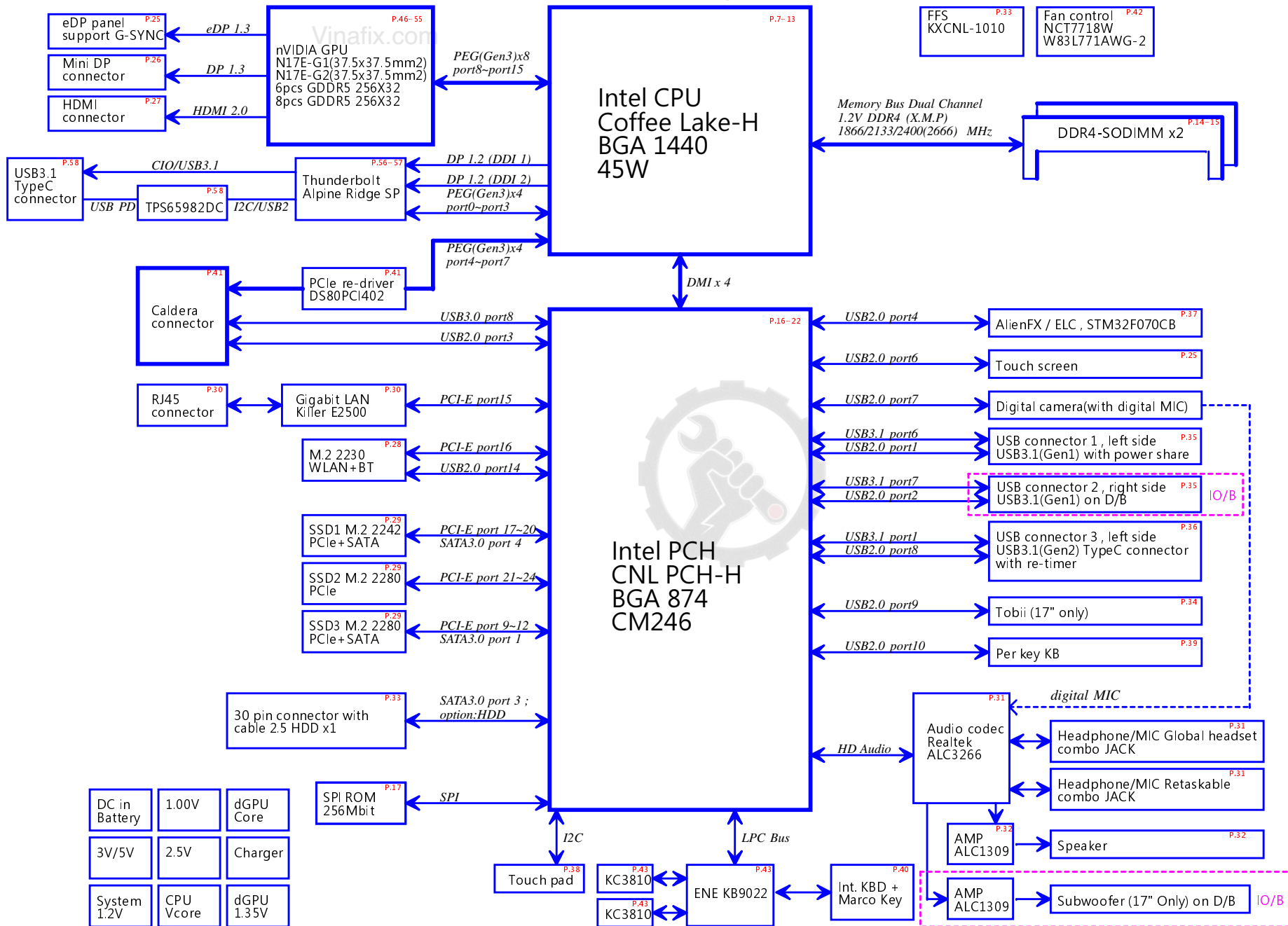
HDMI@ ROYALTY HDMI W/LOGO	
Part Number	Description
LA-F552P-52P	LA-F552P W/Logo (RODR0000030K)

Layout Dell logo



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REV: X00
PWB: XXXXX
DATE: 1450-06

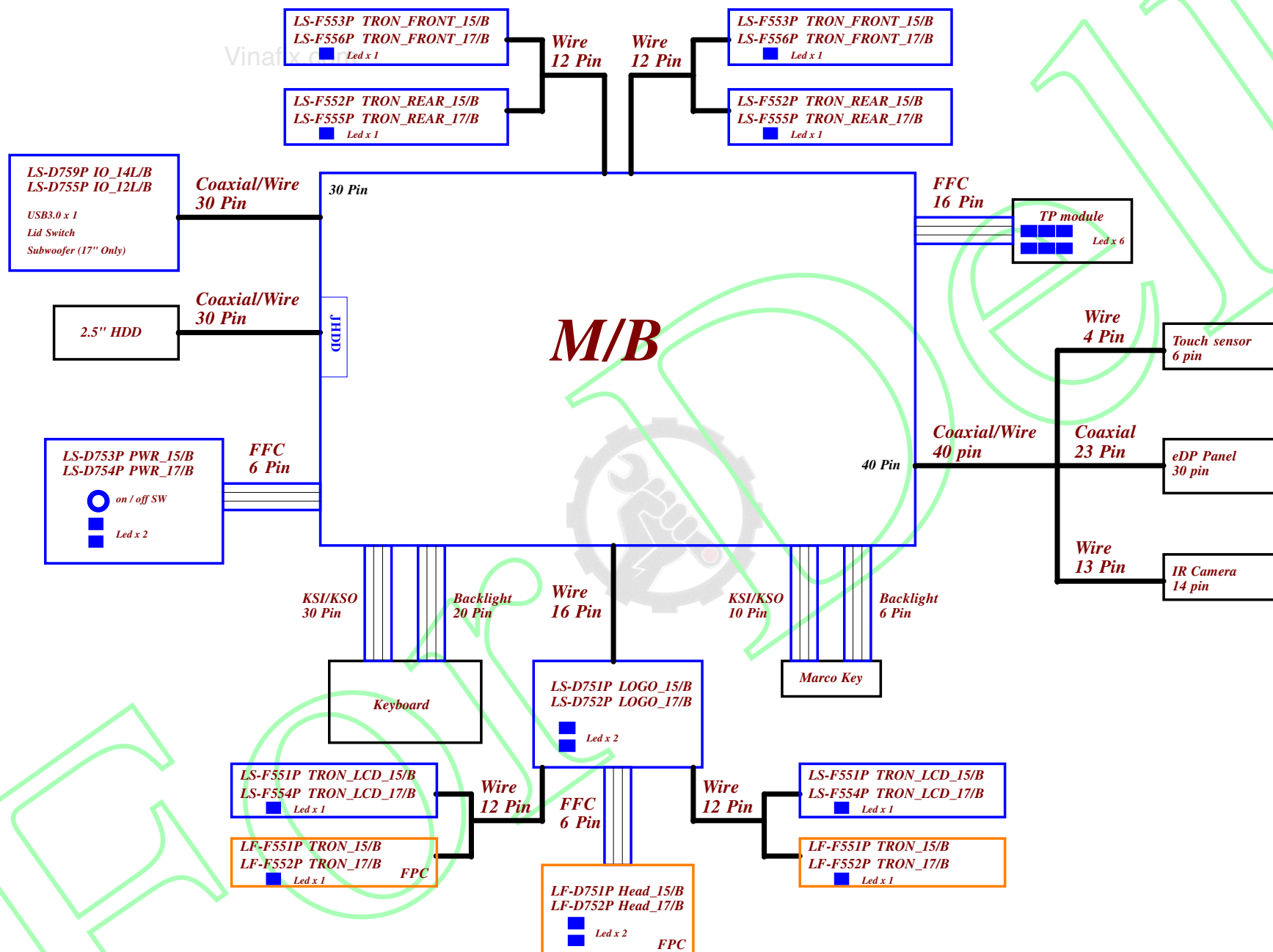
Block Diagram



PCB

FPC

Module



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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

NVIDIA
GraphicAMD
Graphic

Voltage Rails

Power Plane	Description	S0	S3	S4 / S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_VDDQ	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCST	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VALW	+1.8VALW power rail for PCH	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Board ID table

NV	AMD	PCB Revision
0	10	EVT-1
1	11	EVT-2
2	12	DVT-1
3	13	DVT-2
4	14	Pilot

PCH-H CM246

HSIO	USB3.1	PCIe	SATA3	Function
0	1			JUSBC2,type C
1	2			
2	3			
3	4			
4	5			
5	6			JUSB1,type A
6	7	1		JIO,IO/B
7	8	2		Caldera
8	9	3		
9	10	4		
10		5		
11		6		
12		7		
13		8		
14		9		
15		10		JSSD3 , 2280 SATA/PCIe x4
16		11	0a	
17		12	1a	
18		13	0b	JSSD4/HDD
19		14	1b	
20		15	2	LAN
21		16	3	WLAN
22		17	4	
23		18	5	JSSD1 , 2242 SATA/PCIe x4
24		19		
25		20		
26		21		
27		22		JSSD2 , 2280 PCIe x4
28		23		
29		24		

USB2	Function
1	JUSB1(Powershare)
2	JIO(IO/B)
3	Caldera
4	ELC
5	
6	Touch screen
7	Camera
8	JUSBC2
9	Tobii
10	Per Key
11	Thunderbolt AR
12	
13	
14	Bluetooth

Symbol Note :



Digital Ground

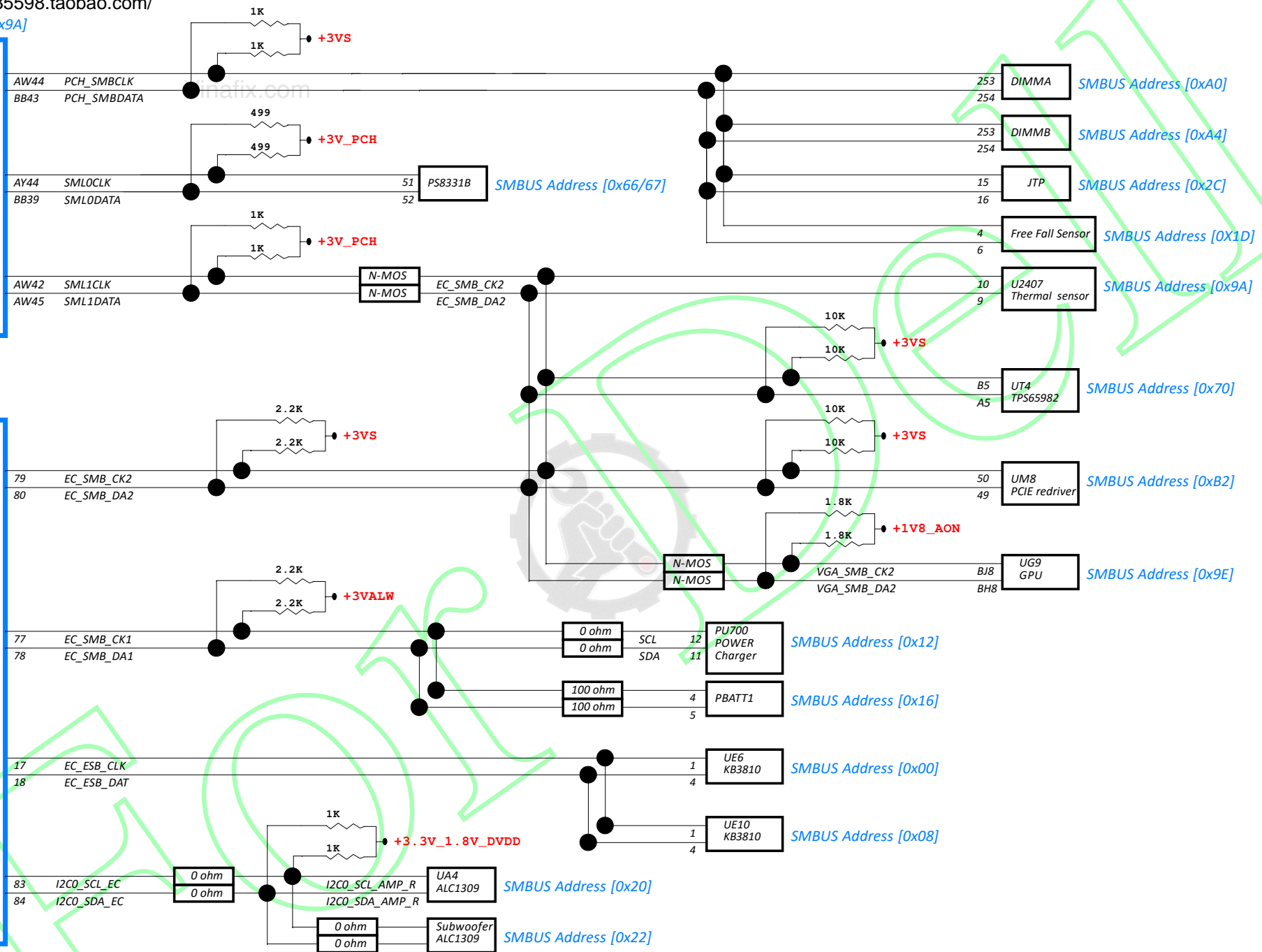


Analog Ground

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Coffee Lake
PCH-H

KBC
KB9022QD



UC1
S IC A31 CL8068403359717 QNCT U0 2.4G
SA0000BPVUL
CPU24@

UC1
S IC A31 CL8068403359715 QNVH U0 2G BGA
SA0000B041L
CPU20@

UC1
S IC A31 CL8068403805708 QPOG U0 2.9G
SA0000BPVUL
CPU9@

UC1
S IC A31 CL8068403359524 QP87 U0 2.2G
SA0000BP20L
CPU17@

UC1
S IC A31 CL8068403373522 QP89 U0 2.3G
SA0000BPJUL
CPU15@

UC1
S IC CL8068403805708 SRCKN U0 2.9G A31 !
SA0000BPV2L
C17R3@

UC1
S IC CL8068403359524 SR3YY U0 2.2G A31!
SA0000BP22L
C17R3@

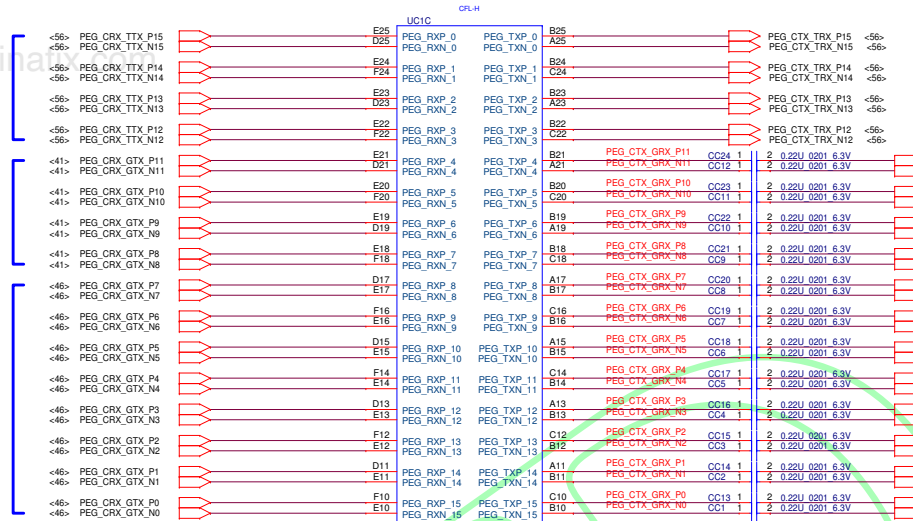
UC1
S IC CL8068403373522 SR3Z0 U0 2.3G A31!
SA0000BP22L
C17R3@

Thunderbolt TX

Caldera TX

GPU TX

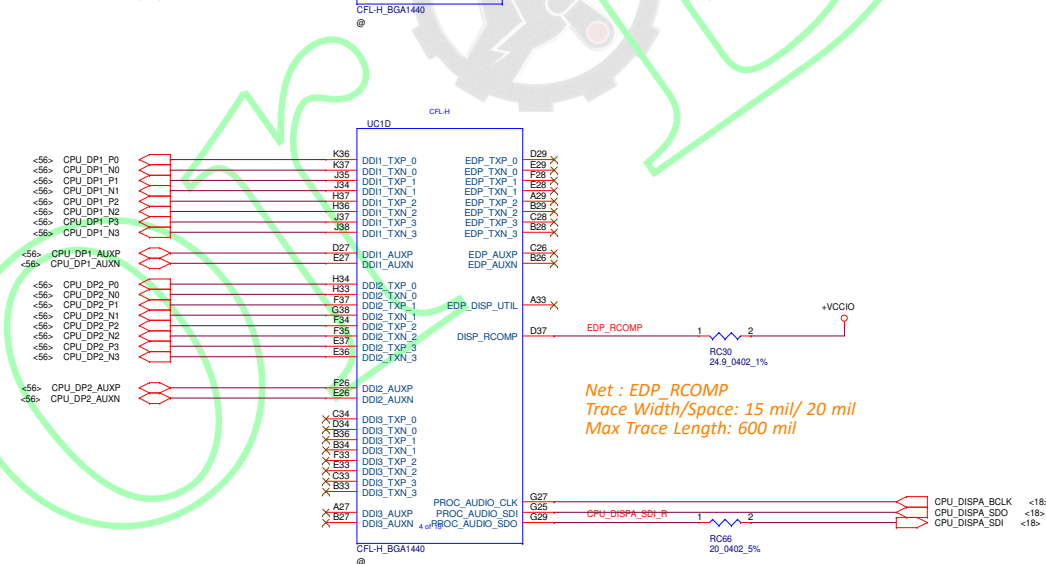
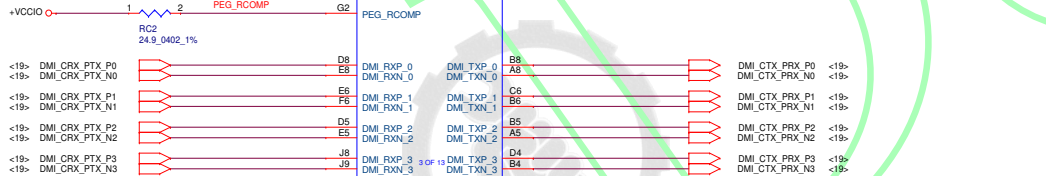
Net : PEG_RCOMP
Trace Width/Space: 15 mil/ 15 mil
Max Trace Length: 600 mil



Thunderbolt RX

Caldera RX

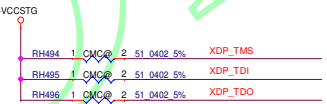
GPU RX

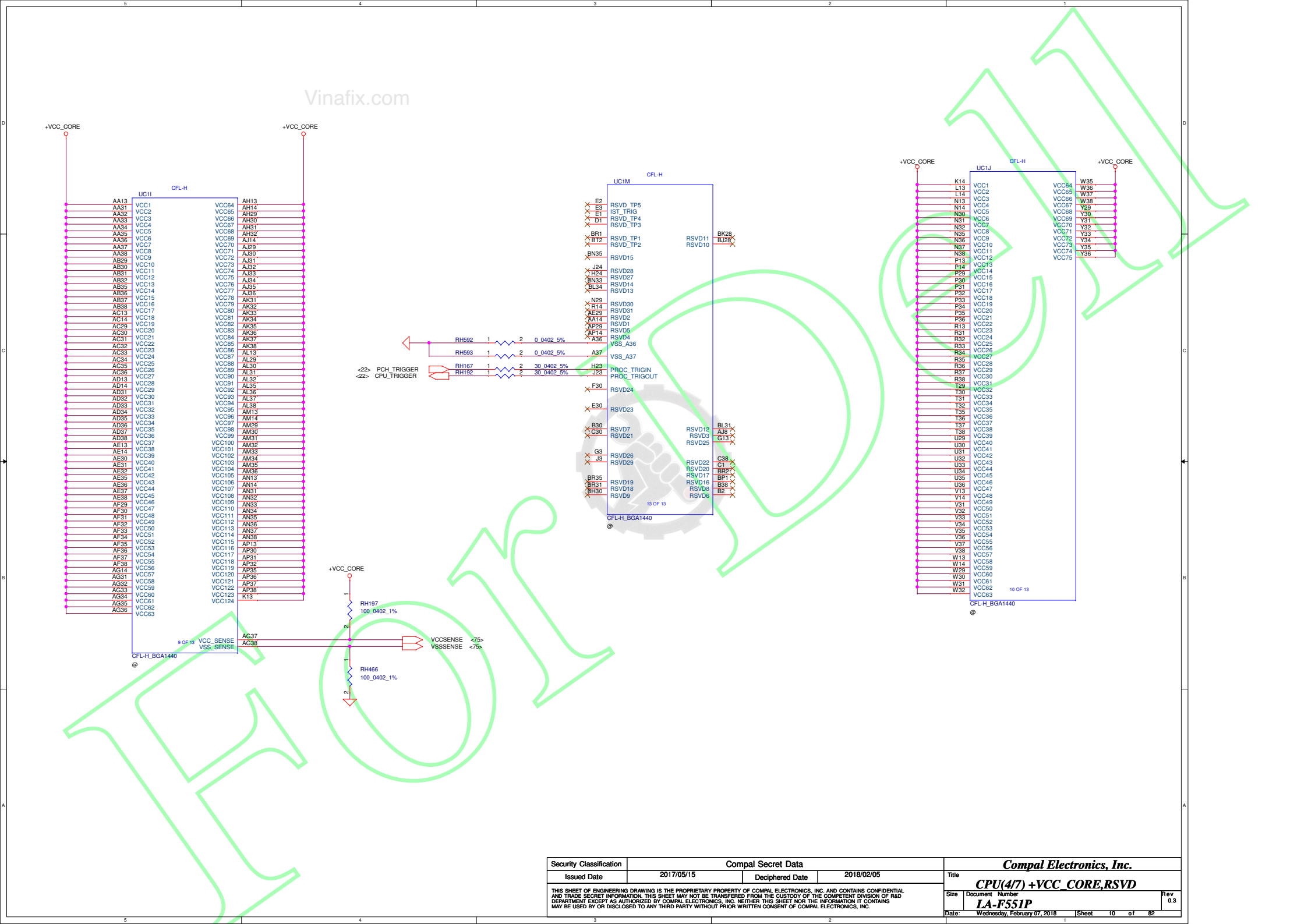


Net : EDP_RCOMP
Trace Width/Space: 15 mil/ 20 mil
Max Trace Length: 600 mil



PEG DEFER TRAINING	
CFG7	<p>* 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>



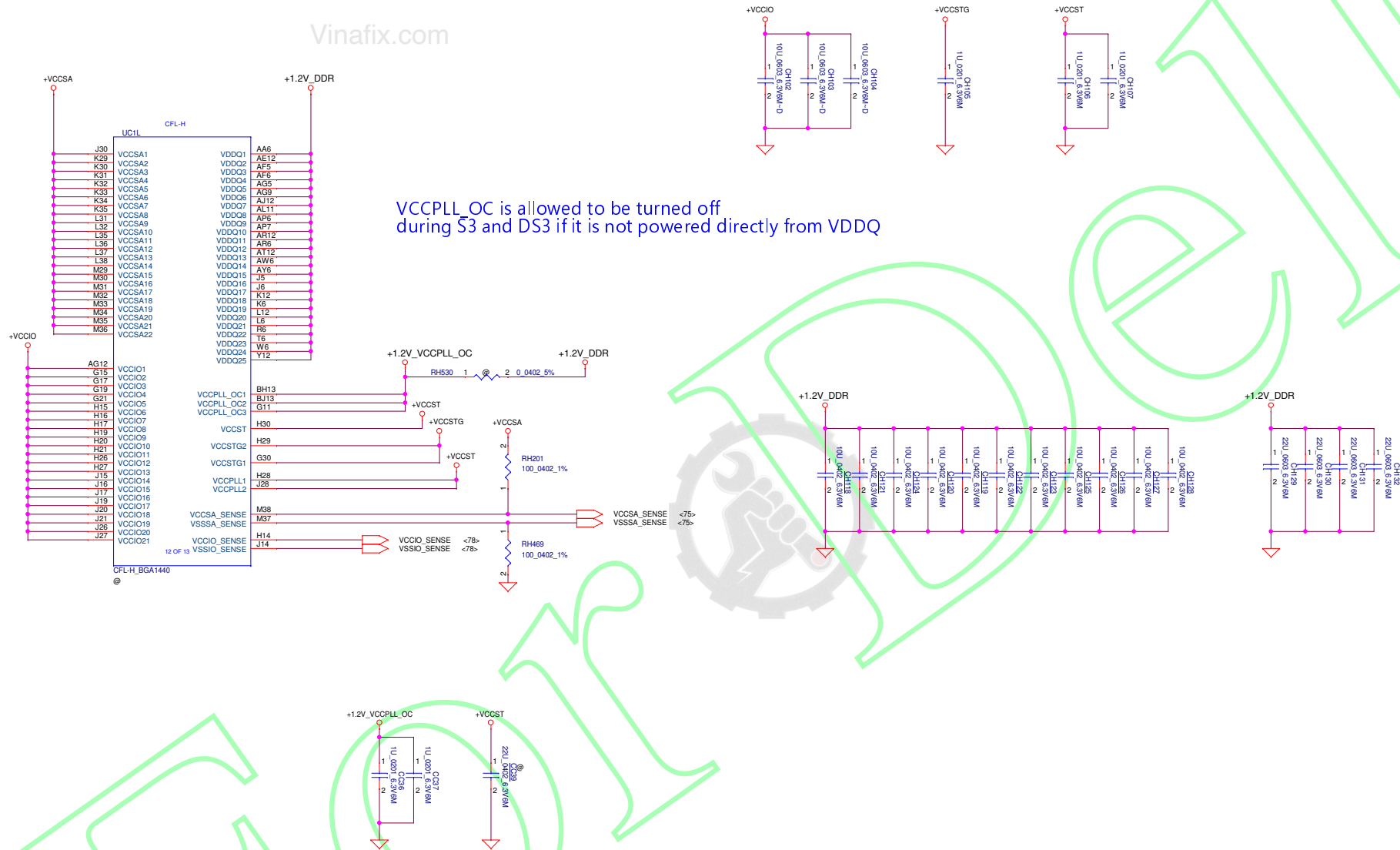


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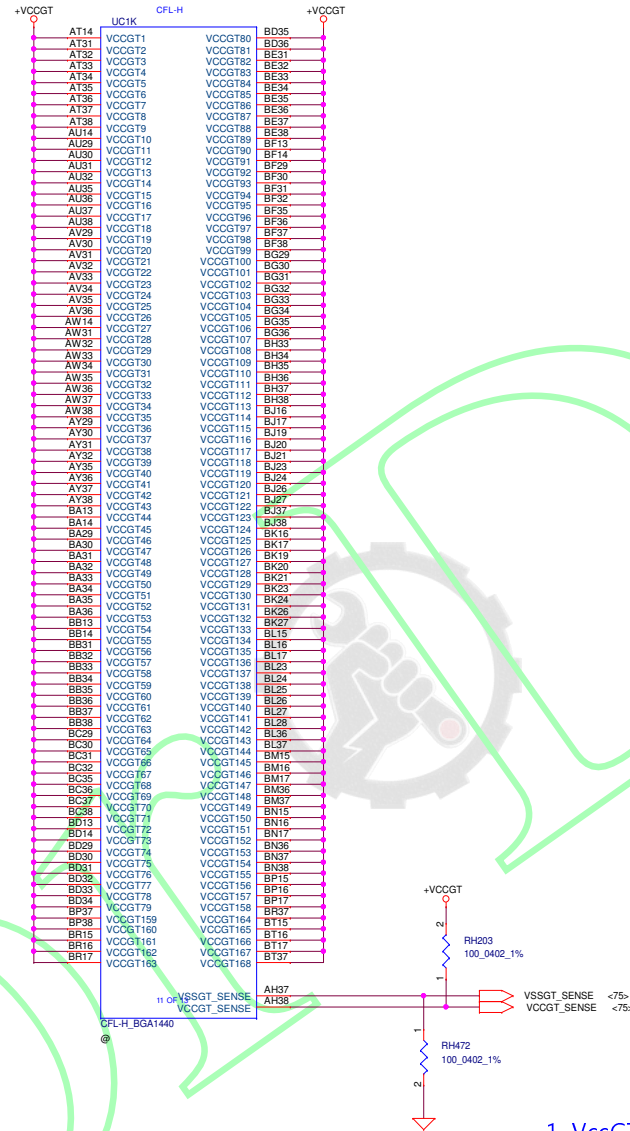
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Title	CPU(4/7) +VCC_CORE,RSVD		Size	Document Number
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1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC1, RC2 should be placed within 2 inches (50.8 mm) of CPU

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CFL-H				CFL-H				CFL-H				CFL-H			
UCIF				UCIG				UCIH				UCIH			
A10	VSS_1	VSS_82	AL10	AW5	VSS_163	VSS_244	BJ15	BN4	VSS_325	VSS_409	F15	BN7	VSS_325	VSS_409	F17
A12	VSS_2	VSS_83	AL12	AY12	VSS_164	VSS_245	BJ22	BP12	VSS_326	VSS_410	F19	BP12	VSS_326	VSS_410	F19
A16	VSS_3	VSS_84	AL14	AY34	VSS_165	VSS_246	BJ25	BP14	VSS_327	VSS_411	F21	BP14	VSS_327	VSS_411	F21
A18	VSS_4	VSS_85	AL14	AY34	VSS_166	VSS_247	BJ29	BP18	VSS_328	VSS_412	F23	BP18	VSS_328	VSS_412	F23
A20	VSS_5	VSS_86	AL34	BA9	VSS_167	VSS_248	BJ30	BP21	VSS_329	VSS_413	F25	BP21	VSS_329	VSS_413	F25
A22	VSS_6	VSS_87	AL4	BA10	VSS_168	VSS_249	BJ31	BP24	VSS_330	VSS_414	F27	BP24	VSS_330	VSS_414	F27
A24	VSS_7	VSS_88	AL7	BA11	VSS_169	VSS_250	BJ32	BP25	VSS_331	VSS_415	F29	BP25	VSS_331	VSS_415	F29
A26	VSS_8	VSS_89	AL9	BA12	VSS_170	VSS_251	BJ33	BP26	VSS_332	VSS_416	F31	BP26	VSS_332	VSS_416	F31
A28	VSS_9	VSS_90	AL9	BA37	VSS_171	VSS_252	BJ34	BP29	VSS_333	VSS_417	F33	BP29	VSS_333	VSS_417	F33
A30	VSS_10	VSS_91	AM1	BA38	VSS_172	VSS_253	BJ35	BP33	VSS_334	VSS_418	F35	BP33	VSS_334	VSS_418	F35
A6	VSS_11	VSS_92	AM12	BA6	VSS_173	VSS_254	BJ36	BP34	VSS_335	VSS_419	F36	BP34	VSS_335	VSS_419	F36
A9	VSS_12	VSS_93	AM2	BA7	VSS_174	VSS_255	BJ36	BP7	VSS_336	VSS_420	F4	BP7	VSS_336	VSS_420	F4
AA12	VSS_13	VSS_94	AM3	BA8	VSS_175	VSS_256	BK13	BR12	VSS_337	VSS_421	F5	BR12	VSS_337	VSS_421	F5
AA29	VSS_14	VSS_95	AM37	BA9	VSS_176	VSS_257	BK14	BR14	VSS_338	VSS_422	F8	BR14	VSS_338	VSS_422	F8
AA30	VSS_15	VSS_96	AM38	BB1	VSS_177	VSS_258	BK15	BR18	VSS_339	VSS_423	F9	BR18	VSS_339	VSS_423	F9
AB33	VSS_16	VSS_97	AM4	BB12	VSS_178	VSS_259	BK18	BR21	VSS_340	VSS_424	G10	BR21	VSS_340	VSS_424	G10
AB34	VSS_17	VSS_98	AM4	BB2	VSS_179	VSS_260	BK22	BR24	VSS_341	VSS_425	G12	BR24	VSS_341	VSS_425	G12
AB6	VSS_18	VSS_99	AM5	BB29	VSS_180	VSS_261	BK25	BR25	VSS_342	VSS_426	G14	BR25	VSS_342	VSS_426	G14
AC1	VSS_19	VSS_100	AN29	BB3	VSS_181	VSS_262	BK29	BR26	VSS_343	VSS_427	G16	BR26	VSS_343	VSS_427	G16
AC12	VSS_20	VSS_101	AN30	BB30	VSS_182	VSS_263	BK6	BR29	VSS_344	VSS_428	G18	BR29	VSS_344	VSS_428	G18
AC2	VSS_21	VSS_102	AN6	BB4	VSS_183	VSS_264	BL13	BR34	VSS_345	VSS_429	G20	BR34	VSS_345	VSS_429	G20
AC3	VSS_22	VSS_103	AN6	BB5	VSS_184	VSS_265	BL14	BR36	VSS_346	VSS_430	G22	BR36	VSS_346	VSS_430	G22
AC37	VSS_23	VSS_104	AP10	BB6	VSS_185	VSS_266	BL18	BR7	VSS_347	VSS_431	G23	BR7	VSS_347	VSS_431	G23
AC38	VSS_24	VSS_105	AP11	BC12	VSS_186	VSS_267	BL19	BT12	VSS_348	VSS_432	G24	BT12	VSS_348	VSS_432	G24
AC4	VSS_25	VSS_106	AP12	BC13	VSS_187	VSS_268	BL20	BT14	VSS_349	VSS_433	G26	BT14	VSS_349	VSS_433	G26
AC5	VSS_26	VSS_107	AP33	BC14	VSS_188	VSS_269	BL21	BT18	VSS_350	VSS_434	G28	BT18	VSS_350	VSS_434	G28
AC6	VSS_27	VSS_108	AP34	BC33	VSS_189	VSS_270	BL22	BT21	VSS_351	VSS_435	G4	BT21	VSS_351	VSS_435	G4
AD10	VSS_28	VSS_109	AP8	BC34	VSS_190	VSS_271	BL29	BT24	VSS_352	VSS_436	G5	BT24	VSS_352	VSS_436	G5
AD11	VSS_29	VSS_110	AP8	BC6	VSS_191	VSS_272	BL33	BT26	VSS_353	VSS_437	G6	BT26	VSS_353	VSS_437	G6
AD12	VSS_30	VSS_111	AR1	BD10	VSS_192	VSS_273	BL38	BT29	VSS_354	VSS_438	G8	BT29	VSS_354	VSS_438	G8
AD29	VSS_31	VSS_112	AR13	BD11	VSS_193	VSS_274	BL6	BT32	VSS_355	VSS_439	G9	BT32	VSS_355	VSS_439	G9
AD30	VSS_32	VSS_113	AR14	BD12	VSS_194	VSS_275	BL6	BT5	VSS_356	VSS_440	H11	BT5	VSS_356	VSS_440	H11
AD6	VSS_33	VSS_114	AR2	BD37	VSS_195	VSS_276	BM11	BT11	VSS_357	VSS_441	H12	BT11	VSS_357	VSS_441	H12
AD8	VSS_34	VSS_115	AR29	BD6	VSS_196	VSS_277	BM12	C13	VSS_358	VSS_442	H18	C13	VSS_358	VSS_442	H18
AD9	VSS_35	VSS_116	AR3	BD7	VSS_197	VSS_278	BM13	C17	VSS_359	VSS_443	H27	BM13	VSS_359	VSS_443	H27
AE33	VSS_36	VSS_117	AR30	BD8	VSS_198	VSS_279	BM14	C19	VSS_360	VSS_444	H25	BM14	VSS_360	VSS_444	H25
AE34	VSS_37	VSS_118	AR31	BD9	VSS_199	VSS_280	BM18	C21	VSS_361	VSS_445	H32	C21	VSS_361	VSS_445	H32
AE6	VSS_38	VSS_119	AR32	BE1	VSS_200	VSS_281	BM2	C19	VSS_362	VSS_446	H35	C19	VSS_362	VSS_446	H35
AF1	VSS_39	VSS_120	AR33	BE2	VSS_201	VSS_282	BM22	C23	VSS_363	VSS_447	H10	C23	VSS_363	VSS_447	H10
AF12	VSS_40	VSS_121	AR34	BE29	VSS_202	VSS_283	BM22	C25	VSS_364	VSS_448	J18	C25	VSS_364	VSS_448	J18
AF13	VSS_41	VSS_122	AR35	BE3	VSS_203	VSS_284	BM23	C27	VSS_365	VSS_449	J22	C27	VSS_365	VSS_449	J22
AF14	VSS_42	VSS_123	AR36	BE30	VSS_204	VSS_285	BM24	C29	VSS_366	VSS_450	J25	C29	VSS_366	VSS_450	J25
AF2	VSS_43	VSS_124	AR37	BE4	VSS_205	VSS_286	BM25	C31	VSS_367	VSS_451	J32	C31	VSS_367	VSS_451	J32
AF3	VSS_44	VSS_125	AR38	BE5	VSS_206	VSS_287	BM26	C37	VSS_368	VSS_452	J33	C37	VSS_368	VSS_452	J33
AF4	VSS_45	VSS_126	AR4	BE6	VSS_207	VSS_288	BM27	C5	VSS_369	VSS_453	J36	C5	VSS_369	VSS_453	J36
AG10	VSS_46	VSS_127	AR5	BF12	VSS_208	VSS_289	BM28	C8	VSS_370	VSS_454	J4	C8	VSS_370	VSS_454	J4
AG11	VSS_47	VSS_128	AT29	BF33	VSS_209	VSS_290	BM29	C9	VSS_371	VSS_455	J7	C9	VSS_371	VSS_455	J7
AG13	VSS_48	VSS_129	AT30	BF34	VSS_210	VSS_291	BM3	D10	VSS_372	VSS_456	K1	D10	VSS_372	VSS_456	K1
AG29	VSS_49	VSS_130	AT30	BF6	VSS_211	VSS_292	BM33	D12	VSS_373	VSS_457	K10	D12	VSS_373	VSS_457	K10
AG30	VSS_50	VSS_131	AU10	BG12	VSS_212	VSS_293	BM35	D14	VSS_374	VSS_458	K11	D14	VSS_374	VSS_458	K11
AG6	VSS_51	VSS_132	AU11	BG13	VSS_213	VSS_294	BM38	D16	VSS_375	VSS_459	K2	D16	VSS_375	VSS_459	K2
AG7	VSS_52	VSS_133	AU12	BG14	VSS_214	VSS_295	BM5	D18	VSS_376	VSS_460	K3	D18	VSS_376	VSS_460	K3
AG8	VSS_53	VSS_134	AU33	BG37	VSS_215	VSS_296	BM6	D20	VSS_377	VSS_461	K38	D20	VSS_377	VSS_461	K38
AH12	VSS_54	VSS_135	AU34	BG38	VSS_216	VSS_297	BM7	D22	VSS_378	VSS_462	K4	D22	VSS_378	VSS_462	K4
AH33	VSS_55	VSS_136	AU6	BG6	VSS_217	VSS_298	BM8	D24	VSS_379	VSS_463	K5	D24	VSS_379	VSS_463	K5
AH34	VSS_56	VSS_137	AU7	BH1	VSS_218	VSS_299	BM9	D26	VSS_380	VSS_464	K7	D26	VSS_380	VSS_464	K7
AH35	VSS_57	VSS_138	AU8	BH10	VSS_219	VSS_300	BN12	D28	VSS_381	VSS_465	K8	D28	VSS_381	VSS_465	K8
AH36	VSS_58	VSS_139	AU9	BH11	VSS_220	VSS_301	BN14	D3	VSS_382	VSS_466	K9	D3	VSS_382	VSS_466	K9
AH6	VSS_59	VSS_140	AV37	BH12	VSS_221	VSS_302	BN18	D30	VSS_383	VSS_467	L29	D30	VSS_383	VSS_467	L29
AJ1	VSS_60	VSS_141	AV38	BH14	VSS_222	VSS_303	BN19	D33	VSS_384	VSS_468	L30	D33	VSS_384	VSS_468	L30
AJ13	VSS_61	VSS_142	AW1	BH2	VSS_223	VSS_304	BN2	D6	VSS_385	VSS_469	L33	D6	VSS_385	VSS_469	L33
AJ2	VSS_62	VSS_143	AW12	BH3	VSS_224	VSS_305	BN20	D9	VSS_386	VSS_470	L34	D9	VSS_386	VSS_470	L34
AJ3	VSS_63	VSS_144	AW2	BH4	VSS_225	VSS_306	BN21	E34	VSS_387	VSS_471	M12	E34	VSS_387	VSS_471	M12
AJ37	VSS_64	VSS_145	AW29	BH5	VSS_226	VSS_307	BN24	E35	VSS_388	VSS_472	M13	E35	VSS_388	VSS_472	M13
AJ38	VSS_65	VSS_146	AW3	BH6	VSS_227	VSS_308	BN29	E38	VSS_389	VSS_473	N10	E38	VSS_389	VSS_473	N10
AJ4	VSS_66	VSS_147	AW30	BH7	VSS_228	VSS_309	BN30	E4	VSS_390	VSS_474	N11	E4	VSS_390	VSS_474	N11
AJ5	VSS_67	VSS_148	AW4	BH8	VSS_229	VSS_310	BN31	E9	VSS_391	VSS_475	N12	E9	VSS_391	VSS_475	N12
AJ6	VSS_68	VSS_149	U6	BH9	VSS_230	VSS_311	BN34	N3	VSS_392	VSS_476	N2	N3	VSS_392	VSS_476	N2
W4	VSS_69	VSS_150	V12	I2	VSS_231	VSS_312	P36	N33	VSS_393	VSS_477	BT8	N33	VSS_393	VSS_477	BT8
W5	VSS_70	VSS_151	V29	T3	VSS_232	VSS_313	R12	N34	VSS_394	VSS_478	BR9	N34	VSS_394	VSS_478	BR9
Y10	VSS_71	VSS_152	V30	T33	VSS_233	VSS_314	R29	N4	VSS_395	VSS_479		N4	VSS_395	VSS_479	
Y11	VSS_72	VSS_153	A14	T34	VSS_234	VSS_315	R3	N5	VSS_396	VSS_480	A3	N5	VSS_396	VSS_480	A3
Y13	VSS_73	VSS_154	AD7	T4	VSS_235	VSS_316	R9	N6	VSS_397	VSS_481	A34	N6	VSS_397	VSS_481	A34
Y14	VSS_74	VSS_155	V6	T5	VSS_236	VSS_317	R30	N7	VSS_398	VSS_482	A4	N7	VSS_398	VSS_482	A4
Y37	VSS_75	VSS_156	W1	T7	VSS_237	VSS_318	R30	N8	VSS_399	VSS_483	B3	N8	VSS_399	VSS_483	B3
Y38	VSS_76	VSS_157	W12	T8	VSS_238	VSS_319	T10	N9	VSS_400	VSS_484	B37	N9	VSS_400	VSS_484	B37
Y7	VSS_77	VSS_158	W2	T9	VSS_239	VSS_320	T11	P12	VSS_401	VSS_485	BR38	P12	VSS_401	VSS_485	BR38
Y8	VSS_78	VSS_159	W3	U37	VSS_240	VSS_321	T12	P37	VSS_402	VSS_486	BT3	P37	VSS_402	VSS_486	BT3
Y9	VSS_79	VSS_160	W33	U38	VSS_241	VSS_322	T13	M14	VSS_403	VSS_487	BT35	M14	VSS_403	VSS_487	BT35
AK29	VSS_80	VSS_161	W34	U39	VSS_242	VSS_323	T14	M6	VSS_404	VSS_488	BT36	M6	VSS_404	VSS_488	BT36
AK30	VSS_81	VSS_162		U40	VSS_243	VSS_324		N1	VSS_405	VSS_489	BT4	N1	VSS_405	VSS_489	BT4

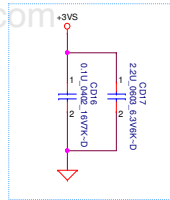
CFL-H_BGA1440

CFL-H_BGA1440

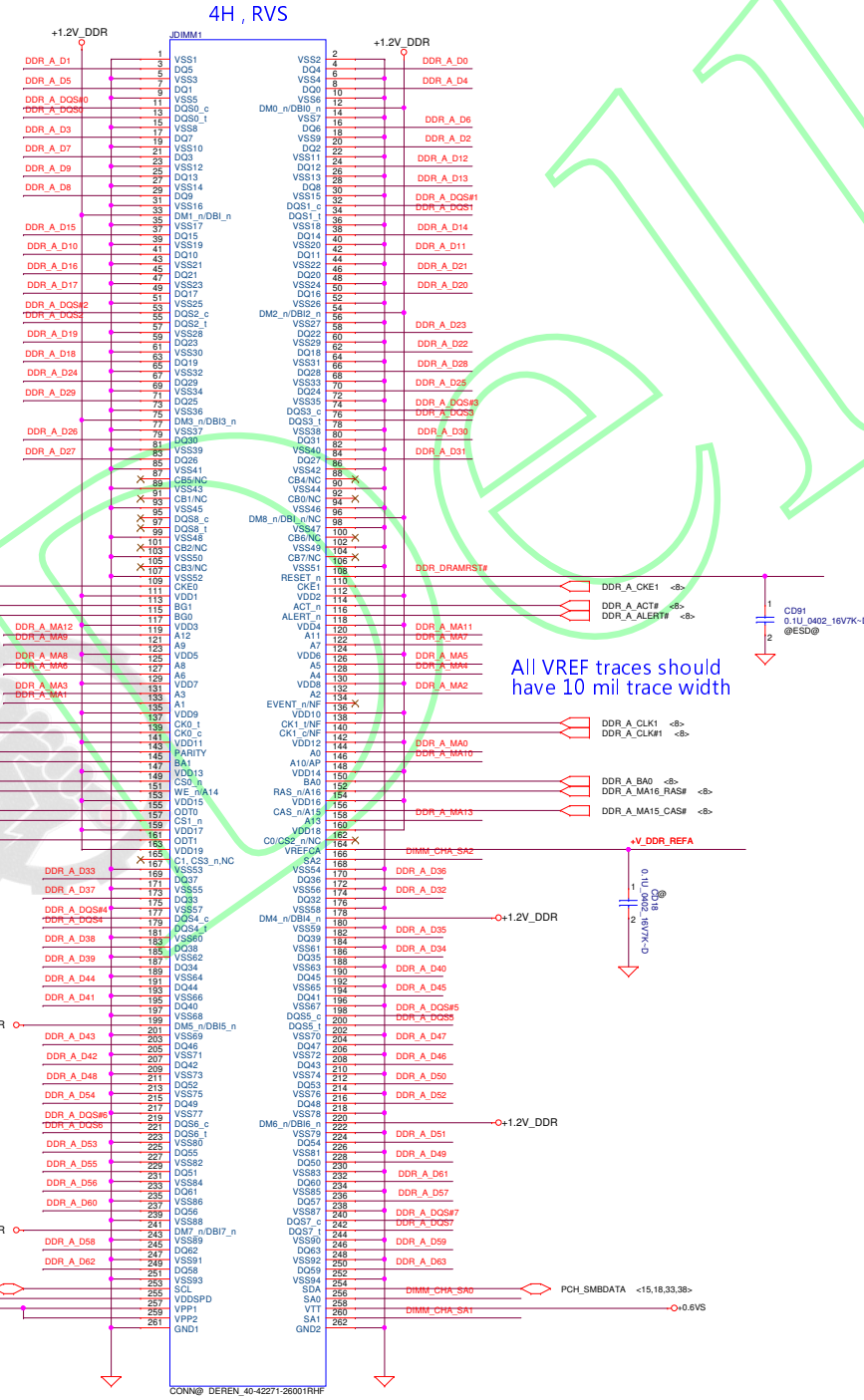
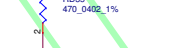
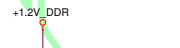
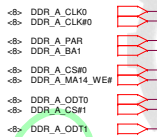
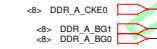
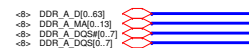
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				Size	Document Number	Rev
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Date: Wednesday, February 07, 2018				Sheet	13	of 82

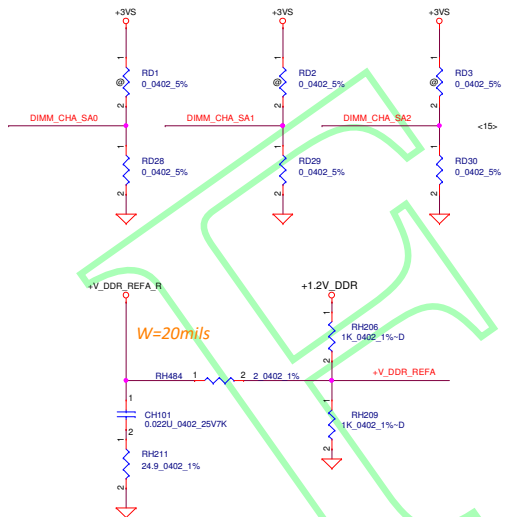
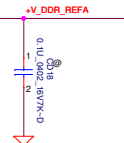
Layout Note:
Place near JDIMM1.255



The schematic diagram illustrates the power supply section of the PCB, featuring two +1.2V DDR power planes. The top plane is connected to a +1.2V_VDDR input and contains decoupling capacitors CD1 through CD7. The bottom plane is connected to a +1.2V_DDR input and contains decoupling capacitors CD5 through CD11. Each capacitor is labeled with its value, tolerance, and manufacturer part number (e.g., 10µ 0.05%, 3.3VW4-D).



All VREF traces should have 10 mil trace width

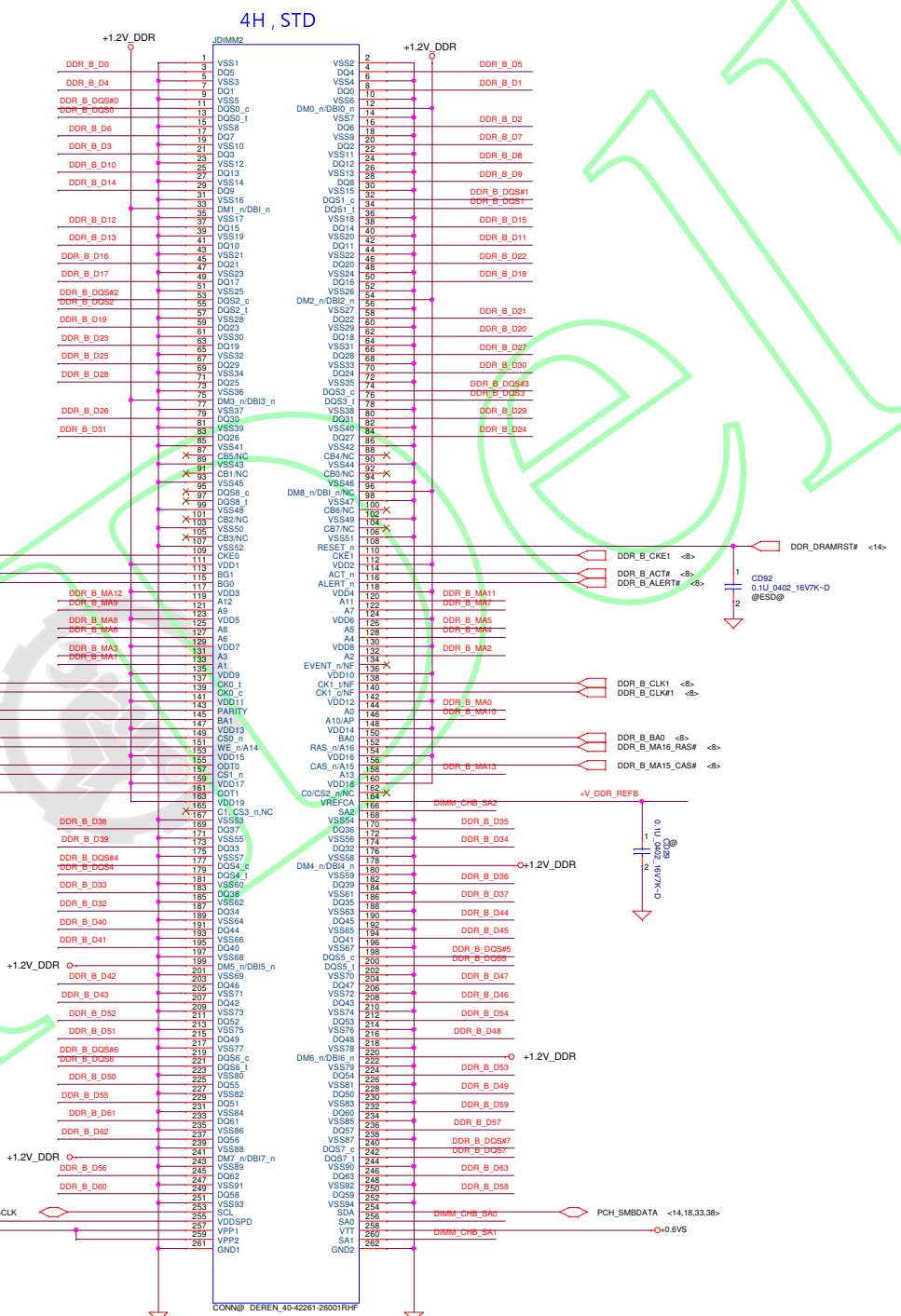
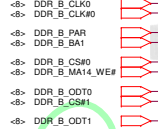
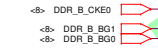
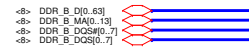


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The circuit diagram shows a 4-bit DAC implemented with an op-amp buffer and four resistors. The input is a 0.6V source. The resistors are labeled: CD02 (10.000, 5.356M-D), CD09 (10.000, 5.356M-D), CD08 (10.000, 5.356M-D), and CD06 (10.000, 5.356M-D). The output is connected to a 0.6V source.

A circuit diagram showing a voltage divider. A +3V source is connected to the top terminal of a resistor network. The network consists of two capacitors in series: CD04 (0.1uF, 50V, K) and CD05 (220uF, 25V, K). The bottom terminal of the network is connected to ground. The output voltage is taken from the node between the two capacitors.

The diagram illustrates the DDR3 memory bank structure, showing two rows of memory modules connected to a +1.2V_DDR power supply. The top row contains modules CD29 through CD38, and the bottom row contains modules CD39 through CD48. Each module is represented by a rectangle with pins 1 and 2. The modules are connected to a common power rail. A capacitor CD33 (220uF, 2VMM, R6M) is connected between the power rail and ground.



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S IC A31 FHSSKU04 QNDO A1 BGA 874P PCH-H
SA0000B40L
CPCHE9@



S IC A31 FHCM246 QNYJ B0 BGA 874P PCH-H
SA0000B60L
CPCHE9@

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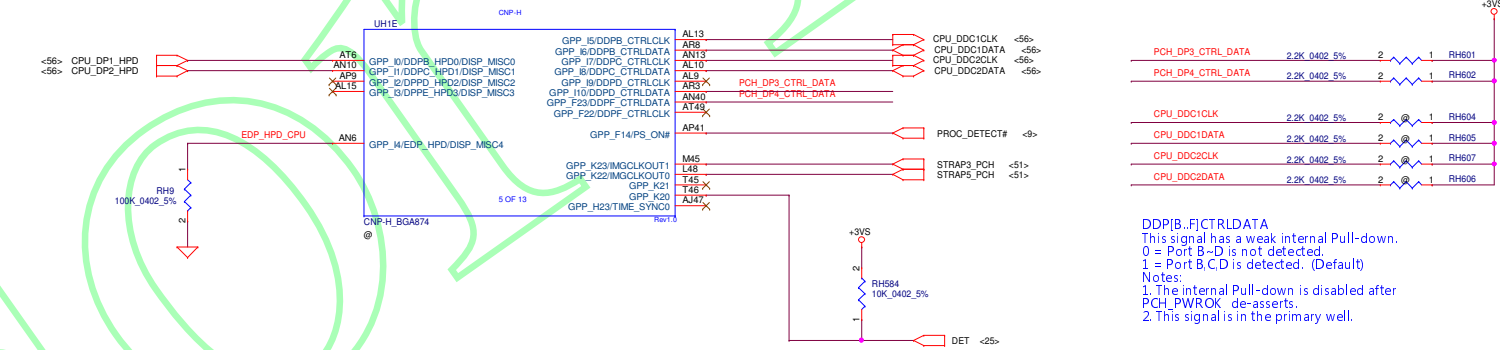
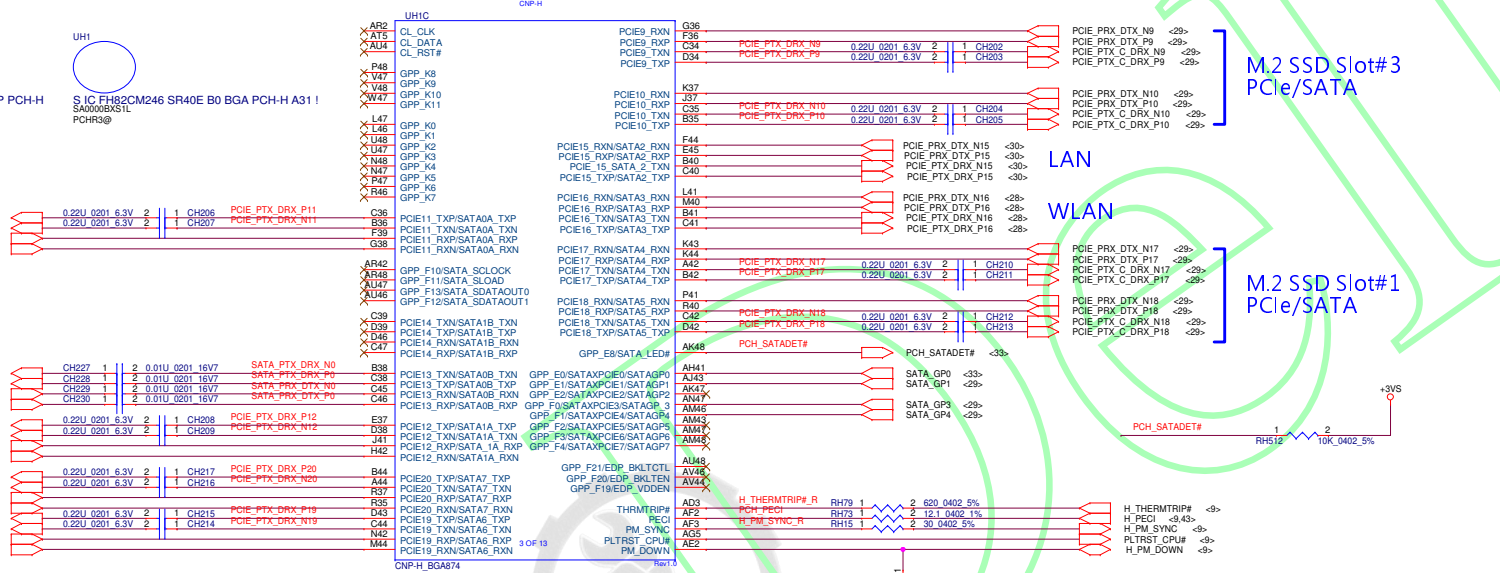
S IC FH82CM246 SR40E B0 BGA PCH-H A31 I
SA0000BXSIL
PCHR3@

M.2 SSD Slot#3
PCIe/SATA

SATA HDD

M.2 SSD Slot#3
PCIe/SATA

M.2 SSD Slot#1
PCIe/SATA

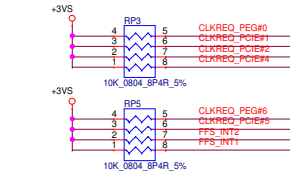


DDPB_FICTRLDATA
This signal has a weak internal Pull-down.
0 = Port B-D is not detected.
1 = Port B-C-D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after PCH_PWR_OK de-asserts.
2. This signal is in the primary well.

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LA-F551P				
Date: Tuesday, March 06, 2018				

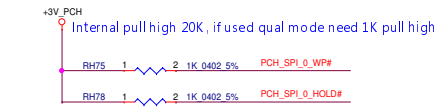
Net : XCLK_BIASREF
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil

PEG(dGPU)
SSD1
SSD2
Thunderbolt
LAN
WLAN
Caldera
SSD3

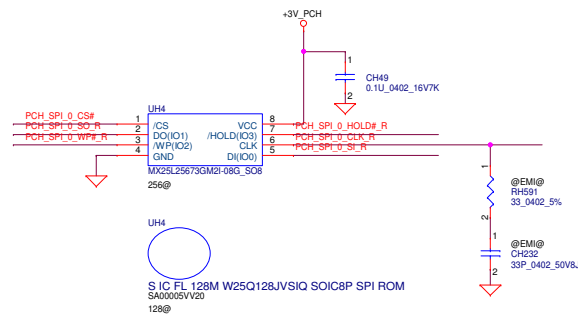
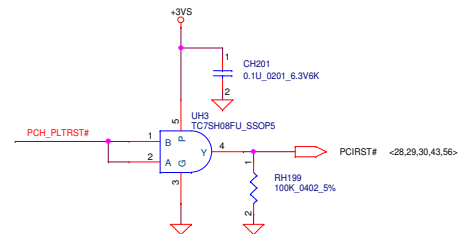
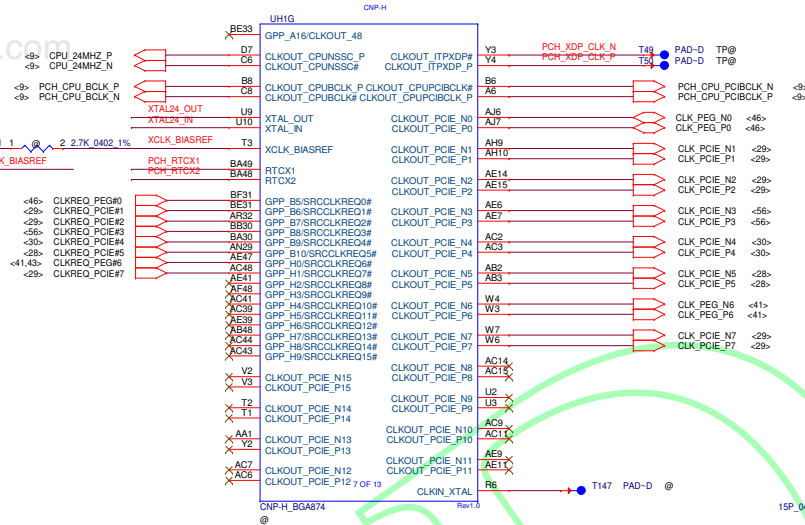
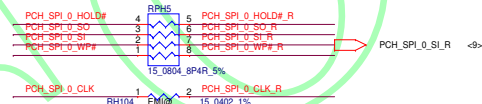


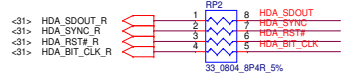
#571182_CNL_PCH_H_EDS_V1_Rev0.7
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
5711007_CFL_MOW_Archive_WW22_2017
STUFF R on GPP_H15

RH1 close to UH4

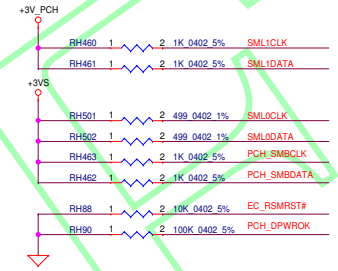
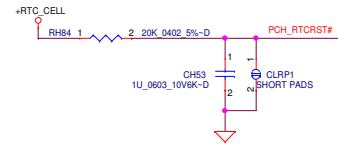
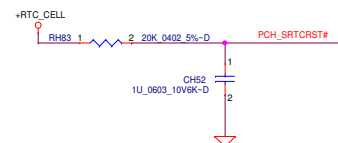


This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Notes:
1. This signal is in the primary well.
Warning: This strap must be configured to 0 if the esPI or LPC strap is configured to 0.

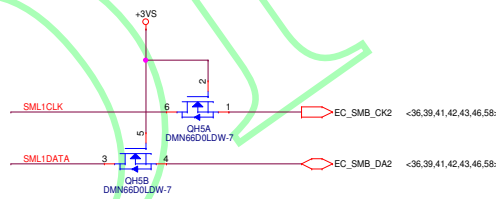




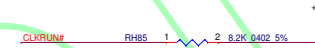
This signal has a weak internal Pull-down.
 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
 Notes:
 1. The internal Pull-down is disabled after RSMRST# de-asserts.
 2. This signal is in the primary well.



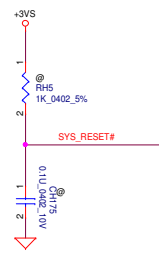
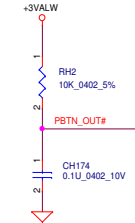
CLRP1 in DIMM door

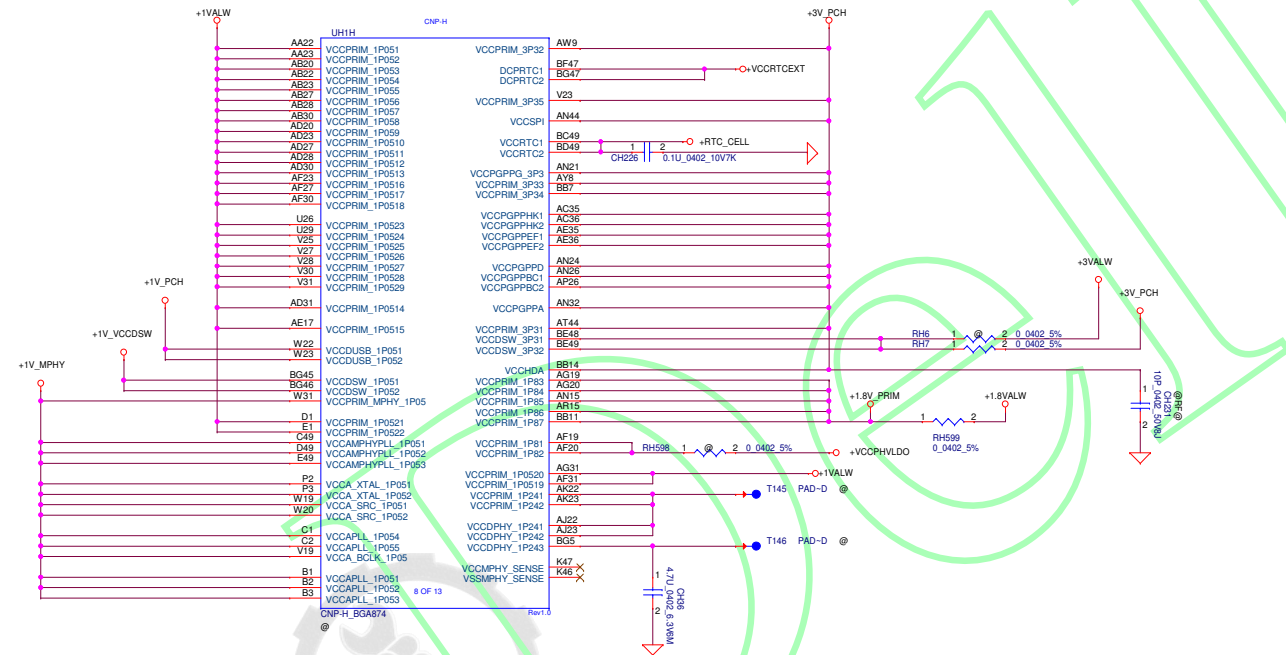


This signal has an internal pull-down.
 0 = Disable Intel DCI-OOB (Default)
 1 = Enable Intel DCI-OOB
 1. The internal pull-down is disabled after RSMRST# de-asserts.
 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.



Top Swap Override
 0 = Disable 'Top Swap', mode (Default)
 1 = Enable 'Top Swap', mode
 The internal Pull-down is disabled after PCH_PWROK is high.

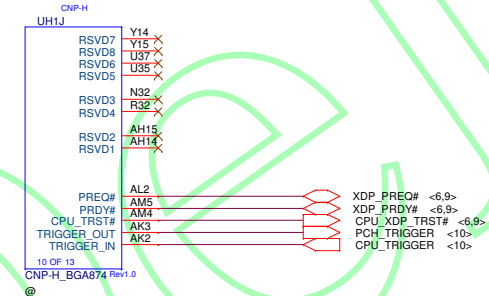
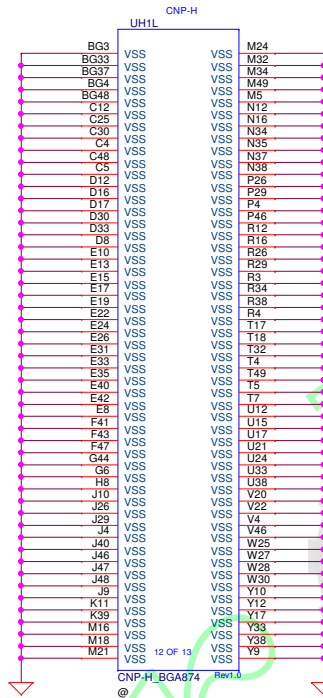
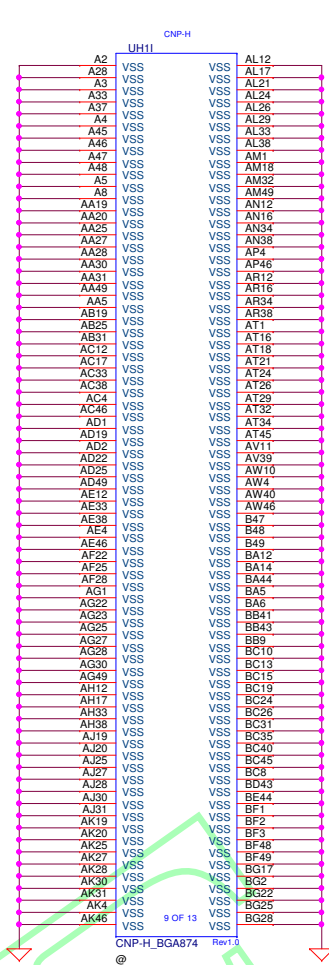




Close to AC35,AC36

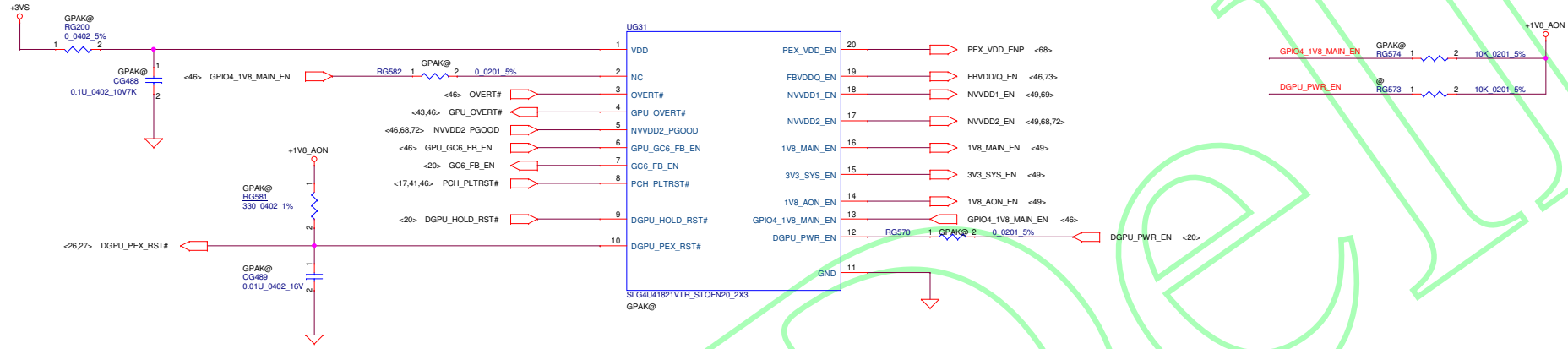
Close to AG19,AG20
,AR15,AN15,BB11

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					LA-F551P	0.3	
				Date:	Wednesday, February 07, 2018	Sheet	22 of 82

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PR801
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SD028000080
NGPAK@

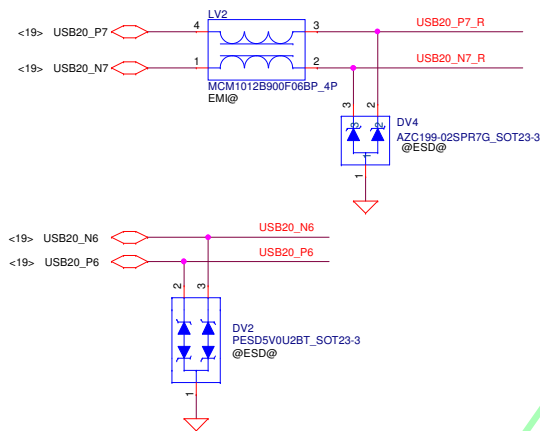
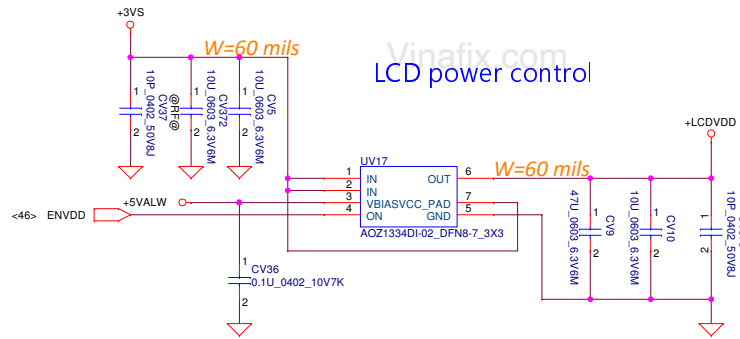
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GPAK@

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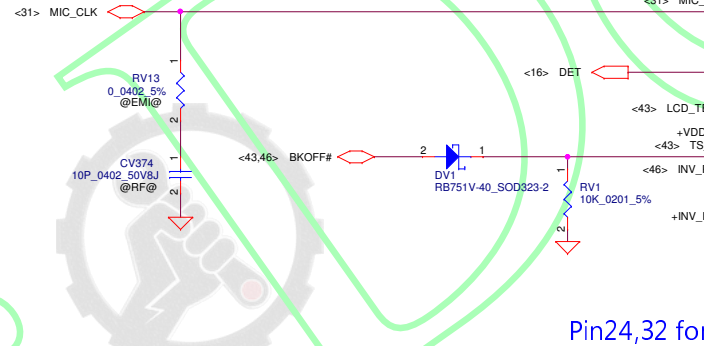
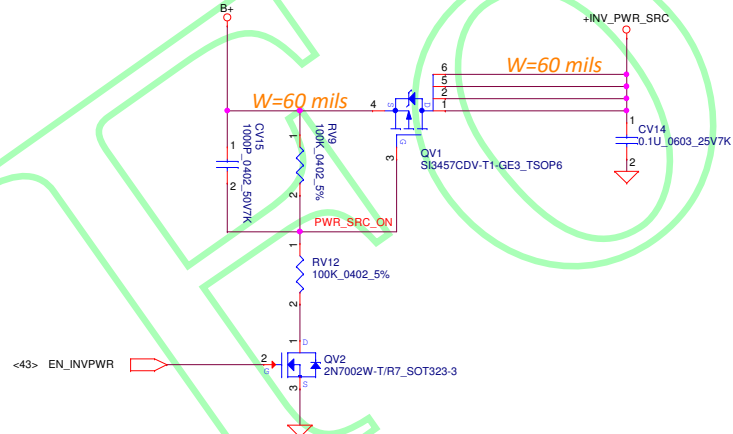


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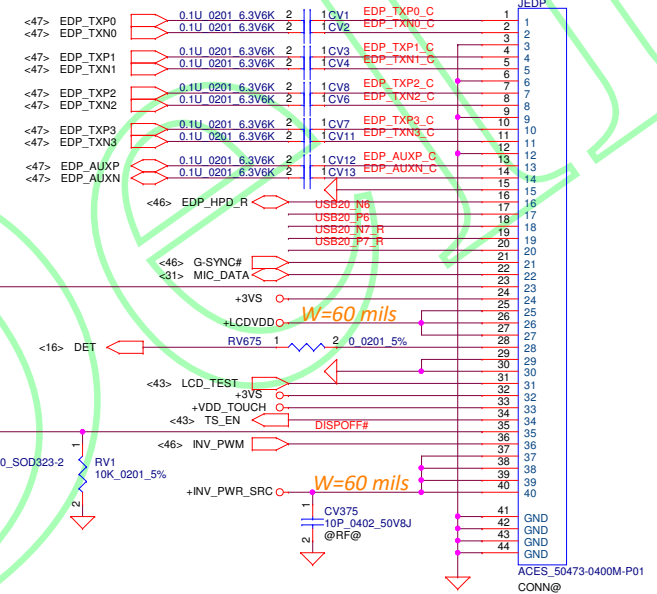
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LCD backlight power control



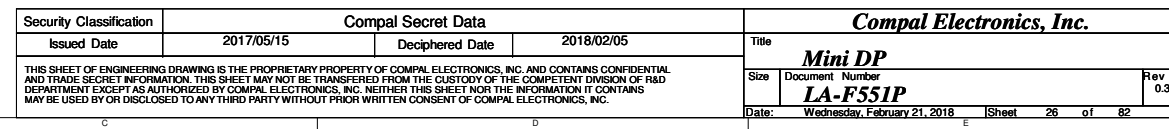
Touch screen panel power

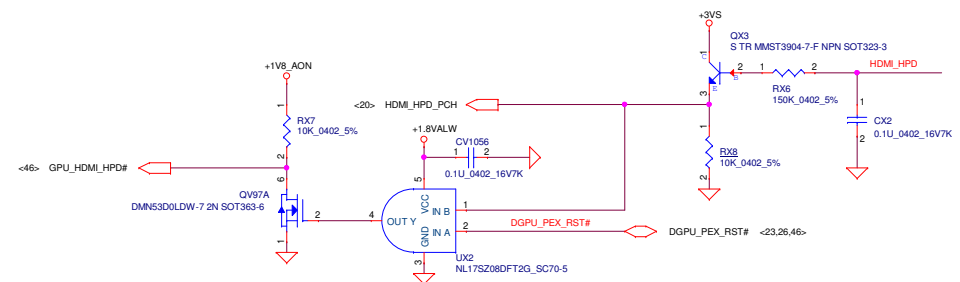
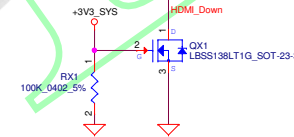
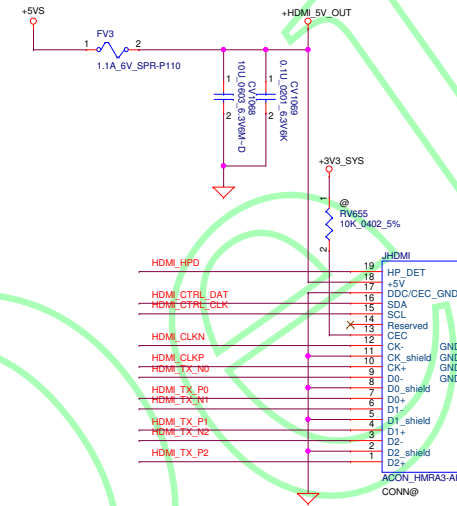


Pin24,32 for Camera power

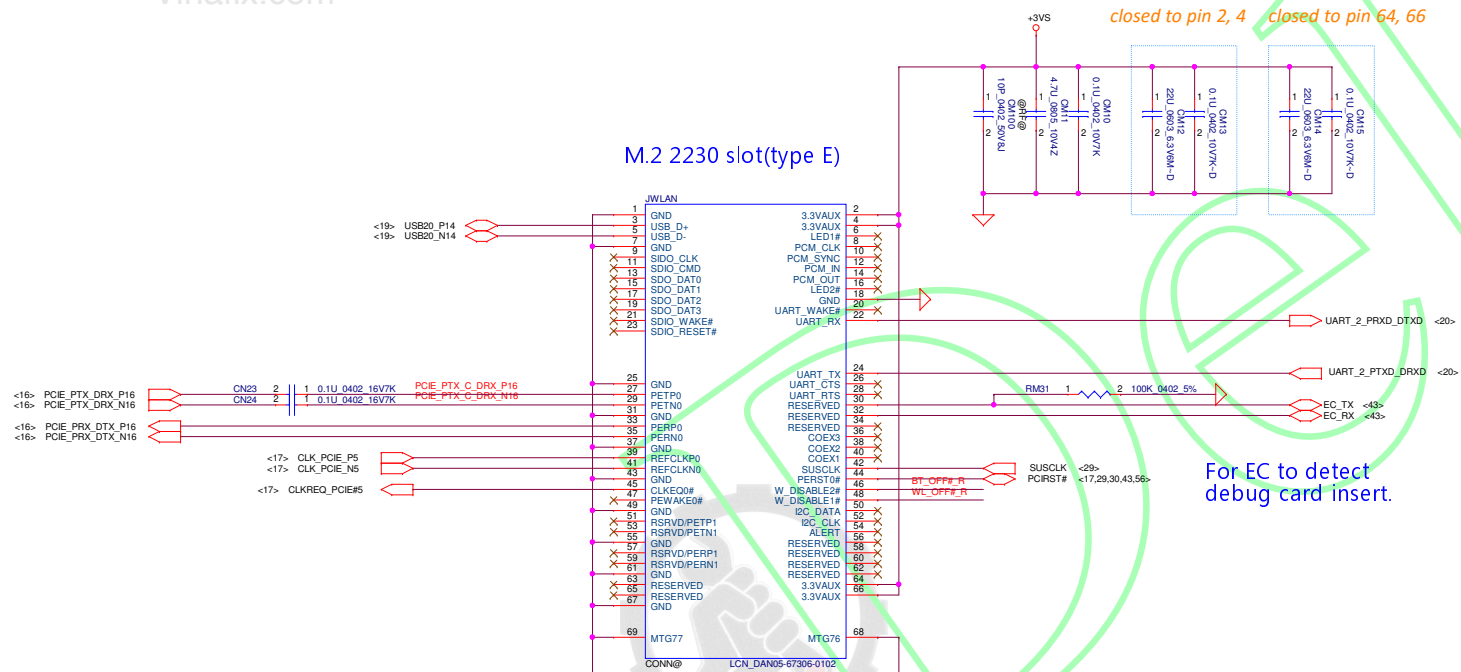
IR camera pindefine :
 IR_LED+
 IR_LED-
 IR_LED+/NC
 IR_LED-/DET , connect to PCH GPIO
 IR_LED-
 IR_LED-
 Diglog_loop , connect to PCH GPIO
 DGND
 D+
 D-
 USB3V3
 MIC_SIG
 MIC_CLK
 DGND

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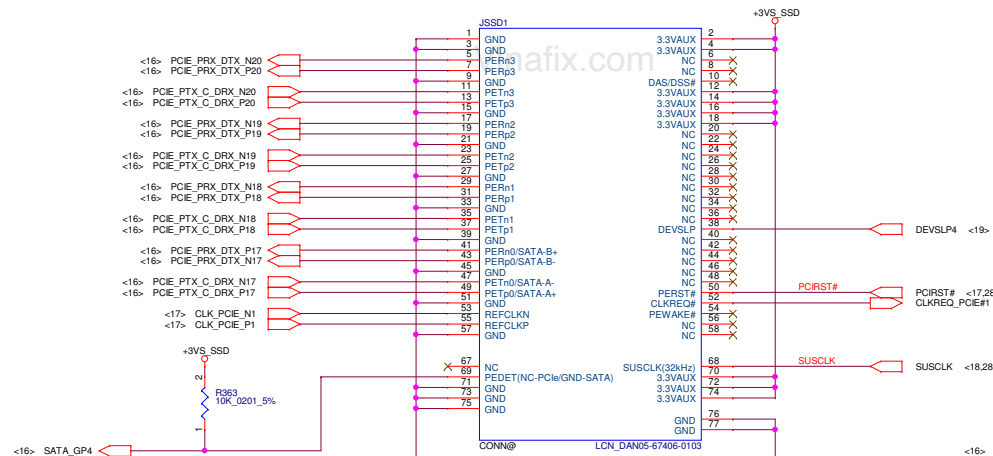


For EC to detect
debug card insert.

Prevent backdriver from +3VS_WLAN_NGFF to +3VS

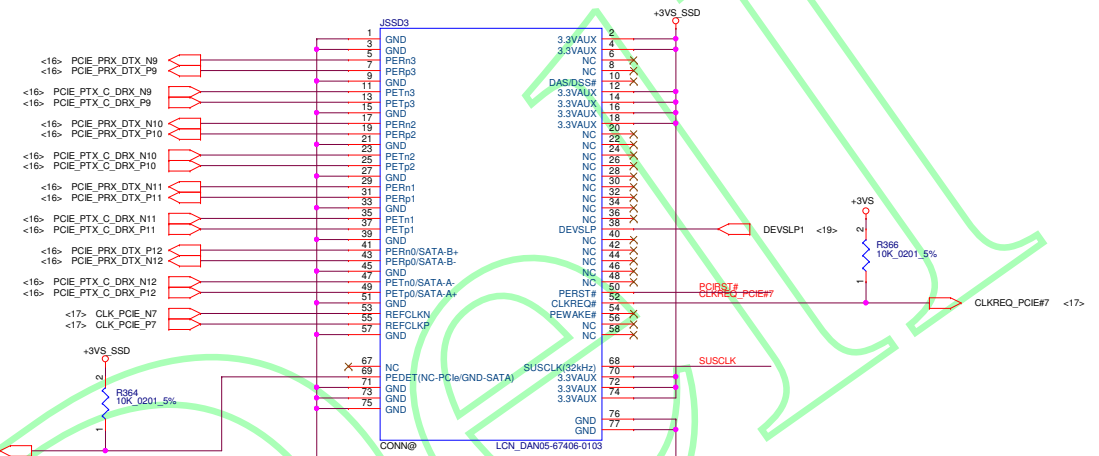
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PCIe / SATA SSD JSSD1, 2242

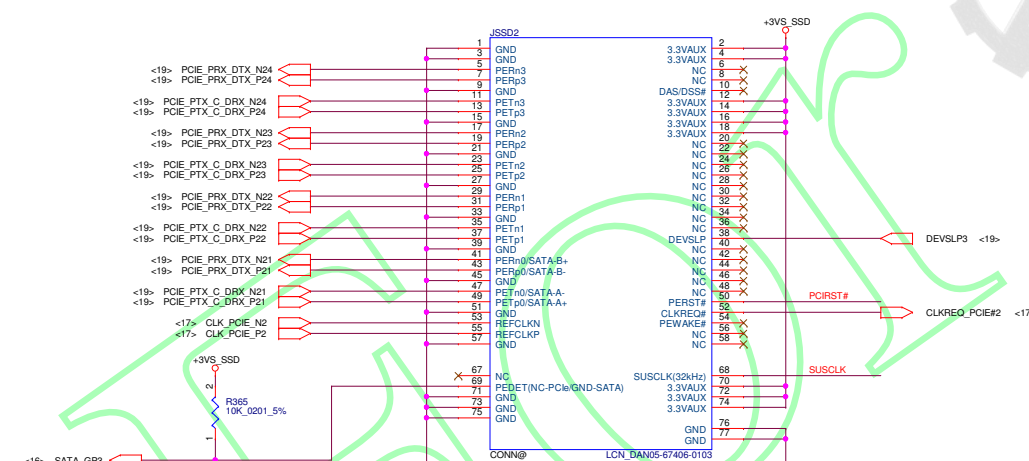


PEDET	Module Type
0	SATA
1	PCIe

PCIe / SATA SSD JSSD3, 2280



PCIe SSD JSSD2, 2280

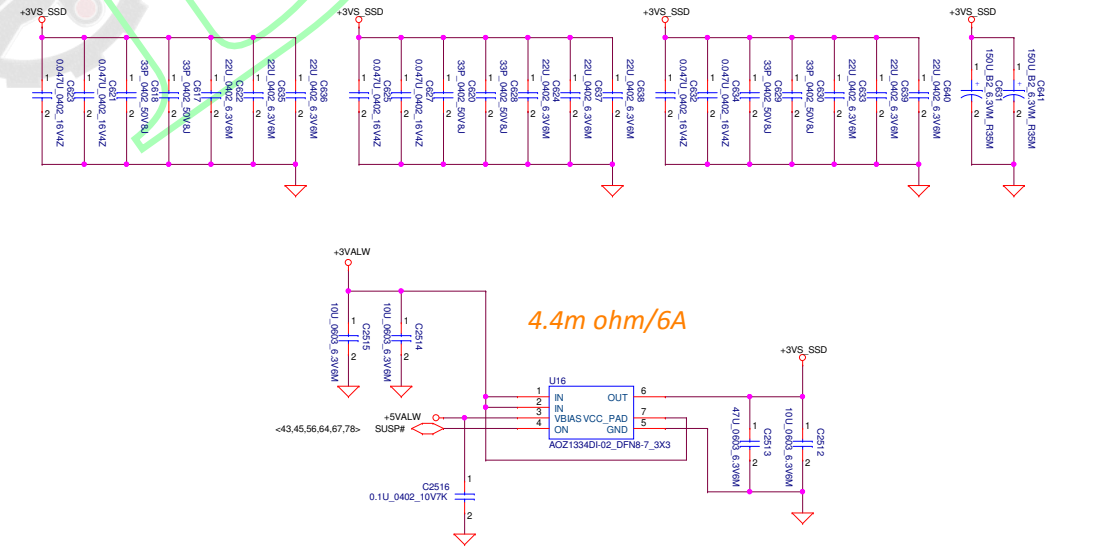


PEDET	Module Type
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1	PCIe

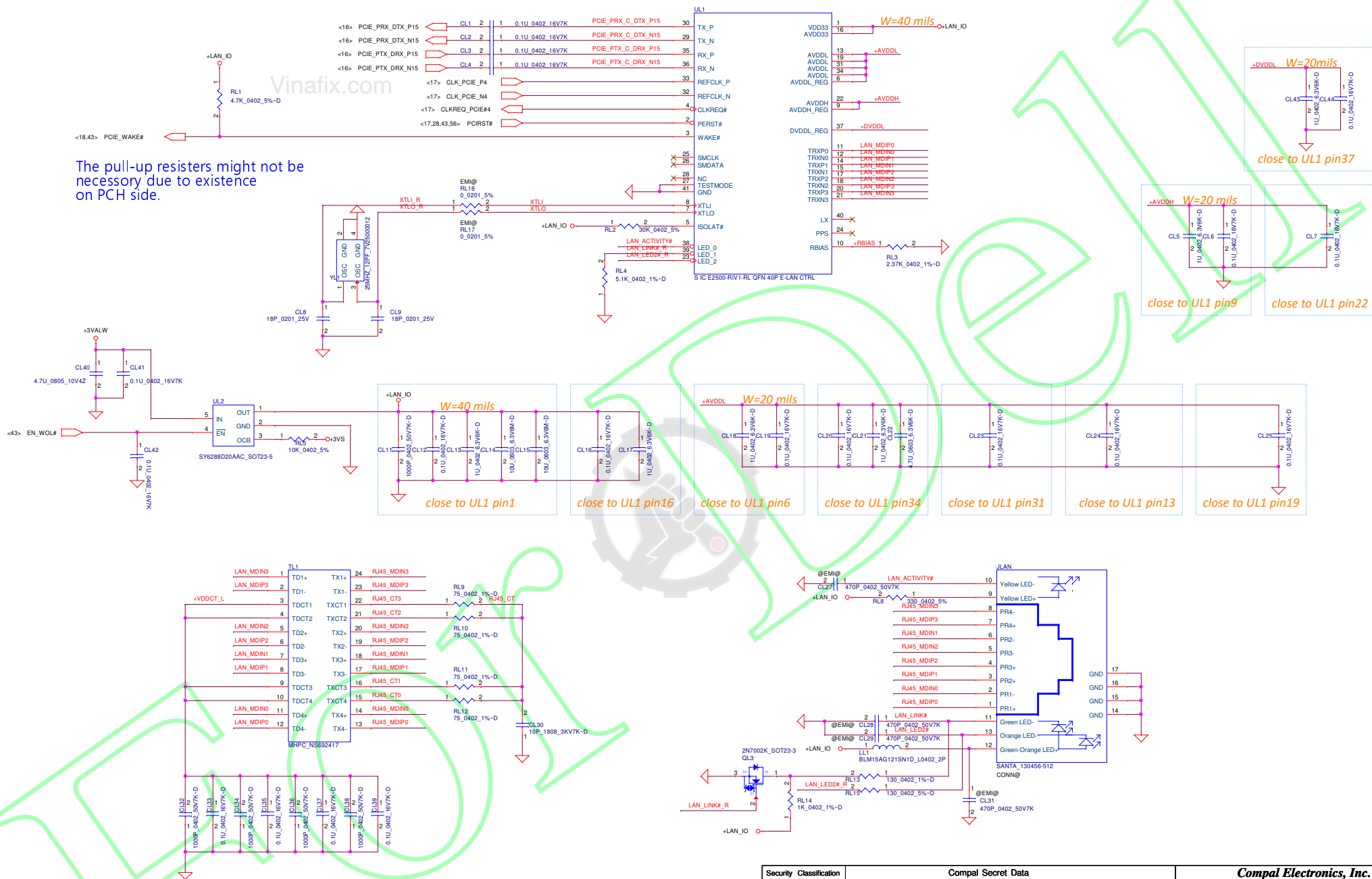
JSSD1

JSSD2

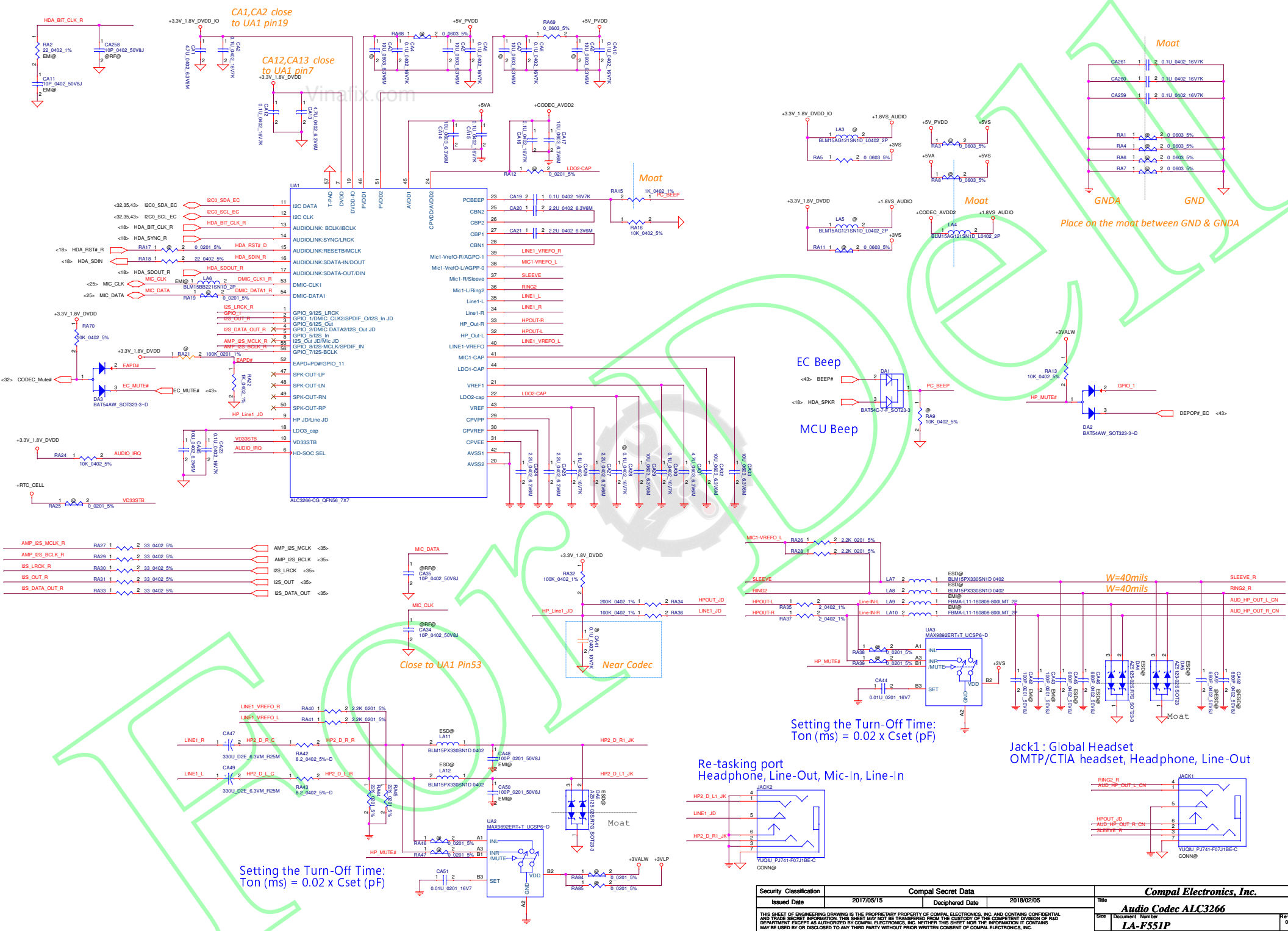
JSSD3



The pull-up resistors might not be necessary due to existence on PCH side.



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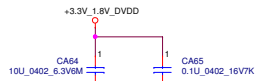
Setting the Turn-Off Time:
 $Ton (ms) = 0.02 \times Cset (pF)$

Jack1: Global Headset
OMTP/CTIA headset, Headphone, Line-Out

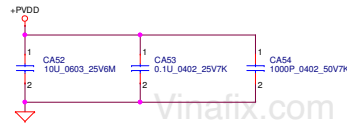
Re-tasking port
Headphone, Line-Out, Mic-In, Line-In

Setting the Turn-Off Time:
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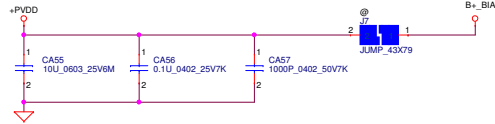
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31		of		82	



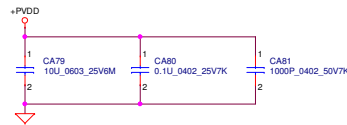
CA64, CA65 close to PIN16



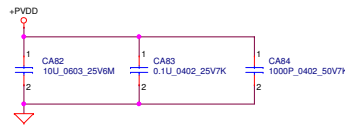
CA52, CA53 and CA54 close to PIN1,56



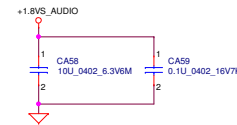
CA55, CA56 and CA57 close to PIN42,43



CA79, CA80 and CA81 close to PIN51



CA82, CA83 and CA84 close to PIN48



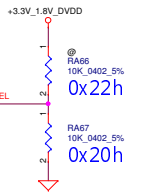
CA58, CA59 close to PIN17



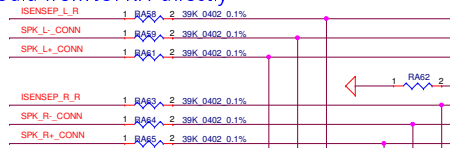
CA60 close to PIN21



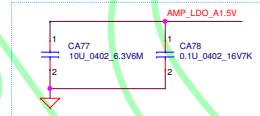
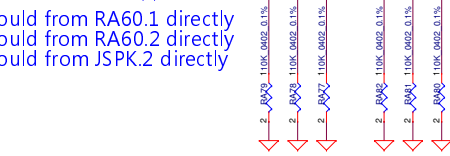
CA61, CA62 and CA63 close to PIN37



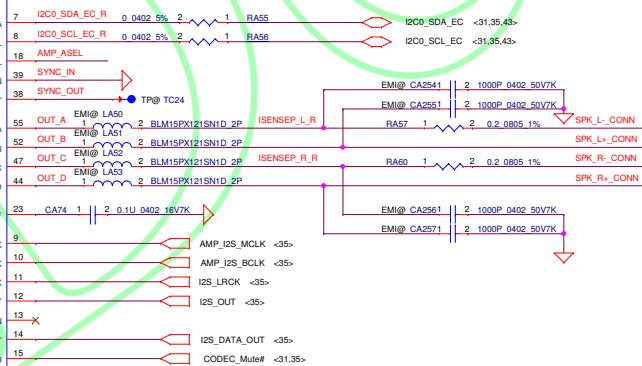
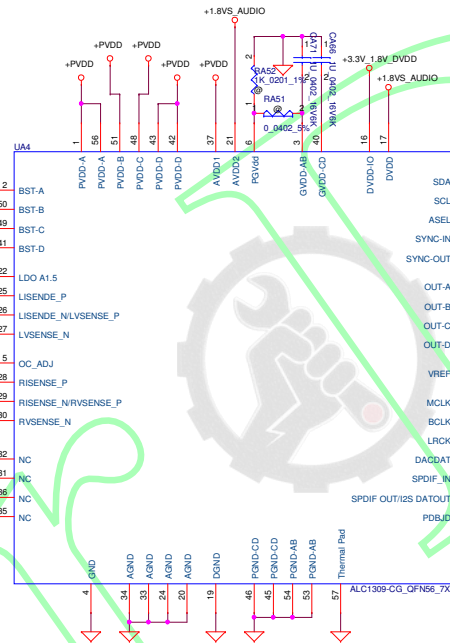
RA58.1 should from RA57.1 directly
RA59.1 should from RA57.2 directly
RA61.1 should from JSPK.4 directly



RA63.1 should from RA60.1 directly
RA64.1 should from RA60.2 directly
RA65.1 should from JSPK.2 directly

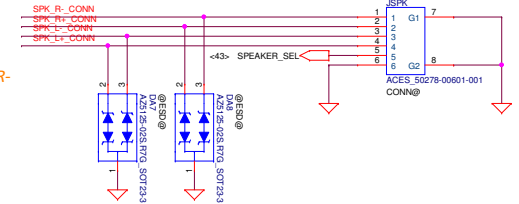


CA77, CA78 close to PIN22



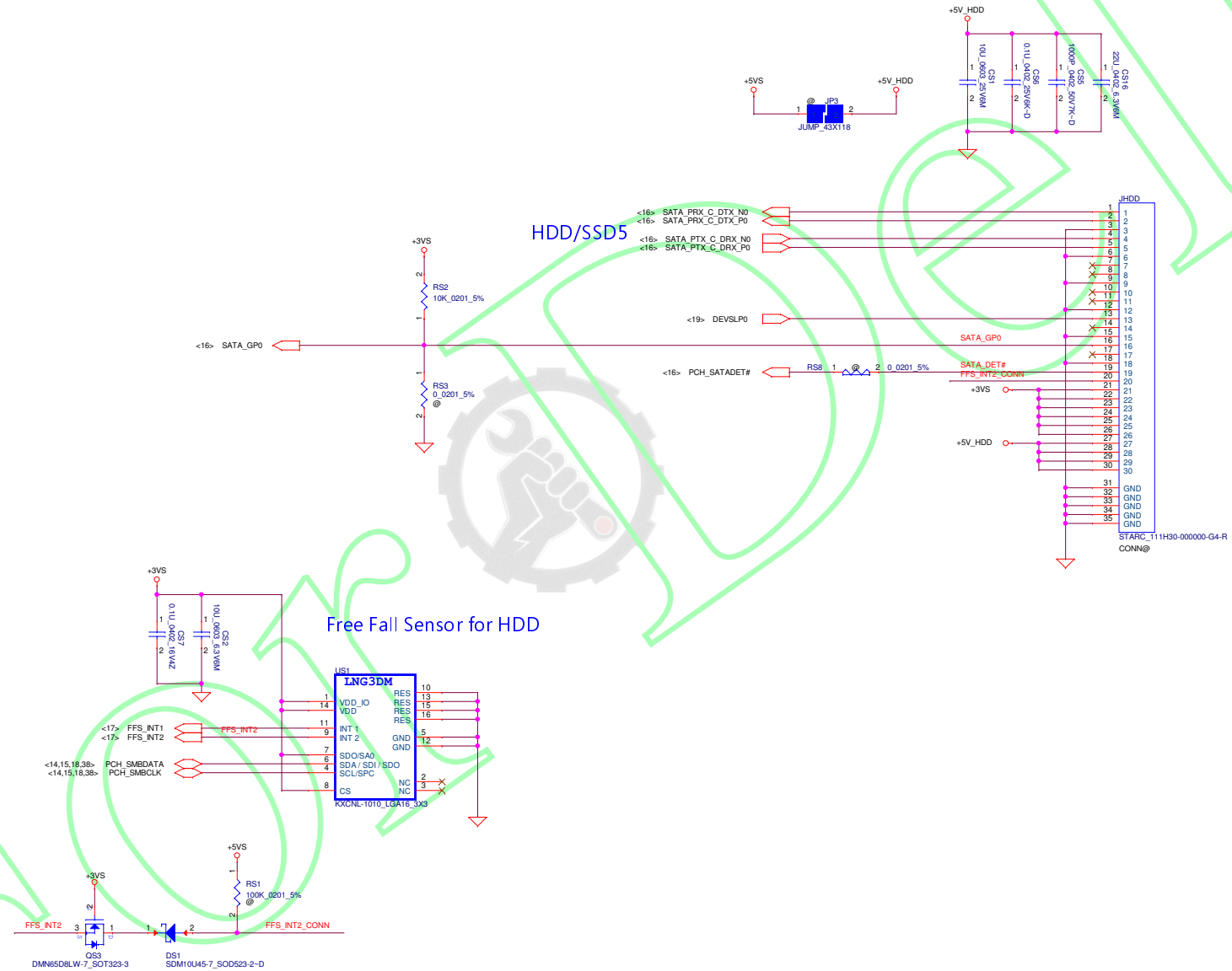
Close to UA4 Pin42,43,44,45
40 mils = For 4 ohm 3W Speaker

Int. Speaker Conn.

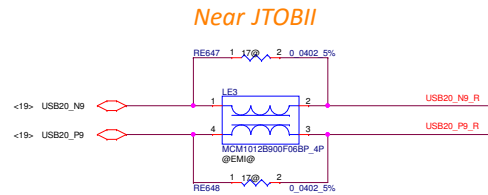


Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40 mil
Speaker 8 ohm : 20 mil

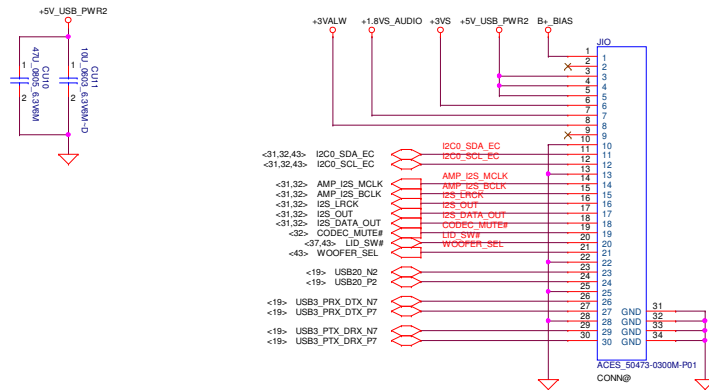
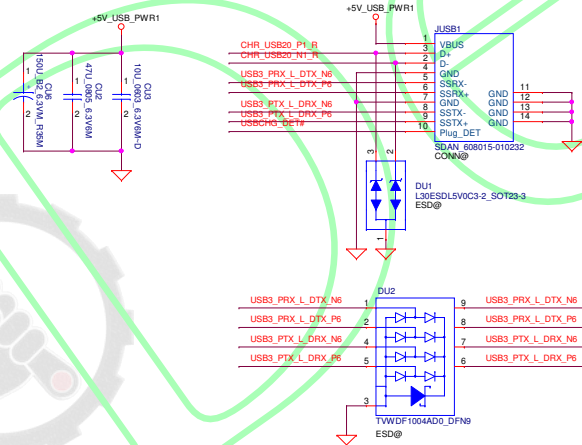
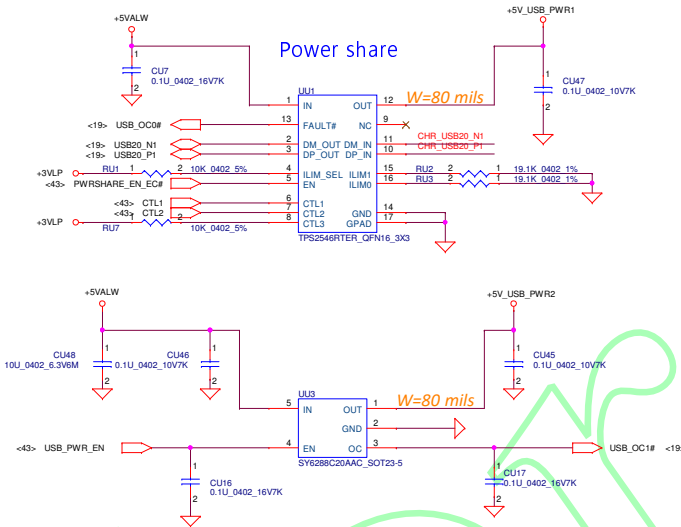
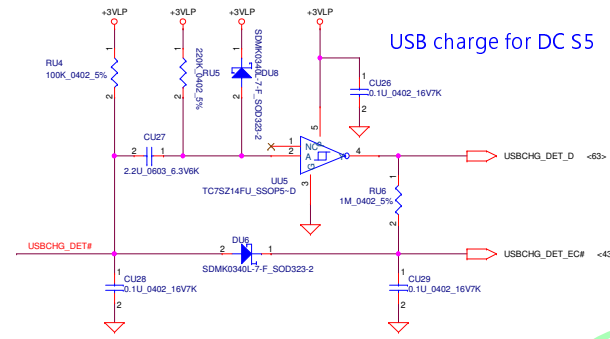
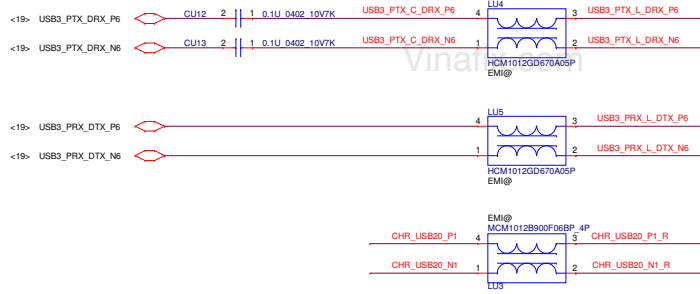
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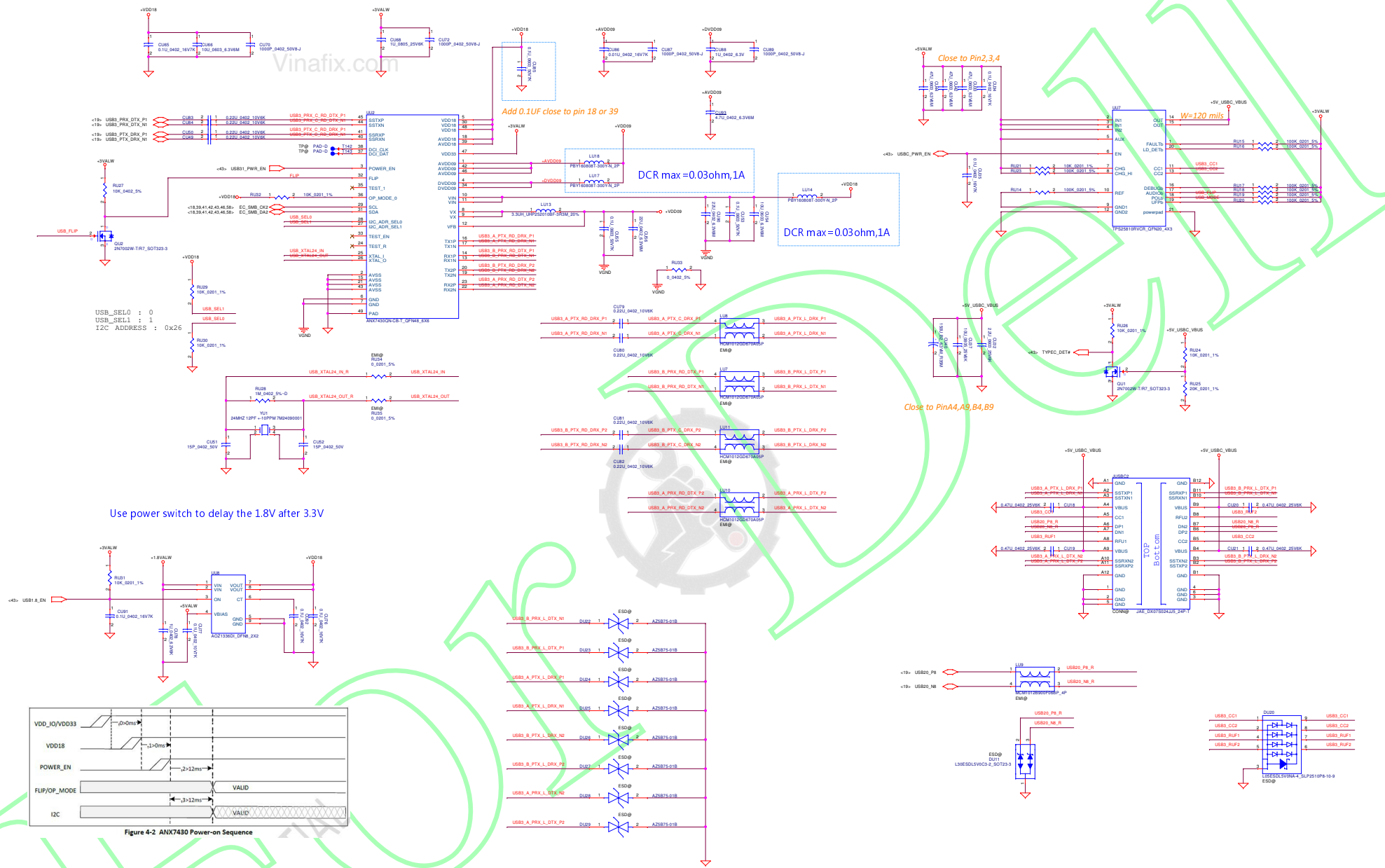
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Date:							Wednesday, February 21, 2018		Sheet 34 of 62	

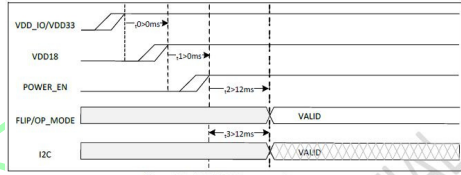


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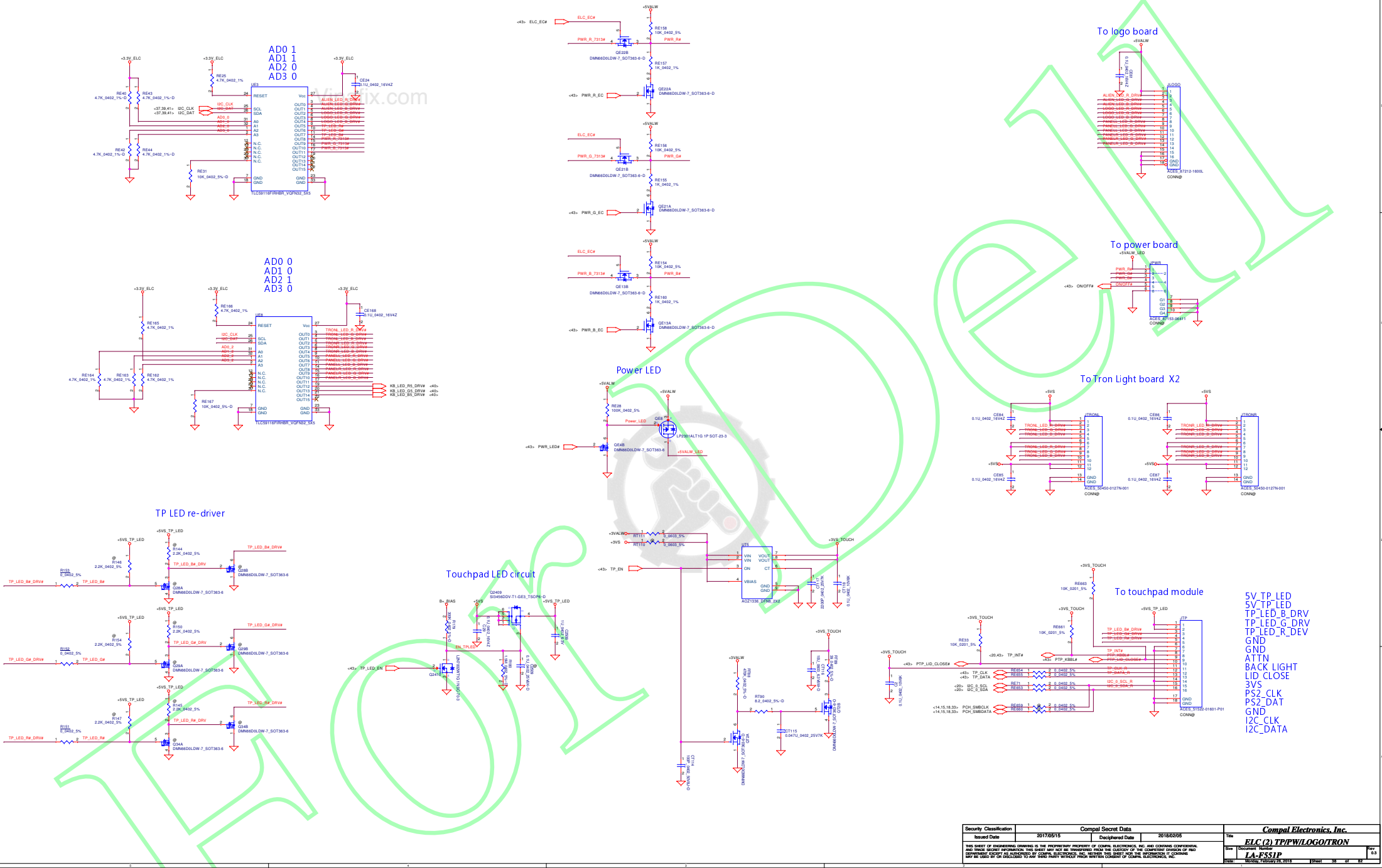


Use power switch to delay the 1.8V after 3.3V

Figure 4-2 ANX7430 Power-on Sequence



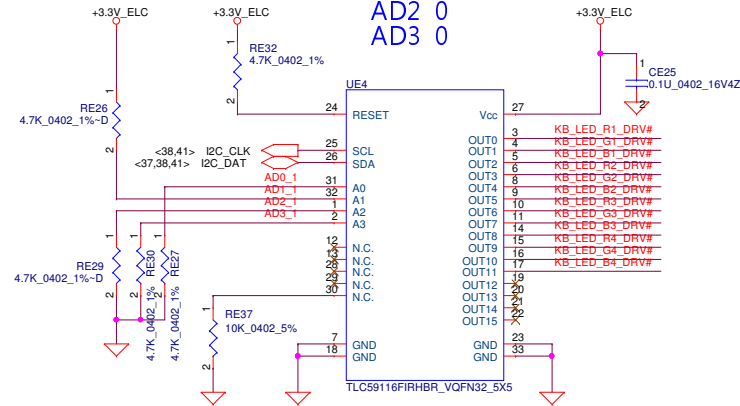
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LA-F551P					
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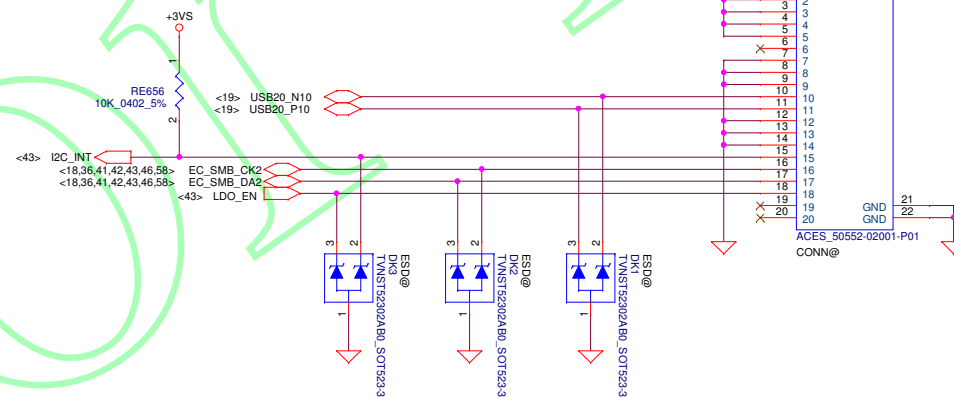
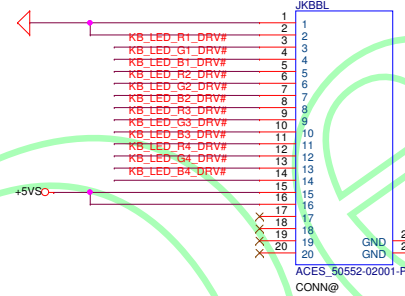
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				Rev	0.1
				Issue	Rev01, February 28, 2018
				Drawn	08
				Check	07
				Rev	0.1

KB Backlight.com

AD0 0
AD1 1
AD2 0
AD3 0



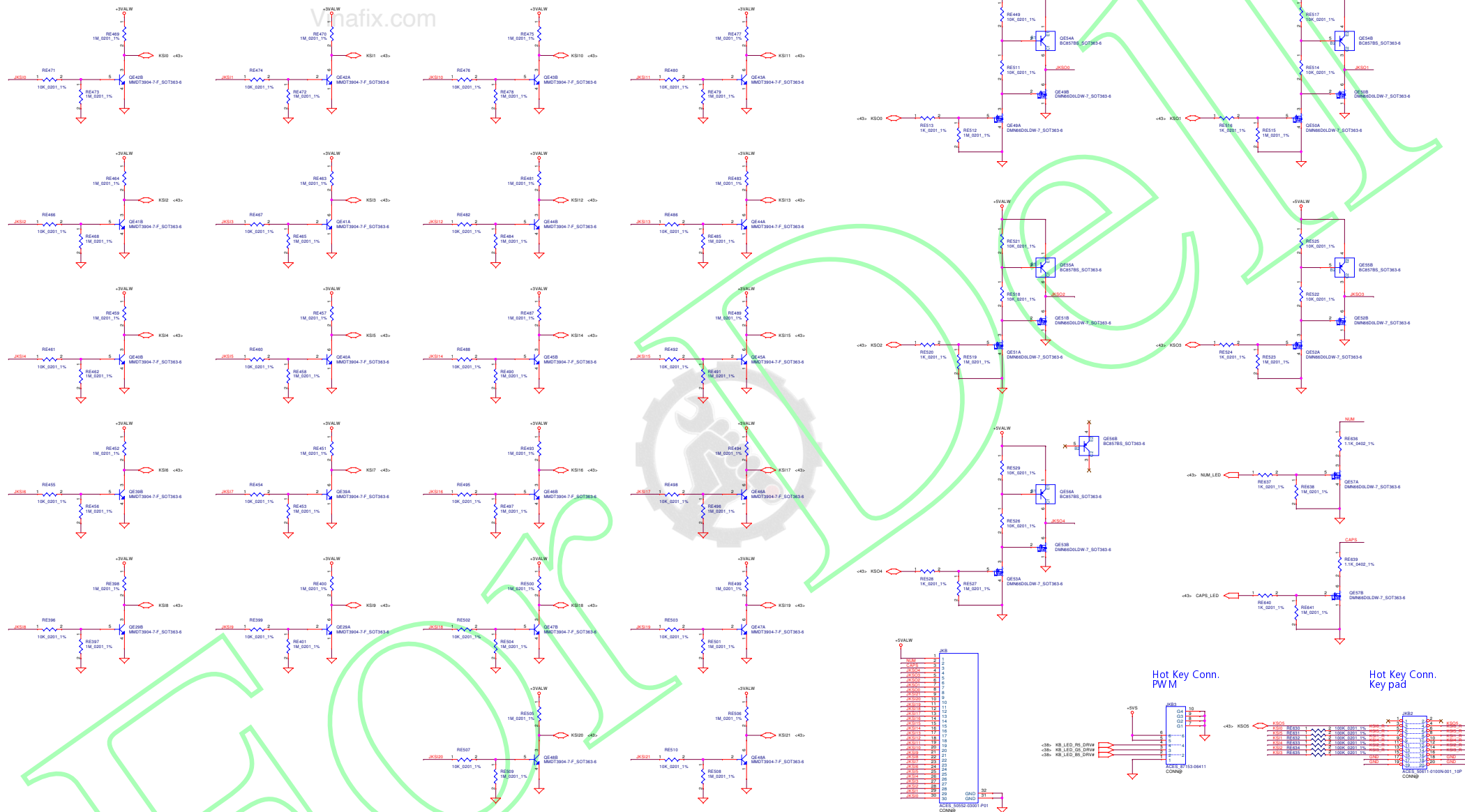
KB BL LED



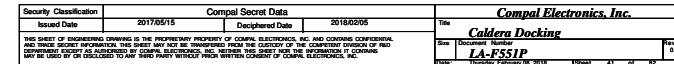
Per Key pin define

Pin1~5 VBUS
Pin6 NC
Pin7~9 GND
Pin10 D-
Pin11 D+
Pin12~14 GND
Pin15 I2C_INT
Pin16 I2C_CLK
Pin17 I2C_DAT
Pin18 LDO_EN
Pin19~20 NC

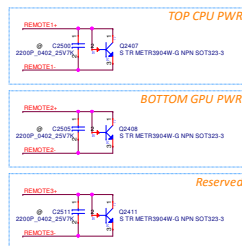
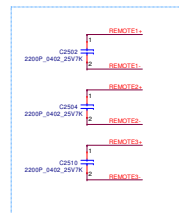
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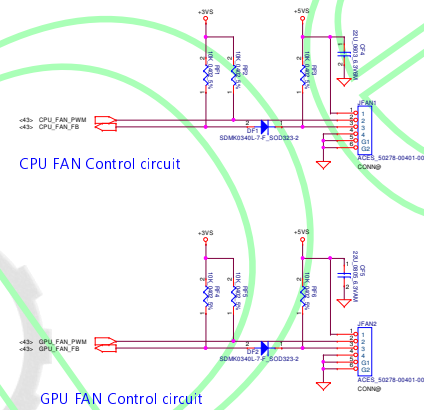
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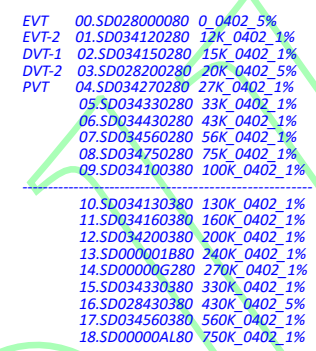


REMOTE1,2 (+/-) :
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Trace length:<8"



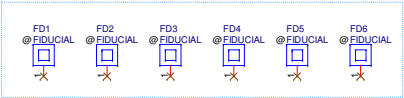
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<p>DATE: 15-February-2018</p>				<p>Sheet 42 of 53</p>		

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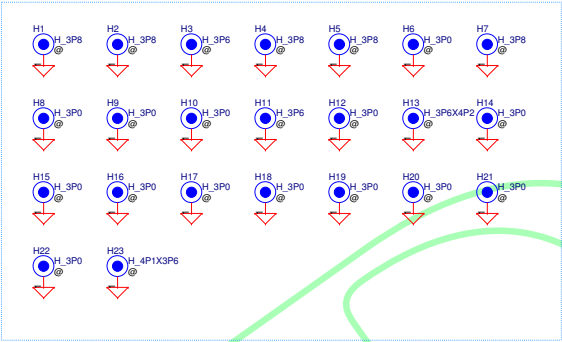


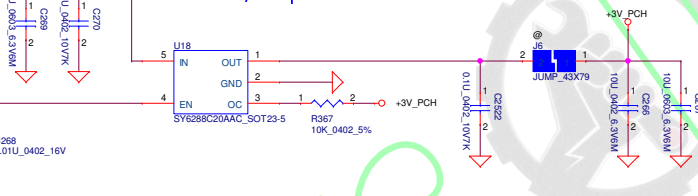
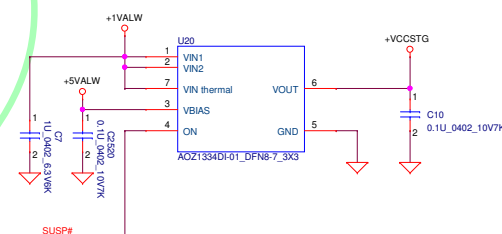
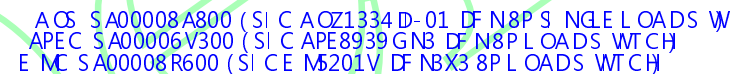
Security Classification	Compal Secret Data			Compal Electronics, Inc. EC ENE-KB9022		
Issued Date	2017/05/15	Deciphered Date	2018/02/05	Title		
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Fiducial Mark



PCB Screw Hole

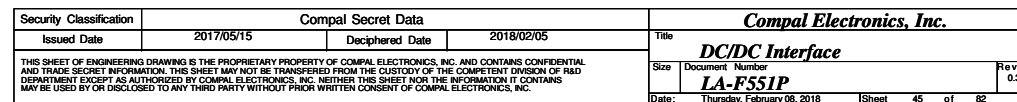


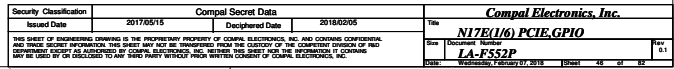


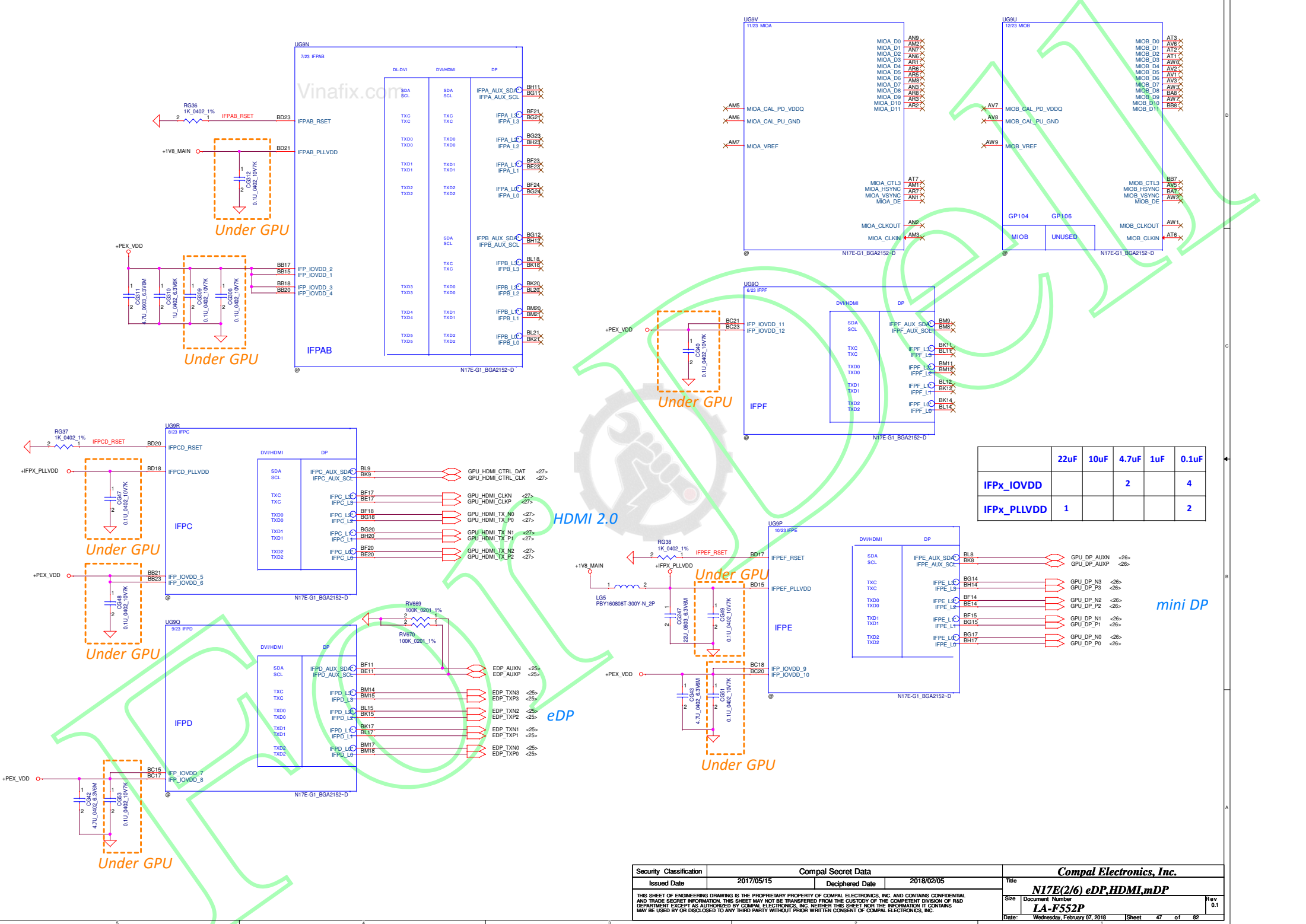
For meet tPLT17 & tCPU28 power down sequence.
tPLT17 : 1us (Max)
tCPU28 : 1us (Max)

- Main source
- 2nd source
- 3rd source

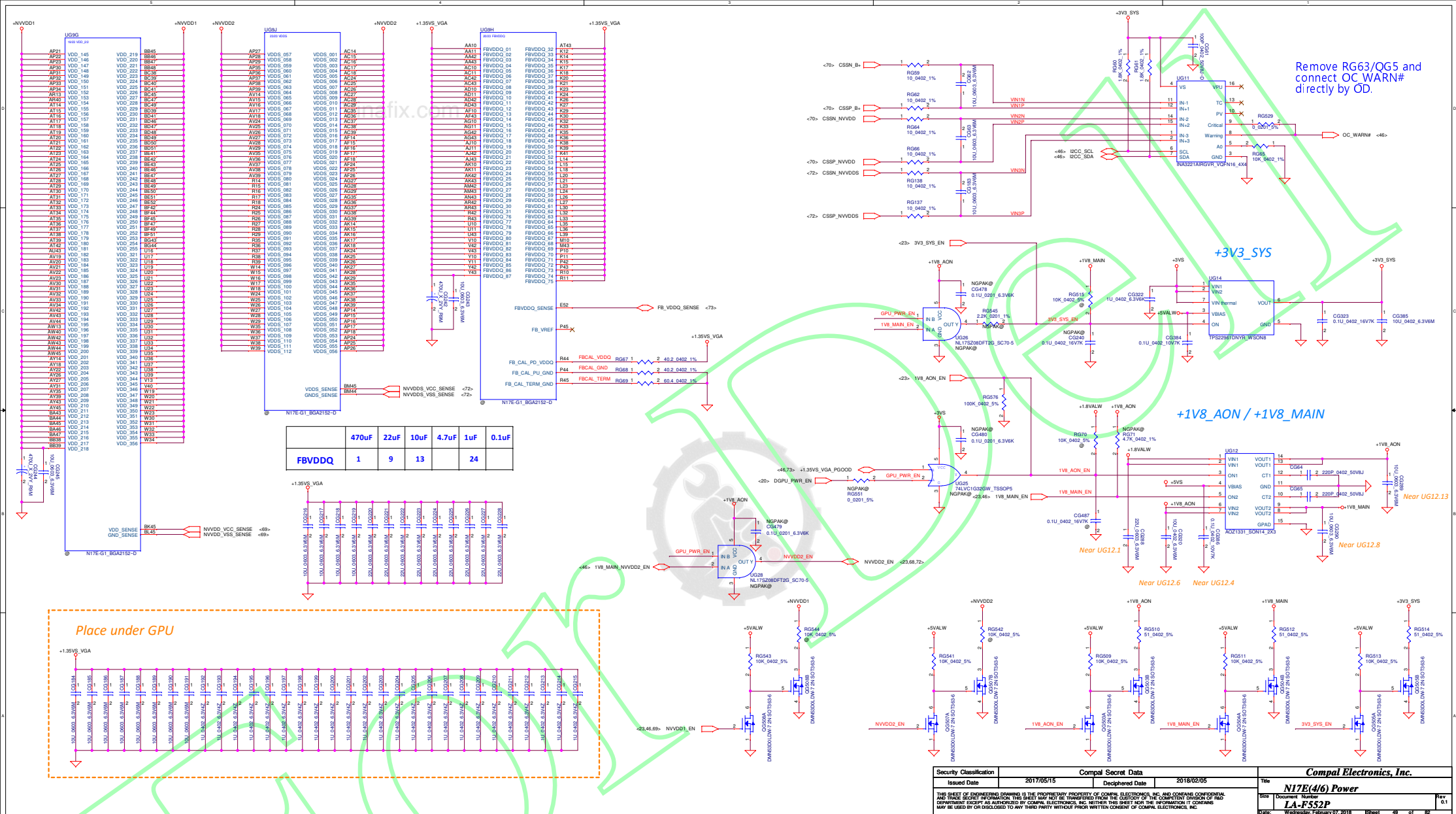
AOS SA00008A800 (SI C AQZ1334 D-01 DF N8P S NGLE L OADS W
APEC SA00006V300 (SI C APE8939 GNB DF N8P L OADS WTCH
E MC SA00008R600 (SI CE M5201V DF NBX3 8P L OADS WTCH



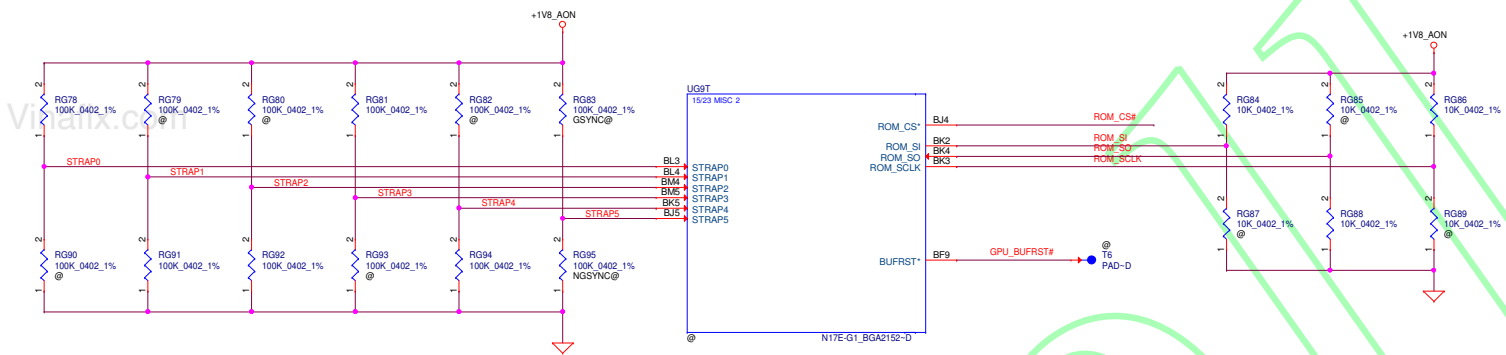




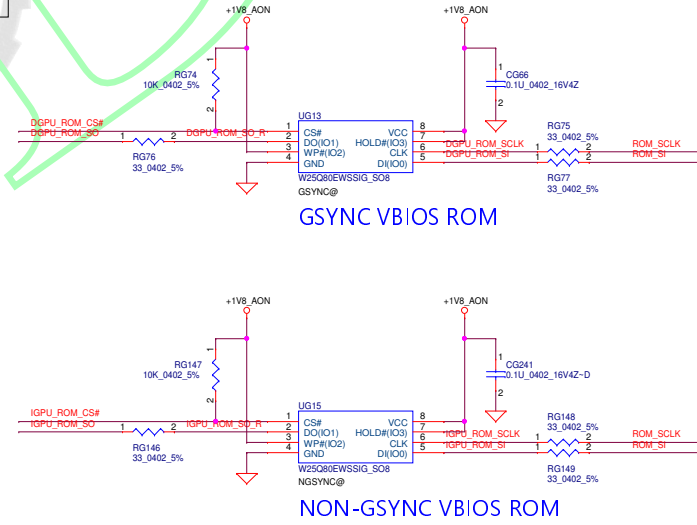
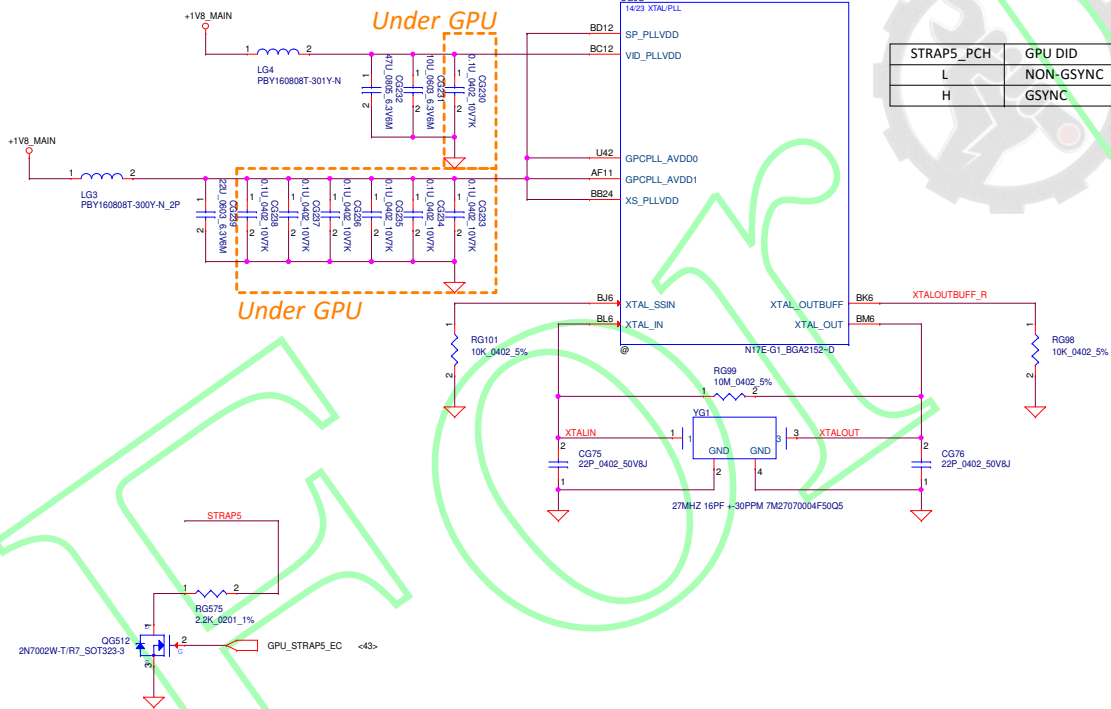
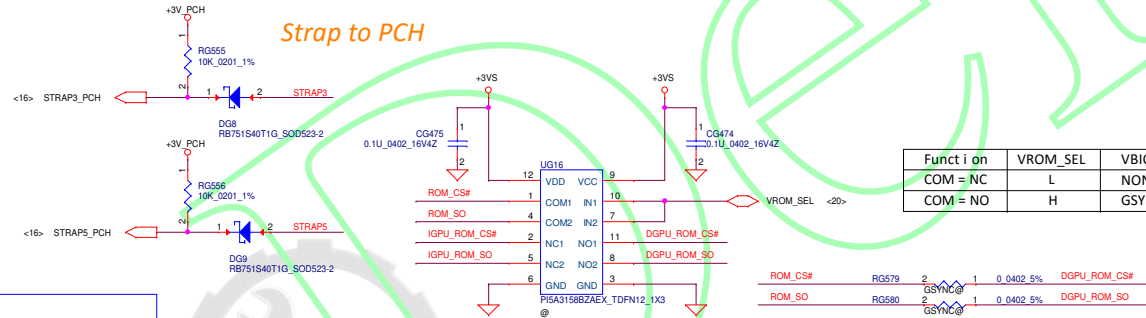
	22uF	10uF	4.7uF	1uF	0.1uF
IFPx_IOVDD			2		4
IFPx_PLLVDD	1				2

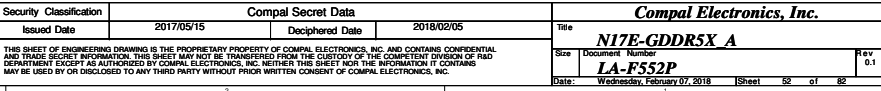


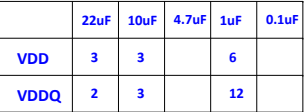
	47uF	22uF	10uF	4.7uF	1uF	0.1uF
VID_PLLVDD	1		1			1
SP_PLLVDD		1				
GPCPLL_AVDD						6



GDDR5x VRAM	Strap0	Strap1	Strap2	Strap3	Strap4	Strap5	RAMCFG
Micron , MT58K256M32JA-100:A	L	L	L	H	L	L	0
Micron , MT58K256M32JA-100:A	H	L	L	H	L	L	1







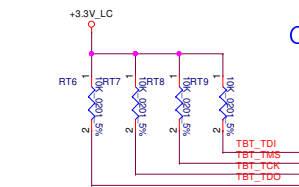
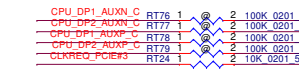
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				Size Document Number		
				LA-F552P		
				Date: Wednesday, February 07, 2018 Sheet 55 of 82		

PEG TX

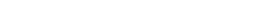
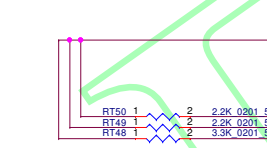
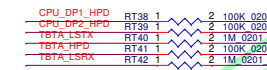
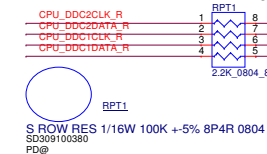
PEG CLK

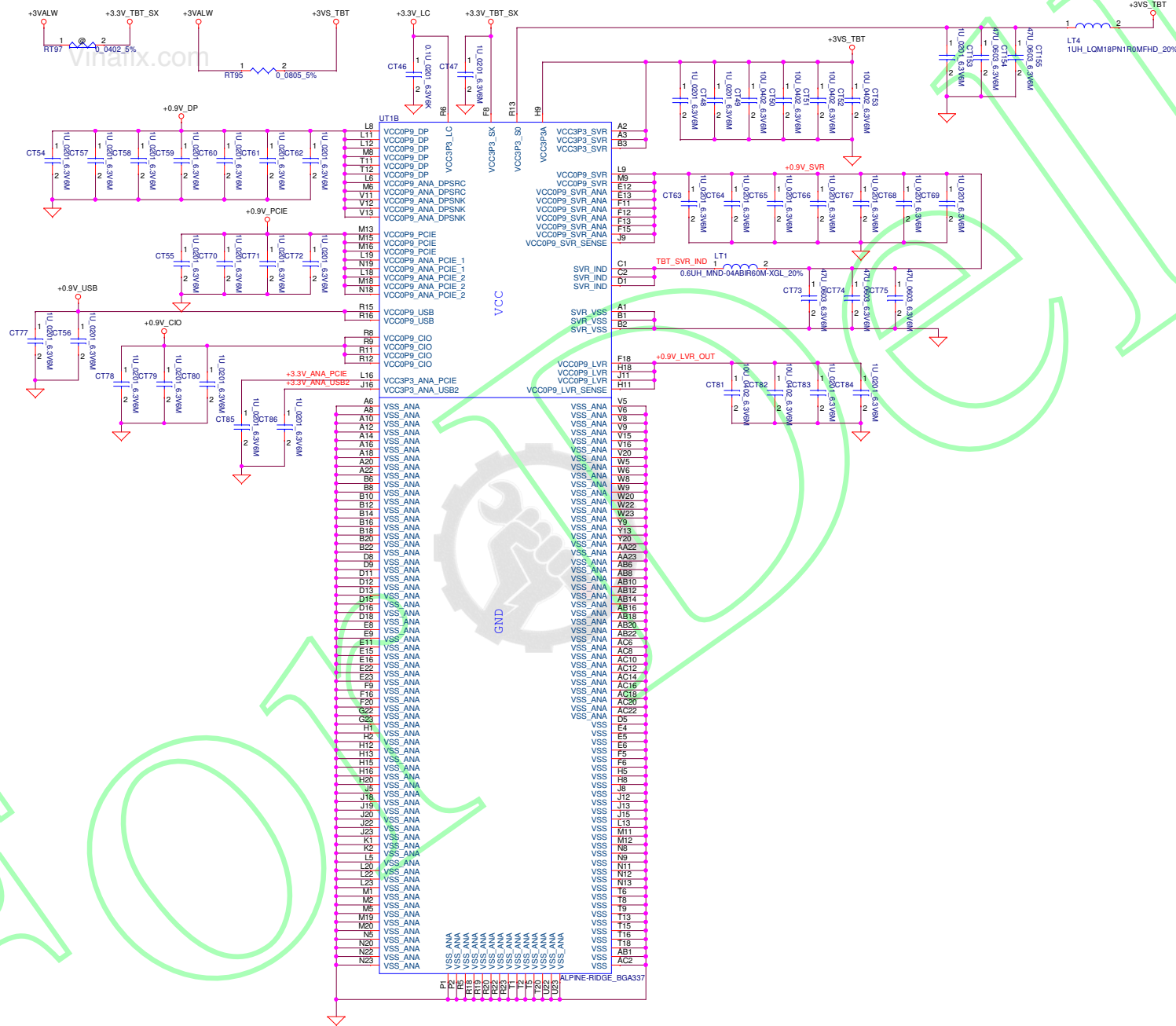
CPU DDI1

CPU DDI2



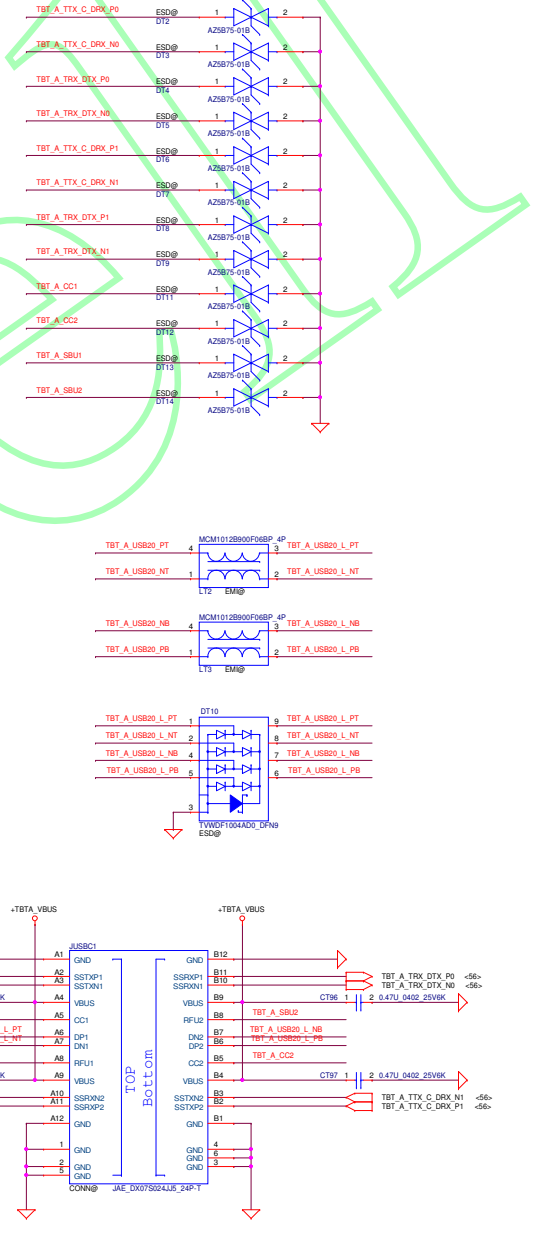
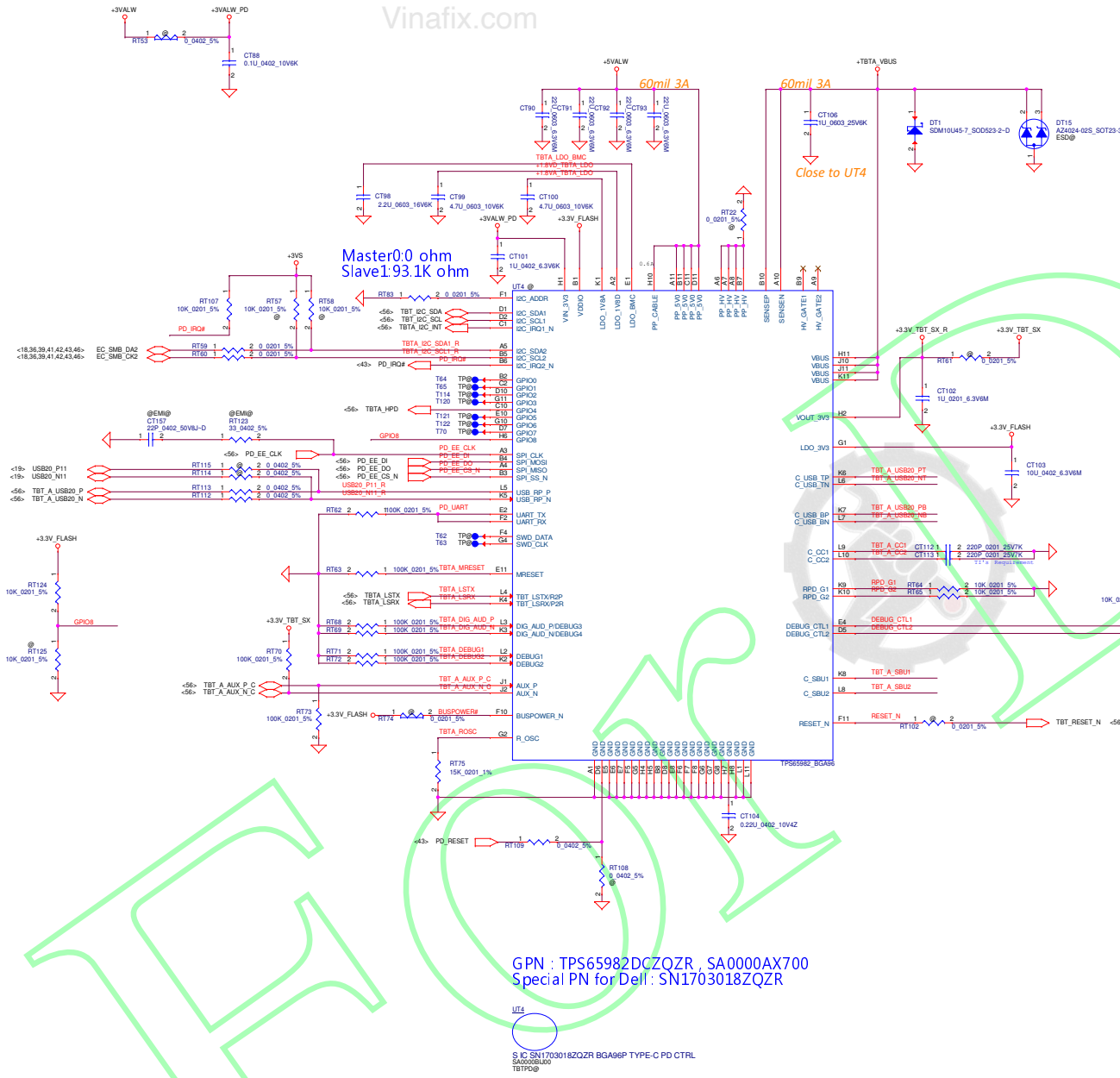
Pull-Up RTP1 is 2.2K ohm
Pull-Down RTP1 is 100K ohm

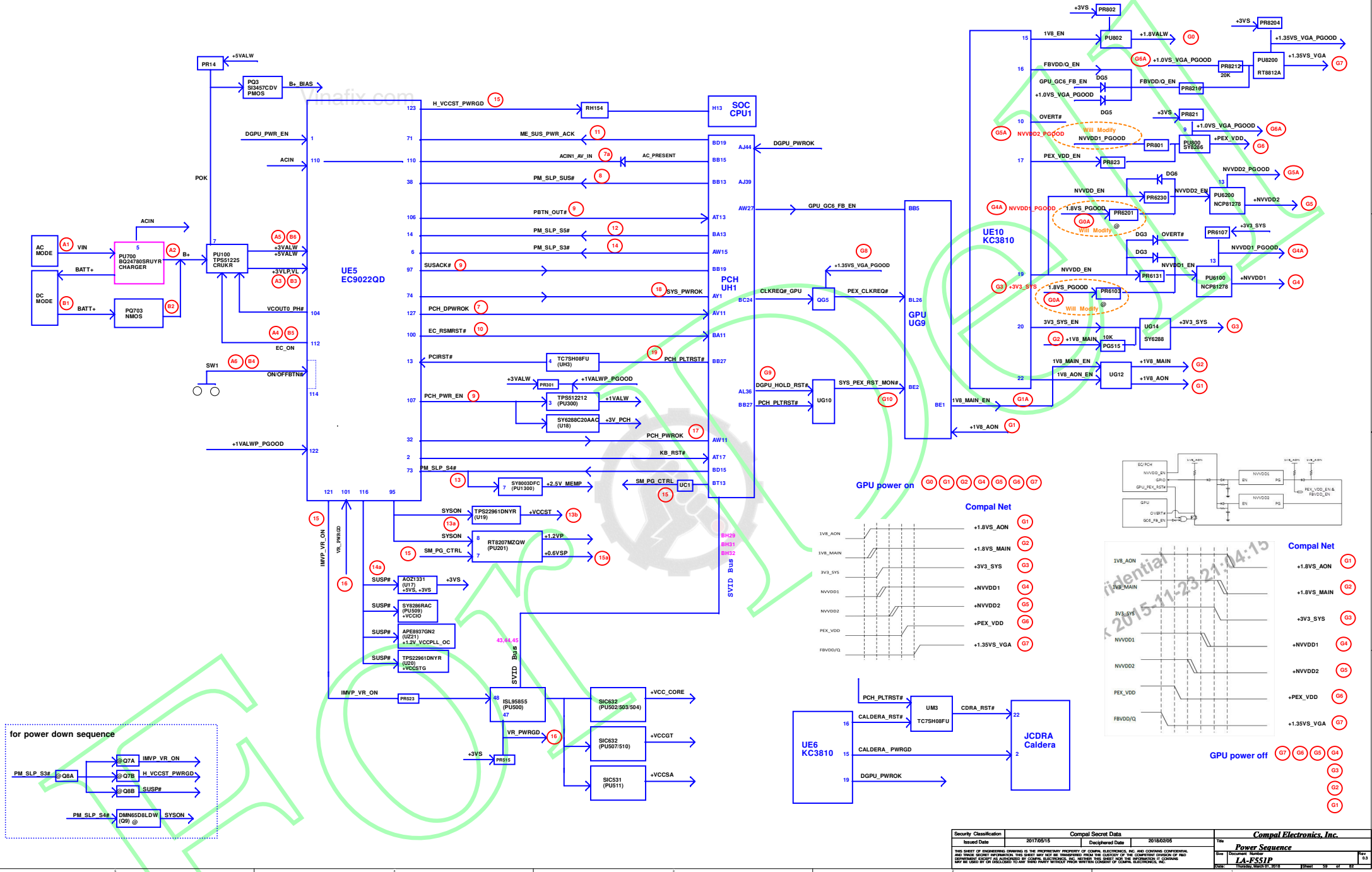


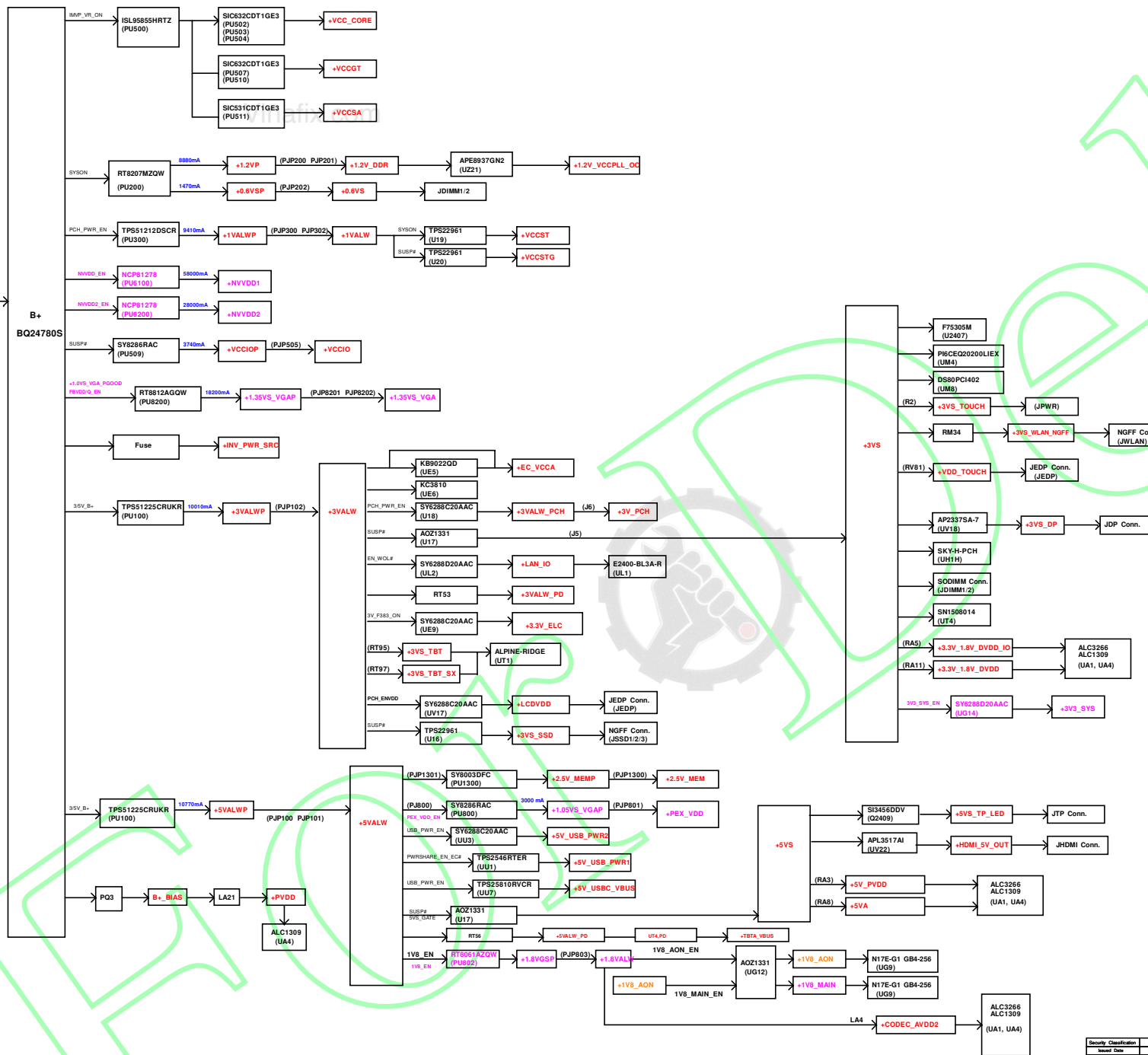
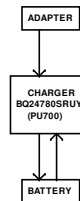


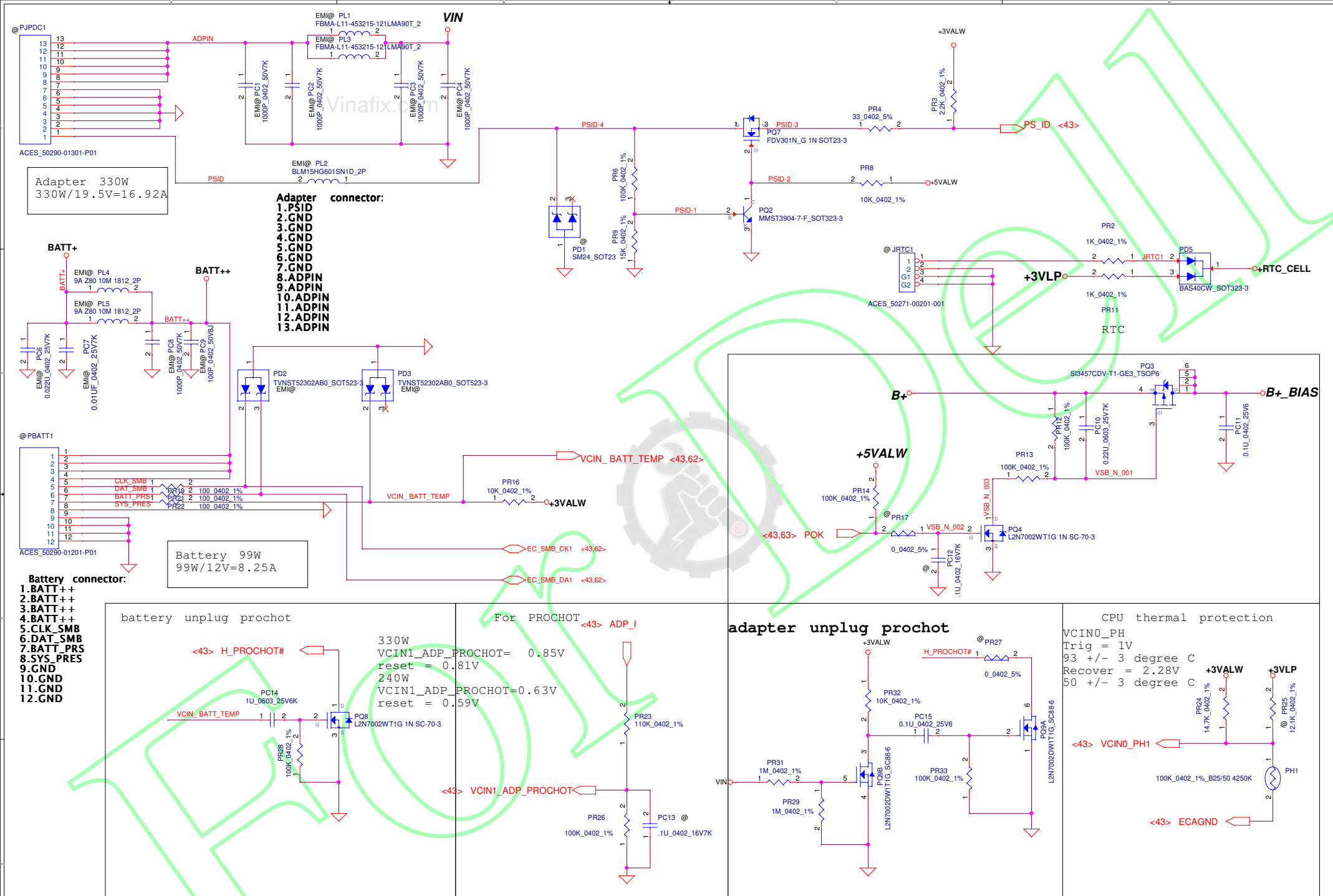
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/05/15	Deciphered Date	2018/02/05	Title	
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				Size	Document Number
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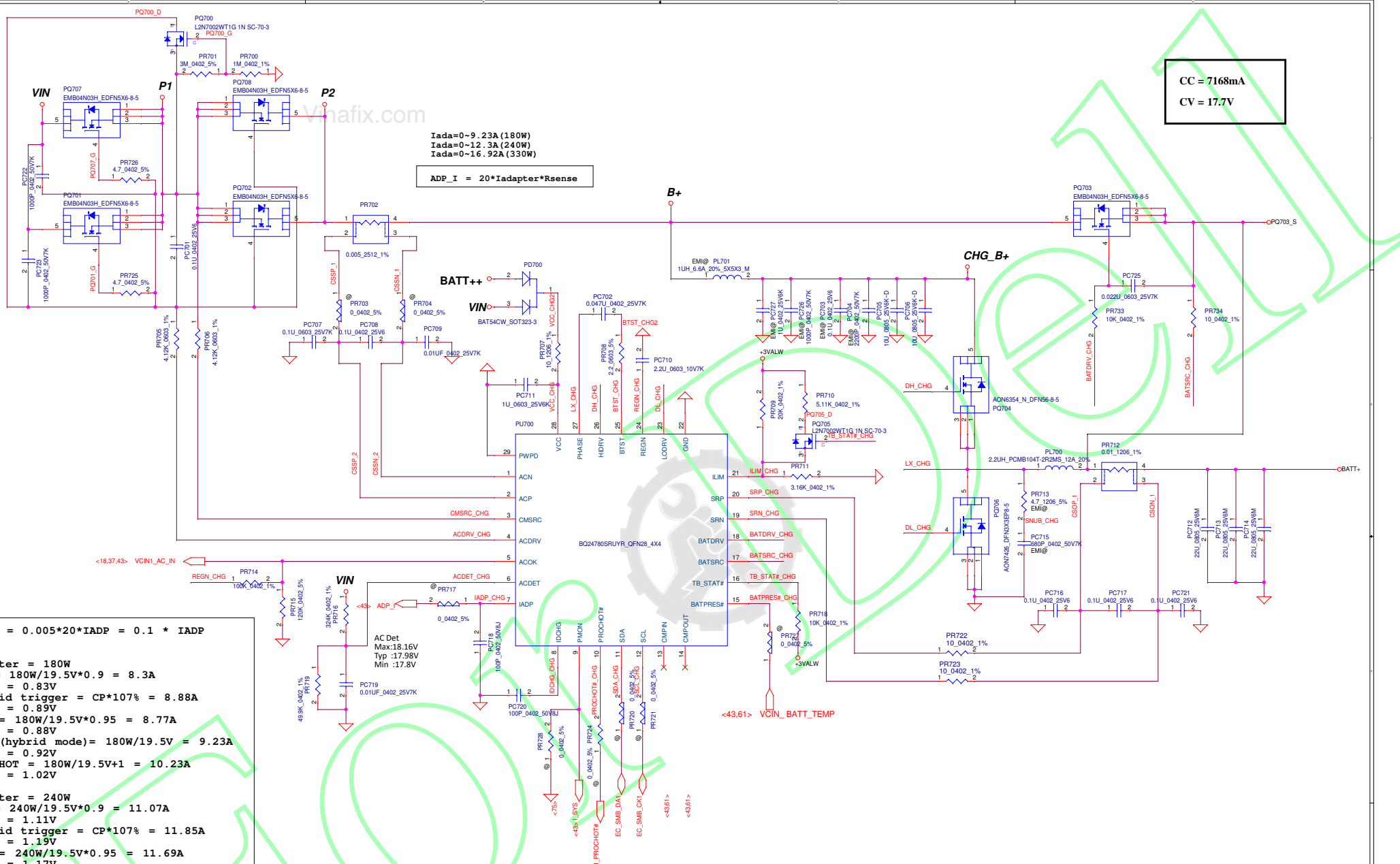
Vinafix.com











CC = 7168mA
CV = 17.7V

I_{ada} = 0~9.23A (180W)
I_{ada} = 0~12.3A (240W)
I_{ada} = 0~16.92A (330W)
ADP_I = 20 * I_{adapter} * R_{sense}

ADPI = 0.005 * 20 * IADP = 0.1 * IADP

Adapter = 180W
CP = 180W/19.5V*0.9 = 8.3A
ADPI = 0.83V
Hybrid trigger = CP*107% = 8.88A
ADPI = 0.89V
IPCC = 180W/19.5V*0.95 = 8.77A
ADPI = 0.88V
IPCC(hybrid mode) = 180W/19.5V = 9.23A
ADPI = 0.92V
PROCHOT = 180W/19.5V+1 = 10.23A
ADPI = 1.02V

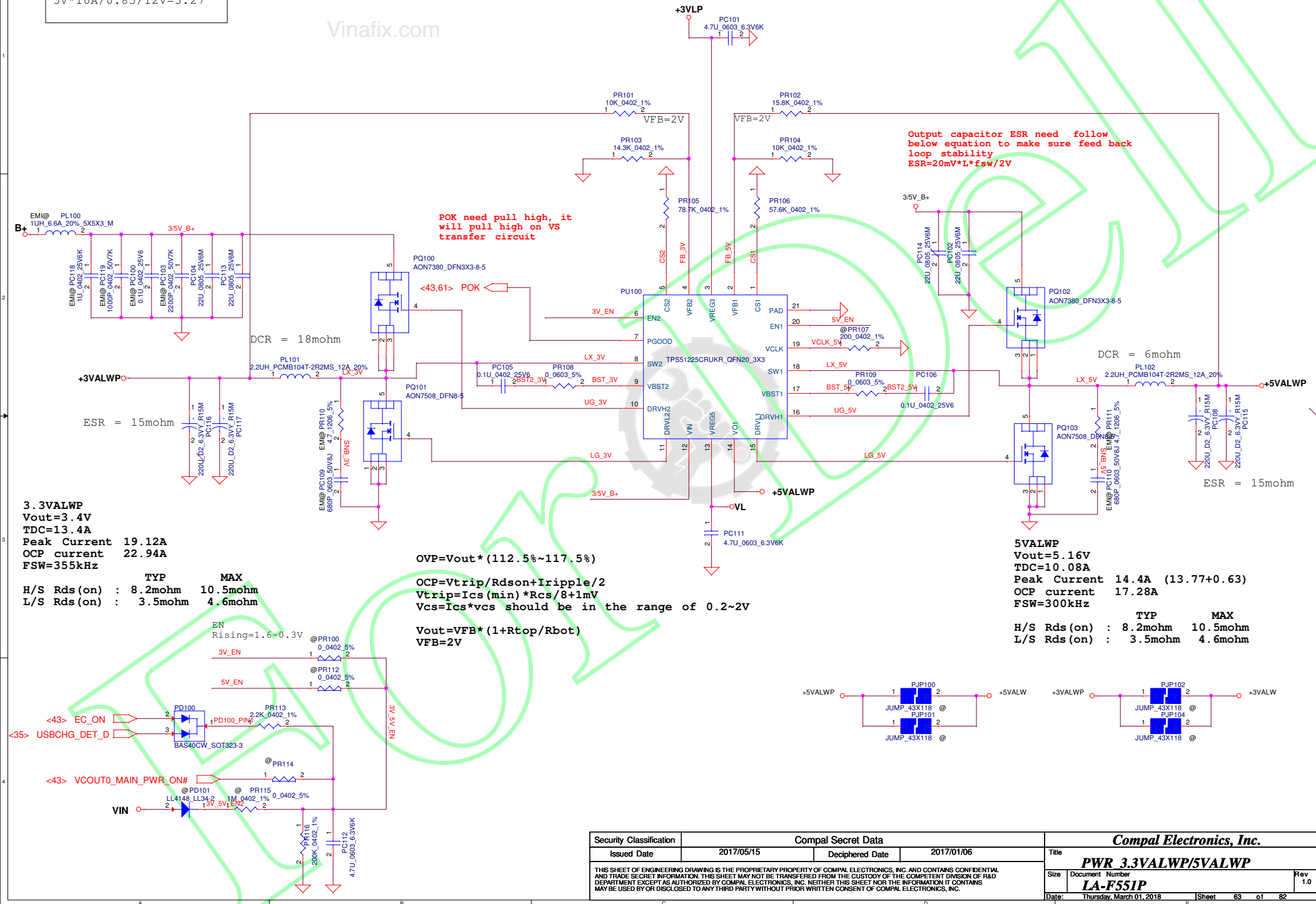
Adapter = 240W
CP = 240W/19.5V*0.9 = 11.07A
ADPI = 1.11V
Hybrid trigger = CP*107% = 11.85A
ADPI = 1.19V
IPCC = 240W/19.5V*0.95 = 11.69A
ADPI = 1.17V
IPCC(hybrid mode) = 240W/19.5V = 12.31A
ADPI = 1.23V
PROCHOT = 240W/19.5V+1 = 13.3A
ADPI = 1.33V

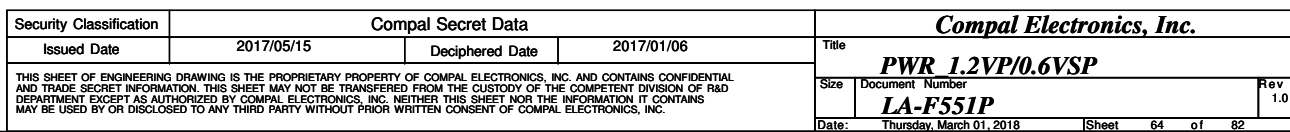
Adapter = 330W
CP = 330W/19.5V*0.9 = 15.23A
ADPI = 1.52V
Hybrid trigger = CP*107% = 16.3A
ADPI = 1.63V
IPCC = 330W/19.5V*(1*0.95) = 16.08A
ADPI = 1.61V
IPCC(hybrid mode) = 330W/19.5V = 16.92A
ADPI = 1.69V
PROCHOT = 330W/19.5V+1 = 17.92A
ADPI = 1.79V

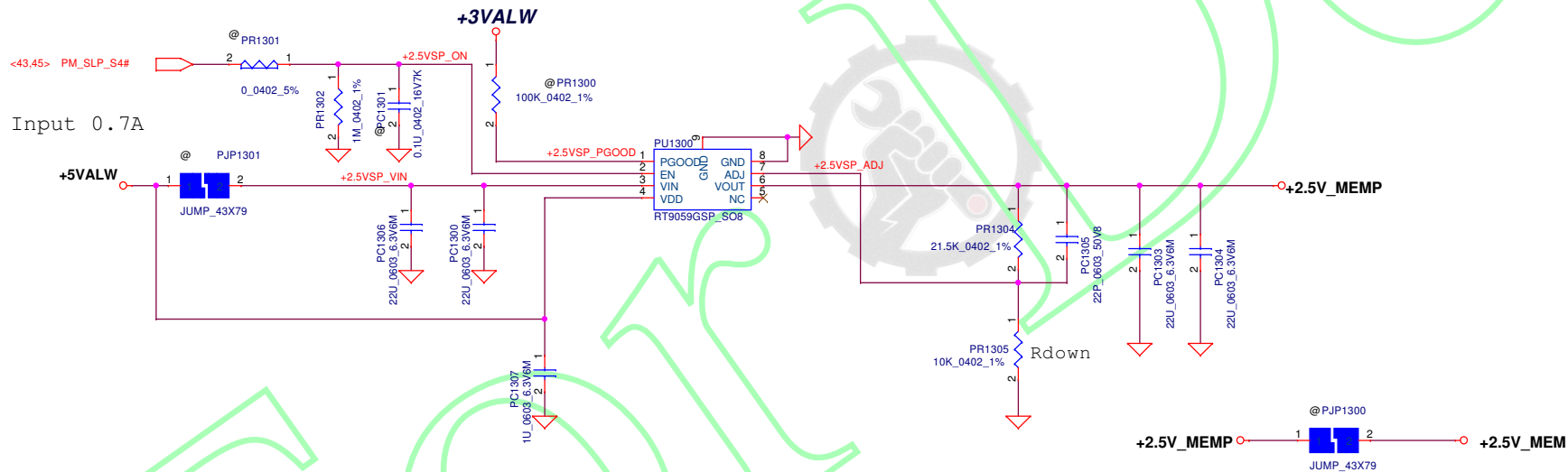
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		PWR CHARGER	
2017/05/15		2017/01/06		LA-F551P	
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Input Current: 7.5A
 $3.3V \cdot 10A / 0.85 / 12V = 2.23$
 $5V \cdot 10A / 0.85 / 12V = 5.27$

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+2.5V_MEM
 TDC 0.63A
 Peak Current 0.9A
 OCP Current 3.5A

$$V_{out} = 0.8V * (1 + R_{up}/R_{down})$$

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Issued Date	2017/05/15	Deciphered Date	2017/01/06	Title	PWR +2.5V MEM
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+1.0VS_VGAP
Vout=1.0V
TDC 2.1A
Peak Current 3.0A
OCF current 6A
FSW=1MHz
Choke DCR TYP MAX
0.045mohm , 0.070mohm

Input 0.7A

+3V3_SYS

PR821
10K_0402_1%

+1.0VS_VGA_PGOOD <46>

PR806
0.0603_5%
PC808
0.1U_0603_25V7K

BS2 1.0VS_VGAP1

BS 1.0VS_VGAP

LX 1.0VS_VGAP

FB 1.0VS_VGAP

VCC 1.0VS_VGAP

SNB 1.0VS_VGAP

EMI@ PR803
7.0603_5%

EMI@ PC802
680P_0402_50V7K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

22U_0402_16V6K

Vout=0.6V* (1+Rup/Rdown)

+1.0VS_VGAP

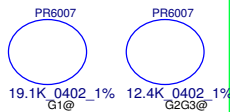
PJP801 @

JUMP_43X79

+PEX_VDD

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OCP setting



Vinafix.com

<https://shop62935598.taobao.com/>

layout 上：
請將 Total DC R sensing 的 component 放靠近 Controller.

NVDD1
TDC 121A
Peak Current 272A
OCP=314A

layout 上：請將 RSEN1~4 放靠近 Controller.

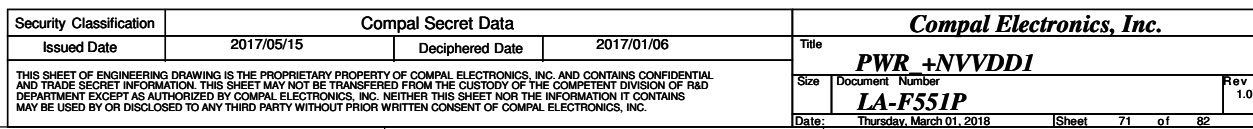
Fsw=300kHz

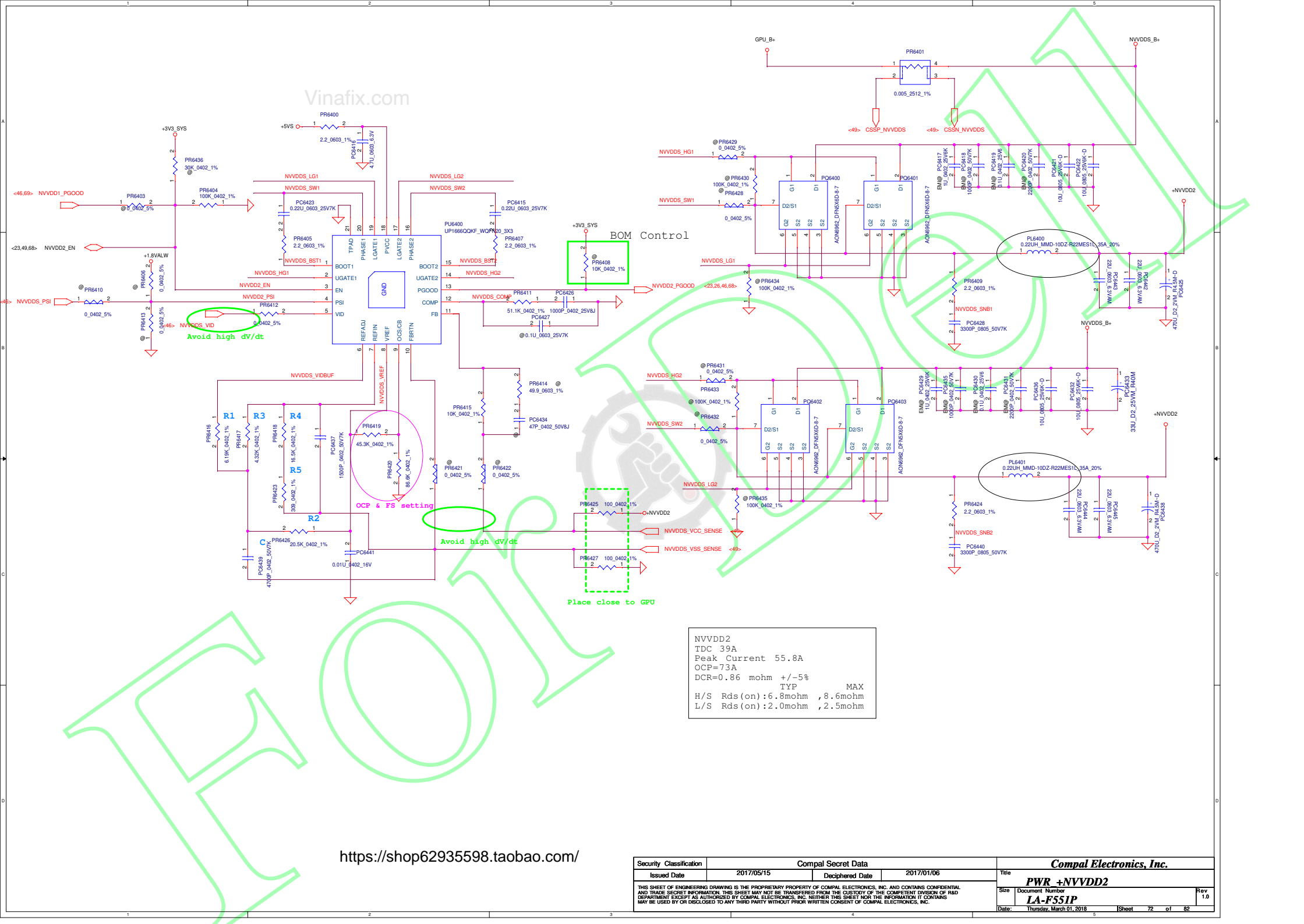
請教 AUD
PHASE 的設定

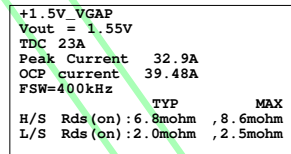
PWMVID 的 RC BOM
請根據 GPU's config
設定

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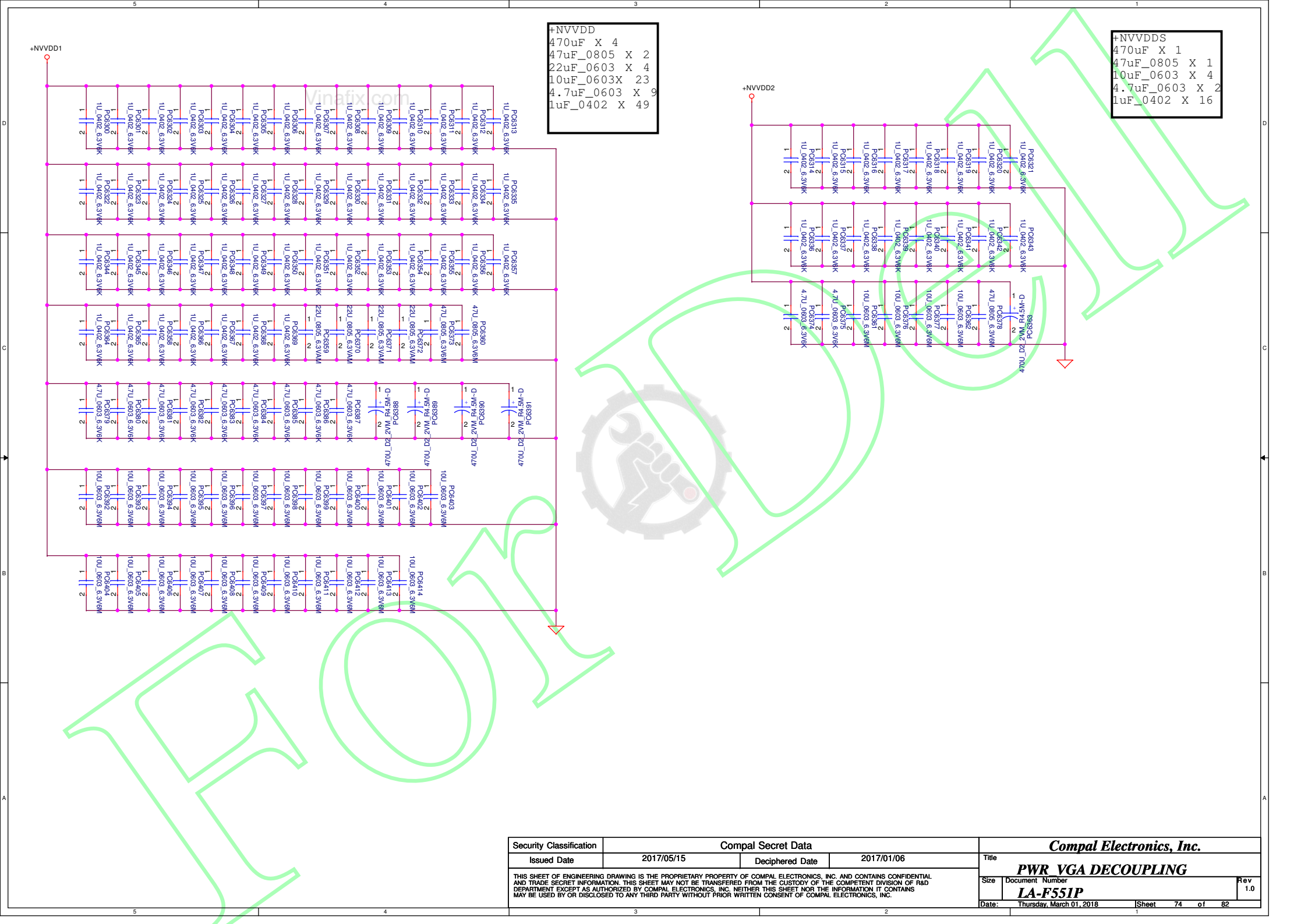
Cold Boot = 4-phase
Warm Boot = 4-phase







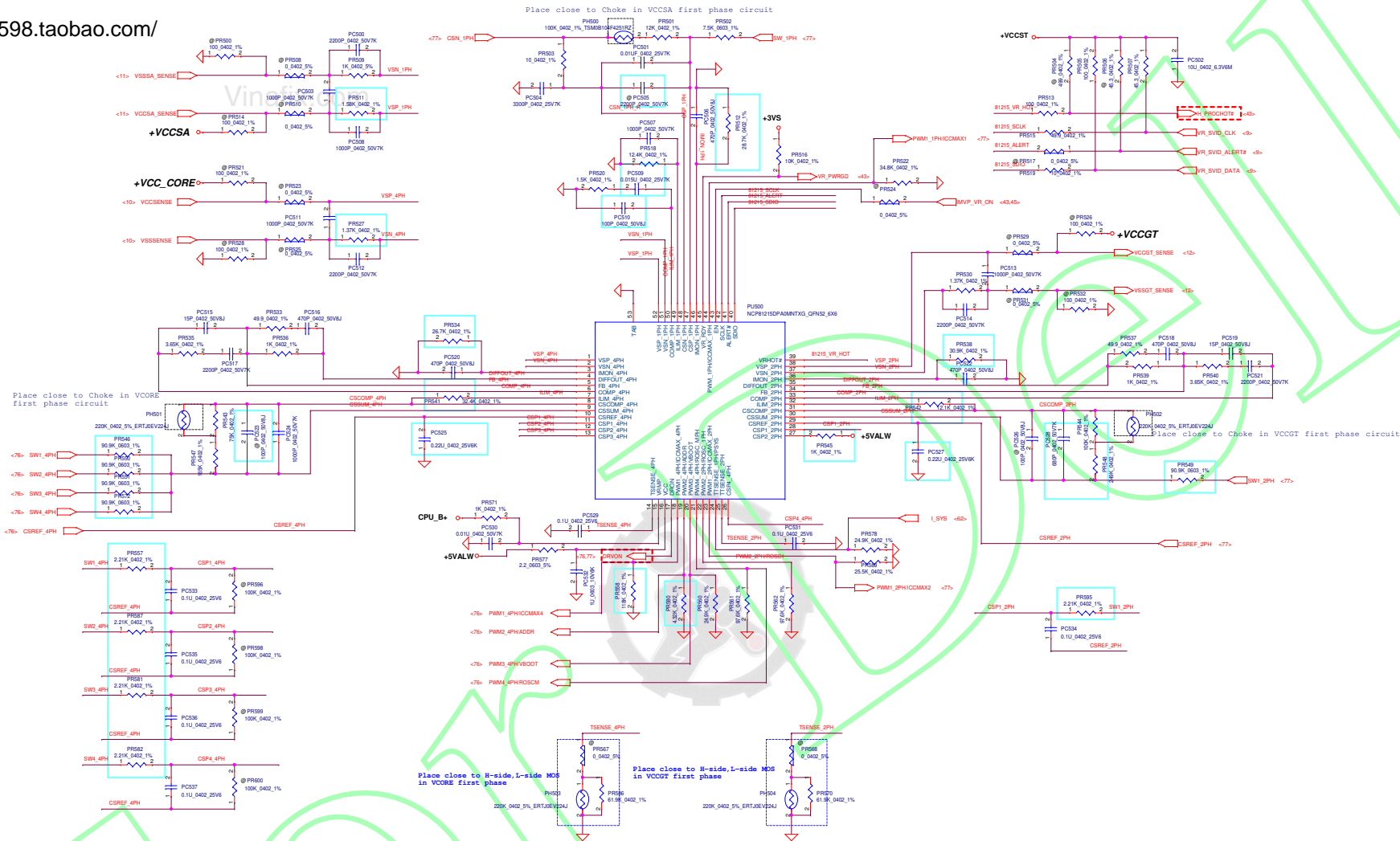
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2017/05/15	Deciphered Date	2017/01/06	Title	PWR +1.55VRAM	
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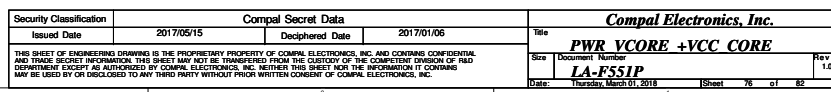
+NVVDD
470uF X 4
47uF_0805 X 2
22uF_0603 X 4
10uF_0603X 23
4.7uF_0603 X 9
1uF_0402 X 49

+NVVDD5
470uF X 1
47uF_0805 X 1
10uF_0603 X 4
4.7uF_0603 X 2
1uF_0402 X 16

Security Classification		Compal Secret Data		Title	
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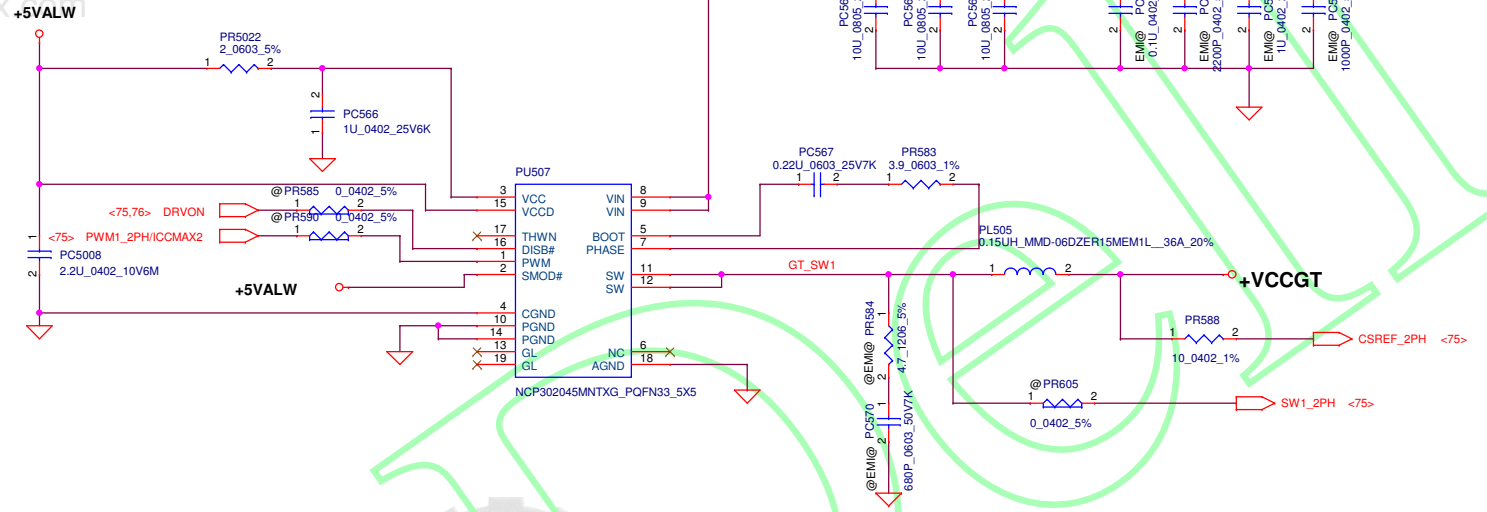


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Issued Date		Deciphered Date		Title PWR Power NCP81215	
2017/05/15		2017/01/06		Doc. Number LA-F551P	
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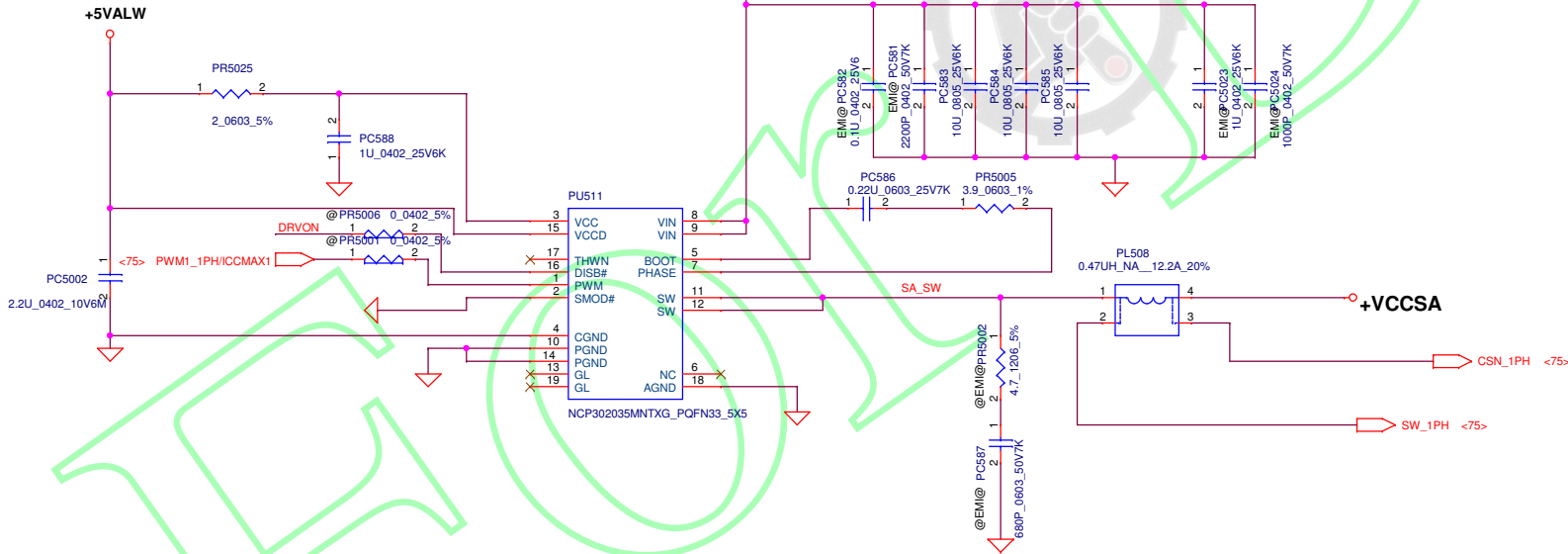
+VCCGT
TDC PL2 :25A
Peak Current 32A
OCP Current 38.4A
DCR 0.67mohm +/-5%
Load Line 2.7mV/A
Fsw=600KHz

Vinafix



CPU_B+

+VCCSA
TDC PL2 :10A
Peak Current 11.1A
OCP Current 17.6A
DCR 6.2mohm +/-5%
Load Line 10.3mV/A
Fsw=600KHz



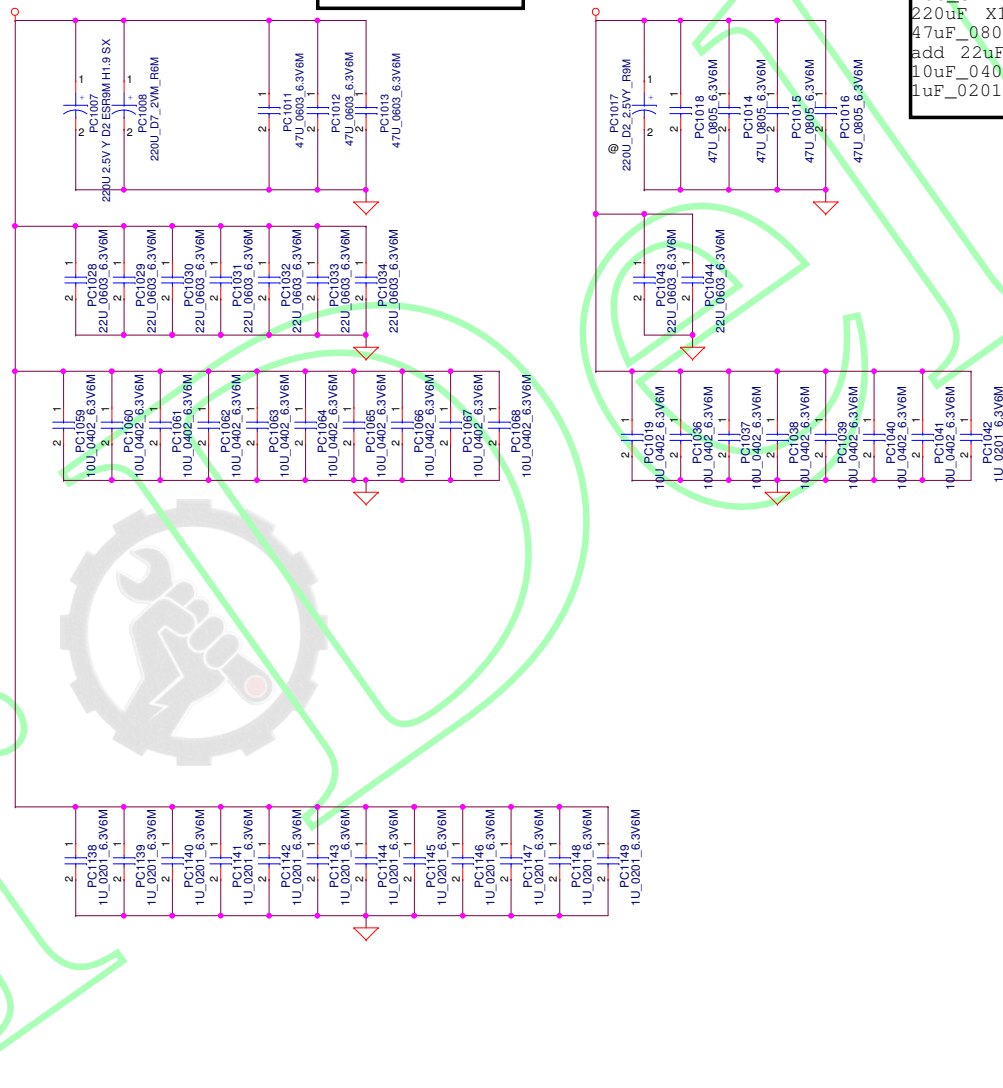
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Issued Date	2017/05/15	Deciphered Date	2017/01/06	Title	
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```
VCC_GT
220uF X4>2
47uF_0805 X 6>3
22uF_0603 X 8>7
10uF_0402 X 35>10
1uF_0201 X 68>12
```

```
VCC_CORE
220uF X3>5
47uF_0805 X 4>5
22uF_0603 X 8>12
10uF_0402 X 28>21
1uF_0201 X 63>48
```

+VCCSA

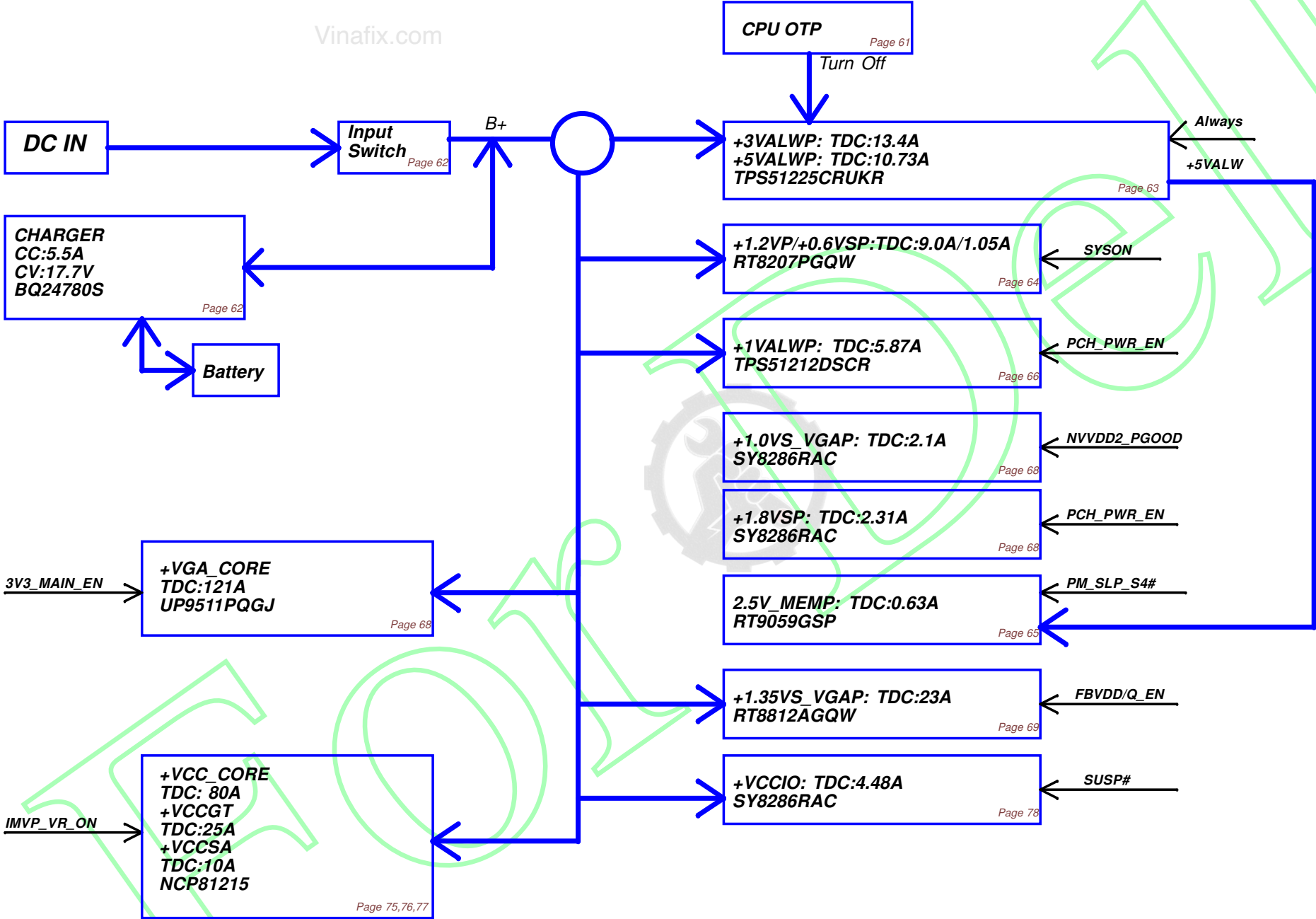
```
VCC_SA
220uF X1>0
47uF_0805 X 1>4
add 22uF_0603 X 2
10uF_0402 X 7
1uF_0201 X 3>1
```



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Power block

Vinafix.com



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1	P.67	PWR_+1.8VSP/ +1.8VSP_AUDIO	2017/08/15	Compal_HW	1.1.8VSP enable signal's sequence have wrong. Cause to PM_SLP_S5# pull low.	1.Change 1.8VSP enable signal change from SUSP# to PCH_PWR_EN. 2.Add enable signal pull high 10k ohm to +3VALW 3.PR807/PR808 un-pop.	0.1
2	P.67	PWR_+1.8VSP/ +1.8VSP_AUDIO	2017/08/15	Compal_HW	1.Need another 1.8V supply to audio codec and usb retimer.	1.Add RT9013 LDO Circuit.	0.1
3	P.66	PWR_+1VALWP	2017/08/15	Compal_HW	1.Modify enable signal RC delay.	1.Change PR300 from 0 ohm to 100K ohm. 2.PC300 0.1uF pop.	0.1
4	P.75	PWR_VCORE_NCP81215	2017/08/17	Compal_PWR	1.PWR and HW side double pull high/down.	1.PR500,PR514,PR521,PR526,PR528,PR531 un-pop.	0.1
5	P.75	PWR_VCORE_NCP81215	2017/08/22	Compal_PWR	1.Modify ICCMAX=150A and OCP=180A.	1.Change PR558 from 100K ohm to 118K ohm. 2.Change PR541 from 27.4K ohm to 32.4K ohm.	0.1
6	P.67	PWR_+1.8VSP/ +1.8VSP_AUDIO	2017/09/04	Compal_HW	1.Modify 1.8VSP enable signal and RC delay time.	1.Delete PR817. 2.Add PR807 100K ohm. 3.Add PC811 0.1uF. 4.Add PR808 1M ohm.	0.1A
7	P.76/77	PWR_VCORE+VCC_CORE/ +VCC_GT	2017/09/11	Compal_ME	1.CPU choke's height are difference with Cassini. VCORE and VCCGT 's choke height change from 3mm to 4mm.	1.Change PL501,PL502,PL503,PL505,PL506 from SH00001DC00 to SH00001EE00.	0.2
8	P.67	PWR_+1.8VSP	2017/09/11	Compal_HW	1.Modify 1.8VS net name.	1.Net name +1.8VS change to +1.8VALW.	0.2
9	P.75	PWR_VCORE_NCP81215	2017/09/14	Compal_PWR	1.Change Choke DCR from 0.9mohm to 0.67mohm (+/-5%).Fine tune FB sense and CSCOMP RC value.	1.Change PR546,PR550,PR551,PR572 from 115K to 90.9K ohm. 2.Change PR557,PR587,PR581,PR582,PR595 from 1.62K to 2.21K ohm. 3.Change PR538 from 25.5K to 28.7K ohm. 4.Change PR549 from 100K to 90.9K ohm. 5.Change PC528 from 560pF to 680pF. 6.PC505,PC523 un-pop. 7.Change PC525,PC527 from 0.1uF to 0.22uF. 8.Change PR527 from 1Kohm to 1.37Kohm. 9.Change PR511 from 1.65Kohm to 1.58Kohm. 10.Change PR512 from 31.6Kohm to 28.7Kohm. 11.Change PC509 from 10nF to 15nF. 12.Change PC510 from 56pF to 100pF. 13.Change PR548 from 261Kohm to 249Kohm.	0.2
10	P.73	PWR_+1.55VRAM	2017/09/13	Compal_PW	1.Modify OCP resistor.	1.Change PR8206 from 8.66K ohm to 7.87K ohm.	0.2
11	P.61	DCIN / BATT CONN / OTP	2017/09/14	Compal_PW	1.Unify mos materials.	1.Change PQ9 from SB000002U00 to SB00000PV00.	0.2
12	P.61/70/71	DCIN / BATT CONN / OTP PWR_+NVVDD1	2017/09/26	Compal_EMI	1.EMI request to modify VIN beed and capcitor.	1.Change PL1,PL3 from SM01000P500 to SM01000DJ00. 2.Change PC2,PC4 from 100pF to 1000pF. 3.Change PC 6100,PC6117,PC6200 from 1uF to 0.1uF. 4.Change PC6104,PC6118,PC6204 from 1000pF to 2200pF.	0.2

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12	P.75	PWR_VCORE_NCP81215	2017/12/14	Compal_PWR	1.NCP81215 change PA0 version P/N.	1.Change PU500 from SA0000AQE00 to SA0000BNK10.	0.3
13	P.61	PWR_DCIN / BATT CONN / OTP	2017/12/14	Compal_PWR	1.Main source SB00000Z500 EOL.	1.Change PQ2 from SB00000Z500 to SB00000Z2R00.	0.3
14	P.76/77	PWR_VCORE_+VCC_CORE	2017/12/14	Compal_PWR	1.Cytec choke SH00001DA00 VRTT fail 2.SA choke change common part include SH000015M00 & SH000015P00.	1.Change PL501,PL502,PL503,PL505,PL506 from SH00001EE00 to SH00001D800. 2.Change PL508 from SH000015M00 to SH00001ED00.	0.3
15	P.64/66/73	PWR_+1.2VP/+0.6VSP PWR_+1VALWP PWR_+1.55VRAM	2017/12/14	Compal_PWR	1.Because of polyme cap non equal substitute, all 220uF H=1.9 polyme cap are unified SGA00009800.	1.Change PC209,PC215,PC306,PC307,PC8207,PC8208 from SGA20221D40 to SGA00009800.	0.3
16	P.75	PWR_VCORE_NCP81215	2017/12/14	Compal_PWR	1.VRTT test for IA & GT main and 2nd Choke to fine tune IMON resistor.	1.Change PR534 from 24.9K to 26.7K. 2.Change PR538 from 28.7K to 30.9K.	0.3
17	P.72/73	PWR_+NVVDD2 PWR_+1.55VRAM	2017/12/14	Compal_PWR	1.Because thermal derating fail,we change capcitor type.	1.Change PC6442,PC6443,PC6444,PC6445 from SE00000M000 to SE00001CA00. 2.Change PC710,PC8200 from SE000006S80 to SE00000GC00.	0.3
18	P.73	PWR_+1.55VRAM	2017/12/18	Compal_PWR	1.Modify OCP resistor setting for main/2nd mos.	1.Change PR8206 from 7.87K to 7.5K.	0.3
19	all	all	2017/02/07	Compal_PWR	1.Change 0 ohm to short-pad.	1.Change PR100,PR112,PR114,PR1301,PR17,PR208,PR211,PR27,PR5001,PR5006,PR5007,PR5017,PR5018,PR508,PR510,PR517,PR523,PR524,PR525,PR529,PR531,PR552,PR556,PR563,PR566,PR567,PR568,PR573,PR576,PR585,PR590,PR591,PR594,PR6005,PR6015,PR6016,PR6018,PR6019,PR6021,PR6025,PR6031,PR6039,PR6044,PR6060,PR6107,PR6114,PR6205,PR6410,PR6421,PR6422,PR6428,PR6429,PR6431,PR6432,PR703,PR704,PR717,PR720,PR721,PR727,PR813,PR815,PR8216,PR8219,PR9000 from 0 ohm to short-pad.	0.3
20	P.68	P68-PWR_+1.0VS_VGA	2017/02/07	Compal_PWR	1.Bom control for 2nd GPU sequence IC.	1.PR801 0 ohm un-pop.	0.3

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